Data Book

Power Transistor Products

1990

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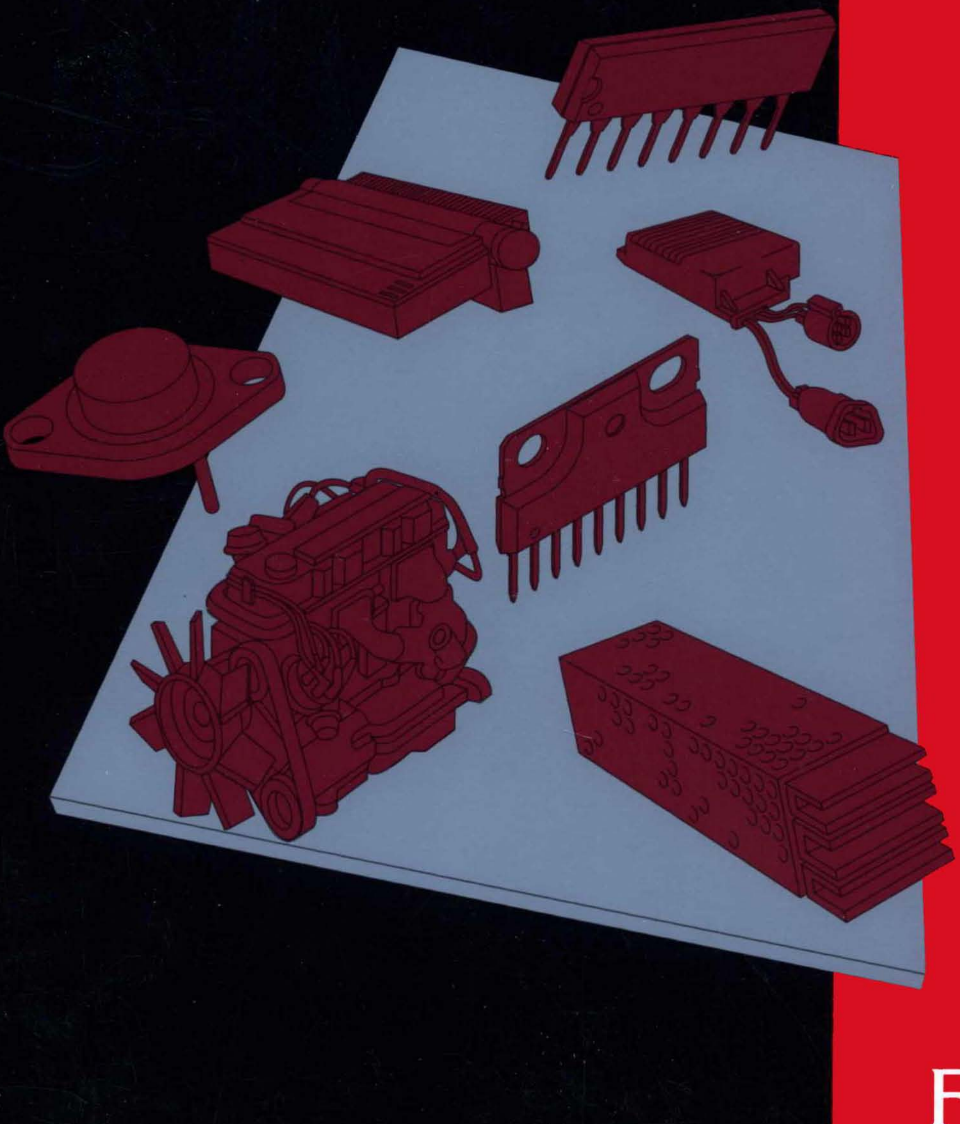

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Power Transistor Products

1990
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Circuit diagrams using Fujitsu products are included to illustrate typical semiconductor applications. Information sufficient for construction purposes may not be shown.

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Fujitsu's Power Transistor Products

Introduction

Fujitsu manufactures a wide range of power actuators that include: ring emitter transistors, darlington transistor arrays and field effect transistor arrays.

The Power Transistor Product line offers devices for use in applications that provide the designer with a complete solution to the implementation of control systems, when combined with Fujitsu's broad line of integrated circuit technologies.

Ring Emitter Transistors (RET)

RET devices offer significant improvement over conventional power transistors due to their high speed switching characteristics and large safe operating area. A typical RET consists of several hundred multiple ring-emitters connected to a common emitter electrode through diffused ballast resistors. The RET structure is a superior transistor for motor control and switch mode converter applications.

Darlington Transistor Arrays

These devices are ideally suited for todays multiple output applications. Features include: large DC current gain and large collector power dissipation. A fast recovery diode to absorb flyback voltage is included, and fast switching speed is also provided This array is well suited for motor drive applications and terminal equipment where IC outputs must be boosted to drive print hammers or solenoids.

Field Effect Transistor Arrays (FET)

FET arrays are faster easier to drive and in motor control or switching power supply applications result in significant parts-count reductions and higher overall efficiency. Telecommunication applications require impedance to be strictly controlled in signal line interfaces; FET arrays offer this control in solid state switching while providing more reliability than traditional reed arrays.

Section 1

Ring Emitter Transistors — *At a Glance*

Page	Device	Case (ns)	Polarity	Maximum Ratings V_{CEO} (V)	I_C (A)
1–3	2SA1041	JEDEC TO–3	PNP	–120	–15
	2SA1042		PNP	–70	–15
	2SC2431		NPN	120	15
	2SC2432		NPN	70	15
1–7	2SA1043	JEDEC TO–3	PNP	–120	–30
	2SA1044		PNP	–70	–30
	2SC2433		NPN	120	30
	2SC2434		NPN	70	30
1–11	2SA1072	JEDEC TO–3	PNP	120	12
	2SA1072A	JEDEC TO–3	PNP	150	12
	2SA1073		PNP	160	12
1–13	2SA1077	JEDEC TO–220	PNP	120	10
1–15	2SA1078	JEDEC TO–220	PNP	120	2
1–17	2SA1080	JEDEC TO–220	PNP	40	0.5
1–19	2SC2428	JEDEC TO–3	NPN	180	12
1–21	2SC2522	JEDEC TO–3	NPN	120	12
	2SC2522A	JEDEC TO–3	NPN	150	12
	2SC2523		NPN	160	12
1–23	2SC2525	RM–60	NPN	120	12
	2SC2526		NPN	160	12
1–25	2SC2527	JEDEC TO–220	NPN	120	10
1–27	2SC2528	JEDEC TO–220	NPN	120	2
1–29	2SC2530	JEDEC TO–220	NPN	40	0.5
1–31	2SC2429	JEDEC TO–3	NPN	400	15
	2SC2429A		NPN	450	15
	2SC2920		NPN	400	15
	2SC2964		NPN	400	15
	2SC2965		NPN	450	15
1–45	2SC3044	JEDEC TO–3	NPN	400	6
	2SC3044A		NPN	450	6
1–51	2SC3045	JEDEC TO–3	NPN	400	10
1–57	2SC3046	JEDEC TO–3	NPN	450	10
1–63	2SC3055	JEDEC TO–220	NPN	400	2
1–69	2SC3056	JEDEC TO–220	NPN	400	6
	2SC3056A		NPN	400	6
1–75	2SC3057	JEDEC TO–220	NPN	400	10
1–81	2SC3058	JEDEC TO–3	NPN	400	30
1–87	2SC3058A	JEDEC TO–3	NPN	450	30

Ring Emitter Transistors — *At a Glance (Continued)*

Page	Device	Case (ns)	Polarity	Maximum Ratings V_{CEO} (V)	I_C (A)
1–93	2SC3059	JEDEC TO–3	NPN	850	2
	2SC3060		NPN	850	5
	2SC3061		NPN	850	10
	2SC3178		NPN	850	2
1–113	FT1551	JEDEC TO–66	NPN	120	2
1–115	FT2551	JEDEC TO–66	PNP	120	2

January 1990
Edition 1.1

2SA1041, 2SA1042, 2SC2431, 2SC2432

Silicon High Speed Power Transistor

DESCRIPTION

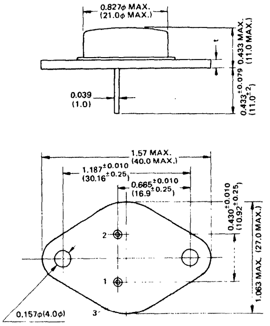
This series are silicon PNP/NPN planer general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

This series are especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

Features

	2SA1041, 2SA1042	2SC2431, 2SC2432
★ f_T :	60MHz (typ.)	80MHz (typ.)
★ t_r :	0.15 μs (typ.)	0.20 μs (typ.)
★ t_s :	0.24 μs (typ.)	0.70 μs (typ.)
★ t_f :	0.08 μs (typ.)	0.12 μs (typ.)
★ Excellent Safe Operating Area:		2SA1041–2SC2431
★ Complements:		2SA1042–2SC2432

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Value		Unit
		2SA1041	2SA1042	2SC2431	2SC2432	
Collector to Base Voltage	V_{CBO}	-120	-70	120	70	V
Emitter to Base Voltage	V_{EBO}	-5	-5	5	5	V
Collector to Emitter Voltage	V_{CEO}	-120	-70	120	70	V
Collector Current	I_C	-15	-15	15	15	A
Base Current	I_B	-5	-5	5	5	A
Collector Power Dissipation (T_C = 25°C)	P_C	100	100	100	100	W
Junction Temperature	T_j	+175		+175		°C
Storage Temperature Range	T_{stg}	-65 ~ +175		-65 ~ +175		°C

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ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

2SA1041, 2SA1042

Parameter	Symbol	Test Conditions	Limits						Unit
			2SA1041			2SA1042			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	$V_{CB} = -120V$, $I_E = 0$	–	-50	–	–	–	–	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = -70V$, $I_E = 0$	–	–	–	–	–	-50	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -4V$, $I_C = 0$	–	–	-50	–	–	-50	μA
Collector Cutoff Current	I_{CEO}	$V_{CE} = -120V$, $I_B = 0$	–	–	-1	–	–	–	mA
Collector Cutoff Current	I_{CEO}	$V_{CE} = -70V$, $I_B = 0$	–	–	–	–	–	-1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -50\mu A$, $I_E = 0$	-120	–	–	-70	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -1mA$, $I_C = 0$	-5	–	–	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10mA$, $R_{BE} = \infty$	-120	–	–	-70	–	–	V
DC Current Gain	h_{FE1}	$V_{CE} = -5V$, $I_C = -1.5A$ *	35	–	200	35	–	200	–
DC Current Gain	h_{FE2}	$V_{CE} = -5V$, $I_C = -15A$ *	7	–	–	10	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -7A$, $I_B = -0.7A$ *	–	-0.6	-1.5	–	-0.6	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.2	-1.8	–	-1.2	-1.8	V
Gain-Bandwidth Product	f_T	$V_{CE} = -10V$, $I_C = -1A$	–	60	–	–	60	–	MHz
Output Capacitance	C_{ob}	$V_{CB} = -10V$, $I_E = 0$, $f = 1MHz$	–	350	–	–	350	–	pF
Rise Time	t_r	$I_C = -7.5A$, $R_L = 4\Omega$ $I_{B1} = -I_{B2} = -0.75A$	–	0.15	0.8	–	0.15	0.8	μs
Storage Time	t_{stg}		–	0.24	1.0	–	0.24	1.0	μs
Fall Time	t_f		–	0.08	0.8	–	0.08	0.8	μs

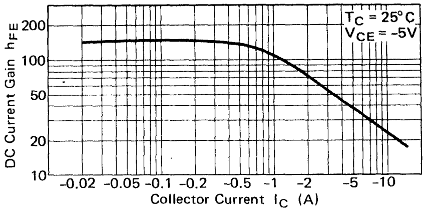
2SC2431, 2SC2432

Parameter	Symbol	Test Conditions	Limits						Unit
			2SC2431			2SC2432			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	$V_{CB} = 120V$, $I_E = 0$	–	–	50	–	–	–	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 70V$, $I_E = 0$	–	–	–	–	–	50	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 4V$, $I_C = 0$	–	–	50	–	–	50	μA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 120V$, $I_B = 0$	–	–	1	–	–	–	mA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 70A$, $I_B = 0$	–	–	–	–	–	1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 50\mu A$, $I_E = 0$	120	–	–	70	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	5	–	–	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10mA$, $R_{BE} = \infty$	120	–	–	70	–	–	V
DC Current Gain	h_{FE1}	$V_{CE} = 5V$, $I_C = 1.5A$ *	35	–	200	35	–	200	–
DC Current Gain	h_{FE2}	$V_{CE} = 5V$, $I_C = 15A$ *	7	–	–	10	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 7A$, $I_B = 0.7A$ *	–	0.4	1.5	–	0.4	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.8	–	1.2	1.8	V
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–	80	–	–	80	–	MHz
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	200	–	–	200	–	pF
Rise Time	t_r	$I_C = 7.5A$, $R_L = 4\Omega$ $I_{B1} = -I_{B2} = 0.75A$	–	0.20	0.8	–	0.20	0.8	μs
Storage Time	t_{stg}		–	0.70	1.0	–	0.70	1.0	μs
Fall Time	t_f		–	0.12	0.8	–	0.12	0.8	μs

* Pulsed $P_W \leq 300\mu$, Duty Ratio $\leq 6\%$

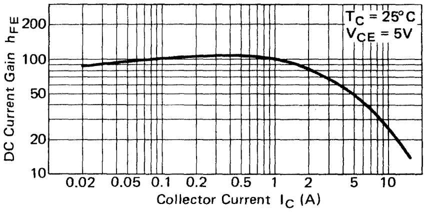
2SA1041, 2SA1042

DC CURRENT GAIN

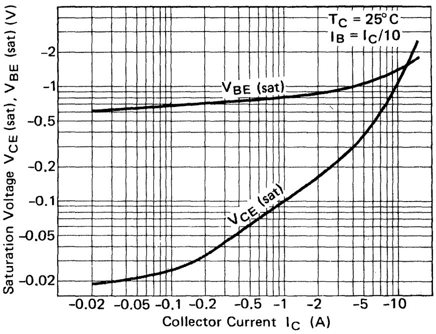


2SC2431, 2SC2432

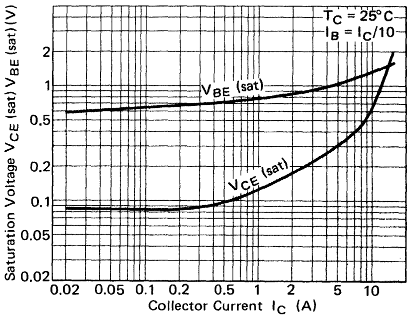
DC CURRENT GAIN



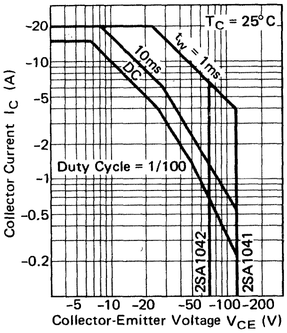
SATURATION VOLTAGE



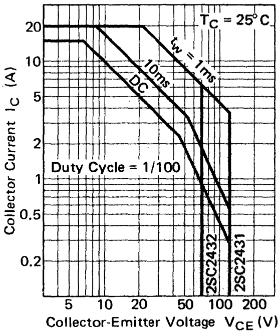
SATURATION VOLTAGE



SAFE OPERATING AREAS

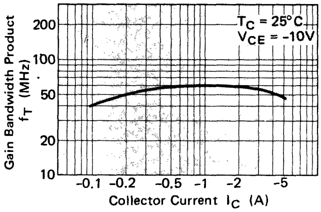


SAFE OPERATING AREAS

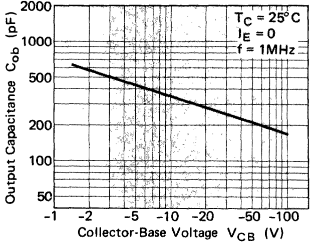


2SA1041, 2SA1042

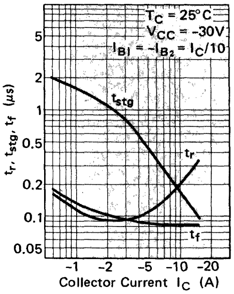
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE

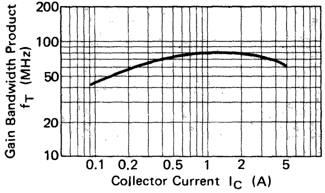


SWITCHING TIME

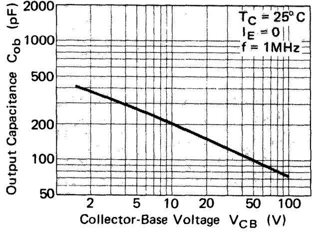


2SC2431, 2SC2432

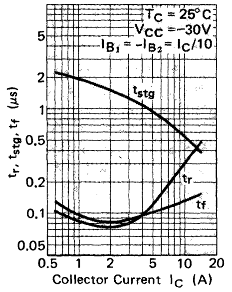
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



SWITCHING TIME



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FUJITSU

PRODUCT PROFILE

2SA1043, 2SA1044, 2SC2433, 2SC2434

Silicon High Speed Power Transistor

DESCRIPTION

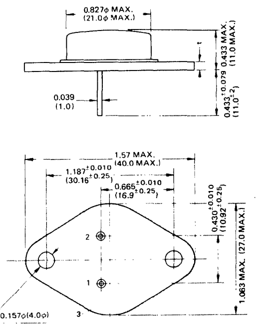
This series are silicon PNP/NPN planer general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

This series are especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

Features

	2SA1043, 2SA1044	2SC2433, 2SC2434
★ f_T :	60MHz (typ.)	80MHz (typ.)
★ t_r :	0.20 μs (typ.)	0.28 μs (typ.)
★ t_s :	0.24 μs (typ.)	0.70 μs (typ.)
★ t_f :	0.08 μs (typ.)	0.15 μs (typ.)
★ Excellent Safe Operating Area:		2SA1043–2SC2433
★ Complements:		2SA1044–2SC2434

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Value		Unit
		2SA1043	2SA1044	2SC2433	2SC2434	
Collector to Base Voltage	V_{CBO}	-120	-70	120	70	V
Emitter to Base Voltage	V_{EBO}	-5	-5	5	5	V
Collector to Emitter Voltage	V_{CEO}	-120	-70	120	70	V
Collector Current	I_C	-30	-30	30	30	A
Base Current	I_B	-10	-10	10	10	A
Collector Power Dissipation (T_C = 25°C)	P_C	150	150	150	150	W
Junction Temperature	T_j	+175		+175		°C
Storage Temperature Range	T_{stg}	-65 ~ +175		-65 ~ +175		°C

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ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

2SA1043, 2SA1044

Parameter	Symbol	Test Conditions	Limits						Unit
			2SA1043			2SA1044			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	$V_{CB} = -120V$, $I_E = 0$	–	–	-50	–	–	–	-50
Collector Cutoff Current	I_{CBO}	$V_{CB} = -70V$, $I_E = 0$	–	–	–	–	–	-50	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -4V$, $I_C = 0$	–	–	-50	–	–	-50	μA
Collector Cutoff Current	I_{CEO}	$V_{CE} = -120V$, $I_B = 0$	–	–	-1	–	–	–	mA
Collector Cutoff Current	I_{CEO}	$V_{CE} = -70V$, $I_B = 0$	–	–	–	–	–	-1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -50\,\mu A$, $I_E = 0$	-120	–	–	-70	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -1mA$, $I_C = 0$	-5	–	–	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10mA$, $R_{BE} = \infty\Omega$	-120	–	–	-70	–	–	V
DC Current Gain	h_{FE1}	$V_{CE} = -5V$, $I_C = -3A$ *	35	–	200	35	–	200	–
DC Current Gain	h_{FE2}	$V_{CE} = -5V$, $I_C = -30A$ *	7	–	–	10	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -15A$, $I_B = -1.5A$*	–	-0.7	-1.5	–	-0.5	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.2	-2.0	–	-1.1	-2.0	V
Gain-Bandwidth Product	f_T	$V_{CE} = -10V$, $I_C = -2A$	–	60	–	–	60	–	MHz
Output Capacitance	C_{ob}	$V_{CB} = -10V$, $I_E = 0$, $f = 1MHz$	–	600	–	–	700	–	pF
Rise Time	t_r	$I_C = -15A$, $R_L = 2\Omega$ $I_{B1} = -I_{B2} = -1.5A$	–	0.20	0.8	–	0.20	0.8	μs
Storage Time	t_{stg}		–	0.24	1.0	–	0.24	1.0	μs
Fall Time	t_f		–	0.08	0.8	–	0.08	0.8	μs

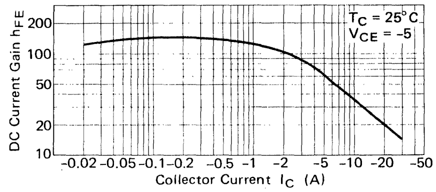
2SC2433, 2SC2434

Parameter	Symbol	Test Conditions	Limits						Unit
			2SC2433			2SC2432			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	$V_{CB} = 120V$, $I_E = 0$	–	–	50	–	–	–	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 70V$, $I_E = 0$	–	–	–	–	–	50	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 4V$, $I_C = 0$	–	–	50	–	–	50	μA
Collector Cutoff Current	I_{CEO}	$V_{CE} = 120V$, $I_B = 0$	–	–	1	–	–	–	mA
Collector Cutoff Current	I_{CEO}	$I_{CE} = 70V$, $I_B = 0$	–	–	–	–	–	1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 50\,\mu A$, $I_E = 0$	120	–	–	70	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	5	–	–	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10mA$, $R_{BE} = \infty\Omega$	120	–	–	70	–	–	V
DC Current Gain	h_{FE1}	$V_{CE} = 5V$, $I_C = 3A$ *	35	–	200	35	–	200	–
DC Current Gain	h_{FE2}	$V_{CE} = 5V$, $I_C = 30A$ *	7	–	–	10	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 15A$, $I_B = 1.5A$*	–	0.5	1.5	–	0.5	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	2.0	–	1.2	2.0	V
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 2A$	–	80	–	–	80	–	MHz
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	350	–	–	350	–	pF
Rise Time	t_r	$I_C = 15A$, $R_L = 2\Omega$ $I_{B1} = -I_{B2} = 1.5A$	–	0.28	0.8	–	0.28	0.8	μs
Storage Time	t_{stg}		–	0.70	1.0	–	0.70	1.0	μs
Fall Time	t_f		–	0.15	0.8	–	0.15	0.8	μs

* Pulsed $P_W \leq 300\,\mu s$, Duty Ratio $\leq 6\%$

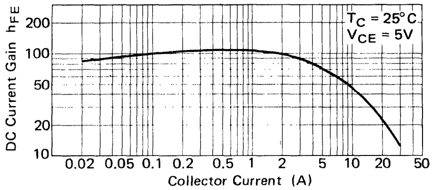
2SC1043, 2SA1044

DC CURRENT GAIN

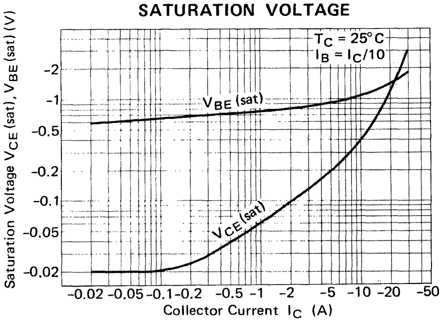


2SC2433, 2SC2434

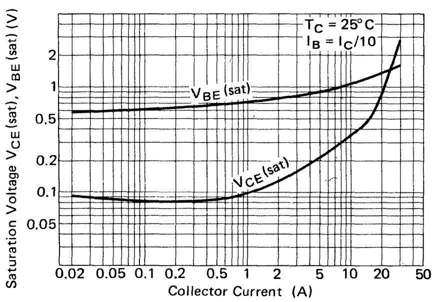
DC CURRENT GAIN



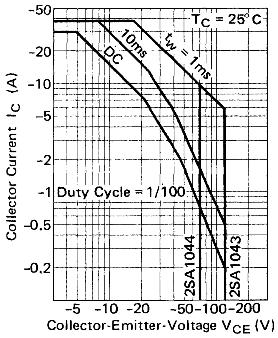
SATURATION VOLTAGE



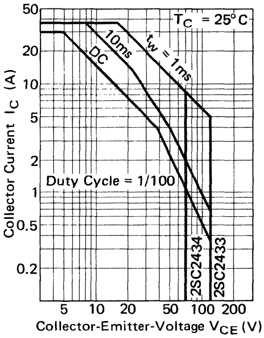
SATURATION VOLTAGE



SAFE OPERATING AREAS

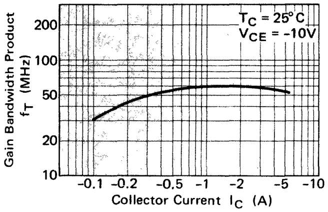


SAFE OPERATING AREAS

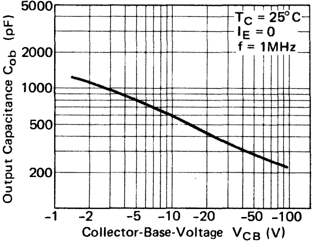


2SA 1043, 2SA1044

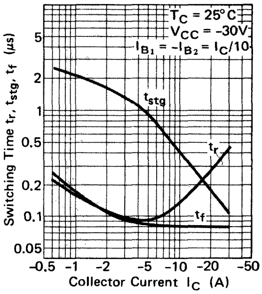
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE

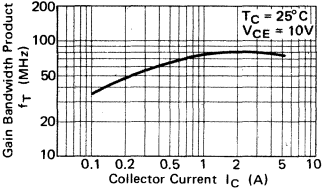


SWITCHING TIME

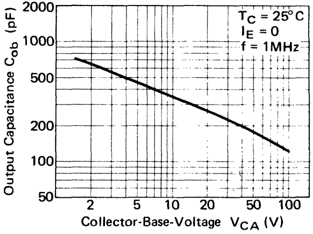


2SC2433, 2SC2434

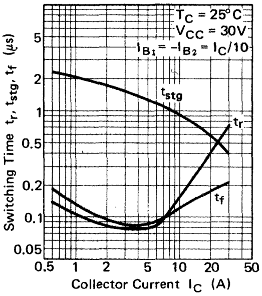
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



SWITCHING TIME



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Edition 1.1

FUJITSU

PRODUCT PROFILE

2SA1072, 2SA1072A, 2SA1073

Silicon High Speed Power Transistor

DESCRIPTION

The 2SA1072/2SA1072A/2SA1073 are silicon PNP general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

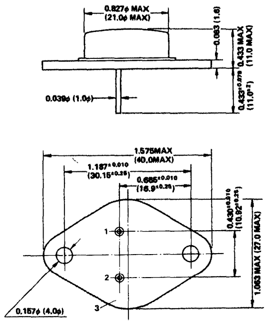
The 2SA1072/2SA1072A/2SA1073 are especially well-suited for high frequency power amplifiers, audio power amplifiers, switching regulators and DC-DC converters. NPN complements, 2SC2522/2SC2522A/2SC2523, are available.

- High f_T = 60 MHz (typ)
- Ultra fast switching speed
- Excellent safe operating area
- Improved reverse second-breakdown capability

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value			Unit
		2SA1072	2SA1072A	2SA1073	
Collector to Base Voltage	V_{CBO}	120	150	160	V
Emitter to Base Voltage	V_{EBO}	7	7	7	V
Collector to Emitter Voltage	V_{CEO}	120	150	160	V
Collector Current	I_C	12	12	12	A
Collector Power Dissipation (T_C = 25°C)	P_C	120	120	120	W
Junction Temperature	T_j	+150			°C
Storage Temperature Range	T_{stg}	–65 to +150			°C

OUTLINE DIMENSION
JEDEC TO–3



1: Emitter 2: Base 3: Collector (Case)
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits						Unit
			2SA1072/2SA1072A			2SA1073			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V/160V, I_E = 0	—	—	50/–	—	—	–/50	µA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7 V, I_C = 0	—	—	50	—	—	50	µA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V/160V, R_{BE} = ∞	—	—	1/–	—	—	–/1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50 µA, I_E = 0	120 150†	—	—	160	—	—	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50 µA, I_C = 0	7	—	—	7	—	—	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, R_{BE} = ∞	120 150†	—	—	160	—	—	V
DC Current Gain	h_{FE1}	V_{CE} = 5 V, I_C = 1 A*	60	—	200	60	—	200	—
DC Current Gain	h_{FE2}	V_{CE} = 5 V, I_C = 7 A*	40	—	—	40	—	—	—
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5 A, I_B – 0.5 A*	—	0.9	1.8	—	09	1.8	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5 A, I_C – 5 A*	—	1.25	1.7	—	1.25	1.7	V
Gain-Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 1 A, f = 10 MHz	45	60	—	45	60	—	MHz
Output Capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz		300	470	—	300	470	pF
Rise Time	t_r	I_C = 7.5 A, R_L = 4Ω I_{B1} = $-I_{B2}$ = 0.75 A	—	0.15	—	—	0.15	—	µs
Storage Time	t_{stg}		—	0.5	—	—	0.5	—	µs
Fall Time	t_f		—	0.11	—	—	0.11	—	µs

* Pulsed: Pulse width ≦ 300µs; Duty Cycle ≦ 6%
† For 2SA1072A only

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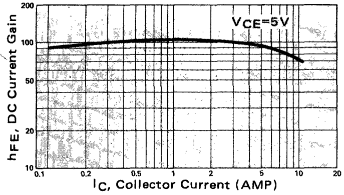
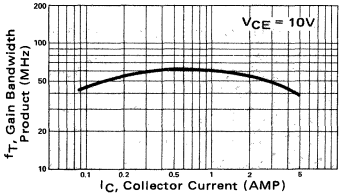
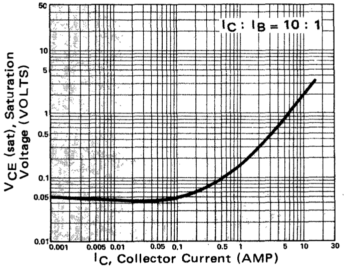
DC CURRENT GAIN



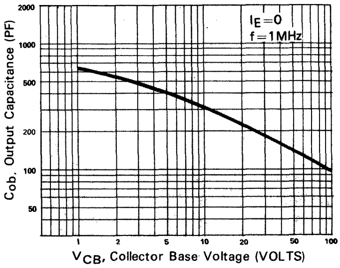
GAIN BANDWIDTH PRODUCT



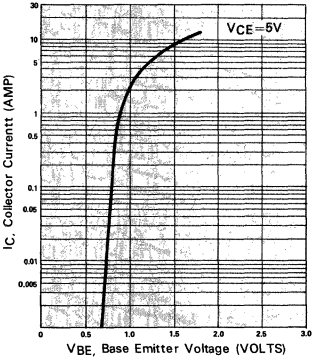
COLLECTOR SATURATION VOLTAGE



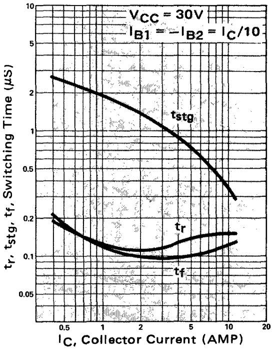
OUTPUT CAPACITANCE



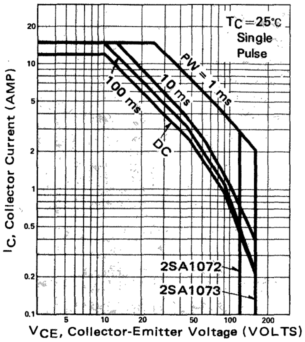
TRANSFER CHARACTERISTICS



SWITCHING TIME



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SA1077

Silicon High Speed Power Transistor

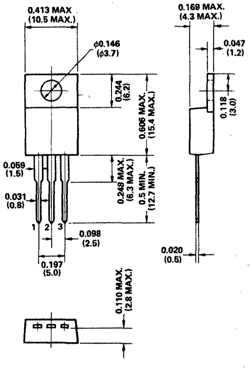
DESCRIPTION

The 2SA1077 is silicon PNP general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

The 2SA1077 is especially well-suited for High frequency power amplifiers, Audio power amplifiers, Switching regulators and DC-DC Converters.
A NPN complement, 2SC2527, is available.

- High f_T = 60 MHz (typ)
- Ultra fast switching speed
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	10	A
Collector Power Dissipation (T_C = 25°C)	P_C	60	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V, I_E = 0	–	–	50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	50	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V, I_B = 0	–	–	1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	7	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 1A *	60	–	200	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 5A *	40	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5A, I_B = 0.5A *	–	0.9	1.8	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 5A *	–	1.25	1.7	V
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=1A, f = 10MHz	30	60	–	MHz
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz	–	300	470	pF
Rise Time	t_r	I_C = 7.5A, R_L = 4Ω I_{B1} = $-I_{B2}$ = 0.75A	–	0.15	–	μs
Storage Time	t_{stg}		–	0.5	–	μs
Fall Time	t_f		–	0.11	–	μs

* Pulsed: Pulse Width ≦ 300μs
Duty Cycle ≦ 6%

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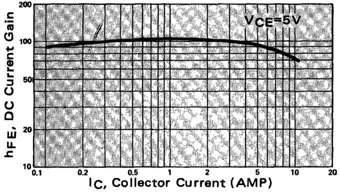
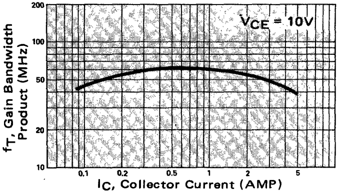
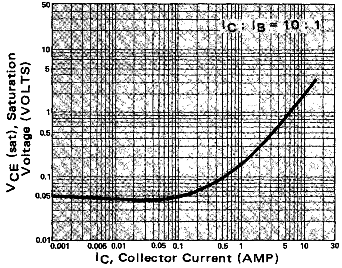


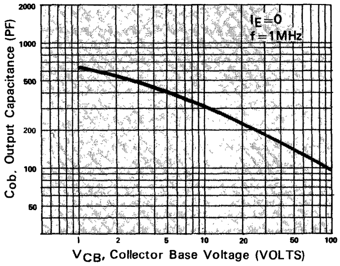
DC CURRENT GAIN



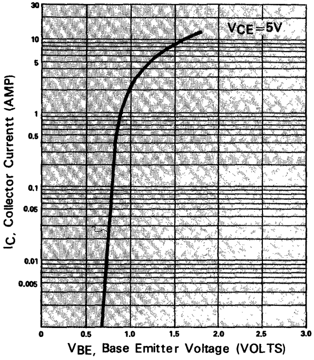
GAIN BANDWIDTH PRODUCT



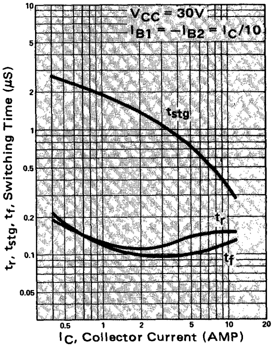
COLLECTOR SATURATION VOLTAGE



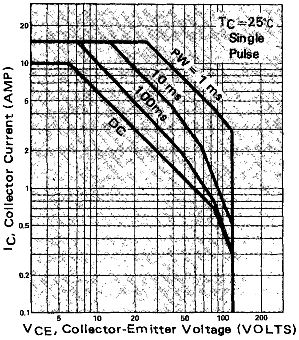
OUTPUT CAPACITANCE



TRANSFER CHARACTERISTICS



SWITCHING TIME



SAFE OPERATING AREAS

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SA1078

Silicon High Speed Power Transistor

DESCRIPTION

The 2SA1078 is a silicon PNP general purpose, medium power transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of medium power transistors with exceptional frequency response in high current applications.

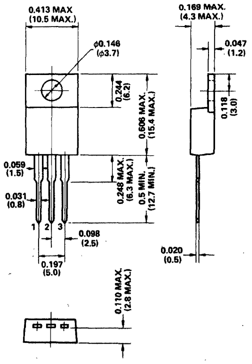
The 2SA1078 is especially well-suited for High frequency power amplifiers, Audio power amplifiers and drivers.
A NPN complement, 2SC2528, is available.

- High f_T = 140 MHz (typ)
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability
- Excellent Current Gain Linearity

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	5	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	2	A
Collector Power Dissipation (T_C = 25°C)	P_C	25	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V, I_E = 0	–	–	1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 5V, I_C = 0	–	–	1	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V, I_B = 0	–	–	100	μA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 1μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 1μA, I_C = 0	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C == 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 0.3A*	60	–	350	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 0.7A*	50	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 0.7A, I_B = 0.07A*	–	0.45	1.0	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 0.7A*	–	0.8	1.7	V
Gain-Bandwidth Product	f_T	V_{CE}=10V,1_C=0.5A,f=10MHz	–	140	–	MHz
Output Capacitance	Cob	V_{CB}=20V,I_E=0,f=1MHz	–	100	–	pF

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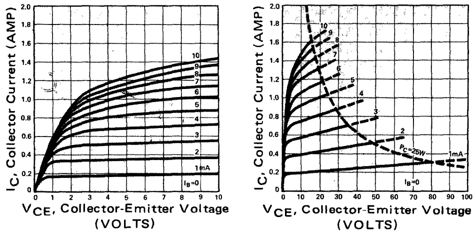
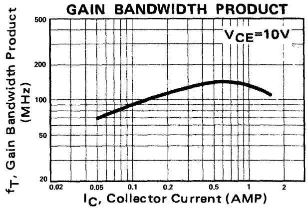
* Pulsed: Pulse Width ≤ 300μs
Duty Cycle ≤ 6%

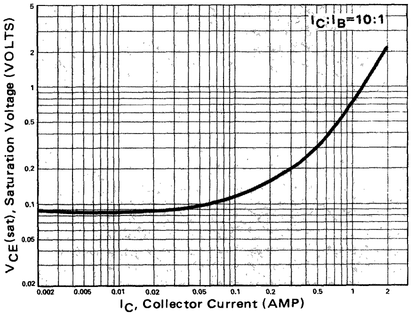
OUTPUT CHARACTERISTICS



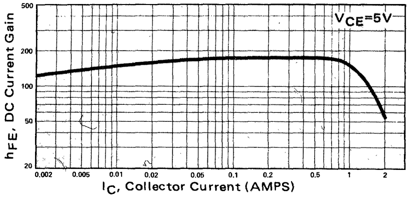
GAIN BANDWIDTH PRODUCT



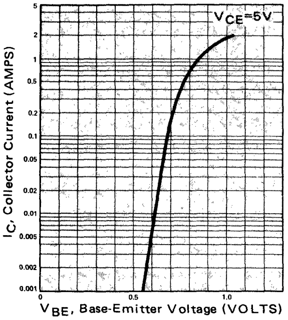
COLLECTOR SATURATION VOLTAGE



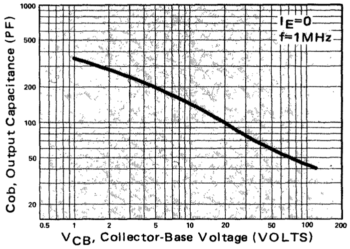
DC CURRENT GAIN



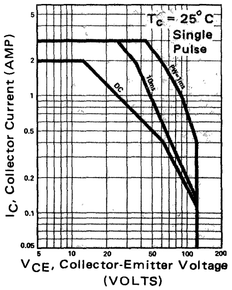
TRANSFER CHARACTERISTICS



OUTPUT CAPACITANCE



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SA1080

Silicon High Speed Power Transistor

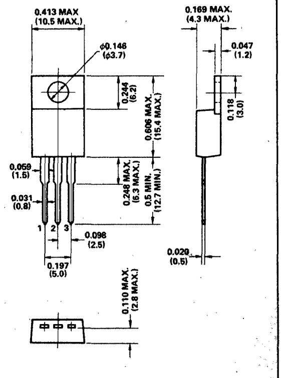
DESCRIPTION

The 2SA 1080 is a silicon PNP M.C.-Head amplifier use transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused balast resistors which provide uniform current density. This structure permits the design of M.C.-Head amplifier use transistors with exceptional frequency response along with excellent current gain linearity.

A NPN complement, 2SC 2530, is available.

- High f_T=30MHz (TYP.)
- Excellent Current Gain-Linearity

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	40	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector to Emitter Voltage	V_{CEO}	40	V
Collector Current	I_C	0.5	A
Collector Power Dissipation (T_C = 25°C)	P_C	20	W
Junction Temperature	T_j	+150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 40V, I_E = 0	–	–	100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	100	nA
Collector Cutoff Current	I_{CEO}	V_{CE} = 40V, I_B = 0	–	–	500	nA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100nA, I_E = 0	40	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100nA, I_C = 0	7	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	40	–	–	V
DC Current Gain	h_{FE}	V_{CE} = 5V, I_C = 10mA *	100	–	350	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10mA, I_B = 1mA *	–	0.025	0.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	I_C = 10mA, I_B = 1mA *	–	0.65	1.0	V
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=10mA, f=10MHz	–	30	–	MHz
Output Capacitance	C_{ob}	V_{CB}=20V, I_E=0, f=1MHz	–	65	–	pF

* Pulsed: Pulse Width $\leqq$ 300μs
Duty Cycle $\leqq$ 6%

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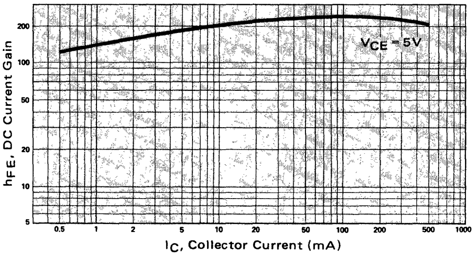
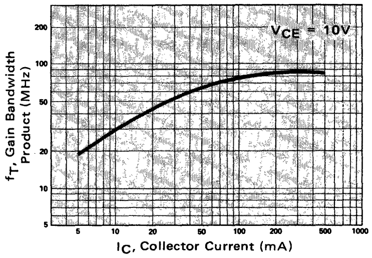
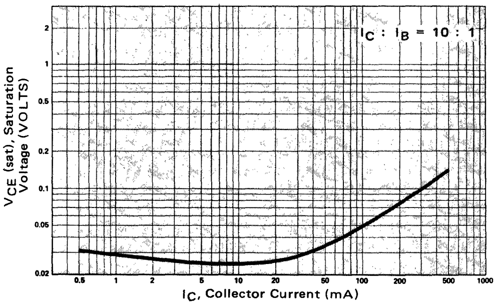


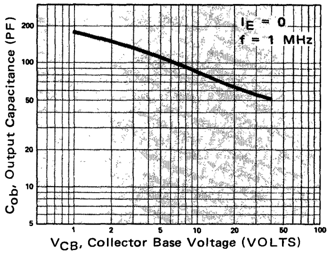
DC CURRENT GAIN



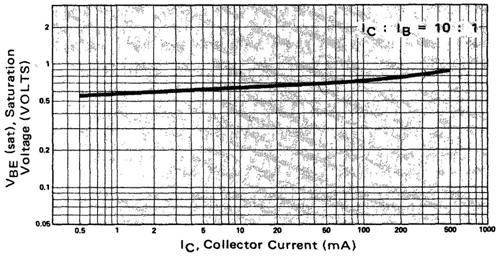
GAIN BANDWIDTH PRODUCT



COLLECTOR TO EMITTER SATURATION VOLTAGE



OUTPUT CAPACITANCE



BASE TO EMITTER SATURATION VOLTAGE

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2428

Silicon High Speed Power Transistor

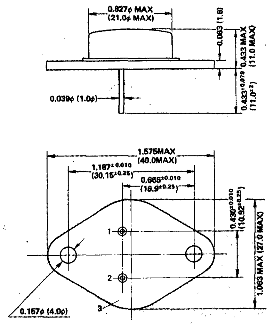
DESCRIPTION

The 2SC 2428 is a silicon NPN general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

The 2SC 2428 is especially well-suited for High frequency power amplifiers, Audio power amplifiers, Switching regulators and DC-DC Converters.

- High f_T = 80 MHz (typ)
- Ultra fast switching speed
- Excellent Safe Operating Area
- Improved Reverse Second-Breakdown Capability

OUTLINE DIMENSION
JEDEC TO–3



1: Emitter 2: Base 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	180	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector to Emitter Voltage	V_{CEO}	180	V
Collector Current	I_C	12	A
Base Current	I_B	3	A
Collector Power Dissipation (T_C = 25°C)	P_C	120	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	-65~+175	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 180V, I_E = 0	–	–	50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	1	mA
Collector Cutoff Current	I_{CEO}	V_{CE} = 180V, I_B = 0	–	–	1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	180	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 1mA, I_C = 0	7	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 10mA, $R_{BE} = \infty$	180	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 0.5A *	35	110	200	–
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 5A *	15	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5A, I_B = 1A *	–	0.3	0.8	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	I_C = 5A, I_B = 1A *	–	1.15	1.5	V
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=1A, f=10MHz	40	80	–	MHz
Rise Time	t_r	I_C = 7.5A, R_L = 4Ω $I_{B1} = -I_{B2}$ = 0.75A	–	0.2	1.0	μs
Storage Time	t_{stg}		–	0.6	1.2	μs
Fall Time	t_f		–	0.15	1.0	μs

* Pulsed: Pulse Width ≦ 300μs
Duty Cycle ≦ 2%

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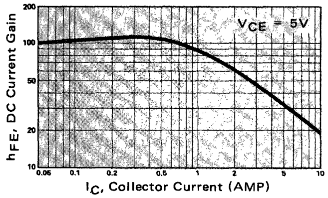
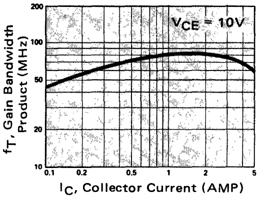
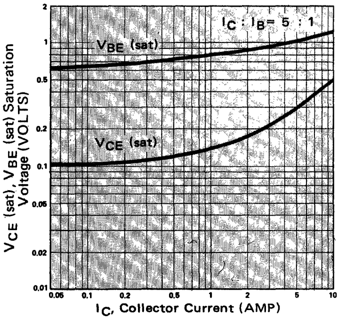
DC CURRENT GAIN



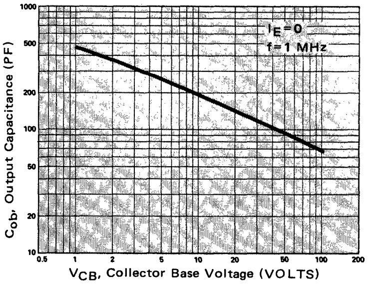
GAIN BANDWIDTH PRODUCT



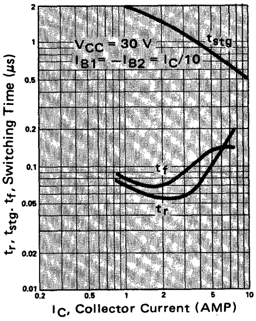
SATURATION VOLTAGE



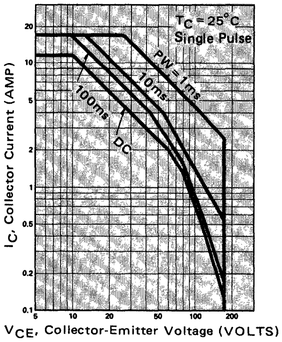
OUTPUT CAPACITANCE



SWITCHING TIME



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2522, 2C2522A, 2C2523

Silicon High Speed Power Transistor

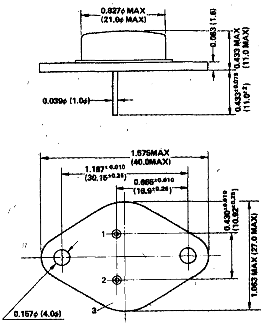
DESCRIPTION

The 2SC2522/2SC2522A/2SC2523 are silicon NPN general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transitor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

The 2SC2522/2SC2522A/2SC2523 are especially well-suited for high frequency power amplifiers, audio power amplifiers, switching regulators and DC-DC converters. PNP complements, 2SA1072/2SA1072A/2SA1073, are available.

- High f_T = 80 MHz (typ)
- Ultra fast switching speed
- Excellent safe operating area
- Improved reverse second-breakdown capability

OUTLINE DIMENSION
JEDEC TO–3



1: Emitter 2: Base 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value			Unit
		2SC2522	2SC2522A	2SC2523	
Collector to Base Voltage	V_{CBO}	120	150	160	V
Emitter to Base Voltage	V_{EBO}	7	7	7	V
Collector to Emitter Voltage	V_{CEO}	120	150	160	V
Collector Current	I_C	12	12	12	A
Collector Power Dissipation (T_C = 25°C)	P_C	120	120	120	W
Junction Temperature	T_j	+150			°C
Storage Temperature Range	T_{stg}	–65 to +150			°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits						Unit
			2SC2522/2SC2522A			2SC2523			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V/160V, I_E = 0	—	—	50/–	—	—	–/50	µA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7 V, I_C = 0	—	—	50	—	—	50	µA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V/160V, R_{BE} = ∞	—	—	1/–	—	—	–/1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50 µA, I_E = 0	120 150†	—	—	160	—	—	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50 µA, I_C = 0	7	—	—	7	—	—	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, R_{BE} = ∞	120 150†	—	—	160	—	—	V
DC Current Gain	h_{FE1}	V_{CE} = 5 V, I_C = 1 A*	60	—	200	60	—	200	
DC Current Gain	h_{FE2}	V_{CE} = 5 V, I_C = 7 A*	40	—	—	40	—	—	—
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5 A, I_B = 0.5 A*	—	0.7	1.8	—	0.7	1.8	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5 V, I_C = 5 A*	—	1.25	1.7	—	1.25	1.7	V
Gain-Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 1 A, f = 10MHz	50	80	—	50	80	—	MHz
Output Capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1MHz		180	300	—	180	300	pF
Rise Time	t_r	I_C = 7.5 A, R_L = 4Ω I_{B1} = –I_{B2} = 0.75 A	—	0.3	—	—	0.3	—	µs
Storage Time	t_{stg}		—	1.3	—	—	1.3	—	µs
Fall Time	t_f		—	0.2	—	—	0.2	—	µs

* Pulsed: Pulse width ≤ 300µs; Duty Cycle ≤ 6%
† For 2SC2522A only

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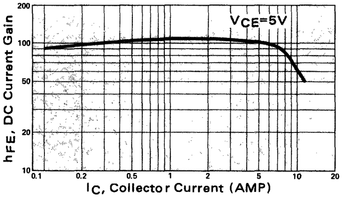
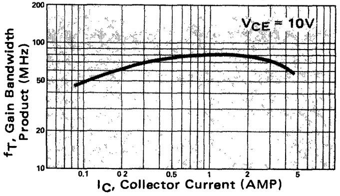
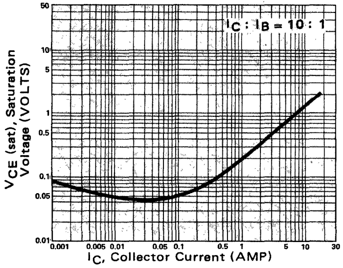
DC CURRENT GAIN



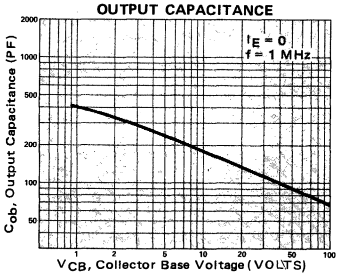
GAIN BANDWIDTH PRODUCT



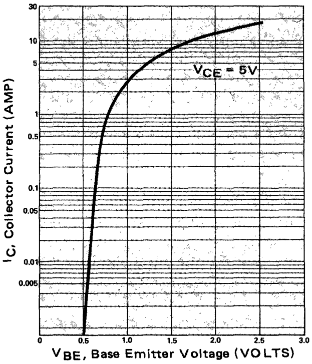
COLLECTOR SATURATION VOLTAGE



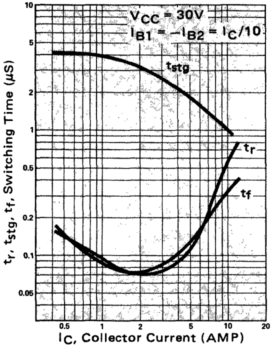
OUTPUT CAPACITANCE



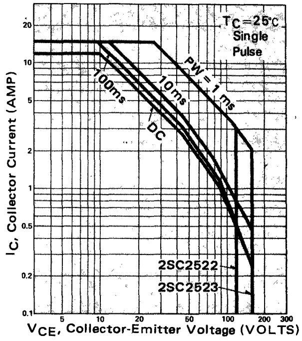
TRANSFER CHARACTERISTICS



SWITCHING TIME



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2525, 2SC2526

Silicon High Speed Power Transistor

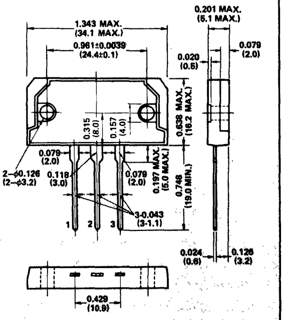
DESCRIPTION

The 2SC2525/2SC2526 are silicon NPN general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

The 2SC2525/2SC2526 are especially well-suited for High frequency power amplifiers, Audio power amplifiers, Switching regulators and DC-DC Converters. PNP complements, 2SA1075/2SA1076, are available.

- High f_T = 80 MHz (typ)
- Ultra fast switching speed
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability

OUTLINE DIMENSION
RM-60



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		2SC 2525	2SC 2526	
Collector to Base Voltage	V_{CBO}	120	160	V
Emitter to Base Voltage	V_{EBO}	7	7	V
Collector to Emitter Voltage	V_{CEO}	120	160	V
Collector Current	I_C	12	12	A
Collector Power Dissipation (T_C = 25°C)	P_C	120	120	W
Junction Temperature	T_j	+150		°C
Storage Temperature Range	T_{stg}	-65 ~ +150		°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits						Unit
			2SC 2525			2SC 2526			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V/160V, I_E = 0	–	–	50/–	–	–	–/50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	50	–	–	50	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V/160V, $R_{BE} = \infty$	–	–	1/–			–/1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	120	–	–	160	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	7	–	–	7	–	–	V
Collector to Emitter Breakdown Voltrage	$V_{(BR)CEO}$	I_C = 1mA, $R_{BE} = \infty$	120	–	–	160	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 1A *	60	–	200	60	–	200	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 7A *	40	–	–	40	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5A, I_B = 0.5A *	–	0.7	1.8	–	0.7	1.8	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 5A *	–	1.25	1.7	–	1.25	1.7	V
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 1A, f = 10MHz	50	80	–	50	80	–	MHz
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz	–	180	300	–	180	300	pF
Rise Time	t_r	I_C = 7.5A, R_L = 4Ω I_{B1} = $-I_{B2}$ = 0.75A	–	0.3	–	–	0.3	–	μs
Storage Time	t_{stg}		–	1.3	–	–	1.3	–	μs
Fall Time	t_f		–	0.2	–	–	0.2	–	μs

* Pulsed: Pulse Width ≦ 300μs
Duty Cycle ≦ 6%

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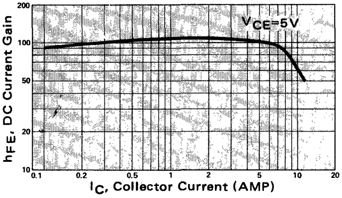
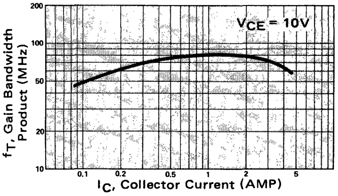
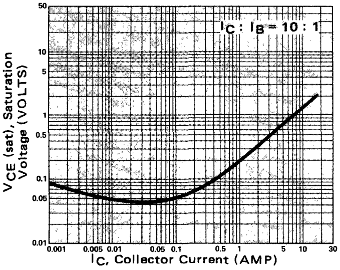
DC CURRENT GAIN



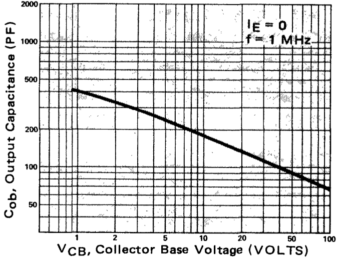
GAIN BANDWIDTH PRODUCT



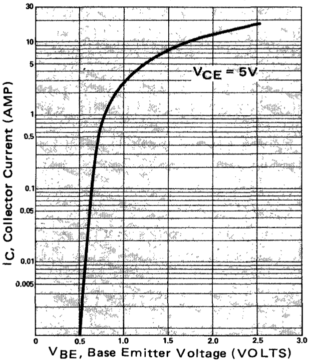
COLLECTOR SATURATION VOLTAGE



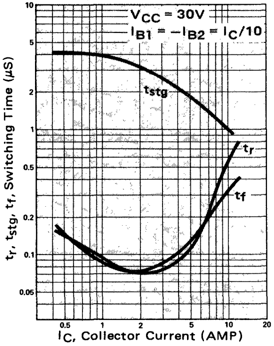
OUTPUT CAPACITANCE



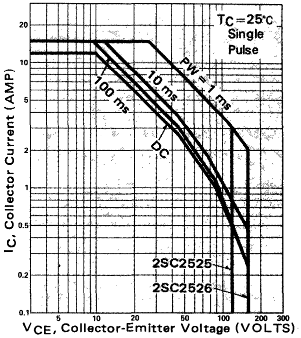
TRANSFER CHARACTERISTICS



SWITCHING TIME



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2527

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC 2527 is silicon NPN general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional switching characteristics and frequency response in high current applications.

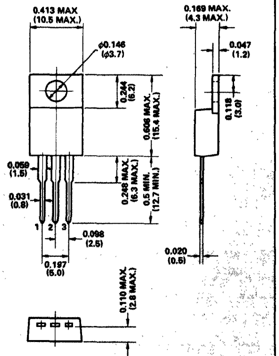
The 2SC 2527 is especially well-suited for High frequency power amplifiers, Audio power amplifiers, Switching regulators and DC-DC Converters.
A PNP complement, 2SA 1077 is available.

- High f_T = 80 MHz (typ)
- Ultra fast switching speed
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	10	A
Collector Power Dissipation (T_C = 25°C)	P_C	60	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V, I_E = 0	–	–	50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	50	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V, I_B = 0	–	–	1	mA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	IE = 50μA, I_C = 0	7	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 1A *	60	–	200	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 5A *	40	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 5A, I_B = 0.5A *	–	0.7	1.8	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 5A *	–	1.25	1.7	V
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=1A, f=10MHz	40	80	–	MHz
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz	–	180	300	pF
Rise Time	t_r	I_C = 7.5A, R_L = 4Ω I_{B1} = $-I_{B2}$ = 0.75A	–	0.3	–	μs
Storage Time	t_{stg}		–	1.3	–	μs
Fall Time	t_f		–	0.2	–	μs

* Pulsed: Pulse Width ≦ 300μs
Duty Cycle ≦ 6%

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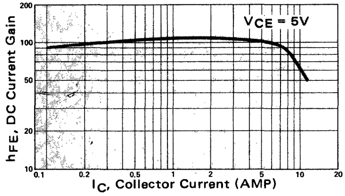
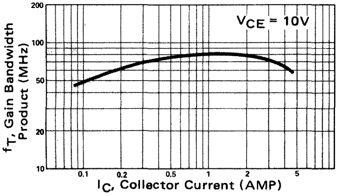
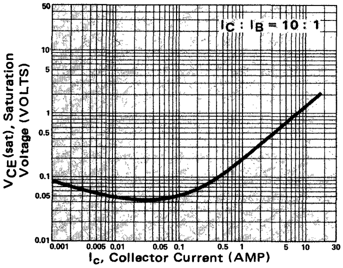
DC CURRENT GAIN



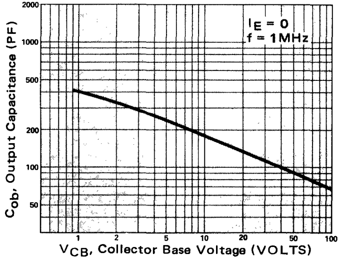
GAIN BANDWIDTH PRODUCT



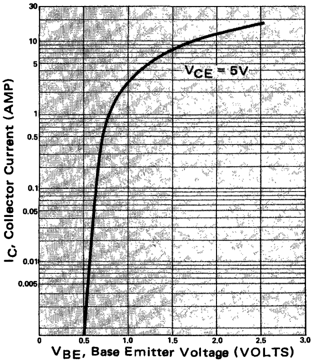
COLLECTOR SATURATION VOLTAGE



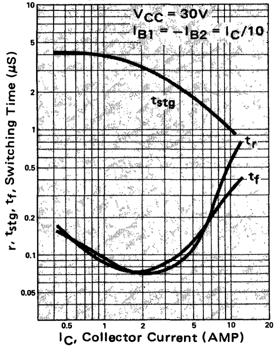
OUTPUT CAPACITANCE



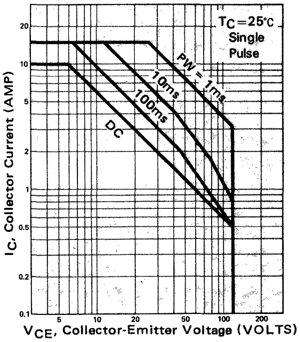
TRANSFER CHARACTERISTICS



SWITCHING TIME



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2528

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC2528 is a silicon NPN general purpose, medium power transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of medium power transistors with exceptional frequency response in high current applications.

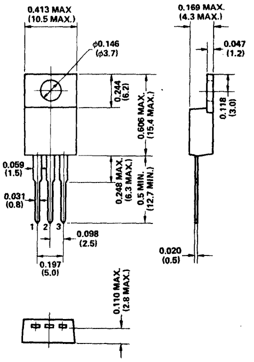
The 2SC2528 is especially well-suited for High frequency power amplifiers, Audio power amplifiers and drivers.
A PNP complement, 2SA1078, is available.

- High f_T = 160 MHz (typ)
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability
- Excellent Current Gain Linearity

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	5	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	2	A
Collector Power Dissipation (T_C = 25°C)	P_C	25	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 120V, I_E = 0	–	–	1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 5V, I_C = 0	–	–	1	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 120V, I_B = 0	–	–	100	μA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 1μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 1μA, I_C = 0	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 0.3A*	60	–	350	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 0.7A*	50	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 0.7A, I_B = 0.07A*	–	0.15	1.0	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 0.7A*	–	0.8	1.7	V
Gain-Bandwidth Product	f_T	V_{CE}=10V,I_C=0.5A,f=10MHz	–	160	–	MHz
Output Capacitance	C_{ob}	V_{CB}=20V,I_E=0,f=1MHz	–	60	–	pF

* Pulsed: Pulse Width ≤ 300μs
Duty Cycle ≤ 6%

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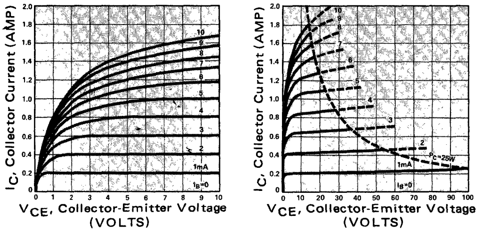
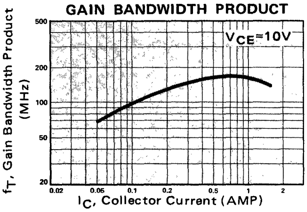
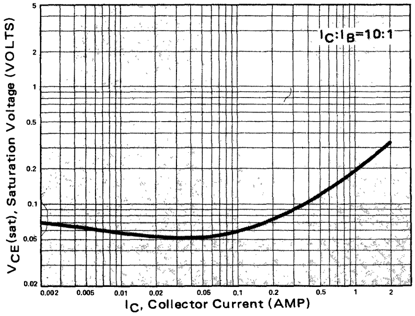
OUTPUT CHARACTERISTICS



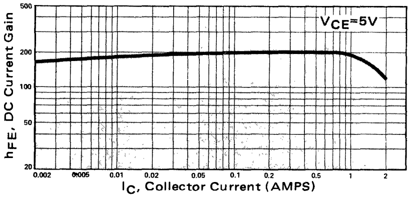
GAIN BANDWIDTH PRODUCT



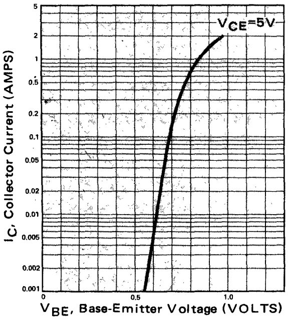
COLLECTOR SATURATION VOLTAGE



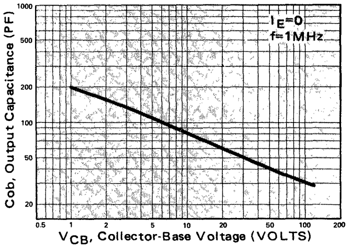
DC CURRENT GAIN



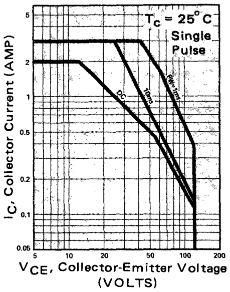
TRANSFER CHARACTERISTICS



OUTPUT CAPACITANCE



SAFE OPERATING AREAS



January 1990
Edition 1.1

PRODUCT PROFILE

2SC2530

Silicon High Speed Power Transistor

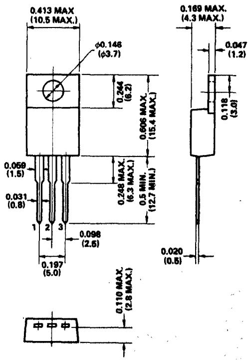
DESCRIPTION

The 2SC 2530 is a silicon NPN M.C.-Head amplifier use transistor fabricated with Fujitus's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused balast resistors which provide uniform current density. This structure permits the design of M.C.-Head amplifier use transistors with exceptional frequency response along with excellent current gain linearity.

A PNP complement, 2SA 1080, is available.

- High f_T=35MHz (TYP.)
- Excellent Current Gain-Linearity

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector 3: Emitter
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	40	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector to Emitter Voltage	V_{CEO}	40	V
Collector Current	I_C	0.5	A
Collector Power Dissipation (T_C = 25°C)	P_C	20	W
Junction Temperature	T_j	+150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 40V, I_E = 0	–	–	100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 7V, I_C = 0	–	–	100	nA
Collector Cutoff Current	I_{CEO}	V_{CE} = 40V, I_B = 0	–	–	500	nA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100nA, I_E = 0	40	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100nA, I_C = 0	7	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} =∞	40	–	–	V
DC Current Gain	h_{FE}	V_{CE} = 5V, I_C = 10 mA *	100	–	350	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10mA, I_B = 1mA *	–	0.065	0.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	IC = 10mA, I_B = 1mA *	–	0.6	1.0	V
Gain-Bandwidth Product	f_T	V_{CE}=10V, I_C=10mA, f=10MHz	–	35	–	MHz
Output Capacitance	C_{ob}	V_{CB}=20V, I_E =0, f=1MHz	–	25	–	pF

* Pulsed: Pulse Width ≤ 300μs
Duty Cycle ≤ 6%

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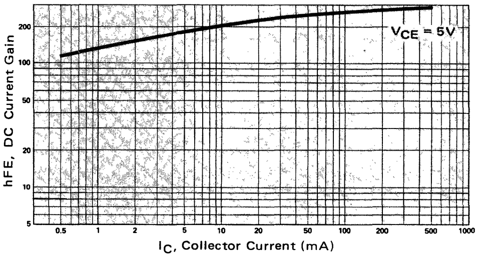
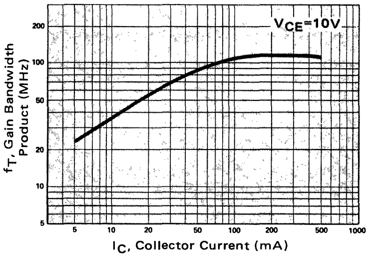
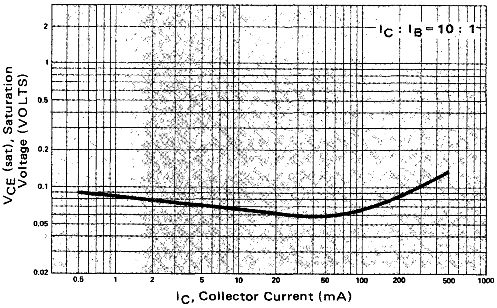
DC CURRENT GAIN



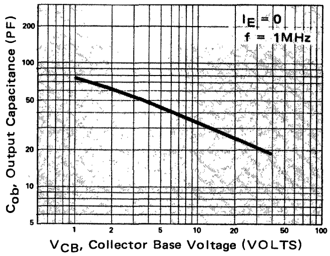
GAIN BANDWIDTH PRODUCT



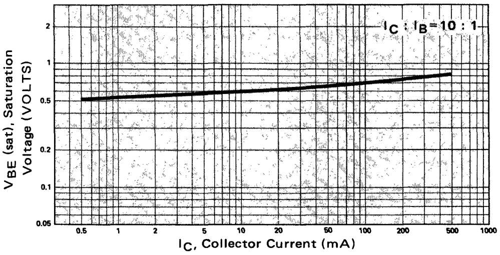
COLLECTOR TO EMITTER SATURATION VOLTAGE



OUTPUT CAPACITANCE



BASE TO EMITTER SATURATION VOLTAGE



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2920, 2SC2429, 2SC2429A, 2SC2964, 2SC2965

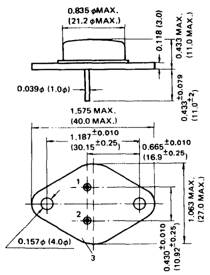
Silicon High Speed Power Transistor

DESCRIPTION

This series are silicon NPN planer general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

This series are especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

OUTLINE DIMENSION
JEDEC TO–3



1: Emitter 2: Base 3: Collector (Case)
Dimension in inches and (millimeters)

Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic oscillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

Outline of the Series (Ta = 25 °C)

Parts Number	V_{CEO} (V) Min.	t_{stg} (μs) Typ. at 10 A	t_f (μs) Typ. at 10 A	Operating Frequency Range of Switching Regulator
2SC2920	400	1.80 *1	0.18 *1	20 ~ 50 kHz
2SC2429	400	1.80 *2	0.11 *2	50 ~ 100 kHz
2SC2429A	450			
2SC2964	400	0.84 *2	0.10 *2	100 ~ 200 kHz
2SC2965	450			

*1: $I_{B1} = -I_{B2} = 1$ A, *2: $I_{B1} = -I_{B2} = 2$ A

Maximum Ratings (Ta = 25 °C)

Item	Symbol	Test Condition	Ratings					Unit
			2SC2920	2SC2429	2SC2429A	2SC2964	2SC2965	
Storage Temperature	T_{stg}		−65 ~ +175					°C
Junction Temperature	T_j		+175					°C
Collector-Base Voltage	V_{CBO}		450		600			V
Emitter-Base Voltage	V_{EBO}		7.0					V
Collector-Emitter Voltage	V_{CEO}		400		450	400	450	V
Collector Current-Continuous	I_C		15					A
Collector Current-Pulsed	I_{CP}	$P_w \leqq 10$ mS D.R. $\leqq 2$ %	20					A
Base Current-Continuous	I_B		5					A
Collector Power Dissipation	P_C	Tc = 25 °C	150					W

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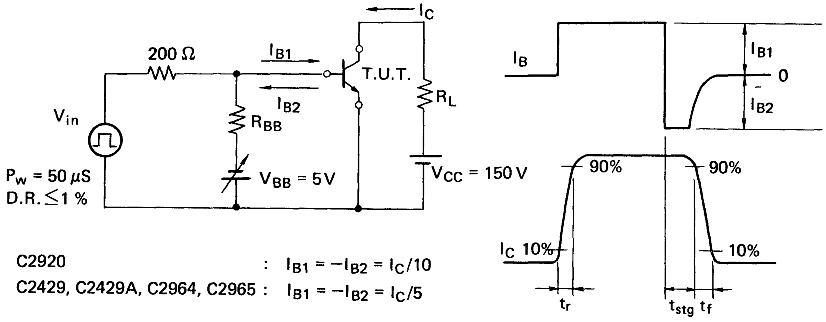
MAY 1982

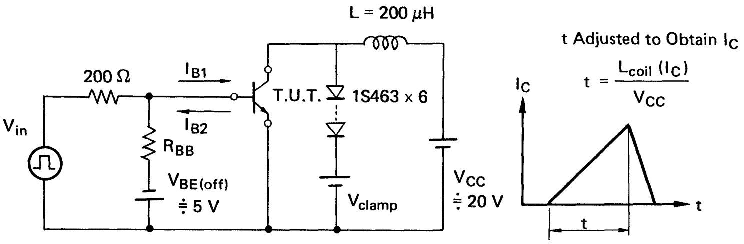
- **Test Circuit used for Measurement of Switching Time (Resistive)**



C2920 : $I_{B1} = -I_{B2} = I_C/10$

C2429, C2429A, C2964, C2965 : $I_{B1} = -I_{B2} = I_C/5$

- **Test Circuit used for Measurement of $V_{CEX(SUS)}$ and Reverse Bias Safe Operating Area**



ⓐ $V_{CEX(SUS)}$

I_C = 8 A, I_{B1} = 2 A, I_{B2} = −1 A, R_{BB} = 5 Ω, V_{clamp} = 450 V

ⓑ Reverse Bias Safe Operating Area

$I_{B1} \leq 4$ A, I_{B2} = −1 A, R_{BB} = 5 Ω

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2920

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Rating	Symbol	2SC2920	Unit
Collector to Emitter Voltage	V_{CEO}	400	V
Collector to Base Voltage	V_{CBO}	450	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	15	A
Collector Current-Pulsed ($P_W \leq 10$ mS, D.R. ≤ 2 %)	I_{CP}	20	A
Base Current-Continuous	I_B	5	A
Collector Power Dissipation ($T_C = 25$ °C)	P_C	150	W
Junction Temperature	T_j	175	°C
Storage Temperature Range	T_{stg}	−65 ~ +175	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

Parameters	Symbols	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\mu A$, $I_E = 0$	450	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1$ mA, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 1$ A, $R_{BE} = \infty\,\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 8$ A, $I_{B2} = -1$ A, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 450$ V, $I_E = 0$	–	–	100	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6$ V, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 2$ V, $I_C = 10$ A (*2)	10	13	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10$ A, $I_B = 1$ A (*2)	–	0.56	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10$ V, $I_E = 0$, f = 1MHz	–	240	–	PF
Gain Bandwidth Product	f_T	$V_{CE} = 10$ V, $I_C = 2$ A	–	30	–	MHz
Rise Time	t_r	$V_{CC} = 150$ V (*1) $I_C = 10$ A, $I_{B1} = -I_{B2} = 1$ A	–	0.20	0.5	μs
Storage Time	t_{stg}		–	1.80	3.0	μs
Fall Time	t_f		–	0.18	0.3	μs

*1 Test Circuit
*2 Pulsed $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6$ %

MARCH 1981

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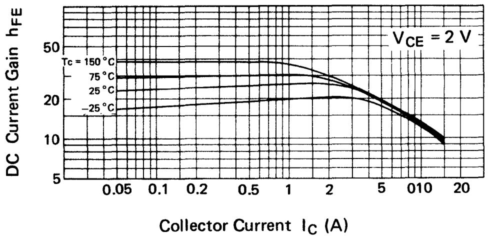
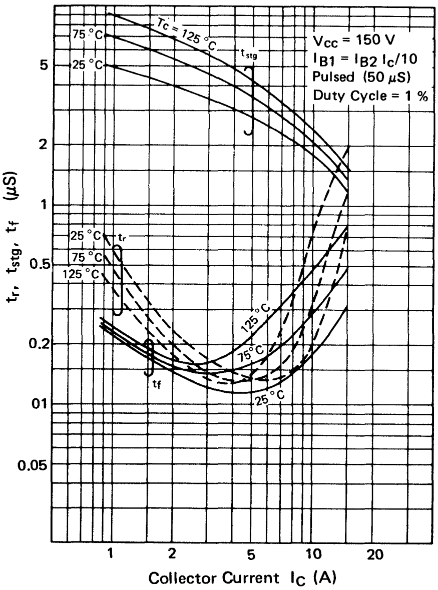
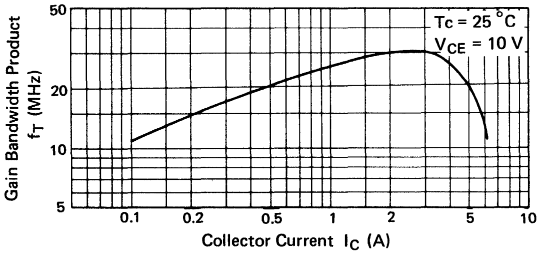
DC Current Gain



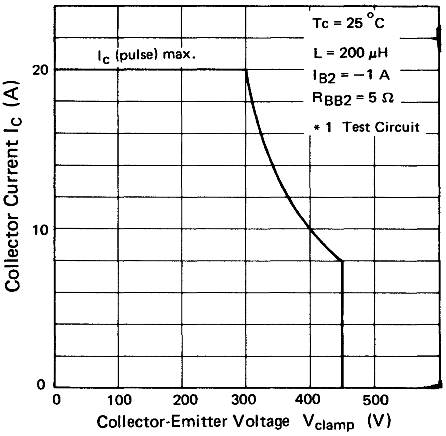
Switching Time



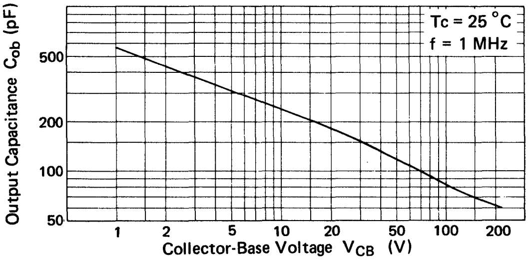
Gain Bandwidth Product



Reverse Bias Safe Operating Area

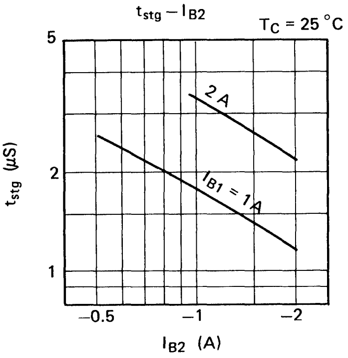


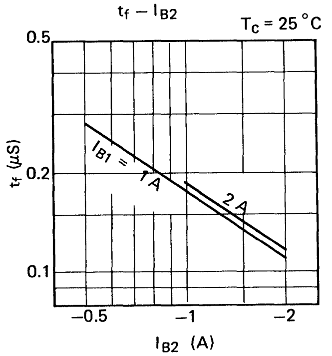
Output Capacitance

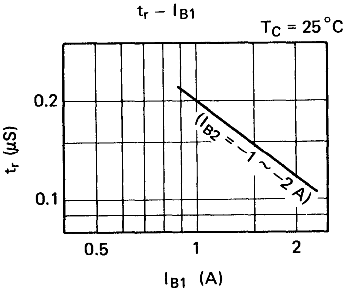


Switching Time

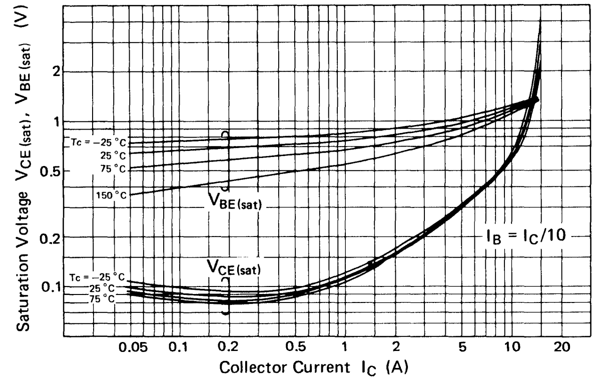
V_{CC} = 150 V
I_C = 10 A
Pulsed (50 μS)
Duty Ratio = 1 %



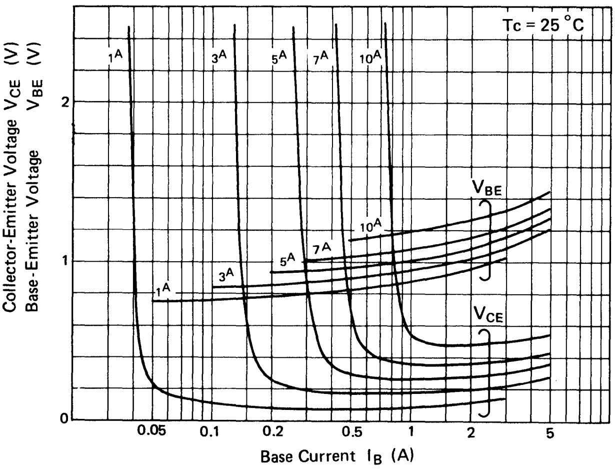




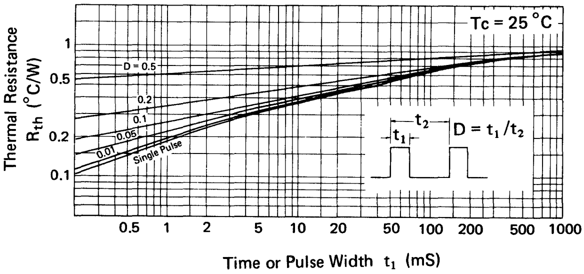
Saturation Voltage



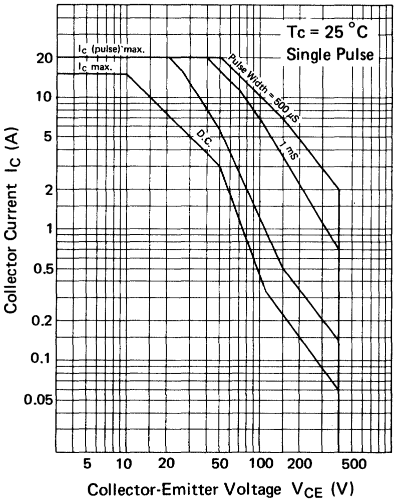
Collector Saturation Region



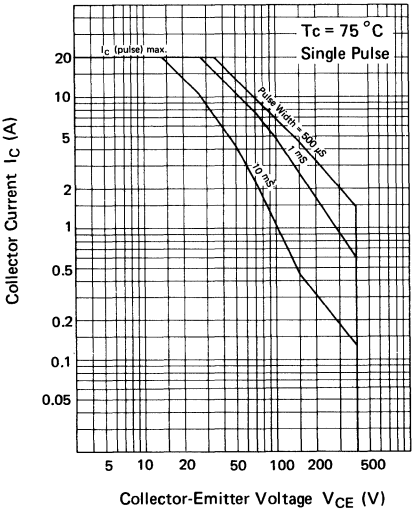
Thermal Response



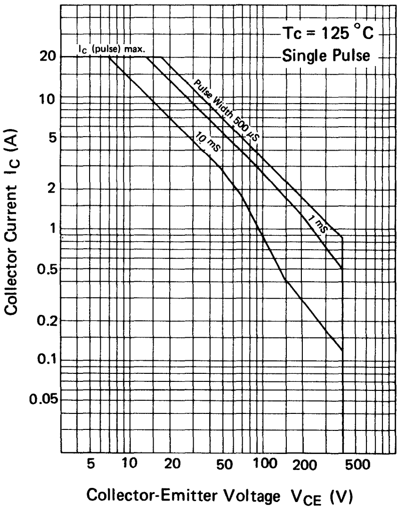
Forward Bias Safe Operating Area



Forward Bias Safe Operating Area



Forward Bias Safe Operating Area



January 1990
Edition 1.1

2SC2429, 2SC2429A

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Rating	Symbol	2SC2429	2SC2429A	Unit
Collector to Emitter Voltage	V_{CEO}	400	450	V
Collector to Base Voltage	V_{CBO}	450	600	V
Emitter to Base Voltage	V_{EBO}	7	7	V
Collector Current-Continuous	I_C	15	15	A
Collector Current-Pulsed ($P_w \leq 10$ mS, D.R. ≤ 2 %)	I_{CP}	20	20	A
Base Current-Continuous	I_B	5	5	A
Collector Power Dissipation (T_C = 25°)	P_C	150	150	W
Junction Temperature	T_j	175	175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

Parameters	Symbols	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	2SC2429: I_C = 100 μA, I_E = 0	450	–	–	V
		2SC2429A: I_C = 1 mA, I_E = 0	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 1 mA, I_C = 0	7	–	–	V
Collector Emitter Sustaining Voltage	$V_{CEO(SUS)}$	I_C = 1 A, R_{BE} = ∞Ω 2SC2429	400	–	–	V
		2SC2429A	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	I_C = 8 A, I_{B2} = −1 A, L = 200 μH (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	2SC2429: V_{CB} = 450 V, I_E = 0	–	–	100	μA
		2SC2429A: V_{CB} = 500 V, I_E = 0	–	–	100	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 6 V, I_C = 0	–	–	100	μA
DC Current Gain	h_{FE}	V_{CE} = 5 V, I_C = 10 A (*2)	10	15	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 A, I_B = 2 A (*2)	–	0.56	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	2SC2429	–	1.25	2.0	V
		2SC2429A	–	1.25	1.5	V
Output Capacitance	C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	–	240	–	PF
Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 2 A	–	30	–	MHz
Rise Time	t_r	V_{CC} = 150 V I_C = 10 A, I_{B1} = $-I_{B2}$ = 2 A (*1)	–	0.13	0.5	μs
Storage Time	t_{stg}		–	1.80	2.5	μs
Fall Time	t_f		–	0.11	0.3	μs

*1 Test Circuit

*2 Pulsed $P_w \leq 300$ μs, Duty Ratio ≤ 6 %

MARCH 1981

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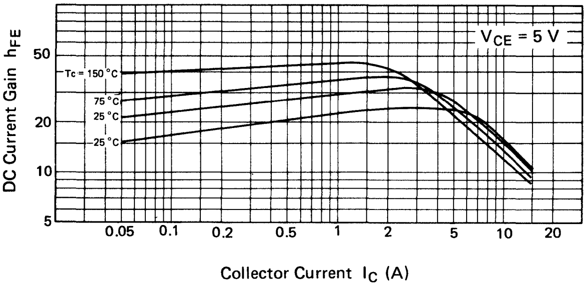
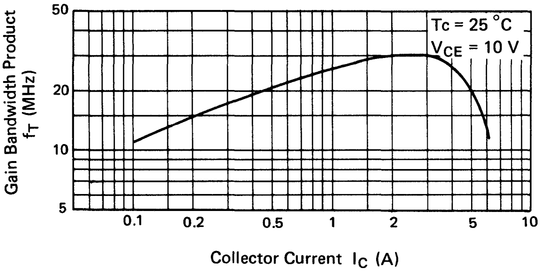
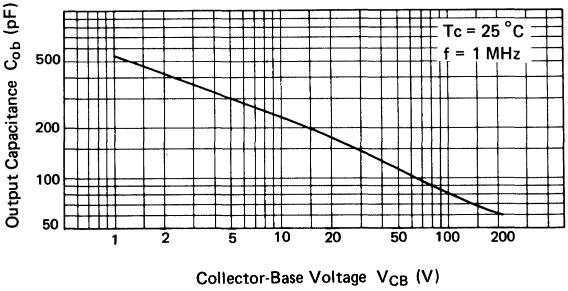
DC Current Gain



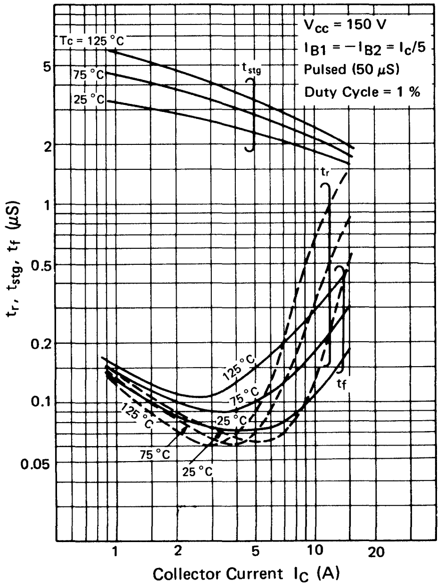
Gain Bandwidth Product



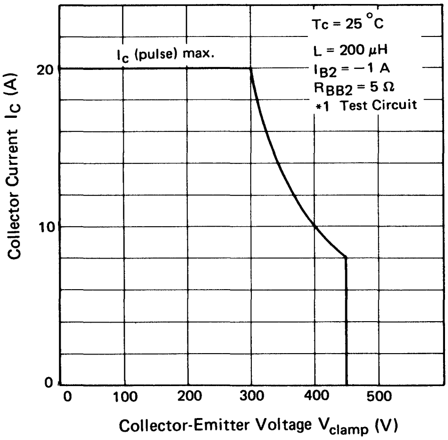
Output Capacitance



Switching Time



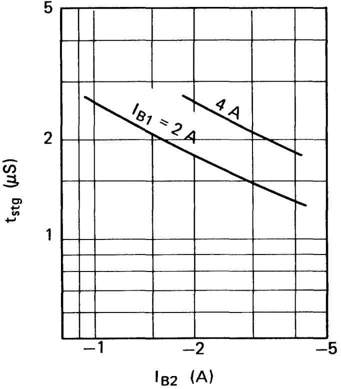
Reverse Bias Safe Operating Area



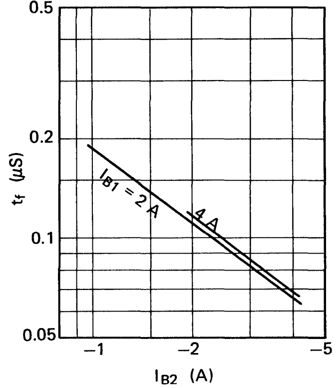
Switching Time

V_{CC} = 150 V
I_C = 10 A
Pulsed (50 μS)
Duty Ratio = 1 %

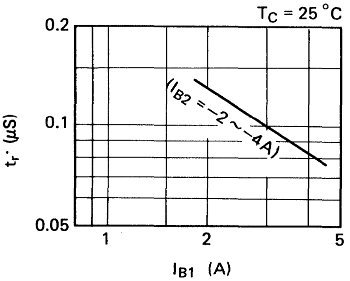
$t_{stg} - I_{B2}$



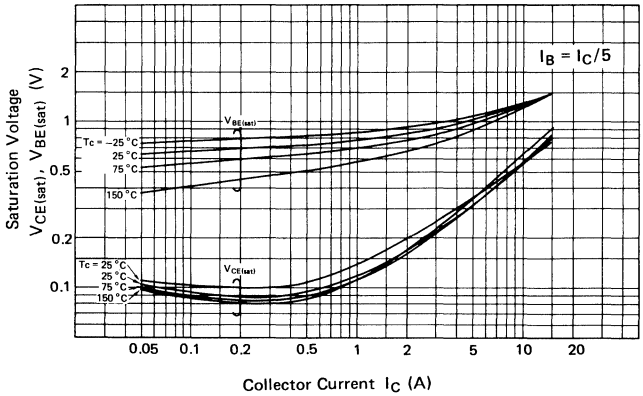
$t_f - I_{B2}$



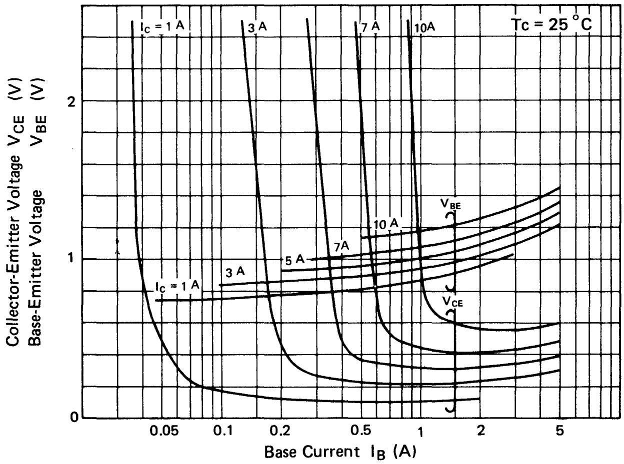
$t_r - I_{B1}$



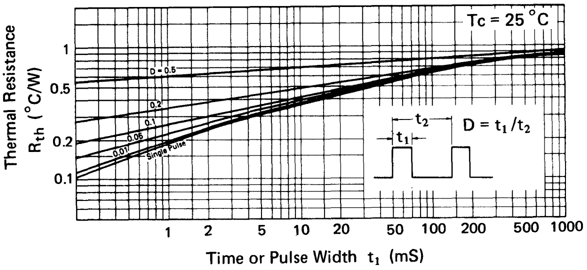
Saturation Voltage



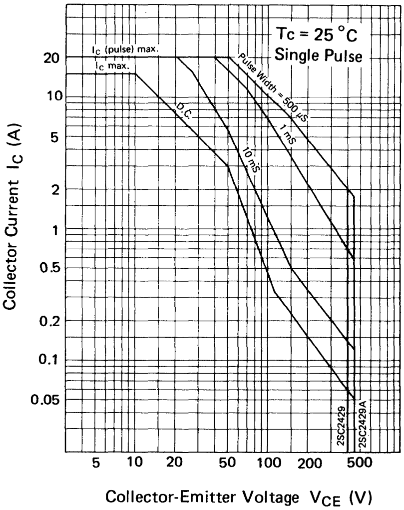
Collector Saturation Region



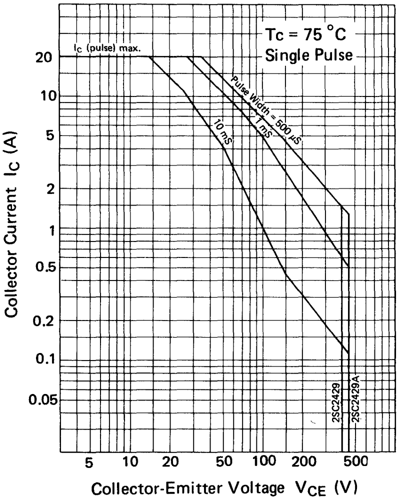
Thermal Response



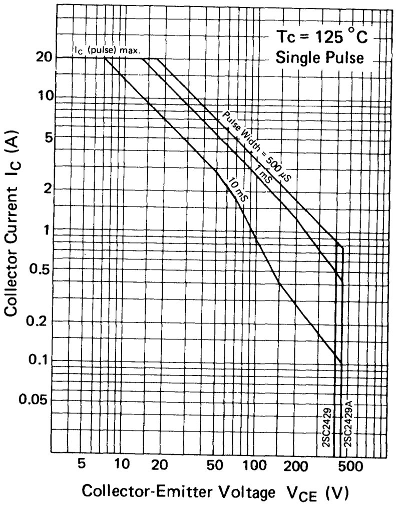
Forward Bias Safe Operating Area



Forward Bias Safe Operating Area



Forward Bias Safe Operating Area



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC2964, 2SC2965

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Rating	Symbol	2SC2964	2SC2965	Unit
Collector to Emittor Voltage	V_{CEO}	400	450	V
Collector Base Voltage	V_{CBO}	600	600	V
Emitter to Base Voltage	V_{EBO}	7	7	V
Collector Current-Continuous	I_C	15	15	A
Collector Current-Pulsed ($P_w \leq 10$ mS, D.R. ≤ 2 %)	I_{CP}	20	20	A
Base Current-Continuous	I_B	5	5	A
Collector Power Dissipation ($T_C = 25$ °C)	P_C	150	150	W
Junction Temperature	T_j	175	175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

Parameters	Symbols	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1$ mA, $I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1$ mA, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 0.8$ A, $R_{BE} = \infty\Omega$ 2SC2964	400	–	–	V
		2SC2965	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 8$ A, $I_{B2} = -1$ A, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500$ V, $I_E = 0$	–	–	100	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6$ V, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5$ V, $I_C = 10$ A (*2)	7	8.5	20	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10$ A, $I_B = 2$ A (*2)	–	0.75	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.25	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10$ V, $I_E = 0$, $f = 1$ MHz	–	230	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10$ V, $I_C = 2$ A	–	28	–	MHz
Rise Time	t_r	$V_{CC} = 150$ V $I_C = 10$ A, $I_{B1} = -I_{B2} = 2$ A (*1)	–	0.15	0.5	μs
Storage Time	t_{stg}		–	0.84	1.0	μs
Fall Time	t_f		–	0.10	0.3	μs

*1 Test Circuit

*2 Pulsed $P_w \leq 300$ μs, Duty Ratio ≤ 6 %

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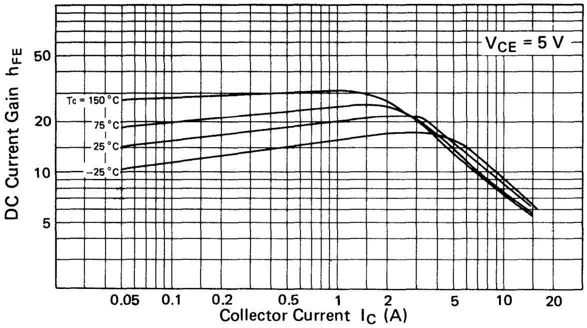
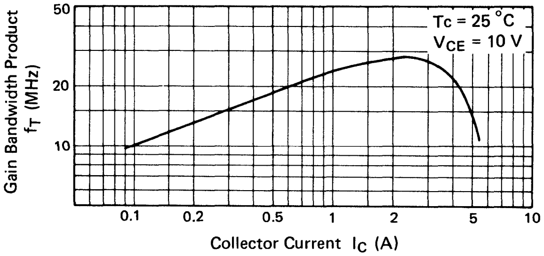
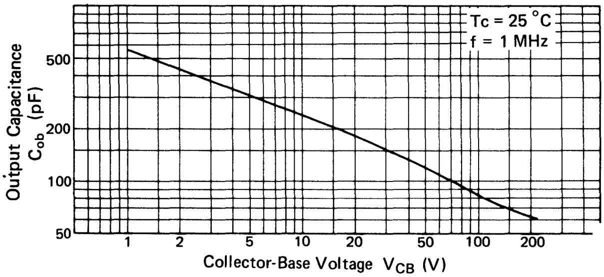
DC Current Gain



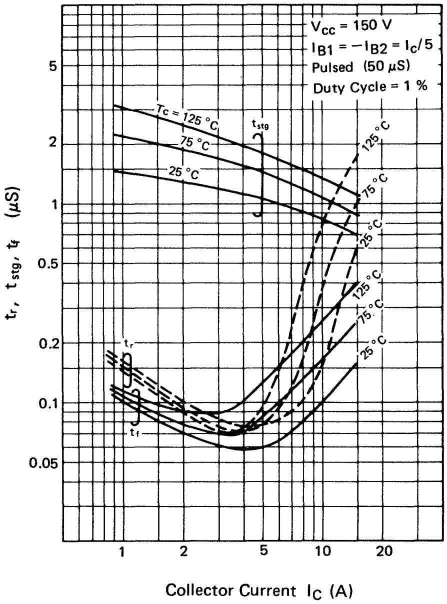
Gain Bandwidth Product



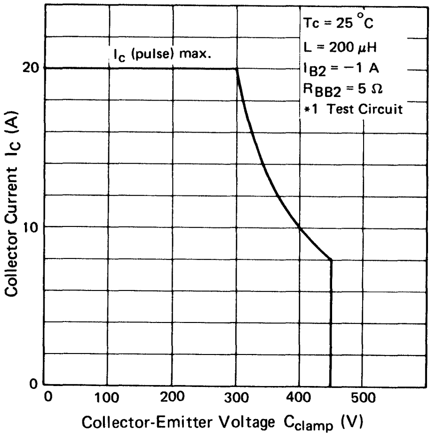
Output Capacitance



Switching Time



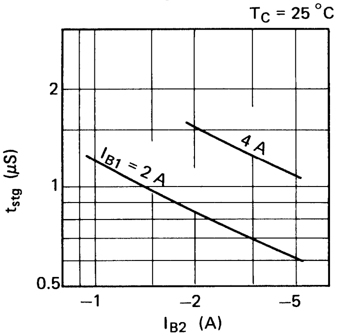
Reverse Bias Safe Operating Area



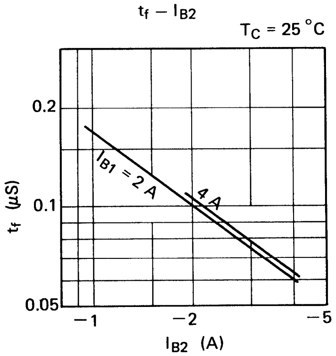
Switching Time

V_{CC} = 150 V
I_C = 10 A
Pulsed (50 μS)
Duty Ratio = 1 %

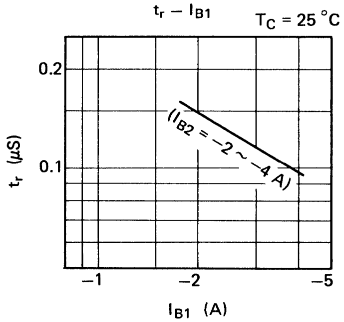
$t_{stg} - I_{B2}$



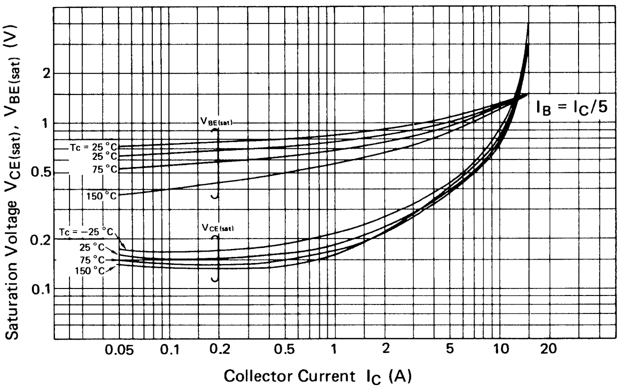
$t_f - I_{B2}$



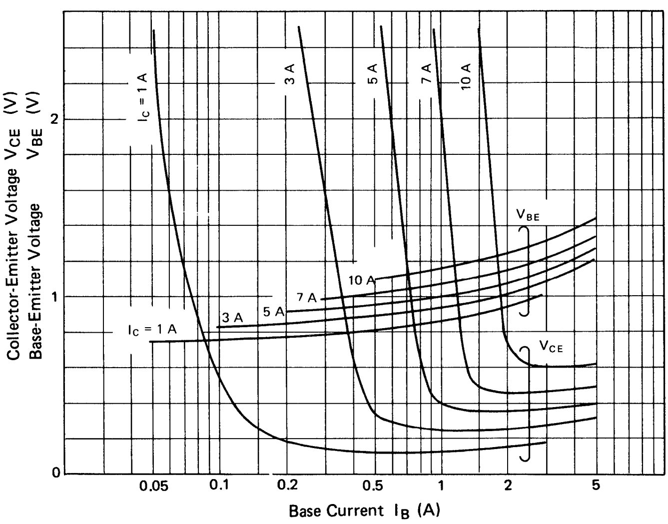
$t_r - I_{B1}$



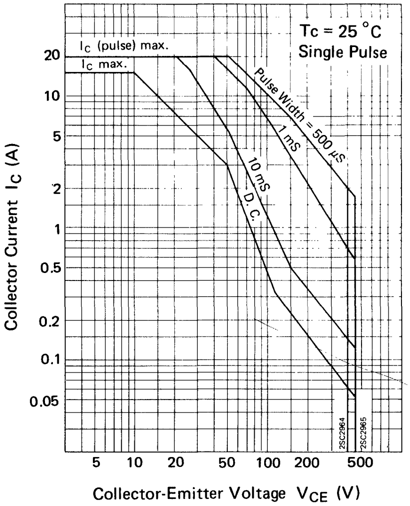
Saturation Voltage



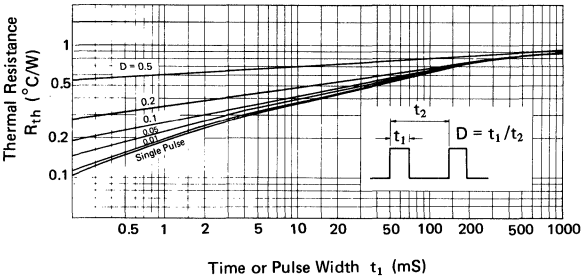
Collector Saturation Region



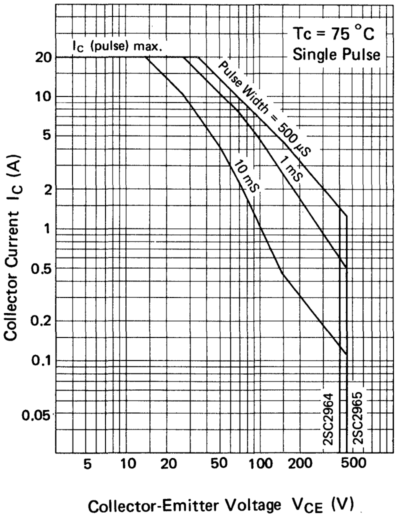
Forward Bias Safe Operating Area



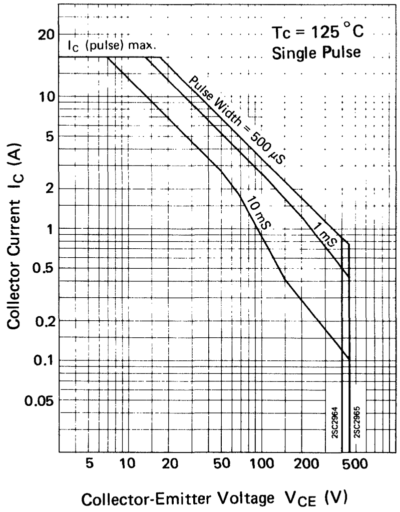
Thermal Response



Forward Bias Safe Operating Area



Forward Bias Safe Operating Area



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3044, 2SC3044A

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3044/2SC3044A are silicon NPN planar general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3044/2SC3044A are especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

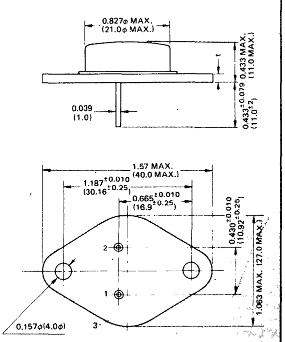
Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		3044	3044A	
Collector to Emitter Voltage	V_{CEO}	400	450	V
Collector to Base Voltage	V_{CBO}	450		V
Emitter to Base Voltage	V_{EBO}	7		V
Collector Current-Continuous	I_C	6		A
Collector Current-Pulsed $P_W \leq 10ms$, D.R. $\leq 2\%$	I_{CP}	15		A
Base Current-Continuous	I_B	4		A
Collector Power Dissipation ($T_C = 25°C$)	P_C	100		W
Junction Temperature	T_j	+175		°C
Storage Temperature Range	T_{stg}	−65 ~ +175		°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	450	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	400 | 450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 2A$, $I_{B2} = -1A$, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 450V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 400V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 3A$ (*2)	10	15	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 3A$, $I_B = 0.6A$ (*2)	–	0.33	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.0	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	100	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–	30	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 3A$, $I_{B1} = -I_{B2} = 0.6A$	–	0.05	0.5	μs
Storage Time	t_{stg}		–	1.25	1.5	μs
Fall Time	t_f		–	0.09	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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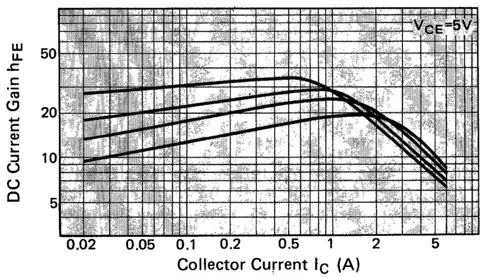
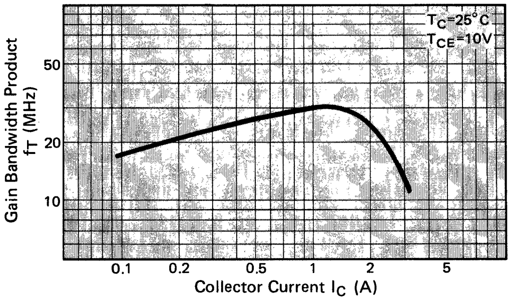
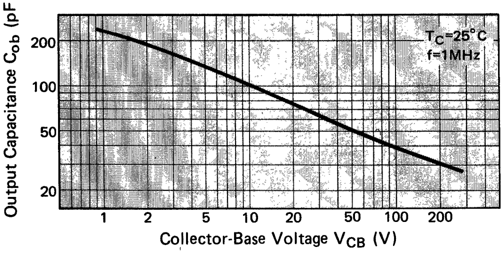


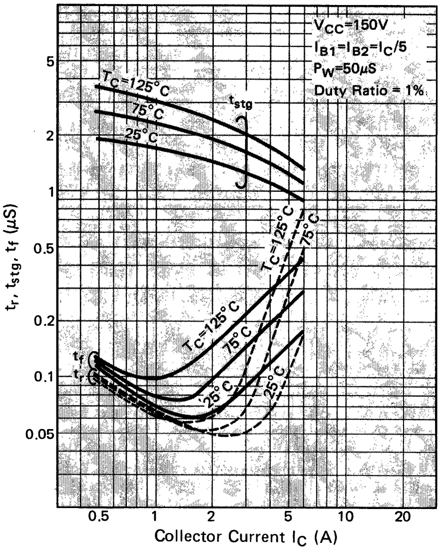
DC CURRENT GAIN



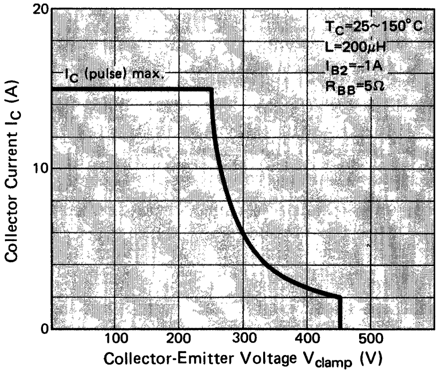
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



SWITCHING TIME

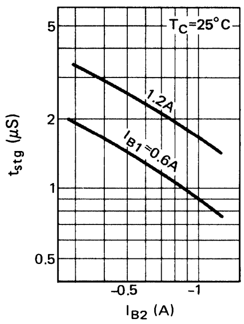


REVERSE BIAS SAFE OPERATING AREA

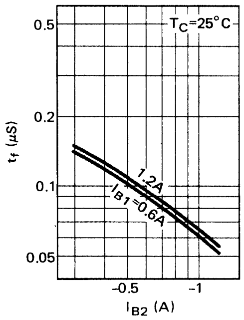
SWITCHING TIME

V_{CC}=150V
I_C=3A
P_W=50μS
Duty Ratio = 1%

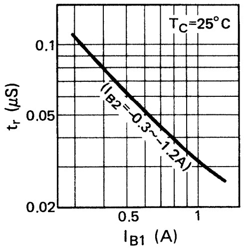
t_{stg}—I_{B2}



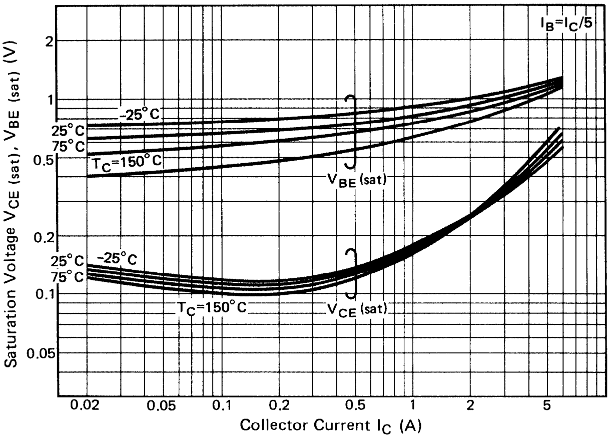
t_f — I_{B2}



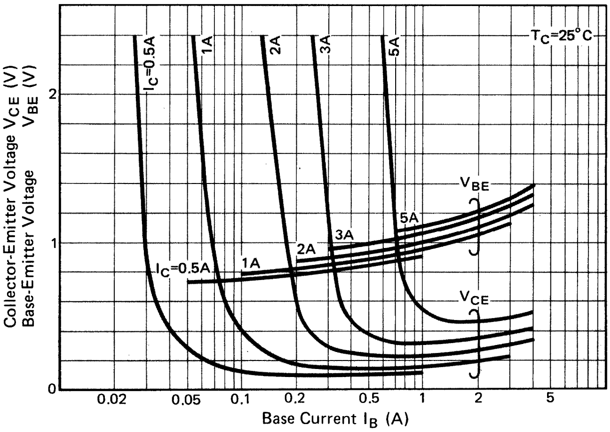
t_r — I_{B1}



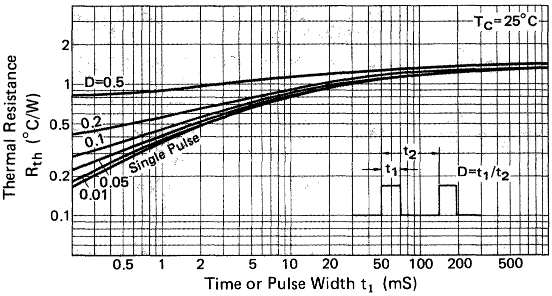
SATURATION VOLTAGE



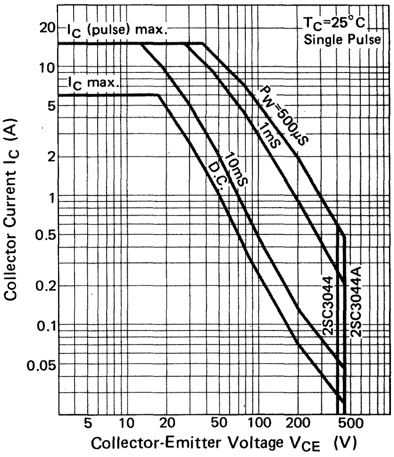
COLLECTOR SATURATION REGION



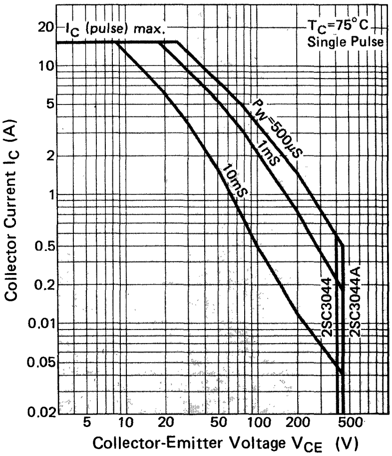
THERMAL RESPONSE



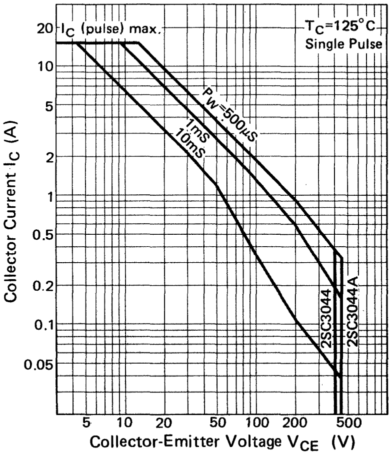
FORWARD BIAS SAFE OPERATING AREA



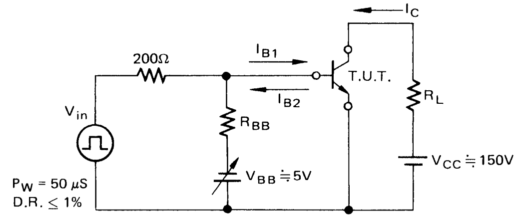
FORWARD BIAS SAFE OPERATING AREA



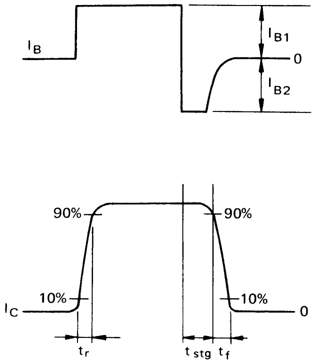
FORWARD BIAS SAFE OPERATING AREA



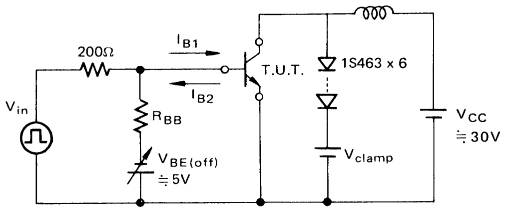
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



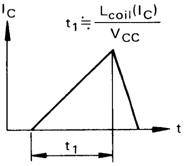
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$

$I_C = 2A, I_{B1} = 1A, I_{B2} = -1A, R_{BB} = 5\Omega, V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area

$I_{B1} \leq 4A, I_{B2} = -1A, R_{BB} = 5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3045

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3045 is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3045 is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

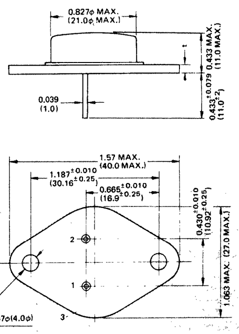
Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	400	V
Collector to Base Voltage	V_{CBO}	450	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	10	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R. $\leq 2\%$	I_{CP}	15	A
Base Current-Continuous	I_B	5	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	100	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	450	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 2A$, $I_{B2} = -1A$, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 450V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 400V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 5A$ (*2)	10	17	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 5A$, $I_B = 1A$ (*2)	–	0.38	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.15	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10A$, $I_E = 0$, $f = 1MHz$	–	100	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–	32	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 5A$, $I_{B1} = -I_{B2} = 1A$	–	0.09	0.5	μs
Storage Time	t_{stg}		–	1.90	2.5	μ
Fall Time	t_f		–	0.14	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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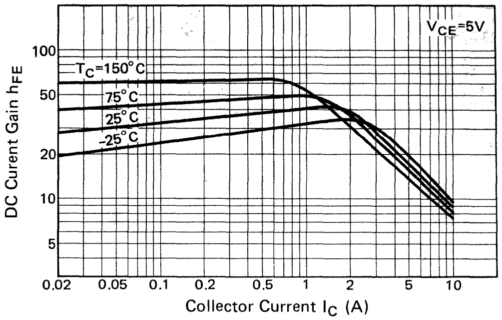
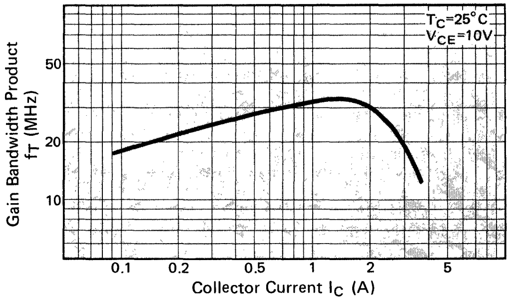
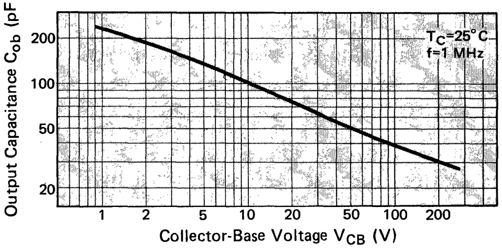
DC CURRENT GAIN



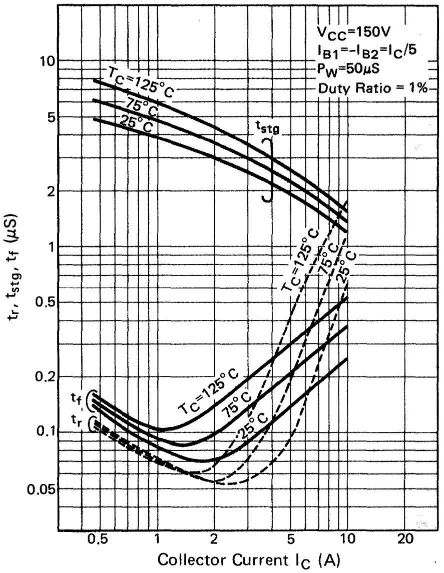
GAIN BANDWIDTH PRODUCT



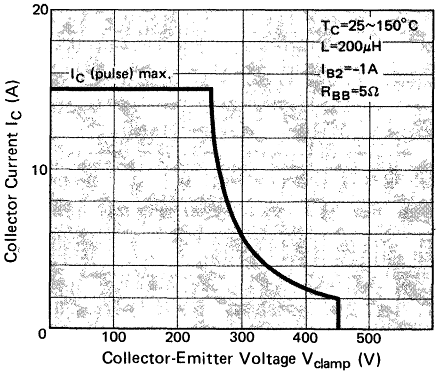
OUTPUT CAPACITANCE



SWITCHING TIME



REVERSE BIAS SAFE OPERATING AREA



SWITCHING TIME

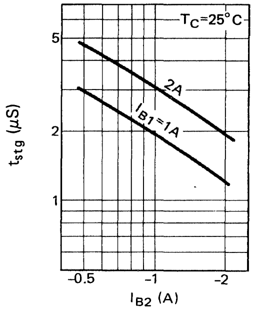
V_{CC}=150V

I_C=5A

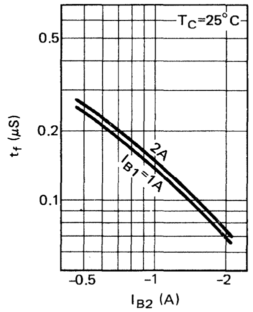
P_W=50μS

Duty Ratio = 1%

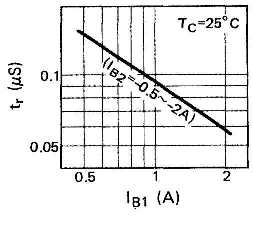
t_{stg}—I_{B2}



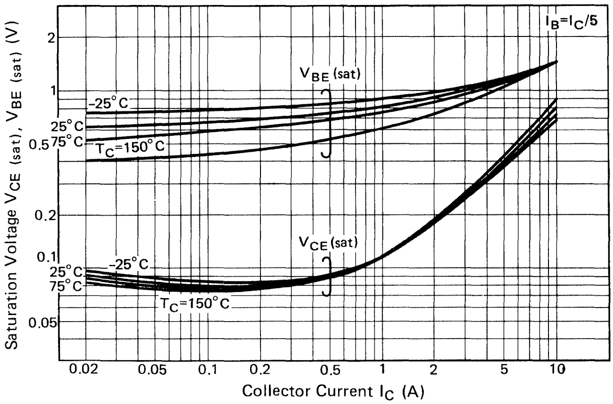
t_f — I_{B2}



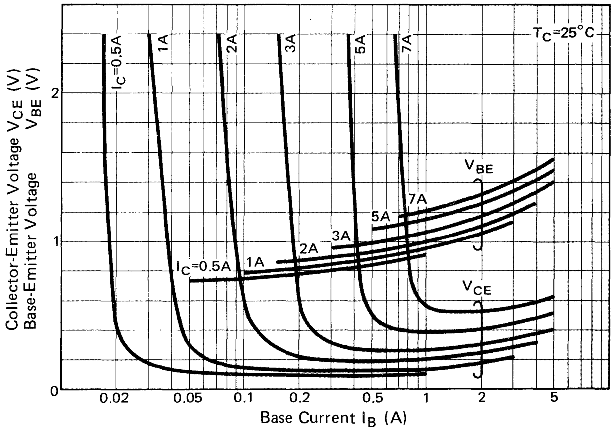
t_r — I_{B1}



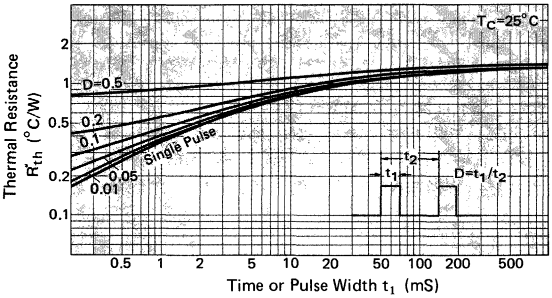
SATURATION VOLTAGE



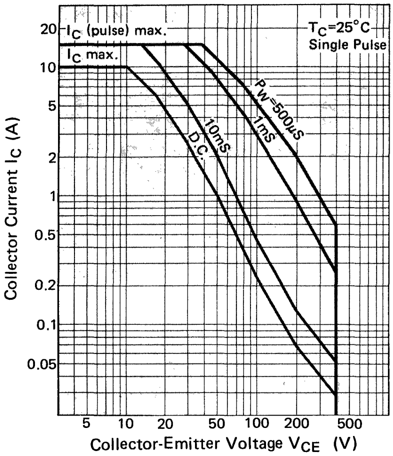
COLLECTOR SATURATION REGION



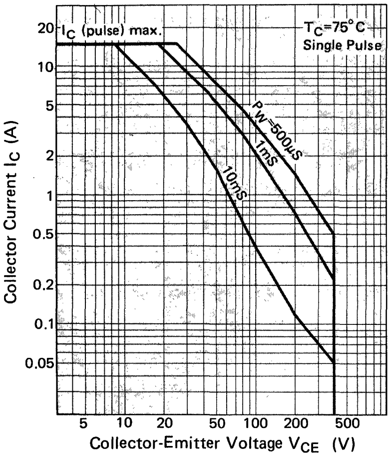
THERMAL RESPONSE



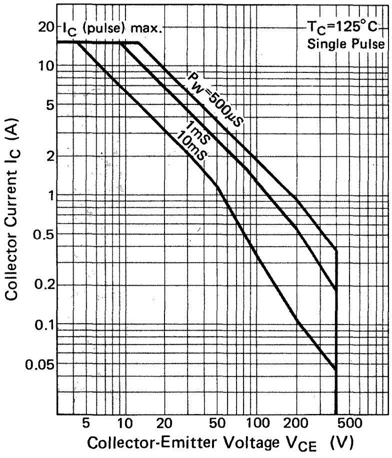
FORWARD BIAS SAFE OPERATING AREA



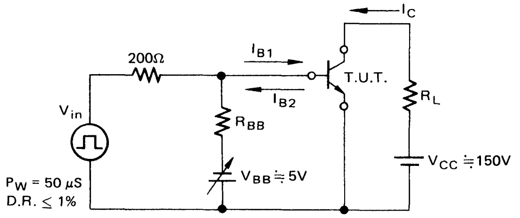
FORWARD BIAS SAFE OPEARTING AREA



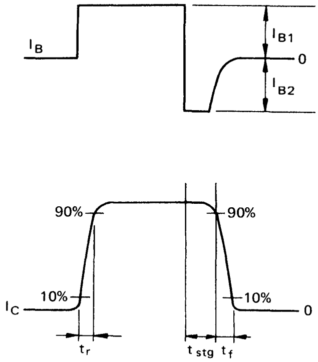
FORWARD BIAS SAFE OPEARTING AREA



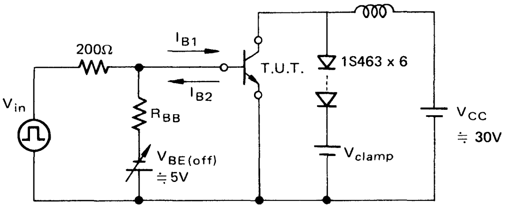
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



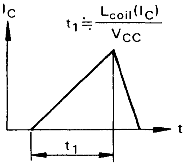
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$
$I_C = 2A$, $I_{B1} = 1A$, $I_{B2} = -1A$, $R_{BB} = 5\Omega$, $V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area
$I_{B1} \leq 4A$, $I_{B2} = -1A$, $R_{BB} = 5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3046

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3046 is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3046 is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

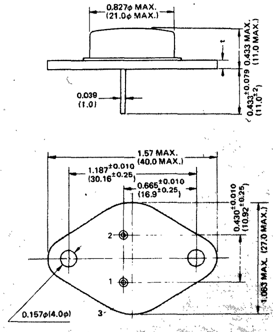
Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	450	V
Collector to Base Voltage	V_{CBO}	600	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	10	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R.$\leq 2\%$	I_{CP}	20	A
Base Current-Continuous	I_B	5	A
Collector Power Dissipation (T_C = 25°C)	P_C	100	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 1mA, I_E = 0	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 1mA, I_C = 0	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	I_C = 0.8A, $R_{BE} = \infty\Omega$	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	I_C = 8A, I_{B2} = –1A, L = 200 μH (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = 500V, I_E = 0	–	–	100	μA
Collector Cutoff Current	I_{CBO}	V_{CB} = 500V, I_E = 0, T_C = 100°C	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 6V, I_C = 0	–	–	100	μA
DC Current Gain	h_{FE}	V_{CE} = 5V, I_C = 6A (*2)	10	14	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 6A, I_B = 1.2A (*2)	–	0.43	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.05	1.5	V
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz	–	230	–	pF
Gain Bandwidth Product	f_T	V_{CE} = 10V, I_C = 2A	–	28	–	MHz
Rise Time	t_r	V_{CC} = 150V (*1) I_C = 6A, I_{B1} = $-I_{B2}$ = 1.2A	–	0.08	0.3	μs
Storage Time	t_{stg}		–	1.25	1.5	μs
Fall Time	t_f		–	0.07	0.2	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300$ μs, Duty Ratio $\leq 6\%$

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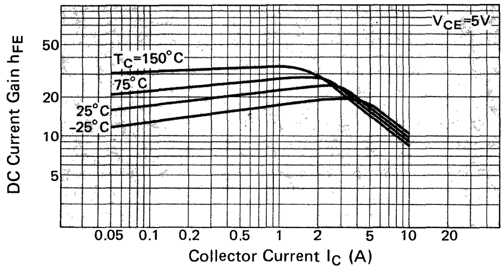
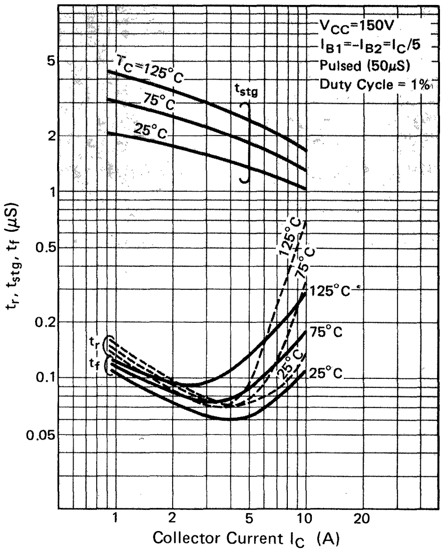
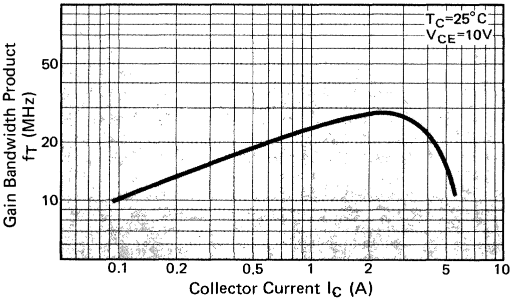
DC CURRENT GAIN



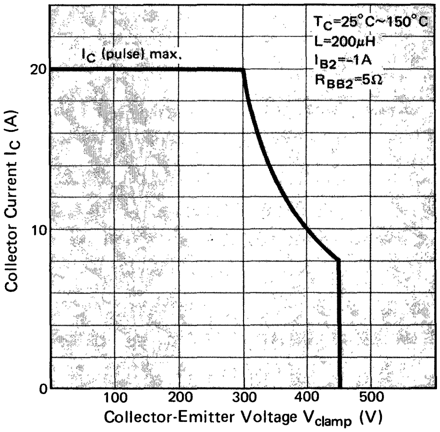
SWITCHING TIME



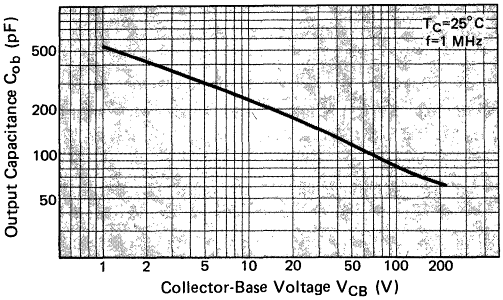
GAIN BANDWIDTH PRODUCT



REVERSE BIAS SAFE OPERATING AREA



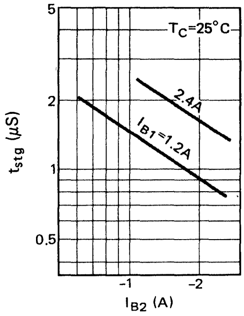
OUTPUT CAPACITANCE



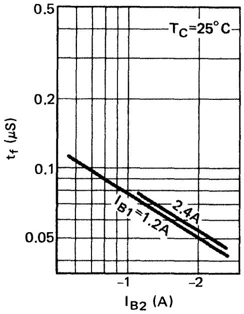
SWITCHING TIME

V_{CC}=150V
I_C=6A
Pulsed (50μS)
Duty Ratio ≈ 1%

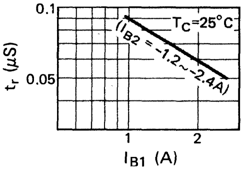
t_{stg}—I_{B2}



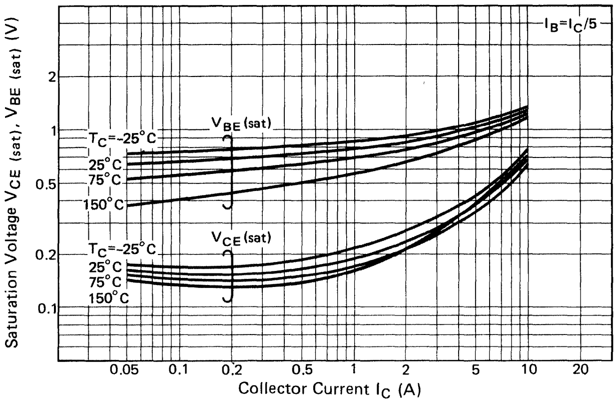
t_f — I_{B2}



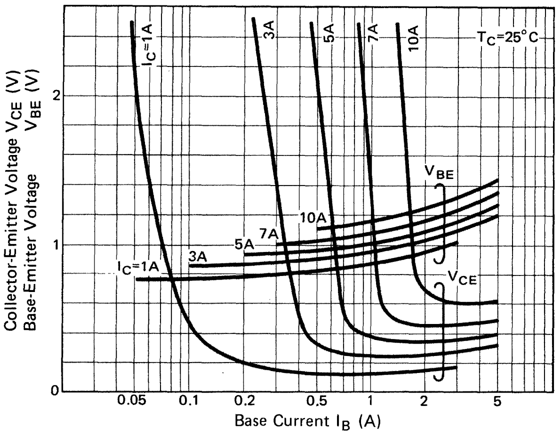
t_r —I_{B1}



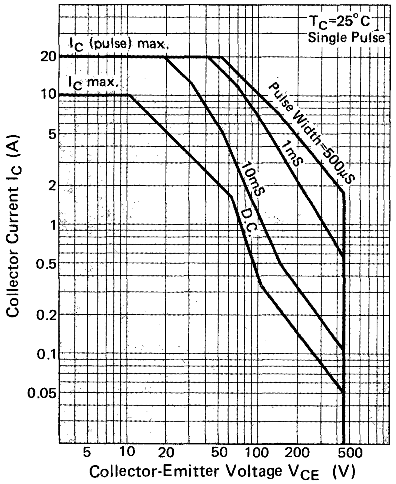
SATURATION VOLTAGE



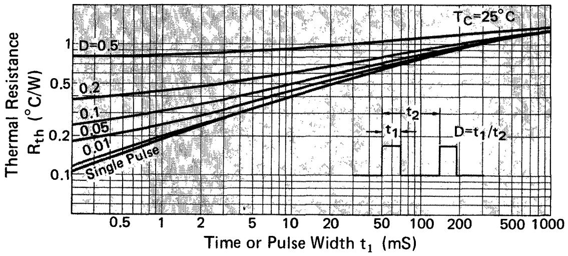
COLLECTOR SATURATION REGION



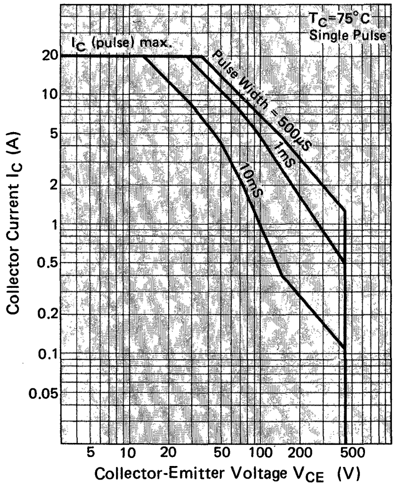
FORWARD BIAS SAFE OPEARTING AREA



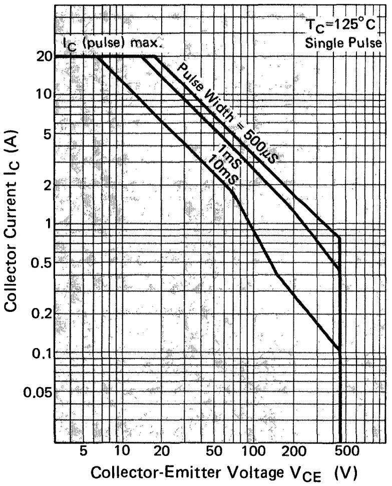
THERMAL RESPONSE



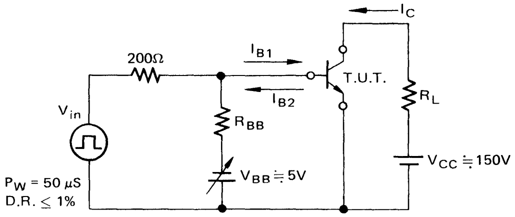
FORWARD BIAS SAFE OPEARTING AREA



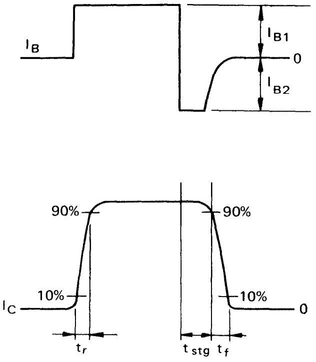
FORWARD BIAS SAFE OPERATING AREA



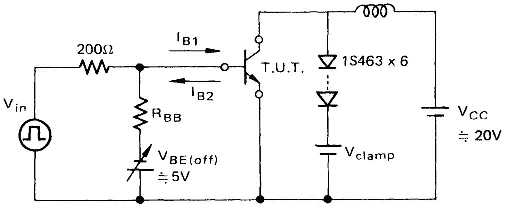
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



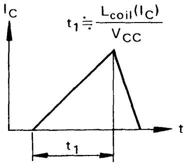
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$

$I_C = 8A$, $I_{B1} = 2A$, $I_{B2} = -1A$, $R_{BB} = 5\Omega$, $V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area

$I_{B1} \leq 4A$, $I_{B2} = -1A$, $R_{BB} = 5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3055

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3055 is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3055 is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

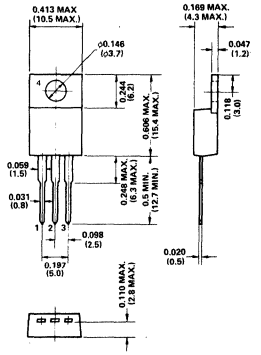
Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic oscillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	400	V
Collector to Base Voltage	V_{CBO}	450	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	2	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R.$\leq 2\%$	I_{CP}	4	A
Base Current-Continuous	I_B	1	A
Collector Power Dissipation (T_C = 25°C)	P_C	15	W
Junction Temperature	T_j	+150	°C
Storage Temperature Range	T_{stg}	-55 ~ +150	°C

OUTLINE DIMENSION
JEDEC TO-220



1: Base 2: Collector
3: Emitter 4: Fin (Collector)
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 1mA, I_E = 0	450	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	I_C = 0.5A, $R_{BE} = \infty\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	I_C = 1A, I_{B2} = -0.2A, L = 200 μH (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = 400V, I_E = 0	–	–	10	μA
Collector Cutoff Current	I_{CBO}	V_{CB} = 400V, I_E = 0, T_C = 100°C	–	–	500	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 6V, I_C = 0	–	–	10	μA
DC Current Gain	h_{FE1}/h_{FE2}	V_{CE} = 5V, I_C = 0.1A/0.5A (*2)	20/10	35/-	80/-	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 0.5A, I_B = 0.1A (*2)	–	0.45	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.1	1.2	V
Output Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1 MHz	–	25	–	pF
Gain Bandwidth Product	f_T	V_{CE} = 10V, I_C = 0.2A	–	28	–	MHz
Rise Time	f_r	V_{CC} = 150V (*1) I_C = 0.5A, I_{B1} = $-I_{B2}$ = 0.1A	–	0.06	0.5	μs
Storage Time	t_{stg}		–	2.00	3.0	μs
Fall Time	t_f		–	0.09	0.3	μs

---

*1 Test Circuit *2 Pulsed $P_W \leqq 300\ \mu s$, Duty Ratio $\leqq 6\%$

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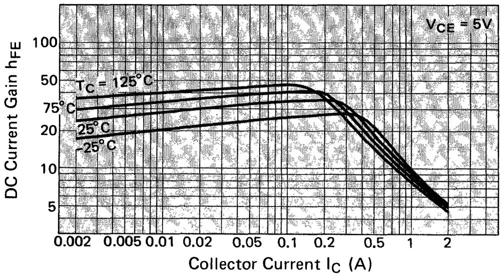
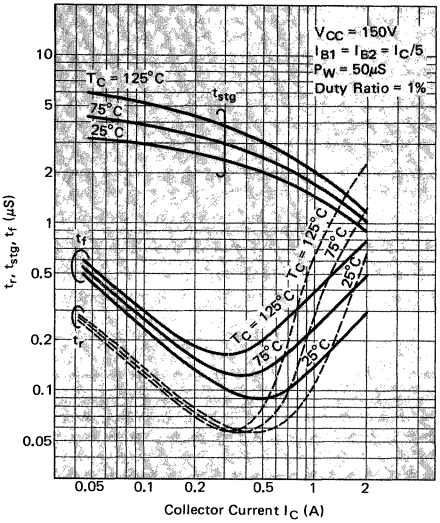
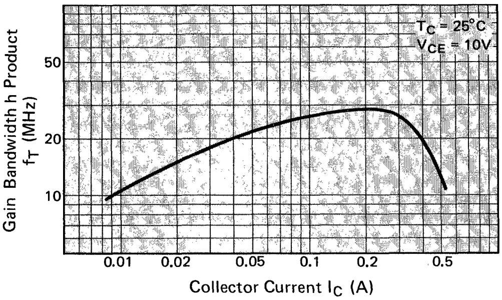
DC CURRENT GAIN



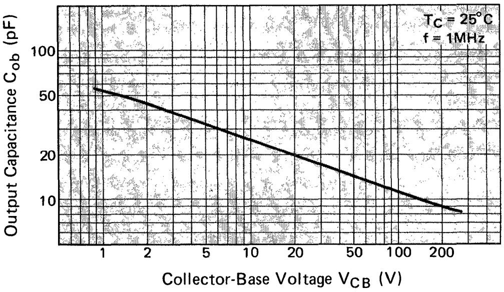
SWITCHING TIME



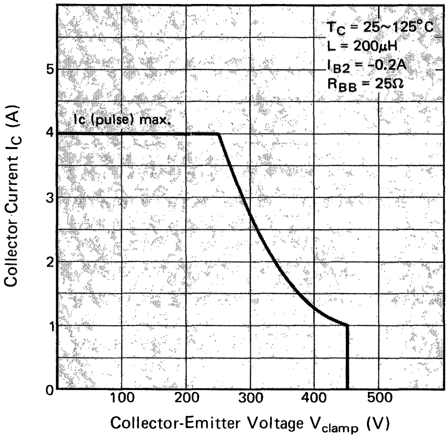
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



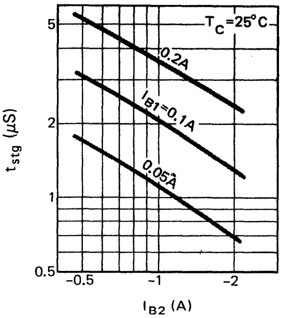
REVERSE BIAS SAFE OPERATING AREA



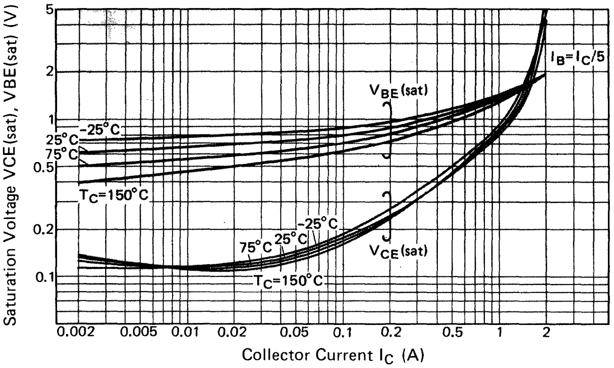
SWITCHING TIME

V_{CC} = 150V
I_C = 0.5A
P_W = 50μS
Duty Ratio = 1%

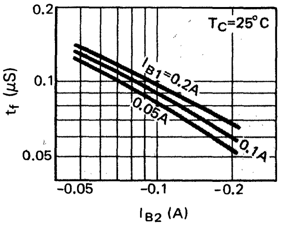
t_{stg}—I_{B2}



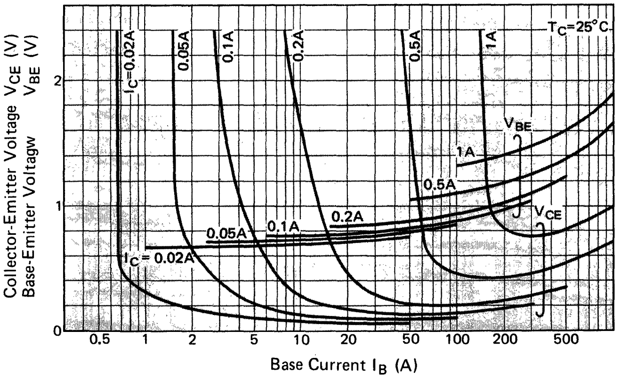
SATURATION VOLTAGE



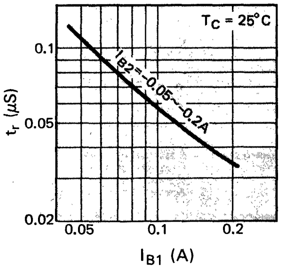
t_f — I_{B2}



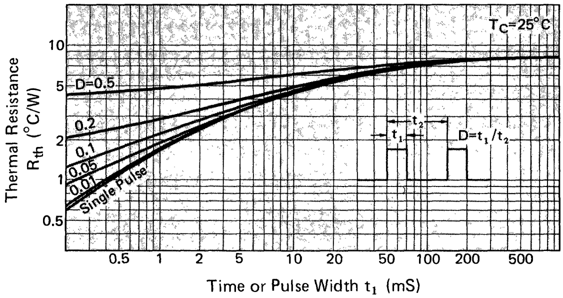
COLLECTOR SATURATION REGION



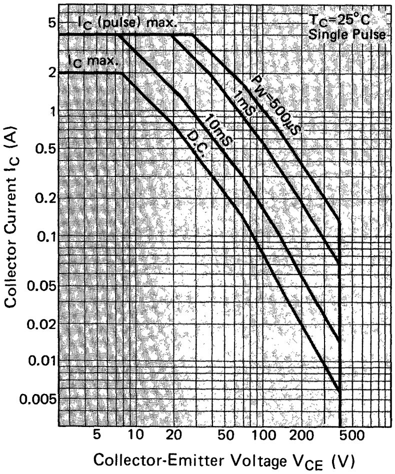
t_r—I_{B1}



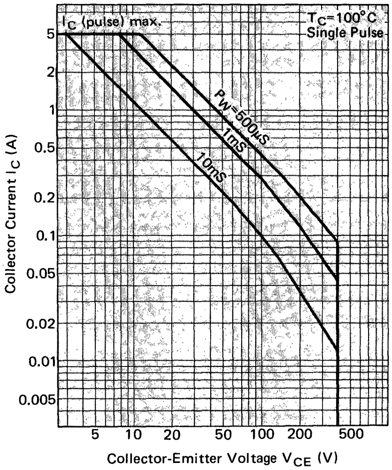
THERMAL RESPONSE



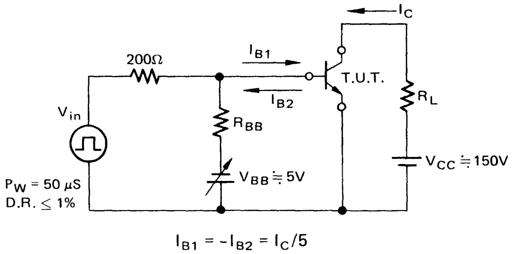
FORWARD BIAS SAFE OPERATING AREA



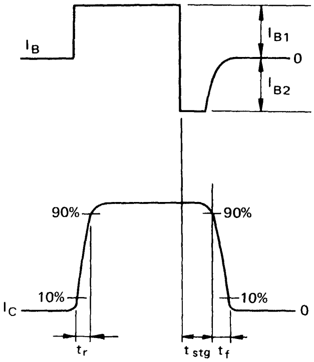
FORWARD BIAS SAFE OPERATING AREA



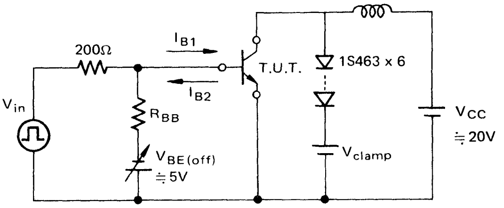
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



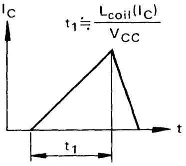
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$
$I_C = 1A$, $I_{B1} = 0.5A$, $I_{B2} = -0.2A$, $R_{BB} = 25\Omega$, $V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area
$I_{B1} \leq 2A$, $I_{B2} = -0.2A$, $R_{BB} = 25\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3056, 2SC3056A

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3056/2SC3056A are silicon NPN planar general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3056/2SC3056A are especially well-suited for high speed/high voltage switching systems or other application where large SOA is required.

Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

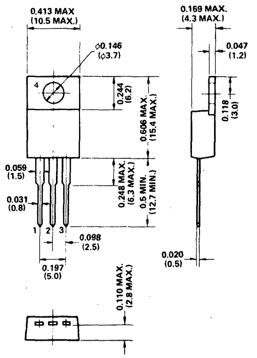
Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		3056	3056A	
Collector to Emitter Voltage	V_{CEO}	400	450	V
Collector to Base Voltage	V_{CBO}	450		V
Emitter to Base Voltage	V_{EBO}	7		V
Collector Current-Continuous	I_C	6		A
Collector Current-Pulsed $P_W \leq 10ms$, D.R.$\leq 2\%$	I_{CP}	15		A
Base Current-Continuous	I_B	4		A
Collector Power Dissipation ($T_C = 25°C$)	P_C	50		W
Junction Temperature	T_j	+150		°C
Storage Temperature Range	T_{stg}	−55 ~ +150		°C

OUTLINE DIMENSION
JEDEC TO-220



1: Base ·2: Collector
3: Emitter 4: Fin (Collector)
Dimension in inches and (milllimeters)

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits				Unit
			Min.		Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	450		–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7		–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	400	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 2A$, $I_{B2} = -1A$, $L = 200\mu H$ (*2)	450		–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 450V$, $I_E = 0$	–		–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 400V$, $I_E = 0$, $T_C = 100°C$	–		–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–		–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 3A$ (*2)	10		15	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 3A$, $I_B = 0.6A$ (*2)	–		0.42	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–		1.0	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–		100	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–		30	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 3A$, $I_{B1} = -I_{B2} = 0.6A$	–		0.05	0.5	μs
Storage Time	t_{stg}		–		1.25	1.5	μs
Fall Time	t_f		–		0.09	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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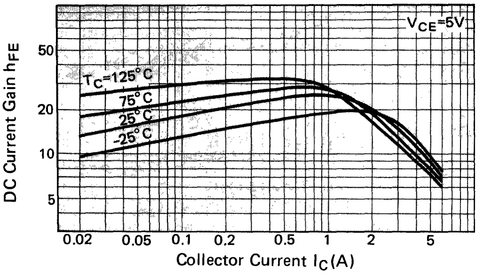
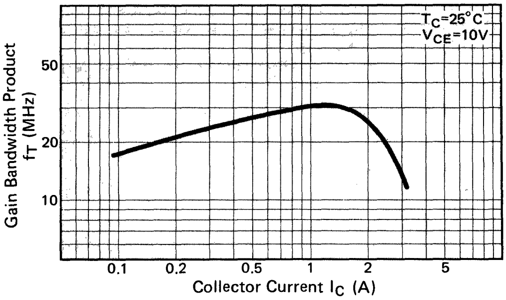
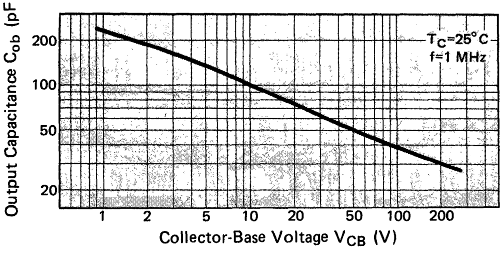
DC CURRENT GAIN



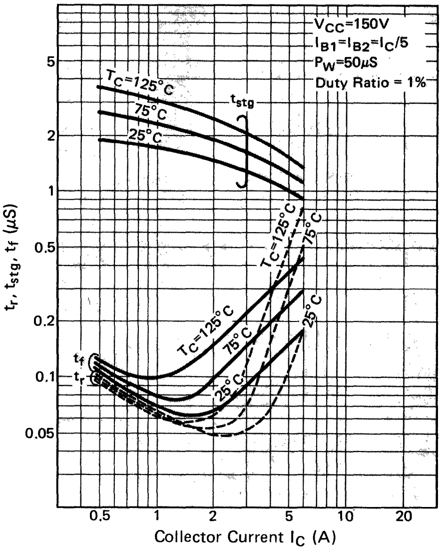
GAIN BANDWIDTH PRODUCT



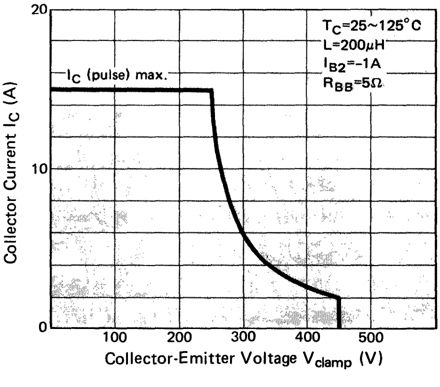
OUTPUT CAPACITANCE



SWITCHING TIME



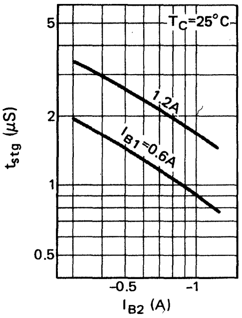
REVERSE BIAS SAFE OPERATING AREA



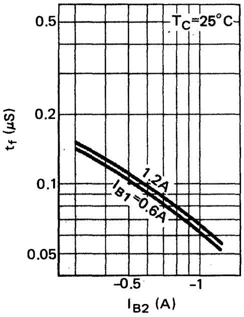
SWITCHING TIME

V_{CC}=150V
I_C=5A
P_W=50μS
Duty Ratio = 1%

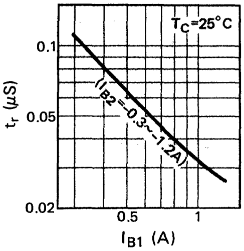
$t_{stg}-I_{B2}$



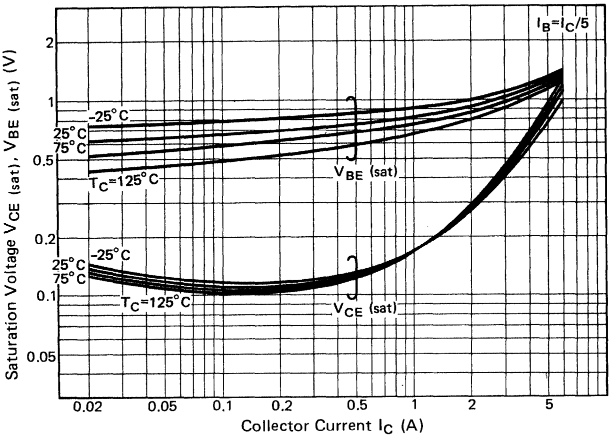
$t_f - I_{B2}$



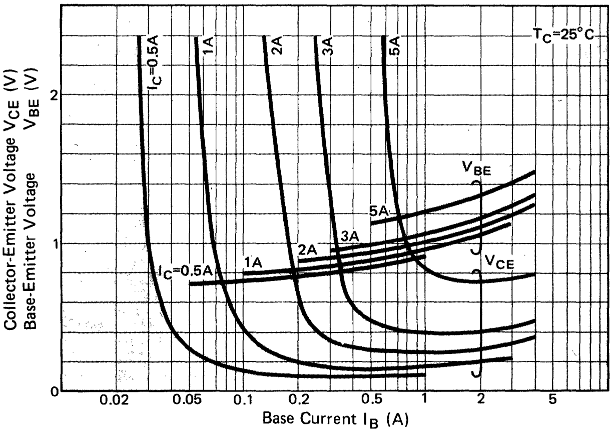
$t_r - I_{B1}$



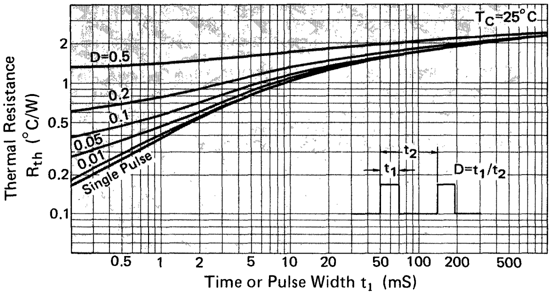
SATURATION VOLTAGE



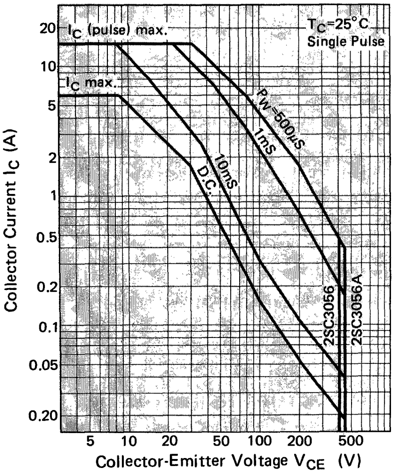
COLLECTOR SATURATION REGION



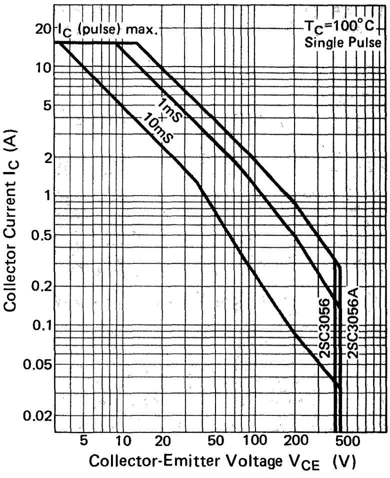
THERMAL RESPONSE



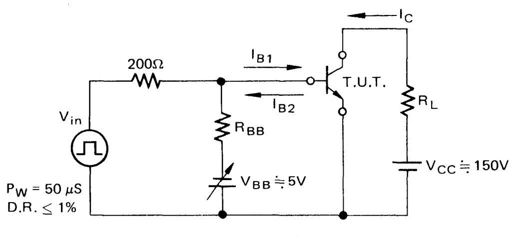
FORWARD BIAS SAFE OPERATING AREA



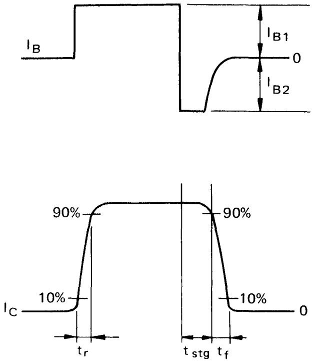
FORWARD BIAS SAFE OPERATING AREA



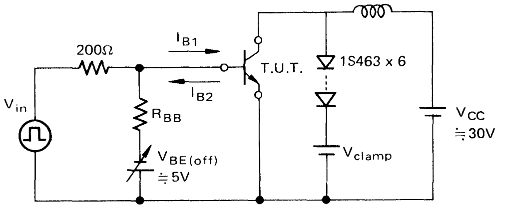
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



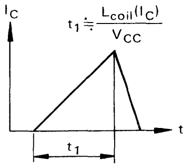
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$
$I_C = 2A,\ I_{B1} = 1A,\ I_{B2} = -1A,\ R_{BB} = 5\Omega,\ V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area
$I_{B1} \leq 4A,\ I_{B2} = -1A,\ R_{BB} = 5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3057

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3057 is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3057 is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

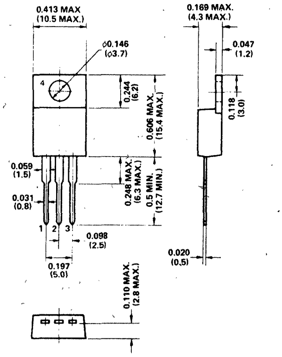
Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	400	V
Collector to Base Voltage	V_{CBO}	450	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	10	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R.$\leq 2\%$	I_{CP}	15	A
Base Current-Continuous	I_B	5	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	50	W
Junction Temperature	T_j	+150	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

OUTLINE DIMENSION JEDEC TO-220



1: Base 2: Collector
3: Emitter 4: Fin (Collector)
Dimension in inches and (millimeters)

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	450	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 2A$, $I_{B2} = -1A$, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 450V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 400V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 5A$ (*2)	10	16	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 5A$, $I_B = 1A$ (*2)	–	0.46	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	100	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–	32	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 5A$, $I_{B1} = -I_{B2} = 1A$	–	0.09	0.5	μs
Storage Time	t_{stg}		–	1.90	2.5	μs
Fall Time	t_f		–	0.14	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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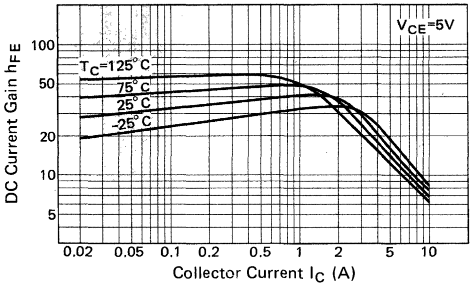
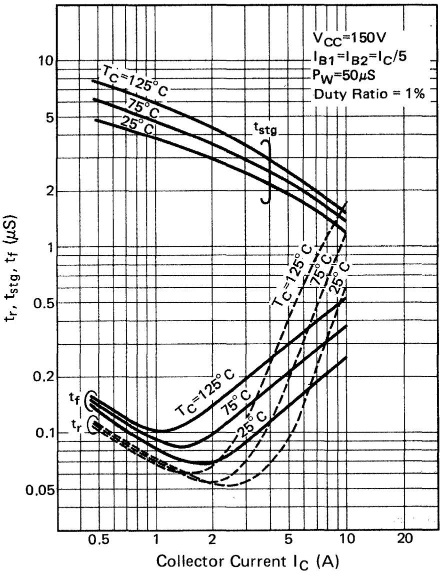
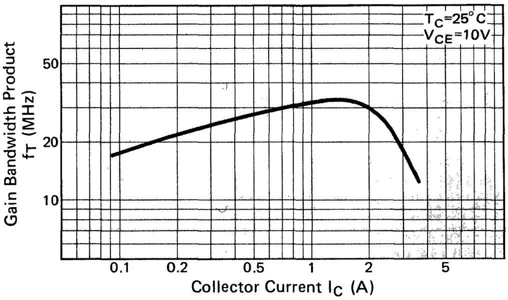
DC CURRENT GAIN



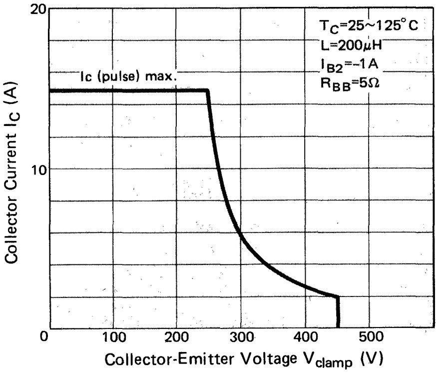
SWITCHING TIME



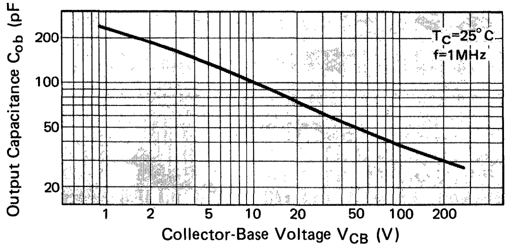
GAIN BANDWIDTH PRODUCT



REVERSE BIAS SAFE OPERATING AREA

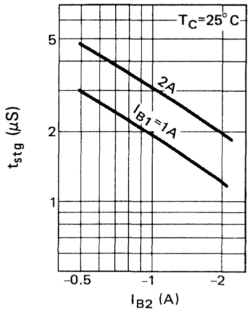


OUTPUT CAPACITANCE

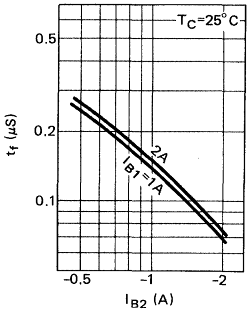


SWITCHING TIME

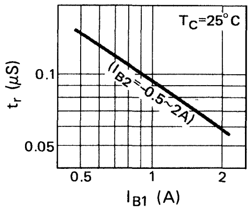
t_{stg}—I_{B2}



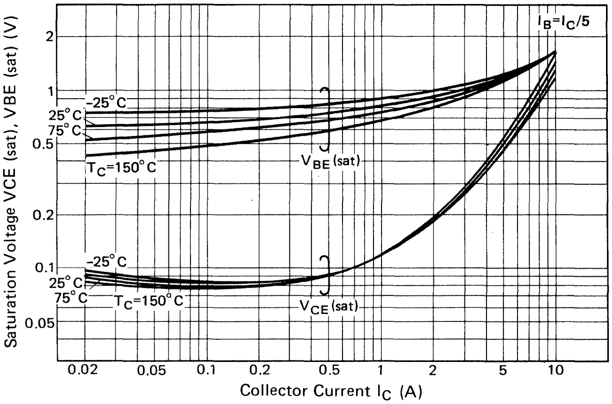
t_f — I_{B2}



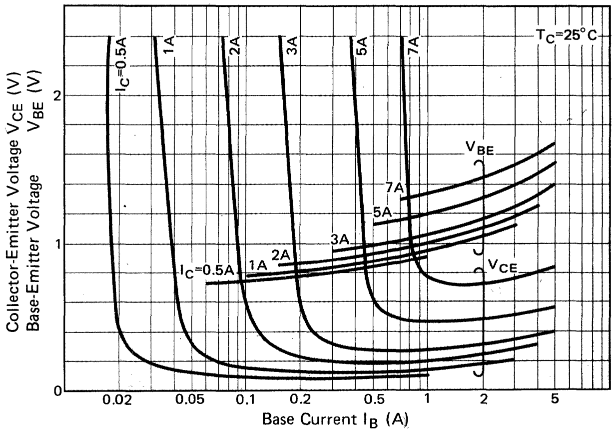
t_r — I_{B1}



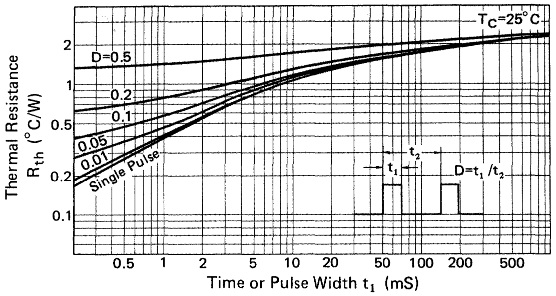
SATURATION VOLTAGE



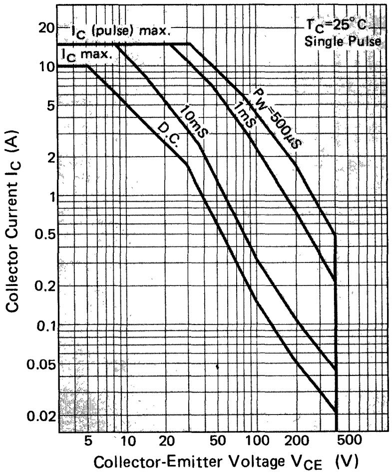
COLLECTOR SATURATION REGION



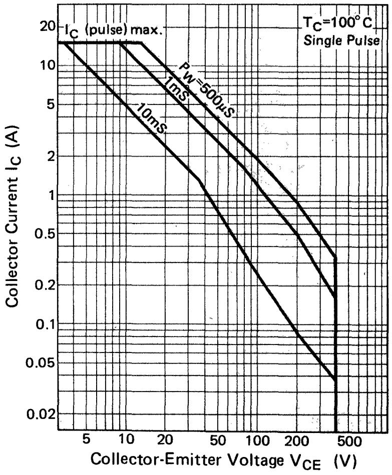
THERMAL RESPONSE



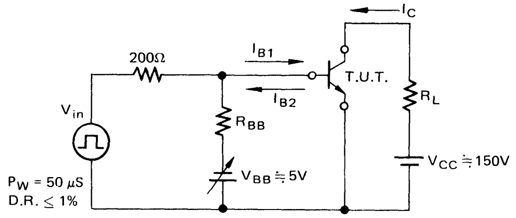
FORWARD BIAS SAFE OPERATING AREA



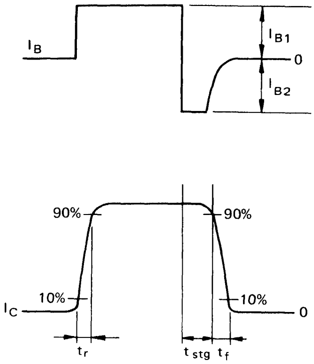
FORWARD BIAS SAFE OPEARTING AREA



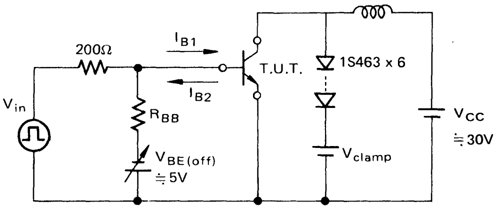
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



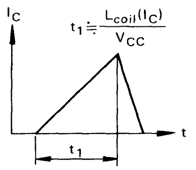
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$

$I_C = 2A,\ I_{B1} = 1A,\ I_{B2} = -1A,\ R_{BB} = 5\Omega,\ V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area

$I_{B1} \leq 4A,\ I_{B2} = -1A,\ R_{BB} = 5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3058

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3058 is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3058 is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

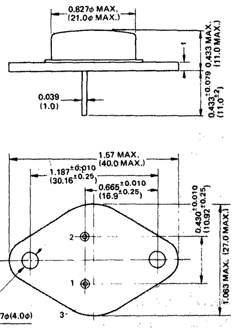
Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

OUTLINE DIMENSION
JEDEC TO–3



1: Base 2: Emitter 3: Collector (Case)
Dimension in inches and (milllimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	400	V
Collector to Base Voltage	V_{CBO}	600	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	30	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R. $\leq 2\%$	I_{CP}	50	A
Base Current-Continuous	I_B	10	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	200	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 10A$, $I_{B2} = -2A$, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V$, $I_E = 0$, $T_C = 100°C$	–	–	2	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6A$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 20A$ (*2)	10	14	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 20A$, $I_B = 4A$ (*2)	–	0.55	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.25	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	420	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 4A$	–	30	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 20A$, $I_{B1} = -I_{B2} = 4A$	–	0.17	0.5	μs
Storage Time	t_{stg}		–	2.10	3.0	μs
Fall Time	t_f		–	0.10	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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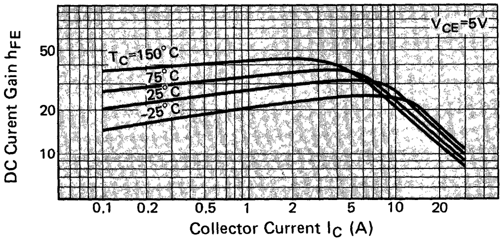
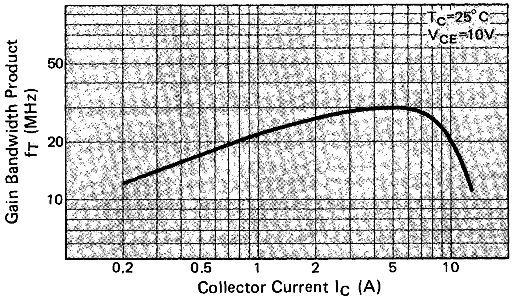
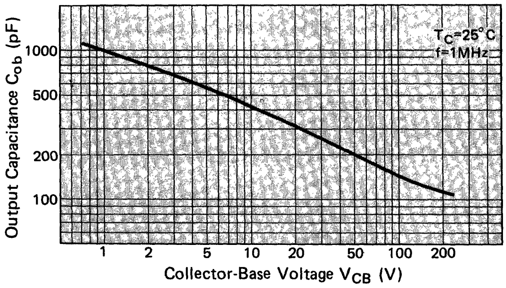
DC CURRENT GAIN



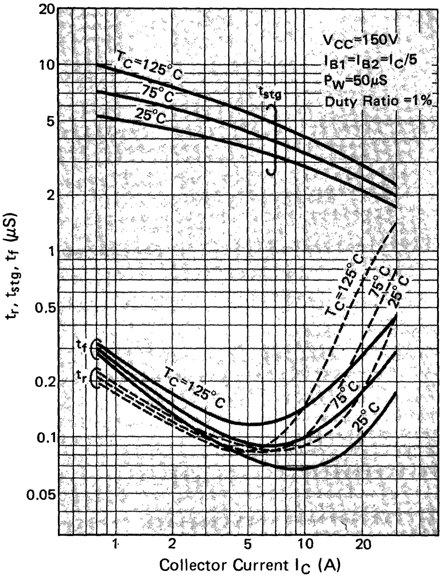
GAIN BANDWIDTH PRODUCT



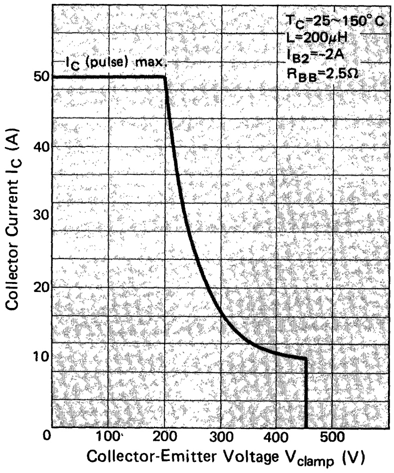
OUTPUT CAPACITANCE



SWITCHING TIME



REVERSE BIAS SAFE OPERATING AREA



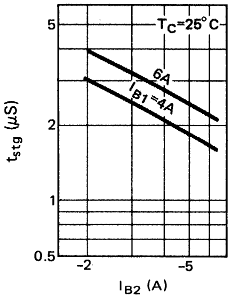
SWITCHING TIME

V_{CC}=150V

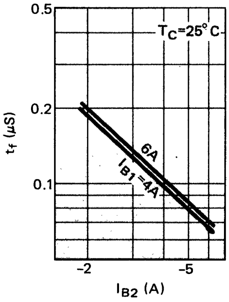
I_C=20A

P_W=50μS

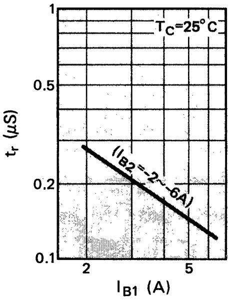
Duty Ratio = 1%



t_{stg}—I_{B2}

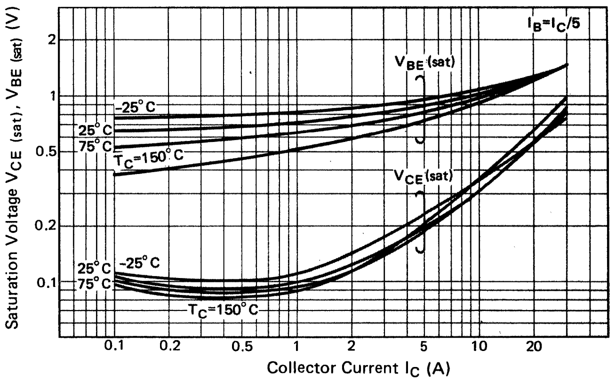


t_f — I_{B2}

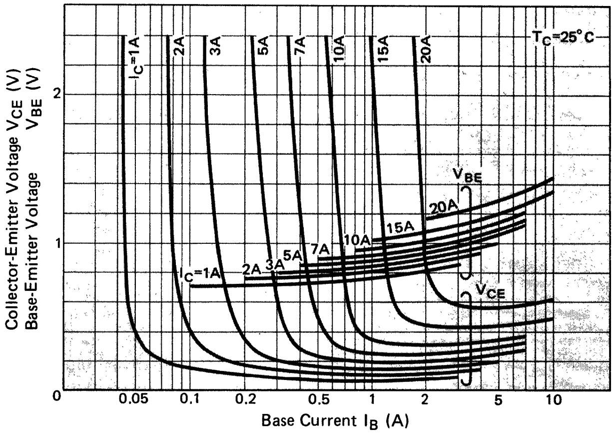


t_r — I_{B1}

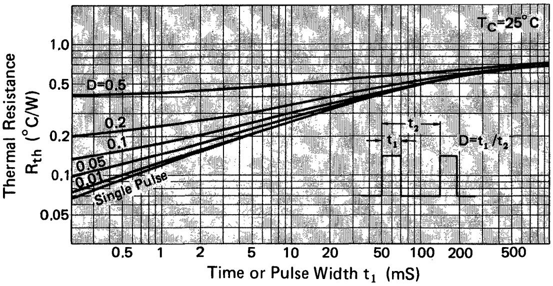
SATURATION VOLTAGE



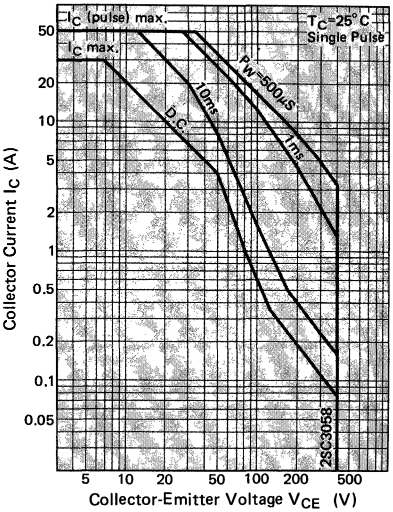
COLLECTOR SATURATION REGION



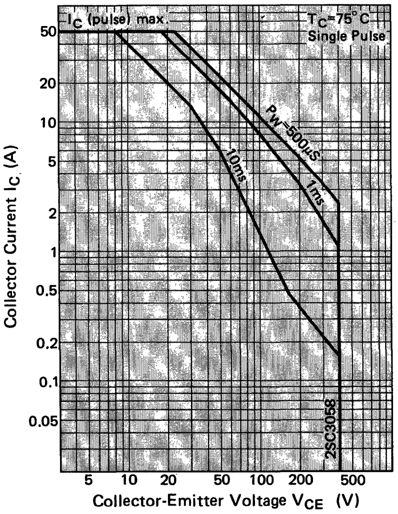
THERMAL RESPONSE



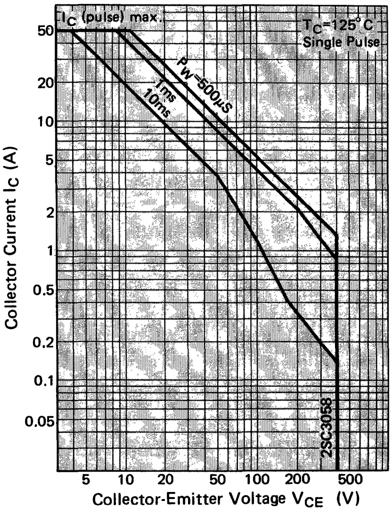
FORWARD BIAS SAFE OPERATING AREA



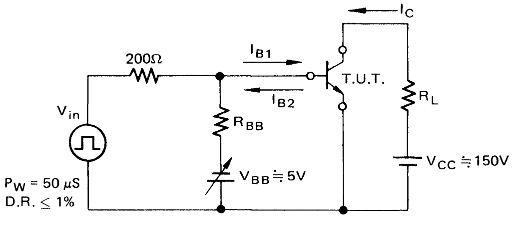
FORWARD BIAS SAFE OPERATING AREA



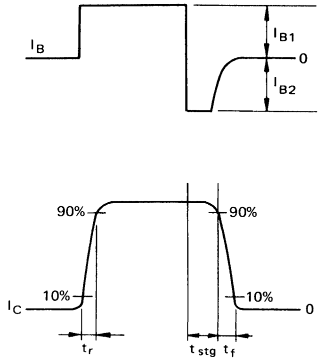
FORWARD BIAS SAFE OPERATING AREA



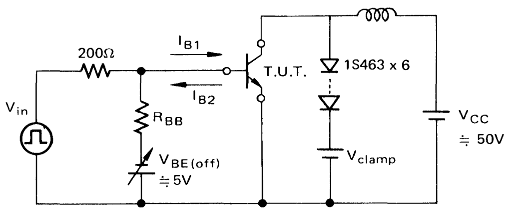
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



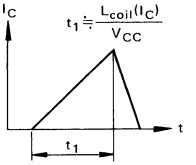
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$
$I_C = 10A$, $I_{B1} = 4A$, $I_{B2} = -2A$, $R_{BB} = 2.5\Omega$, $V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area
$I_{B1} \leq 8A$, $I_{B2} = -2A$, $R_{BB} = 2.5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3058A

Silicon High Speed Power Transistor

DESCRIPTION

The 2SC3058A is a silicon NPN planar general purpose, high power switching transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

The 2SC3058A is especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

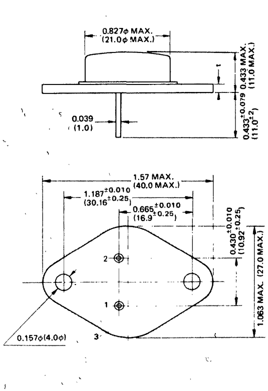
Features

- ★ High voltage
- ★ Ultra-fast switching
- ★ Large safe operating area

Applications

- ★ Switching regulators
- ★ Motor controls
- ★ Ultrasonic osicillators
- ★ Class C and D amplifiers
- ★ Deflection circuits

OUTLINE DIMENSION
JEDEC TO–3



1: Base, 2: Emitter 3: Collector (Case)
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	450	V
Collector to Base Voltage	V_{CBO}	600	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	30	A
Collector Current-Pulsed $P_W \leq 10ms$, D.R.$\leq 2\%$	I_{CP}	50	A
Base Current-Continuous	I_B	10	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	200	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	–65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 10A$, $I_{B2} = -2A$, $L = 200\mu H$ (*1)	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V$, $I_E = 0$, $T_C = 100°C$	–	–	2	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 20A$ (*2)	10	12	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 20A$, $I_B = 4A$ (*2)	–	0.7	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.25	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	420	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 4A$	–	30	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ (*1) $I_C = 20A$, $I_{B1} = -I_{B2} = 4A$	–	0.20	0.5	μs
Storage Time	t_{stg}		–	1.70	2.0	μs
Fall Time	t_f		–	0.10	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

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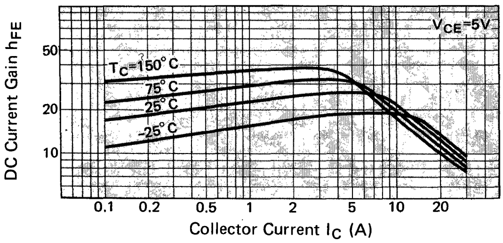
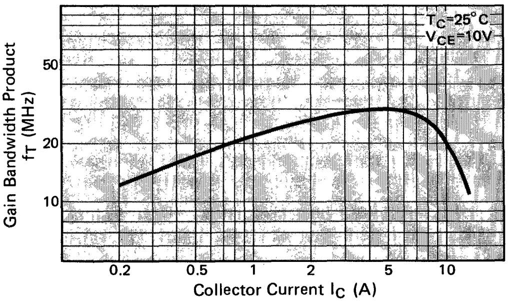
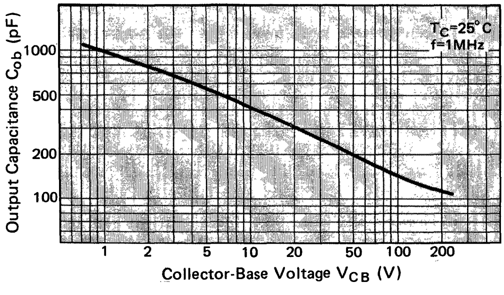
DC CURRENT GAIN



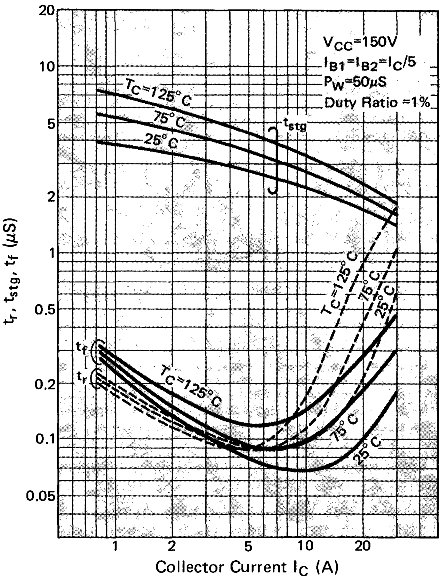
GAIN BANDWIDTH PRODUCT



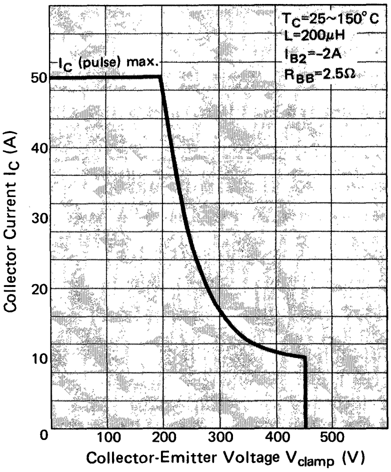
OUTPUT CAPACITANCE



SWITCHING TIME



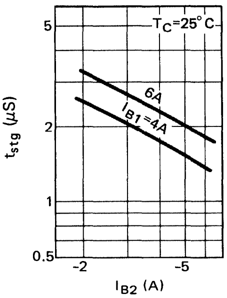
REVERSE BIAS SAFE OPERATING AREA



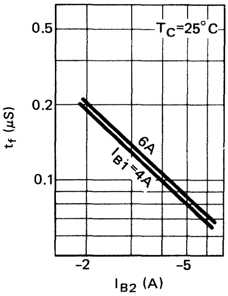
SWITCHING TIME

V_{CC}=150V
I_C=20A
P_W=50μS
Duty Ratio =1%

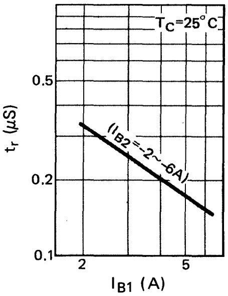
t_{stg}—I_{B2}



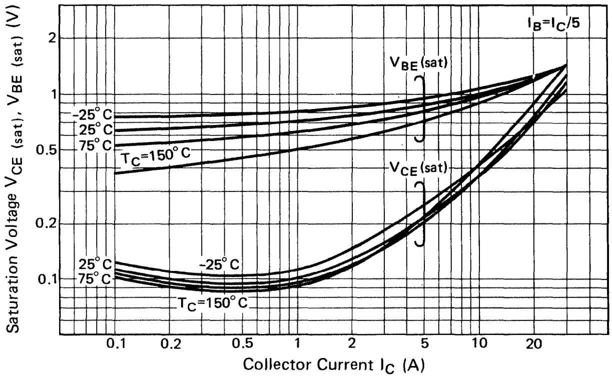
t_f — I_{B2}



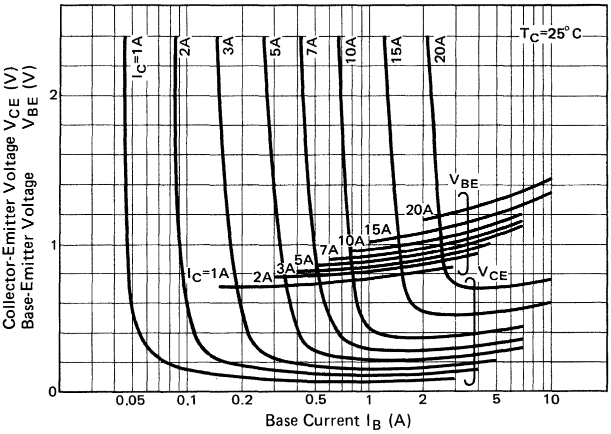
t_r — I_{B1}



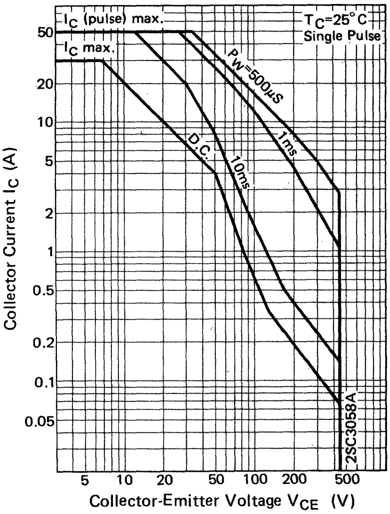
SATURATION VOLTAGE



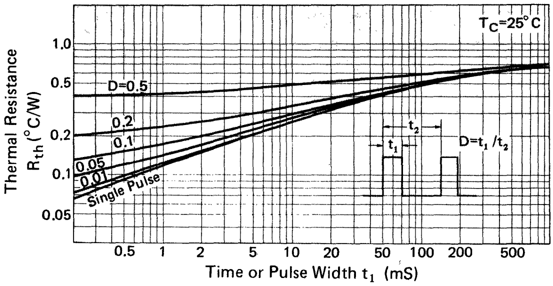
COLLECTOR SATURATION REGION



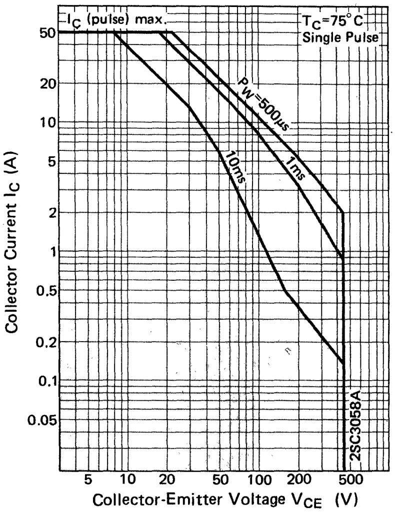
FORWARD BIAS SAFE OPERATING AREA



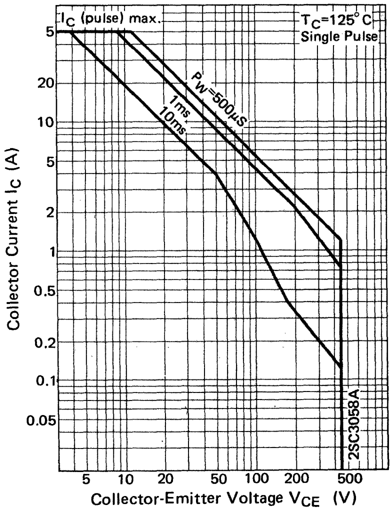
THERMAL RESPONSE



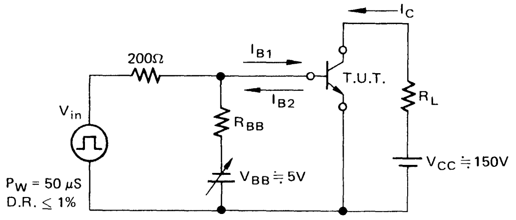
FORWARD BIAS SAFE OPERATING AREA



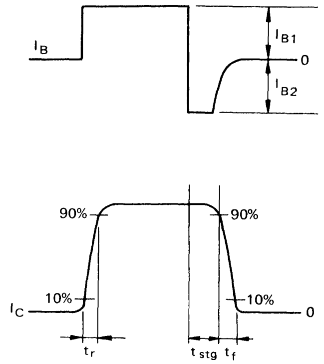
FORWARD BIAS SAFE OPEARTING AREA



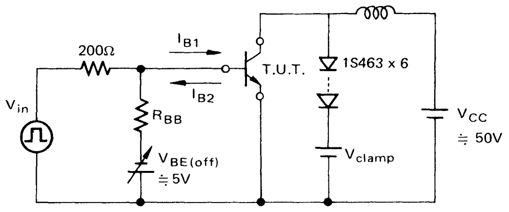
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)



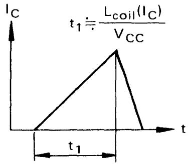
$I_{B1} = -I_{B2} = I_C/5$



TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA



t_1 Adjusted to Obtain I_C



ⓐ $V_{CEX(SUS)}$
$I_C = 10A,\ I_{B1} = 4A,\ I_{B2} = -2A,\ R_{BB} = 2.5\Omega,\ V_{clamp} = 450V$

ⓑ Reverse Bias Safe Operating Area
$I_{B1} \leq 8A,\ I_{B2} = -2A,\ R_{BB} = 2.5\Omega$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3178, 2SC3059, 2SC3060, 2SC3061

Silicon High Speed Power Transistor

DESCRIPTION

This series are silicon NPN planer general purpose, high power switching transistors fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through ballast resistors which provide uniform current density. This structure permits the design of high power transistors with superior switching characteristics and frequency response in high current applications.

This series are especially well-suited for high speed/high voltage switching systems or other applications where large SOA is required.

Features

- High voltage
- Ultra-fast switching
- Large safe operating area

Applications

- Switching regulators
- Motor controls
- Ultrasonic oscillators
- Class C and D amplifiers
- Deflection circuits

Outline of the Series

Item	Symbol	2SC3178	2SC3059	2SC3060	2SC3061	Unit
Collector to Base Breakdown Voltage	V_{CBO}	1200				V
Collector to Emitter Breakdown Voltage	V_{CEO}	850				V
Emitter to Base Breakdown Voltage	V_{EBO}	7				V
Collector Current (continuous)	I_C	2		5	10	A
Collector Current (pulsed)	I_{CP}	4		8	20	A
Collector Power Dissipation	P_C	60	100	150	200	W
Reverse Bias Safe Operating Area @ 900V	RBSOA	2.5		5	7	A
Rise Time (Typ.)	t_r	0.20				μs
Storage Time (Typ.)	t_{stg}	2.50				μs
Fall Time (Typ.)	t_f	0.07				μs
Collector to Emitter Saturation Voltage (Typ.)	$V_{CE(sat)}$	0.3				V
Base to Emitter Saturation Voltage (Typ.)	$V_{BE(sat)}$	1.0				V
Package	–	TO-220	TO-3			–

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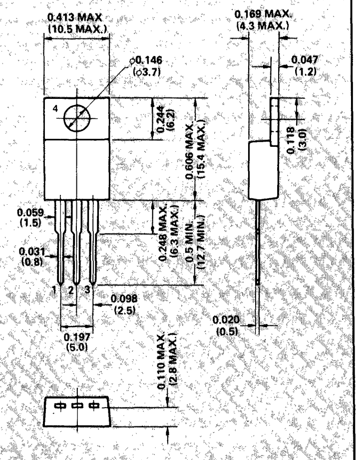
OUTLINE DIMENSION

2SC3178

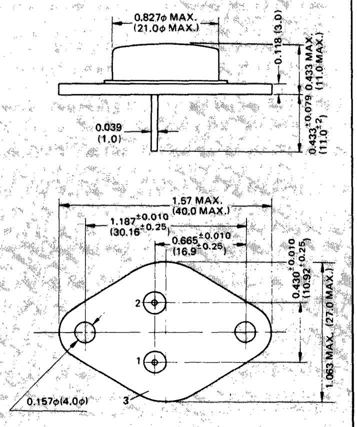
2SC3059
2SC3060
2SC3061

OUTLINE DIMENSION
JEDEC TO-220



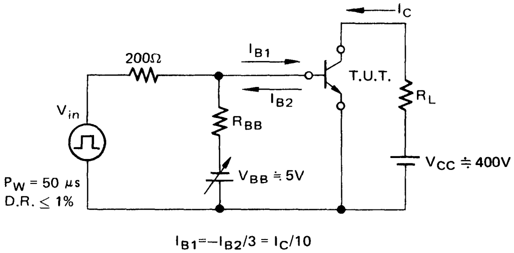
1: Base 2: Collector
3: Emitter 4: Fin (Collector)
Dimensions in inches (millimeters)

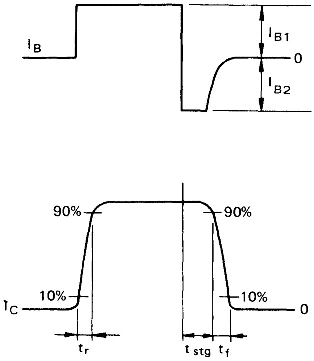
OUTLINE DIMENSION
JEDEC TO-3



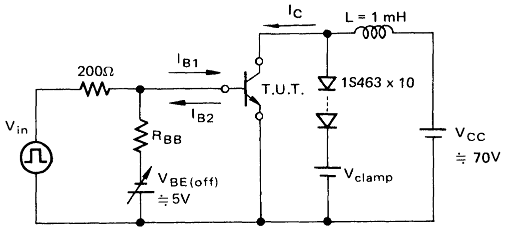
1: Base 2: Emitter 3: Collector (Case)
Dimensions in inches (millimeters)

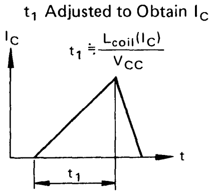
TEST CIRCUIT USED FOR MEASUREMENT OF SWITCHING TIME (RESISTIVE)





TEST CIRCUIT USED FOR MEASUREMENT OF $V_{CEX(SUS)}$ AND REVERSE BIAS SAFE OPERATING AREA





$V_{CEX(SUS)}$

Type No.	I_C (A)	I_{B2}(A)	$R_{BB}(\Omega)$
2SC3178	2.5	-0.3	20
2SC3059			
2SC3060	5.0	-0.6	10
2SC3061	7.0	-1.2	5

V clamp = 900V

REVERSE BIAS SAFE OPERATING AREA

Type No.	I_{B2}(A)	$R_{BB}(\Omega)$
2SC3178	-0.3	20
2SC3059		
2SC3060	-0.6	10
2SC3061	-1.2	5

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3178

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	850	V
Collector to Base Voltage	V_{CBO}	1200	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	2	A
Collector Current-Pulsed $P_W \leqq 25\ \mu s$, D.R.$\leqq 50\%$	I_{CP}	4	A
Base Current-Continuous	I_B	1	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	60	W
Junction Temperature	T_j	+150	°C
Storage Temperature Range	T_{stg}	-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	850	–	–	V
Collector to Emitter Sustaining Voltage	V_{CEX} (SUS)	I_C=2.5A, I_{B2}=−0.3A, L=1mH(*1)	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0, T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V, I_C = 1A$ (*2)	10	15	30	–
Collector to Emitter Saturation Voltage	V_{CE} (sat)	$I_C = 1A, I_B = 0.2A$ (*2)	–	0.3	1.5	V
Base to Emitter Saturation Voltage	V_{BE} (sat)		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	60	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 0.2A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ (*1) $I_C = 1A, 31_{B1} = -I_{B2} = 0.3A$	–	0.2	0.5	μs
Storage Time	t_{stg}		–	2.5	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit *2 Pulse $P_W \leqq 300\ \mu s$, Duty Ratio $\leqq 6\%$

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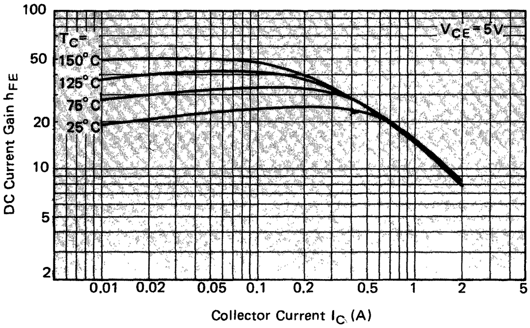
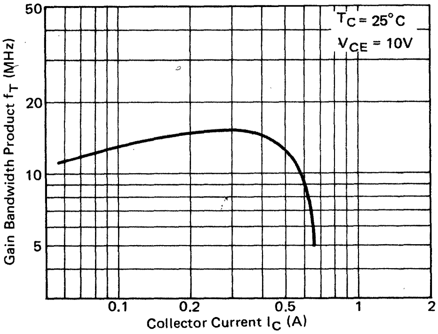
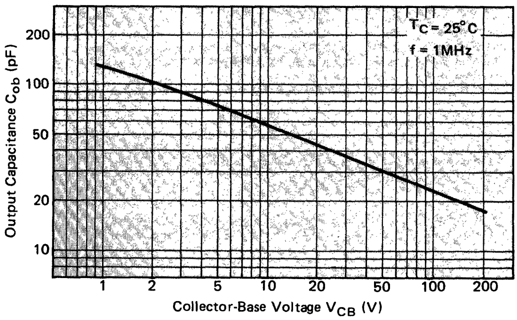
DC CURRENT GAIN



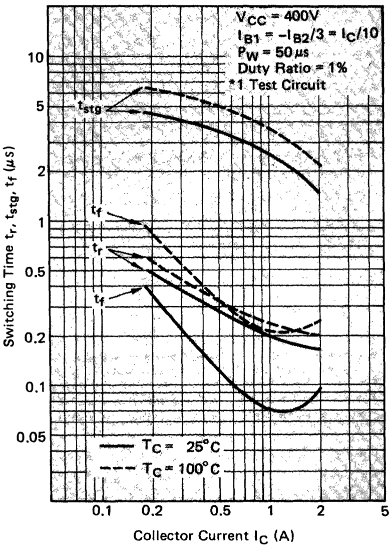
GAIN BANDWIDTH PRODUCT



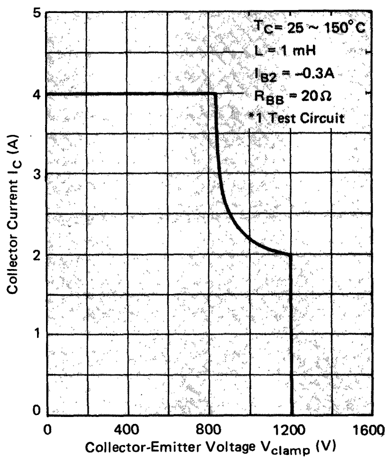
OUTPUT CAPACITANCE



SWITCHING TIME



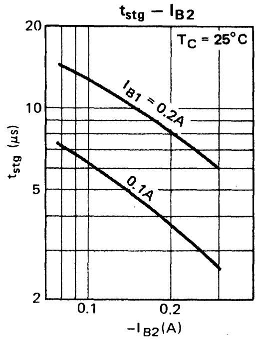
REVERSE BIAS SAFE OPERATING AREA



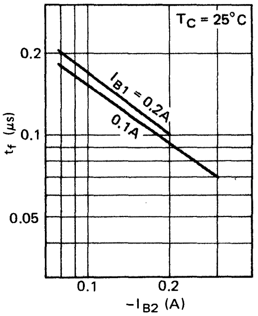
SWITCHING TIME

V_{CC} = 400V
I_C = 1A
P_W = 50 μs
Duty ratio = 1%

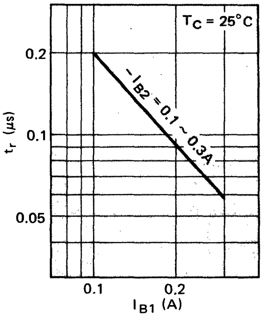
t_{stg} — I_{B2}



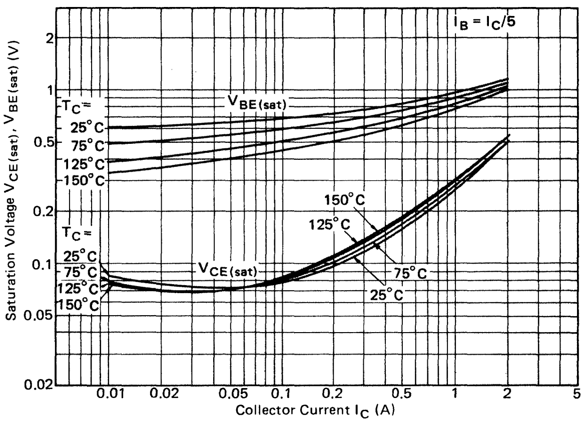
t_f — I_{B2}



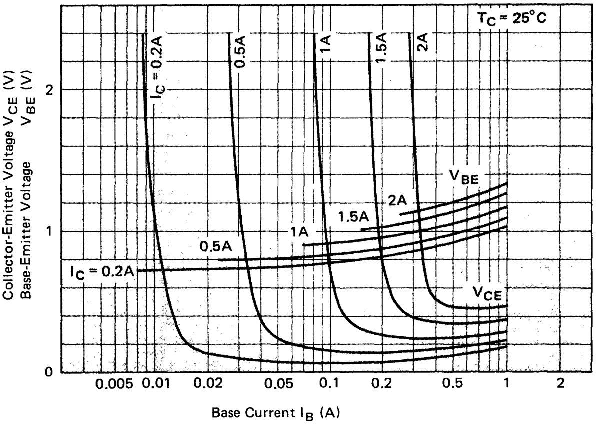
t_r — I_{B1}



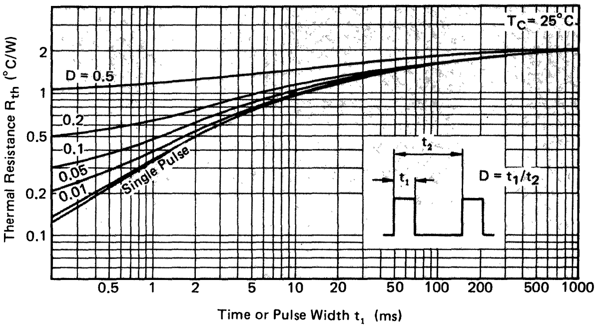
SATURATION VOLTAGE



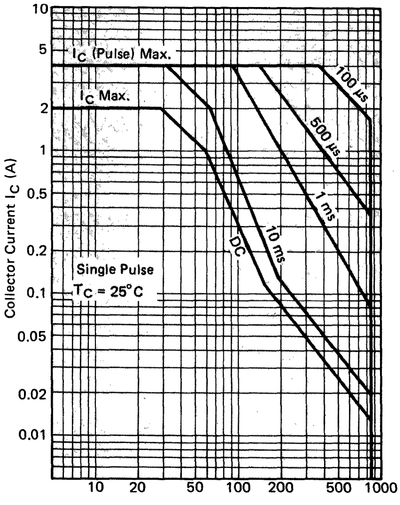
COLLECTOR SATURATION REGION



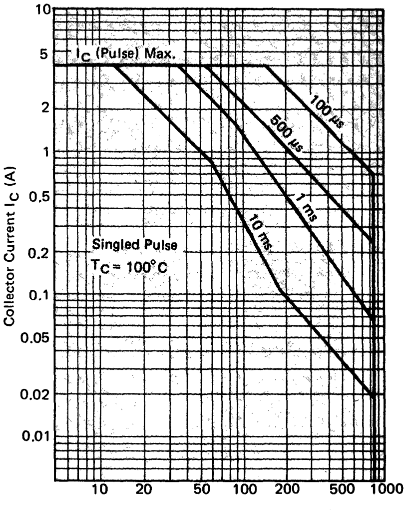
THERMAL RESPONCE



FOWARD BIAS SAFE OPERATING AREA



FOWARD BIAS SAFE OPERATING AREA



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3059

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	850	V
Collector to Base Voltage	V_{CBO}	1200	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	2	A
Collector Current-Pulsed $P_W \leqq 25\,\mu s$, D.R. $\leqq 50\%$	I_{CP}	4	A
Base Current-Continuous	I_B	1	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	100	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	−65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)}CBO$	$I_C = 1mA, I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)}EBO$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)}CEO$	$I_C = 10mA, R_{BE} = \infty\Omega$	850	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX}(SUS)$	I_C=2.5A, I_{B2}=−0.3A, L=1mH(*1)	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0, T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V, I_C = 1A$ (*2)	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE}(sat)$	$I_C = 1A, I_B = 0.2A$ (*2)	–	0.3	1.5	V
Base to Emitter Saturation Voltage	$V_{BE}(sat)$		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E 0, f = 1MHz$	–	60	–	PF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 0.2A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ (*1) $I_C = 1A, 3I_{B1} = -I_{B2} = 0.3A$	–	0.2	0.5	μs
Storage Time	t_{stg}		–	2.5	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leqq 300\,\mu s$, Duty Ratio $\leqq 6\%$

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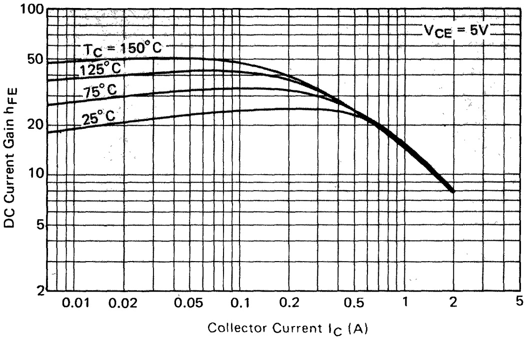
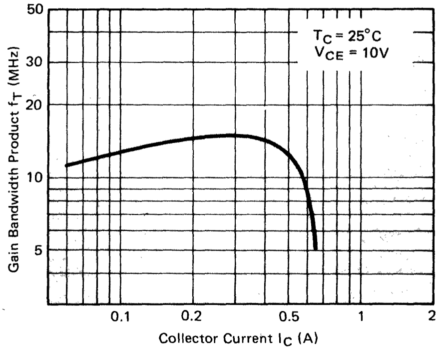
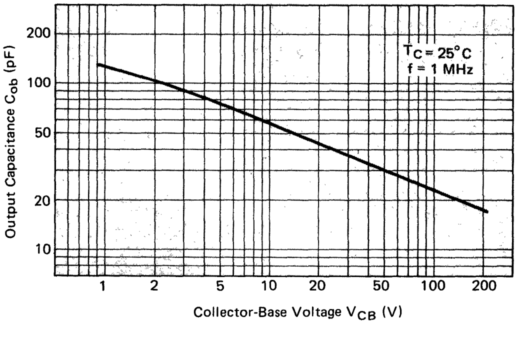
DC CURRENT GAIN



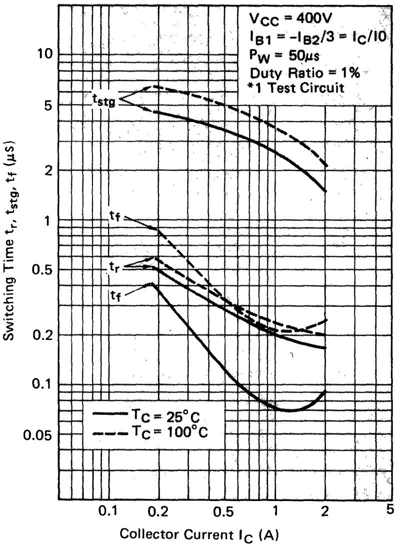
GAIN BANDWIDTH PRODUCT



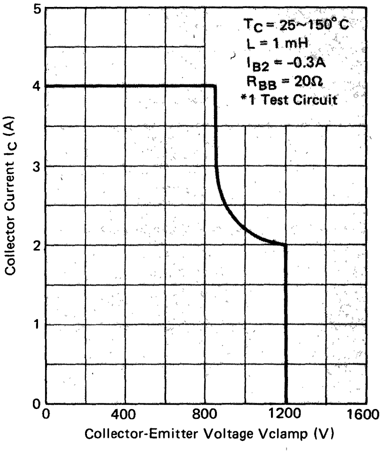
OUTPUT CAPACITANCE



SWITCHING TIME



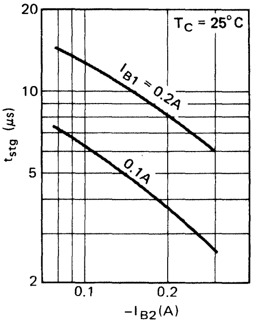
REVERSE BIAS SAFE OPERATING AREA



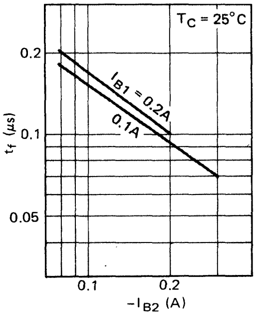
SWITCHING TIME

V_{CC} = 400V
I_C = 1A
Pw = 50μs
Duty Ratio = 1%

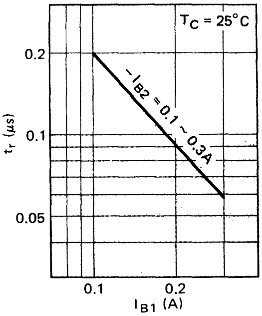
t_{stg} — I_{B2}



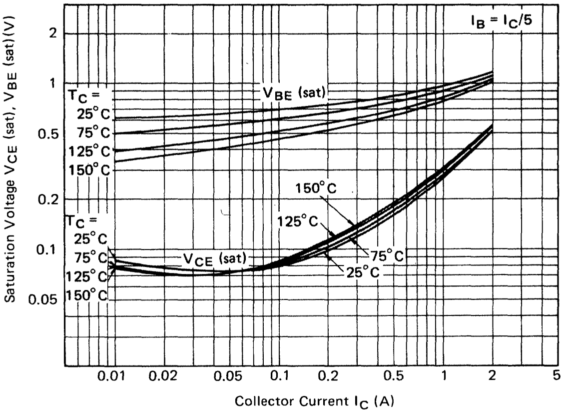
t_f — I_{B2}



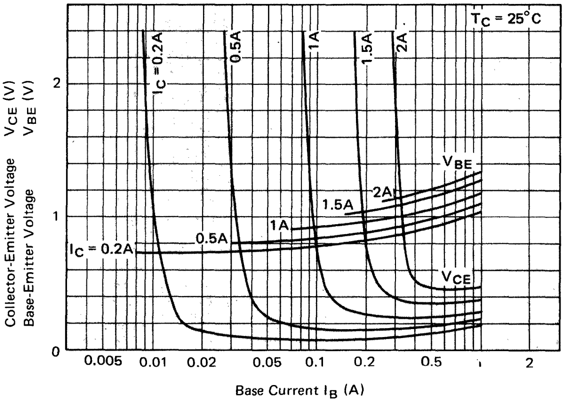
t_r — I_{B1}



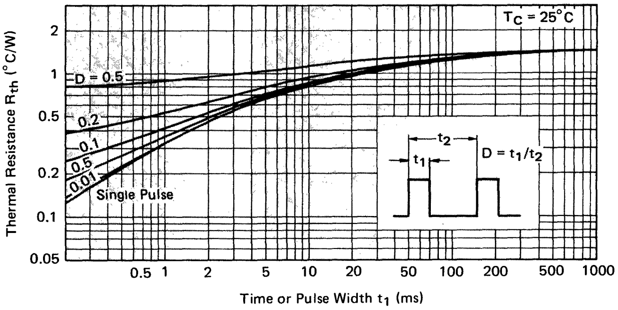
SATURATION VOLTAGE



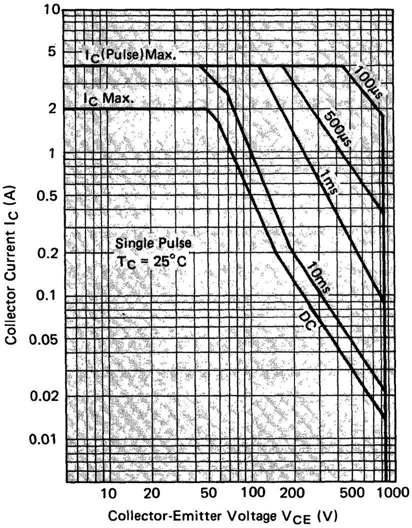
COLLECTOR SATURATION REGION



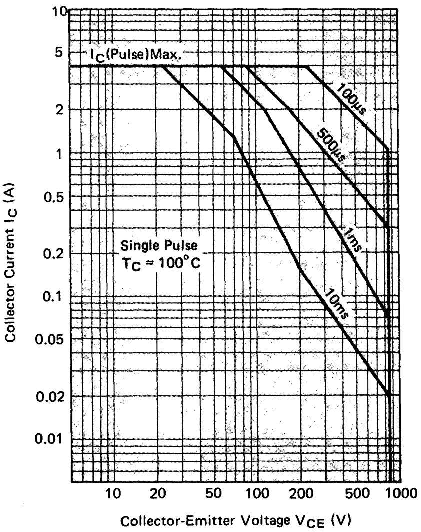
THERMAL RESPONSE



FOWARD BIAS SAFE OPERATING AREA



FOWARD BIAS SAFE OPERATING AREA



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3060

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	850	V
Collector to Base Voltage	V_{CBO}	1200	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	5	A
Collector Current-Pulsed $P_W \leqq 25\,\mu s$, D.R. $\leqq 50\%$	I_{CP}	8	A
Base Current-Continuous	I_B	3	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	150	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	−65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)}$ CBO	$I_C = 1mA$, $I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)}$ EBO	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)}$ CEO	$I_C = 10mA$, $R_{BE} = \infty\Omega$	850	–	–	V
Collector to Emitter Sustaining Voltage	V_{CEX} (SUS)	$I_C = 5A, I_{B2} = -0.6A, L = 1mH$(*1)	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V$, $I_E = 0, T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 2A$ (*2)	10	15	30	–
Collector to Emitter Saturation Voltage	V_{CE} (sat)	$I_C = 2A$, $I_B = 0.4A$ (*2)	–	0.3	1.5	V
Base to Emitter Saturation Voltage	V_{BE} (sat)		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, f = 1MHz	–	120	–	PF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 0.5A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ (*1) $I_C = 2A$, $3I_{B1} = -I_{B2} = 0.6A$	–	0.2	0.5	μs
Storage Time	t_{stg}		–	2.5	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leqq 300\,\mu s$, Duty Ratio $\leqq 6\%$

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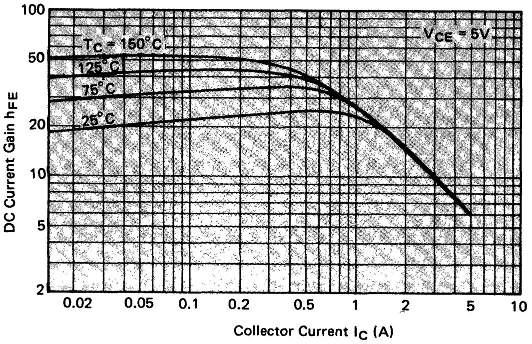
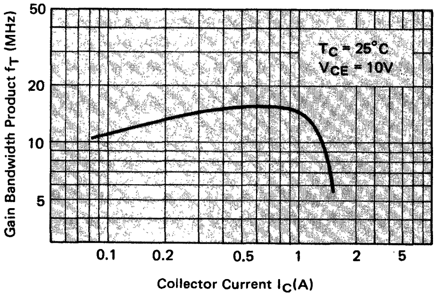
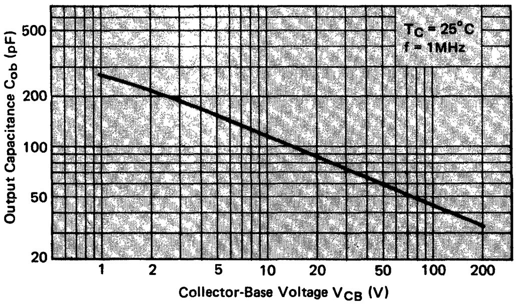
DC CURRENT GAIN



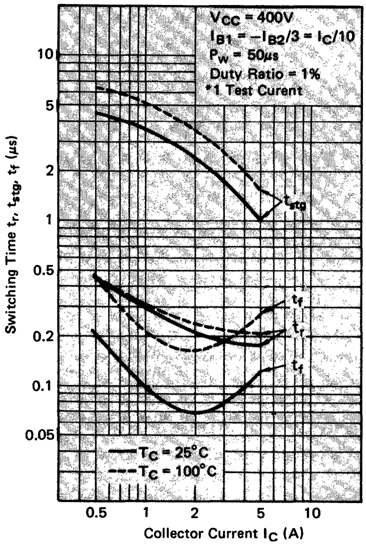
GAIN BANDWIDTH PRODUCT



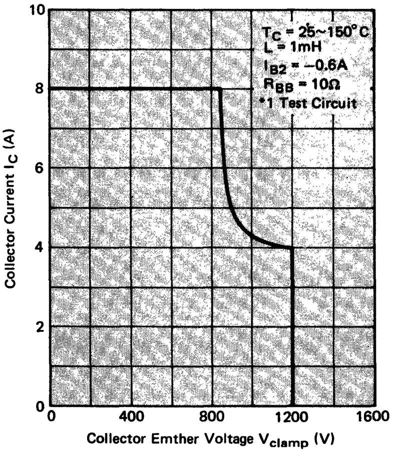
OUTPUT CAPACITANCE



SWITCHING TIME



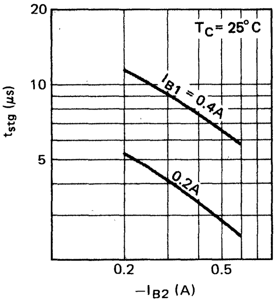
REVERSE BIAS SAFE OPERATING AREA



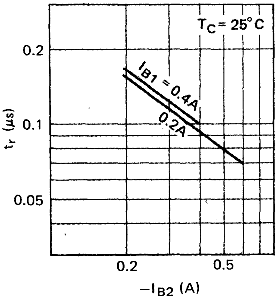
SWITCHING TIME

V_{CC} = 400V
I_C = 2A
P_w = 50μs
Duty Ratio = 1%

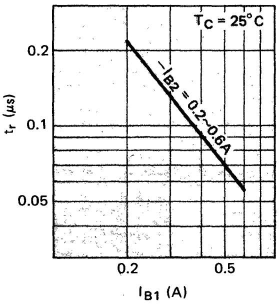
t_{stg} — I_{B2}



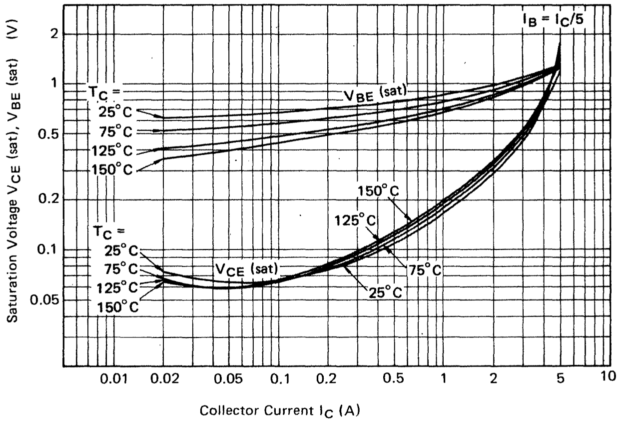
t_f — I_{B2}



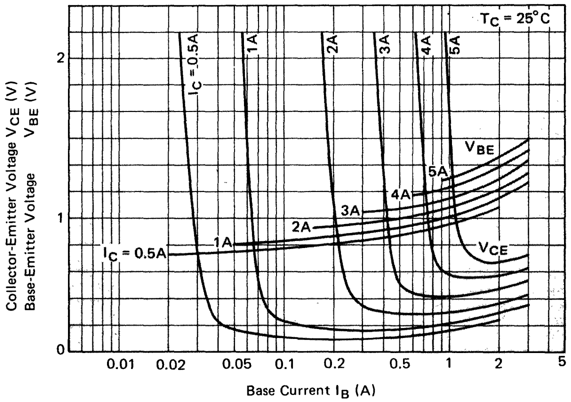
t_r — I_{B1}

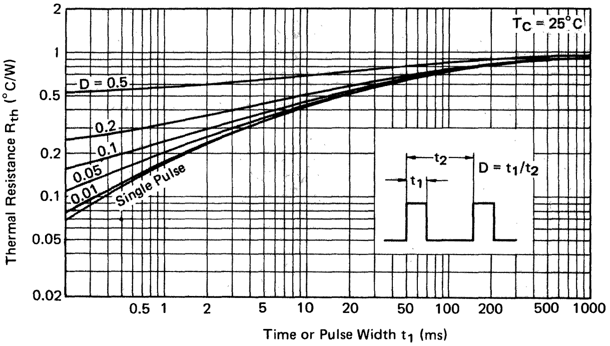


SATURATION VOLTAGE

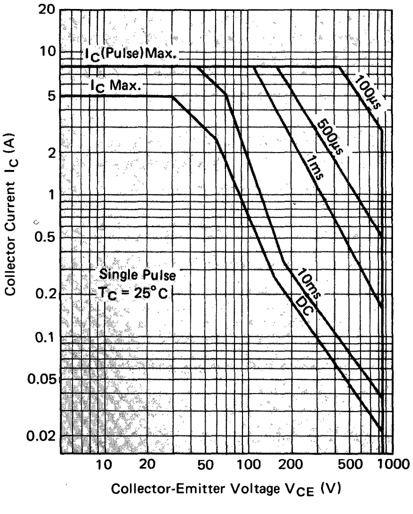


COLLECTOR SATURATION REGION

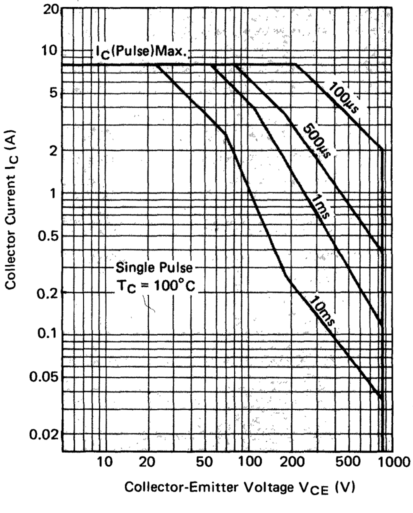




THERMAL RESPONSE



FORWARD BIAS SAFE OPERATING AREA



FORWARD BIAS SAFE OPERATING AREA

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3061

Silicon High Speed Power Transistor

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Emitter Voltage	V_{CEO}	850	V
Collector to Base Voltage	V_{CBO}	1200	V
Emitter to Base Voltage	V_{EBO}	7	V
Collector Current-Continuous	I_C	10	A
Collector Current-Pulsed $P_W \leqq 25\,\mu s$, D.R $\leqq$ 50%	I_{CP}	20	A
Base Current-Continuous	I_B	5	A
Collector Power Dissipation ($T_C = 25°C$)	P_C	200	W
Junction Temperature	T_j	+175	°C
Storage Temperature Range	T_{stg}	−65 ~ +175	°C

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)}$ CBO	$I_C = 1mA$, $I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)}$ EBO	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)}$ CEO	$I_C = 10mA$, $R_{BE} = \infty\Omega$	850	–	–	V
Collector to Emitter Sustaining Voltage	V_{CEX} (sus)	$I_C = 7A$, $I_{B2} = -1.2A$, L=1mH(*1)	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V$, $I_E = 0$	–	–	100	μA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 4A$(*2)	10	15	30	–
Collector to Emitter Saturation Voltage	V_{CE} (sat)	$I_C = 4A$, $I_B = 0.8A$(*2)	–	0.3	1.5	V
Base to Emitter Saturation Voltage	V_{BE} (sat)		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, f = 1MHz	–	220	–	PF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 1A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ (*1) $I_C = 4A$, $3I_{B1} = -I_{B2} = 1.2A$	–	0.2	0.5	μs
Storage Time	t_{stg}		–	2.5	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit *2 Pulsed $P_W \leqq 300\,\mu s$, Duty Ratio $\leqq$ 6%

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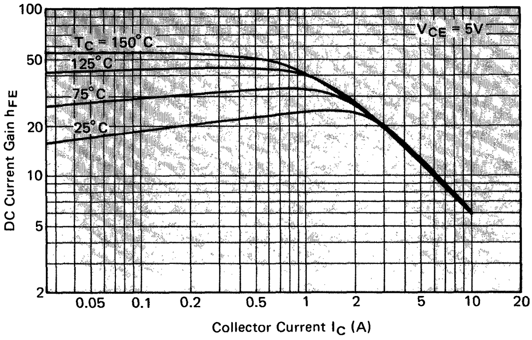
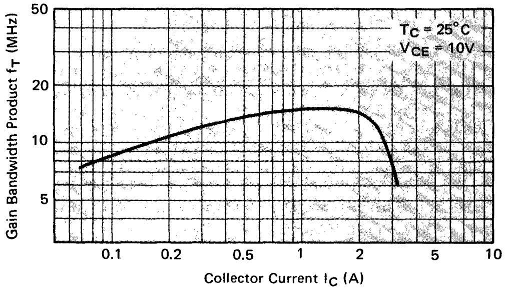
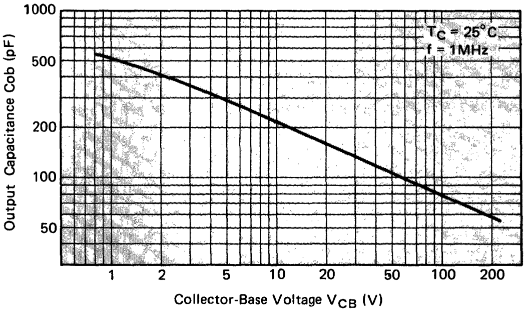
DC CURRENT GAIN



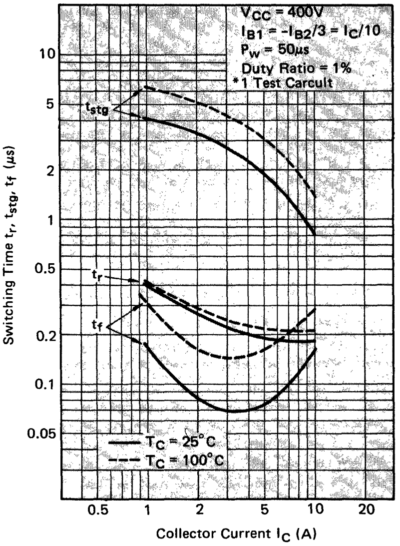
GAIN BANDWIDTH PRODUCT



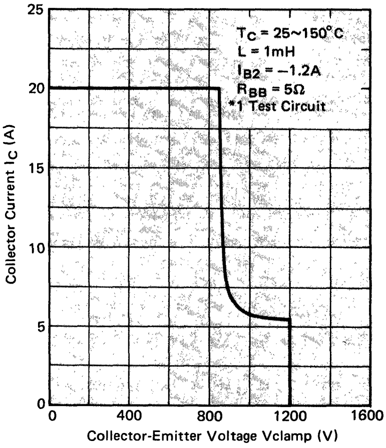
OUTPUT CAPACITANCE



SWITCHING TIME



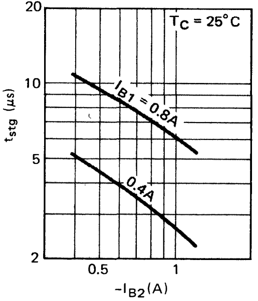
REVERSE BIAS SAFE OPERATING AREA



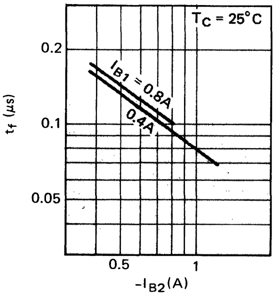
SWITCHING TIME

V_{CC} = 400V
I_C = 4A
P_w = 50μs
Duty Ratio = 1%

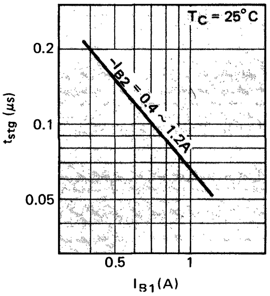
t_{stg} — I_{B2}



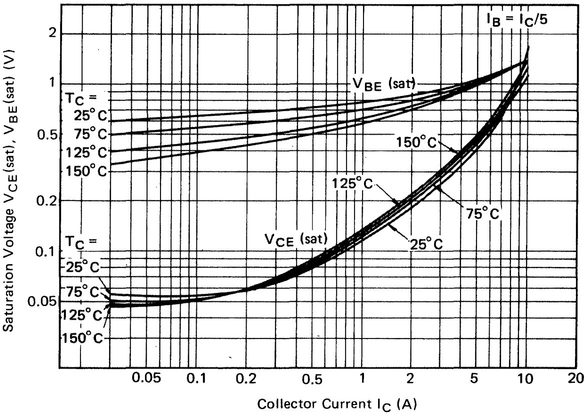
t_f — I_{B2}



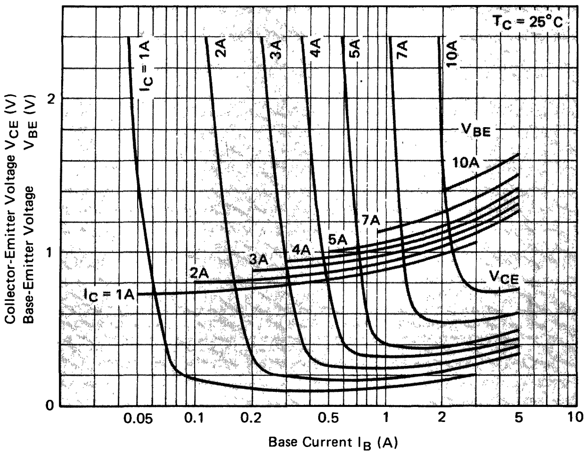
t_r — I_{B1}



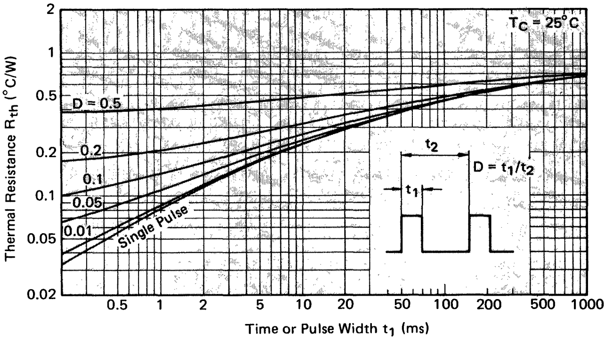
SATURATION VOLTAGE



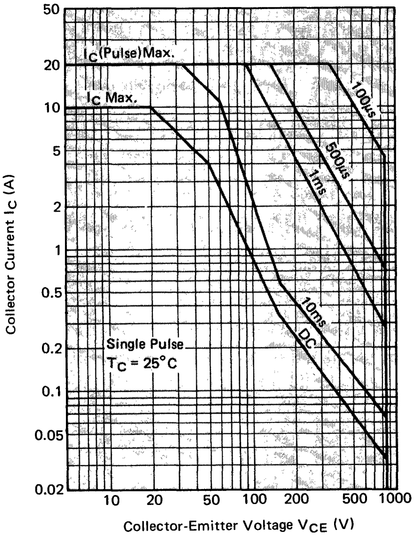
COLLECTOR SATURATION REGION



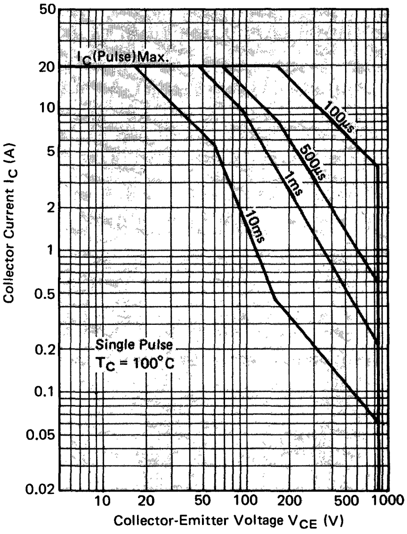
THERMAL RESPONSE



FORWARD BIAS SAFE OPERATING AREA



FOWARD BIAS SAFE OPERATING AREA



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

FT1551

Silicon High Speed Power Transistor

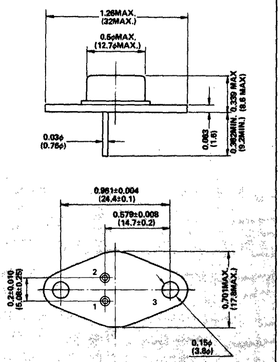
DESCRIPTION

The FT1551 is a silicon NPN general purpose, medium power transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of high power transistors with exceptional frequency response in high current applications.

The FT1551 is especially well-suited for High frequency power amplifiers, Audio power amplifiers and drivers.
A PNP complement, FT2551, is available.

- High f_T = 85 MHz (typ)
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability
- Excellent Current Gain Linearity

OUTLINE DIMENSION JEDEC TO-66



1: Base 2: Emitter 3: Collector
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	4	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	2	A
Collector Power Dissipation (T_C = 25°C)	P_C	20	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 100V, I_E = 0	–	–	10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 4V, I_C = 0	–	–	50	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 100V, I_B = 0	–	–	100	μA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	4	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 10mA*	60	–	350	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 0.3A *	50	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 0.7A, I_B = 0.07A*	–	0.1	1.0	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 0.7A*	–	0.8	1.5	V
Gain-Bandwidth Product	f_T	V_{CE}=10V,I_C=0.2A,f=10MHz	–	85	–	MHz
Output Capacitance	C_{ob}	V_{CB}=10V,I_E=0,f=1MHz	–	75	–	pF

* Pulsed: Pulse Width ≦ 300μs
Duty Cycle ≦ 6%

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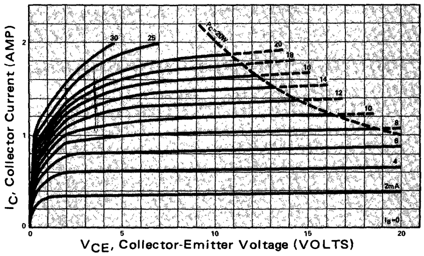
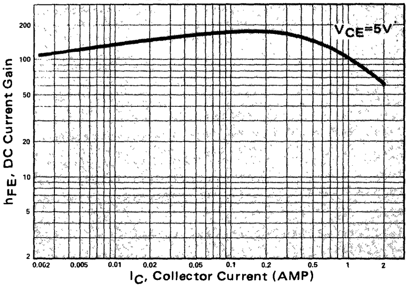
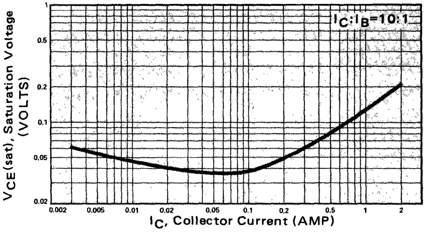
OUTPUT CHARACTERISTICS



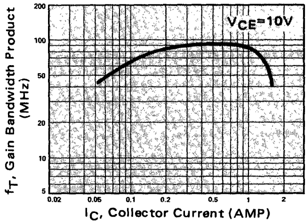
DC CURRENT GAIN



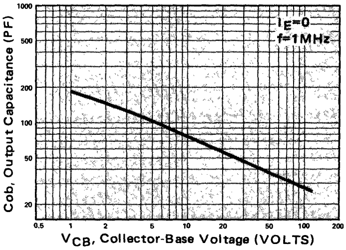
COLLECTOR SATURATION VOLTAGE



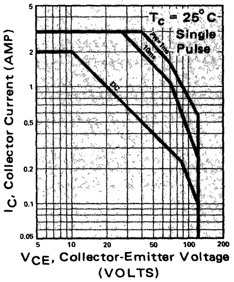
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



SAFE OPERATING AREAS



January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

FT2551

Silicon High Speed Power Transistor

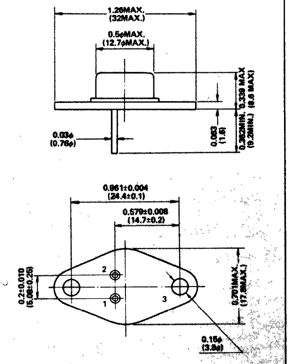
DESCRIPTION

The FT2551 is a silicon PNP general purpose, medium power transistor fabricated with Fujitsu's unique Ring Emitter Transistor (RET) technology. RET devices are constructed with multiple emitters connected through diffused ballast resistors which provide uniform current density. This structure permits the design of medium power transistors with exceptional frequency response in high current applications.

The FT2551 is especially well-suited for High frequency power amplifiers, Audio power amplifiers and drivers.
A NPN complement, FT1551, is available.

- High f_T = 60 MHz (typ)
- Excellent Safe Operating Area
- Improved reverse Second-Breakdown Capability
- Excellent Current Gain Linearity

OUTLINE DIMENSION
JEDEC TO–66



1: Base 2: Emitter 3: Collector
Dimension in inches and (millimeters)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector to Base Voltage	V_{CBO}	120	V
Emitter to Base Voltage	V_{EBO}	4	V
Collector to Emitter Voltage	V_{CEO}	120	V
Collector Current	I_C	2	A
Collector Power Dissipation (T_C = 25°C)	P_C	20	W
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	-65~+150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector Cutoff Current	I_{CBO}	V_{CB} = 100V, I_E = 0	–	–	10	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 4V, I_C = 0	–	–	50	μA
Collector Cutoff Current	I_{CEO}	V_{CE} = 100V, I_B = 0	–	–	100	μA
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	120	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	4	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	120	–	–	V
DC Current Gain	h_{FE1}	V_{CE} = 5V, I_C = 10mA*	60	–	350	
DC Current Gain	h_{FE2}	V_{CE} = 5V, I_C = 0.3A*	50	–	–	
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 0.7A, I_B = 0.07A*	–	0.1	1.0	V
Base to Emitter Voltage	V_{BE}	V_{CE} = 5V, I_C = 0.7A*	–	0.8	1.5	V
Gain-Bandwidth Product	f_T	V_{CE}=10V,I_C=0.2A,f=10MHz	–	60	–	MHz
Output Capacitance	C_{ob}	V_{CB}=10V,I_E=0,f=1MHz	–	120	–	pF

* Pulsed: Pulse Width ≤ 300μs
Duty Cycle ≤ 6%

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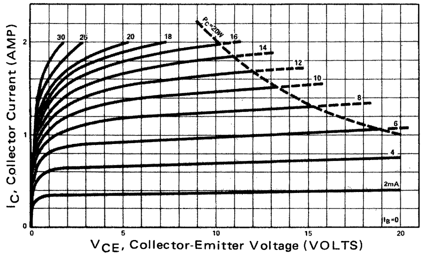
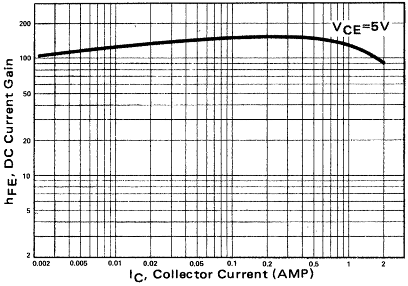
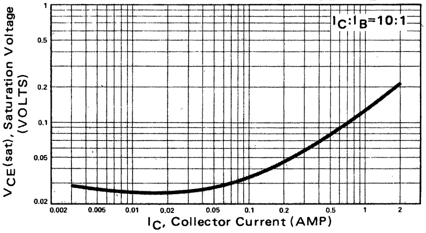
OUTPUT CHARACTERISTICS



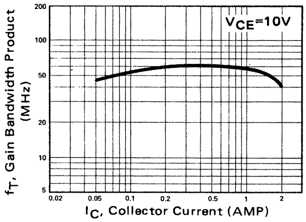
DC CURRENT GAIN



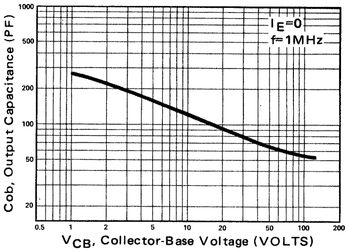
COLLECTOR SATURATION VOLTAGE



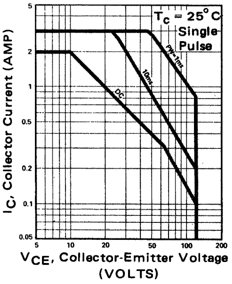
GAIN BANDWIDTH PRODUCT



OUTPUT CAPACITANCE



SAFE OPERATING AREAS



Full Plastic Mold Ring Emitter Transistors — *At a Glance*

Page	Device	Case (ns)	Polarity	Maximum Ratings V_{CEO} (V)	I_C (A)
2–5	2SC3842	TO–3PF	NPN	400	10
2–9	2SC3843	TO–3PF	NPN	450	10
2–13	2SC3844	TO–3PF	NPN	450	15
2–17	2SC3845	TO–3PF	NPN	800	3
2–21	2SC3846	TO–3PF	NPN	800	6
2–25	2SC3847	TO–3PF	NPN	800	10
2–29	2SC3947	TO–3PF	NPN	500	5
2–33	2SC3948	TO–3PF	NPN	500	10
2–37	2SC3949	TO–3PF	NPN	500	15

INTRODUCTION

TO-3PF Full Plastic Mold Power NPN Transistors (Ring Emitter Transistors)

Fujitsu's exclusive line of Full Plastic Mold TO-3PF High Speed Switching Power NPN Transistors eliminates the need for electrically isolating the package from the heatsink with materials such as mica and/or a mounting screw bushing. Collector power dissipation (P_c) is equal to or higher than other TO-3P type packages that require insulating materials and mounting screw isolation bushings as shown in the table below.

Features:

- High Reliability RET Transistor Design
- Up to 85 W collector power dissipation (P_c)
- Voltage ratings (V_{CEO}) up to 800 Volts
- DC current ratings (I_c) up to 15 Amps maximum at 25°C T_A
- No need to isolate package from heat sink
- Up to 2.5 KV isolation voltage (package and heatsink)

Applications:

- Switching regulators (60 to 200 KHz)
- CRT display deflection circuits (32 to 128 KHz)
- Ultrasound systems

Package	Isolation Material	P_c
Full Mold TO-3PF	Not Required	85 W
Other TO-3P	MICA 100μ (600 V)	85 W
	MICA 150μ (1200 V)	65 W
	Cool Sheet 200μ	55 W

(T_C = 25C, with silicon grease)

The mounting of this TO-3PF on the heatsink is completed with just one screw, so the mounting labor cost is reduced.

Tighten Torque requirement

5 kg * cm (Standard)
8 kg * cm (Maximum)

Isolation Voltage between package and heatsink:

2.5 KV minimum

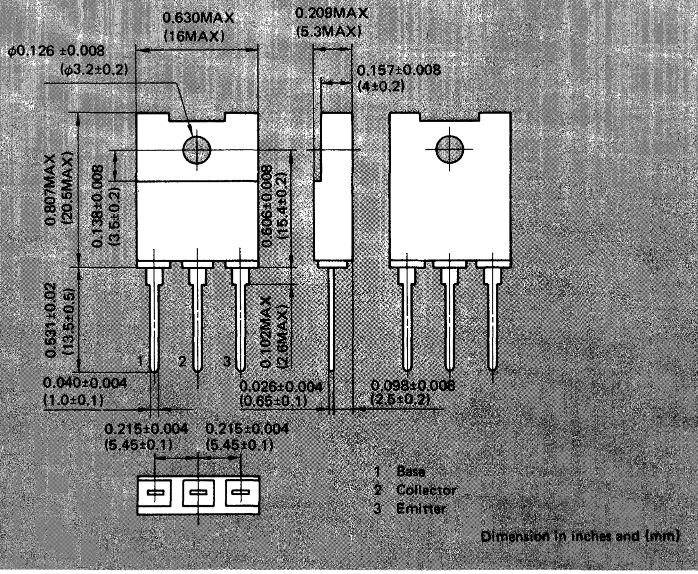
TO-3PF FULL PLASTIC MOLD POWER TRANSISTORS (RING EMITTER TRANSISTORS)

ELECTRICAL CHARACTERISTICS

Type No.	Maximum Ratings (T_a = 25°C)					Electrical Characteristics (T_a = 25°C)			
	V_{CBO} (V)	V_{CEO} (V)	I_C (A)	I_{CM}* (A)	P_C (W)	V_{CE} (V)	I_C (A)	h_{FE} Min.	t_f (μs) Max.
2SC3842	600	400	10	15	70	5	5	10	0.3
2SC3843	600	450	10	20	75	5	6	10	0.2
2SC3844	600	450	15	20	75	5	10	10	0.3
2SC3845	1200	800	3	6	75	5	1	10	0.3
2SC3846	1200	800	6	10	80	5	2	10	0.3
2SC3847	1200	800	10	20	85	5	4	10	0.3
2SC3947	850	500	5	8	70	5	2.5	10	0.3
2SC3948	850	500	10	15	75	5	5	10	0.3
2SC3949	850	500	15	20	80	5	10	10	0.3

* Pulsed $P_W \leq 25\mu s$, D.R. $\leq 50\%$

- **Package Outline and Terminal Configuration**



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Edition 1.1

PRODUCT PROFILE

2SC3842

Silicon High Speed Power Transistor

3SC3842 400V, 10A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		600	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		400	V
Collector Current	I_C		10	A
	I_{CM}	$P_W \leqq 10ms$, D.R. $\leqq 2\%$	15	
Base Current	I_B		5	A
Collector Power Dissipation	P_C	$T_C = 25°C$	70	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 0.8A, R_{BE} = \infty\Omega$	400	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 2A, I_{B2} = -1A$, $L = 200\mu H$*	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V, I_E = 0$	–	–	100	μA
		$V_{CB} = 500V, I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{BE} = 6V, I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 5A$**	10	17	40	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 5A, I_B = 1A$**	–	0.38	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.15	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	100	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 1A$	–	32	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ $I_C = 5A, I_{B1} = -I_{B2} = 1A$*	–	0.09	0.5	μs
Storage Time	t_{stg}		–	1.90	2.5	μs
Fall Time	t_f		–	0.14	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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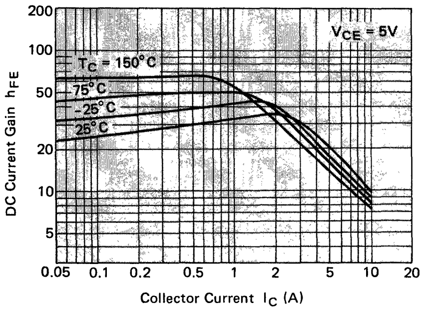
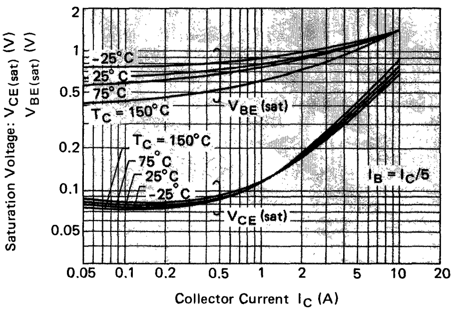
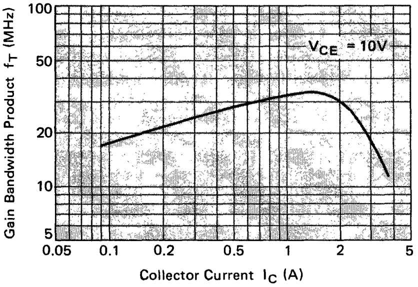


$h_{FE} - I_C$

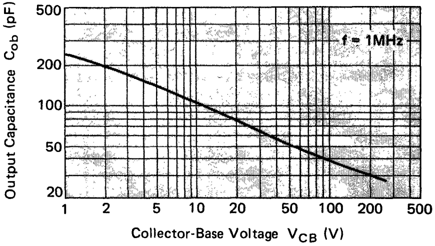


V_{CE} (sat), V_{BE} (sat) $- I_C$



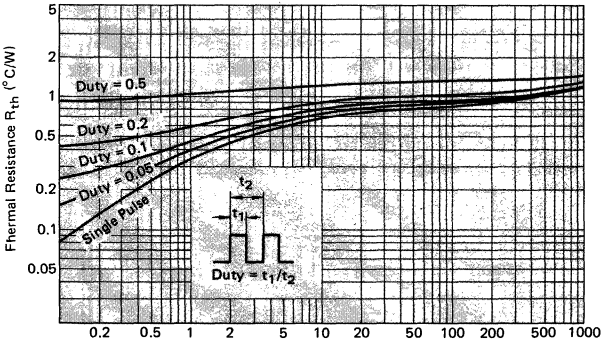
$f_T - I_C$

T_C = 25°C



$C_{ob} - V_{CB}$

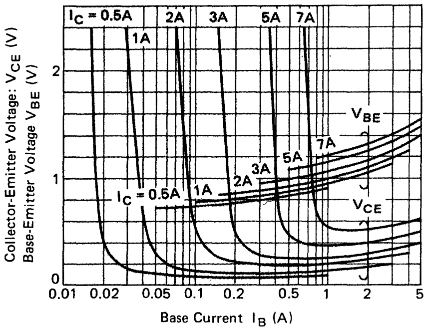
T_C = 25°C



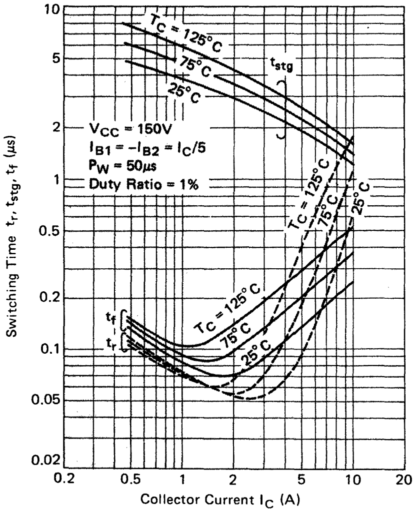
Thermal Response

T_C = 25°C

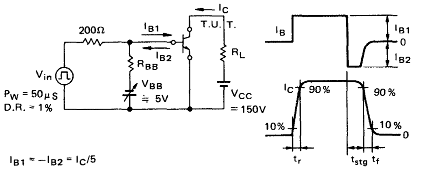
V_{CE}, V_{BE} — I_B T_C = 25°C



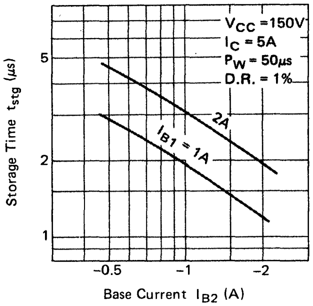
t_r, t_{stg}, t_f — I_C



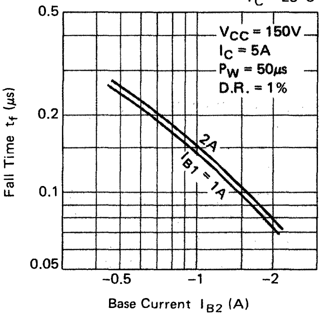
Test Circuit for Switching Time



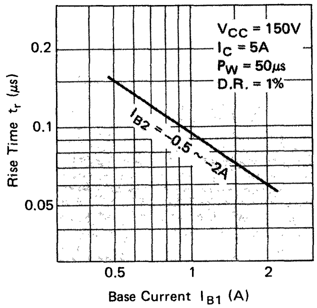
t_{stg} — I_{B2} T_C = 125°C



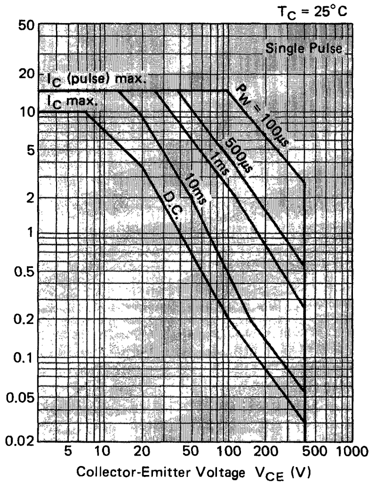
t_f — I_{B2} T_C = 25°C



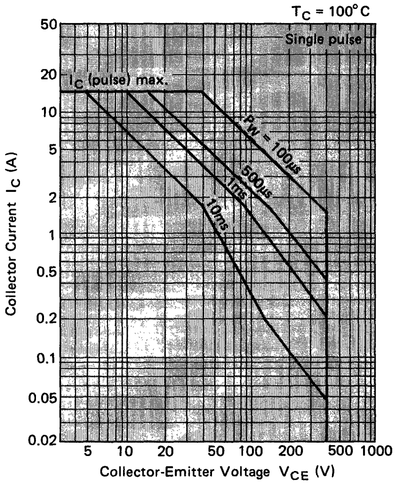
t_r — I_{B1} T_C = 25°C



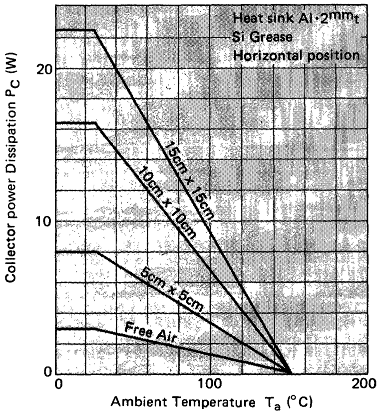
Forward Bias Safe Operating Area — 1



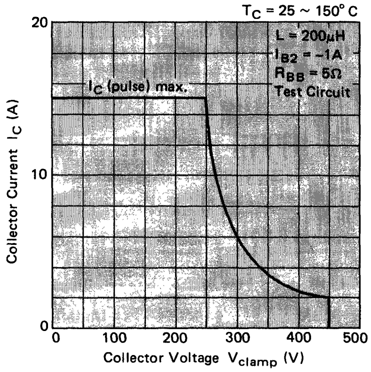
Forward Bias Safe Operating Area — 2



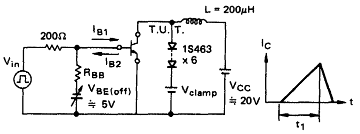
$P_C - T_a$



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$V_{CEX(SUS)}$: V_{clamp} = 450V
I_C = 2A R_{BB} = 5Ω
I_{B1} = $-I_{B2}$ = 1A

$t_1 \doteqdot \frac{L_{coil}(I_C)}{V_{CC}}$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3843

Silicon High Speed Power Transistor

2SC3843 450V, 10A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		600	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		450	V
Collector Current	I_C		10	A
	I_{CM}	$P_W \leqq 10ms$, D.R. $\leqq 2\%$	20	
Base Current	I_B		5	A
Collector Power Dissipation	P_C	$T_C = 25°C$	75	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 0.8A, R_{BE} = \infty\Omega$	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 8A, I_{B2} = -1A$, $L = 200\mu H$*	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V, I_E = 0$	–	–	100	μA
		$V_{CB} = 500V, I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 6A$**	10	14	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 6A, I_B = 1.2A$**	–	0.43	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.05	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	230	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_E = 2A$	–	28	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ $I_C = 6A, I_{B1} = -I_{B2} = 1.2A$*	–	0.08	0.3	μs
Storage Time	t_{stg}		–	1.25	1.5	μs
Fall Time	t_f		–	0.07	0.2	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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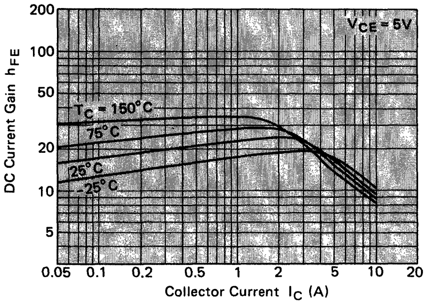
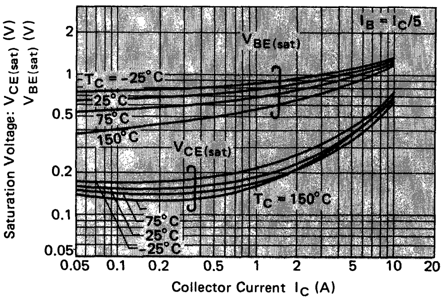
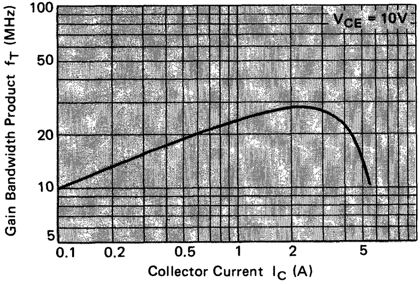
$h_{FE} - I_C$



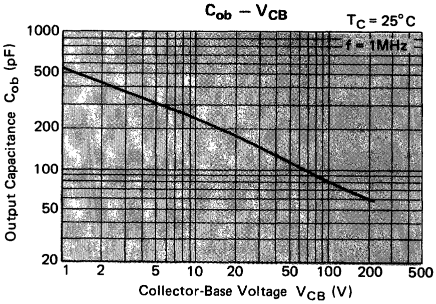
V_{CE} (sat), V_{BE} (sat) $- I_C$



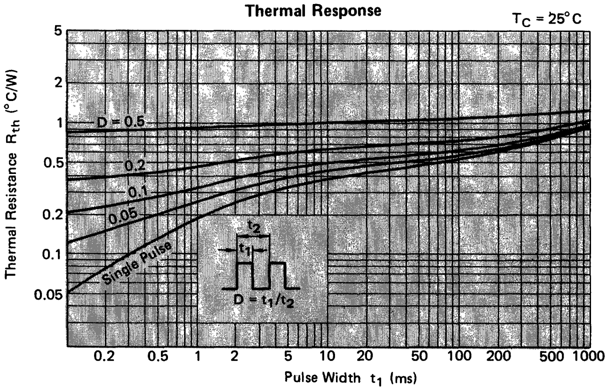
$f_T - I_C$



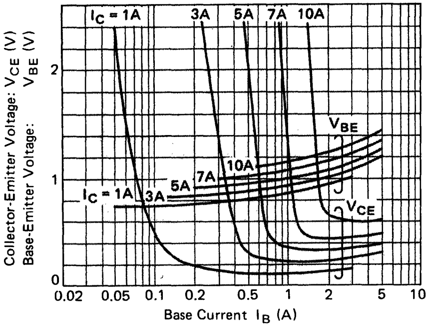
$C_{ob} - V_{CB}$



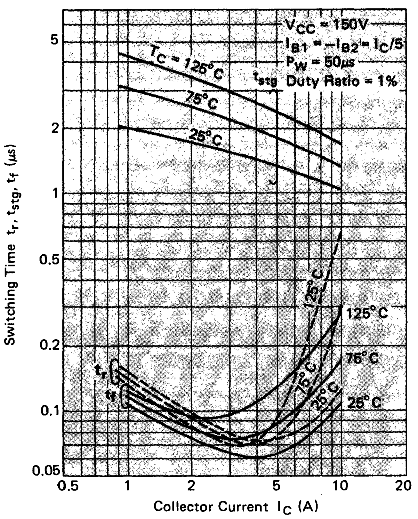
Thermal Response



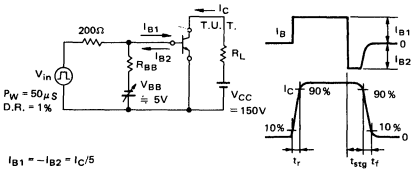
V_{CE}, V_{BE} – I_B



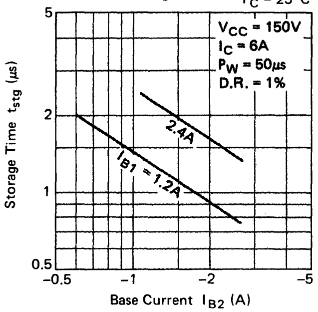
t_r, t_{stg}, t_f – I_C



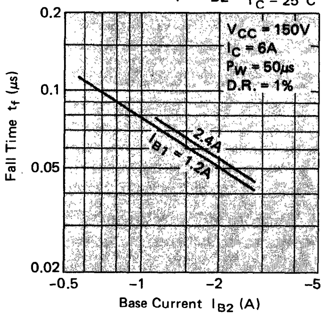
Test Circuit for Switching Time



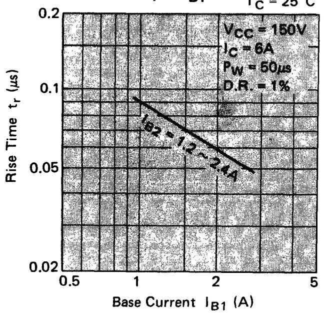
t_{stg} – I_{B2}



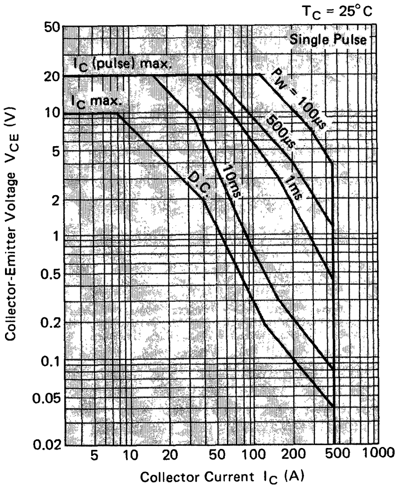
t_f – I_{B2}



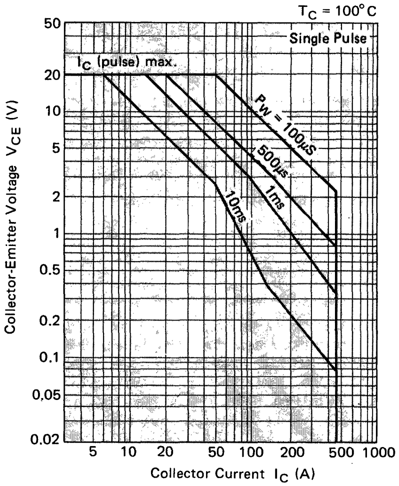
t_r – I_{B1}



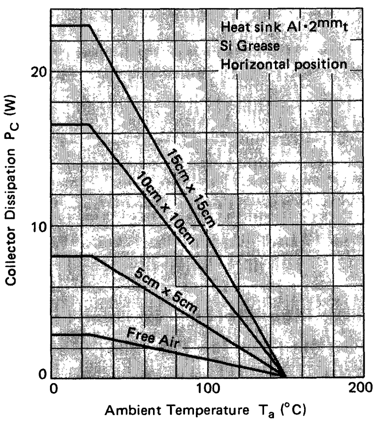
Forward Bias Safe Operating Area — 1



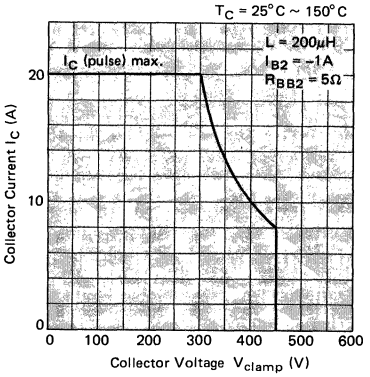
Forward Bias Safe Operating Area — 2



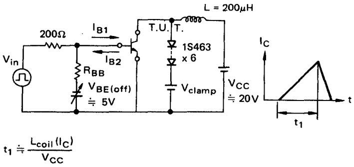
$P_C - T_a$



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$V_{CEX(SUS)}$: V_{clamp} = 450V
I_C = 2A R_{BB} = 5Ω
I_{B1} = 2A
I_{B2} = −1A

$$t_1 \doteqdot \frac{L_{coil}(I_C)}{V_{CC}}$$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3844

Silicon High Speed Power Transistor

2SC3844 450V, 15A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		600	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		450	V
Collector Current	I_C		15	A
	I_{CM}	$P_W \leqq 10ms$, D.R. $\leqq 2\%$	20	
Base Current	I_B		5	A
Collector Power Dissipation	P_C	$T_C = 25°C$	75	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	600	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEO(SUS)}$	$I_C = 0.8A$, $R_{BE} = \infty\Omega$	450	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 8A$, $I_{B2} = -1A$, $L = 200\mu H^*$	450	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500V$, $I_E = 0$	–	–	100	μA
		$V_{CB} = 500V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 10A^{**}$	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10A$, $I_B = 2A^{**}$	–	0.56	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	240	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 2A$	–	30	–	MHz
Rise Time	t_r	$V_{CC} = 150V$ $I_C = 10A$, $I_{B1} = -I_{B2} = 2A^*$	–	0.13	0.5	μs
Storage Time	t_{stg}		–	1.80	2.5	μs
Fall Time	t_f		–	0.11	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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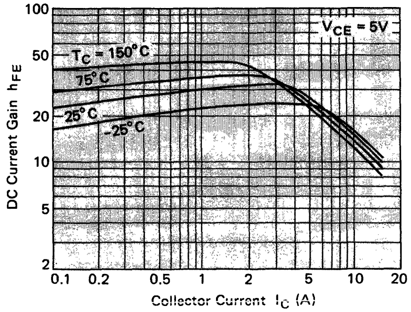
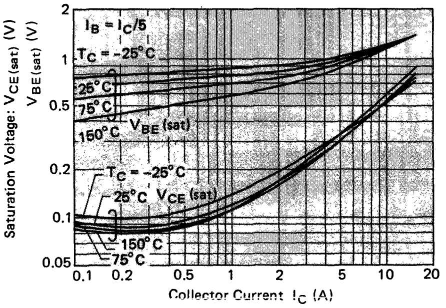
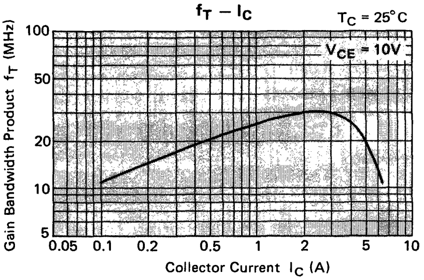
h_{FE} − I_C



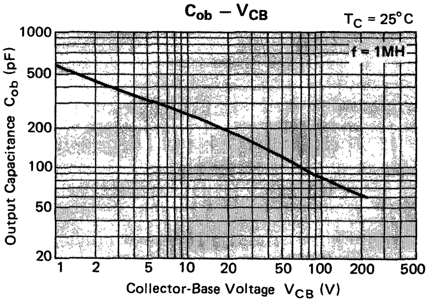
V_{CE} (sat), V_{BE} (sat) − I_C



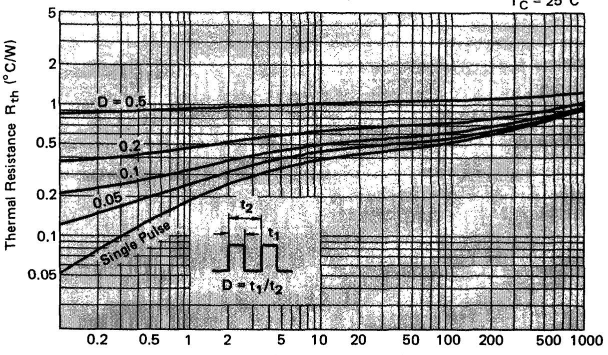
f_T − I_C



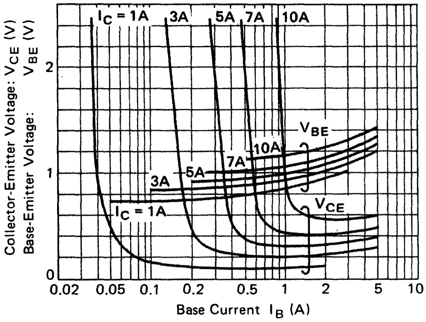
C_{ob} − V_{CB}



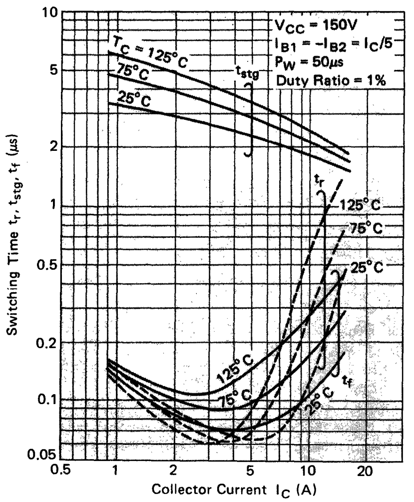
Thermal Response



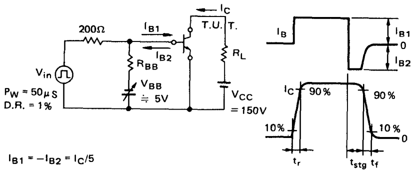
V_{CE}, V_{BE} – I_B



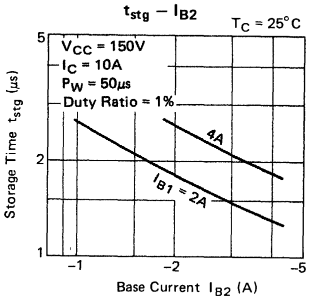
t_r, t_{stg}, t_r – I_C



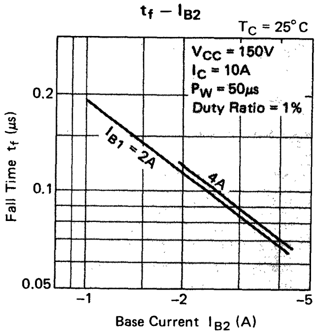
Test Circuit for Switching Time



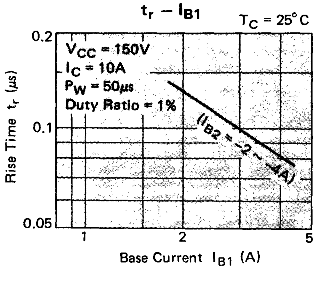
t_{stg} – I_{B2}



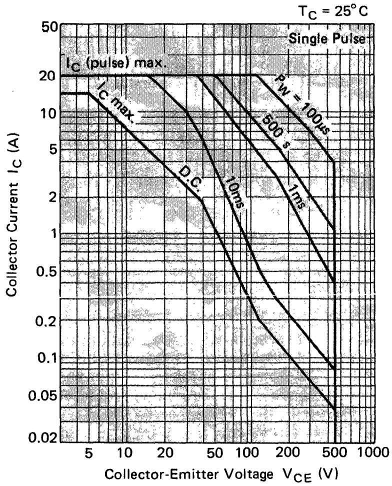
t_f – I_{B2}



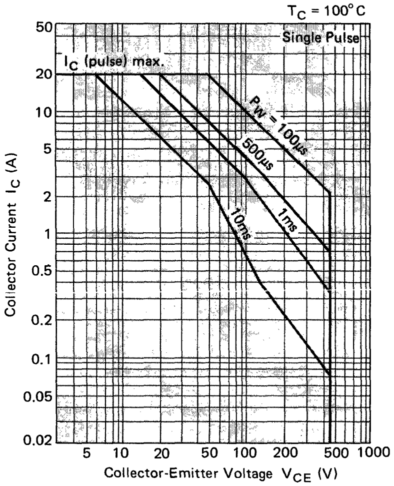
t_r – I_{B1}



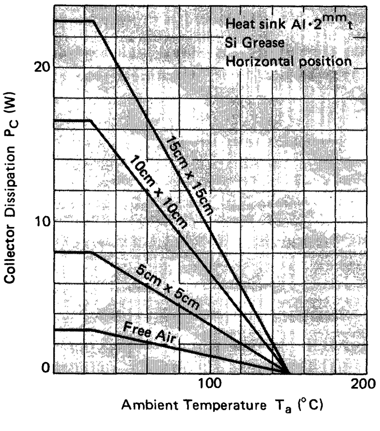
Forward Bias Safe Operating Area — 1



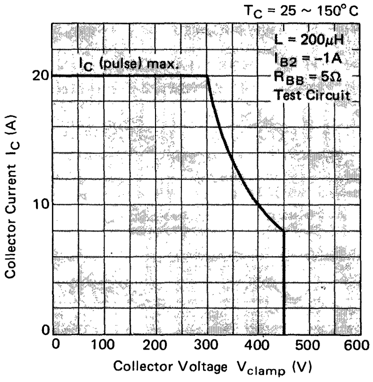
Forward Bias Safe Operating Area — 2



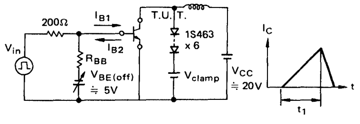
P_C — T_a



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$V_{CEX(SUS)}$: V_{clamp} = 450V

I_C = 8A R_{BB} = 5Ω

I_{B1} = 2A

I_{B2} = −1A

$t_1 \doteqdot \frac{L_{coil}(I_C)}{V_{CC}}$

January 1990
Edition 1.1

2SC3845

Silicon High Speed Power Transistor

2SC3845 800V, 3A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		1200	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		800	V
Collector Current	I_C		3	A
	I_{CM}	$P_W \leqq 25\mu s$, D.R. $\leqq 50\%$	6	
Base Current	I_B		1	A
Collector Power Dissipation	P_C	$T_C = 25°C$	75	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	800	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 2.5A, I_{B2} = -0.3A$, $L = 1mH$*	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0$	–	–	100	µA
		$V_{CB} = 1000V, I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	µA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 1A$**	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 1A, I_B = 0.2A$**	–	0.3	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0$, f = 1HMz	–	60	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 0.2A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ $I_C = 1A, 3I_{B1} = -I_{B2} = 0.3A$*	–	0.20	0.5	µs
Storage Time	t_{stg}		–	2.50	3.5	µs
Fall Time	t_f		–	0.07	0.3	µs

*1 Test Circuit **2 Pulse $P_W \leqq$ 300=s, Duty Ratio $\leqq 6\%$

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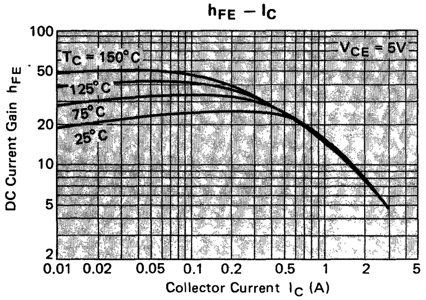
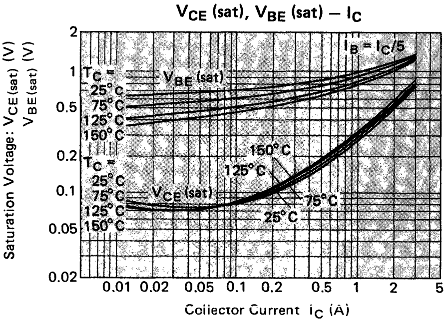
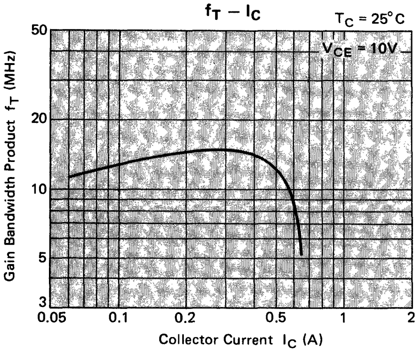
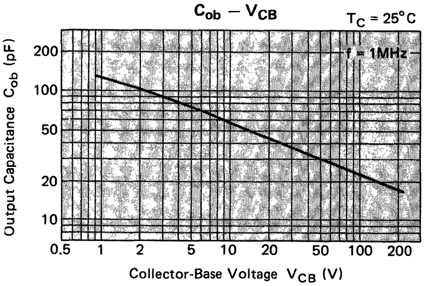
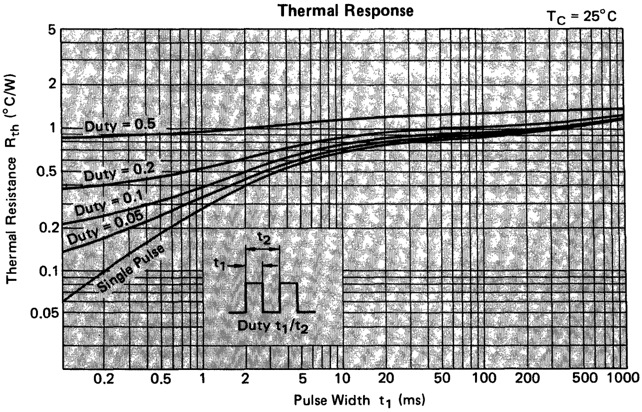

$h_{FE} - I_C$
$V_{CE} = 5V$
$T_C = 150°C$
125°C
75°C
25°C
DC Current Gain h_{FE}
100
50
20
10
5
2
0.01
0.02
0.05
0.1
0.2
0.5
1
2
5
Collector Current I_C (A)

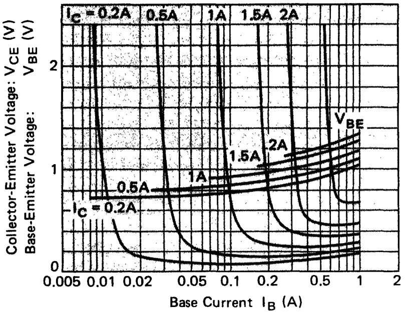

V_{CE} (sat), V_{BE} (sat) $- I_C$
$I_B = I_C/5$
T_C =
25°C
75°C
125°C
150°C
V_{BE} (sat)
V_{CE} (sat)
150°C
125°C
75°C
25°C
Saturation Voltage: $V_{CE(sat)}$ (V) $V_{BE(sat)}$ (V)
2
1
0.5
0.2
0.1
0.05
0.02
0.01
0.02
0.05
0.1
0.2
0.5
1
2
5
Collector Current I_C (A)


$f_T - I_C$
$T_C = 25°C$
$V_{CE} = 10V$
Gain Bandwidth Product f_T (MHz)
50
20
10
5
3
0.05
0.1
0.2
0.5
1
2
Collector Current I_C (A)

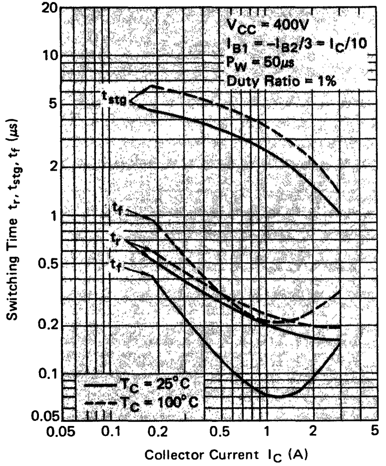

$C_{ob} - V_{CB}$
$T_C = 25°C$
f = 1MHz
Output Capacitance C_{ob} (pF)
200
100
50
20
10
0.5
1
2
5
10
20
50
100
200
Collector-Base Voltage V_{CB} (V)


Thermal Response
$T_C = 25°C$
Duty = 0.5
Duty = 0.2
Duty = 0.1
Duty = 0.05
Single Pulse
t_1
t_2
Duty t_1/t_2
Thermal Resistance R_{th} (°C/W)
5
2
1
0.5
0.2
0.1
0.05
0.2
0.5
1
2
5
10
20
50
100
200
500
1000
Pulse Width t_1 (ms)

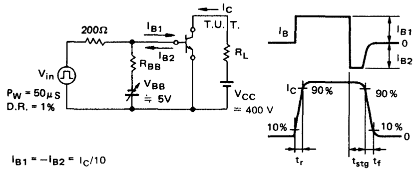
V_{CE}, V_{BE} – I_B T_C = 25°C



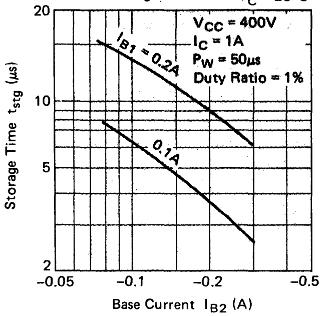
t_r, t_{stg}, t_r – I_C



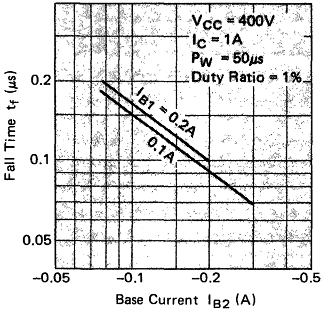
Test Circuit for Switching Time



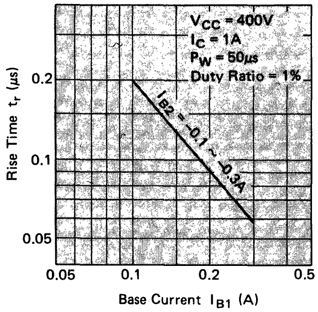
t_{stg} – I_{B2} T_C = 25°C

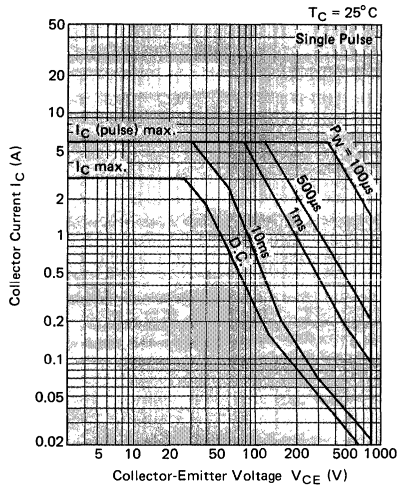


t_f – I_{B2} T_C = 25°C

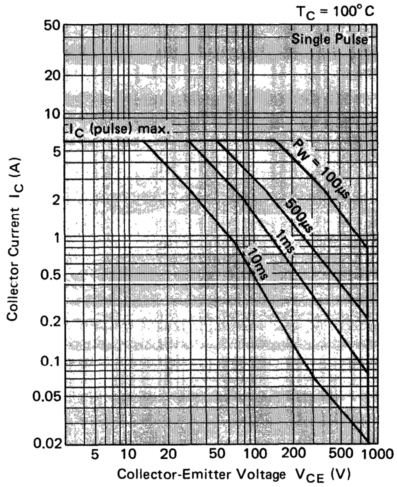


t_r – I_{B1} T_C = 25°C

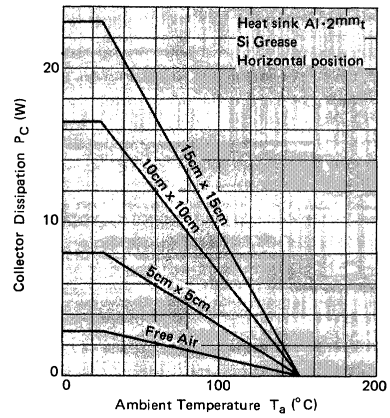




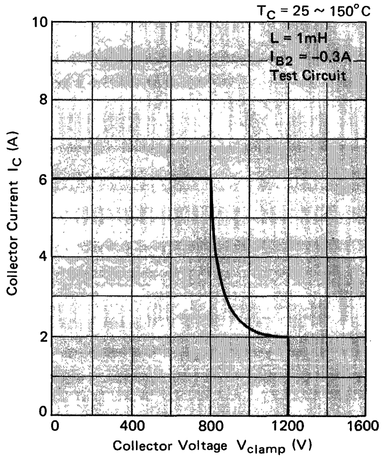
Forward Bias Safe Operating Area — 1



Forward Bias Safe Operating Area — 2

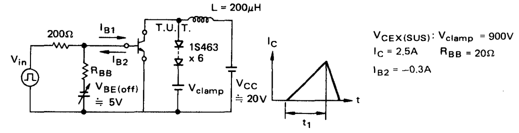


$P_C - T_a$



Reverse Bias Safe Operating Area

Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$t_1 \fallingdotseq \frac{L_{coil}(I_C)}{V_{CC}}$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3846

Silicon High Speed Power Transistor

2SC3846 800V, 6A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		1200	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		800	V
Collector Current	I_C		6	A
	I_{CM}	$P_W \leqq 25\mu s$, D.R. $\leqq 50\%$	10	
Base Current	I_B		3	A
Collector Power Dissipation	P_C	$T_C = 25°C$	80	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	800	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 5A, I_{B2} = -0.6A$, $L = 1mA^{*}$	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V, I_E = 0$	–	–	100	μA
		$V_{CB} = 1000V, I_E = 0$, $T_a = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 2A^{**}$	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 2A, I_B = 0.4A^{**}$	–	0.3	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	120	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 0.5A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ $I_C = 2A, 3I_{B1} = -I_{B2} = 0.6A^{*}$	–	0.20	0.5	μs
Storage Time	t_{stg}		–	2.50	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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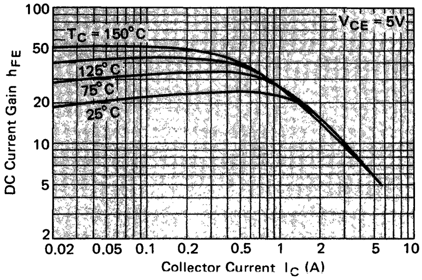
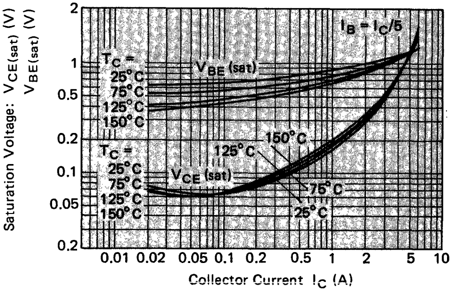
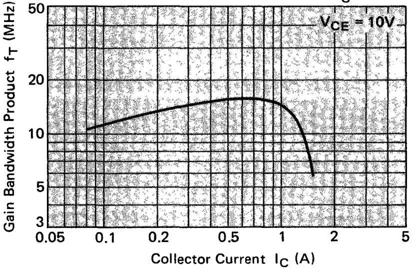
$h_{FE} - I_C$



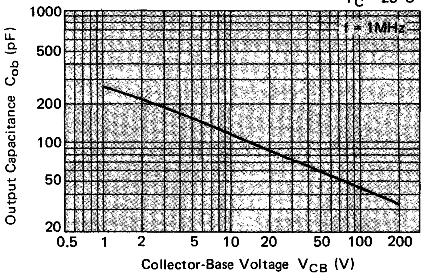
V_{CE} (sat), V_{BE} (sat) – I_C



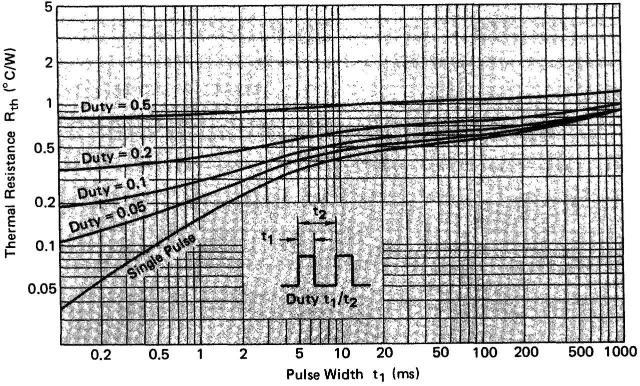
$f_T - I_C$



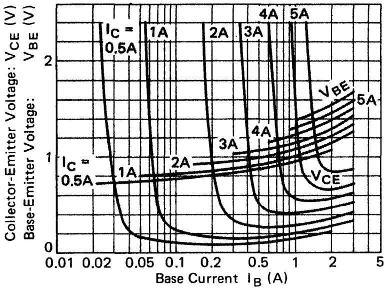
$C_{ob} - V_{CB}$



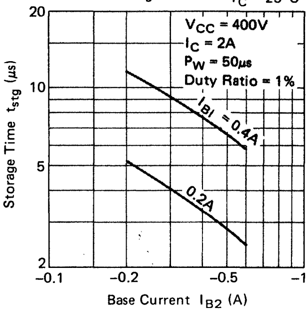
Thermal Response



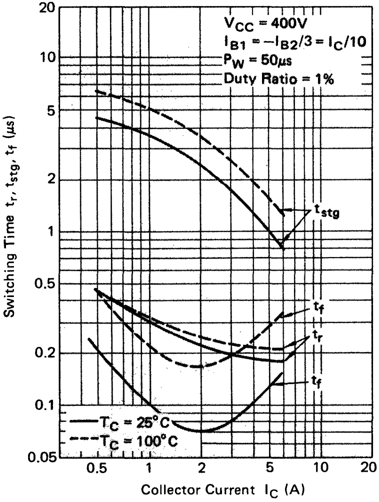
V_{CE}, V_{BE} – I_B T_C = 25°C



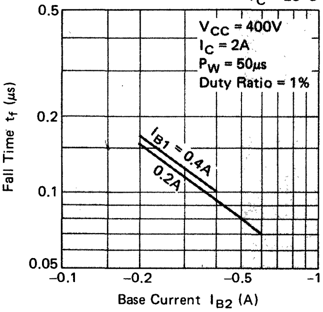
t_{stg} – I_{B2} T_C = 25°C



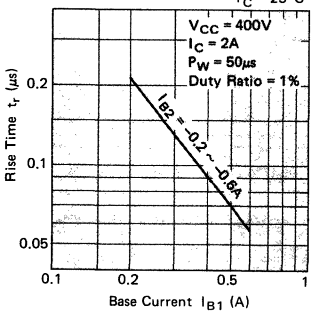
t_r, t_{stg}, t_f – I_C



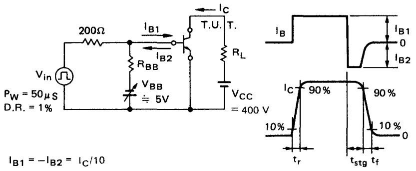
t_f – I_{B2} T_C = 25°C



t_r – I_{B1} T_C = 25°C

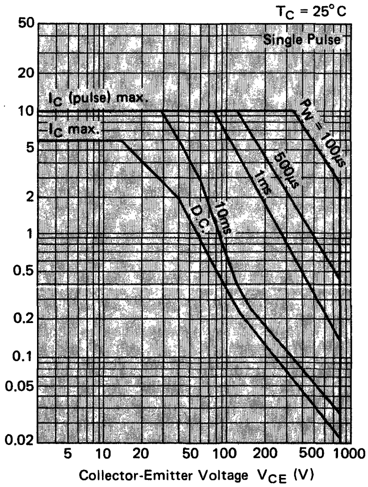


Test Circuit for Switching Time

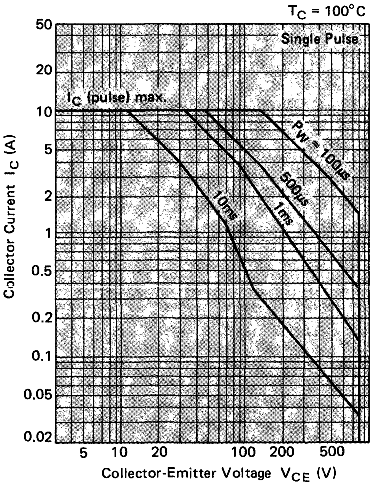


I_{B1} = −I_{B2} = I_C/10

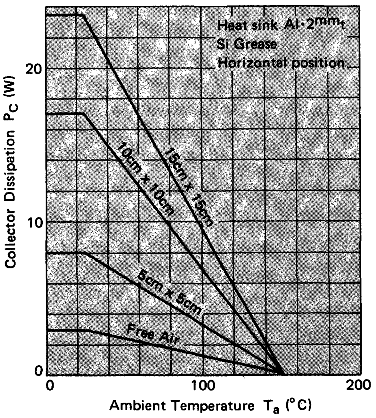
Forward Bias Safe Operating Area — 1



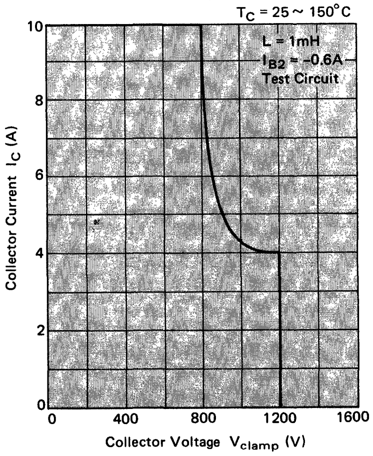
Forward Bias Safe Operating Area — 2



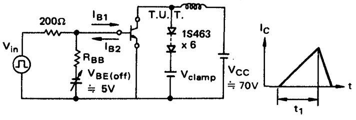
P_C — T_a



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$V_{CEX(SUS)}$: V_{clamp} = 900V
I_C = 5A R_{BB} = 10Ω
I_{B2} = −0.6A

$$t_1 \fallingdotseq \frac{L_{coil}(I_C)}{V_{CC}}$$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3847

Silicon High Speed Power Transistor

2SC3847 800V, 10A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		1200	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		800	V
Collector Current	I_C		10	A
	I_{CM}	$P_W \leqq 25\mu s$, D.R. $\leqq 50\%$	20	
Base Current	I_B		5	A
Collector Power Dissipation	P_C	$T_C = 25°C$	85	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	1200	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA$, $R_{BE} = \infty\Omega$	800	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 7A$, $I_{B2} = -1.2A$, $L = 1mH$*	900	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 1000V$, $I_E = 0$	–	–	100	μA
		$V_{CB} = 1000V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 4A$**	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 4A$, $I_B = 0.8A$**	–	0.3	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.0	2.0	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	220	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 0.1A$	–	15	–	MHz
Rise Time	t_r	$V_{CC} = 400V$ $I_C = 4A$, $31B1 = -I_{B2} = 1.2A$*	–	0.20	0.5	μs
Storage Time	t_{stg}		–	2.50	3.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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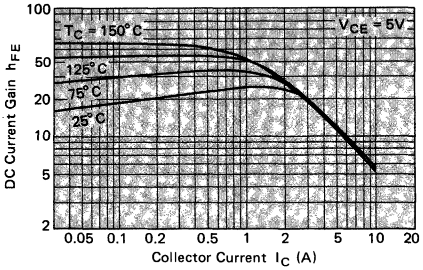
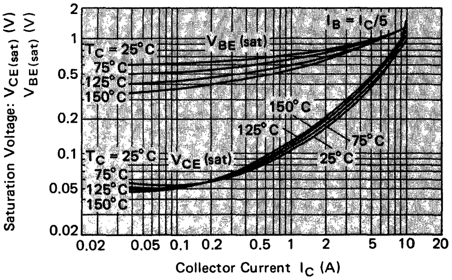
h_{FE} − I_C

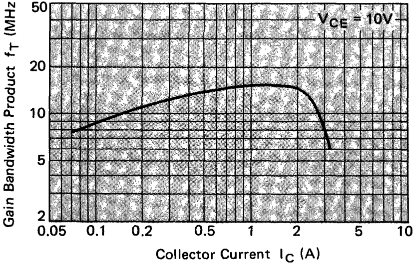


V_{CE} (sat), V_{BE} (sat) − I_C



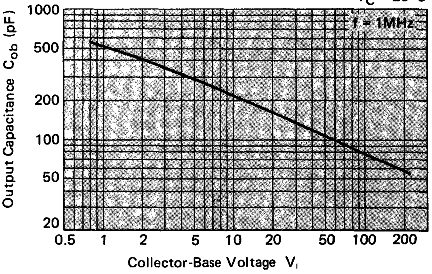
f_T − I_C

T_C = 25°C



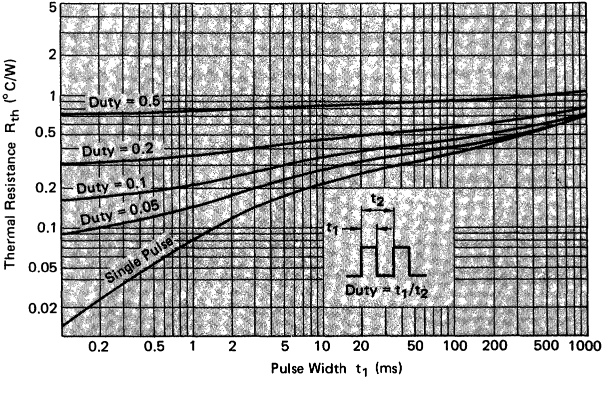
C_{ob} − V_{CB}

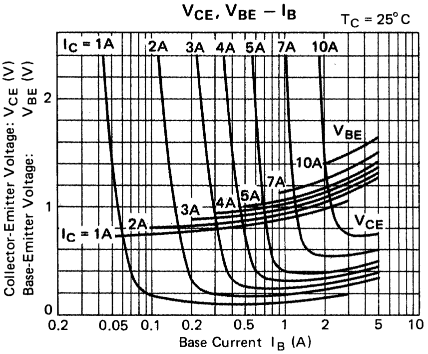
T_C = 25°C

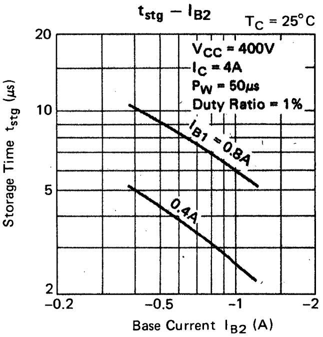


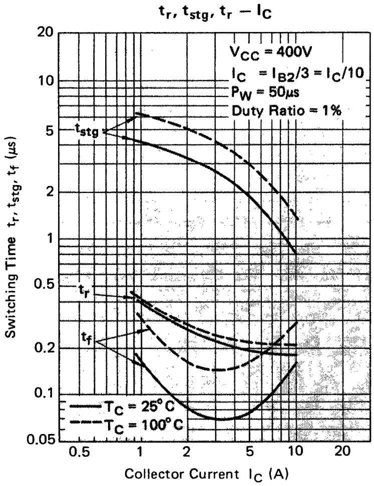
Thermal Response

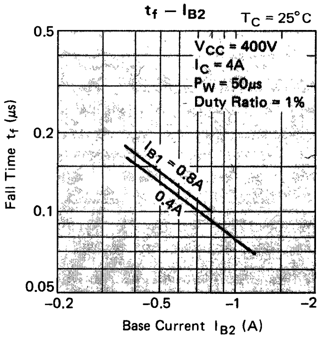
T_C = 25°C



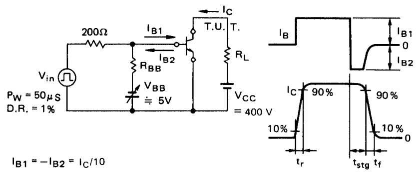

V_{CE}, V_{BE} – I_B $T_C = 25°C$

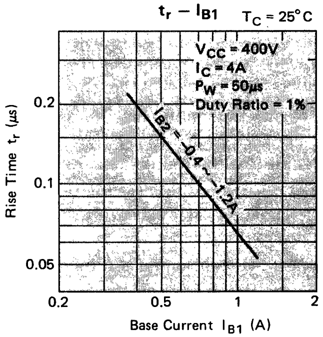

t_{stg} – I_{B2} $T_C = 25°C$


t_r, t_{stg}, t_r – I_C

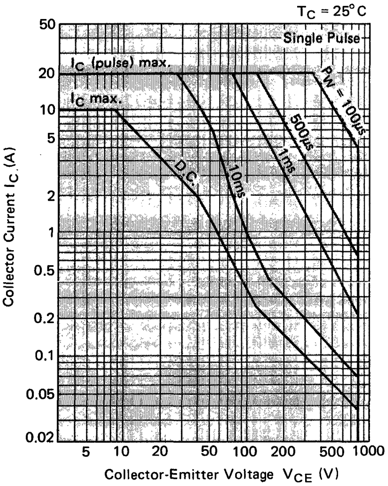

t_f – I_{B2} $T_C = 25°C$

Test Circuit for Switching Time

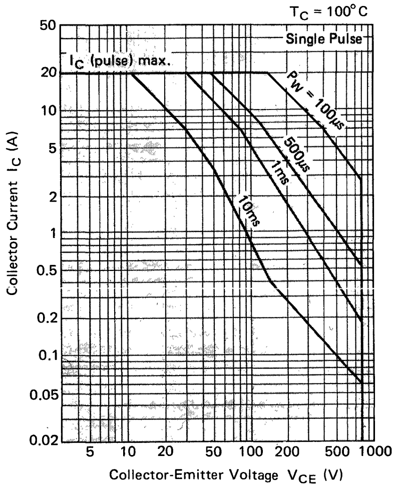



t_r – I_{B1} $T_C = 25°C$

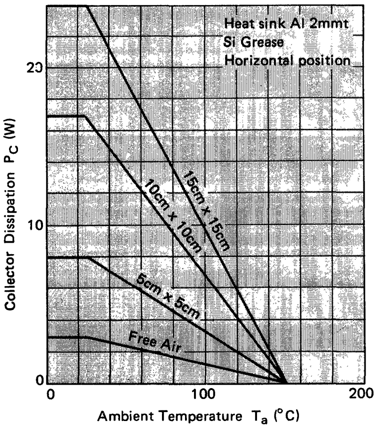
Forward Bias Safe Operating Area — 1



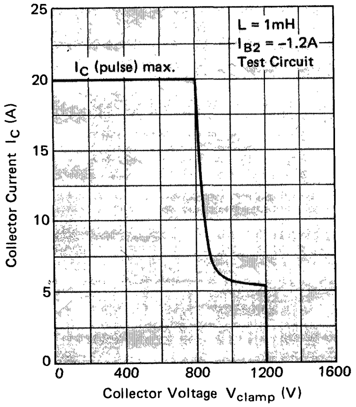
Forward Bias Safe Operating Area — 2



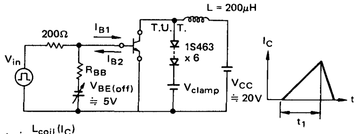
P_C — T_a



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$V_{CEX(SUS)}$: V_{clamp} = 900V

I_C = 7A R_{BB} = 5Ω

I_{B2} = −1.2A

$$t_1 \fallingdotseq \frac{L_{coil}(I_C)}{V_{CC}}$$

January 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3947

Silicon High Speed Power Transistor

2SC3947 500V, 5A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		850	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		500	V
Collector Current	I_C		5	A
	I_{CM}	$P_W \leq 25\mu s$, D.R. $\leq$ 50%	8	
Base Current	I_B		2	A
Collector Power Dissipation	P_C	$T_C = 25°C$	70	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA$, $I_E = 0$	850	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA$, $I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA$, $R_{BE} = \infty\Omega$	500	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 3A$, $I_{B2} = -1A$, $L = 200\mu H$*	700	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 800V$, $I_E = 0$	–	–	100	μA
		$V_{CB} = 800V$, $I_E = 0$, $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V$, $I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V$, $I_C = 2.5A$**	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 2.5A$, $I_B = 0.5A$**	–	0.5	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V$, $I_E = 0$, $f = 1MHz$	–	70	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V$, $I_E = 0.5A$	–	20	–	MHz
Rise Time	t_r	$V_{CC} = 250V$ $I_C = 2.5A$, $2I_{B1} = -I_{B2} = 1A$	–	0.18	0.5	μs
Storage Time	t_{stg}		–	1.50	3.0	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leq 300\mu s$, Duty Ratio $\leq$ 6%

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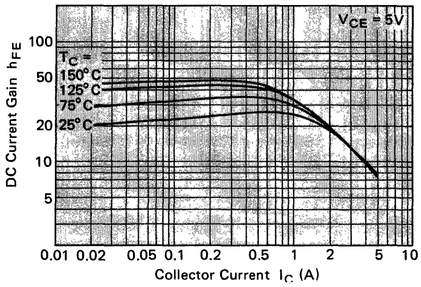
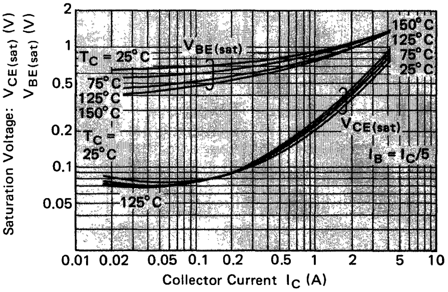
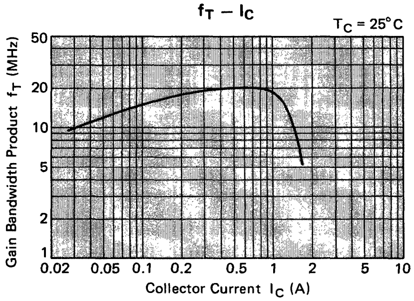
$h_{FE} - I_C$



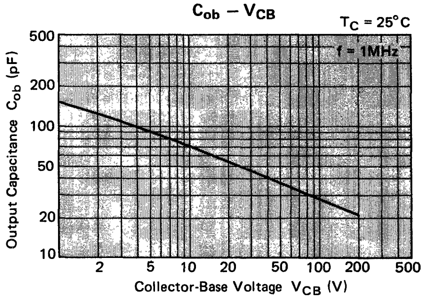
V_{CE} (sat), V_{BE} (sat) $- I_C$



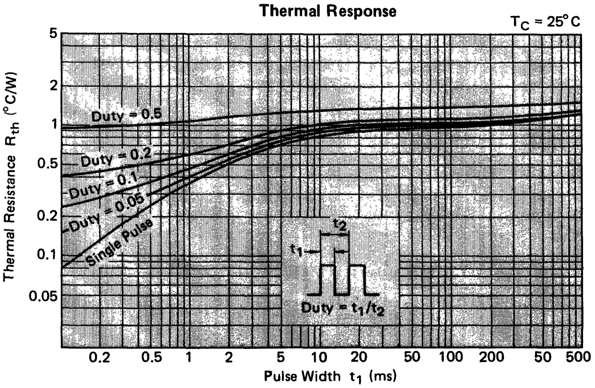
$f_T - I_C$

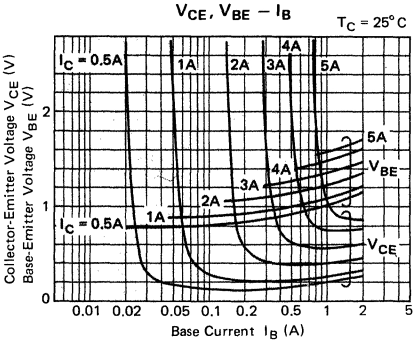


$C_{ob} - V_{CB}$

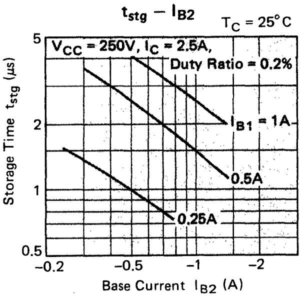


Thermal Response

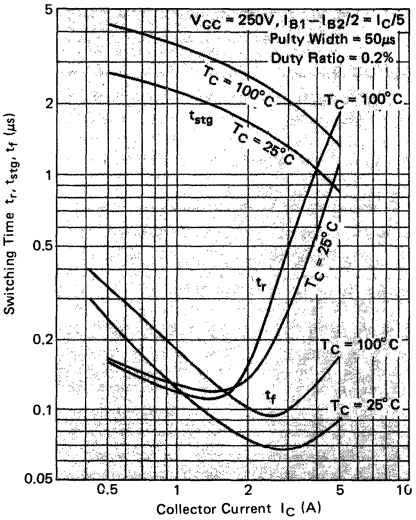


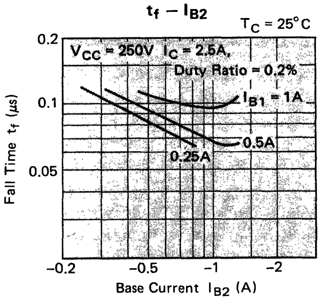


$V_{CE}, V_{BE} - I_B$

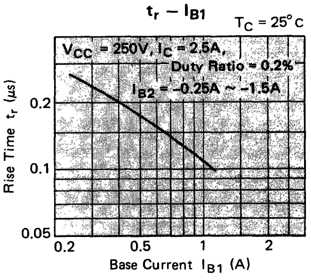


$t_{stg} - I_{B2}$



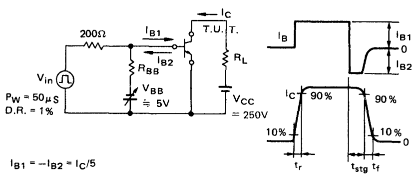


$t_f - I_{B2}$

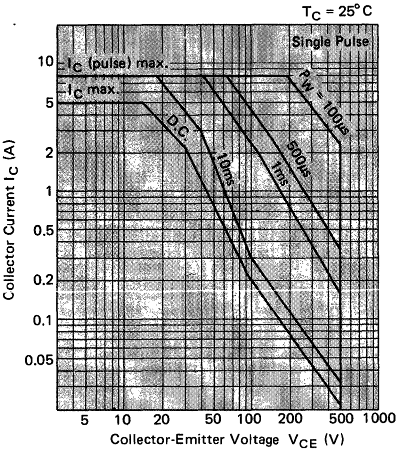


$t_r - I_{B1}$

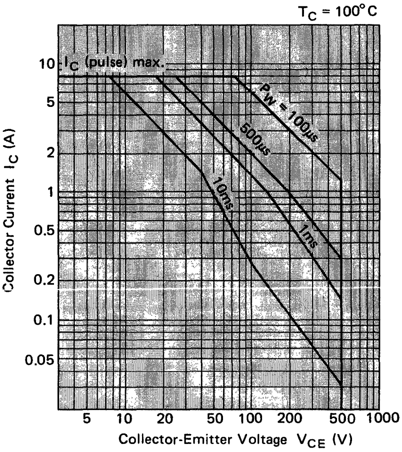
Test Circuit for Switching Time



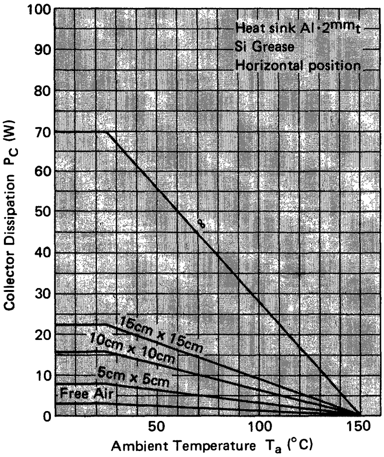
Forward Bias Safe Operating Area — 1



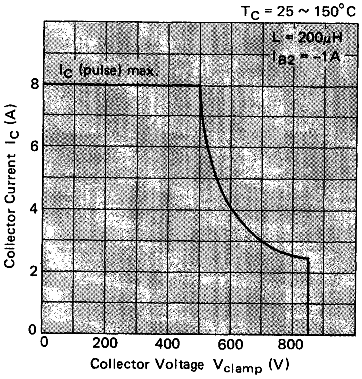
Forward Bias Safe Operating Area — 2



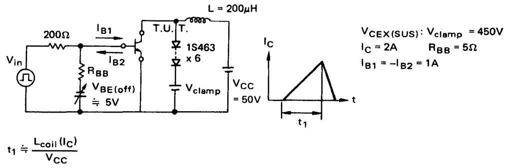
$P_C - T_a$



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



$$t_1 \fallingdotseq \frac{L_{coil}(I_C)}{V_{CC}}$$

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PRODUCT PROFILE

2SC3948

Silicon High Speed Power Transistor

2SC3948 500V, 10A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		850	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		500	V
Collector Current	I_C		10	A
	I_{CM}	$P_W \leqq 25\mu s$, D.R. $\leqq 50\%$	15	
Base Current	I_B		4	A
Collector Power Dissipation	P_C	$T_C = 25°C$	75	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	850	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	500	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 4A, I_{B2} = -2A,$ $L = 200\mu H^*$	700	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 800V, I_E = 0$	–	–	100	μA
		$V_{CB} = 800V, I_E = 0,$ $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 5A^{**}$	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 5A, I_B = 1A^{**}$	–	0.5	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	130	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 1A$	–	20	–	MHz
Rise Time	t_r	$V_{CC} = 250V$ $I_C = 5A, 2I_{B1} = -I_{B2} = 2A^*$	–	0.18	0.5	μs
Storage Time	t_{stg}		–	1.50	2.5	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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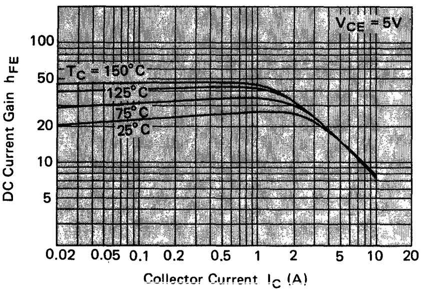
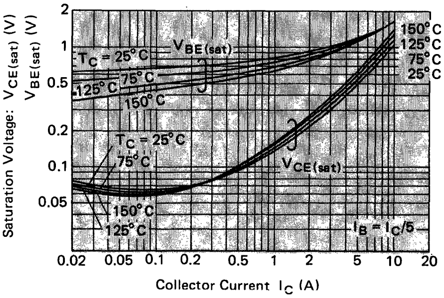
h_{FE} – I_C

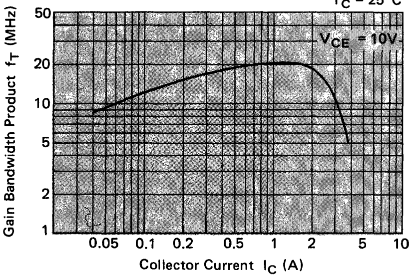


V_{CE} (sat), V_{BE} (sat) – I_C



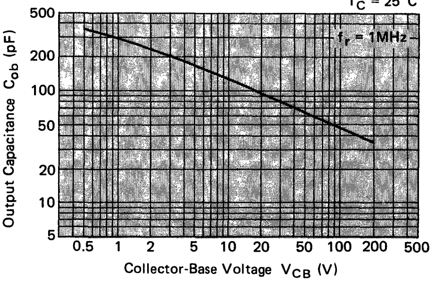
f_T – I_C

T_C = 25°C



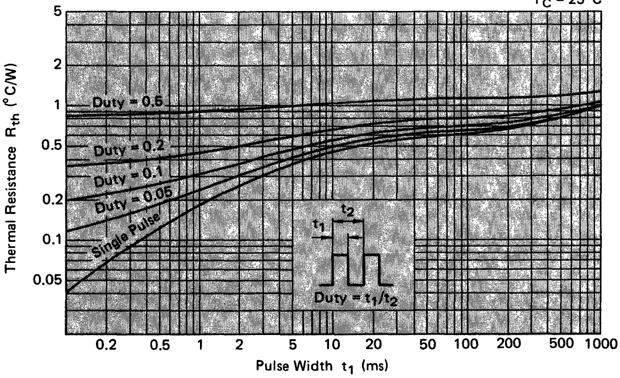
C_{ob} – V_{CB}

T_C = 25°C

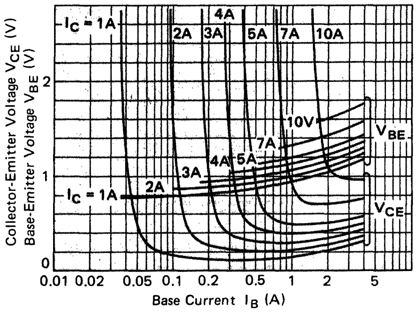


Thermal Response

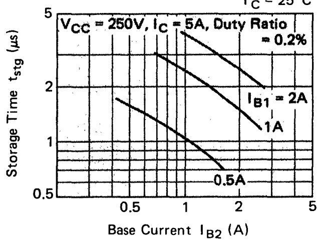
T_C = 25°C



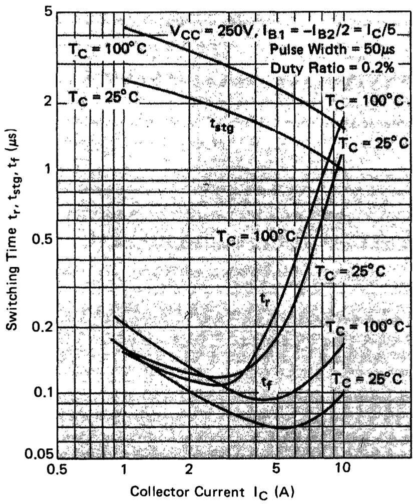
V_{CE}, V_{BE} – I_B



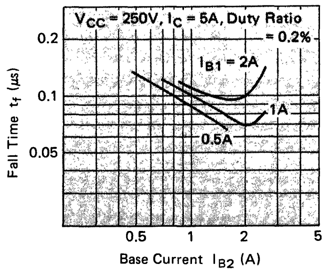
t_{stg} – I_{B2}



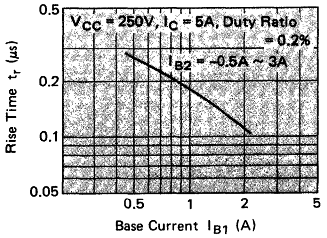
t_r, t_{stg}, t_f – I_C



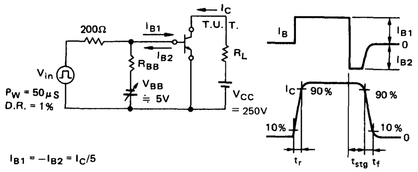
t_f – I_{B2}



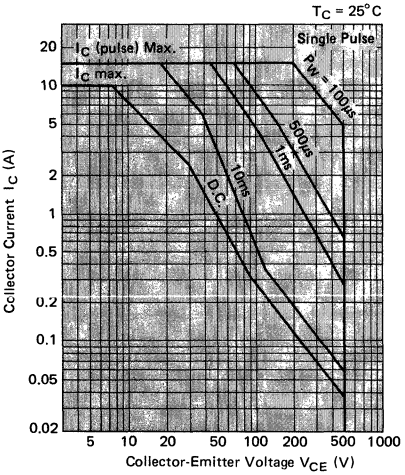
t_r – I_{B1}



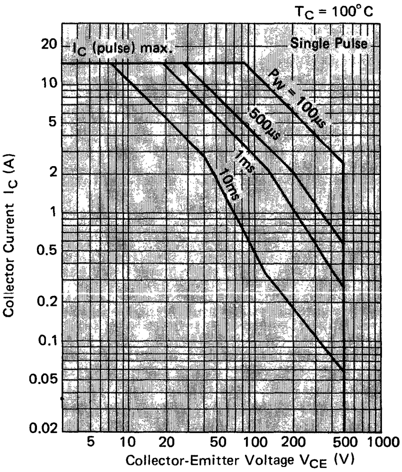
Test Circuit for Switching Time



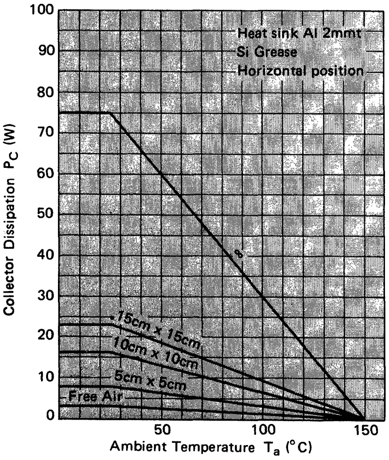
Forward Bias Safe Operating Area — 1



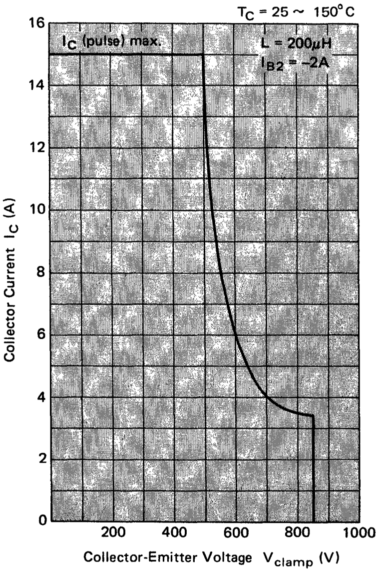
Forward Bias Safe Operating Area — 2



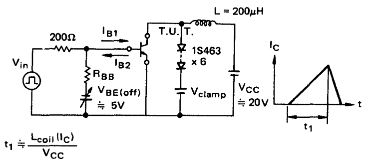
$P_C - T_a$



Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area



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Edition 1.1

FUJITSU

PRODUCT PROFILE

2SC3949

Silicon High Speed Power Transistor

2SC3949 500V, 15A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		850	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		500	V
Collector Current	I_C		15	A
	I_{CM}	$P_W \leqq 25\mu s$, D.R. $\leqq 50\%$	20	
Base Current	I_B		6	A
Collector Power Dissipation	P_C	$T_C = 25°C$	80	W

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	850	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	–	–	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	500	–	–	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 6A, I_{B2} = -4A,$ $L = 200\mu H^*$	700	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 800V, I_E = 0$	–	–	100	μA
		$V_{CB} = 800V, I_E = 0,$ $T_C = 100°C$	–	–	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	–	–	100	μA
DC Currentt Gain	h_{FE}	$V_{CE} = 5V, I_C = 10A^{**}$	10	15	30	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10A, I_B = 2A^{**}$	–	0.5	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	–	260	–	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 2A$	–	20	–	MHz
Rise Time	t_r	$V_{CC} = 250V$ $I_C = 10A, 2I_{B1} = -I_{B2} = 4A^*$	–	0.18	0.5	μs
Storage Time	t_{stg}		–	1.50	3.0	μs
Fall Time	t_f		–	0.07	0.3	μs

*1 Test Circuit **2 Pulse $P_W \leqq 300\mu s$, Duty Ratio $\leqq 6\%$

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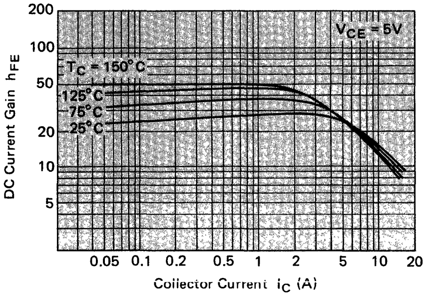
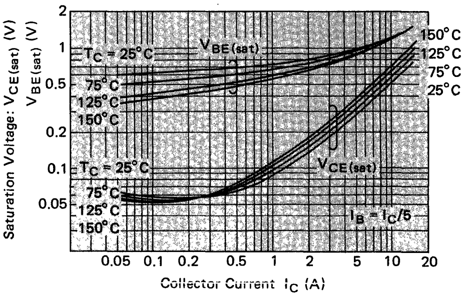
$h_{FE} - I_C$

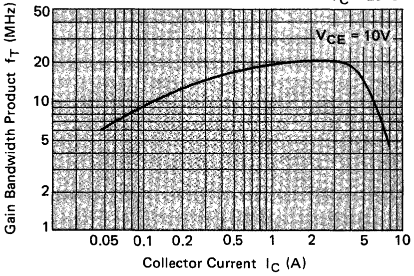


V_{CE} (sat), V_{BE} (sat) $- I_C$



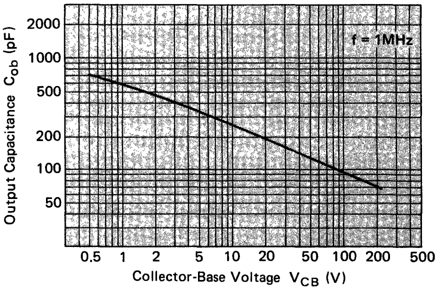
$f_T - I_C$

$T_C = 25°C$



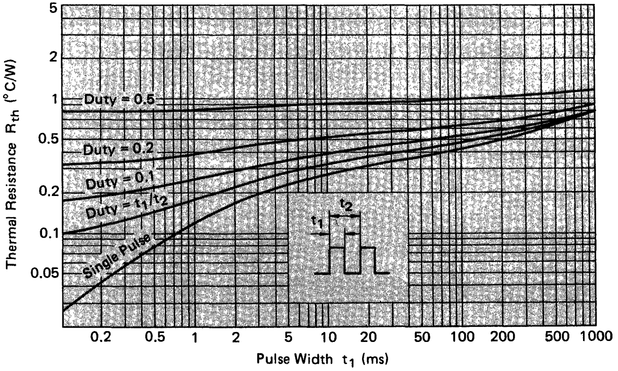
$C_{ob} - V_{CB}$

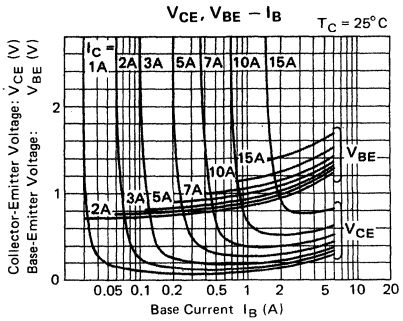
$T_C = 25°C$



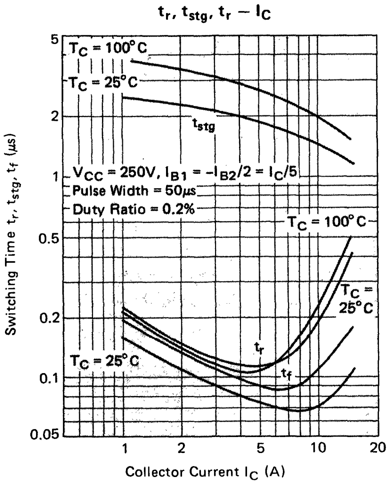
Thermal Response

$T_C = 25°C$



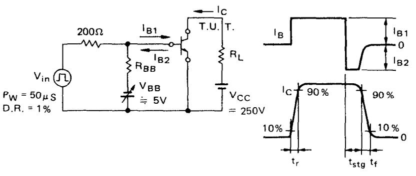


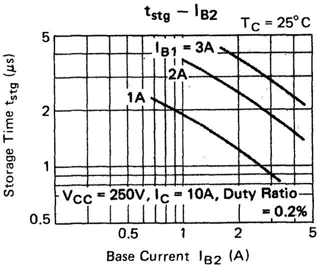
V_{CE}, V_{BE} – I_B



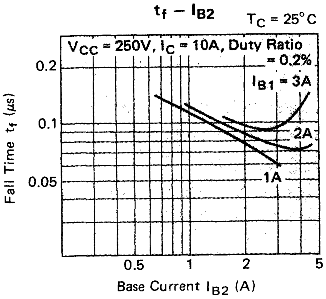
t_r, t_{stg}, t_f – I_C

Test Circuit for Switching Time

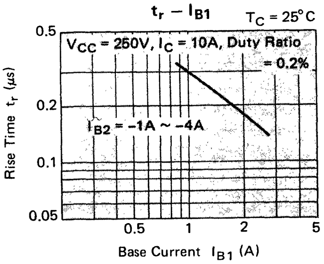




t_{stg} – I_{B2}

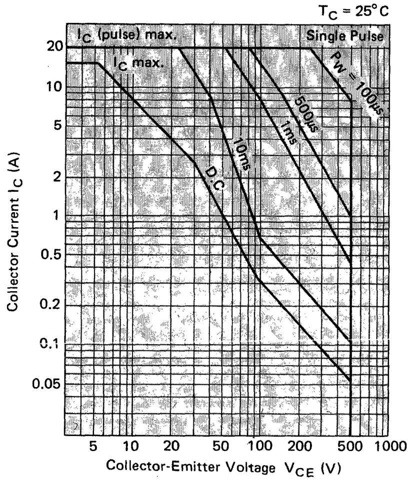


t_f – I_{B2}

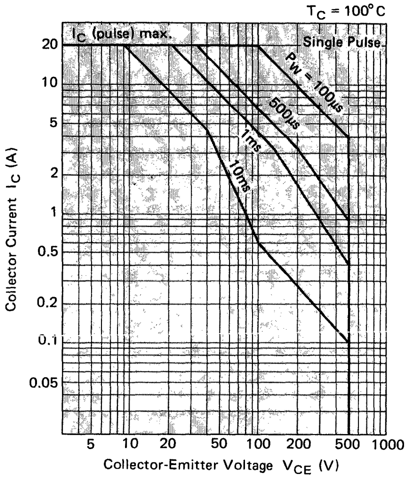


t_r – I_{B1}

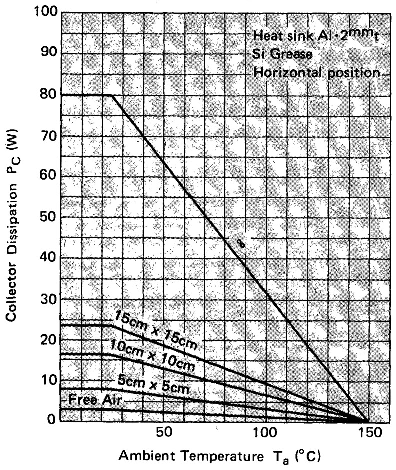
Forward Bias Safe Operating Area — 1



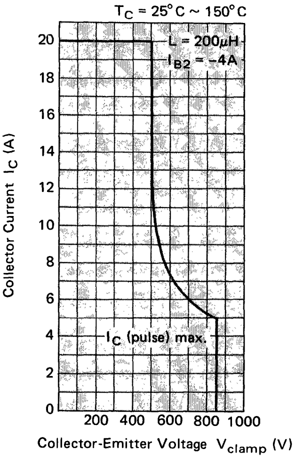
Forward Bias Safe Operating Area — 2



P_C − T_a

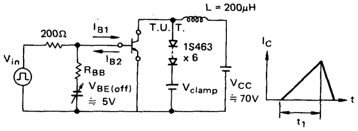


Reverse Bias Safe Operating Area



Test Circuit for $V_{CEX(sus)}$ and Reverse Bias Safe Operating Area

$t_1 \doteqdot \frac{L_{coil}(I_C)}{V_{CC}}$



Section 3

Darlington Transistor Arrays — *At a Glance*

Page	Device	Case (ns)	Polarity	Maximum Ratings	
				V_{CEO} (V)	I_C (A)
3–9	FT5753M	RM–65	NPN	100	± 1.5
	FT5756M		NPN	100	± 1.5
3–11	FT5754M	RM–65	NPN	100	± 3
	FT5757M		NPN	100	± 3
3–13	FT5755M	RM–65	NPN	100	± 5
	FT5758M		NPN	100	± 5
3–15	FT5759M	RM–65	PNP	–100	± 1.5
3–17	FT5760M	RM–65	PNP	–100	± 3
3–19	FT5761M	RM–65	PNP	–100	± 5
3–21	FT5763M	RM–67	NPN	100	± 1.5
	FT5766M		NPN	100	± 1.5
3–23	FT5764M	RM–67	NPN	100	± 3
	FT5767M		NPN	100	± 3
3–25	FT5769M	RM–67	PNP	–100	± 1.5
3–27	FT5770M	RM–67	PNP	–100	± 3
3–29	FT5776M	RM–65	NPN/PNP	100 –100	± 1.5
3–33	FT5777M	RM–65	NPN/PNP	100 –100	± 3
3–37	FT5778M	RM–65	NPN/PNP	100 –100	± 5
3–41	FT5786M	RM–67	NPN/PNP	100 –100	± 1.5
3–45	FT5787M	RM–67	NPN/PNP	100 –100	± 3

INTRODUCTION

DARLINGTON TRANSISTOR ARRAY SERIES

Description

This series is Silicon Darlington Transistor Arrays. Each array consists of 4-Darlington Transistors. The array is packaged in a small plastic 12-pin single in-line package with or without an isolated heatsink.

The series is well suited for motor drive applications where IC outputs must be boosted to drive print hammers. The series are extremely cost effective and space saving compared to using four separate TO-220 type Darlington transistors.

Features

- 4-Circuits included in one package
- Large DC Current Gain
- Large Collector Power Dissipation
- Fastrecovery diode included to absorb fly-back voltage
- Fast switching speed

Application

- Solenoid Drives Printer Head Drives
  Hummer Drives
- Motor Drives
- Amplifiers

Outline of the series

Device Type	Diode*	I_C = 1.5A	I_C = 3.0A	I_C = 5.0A
NPN 2 devices + 2 devices	Yes	FT5753M FT5763M Circuit A	FT5754M FT5764M Circuit A	FT5755M Circuit B
NPN 4 device independent	No	FT5756M FT5766M Circuit C	FT5757M FT5767M Circuit C	FT5758M Circuit D
PNP 4 device independent	No	FT5759M FT5769M Circuit E	FT5760M FT5770M Circuit E	FT5761M Circuit E
NPN + PNP 2NPN + 2PNP independent	No	FT5776M FT5786M Circuit F	FT5777M FT5787M Circuit F	FT5778M Circuit F

* Diode: Fast recovery diode which absorb fly back energy.

DARLINGTON TRANSISTOR ARRAY SERIES

- **Selection Guide**

RM-65 Series

Device Number		V_{CBO} ((V)	V_{CEO} (V)	I_C DC (A)	I_{CP} Pulsed (A)	*P_T Ta = 25°C (W)	*P_T Tc = 25°C (W)	h_{FE} TYP.	PAGE
NPN	FT5753M	150	100	±1.5	±3	4	19	6000	3–9
	FT5754M	150	100	±3	±5	5	21	6000	3–11
	FT5755M	150	100	±5	±8	5	25	4000	3–13
	FT5756M	150	100	±1.5	±3	4	19	6000	3–9
	FT5757M	150	100	±3	±5	5	21	6000	3–11
	FT5758M	150	100	±5	±8	5	25	4000	3–13
PNP	FT5759M	-100	-100	±1.5	±3	4	19	6000	3–15
	FT5760M	-100	-100	±3	±5	5	21	6000	3–17
	FT5761M	-100	-100	±5	±8	5	25	6000	3–19
NPN + PNP	FT5776M	100 -100	100 -100	±1.5	±3	4	19	6000	3–29
	FT5777M	100 -100	100 -100	±3	±5	5	21	6000	3–33
	FT5778M	100 -100	100 -100	±5	±8	5	25	6000	3–37

*4 Darlington Transistors

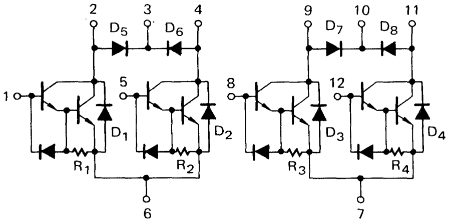
RM-67 Series

Device Number		V_{CBO} (V)	V_{CEO} (V)	I_C DC (A)	I_{CP} Pulsed (A)	*P_T Ta = 25°C (W)	*P_T Tc = 25°C (W)	h_{FE} TYP.	PAGE
NPN	FT5763M	150	100	±1.5	±3	3.5	17	6000	3–21
	FT5764M	150	100	±3	±5	4	19	6000	3–23
	FT5766M	150	100	±1.5	±3	3.5	17	6000	3–21
	FT5767M	150	100	±3	±5	4	19	6000	3–23
PNP	FT5769M	-100	-100	±1.5	±3	3.5	17	6000	3–25
	FT5770M	-100	-100	±3	±5	4	19	6000	3–27
NPN + PNP	FT5786M	100 -100	100 -100	±1.5	±3	3.5	17	6000	3–41
	FT5787M	100 -100	100 -100	±3	±5	4	19	6000	3–45

*4 Darlington Transistors

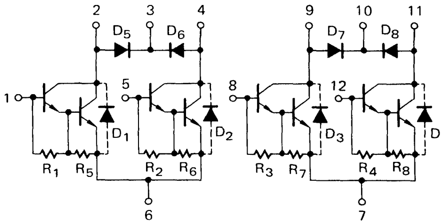
CIRCUIT AND PIN ASSIGNMENT

A



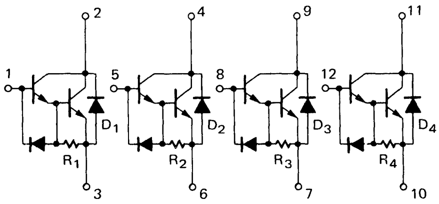
13: FIN (N.C.)
$D_1 \sim D_4$: Flywheel diode
$D_5 \sim D_8$: Fast recovery diode to absorb fly-back voltage
$R_1 \sim R_4$: ~100Ω

B



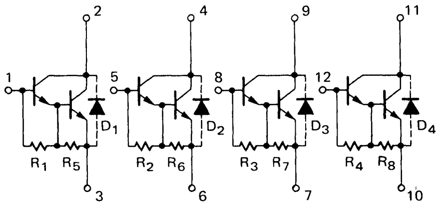
13: FIN (N.C.)
$D_1 \sim D_4$: Flywheel diode
$D_5 \sim D_8$: Fast recovery diode to absorb fly-back voltage
$R_1 \sim R_4$: ≒ 2 kΩ
$R_5 \sim R_8$: ≒ 200Ω

C



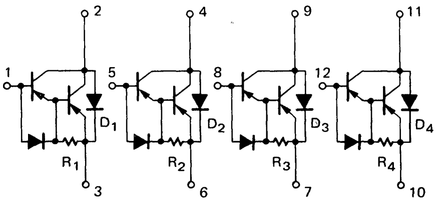
13: Fin (N.C.)
$D_1 \sim D_4$: Flywheel diode
$R_1 \sim R_4$: ~100Ω

D

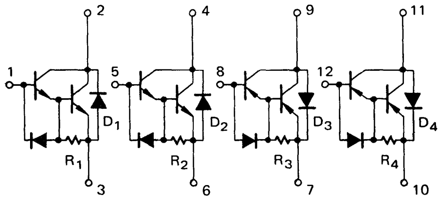


13: Fin (N.C.)
$D_1 \sim D_4$: Flywheel diode
$R_1 \sim R_4$: ≒ 2 kΩ
$R_5 \sim R_8$ ≒ 200Ω

E



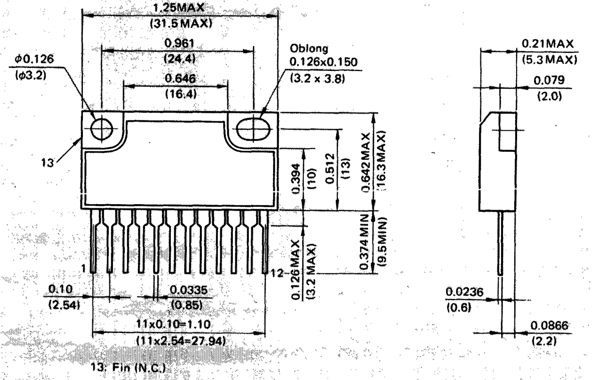
F



13: Fin (N.C.)
$D_1 \sim D_4$: Flywheel diode

PACKAGE DIMENSIONS

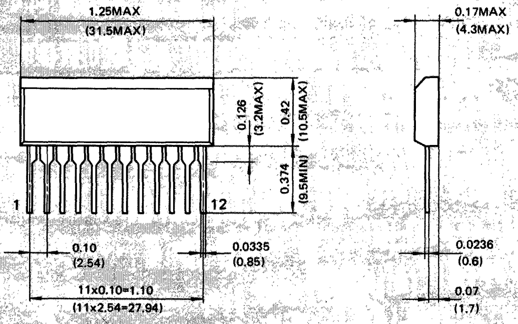
FUJITSU PKG No. RM-65



13: Fin (N.C.)

Unit in inch (mm)

FUJITSU PKG No. RM-67



Unit in inch (mm)

Applications for solenoid drives and motor drives

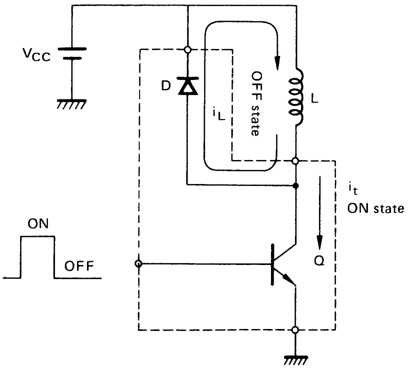
1) General Discription

In solenoid drive applicatins and motor drive applications, the fly-back voltage is generated at the mode of a transistor inductive turn-off.
The darlington transistor array series (FT5753M, FT5754M, FT5755M, FT5763M, FT5764M) can easily absorb the fly-back energy through the fast recovery diodes with the flywheel diode connected between the collector and emitter of the Darlington pair. This guarantees the arrays a very efficient operation.

- Flyback energy absorption circuit

Fig. 1 shows the equivalent drive circuit for a single device of the DLTARY.
During the turn-on mode of the darlington transistor (Q), the current (it) flows through the inductive load (L).
During the turn-off of the darlington transistor (Q), the fly-back energy which is stored in the inductive load (L) is absorbed by current (i_L) which flows through the fast recovery diode.

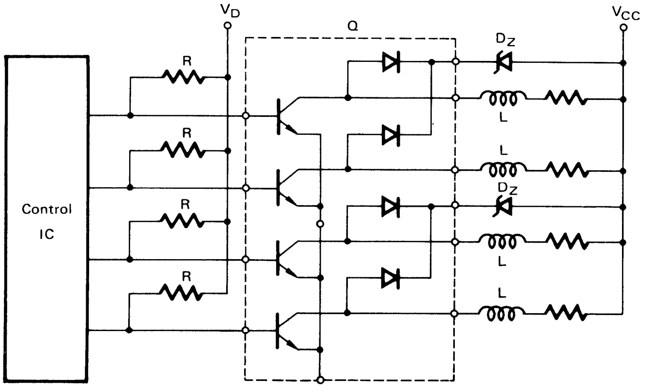
Fig. 1—Circuit for absorbing fly-back energy



2) Solenoid drive circuit

Four solenoids can be driven by one DLTARY.

Fig. 2— Solenoid drive circuit



Q : DLTARY
L : Solenoid
D_Z : Speed-up zener diode
R : Drive current limiting resistance
V_{CC} : Collector supply voltage
V_D : Drive voltage

3) Motor Drive

3—1) Driving form (ex. 4-phase motor)

Motors may be driven in either a unipolar or (Fig.-3(a)) bipolar manner (Fig.-3(b)). The current in uni-polar mode flows in only one direction while the current in bi-polar mode flows in both directions.

Fig. 3—(a) Uni-polar driving form
* Easy Construction

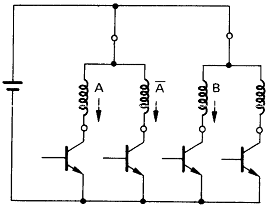
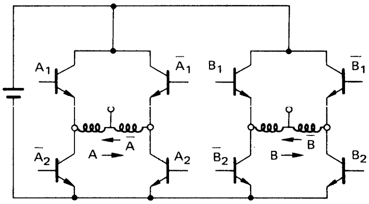
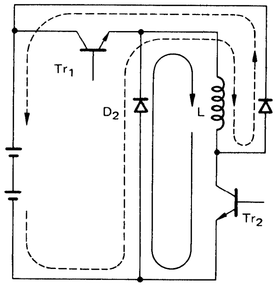


Fig. 3—(b) Bipolar driving form
* Large Output Torque



3—2) Principle circuit for pulse width modulate drive

Fig. 4— Principle circuit for pulse width modulate drive



The output current is controlled by the pulse width of modulator transistor (Tr_1), when the PWM transistor (Tr_1) is in the off-state and the darlington transistor (Tr_2) is in the on-state, the current flows through the fast recovery diode (D_2). (Solid line)

In this mode the fast recovery diode operates similarly to a flywheel diode.

When both the PWM transistor (Tr_1) and darlington transistor are in the off-state current flows through the flywheel diode. (Dashed line)

In this mode, the current flows back to the DC power supply to improve the operating efficiency.

Example of Pulse Width Modulate Drive

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PRODUCT PROFILE

FT5753M, FT5756M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		–55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		150	V
Emitter to Base Voltage		V_{EBO}		5	V
Collector to Emitter Voltage		V_{CEO}		100	V
Collector Current	(Continuous)	I_C		±1.5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±3	A
Base Current (Continuous)		I_B		0.1	A
Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, D.R. $\leqq 25\%$ (*)	1.5	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse (*)	3	A
Diode Reverse Voltage		V_R	Pin 3 – Pin 2, 4. Pin 10 – Pin 9, 11 (*)	110	V
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	1.9	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	4	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	19	W

(*) Fast recovery Diode DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\ \mu A,\ I_E = 0$	150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μA
DC Current Gain	h_{FE1}	$I_C = 0.75$ A, $V_{CE} = 5$ V (**)	2000	6000	15000	–
	h_{FE2}	$I_C = 1.5$ A, $V_{CE} = 5$ V (**)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 0.75$A, $I_B = 1.5$ mA (**)	–	1.1	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V (***)	–	0.5	–	μs
Storage Time	t_{stg}	$I_C = 0.75$A	–	2.1	–	μs
Fall Time	t_f	$I_{B1} = -I_{B2} = 1.5$ mA	–	0.4	–	μs

Single Fastrecovery Diode Operation (FT5753M Only)

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	$I_F = 100$ mA	–	–	1.0	V
Reverse Current	I_R	$V_R = 100$ V	–	–	5	μA
Reverse Voltage	V_R	$I_R = 10\ \mu A$	110	–	–	V

(**) Pulsed Pulse Width $\leqq 300\ \mu s$
Duty Ratio $\leqq 6\%$

(***) Pulsed Pulse Width = 50 μs
Duty Ratio $\leqq 1\%$

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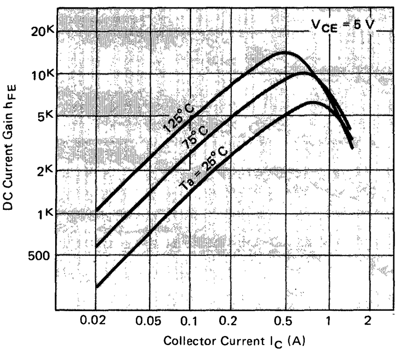
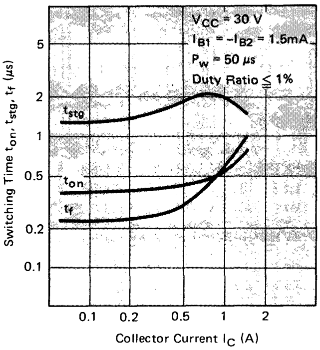
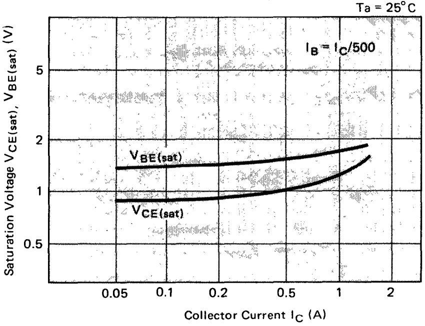
DC CURRENT GAIN



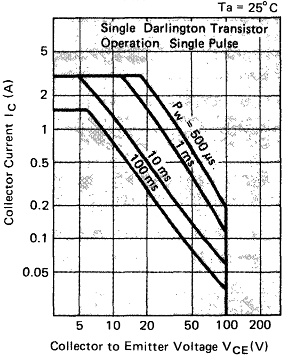
SWITCHING TIME



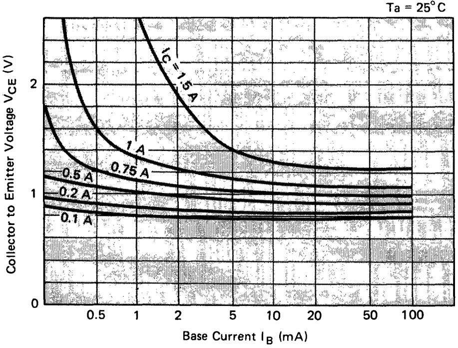
SATURATION VOLTAGE



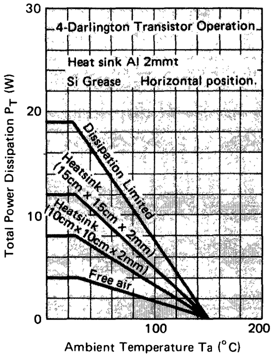
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5754M, FT5757M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		150	V
Emitter to Base Voltage		V_{EBO}		5	V
Collector to Emitter Voltage		V_{CEO}		100	V
Collector Current	(Continuous)	I_C		±33	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±5	A
Base Current (Continuous)		I_B		0.2	A
Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, D.R. $\leqq 25\%$ (*)	3	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse (*)	5	A
Diode Reverse Voltage		V_R	Pin 3 – Pin 2, 4. Pin 10 – Pin 9, 11 (*)	110	V
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	2.3	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	21	W

(*) Fast recovery Diode DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\ \mu A$, $I_E = 0$	150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μA
DC Current Gain	h_{FE1}	$I_C = 1.5$ A, $V_{CE} = 5V$ (**)	2000	6000	15000	–
	h_{FE2}	$I_C = 3.0$ A, $V_{CE} = 5V$ (**)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 1.5$ A, $I_B = 3$ mA (**)	–	1.2	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.7	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V (***)	–	0.6	–	μs
Storage Time	t_{stg}	$I_C = 1.5$ A	–	1.8	–	μs
Fall Time	t_f	$I_{B1} = I_{B2} = 3$ mA	–	0.6	–	μs

Single Fastrecovery Diode Operation (FT5754M Only)

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	$I_F = 100$ mA	–	–	1.0	V
Reverse Current	I_R	$V_R = 100$ V	–	–	5	μA
Reverse Voltage	V_R	$I_R = 10\ \mu A$	110	–	–	V

(**) Pulsed Pulse Width $\leqq 300\ \mu s$
Duty Ratio $\leqq 6\%$

(***) Pulsed Pulse Width = 50 μs
Duty Ratio $\leqq 1\%$

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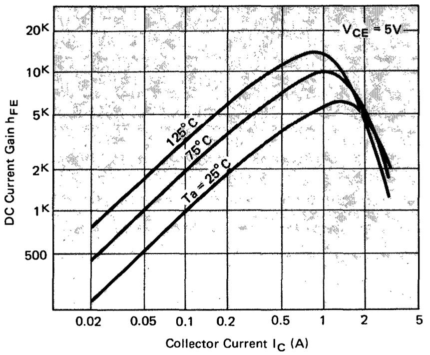
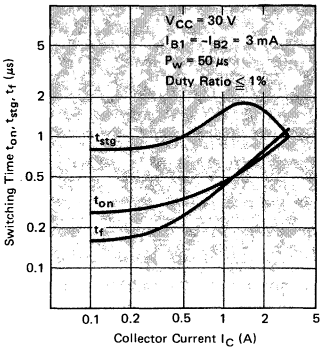
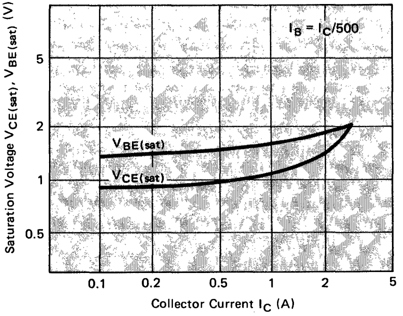
DC CURRENT GAIN



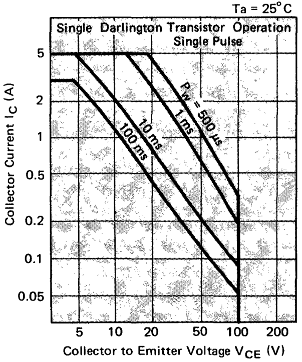
SWITCHING TIME



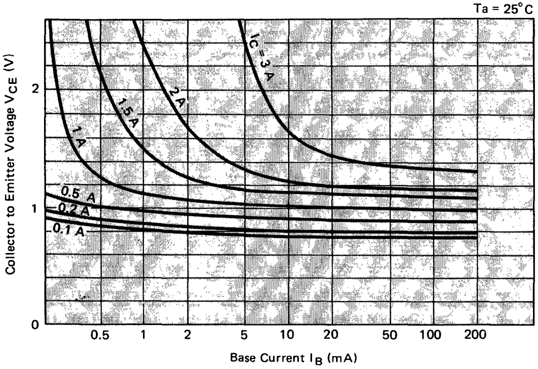
SATURATION VOLTAGE



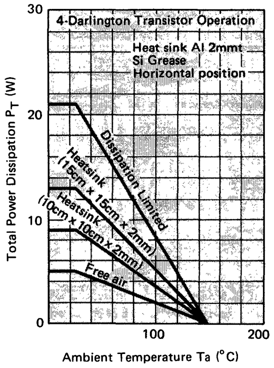
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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Edition 1.1

FUJITSU

PRODUCT PROFILE

FT5755M, FT5758M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		150	V
Emitter to Base Voltage		V_{EBO}		7	V
Collector to Emitter Voltage		V_{CEO}		100	V
Collector Current	(Continuous)	I_C		5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	8	A
Base Current (Continuous)		I_B		0.5	A
Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, D.R. $\leqq 25\%$ (*)	5	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse (*)	8	A
Diode Reverse Voltage		V_R	Pin 3 – Pin 2, 4. Pin 10 – Pin 9, 11 (*)	110	V
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	2.5	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	25	W

(*) Fast recovery Diode DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\,\mu A$, $I_E = 0$	150	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 25$ mA, $R_{BE} = \infty$	100	–	–	V
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 7V$, $I_C = 0$	–	–	5	mA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$ (**)	–	–	1	μA
DC Current Gain	h_{FE1}	$I_C = 3A$, $V_{CE} = 2V$ (**)	2000	4000	15000	–
	h_{FE2}	$I_C = 5A$, $V_{CE} = 2V$ (**)	5000	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 3A$, $I_B = 3$ mA (**)	–	1.2	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 50$ V (***) $I_C = 3A$ $I_{B1} = -I_{B2} = 3$ mA	–	1.0	–	μs
Storage Time	t_{stg}		–	2.0	–	μs
Fall Time	t_f		–	1.0	–	μs

Single Fastrecovery Diode Operation (FT5755M Only)

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	$I_F = 1A$	–	–	1.0	V
Reverse Current	I_R	$V_R = 100$ V	–	–	10	μA
Reverse Voltage	V_R	$I_R = 15\,\mu A$	110	–	–	V

(**) Pulsed Pulse Width $\leqq 300\,\mu s$
Duty Ratio $\leqq 6\%$

(***) Pulsed Pulse Width = $50\,\mu s$
Duty Ratio $\leqq 1\%$

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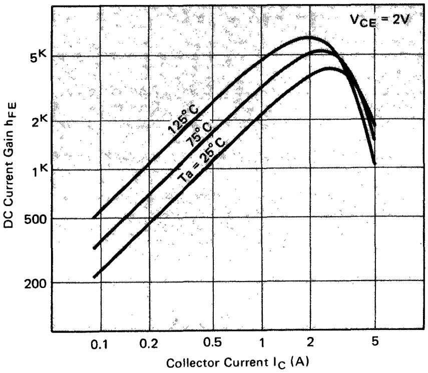
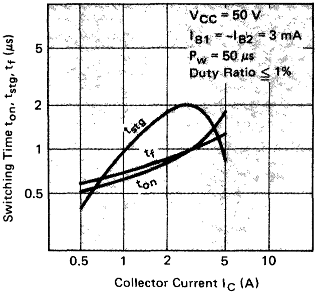
DC CURRENT GAIN



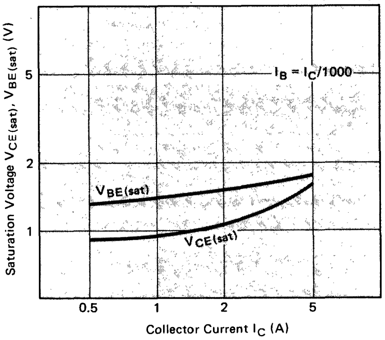
SWITCHING TIME

Ta = 25°C



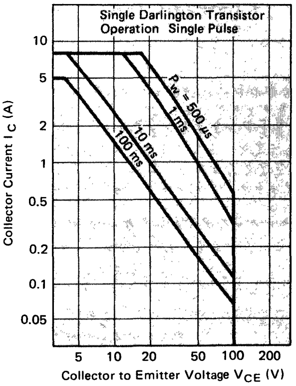
SATURATION VOLTAGE

Ta = 25°C



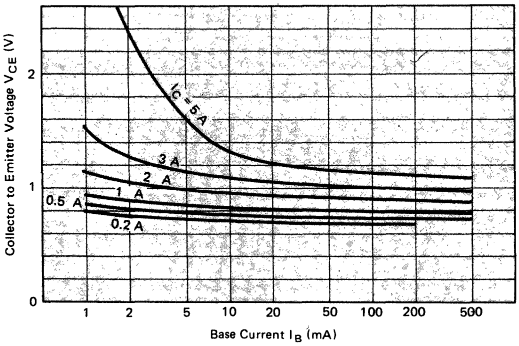
FORWARD BIAS SAFE OPERATING AREA

Ta = 25°C

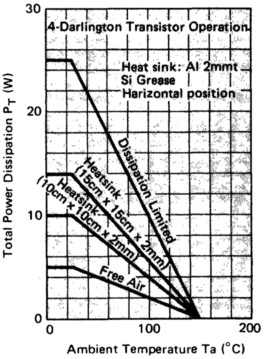


COLLECTOR SATURATION REGION

Ta = 25°C



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5759M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		-100	V
Emitter to Base Voltage		V_{EBO}		-5	V
Collector to Emitter Voltage		V_{CEO}		-100	V
Collector Current	(Continuous)	I_C		±1.5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±3	A
Base Current (Continuous)		I_B		-0.1	A
Isolation Voltage		V_{iso}	Pin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT, operation	1.9	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	4	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	19	W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\,\mu A$, $I_E = 0$	-150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -80 mA$, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90V$, $I_E = 0$	–	–	-10	μA
DC Current Gain	h_{FE1}	$I_C = -0.75$ A, $V_{CE} = -5$ V (*)	2000	6000	15000	–
	h_{FE2}	$I_C = -1.5$ A, $V_{CE} = -5$ V (*)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -0.75$ A, $I_B = -1.5$ mA (*)	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.6	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V (**) $I_C = -0.75$ A $I_{B1} = -I_{B2} = -1.5$mA	–	0.5	–	μs
Storage Time	t_{stg}		–	1.4	–	μs
Fall Time	t_f		–	0.4	–	μs

(*) Pulsed Pulse Width ≦ 300 μs
Duty Ratio ≦ 6%

(**) Pulsed Pulse width = 50 μs
Duty Ratio ≦ 1%

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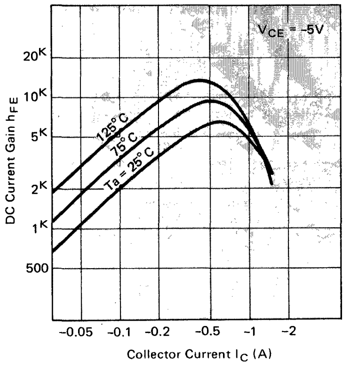
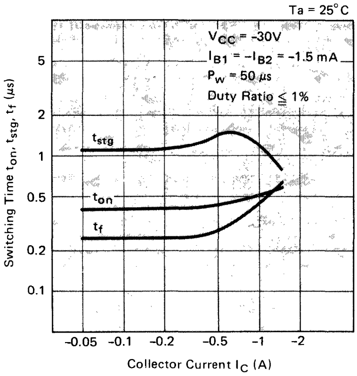
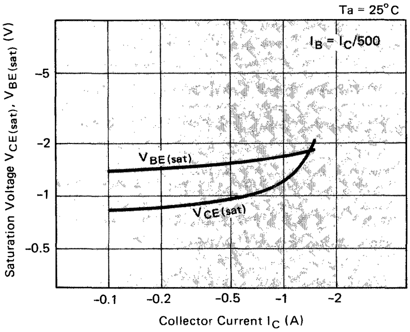
DC CURRENT GAIN



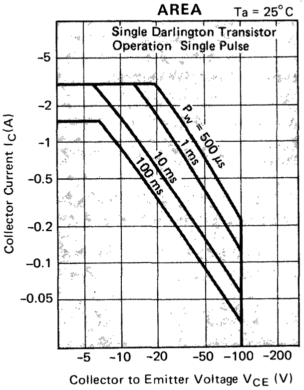
SWITCHING TIME



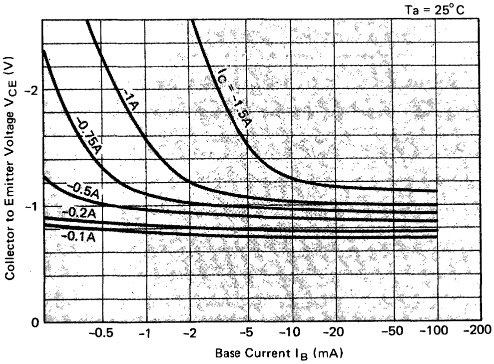
SATURATION VOLTAGE



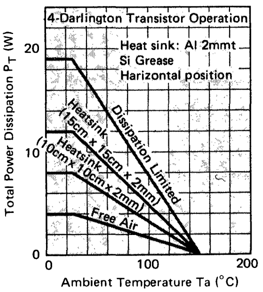
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5760M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		-100	V
Emitter to Base Voltage		V_{EBO}		-5	V
Collector to Emitter Voltage		V_{CEO}		-100	V
Collector Current	(Continuous)	I_C		±3.0	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±5.0	A
Base Current (Continuous)		I_B		-0.2	A
Isolation Voltage		V_{iso}	Pin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	2.3	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	21	W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\,\mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -90$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90$ V, $I_E = 0$	–	–	-10	µA
DC Current Gain	h_{FE1}	$I_C = -1.5$ A, $V_{CE} = -5$ V (**)	2000	6000	15000	–
	h_{FE2}	$I_C = -3$ A, $V_{CE} = -5$ V (**)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.5$A, $I_B = -3$mA (**)	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V (***)	–	0.5	–	µs
Storage Time	t_{stg}	$I_C = -1.5$ A	–	1.3	–	µs
Fall Time	t_f	$I_{B1} = -I_{B2} = -3$ mA	–	0.5	–	µs

(**) Pulsed Pulse Width ≦ 300 µs
Duty Ratio ≦ 6%

(***) Pulsed Pulse Width = 50 µs
Duty Ratio ≦ 1%

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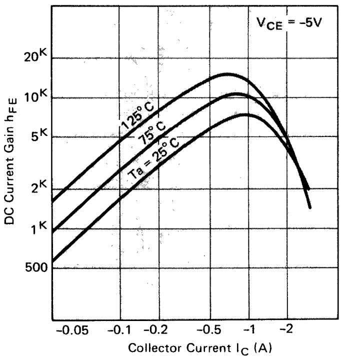
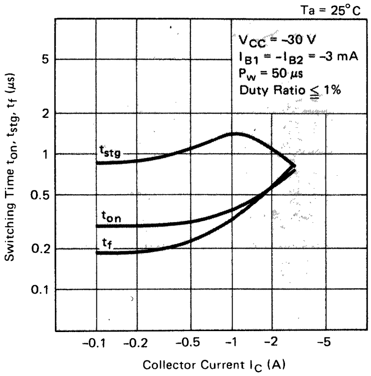
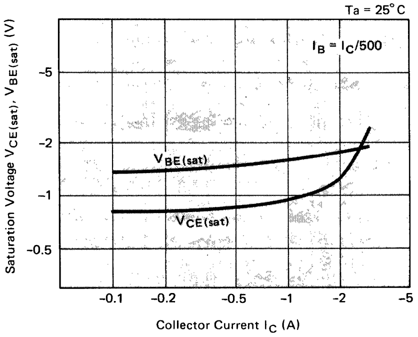
DC CURRENT GAIN



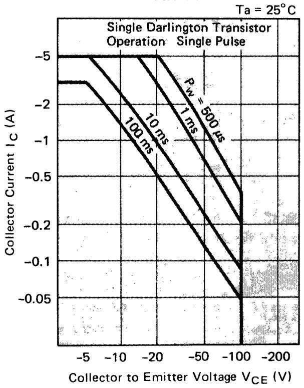
SWITCHING TIME



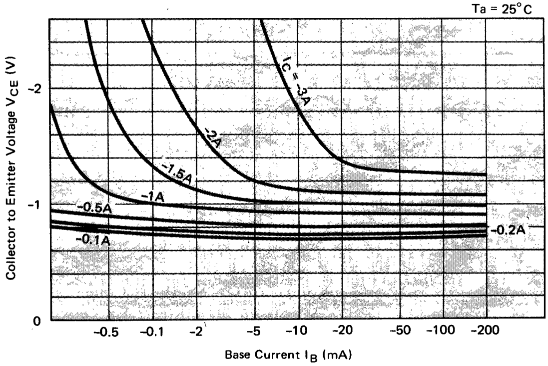
SATURATION VOLTAGE



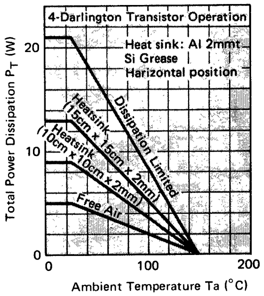
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5761M

Silicon Darlington Transistor Array

FT5761M

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		-100	V
Emitter to Base Voltage		V_{EBO}		-5	V
Collector to Emitter Voltage		V_{CEO}		-100	V
Collector Current	(Continuous)	I_C		±5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq$ 50%	±8	A
Base Current (Continuous)		I_B		-0.5	A
Isolation Voltage		V_{iso}	Pin 13 – Pin 1 ~ 12	500	$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT, operation	2.5	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	25	W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = -100 µ A, I_E = 0	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = -150 mA, I_C = 0	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = -25 mA, $R_{BE} = \infty$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = -90 V, I_E = 0	–	–	-10	µA
DC Current Gain	h_{FE1}	I_C = -3 A, V_{CE} = -5 V (*)	2000	6000	15000	–
	h_{FE2}	I_C = -5 A, V_{CE} = -5 V (*)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = -3 A, I_B = -6 mA (*)	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	V_{CC} = -30 V (**)	–	0.4	–	µs
Storage Time	t_{stg}	I_C = -3 A	–	1.2	–	µs
Fall Time	t_f	$I_{B1} = -I_{B2}$ = -6 mA	–	0.5	–	µs

(*) Pulsed Pulse Width $\leqq$ 300 µs
Duty Ratio $\leqq$ 6%

(**) Pulsed Pulse Width = 50 µs
Duty Ratio $\leqq$ 1%

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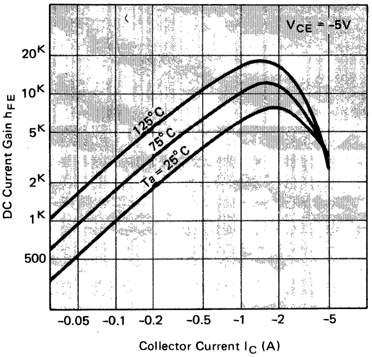
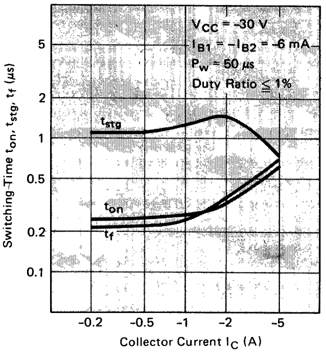
DC CURRENT GAIN

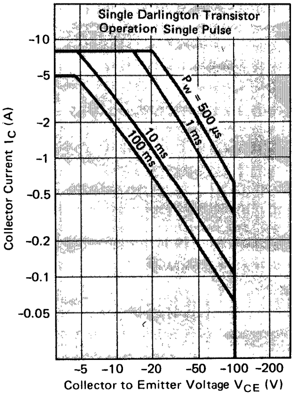


SWITCHING TIME



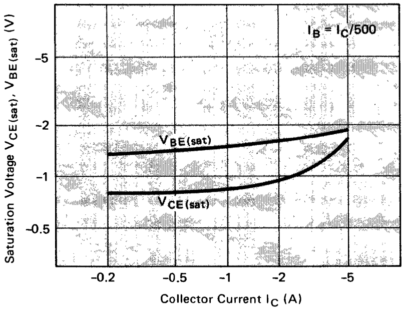
FORWARD BIAS SAFE OPERATING AREA

Ta = 25°C



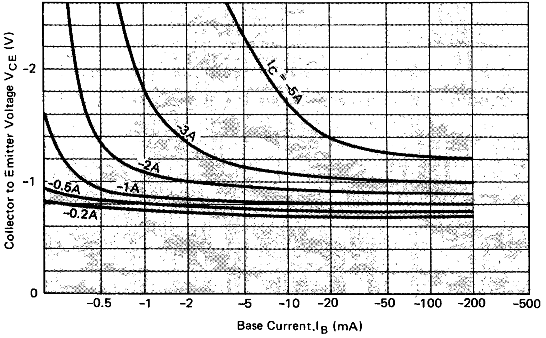
SATURATION VOLTAGE

Ta = 25°C

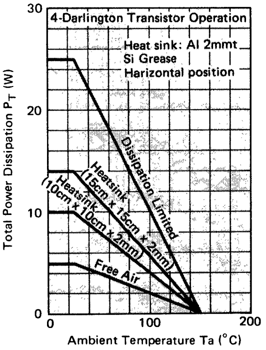


COLLECTOR SATURATION REGION

Ta = 25°C



POWER DISSIPATION DERATING



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Edition 1.1

PRODUCT PROFILE

FT5763M, FT5766M

Silicon Darlington Transistor Array

FT5763M, FT5766M

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		150	V
Emitter to Base Voltage		V_{EBO}		5	V
Collector to Emitter Voltage		V_{CEO}		100	V
Collector Current	(Continuous)	I_C		±1.5	A
	(Pulsed)	I_{cp}	$P_W \leq 1$ ms, D.R. $\leq 50\%$	±3	A
Base Current (Continuous)		I_B		0.1	A
Diode Forward Current		I_{FM}	$P_W \leq 0.5$ ms, D.R. $\leq 15\%$ (*)	0.5	A
		I_{FSM}	$P_W \leq 100$ ms, Single Pulse (*)	3	A
Diode Reverse Voltage		V_R	Pin 3 – Pin 2, 4. Pin 10 – Pin 9, 11 (*)	110	V
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	1.5	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	3.5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	17	W

(*) Fast recovery Diode DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 100\ \mu A$, $I_E = 0$	150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μA
DC Current Gain	h_{FE1}	$I_C = 0.75A$, $V_{CE} = 5$ V (**)	2000	6000	15000	–
	h_{FE2}	$I_C = 1.5A$, $V_{CE} = 5$ V (**)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 0.75A$, $I_B = 1.5$ mA (**)	–	1.1	1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V (***) $I_C = 0.75$ A $I_{B1} = -I_{B2} = 1.5$ mA	–	0.5	–	μs
Storage Time	t_{stg}		–	2.1	–	μs
Fall Time	t_f		–	0.4	–	μs

Single Fast Recovery Diode Operation (FT5763M Only)

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	$I_F = 100$ mA	–	–	1.0	V
Reverse Current	I_R	$V_R = 100$ V	–	–	5	μA
Reverse Voltage	V_R	$I_R = 10\ \mu A$	110	–	–	V

(**) Pulsed Pulse Width $\leq 300\ \mu s$
Duty Ratio $\leq 6\%$

(***) Pulse Pulse Width = 50 μs
Duty Ratio $\leq 1\%$

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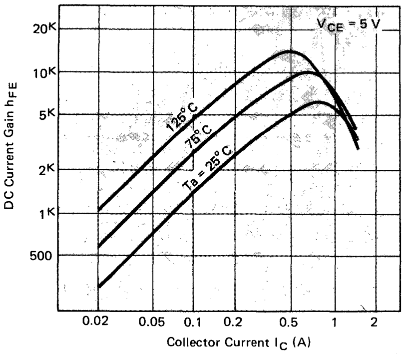
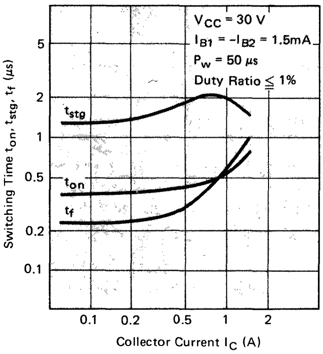
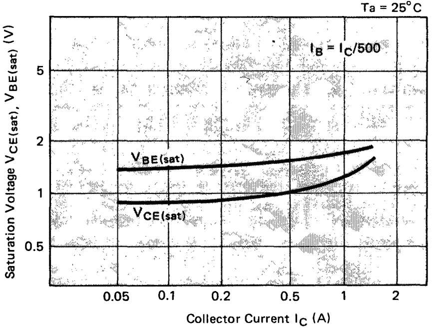
DC CURRENT GAIN



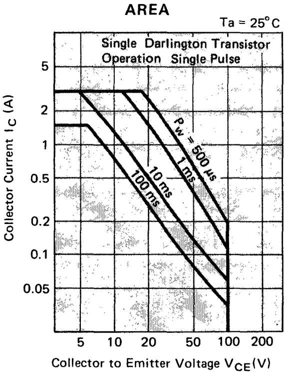
SWITCHING TIME



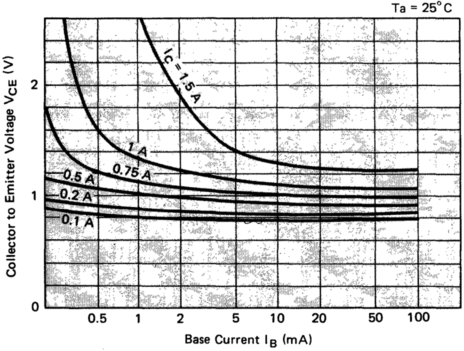
SATURATION VOLTAGE



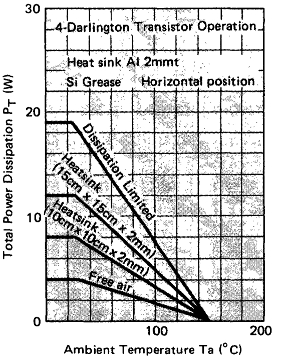
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5764M, FT5767M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		150	V
Emitter to Base Voltage		V_{EBO}		5	V
Collector to Emitter Voltage		V_{CEO}		100	V
Collector Current	(Continuous)	I_C		±3	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq$ 30%	±5	A
Base Current (Continuous)		I_B		0.2	A
Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, D.R. $\leqq$ 15% (*)	3	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse (*)	5	A
Diode Reverse Voltage		V_R	Pin 3 – Pin 2,4. Pin 10 – Pin 9,11 (*)	110	V
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	1.7	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	4	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	19	W

(*) Fast recovery Diode DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100 μA, I_E = 0	150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 70 mA, I_C = 0	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 10 mA, $R_{BE} = \infty$	100	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = 100 V, I_E = 0	–	–	10	μA
DC Current Gain	h_{FE1}	I_C = 1.5 A, V_{CE} = 5 V (**)	2000	6000	15000	–
	h_{FE2}	I_C = 3.0 A, V_{CE} = 5 V (**)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 1.5 A, I_B = 3 mA (**)	–	1.2	1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	1.7	2.0	V
Turn-On Time	t_{on}	V_{CC} = 30 V (***) I_C = 1.5 A $I_{B1} = -I_{B2}$ = 3 mA	–	0.6	–	μs
Storage Time	t_{stg}		–	1.8	–	μs
Fall Time	t_f		–	0.6	–	μs

Single Fast Recovery Diode Operation (FT5764M Only)

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Forward Voltage	V_F	I_F = 100 mA	–	–	1.0	V
Reverse Current	I_R	V_R = 100 V	–	–	5	μA
Reverse Voltage	V_R	I_R = 10 μA	110	–	–	V

(**) Pulsed Pulse Width $\leqq$ 300 μs
Duty Ratio $\leqq$ 6%

(***) Pulsed Pulse Width = 50 μs
Duty Ratio $\leqq$ 1%

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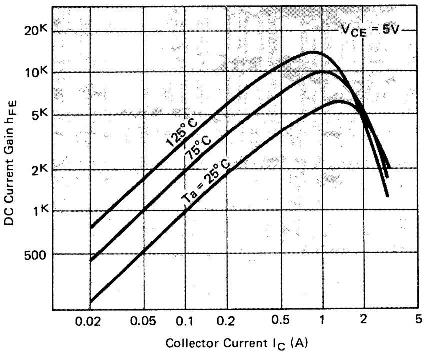
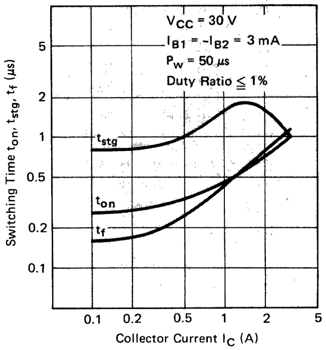
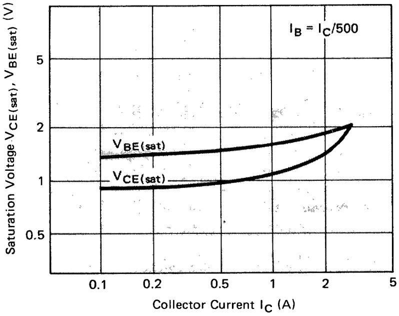
DC CURRENT GAIN



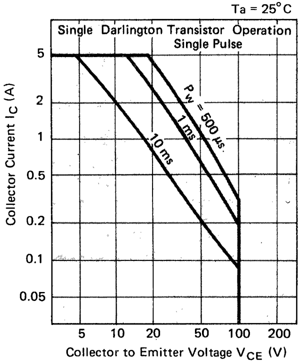
SWITCHING TIME



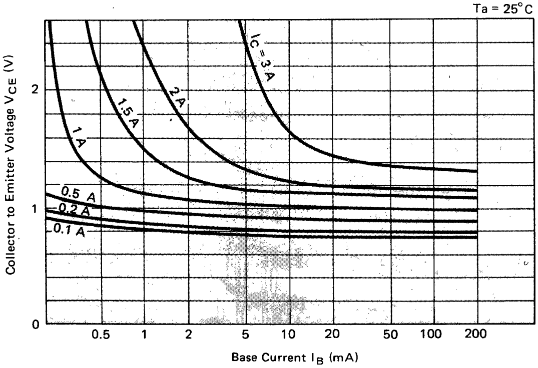
SATURATION VOLTAGE



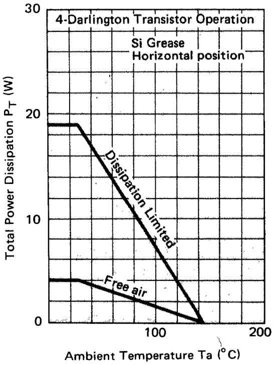
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5769M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		-100	V
Emitter to Base Voltage		V_{EBO}		-5	V
Collector to Emitter Voltage		V_{CEO}		-100	V
Collector Current	(Continuous)	I_C		±1.5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 30\%$	±3	A
Base Current (Continuous)		I_B		-0.1	A
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	1.5	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	3.5	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	17	W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\ \mu A$, $I_E = 0$	-150	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -80$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90$ V, $I_E = 0$	–	–	-10	µA
DC Current Gain	h_{FE1}	$I_C = -0.75$ A, $V_{CE} = -5$ V (*)	2000	6000	15000	–
	h_{FE2}	$I_C = -1.5$ A, $V_{CE} = -5$ V (*)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -0.75$ A, $I_B = -1.5$ mA(*)	–	-1.1	-1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	-1.6	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V (**) $I_C = -0.75$ A $I_{B1} = -I_{B2} = -1.5$ mA	–	0.5	–	µs
Storage Time	t_{stg}		–	1.4	–	µs
Fall Time	t_f		–	0.4	–	µs

(*) Pulsed Pulse Width $\leqq 300\ \mu s$
Duty Ratio $\leqq 6\%$

(**) Pulsed Pulse width = 50 µs
Duty Ratio $\leqq 1\%$

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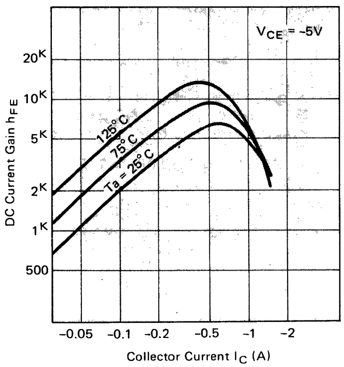
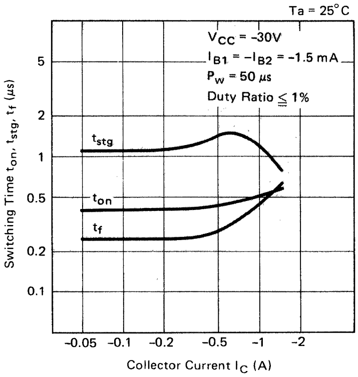
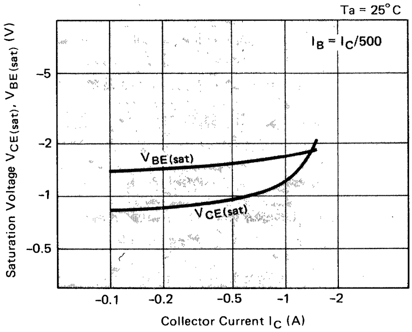
DC CURRENT GAIN



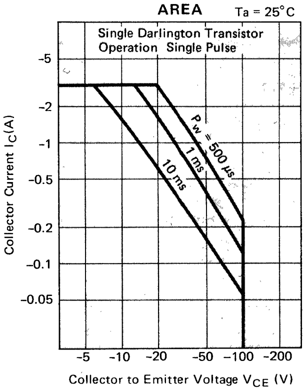
SWITCHING TIME



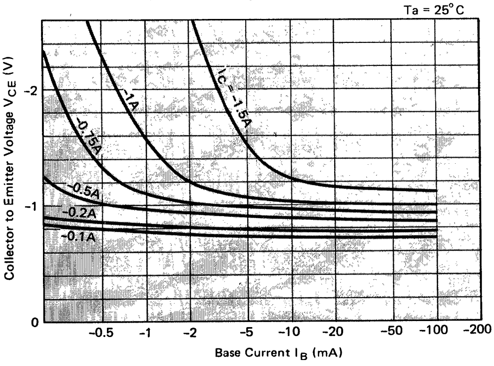
SATURATION VOLTAGE



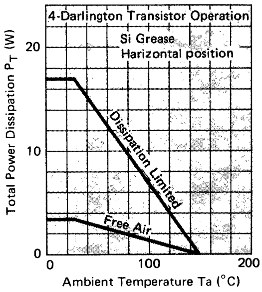
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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FT5770M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Storage Temperature		T_{stg}		-55 ~ +150	°C
Junction Temperature		T_j		+150	°C
Collector to Base Voltage		V_{CBO}		-100	V
Emitter to Base Voltage		V_{EBO}		-5	V
Collector to Emitter Voltage		V_{CEO}		-100	V
Collector Current	(Continuous)	I_C		±3	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±5	A
Base Current (Continuous)		I_B		-0.2	A
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	1.7	W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	4	W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	19	W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS

Single Darlington Transistor Operation

(Ta = 25°C)

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\ \mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -90$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90$ V, $I_E = 0$	–	–	-10	μA
DC Current Gain	h_{FE1}	$I_C = -1.5$ A, $V_{CE} = -5$ V (*)	2000	6000	15000	–
	h_{FE2}	$I_C = -3$ A, $V_{CE} = -5$ V (*)	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.5$ A, $I_B = -3$ mA (*)	–	-1.1	-1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V $I_C = -1.5$ A (**) $I_{B1} = -I_{B2} = -3$ mA	–	0.5	–	μs
Storage Time	t_{stg}		–	1.3	–	μs
Fall Time	t_f		–	0.5	–	μs

(*) Pulsed Pulse Width $\leqq 300\ \mu s$
Duty Ratio $\leqq 6\%$

(**) Pulsed Pulse Width = $50\ \mu s$
Duty Ratio $\leqq 1\%$

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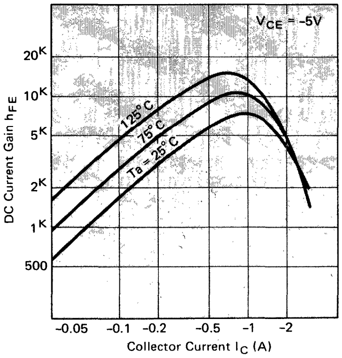
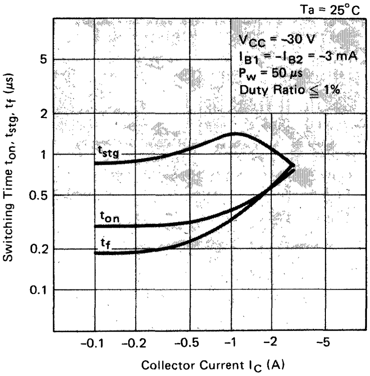
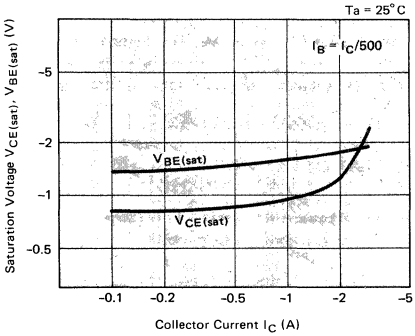
DC CURRENT GAIN



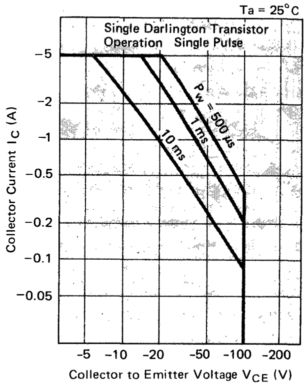
SWITCHING TIME



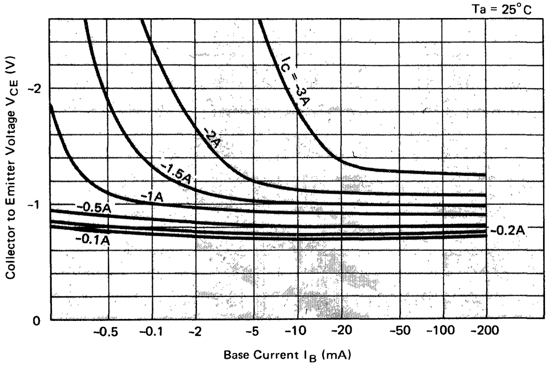
SATURATION VOLTAGE



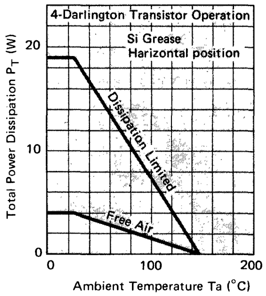
FORWARD BIAS SAFE OPERATING AREA



COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



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PRODUCT PROFILE

FT5776M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating		Symbol	Conditions	Value NPN	Value PNP	Unit
Storage Temperature		T_{stg}		-55 ~ +150		°C
Junction Temperature		T_j		+150		°C
Collector to Base Voltage		V_{CBO}		100	-100	V
Emitter to Base Voltage		V_{EBO}		5	-5	V
Collector to Emitter Voltage		V_{CEO}		100	-100	V
Collector Current	(Continuous)	I_C		±1.5	±1.5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±3	±3	A
Base Current (Continuous)		I_B		0.1	0.1	A
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500		$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT Operation	1.9		W
Total Power Dissipation		P_T	Ta = 25°C: 4-DLT Operation	4		W
Total Power Dissipation		P_T	Tc = 25°C: 4-DLT Operation	19		W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS SINGLE DARLINGTON TRANSISTOR OPERATION

[NPN]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\ \mu A$, $I_E = 0$	100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty\ \Omega$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	µs
DC Current Gain	h_{FE1}	$I_C = 0.75$ A, $V_{CE} = 5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = 1.5$ A, $V_{CE} = 5$V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 0.75$ A, $I_B = 1.5$ mA *	–	1.1	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V $I_C = 0.75$ A $I_{B1} = -I_{B2} = 1.5$ mA	–	0.5	–	µs
Storage Time	t_{stg}		–	2.1	–	µs
Fall Time	t_f		–	0.4	–	µs

[PNP]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\ \mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -80$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty\Omega$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90$V, $I_E = 0$	–	–	-10	µs
DC Current Gain	h_{FE1}	$I_C = -0.75$ A, $V_{CE} = -5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = -1.5$ A, $V_{CE} = -5$ V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -0.75$ A, $I_B = -1.5$ mA*	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.6	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V $I_C = -0.75$ A $I_{B1} = -I_{B2} = -1.5$ mA	–	0.5	–	µs
Storage Time	t_{stg}		–	1.4	–	µs
Fall Time	t_f		–	0.4	–	µs

* Pulsed $P_W \leqq 300\ \mu s$, D.R. $\leqq 6\%$

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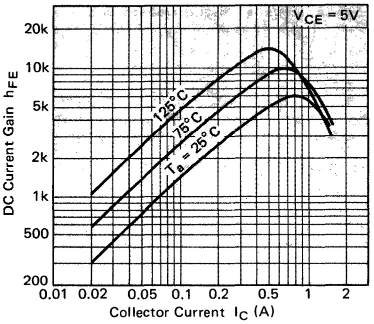
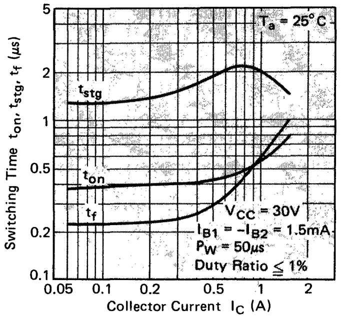
[NPN]

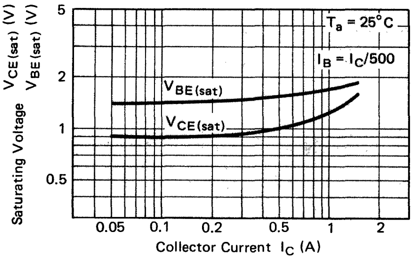
DC CURRENT GRAIN



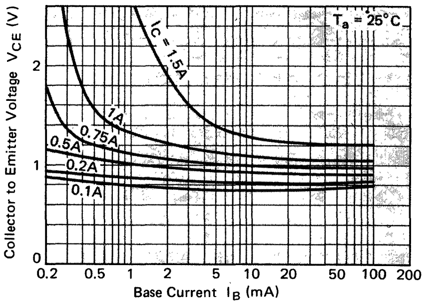
SWITCHING TIME



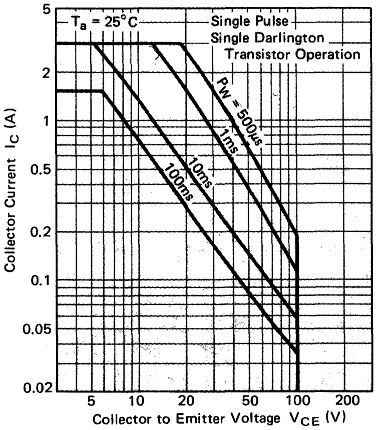
SATURATION VOLTAGE



COLLECTOR SATURATION REGION

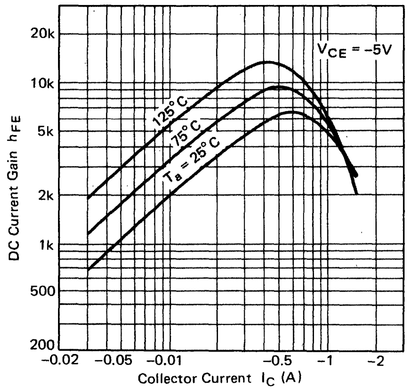


SAFE OPERATING AREA

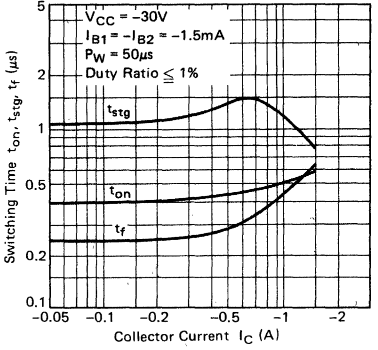


[PNP]

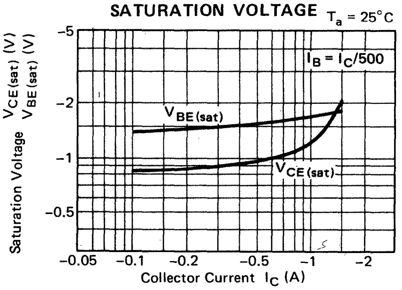
DC CURRENT GAIN



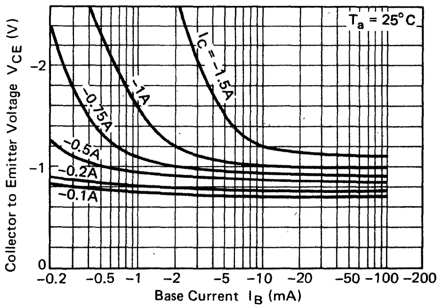
SWITCHING TIME



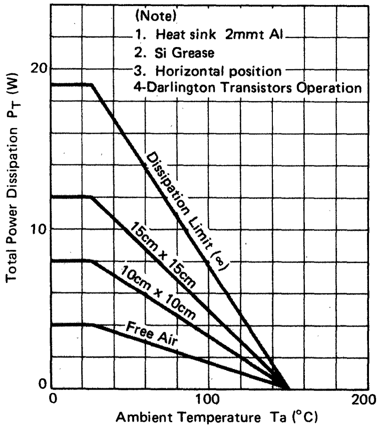
SATURATION VOLTAGE



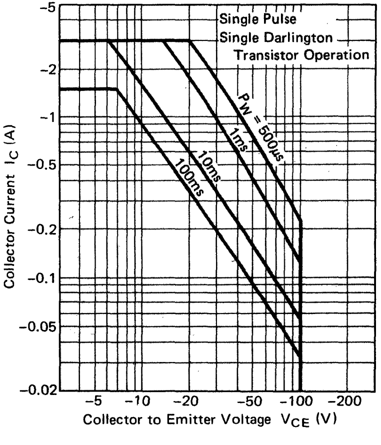
COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



SAFE OPERATING AREA



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Edition 1.1

FUJITSU

PRODUCT PROFILE

FT5777M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating		Symbol	Conditions	Value NPN	Value PNP	Unit
Strage Temperature		T_{stg}		-50 ~ +150		°C
Junction Temperature		T_j		+150		°C
Collector to Base Voltage		V_{CBO}		100	-100	V
Emitter to Base Voltage		V_{EBO}		5	-5	V
Collector to Emitter Voltage		V_{CEO}		100	-100	V
Collector Current	(Continuous)	I_C		±3	±3	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq$ 50%	±5	±5	A
Base Current (Continuous)		I_B		0.2	-0.2	A
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500		$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT operation	2.3		W
Total Collector Power Dissipation		P_T	Ta = 25°C: 4-DLT operation	5		W
Total Collector Power Dissipation		P_T	Tc = 25°C: 4-DLT operation	21		W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS (SINGLE DARLINGTON TRANSISTOR OPERATION)

[NPN]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100 μA, I_E = 0	100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 70 mA, I_C = 0	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 10 mA, R_{BE} = ∞Ω	100	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = 100 V, I_E = 0	–	–	10	μA
DC Current Gain	h_{FE1}	I_C = 1.5 A, V_{CE} = 5 V *	2000	6000	15000	–
	h_{FE2}	I_C = 3 A, V_{CE} = 5 V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 1.5 A, I_B = 3 mA *	–	1.2	1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	1.7	2.0	V
Turn-On Time	t_{on}	V_{CC} = 30 V I_C = 1.5 A $I_{B1} = -I_{B2}$ = 3 mA	–	0.6	–	μs
Storage Time	t_{stg}		–	1.8	–	μs
Fall Time	t_f		–	0.6	–	μs

[PNP]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = -100 μA, I_E = 0	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = -90 mA, I_C = 0	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = -10 mA, R_{BE} = ∞Ω	-100	–	–	V
Collector Cutoff Current	I_{CBO}	V_{CB} = -90 V, I_E = 0	–	–	-10	μA
DC Current Gain	h_{FE1}	I_C = -1.5 A, V_{CE} = -5 V *	2000	6000	15000	–
	h_{FE2}	I_C = -3 A, V_{CE} = -5 V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = -1.5 A, I_B = -3 mA *	–	-1.1	-1.5	V
Base to Emitter Saturation Votage	$V_{BE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	V_{CC} = -30 V I_C = -1.5 A $I_{B1} = -I_{B2}$ = -3 mA	–	0.5	–	μs
Storage Time	t_{stg}		–	1.3	–	μs
Fall Time	t_f		–	0.5	–	μs

* Pulsed $P_W \leqq 300$ μs' D.R. $\leqq$ 6%

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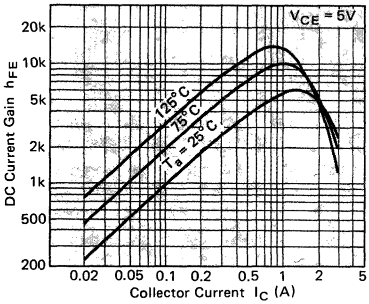
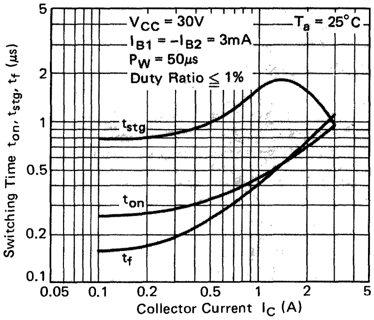
[NPN]

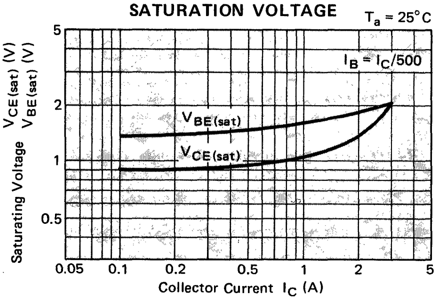
DC CURRENT GRAIN



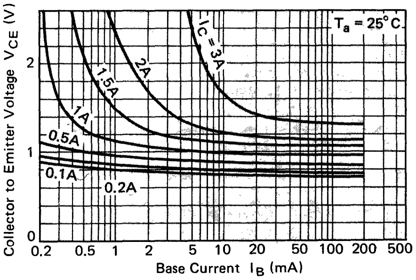
SWITCHING TIME



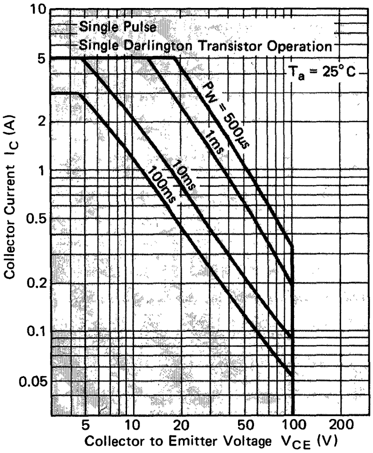
SATURATION VOLTAGE



COLLECTOR SATURATION REGION

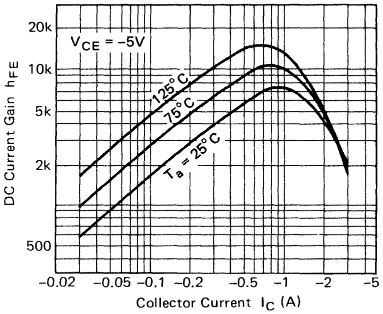


SAFE OPERATING AREA

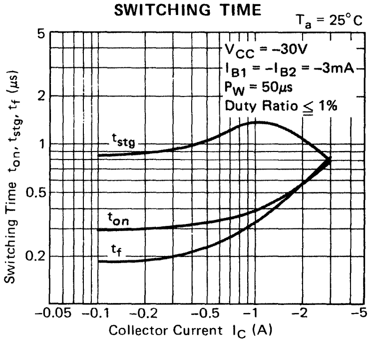


[PNP]

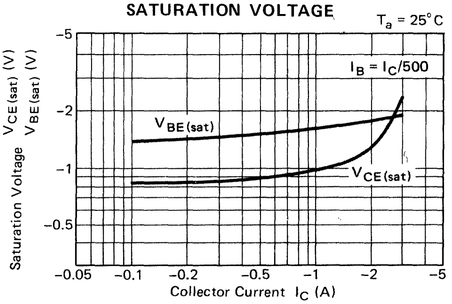
DC CURRENT GAIN



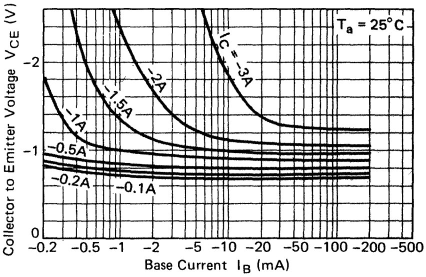
SWITCHING TIME



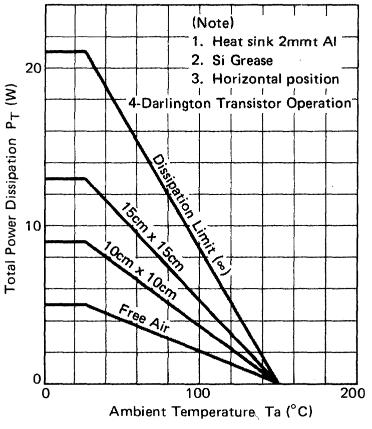
SATURATION VOLTAGE



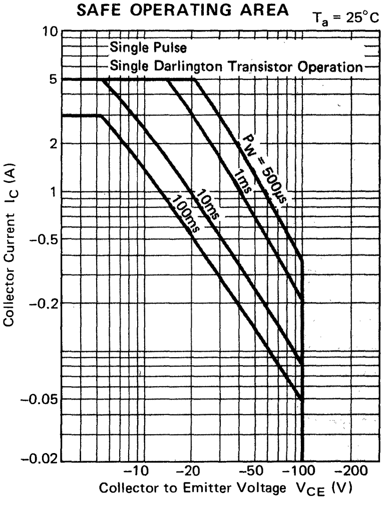
COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



SAFE OPERATING AREA



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PRODUCT PROFILE

FT5778M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating		Symbol	Conditions	Value		Unit
				NPN	PNP	
Storage Temperature		T_{stg}		–55 ~ +150		°C
Junction Temperature		T_j		+150		°C
Collector to Base Voltage		V_{CBO}		100	–100	V
Emitter to Base Voltage		V_{EBO}		5	–5	V
Collector to Emitter Voltage		V_{CEO}		100	–100	V
Collector Current	(Continuous)	I_C		±5	±5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq$ 50%	±8	±8	A
Base Current (Continuous)		I_B		0.5	–0.5	A
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500		$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT Operation	2.5		W
Total Power Dissipation		P_T	Ta = 25°C: 4-DLT Operation	5		W
Total Power Dissipation		P_T	Tc = 25°C: 4-DLT Operation	25		W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS (SINGLE DARLINGTON TRANSISTOR OPERATION)

[NPN]

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\ \mu A$, $I_E = 0$	100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 5$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 25$ mA, $R_{BE} = \infty\ \Omega$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μs
DC Current Gain	h_{FE1}	$I_C = 3$ A, $V_{CE} = 5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = 5$ A, $V_{CE} = 5$ V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 3$ A, $I_B = 6$ mA *	–	1.2	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V	–	1	–	μs
Storage Time	t_{stg}	$I_C = 3$ A	–	2	–	μs
Fall Time	t_f	$I_{B1} = -I_{B2} = 3$ mA	–	1	–	μs

[PNP]

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\ \mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -150$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -2$ mA, $R_{BE} = \infty \Omega$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -100$ V, $I_E = 0$	–	–	-10	μs
DC Current Gain	h_{FE1}	$I_C = -3$ A, $V_{CE} = -5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = -5$ A, $V_{CE} = -5$ V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -3$ A, $I_B = -6$ mA *	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{CE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V	–	0.4	–	μs
Storage Time	t_{stg}	$I_C = -3$ A	–	1.2	–	μs
Fall Time	t_f	$I_{B1} = -I_{B2} = -6$ mA	–	0.5	–	μs

* Pulsed $P_W \leqq 300\ \mu s$, D.R. $\leqq$ * 6%

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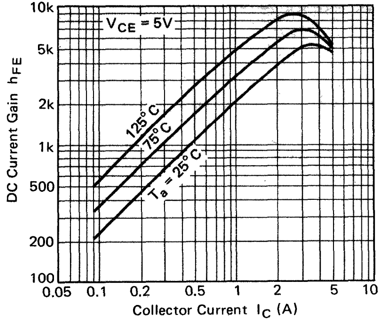
[NPN]

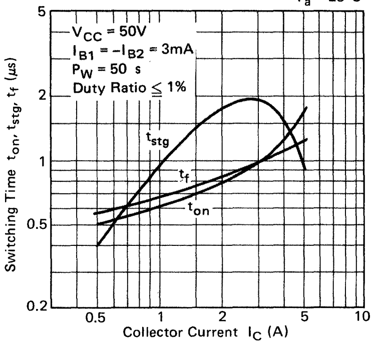
DC CURRENT GRAIN

$T_a = 25°C$



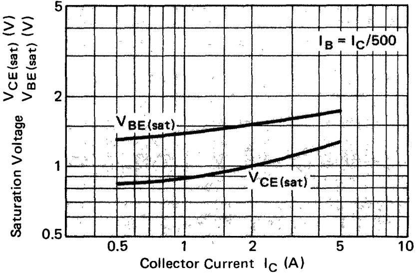
SWITCHING TIME

$T_a = 25°C$

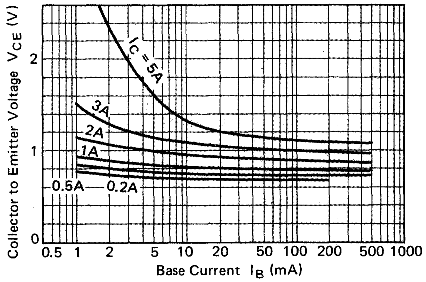


SATURATION VOLTAGE

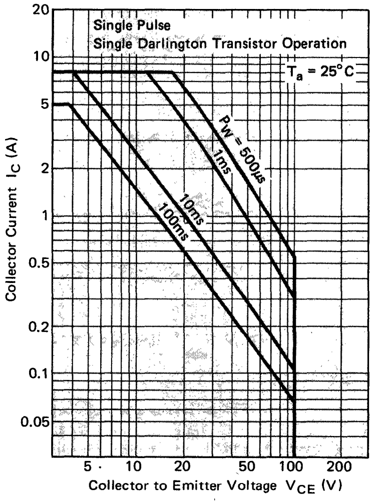
$T_a = 25°C$



COLLECTOR SATURATION REGION

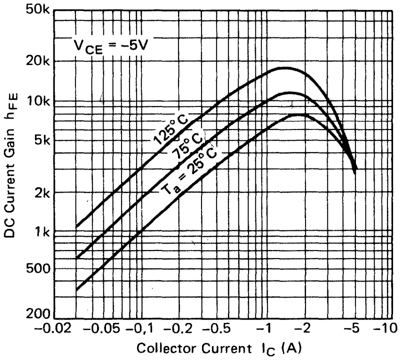


SAFE OPERATING AREA

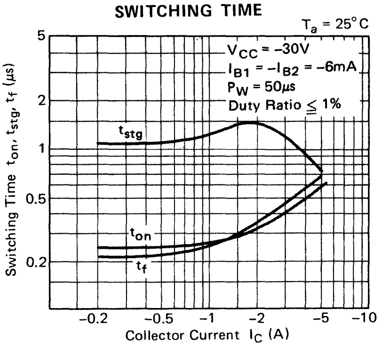


[PNP]

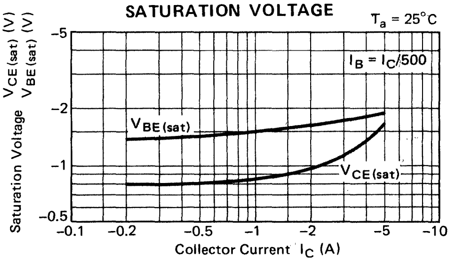
DC CURRENT GAIN



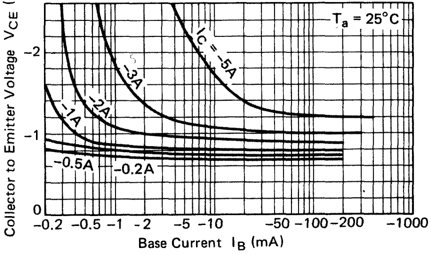
SWITCHING TIME



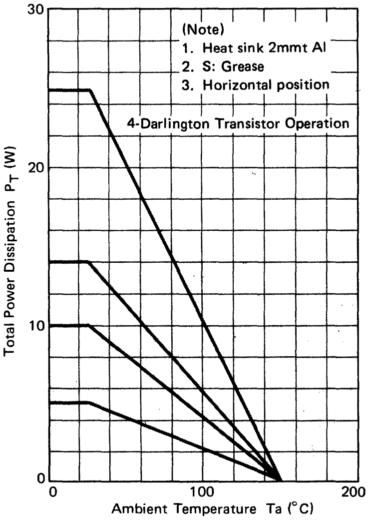
SATURATION VOLTAGE



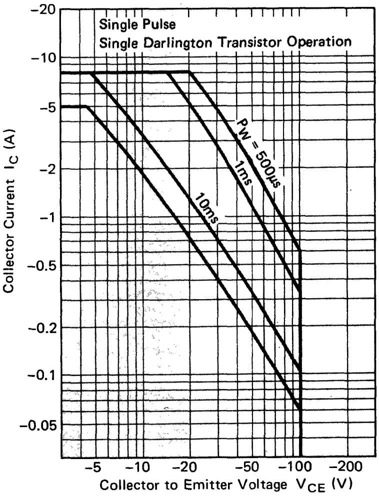
COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



SAFE OPERATING AREA



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FUJITSU

PRODUCT PROFILE

FT5786M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating		Symbol	Conditions	Value		Unit
				NPN	PNP	
Storage Temperature		T_{stg}		-55 ~ +150		°C
Junction Temperature		T_j		+150		°C
Collector to Base Voltage		V_{CBO}		100	-100	V
Emitter to Base Voltage		V_{EBO}		5	-5	V
Collector to Emitter Voltage		V_{CEO}		100	-100	V
Collector Current	(Continuous)	I_C		±1.5	±1.5	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq$ 50%	±3	±3	A
Base Current (Continuous)		I_B		0.1	0.1	A
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500		$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT Operation	1.5		W
Total Power Dissipation		P_T	Ta = 25°C: 4-DLT Operation	3.5		W
Total Power Dissipation		P_T	Tc = 25°C: 4-DLT Operation	17		W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS (SINGLE DARLINGTON TRANSISTOR OPERATION)

[NPN]

Parameter		Symbol	Test Condition	Limit			Unit
				Min.	Typ.	Max.	
Collector to Base Breakdown Voltage		$V_{(BR)CBO}$	$I_C = 100\ \mu A$, $I_E = 0$	100	–	–	V
Emitter to Base Breakdown Voltage		$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage		$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty\Omega$	100	–	–	V
Collector Cutoff Current		I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μs
DC Current Gain		h_{FE1}	$I_C = 0.75$ A, $V_{CE} = 5$ V *	2000	6000	15000	–
		h_{FE2}	$I_C = 1.5$ A, $V_{CE} = 5$V *	500	–	–	–
Collector to Emitter Saturation Voltage		$V_{CE(sat)}$	$I_C = 0.75$ A, $I_B = 1.5$ mA *	–	1.1	1.5	V
Base to Emitter Saturation Voltage		$V_{BE(sat)}$		–	1.6	2.0	V
Turn-On Time		t_{on}	$V_{CC} = 30$ V $I_C = 0.75$ A $I_{B1} = -I_{B2} = 1.5$ mA	–	0.5	–	μs
Storage Time		t_{stg}		–	2.1	–	μs
Fall Time		t_f		–	0.4	–	μs

[PNP]

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\ \mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -80$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty\ \Omega$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	-10	μs
DC Current Gain	h_{FE1}	$I_C = -0.75$ A, $V_{CE} = -5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = -1.5$ A, $V_{CE} = -5$ V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -0.75$ A, $I_B = -1.5$ mA*	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.6	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V $I_C = -0.75$ A $I_{B1} = -I_{B2} = -1.5$ mA	–	0.5	–	μs
Storage Time	t_{stg}		–	1.4	–	μs
Fall Time	t_f		–	0.4	–	μs

* Pulsed $P_W \leqq 300\ \mu s$, D.R. $\leqq$ 6%

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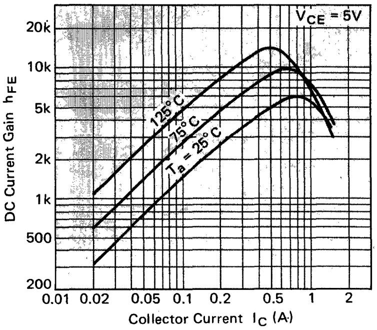
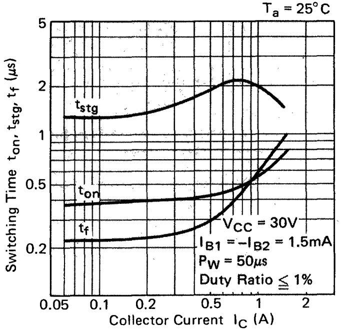
[NPN]

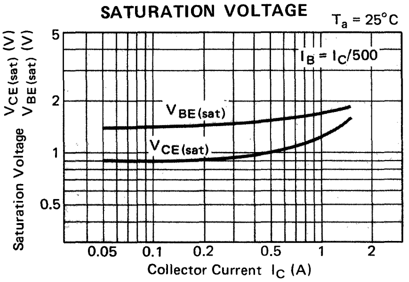
DC CURRENT GAIN



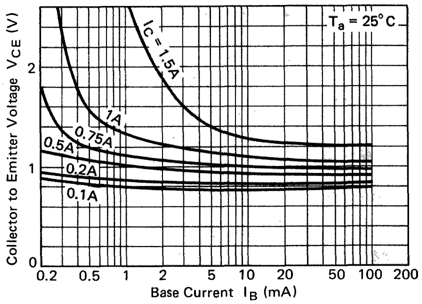
SWITCHING TIME



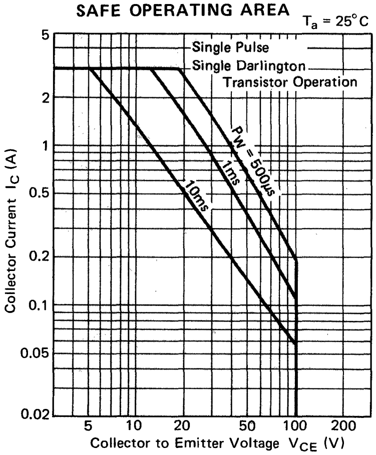
SATURATION VOLTAGE



COLLECTOR SATURATION REGION

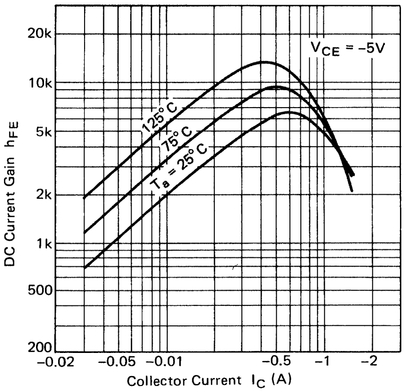


SAFE OPERATING AREA

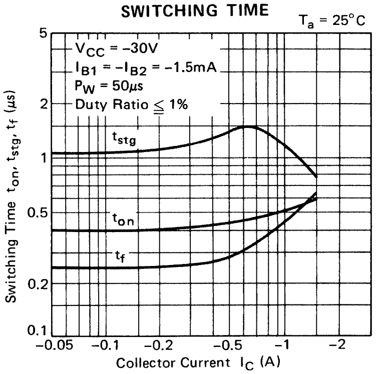


[PNP]

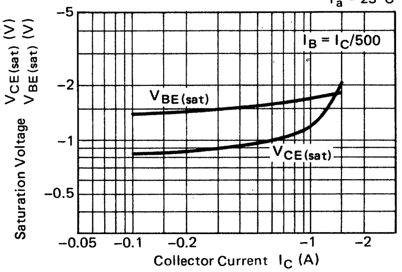
DC CURRENT GRAIN



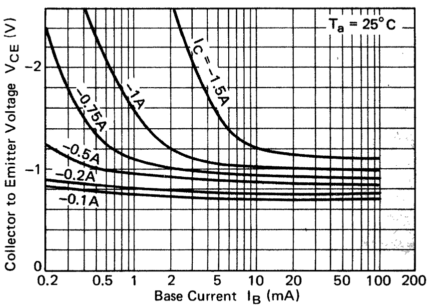
SWITCHING TIME



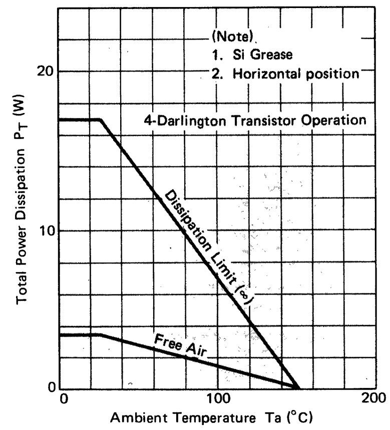
SATURATION VOLTAGE



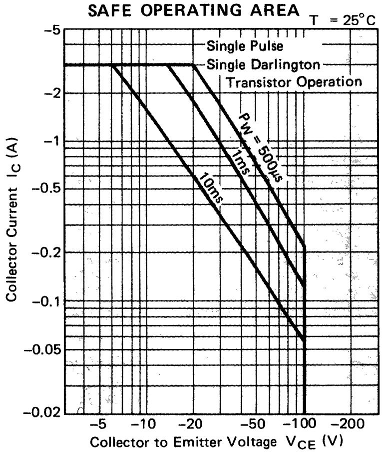
COLLECTOR SATURATION REGION



POWER DISSIPATION DERATING



SAFE OPERATING AREA



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PRODUCT PROFILE

FT5787M

Silicon Darlington Transistor Array

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Rating		Symbol	Conditions	Value NPN	Value PNP	Unit
Storage Temperature		T_{stg}		-55 ~ +150		°C
Junction Temperature		T_j		+150		°C
Collector to Base Voltage		V_{CBO}		100	-100	V
Emitter to Base Voltage		V_{EBO}		5	-5	V
Collector to Emitter Voltage		V_{CEO}		100	-100	V
Collector Current	(Continuous)	I_C		±3	±3	A
	(Pulsed)	I_{cp}	$P_W \leqq 1$ ms, D.R. $\leqq 50\%$	±5	±5	A
Base Current (Continuous)		I_B		0.2	-0.2	A
Isolation Voltage		V_{iso}	Fin 13 – Pin 1 ~ 12	500		$V_{r.m.s.}$
Collector Power Dissipation		P_C	Ta = 25°C: Single DLT Operation	1.7		W
Total Power Dissipation		P_T	Ta = 25°C: 4-DLT Operation	4		W
Total Power Dissipation		P_T	Tc = 25°C: 4-DLT Operation	19		W

DLT: Darlington Transistor

ELECTRICAL CHARACTERISTICS (SINGLE DARLINGTON TRANSISTOR OPERATION)

[NPN]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 100\,\mu A$, $I_E = 0$	100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 70$ mA, $I_C = 0$	5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 10$ mA, $R_{BE} = \infty\Omega$	100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 100$ V, $I_E = 0$	–	–	10	μs
DC Current Gain	h_{FE1}	$I_C = 1.5$ A, $V_{CE} = 5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = 3$ A, $V_{CE} = 5$V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 1.5$ A, $I_B = 3$ mA *	–	1.2	1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	1.7	2.0	V
Turn-On Time	t_{on}	$V_{CC} = 30$ V $I_C = 1.5$ A $I_{B1} = -I_{B2} = 3$ mA	–	0.6	–	μs
Storage Time	t_{stg}		–	1.8	–	μs
Fall Time	t_f		–	0.6	–	μs

[PNP]

Parameter	Symbol	Test Condition	Limit Min.	Limit Typ.	Limit Max.	Unit
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -100\,\mu A$, $I_E = 0$	-100	–	–	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -90$ mA, $I_C = 0$	-5	–	–	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -10$ mA, $R_{BE} = \infty\Omega$	-100	–	–	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = -90$ V, $I_E = 0$	–	–	-10	μs
DC Current Gain	h_{FE1}	$I_C = -1.5$ A, $V_{CE} = -5$ V *	2000	6000	15000	–
	h_{FE2}	$I_C = -3$ A, $V_{CE} = -5$V *	500	–	–	–
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1.5$ A, $I_B = -3$ mA *	–	-1.1	-1.5	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		–	-1.7	-2.0	V
Turn-On Time	t_{on}	$V_{CC} = -30$ V $I_C = -1.5$ A $I_{B1} = -I_{B2} = -3$ mA	–	0.5	–	μs
Storage Time	t_{stg}		–	1.3	–	μs
Fall Time	t_f		–	0.5	–	μs

* Pulsed $P_W \leqq 300\,\mu s$, D.R. $\leqq 6\%$

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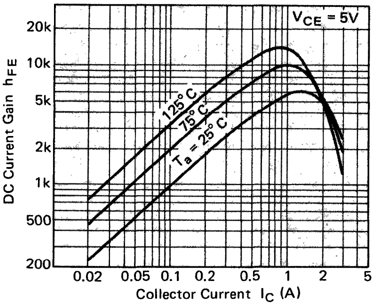
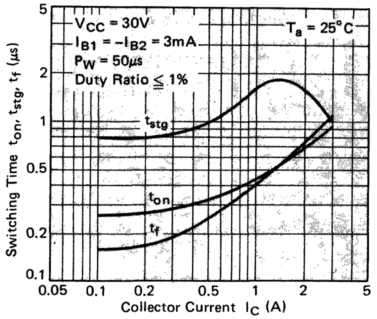
[NPN]

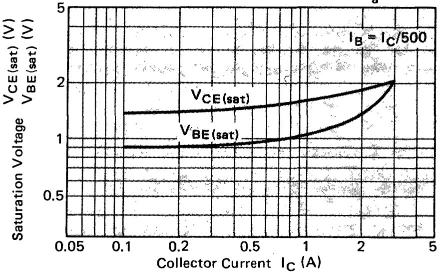
DC CURRENT GRAIN



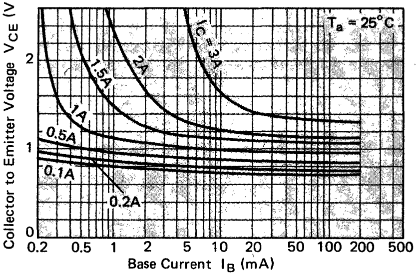
SWITCHING TIME



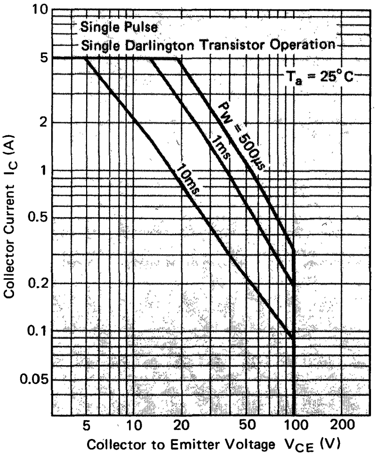
SATURATION VOLTAGE



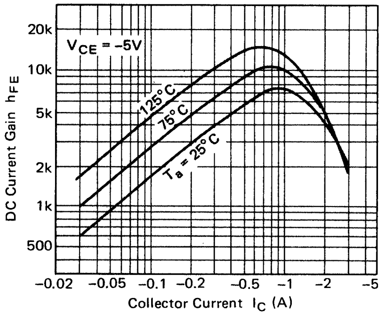
COLLECTOR SATURATION REGION

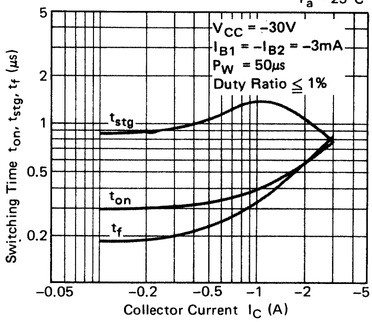


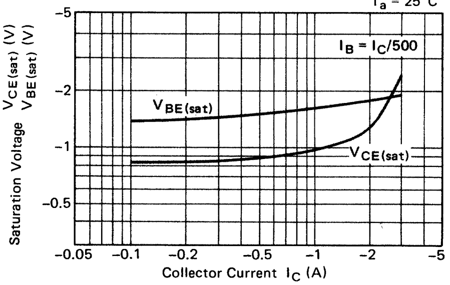
SAFE OPERATING AREA



[PNP]


DC CURRENT GAIN


SWITCHING TIME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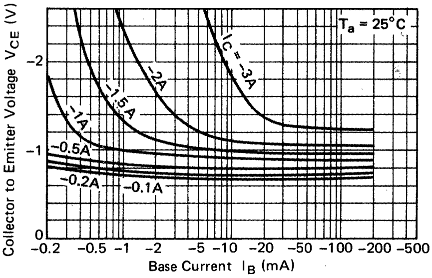
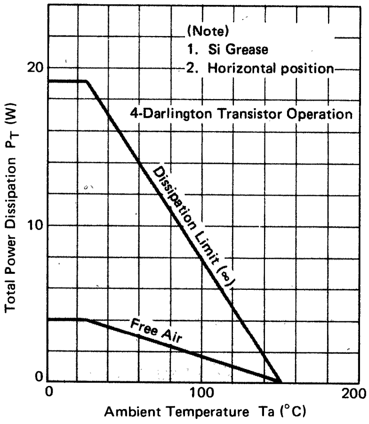
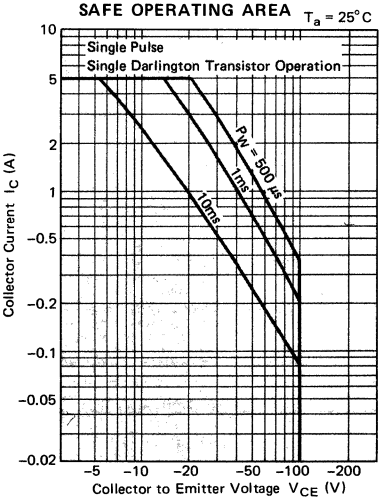

COLLECTOR SATURATION REGION


POWER DISSIPATION DERATING


SAFE OPERATING AREA

Section 4

Field Effect Transistor Arrays — *At a Glance*

Page	Device	Case (ns)	Maximum Frequency	
			V_{DSS} (V)	I_D (A)
4–7	FT6110	RM–65	120	±2
	FT6110D		120	±2
4–11	FT6111	RM–65	120	±3
	FT6111D		120	±3
4–15	FT6112	RM–65	120	±4.5
	FT6112D		120	±4.5
4–19	FT6120	RM–67	120	±1.5
	FT6120D		120	±1.5
4–23	FT6121	RM–67	120	±2.5
	FT6121D		120	±2.5
4–27	FT6122	RM–67	120	±4
	FT6122D		120	±4

INTRODUCTION

POWER MOS FET ARRAY SERIES

Description

This series is Silicon Enhancement-Mode Power MOS FET Arrays. Each array consists of 4 MOS FETs. The array is packaged in a small plastic 12-pin single in-line package with or without an isolated heatsink.

The series is well suited for motor drive applications where IC outputs must be boosted to drive print hammets. The series are extremely cost effective and space saving compared to using four separate TO-220 type Power MOS FETs.

Features

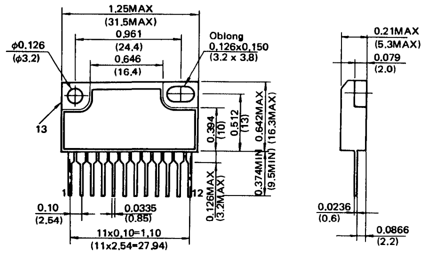
- 4-Circuits included in one package
- Direct Drive from Logic-Level
- Large Power Dissipation
- Built-in fast recovery diode to absorb fly-back voltage
- Fast switching speed
- No Secondary Breakdown

Application

- Solenoid Drives
  - Printer Head Drives
  - Hammer Drives
- Motor Drives
- Amplifiers

PACKAGE DIMENSIONS

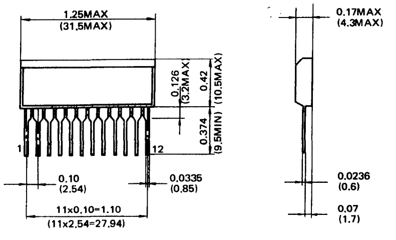
FUJITSU PKG No. RM-65



13: Fin (N.C.)

Unit in inch (mm)

FUJITSU PKG No. RM-67



Unit in inch (mm)

- Selection Guide

RM-65 Series (with isolatedd heatsink)

Device Number	Circuit Config.	Maximum Ratings (Ta = 25°C)				Electrical Characteristics (Ta = 25°C)		
		V_{DSS} (V)	$I_{D(DC)}$ (A)	P_T* (W)	T_{ch} (°C)	$R_{DS(on)}$** TYP. (OHM)	$V_{GS(off)}$ TYP. (V)	C_{iss} TYP. (pF)
FT6110D	A	120	±2	4	150	1.2	1.3	130
FT6111D			±3	5		0.55		280
FT6112D			±4.5	5		0.32		450
FT6110	B		±2	4		1.2		130
FT6111			±3	5		0.55		280
FT6112			±4.5	5		0.32		450

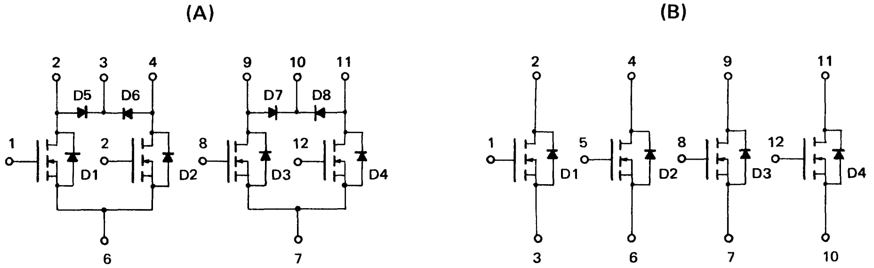
* ; 4-MOSFET operation ** ; V_{GS} = 4 V

RM-67 Series (without isolated heatsink)

Device Number	Circuit Config.	Maximum Ratings (Ta = 25°C)				Electrical Characteristics (Ta= 25°C)		
		V_{DSS} (V)	$I_{D(DC)}$ (A)	P_T* (W)	T_{ch} (°C)	$R_{DS(on)}$ TYP. (OHM)	$V_{GS(off)}$ TYP. (V)	C_{iss} TYP. (pF)
FT6120D	A	120	±1.5	3.5	150	1.2	1.3	130
FT6121D			±2.5	4		0.55		280
FT6122D			±4	4		0.32		450
FT6120	B		±1.5	3.5		1.2		130
FT6121			±2.5	4		0.55		280
FT6122			±4	4		0.32		450

* ; 4-MOSFET operation, ** ; V_{GS} = 4 V

- Circuit Configuration



13 : FIN (N.C.)
$D_1 \sim D_4$: Flywheel diode
$D_5 \sim D_8$: Fast recovery diode to absorb fly-back voltage

13 : FIN (N.C.)
$D_1 \sim D_4$: Flywheel diode

Applications for solenoid drives and motor drives

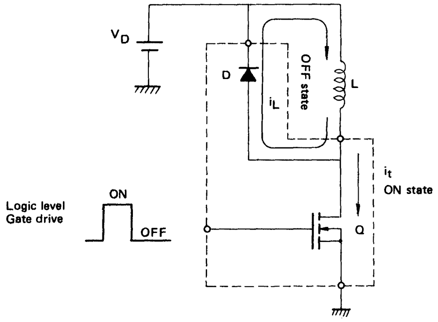
1) General Discription

In solenoid drive applications and motor drive applications, the fly-back voltage is generated at the mode of a transistor inductive turn-off.
The power MOS FET array series (FT6110D, FT6111D, FT6112D, FT6120D, FT6121D, FT6122D) can easily absorb the flyback energy through the fast recovery diodes. This guarantees the arrays a very efficient operation.

- Flyback energy absorption circuit

Fig. 1 shows the equivalent drive circuit for a single device of the power MOS FET array.
During the turn-on mode of the power MOS FET (Q), the current (it) flows through the inductive load (L).
During the turn-off of the power MOS FET (Q), the fly-back energy which is stored in the inductive load (L) is absorbed by current (i_L) which flows through the fast recovery diode.

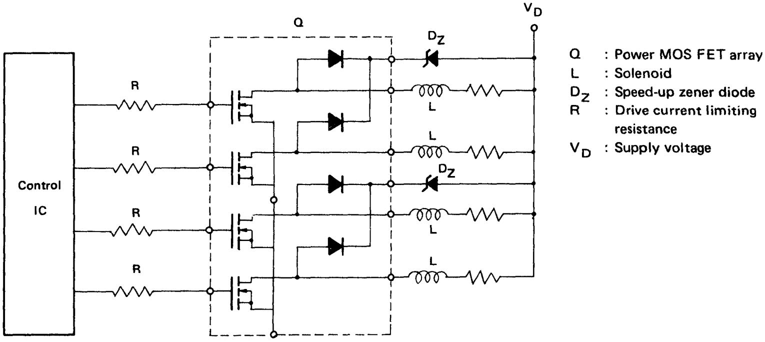
Fig. 1—Circuit for absorbing fly-back energy



2) Solenoid drive circuit

Four solenoids can be driven by one power MOS FET array

Fig. 2—Solenoid drive circuit



Q : Power MOS FET array
L : Solenoid
D_Z : Speed-up zener diode
R : Drive current limiting resistance
V_D : Supply voltage

3) Motor Drive

3–1) Driving form (ex. 4-phase motor)

Motors may be driven in either a unipolar or (Fig.-3(a)) bipolar manner (Fig.-3(b)). The current in unipolar mode flows in only one direction while the current in bi-polar mode flows in both directions.

Fig. 3–(a) Uni-polar driving form
*** Easy Construction**

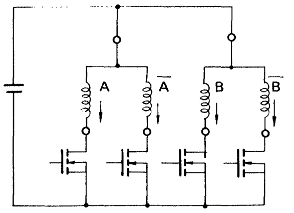
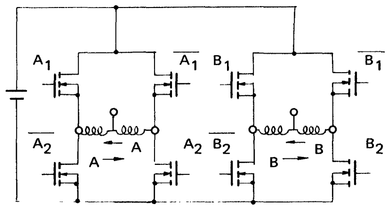
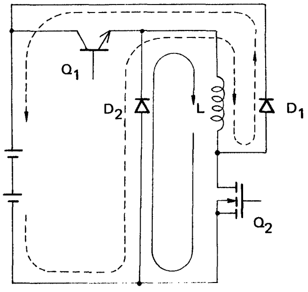


Fig. 3–(b) Bipolar driving form
*** Large Output Torque**



3–2) Principle circuit for pulse width modulate drive

Fig. 4— Principle circuit for pulse width modulate drive



The output current is controlled by the pulse width of modulator transistor (Q_1), when the PWM transistor (Q_1) is in the off-state and the power MOS FET (Q_2) is in the on-state, the current flows through the fast recovery diode (D_2). (Solid line) In this mode the fast recovery diode operates similarly to a flywheel diode.

When both the PWM transistor (Q_1) and power MOS FET are in the off-state current flows through the flywheel diode.

(Dashed line)

In this mode, the current flows back to the DC power supply to improve the operating efficiency.

Example of Pulse Width Modulate Drive

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PRODUCT PROFILE

FT6110, FT6110D

Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET Arrays

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	2	A
	Pulsed	I_{DM}		4	A
Reverse Drain Current (Continuous)		I_{DR}		2	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq 25\%$	2	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	4	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOS FET operation	4	W
		P_T	Tc = 25°C, 4-MOS FED operation	32	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOS FED operation	3.9	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 100\,\mu A$, $V_{GS} = 0$ V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120$ V, $V_{GS} = 0$ V	–	–	100	µA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$I_D = 1$ mA, $V_{DS} = 10$ V	0.9	1.3	1.7	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	$I_D = 1$ A, $V_{GS} = 4$ V *	–	1.2	1.7	Ω
	$R_{DS(on)}$	$I_D = 1$ A, $V_{GS} = 10$ V *	–	0.9	1.3	Ω
Forward Transconductance	g_{fs}	$I_D = 1$ A, $V_{DS} = 10$ V *	0.8	1.3	–	S
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	–	130	170	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	–	45	80	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	15	30	pF
Turn-On Delay Time	$t_{d(on)}$	$I_D = 1$ A (See Test Circuit)	–	20	–	ns
Rise Time	t_r	$V_{DD} = 60$ V	–	10	–	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS} = 10$ V	–	40	–	ns
Fall Time	t_f	$R_{GS} = 50\,\Omega$	–	10	–	ns

* Pulsed : Pulse Width $\leqq 300\,\mu s$, D.R. $\leqq 6\%$

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	$I_{DR} = 1$ A, $V_{GS} = 0$ V	–	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$I_{DR} = 1$ A, $dI_{DR}/dt = 100$ A/µs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6110D only)

Forward Voltage	V_F	$I_F = 100$ mA	–	–	1.0	V
Reverse Current	I_R	$V_R = 120$ V	–	–	5	µA
Reverse Voltage	V_R	$I_R = 10\,\mu A$	130	–	–	V

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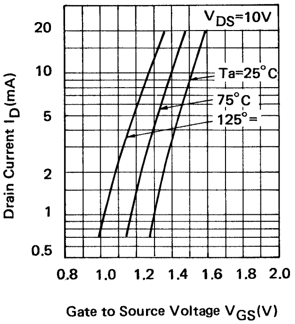
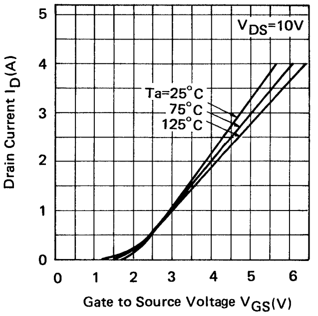
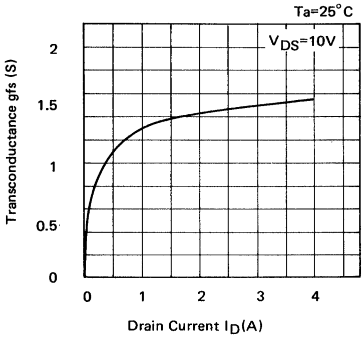
Threshhold



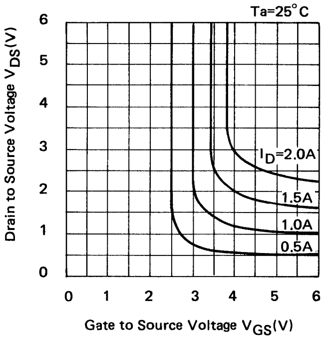
Transfer Characteristics



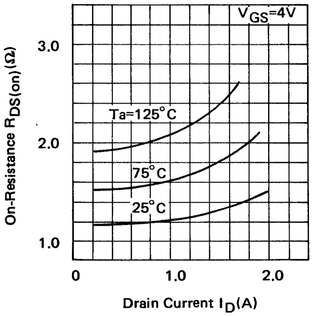
Transconductance-Drain Current



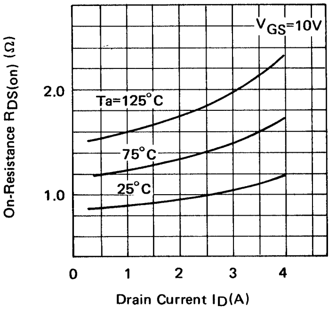
Drain to Source Saturation Region



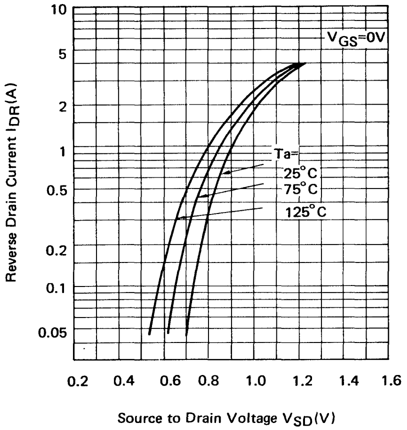
On-Resistance — Drain Current



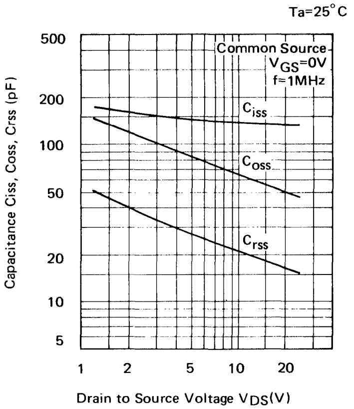
On-Resistance-Drain Current



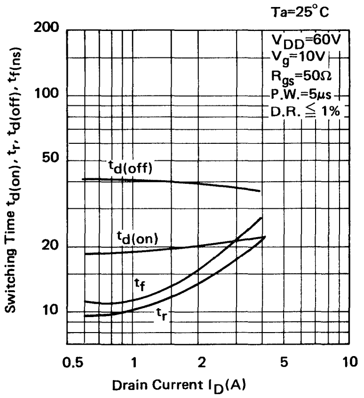
Source-Drain Diode Forward Voltage



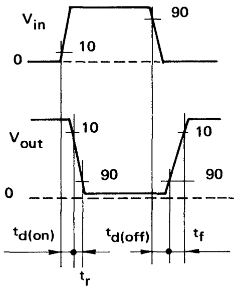
Capacitance-Drain to Source Voltage



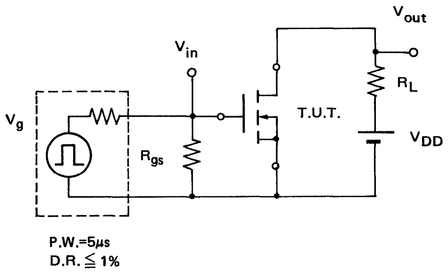
Switching Time — Drain Current



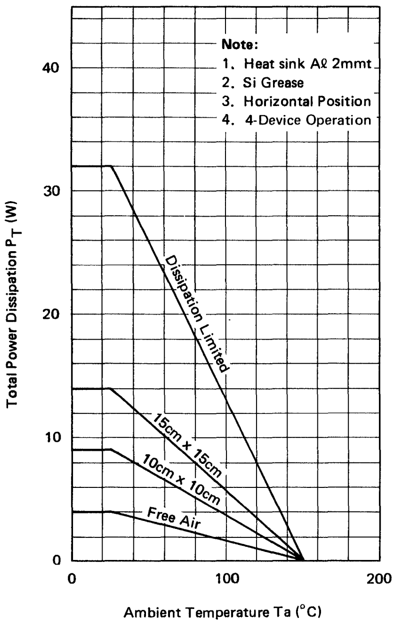
Switching Waveform



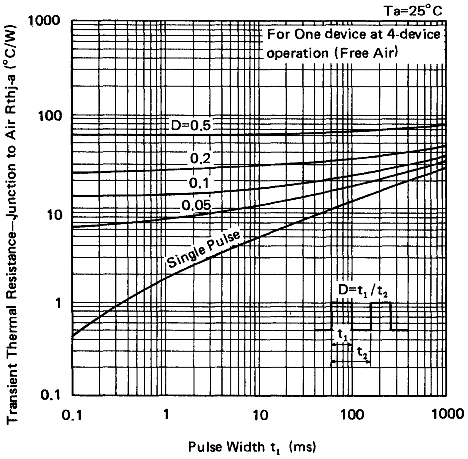
Test Circuit for Switching Time



Power Dissipation Derating



Maximum Transient Thermal Resistance



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PRODUCT PROFILE

FT6111, FT6111D
Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET Array

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	3	A
	Pulsed	I_{DM}		6	A
Reverse Drain Current (Continuous)		I_{DR}		3	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq$ 25%	3	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	6	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOSFET operation	5	W
		P_T	Tc = 25°C, 4-MOSFET operation	36	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOSFET operation	3.5	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition		Limit		Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 100 μA, V_{GS} = 0 V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	–	–	100	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D = 1 mA, V_{DS} = 10 V	0.9	1.3	1.7	V
Static Drain to Source on-State Resistance	$R_{DS(on)}$	I_D = 1.5 A, V_{GS} = 4 V *	–	0.55	0.75	Ω
	$R_{DS(on)}$	I_D = 1.5 A, V_{GS} = 10 V *	–	0.45	0.6	Ω
Forward Transconductance	g_{fs}	I_D = 1.5 A, V_{DS} = 10 V *	1.2	2.4	–	S
Input Capacitance	C_{iss}	V_{DS} = 25 V	–	280	360	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	–	80	130	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	35	60	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1.5 A (See Test Circuit)	–	20	–	ns
Rise Time	t_r	V_{DD} = 60 V	–	15	–	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} = 10 V	–	55	–	ns
Fall Time	t_f	R_{GS} = 50 Ω	–	15	–	ns

* Pulsed : Pulse Width $\leqq$ 300 μs, D.R. $\leqq$ 6%

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	I_{DR} = 1.5 A, V_{GS} = 0 V	–	0.9	1.2	V
Reverse Recovery Time	t_{rr}	I_{DR} = 1.5 A, dI_{DR}/dt=100 A/μs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6111D only)

Forward Voltage	V_F	I_F = 100 mA	–	–	1.0	V
Reverse Current	I_R	V_R = 120 V	–	–	5	μA
Reverse Voltage	V_R	I_R = 10 μA	130	–	–	V

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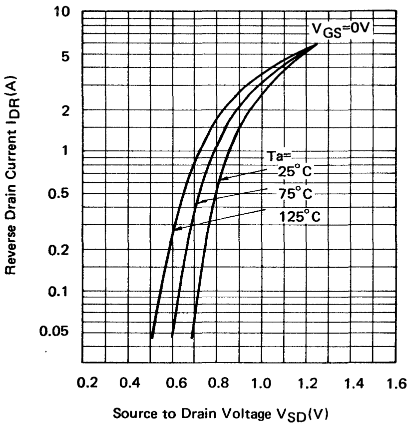
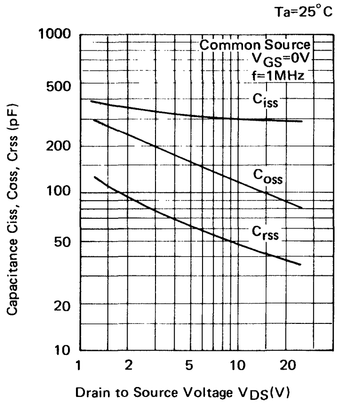
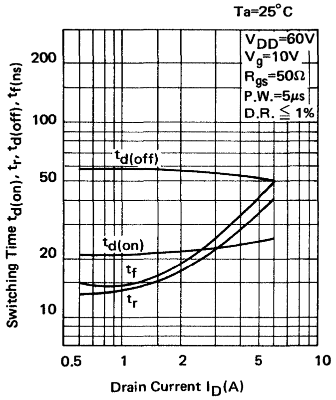
Source-Drain Diode Forward Voltage



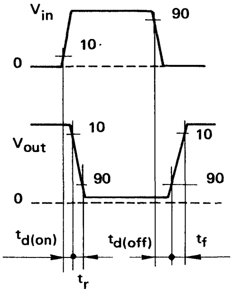
Capacitance-Drain to Source Voltage



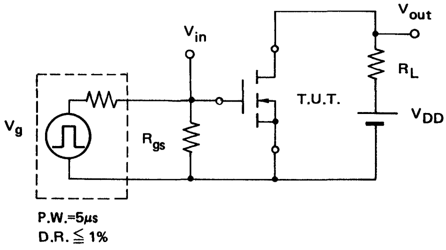
Switching Time — Drain Current

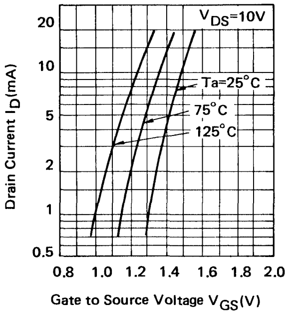


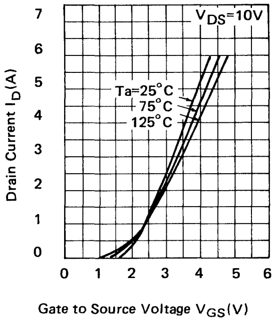
Switching Waveform

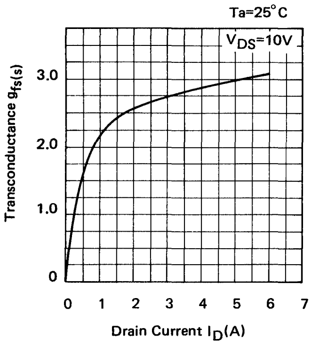


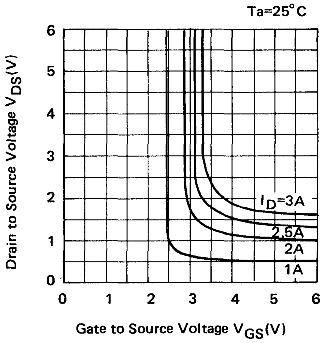
Test Circuit for Switching Time

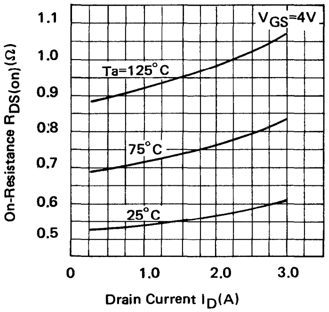


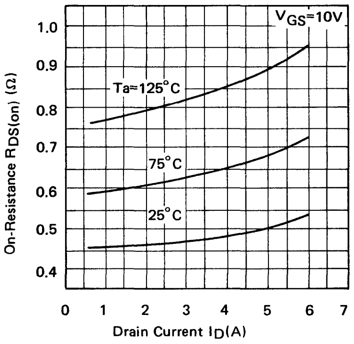

Threshhold Region


Transfer Characteristics

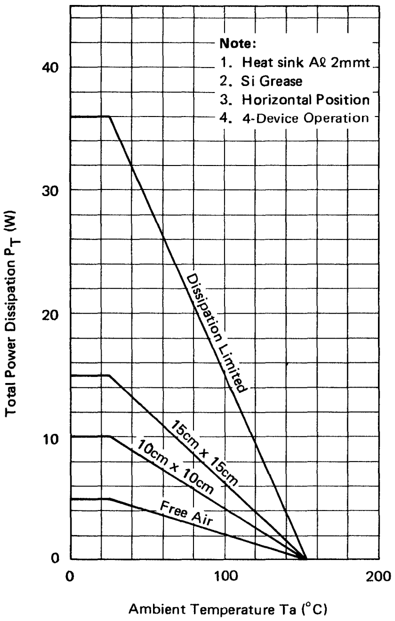

Transconductance-Drain Current


Drain to Source Saturation Region

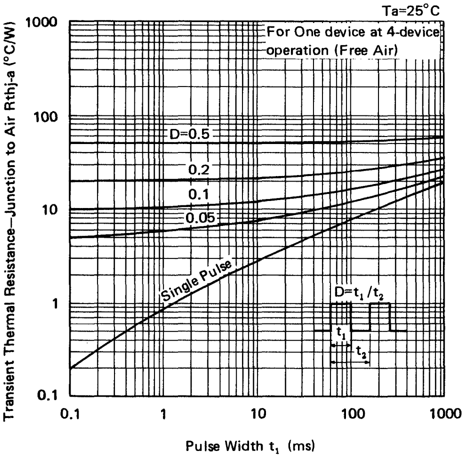

On-Resistance — Drain Current


On-Resistance-Drain Current

Power Dissipation Derating



Maximum Transient Thermal Resistance



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PRODUCT PROFILE

FT6112, FT6112D

Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET Arrays

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	4.5	A
	Pulsed	I_{DM}		9	A
Reverse Drain Current (Continuous)		I_{DR}		4.5	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq$ 25%	4.5	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	9	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOSFET operation	5	W
		P_T	Tc = 25°C, 4-MOSFET operation	40	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOSFET operation	3.2	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 100 μA, V_{GS} = 0 V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	–	–	100	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D = 1 mA, V_{DS} = 10 V	0.9	1.3	1.7	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	I_D = 3 A, V_{GS} = 4 V *	–	0.32	0.5	Ω
	$R_{DS(on)}$	I_D = 3 A, V_{GS} = 10 V *	–	0.25	0.4	Ω
Forward Transconductance	g_{fs}	I_D = 3 A, V_{DS} = 10 V *	2.5	4.5	–	S
Input Capacitance	C_{iss}	V_{DS} = 25 V	–	450	550	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	–	140	210	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	60	90	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 3 A (Set Test Circuit)	–	25	–	ns
Rise Time	t_r	V_{DD} = 60 V	–	30	–	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} = 10 V	–	75	–	ns
Fall Time	t_f	R_{GS} = 50 Ω	–	35	–	ns

* Pulsed : Pulse Width $\leqq$ 300 μs, D.R. $\leqq$ 6%

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	I_{DR} = 3 A, V_{GS} = 0 V	–	1.0	1.3	V
Reverse Recovery Time	t_{rr}	I_{DR} = 3 A, dI_{DR}/dt = 100 A/μs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6112D only)

Forward Voltage	V_F	I_F = 1 A	–	–	1.0	V
Reverse Current	I_R	V_R = 120 V	–	–	10	μA
Reverse Voltage	V_R	I_R = 15 μA	130	–	–	V

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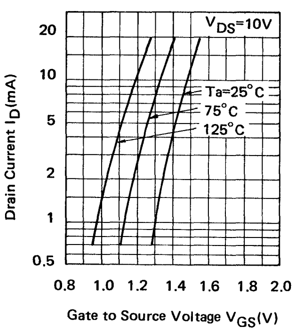
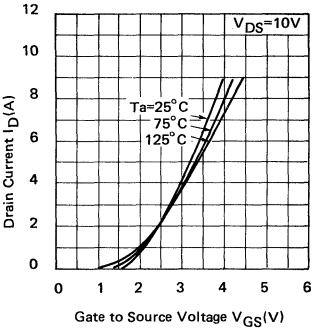
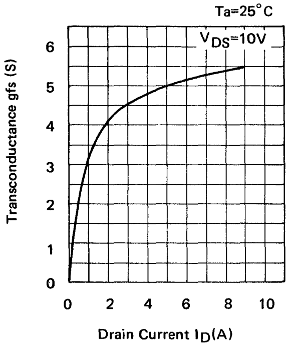


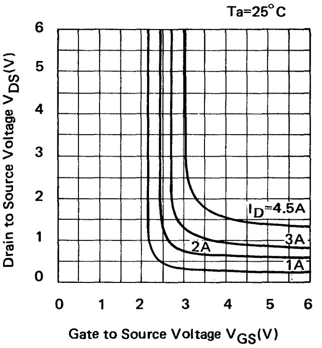
Threshhold Region



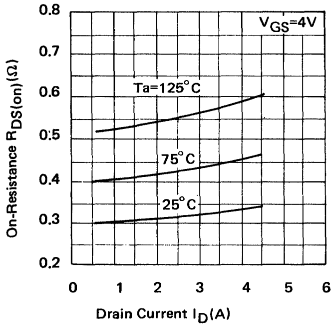
Transfer Characteristics



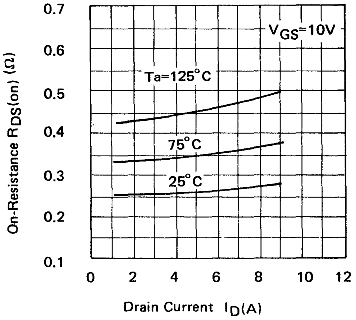
Transconductance-Drain Current



Drain to Source Saturation Region

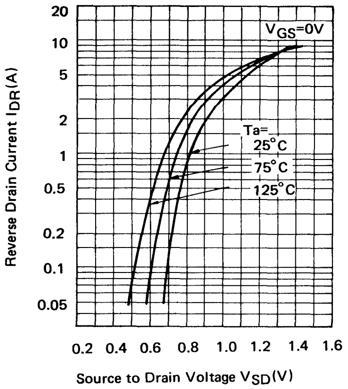


On-Resistance — Drain Current

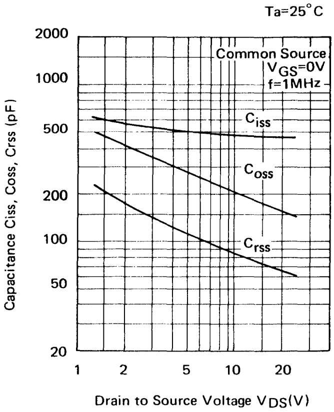


On-Resistance-Drain Current

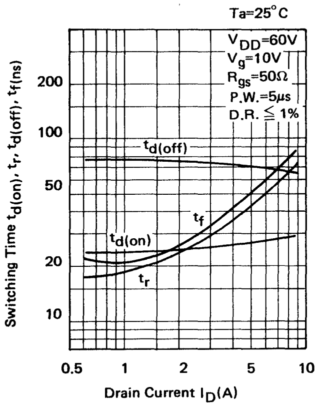
Source-Drain Diode Forward Voltage



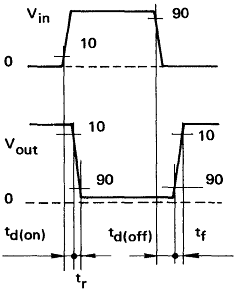
Capacitance-Drain to Source Voltage



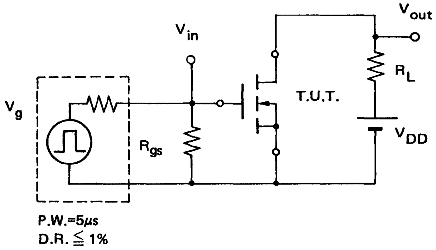
Switching Time — Drain Current



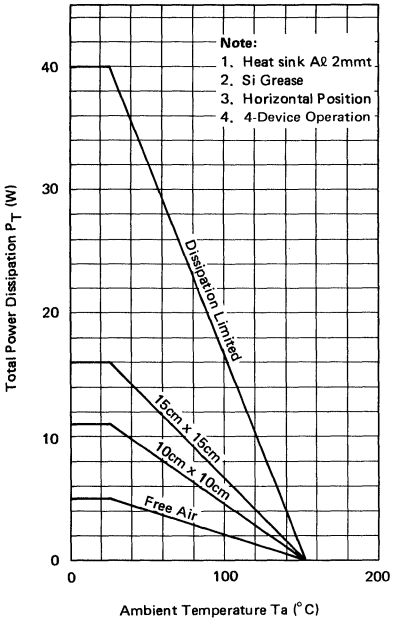
Switching Waveform



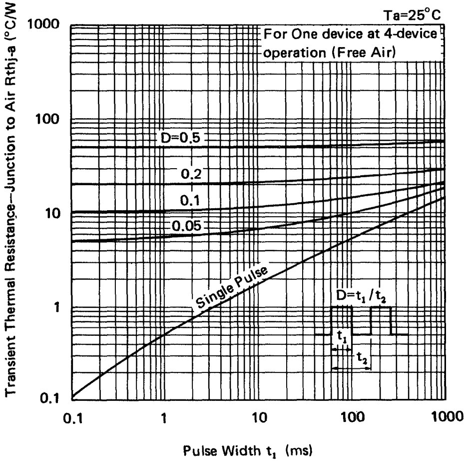
Test Circuit for Switching Time



Power Dissipation Derating



Maximum Transient Thermal Resistance



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PRODUCT PROFILE

FT6120, FT6120D

Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	1.5	A
	Pulsed	I_{DM}		3	A
Reverse Drain Current (Continuous)		I_{DR}		1.5	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq$ 25%	1.5	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	3	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOSFET operation	3.5	W
		P_T	Tc = 25°C, 4-MOSFET operation	28	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOSFET operation	4.5	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 100 μA, V_{GS} = 0 V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	–	–	100	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	I_D = 1 mA, V_{DS} = 10 V	0.9	1.3	1.7	V
Static Drain to Source on State Resistance	$R_{DS(on)}$	I_D = 1 A, V_{GS} = 4 V *	–	1.2	1.7	Ω
	$R_{DS(on)}$	I_D = 1 A, V_{GS} = 10 V *	–	0.9	1.3	Ω
Forward Transconductance	g_{fs}	I_D = 1 A, V_{DS} = 10 V *	0.8	1.3	–	S
Input Capacitance	C_{iss}	V_{DS} = 25 V	–	130	170	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	–	45	80	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	15	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1 A (See Test Circuit)	–	20	–	ns
Rise Time	t_r	V_{DD} = 60 V	–	10	–	ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} = 10 V	–	40	–	ns
Fall Time	t_f	R_{GS} = 50 Ω	–	10	–	ns

* Pulsed : Pulse Width $\leqq 300\ \mu$s, D.R. $\leqq$ 6%

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	I_{DR} = 1 A, V_{GS} = 0 V	–	0.9	1.2	V
Reverse Recovery Time	t_{rr}	I_{DR} = 1 A, dI_{DR}/dt = 100 A/μs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6120D only)

Forward Voltage	V_F	I_F = 100 mA	–	–	1.0	V
Reverse Current	I_R	V_R = 120 V	–	–	5	μA
Reverse Voltage	V_R	I_R = 10 μA	130	–	–	V

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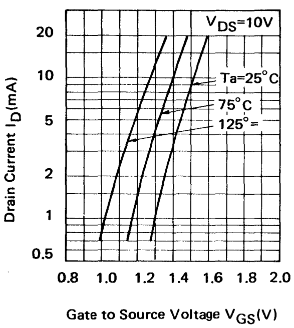
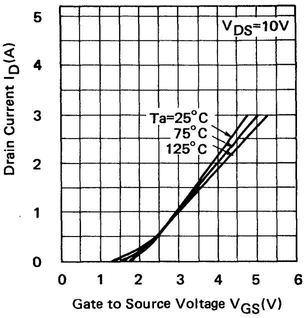
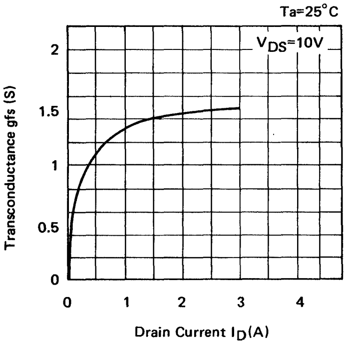
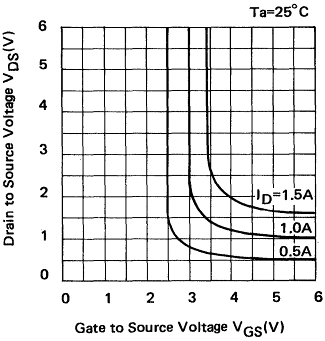
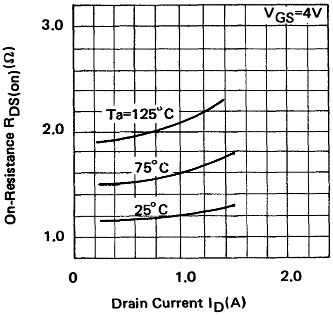
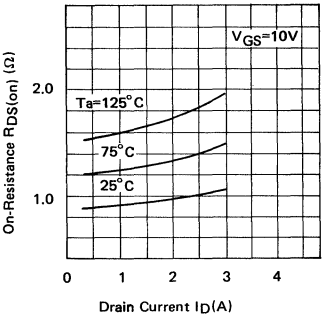

Threshhold Region


Transfer Characteristics

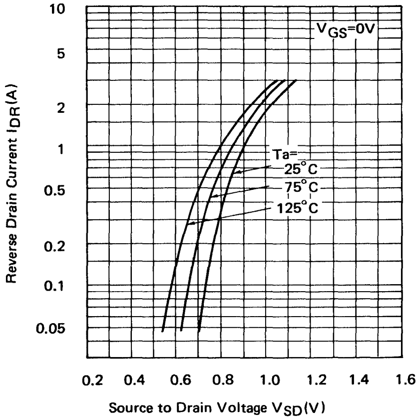

Transconductance-Drain Current


Drain to Source Saturation Region

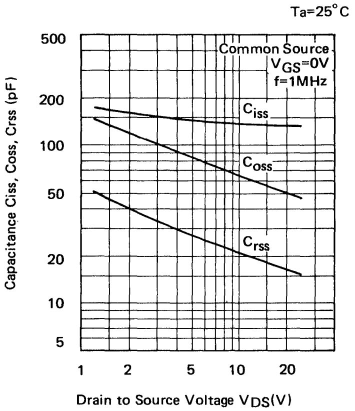

On-Resistance — Drain Current


On-Resistance-Drain Current

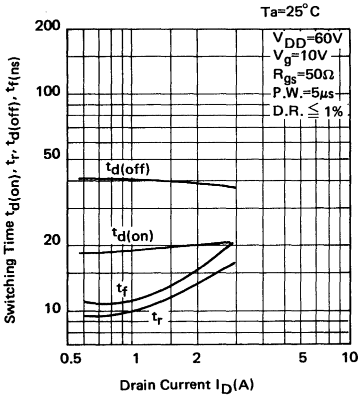
Source-Drain Diode Forward Voltage



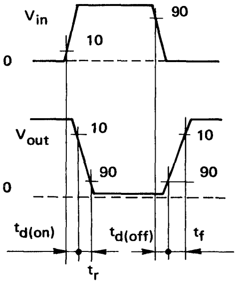
Capacitance-Drain to Source Voltage



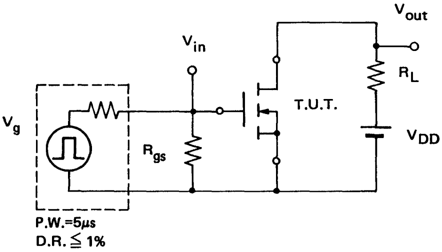
Switching Time — Drain Current



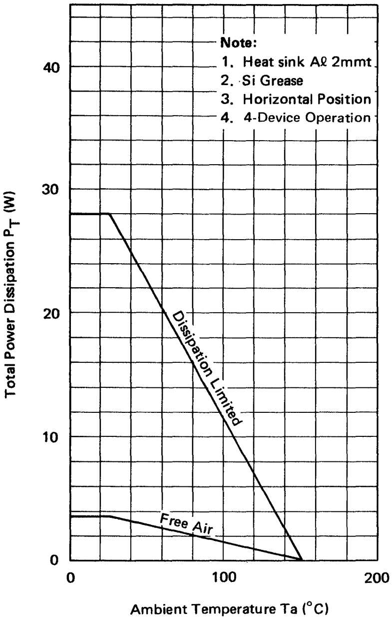
Switching Waveform



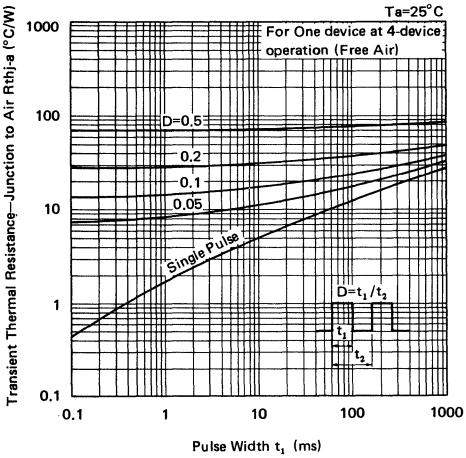
Test Circuit for Switching Time



Power Dissipation Derating



Maximum Transient Thermal Resistance



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PRODUCT PROFILE

FT6121, FT6121D

Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	2.5	A
	Pulsed	I_{DM}		5	A
Reverse Drain Current (Continuous)		I_{DR}		2.5	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq 25\%$	2.5	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	5	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOSFET operation	4	W
		P_T	Tc = 25°C, 4-MOSFET operation	32	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOSFET operation	3.9	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 100\,\mu A$, $V_{GS} = 0$ V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120$ V, $V_{GS} = 0$ V	–	–	100	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$I_D = 1$ mA, $V_{DS} = 10$ V	0.9	1.3	1.7	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	$I_D = 1.5$ A, $V_{GS} = 4$ V *	–	0.55	0.75	Ω
	$R_{DS(on)}$	$I_D = 1.5$ A, $V_{GS} = 10$ V *	–	0.45	0.6	Ω
Forward Transconductance	g_{fs}	$I_D = 1.5$ A, $V_{DS} = 10$ V *	1.2	2.4	–	S
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	–	280	360	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	–	80	130	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	35	60	pF
Turn-On Delay Time	$t_{d(on)}$	$I_D = 1.5$ A (See Test Circuit)	–	20	–	ns
Rise Time	t_r	$V_{DD} = 60$ V	–	15	–	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS} = 10$ V	–	55	–	ns
Fall Time	t_f	$R_{GS} = 50\,\Omega$	–	15	–	ns

* Pulsed : Pulse Width $\leqq 300\,\mu s$, D.R. $\leqq 6\%$

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	$I_{DR} = 1.5$ A, $V_{GS} = 0$ V	–	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$I_{DR} = 1.5$ A, $dI_{DR}/dt = 100$ A/μs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6121D only)

Forward Voltage	V_F	$I_F = 100$ mA	–	–	1.0	V
Reverse Current	I_R	$V_R = 120$ V	–	–	5	μA
Reverse Voltage	V_R	$I_R = 10\,\mu A$	130	–	–	V

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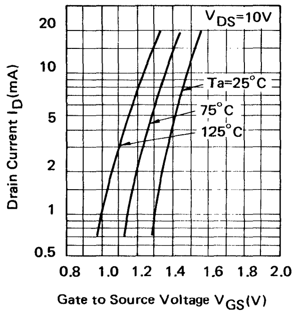
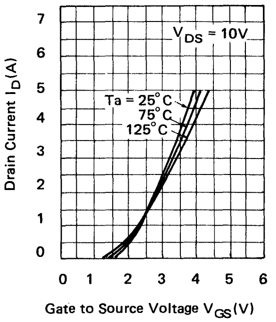
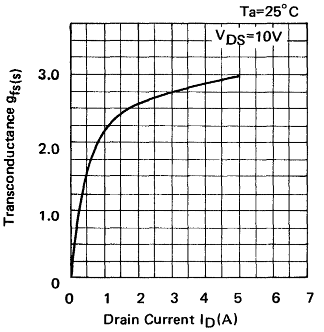
Threshhold Region



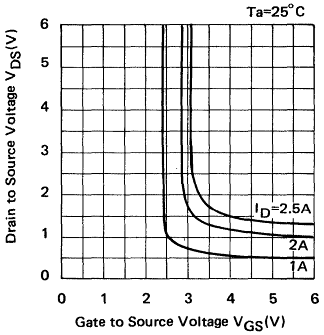
Transfer Characteristics



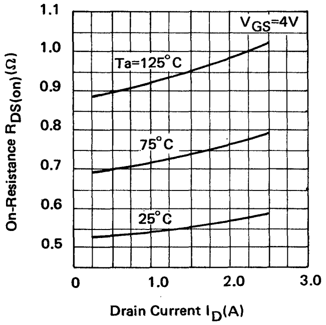
Transconductance-Drain Current



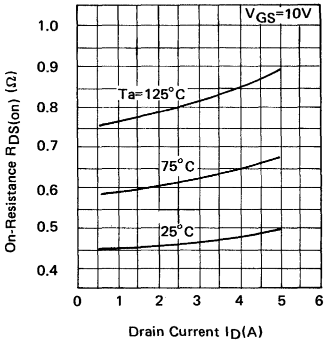
Drain to Source Saturation Region



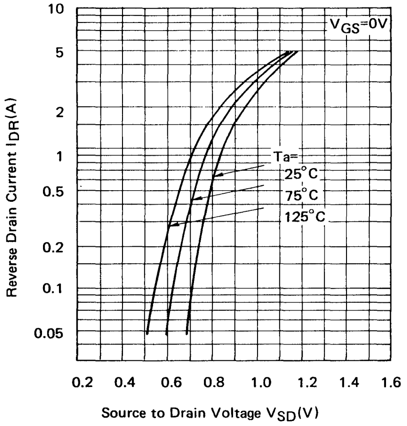
On-Resistance — Drain Current



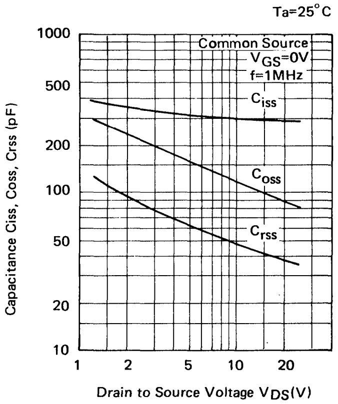
On-Resistance-Drain Current



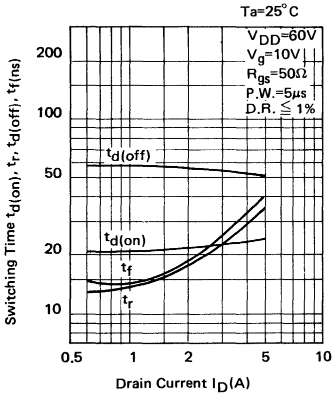
Source-Drain Diode Forward Voltage



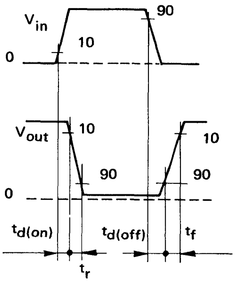
Capacitance-Drain to Source Voltage



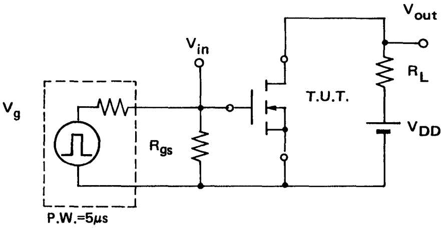
Switching Time — Drain Current



Switching Waveform

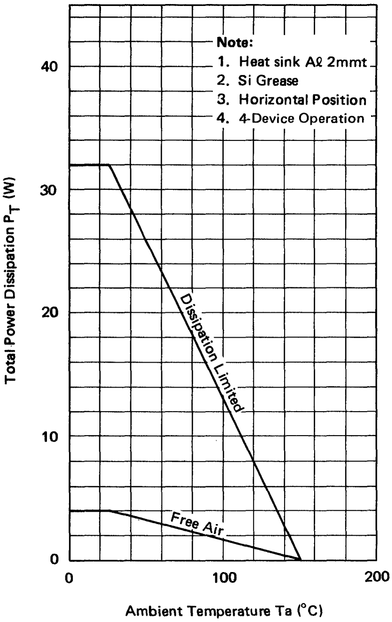


Test Circuit for Switching Time

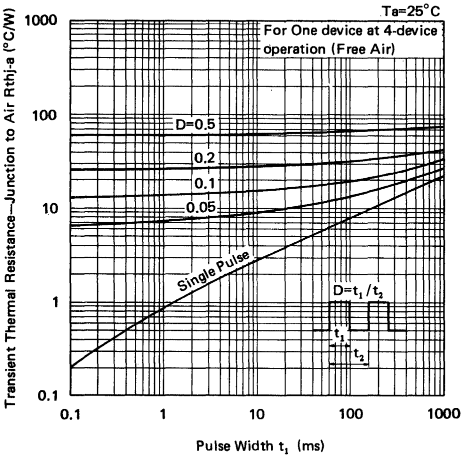


P.W.=5μs
D.R. ≦ 1%

Power Dissipation Derating



Maximum Transient Thermal Resistance



January 1990
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FUJITSU

PRODUCT PROFILE

FT6122, FT6122D

Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET Arrays

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating		Symbol	Condition	Value	Unit
Drain Source Voltage		V_{DSS}		120	V
Gate Source Voltage		V_{GS}		±20	V
Drain Current	Continuous	I_D	Tc = 25°C	4	A
	Pulsed	I_{DM}		8	A
Reverse Drain Current (Continuous)		I_{DR}		4	A
Fast Recovery Diode Forward Current		I_{FM}	$P_W \leqq 0.5$ ms, DR $\leqq$ 25%	4	A
		I_{FSM}	$P_W \leqq 100$ ms, Single Pulse	8	A
Fast Recovery Diode Reverse Voltage		V_R		130	V
Total Drain Power Dissipation		P_T	Ta = 25°C, 4-MOSFET operation	4	W
		P_T	Tc = 25°C, 4-MOSFET operation	36	W
Thermal Resistance Junction to Case		$R_{thj\text{-}c}$	Tc = 25°C, 4-MOSFET operation	3.5	°C/W
Channel Temperature		T_{ch}		+150	°C
Storage Temperature		T_{stg}		-55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 100\ \mu A$, $V_{GS} = 0$ V	120	–	–	V
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120$ V, $V_{GS} = 0$ V	–	–	100	μA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$I_D = 1$ mA, $V_{DS} = 10$ V	0.9	1.3	1.7	V
Static Drain to Source On-State Resistance	$R_{DS(on)}$	$I_D = 3$ A, $V_{GS} = 4$ V *	–	0.32	0.5	Ω
	$R_{DS(on)}$	$I_D = 3$ A, $V_{GS} = 10$ V *	–	0.25	0.4	Ω
Forward Transconductance	g_{fs}	$I_D = 3$ A, $V_{DS} = 10$ V *	2.5	4.5	–	S
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	–	450	550	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	–	140	210	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	–	60	90	pF
Turn-On Delay Time	$t_{d(on)}$	$I_D = 3$ A (See Test Circuit)	–	25	–	ns
Rise Time	t_r	$V_{DD} = 60$ V	–	30	–	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS} = 10$ V	–	75	–	ns
Fall Time	t_f	$R_{GS} = 50\ \Omega$	–	35	–	ns

* Pulsed : Pulse Width $\leqq$ 300 μs, D.R. $\leqq$ 6%

SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

Forward On-Voltage	V_{SD}	$I_{DR} = 3$ A, $V_{GS} = 0$ V	–	1.0	1.2	V
Reverse Recovery Time	t_{rr}	$I_{DR} = 3$ A, $dI_{DR}/dt = 100$ A/μs	–	140	–	ns

FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6122D only)

Forward Voltage	V_F	$I_F = 1$ A	–	–	1.0	V
Reverse Current	I_R	$V_R = 120$ V	–	–	10	μA
Reverse Voltage	V_R	$I_R = 15\ \mu A$	130	–	–	V

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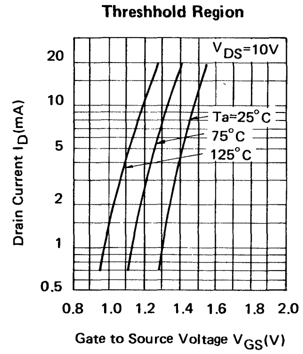
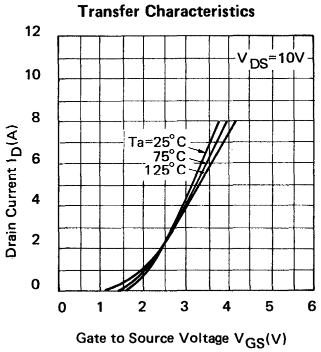
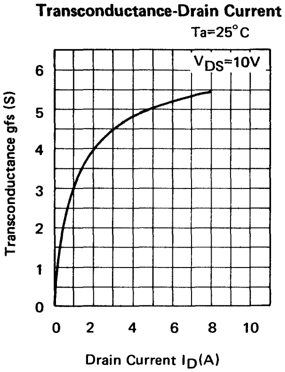
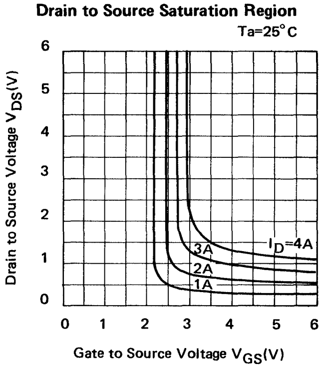
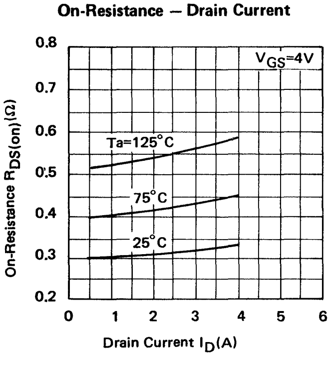
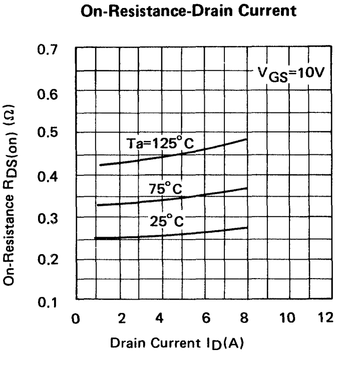

Threshhold Region
V_{DS}=10V
Ta=25°C
75°C
125°C
20
10
5
2
1
0.5
Drain Current I_D(mA)
0.8 1.0 1.2 1.4 1.6 1.8 2.0
Gate to Source Voltage V_{GS}(V)


Transfer Characteristics
V_{DS}=10V
Ta=25°C
75°C
125°C
12
10
8
6
4
2
0
Drain Current I_D(A)
0 1 2 3 4 5 6
Gate to Source Voltage V_{GS}(V)

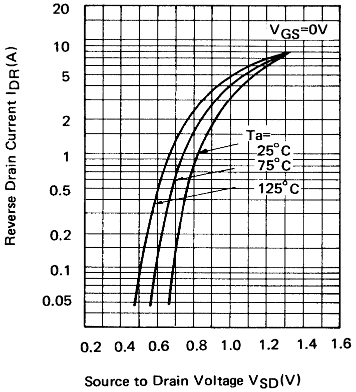

Transconductance-Drain Current
Ta=25°C
V_{DS}=10V
6
5
4
3
2
1
0
Transconductance gfs (S)
0 2 4 6 8 10
Drain Current I_D(A)


Drain to Source Saturation Region
Ta=25°C
I_D=4A
3A
2A
1A
6
5
4
3
2
1
0
Drain to Source Voltage V_{DS}(V)
0 1 2 3 4 5 6
Gate to Source Voltage V_{GS}(V)


On-Resistance — Drain Current
V_{GS}=4V
Ta=125°C
75°C
25°C
0.8
0.7
0.6
0.5
0.4
0.3
0.2
On-Resistance $R_{DS(on)}$(Ω)
0 1 2 3 4 5 6
Drain Current I_D(A)

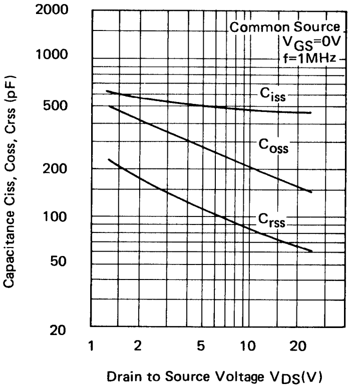

On-Resistance-Drain Current
V_{GS}=10V
Ta=125°C
75°C
25°C
0.7
0.6
0.5
0.4
0.3
0.2
0.1
On-Resistance $R_{DS(on)}$ (Ω)
0 2 4 6 8 10 12
Drain Current I_D(A)

Source-Drain Diode Forward Voltage



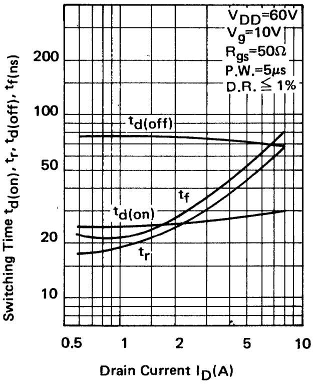
Capacitance-Drain to Source Voltage

Ta=25°C

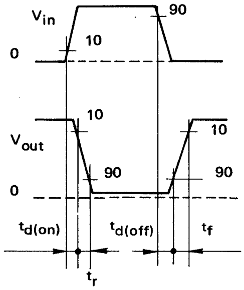


Switching Time — Drain Current

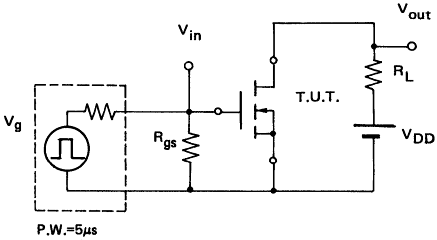
Ta=25°C



Switching Waveform

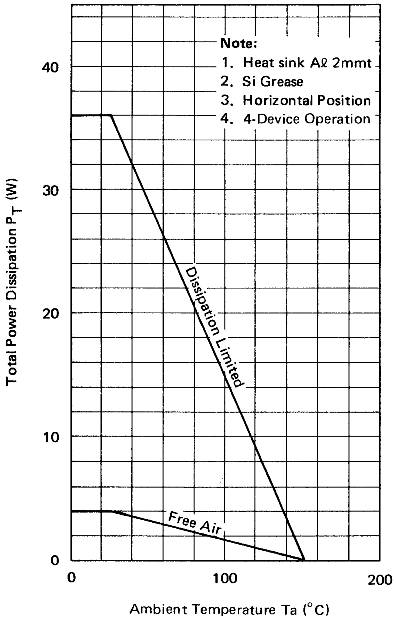


Test Circuit for Switching Time

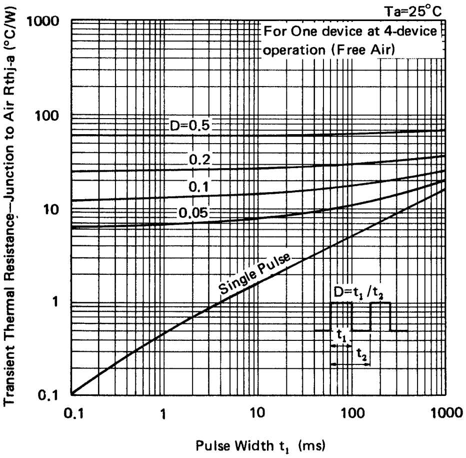


P.W.=5μs
D.R.≦1%

Power Dissipation Derating



Maximum Transient Thermal Resistance



Section 5

Design Information — *At a Glance*

Page **Title**

January 1990
Edition 1.1

A New Ultra-High Speed Voltage Switching Transistor

Fujitsu Microelectronics, Inc.

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ABSTRACT

The silicon Ring Emitter Transistor (RET) device is a power semiconductor which utilizes a concept of combining many small, high frequency transistor cells on one chip, in order to provide high power handling capability. A typical RET consists of several hundred multiple ring-emitters connected to a common emitter electrode through diffused ballast resistors. RET devices offer significant improvement over conventional power transistors due to their high speed switching characteristics and large reverse bias safe operating area (RBSOA). An ultra-high speed switching regulator was constructed with RET devices; based upon test results, this application appears practical and superior to low frequency designs utilizing conventional; transistors.

Introduction

The past decade has witnessed rapid progress in the design of voltage regulators for sophisticated electronic systems. Perhaps the most significant advance has been the development of switching regulators which, compared to series-pass regulators, offer improved efficiency, small size, lighter weight and better reliability. Applications for switching regulators now encompass a wide range of electronic systems; these include computers, microcomputers, communication equipment, test and measurement equipment and consumer products such as audio amplifiers.

The normal switching frequency for switching regulators has been limited to about 20 KHz because of practical limitations imposed by the components utilized to manufacture the products. However, it is recognized that higher frequency regulators would have advantages in size and weight reduction, as well as improved reliability by eliminating the electrolytic capacitor. But in order to design a high frequency switching regulator, new power transistors that can operate reliably at high switching frequencies without additional switching losses are required.

The advanced technology of the RET device offers features which make such high frequency switching regulators possible. This paper will discuss the RET structure, performance and application in a 0.5 MHz switching regulator.

The Ring Emitter Transistor

In power transistor device fabrication, the historical trade-off between speed and power has resulted in optimized performance for safe operating area (SOA) or switching speed (or frequency response), but not both. Usually, high switching speed or frequency could only be obtained by limiting voltage or current parameters to a reduced SOA.

The unique RET structure (discussed in the next section) was developed to solve this problem by permitting a more optimum high switching speed and frequency response without reduction is SOA.

RET Structure

In general, the RET design concept consists of many small geometry high frequency transistor devices integrated on one silicon chip. The multiplicity of parallel connected devices provides the high current capability of the integrated structure.

The RET device typically consists of several hundred small, ring-like shaped emitters connected by a common emitter electrode through diffused resistors. The ballast resistors insure uniform distribution of current to each emitter and prevent thermal runaway, even with a shallow base diffusion.

Figure 1 is a photo-micrograph of a RET transistor chip. In Figure 2 and Figure 3, two types of RET cell geometry are shown. Both types have similar performance characteristics. In Figure 2a, the outer ring-like area is the base contact region, and the enclosed inner region (bold line) is the emitter area. Cross-hatching indicates the diffused ballast resistors. Circular areas in the base contact region are base contact windows. Within the emitter region, there are five rectangular contact windows. The two windows connected by the ballast resistor regions connect the emitter electrodes to the ballast resistors; and the center window connects the ballast resistors to the shorting-bar electrode. The other two windows are emitter area contacts to the shorting-bar electrode. All electrodes are aluminum and are indicated by dashed lines. The cell shown in Figure 2a is 150 x 150μm.

A cell cross-section is shown in Figure 2b at the line A-A indicated in Figure 2a. The base diffusion depth is about 5μm and the emitter diffusion depth is about 2.5μm. The ballast resistor is diffused about 1μm. The center portion of the emitter area is more shallow than the active emitter area in order to reduce internal base resistance and prevent current crowding during turn-off mode.

Current flow in the RET device, referring to Figure 2b is "C" — "i" — "B" — "E" — "S.E." — "R" — "E.E" for an NPN transistor.

The equivalent circuit for the RET device is shown in Figure 2c.

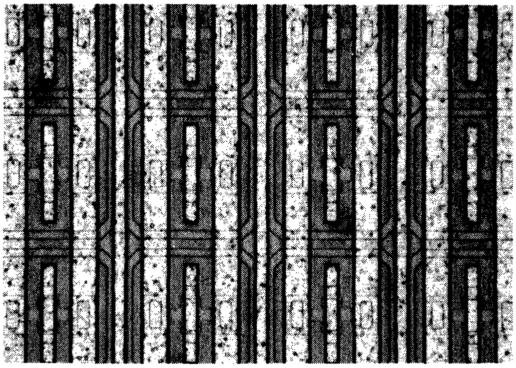


Figure 1. Photomicrograph of RET Chip

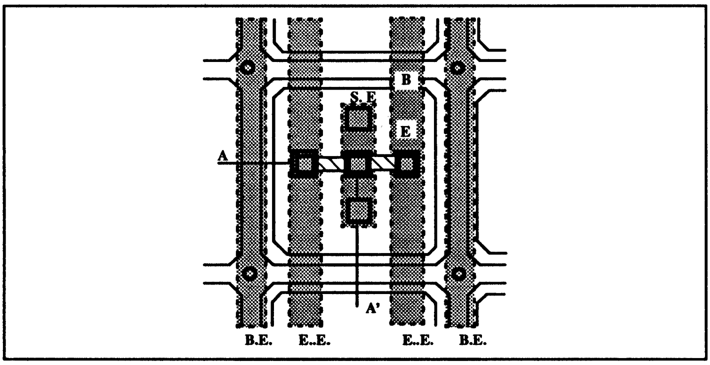


Figure 2a. RET Cell Geometry Dashed Lines Indicate Electrodes

Legend:
E: emitter area
B: base area
E.E: emitter electrodes
B.E: base electrodes
S.E: shorting-bar electrode

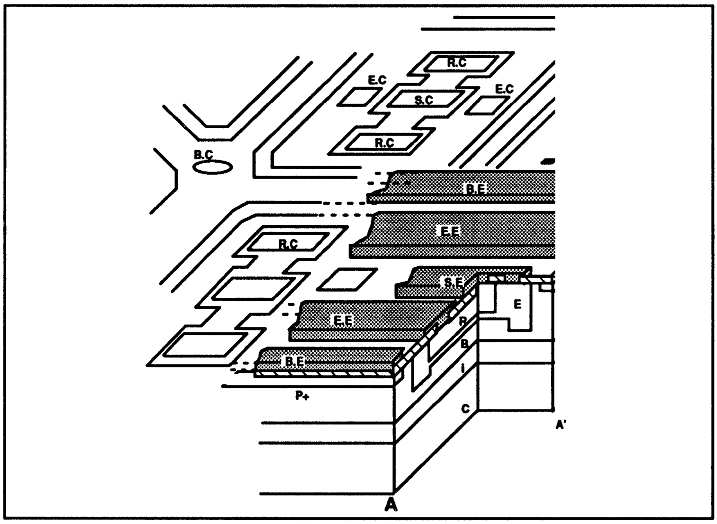
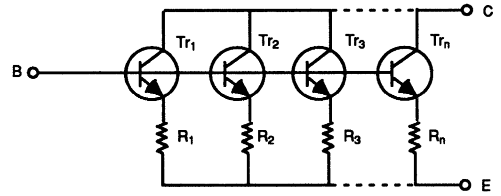


Figure 2b. RET Single Cell Cross Section of Figure 2a, Line A-A.

Legend:
R: diffused ballast resistor layer
E: emitter layer
B: base layer
P+: base contact layer
i: intrinsic layer
C: collector layer
E.E: emitter electrodes
B.E: base electrodes
S.E: shorting-bar electrode
R.C: resistor contact windows
S.C: shorting-bar contact windows
E.C: emitter contact windows
B.C: base contact windows
Cross-hatch areas are silicon dioxide passivation.

Planar technology is utilized in the RET structure to provide stable high voltage operation; and silicon dioxide passivation prevents surface contamination.



Tr1 and R1 represent one RET cell. The RET structure consists of several hundred cells.

Figure 2c. RET Equivalent Circuit

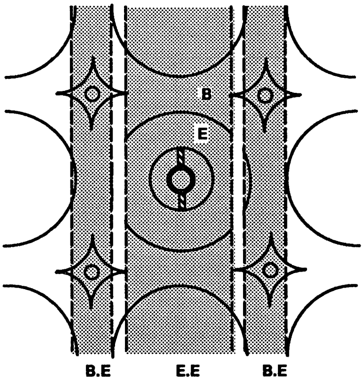


Figure 3. RET Single Cell Geometry

Dashed lines indicate electrodes.

Legend: E: emitter area
B: base area
E.E: emitter electrode
B.E: base electrode

RET Performance Characteristics

DC Current Gain

RET devices have very linear DC current gain. This is attributed to the large emitter periphery, reduced base resistance and uniform current distribution through the diffused ballast resistors.

Gain Bandwidth Product and Safe Operating Area

Gain bandwidth product (f_t) is a function of base width. Conventional power transistors can be built with a high gain bandwidth product, but only by sacrificing SOA. However, with the RET structure, both high f_t and large SOA can be achieved. The RET shallow base, which permits high f_t, will not result in thermal runaway problems because the ballast resistors control uniform current distribution to each emitter. Further, the ballast resistors provide greater power dissipation area and improve the secondary breakdown characteristics of the device.

Saturation Voltage

Saturation voltage is a function of emitter periphery and the resistance of the collector layer, intrinsic layer, base layer, emitter layer and, in the case of a RET, the ballast resistor; that is, the resistance of the current path in the transistor. For a unit RET cell, the diffused ballast resistor has a value of about 15 ohms. For a RET device with 758 cells, the parallel resistance value of all the cells is only about 20 milliohms for the entire chip. Further, the base resistance is reduced by the long emitter periphery relative to the small base area. This permits relatively low saturation voltage at high operating currents.

Switching Time and Reverse Bias Safe Operating Area (RBSOA)

In general, a conventional power transistor designed for high switching speed cannot withstand the energy in-rush in the reverse bias turn-off mode. The flyback voltage (V_f) at turn-off can be written as:

$$V_f = V_{CEX} - V_{CC} = L \frac{di}{dt}$$

$$\cong L \frac{I_{cp}}{t_f} \quad (1)$$

Where: V_{CEX} = collector-emitter voltage
V_{CC} = collector bias voltage
L = load inductance
I_{cp} = peak collector current
t_f = fall time

Thus, a fast turn-off device with limited current handling capability (or vice-versa) is limited by its maximum RBSOA to driving relatively smaller inductive loads.

With the RET structure, a method for solving the problem caused by the relationship between RBSOA and switching time has been determined. Two different kinds of RET structure were made experimentally. In Type-A, the length of one side of the unit cell was 150µm; in Type-B, the cell side dimension was 400µm. Identical wafer processing conditions were utilized, and both devices had the same base area and electrical ratings (V_{CEO} = 400 V, I_C = 15 A, P_C = 150 W). Experimental results are shown in Table 1.

Table 1. Comparison of Experimental Data for Two Types of RET Structure

Characteristics	Units	A	B
Unit Size	µ	150	400
No. of Unit at One Chip	pcs	758	112
Emitter Area (AE)	cm2	0.078	0.076
Emitter Periphery (LE)	cm	33.6	15.2
LE/AE	1/cm	431	200
DC Current Drain	—	35	35
Gain Bandwidth Product	MHz	35	35
Rise Time	µS	0.15	0.32
Storage Time	µS	1.20	1.20
Fall Time	µs	0.10	0.28
Secondary Breakdown			
Current	A	12	3

From Poisson's equation, the secondary breakdown current, $I_{S/B}$, (3), (4), (5) can be written by:

$$I_{S/B} = E_C^2.Z^2.\ \begin{array}{l} E.V.\ V.W \\ (S\ t\ B)\ (2) \\ V_{CE}.I_{BV}.P_B \end{array}$$

Where: E_C = critical field corresponding to the onset of avalanche injection
Z = emitter periphery dimension
E = permittivity
V_S = electron saturation voltage
V_T = thermal voltage
W_B = base width
V_{CE} = clamped voltage
I_B = base current
P_B = base resistivity

$I_{S/B}$ is measured with the test circuit shown in Figure 4.

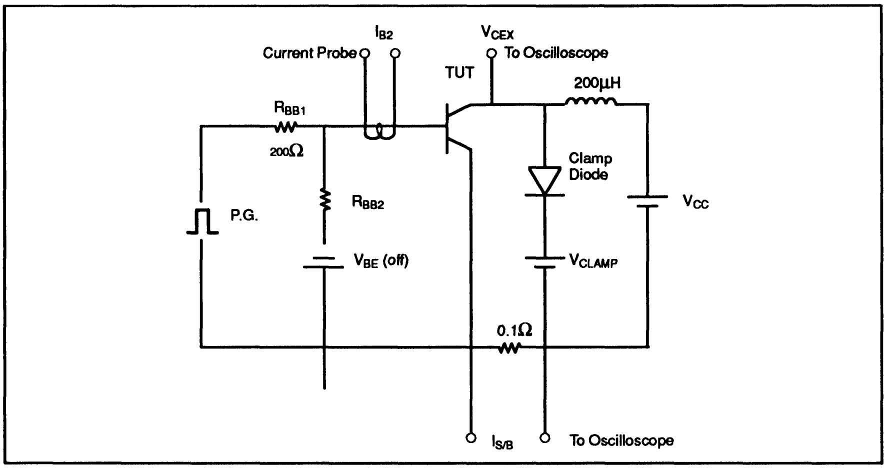
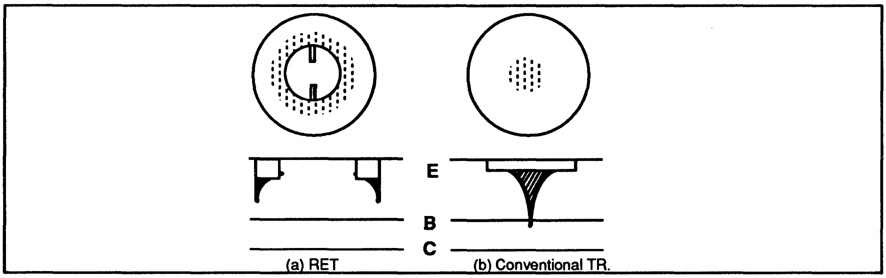


Figure 4. Test Circuit Used for Measurement of Reverse Bias SOA and V_{CEX} (sus)

Under reverse bias turn-off conditions, the current is usually concentrated in the center portion of the emitter area of a conventional power transistor. But in a RET structure, the ring emitter geometry constrains current concentration to a large periphery at the inner edge of the ring. Figure 5 shows the RET current concentration, Figure 5a, compared with a conventional device, Figure 5b. Therefore, as the Figure indicates, a shallow, low resistance base is adequate for a higher current density.



(a) RET (b) Conventional TR.

Figure 5. Transistor Current Concentration in Turn-off Mode

Legend: E: emitter
B: base layer
C: collector layer

Experimental results indicate that $I_{S/B}$ and fall time collate to cell unit size; that is, they are proportional to internal base resistance. This is shown in Figure 6 for the experimental results listed in Table 1. The results compare well with the theoretical calculation of Poisson's equation [eq. (2)] $I_{S/B}$ which is plotted with a dashed line in Figure 6.

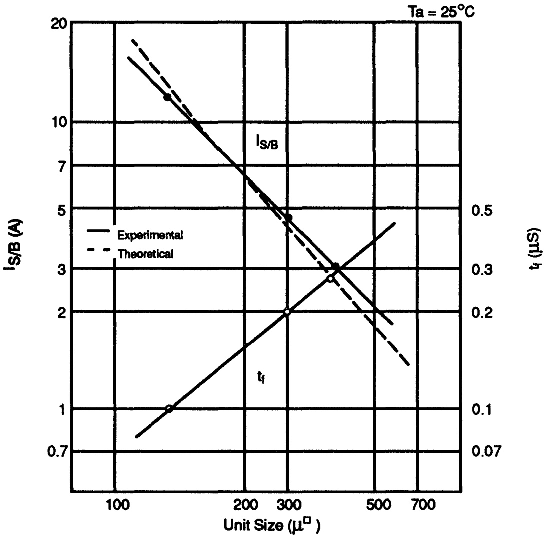


Figure 6. $I_{S/B}$ and t_f at the Dependence of Unit Size

Therefore, the structural features of a power transistor device which offers good RBSOA and fast switching characteristics, such as the RET, can be summarized as follows:

a. Large emitter periphery in a limited base area.
b. Reduced base resistance.
c. Hollowed-out center portion of the emitter area.
d. Uniform, shallow diffusion of the base and emitter regions.

Figure 7 shows switching time at the dependence of collector current for the Type-A RET, 2SC2429. Figure 8 shows RBSOA for the same device compared to a conventional power transistor geometry.

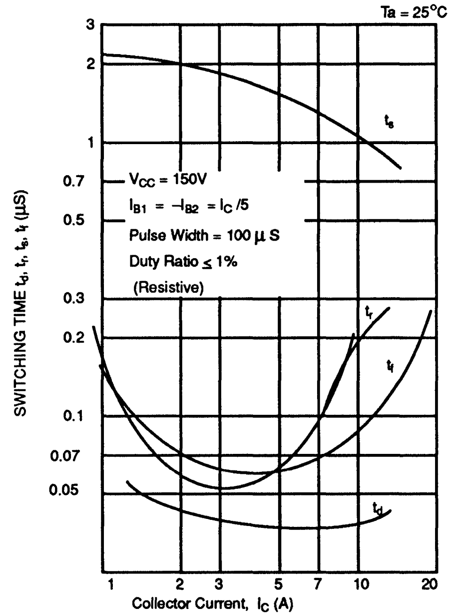


Figure 7. Switching Time

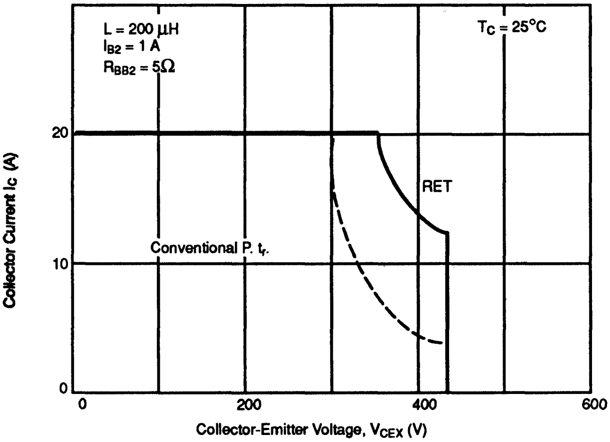


Figure 8. Reverse Bias Safe Operation Area

Temperature Characteristics

In a power transistor, electrical characteristics at the dependence of temperature are of critical importance in most applications. In a conventional transistor, case temperature must be maintained in the 60°C to 80°C region for normal steady state operation to prevent degradation of switching speeds. With the RET structure, the device characteristics exhibit less variation at the dependence of temperature. This is shown in Figure 9 which compares fall time and storage time for conventional and RET (2SC2429) devices at the dependence of case temperature.

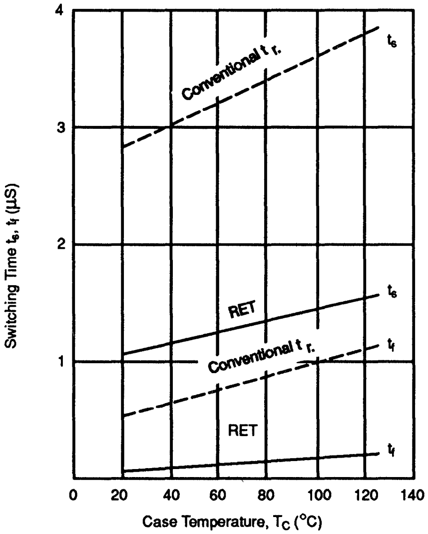


Figure 9. Switching Time at the Dependence of Case Temperature

A High Frequency Switching Regulator Using RET

A high frequency, single-end forward type DC-DC switching converter can be constructed with RET devices.For experimental purposes, four such systems were constructed utilizing the 2SA1041 RET at switching frequencies of 20 KHz, 100 KHz, 0.5 Hz and 1.0 MHz. The same circuit was also utilized for comparison with conventional switching transistors except that operation was found to be impractical above 200 KHz. Results comparing the RET to the conventional transistor are shown in Figure 10 which plots power loss vs. frequency for the power transistor.

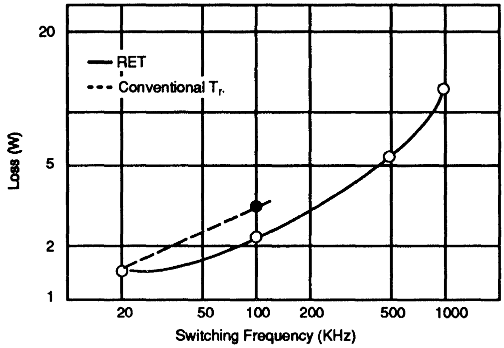


Figure 10. Loss Measurement in Converter Application

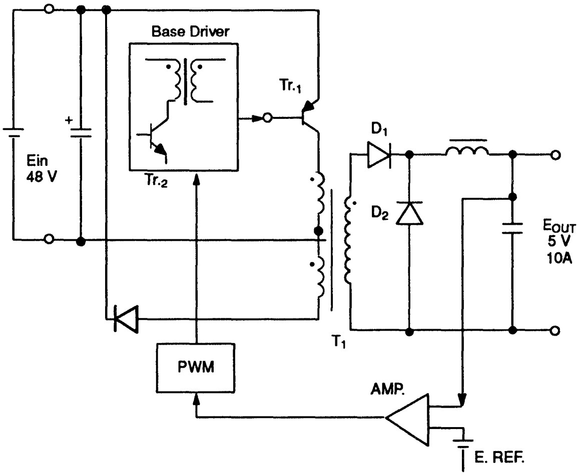
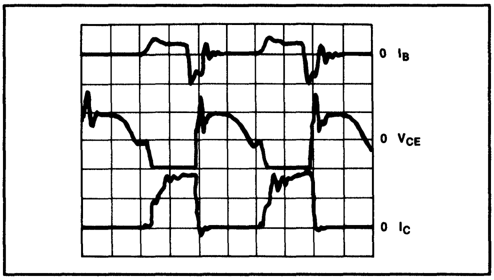


Figure 11. Block Diagram of DC-DC Converter, 0.5 MHz

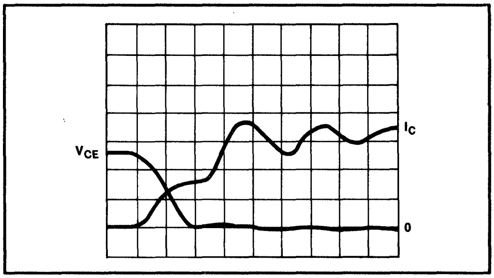
tr.$_1$ RET (2SA1041)

TR$_2$: 2SC2080, 2SC1150

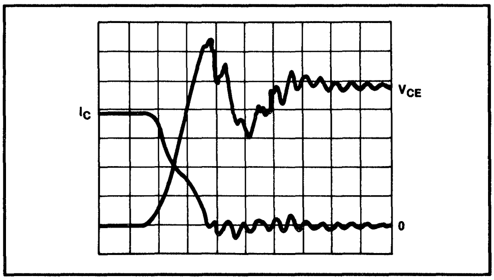
Figure 11 shows the circuit block diagram of the 0.5 MHz converter. Input voltage is 48 V DC, and output voltage is 5 V and 10 A. Rectifiers D_1 and D_2 are Schottky barrier diodes. The magnetic core material of the main transformer is ferrite. The operating waveforms for the main switching device, RET 2SA1041, are shown in Figure 12. Figure 13 shows output voltage regulation and efficiency at the dependence of the output current. Total conversion efficiency above 4 amps was better than 80 percent..



**12a. Operating Waveforms Time: 0.5μS/div.,
I_B: 500 mA/div.,V_{CE}: 50/div., I_C: 2A/div.**



**12b. Turn-on Waveforms Time: 50 nsS/div.,
V_{CE}: 20V/div., I_C: 1A/div.**



**12c. Turn-off Waveforms Time: 50 nsS/div.,
V_{CE}: 20V/div., I_C: 1A/div.**

Figure 12. Operating Waveforms of DC-DC Converter, 0.5 MHz

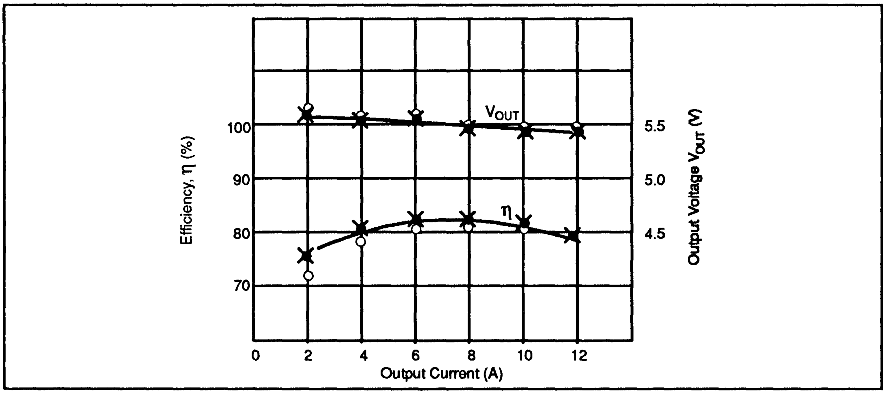


Figure 13. Output and Efficiency of RET Converter

Legend: X: $V_{IN} = 43$ V DC
•: $V_{IN} = 48$ V DC
0: $V_{IN} = 53$ V DC

Conclusion

The RET structure is a superior power transistor for applications where high RBSOA and fast switching speed are required.

Switching speed and RBSOA depend on internal base resistance which is minimized in the design of a RET. RET devices can operate satisfactorily in high frequency switching regulators. An experimental circuit was constructed that result in 80 percent efficiency at a switching frequency of 0.5 MHz.

In the future, if smaller geometry cells are realized, even better RBSOA and higher switching speeds may be obtainable.

Acknowledgement

The authors would like to thank Mr. Y. Saito and Mr. K. Katori for their helpful suggestions and comments.

References

J. R. Hauser. *IEEE Trans. on Electron Devices*. Ed. 11, pp.238–242 (1964)

P. L. Hawer and V. G. K. Reddi. *IEEE Trans. on Electron Devices*, Ed. 17, pp. 320–335 (1970)

M. Kobayashi and Y. Nawata. *Nikkei Electronics No. 165*, pp. 106–1215 (1073) (in Japanses)

S. Krishina and P. L. Hower. *Proceeding of the IEEE*, No,. 61, pp. 393–395 (1973)

K. Tsuda. *Mikkei Electronic No. 191*, pp. 87–99 (1978) (in Japanese)

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FUJITSU

APPLICATION NOTE

Power Transistor Application

Techniques for Obtaining Optimum Performance from Ring Emitter Transistors

(Reprinted from Application Note AN003)

Fujitsu Microelectronics, Inc.

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Introduction

The past decade has witnessed rapid progress toward the sophistication of efficient switching regulators for use in electronic systems.

The normal switching frequency of regulators has been limited to around 20 KHz because of inadequacies in both active and passive components used to manufacture the regulator. However, it is recognized that higher frequency regulators would offer incredible advantages in decreasing size and weight, not to mention a savings in energy and resources.

In order to design such a high frequency switching regulator, new power transistors are needed that can operate reliably at high speed without additional switching losses. The advanced bipolar technology of the Ring Emitter Transistor device now makes such high frequency operation possible and economical.

This application note will discuss how to derive the maximum performance from the RET.

Maximum Ratings and Electrical Characteristics

(Note: This section will reference a 2SC3056A, which is a 450 V, 6 amp RET.)

Collector-Emitter Avalanche Voltage

Figure 1 shows the shape of the avalanche characteristics of a triple diffused power transistor which is identical to that of the RET.

V_{CEO}	Collector-Emitter Breakdown Voltage, Base Open
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage, Base Open
V_{CER}	Collector-Emitter Breakdown Voltage, Base-Emitter Resistor
$V_{CEX(VCEV)}$	Collector-Emitter Breakdown Voltage, Base-Emitter Reverse Bias
V_{CES}	Collector-Emitter Breakdown Voltage, Base-Emitter Short
V_{CBO}	Collector-Base Breakdown Voltage, Emitter Open

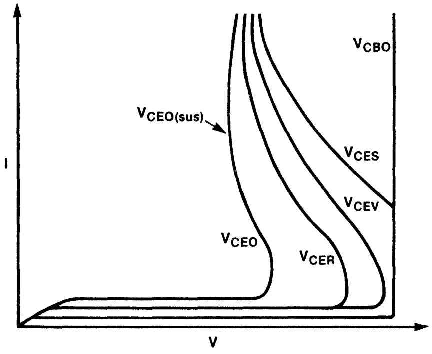

Figure 1. Avalanche Characteristics

Collector and Base Count

The maximum collector current (continuous and pulsed) and base current (continuous) are determined as follows:

Collector Current (continuous) – I_C:

DC current applied for five minutes with no damage.

Collector Current (pulse) – I_{CP}:

$P_W \leq 10$ ms, D. R. $\leq 2\%$ (2SC3056A)

Base Current (continuous):

Same condition as for I_C

Safe Operating Area

Forward Bias Safe Operating Area, Base-Emitter Forward Bias (Figure 2).

There are four types of limitations:

1. Collector Current (pulse) Limit
2. Thermal Limit
3. Secondary Breakdown Limit
4. $V_{CEO(sus)}$ Limit

The RET has FBSOA also specified at high temperature.

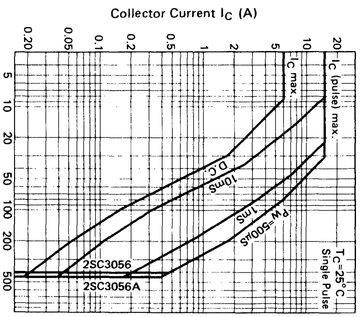

Figure 2. Forward Bias Safe Operating Area

Reverse Bias Safe Operating Area, Base Emitter Reverse Bias (Figure 3)

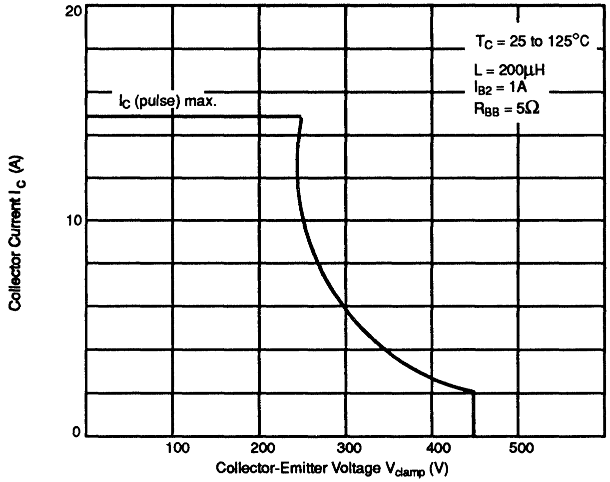

Figure 3. Reverse Bias Safe Operating Area

RBSOA is the most important criteria for determining how a transistor performs during inductive turn-off. The RBSOA of the RET is 100 percent tested for the load line being shaped inside the RBSOA line.

Leakage Current

Collector leakage current represents one aspect of reliability for a transistor device. In general, the collector leakage current is only specified at T_a = 25°C, but since switching regulators rarely run at this low temperature, high temperature characterization is necessary. This is also especially important when considering that leakage current increases over temperature. The leakage current of the RET is specified at t_C = 100°C as well as t_a = 25°C.

Saturation Region and Switching Speed

Figure 4 shows the familiar V_{CE} versus I_C curve.

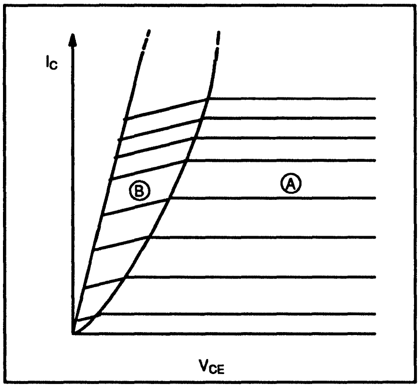

Figure 4. Saturation Regions

There are two kinds of saturation regions; hard saturation region (A) and quasi-saturation region (B). Figure 5 shows the saturation region of the 2SC3056A. If the transistor is used at I_C = 3 A, the base current for saturation is more than .4 amps. The saturation region is closely related to the switching time, because of the stores charge.

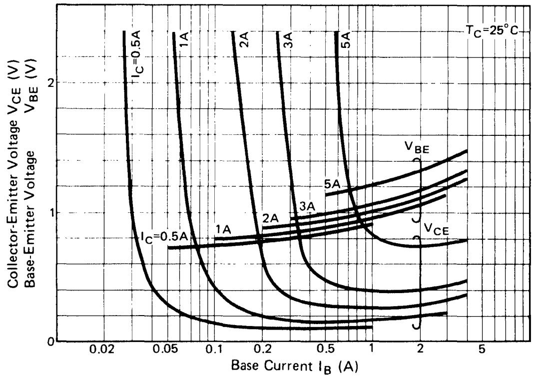

Figure 5. Collector Saturation Region

Switching Time

The switching characteristics of a transistor depend on the rate of decrease or increase of stored charges in the base and collector region. Figure 6 shows the switching waveform and the stored charge changes.

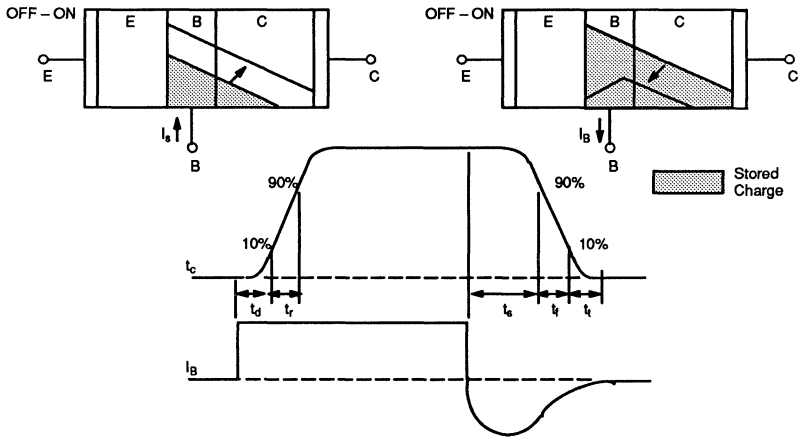

Figure 6. Schematic Drawing of a Transistor as a Switch

The following transistor states occur during various states of the RET device.

OFF State to ON State

1. Base emitter bias added
2. Base emitter junction capacitance charge
3. Junction is forward biased
4. Accumulation of charge in the collector
5. Accumulation of charge in the base continues until it reaches the final value of the collector current.

ON State

1. Conductive modulation; the transistor is in the saturation region $V_{CE(SAT)}$

ON State to OFF State

1. Base emitter bias reduced and negative bias added
2. Reduction of collector current
3. Reduction of the stored charge in the collector and base region
4. Base emitter junction and collector-base junction return to the cut off state independently

Specific recommendations for obtaining maximum performance from the RET

It is important not to have too little base drive current. If the transistor is not in the saturation region, the collector current and the collector emitter voltage add simultaneously and the SOA is exceeded, hence burn-out.

It is also important not to have too much base drive current. Assuming the transistor is in the hard saturation region, the switching speed (storage time, fall time) becomes very slow. Figure 7 shows the switching speed at the dependence of the base drive current. Under the conditions $I_C = 3$ A, $I_{B1} = 0.6$ A and $I_{B2} = 1$ A, we can obtain $t_{stg} = 900$ ns, $t_f = 60$ ns.

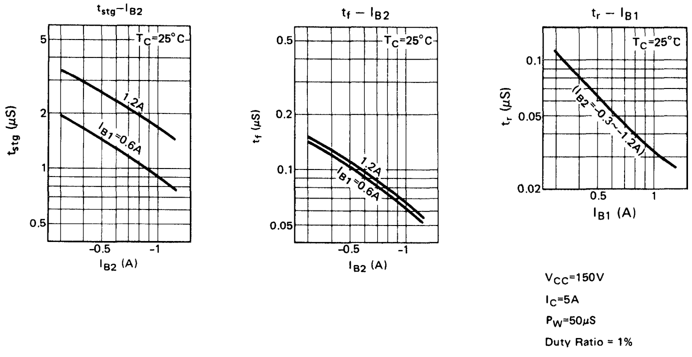

Figure 7. Switching Time

The fast switching speed means the following:

Base Drive (Figure 8)

1. Large volume of capacitance (C) is not required.
2. The speed-up diode (D) is not always required.
3. The distance between the transistor and drive magnetic core has to be short without any leakage inductance.
4.. The distance between the emitter of the transistor and ground has to be short without any leakage inductance.

Main Transformer

The distance between the transistor and the main transformer has to be short without any leakage inductance.

Using the techniques recommended in this application note, we have constructed experimental regulators capable of switching at 500 KHz with over 80 percent efficiency. In the future, as smaller geometry RET cells are realized, even better RBSOA and faster switching speeds will be obtained.

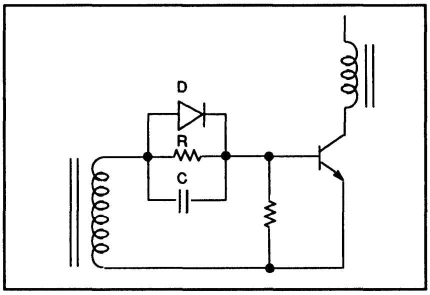

Figure 8. Base Drive Circuit Example

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APPLICATION NOTE

Power Transistor Application

A 100 KHz, 50 Watt Switching Regulator (Single-Ended Forward Type) Using the Bipolar Ring Emitter Transistor

(Reprinted from Application Note AN005)

Fujitsu Microelectronics, Inc.

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Introduction

The 100 KHz regulator was designed and built to demonstrate how an extremely efficient low ripple switching regulator can be built cost effectively by taking advantage of the performance inherent to the RET transistor.

The major constraint of this design was to keep the component cost low and still achieve very respectable output characteristics. Small size and light weight were a primary consideration as well.

A conversion efficiency of 74 percent with an output ripple content of 30 mV peak-to-peak was achieved. Voltage regulation was maintained to within 1 percent. (See Figure 1.)

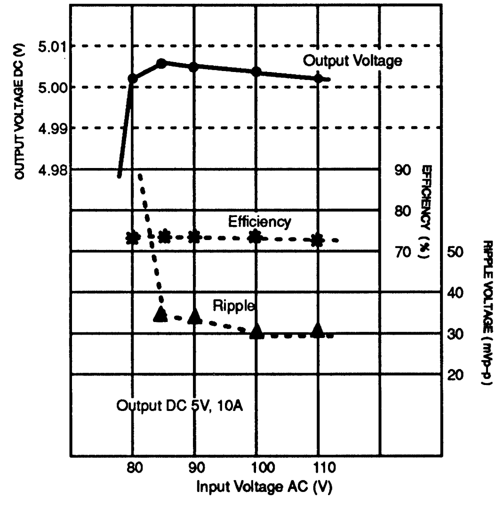

Figure 1. 100 KHz – 50 W Single-Ended Forward Type Switching Regulator (2SC3056A)

A block diagram is shown in Figure 2.

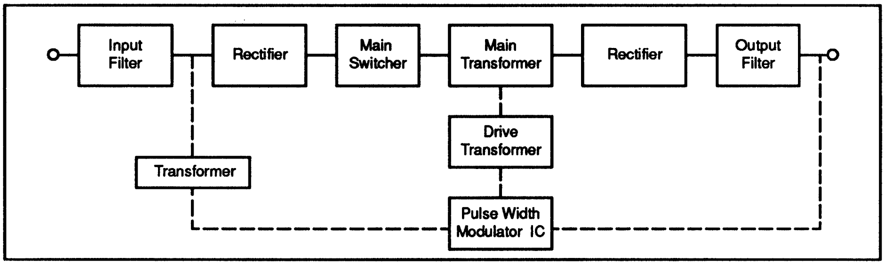

Figure 2. Block Diagram of 100 KHz – 50 W Switching Regulator

Circuit

The circuit detail is shown in Figure 3 and the parts list is shown in Table 1.

Turn-on and Turn-off

Turn-on and turn-off waveforms are shown in Figures 4, 5, and 6. The following losses were measured:

Turn-on loss – 0.06 W
Output 5 VDC, 10A (50 W)
Turn-off loss – 0.92 W

Transistor operating regions are shown in Figures 5 and 6. The characteristics of the main switching transistor (2SC3056A) are as follows:

Turn-on Crossover Time – 90 ns	IC = 1.6 A
Turn-off Crossover Time – 60 ns	IB_1 = 0.35 A
Storage Time – 600 ns	IB_2 = –0.8 A

Switching Regulator-Physical Size

The outline of the 100 KHz – 50 W switching regulator is shown in Figure 8. The volume without the heatsink radiator is 20.58 cu in (4.2″L x 3.5″W x 1.4 ″H″).

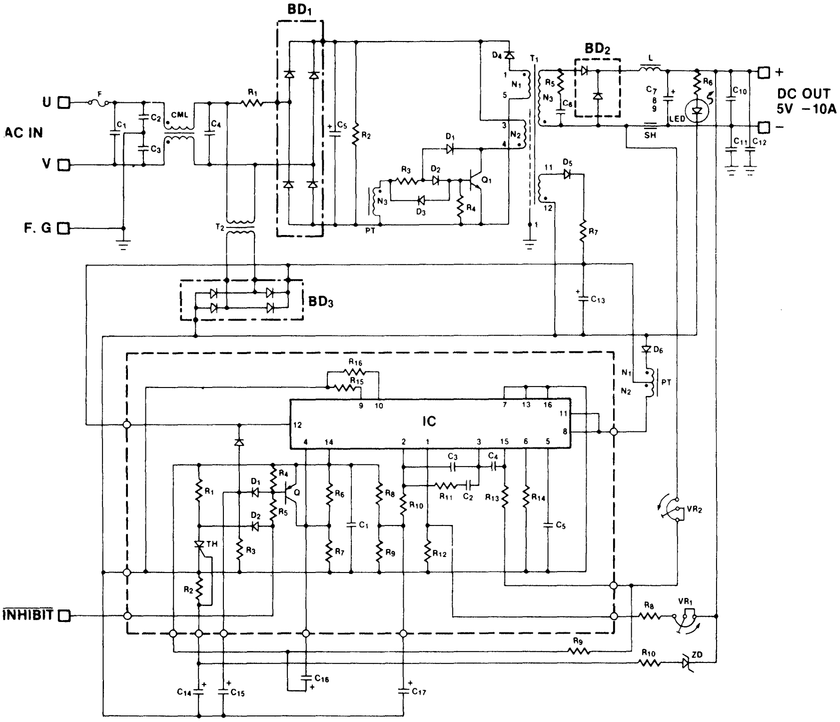

Figure 3. 100 KHz – 50 W (Single-Ended Forward Type) Switching Regulator (2SC3056A)

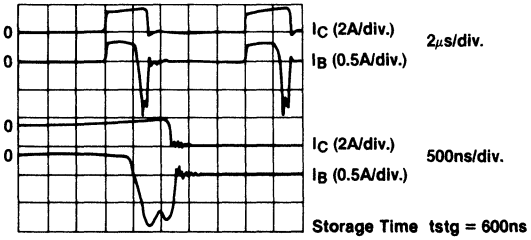

Figure 4.

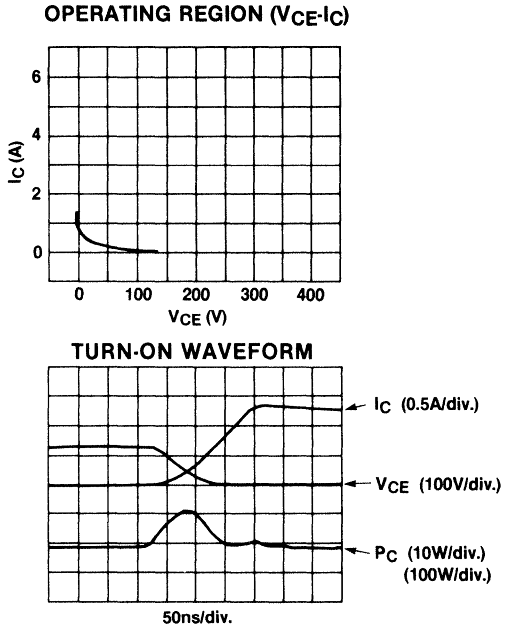

Figure 5. Operating Region of Turn-on Waveform

Table 1. Parts List

RESISTORS
Main Circuit
R1 – 5W, 1Ω, 10% wirewound
R2 – 1W, 100KΩ, 5% metal fillm
R3 – 1W, 15Ω, 5% metal fillm
R4 – 1/2W, 56Ω, 5% carbon fillm
R5 – 1/2W, 15Ω, 5% carbon fillm
R6 – 1/2W, 470Ω, 5% carbon fillm
R7 – 1/4W, 2.2Ω, 5% carbon fillm
R8 – 1/4W, 1KΩ, 5% carbon fillm
R9 – 1/4W, 4.7Ω, 5% carbon fillm
R10 – 1/4W, 1KΩ, 5% carbon fillm
Control Circuit
R1 – 1/8W, 1KΩ,5% carbon film
R2 – 1/8W, 1KΩ,5% carbon film
R3 – 1/8W, 3.3KΩ,5% carbon film
R4 – 1/8W, 2.2KΩ,5% carbon film
R5 – 1/8W, 2.2KΩ,5% carbon film
R6 – 1/8W, 3.9KΩ,5% carbon film
R7 – 1/8W, 1.8KΩ,5% carbon film
R8 – 1/8W, 1KΩ,5% carbon film
R9 – 1/8W, 1KΩ,5% carbon film
R10 – 1/8W, 10KΩ,5% carbon film
R11 – 1/8W, 100KΩ,5% carbon film
R12 – 1/8W, 2.2KΩ,5% carbon film
R13 – 1/8W, 10KΩ,5% carbon film
R14 – 1/8W, 1.5KΩ,5% carbon film
R15 – 1/4W, 2.2KΩ,5% carbon film
R16 – 1/4W, 2.2KΩ,5% carbon film

CAPACITORS
Main Current
C1 – .1MF, 100 V, metalized film
C2 – 2200PF, 1000 V, ceramic
C3 2200PF, 1000 V, ceramic
C4 – .1MF, 100 V, metalized film
C5 – 330MF, 50, electrolytic
C6 – 4700PF, 1K V, ceramic
C7 – 2200MF, 50 V, electrolytic
C8 – 2200MF, 50 V, electrolytic
C9 – 2200MF, 50 V, electrolytic
C10 – 2200MF, 50 V, electrolytic
C11 – 4700PF, 1K V, ceramic
C12 – 4700PF, 1K V, ceramic
C13 – CEUSM1E331 (330MF, 25 V)
C14 – CESSM1H010 (1MF, 50 V)
C15 – CESSM1H010 (1MF, 50 V)
C16 – CESSM1C100 (10MF)
C17 – CESSM1C100 (10MF)
Control Circuit
C1 –.01MF, 50 V, ceramic
C2 –.0068MF, 50 V, ceramic
C3 –100PF, 50 V, ceramic
C4 –.0022MF, 50 V, ceramic
C5 –.0047MF, 50 V, ceramic

DIODES
Main Circuit
D1 –Switching Diode (V196 Hitachi)
D2 –Switching Diode (V196 Hitachi)
D3 –Switching Diode (V196 Hitachi)
D4 –Switching Diode (V196 Hitachi)
D5 –Switching Diode (V196 Hitachi)
D6 –Switching Diode (1S1585 Toshiba)
BD1 –Diode Bridge (1G4B41 Toshiba)
BD2 –Schottky Twin Diode (ESA D83-004 Fuji Electronics)
BD3 –Diode Bridge (1B4B42 Toshiba)
2D –5.2 V, ±2% Zener (H25C Hitachi)
D1-D2 –Switching Diode (1S1585 Toshiba)
Control Circuit
2D –4.3 V, ±2% Zener (H24C Hitachi)

TRANSISTORS
Main Circuit
Q1 –2SC3056A (Fujitsu)
Control Circuit
Q2 –2SA495 (Tobisha)

TRANSFORMERS
T1, T2, T3–TDK H7C1 core, n1 = n2 = 22T
1 mm wire n3 = 3T 2 mm wire
PT –TDK H7C1 core, n1 = n2 = 45T
1 mm wire n3 = 15T 2 mm wire

POTENTIOMETER
VR1 –Murata 3321N-1-102
VR2 –Murata 3321N-1-201
TH –Thyristor (SFOR1A42 Toshiba)
IC –Pulse Width Modulator (MB3759 Fujitsu)

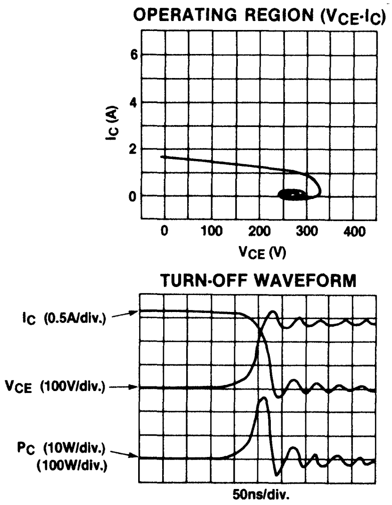

Figure 6. Operating Region of Turn-off region

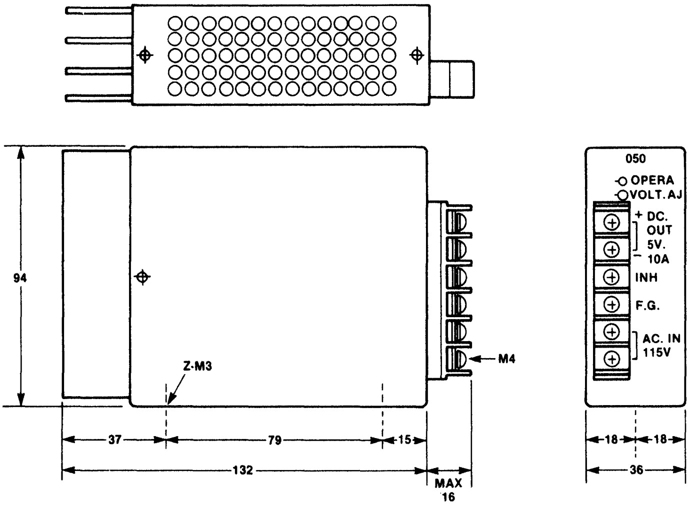

Figure 7. Outline of 100 KHz-50 W Switching Regulator (Dimensions in mm)

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APPLICATION NOTE

Power Transistor Application

A 50 KHz, 200 Watt Half-Bridge Switching Power Supply Using Ring Emitter Transistors

Fujitsu Microelectronics, Inc.

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Introduction

To demonstrate how excellent performance characteristics can be achieved when using bipolar ring emitter transistors in classic switching regulator circuits, a half-bridge supply was constrructed with the Fujitsu 2SC3058 transistor. The total conversion efficiency was 82 percent. Figure 1 is a block diagram of the regulator.

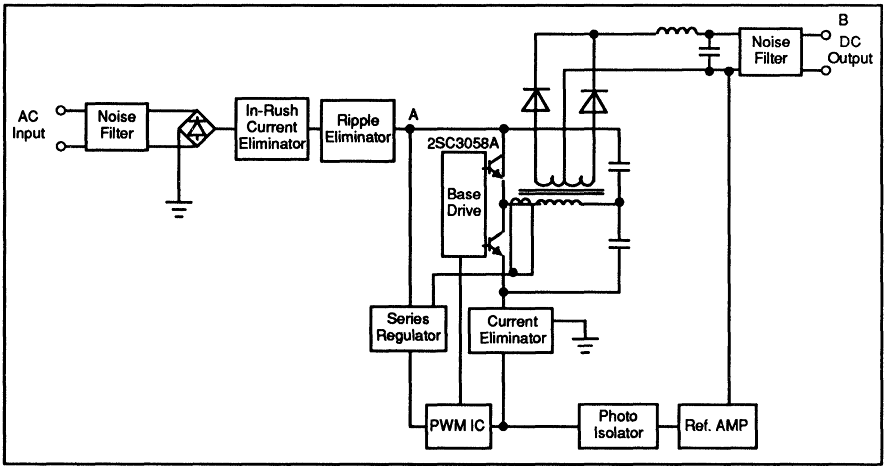


Figure 1. 50 KH-200 W Half-Bridge Switching Regulator Block Diagram

Characteristics of the 2SC3058A

The 2SC3058A is a high voltage, high current and fast switching device which was specifically designed for high frequency, high power switching regulators. Its electrical characteristics are shown in Table 1.

Table 1. Electrical Characteristics (T_A = 25°C)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1\text{mA}, I_E = 0$	600	—	—	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1\text{mA}, I_C = 0$	7	—	—	V
Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	$I_C = 0.8\text{A}, R_{BE} = \infty\Omega$	450	—	—	V
Collector to Emitter Sustaining Voltage	$V_{CEX(sus)}$	$I_C = 10\text{A}, I_{B2} = -2\text{A}, L = 200\ \mu\text{H}$ (*1)	450	—	—	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500\text{ V}, I_E = 0$	—	—	100	µA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 500\text{ V}, I_E = 0, T_C = 100°\text{C}$	—	—	2	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6\text{ V}, I_C = 0$	—	—	100	µA
DC Current Gain	h_{FE}	$V_{CE} = 5\text{ V}, I_C = 20\text{A}$ (*2)	10	12	40	—
Collector to Emitter-saturation Voltage	$V_{CE(SAT)}$	$I_C = 20\text{A}, I_B = 4\text{A}$ (*2)	—	0.7	1.0	V
Base to Emitter-saturation Voltage	$V_{BE(SAT)}$		—	1.25	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10\text{ V}, I_{E,} = 0, f = 1\text{MHz}$	—	420	—	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10\text{ V}, I_C = 4\text{A}$	—	30	—	MHz
Rise Time	t_r	$V_{CC} = 150\text{ V}$ (*1) $I_C = 20\text{A}, I_{B1} = I_{B2} = 4\text{A}$	—	0.20	0.5	µs
Storage Time	t_{stg}		—	1.70	2.0	µs
Fall Time	t_f		—	1.10	0.3	µs

Legend: *1 Test Circuit

*2 Pulsed $P_W \leq 300\mu s$, Duty Ratio 8–6%

The Circuit

Figure 2 describes the circuit of the 50 KHz power supply. Other than the 2SC3058A, the major switching components are:

Drive Transformer

EE-30, Ferrite (H7C1, TDK)
N1 = 15T, N2 = 15T, N3 = 2T

Main Transformer

EE-40, Ferrite (H7C1, TDK)
N1 = 8T, N2 = 1T, N3 = 1T

Schottky Diode

ERG – 81 – 004

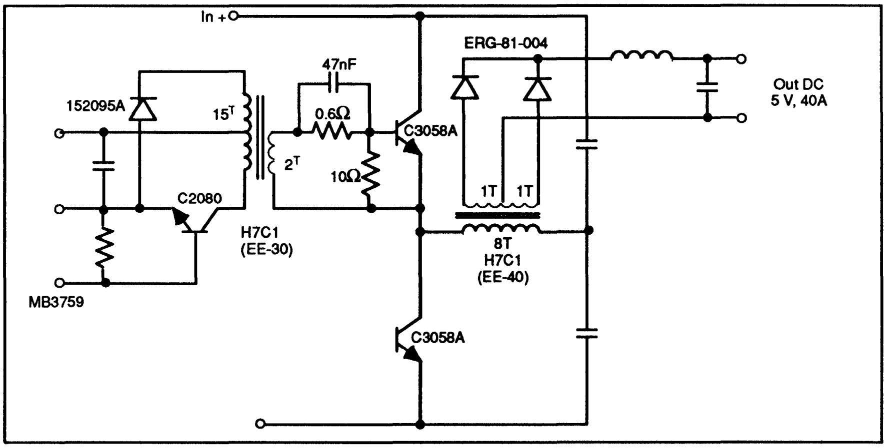


Figure 2. The Circuit

Characteristics of the Regulator

To measure switching speeds, several kinds of waveforms must be analyzed.

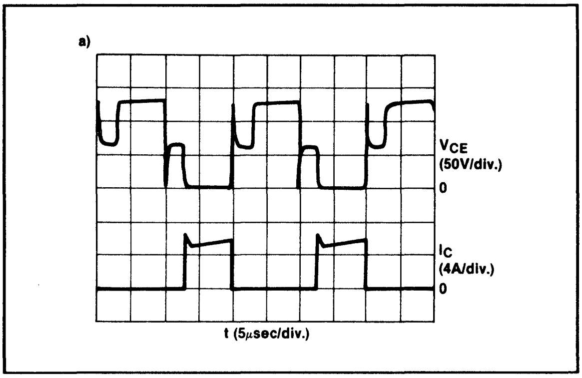


Figure 3a. V_{CE} and I_C vs. t

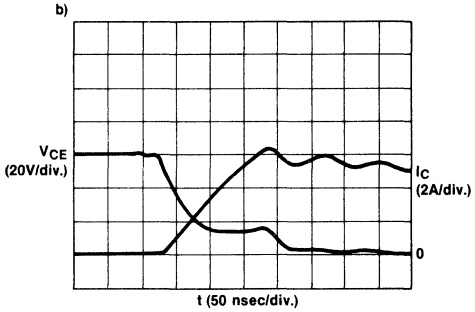


Figure 3b. V_{CE} and I_C vs. t (Turn-on)

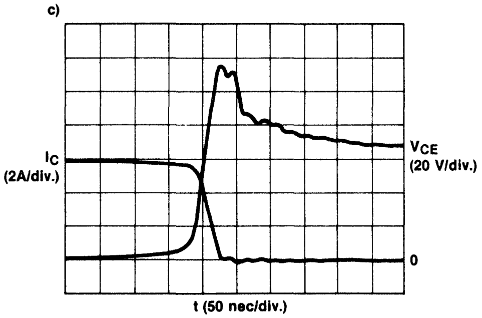


Figure 3c. V_{CE} and I_C vs. t (Turn-off)

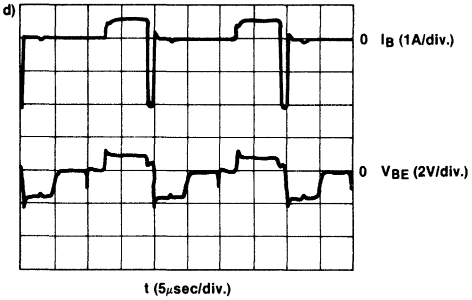


Figure 3d. I_B and V_{BE} vs. t

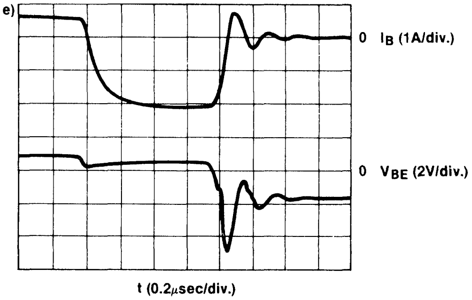


Figure 3e. I_B and V_{BE} vs. t (Turn-off)

A measured conversion efficiency of 82 percent was achieved with the regulator switching speed determined to be:

$t_r = 120$ ms $I_{B1} = .6$A,
$t_{stg} = 850$ ms $I_{B2} = -2.2$A, $I_C = 6$A
t_c (crossover time) = 40 ms I_C

Figure 4 shows the efficiency and voltage regulation as a function of DC output current.

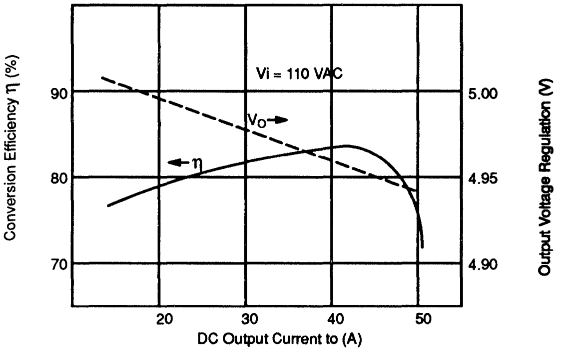


Figure 4. Characteristics of the Regulator

Quality Control at Fujitsu

Built-In Quality and Reliability

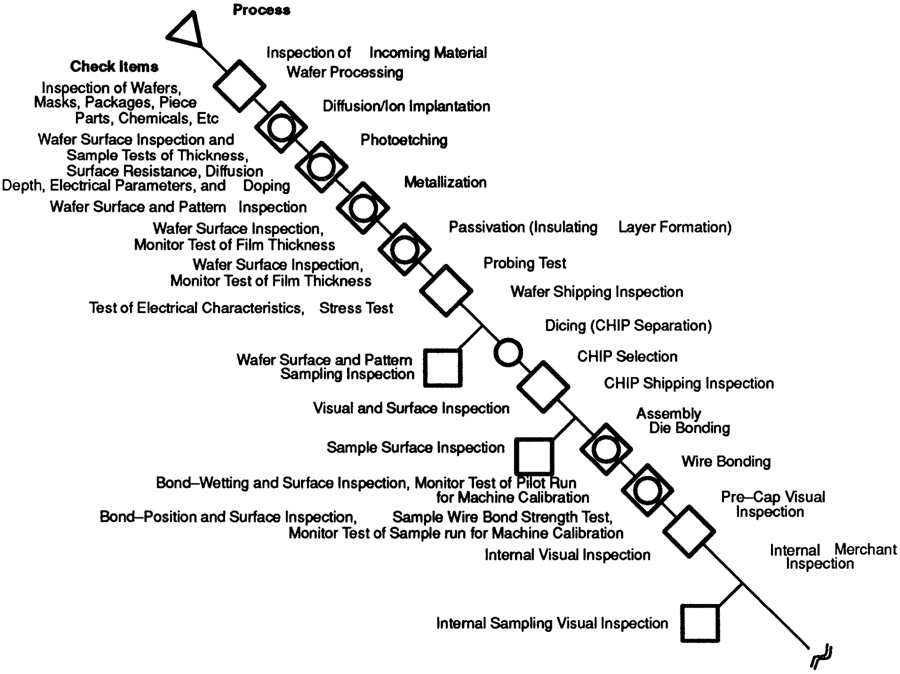
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



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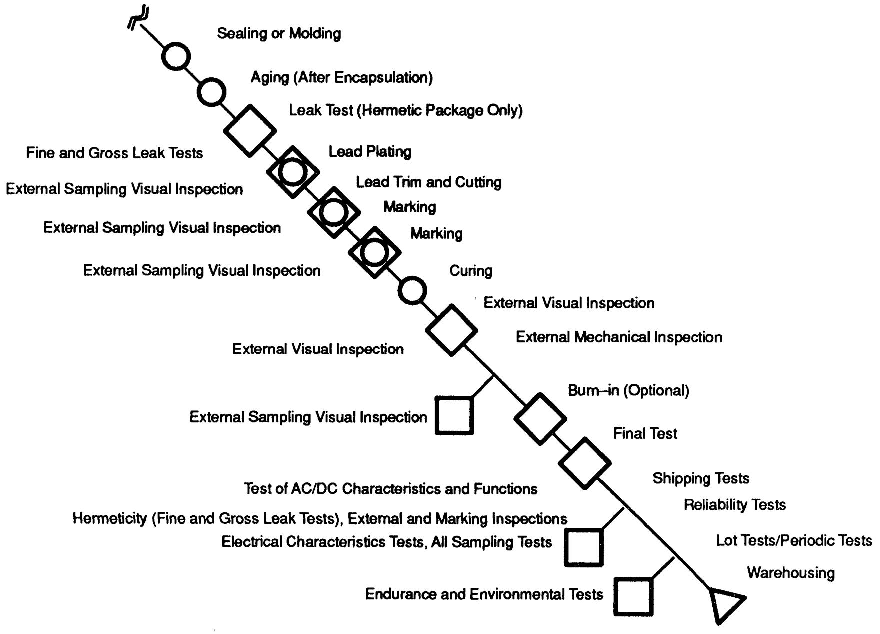
Quality Control Processes at Fujitsu (Continued)



Legend:

○ Production Process

□ Test/Inspection

◙ Production Process and Test/Inspection

◇ QC Gate (Sampling)

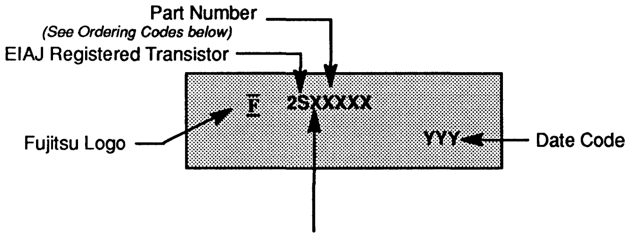
Note:
The flow sequence may vary slightly with individual product type.

Section 6

Ordering Information — *At a Glance*

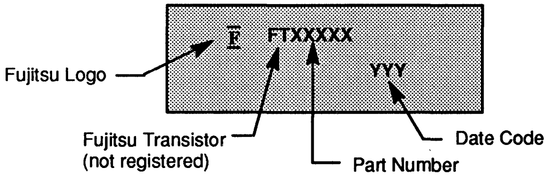
Transistor Product Marking

Ring Emitter Transistors (RETs)



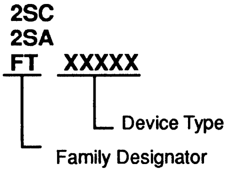
Polarity
A = PNP, High Frequency
B = NPN, High Frequency
C = NPN, Low Frequency
D = NPN, Low Frequency

Darlington Arrays, MOSFET Arrays, RETs



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

Transistor Ordering Code (Part Number)



2SC = High Frequency NPN
2SA = High Frequency PNP
FT = Fujitsu Transistor
Example: 2SC2429 High Frequency NPN Transistor, V_{CEO} = 400 V, I_C = 15 A

Transistor Package Types

Products are available in the following package types.

TO–3		TO–220		TO–3pF		TO–66	
PNP	NPN	PNP	NPN	PNP	NPN	PNP	NPN
2SA1041	2SC2428	2SA1077	2SC2527		2SC3842	FT2551	FT1551
2SA1042	2SC2429	2SA1078	2SC2528		2SC3843		
2SA1043	2SC2429A	2SA1080	2SC2530		2SC3844		
2SA1044	2SC2431		2SC3055		2SC3845		
2SA1045	2SC2432		2SC3056		2SC3846		
2SA1072	2SC2433		2SC3056A		2SC3847		
2SA1073	2SC2434		2SC3057		2SC3947		
2SA1180	2SC2522		2SC3178		2SC3948		
	2SC2522A				2SC3949		
	2SC2523						
	2SC2920						
	2SC2964						
	2SC2965						
	2SC3044						
	2SC3044A						
	2SC3045						
	2SC3046						
	2SC3058						
	2SC3058A						
	2SC3059						
	2SC3060						
	2SC3061						

Section 7

Sales Information — *At a Glance*

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

DRAMs and DRAM Modules
EPROMs
EEPROMs
NOVRAMs
CMOS masked ROMs
CMOS SRAMs and CMOS SRAM Modules
BiCMOS SRAMs
Bipolar PROMs
ECL RAMs
STRAMs (self-timed RAM)
Hi-Rel PROMs and SRAMs
Ultra High-speed ECL/ECL—TTL Translator Circuits
Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet^{R} is a registered trademark of Xerox Corporation.
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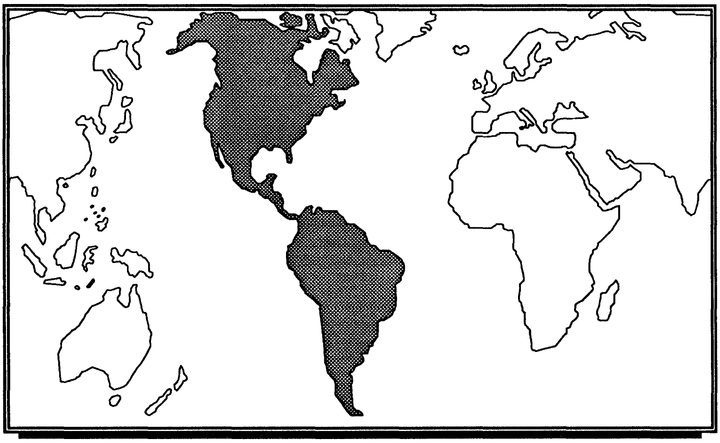

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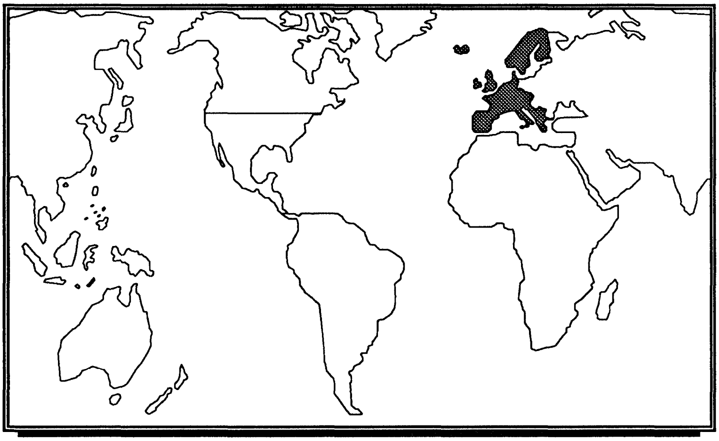

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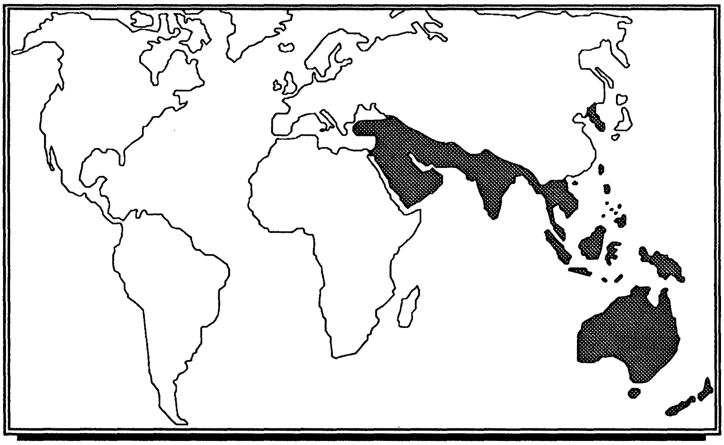

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Section 8

Appendix – Table of Product Specifications

Appendix – Product Specifications for Ring Emitter Transistors

Page	Device	Case	Type	Absolute Maximum Ratings							
				V_{CBO} (V)	V_{EBO} (V)	V_{CEO} (V)	I_C (A)	I_B (A)	P_C (W)	T_J (°C)	T_{STG} (°C)
1–3	2SA1041	JEDECTO-3	PNP	–120	–5	–120	–15	–5	100	+175	–65 - +175
	2SA1042	JEDECTO-3	PNP	–70	–5	–70	–15	–5	100	+175	–65 - +175
	2SC2431	JEDECTO-3	NPN	120	5	120	15	5	100	+175	–65 - +175
	2SC2432	JEDECTO-3	NPN	70	5	70	15	5	100	+175	–65 - +175
1–7	2SA1043	JEDECTO-3	PNP	–120	–5	–120	–30	–10	150	+175	–65 - +175
	2SA1044	JEDECTO-3	PNP	–70	–5	–70	–30	–10	150	+175	–65 - +175
	2SC2433	JEDECTO-3	NPN	120	5	120	30	10	150	+175	–65 - +175
	2SC2434	JEDECTO-3	NPN	70	5	70	30	10	150	+175	–65 - +175
1–11	2SA1072	JEDECTO-3	PNP	120	7	120	12		120	+150	–65 - +150
	2SA1072A	JEDECTO-3	PNP	150	7	150	12		120	+150	–65 - +150
	2SA1073	JEDECTO-3	PNP	160	7	160	12		120	+150	–65 - +150
1–13	2SA1077	JEDECTO-220	PNP	120	7	120	10		60	+150	–65 - +150
1–15	2SA1078	JEDECTO-220	PNP	120	5	120	2		25	+150	–65 - +150
1–17	2SA1080	JEDECTO-220	PNP	40	7	40	0.5		20	+150	–65 - +150
1–19	2SC2428	JEDECTO-3	NPN	180	7	180	12	3	120	+175	–65 - +175
1–21	2SC2522	JEDECTO-3	NPN	120	7	120	12		120	+150	–65 - +150
	2SC2522A	JEDECTO-3	NPN	150	7	150	12		120	+150	–65 - +150
	2SC2523	JEDECTO-3	NPN	160	7	160	12		120	+150	–65 - +150
1–23	2SC2525	RM-60	NPN	120	7	120	12		120	+150	–65 - +150
	2SC2526	RM-60	NPN	160	7	160	12		120	+150	–65 - +150
1–25	2SC2527	JEDECTO-220	NPN	120	7	120	10		60	+150	–65 - +150
1–27	2SC2528	JEDECTO-220	NPN	120	5	120	2		25	+150	–65 - +150
1–29	2SC2530	JEDECTO-220	NPN	40	7	40	0.5		20	+150	–65 - +150
1–31	2SC2429	JEDECTO-3	NPN	450	7	400	15	5	150	+175	–65 - +175
	2SC2429A	JEDECTO-3	NPN	600	7	450	15	5	150	+175	–65 - +175
	2SC2920	JEDECTO-3	NPN	450	7	400	15	5	150	+175	–65 - +175
	2SC2964	JEDECTO-3	NPN	600	7	400	15	5	150	+175	–65 - +175
	2SC2965	JEDECTO-3	NPN	600	7	450	15	5	150	+175	–65 - +175

Appendix – Product Specifications for Ring Emitter Transistors (Continued)

Page	**Device**	**Case**	**Type**	**Absolute Maximum Ratings**							
				V_{CBO} (V)	**V_{EBO} (V)**	**V_{CEO} (V)**	**I_C (A)**	**I_B (A)**	**P_C (W)**	**T_J (°C)**	**T_{STG} (°C)**
1–45	2SC3044	JEDECTO-3	NPN	450	7	400	6	4	100	+175	–65 - +175
	2SC3044A	JEDECTO-3	NPN	450	7	450	6	4	100	+175	–65 - +175
1–51	2SC3045	JEDECTO-3	NPN	450	7	400	10	5	100	+175	–65 - +175
1–57	2SC3046	JEDECTO-3	NPN	600	7	450	10	5	100	+175	–65 - +175
1–63	2SC3055	JEDECTO-220	NPN	450	7	400	2	1	15	+150	–55 - +150
1–69	2SC3056	JEDECTO-220	NPN	450	7	400	6	4	50	+150	–55 - +150
	2SC3056A	JEDECTO-220	NPN	450	7	450	6	4	50	+150	–55 - +150
1–75	2SC3057	JEDECTO-220	NPN	450	7	400	10	5	50	+150	–65 - +150
1–81	2SC3058	JEDECTO-3	NPN	600	7	400	30	10	200	+175	–65 - +175
1–87	2SC3058A	JEDECTO-3	NPN	600	7	450	30	10	200	+175	–65 - +175
1–93	2SC3059	JEDECTO-3	NPN	1200	7	850	2	1	100	+175	–65 - +175
	2SC3060	JEDECTO-3	NPN	1200	7	850	5	3	150	+175	–65 - +175
	2SC3061	JEDECTO-3	NPN	1200	7	850	10	5	200	+175	–65 - +175
	2SC3178	JEDECTO-3	NPN	1200	7	850	2	1	60	+150	–55 - +150
1–113	FT1551	JEDECTO-66	NPN	120	4	120	2		20	+150	–65 - +150
1–115	FT2551	JEDECTO-66	PNP	120	4	120	2		20	+150	–65 - +150

Appendix – Product Specifications for Full Plastic Mold Ring Emitter Transistors

				Absolute Maximum Ratings							
Page	**Device**	**Case**	**Type**	V_{CBO} (V)	V_{EBO} (V)	V_{CEO} (V)	I_C (A)	I_B (A)	P_C (W)	T_J (°C)	T_{STG} (°C)
2–5	2SC3842	TO-3PF	NPN	600	7	400	10	5	70	+150	–55 - +150
2–9	2SC3843	TO-3PF	NPN	600	7	450	10	5	75	+150	–55 - +150
2–13	2SC3844	TO-3PF	NPN	600	7	450	15	5	75	+150	–55 - +150
2–17	2SC3845	TO-3PF	NPN	1200	7	800	3	1	75	+150	–55 - +150
2–21	2SC3846	TO-3PF	NPN	1200	7	800	6	3	80	+150	–55 - +150
2–25	2SC3847	TO-3PF	NPN	1200	7	800	10	5	85	+150	–55 - +150
2–29	2SC3947	TO-3PF	NPN	850	7	500	5	2	70	+150	–55 - +150
2–33	2SC3948	TO-3PF	NPN	850	7	500	10	4	75	+150	–55 - +150
2–37	2SC3949	TO-3PF	NPN	850	7	500	15	6	80	+150	–55 - +150

Appendix – Product Specifications for Darlington Transistor Arrays

Page	Device	Case	Polarity	Absolute Maximum Ratings						
				V_{CBO}(V)	V_{CEO} (V)	I_C, D_C (A)	I_{CP} Pulsed (A)	*P_T T_a = 25°C (W)	*P_T T_c = 25°C (W)	Typical h_{FE}
3–9	FT5753M	RM–65	NPN	150	100	±1.5	±3	4	19	6000
	FT5756M	RM–65	NPN	150	100	±1.5	±3	4	19	6000
3–11	FT5754M	RM–65	NPN	150	100	±3	±5	5	21	6000
	FT5757M	RM–65	NPN	150	100	±3	±5	5	21	6000
3–13	FT5755M	RM–65	NPN	150	100	±5	±8	5	25	4000
	FT5758M	RM–65	NPN	150	100	±5	±8	5	25	4000
3–15	FT5759M	RM–65	PNP	–100	–100	±1.5	±3	4	19	6000
3–17	FT5760M	RM–65	PNP	–100	–100	±3	±5	5	21	6000
3–19	FT5761M	RM–65	PNP	–100	–100	±5	±8	5	25	6000
3–21	FT5763M	RM–67	NPN	150	100	±1.5	±3	3.5	17	6000
	FT5766M	RM–67	NPN	150	100	±1.5	±3	3.5	17	6000
3–23	FT5764M	RM–67	NPN	150	100	±3	±5	4	19	6000
	FT5767M	RM–67	NPN	150	100	±3	±5	4	19	6000
3–25	FT5769M	RM–67	PNP	–100	–100	±1.5	±3	3.5	17	6000
3–27	FT5770M	RM–67	PNP	–100	–100	±3	±5	4	19	6000
3–29	FT5776M	RM–65	NPN/PNP	100 –100	100 –100	±1.5	±3	4	19	6000
3–33	FT5777M	RM–65	NPN/PNP	100 –100	100 –100	±3	±5	5	21	6000
3–37	FT5777M	RM–65	NPN/PNP	100 –100	100 –100	±5	±8	5	25	6000
3–41	FT5786M	RM–67	NPN/PNP	100 –100	100 –100	±1.5	±3	3.5	17	6000
3–45	FT5787M	RM–67	NPN/PNP	100 –100	100 –100	±3	±5	4	19	6000

*4 DARLINGTON TRANSISTORS OPERATION

Appendix – Product Specifications for Field Effect Transistor Arrays

			Maximum Ratings (T_a = 25°C)				Electrical Characteristics (T_a = 25°C)		
Page	Device	Case	V_{DSS} (V)	I_D, D_C (A)	*P_T (W)	T_{CH} (°C)	**R_{DS} (on) Typical (OHM)	V_{GS} (off) Typical (V)	C_{ISS} Typical (pF)
4–7	FT6110	RM–65	120	±2	4	150	1.2	1.3	130
	FT6110D	RM–65	120	±2	4	150	1.2	1.3	130
4–11	FT6111	RM–65	120	±3	5	150	0.55	1.3	280
	FT6111D	RM–65	120	±3	5	150	0.55	1.3	280
4–15	FT6112	RM–65	120	±4.5	5	150	0.32	1.3	450
	FT6112D	RM–65	120	±4.5	5	150	0.32	1.3	450
4–19	FT6120	RM–67	120	±1.5	3.5	150	1.2	1.3	130
	FT6120D	RM–67	120	±1.5	3.5	150	1.2	1.3	130
4–23	FT6121	RM–67	120	±2.5	4	150	0.55	1.3	280
	FT6121D	RM–67	120	±2.5	4	150	0.55	1.3	280
4–27	FT6122	RM–67	120	±4	4	150	0.32	1.3	450
	FT6122D	RM–67	120	±4	4	150	0.32	1.3	450

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