Data Book

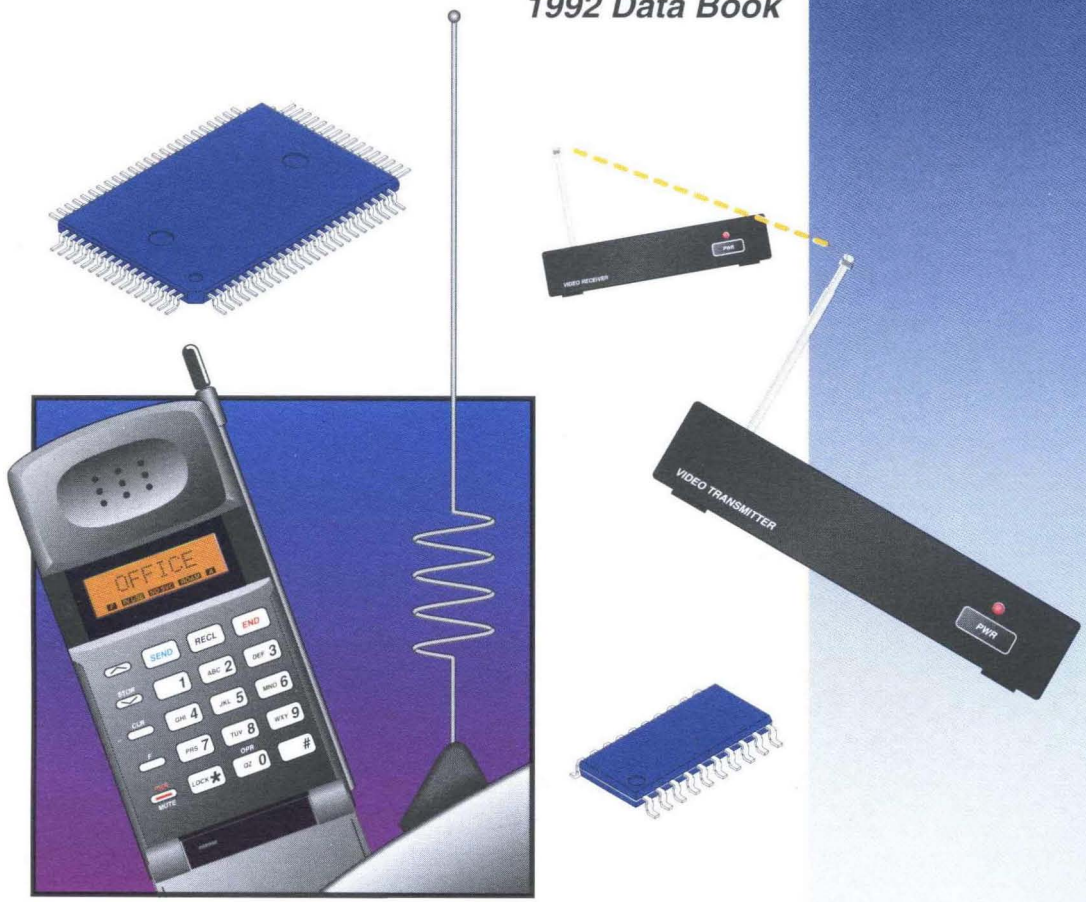
Telecommunications Products

1992

FUJITSU

Telecommunications Products

1992 Data Book



FUJITSU

Prescalers 1
Phase-Locked Loops (PLLs) 2
Single-Chip PLLs/Prescalers 3
Single-Chip VCOs/Prescalers 4
Piezoelectric Devices 5
Cordless Telephone Integrated Circuits 6
Telephone Integrated Circuits 7
Coders/Decoders (CODECs) 8
Quality and Reliability 9
Ordering Information 10
Sales Information 11
Appendix: Design Information 12

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Telecommunication Products

1992
Data Book

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Fujitsu Microelectronics, Inc.
San Jose, California, U.S.A.

Fujitsu Mikroelektronik GmbH
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Singapore

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Circuit diagrams using Fujitsu products are included to illustrate typical semiconductor applications. Information sufficient for construction purposes may not be shown.

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PREFACE

This data book contains the latest product information for Fujitsu's line of Telecommunications Products. This year's edition includes Piezoelectric Devices and IC Compandors, as well as sustaining products from the previous edition. Please note that the contents of this edition have been reorganized to better categorize products for your ease of use.

In addition to the collection of data sheets, you will find valuable information on ordering and expanded packaging descriptions, both in the *Order Information* section. One appendix, *Design Information*, is included as a guideline for selecting and designing Fujitsu prescalers and phase-locked loops for VHF and UHF frequency synthesis.

If you are interested in obtaining other Fujitsu product information, see the publication listing on the following pages for titles and brief descriptions of other Fujitsu product literature. To obtain a copy of any of the documents, contact one of our sales offices.

FUJITSU PRODUCT PUBLICATIONS

The following is a list of the product publications available from Fujitsu Microelectronics, Inc. Call your nearest FMI Sales Office or Sales Representative to order any document(s) you need. (See the Sales Information section for phone numbers.)

STANDARD PRODUCTS

Dynamic RAM Products Data Book	Contains product data sheets for NMOS and CMOS DRAMs, including 1M and 4M devices, and MOS application-specific RAMs.
Static RAM Products Data Book	Contains product data sheets for high-speed CMOS and BiCMOS SRAMs, low-power CMOS SRAMs and application-specific SRAMs.
ECL RAM Products Data Book	Contains product data sheets for ECL and TTL bipolar ECL RAMs, BiCMOS ECL RAMs, and application-specific RAMS including self-timed RAMs (STRAMs).
Programmable Memory Products Data Book	Contains product data sheets for programmable ROMs (including registered and wide-temperature range PROMs); CMOS mask-programmable ROMS, OTP ROMs, erasable PROMs, and EEPROMs; NMOS erasable PROMs and non-volatile RAMs.
Memory Card Products Data Book	Contains product data sheets and programming information for 68-pin JEIDA and PCMCIA standard memory cards and connectors and for 38-pin memory cards.
Power Transistor Products Data Book	Contains product data sheets for RETs, Darlington arrays, and FETs.
Linear Products Data Book	Contains product data sheets for audio products, power supply controls, motor drivers, disk drivers, and converters (A/D, D/A, A/D-D/A, and F/V), and other linear products.
Linear Products Selector Guide	Presents an overview of linear products.
Telecommunication Products Data Book	Contains product data sheets for prescalers and VCOs, PLLs, single-chip PLLs and Prescalers, CODECs, telephone ICs, and cellular telephone ICs, cordless telephone ICs, and piezoelectric devices.
Telecommunication Devices Selector Guide	Presents an overview of telecommunication products and piezoelectric devices.
Interface and Logic Products Selector Guide	Presents an overview of logic and interface devices.
CMOS 4-bit Microcontrollers Data Book, Vol. I	Contains product information, including the development tool for the MB8850 and MB88200 families of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Data Book, Vol. II	Contains product information, including the development tool for the MB88500 family of 4-bit microcontrollers.
CMOS 4-bit Microcontrollers Selector Guide	Presents an overview of the MB88500 (high end), MB8850 (mid-range), and MB88200 (low end) families of 4-bit microcontrollers.
Master Product Guide	Presents an overview of the entire range of products offered by the Integrated Circuits Division: Standard and ASIC products.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC PRODUCTS

CMOS Channeled Gate Arrays Data Book and Design Evaluation Guide	Contains product information for UHB Series High Drive CMOS Gate Arrays and CG10 Series High Drive CMOS Gate Arrays.
CMOS Channelless Gate Arrays Data Book and Design Evaluation Guide	Contains product information for AU Series CMOS Series Gate Arrays and CG21 Series CMOS Gate Arrays.
ASIC Products Selector Guide	Presents an overview of CMOS, BiCMOS, ECL, and GaAs gate arrays and CMOS standard cell products.
BiCMOS Gate Arrays Data Book and Design Evaluation Guide	Contains product information for BC Series BiCMOS Gate Arrays and BC-H Series BiCMOS Gate Arrays.
ECL Gate Arrays Data Book and Design Evaluation Guide	Contains product information for ET Series ECL Gate Arrays, H Series ECL Gate Arrays, Ultra-High Performance ECL Gate Arrays, and VH Series ECL Gate Arrays.

ASIC SOFTWARE

The ASIC Gallery™ (catalog)	Discusses the trend in ASICs: migration from using gates as primitives to using LSI and even VLSI macros as design elements.
The ASIC Design Environment (catalog)	Provides an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD™, BankCAD™, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.
ViewCAD User's Guide	Provides a basic understanding of Fujitsu's proprietary CAD/CAE system, ViewCAD. This book provides information necessary to design, test, simulate, and analyze circuits using Fujitsu's unit cell libraries for AU, UHB, CG10, CG21, and CG31 CMOS technologies.
ViewCAD Installation Guide	Explains how to install Fujitsu's proprietary CAD/CAE system, ViewCAD.
CMOS ASIC Reference Manual for Valid	Provides a basic understanding of the Valid System on the Sun platform as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries for AU and UHB CMOS technologies.
FAME User's Guide	Provides a basic understanding of the Fujitsu ASIC Management Environment (FAME) software as it interfaces with third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
FAME Reference Manual	Provides installation and directory information for the Fujitsu ASIC Management Environment (FAME) software, which uses third-party tools (Sun or PC) to build circuits using Fujitsu's unit cell libraries.
Synopsys User's Guide	Provides a basic understanding of the Synopsys® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.

FUJITSU PRODUCT PUBLICATIONS (Continued)

ASIC SOFTWARE (Continued)

Verilog-XL User's Guide	Provides a basic understanding of the Verilog-XL® system as it interfaces with Fujitsu programs to build circuits using Fujitsu's unit cell libraries.

Future Publications

For Memory Products:

Hybrid Products (1992)	Presents Fujitsu's hybrid products and discusses thick- and thin-film capabilities.

For ASIC Software:

ASIC Design Environment Data Book (1992)	Provides detailed information about the ASIC Design Methodology at Fujitsu. It contains an overview of the third-party tools that work in concert with Fujitsu's proprietary tools, ViewCAD, BankCAD, and FAME. Also included are product profiles explaining how the third-party tools fit within the design framework.

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Contents and Alphanumeric Product List

Fujitsu's Telecommunication Products

Introduction vii

Section 1 – Prescalers — *At a Glance* 1–1

MB467	200 MHz Low Power High Frequency Prescaler	1–3
MB501/L	1.0/1.1 GHz Two Modulus Prescaler	1–11
503	200 MHz Two Modulus Prescaler	1–11
504/L	520 MHz Two Modulus Prescaler	1–11
MB501LV	1.1 GHz Low Voltage/Low Power Two Modulus Prescaler	1–23
MB504LV	520 GHz Low Voltage/Low Power Two Modulus Prescaler	1–23
MB501SL	1.1 GHz Super Low Power Two Modulus Prescaler	1–33
MB505–16	1.6 GHz Ultra-high Frequency Prescaler	1–43
MB506	2.4 GHz Ultra-high Frequency Prescaler	1–47
MB507	1.6 GHz Two Modulus Prescaler	1–51
MB508	2.3 GHz Two Modulus Prescaler	1–59
MB509	1.1 GHz Two Modulus Prescaler with Stand-by Mode	1–67
MB510	2.7 GHz Two Modulus Prescaler	1–75
MB511	1.0 GHz High-speed Prescaler	1–83

Section 2 – Phase-Locked Loops (PLLs) — *At a Glance* 2–1

MB87001A	13 MHz CMOS Serial Input PLL Frequency Synthesizer	2–3
MB87006A	17 MHz CMOS Serial Input PLL Frequency Synthesizer	2–15
MB87014A	CMOS Serial Input PLL Frequency Synthesizer with 180 MHz Prescaler	2–27
MB87076	13 MHz CMOS Serial Input PLL Frequency Synthesizer With Power Down Mode	2–37
MB87086A	15 MHz CMOS Serial Input PLL Frequency Synthesizer	2–51
MB87087	17 MHz CMOS Serial Input PLL Frequency Synthesizer	2–61
MB87090	13 MHz CMOS Serial Input PLL Frequency Synthesizer with Constant Current Output Charge Pump	2–73

Section 3 – Single-Chip PLLs/Prescalers — *At a Glance* 3–1

MB1501	Serial Input PLL Frequency Synthesizer with 1.1 GHz Prescaler	3–3
1501H		
1501L		
MB1502	Low Power Serial Input PLL Synthesizer with 1.1 GHz Prescaler	3–21
MB1503	Serial Input PLL Frequency Synthesizer with 1.1 GHz Prescaler	3–35
MB1504	Serial Input PLL Frequency Synthesizer with 520 MHz Prescaler	3–49
1504H		
1504L		
MB1505	Serial Input PLL Frequency Synthesizer with 600 MHz Prescaler	3–67
MB1507	Low Power Serial Input PLL Frequency Synthesizer with 2.0 GHz Prescaler	3–79

Contents and Alphanumeric Product List (Continued)

MB1508	Serial Input PLL Frequency Synthesizer with 2.5 GHz Prescaler	3–91
MB1509	Dual Serial Input PLL Frequency Synthesizer with 400 MHz Prescaler	3–101
MB1511	Low Power and Low Voltage Serial Input PLL Frequency Synthesizer with 1.1 GHz Prescaler	3–115
MB1512	Low Power Serial Input PLL Frequency Synthesizer with 1.1 GHz Prescaler	3–127
MB1513	Serial Input PLL Frequency Synthesizer with 1.1 GHz Prescaler	3–139
MB1518	Serial Input PLL Frequency Synthesizer with 2.5 GHz Prescaler	3–153
MB1519	Dual Serial Input PLL Frequency Synthesizer with 600 MHz Prescaler	3–161

Section 4 – Single-Chip VCOs/Prescalers — *At a Glance* 4–1

MB551	1 GHz Dual Modulus Prescaler with VCO Circuit	4–3

Section 5 – Piezoelectric Devices — *At a Glance* 5–1

F5CB Series	SAW-Bandpass Filter Devices	5–3
M2 Series	Piezoelectric Devices (D100) with VCO	5–17
M2 Series	Piezoelectric Devices (D300) with VCO	5–25
M3 Series	Piezoelectric Devices (D001) with VCO	5–35
M3 Series	Piezoelectric Devices (D101) with VCO	5–39

Section 6 – Cordless Telephone Integrated Circuits — *At a Glance* 6–1

MB86460A	Modem with Internal Voice-Band Filters	6–3
MB87002	CMOS 1200 bps Minimum Shift Keying Modem	6–25

Section 7 – Telephone Integrated Circuits — *At a Glance* 7–1

MB3120	Compandor IC	7–3
MB3121	Compandor IC	7–15
MB4513	Telephone Amplifier/Tone Ringer	7–19
MB4518	Telecommunication Circuit	7–31
MB4752A	Subscriber Line Interface IC	7–47
MB87007A 87008A	Dual Tone Multifrequency Pulse Dialer	7–57
MB87009	Dual Tone Multifrequency Pulse Dialer	7–83
MB87017B	Dual Tone Multifrequency Receiver	7–111
MB87029	Dual Tone Multifrequency Pulse Dialer	7–123
MB87057	Dual Tone Multifrequency Receiver	7–149

Section 8 – Coders/Decoders (CODECs) — *At a Glance* 8–1

MB6021A 6022A	μ-law and A-law Single-chip CODEC with Filters	8–3

Contents and Alphanumeric Product List (Continued)

Section 9 – Quality and Reliability — *At a Glance* 9–1
Quality Control at Fujitsu 9–3
Quality Control Processes at Fujitsu 9–4

Section 10 – Ordering Information — *At a Glance* 10–1
IC Packages, Inserted Types 10–3
IC Packages, Surface Mounted Types 10–4
Part Number System 10–6

Section 11 – Sales Information — *At a Glance* 11–1
Fujitsu Worldwide Locations
Fujitsu Limited (Japan) 11–3
Fujitsu Microelectronics, Inc. (U.S.A.) 11–4
Fujitsu Electronic Devices Europe: 11–6
Fujitsu Mikroelektronik GmbH (West Germany)
Fujitsu Microelectronics, Limited. (U.K.)
Fujitsu Microelectronics, Italia S.R.L. (Italy)
Fujitsu Microelectronics, Ireland, Ltd. (Ireland)
Fujitsu Microelectronics Asia PTE Ltd. (Singapore) 11–8
Integrated Circuits Corporate Headquarters – Worldwide 11–9
FMI Sales Offices for North and South America 11–10
FMI Representatives – USA 11–11
FMI Representatives – Canada 11–14
FMI Representatives – Mexico 11–14
FMI Representatives – Puerto Rico 11–14
FMI Distributors – USA 11–15
FMI Distributors – Canada 11–17
FMG, FML, FMIL Sales Offices for Europe 11–18
FMG, FML, FMIL Distributors – Europe 11–19
FMAP Sales Offices for Asia, Australia and Oceania 11–20
FMAP Representatives – Asia and Australia 11–21
FMAP Distributors – Asia 11–21

Section 12 – Appendix – Design Information
Application Note: Prescalers and PLLs 12–1

Contents and Alphanumeric Product List

Telecommunications Products

Alphanumeric List of Fujitsu Part Numbers

Device	*Page*
F5 Series	5–3
M2 Series (D100)	5–17
M2 Series (D300)	5–25
M3 Series (D001)	5–35
M3 Series (D101)	5–39
MB467	1–3
MB501	1–11
MB501L	1–11
MB501LV	1–23
MB501SL	1–33
MB503	1–11
MB504	1–11
MB504L	1–11
MB506	1–47
MB507	1–51
MB508	1–59
MB509	1–67
MB510	1–75
MB511	1–83
MB551	4–3
MB1501	3–3
MB1501H	3–3
MB1501L	3–3
MB1502	3–21
MB1503	3–35
MB1504	3–49
MB1504H	3–49
MB1504L	3–49
MB1505	3–67
MB1507	3–79
MB1508	3–91
MB1509	3–101
MB1511	3–115
MB1512	3–127
MB1513	3–139
MB1518	3–153
MB1519	3–163
MB3120	7–3
MB3121	7–15
MB4513	7–19
MB4518	7–31
MB4752A	7–47
MB6021A	8–3
MB6022A	8–3
MB86460A	6–3
MB87001A	2–3
MB87002	6–25
MB87006A	2–15
MB87007A	7–57
MB87008A	7–57
MB87009	7–83
MB87014A	2–27
MB87017B	7–111
MB87029	7–123
MB87057	7–149
MB87076	2–37
MB87086A	2–51
MB87087	2–61
MB87090	2–73

Introduction

Page	Title
xiii	Fujitsu's Telecommunication Products

Fujitsu's Telecommunication Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs.

The telecommunication product line offers devices for use in a wide range of applications. These telecommunication products are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

Prescalers

Fujitsu offers a wide range of prescaler devices capable of satisfying the technical requirements of today's applications. Features such as the 200 MHz to 2.7 GHz frequency range, low power consumption, and a multitude of divide ratios are some of the advantages of Fujitsu's prescaler family.

Phase-Locked Loops (PLLs)

The Fujitsu family of PLLs offers a wide range of operating frequencies with low supply currents and voltages to meet design needs. The serial input capability of these devices is an outstanding feature of Fujitsu's PLLs.

Single-Chip PLLs/Prescalers

Fujitsu is one of only a few semiconductor manufacturers to offer single-chip PLL/Prescaler devices. Fujitsu is the only manufacturer with a BiCMOS version that combines high speed and low power consumption in a single chip. With the increasing emphasis on board space reduction (to improve cost), reliability, and overall product size, these single-chip devices provide solutions for designers.

Single-Chip VCOs/Prescalers

Fujitsu is the only semiconductor manufacturer with a single-chip VCO/Prescaler family of products. With the increasing emphasis on overall product size reduction and added on-chip functionality, this new family of devices provides the needed design solution.

Continued on next page

Fujitsu's Telecommunication Devices

Piezoelectric Devices

Fujitsu's lithium tantalate peizoelectric bandpass SAW filters provide sharp roll-off characteristics and excellent stability over temperature in a tiny 5 mm x 5 mm surface mount package. Standard frequencies are available for AMPS, NTACS, NMT, and ETACS transmit and receive frequencies. This family of devices also includes a series of voltage controlled oscillators.

Cordless Telephone Integrated Circuits

Fujitsu's family of cordless telephone ICs offers low power consumption, ideal for application of this type. This family of products consists of minimum-shift keying modems for data transfer applications.

Telephone Integrated Circuits

Fujitsu offers a complete family of telephone ICs as an application-specific product line. These devices are capable of performing advanced telephone functions such as SLIC, speech transmission/reception, DTMF, on-hook dialing, last number repeat, tone amplification, and companding functions.

Coder/Decoders (CODECs)

The Fujitsu family of CODECs consists of the MB6020 series. All devices conform to CCITT and AT&T specifications.

Prescalers — *At a Glance*

Page	Device	Maximum Frequency	Supply I_{CC}	Supply V_{CC}	Divide Ratio	Package Options		
1–3	MB467	200 MHz	6 mA	5 V	10/20	8-pin	Plastic	DIP, FPT
1–11	MB501	1.0 GHz	30 mA	5 V	64/65, 128/129	8-pin	Plastic	DIP, FPT
	501L	1.1 GHz	10 mA	5 V	64/65, 128/129			
	503	200 MHz	8 mA	5 V	16/17, 32/33			
	504	520 MHz	10 mA	5 V	32/33, 64/65,			
	504L	520 MHz	5 mA	5 V	32/33, 64/65			
1–23	MB501LV	1.1 GHz	12 mA	3 V	64/65, 128/129	8-pin	Plastic	DIP, FPT
	504LV	520 MHz	6 mA	3 V	32/33, 64/65			
1–33	MB501SL	1.1 GHz	5 mA	5 V	64/65, 128/129	8-pin	Plastic	DIP, FPT
1–43	MB505–16	1.6 GHz	9 mA	5 V	128/256	8-pin	Plastic	DIP, FPT
1–47	MB506	2.4 GHz	18 mA	5 V	64/128/256	8-pin	Plastic	DIP, FPT
1–51	MB507	1.6 GHz	18 mA	5 V	128/129, 256/257	8-pin	Plastic	DIP, FPT
1–59	MB508	2.3 GHz	24 mA	5 V	128/130, 256/258, 512/514	8-pin	Plastic	DIP, FPT
1–67	MB509	1.1 GHz	11.6 mA	5 V	64/65, 128/129	8-pin	Plastic	DIP, FPT
1–75	MB510	2.7 GHz	10 mA	5 V	128/144, 256/272	8-pin	Plastic	FPT
1–83	MB511	1.0 GHz	23 mA	5 V	1, 2, 8	8-pin	Plastic	DIP, FPT

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FUJITSU

DATA SHEET

1

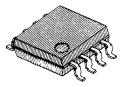
MB467
LOW POWER PRESCALER

200MHz, LOW POWER PRESCALER

The Fujitsu MB467 is a prescaler, which is used in Phase Locked Loop (PLL) frequency synthesizer. The MB467 will divide by 10 when SW pin is high (Vcc level) and by 20 when SW pin is low (open or 1/2Vcc level). The output is an open collector output to drive TTL or CMOS logic circuit.

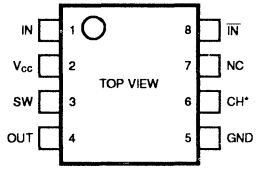
- Operating Frequency: 200MHz max.
- Low Power Comsumption: 30mW typ.
- Low Level Input Voltage: $V_{IN} \geq 150mV_{P-P}$
- Wide Operation Temperature: T_A=–30°C to +85°C
- Power Supply Voltage: V_{CC}=+5V±10%
- Interface
  Input: Capacitor coupling due to internal biased input
  Output: Open collector output
- Plastic 8–pin Standard Dual–In–Line Package: (Suffix: –P)
- Plastic 8–pin Standard Flat Package: (Suffix: –PF)

PLASTIC PACKAGE
DIP–08P–M01



PLASTIC PACKAGE
FPT–08P–M01

PIN ASSIGNMENT



Note: *It should be open.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_o	0 to +5	mA
Junction Temperature	T_j	+125	°C
Storage Temperature	T_{STG}	–55 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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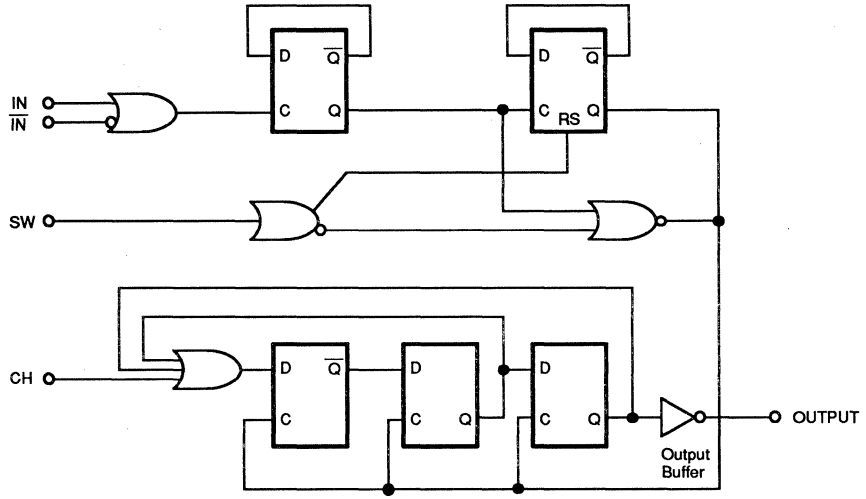
1

BLOCK DIAGRAM



SW	Divide Ratio
H	1/10
L	1/20
Open	1/20

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage Input
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	CH	Check Input For Outgoing Test. It should be open.
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	–30		+85	°C
Load Capacitance	C_L			7	pF

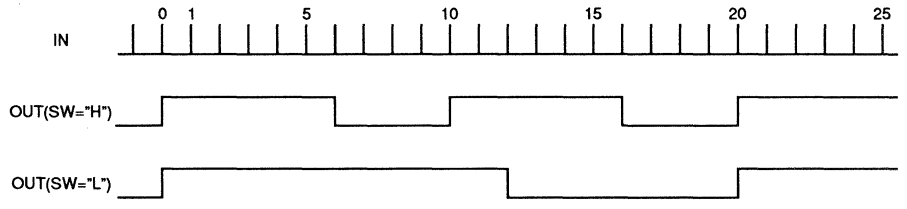
ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, T_A=–30 to +85°C)

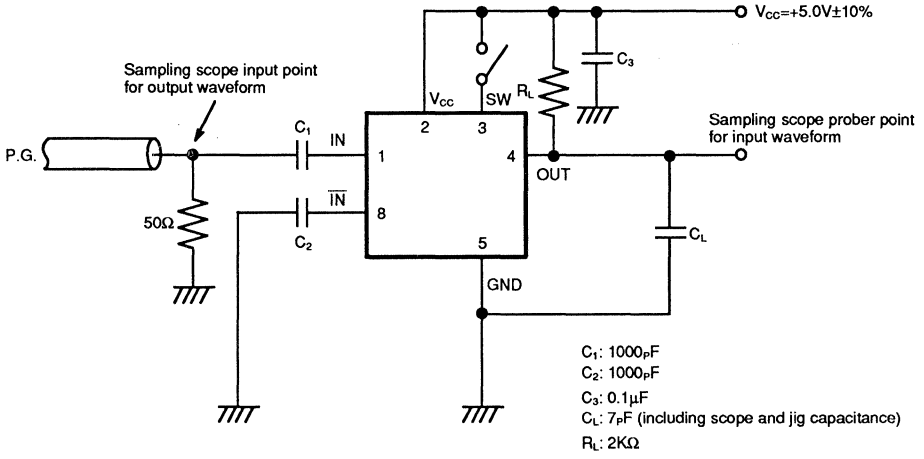
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}	V_{CC}=5.0V, T_A=25°C		6	10	mA
High–level Output Voltage	V_{OH}	With 2kΩ pull–up resistor to V_{CC}	4.0			V
Low–level Output Voltage	V_{OL}	With 2kΩ pull–up resistor to V_{CC}			0.4	V
Input Frequency	f_{IN}	V_{IN}: 150mV_{P-P} sine wave	10		200	MH_z
Input Signal Amplitude for IN	V_{IN}		150		2000	mV_{P-P}

1

TIMING CHART



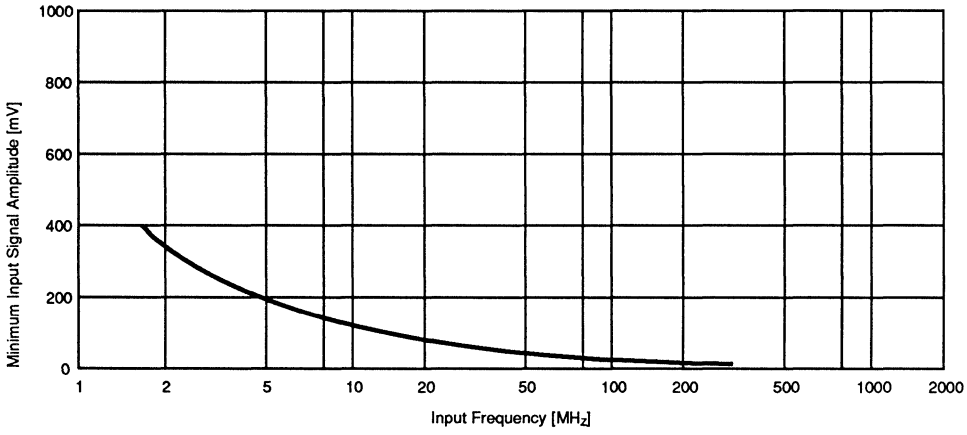
TEST CIRICUIT



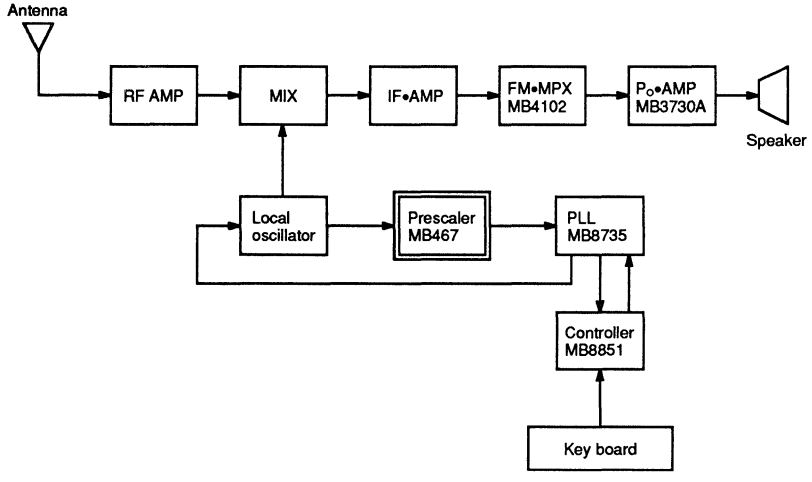
Note: Input frequency has a influence of input signal amplitude, input signal slew rate, and input coupling capacitor value.
The MB467 can operate down to DC when large value of above parameters are selected.
The MB467 starts self-oscillation unless signal is input.
When a double drive, please connect either of input pins to GND by a 39 kohms pull down resistor. The oscillation is prevented easily.
When a single drive, please connect a pull down resistor to unused pin.

TYPICAL CHARACTERISTICS CURVE

INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY



APPLICATION EXAMPLE



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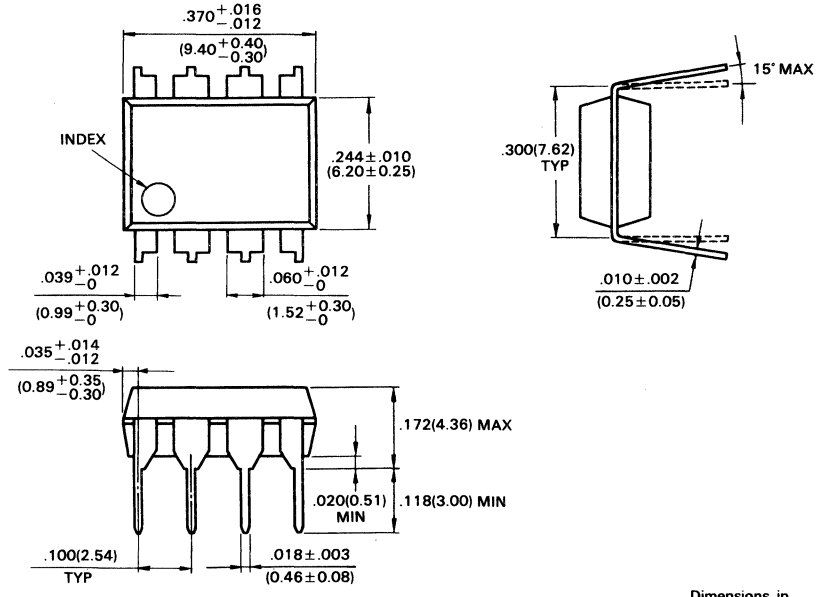
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No. : DIP-08P-M01)



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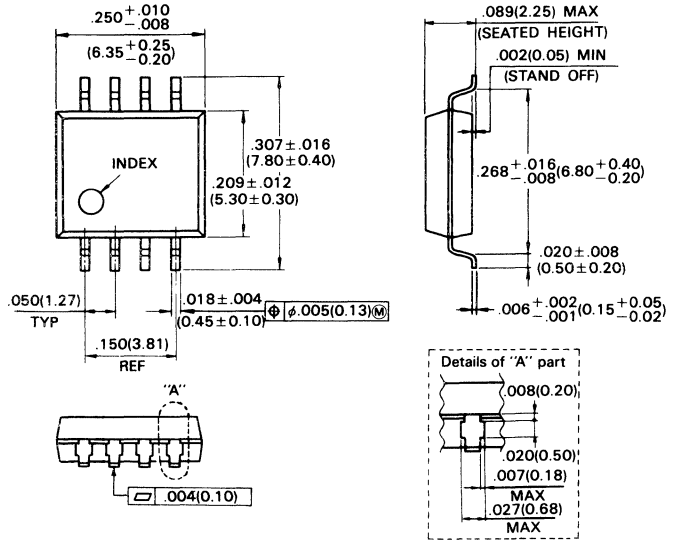
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: –PF)

8–LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT–08P–M01)



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Dimensions in
inches (millimeters)

1

April 1990
Edition 6.0

FUJITSU

DATA SHEET

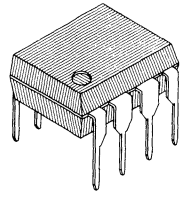
1

MB501/501L/503/504/504L
TWO MODULUS PRESCALERS

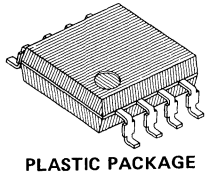
TWO MODULUS PRESCALERS

The Fujitsu MB 501/503/504 are two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 64/65 or 128/129, 16/17 or 32/33, and 32/33 or 64/65 respectively. MB 501L/MB 504L is the low-power version of MB 501/MB 504; it will perform exactly the same function as MB 501/MB 504 but with much lower power dissipation.

The output is 1.6 V peak to peak on ECL level.



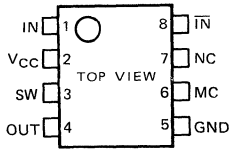
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

- High Operating Frequency, Low Power Operation.
  - 1.0 GHz at 150 mW typ. (MB 501)
  - 1.1 GHz at 50 mW typ. (MB 501L)
  - 200 MHz at 40 mW typ. (MB 503)
  - 520 MHz at 50 mW typ. (MB 504)
  - 520 MHz at 25 mW typ. (MB 504L)
- Pulse Swallow Function
- Wide Operation Temperature T_A = -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

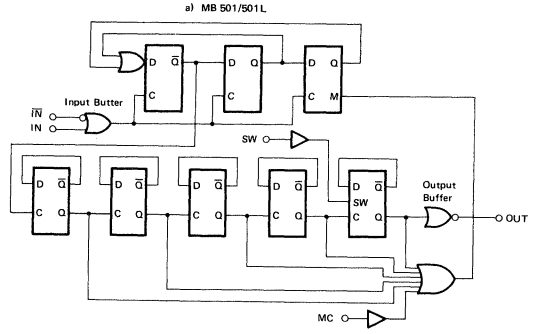
Rating		Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	V_0	10	mA
Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to + 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAMS

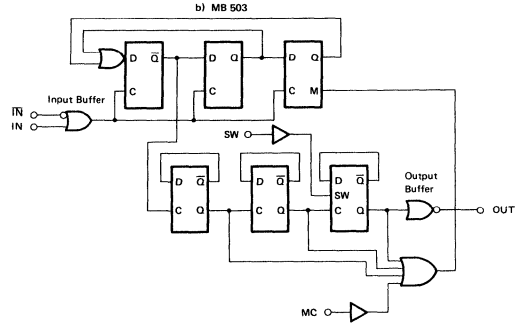
a) MB 501/501L



	SW	MC	Divide Ratio
MB 501/ MB 501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

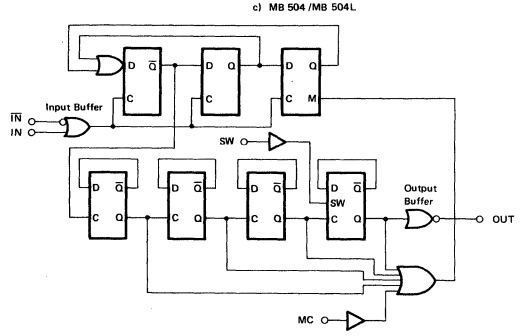
b) MB 503



	SW	MC	Divide Ratio
MB 503	H	H	1/16
	H	L	1/17
	L	H	1/32
	L	L	1/33

Note: SW : H = V_{CC}, L = open
MC : H = 2.0 V to V_{CC},
L = GND to 0.8 V

c) MB 504 /MB 504L



	SW	MC	Divide Ratio
MB 504/ MB 504L	H	H	1/32
	H	L	1/33
	L	H	1/64
	L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	−40		+85	°C
Load Capacitance	C_L			12	pF

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

1

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power Supply Current	MB501	I_{CC}	I/O pins are open		30	42*	mA
	MB501L				10	14*	mA
	MB503				8	12*	mA
	MB504				10	14*	mA
	MB504L				5	7*	mA
Output Amplitude		V_O		1.0	1.6		V_{P-P}
Input Frequency	MB501	f_{IN}	With input coupling capacitor 1000pF	10		1000	MHz
	MB501L			10		1100	MHz
	MB503			10		200	MHz
	MB504			10		520	MHz
	MB504L			10		520	MHz
Input Signal Amplitude for IN	MB501	V_{IN}		-4		5.5	dBm
	MB501L			-4		5.5	dBm
	MB503			-12		10	dBm
	MB504			-12		10	dBm
	MB504L			-12		10	dBm
High Level Input Voltage for MC		V_{IHM}		2.0			V
Low Level Input Voltage for MC		V_{ILM}				0.8	V
High Level Input Voltage for SW		V_{IHS}**		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW		V_{ILS}		Open			V
High Level Input Current for MC		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC		I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	MB501	t_{SET}			18	28	ns
	MB501L				16	26	ns
	MB503				38	46	ns
	MB504				20	30	ns
	MB504L				18	28	ns

NOTE: * V_{CC} = 5V, T_A = 25°C
** Design Guarantee

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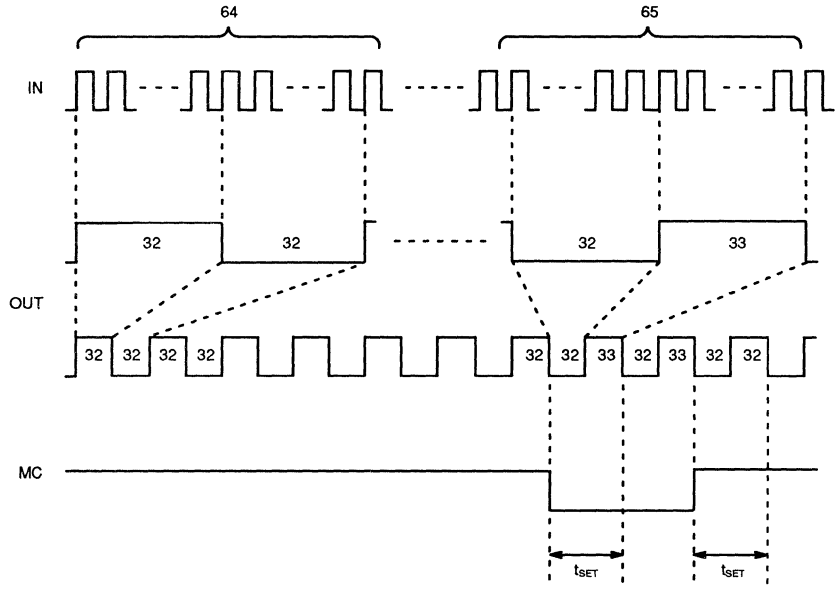
MB501/MB501L TIMING CHART (2 MODULUS)

Example: Divide ratio = 64/65

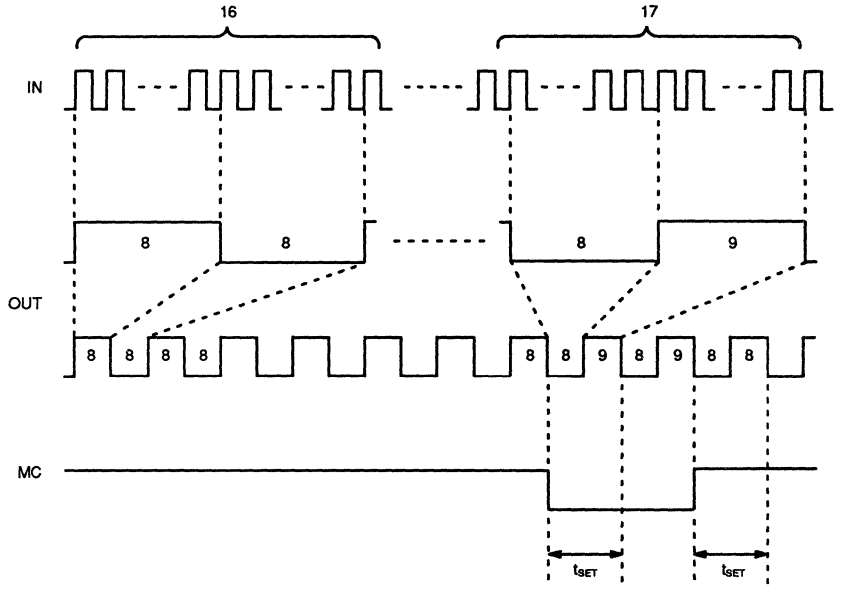


Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 18 ns (MB501), 16 ns (MB501L) from the MC signal input to the timing of change of prescaler divide ratio.

1

MB503 TIMING CHART (2 MODULUS)

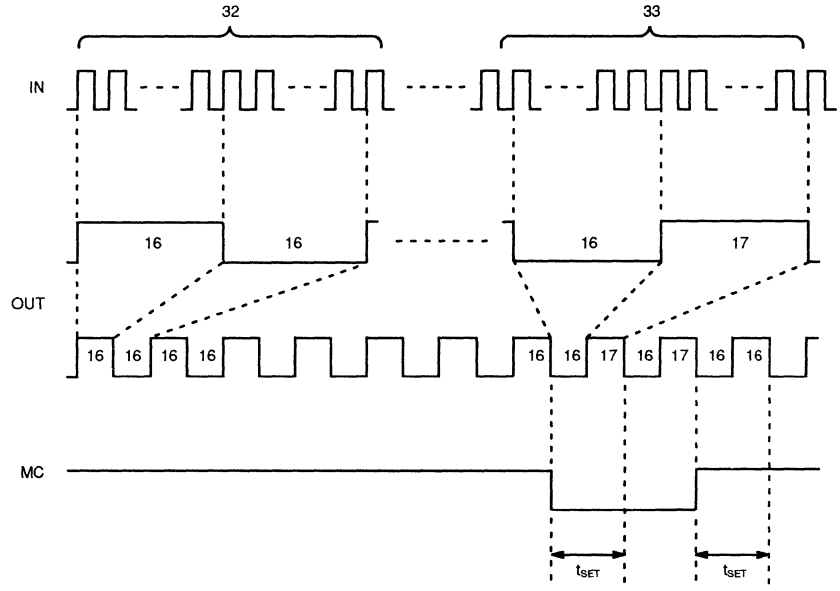
Example: Divide ratio = 16/17



Note: When divide ratio of 17 is selected, positive pulse is applied by one to 9.
The typical set up time is 38 ns from the MC signal input to the timing of change of prescaler divide ratio.

MB504/MB504LV TIMING CHART (2 MODULUS)

Example: Divide ratio = 32/33



Note: When divide ratio of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 20 ns (MB504), 18 ns (MB504L) from the MC signal input to the timing of change of prescaler divide ratio.

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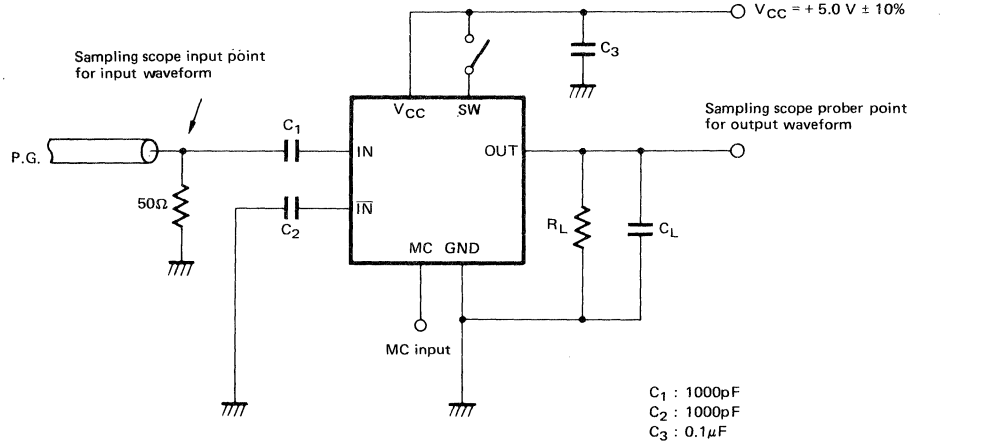
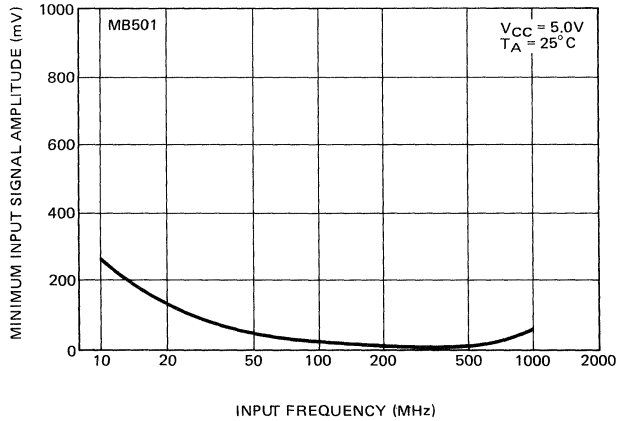
Fig. 2 – TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 4 — INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

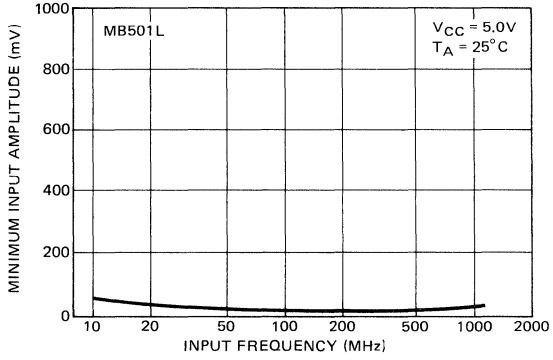


Fig. 5 — INPUT SIGNAL AMLITUDE vs. INPUT FREQUENCY

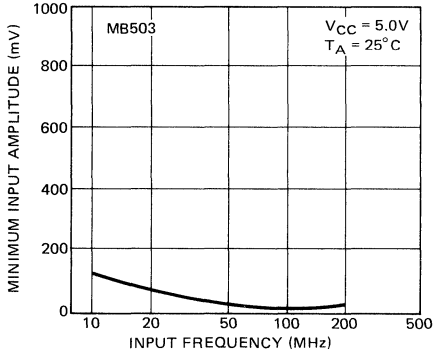
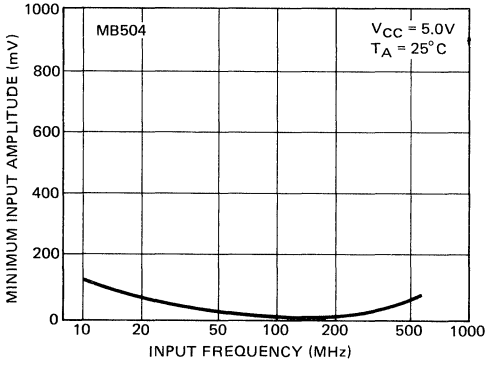


Fig. 6 — INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 7 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

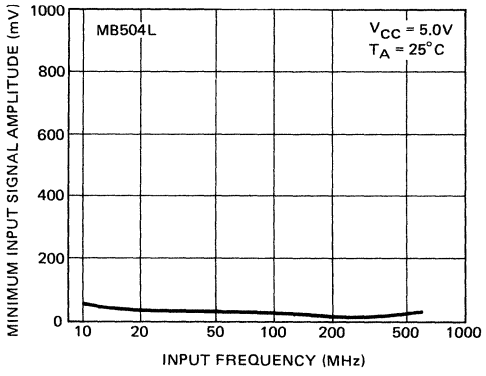
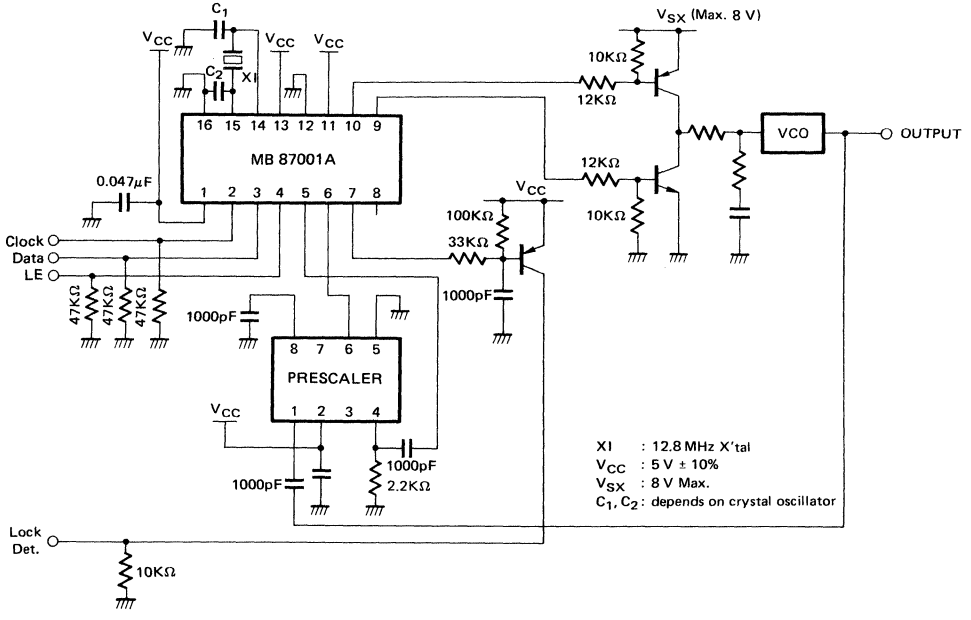


Fig. 8 – TYPICAL APPLICATION EXAMPLE

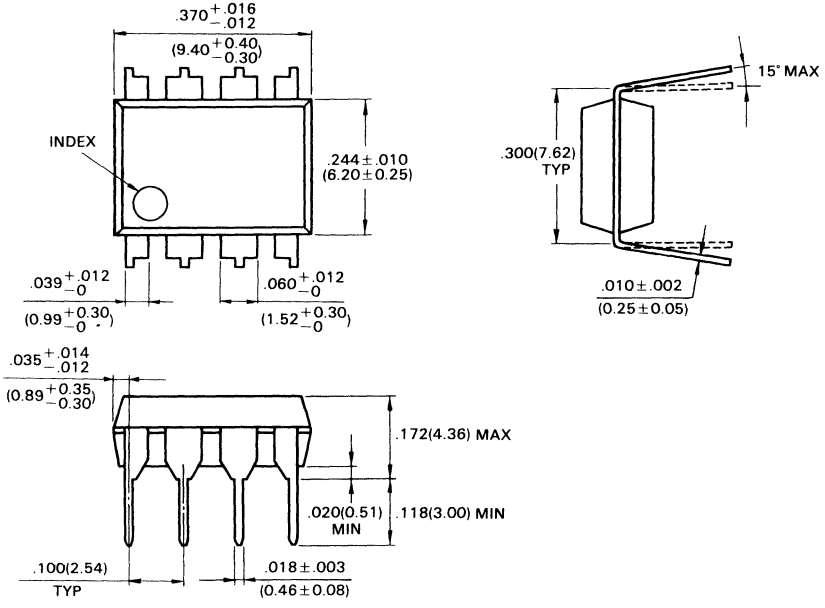


An example of application of MB501/501L/503/504/504L with PLL Synthesizer IC MB87001A

1

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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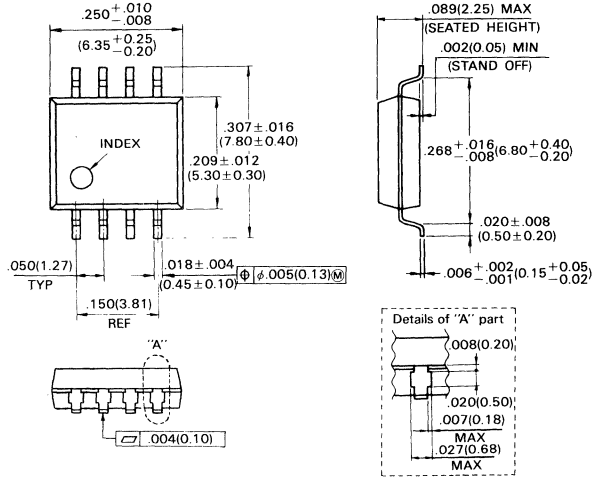
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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Dimensions in
inches (millimeters)

April 1990
Edition 4.0

FUJITSU

DATA SHEET

MB501LV/504LV
LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

1

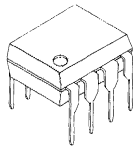
LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

The Fujitsu MB501LV/504LV are low power and low voltage versions of MB501/504 two modulus prescalers used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 64/65 or 128/129, and 32/33 or 64/65 respectively.
The output level is 1.1 V peak to peak on ECL level.

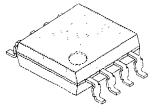
- Wide Low Voltage Operation 3.0 V typ., +2.7 to 4.5 V
- High Frequency Operation, Low Power Operation (V_{IN} = -12dBm min.)

  1.1 GHz at 36 mW typ. (MB 501LV)

  520 MHz at 18 mW typ. (MB 504LV)
- Pulse Swallow Function
- Wide Operation Temperature T_A = -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.1 $V_{p\text{-}p}$ typ.
- Built-in a termination resistor
  Stable output amplitude is obtained up to output load capacitance of 8 pF.
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

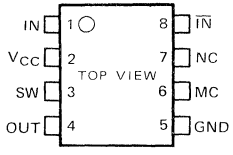


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

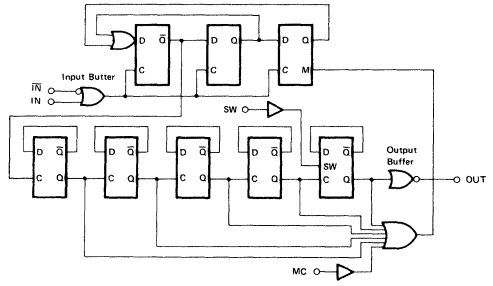
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – BLOCK DIAGRAMS

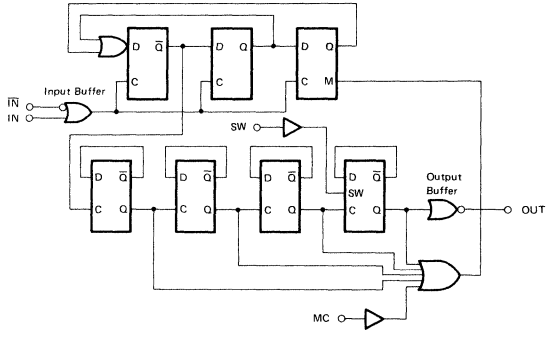
a) MB 501LV



SW	MC	Divide Ratio
H	H	1/64
H	L	1/65
L	H	1/128
L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

b) MB 504LV



SW	MC	Divide Ratio
H	H	1/32
H	L	1/33
L	H	1/64
L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	2.7	3.0	4.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			8	pF

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

1

ELECTRICAL CHARACTERISTICS

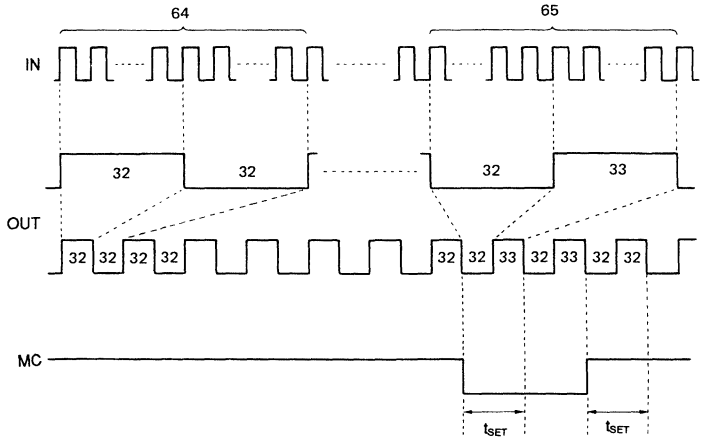
(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power Supply Current	MB501LV	I_{CC}	V_{CC} = 3.0V		12		mA
	MB504LV				6		mA
Output Amplitude		V_O		0.8	1.1		V_{P-P}
Input Frequency	MB501LV	f_{IN}	with input coupling capacitor 1000 pF	10		1100	MHz
	MB504LV			10		520	MHz
Input Signal Amplitude		V_{IN}		-12		5.5	dBm
High Level Input Voltage for MC Input		V_{IHM}	V_{IHM} = ½V_{CC} +0.3	V_{IHM}			V
Low Level Input Voltage for MC Input		V_{ILM}				0.8	V
High Level Input Voltage for SW Input		V_{IHS}*		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW Input		V_{ILS}		OPEN			V
High Level Input Current for MC Input		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input		I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	MB501LV	t_{SET}			16	26	ns
	MB504LV				18	28	ns

Note: *Design Guarantee

MB501LV TIMING CHART (2 MODULUS)

Example: Divide ratio = 64/65



Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

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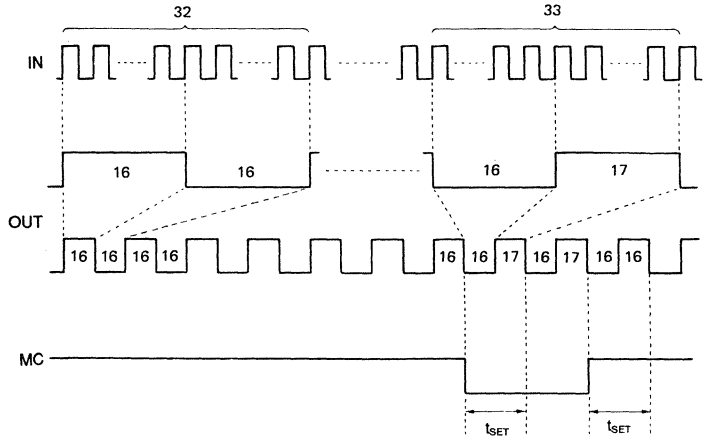
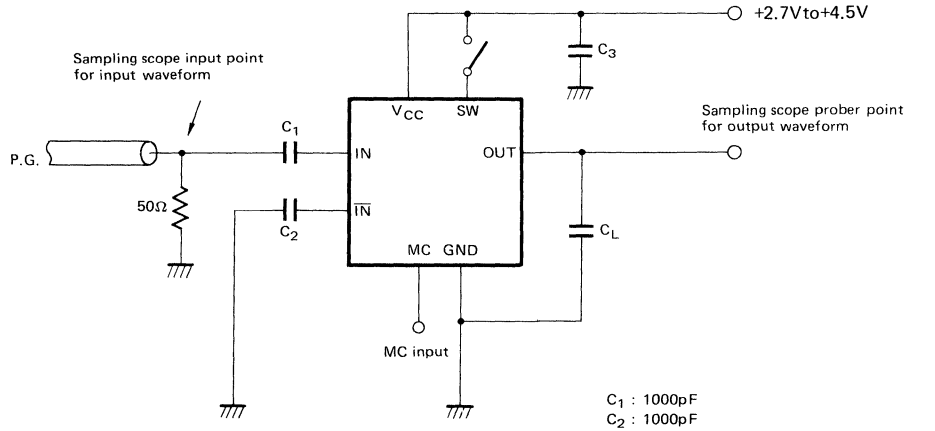
MB504LV TIMING CHART (2 MODULUS)

Example: Divide ratio = 32/33



Note: When divide of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

Fig. 2 – TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

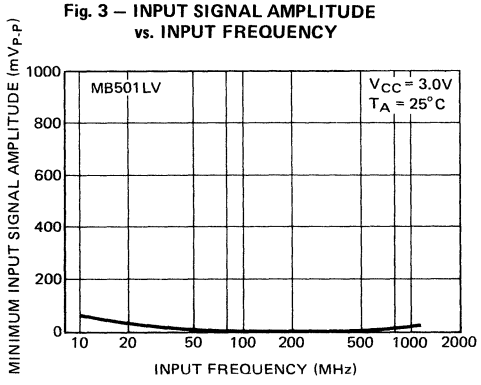


Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

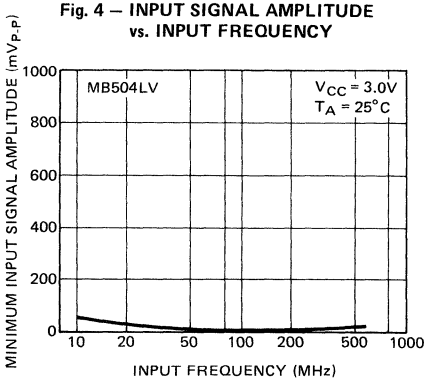


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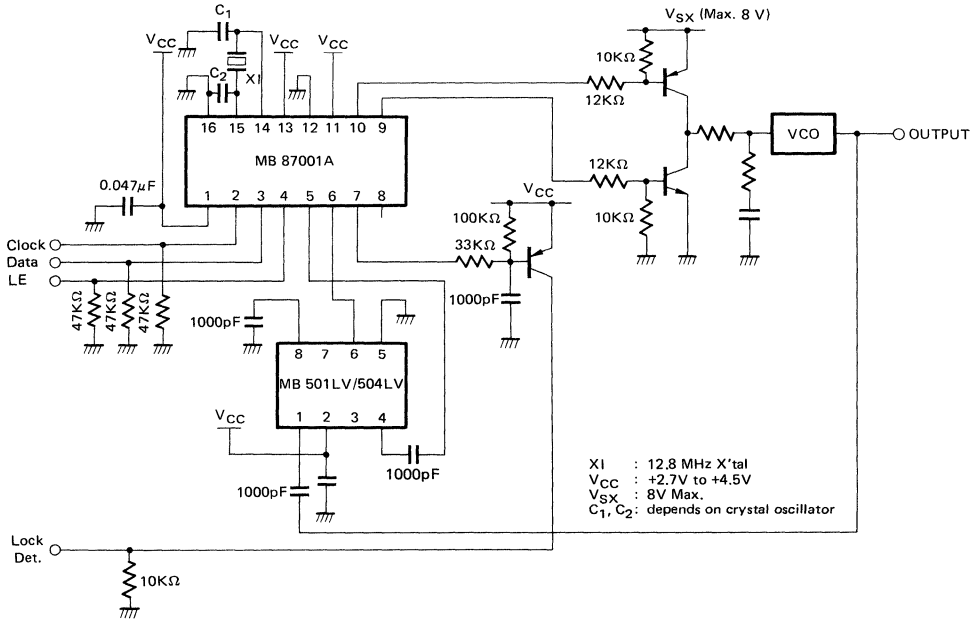
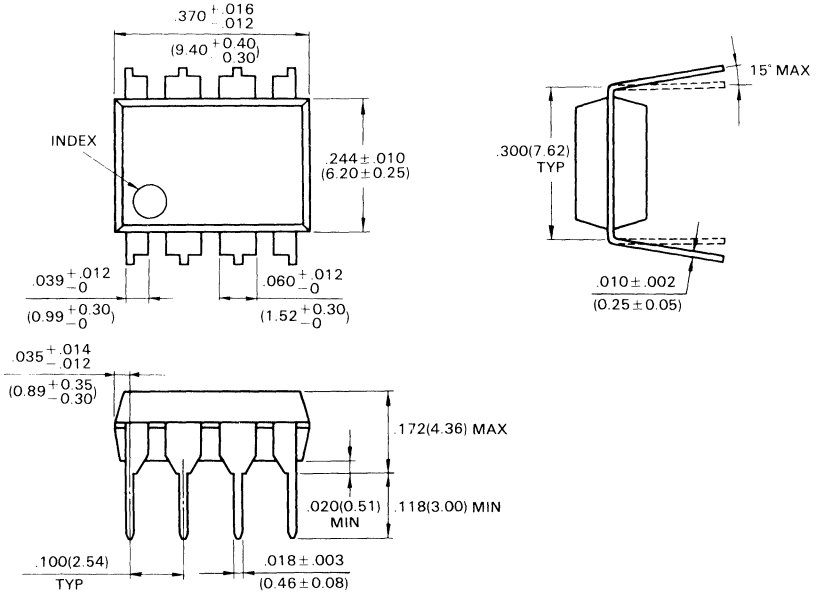
Fig. 5 – TYPICAL APPLICATION EXAMPLE



1

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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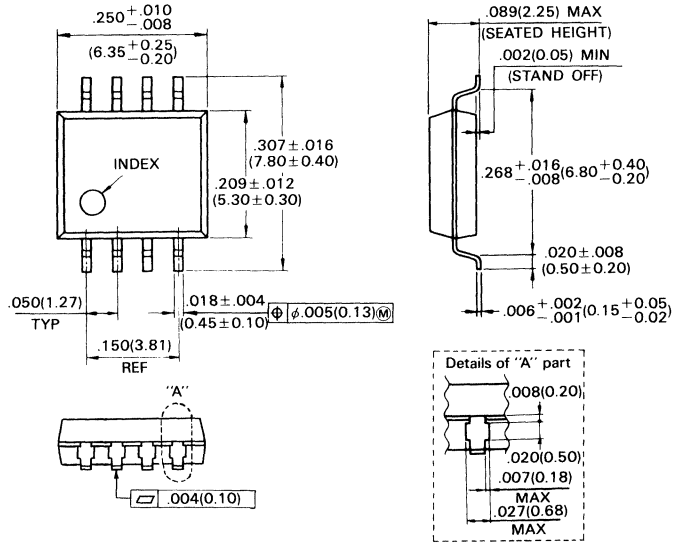
Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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Dimensions in
inches (millimeters)

May 1990
Edition 3.0

FUJITSU

DATA SHEET

1

MB501SL

SUPER LOW POWER TWO MODULUS PRESCALER

SUPER LOW POWER TWO MODULUS PRESCALER

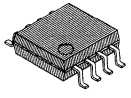
The Fujitsu MB501SL is a super low power version of MB501 two modulus prescaler used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 64/65 or 128/129, respectively. The MB501SL achieves extremely small stay capacitance of internal element, realized through the use of Fujitsu Advanced Process Technology. As the results, high speed operation is achieved with low power supply current of 5 mA typ., about a half current value of MB501L.

- High Frequency Operation fmax = 1.1 GH_Z max. (V_{IN} = −14bBm)
- Pulse Swallow Function: 64/65, 128/129
- Low Power Supply Current: 5.0mA typ.
- Stable Output Amplitude: V_O = 1.6Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Plastic 8-pin Dual-In-Line Package

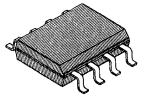
  Plastic 8-pin Mini Flat Package
- Built-in Termination Resistor

  Stable output amplitude is obtained up to output load capacitance of 8 pF.

PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01



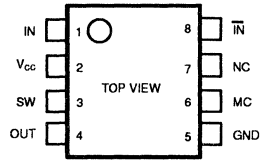
PLASTIC PACKAGE
FPT-08P-M02

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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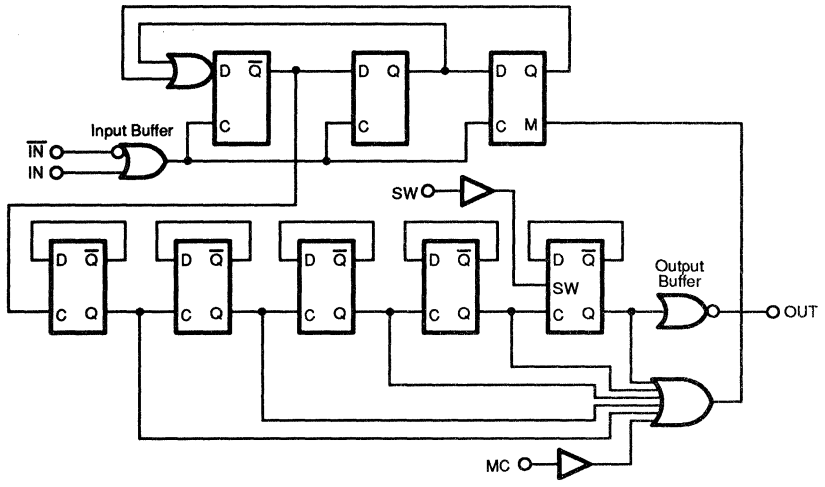
1

Fig. 1 – MB501SL BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB501SL	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	–40	–	+85	°C
Load Capacitance	CL	–	–	8	pF

ELECTRICAL CHARACTERISTICS

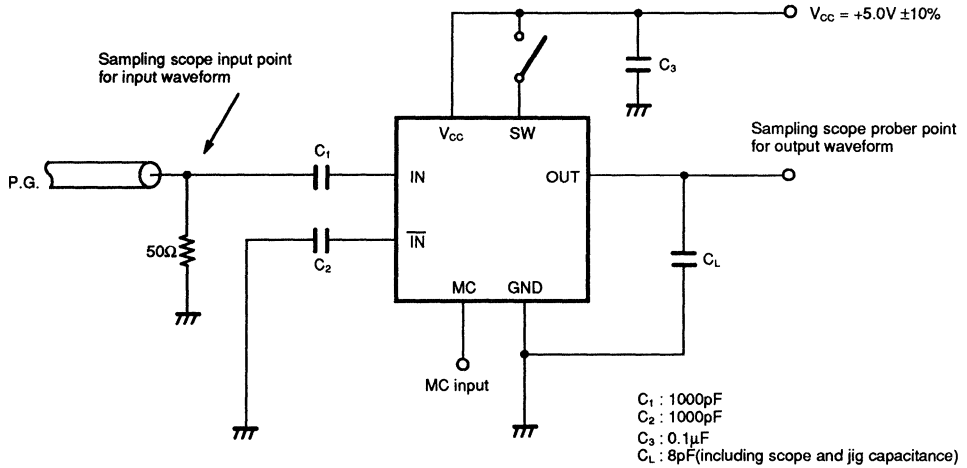
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}	–	–	5.0	7.0	mA
Output Amplitude	V_O	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6	–	V_{P-P}
Input Frequency	fin	With input coupling capacitor 1000pF	10	–	1100	MHz
Input Signal Amplitude	V_{IN}	–	–14	–	0	dBm
High Level Input Voltage for MC	V_{IHM}	–	2.0	–	–	V
Low Level Input Voltage for MC	V_{ILM}	–	–	–	0.8	V
High Level Input Voltage for SW	V_{IHS}*	–	V_{CC} – 0.1	V_{CC}	V_{CC} + 0.1	V
Low Level Input Voltage for SW	V_{ILS}	–	OPEN			V
High Level Input Current for MC	I_{IHM}	V_{IH} = 2.0V	–	–	0.4	mA
Low Level Input Current for MC	I_{ILM}	V_{IL} = 0.8V	–0.2	–	–	mA
Modulus Set-up Time MC to Output	t_{SET}	–	–	16	26	ns

Note: * Design Guarantee

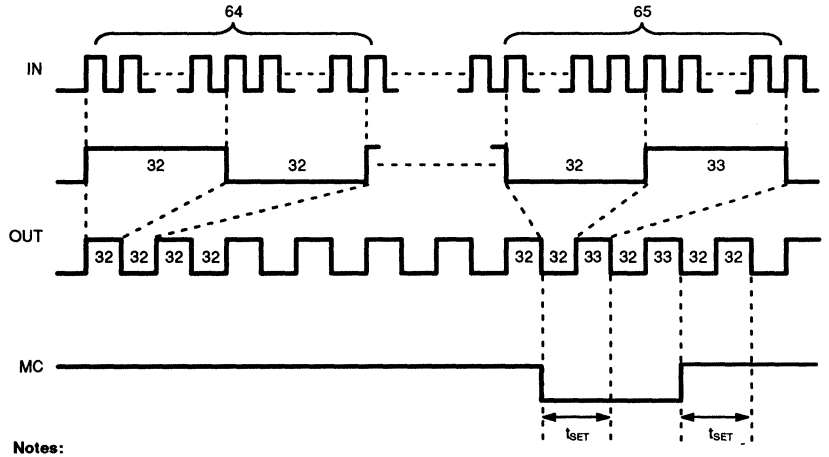
1

Fig. 2 –TEST CIRCUIT



TWO MODULUS OPERATING TIMING CHART

Example. Divide Ratio of 64/65



Notes:
When divide ratio of 129 is selected, positive pulse is added by one to 65.
The typical set up time(t_{SET}) is 16 ns from MC signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

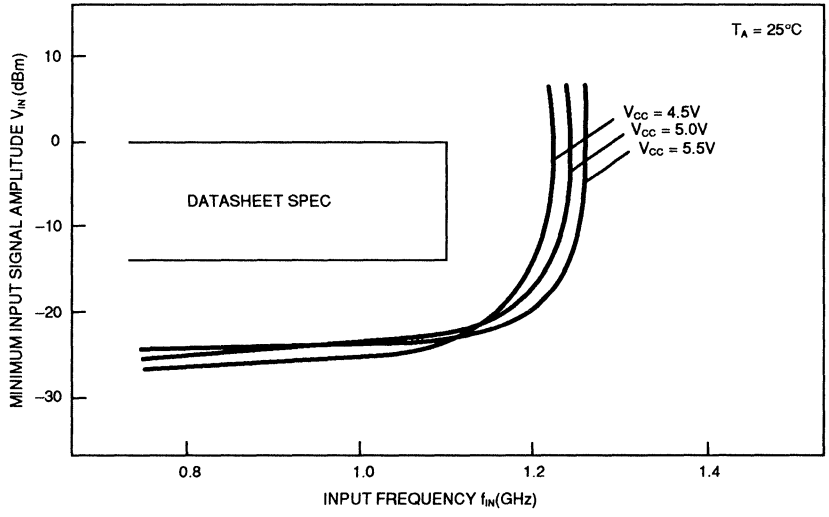


Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

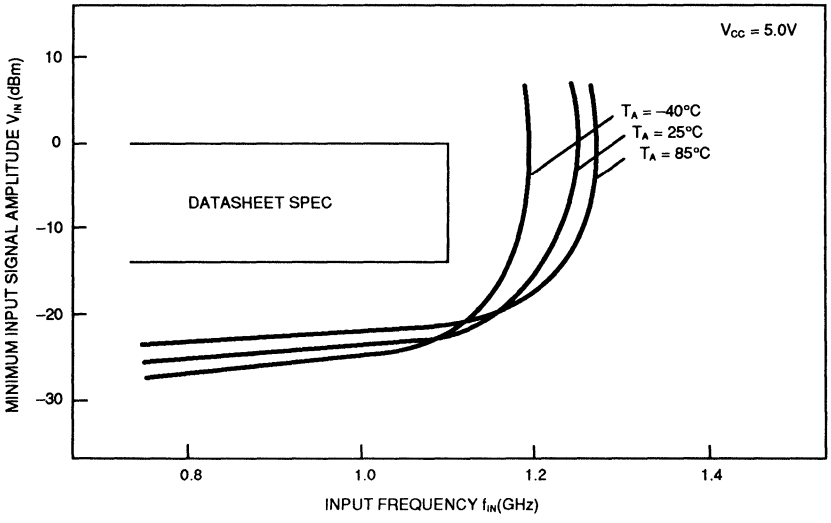


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Fig. 5 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

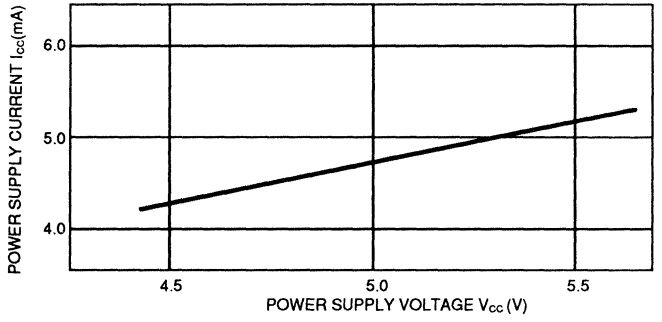


Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

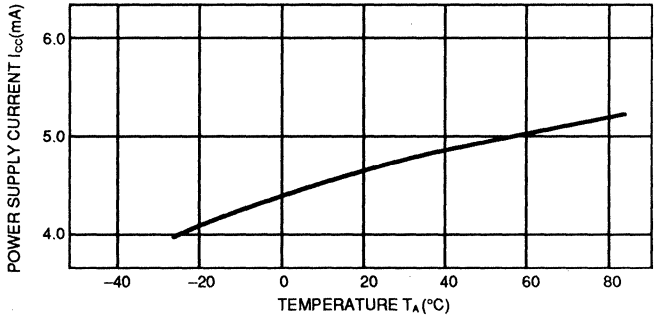


Fig. 7 – INPUT SIGNAL vs. INPUT FREQUENCY

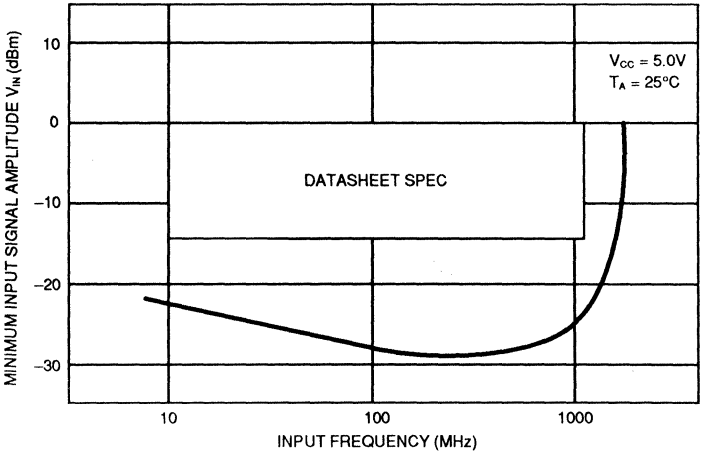
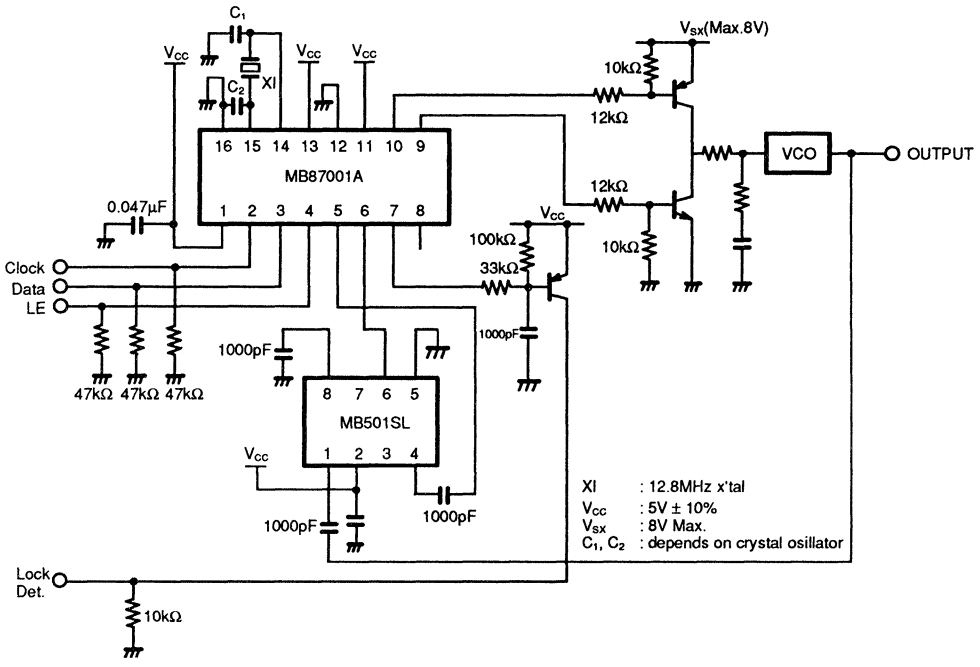


Fig. 8 –TYPICAL APPLICATION EXAMPLE



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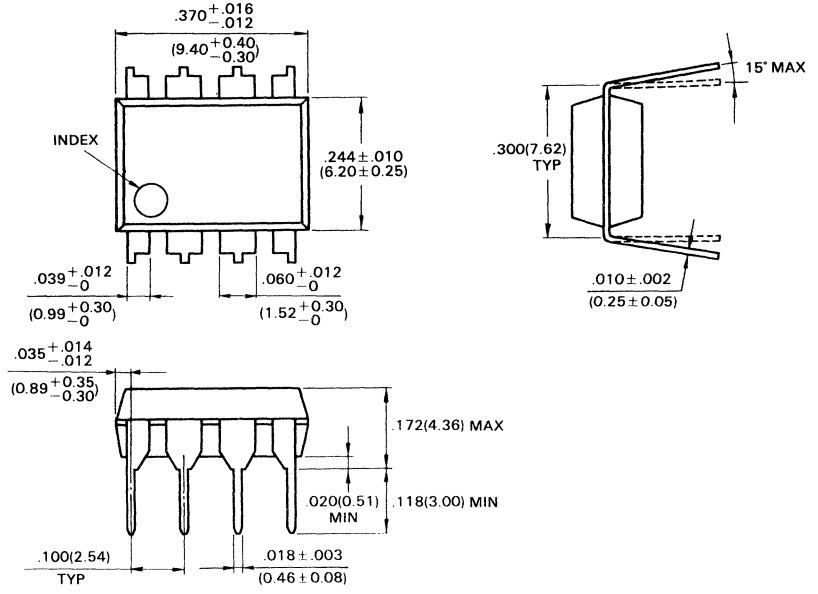
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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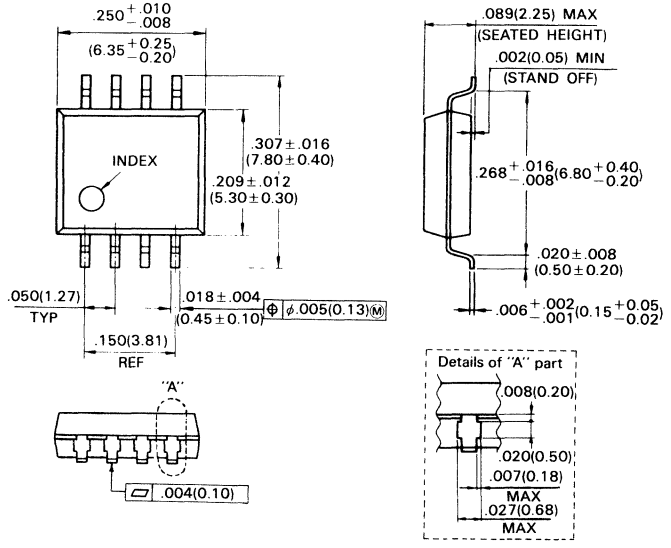
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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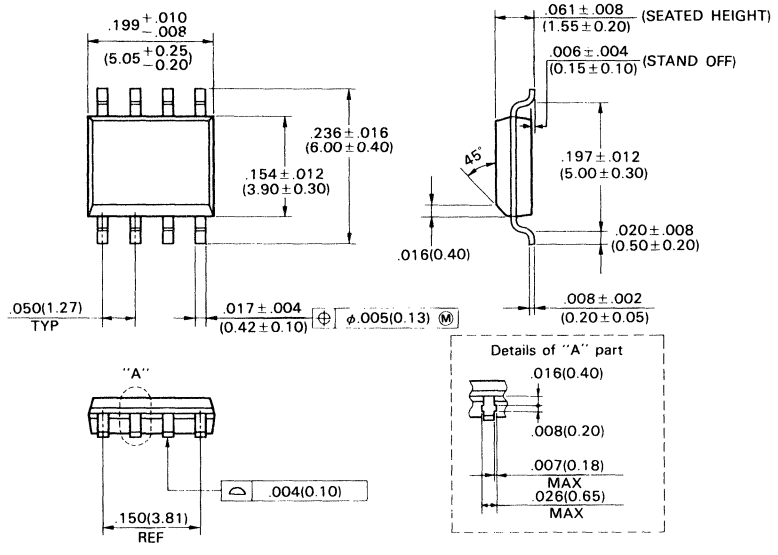
Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M02)



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Dimensions in
inches (millimeters)

FUJITSU

DATA SHEET

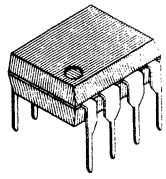
MB505-16
Ultra High Frequency Prescaler

ULTRA HIGH FREQUENCY PRESCALER

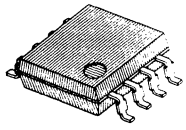
The Fujitsu MB505 is a high frequency prescaler used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 128 or 256. The output level is 1.6V peak to peak on ECL level.

Its ultra high frequency operation provides wide application range, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.

- High Frequency Operation 1.6GHz max.
- Low Power Dissipation 45 mW typ.
- Wide Operation Temperature −40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87006A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or Flat Package

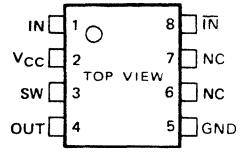


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

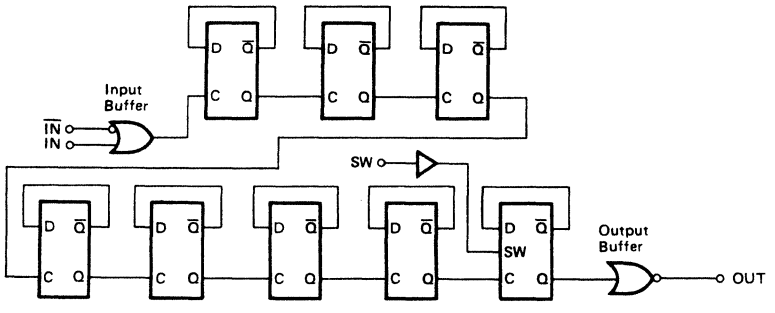
Raging	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 505 BLOCK DIAGRAM



SW	Divide Ratio
H	1/128
L	1/256

Note: SW: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	NC	No Connection
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

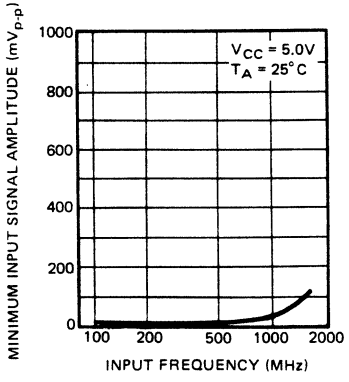
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply Current	I_{CC}			9		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000 pF	100		1600	MHz
Input Signal Amplitude	V_{IN}		0.15		1.2	V_{p-p}
High Level Input Voltage for SW	V_{IHS}		V_{CC}-0.1	V_{CC}	V_{CC}-0.1	V
Low Level Input Voltage for SW	V_{ILS}			Open		V

Fig. 2 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

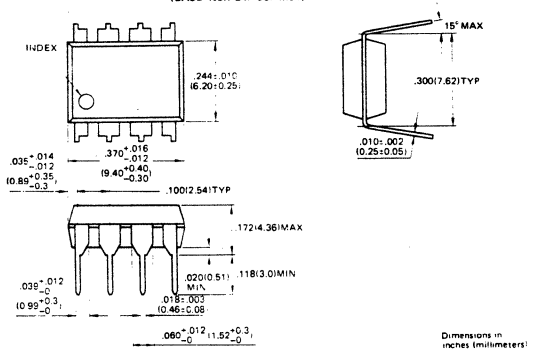


1

PACKAGE DIMENSIONS

(Suffix: -P) (Suffix: -PF)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

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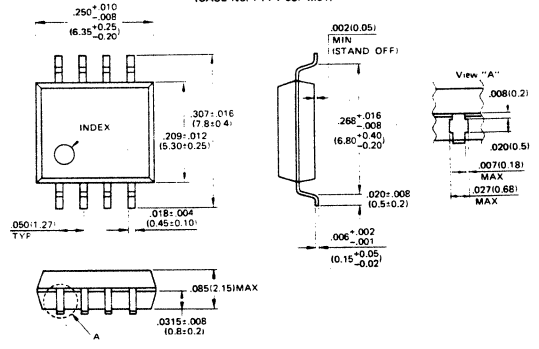
8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

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February 1990
Edition 3.0

FUJITSU

DATA SHEET

1

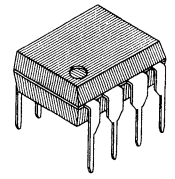
MB506
ULTRA HIGH FREQUENCY PRESCALER

ULTRA HIGH FREQUENCY PRESCALER

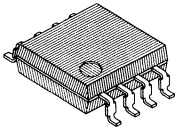
The Fujitsu MB506 is a high frequency prescaler used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 64, 128 or 256. The output level is 1.6V peak to peak on ECL level.

Its ultra high frequency operation provides wide application range, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.

- High Frequency Operation 2.4GHz max.
- Power Dissipation 90 mW typ.
- Wide Operation Temperature −40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87006A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or Flat Package

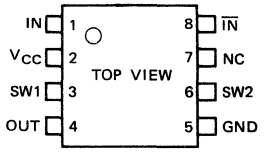


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
PFT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

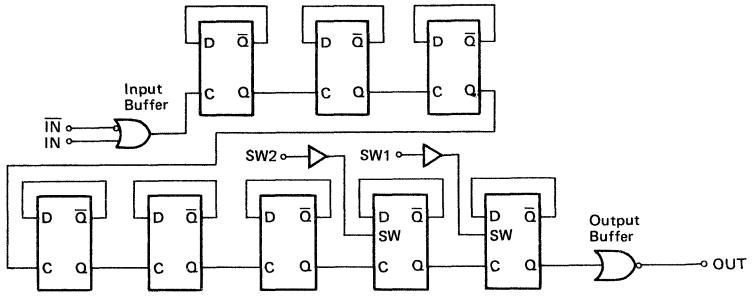
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 506 BLOCK DIAGRAM



SW1	SW2	Divide Ratio
H	H	1/64
L	H	1/128
H	L	1/128
L	L	1/256

Note: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW1	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	SW2	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
7	NC	No Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	−40		+85	°C
Load Capacitance	C_L			12	pF

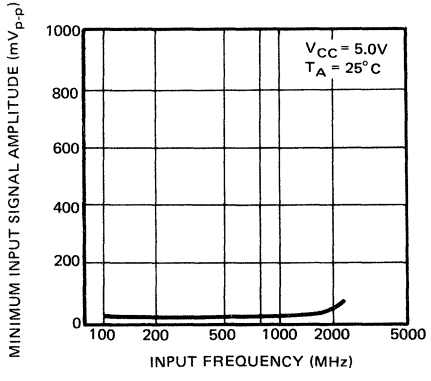
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Supply Current	I_{CC}				18		mA
Output Amplitude	V_O			1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	with input coupling capacitor 1000 pF	T_A = −40°C to 85°C	100		2200	MHz
			T_A = −40°C to 60°C	100		2400	
Input Signal Amplitude	V_{IN}	f_{IN} = 100 MHz to 1.3 GHz		−16		5.5	dBm
		f_{IN} = 1.3 MHz to 2.4 GHz		−4		5.5	
High Level Input Voltage for SW	V_{IHS}*			V_{CC}−0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW	V_{ILS}				Open		V

Note: *Design Guarantee

Fig. 2 — INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY



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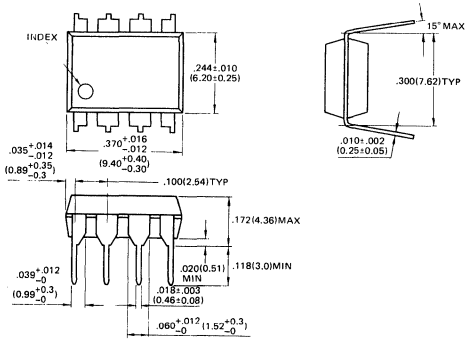
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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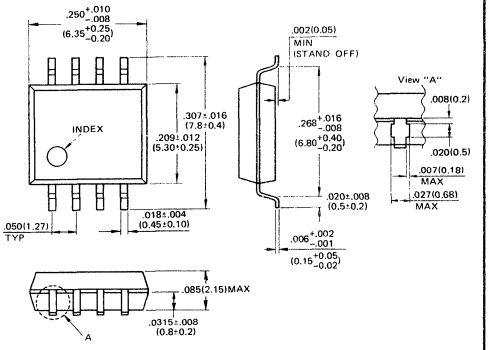
Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACJAGE
(CASE No.: FPT-08P-M01)



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Dimensions in inches (millimeters)

April 1990
Edition 4.0

FUJITSU

DATA SHEET

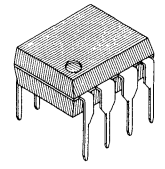
1

MB507
1.6 GHz TWO MODULUS PRESCALER

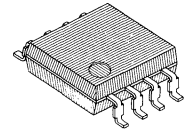
1.6 GHz TWO MODULUS PRESCALER

The Fujitsu MB507 is a 1.6 GHz two modulus prescaler used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency modulus of 128/129 or 256/257.
The output level is 1.6 V peak to peak on ECL level.

- High Frequency Operation: 1.6 GHz max.
- Power Dissipation: 90 mW typ.
- Pulse Swallow Function
- Wide Operation Temperature: −40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Package
  Standard 8-pin Dual-In-Line Package (Suffix: -P)
  Standard 8-pin Flat Package (Suffix: -PF)

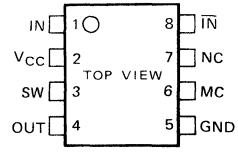


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

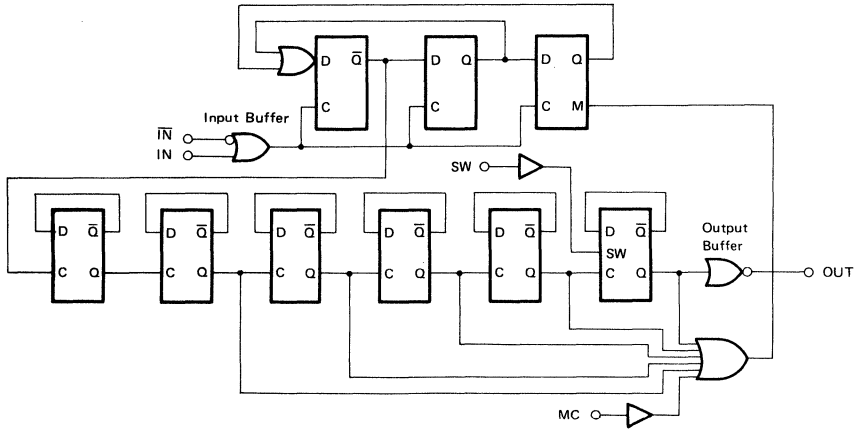
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB507 BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB 507	H	H	1/128
	H	L	1/129
	L	H	1/256
	L	L	1/257

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

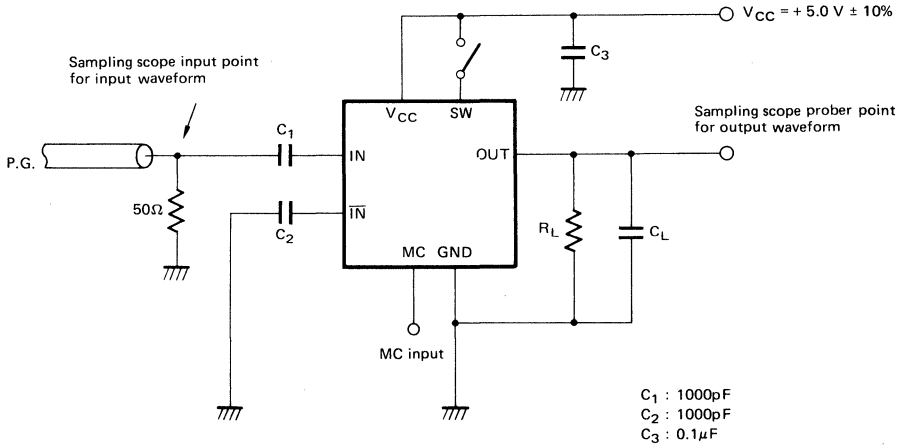
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply Current	I_{CC}			18		mA
Output Amplitude	V_O		1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	100		1600	MHz
Input Signal Amplitude	V_{IN}		-4		10	dBm
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}				0.8	V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW Input	V_{ILS}		OPEN			V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}	1.6 GHz Operation		18	28	ns

Note: * Design Guarantee

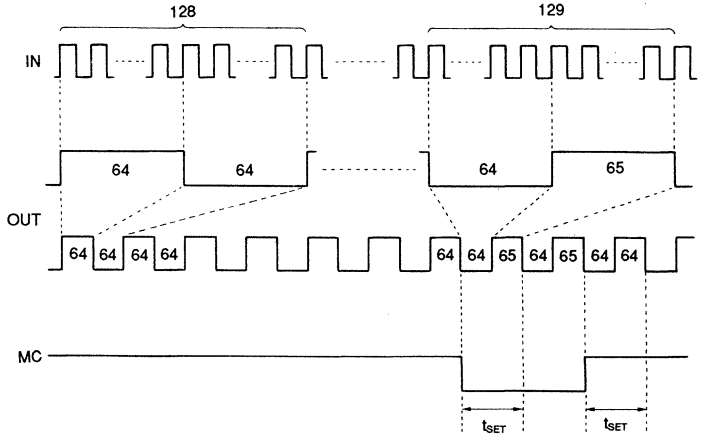
1

Fig. 2 – TEST CIRCUIT



TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/129



Note: When divide of 129 is selected, positive pulse is applied by one to 65.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

Fig. 3 — INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

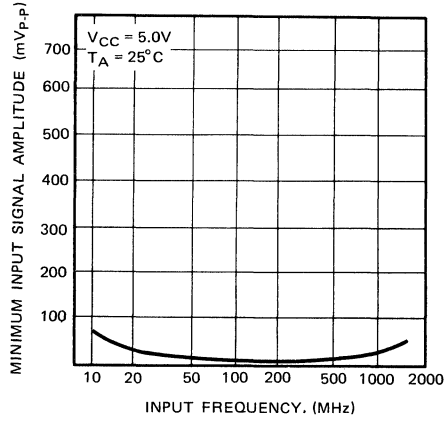
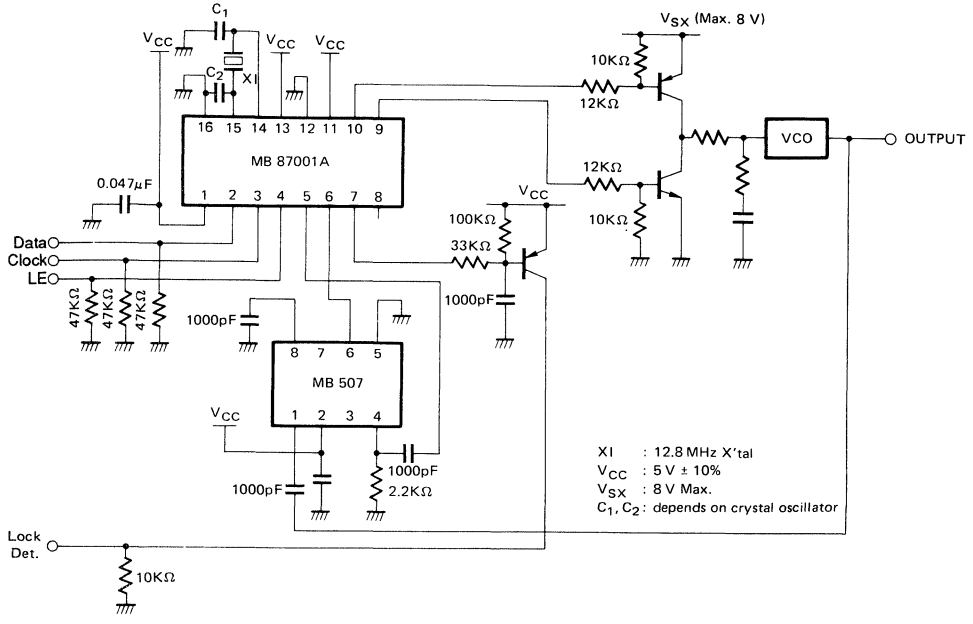


Fig. 4 — TYPICAL APPLICATION EXAMPLE



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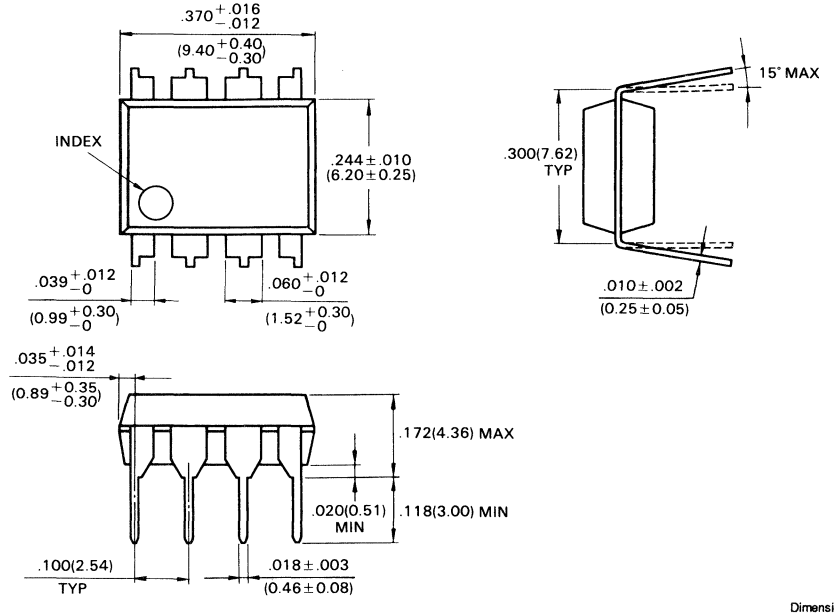
PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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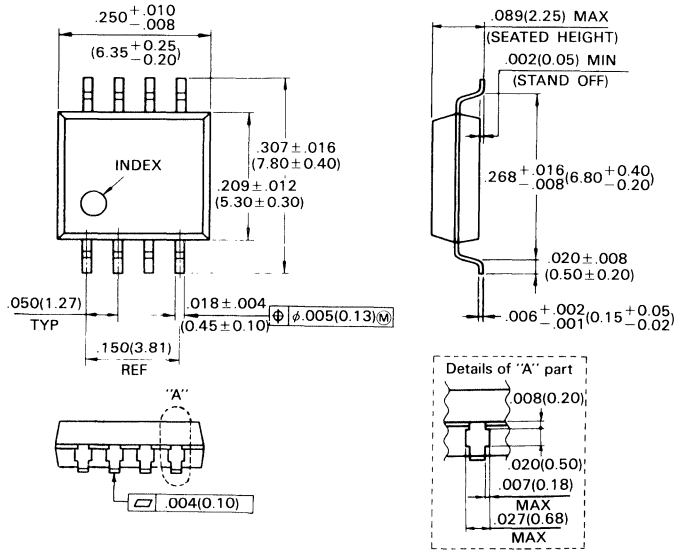
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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Dimensions in
inches (millimeters)

April 1990
Edition 3.0

FUJITSU

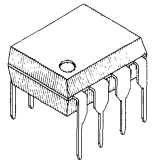
DATA SHEET

1

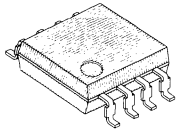
MB508
2.3GHz TWO MODULUS PRESCALER

2.3 GHz TWO MODULUS PRESCALER

The Fujitsu MB508 is a 2.3 GHz two modulus prescaler used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by a modulus of 128/130, 256/258 or 512/514. The output level is 1.6V peak to peak ECL level. Its ultra high frequency operation provides wide application, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.



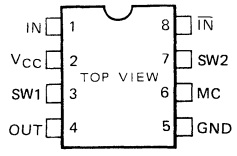
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

- High Frequency Operation: f = 2.3 GHz max. (V_{IN} = -4dBm min.)
- Input Signal Amplitude: V_{IN} = 100 mV_{P-P} (f_{IN} = 100 MHz to 1.8 GHz)
- Pulse Swallow Function: 128/130, 256/258, 512/514
- Power Dissipation: 120 mW typ.
- Wide Operation Temperature: -40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6V_{P-P} typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Standard Plastic 8-pin Dual-In-Line Package or Flat Package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

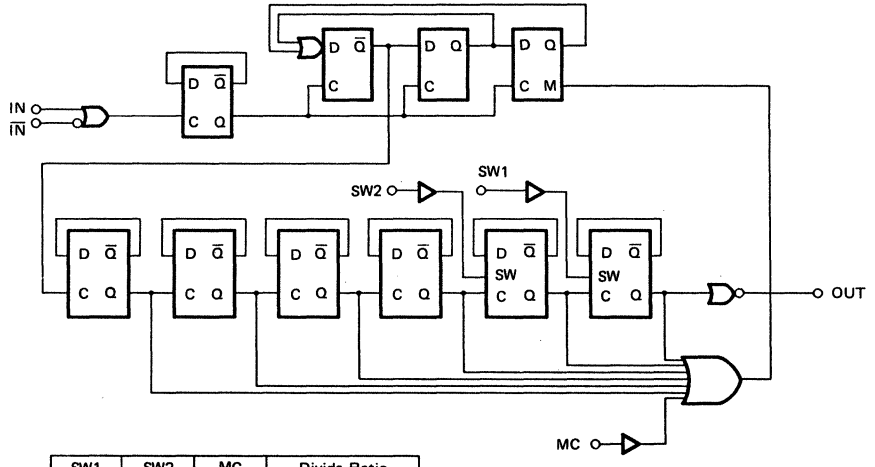
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB508 BLOCK DIAGRAM



SW1	SW2	MC	Divide Ratio
H	H	H	1/128
H	H	L	1/130
H	L	H	1/256
L	H	H	1/256
H	L	L	1/258
L	H	L	1/258
L	L	H	1/512
L	L	L	1/514

Note: SW: H=V_{CC}, L=Open
MC: H=2.0V to V_{CC}, L=GND to 0.8V

PIN DESCRIPTION

Pin Number	Symbol	Descriptions
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW1	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	SW2	Divide Ratio Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Operating Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

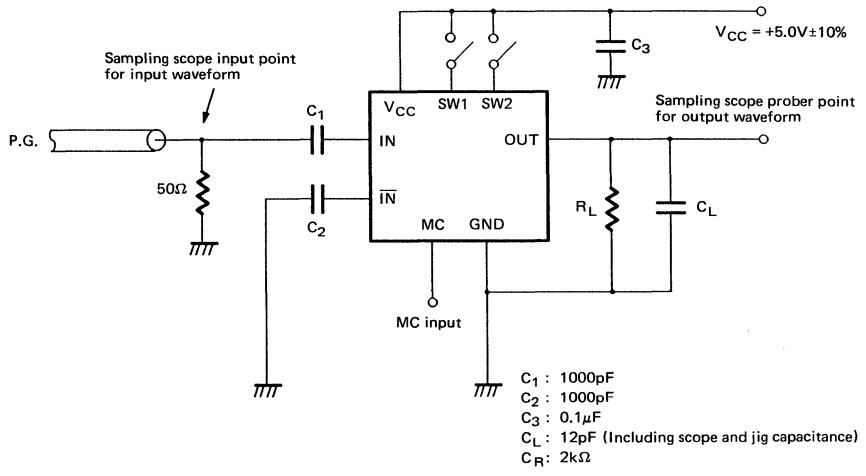
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			24		mA
Output Amplitude	V_O		1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	100		2300	MHz
Input Signal Amplitude	V_{INA}	f_{IN} = 1800MHz to 2300MHz	-4		5.5	dBm
	V_{INB}	f_{IN} = 100MHz to 1800MHz	-16		10	dBm
High Level Input Voltage for MC	V_{IHM}		2.0			V
Low Level Input Voltage for MC	V_{ILM}				0.8	V
High Level Input Voltage for SW	V_{IHS}*		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW	V_{ILS}		OPEN			V
High Level Input Current for MC	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC	I_{ILM}	V_{IL} = 0.8V	-0.2			mA
High Level Input Current for SW	I_{IHS}	$V_{IH} = V_{CC}$			250	μA
Modulus Set-up Time MC to Output at 2.3GHz Operation	t_{SET}			18	28	ns

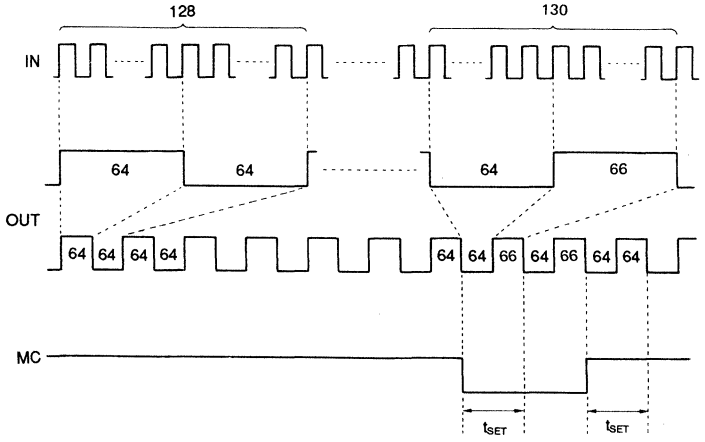
Note: *Design Guarantee

Fig. 2 – TEST CIRCUIT



TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/130



Note: When divide ratio of 130 is selected, positive pulse is applied by two to 66.
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

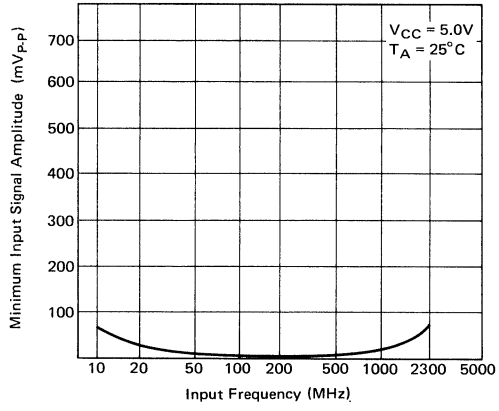
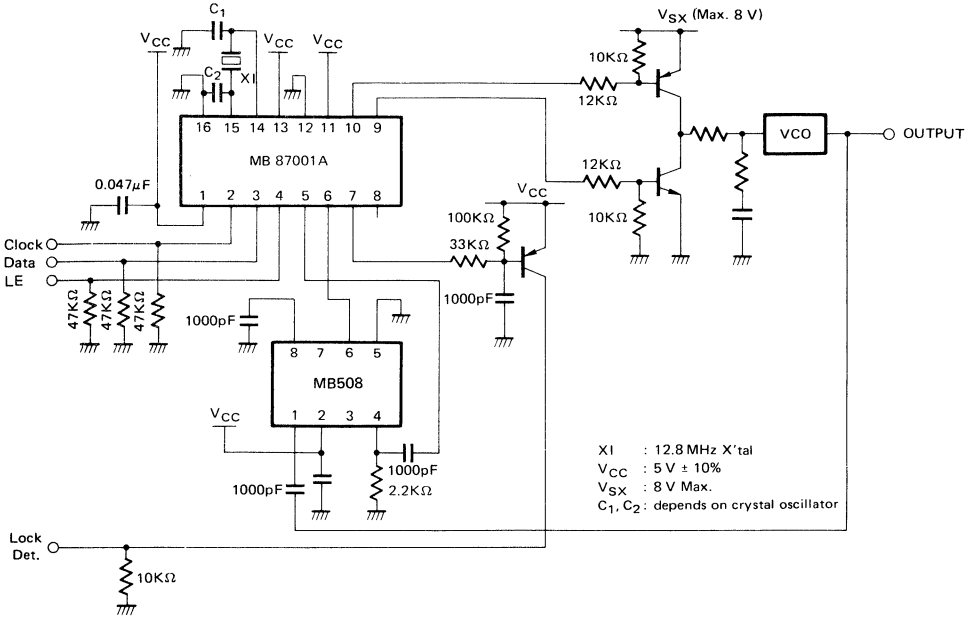


Fig. 4 – TYPICAL APPLICATION EXAMPLE



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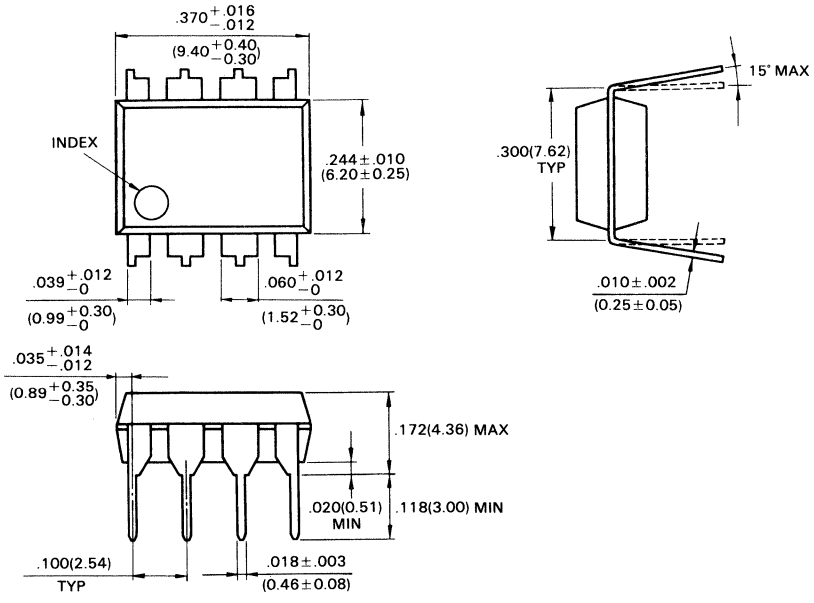
PACKAGE DIMENSIONS

(Suffix: -P)

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



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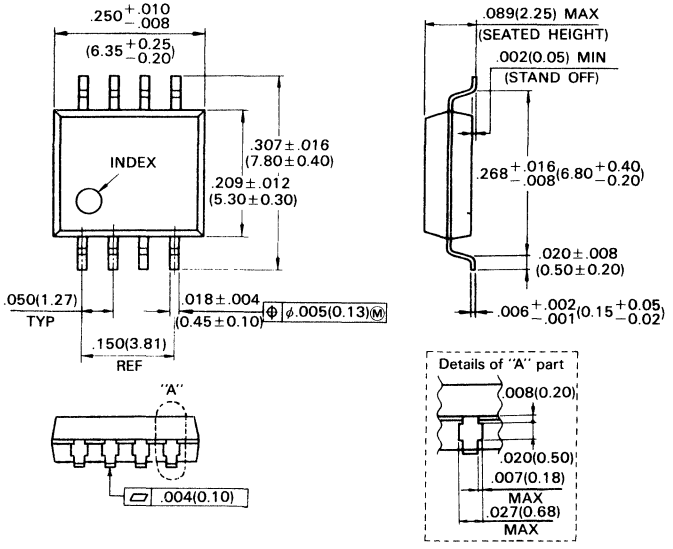
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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Dimensions in
inches (millimeters)

June 1990
Edition 3.0

FUJITSU

DATA SHEET

1

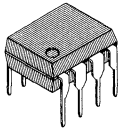
MB509
TWO MODULUS PRESCALER WITH STAND-BY MODE

TWO MODULUS PRESCALER WITH STAND-BY MODE

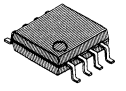
The Fujitsu MB509 is a low power two modulus prescaler which enables pulse swallow function. The MB509 is used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 64/65 or 128/129, respectively.

Power consumption is 58mW typ. at power supply voltage of 5.0V. The MB509 is equipped with the stand by mode which cuts off the power supply current I_{CC} under PLL phase lock condition. (I_{CC}=180μA under current cut condition)
Intermittent operating mode is achieved by using MB509 and MB87076.

- High Speed: fmax=1.1GHz max. (V_{IN}=–4dBm min.)
- Pulse Swallow Function: 64/65, 128/129
- Power Supply Consumption: 58mW typ.
- Stand-by Current: 180μA typ.
- Stable Output Amplitude: V_O=1.6 V_{P-P} typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87076, PLL frequency synthesizer IC.
- Plastic 8-pin Dual-In-Line Package (Suffix: –P)
  Plastic 8-pin Mini Flat Package (Suffix: –PF)
- Built-in a Termination Resistor
  Stable output amplitude is obtained up to output load capacitance of 8pF.

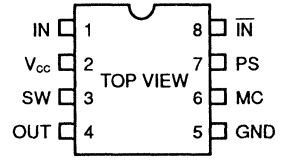


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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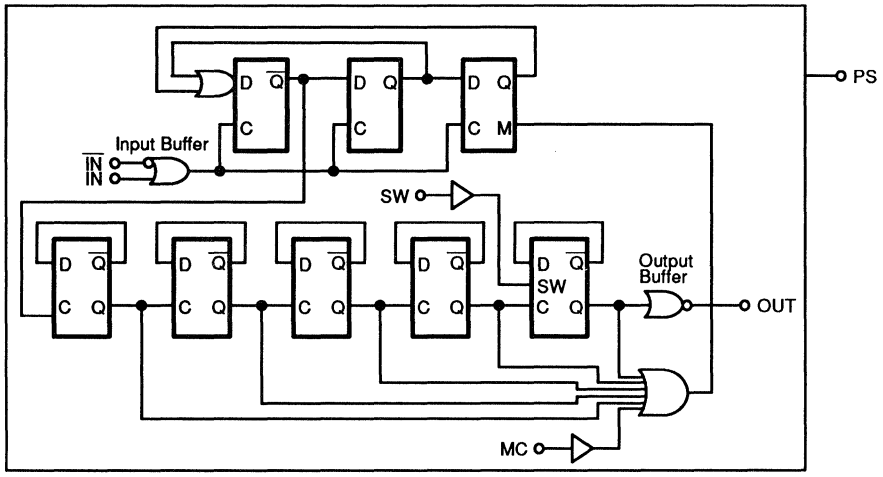
Fig. 1 – MB509 BLOCK DIAGRAM



PS	SW	MC	Divide Ratio
H	H	H	1/64
H	H	L	1/65
H	L	H	1/128
H	L	L	1/129
L	–	–	Stand-by mode

Note: SW: H=V_{CC}, L=open
MC: H=3.0V to V_{CC}, L=GND to 0.8V
PS: H=2.0V to V_{CC}, L=GND to 0.4V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	PS	Stand-by Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	–40	–	+85	°C
Load Capacitance	CL	–	–	8	pF

ELECTRICAL CHARACTERISTICS

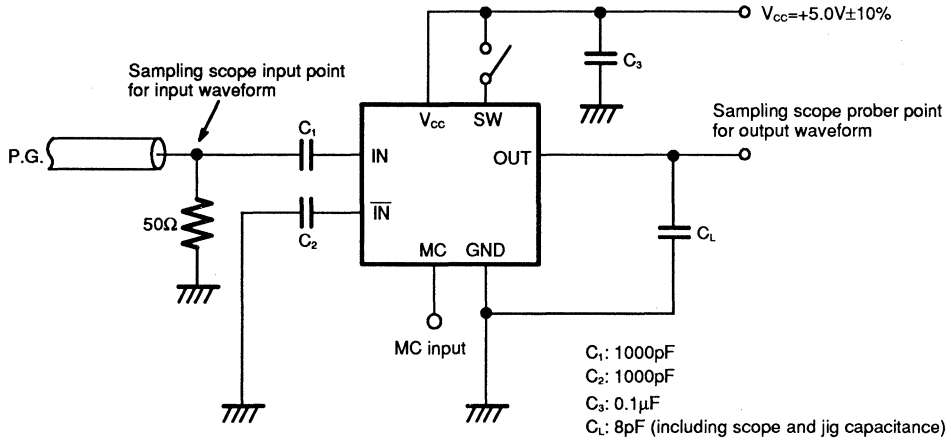
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}		–	11.6	–	mA
	I_{PS}	Stand-by mode	–	180	–	µA
Output Amplitude	V_O	Built-in a Termination Resitor. Load capacitance=8pF	1.0	1.6	–	V_{P-P}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10	–	1100	MHz
Input Signal Amplitude	V_{IN}	–	–4	–	5.5	dBm
High Level Input Voltage for MC	V_{IH}	–	3.0	–	–	V
Low Level Input Voltage for MC	V_{IL}	–	–	–	0.8	V
High Level Input Voltage for SW	V_{IHS}*		V_{CC}–0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW	V_{ILS}		Open			V
High Level Input Voltage for PS	V_{IH}	–	2.0	–	–	V
Low Level Input Voltage for PS	V_{IL}	–	–	–	0.4	V
High Level Input Current for MC	I_{IH}	V_{IH}=3.0V	–	–	0.4	mA
Low Level Input Current for MC	I_{IL}	V_{IL}=0.8V	–0.2	–	–	mA
Modulus Set-up Time MC to Output	t_{SET}	–	–	16	26	ns

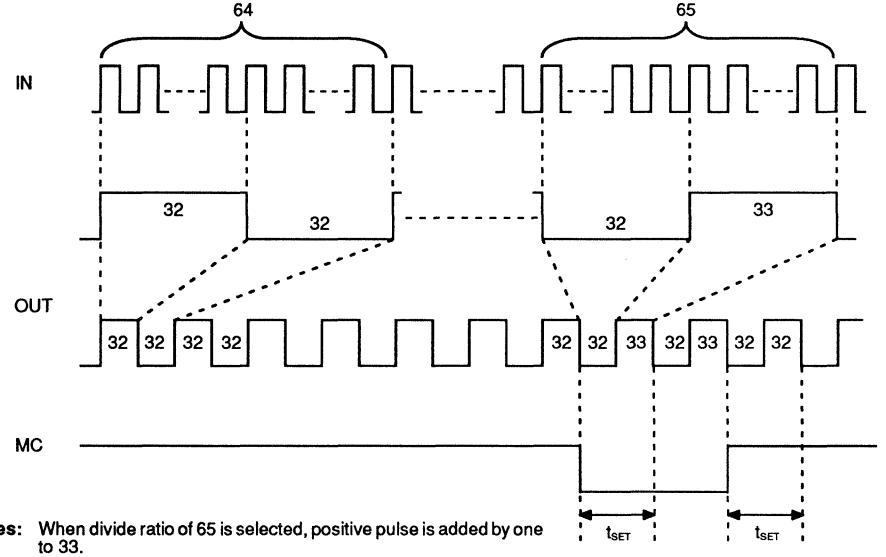
Note: * Design Guarantee

1

Fig. 2 – TEST CIRCUIT



TWO MODULUS OPERATING TIMING CHART (64/65 DIVIDE RATIO)



Notes: When divide ratio of 65 is selected, positive pulse is added by one to 33.
The typical set up time is 16ns from the MC signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

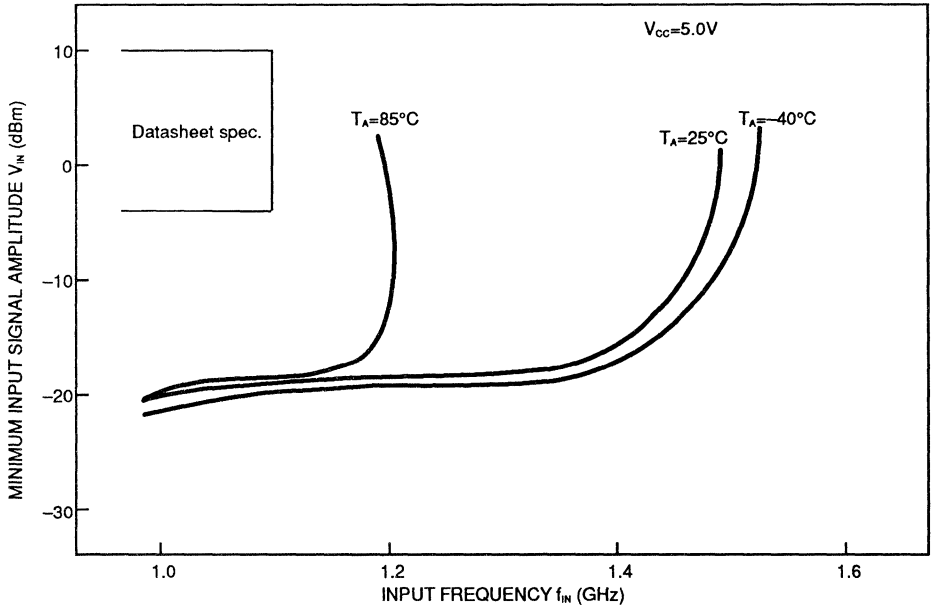
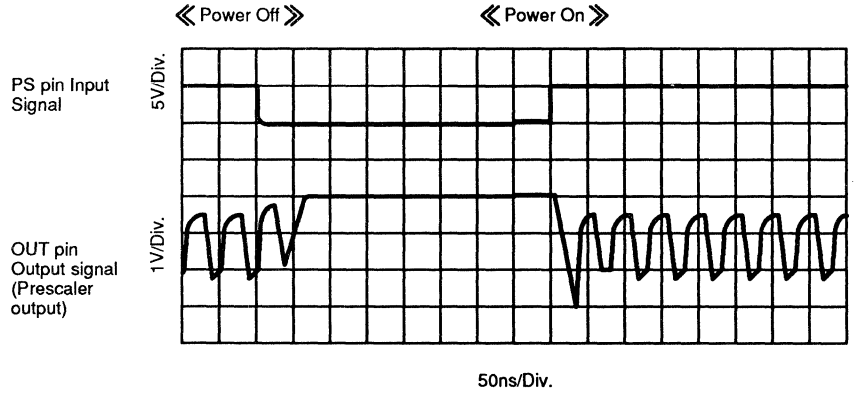


Fig. 4 – WAVEFORM OF STAND BY MODE



Note: About 50 ns of set up time is required both power on/off.

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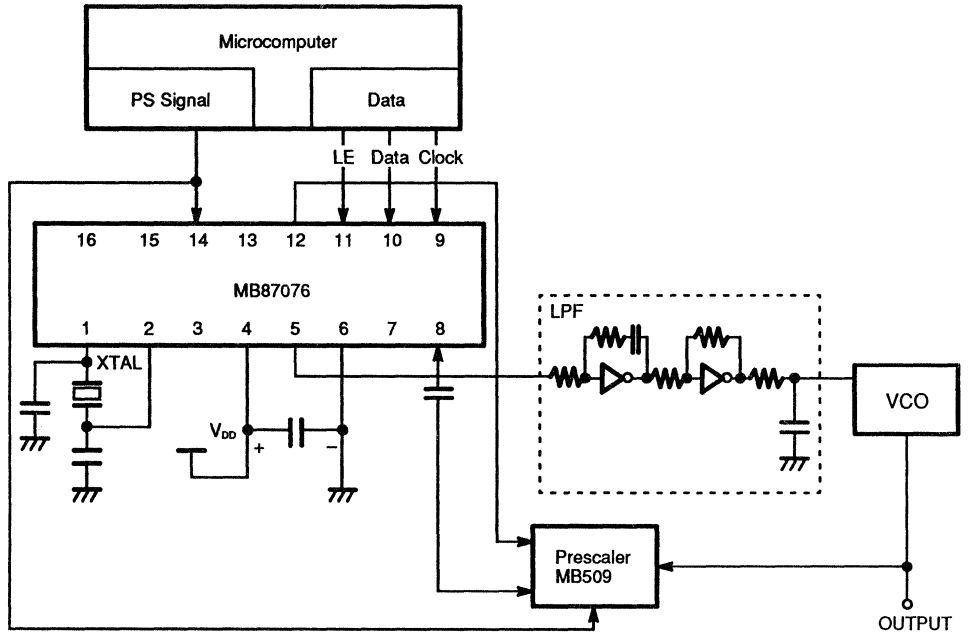
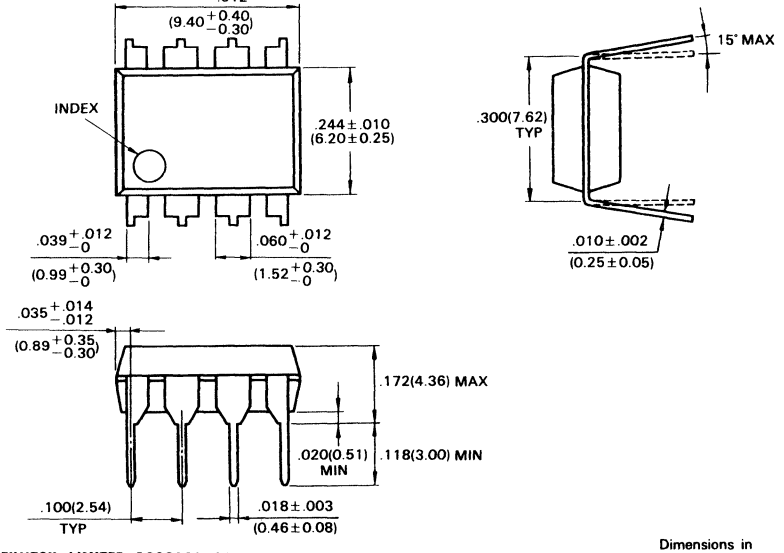
Fig. 5 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-8P-M01)



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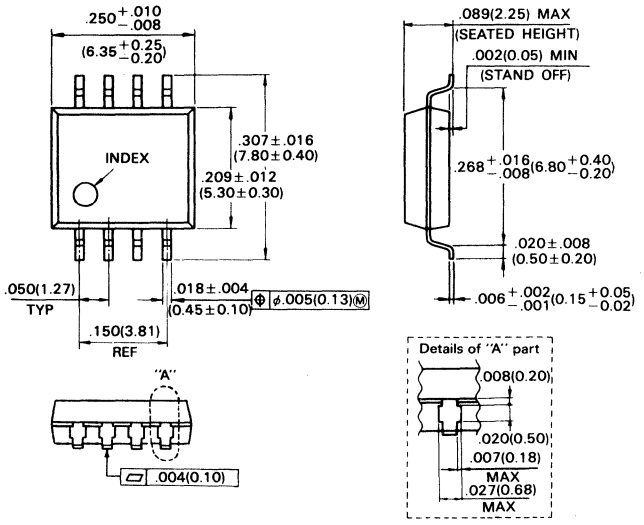
Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-8P-M01)



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Dimensions in inches (millimeters)

April 1990
Edition 3.0

FUJITSU

DATA SHEET

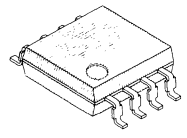
1

MB510
2.7 GHz TWO MODULUS PRESCALER

2.7 GHz TWO MODULUS PRESCALER

The Fujitsu MB510 is a ultra high speed two modulus prescaler which enables pulse swallow function. The MB510 is used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 128/144 or 256/272, respectively.

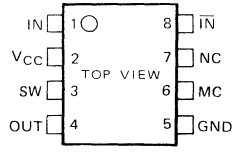
The MB510 achieves extremely small stray capacitance of internal element, realized through the use of Fujitsu Advanced Process Technology. As the results, ultra high speed is achieved with low power supply current of 10 mA typ.



PLASTIC PACKAGE
FPT-08P-M01

- High Frequency Operation: 2.7GHz max.
- Power Dissipation: 50 mW typ.
- Pulse Swallow Function: 128/144, 256/272
- Wide Operation Temperature: -40°C to +85°C
- Stable Output Amplitude: V_{OUT} = 1.6 V_{P-P} typ.
- Built-in a Termination Resistor
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer IC
- Package
  Standard 8-pin Flat Package (Suffix: -PF)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

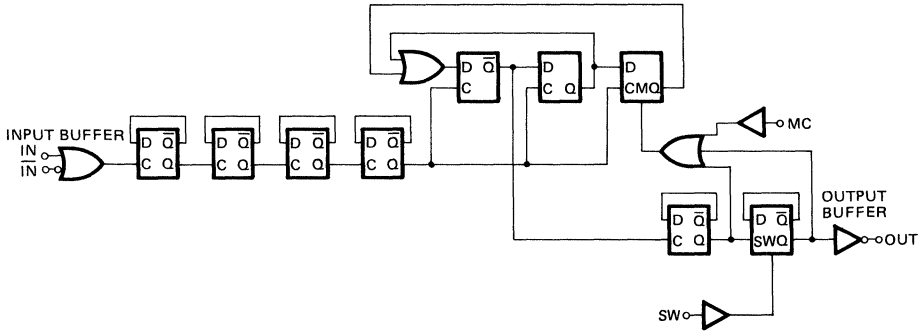
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB510 BLOCK DIAGRAM



SW	MC	Divide Ratio
H	H	1/128
H	L	1/144
L	H	1/256
L	L	1/272

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Current	I_{CC}			10.0	15.0	mA
Output Amplitude	V_O	Built-in a termination resistor. Load capacitance = 8pF	1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10		2700	MHz
Input Signal Amplitude	V_{IN}	f_{IN} = 10 to 2200 MHz	-10		10	dBm
		f_{IN} = 2200 to 2700 MHz	-4		10	
High Level Input Voltage for MC Input	V_{IHM}		2.0			V
Low Level Input Voltage for MC Input	V_{ILM}				0.8	V
High Level Input Voltage for SW Input	V_{IHS}*		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW Input	V_{ILS}		OPEN			V
High Level Input Current for MC Input	I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	t_{SET}			16	26	ns

Note: *Design Guarantee

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Fig. 2 – TEST CIRCUIT

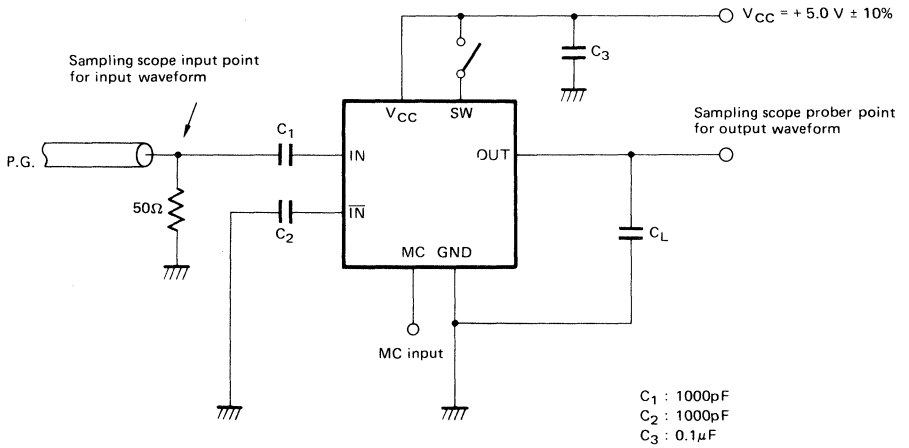
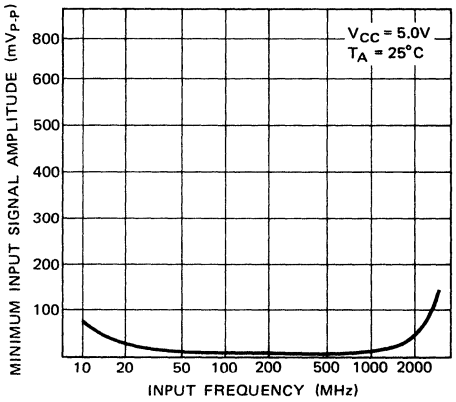
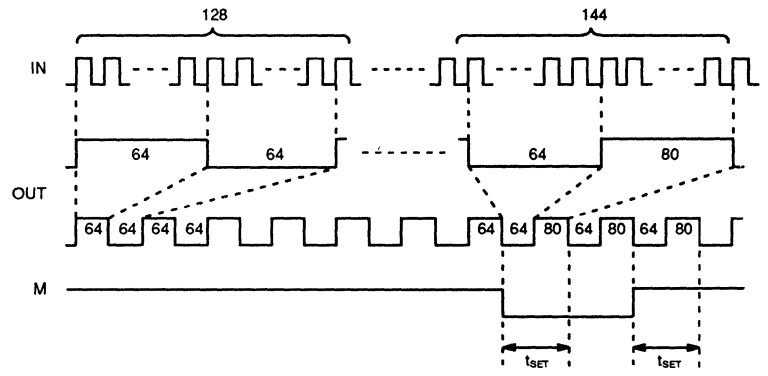


Fig. 3 – INPUT SIGNAL AMPLIFITUDE vs. INPUT FREQUENCY



TWO MODULUS TIMING CHART

Example. Divide Ratio of 128/144



Note: When divide ratio of 144 is selected, positive pulse is applied by 16 to 80.
The typical set up time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

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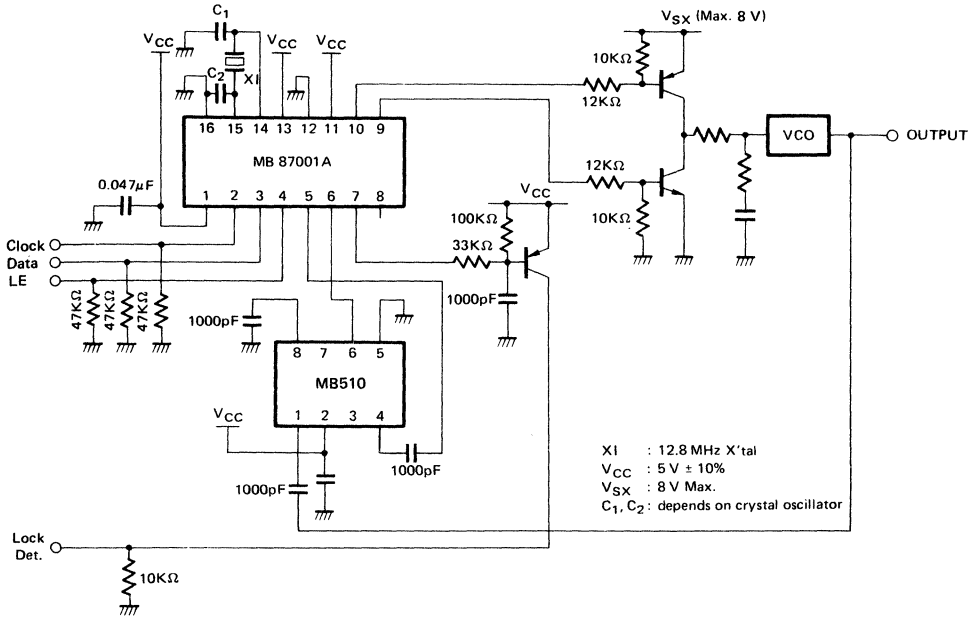
Fig. 4 – TYPICAL APPLICATION EXAMPLE



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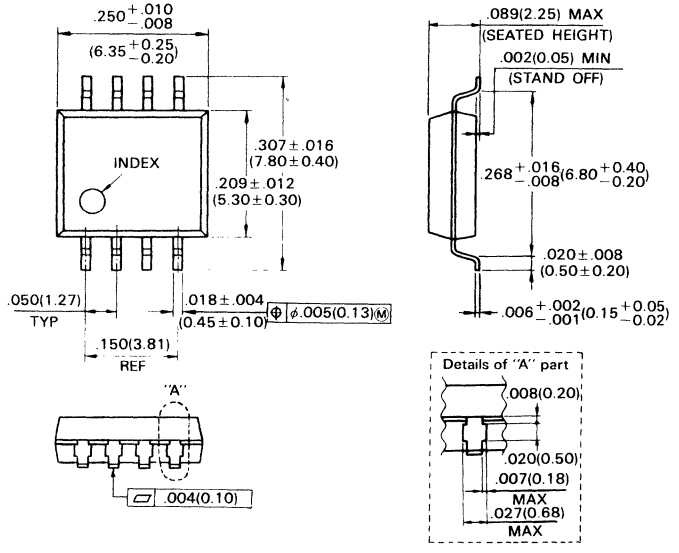
PACKAGE DIMENSIONS

(Suffix: -PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



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Dimensions in
inches (millimeters)

January 1990
Edition 2.0

FUJITSU

DATA SHEET

1

MB511
1GHz HIGH SPEED PRESCALER

HIGH SPEED PRESCALER

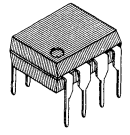
The Fujitsu MB511 is a 1GHz high speed prescaler designed for use in PLL (Phase Locked Loop) frequency synthesizer application.

The MB511 consumes low power 23mA at 5V up to 1GHz input frequency due to adoption of Fujitsu advanced bipolar process.

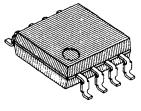
The MB511 will divide by 1, 2, or 8, respectively and very sensitivity (-20dBm min.). So, the MB511 is well suited for electronically tuned TV and CATV applications.

- Wide operating frequency range: f_{in} = 50 to 1000MHz (V_{in} = -20dBm)
- Maximum operating frequency depends upon a divide ratio
  1/1: 250MHz max. (Buffer through)
  1/2: 500MHz max.
  1/8: 1000MHz max.
- Low supply current: 23mA @5V
- High input sensitivity: -20dBm min
- Stable output amplitude: 800mVp-p ($C_L \leq 5pF$)
- Wide temperature range: T_A = -40 to +85°C
- Plastic 8-pin dual-in-line package (Suffix: -P)

  Plastic 8-pin flat package (Suffix: -PF)

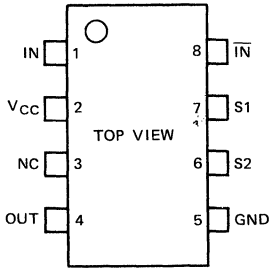


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

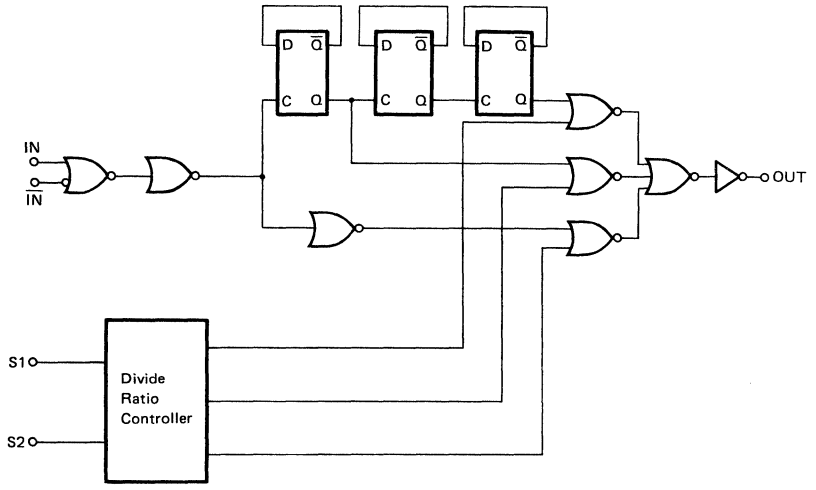
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.5	V
Output Current	V_O	10	mA
Storage Temperature	T_{STG}	-55 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB511 BLOCK DIAGRAM



FUNCTION TABLE

S1	S2	Divide Ratio	Operating Frequency
L	L	Not use	–
L	H	1	250 MHz
H	L	2	500 MHz
H	H	8	1000 MHz

H = V_{CC}
L = OPEN

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Descriptions
1	IN	I	Input. The connection with VCO should be an AC connection.
2	V_{CC}	–	Power supply voltage input.
3	NC	–	No connection.
4	OUT	O	Output. Termination resistor is necessary due to emitter follower output.
5	GND	–	Ground.
6	S2	I	Divide ratio control input.
7	S1	I	Divide ratio control input.
8	$\overline{IN}$	I	Complementary input.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Operating Temperature	T_A	−40		+85	°C	
Load Capacitance	C_L			5	pF	Termination resistor 500Ω

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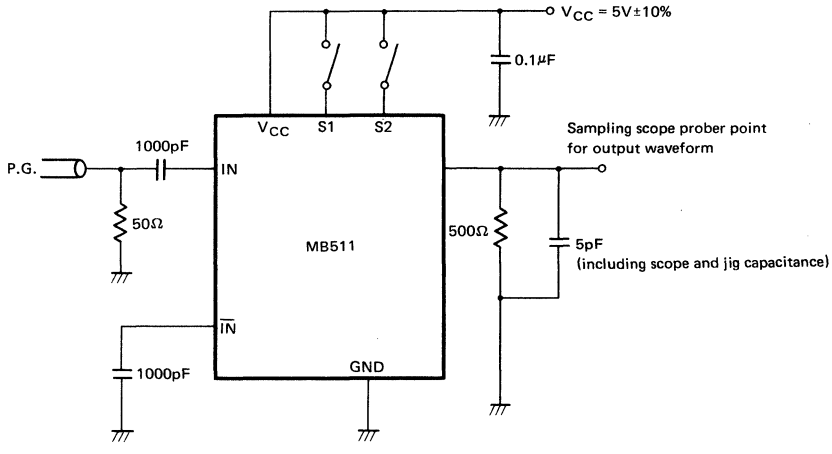
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Power Supply Current		I_{CC}	15	23	32	mA	Except termination output current.
Output Amplitude		V_O	0.4	0.8	1.2	V_{p-p}	500Ω termination, C_L = 5pF max.
Input Frequency	1/1	f_1	50		250	MHz	Min value is measured with coupling capacitor of 1000pF.
	1/2	f_2	50		500	MHz	
	1/8	f_3	50		1000	MHz	
Input Signal Amplitude		V_{in}	-20		+10	dBm	50Ω
High Level Input Voltage	S1, S2	V_{IH}	V_{CC}-0.7	V_{CC}	V_{CC}+0.5	V	
Low Level Input Voltage		V_{IL}		OPEN		V	
High Level Input Current	S1, S2	I_{IH}	40		160	μA	V_{CC} = 5V

Fig. 2 – TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SENSITIVITY CURVE (1/8 DIVIDE RATIO) POWER SUPPLY VOLTAGE DEPENDENCY

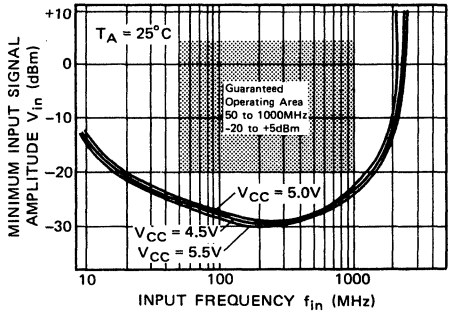


Fig. 4 – INPUT SENSITIVITY CURVE (1/2 DIVIDE RATIO) POWER SUPPLY VOLTAGE DEPENDENCY

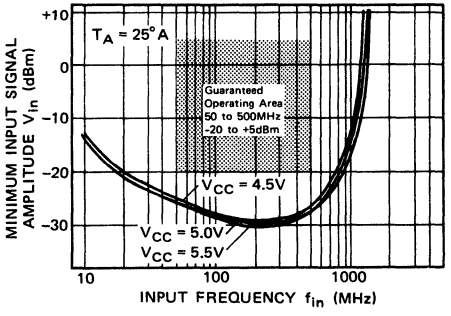


Fig. 5 – INPUT SENSITIVITY CURVE (1/1 DIVIDE RATIO) POWER SUPPLY VOLTAGE DEPENDENCY

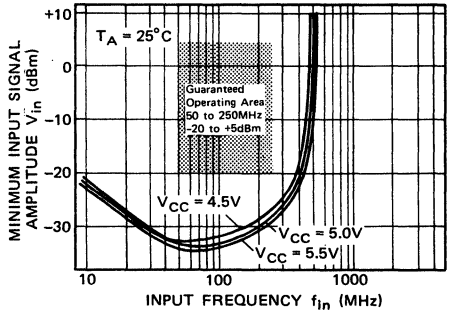
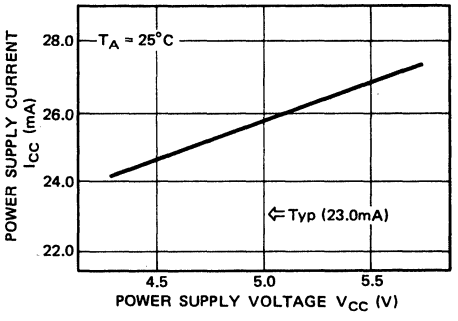


Fig. 6 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 7 – INPUT SENSITIVITY CURVE (1/8 DIVIDE RATIO) TEMPERATURE DEPENDENCY

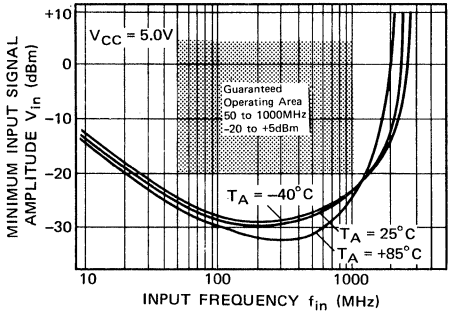


Fig. 8 – INPUT SENSITIVITY CURVE (1/2 DIVIDE RATIO) TEMPERATURE DEPENDENCY

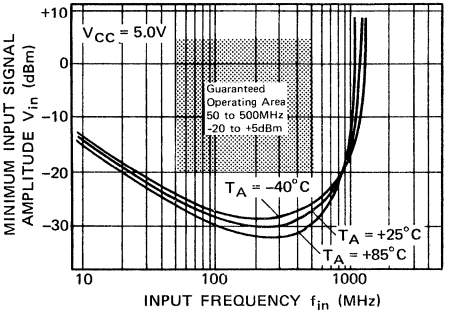


Fig. 9 – INPUT SENSITIVITY CURVE (1/1 DIVIDE RATIO) TEMPERATURE DEPENDENCY

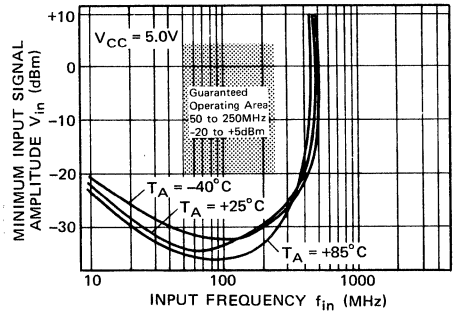
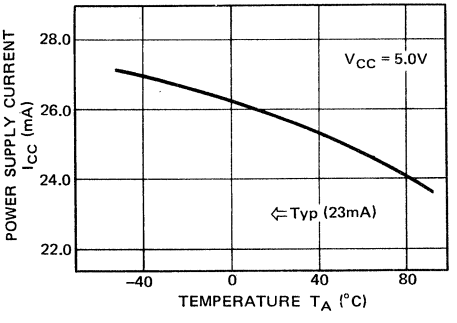


Fig. 10 – POWER SUPPLY CURRENT vs. TEMPERATURE

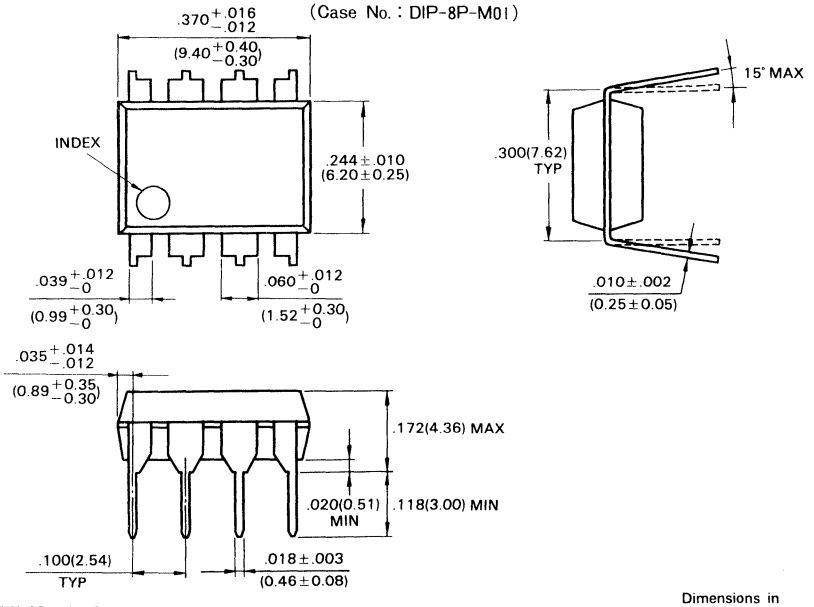


1

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-8P-M01)



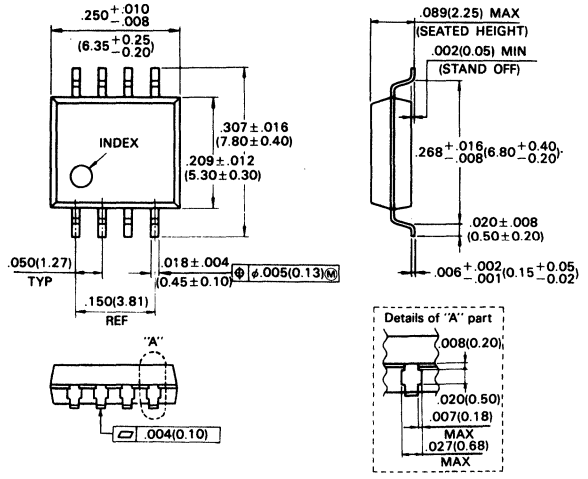
© 1988 FUJITSU LIMITED D08006S-2C

Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-8P-M01)



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Dimensions in
inches (millimeters)

Phase-Locked Loops (PLLs) — *At a Glance*

Page	Device	Maximum Frequency	Supply I_{CC}	Supply V_{CC}	Programmable Counter	Swallow Counter	Reference Counter
2–3	MB87001A	13 MHz	2.0 mA typ.	4.5 V– 5.5 V	Binary 16–1023	Binary 0–127	Binary 8–2048
2–15	MB87006A	10 MHz	3.5 mA	3.0 V– 6.0 V	Binary 16–1023	Binary 0–127	Binary 8–16383
2–27	MB87014A*	40 MHz	8.0 mA typ.	4.5 V– 5.5 V	Binary 5–1023	Binary 0–63	Binary 5–65535
2–37	MB87076	15 MHz	3.0 mA	2.7 V– 5.5 V	Binary 16–2047	Binary 0–127	Binary 8–16383
2–51	MB87086A	95 MHz	8.0 mA	4.5 V– 5.5 V	Binary 5–1023	None	Binary 5–65535
2–61	MB87087	10 MHz	2.5 mA typ. at 3.0 V 3.5 mA typ. at 5.0 V	3.0 V– 6.0 V	Binary 5–1023	Binary 0–127	Binary 5–16383
2–73	MB87090	15 MHz	4.0 mA typ. at 5.0 V	2.7 V– 5.5 V	Binary 16–1023	Binary 0–127	Binary 8–2048
		13 MHz	3.0 mA typ. at 3.0 V				

NOTES: All devices are available in 16-pin plastic DIP and FPT packages.
*Also has on-chip 180 MHz dual modulus (÷ 64/65) prescaler.

2

November 1990
Edition 7.0

FUJITSU

DATA SHEET

MB87001A
CMOS PLL FREQUENCY SYNTHESIZER

2

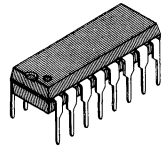
CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87001A, fabricated in CMOS technology, is a serial input PLL frequency synthesizer.

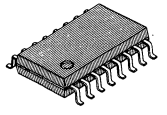
The MB87001A contains an inverter for oscillator, a programmable reference divider, a divide factor of programmable reference divider control circuit, a phase detector, a charge pump, a 17-bit shift register, a 17-bit latch, a programmable divider (a binary 7-bit swallow counter, a binary 10-bit programmable counter), and a control generator for an external dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87001A contains the necessary circuit to make up PLL frequency synthesizer. Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

- Single power supply voltage: V_{DD} = 2.7V to 5.5V
- Wide temperature range: T_A = –40 to 85°C
- 13MHz typical input capability @5V (fin input)
- On-chip inverter for oscillator
- 8 divide factors for programmable reference divider are selected by S_1, S_2 and S_3 input (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)
- Programmable 17-bit divider with input amplifier consisting of: Binary 7-bit swallow counter Binary 10-bit programmable counter
- Two types of phase detector output: On-chip charge pump output Output for external charge pump
- Easy interface to Fujitsu dual modulus prescaler

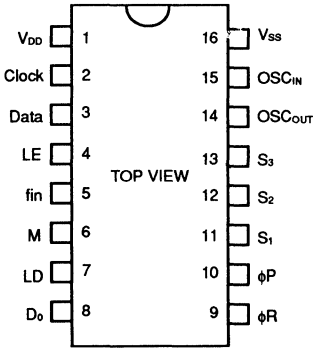


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE) **(V_{SS} = 0V)**

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Open-drain Output	V_{OOP}	V_{SS}–0.5 to V_{DD} +3.0	V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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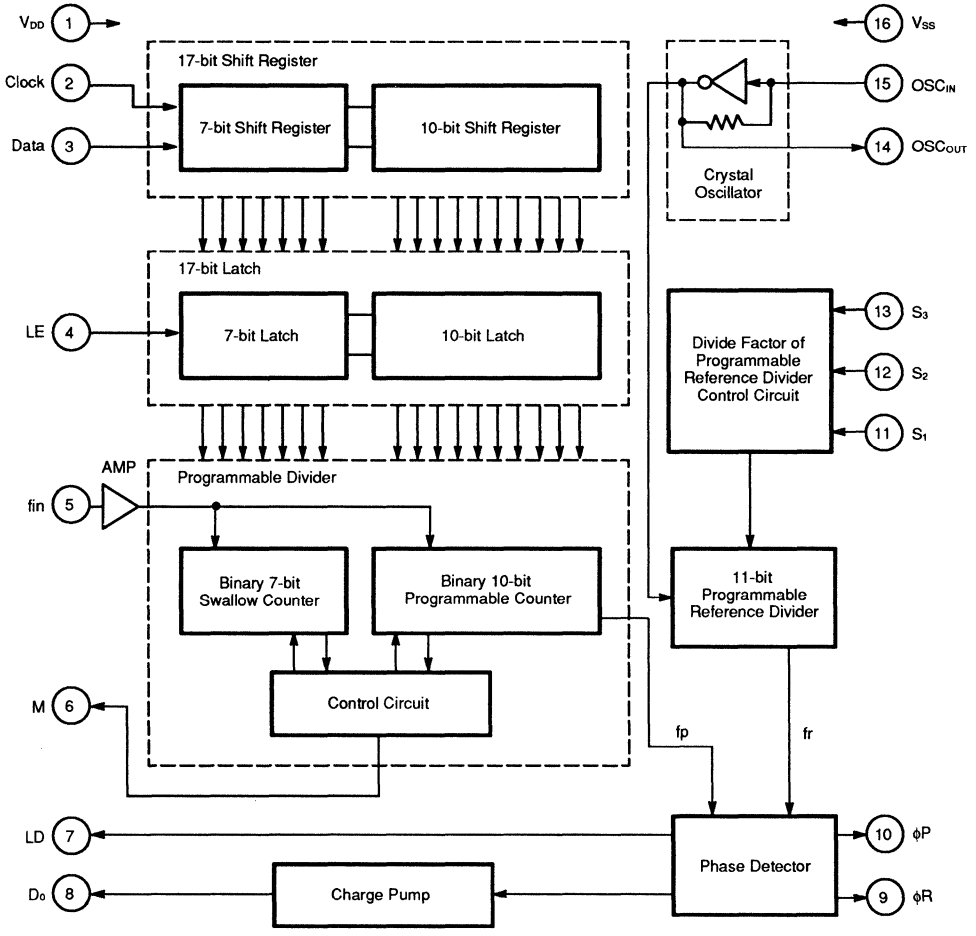
2

Fig. 1 – MB87001A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_{DD}	–	Power supply voltage input.
2	Clock	I	Clock signal input for 17-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift register.
3	Data	I	Serial data input for 17-bit shift register. The data is used for setting the divide factor of programmable divider.
4	LE	I	Load enable input. When this pin is high level (high active), the data stored in the 17-bit shift register is transferred to 17-bit latch.
5	fin	I	Input for programmable divider from VCO or prescaler output. This input involves bias circuit and amplifier. The connection with external dual modulus prescaler should be an AC connection.
6	M	O	Control output for external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #5). Pulse Swallow Function: MB501L M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 or 129
7	LD	O	Output of phase detector. It is high level when fr and fp are equal, and then the loop is locked. Otherwise it outputs negative pulse signal.
8	D_O	O	Three-state charge pump output of the phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency fp as listed below: fr > fp: Drive mode (D_O = High level) fr = fp: High-impedance mode fr < fp: Sink mode (D_O = Low level)
9 10	ϕR ϕP	O O	Phase detector outputs for an external charge pump. The mode of ϕR and ϕP is changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency fp as listed below: ϕR ϕP fr > fp: Low Low fr = fp: Low High-Impedance fr < fp: High High-Impedance * ϕP is a N-channel open drain output.

PIN DESCRIPTION (Continued)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>11
12
13</td><td>S_1
S_2
S_3</td><td>I
I
I</td><td>Control input for programmable reference divider. The combination of these inputs provides 8 kinds of divide factor for the programmable reference divider.
<table>
<tr><th>Sn \ Divide Factor</th><th>$\frac{1}{8}$</th><th>$\frac{1}{16}$</th><th>$\frac{1}{64}$</th><th>$\frac{1}{128}$</th><th>$\frac{1}{256}$</th><th>$\frac{1}{512}$</th><th>$\frac{1}{1024}$</th><th>$\frac{1}{2048}$</th></tr>
<tr><td>S_1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>S_2</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>S_3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>14</td><td>OSC_{OUT}</td><td>O</td><td>Output pin for crystal oscillator.
Output of the inverting amplifier. This pin should be open when an external oscillator is used.</td></tr>
<tr><td>15</td><td>OSC_{IN}</td><td>I</td><td>Input pin for crystal oscillator.
Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used.
For large amplitude signals (standard CMOS levels) DC coupling may also be used.</td></tr>
<tr><td>16</td><td>V_{SS}</td><td>–</td><td>Ground</td></tr>
</table>

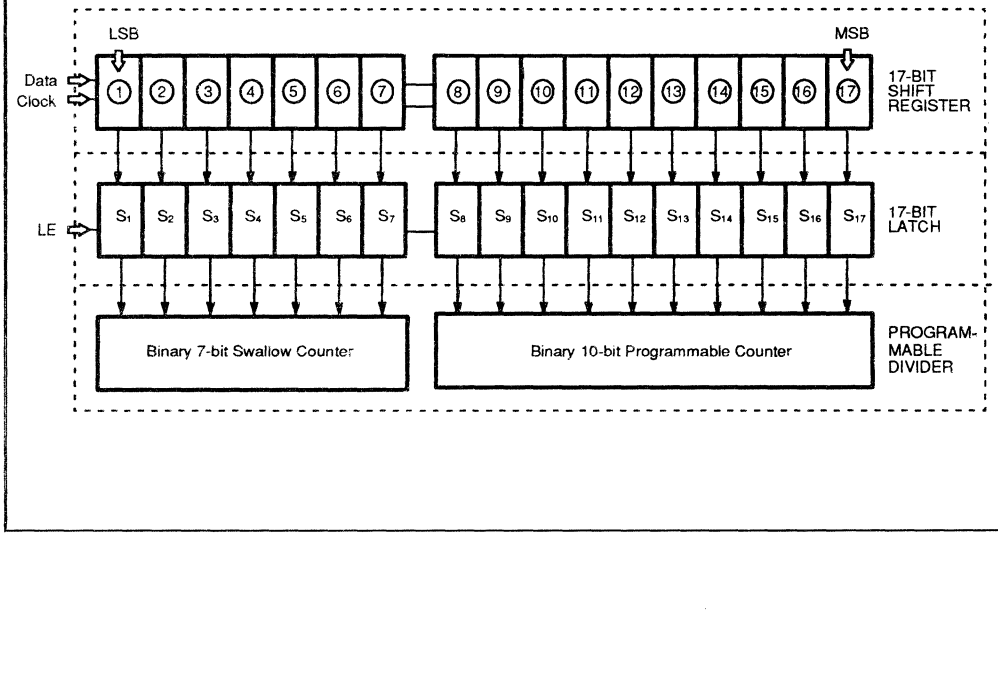
FUNCTIONAL DESCRIPTION

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to Data pin. These data are loaded into the 17-bit shift register from MSB. When load enable signal LE is high, the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The data ① to ⑦ set a divide factor of the binary 7–bit swallow counter and data ⑧ to ⑰ set a divide factor of binary 10-bit programmable counter. In other words, serial data is equivalent to the divide factor of programmable divider.

Fig. 2 – BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER



2

Binary 7-bit Swallow Counter Data Input

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
Example MB501L
SW = H (64/65): Bit 7 of shift register (7) should be zero.

Binary 10-bit Programmable Counter Data Input

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

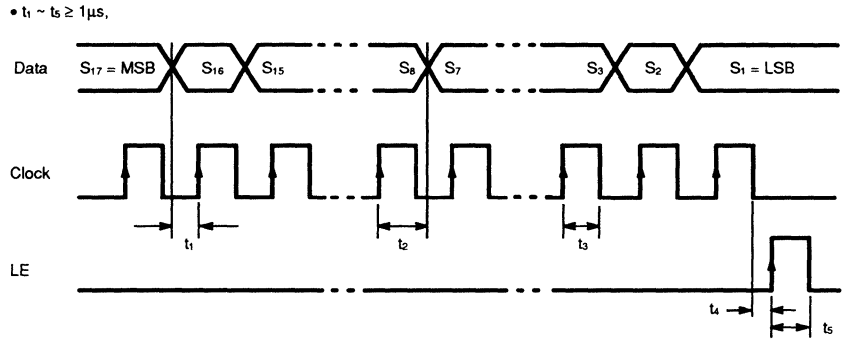
Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 1023

PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times fr$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
fr : Output frequency of the programmable reference divider

TIMING CHART



Clock : Clock signal input for the 17-bit shift register.
Each rising edge of the clock shifts one bit of data into the shift register.

Data : Serial data input for the 17-bit shift register.

LE : Load enable input.
When LE is high (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
The 17-bit data is used for setting a divide factor of the programmable divider.

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7		5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		2.1			V
Low-level Input Voltage		V_{IL}				0.9	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	0.8			V_{P-P}
	OSC_{IN}	V_{OSC}		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		–1.0		
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}		±30		µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±30		
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
Low-level Output Voltage	ϕP	V_{OLP}	I_{OL} = 0.8mA			0.8	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	2.50			
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA			0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	–0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	0.5			
N–channel Open Drain Cut Off Current	ϕP	I_{OFF}	$V_O = V_{DD}$ +3.0		1.0		µA
Power Supply Current*1		I_{DD}			2.0		mA
Max. Operating Frequency of Programmable Reference Divider		fmaxd		13	20		MHz
Max. Operating Frequency of Programmable Divider		fmaxp		10	20		MHz

Note: *1: fin = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for fin and OSC_{IN}. Outputs are open.

ELECTRICAL CHARACTERISTICS (continued)

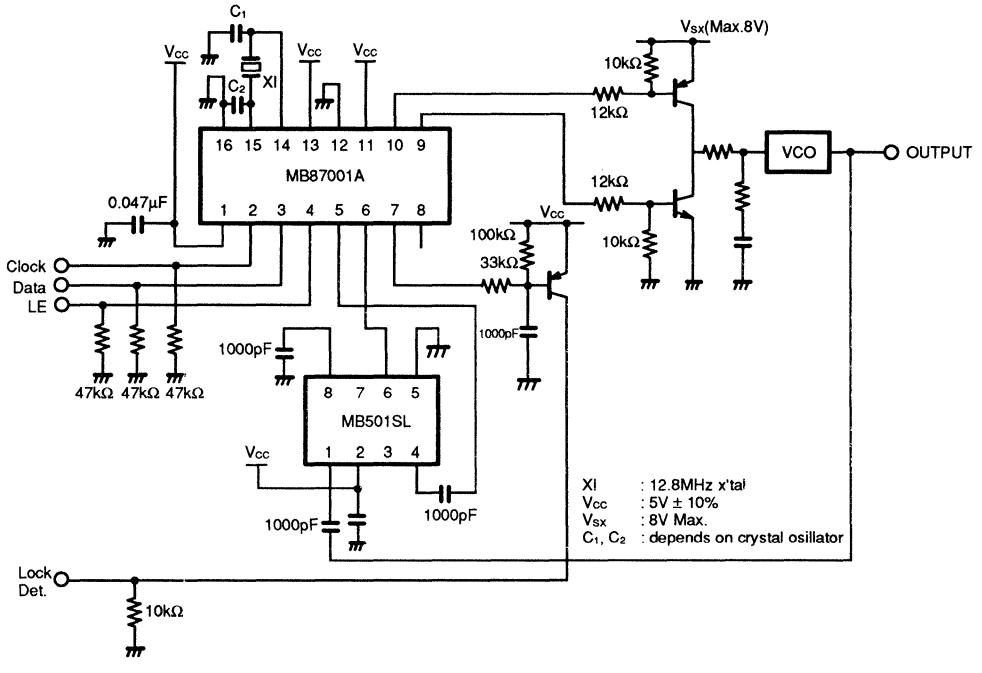
(V_{DD} = 5.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	1.0			V_{P-P}
	OSC_{IN}	V_{OSC}		1.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		–1.0		
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
Low-level Output Voltage	ϕP	V_{OLP}	I_{OL} = 2mA			1.0	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	4.50			
Low-level Output Voltage		I_{OLX}	I_{OL} = 0µA			0.50	
High-level Output Current	Except ϕP and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	–1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	1.0			
N–channel Open Drain Cut Off Current	ϕP	I_{OFF}	$V_O = V_{DD}$ +3.0		1.0		µA
Power Supply Current*1		I_{DD}			3.0		mA
Max. Operating Frequency of Programmable Reference Divider		fmaxd		15	25		MHz
Max. Operating Frequency of Programmable Divider		fmaxp		13	25		MHz

Note: *1: fin = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for fin and OSC_{IN}. Outputs are open.

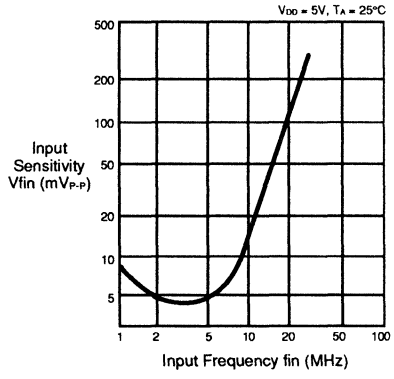
2

Fig. 3 –TYPICAL APPLICATION EXAMPLE

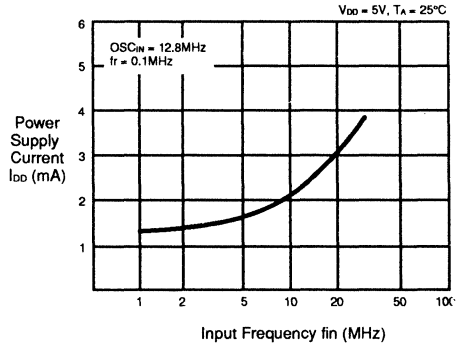


TYPICAL CHARACTERISTICS CURVES

Inupt Sensitivity vs. Input Frequency (fin Section)

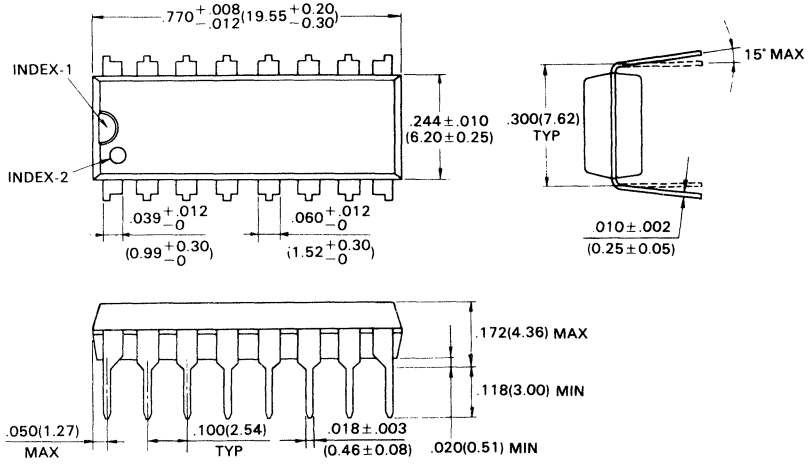


Power Supply Current vs. Input Frequency



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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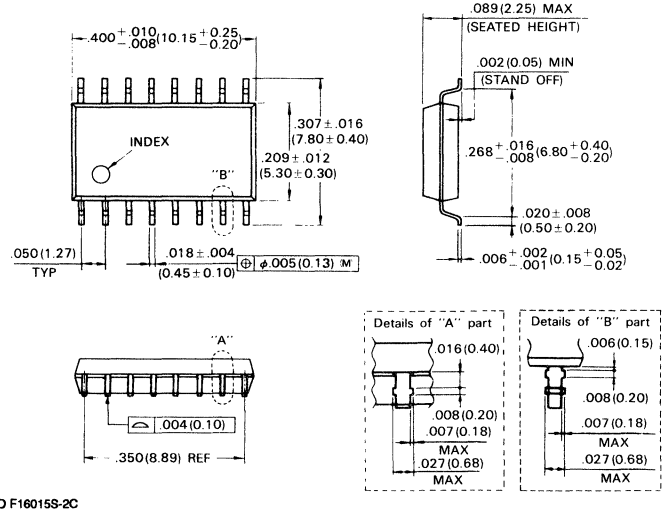
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

2

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in inches (millimeters)

November 1990
Edition 6.0

FUJITSU

DATA SHEET

MB87006A
CMOS PLL FREQUENCY SYNTHESIZER

2

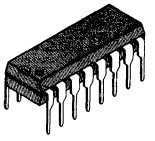
CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87006A, fabricated in CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer.

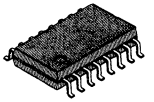
The MB87006A contains an inverter for oscillator, programmable reference divider (binary 14-bit programmable reference counter), 14-bit shift register, 14-bit latch, phase detector, charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter) and control generator for dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87006A contains the necessary circuit to make up a PLL frequency synthesizer. Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

- Wide range power supply voltage: V_{CC} = 3.0 to 6.0 V
- Wide temperature range: T_A = –40 to 85 °C
- 17 MHz typical input capability at 5 V (fin input)
- Programmable divider with input amplifier consisting of:
  –Binary 7-bit swallow counter
  –Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of binary 14-bit programmable reference counter
- On-chip inverter for oscillator
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is control bit.)
- Two types of phase detector output:
  –On-chip charge pump output
  –Output for external charge pump
- Easy interface with Fujitsu prescalers
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)

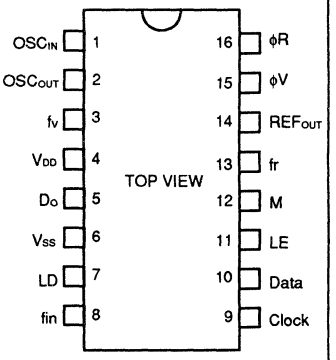


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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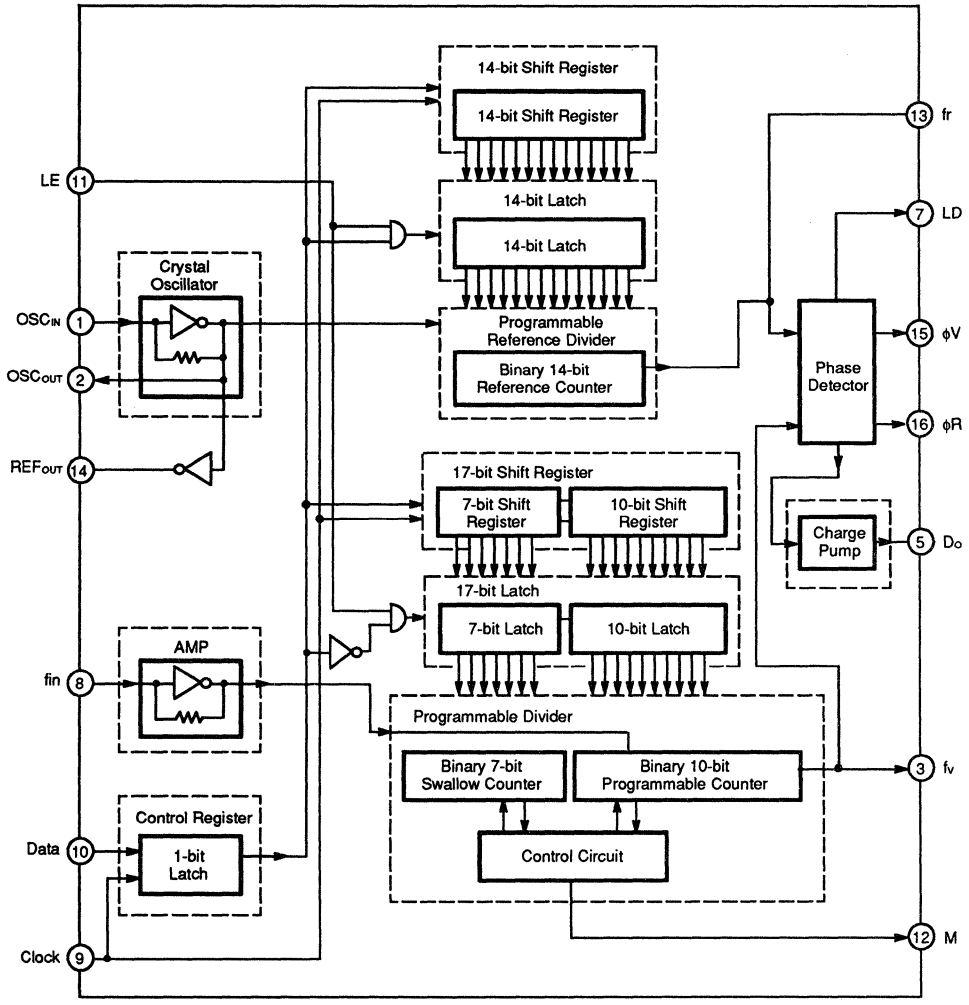
2

Fig. 1 – MB87006A BLOCK DIAGRAM



PIN DESCRIPTION

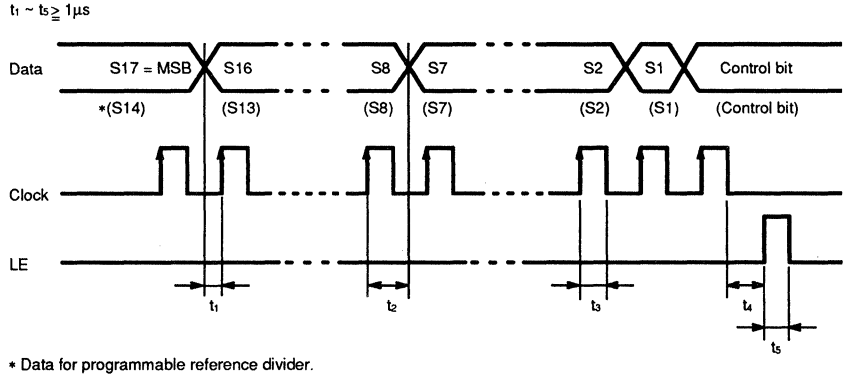
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	O	Monitor output of the phase detector. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_O	O	Three-state charge pump output of phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: $fr > f_V$: Drive mode (D_O = High level) $fr = f_V$: High impedance $fr < f_V$: Sink mode (D_O = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are equal, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	fin	I	Clock input for programmable divider. This input contains internal bias circuit and amplifier. The connection with an external dual-modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 17-bit shift register and 14-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for programmable divider and programmable reference divider. The last bit of the data is the control bit. Control bit determines which latch is activated. The data stored in the shift register is transferred to the 14-bit latch when the bit is high, and to 17-bit latch when low.
11	LE	I	Load enable input with internal pull up resistor. When this pin is high (active high), the data stored in shift register is transferred to 14-bit latch or 17-bit latch depending on the control bit data.
12	M	O	Control output for an external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #8). Pulse swallow function: e.g. MB501L: M = High: Preset modulus factor 64 or 128 M = Low Preset modulus factor 65 to 129

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
13	fr	O	Monitors output of phase detector input. This pin is tied to the programmable reference divider output.
14	REF_{OUT}	O	Monitor output pin of the reference frequency. This output can be used as system clock for microprocessor, or reference oscillator for another PLL frequency synthesizer.
15 16	ϕV ϕR	O O	Output for external charge pump. The mode of ϕR and ϕV is changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency f_V as listed below. ϕR ϕV fr > fv: Low-level HIgh-level fr = fv: High-level High-level fr < fv: High-level Low-level

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT TIMING



* Data for programmable reference divider.

Notes: Data: Serial data input is used for setting divide factor of programmable reference divider and programmable divider.
Data is input from MSB, and last bit data is a control bit.
Control bit is set high when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Data is input to internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data stored in shift register is transferred to 14-bit latch, or 17-bit latch depending on the control bit setting.

PULSE SWALLOW FUNCTION

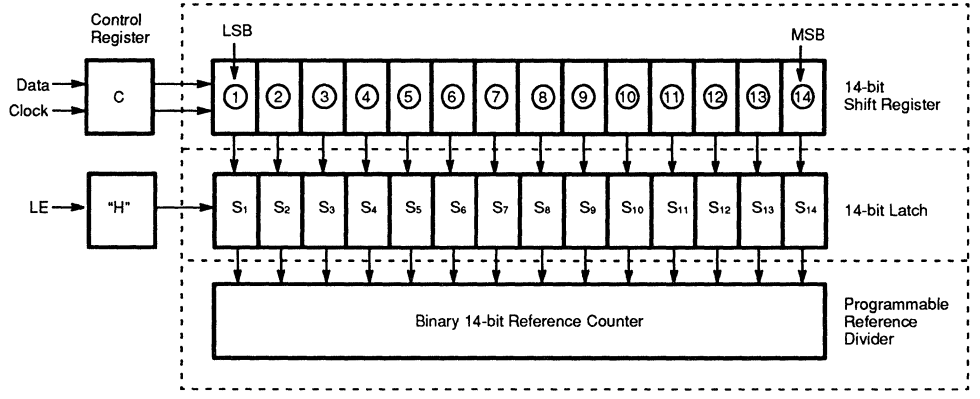
$$f_{VCO} = [(N \times M) + A] \times f_{OSC} \div R \quad (N > A)$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler
(e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit programmable counter (0 to 127, A < N)
f_{OSC} : Output frequency of external oscillator
R : Preset divide factor of binary 14-bit programmable reference counter (5 to 16383)

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

Serial data consists of 14-bit data, which is used for setting divide factor of programmable reference counter, and 1-bit control data. In this case, control bit is set high level.

The data format is shown below.



BINARY 14-BIT REFERENCE COUNTER DATA INPUT

⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

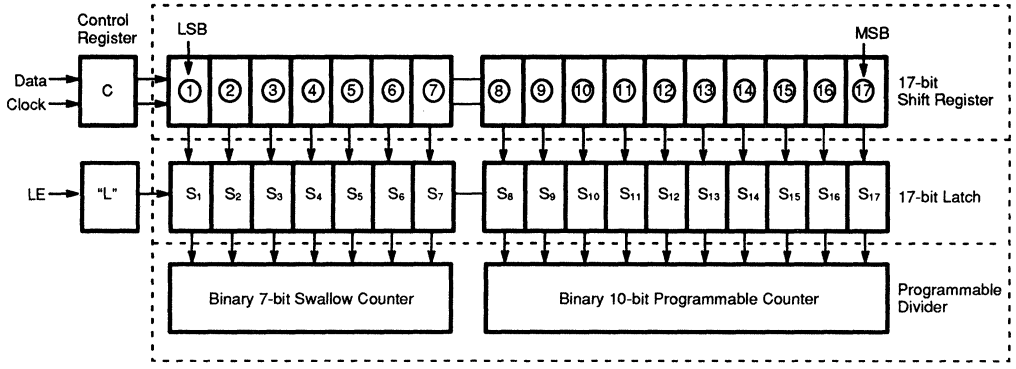
Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 16383

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data consists of 17-bit data, which is used for setting divide factor of programmable divider, and 1-bit control data. In this case, control bit is set low level. The data ① to ⑦ set a divide factor of 7-bit swallow counter and data ⑧ to ⑰ set divide factor of 10-bit programmable counter.

2

The data format is shown below.



BINARY 7-BIT SWALLOW COUNTER DATA INPUT

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

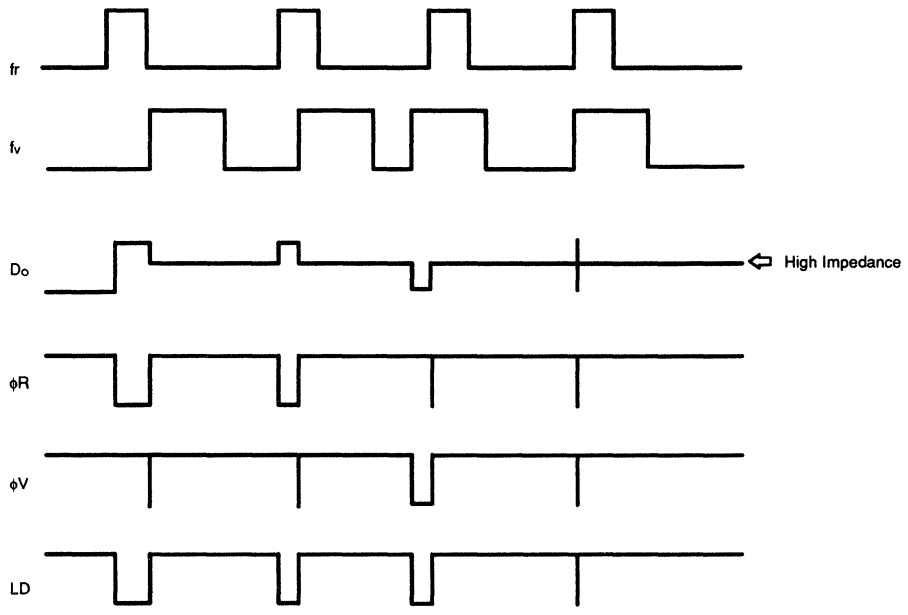
Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
e.g. MB501L (+65/65)prescaler
SW = H (64/65): Bit 7 to shift register ⑦ should be zero.

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited.
Divide factor N : 5 to 1023

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	3.0		6.0	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	Vsin		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±30		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±30		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–40		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 2.6V	–0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	0.5			
High-level Output Current	M	I_{OHM}	V_{OH} = 2.6V	–0.7			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	1.5			
Power Supply Current *1		I_{DD}			2.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	20		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		10	20		MHz

Notes: *1: fin = 8.0MHz 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except for fin and OSC_{IN}. Output are open.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = –40 to 85°C)

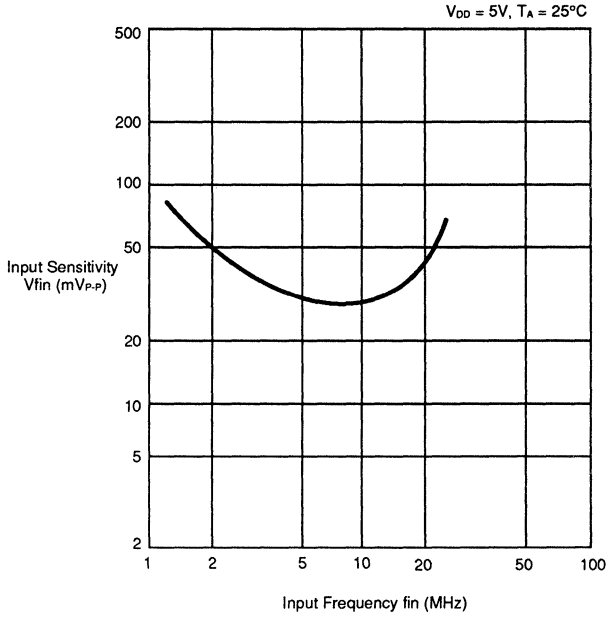
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	Vsin		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±50		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–60		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	–1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
High-level Output Current	M	I_{OHM}	V_{OH} = 4.6V	–1.5			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	3.0			
Power Supply Current *1		I_{DD}			3.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	25		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		17	25		MHz

Note: *1. fin = 8.0MHz, 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are ground except for fin and OSC_{IN}. Outputs are open.

TYPICAL CHARACTERISTICS CURVE

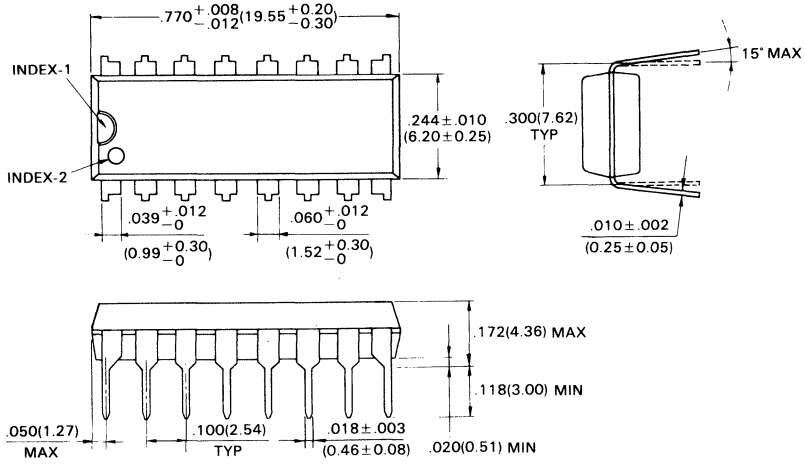
2

Input Sensitivity vs. Input Frequency (fin Section)



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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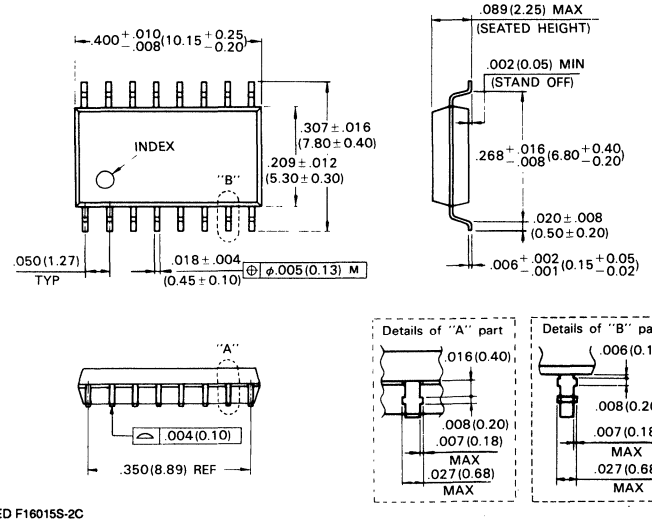
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in inches (millimeters)

FUJITSU

DATA SHEET

MB87014A

CMOS PLL Frequency Synthesizer/Prescaler

The Fujitsu MB87014A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer with an on-chip 180 MHz dual modulus prescaler.

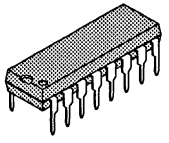
The MB87014A contains dual modulus prescaler, inverter for oscillator, programmable reference divider, control circuit, phase detectors, charge pump, programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter).

The MB87014A contains the necessary circuit to make up a PLL frequency synthesizer that operates at a speed up to 180 MHz.

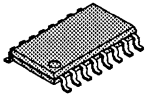
- Single power supply voltage: V_{DD} = 4.5 V to 5.5 V
- Wide temperature range: T_A = –30 to 60 °C
- 180 MHz input capability at 5 V (fin input)
- On-chip inverter for oscillator
- Programmable divider with input amplifier consisting of:
  Binary 6-bit swallow counter
  Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of binary 16-bit programmable reference counter
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is a control bit.)
- Three types of phase detector outputs:
  – On-chip charge pump output for active LPF
  – On-chip charge pump output for passive LPF
  – Output for external charge pump
- 16-pin standard dual-in-line package (Suffix: –P)
  16-pin standard flat package (Suffix: –PF)
- Pulse swallow function

$f_{VCO} = [(N \times M) + A] \times (F_{OSC} \div R)$ $(N > A)$

f_{VCO} :Output frequency of external voltage controlled oscillator (VCO)
N :Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M :Preset modulus factor of internal dual modulus prescaler (64/65)
A :Preset divide factor of binary 6-bit swallow counter (0 to 63)
f_{OSC} :Output frequency of the external oscillator
R Preset divide factor of binary 16-bit programmable reference counter (5 to 65535)

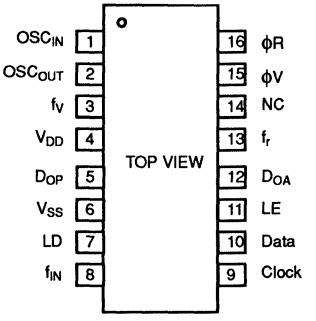


Plastic Package
DIP-16P-M04



Plastic Package
FPT-16P-M02

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.3 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.5	
Output Voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	T_A	–30 to +80	°C
Storage Temperature	T_{STG}	–40 to +125	°C
Power Dissipation	P_D	300	mW

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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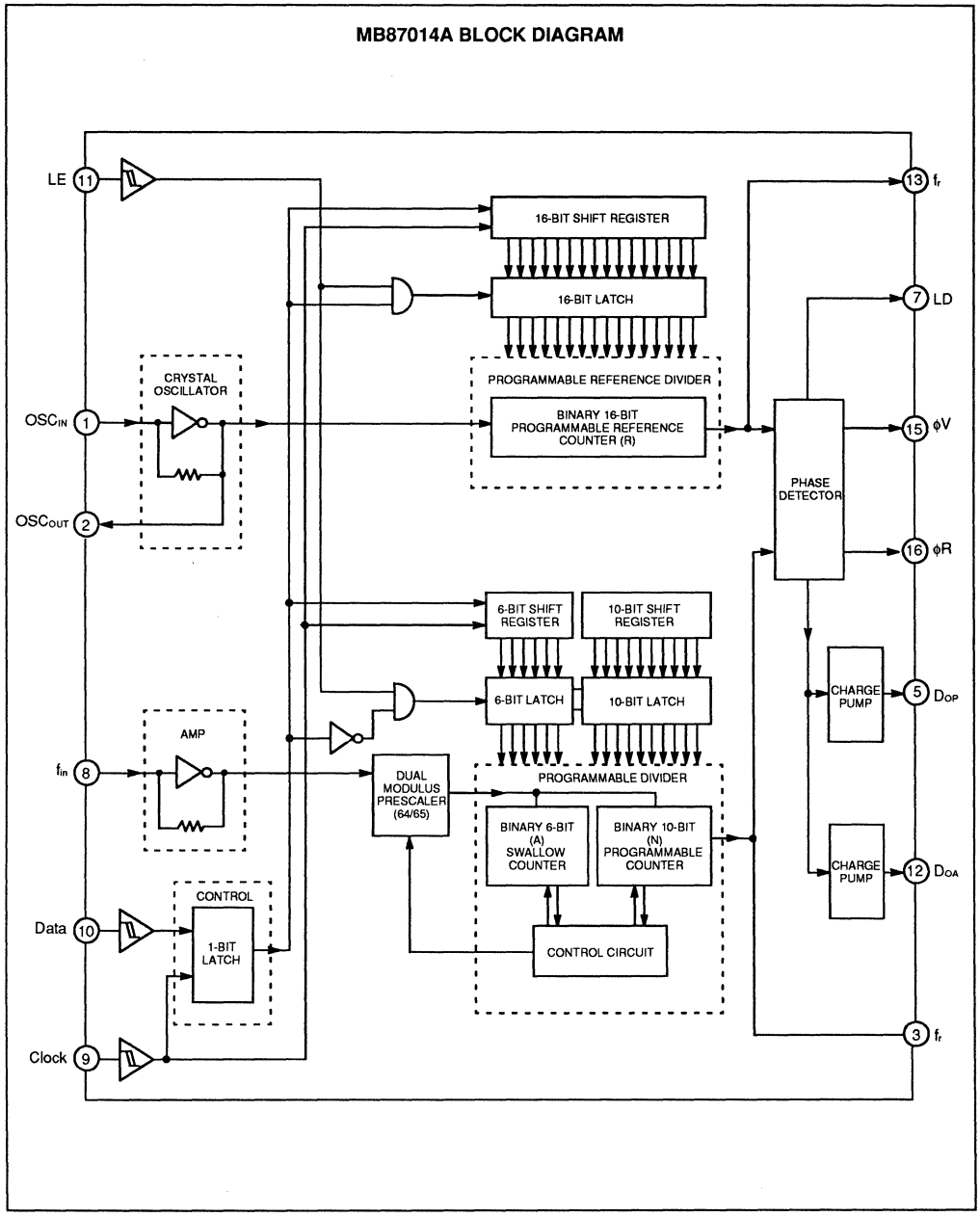
MB87014A BLOCK DIAGRAM



PIN DESCRIPTION

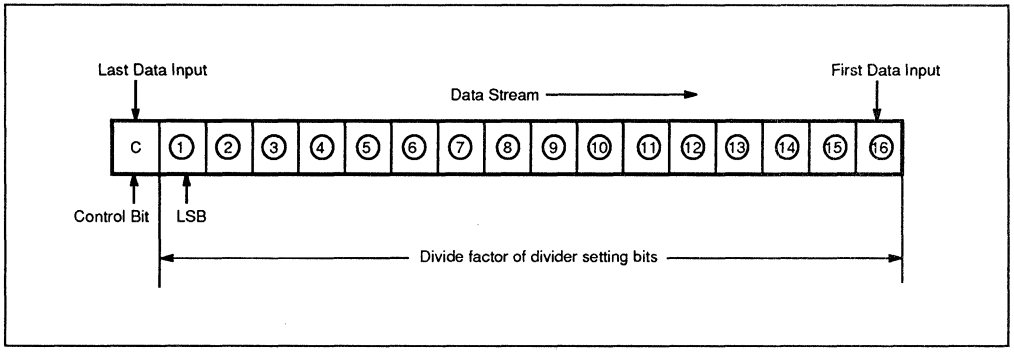
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be left open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Drive mode (D_{OP} = High level) $f_r = f_V$: High-impedance $f_r < f_V$: Sink mode (D_{OP} = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when f_r and f_V are coherent, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	f_{in}	I	Frequency input to an internal prescaler from VCO. The connection with VCO should be AC connection.
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	**Serial data input for shift registers.** **The last bit of the data is the control bit. The control data determines which latch is activated.**
11	LE	I	Load enable input. When this pin is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon a control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below: $f_r > f_V$: Sink mode (D_{OA} = Low level) $f_r = f_V$: High-impedance $f_r < f_V$: Drive mode (D_{OA} = High level)
13	f_r	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency f_r, and programmable divider output frequency f_V as listed below. ϕV / ϕR $f_r > f_V$: High level / Low level $f_r = f_V$: High level / High level $f_r < f_V$: Low level / High level

FUNCTIONAL DESCRIPTIONS

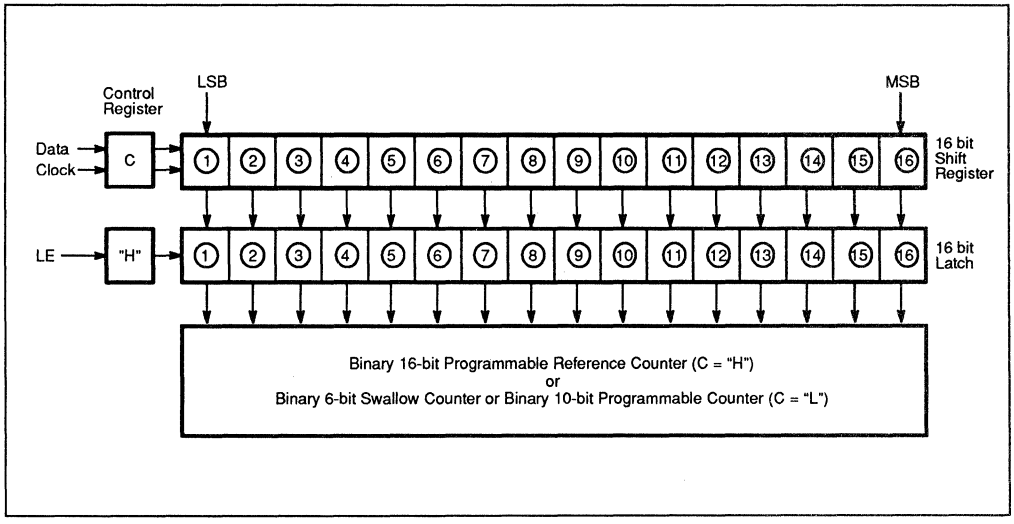
DIVIDE FACTOR OF DIVIDER

2

Binary code serial data is input to data pin. On rising edge of clock, one bit of data shifts into the shift register. Input data consists of 16-bit data and 1-bit control data. The control data determines which latch is activated. When control is high, 16-bit latch is selected; when low, 6-bit latch and 10-bit latch are selected.



The serial data is input to 16-bit shift registers and 1-bit control register. When load enable is high, the data from the shift register is latched into the programmable reference divider (binary 16-bit programmable reference counter) or programmable divider (binary 6-bit swallow counter and binary 10-bit programmable counter) depending upon a control bit setting.



FUNCTIONAL DESCRIPTIONS (Continued)

BINARY 6-BIT SWALLOW COUNTER DATA INPUT

Divide Factor	①	②	③	④	⑤	⑥
0	0	0	0	0	0	0
1	1	0	0	0	0	0
2	0	1	0	0	0	0
. .	. .	. .	. .	. .	. .	. .
63	1	1	1	1	1	1

- Divide factor A: 0 to 63

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

Divide Factor	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0
7	1	1	1	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
1023	1	1	1	1	1	1	1	1	1	1

- Divide factor N: 5 to 1023
- Divide factor less than 5 is prohibited.

BINARY 16-BIT PROGRAMMABLE COUNTER DATA INPUT

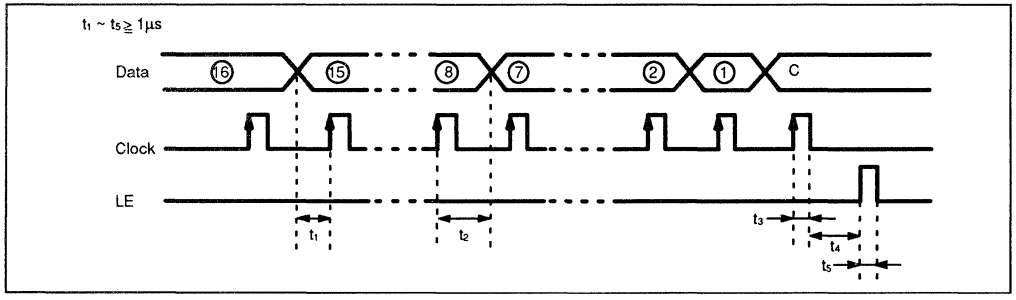
Divide Factor	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭	⑮	⑯
5	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .	. .
65535	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- Divide factor R: 5 to 65535
- Divide factor less than 5 is prohibited.

STAND-BY MODE

When zero data of 16-bit serial data is input, the MB87014 goes to stand-by mode. During stand-by mode, an internal circuit stops operation and f_{in} and OSC_{in} are forced to high level. Thus, a low supply current is achieved. Stand-by down mode is released when data other than low is input.

SERIAL DATA INPUT TIMING



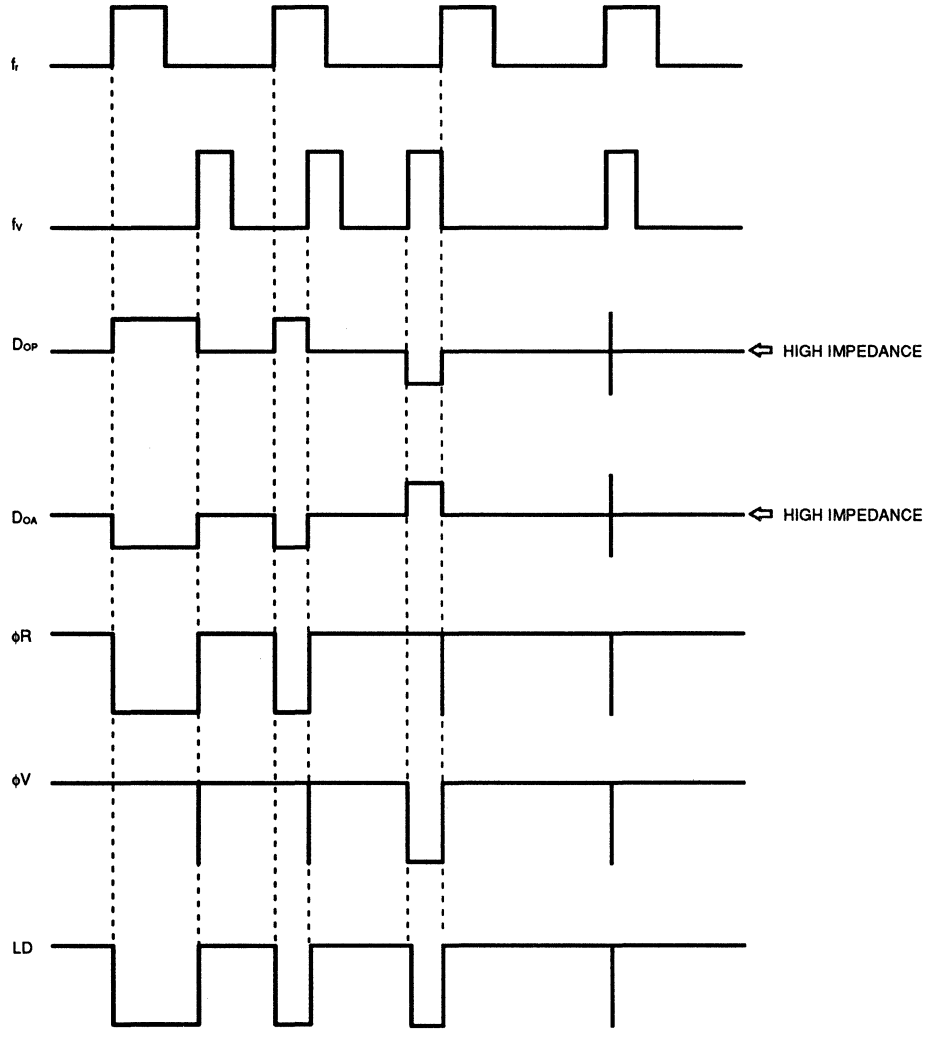
Notes: Data: Serial data input is used for setting divide factor of programmable reference divider or programmable divider
Data is input from MSB and last bit data is control bit.
Control bit is high level when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Clock input for 16-bit shift registers and control register. Data is input into internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data from shift register is latched into programmable reference divider or programmable divider depending upon the control bit setting.

2

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–30		+60	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = –30 to 60°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, Sine wave	1.0			V_{P-P}
	OSC_{IN}	V_{sin}		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$		–1.0		
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	–1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
Power Dissipation*1		I_{DDP}			8.0		mA
Stand-by Current*2		I_{DDS}			100		µA
Maximum Operating*3 Frequency	REF Section	f_{maxd}		40	60		MHz
	PD Section	f_{maxp}		180	250		MHz

Notes: *1: f_{in} = 180MHz, 22MHz cystal is connected between OSC_{IN} and OSC_{OUT} pins.
Inputs are grounded except f_{in} and OSC_{IN}. Outputs are open.

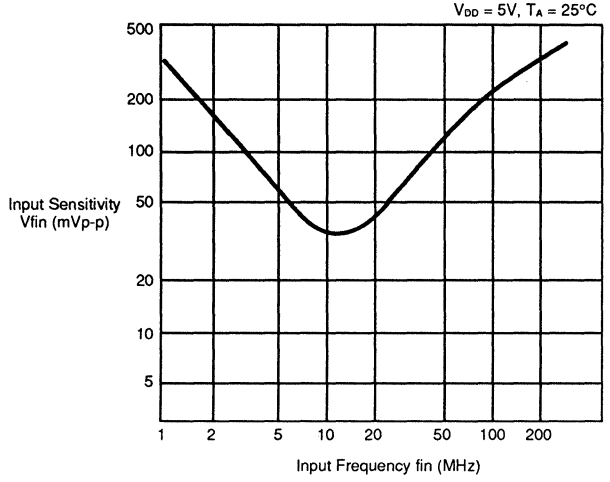
*2 All serial data is set to zero. Input are grounded except f_{in} and OSC_{IN}. Output are open.

*3 REF Section :Maximum operating frequency of programmable reference divider.
PD Section :Maximum operating frequency of programmable divider.

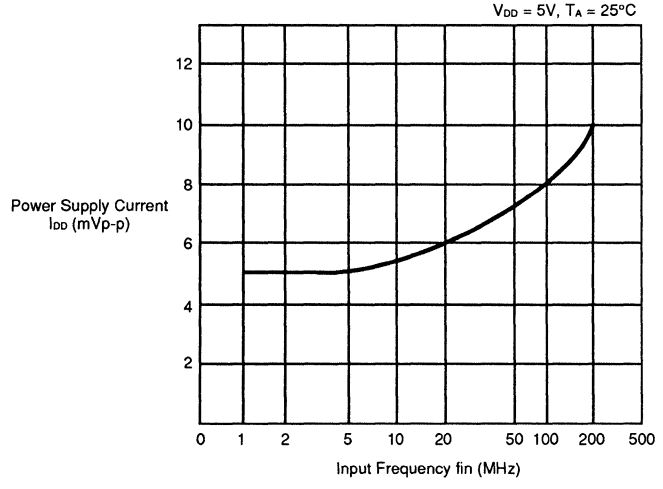
TYPICAL CHARACTERISTICS CURVES

2

Input Sensitivity vs. Input Frequency (fin Section)

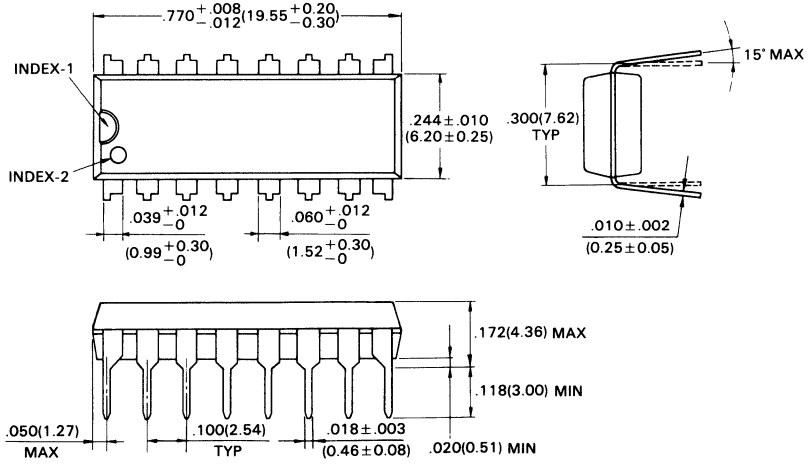


Power Supply Current vs. Input Frequency



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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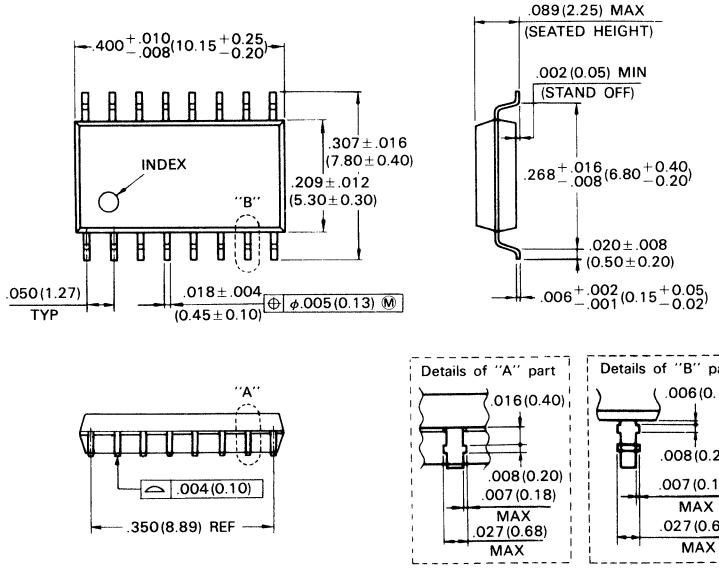
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

2

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in
inches (millimeters)

May 1990
Edition 2.0

FUJITSU

DATA SHEET

MB87076

CMOS PLL FREQUENCY SYNTHESIZER

2

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER WITH POWER DOWN MODE

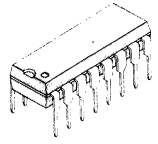
The Fujitsu MB87076, fabricated in CMOS technology, is a serial input PLL frequency synthesizer that features a power down mode.

The MB87076 contains an inverter for Oscillator, 14-bit Shift Register, 18-bit Shift Register, 1-bit Control Register, 14-bit Latch, 18-bit Latch, Programmable Divider (Binary 11-bit Programmable Counter and Binary 7-bit Swallow Counter), Programmable Reference Divider (Binary 14-bit Programmable Reference Counter), Phase Detector, Charge Pump, Control Generator for Two Modulus Prescaler, and Power Down Circuit.

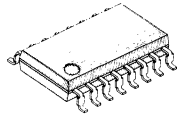
The MB87076 selects either operation mode or power down mode, depending on PS input signal level. When device begins operation, phase f_r and f_v are synchronized.

- Single Power Supply Voltage: V_{DD} = 2.7 to 5.5V
- Wide Temperature Range: T_A = –40 to 85°C
- Low Power Supply Current: 3mA typ, (100µA in power down mode)
- On-chip Inverter for Oscillator
- Programmable Reference Divider with Input Amplifier
  Programmable Divider with Input Amplifier
- 2 Types of Phase Detector Output
  On-chip Charge Pump Output
  Output for External Charge Pump
- On-chip Power Down Circuit
- 16-pin Standard Dual-in-line Package (Suffix: -P)
  16-pin Standard Flat Package (Suffix: -PF)
- Pulse Swallow Function

  f_{VCO} = [(N x M) +A] x f_{OSC} ÷ R
  f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
  N : Preset Divide Factor of Binary 11-bit Programmable Counter (16 to 2047)
  M : Preset Modulus Factor of External Two Modulus Prescaler (64 in 64/65 mode, 128 in 128/129 mode)
  A : Preset Divide Factor of Binary 7-bit Swallow Counter (0 to 127)
  f_{OSC} : Output Frequency of an External Oscillator
  R : Preset Divide Factor of Binary 14-bit Programmable Reference Counter (8 to 16383)

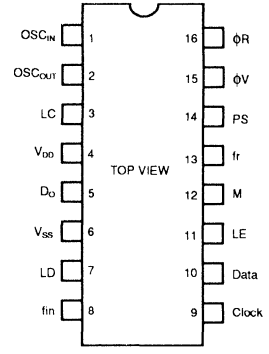


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Open Drain Output	V_{OP}	V_{SS} –0.5 to V_{DD} +3.0	V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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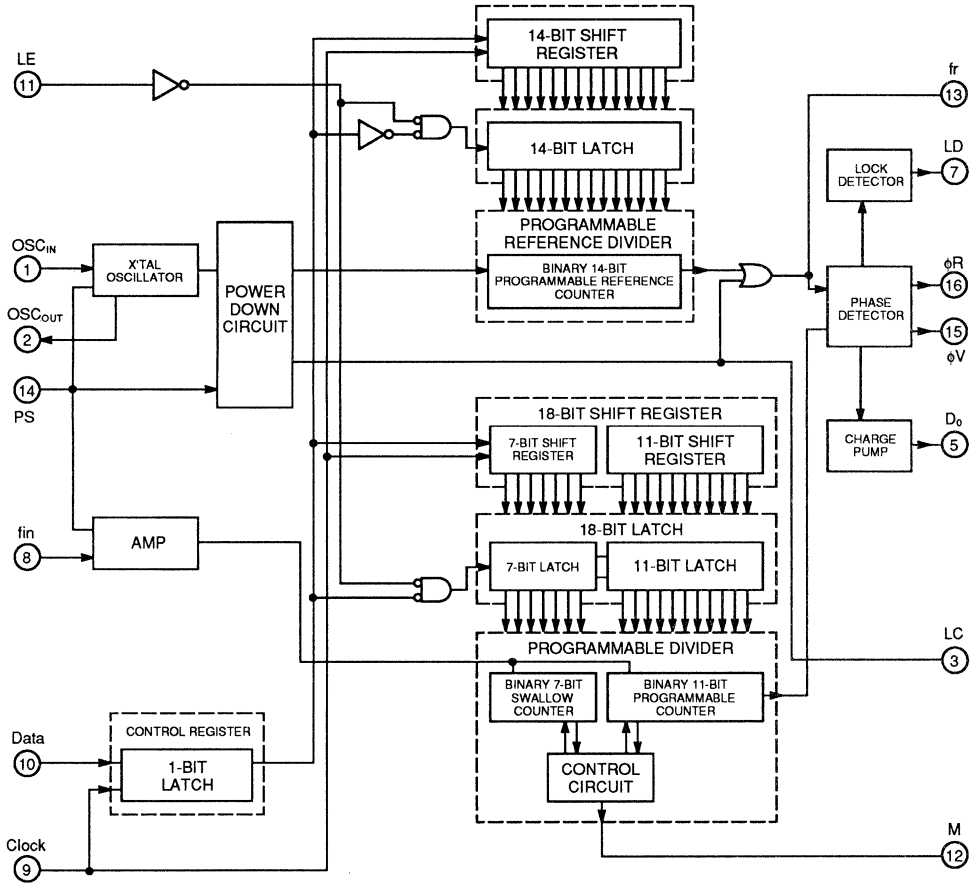
2

Fig. 1 – MB87076 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Pin for Crystal Oscillator; Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Pin for Crystal Oscillator; Output of the inverting amplifier. This pin should be connected to ground when an external oscillator is used.
3	LC	O	Output pin for Loop Control Signal; It is at high level, when operation mode is selected. It is at low level, when power down mode is selected.
4	V_{DD}	–	Power Supply Voltage
5	D_O	O	Three-state Charge Pump Output; The mode of D_O is changed by the combination of Programmable Reference Divider output frequency f_r and Programmable Divider output frequency f_P as listed below: $f_r > f_P$: D_O = H level $f_r = f_P$: D_O = High-impedance level $f_r < f_P$: D_O = L level
6	V_{SS}	–	Ground
7	LD	O	Output of Phase Comparator; It is at Low level when f_r and f_P are coherent, and then the loop is locked. Otherwise it outputs high level.
8	fin	I	Input for Binary 7-bit Swallow Counter and Binary 11-bit Programmable Counter from VCO; This input involves bias circuit and amplifier. The connection with Dual Modulus Prescaler should be AC connection.
9	Clock	I	Clock signal input for 18-bit Shift Register and 14-bit Shift Register; Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for Shift Registers. This data is the divide ratio of the divider, which is provided from the corresponded shift register. The last bit of the data is the control bit which specified destination of shift register. The data is transferred to 14-bit Shift Register when the bit is at high level, and to 18-bit Shift Register when at low level.

PIN DESCRIPTION (Continued)

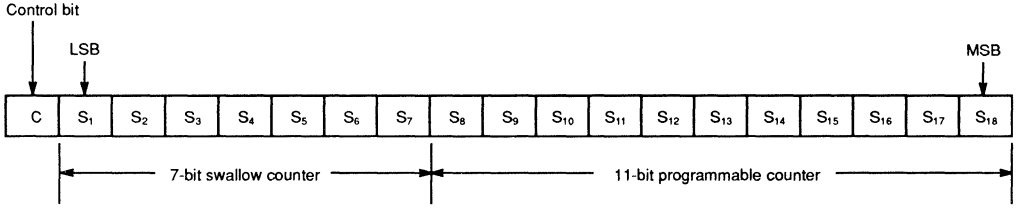
Pin No.	Symbol	I/O	Description
11	LE	I	Load Enable Input; When this pin is at high level, the data latched from the Shift Register is transferred to Programmable Reference Divider or Programmable Divider depending on the control bit data.
12	M	O	Control output for external Dual Modulus Prescaler. The connection should be DC connection. Pulse Swallow Function: (Example) MB501: M = High: Preset Modules Factor 64 or 128 M = Low: Preset Modules Factor 65 or 129
13	f_r	O	Monitors output of the phase comparator input; as well as monitoring the output of the reference divider.
14	PS	I	Power down control input; When this pin is at High level, operation mode is selected. When this pin is at Low level, power down mode is selected.
15 16	ϕV ϕR	O O	Output for external charge pump. ϕR ϕV $f_r > f_P$: Low Low $f_r = f_P$: Low High-impedance $f_r < f_P$: High High-impedance

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER

Binary serial data is input to Data pin. Each rising edge of clock shifts one bit of the data into the shift registers and control register. Input data consists of 18-bit data and 1-bit of control bit data. In this case, control bit is set at low level. S_1 to S_7 is used for setting the divide ratio of 7-bit swallow counter and S_8 to S_{18} is used for setting the divide ratio of 11 bit programmable counter.

The data format is shown below.



7-bit Swallow Counter Data Input

Divide factor A	S_7	S_6	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide factor: 0 to 127

11-bit Programmable Divider Data Input

Divide factor N	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide factor less than 5 is prohibited.
Divide factor: 5 to 2047

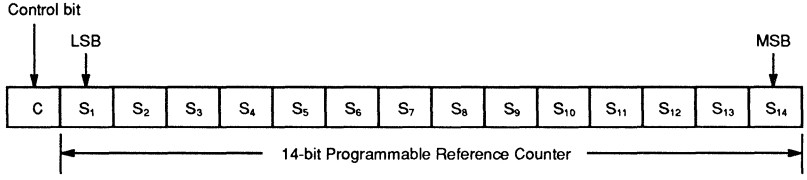
FUNCTIONAL DESCRIPTION (Continued)

SERIAL DATA INPUT FOR PROGRAMMABLE REFERENCE DIVIDER

2

Binary serial data is input to Data pin. Each rising edge of clock shifts one bit of the data into the shift registers and control register. Input data consists of 14-bit data and 1-bit of control bit data. In this case, control bit is set at high level.

The data format is shown below.

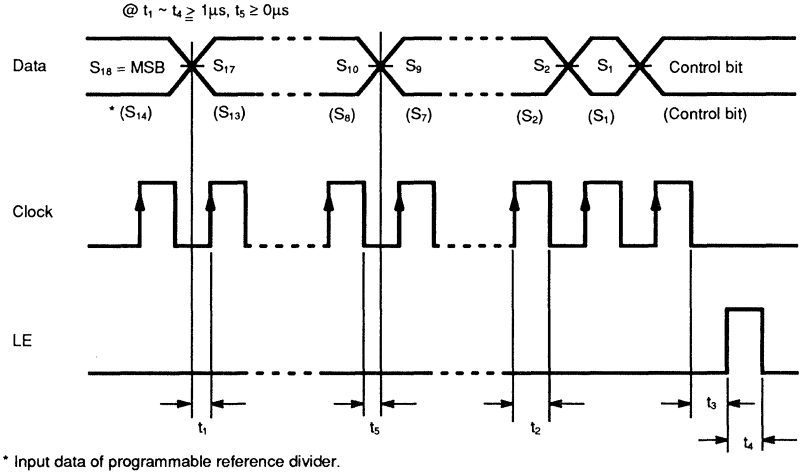


14-bit Programmable Divider Data Input

Divide factor R	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

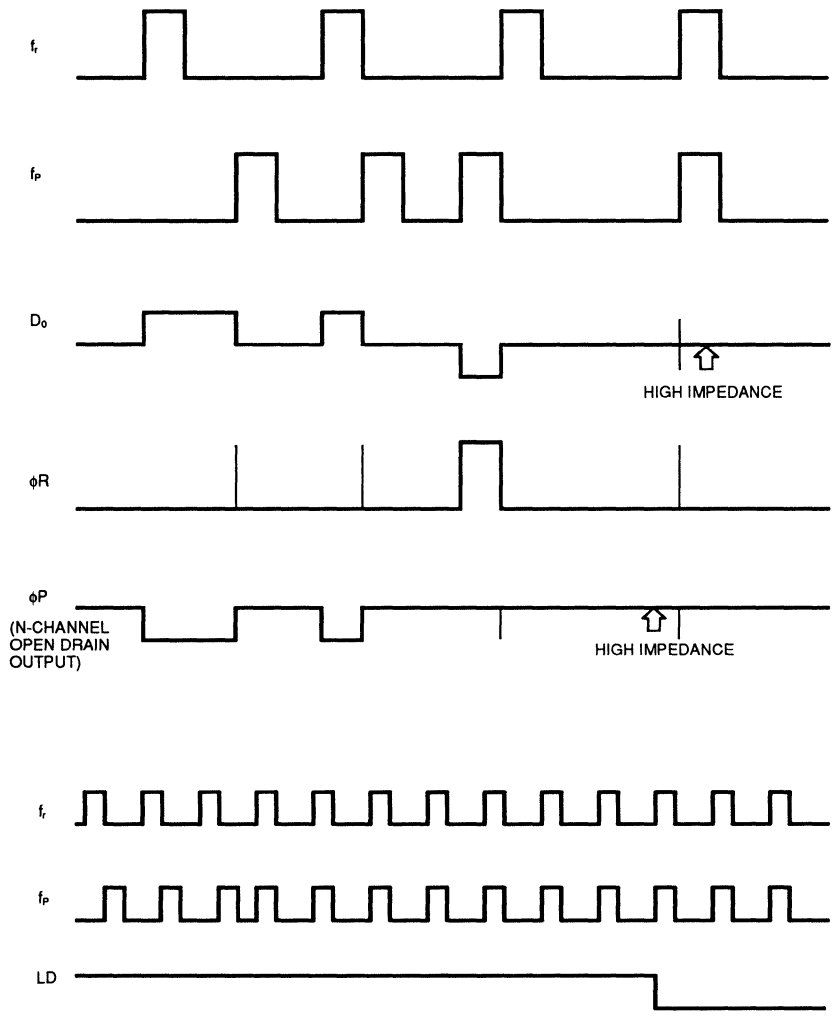
Note: Divide factor less than 8 is prohibited.
Divide factor: 8 to 16383

Fig. 2 – SERIAL DATA INPUT TIMING



* Input data of programmable reference divider.

Fig. 3 – PHASE DETECTOR WAVEFORM



Note: LD is set at High level when $f_r \neq f_v$. (Unclock condition)
LD is set at Low level when $f_r = f_v$. (Lock condition)

POWER DOWN OPERATION DESCRIPTION

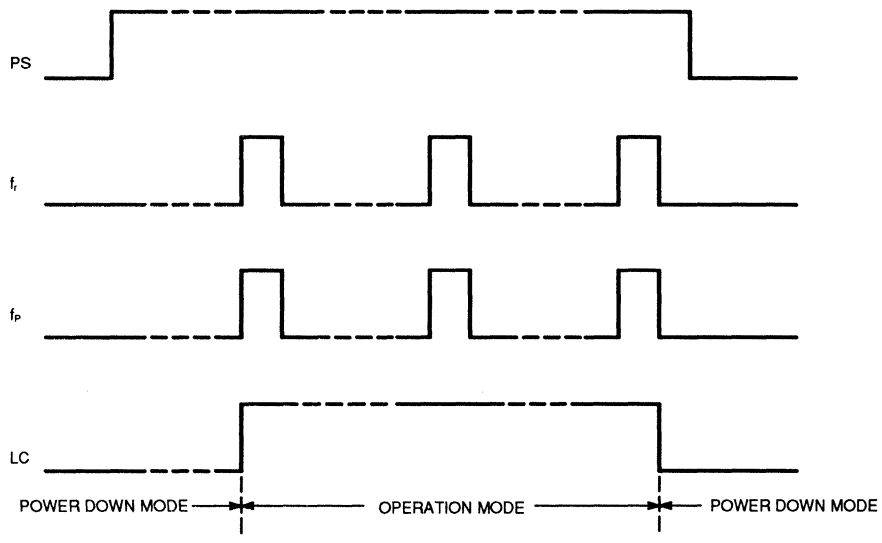
The MB87076 has power down function which selects operation mode or power down mode depending on PS input signal level.
When PS is set at low level, power down mode is selected. During power down mode, internal dividers stop operation. Thus, very low power supply consumption is achieved and LC pin is set at Low level.

Then the PS level goes High with the frequency of VCO as almost the same value as that under the condition of phase lock, the following sequence is taken.

1) Programmable divider starts operation
2) f_P is output with some delay
3) Programmable reference divider starts operation when it receives f_P.
4) f_r is output
5) LC is forced to set at High level (Normal operation mode is selected)

When the f_r outputs immediately after the f_P outputs, and goes into the phase detector, the phase lock condition is obtained just after the first clock.
When PS is set at Low level again, internal dividers stop operation. Then internal condition is reset.

Fig. 4 – POWER DOWN MODE



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Output Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		2.1			V
Low-level Input Voltage		V_{IL}				0.9	
Input Sensitivity	fin	V_{fpp}	Amplitude in AC coupling, sine wave	0.5			V_{P-P} Sine
	OSC_{IN}	V_{sin}		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		–1.0		
Input Current	fin	I_{fIN}	$V_{IN} = V_{SS}$ to V_{DD}		±30		µA
	OSC_{IN}	I_{XIN}	$V_{IN} = V_{SS}$ to V_{DD}		±30		
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	

ELECTRICAL CHARACTERISTICS (Continued)

(V_{SS} = 0V, V_{DD} = 3.0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Low-level Output Voltage	φP	V_{OLV}	I_{OL} = 0.8mA			0.80	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0μA	2.50			V
Low-level Output Voltage	OSC_{OUT}	V_{OLX}	I_{OL} = 0μA			0.50	V
High-level Output Current	Except φP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	–0.5			mA
Low-level Output Current	Except φP and OSC_{OUT}	I_{OL}	V_{OL} = 0.8V	0.5			mA
N-channel open drain Cut Off Current		I_{OFF}	V_O = V_{DD} +3.0V		1.0		μA
Power Supply Current *1		I_{DDOP}	Operation mode		2.50		mA
Power Supply Current *1		I_{DDPS}	Power down mode			80	μA
Max. Operation Frequency of Programmable Reference Divider		f_{maxd}		10	20		MHz
Max. Operation Frequency of Programmable Divider		f_{maxp}		10	20		MHz

Note: *1 fin = 8.0MHz, 11.5MHz Crystal is conneceted between OSC_{IN} and OSC_{OUT}. PS is set at high level, all other inputs are set at low level. Outputs are open.

ELECTRICAL CHARACTERISTICS (Continued)

(V_{SS} = 0V, V_{DD} = 5.0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	fin	V_{fpp}	Amplitude in AC coupling, sine wave	0.8			V_{P-P} Sine
	OSC_{IN}	V_{sin}		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		–1.0		
Input Current	fin	I_{IIN}	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	I_{XIN}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except ϕP and OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	

ELECTRICAL CHARACTERISTICS (Continued)

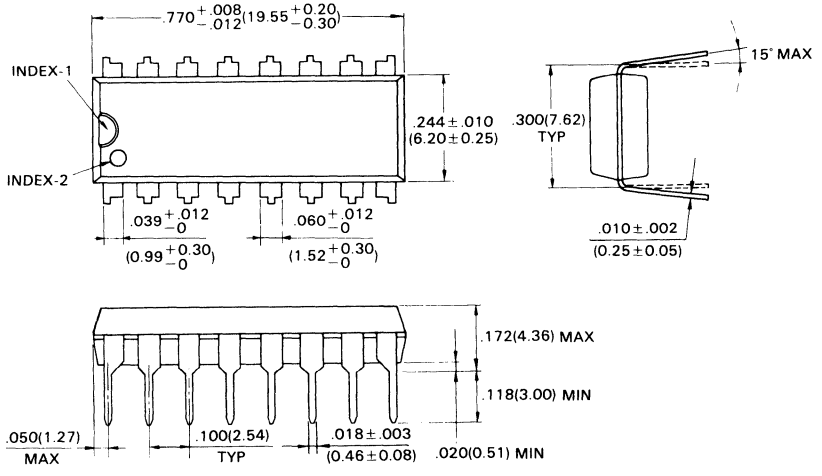
(V_{SS} = 0V, V_{DD} = 5.0V, T_A = −40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Low-level Output Voltage	φP	V_{OLV}	I_{OL} = 1mA			0.50	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0μA	4.50			V
Low-level Output Voltage	OSC_{OUT}	V_{OLX}	I_{OL} = 0μA			0.50	V
High-level Output Current	Except φP and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	−1.0			mA
Low-level Output Current	Except φP and OSC_{OUT}	I_{OL}	V_{OL} = 0.8V	1.0			mA
N-channel open drain Cut Off Current		I_{OFF}	V_O = V_{DD} +3.0V		1.0		μA
Power Supply Current *1		I_{DDOP}	Operation mode		3.0		mA
Power Supply Current *1		I_{DDPS}	Power down mode			100	μA
Max. Operation Frequency of Programmable Reference Divider		f_{maxd}		15	25		MHz
Max. Operation Frequency of Programmable Divider		f_{maxp}		10	25		MHz

Note: *1 fin = 8.0MHz, 11.5MHz Crystal is conneceted between OSC_{IN} and OSC_{OUT}. PS is set at high level, all other inputs are set at low level. Outputs are open.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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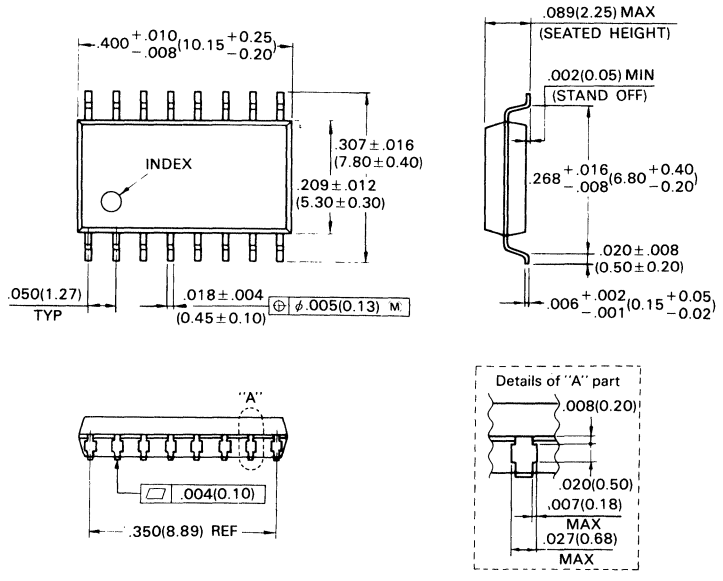
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

2

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



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Dimensions in inches (millimeters)

FUJITSU

DATA SHEET

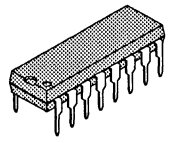
MB87086A

CMOS PLL Frequency Synthesizer/Prescaler

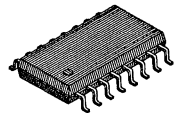
The Fujitsu MB87086A, fabricated in advanced CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer. The MB87086A contains an inverter for oscillator, programmable reference divider (binary 16-bit programmable reference counter), programmable divider (binary 10-bit programmable counter), phase detector, charge pump.

The MB87086A contains the necessary circuit to make up a PLL frequency synthesizer that operates at a speed up to 95 MHz.

- Single power supply voltage: V_{DD} = 4.5 V to 5.5 V
- Wide temperature range: T_A = –30 to 60 °C
- On-chip inverter for oscillator
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is a control bit).
- Three types of phase detector outputs:
  –On-chip charge pump output for active LPF
  –On-chip charge pump output for passive LPF
  –Output for external charge pump
- 16-pin standard dual-in-line package (Suffix: –P)
  16-pin standard flat package (Suffix: –PF)
- 95 MHz input capability at 5 V (fin input)
- fin, Clock, Data input circuits involve schmitt circuit
- The divide factor is selected according to the following equation:
  $f_{VCO} = N \times f_{OSC} \div R$
  f_{VCO} :Output frequency of external voltage controlled oscillator (VCO)
  N :Preset divide factor of programmable divider (5 to 1023)
  M :Preset modulus factor of internal dual modulus prescaler (64/65)
  f_{OSC} :Output frequency of the external oscillator
  R Preset divide factor of binary programmable reference divider (5 to 65535)

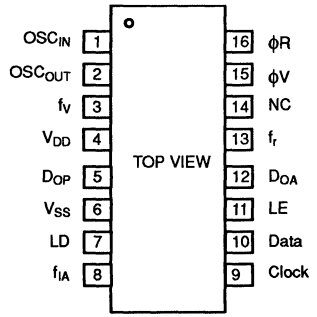


Plastic Package
DIP-16P-M04



Plastic Package
FPT-16P-M06

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.3 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Voltage	V_{OUT}	V_{SS} –0.3 to V_{DD} +0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	T_A	–30 to +80	°C
Storage Temperature	T_{STG}	–40 to +125	°C
Power Dissipation	P_D	300	mW

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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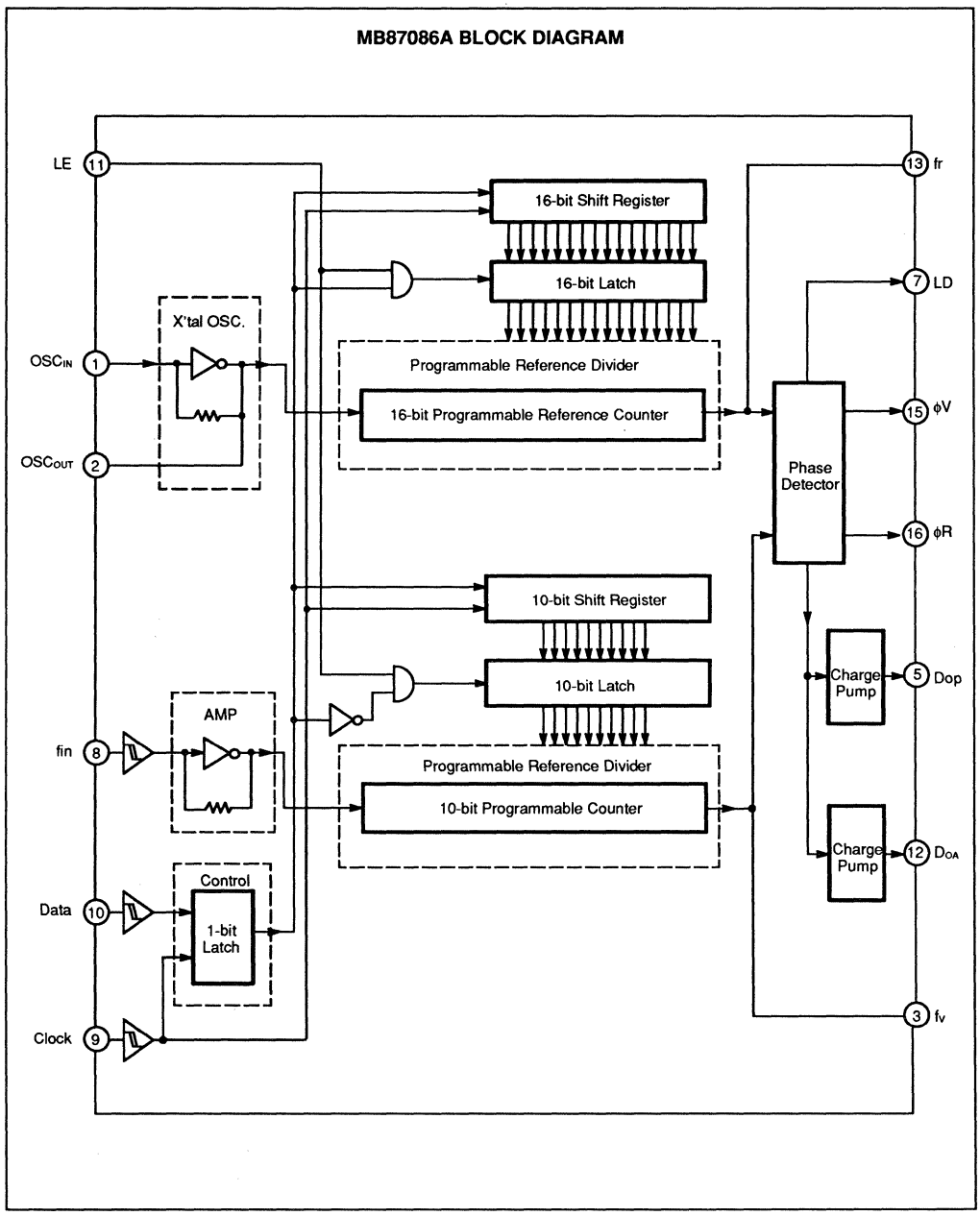
2

MB87086A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be connected to open when an external oscillator is used.
3	f_V	O	Monitor pin for the phase detector input. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_{OP}	O	Output pin for low pass filter (Passive type). The mode of D_{OP} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > f_V: Drive mode (D_{OP} – High level) fr = f_V: High-impedance fr < f_V: Sink mode (D_{OP} = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are coherent, and when the loop is locked. Otherwise it outputs low pulse signal.
8	fin	I	Frequency input to programmable divider from VCO or prescaler output. (This input has an internal feed back resistor.)
9	Clock	I	Clock signal input for shift registers. Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	I	Serial data input for shift registers. The last bit of the data is the control bit. The control data determines which latch is activated.
11	LE	I	Load enable input. When this pin is high level, the data stored in the shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.
12	D_{OA}	O	Output pin for low pass filter (Active type). The mode of D_{OA} is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: fr > f_V: Drive mode (D_{OA} – Low level) fr = f_V: High-impedance fr < f_V: Sink mode (D_{OA} = High level)
13	fr	O	Monitor pin for the phase detector input. This pin is tied to the programmable reference divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output pins for low pass filter (differential filter type). Outputs for external charge pump are changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below. ϕV / ϕR fr > f_V: High level / Low level fr = f_V: High level / High level fr < f_V: Low level / High level

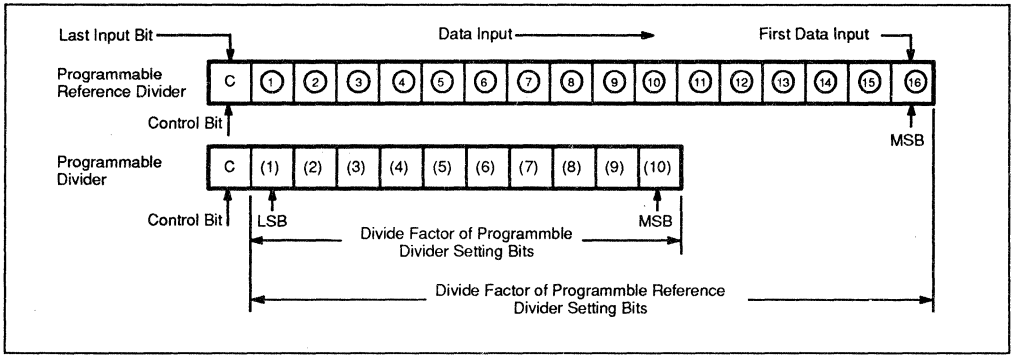
FUNCTIONAL DESCRIPTIONS

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

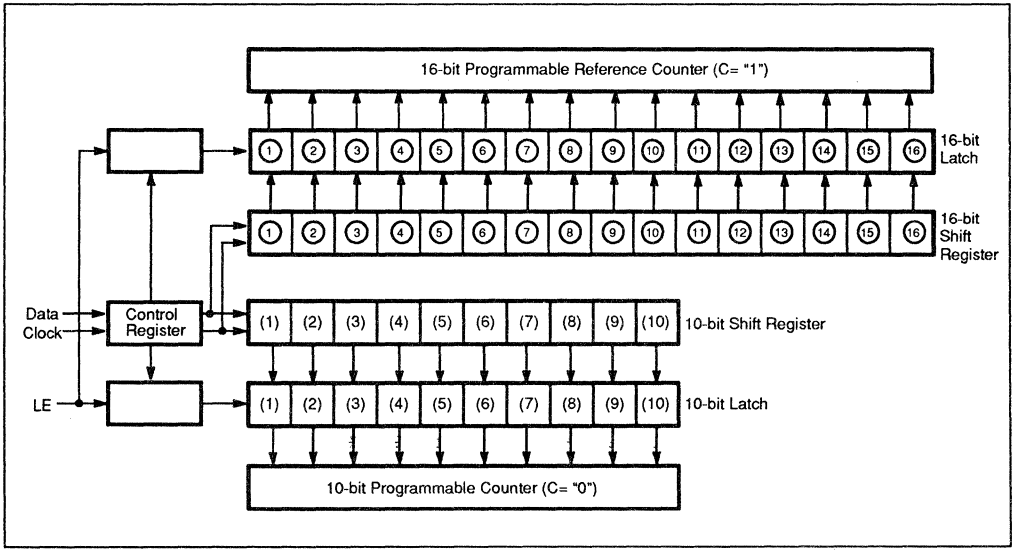
Binary code serial data is input to data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 16-bit or 10-bit data and 1-bit of control bit data. The 16-bit data is used for setting the divide factor of programmable reference divider. The 10-bit data is used for setting the divide factor of programmable divider.

The last bit of the data stored in control register is a control bit. Control data determines which latch is activated. When this bit is at high level, 16-bit latch is selected; when this is at low level, 10-bit latch is selected.

The data format is shown below.



When LE is high level and control bit is high level, the data stored in 16-bit shift register is transferred to 16-bit latch. When LE is high level and control bit is at low level, the data stored in 10-bit shift register is transferred to 10-bit latch.



BINARY 10-BIT PROGRAMMABLE DIVIDER DATA INPUT

(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	Divide Factor
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

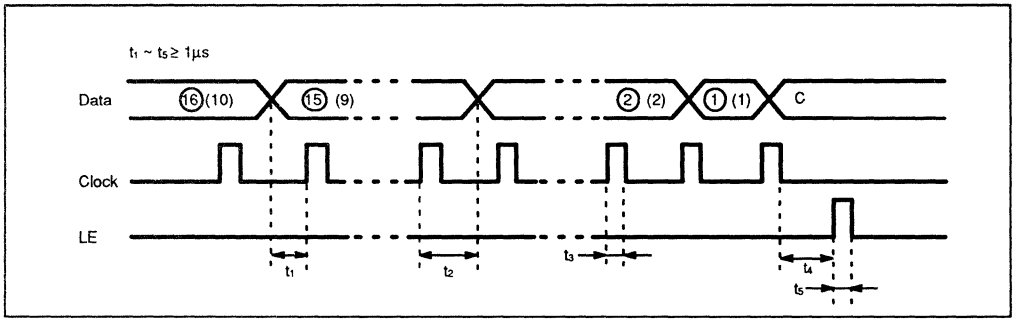
Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 1023

BINARY 16-BIT PROGRAMMABLE REFERENCE DIVIDER DATA INPUT

⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65535

Note: Divide factor less than 5 is prohibited.
Divide factor R: 5 to 65535

SERIAL DATA INPUT TIMING



Notes: ○ Data input for programmable reference divider.

( ) Data input for programmable divider.

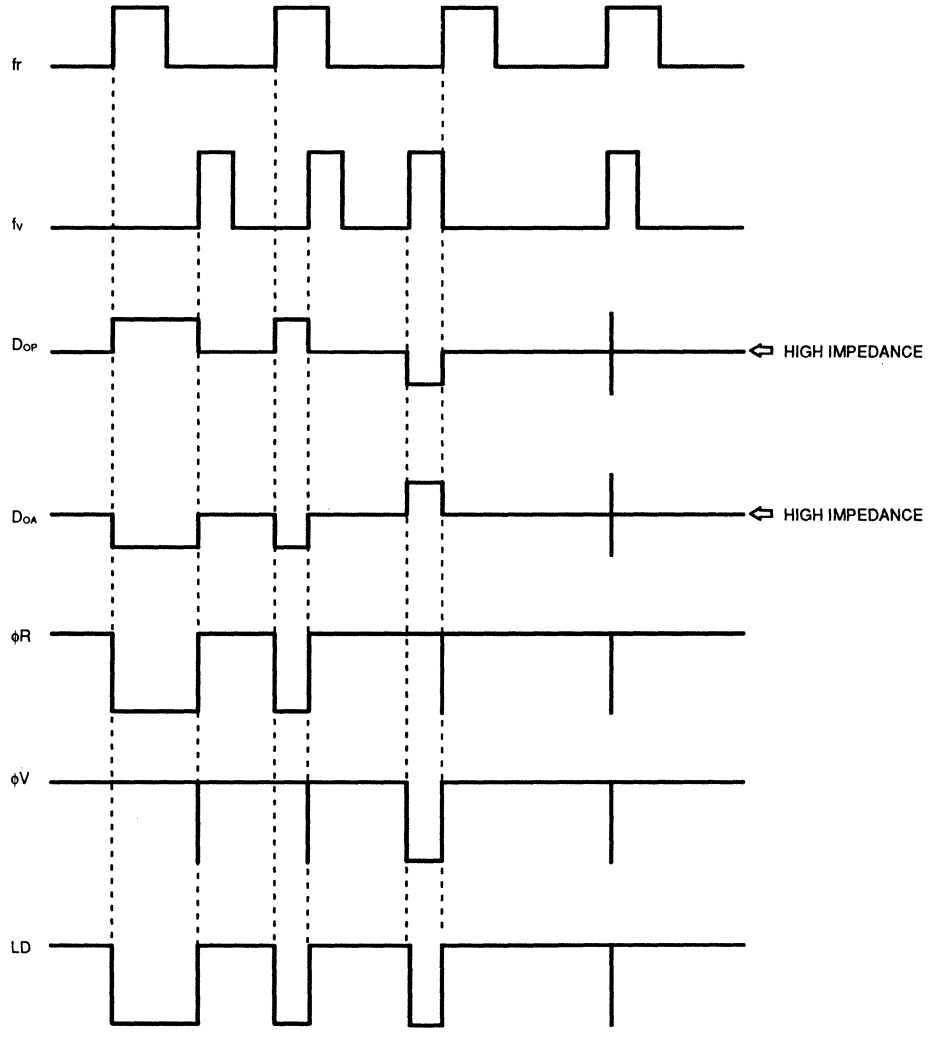
Data Serial data input is used for setting divide factor of programmable reference divider or programmable divider.
Data is input from MSB and last bit data is control bit.
Control bit is set at high level when divide factor of programmable reference divider is set. Control bit is set at low level when divide factor of programmable divider is set.

Clock Clock input for 10-bit shift register, 16-bit shift register and control register. Data is input into internal shift registers by rising edge of the clock.

LE Load enable input:
When LE is high level, the data stored in shift registers is transferred to 16-bit latch, or 10-bit latch depending on the control bit setting.

2

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–30		+60	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = –30 to 60°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	fin	Vfpp	Amplitude in AC coupling, Sine wave	1.0			V_{P-P}
	OSC_{IN}	Vsin		1.0			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	$V_{IH} = V_{DD}$		1.0		µA
Low-level Input Current		I_{IL}	$V_{IL} = V_{SS}$		–1.0		
Input Current	fin	Ifin	$V_{IN} = V_{SS}$ to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	–1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
Power Dissipation*1		I_{DD}			8.0		mA
Maximum Operating*2 Frequency	REF Section	fmaxd		40	60		MHz
	PD Section	fmaxp		95	130		MHz

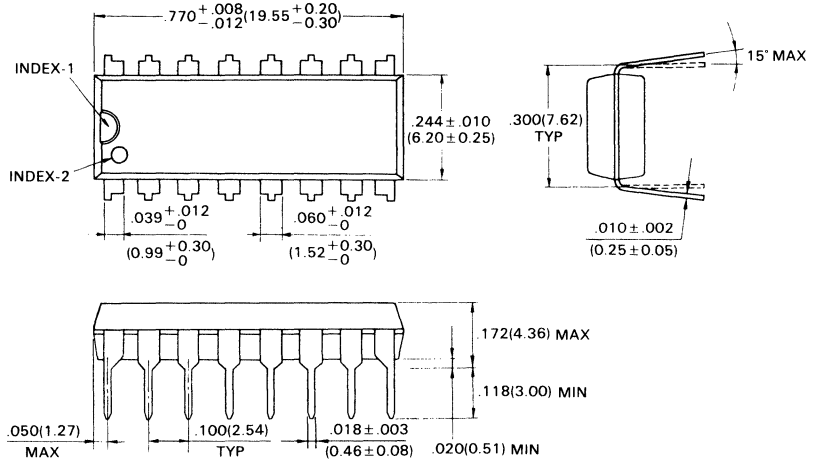
Notes: *1: fin 100MHz, 22MHz cystal is connected between OSC_{IN} and OSC_{OUT} pins.
Inputs are grounded except fin and OSC_{IN}. Outputs are open.

*2 REF Section: Maximum operating frequency of programmable reference divider.
PD Section: Maximum operating frequency or programmable divider.

PACKAGE DIMENSIONS

2

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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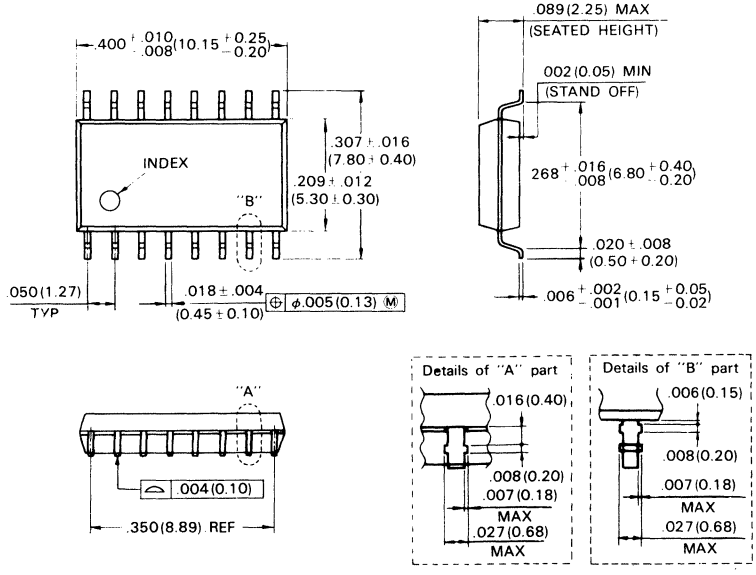
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in
inches (millimeters)

2

January 1991
Edition 3.0

FUJITSU

DATA SHEET

MB87087
CMOS PLL FREQUENCY SYNTHESIZER

2

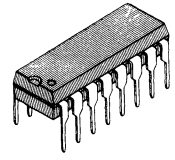
CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87087, fabricated in CMOS technology, is a serial input phase locked loop (PLL) frequency synthesizer.

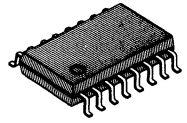
The MB87087 contains an inverter for oscillator, programmable reference divider (binary 14-bit programmable reference counter), 14-bit shift register, 14-bit latch, phase detector, charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter) and control generator for dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87087 contains the necessary circuit to make up a PLL frequency synthesizer. Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

- Wide range power supply voltage: V_{CC} = 3.0 to 6.0 V
- Wide temperature range: T_A = −40 to 85 °C
- 17 MHz typical input capability at 5 V (fin input)
- Programmable divider with input amplifier consisting of:
  –Binary 7-bit swallow counter
  –Binary 10-bit programmable counter
- Programmable reference divider with input amplifier consisting of binary 14-bit programmable reference counter
- On-chip inverter for oscillator
- Divide factor of programmable divider and programmable reference divider are set by serial data input. (The last data bit is control bit.)
- Two types of phase detector output:
  –On-chip charge pump output
  –Output for external charge pump
- Easy interface with Fujitsu prescalers
- 16-pin standard dual-in-line package (MB87087P)
  16-pin standard flat package (MB87087PF)

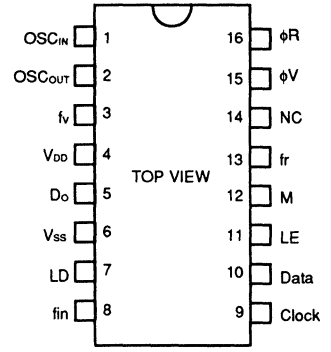


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} −0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} −0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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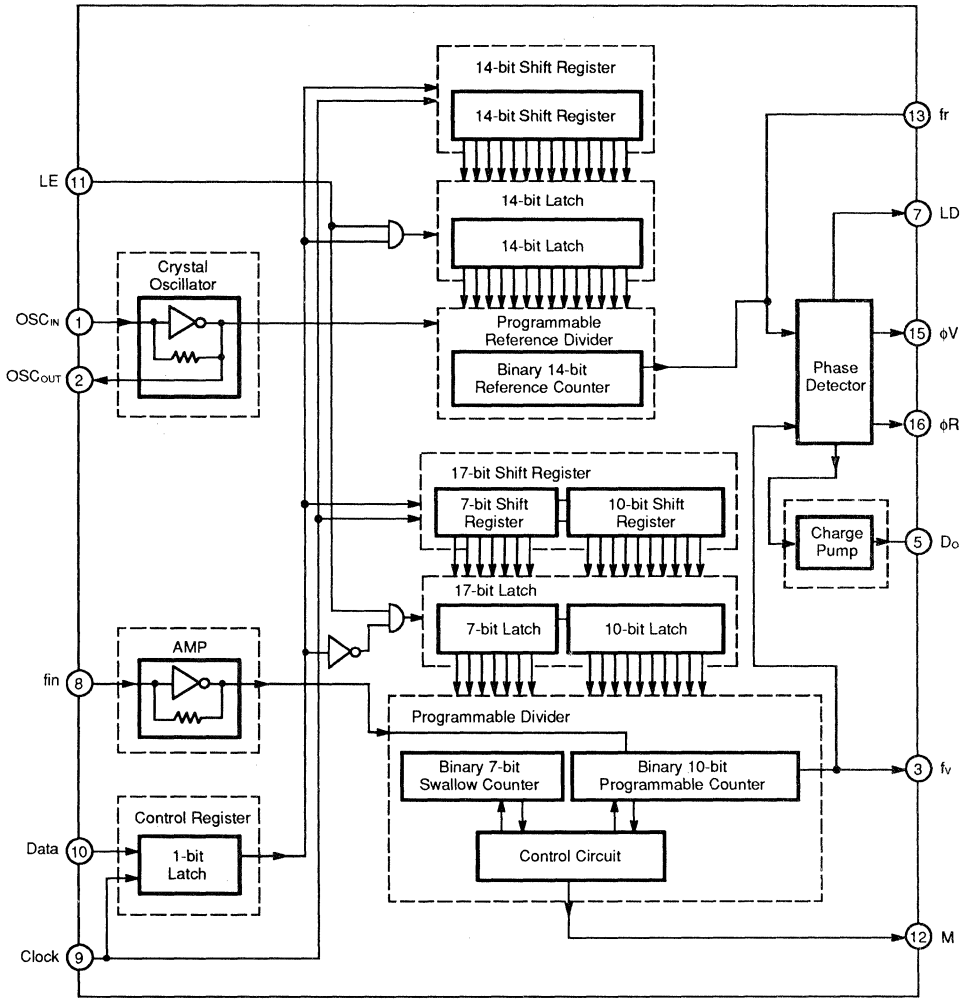
2

MB87087 BLOCK DIAGRAM



PIN DESCRIPTION

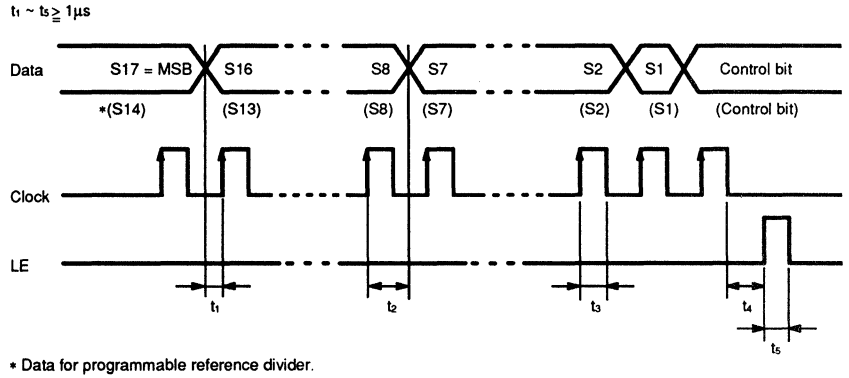
Pin No.	Symbol	I/O	Description
1	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	O	Monitor output of the phase detector. This pin is tied to the programmable divider output.
4	V_{DD}	–	Power supply voltage input.
5	D_O	O	Three-state charge pump output of phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency fr, and programmable divider output frequency f_V as listed below: $fr > f_V$: Drive mode (D_O = High level) $fr = f_V$: High impedance $fr < f_V$: Sink mode (D_O = Low level)
6	V_{SS}	–	Ground.
7	LD	O	Output of phase detector. It is high level when fr and f_V are equal, and when the loop is locked. Otherwise it outputs negative pulse signal.
8	fin	I	Clock input for programmable divider. This input contains internal bias circuit and amplifier. The connection with an external dual-modulus prescaler should be an AC connection.
9	Clock	I	Clock signal input for 17-bit shift register and 14-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift registers.
10	Data	I	Serial data input for programmable divider and programmable reference divider. The last bit of the data is the control bit. Control bit determines which latch is activated. The data stored in the shift register is transferred to the 14-bit latch when the bit is high, and to 17-bit latch when low.
11	LE	I	Load enable input with internal pull up resistor. When this pin is high (active high), the data stored in shift register is transferred to 14-bit latch or 17-bit latch depending on the control bit data.
12	M	O	Control output for an external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of input signal fin (pin #8). Pulse swallow function: e.g. MB501L: M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 to 129

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description
13	fr	O	Monitor output of phase detector input. This pin is tied to the programmable divider output.
14	NC	–	No connection.
15 16	ϕV ϕR	O O	Output for external charge pump. The mode of ϕR and ϕV is changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency f_V as listed below. ϕR ϕV fr > f_V: Low-level High-level fr = f_V: High-level High-level fr < f_V: High-level Low-level

FUNCTIONAL DESCRIPTION

SERIAL DATA INPUT TIMING



* Data for programmable reference divider.

Notes: Data: Serial data input is used for setting divide factor of programmable reference divider and programmable divider. Data is input from MSB, and last bit data is a control bit.
Control bit is set high when divide factor of programmable reference divider is set. Control bit is set low level when divide factor of programmable divider is set.

Clock: Data is input to internal shift registers by rising edge of the clock.

LE: Load enable input:
When LE is high, the data stored in shift register is transferred to 14-bit latch, or 17-bit latch depending on the control bit setting.

PULSE SWALLOW FUNCTION

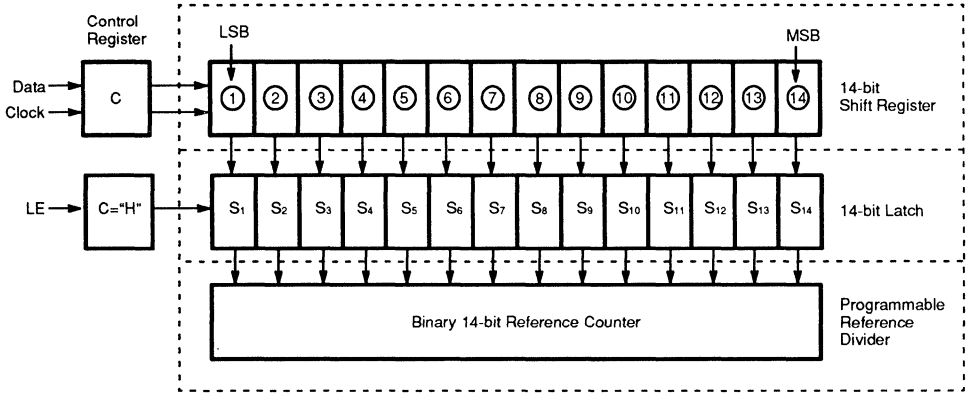
$$f_{VCO} = [(N \times M) + A] \times f_{OSC} \div R \quad (N > A)$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler
(e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit programmable counter (0 to 127, A < N)
f_{OSC} : Output frequency of external oscillator
R : Preset divide factor of binary 14-bit programmable reference counter (5 to 16383)

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

Serial data consists of 14-bit data, which is used for setting divide factor of programmable reference counter, and 1-bit control data. In this case, control bit is set high level.

The data format is shown below.



BINARY 14-BIT REFERENCE COUNTER DATA INPUT

⑭	⑬	⑫	⑪	⑩	⑨	⑧	⑦	⑥	⑤	④	③	②	①	Divide Factor
0	0	0	0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1	1	1	1	16383

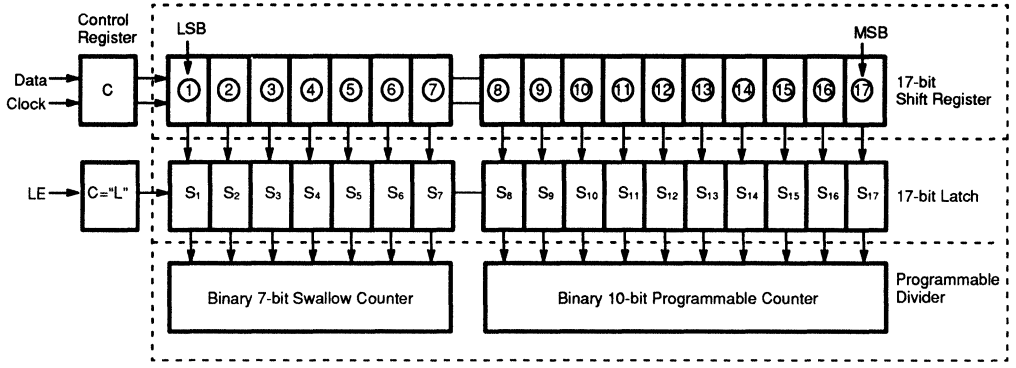
Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 16383

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data consists of 17-bit data, which is used for setting divide factor of programmable divider, and 1-bit control data. In this case, control bit is set low level. The data ① to ⑦ set a divide factor of 7-bit swallow counter and data ⑧ to ⑰ set divide factor of 10-bit programmable counter.

2

The data format is shown below.



BINARY 7-BIT SWALLOW COUNTER DATA INPUT

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

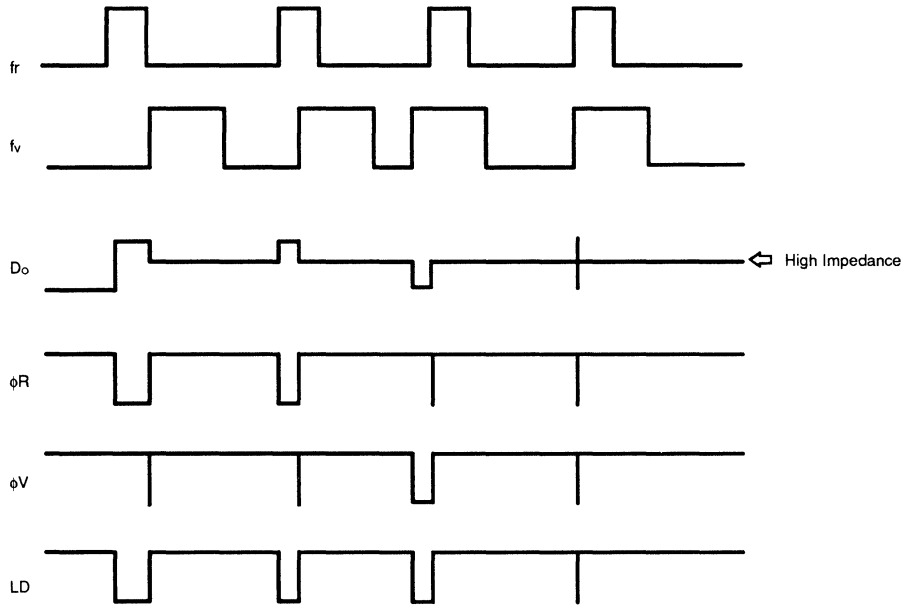
Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
e.g. MB501L (÷65/65)prescaler
SW = H (64/65): Bit 7 to shift register ⑦ should be zero.

BINARY 10-BIT PROGRAMMABLE COUNTER DATA INPUT

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited.
Divide factor N : 5 to 1023

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	3.0		6.0	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	V_{OSC}		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		–1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±30		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±30		µA
	LE	I_{LE}	V_{IN} = V_{SS}		–40		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 2.6V	–0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	0.5			
High-level Output Current	M	I_{OHM}	V_{OH} = 2.6V	–0.7			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	1.5			
Power Supply Current *1		I_{DD}			2.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	20		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		10	20		MHz

Notes: *1: fin = 8.0MHz 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except fin and OSC_{IN}. Output are open.

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = −40 to 85°C)

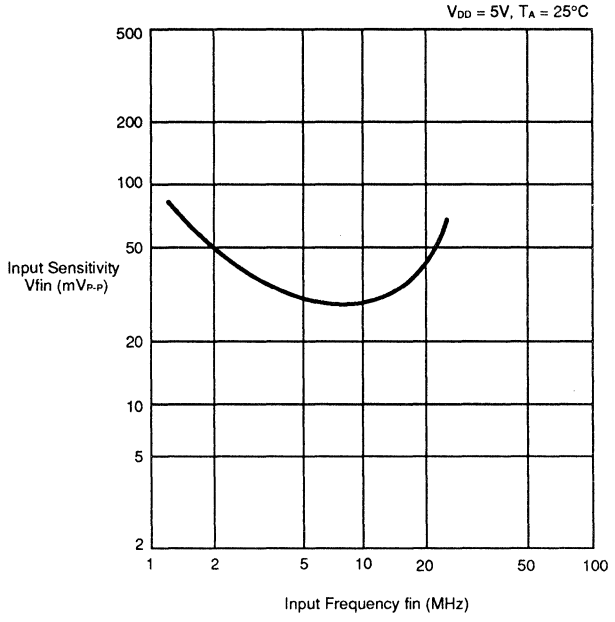
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{DD}x0.7			V
Low-level Input Voltage		V_{IL}				V_{DD}x0.3	
Input Sensitivity	fin	Vfin	Amplitude in AC coupling, sine wave	0.5			V_{P-P}
	OSC_{IN}	V_{OSC}		0.5			
High-level Input Current	Except fin and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}		1.0		µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}		−1.0		
Input Current	fin	Ifin	V_{IN} = V_{SS} to V_{DD}		±50		µA
	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}		±50		µA
	LE	I_{LE}	V_{IN} = V_{SS}		−60		µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA			0.05	
High-level Output Current	Except M and OSC_{OUT}	I_{OH}	V_{OH} = 4.6V	−1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.4V	1.0			
High-level Output Current	M	I_{OHM}	V_{OH} = 4.6V	−1.5			mA
Low-level Output Current		I_{OLM}	V_{OL} = 0.4V	3.0			
Power Supply Current *1		I_{DD}			3.5		mA
Maximum Operating Frequency of Programmable Reference Divider		fmaxd		10	25		MHz
Maximum Operating Frequency of Programmable Divider		fmaxp		17	25		MHz

Note: *1. fin = 8.0MHz, 11.5MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are grounded except fin and OSC_{IN}. Outputs are open.

TYPICAL CHARACTERISTICS CURVE

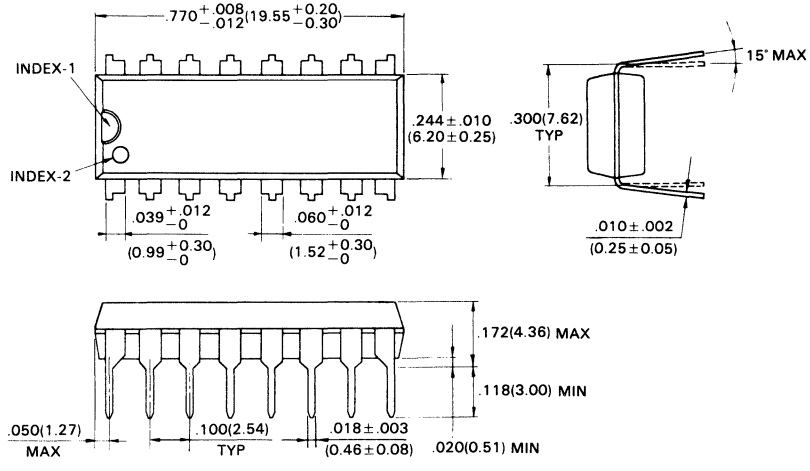
2

Input Sensitivity vs. Input Frequency (fin Section)



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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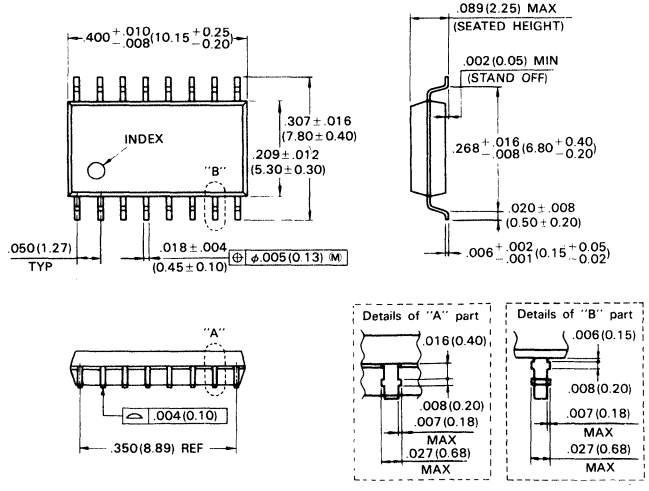
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

2

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in inches (millimeters)

April 1991
Edition 4.0

FUJITSU

DATA SHEET

MB87090

CMOS PLL FREQUENCY SYNTHESIZER

2

CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER WITH CONSTANT CURRENT OUTPUT CHARGE PUMP

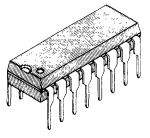
The Fujitsu MB87090, fabricated in CMOS technology, is a serial input PLL frequency synthesizer with constant current output charge pump.

The MB87090 contains an inverter for oscillator, programmable reference divider, divide factor of programmable reference divider control circuit, phase detector, constant current output charge pump, 17-bit shift register, 17-bit latch, programmable divider (binary 7-bit swallow counter, binary 10-bit programmable counter), and a control generator for an external dual modulus prescaler.

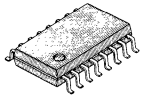
When supplemented with a loop filter and VCO, the MB87090 contains the necessary circuit to make up a PLL frequency synthesizer.

Unique to this device is a constant current output charge pump. This allows improved modulation characteristics, tracking and noise performance compared to earlier devices.

- Constant current output charge pump. Magnitude of current controlled by external resistor: 0 to 4 mA.
- 13MHz input capability @5V (fin input)
- Single power supply voltage: V_{DD} = 2.7V to 5.5V
- Wide temperature range: T_A = –40 to 85°C
- On-chip inverter for oscillator
- **Eight divide factors for programmable reference divider are selected by external input S_1, S_2, and S_3 (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)**
- Programmable 17-bit divider with input amplifier consisting of:
  Binary 7-bit swallow counter
  Binary 10-bit programmable counter
- Easy interface to Fujitsu dual modulus prescalers.
- 16-pin standard dual-in-line package (Suffix: -P)
  16-pin standard flat package (Suffix: -PF)

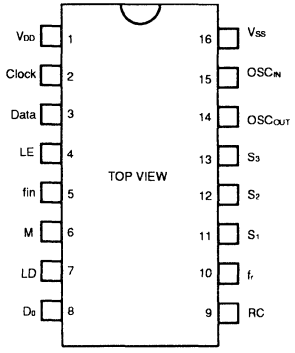


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE) (V_{SS} = 0V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS} –0.5 to V_{SS} +7.0	V
Input Voltage	V_{IN}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Voltage	V_{OUT}	V_{SS} –0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	±10	mA
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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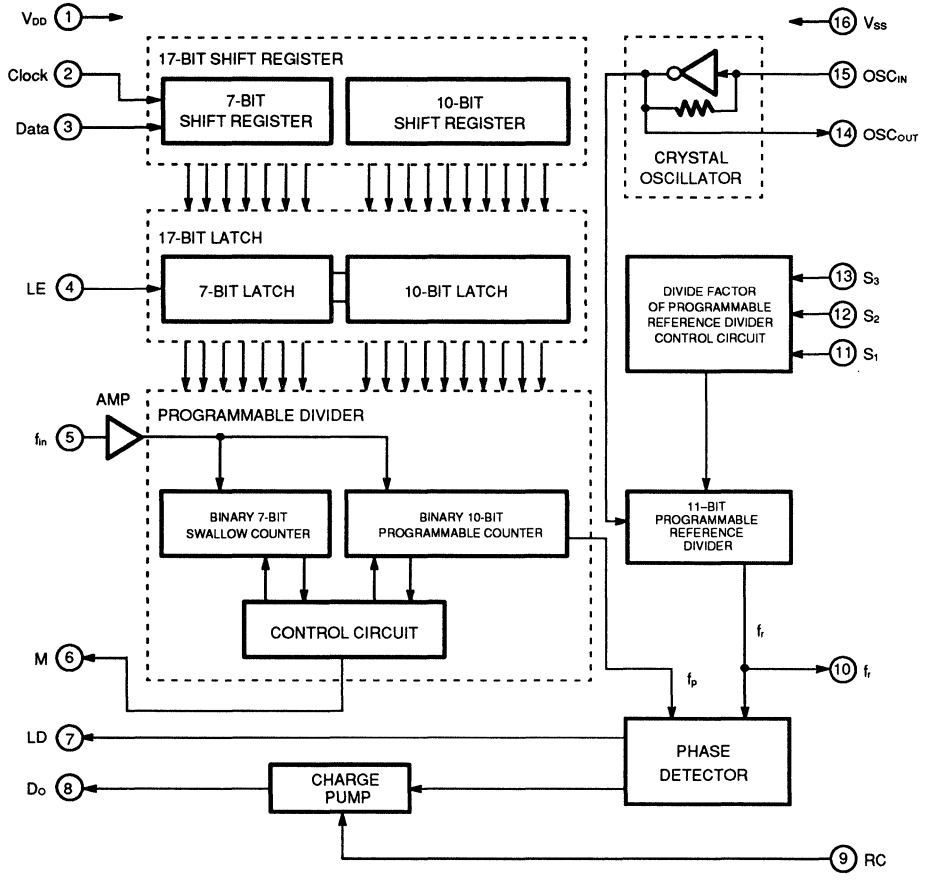
2

Fig. 1 – MB87090 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_{DD}	–	Power supply voltage input.
2	Clock	I	Clock signal input for 17-bit shift register. Each rising edge of the clock shifts one bit of the data into the shift register.
3	Data	I	Serial data input for 17-bit shift register. This data is used for setting the divide factor of programmable divider.
4	LE	I	Load enable input. When this pin is high level (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
5	fin	I	Input for programmable divider from VCO or prescaler output. This input involves bias circuit and amplifier. The connection with external dual modulus prescaler should be an AC connection.
6	M	O	Control output for external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #5). Pulse Swallow Function: MB501L M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 or 129
7	LD	O	Output of phase detector. It is high level when f_r and f_p are equal, and then the loop is locked. Otherwise it outputs negative pulse signal.
8	D_O	O	Three-state charge pump output of the phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency f_r and programmable divider output frequency f_p as listed below: $f_r > f_p$: Drive mode (D_O = High level) $f_r = f_p$: High-impedance mode $f_r < f_p$: Sink mode (D_O = Low level)
9	RC	I	The value of external resistor connected to this pin determines the magnitude of the current delivered by the charge pump. See graph on page 10.
10	f_r	O	This pin is tied to programmable reference divider output.
11 12 13	S_1 S_2 S_3	I I I	Control input for programmable reference divider. The combination of these inputs provides divide factor to programmable reference divider. See following page.
14	OSC_{OUT}	O	Pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
15	OSC_{IN}	I	Pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
16	V_{SS}	–	Ground

FUNCTIONAL DESCRIPTION

DIVIDE FACTOR OF PROGRAMMABLE REFERENCE DIVIDER

2

Divide factor of programmable reference divider is set depending on input dignal S_1 to S_3.

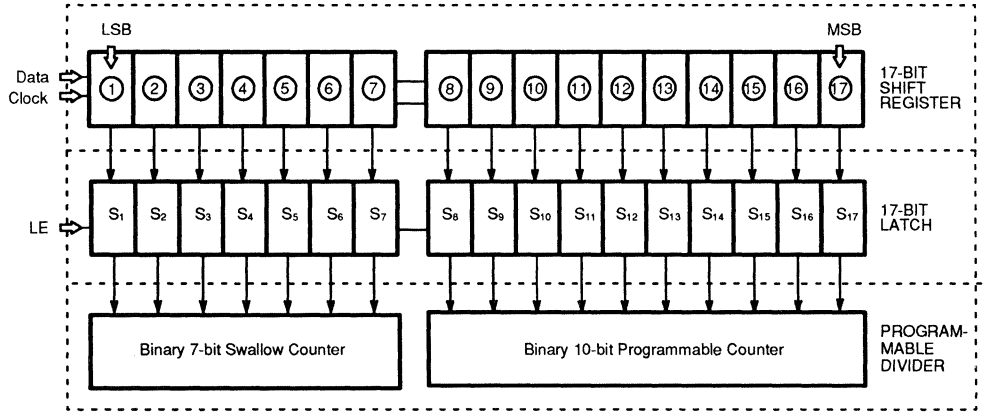
S_n	1/8	1/16	1/64	1/128	1/256	1/512	1/1024	1/2048
S_1	0	1	0	1	0	1	0	1
S_2	0	0	1	1	0	0	1	1
S_3	0	0	0	0	1	1	1	1

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to Data pin. These data are loaded into the 17-bit shift register from MSB. When load enable signal LE is high, the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The data ① to ⑦ set a divide factor of the binary 7-bit swallow counter and data ⑧ to ⑰ set a divide factor of binary 10-bit programmable counter. In other words, serial data is **equivalent to the divide factor of programmable divider.**

Fig. 2 – BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER



Binary 7-bit Swallow Counter Data Input

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127

Note: Divide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
Example MB501L
SW = H (64/65): Bit 7 of shift register (7) should be zero.

Binary 10-bit Programmable Counter Data Input

⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	1023

Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 1023

PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times f_{OSC} \div R \qquad (N > A)$$

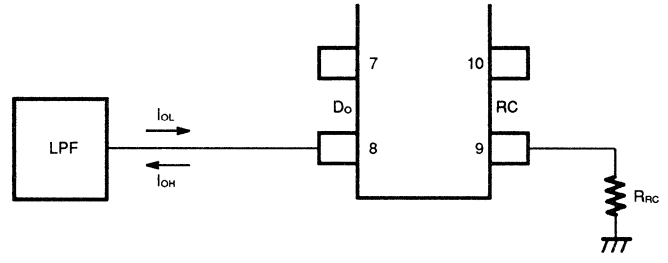
f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
f_{OSC} : Output frequency of the external oscillator
R : Preset divide factor of programmable reference divider (8, 16, 64, 128, 256, 512, 1024, 2048)

CONSTANT CURRENT OUTPUT CHARGE PUMP

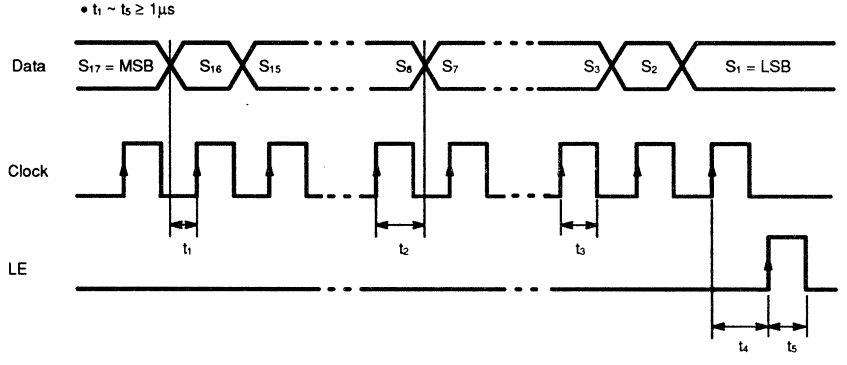
The MB87090 adopts constant current output charge pump. The output current of charge pump is controlled by an external resistor shown in Fig. 3.

2

Fig. 3 – EXTERNAL RESISTOR CONNECTION EXAMPLE



TIMING CHART

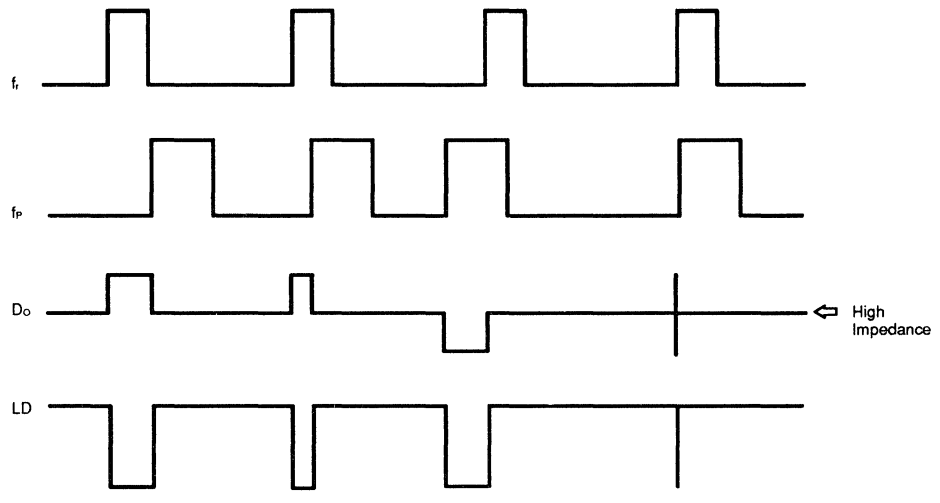


Clock : Clock signal input for the 17-bit shift register.
Each rising edge of the clock shifts one bit of data into the shift register.

Data : Serial data for the 17-bit shift register is input.

LE : Load enable input.
When LE is high (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.
The 17-bit data is used for setting a divide factor of the programmable divider.

PHASE DETECTOR OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	–	5.5	V
Input Voltage	V_{IN}	V_{SS}	–	V_{DD}	V
Operating Temperature	T_A	–40	–	+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = −40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	2.1	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	0.9	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, sine wave	0.8	–	–	V_{P-P}
	OSC_{IN}	V_{sin}		1.0	–	–	
High-level Input Current	Except f_{in} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$	–	1.0	–	µA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$	–	−1.0	–	
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
Input Current	OSC_{IN}	I_{osc}	$V_{IN} = V_{SS}$ to V_{DD}	–	±30	–	µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	2.95	–	–	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	–	–	0.05	
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	2.50	–	–	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	–	–	0.50	
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	−0.5	–	–	mA
Low-level Output Current		I_{OL}	V_{OL} = 1.0V	0.5	–	–	
High-level Output Current	D_O*1	I_{OHD}	V_{OH} = 2.0V	−1.0	−3.0	–	mA
Low-level Output Current		I_{OLD}	V_{OL} = 1.0V	1.0	3.0	–	
Power Supply Current*2		I_{DD}	–	–	2.0	4.0	mA
Max. Operating Frequency of Programmable Reference Divider		f_{maxd}	–	13	20	–	MHz
Max. Operating Frequency of Programmable Divider		f_{maxp}	–	10	20	–	MHz

Notes: *1: RC pin external resistor R_{RC} = 5kΩ.

*2 f_{in} = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
RC pin external resistor R_{RC} = 5kΩ.
Inputs are connected to ground except for f_{in} and OSC_{IN}. Outputs are open.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = –40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	3.5	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	1.5	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, sine wave	1.0	–	–	V_{P-P}
	OSC_{IN}	V_{sin}		1.5	–	–	
High-level Input Current	Except f_{in} and OSC_{IN}	I_{IH}	V_{IN} = V_{DD}	–	1.0	–	µA
Low-level Input Current		I_{IL}	V_{IN} = V_{SS}	–	–1.0	–	
Input Current	f_{in}	I_{IHF}	V_{IN} = V_{SS} to V_{DD}	–	±50	–	µA
Input Current	OSC_{IN}	I_{OSC}	V_{IN} = V_{SS} to V_{DD}	–	±50	–	µA
High-level Output Voltage	Except OSC_{OUT}	V_{OH}	I_{OH} = 0µA	4.95	–	–	V
Low-level Output Voltage		V_{OL}	I_{OL} = 0µA	–	–	0.05	
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0µA	4.50	–	–	V
Low-level Output Voltage		V_{OLX}	I_{OL} = 0µA	–	–	0.50	
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	–1.0	–	–	mA
Low-level Output Current		I_{OL}	V_{OL} = 1.0V	1.0	–	–	
High-level Output Current	D_O*1	I_{OHD}	V_{OH} = 4.0V	–2.0	–5.0	–	mA
Low-level Output Current		I_{OLD}	V_{OL} = 1.0V	2.0	5.0	–	
Power Supply Current*2		I_{DD}	–	–	3.0	6.0	mA
Max. Operating Frequency of Programmable Reference Divider		f_{maxd}	–	15	25	–	MHz
Max. Operating Frequency of Programmable Divider		f_{maxp}	–	13	25	–	MHz

Note: *1. RC pin external resistor R_{RC} = 5kΩ.

*2. f_{in} = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
RC pin external resistor R_{RC} = 5kΩ.
Inputs are connected to ground except for f_{in} and OSC_{IN}. Outputs are open.

TYPICAL CHARACTERISTICS CURVES

Conditions: V_{DD} = 5.0V/3.0V, Input amplitude of f_{in} = 1.0V_{p-p}, T_A = 25°C

2

Fig. 4 – INPUT FREQUENCY vs. INPUT SENSITIVITY (f_{in} Section)

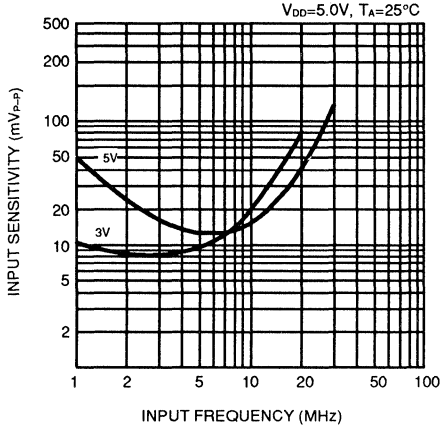


Fig. 5 – OUTPUT RESISTANCE vs. OUTPUT CURRENT

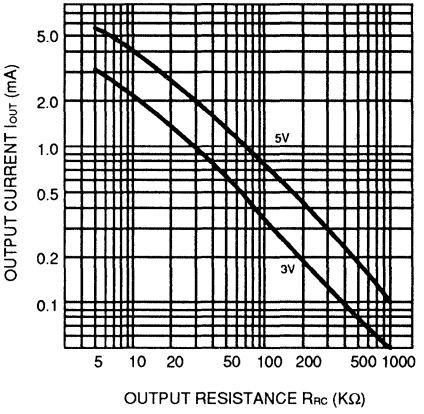


Fig. 6 – SUPPLY VOLTAGE vs. SUPPLY CURRENT

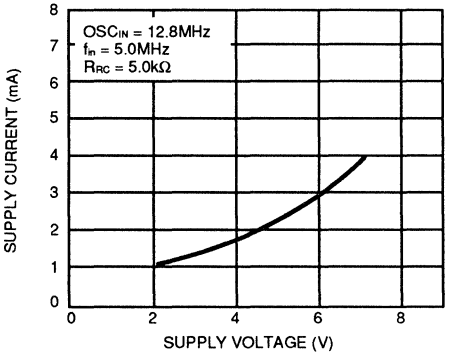
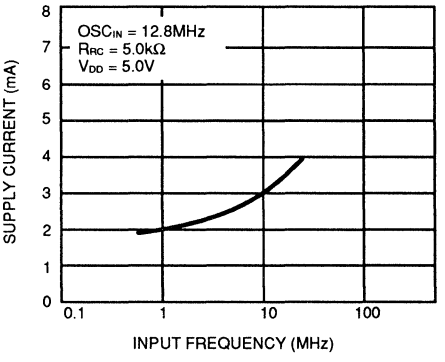
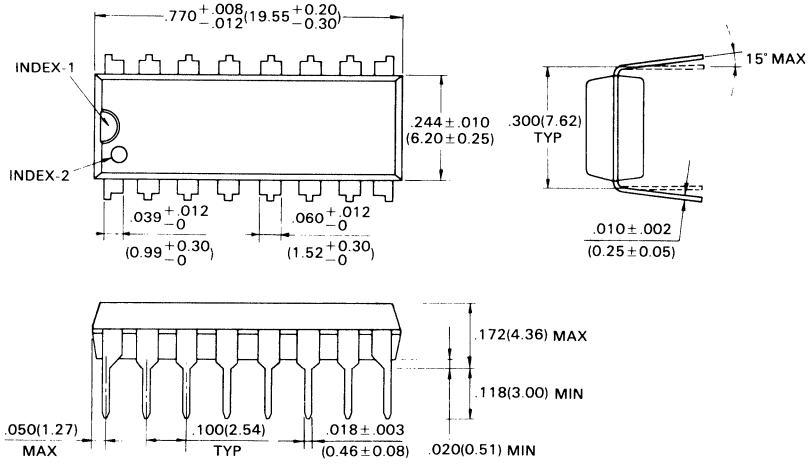


Fig. 7 – INPUT FREQUENCY vs. SUPPLY CURRENT



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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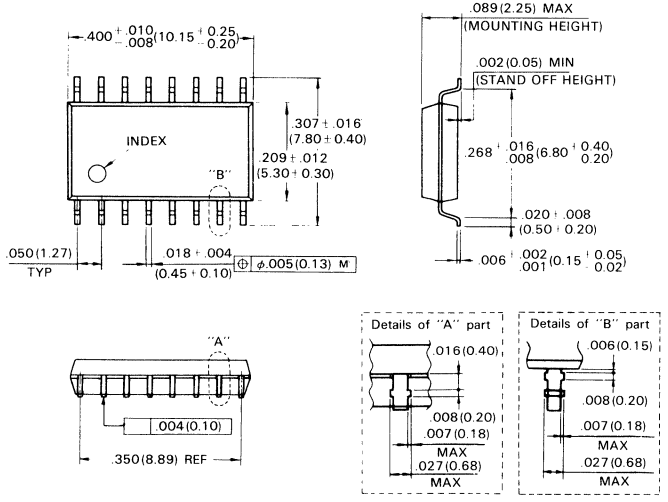
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

2

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in inches (millimeters)

Single-Chip PLLs/Prescalers — *At a Glance*

Page	Device	Maximum Frequency	Divide Ratio	Supply I_{CC}	Supply V_{CC}	Programmable Counter	Swallow Counter	Reference Counter	Package Options
3–3	MB1501 1501H 1501L	1.1 GHz	64/65 or 128/129	15 mA	2.7 V to 5.5 V	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	16-pin Plastic FPT
3–21	MB1502	1.1 GHz	64/65 or 128/129	8 mA	5.0 V (typ)	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	16-pin Plastic FPT
3–35	MB1503	1.1 GHz	128/129	8 mA	5.0 V (typ)	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	16-pin Plastic FPT
3–49	MB1504 1504H 1504L	520 MHz	32/33 or 64/65	10 mA	2.7 V to 5.5 V	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	16-pin Plastic FPT
3–67	MB1505	600 MHz	32/33 or 64/65	6 mA	5.0 V (typ.)	Binary 16 to 2047	Binary 0 to 63	Binary 8 to 16383	16-pin Plastic FPT
3–79	MB1507	2.0 GHz	128/129 or 256/257	18 mA	5.0 V (typ)	Binary 16 to 2047	Binary 0 to 255	Binary 8 to 16383	16-pin Plastic FPT
3–91	MB1508	2.5 GHz	256/272 or 512/528	16 mA	5.0 V (typ)	Binary 32 to 4095	Binary 0 to 31	Binary 256, 512, 1024, 2048	20-pin Plastic FPT
3–101	MB1509*	400 MHz	32/33 or 64/65	8 mA	3.0 V (typ)	Binary 16 to 2047	Binary 0 to 127	Binary 512 or 1024	20-pin Plastic FPT
3–115	MB1511	1.1 GHz	64/65 or 128/129	7 mA	2.7 V to 5.5 V	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	20-pin Plastic FPT
3–127	MB1512	1.1 GHz	64/65 or 128/129	8 mA	5.0 V (typ)	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	20-pin Plastic FPT
3–139	MB1513	1.1 GHz	128/29	8 mA	5.0 V	Binary 16 to 2047	Binary 0 to 127	Binary 8 to 16383	20-pin Plastic FPT
3–153	MB1518	2.5 GHz	512/528	16 mA	5.0 V (typ)	Binary 32 to 511	Binary 0 to 31	512	16-pin Plastic FPT
3–163	MB1519*	600 MHz	64/65	11 mA	2.7 V to 5.5 V	Binary 16 to 2047	Binary 0 to 127	512, 1024	20-pin Plastic FPT

*Dual PLL/Prescaler

November 1990
Edition 5.0

FUJITSU

DATA SHEET

MB1501/MB1501H/MB1501L
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

The Fujitsu MB1501/MB1501H/MB1501L, utilizing BI-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse-swallow function.

The MB1501 series contain a 1.1GHz two modulus prescaler that can select either 64/65 or 128/129 divide ratio; control signal generator; 16-bit shift register; 15-bit latch; programmable reference divider (binary 14-bit programmable reference counter); 1-bit switch counter; phase comparator with phase inverse function; charge pump; crystal oscillator; 19-bit shift register; 18-bit latch; programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

The MB1501 operates on a low supply voltage (3V typ) and consumes low power (45mW at 1.1GHz).

MB1501 Product Line

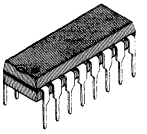
	V_P Voltage	V_{OOP} Voltage	Lock up time	D_O Output Width	High-level Output Current	Low-level Output Current
MB1501	8V max	8.5V max	Middle speed	Middle	Middle	Middle
MB1501H	10V max	10.0V max	High speed	Low	High	Low
MB1501L	8V max	8.5V max	Low speed	High	Low	High

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($V_{IN\ MIN}$=0.20V_{P-P})
- On-chip prescaler
- Low power supply voltage: 2.7V to 5.5V (3.0V typ)
- Low power supply consumption: 45mW (3.0V, 1.1GHz operation)
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  - Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter (Divide ratio: 8 to 16383)
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: T_A=−40°C to +85°C

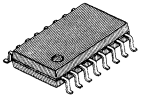
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{PH}	MB1501H	V_{CC} to 12.0	V
	V_P, V_{PL}	MB1501/1501L	V_{CC} to 10.0	
Output Voltage	V_{OUT}		−0.5 to V_{CC} +0.5	V
Open-drain Output	V_{OOPH}	MB1501H	−0.5 to 11.0	V
	V_{OOP}, V_{OOPL}	MB1501/1501L	−0.5 to 9.0	
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

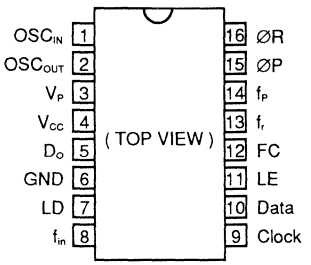


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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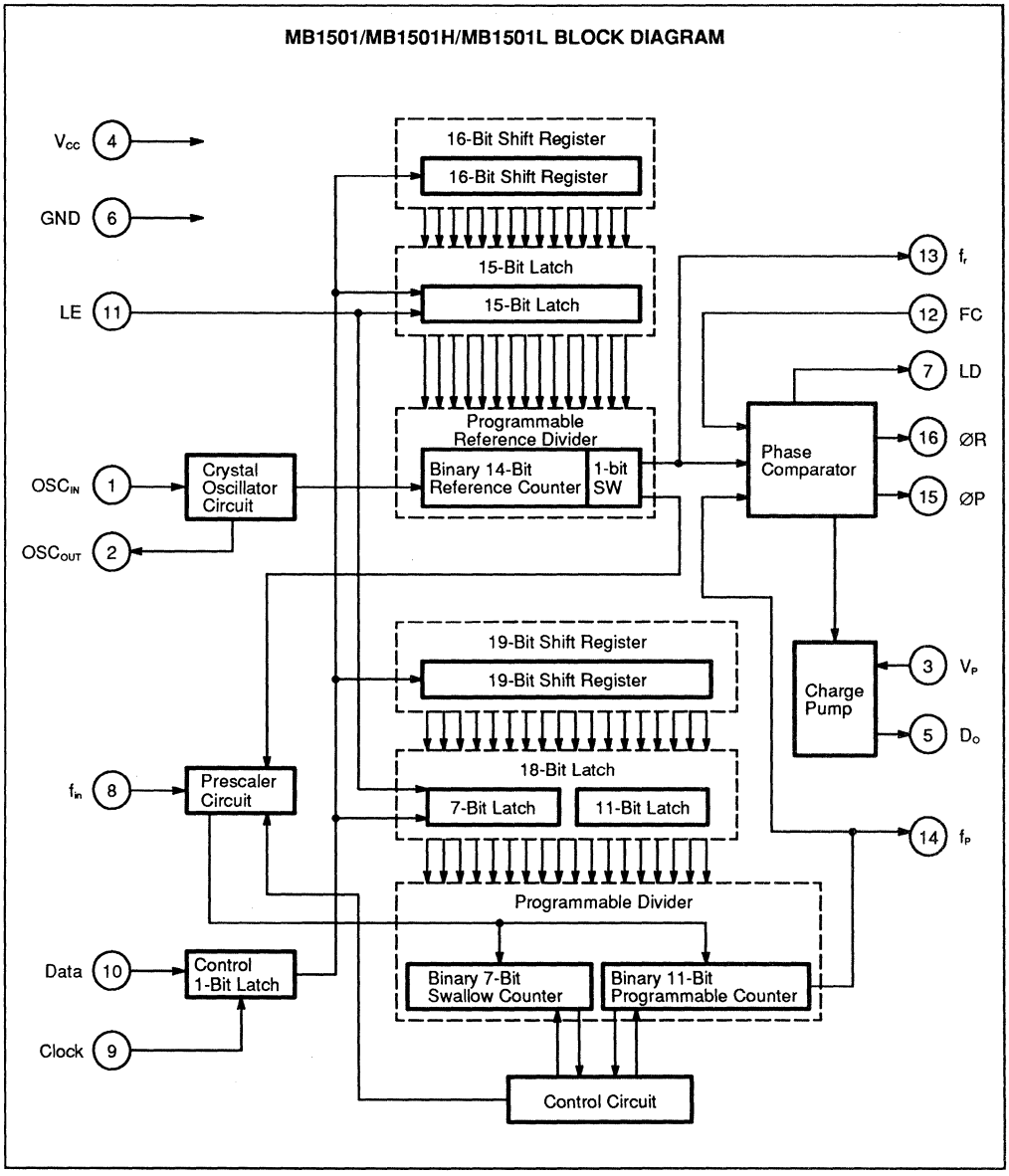
3

MB1501/MB1501H/MB1501L BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. Phase characteristic can be inversed depending upon FC input.
6	GND	—	Ground.
7	LD	O	Phase comparator output. This pin outputs high when the phase is locked. While the phase difference of f_r and f_p exists, the output level goes low.
8	f_{in}	I	Prescaler input. The connection with an external VCO should be an AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input. The last bit of the data is a control bit. The last data bit specifies which latch is activated. When the last bit is high level and LE is high-level, data is transferred to 15-bit latch. When the last bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high level (or open), data stored in the shift register is transferred to latch depending on the control data.
12	FC	O	Phase selecting input of phase comparator (with internal pull up resistor). When FC is low level, charge pump and phase detector characteristics can be inversed.
13	f_r	O	Monitor pin of phase comparator input. It is the same as programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input. It is the same as programmable divider output.
15 16	ØP ØR	O O	Outputs for external charge pump. Phase characteristics can be inversed depending on FC input. ØP pin is an N-channel open-drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is input using Data pin, Clock pin and LE pin, The 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.

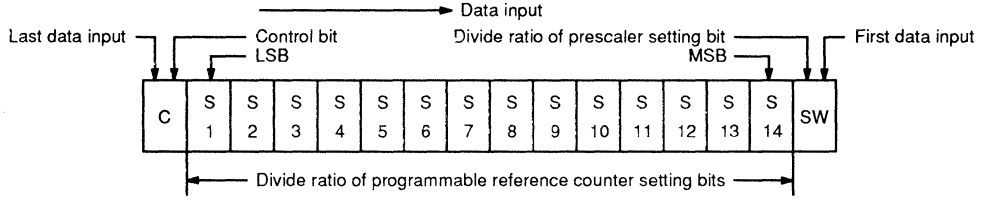
On rising edge of the clock shifts one bit of the data into the internal shift registers.

When load enable (LE) is high level (or open), data stored in shift resisters is transferred to 15-bit latch or 18-bit latch depending upon the control bit level.

Control data "H" ; Data is transferred into 15-bit latch.
Control data "L" ; Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



◎ 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

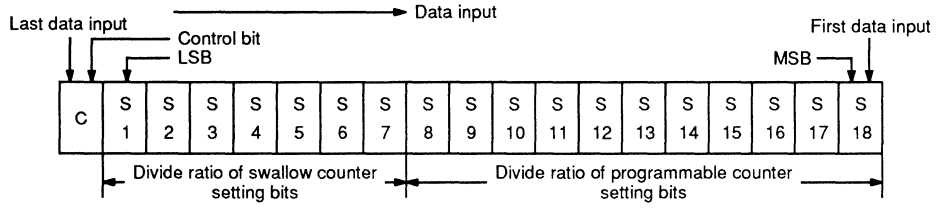
Divide ratio less than 8 is prohibited.
Divide ratio R: 8 to 16383

SW: Divide ratio of prescaler setting bit.
SW="H" : 64
SW="L" : 128
S_1 to S_{14}: Divide ratio of programmable reference counter setting bits (8 to 16383)
C: Control bit (Control bit is set to high.)

FUNCTIONAL DESCRIPTIONS

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown below.



◎ 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide ratio A : 0 to 127

◎ 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

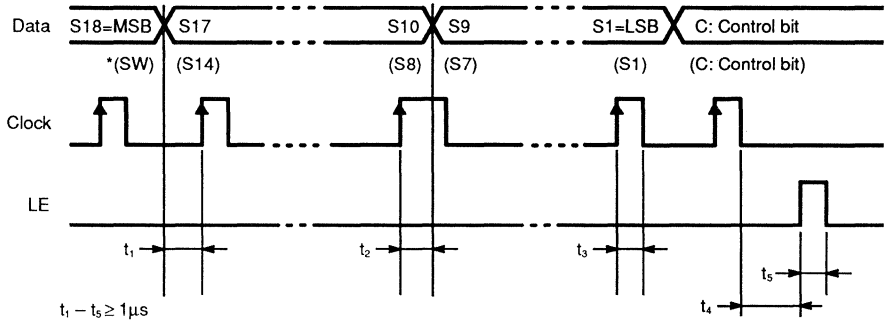
Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited.
Divide ratio N : 16 to 2047

S_8 to S_{18} : Divide ratio of programmable counter setting bits (16 to 2047)
S_1 to S_7 : Divide ratio of swallow counter setting bits (0 to 127)
C: Control bit (Control bit is set to low.)
Dara is input from MSB data.

3

SERIAL DATA INPUT TIMING



On the rising edge of the clock shifts one bit of the data into the shift registers.
Parenthsis data is used for setting the divide ratio of the programmable reference divider.

PHASE CHARACTERISTICS

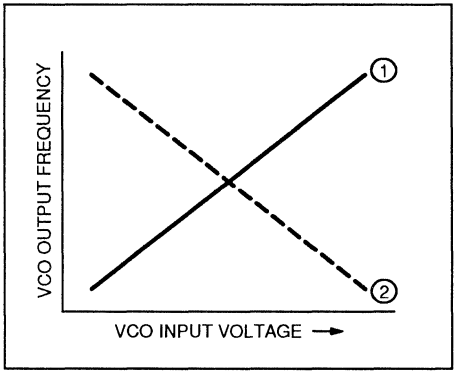
FC pin (pin 12) is provided to inverse the phase comparator characteristics. The characteristics of internal charge pump output (D_O), phase detector outputs (øR, øP) can be inversed depending upon FC input data. Outputs are shown below.

	FC=H (or open)			FC=L		
	D_O	ØR	ØP	D_O	øR	øP
$f_r > f_p$	H	L	L	L	H	Z
$f_r < f_p$	L	H	Z	H	L	L
$f_r = f_p$	Z	L	Z	Z	L	Z

Note: Z=(High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.

VCO CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}		2.7	3.0	5.5	V
	V_{PH}	MB1501H	V_{CC}		10.0	V
	V_P, V_{PL}	MB1501 MB1501L	V_{CC}		8.5	
Open-drain Output	V_{OOPH}	MB1501H	V_{CC}		10.0	V
	V_{OOP}, V_{OOPL}	MB1501 MB1501L	V_{CC}		8.5	
Input Voltage	V_{IN}		GND		V_{CC}	V
Operating temperature	T_A		–40		+85	°C

3

ELECTRICAL CHARACTERISTICS

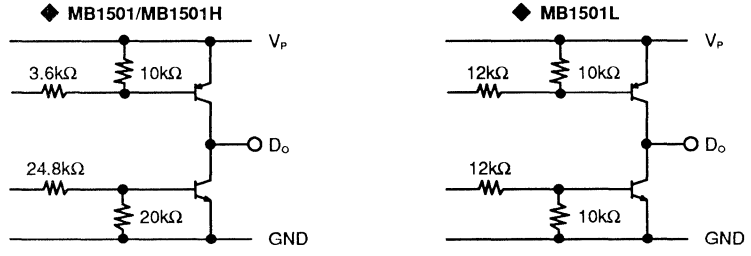
(V_{CC}=2.7 to 5.5V, T_A=–40 to +85°C)

Parameter	Pin Name	Symbol	Condition	Value Min	Value Typ	Value Max	Unit
Power Supply Current	V_{CC}	I_{CC}	*1	—	15	—	mA
Operating Frequency	f_{in}	f_{IN}	*2	10	—	1100	MHz
	OSC_{IN}	f_{OSC}		—	12	20	MHz
Input Sensitivity	f_{in}	V_{fin1}	V_{CC}=2.7 ~ 4.0V	–10	—	6	dBm
		V_{fin2}	V_{CC}=4.0 ~ 5.5V	–4	—	6	dBm
	OSC_{IN}	V_{IN}		0.5	—	—	V_{P-P}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		0.7xV_{CC}	—	—	V
Low-level Input Voltage		V_{IL}		—	—	0.3xV_{CC}	V
High-level Input Current	Data, Clock	I_{IH}		—	1.0	—	µA
Low-level Input Current		I_{IL}		—	–1.0	—	µA
Input Current	OSC_{IN}	I_{IN}		—	±50	—	µA
	LE, FC	I_{LE}		—	–60	—	µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3.0V	2.4	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	V
N-channel Open-drain Cutoff Current	ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$	—	—	1.1	µA
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	—	—	mA
Low-level Output Current		I_{OL}		1.0	—	—	mA
High-level Output Current	D_O	I_{DOHH}	MB1501H: V_{CC}=3V, V_P=12V, T_A=25°C	–2.2	–4.5	—	mA
		I_{DOH}	MB1501: V_{CC}=3V, V_P=6V, T_A=25°C	–0.5	–2.0	—	mA
		I_{DOHL}	MB1501L: V_{CC}=3V, V_P=6V, T_A=25°C	–0.5	–1.1	–2.2	mA
Low-level Output Current		I_{DOLH}	MB1501H: V_{CC}=3V, V_P=12V, T_A=25°C	2.2	6.0	—	mA
		I_{DOL}	MB1501: V_{CC}=3V, V_P=6V, T_A=25°C	1.5	6.0	—	mA
		I_{DOLL}	MB1501L: V_{CC}=3V, V_P=6V, T_A=25°C	4.5	12.0	—	mA
Leakage Current	D_O, ØP	D_{OZ}	MB1501H: V_{CC}=3V, V_P=12V, T_A=25°C	—		1.0	µA
			MB1501, MB1501L: V_{CC}=3V, V_P=9V, T_A=25°C				

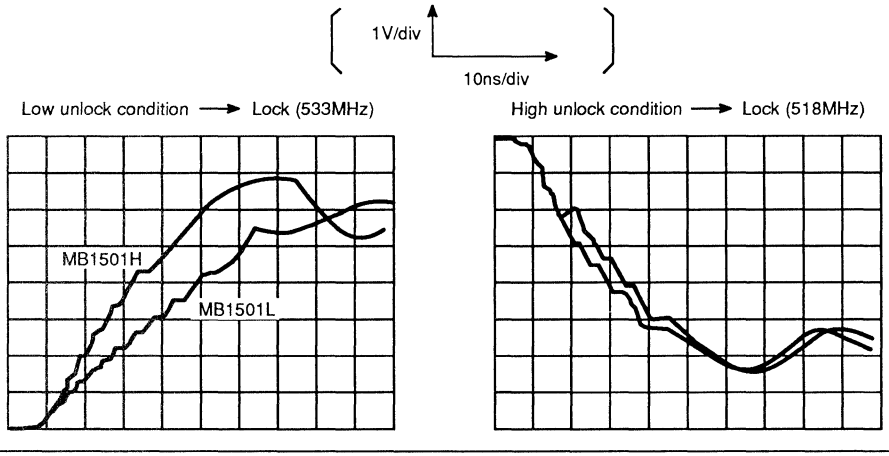
Note: *1 V_{CC}=3.0V, f_{IN}=1.1GHz, f_{OSC}=12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2 Input coupling capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

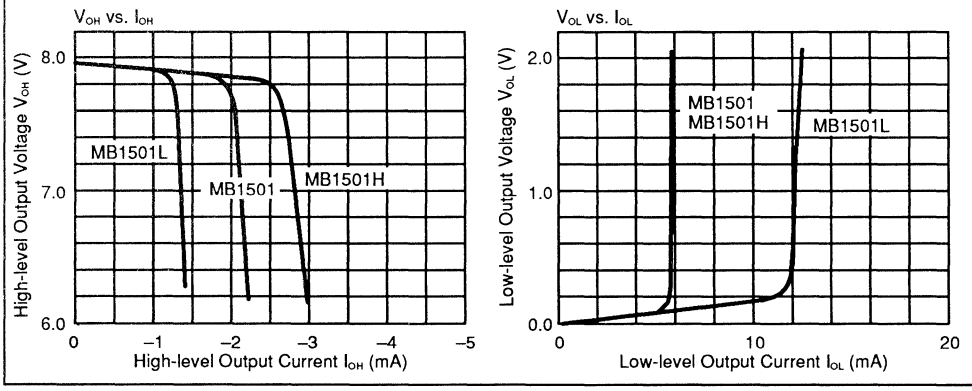
CHARGE PUMP CHARACTERISTICS



LOCK UP TIME MEASUREMENT



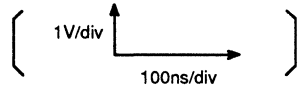
DO PIN OUTPUT CURRENT CURVES (TYPICAL)



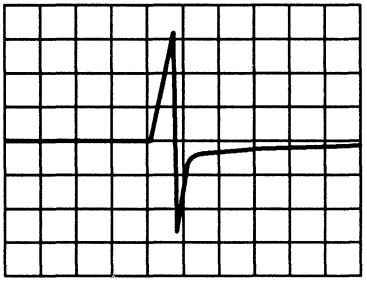
3

Do PIN OUTPUT WAVEFORM AT LOCK CONDITION

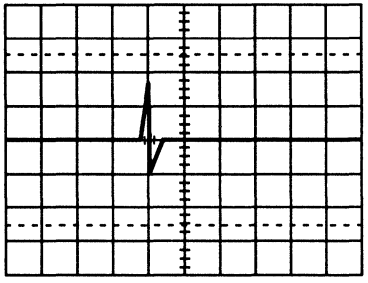
Output Waveform



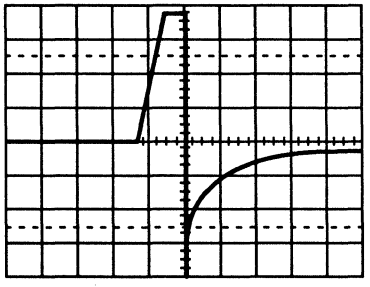
MB1501



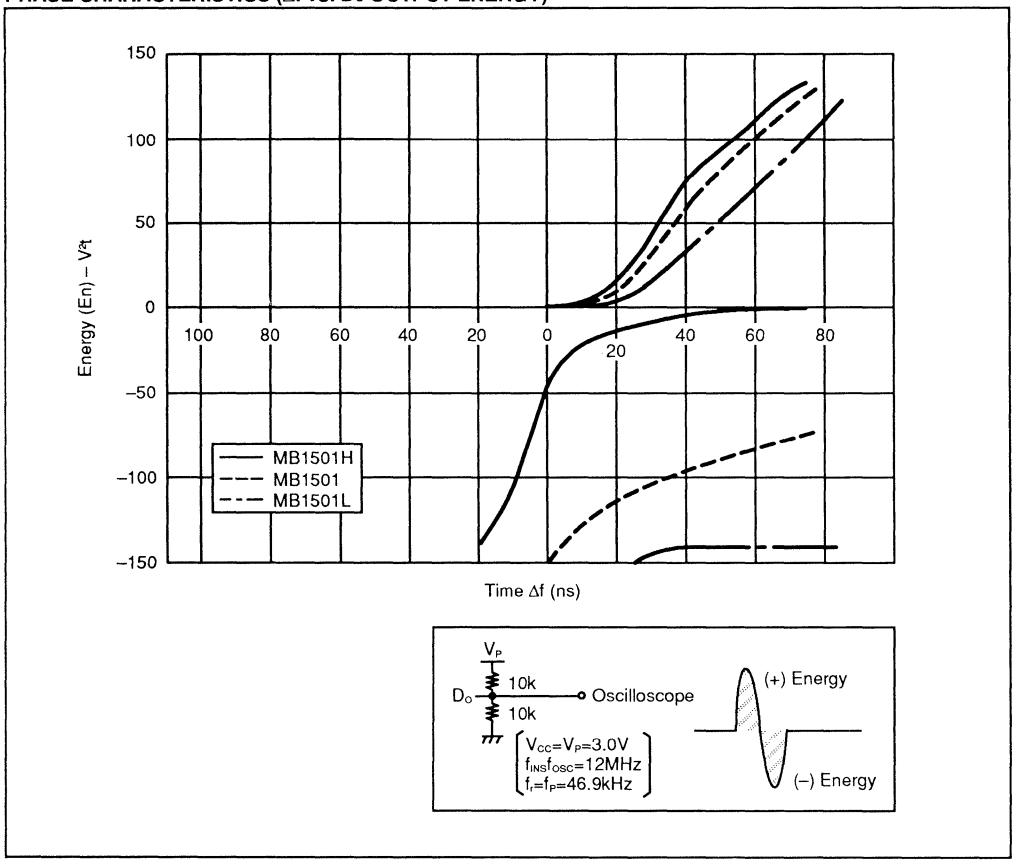
MB1501H



MB1501L



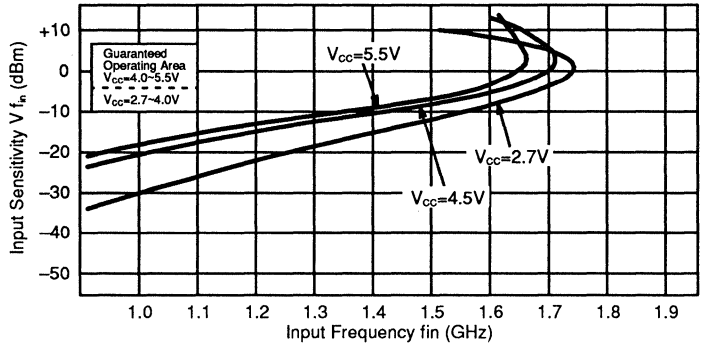
PHASE CHARACTERISTICS (Δf vs. Do OUTPUT ENERGY)

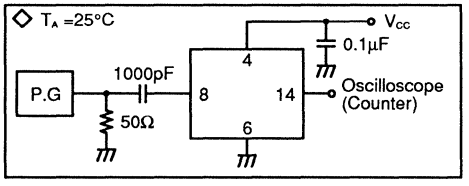


3

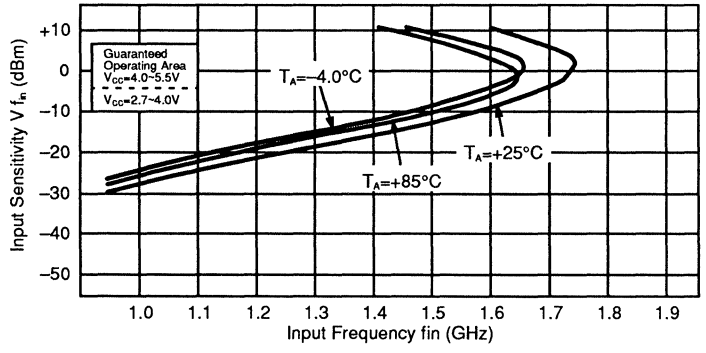
INPUT SENSITIVITY

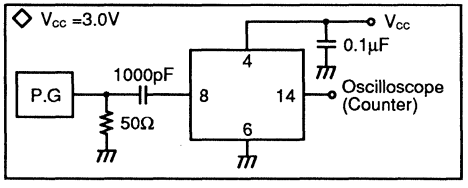
Input Sensitivity vs. Input Frequency (Supply Voltage Dependence)



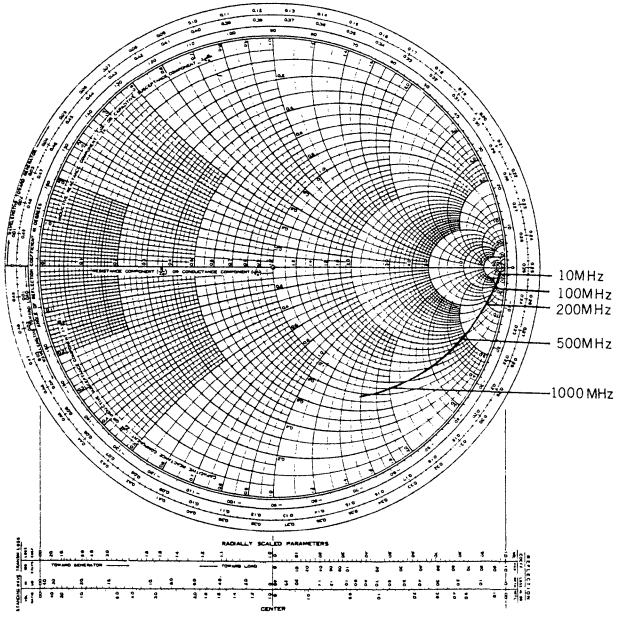


Input Sensitivity vs. Input Frequency (Temperature Dependence)



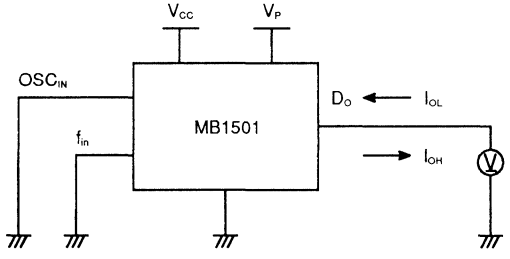


INPUT IMPEDANCE



TEST CIRCUIT

D_O Pin Output Current (I_{OH}, I_{OL}) Measurement



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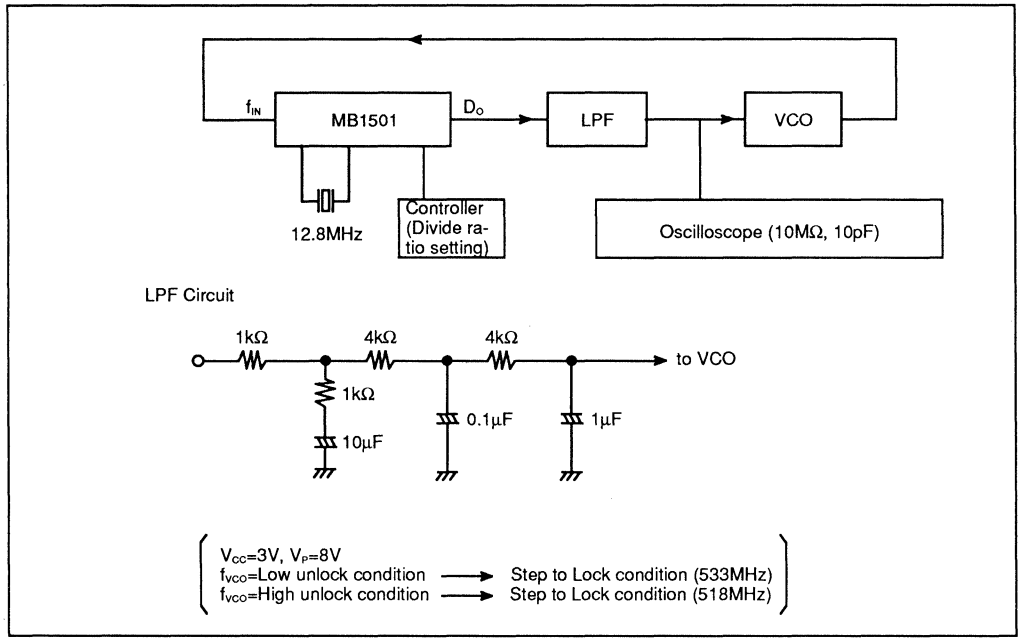
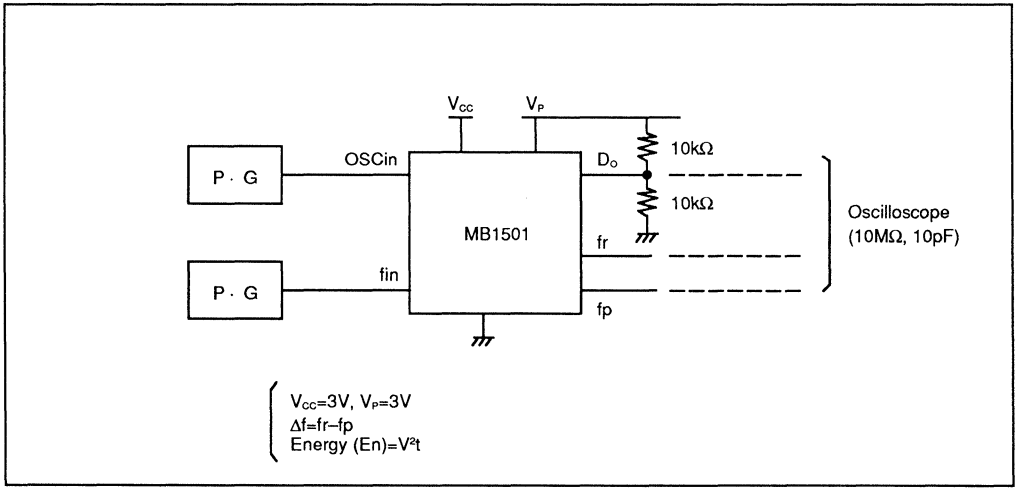
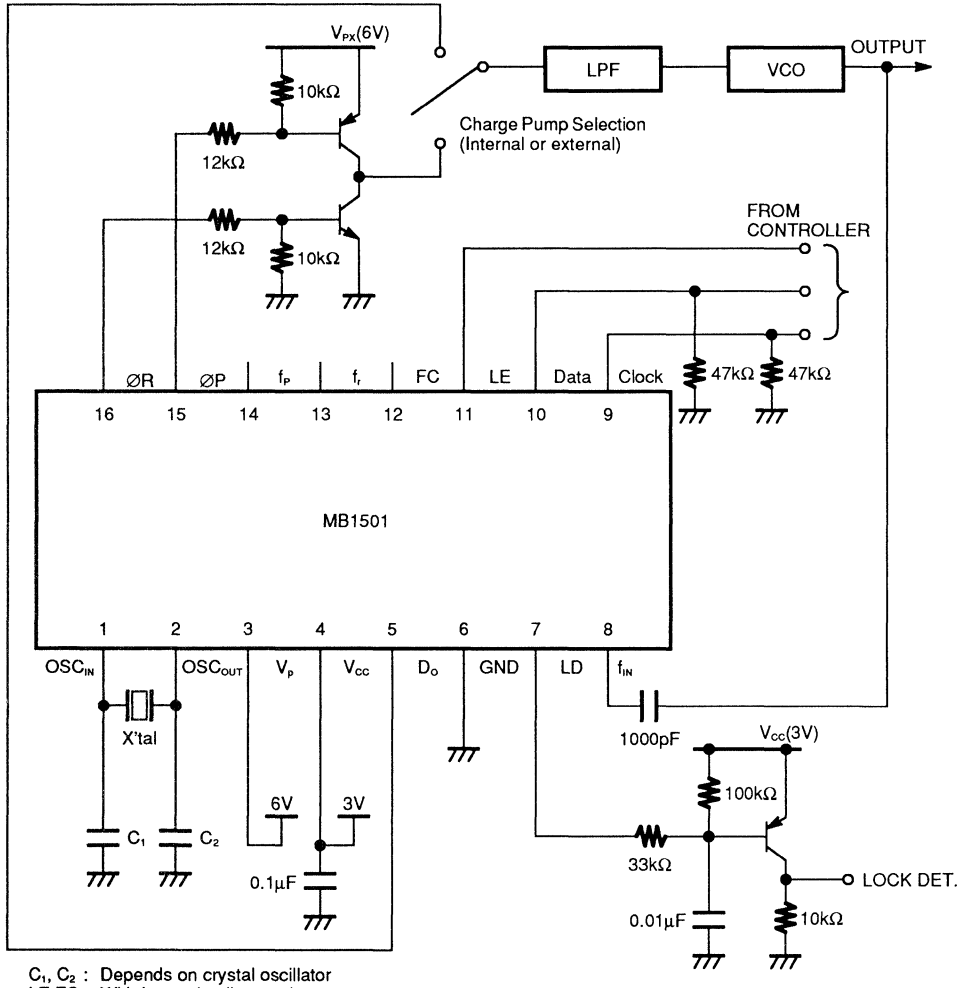
Lock up Time Measurement



Phase Characteristics Measurement



TYPICAL APPLICATION EXAMPLE



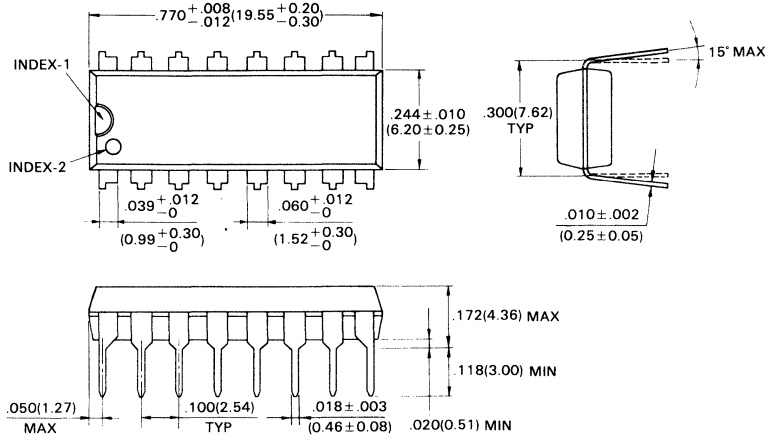
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

3

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)



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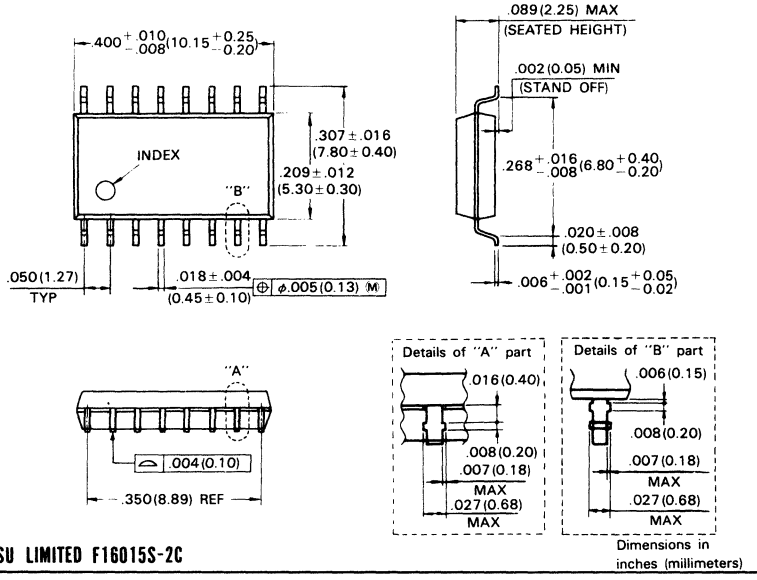
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-16P-M06)



Dimensions in inches (millimeters)

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3

FUJITSU

DATA SHEET

MB1502

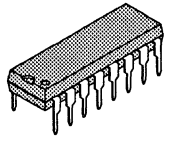
Serial Input PLL Frequency Synthesizer

The Fujitsu MB1502 fabricated in Bi-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.

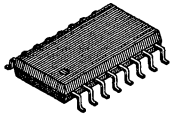
The MB1502 contains the following: analog switch to speed up lock up time, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and a 1.1 GHz two modulus prescaler that can select either a 64/65 or 128/129 divide ratio.

It operates supply voltage of 5 V typ. and achieves very low power supply current of 8 mA typ. realized through the use of Fujitsu Advanced Process Technology.

- High operating frequency: $f_{IN\ MAX}$ = 1.1 GHz ($V_{IN\ MAX}$ = −10 dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC} = 8 mA typ.
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  – Binary 14-bit programmable reference counter: 8 to 16383
  – 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- Two types of phase detector output:
  – On-chip charge pump (Bipolar type)
  – Output for external charge pump
- Wide operating temperature: −40 °C to +85 °C
- 16-pin Plastic DIP Package (Suffix: –P)
  16-pin Plastic Flat Package (Suffix: –PF)

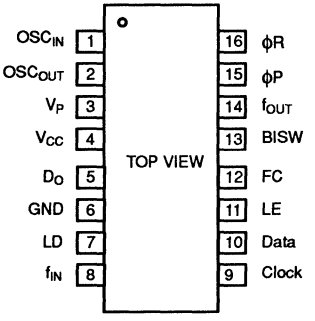


Plastic Package
DIP-16P-M04



Plastic Package
FPT-16P-M06

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	−0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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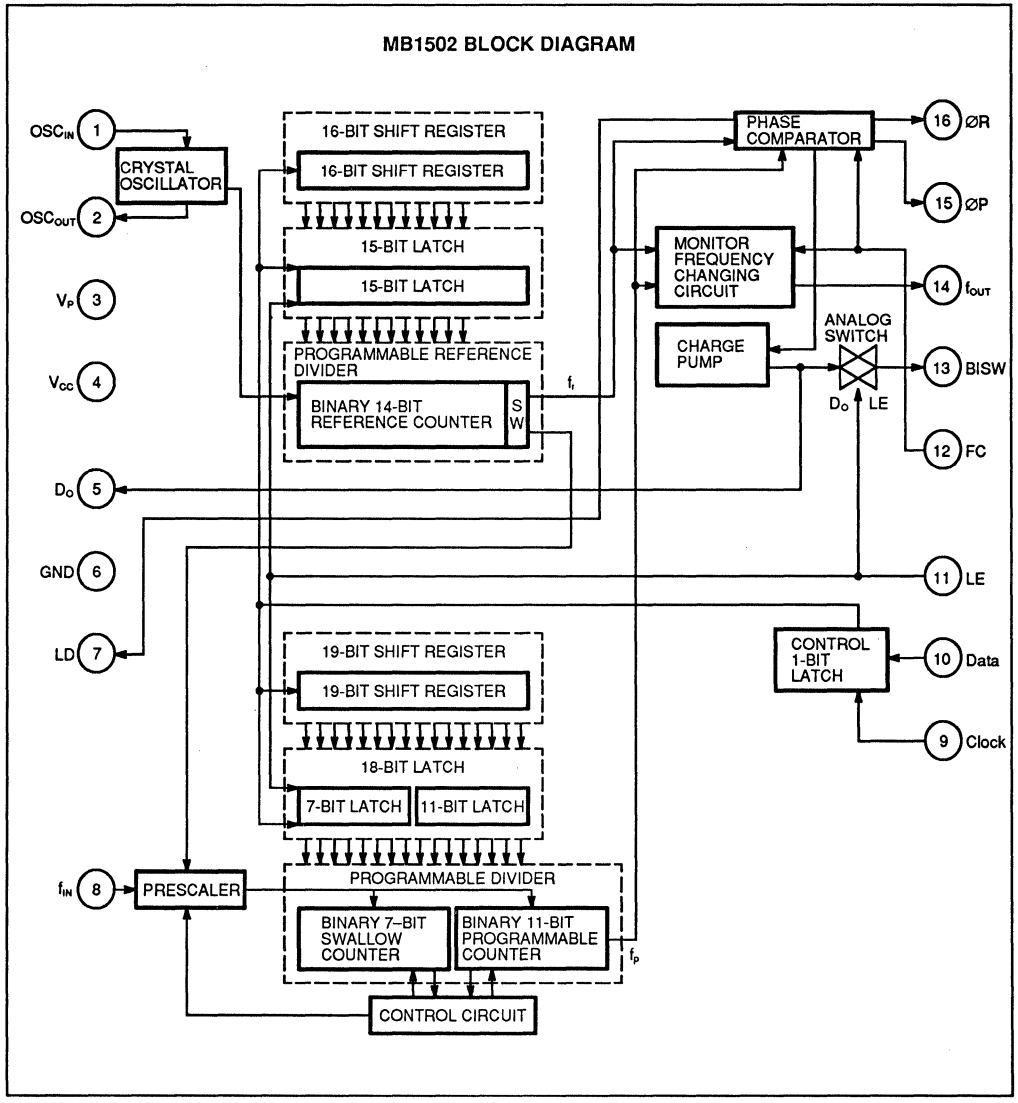
3

MB1502 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	–	Power supply input for charge pump and analog switch.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump are reversed depending upon FC input.
6	GND	–	Ground.
7	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f, and f_p exists, this pin outputs low level.
8	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift register.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{out} pin (test pin) output level, f, or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f, output level. FC=L: It is the same as f_p output level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.

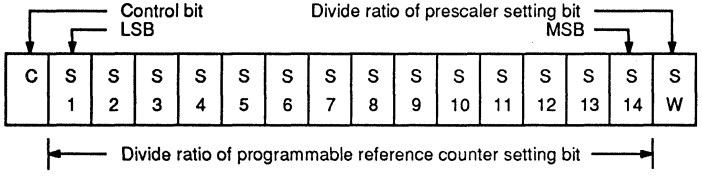
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



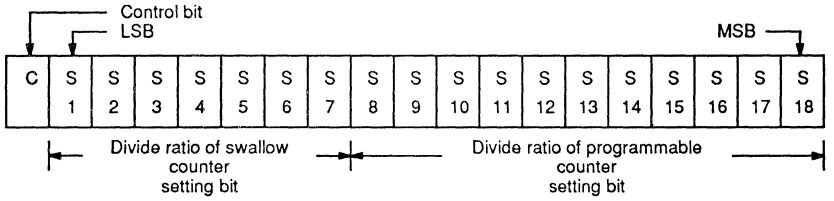
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64
SW=L : 128
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown on the following page



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

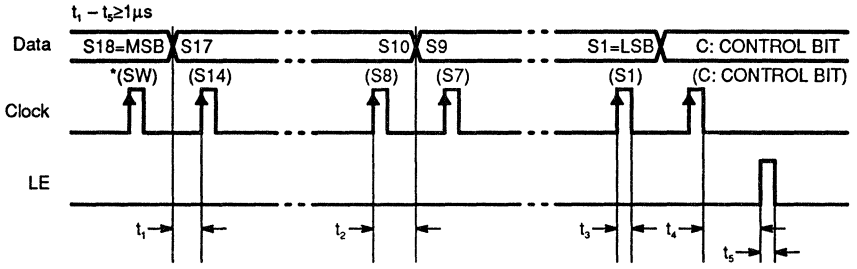
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{vco} = [(PxN)+A] \times f_{osc} \div R$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{osc}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

SERIAL DATA INPUT TIMING



NOTES: The data noted in parentheses is used for setting the divide ratio.
On rising edge of clock, one bit of data shifts into the shift register.

NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

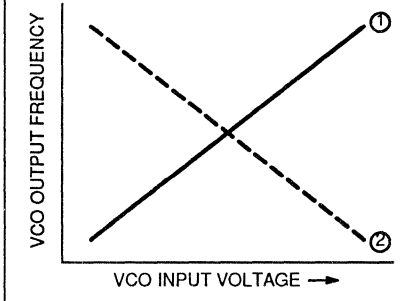
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level ($\varnothing R$, $\varnothing P$) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relationship between outputs ($D\phi_1$, ϕR, ϕP) and FC input level is shown below.

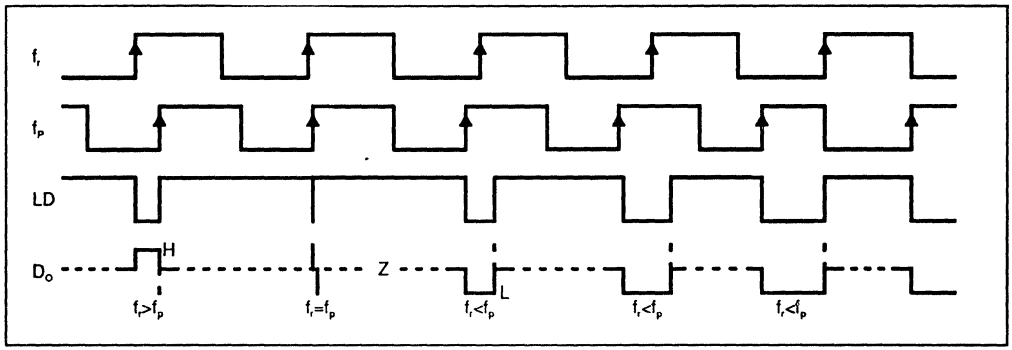
	FC=H or open				FC=L			
	D_O	$\varnothing R$	$\varnothing P$	f_{out}	D_O	$\varnothing R$	$\varnothing P$	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.



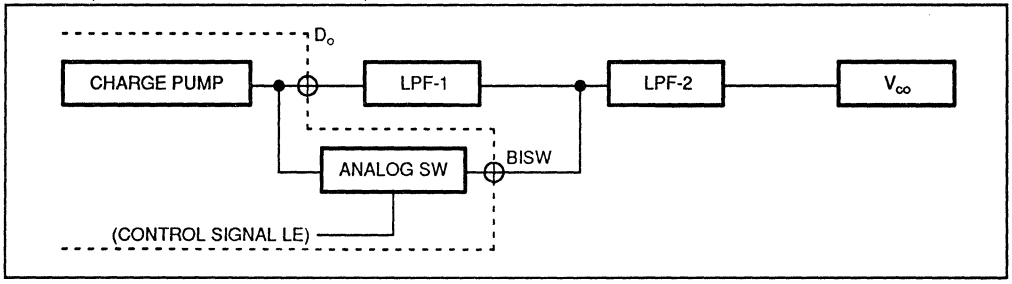
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) is connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode) : Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	−40		85	°C

ELECTRICAL CHARACTERISTICS

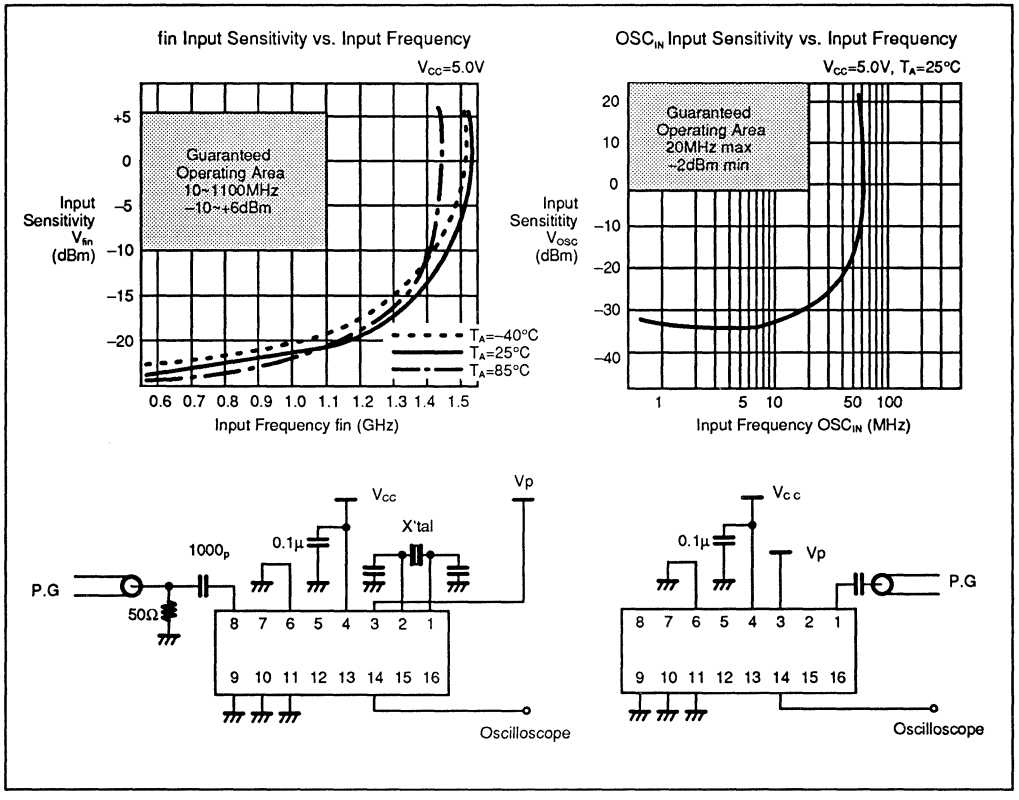
(V_{CC}=4.5 to 5.5V, T_A=–40 to +85°C, unless otherwise noticed.)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		8.0	12.0	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10		1100	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in}	Vf_{in}		–10		6	dBm
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except fi_n and OSC_{IN}	V_{IH}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			–1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			–60		µA
High-level Output Current	Except D_o and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_o, ØP	I_{OFF}	V_P=V_{CC} to 8V V_{OOP}=GND to 8V			1.1	µA
Output Current	Except D_o and OSC_{OUT}	I_{OH}		–1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistor		R_{ON}			25		Ω

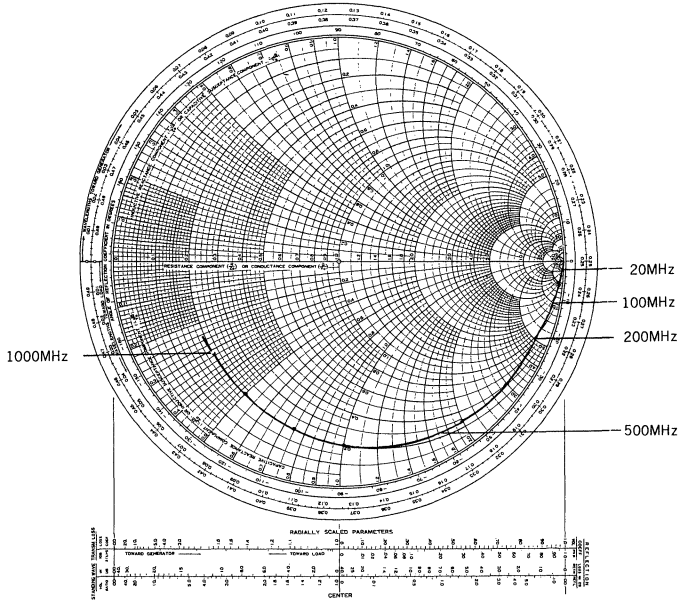
NOTE 1: f_{in}=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

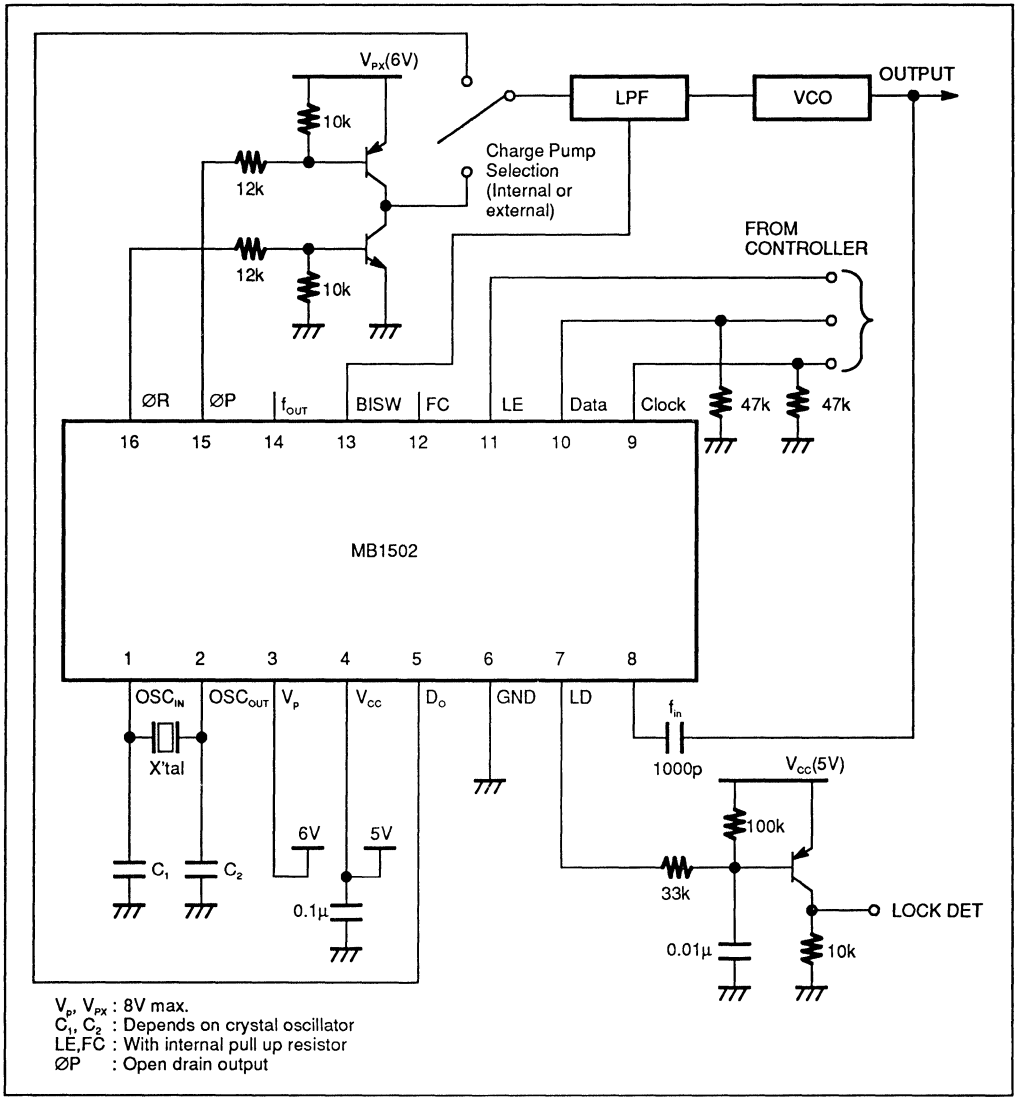
INPUT SENSITIVITY CHARACTERISTICS



INPUT IMPEDANCE CHARACTERISTICS



TYPICAL APPLICATION EXAMPLE

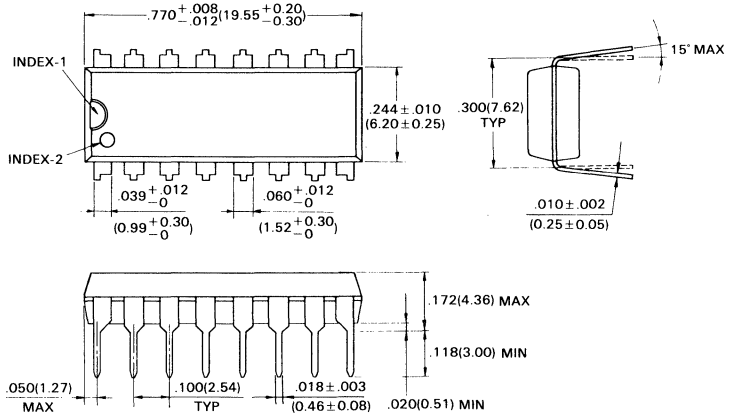


V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)



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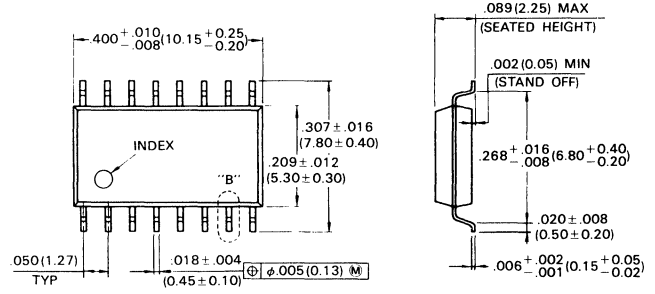
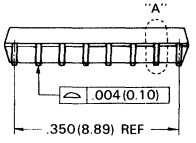
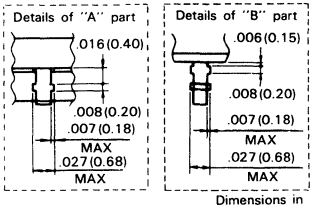
Dimensions in
inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-16P-M06)







Dimensions in inches (millimeters)

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3

FUJITSU

DATA SHEET

MB1503

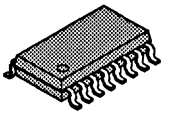
Serial Input PLL Frequency Synthesizer

The Fujitsu MB1503 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.

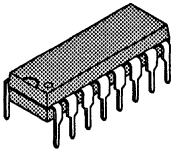
The MB1503 is configured with a 1.1 GHz dual-modulus prescaler with a 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and intermittent operation control circuit that selects the operating or stand-by mode depending on the power-save control input state (PS).

The MB1503 operates from a single +5 V supply. Fujitsu's advanced technology achieves an I_{CC} of 8 mA, typical. The stand-by mode current consumption is just 100 µA.

- High operating frequency: f_{IN} = 1.1 GHz (V_{IN} = –10 dBm)
- Pulse-swallow function: high-speed dual-modulus prescaler with 128/129 divide ratio
- Low supply current: I_{CC} = 8 mA typ. at 5 V
- Power-saving stand-by mode: 100 µA
- Serial input, 18-bit programmable reference divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 0 to 2,047
- Serial input, 15-bit programmable reference divider consisting of binary 15-bit programmable reference counter: 8 to 16,383 1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lock-up
- On-chip charge pump
- Wide operating temperature range: –40 to +85 °C
- Plastic 16-pin dual inline package (Suffix: –P)
  Plastic 16-pin small outline package (Suffix: –PF)

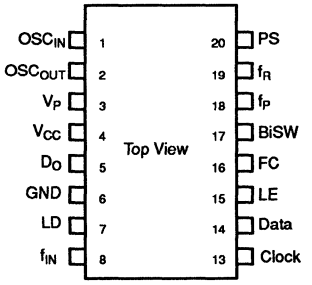


FPT-16P-M06



DIP-16P-M04

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	$V_{CC} \leq V_P \leq 10.0$	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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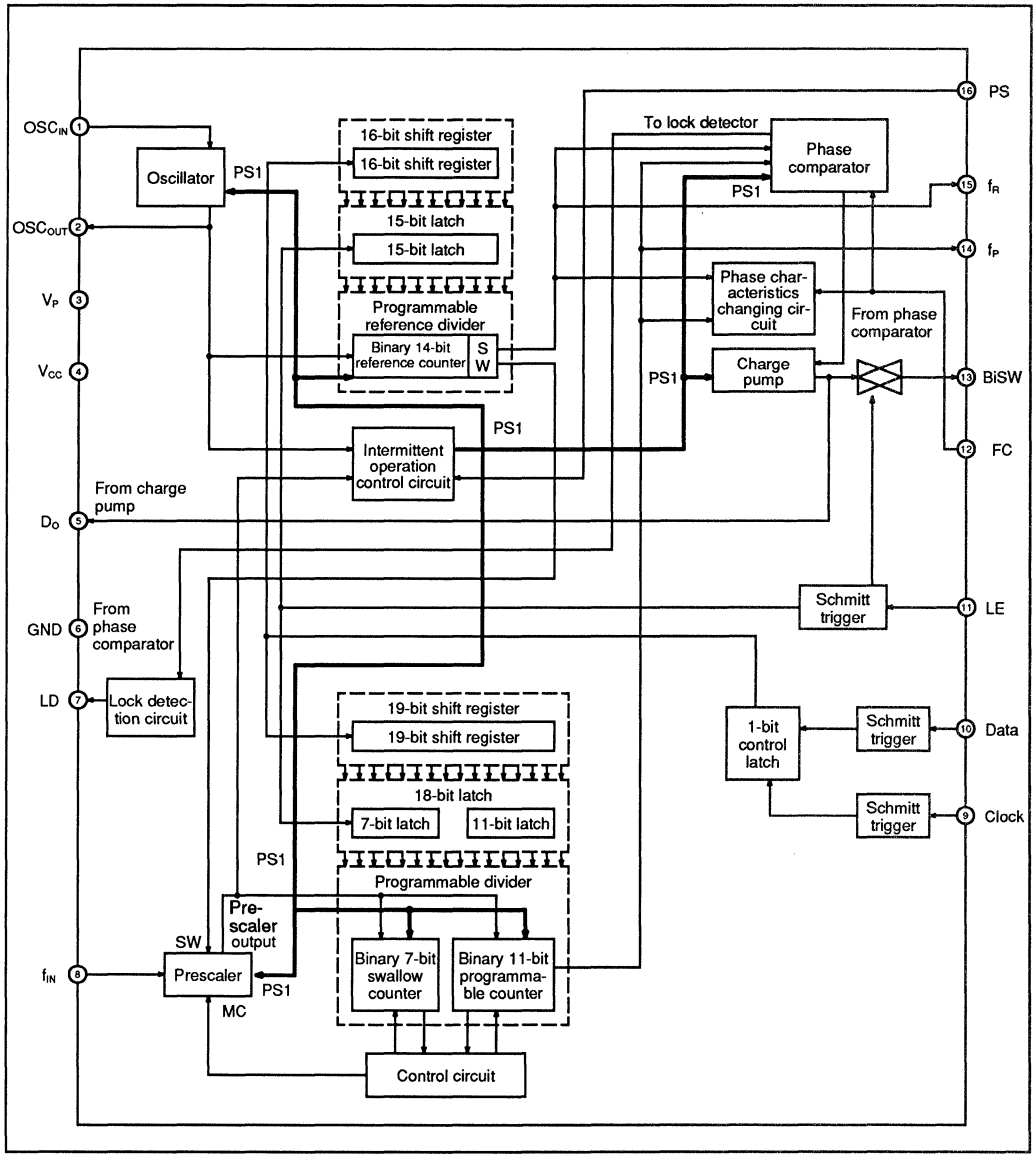
BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin
2	OSC_{OUT}	O	Oscillator output An external crystal is connected to this pin
3	V_P	–	Power supply input for charge pump and analog switch
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output Phase of charge pump is reversed depending on FC input
6	GND	–	Ground
7	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done by AC coupling
9	Clock	I	Clock input for 19-bit and 16-bit shift registers Data is shifted into the shift register on the rising edge of the clock Schmitt trigger circuit is involved
10	Data	I	Serial data input using binary code The last bit of the data is a control bit When the control bit is high, data is transmitted to the 15-bit latch When it is low, data is transmitted to the 18-bit latch Schmitt trigger input is involved
11	LE	I	Load enable signal input When LE is high, the data of the shift register is transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin Schmitt trigger input is involved
12	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f_{OUT} pin (test pin) of f_R or f_P
13	BiSW	O	Analog switch output BiSW is usually in the high-impedance state. When the switch is turned on (LE is high), the state of the internal charge pump is output
14	f_P	O	Programmable counter output monitor pin
15	f_R	O	Reference counter output monitor pin
16	PS	I	Power save signal input Set PS low while the system is powered (Never use pin 16 as it is opened) PS = High : Operation mode PS = Low : Stand-by mode

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

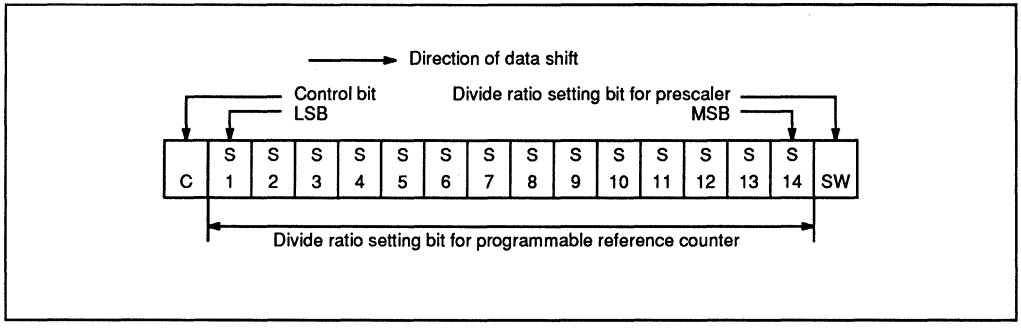
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of modulus prescaler (128)

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	15 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The serial 16-bit data format is shown below:



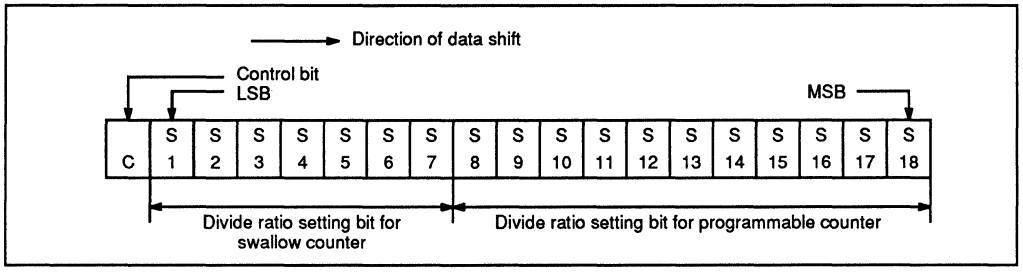
- 14-bit programmable reference counter divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited.
2. SW: This bit selects the divide ratio of the prescaler
SW Low: 128 or 129
(SW must be always be low.)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383).
4. C: Control bit: Set high.
5. Input data MSB first.

(b) Programmable divider divide ratio
The programmable divider consists of a 19-bit shift register, an 18-bit latch, a 7-bit swallow counter, and an 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

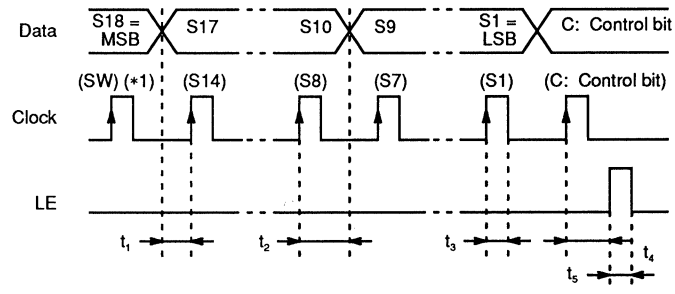
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 16 to 2,047)

Notes: 1. Divide ratios less than 16 are prohibited for 11–bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (16 to 2,047).
4. C: Control bit: (Set low)
5. Input data MSB first.

Serial data input timing

- t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
  t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or starting the internal circuits according to its necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost.
To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enters the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS = High)
  All circuits are operating, and PLL operation is normal.

- Stand-by mode (PS = Low level)
  Circuits that do not affect operation are power-down to limit current consumption.
  The current in the power save state is typically 100 µA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

Relationship between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed, depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

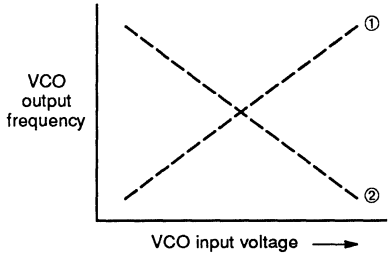
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (*1)	Z (*1)

*1: High impedance

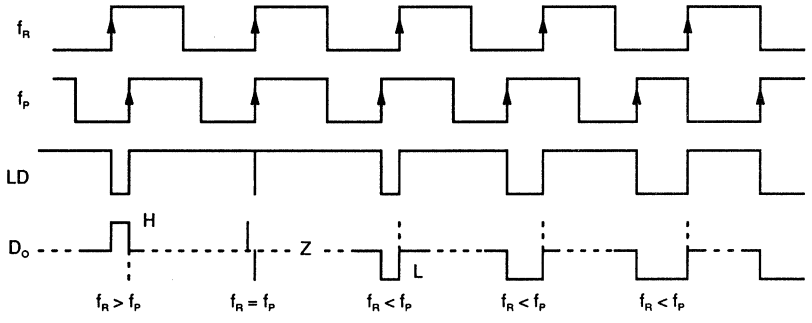
When designing a synthesizer, the FC pin setting depends on the VCO characteristics.

*: When the VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveform (FC = High)



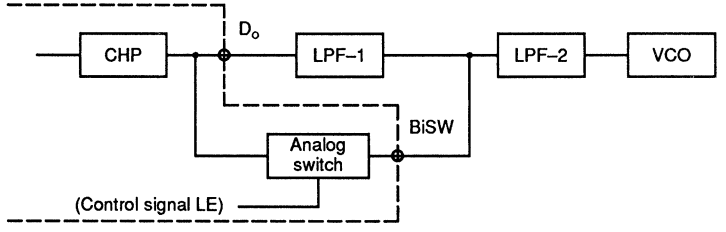
Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. Also, the spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, spike might not appear depending on the charge pump characteristics.
4. LD is low when the phase difference is two or more. LD is high when the phase difference is two or less for three or more cycles (when f_{OSCIN} = 12.8 MHz, tw = 625 to 1,250 ns).

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (D_O) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$			V
Input voltage	V_I	GND	–	V_{CC}	V
Operating temperature	T_A	–40	–	+85	°C

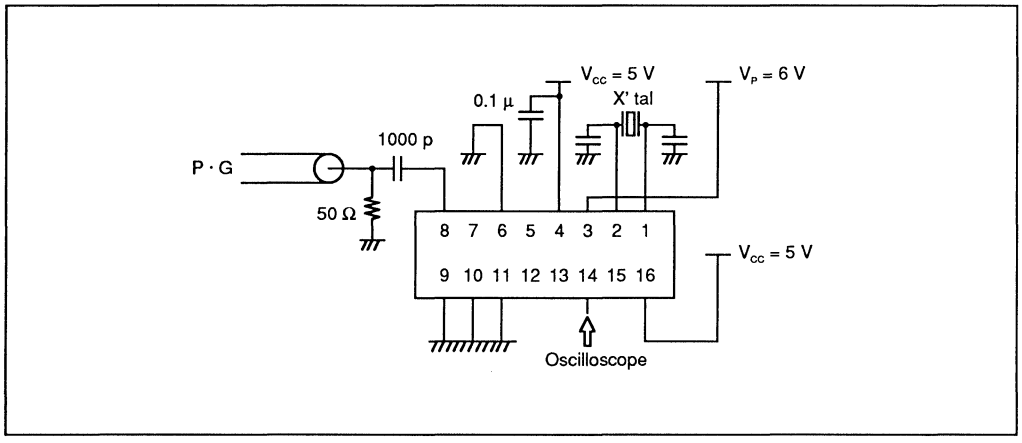
Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device from a socket
- Protect leads of the device using conductive sheet when handling PC boards on which devices are mounted.

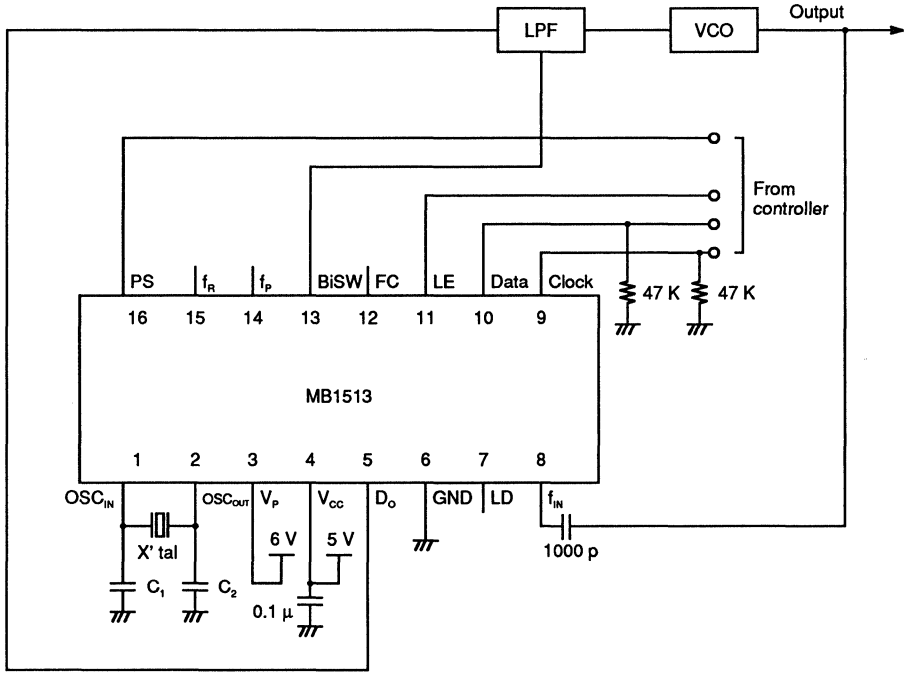
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	8.0	12.0	mA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5.0 V. Inputs are V_{CC} and outputs are open
Stand-by current		IPS	–	100	–	µA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5.0 V. The PS pin is grounded, remaining inputs are at V_{CC}, and outputs are open
Operating frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 100-pF capacitor connected
	OSC_{IN}	f_{OSC}	–	12	20	MHz	
Input sensitivity	f_{IN}	V_{fIN}	–10	–	6	dBm	
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE	I_{IH}	–	1.0	–	µA	
Low-level input current		I_{IL}	–	–1.0	–	µA	
	FC	I_{FC}	–	–60	–	µA	
Input current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	–	–	V	V_{CC} = 5 V
Low-level output voltage		V_{OL}	–	–	0.4	V	
High-impedance Cut off current	D_O	I_{OFF}	–	–	1.1	µA	V_{DO} = GND to 8 V $V_{CC} \leq V_P \leq 8$ V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	
		I_{OL}	1.0	–	–	mA	
Analog switch ON resistance		R_{ON}	–	25	–	Ω	

TEST CIRCUIT
(FOR MEASURING PRESCALER INPUT SENSITIVITY)



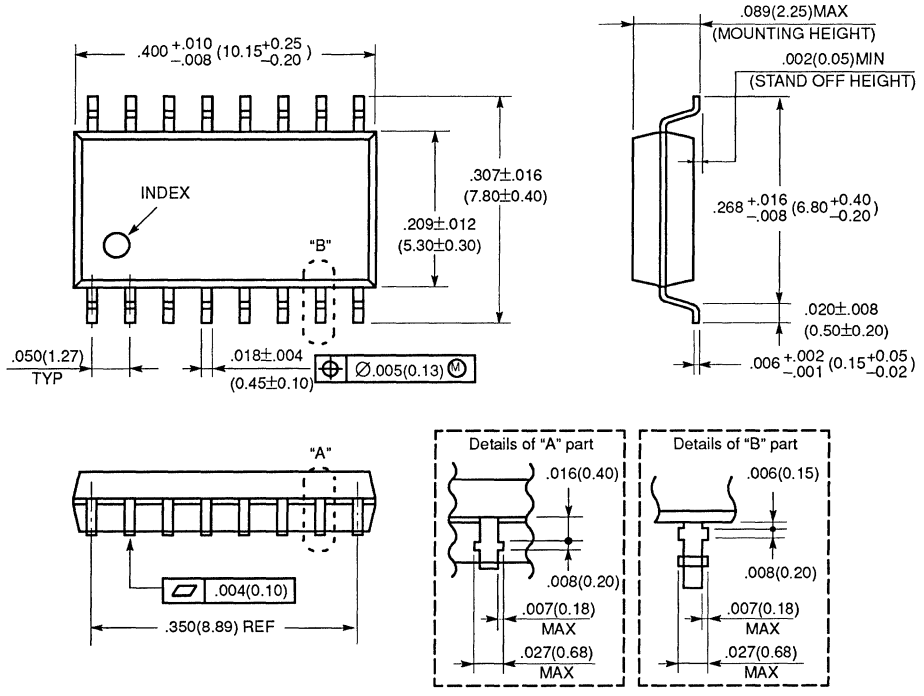
APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8 V
C_1, C_2 : Depend on the crystal parameters

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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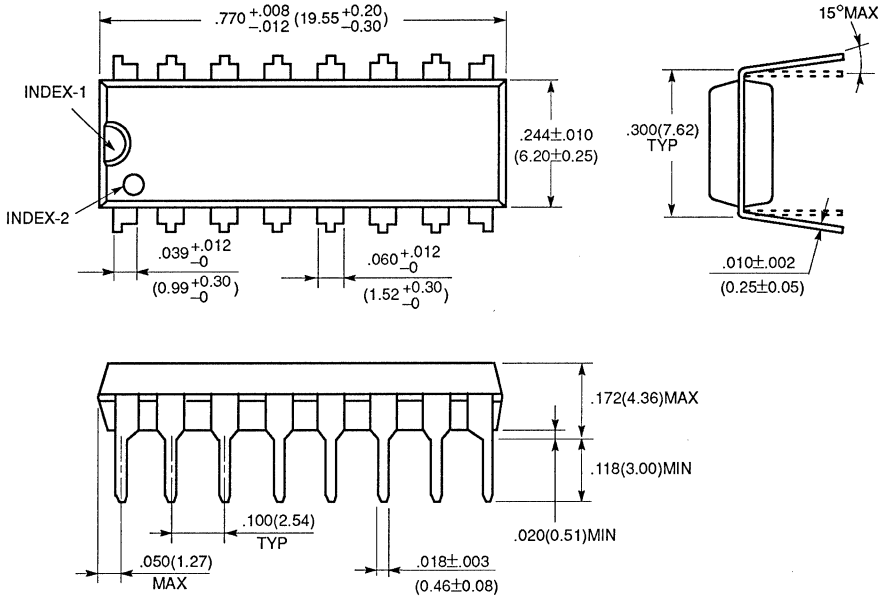
Dimensions in inches (millimeters)

3

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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Dimensions in
inches (millimeters)

October 1990
Edition 4.0

FUJITSU

DATA SHEET

MB1504/MB1504H/MB1504L
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 520MHz PRESCALER

The Fujitsu MB1504/MB1504H/MB1504L, utilizing BI-CMOS technology, is a single chip serial input PLL frequency synthesizer with pulse-swallow function.

The MB1504 series contain a 520MHz two modulus prescaler that can select either 32/33 or 64/65 divide ratio; control signal generator; 16-bit shift register; 15-bit latch; programmable reference divider (binary 14-bit programmable reference counter); 1-bit switch counter; phase comparator with phase inverse function; charge pump; crystal oscillator; 19-bit shift register; 18-bit latch; programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

The MB1504 operates on a low supply voltage (3V typ) and consumes low power (30mW at 520MHz).

MB1504 Product Line

	V_P Voltage	V_{OOP} Voltage	Lock up time	D_O Output Width	High-level Output Current	Low-level Output Current
MB1504	8V max	8.5V max	Middle speed	Middle	Middle	Middle
MB1504H	10V max	10.0V max	High speed	Low	High	Low
MB1504L	8V max	8.5V max	Low speed	High	Low	High

- High operating frequency: $f_{IN\ MAX}$=520MHz ($V_{IN\ MIN}$=0.20V_{P-P})
- On-chip prescaler
- Low power supply voltage: 2.7V to 5.5V (3.0V typ)
- Low power supply consumption: 30mW (3.0V, 520MHz operation)
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  - Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter (Divide ratio: 8 to 16383)
  - 1-bit switch counter (SW) Sets divide ratio of prescaler
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: T_A=−40°C to +85°C

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		−0.5 to +7.0	V
	V_{PH}	MB1504H	V_{CC} to 12.0	V
	V_P,V_{PL}	MB1504/1504L	V_{CC} to 10.0	
Output Voltage	V_{OUT}		−0.5 to V_{CC} +0.5	V
Open-drain Output	V_{OOPH}	MB1504H	−0.5 to 11.0	V
	V_{OOP},V_{OOPL}	MB1504/1504L	−0.5 to 9.0	
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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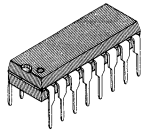
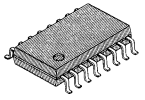
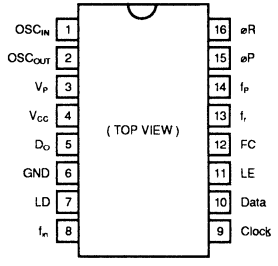


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M06

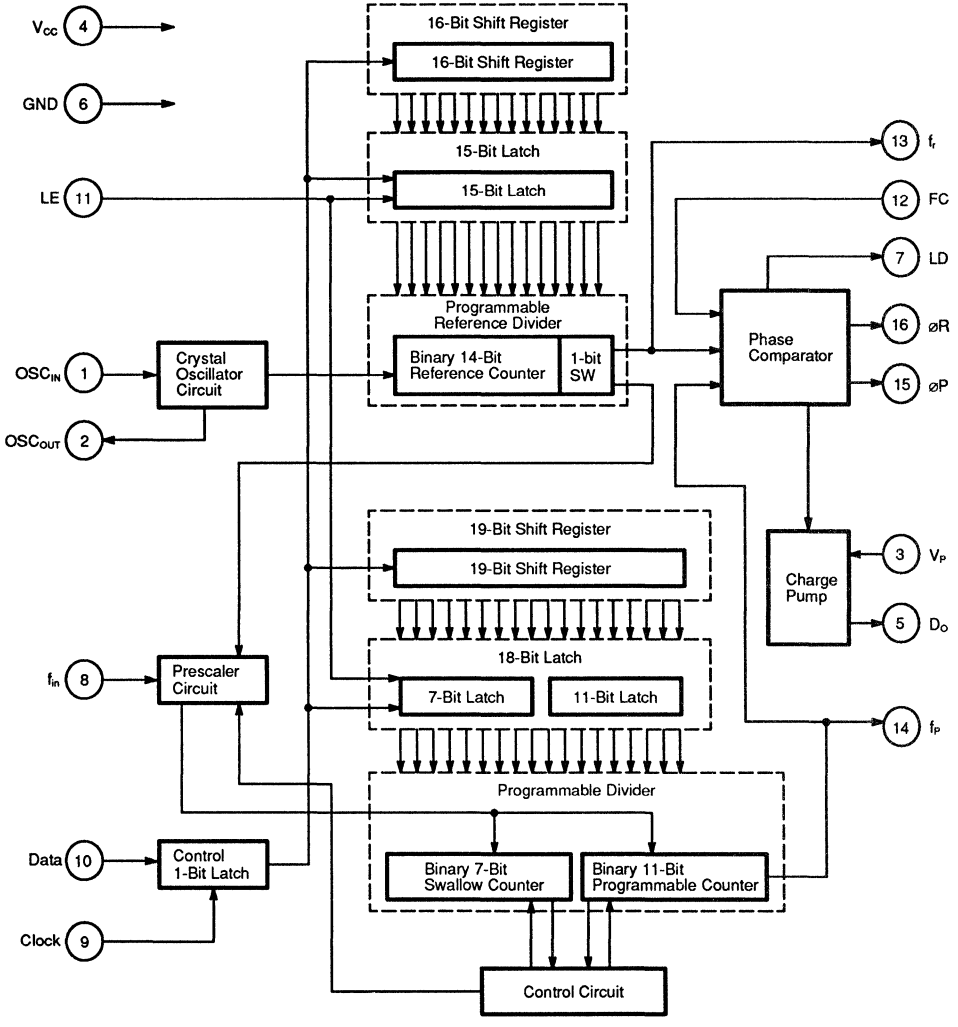
PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

MB1504/MB1504H/MB1504L BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	—	Power supply input for charge pump.
4	V_{CC}	—	Power supply voltage input.
5	D_O	O	Charge pump output. Phase characteristic can be inversed depending upon FC input.
6	GND	—	Ground.
7	LD	O	Phase comparator output. This pin outputs high when the phase is locked. While the phase difference of f_r and f_p exists, the output level goes low.
8	f_{in}	I	Prescaler input. The connection with an external VCO should be an AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Serial data of binary code input. The last bit of the data is a control bit. The last data bit specifies which latch is activated. When the last bit is high level and LE is high-level, data is transferred to 15-bit latch. When the last bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high level (or open), data stored in the shift register is transferred to latch depending on the control data.
12	FC	O	Phase selecting input of phase comparator (with internal pull up resistor). When FC is low level, charge pump and phase detector characteristics can be inversed.
13	f_r	O	Monitor pin of phase comparator input. It is the same as programmable reference divider output.
14	f_P	O	Monitor pin of phase comparator input. It is the same as programmable divider output.
15 16	øP øR	O O	Outputs for external charge pump. Phase characteristics can be inversed depending on FC input. øP pin is an N-channel open-drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is input using Data pin, Clock pin and LE pin, The 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.

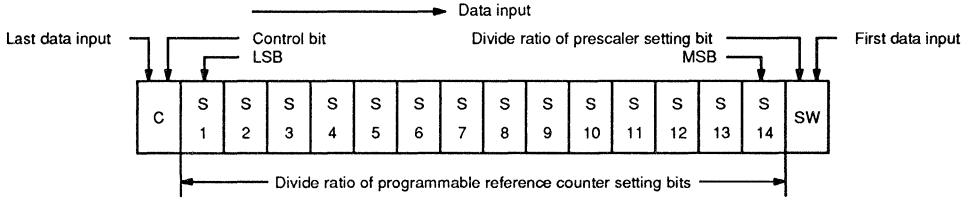
On rising edge of the clock shifts one bit of the data into the internal shift registers.

When load enable (LE) is high level (or open), data stored in shift resisters is transferred to 15-bit latch or 18-bit latch depending upon the control bit level.

Control data "H" ; Data is transferred into 15-bit latch.
Control data "L" ; Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



◎ 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

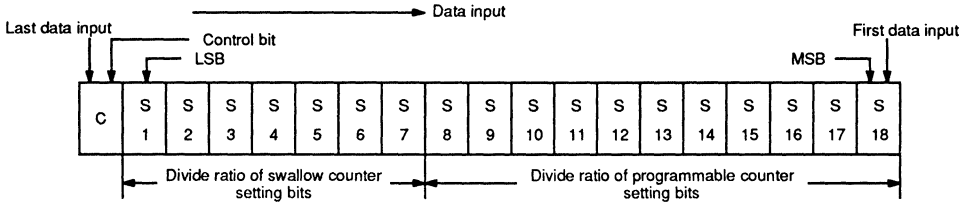
Divide ratio less than 8 is prohibited.
Divide ratio R: 8 to 16383

SW: Divide ratio of prescaler setting bit.
SW="H": 32
SW="L": 64
S_1 to S_{14}: Divide ratio of programmable reference counter setting bits (8 to 16383)
C: Control bit (Control bit is set to high.)

FUNCTIONAL DESCRIPTIONS

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown below.



◎ 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Divide ratio A : 0 to 127

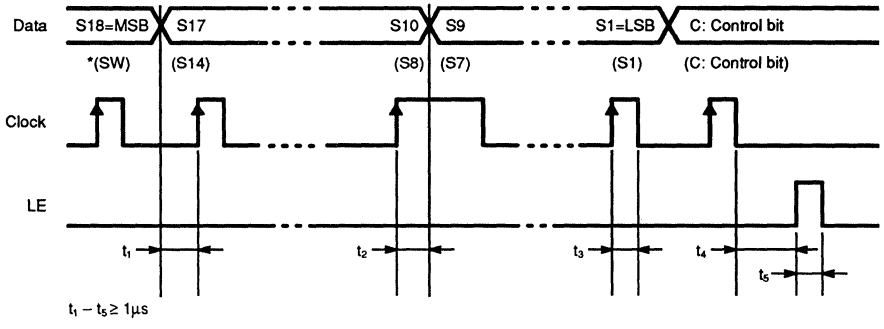
◎ 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Divide ratio less than 16 is prohibited.
Divide ratio N : 16 to 2047

S_8 to S_{18} : Divide ratio of programmable counter setting bits (16 to 2047)
S_1 to S_7 : Divide ratio of swallow counter setting bits (0 to 127)
C: Control bit (Control bit is set to low.)
Dara is input from MSB data.

SERIAL DATA INPUT TIMING



On the rising edge of the clock shifts one bit of the data into the shift registers.
Parenthsis data is used for setting the divide ratio of the programmable reference divider.

PHASE CHARACTERISTICS

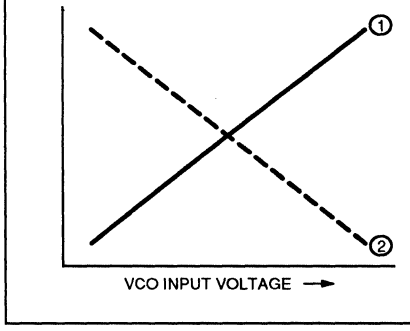
FC pin (pin 12) is provided to inverse the phase comparator characteristics. The characteristics of internal charge pump output (D_O), phase detector outputs (øR, øP) can be inversed depending upon FC input data. Outputs are shown below.

	FC=H (or open)			FC=L		
	D_O	øR	øP	D_O	øR	øP
$f_r > f_p$	H	L	L	L	H	Z
$f_r < f_p$	L	H	Z	H	L	L
$f_r = f_p$	Z	L	Z	Z	L	Z

Note: Z=(High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ① , FC should be set high or open circuit;
When VCO characteristics are like ② , FC should be set Low.

VCO CHARACTERISTICS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}		2.7	3.0	5.5	V
	V_{PH}	MB1504H	V_{CC}		10.0	V
	V_P, V_{PL}	MB1504 MB1504L	V_{CC}		8.5	
Open-drain Output	V_{OOPH}	MB1504H	V_{CC}		10.0	V
	V_{OOP}, V_{OOPL}	MB1504 MB1504L	V_{CC}		8.5	
Input Voltage	V_{IN}		GND		V_{CC}	V
Operating temperature	T_A		–40		+85	°C

3

ELECTRICAL CHARACTERISTICS

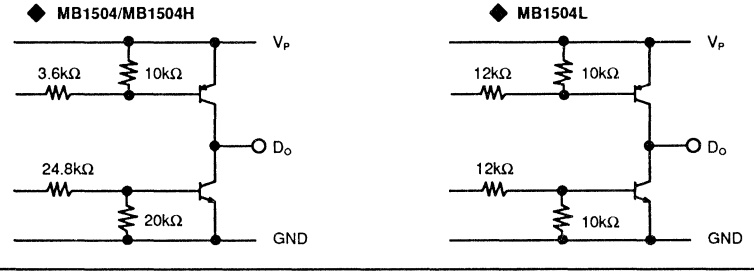
(V_{CC}=2.7 to 5.5V, T_A=–40 to +85°C)

Parameter	Pin Name	Symbol	Condition	Value Min	Value Typ	Value Max	Unit
Power Supply Current	V_{CC}	I_{CC}	*1	—	10	—	mA
Operating Frequency	f_{in}	f_{IN}	*2	10	—	520	MHz
	OSC_{IN}	f_{OSC}		—	12	20	MHz
Input Sensitivity	f_{in}	V_{fin1}	V_{CC}=2.7 ~ 4.0V	–10	—	6	dBm
		V_{fin2}	V_{CC}=4.0 ~ 5.5V	–4	—	6	dBm
	OSC_{IN}	V_{IN}		0.5	—	—	V_{P-P}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		0.7xV_{CC}	—	—	V
Low-level Input Voltage		V_{IL}		—	—	0.3xV_{CC}	V
High-level Input Current	Data, Clock	I_{IH}		—	1.0	—	µA
Low-level Input Current		I_{IL}		—	–1.0	—	µA
Input Current	OSC_{IN}	I_{IN}		—	±50	—	µA
	LE, FC	I_{LE}		—	–60	—	µA
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3.0V	2.4	—	—	V
Low-level Output Voltage		V_{OL}		—	—	0.4	V
N-channel Open-drain Cutoff Current	øP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$	—	—	1.1	µA
High-level Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	—	—	mA
Low-level Output Current		I_{OL}		1.0	—	—	mA
High-level Output Current	D_O	I_{DOHH}	MB1504H; V_{CC}=3V, V_P=12V, T_A=25°C	–2.2	–4.5	—	mA
		I_{DOH}	MB1504; V_{CC}=3V, V_P=6V, T_A=25°C	–0.5	–2.0	—	mA
		I_{DOHL}	MB1504L; V_{CC}=3V, V_P=6V, T_A=25°C	–0.5	–1.1	–2.2	mA
Low-level Output Current		I_{DOLH}	MB1504H; V_{CC}=3V, V_P=12V, T_A=25°C	2.2	6.0	—	mA
		I_{DOL}	MB1504; V_{CC}=3V, V_P=6V, T_A=25°C	1.5	6.0	—	mA
		I_{DOLL}	MB1504L; V_{CC}=3V, V_P=6V, T_A=25°C	4.5	12.0	—	mA
Leakage Current	D_O, øP	D_{OZ}	V_{CC}=3V, V_P=12V, T_A=25°C	—		1.0	µA

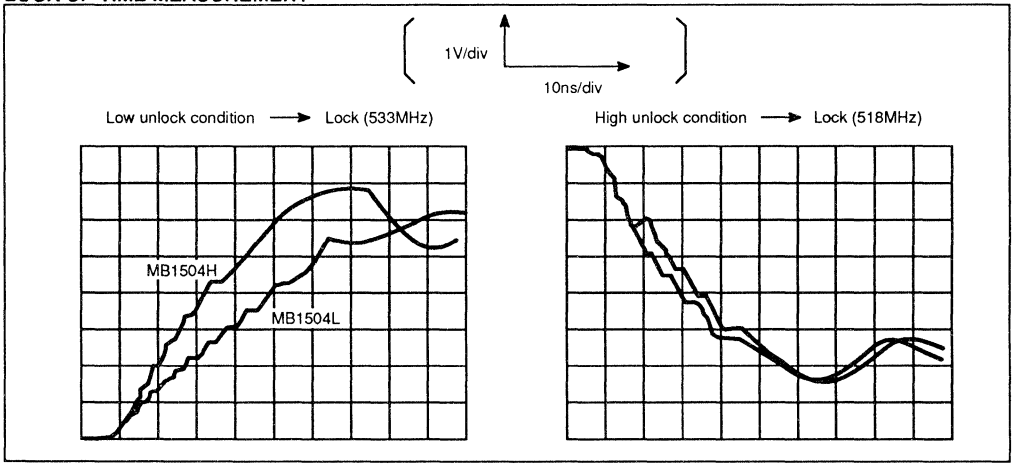
Note: *1 V_{CC}=3.0V, f_{IN}=520MHz, f_{OSC}=12MHz crystal.
Inputs are grounded except f_{IN}, and outputs are open.
*2 Input coupling capacitor 1000pF is connected.

TYPICAL CHARACTERISTICS CURVES

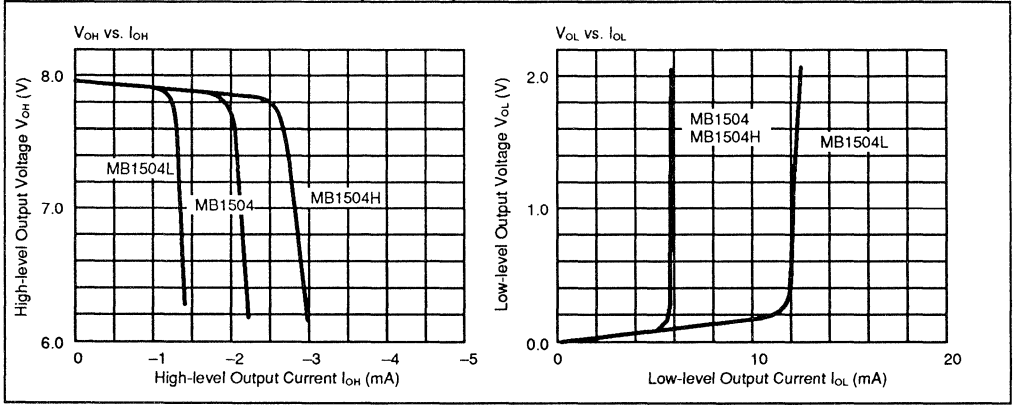
CHARGE PUMP CHARACTERISTICS



LOCK UP TIME MEASUREMENT



DO PIN OUTPUT CURRENT CURVES (TYPICAL)



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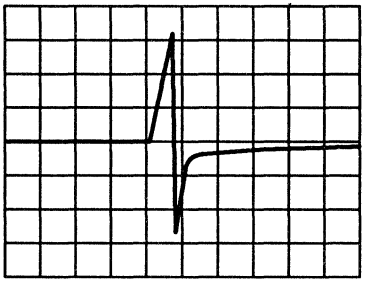
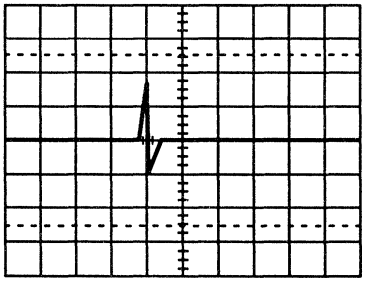
Do PIN OUTPUT WAVEFORM AT LOCK CONDITION

Output Waveform

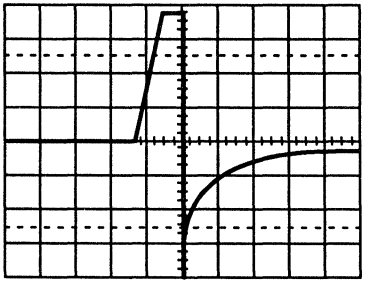
MB1504



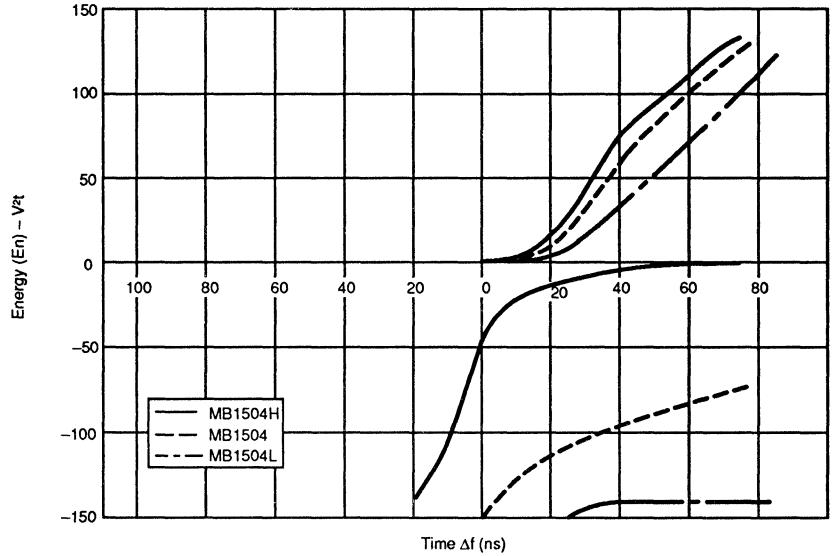
MB1504H

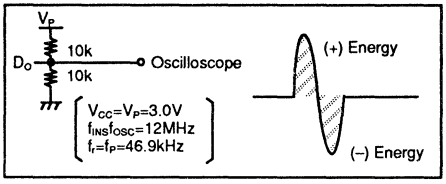


MB1504L



PHASE CHARACTERISTICS (Δf vs. Do OUTPUT ENERGY)





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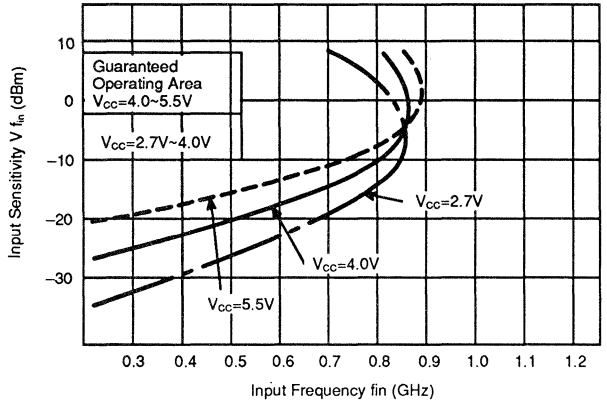
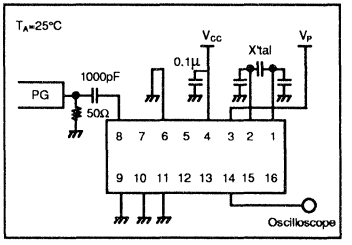
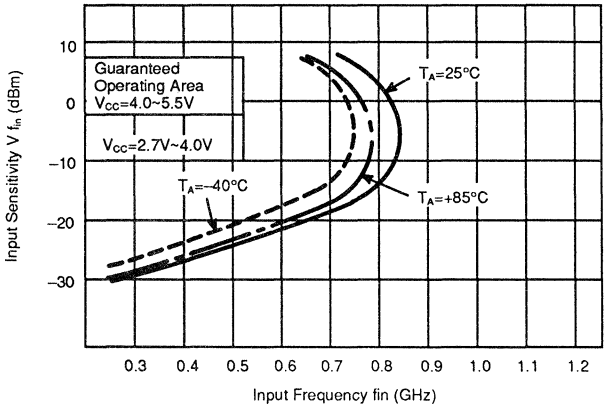
INPUT SENSITIVITY

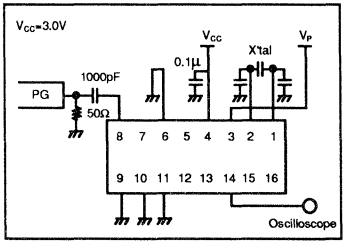
Input Sensitivity vs. Input Frequency (Supply Voltage Dependence)



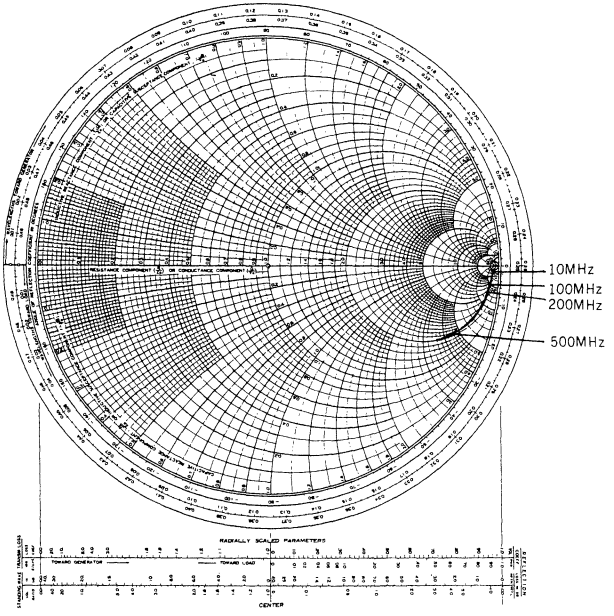


Input Sensitivity vs. Input Frequency (Temperature Dependence)



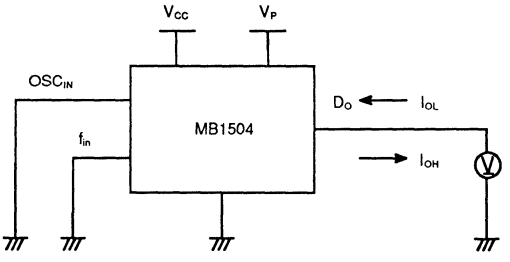


INPUT IMPEDANCE



TEST CIRCUIT

D_O Pin Output Current (I_{OH}, I_{OL}) Measurement



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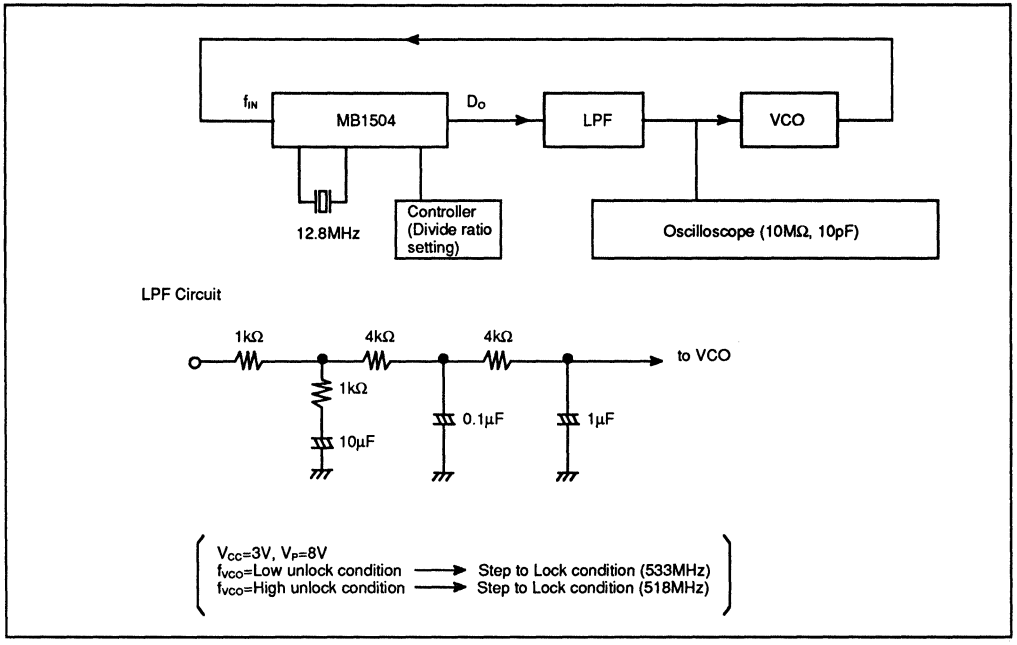
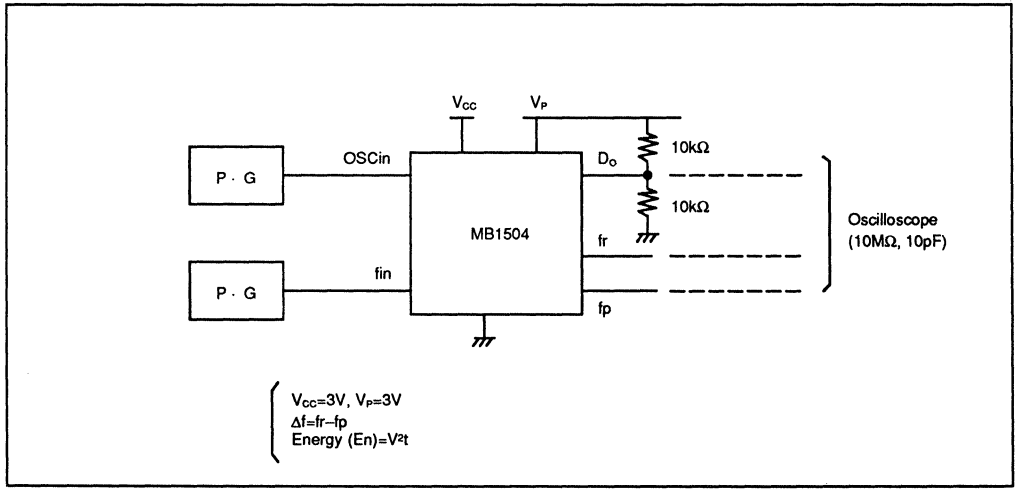
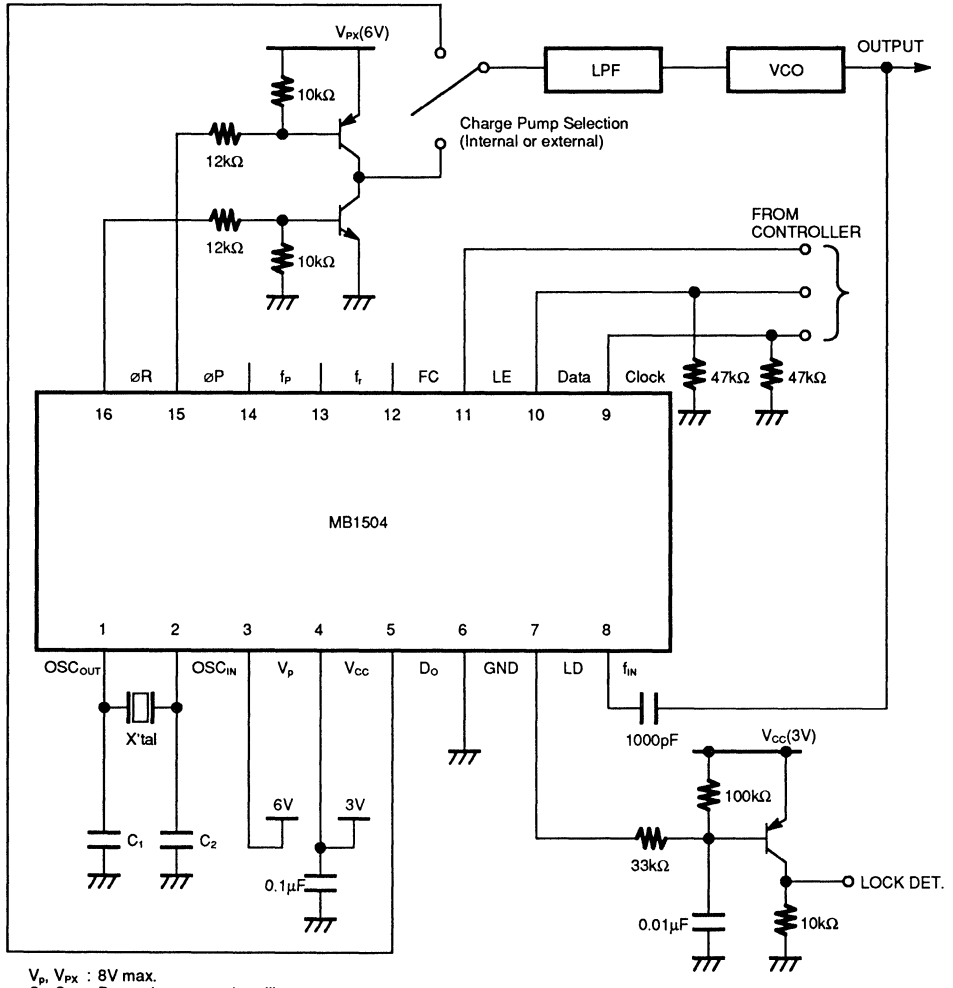
Lock up Time Measurement



Phase Characteristics Measurement



TYPICAL APPLICATION EXAMPLE



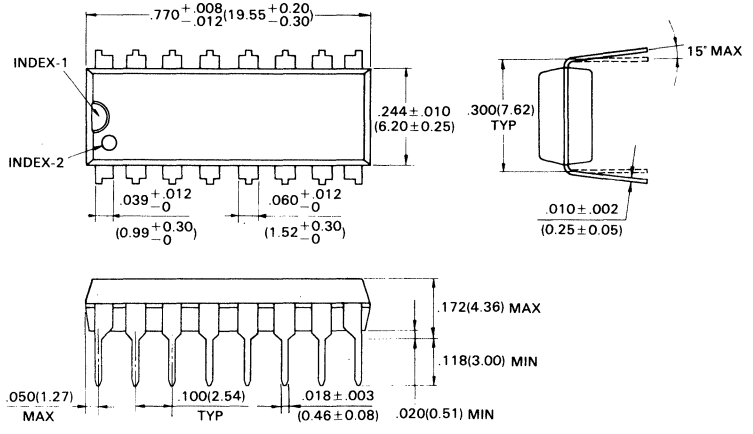
V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
øP : Open drain output

3

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)



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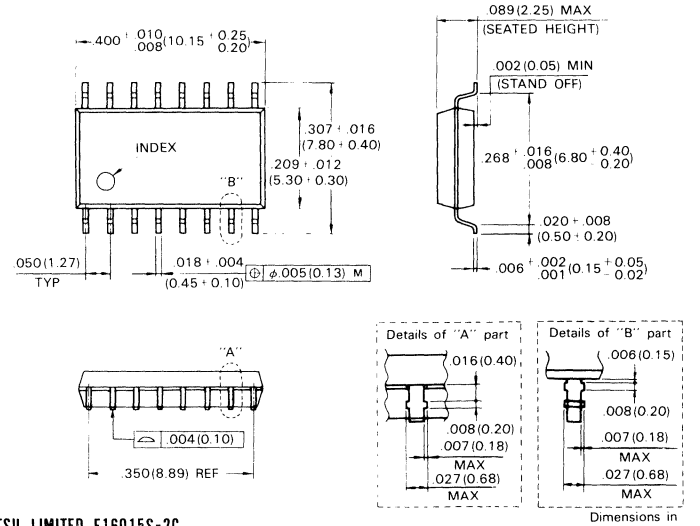
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-16P-M06)



Dimensions in inches (millimeters)

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March 1990
Edition 1.0

FUJITSU

DATA SHEET

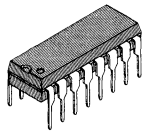
MB1505
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 600MHz PRESCALER

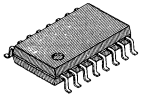
PRELIMINARY

The Fujitsu MB1505, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB1505 contains a 600MHz two modulus prescaler that can select of either 32/33 or 64/65 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.
It operates supply voltage of 5V typ. and achieves very low supply current of 6mA typ. realized through the use of Fujitsu Advanced Process Technology.

- High operating frequency: $f_{IN\ MAX}$=600MHz ($V_{IN\ MIN}$=–4dBm)
- Pulse swallow function: 32/33 or 64/65
- Low supply current: I_{CC}=6mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 63
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic DIP Package (Suffix : –P)
  16-pin Plastic Flat Package (Suffix : –PF)

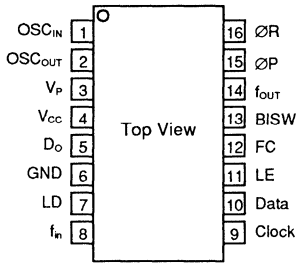


PLASTIC PACKAGE
DIP–16P–M04



PLASTIC PACKAGE
FPT-16P–M02

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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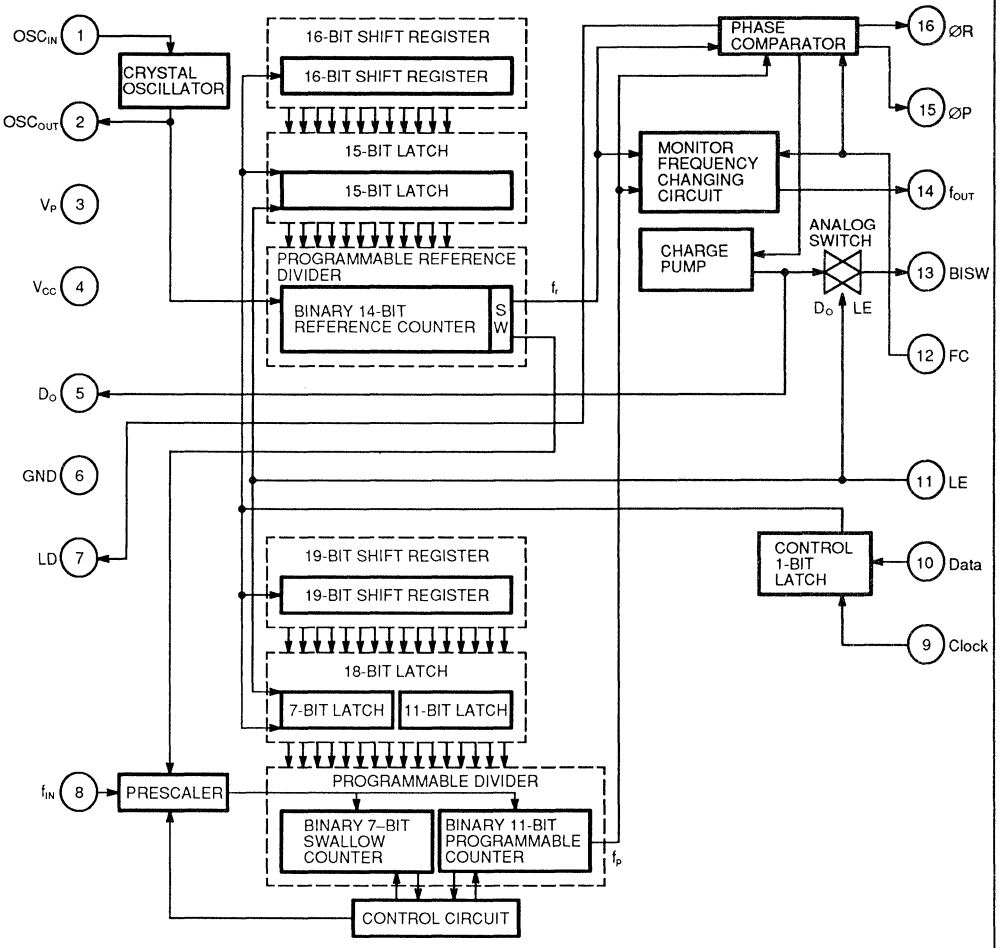
3

MB1505 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	–	Power supply input for charge pump and analog switch.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
6	GND	–	Ground.
7	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
8	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{out} pin (test pin) output level, f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
14	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
15 16	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.

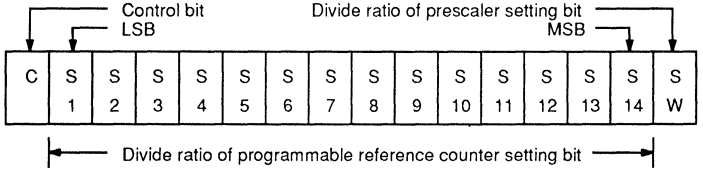
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



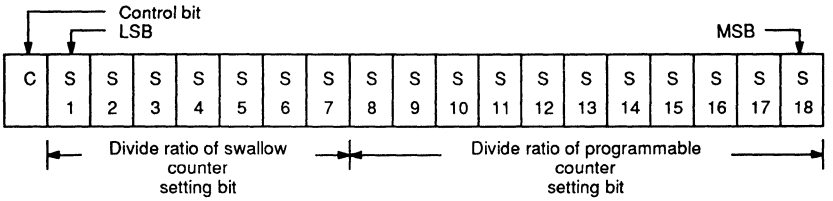
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 32/33
SW=L : 64/65
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter.
Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
63	0	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 63
S7 should be set to zero

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

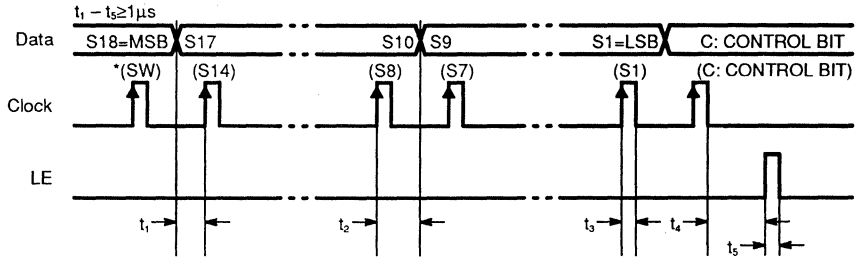
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 63)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{vco} = [(PxN)+A] \times f_{osc} \div R$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 63$, $A < N$)
f_{osc}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)
P: Preset modulus of external dual modulus prescaler (32 or 64)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

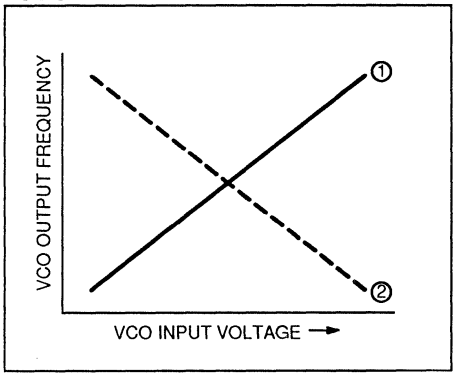
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level ($\phi R, \phi P$) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, $\phi R, \phi P$) and FC input level are shown below.

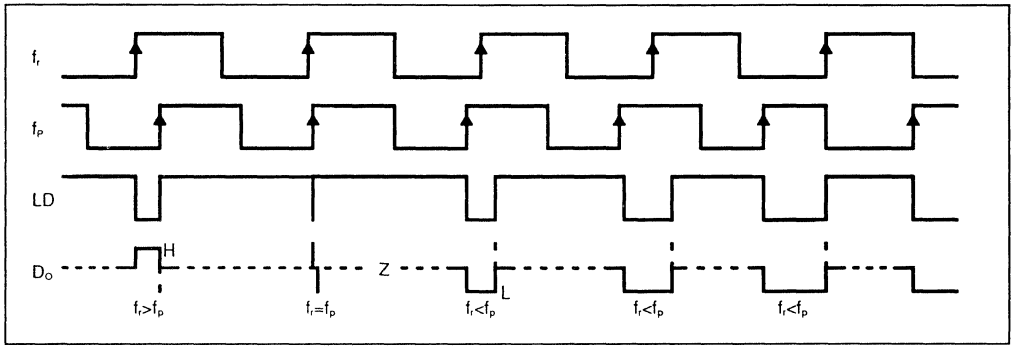
	FC=H or open				FC=L			
	D_O	ϕR	ϕP	f_{out}	D_O	ϕR	ϕP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.



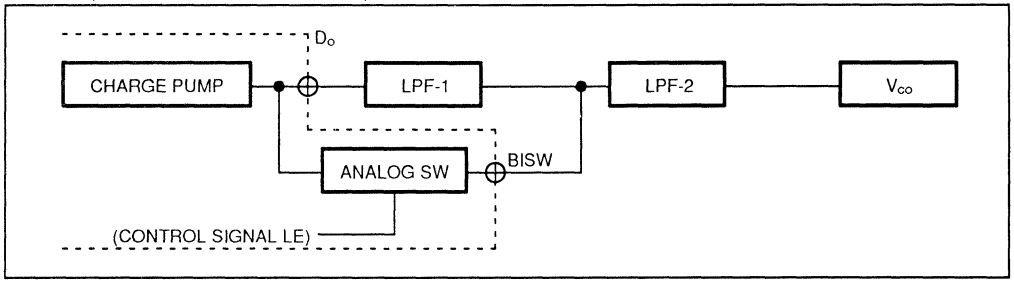
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode) : Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

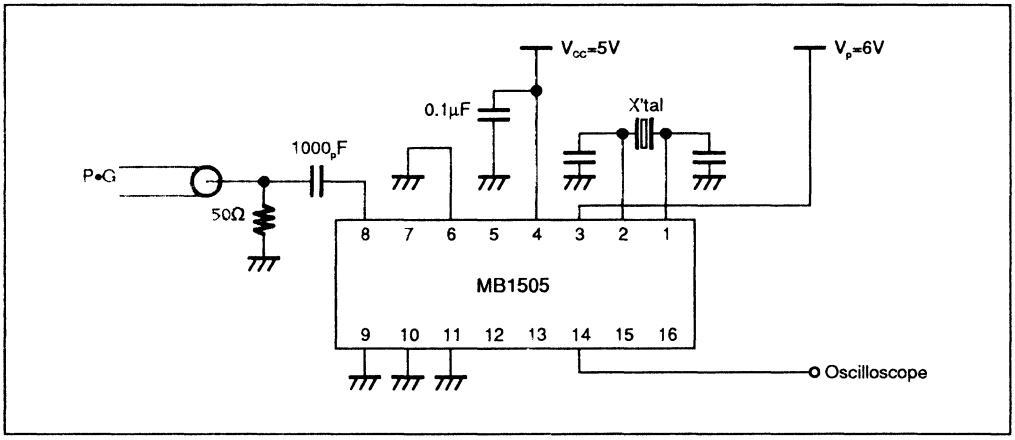
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	−40		85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		6.0		mA
Operating Frequency	f_{in}	f_{in}	Note 2	10		600	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in}	Vf_{in}		−4		6	dBm
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except fi_n and OSC_{IN}	V_{IH}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			−1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			−60		µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	V_P=V_{CC} to 8V V_{OOP}=GND to 8V			1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		−1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistor		R_{ON}			25		Ω

NOTE 1: f_{in}=600MHz, OSC_{IN}=12MHz, V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT



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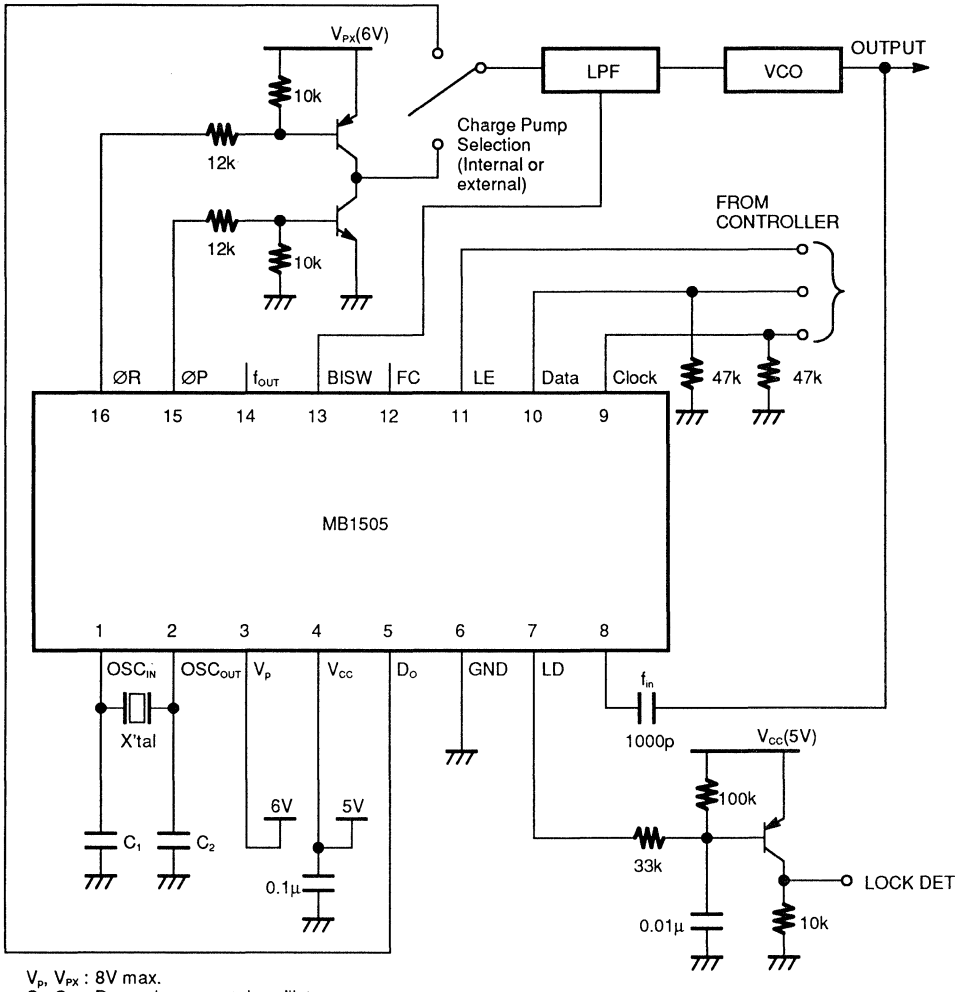
TYPICAL APPLICATION EXAMPLE

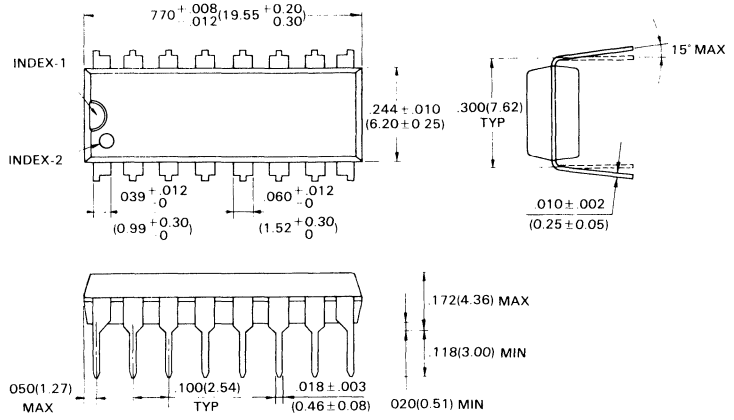


V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)



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Dimensions in inches (millimeters)

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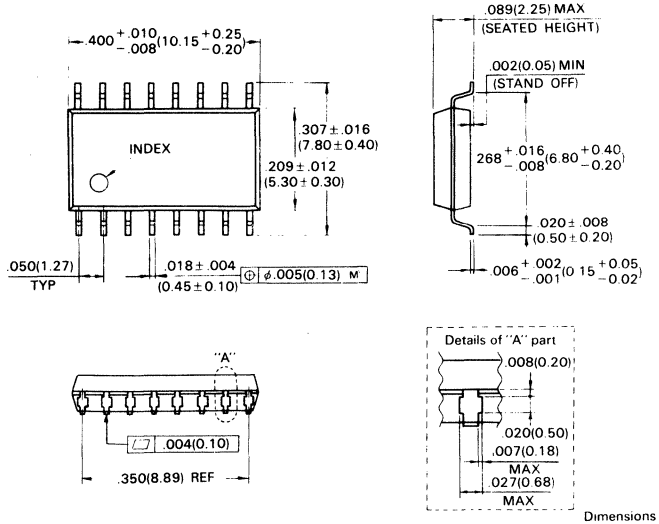
16-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-16P-M02)



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Dimensions in inches (millimeters)

March 1991
Edition 3.0

FUJITSU

DATA SHEET

MB1507
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

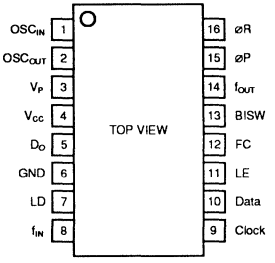
SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 2.0GHz PRESCALER

The Fujitsu MB1507 is a single chip serial input PLL frequency synthesizer designed for BS tuner and cellular telephone applications.
It contains a 2.0 GH_Z dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.
It operates supply voltage of 5.0V typ. and dissipates 18mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: $f_{IN\ MAX}$=2.0GHz ($V_{IN\ MIN}$=–4dBm)
- Pulse swallow function: 128/129 or 256/257
- Low supply current: I_{CC}=18mA typ.
- Serial input 19-bit programmable divider consisting of:
  - Binary 8-bit swallow counter: 0 to 255
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) sets divide ration of prescaler
- On-chip analog switch achieves fast lock up time
- Two types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic Flat Package (Suffix: –PF)

PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 8.0	V
Output Current	I_{OUT}	+10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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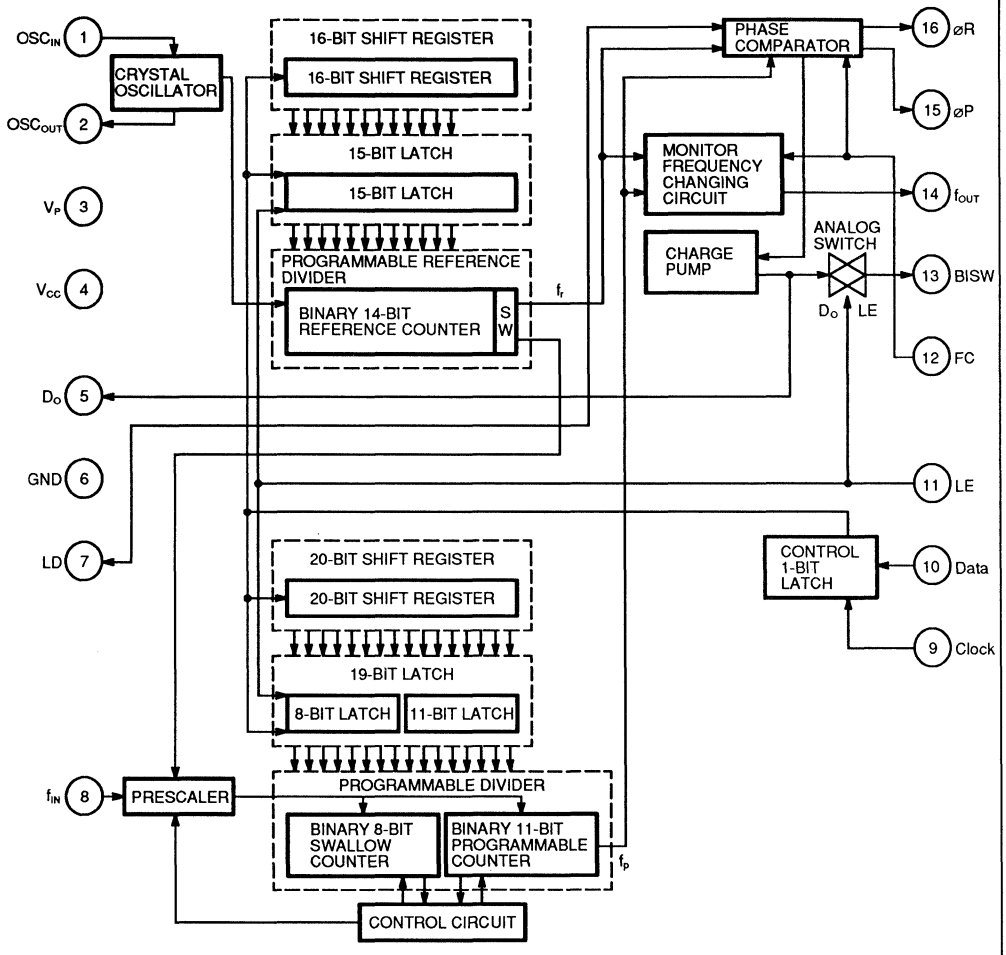
3

MB1507 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 2	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	–	Power supply input for charge pump and analog switch.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. The characteristics of charge pump are reversed depending upon FC input.
6	GND	–	Ground.
7	LD	O	Phase comparator output. Normally the output level is high level. While the phase difference of f_r and f_p exists, the output becomes low level.
8	f_{IN}	I	Prescaler input. The connection with VCO should be AC connection.
9	Clock	I	Clock input for 20-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into shift registers
10	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 19-bit latch.
11	LE	I	Load enable input (with pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
12	FC	I	Phase select input of phase comparator (with pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator are reversed. FC pin input signal controls f_{out} pin (test pin) output level, f_r or f_p.
13	BISW	O	Analog switch output. Usually BISW pin is set at high-impedance state. When internal analog switch in ON (LE pin is set at high level), this pin outputs internal charge pump output.
14	f_{OUT}	O	Monitor pin of phase comparator input. f_{out} pin outputs programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
15 16	øP øR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. øP pin is N-channel open drain output.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15–bit programmable reference divider and 19–bit programmable divider, respectively.
Binary serial data is input to Data pin.
Each rising edge of the clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15–bit latch.
Control data "L" data is transferred into 19–bit latch.

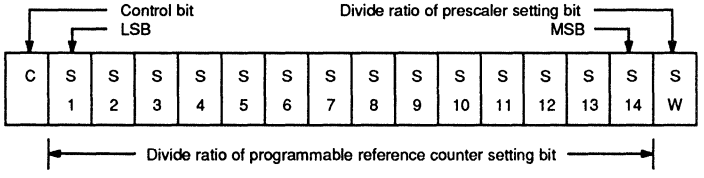
THE DIVIDE RATIO SETTING

$f_{VCO}=[(MxN)+A]xf_{OSC}+R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset modulus of external dual modulus prescaler (128 or 256)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 8-bit swallow counter ($0 \leq A \leq 255$, $A<N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



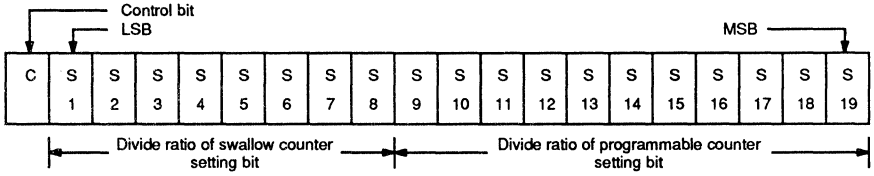
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 128/129
SW=L : 256/257
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 20-bit shift register, 19-bit latch, 8-bit swallow counter and 11-bit programmable counter. Serial 20-bit data format is shown below.



8-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S8	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

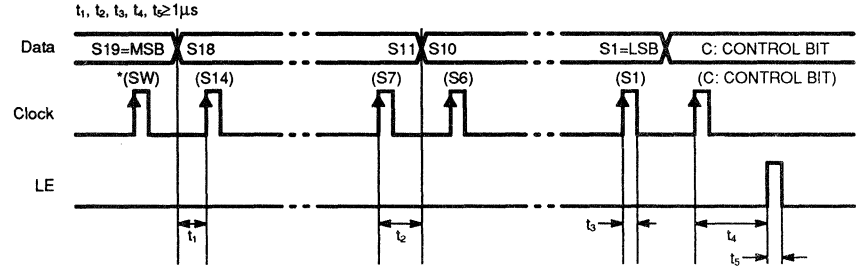
NOTE: Divide ratio: 0 to 255

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S8: Swallow counter divide ratio setting bit. (0 to 255)
S9 to S19: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets to low level).
Data is input from MSB side.

SERIAL DATA INPUT TIMING



NOTES: The data noted in parenthesis is used for setting divide ratio of programmable reference divider.
On rising edge of clock, one bit of data shifts into the shift register.

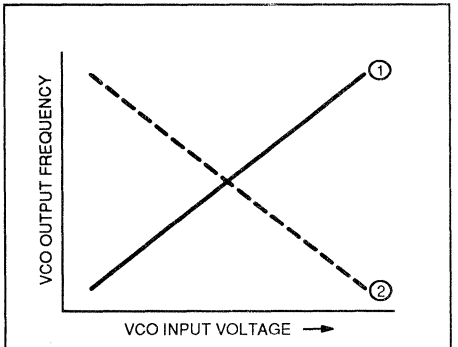
PHASE CHARACTERISTICS

FC pin is provided to change phase polarity of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (øR, øP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level.

	FC=H or open				FC=L			
	D_O	øR	øP	f_{out}	D_O	øR	øP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)

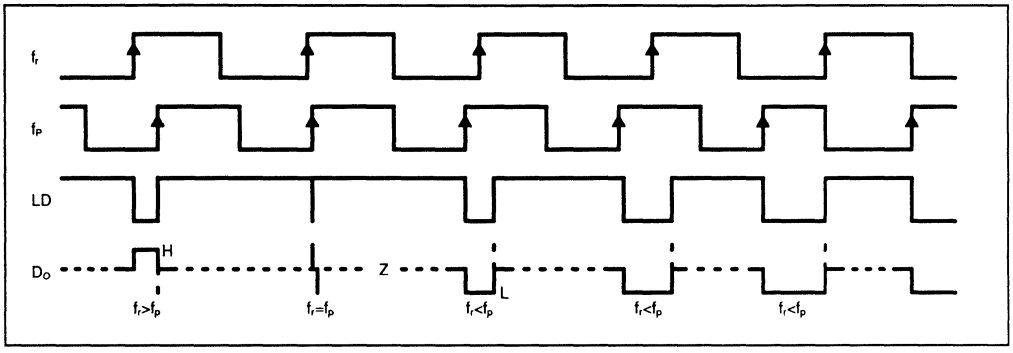
Note: Z=(High impedance)

VCO POLARITY



Depending upon VCO polarity, FC pin should be set accordingly:
When VCO polarity are like ①, FC should be set High or open circuit;
When VCO polarity are like ②, FC should be set Low.

PHASE DETECTOR OUTPUT WAVEFORM (FC=High)



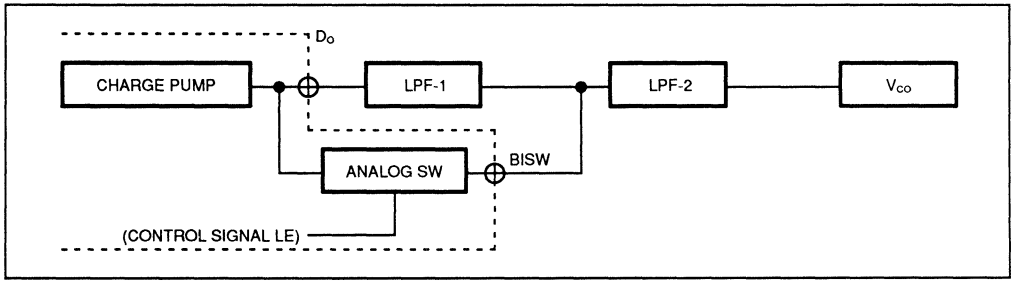
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) is connected to BISW pin. When the analog switch is OFF, BI-SW pin is set to high-impedance state.

LE	Analog Switch
H(Changing the divide ratio of internal prescaler)	ON
L(Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	–40	—	85	°C

HANDLING PRECAUTIONS

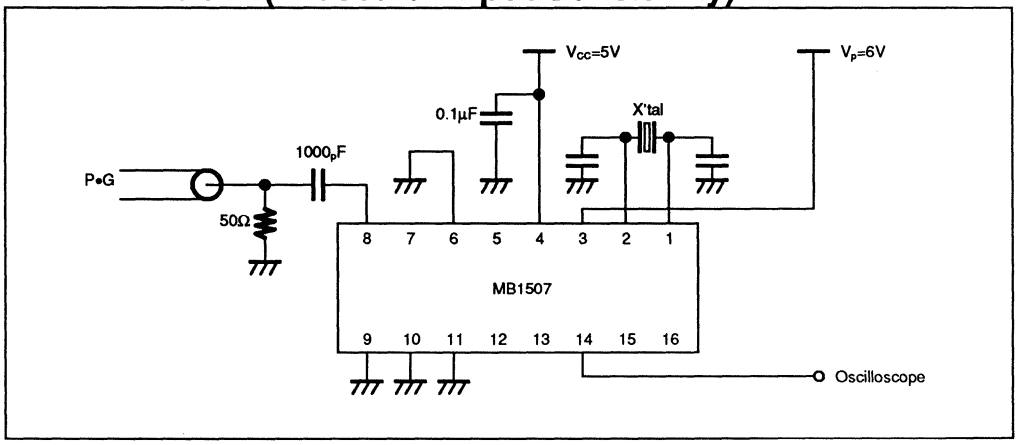
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

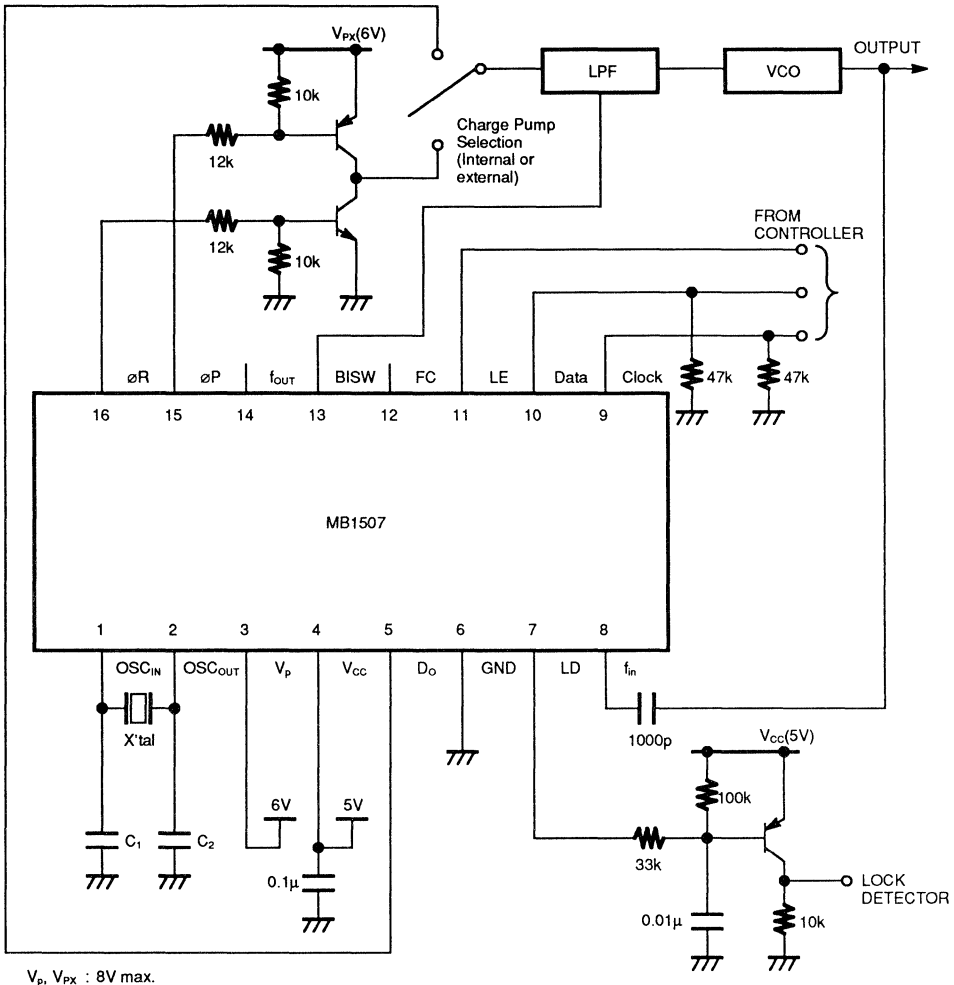
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1	—	18.0	25.0	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10	—	2000	MHz
	OSC_{IN}	f_{osc}	—	—	12	20	MHz
Input Sensitivity	f_{in}	V_{fin}	50Ω	–4	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	—	V_{CC}x0.7	—	—	V
Low-level Input Voltage		V_{IL}	—	—	—	V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}	—	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	—	–1.0	—	µA
Input Current	OSC_{IN}	I_{OSC}	—	—	+50	—	µA
	LE, FC	I_{LE}	—	—	–60	—	µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4	—	—	V
Low-level Output Current		V_{OL}		—	—	0.4	V
High Impedance Cutoff Current	D_O, øP	I_{OFF}	V_P=V_{CC} to 8V V_{OOP}=GND to 8V	—	—	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}	—	–1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Analog Switch On Resistance		R_{ON}	—	—	25	—	Ω

NOTE 1: f_{in}=2.0GHz, f_{osc} =12MHz X'tal V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

TEST CIRCUIT (Prescaler Input Sensitivity)



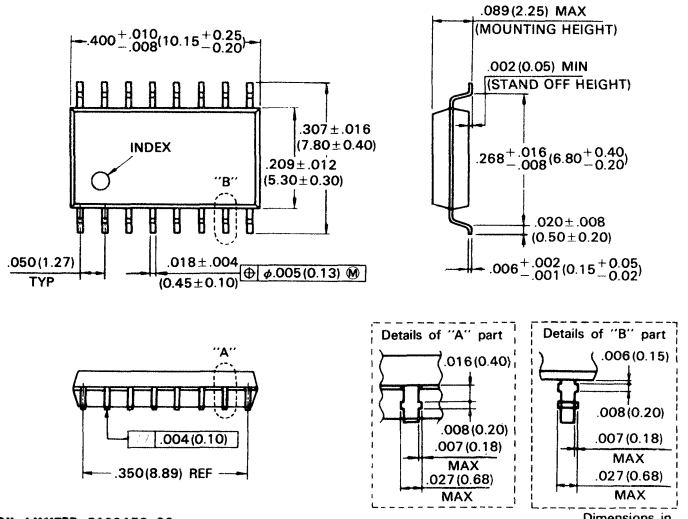
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With pull up resistor
øP : Open drain output

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-16P-M06)



Dimensions in inches (millimeters)

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April 1991
Edition 2.0

FUJITSU

DATA SHEET

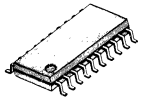
MB1508
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER ON CHIP 2.5GHz PRESCALER

The Fujitsu MB1508 on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system, and TV tuner applications.

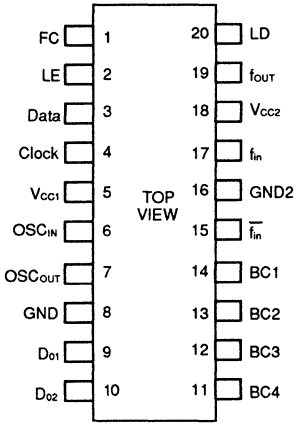
It operates supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- Power supply voltage: V_{CC} = 4.5 to 5.5V
- High operating frequency: f_{in} = 2.5GHz (V_{in} = –4dBm)
- 2.5GHz dual modulus prescaler: P = 256/272, 512/528
- Low power supply current: I_{CC} = 16mA typ.
- Programmable reference divider consisting of:
  Binary 2–bit programmable reference counter (R = 256, 512, 1024, 2048)
- Programmable divider consisting of:
  Binary 5–bit swallow counter (A = 0 to 31)
  Binary 12-bit programmable counter (N = 32 to 4095)
- Wide operating temperature: T_A = –40 to +85°C
- Plastic 20-pin flat package (Suffix: –PF)



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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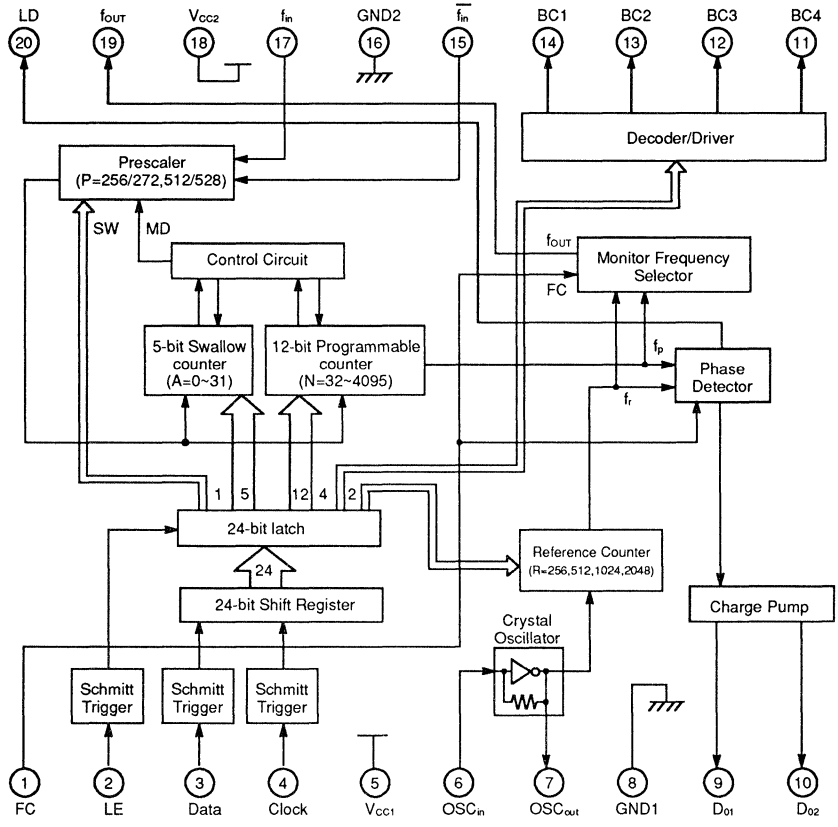
MB1508 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either fr or fp. See Functional Description section, Phase Detector Characteristics.
2	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.
3	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.
4	Clock	I	Clock input pin of the 24–bit shift register. This pin involves a schmitt trigger circuit. Each rising edge of the clock shifts one bit of data into the shift register.
5	V_{CC1}	–	PLL power supply voltage input pin.
6 7	OSC_{IN} OSC_{OUT}	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.
8	GND1	–	PLL ground pin.
9 10	D_{O1} D_{O2}	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.
11 12 13 14	BC4 BC3 BC2 BC1	O O O	Band switching output pins. (Open–collector output) Output is controlled by a band bit data, individually. BCX–bit=H : BCX output transistor is ON. BCX–bit=L : BCX output transistor is OFF. (X=1 to 4)
15	$\overline{f_{in}}$	I	Complementary input pin of f_{in}. Please connect to GND through a capacitor.
16	GND2	–	Prescaler ground pin.
17	f_{in}	I	Prescaler input pin, This signal is AC coupled.
18	V_{CC2}	–	Prescaler power supply voltage input pin.
19	f_{OUT}	O	Monitor pin of the phase detector input. f_{OUT} pin outputs either of the programmable reference divider output frequency fr or programmable divider output frequency fp depending upon the FC pin input level. FC pin: H → fout output signal: fr; FC pin: L → fout output signal: fp
20	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

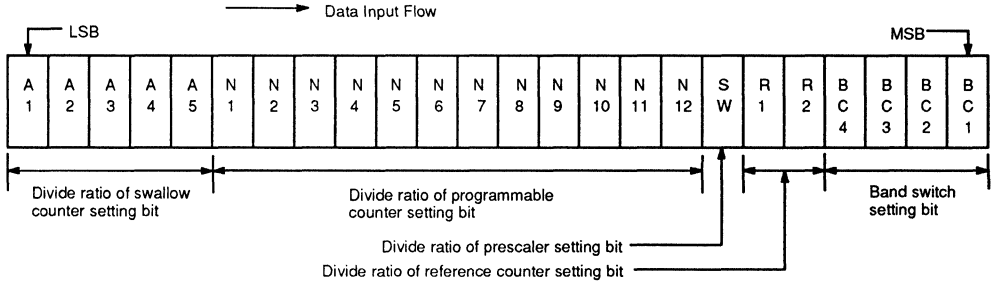
$f_{vco} = \{(P \times N) + (16 \times A)\} \times f_{osc} + R$

f_{vco}: Output frequency of an external voltage controlled oscillator (VCO)
P: Preset divide ratio of an internal dual modulus prescaler (256 or 512)
N: Preset divide ratio of binary 12-bit programmable counter (32 to 4095)
A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
f_{osc}: Reference oscillator frequency
R: Preset divide ratio of reference counter (256,512,1024,2048)

SERIAL DATA I NPUT

Each rising edge of the clock shifts one bit of data into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

The data format of 24 bits is shown below.



5-bit swallow counter divide ratio (A1 to A5)

Divide ratio A	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

12-bit programmable counter divide ratio (N1 to N12)

Divide ratio	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
32	0	0	0	0	0	0	1	0	0	0	0	0
33	0	0	0	0	0	0	1	0	0	0	0	1
34	0	0	0	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:
4095	1	1	1	1	1	1	1	1	1	1	1	1

FUNCTIONAL DESCRIPTIONS

Reference counter divide ratio (R1 to R2)

Divide ratio	R	R
R	2	1
256	0	0
512	0	1
1024	1	0
2048	1	1

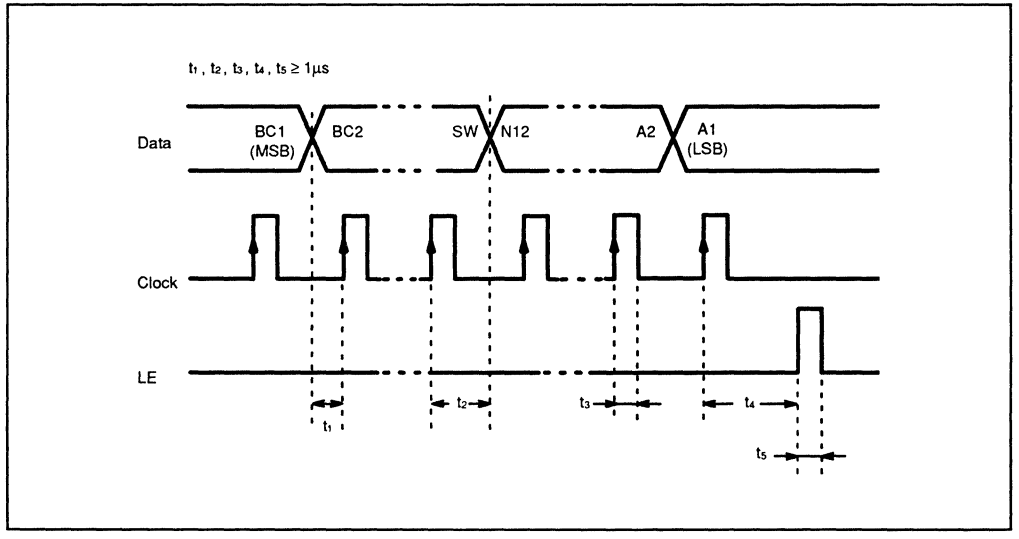
Prescaler divide ratio (SW)

When divide ratio of prescaler setting bit is high, divide ratio of 256/272 is selected.
When divide ratio of prescaler setting bit is low, divide ratio of 512/528 is selected.

Band Switch Setting (BC1 to BC4)

When band switch setting bit is high, output is ON.
When band switch setting bit is low, output is OFF.

SERIAL DATA INPUT TIMING



Note: Each rising edge of the clock shifts one bit of data into the shift register.
When LE is high, the data stored in the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (charge pump output) can be reversed depending upon the FC pin. input level. Monitor pin (fout) output level is selected by the FC pin input level as well.

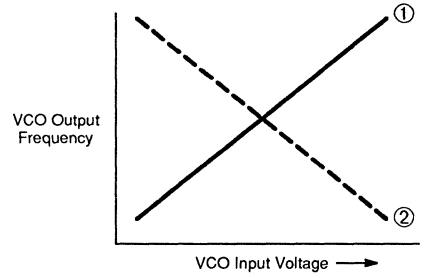
	FC = H (or open)		FC = L	
	D_{O1}, D_{O2}	fout	D_{O1}, D_{O2}	fout
fr > fp	H	Outputs programmable reference divider output frequency fr.	L	Outputs programmable divider output frequency fp.
fr = fp	Z		Z	
fr < fp	L		H	

Note:
Z: High-impedance

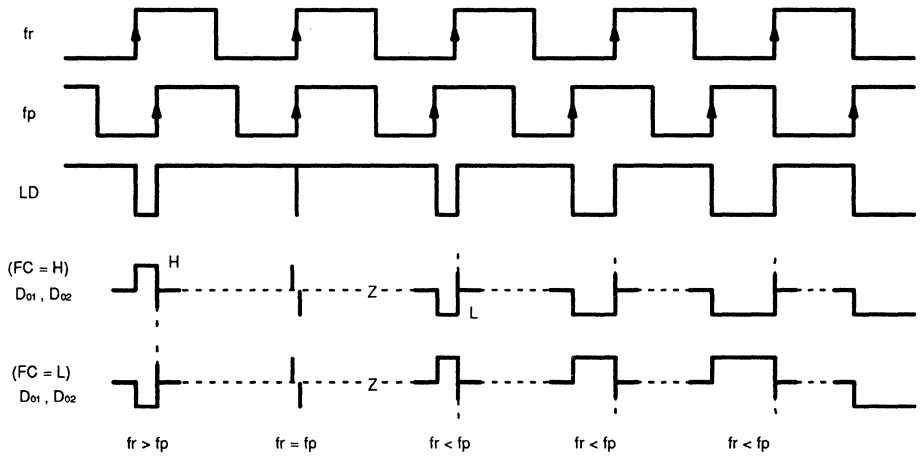
Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like 1,
FC should be set high or open.
When VCO polarity is like 2,
FC should be set low.

VCO POLARITY



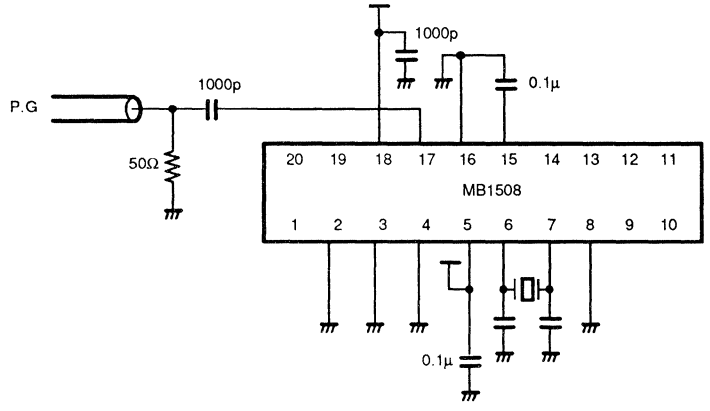
PHASE DETECTOR WAVEFORM



Note: Phase difference detection range : -2π to $+2\pi$

Spike shape depends on the charge pump characteristics.
The spike is output to diminish the dead band.

TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	−40	–	+85	°C

HANDLING PRECAUTIONS

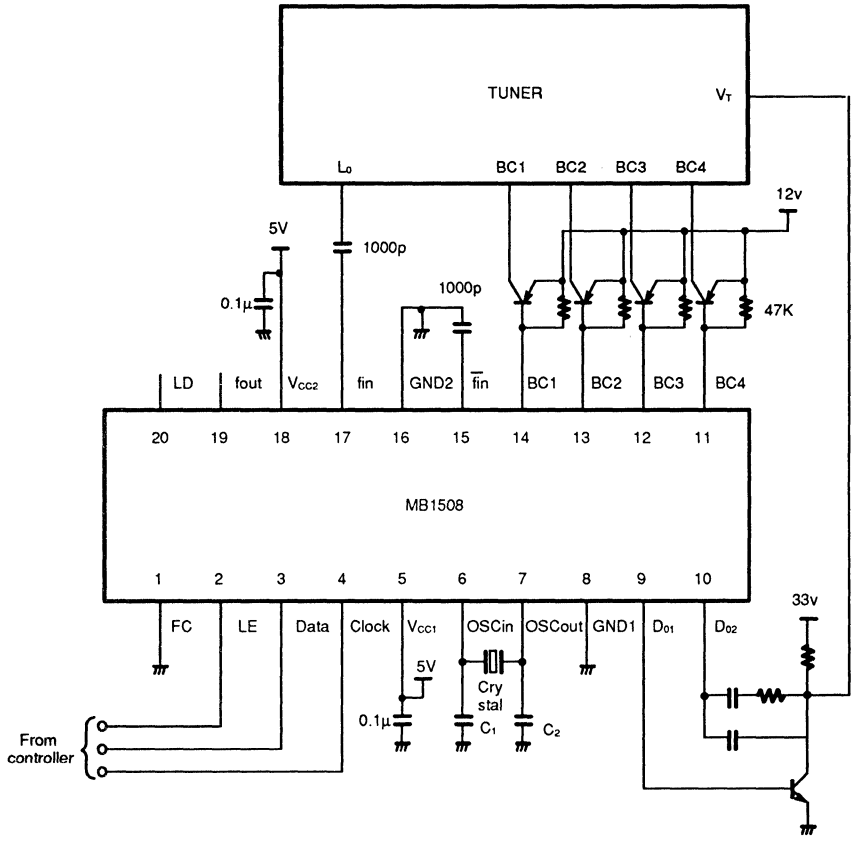
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note1	–	16.0	–	mA
Operating Frequency	f_{in}	f_{in}	Note2	10	–	2500	MHz
	OSC_{IN}	f_{OSC}	–	–	4	10	
Input Sensitivity	f_{in}	Vfin	2300 to 2500MHz	–4	–	6	dBm
			1900 to 2300MHz	–7	–	6	
			10 to 1900MHz	–10	–	6	
	OSC_{IN}	V_{OSC}	–	0.5	–	–	V_{PP}
High–level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock, LE	I_{IH}	–	–	1.0	–	µA
Low-level Input Current		I_{IL}	–	–	–1.0	–	
	FC	I_{ILFC}	–	–	–60	–	
Input Current	OSC_{IN}	I_{IOSC}	–	–	±50	–	
High–level Output Voltage	Except D_O	V_{OH}	V_{CC} = 5.0V	4.4	–	–	V
Low-level Output Voltage		V_{OL}	–	–	–	0.4	
High–impedance Cutoff Current	D_{O1},D_{O2} BC1 to BC4	I_{OFF}	–	–	–	1.1	µA
High-level Output Current	Except D_O	I_{OH}	–	–1.0	–	–	mA
Low-level Output Current		I_{OL}	–	1.0	–	–	
Withstand Output Voltage	BC1 to BC4	V_B	–	–	–	12	V

Note1: f_{in}=2.5GHz, OSC_{IN}=4.0MHz, V_{cc}=5.0V. Input pins are grounded and output pins are open.
Note2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

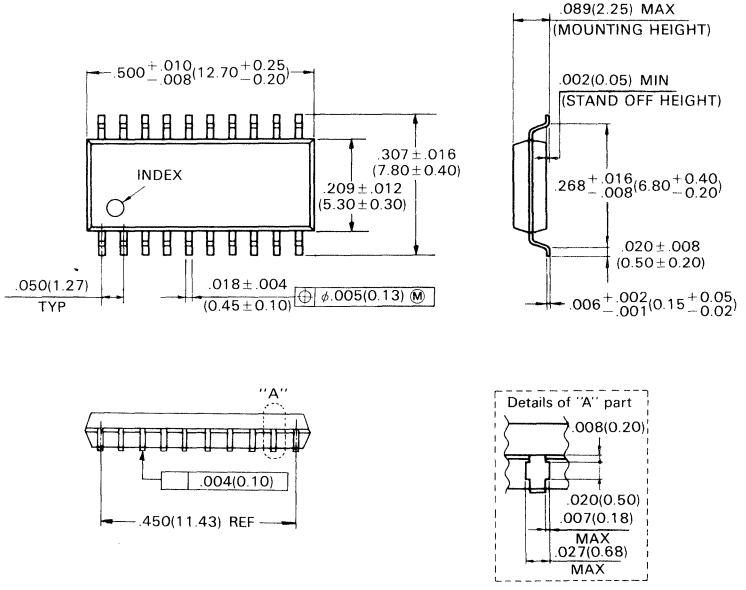
MB1508 APPLICATION CIRCUIT



C_1, C_2 : depends on the crystal oscillator.
FC : with internal pull up resistor.

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



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Dimensions in
inches (millimeters)

April 1991
Edition 2.0

FUJITSU

DATA SHEET

MB1509

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 400MHz PRESCALER

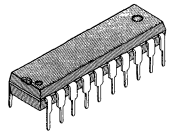
The Fujitsu MB1509 is a 400 MHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cordless telephone application.

The MB1509 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

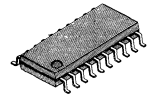
The MB1509 incorporates two 400 MHz dual modulus prescalers to enable implemention of a pulse swallow function.

It operates supply voltage of 3.0V typ. and dissipates 8mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 400MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 8mA typ, @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin dual in line package (Suffix: -P)
  Plastic 20-pin flat package (Suffix: -PF)

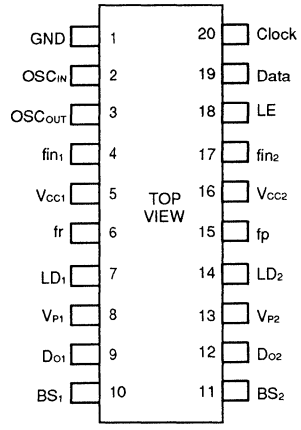


PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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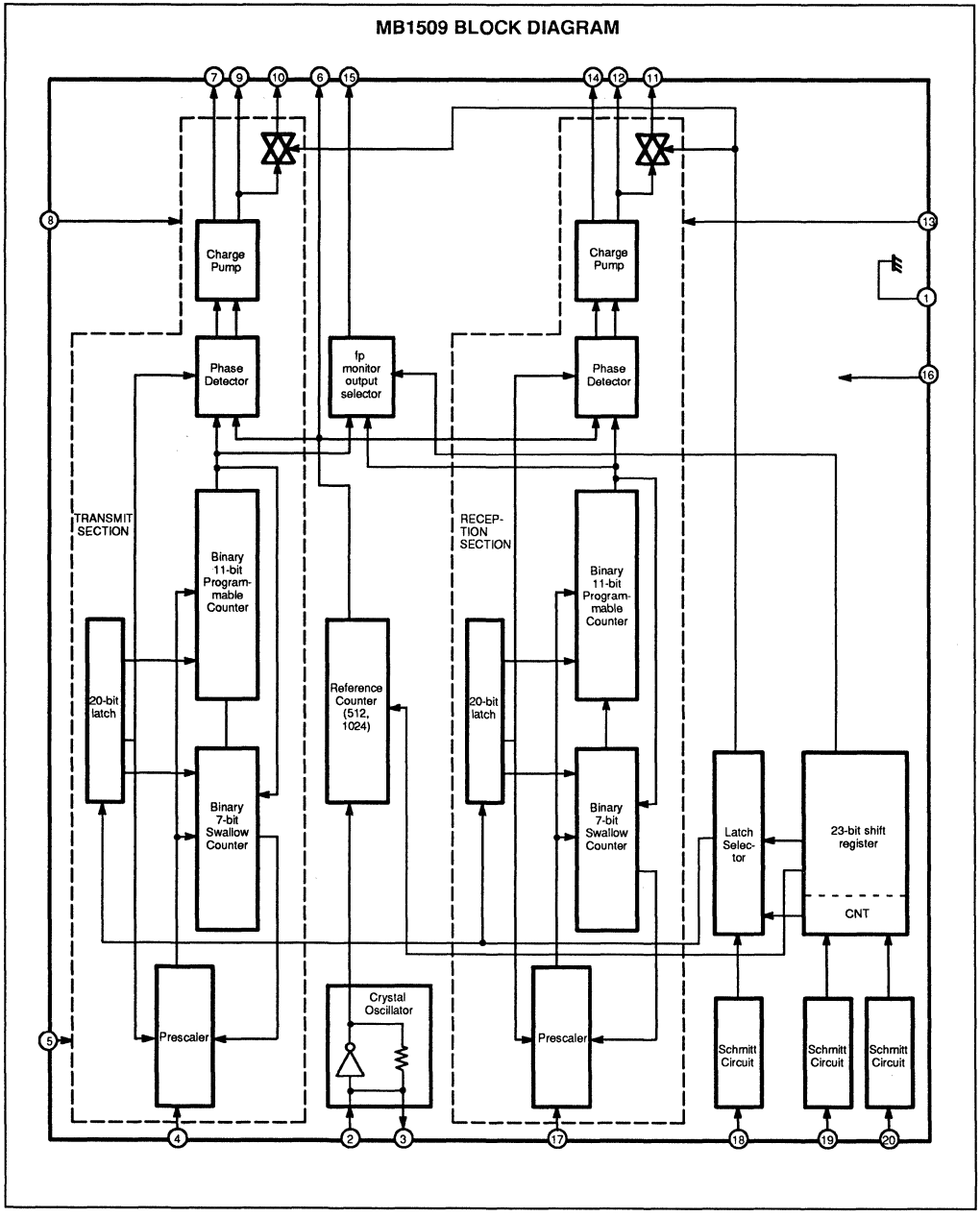
3

MB1509 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 400MHz dual modulus prescaler (Divide ratio: 32/33, 64/65)
- Charge pump

COMMON BLOCK

- 23-bit shift register
- Programmable divider consisting of:
  Reference counter (Divide ratio: 512, 1024)
  (Divide frequency = 25kHz, 12.5kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fin_1</td><td>I</td><td>Prescaler input pin of transmit section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>–</td><td>Power supply voltage input pin of transmit section.
When power is OFF, latched data of transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output.</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section.
<table><tr><td>Condition</td><td>LD pin output level</td></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of transmit section.</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of reception section.</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section.
<table><tr><td>Condition</td><td>LD pin output level</td></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output.
This pin outputs divided frequency of transmit section or reception section depending upon FP bit setting.
<table><tr><td>FP bit</td><td>Output</td></tr><tr><td>H</td><td>Transmit section (fp1)</td></tr><tr><td>L</td><td>Reception section (fp2)</td></tr></table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of reception section and reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section. The connection with VCO should be AC connection.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog swith becomes ON.
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmit section or reception section depending upon a control data. Control bit data: H → Latch of transmit section; L → Latch of reception section
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. Each rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

M: Preset divide ratio of dual modulus prescaler (32 or 64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins: Data pin, Clock pin, and LE pin. Programmable divider of transmit section and programmable divider of reception section are controlled individually.
Serial data of binary data is input into Data pin.
Each rising edge of the clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of the transmit section or the latch of the reception section, depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of transmit section
L	Latch of reception section

SHIFT REGISTER CONFIGURATION

Control bit

LSB

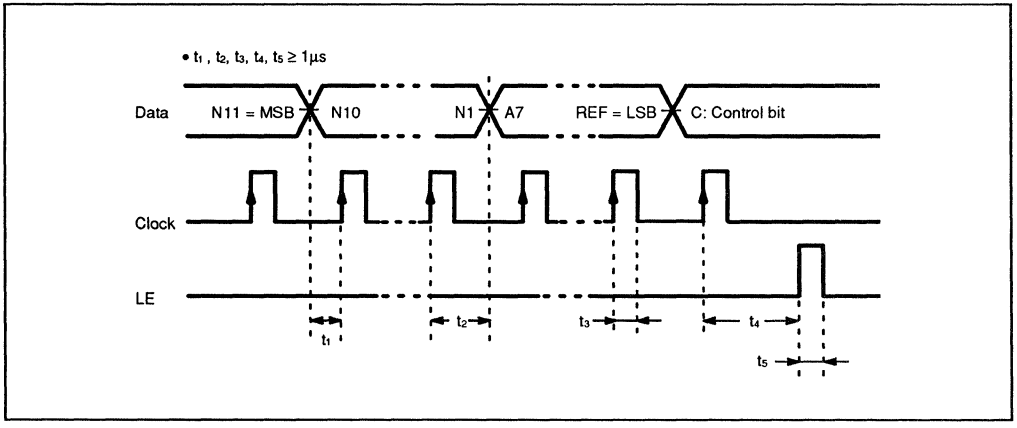
Data Flow →

MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CNT	REF	FP	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
PRE : Divide ratio of the prescaler setting bit (32/33 or 64/65)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CNT : Control bit

SERIAL DATA INPUT TIMING



Each rising edge of the clock shifts one bit of data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
·	·	·	·	·	·	·	·	·	·	·	·
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
·	·	·	·	·	·	·	·
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

PRE : DIVIDE RATIO (P) OF THE PRESCALER SETTING BIT
H = 32/33
L = 64/65

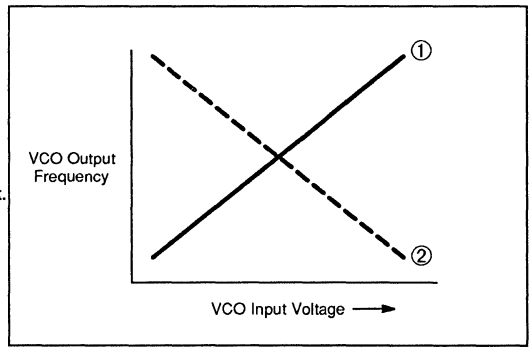
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 512 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section.

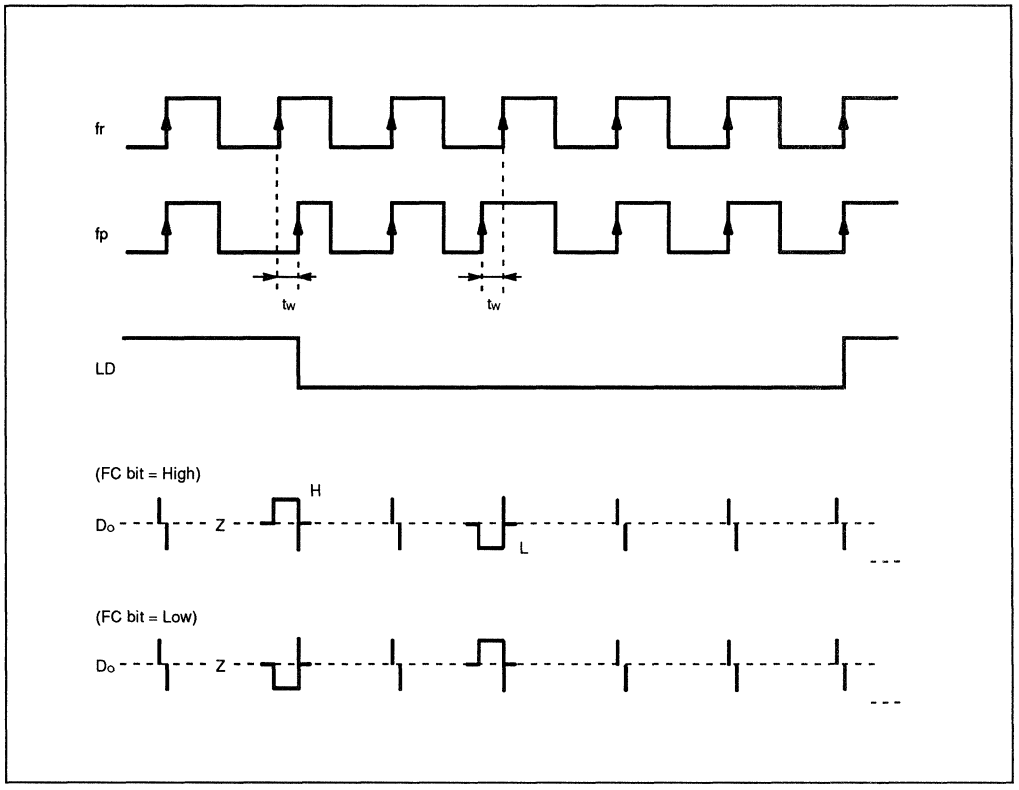
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO polarity, FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



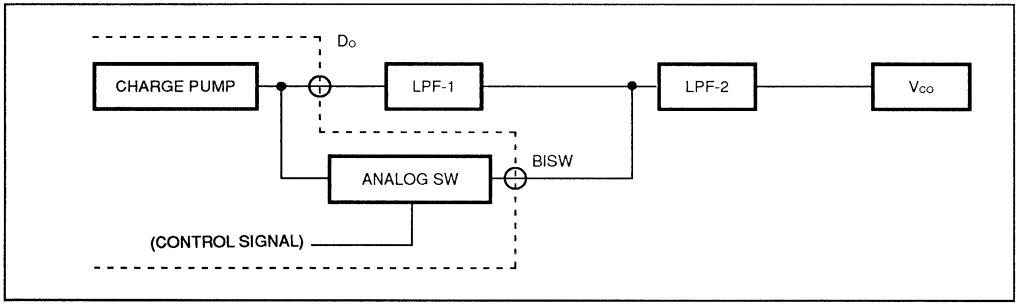
Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is t_w or more.
  LD output becomes high when phase difference less than t_w is reperated 3 times or more.
  (e. g. t_w = 625 to 1250 ns, foscin = 12.8 MHz)
- Spike apperance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending upon the VCO characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pin output the charge pump output (D_{O1}, D_{O2}). When analog switch is OFF, BS pin is set to high impedance.

	Control data = H Divide ratio of transmit section is set		Control data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	–	8.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	−40	–	+85	°C	

HANDLING PRECAUTIONS

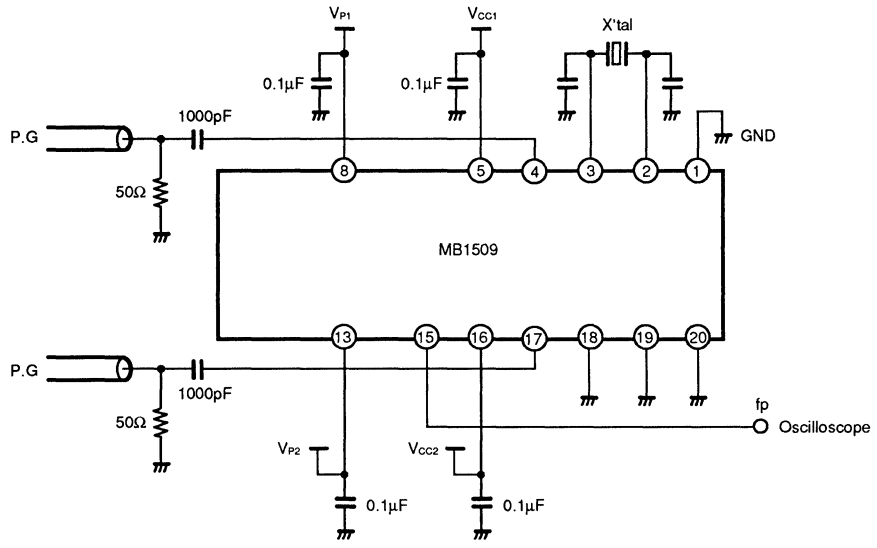
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

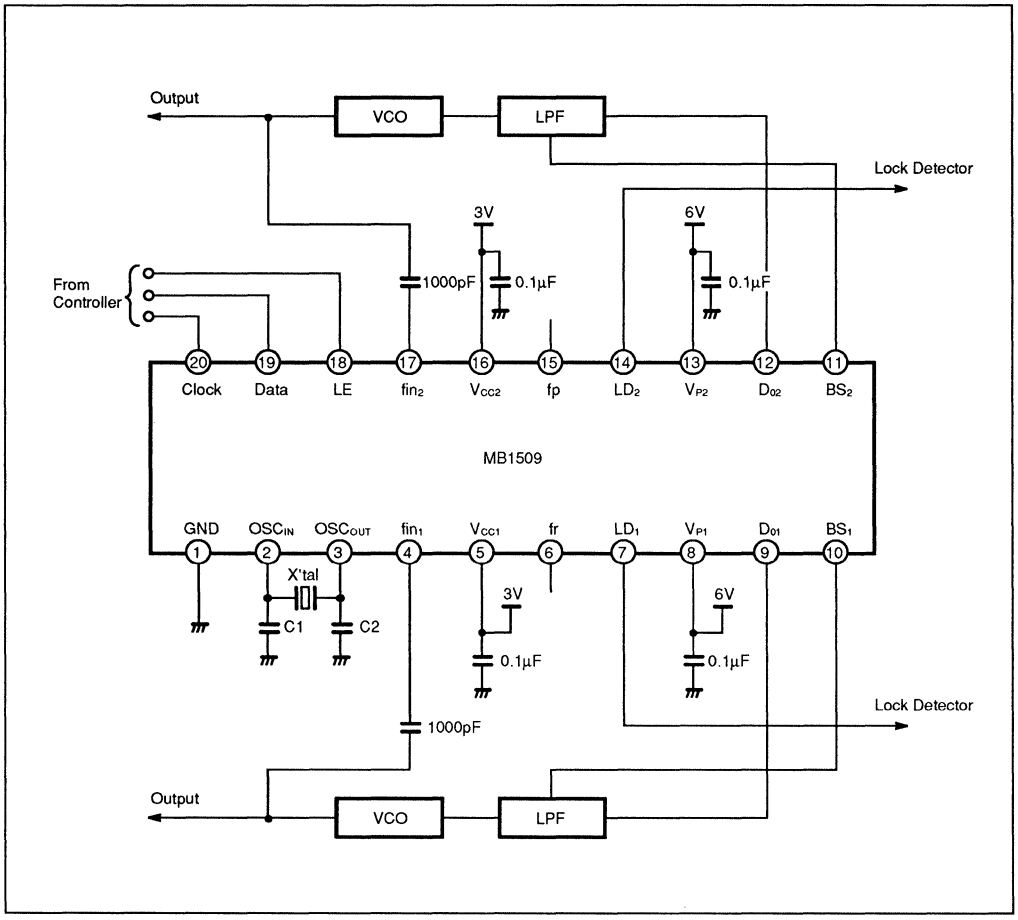
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current*		I_{CC1}	Reception section is active.	–	4.0	–	mA
		I_{CC2}	Transmit/reception section are active.	–	8.0	12.0	
Operating Frequency**	fin	fin1	P = 64/65	10	–	400	MHz
		fin2	P = 32/33	10	–	200	
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	Vfin	V_{CC} = 2.7 to 4.0V, 50Ω	–10	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	2	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	D_O	I_{OFF}	V_P = V_{CC} to 8.0V	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

Notes: *: fin = 400MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
**: AC coupling. Minimum operating frequency is measured with capacitor 1000pF.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



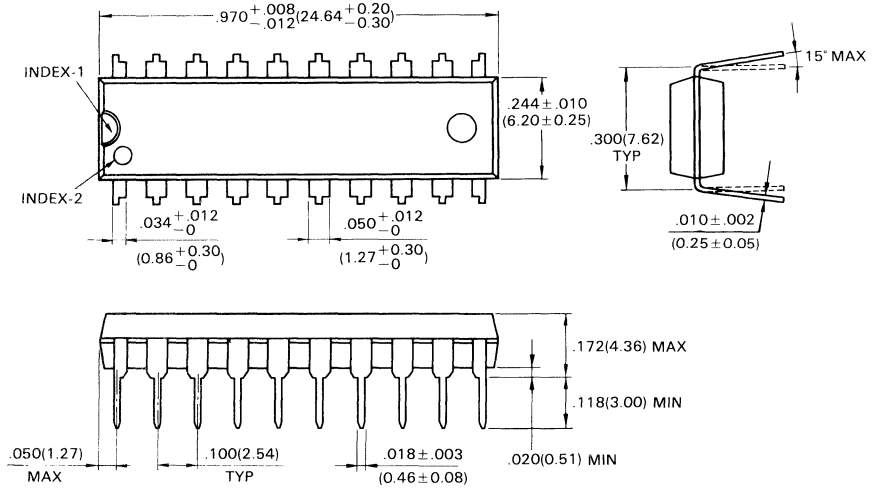
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8 V max.
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : involve the schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



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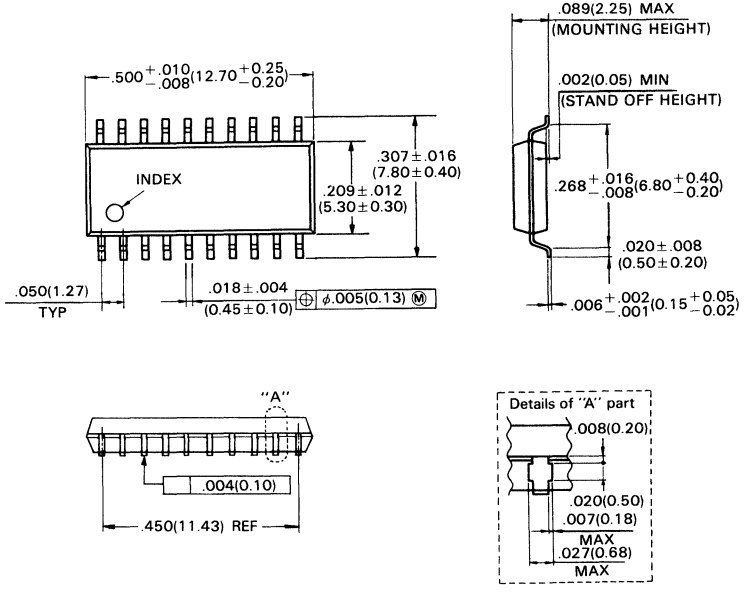
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



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Dimensions in
inches (millimeters)

April 1991
Edition 3.0

FUJITSU

DATA SHEET

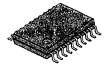
MB1511
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

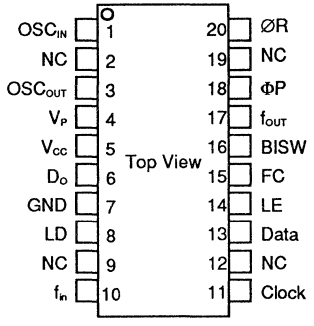
The Fujitsu MB1511 is a single chip serial input PLL frequency synthesizer designed for VHF tuner and cellular telephone applications.
It contains a 1.1 GH_Z dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.
It operates supply voltage of 3.0V typ. and dissipates 7mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.
The MB1511 is housed in SSOP package, this enables high integration.

- Low power supply voltage: V_{CC}=2.7 to 5.5V
- High operating frequency: $f_{IN\ MAX}$=1.1GH_Z ($V_{IN\ MIN}$=–10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC}=7mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package (Suffix: – PFV)



PLASTIC PACKAGE
FPT-20P-M03

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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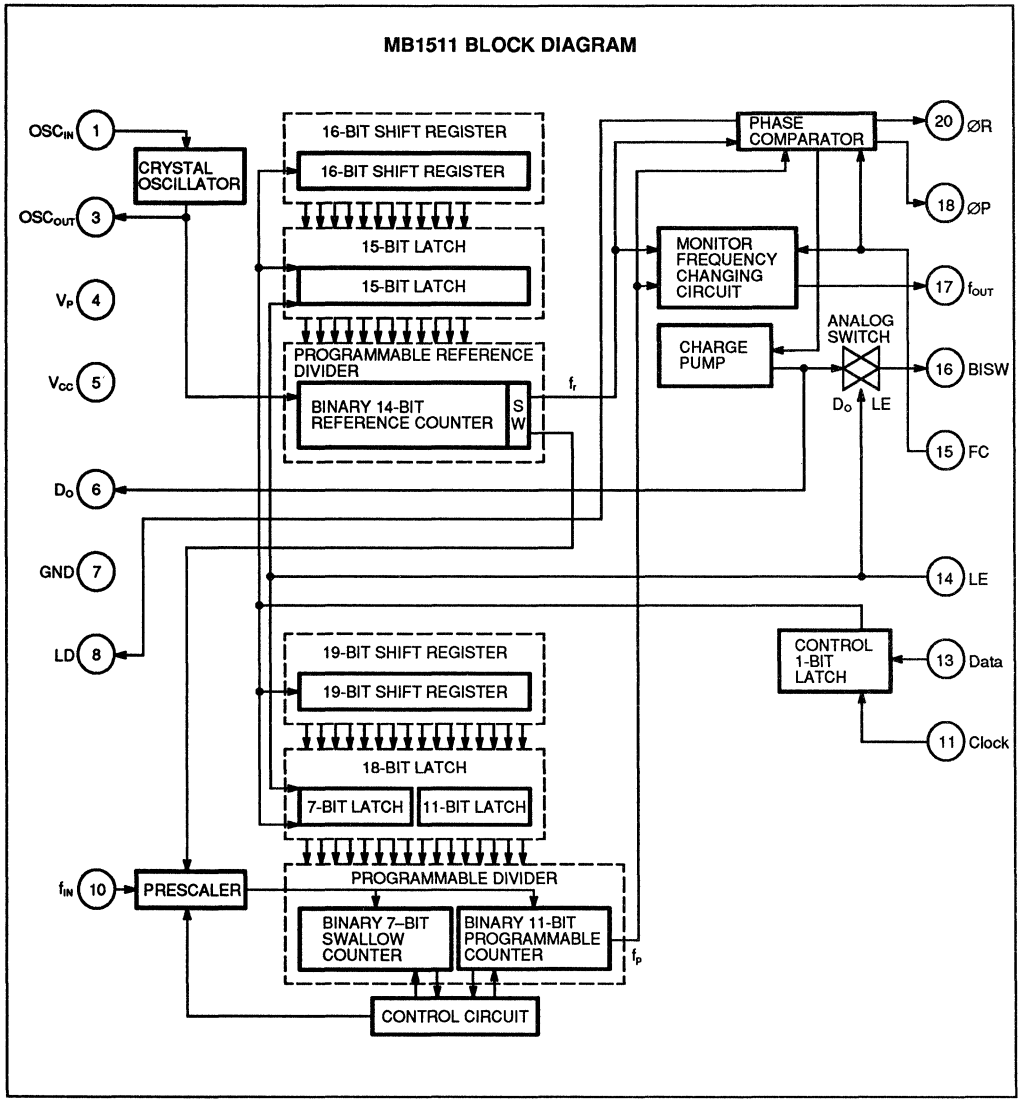
3

MB1511 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
4	V_P	–	Power supply input for charge pump and analog switch.
5	V_{CC}	–	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	–	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output is connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal controls f_{out} pin (test pin) output level, f_r or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
18 20	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
2,9 12,19	NC	–	No connection.

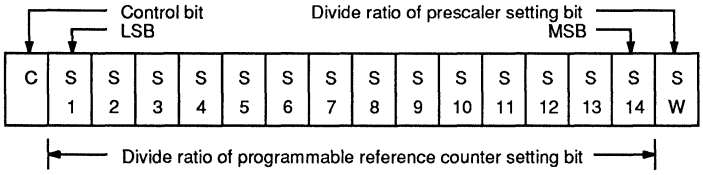
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



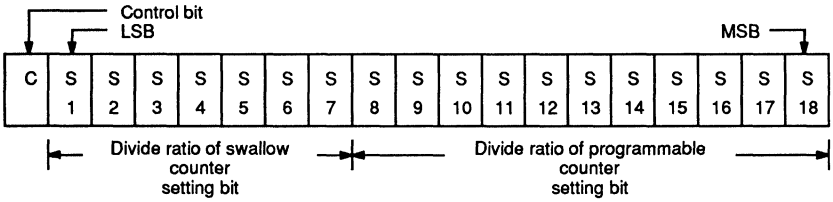
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

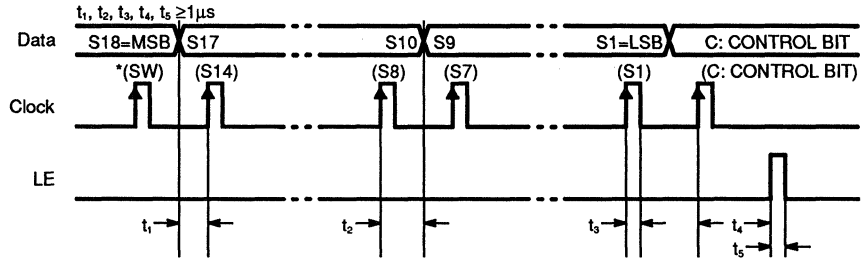
PULSE SWALLOW FUNCTION

The divide ratio is set using the following equation.

$f_{VCO} = [MxN)+A] \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
M: Preset modulus of external dual modulus prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$, $A < N$)
f_{OSC}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

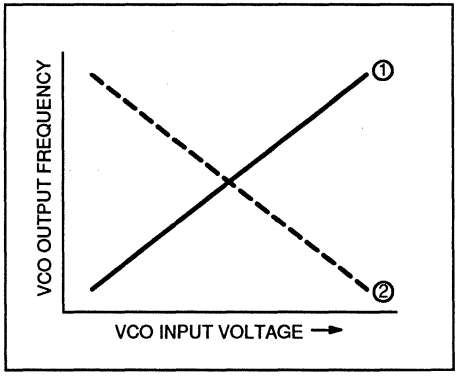
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (øR, øP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, øR, øP) and FC input level are shown below.

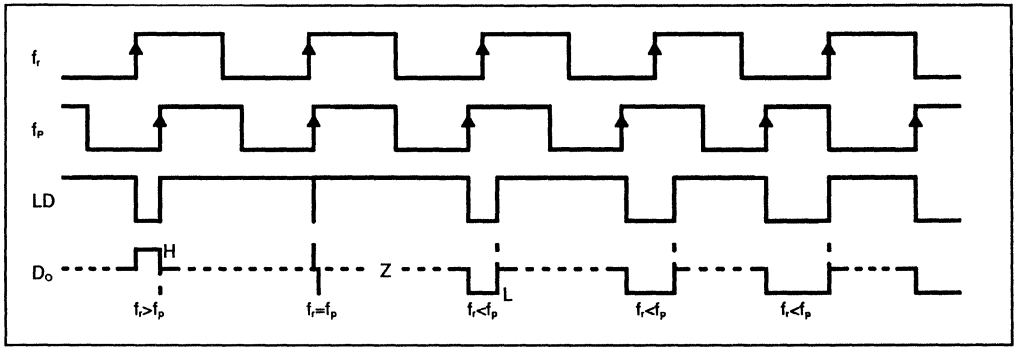
	FC=H or open				FC=L			
	D_O	øR	øP	f_{out}	D_O	øR	øP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.



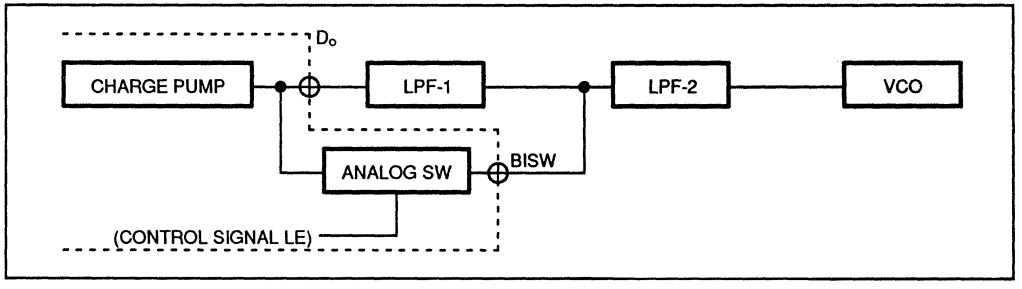
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_P$ or $f_r<f_P$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) is connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE	Analog Switch
H (Changing the divide ratio of intermal prescaler)	ON
L (Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up times is achieved to reduce LPF time constant during PLL channal switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_I	GND	—	V_{CC}	V
Operating Temperature	T_A	–40	—	85	°C

HANDLING PRECAUTIONS

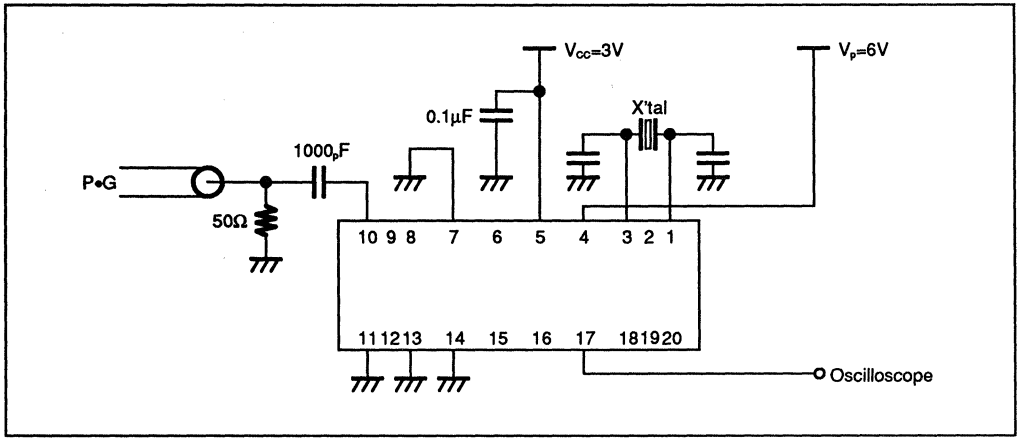
- This device should be transported and stored in anti-static containers.
- This is static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off befer inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handing or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

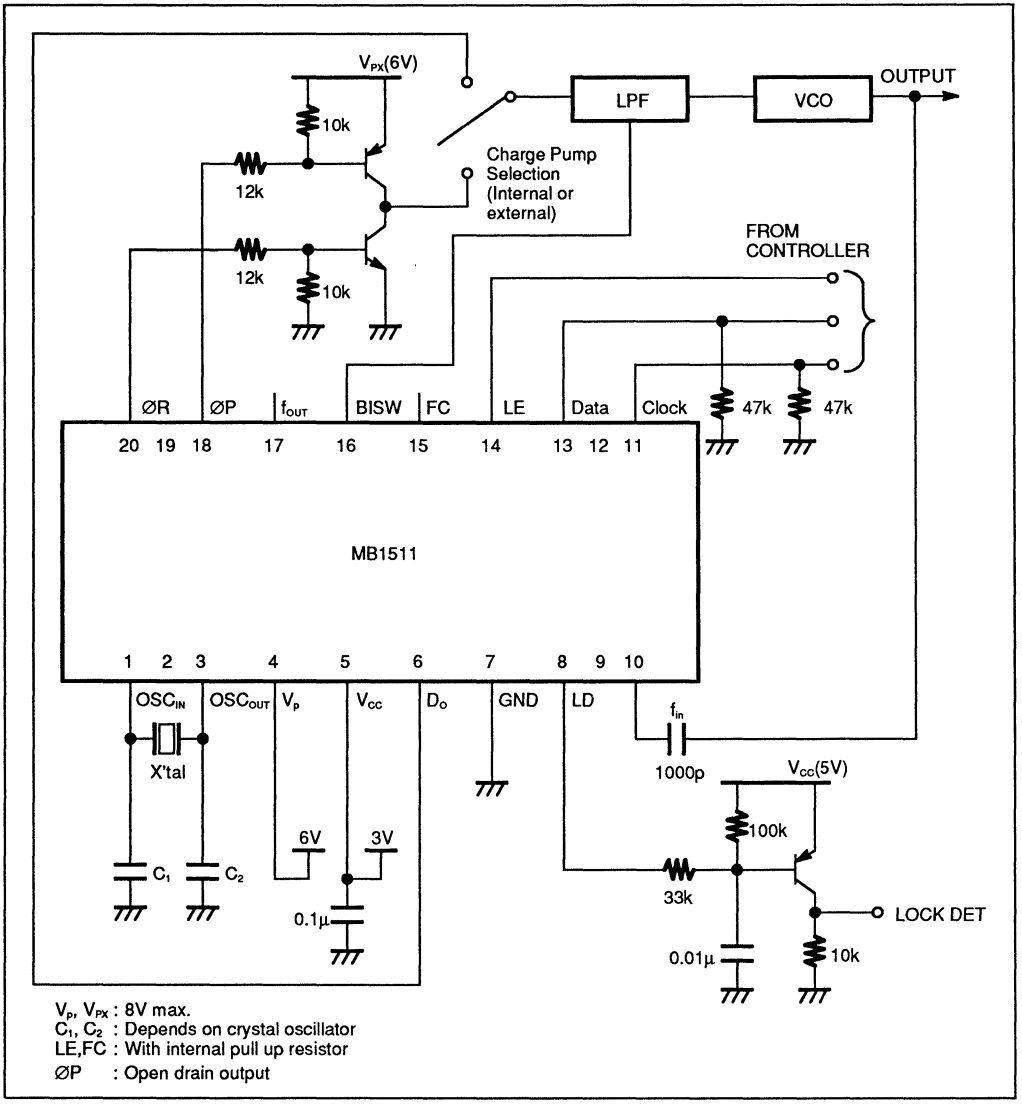
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		7.0		mA
Operating Frequency	f_{in}	f_{in}	Note 2	10		1100	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in1}	Vf_{in1}	V_{CC}=4.0 to 5.5V	–4		6	dBm
	f_{in2}	Vf_{in2}	V_{CC}=2.7 to 4.0V	–10		6	
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except fi_n and OSC_{IN}	V_{IH}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			–1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			–60		µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=3V	2.2			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$			1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistance		R_{ON}			50		Ω

NOTE 1: f_{in}=1.1GHz, OSC_{IN}=12MHz, V_{CC}=3V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF.

TEST CIRCUIT



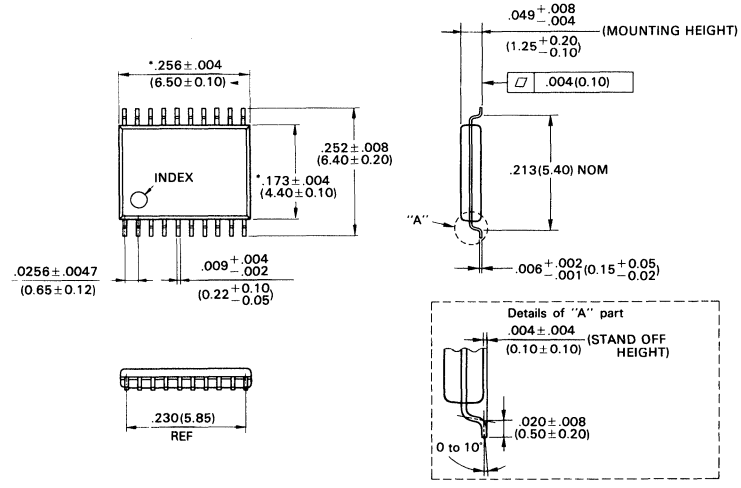
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



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* : This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

July 1990
Edition 1.0

FUJITSU

DATA SHEET

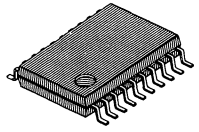
MB1512
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1GHz PRESCALER

PRELIMINARY

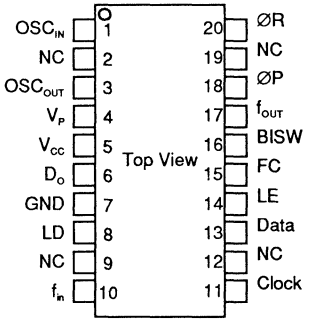
The Fujitsu MB1512, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB1512 contains a 1.1 GH_z two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.
It operates supply voltage of 5V typ. and achieves very low supply current of 8mA typ. realized through the use of Fujitsu Advanced Process Technology.



PLASTIC PACKAGE
FPT-20P-M03

- High operating frequency: $f_{IN\ MAX}$=1.1GH_z ($V_{IN\ MIN}$=–10dBm)
- Pulse swallow function: 64/65 or 128/129
- Power supply voltage: V_{CC}=4.5 to 5.5V
- Low supply current: I_{CC}=8mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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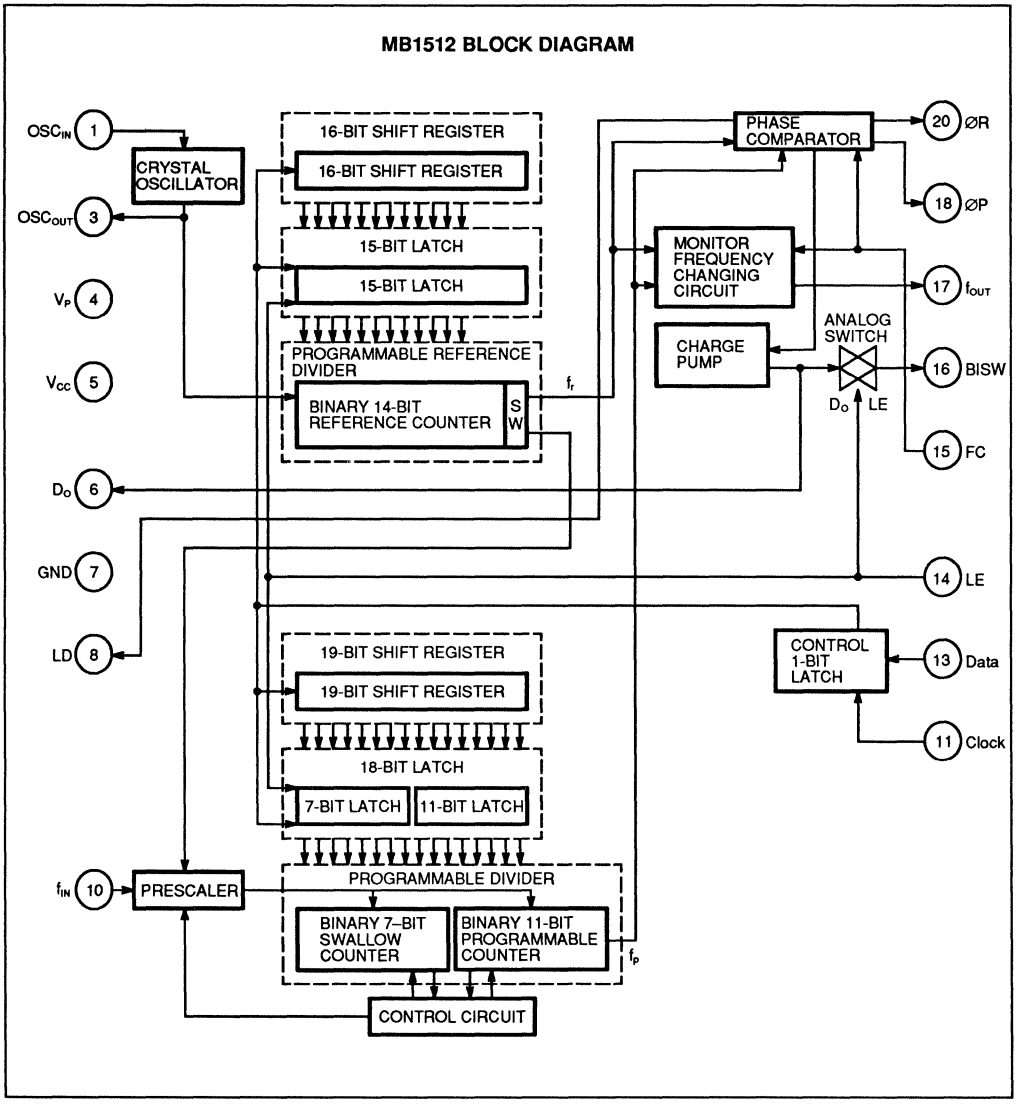
3

MB1512 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
4	V_P	–	Power supply input for charge pump and analog switch.
5	V_{CC}	–	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	–	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f, and f_p exists, this pin outputs low level.
9	NC	–	No connection.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
12	NC	–	No connection.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{out} pin (test pin) output level, f, or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f, output level. FC=L: It is the same as f_p output level.
18 20	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
2 19	NC	–	No connection.

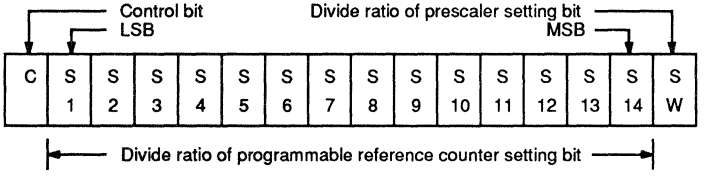
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



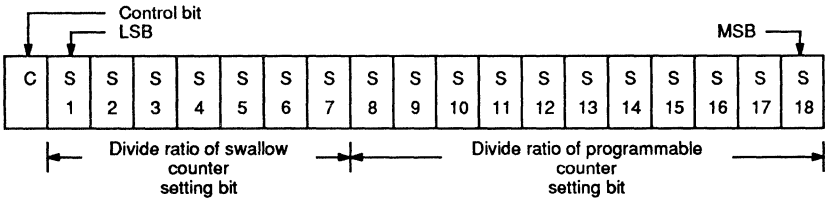
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

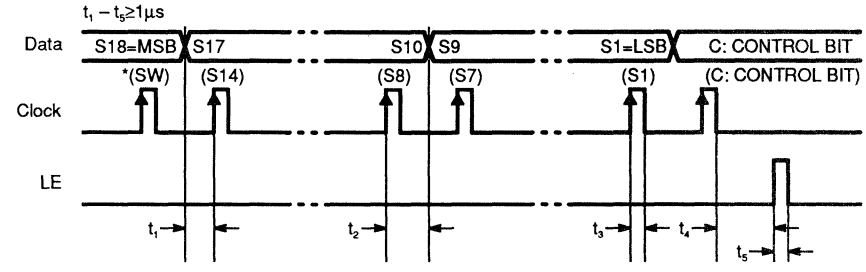
NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{vco} = [(PxN)+A] \times f_{osc} \div R$

f_{vco}: Output frequency of external voltage controlled oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{osc}: Output frequency of the external reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)
P: Preset modulus of external dual modulus prescaler (64 or 128)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

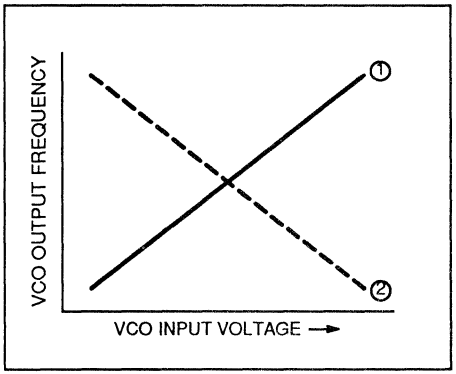
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ϕR, ϕP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ϕR, ϕP) and FC input level are shown below.

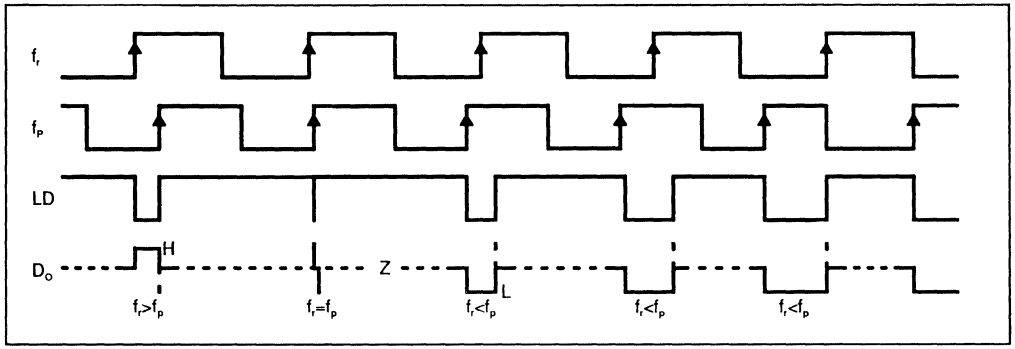
	FC=H or open				FC=L			
	D_O	ϕR	ϕP	f_{out}	D_O	ϕR	ϕP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set High or open circuit;
When VCO characteristics are like ②, FC should be set Low.



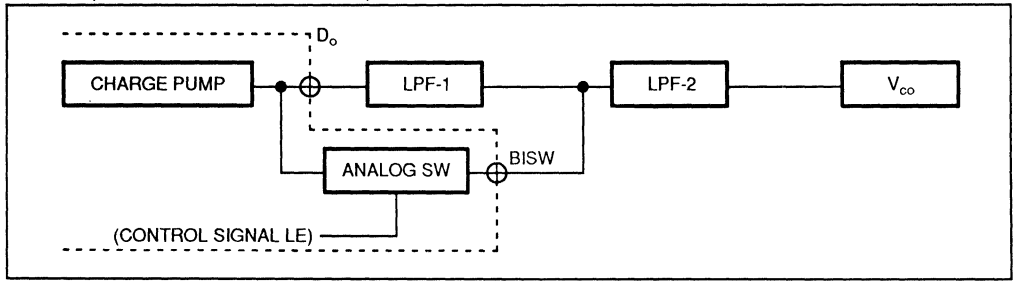
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode) : Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

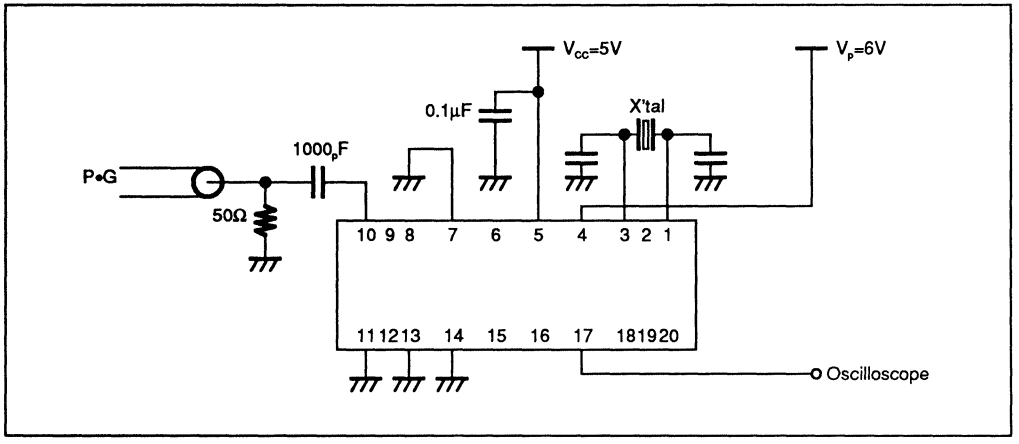
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	V_P	8.0	V
Input Voltage	V_I	GND		V_{CC}	V
Operating Temperature	T_A	–40		85	°C

ELECTRICAL CHARACTERISTICS

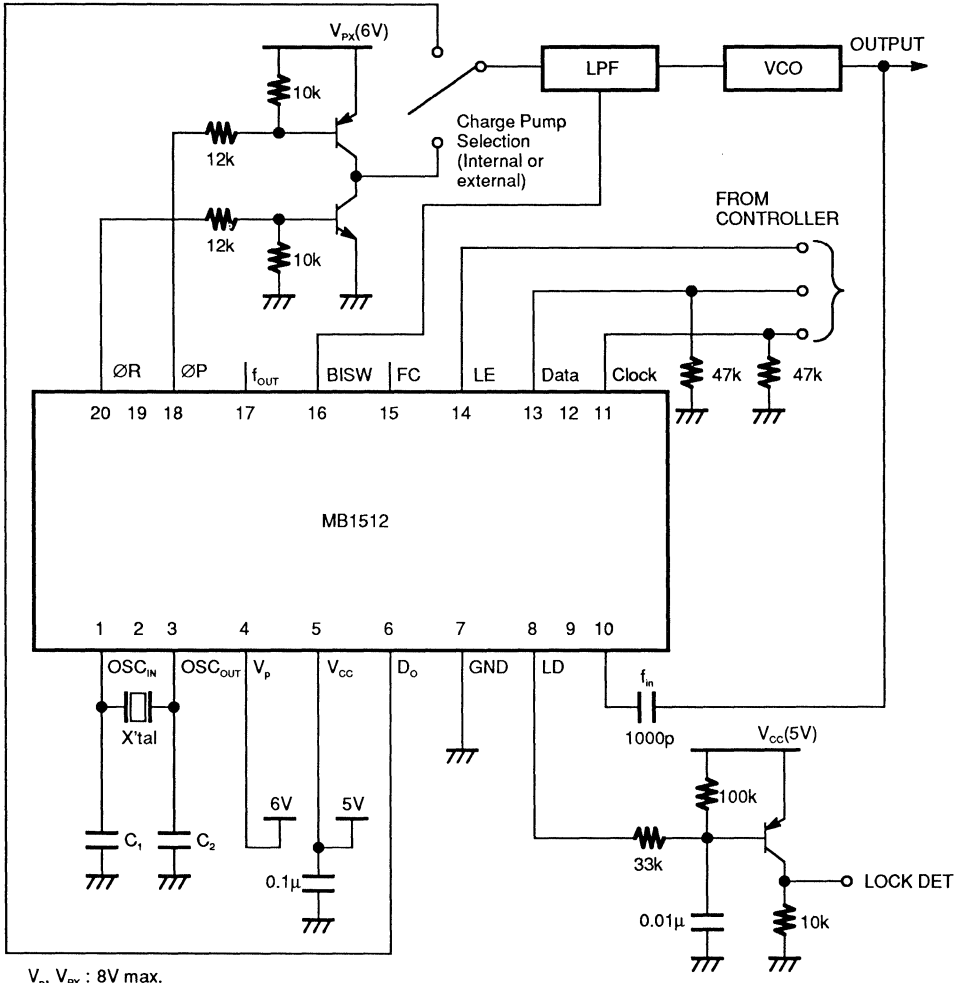
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1		8.0		mA
Operating Frequency	f_{in}	f_{in}	Note 2	10		1100	MHz
	OSC_{IN}	f_{OSC}			12	20	MHz
Input Sensitivity	f_{in}	Vf_{in}		−10		6	dBm
	OSC_{IN}	V_{OSC}		0.5			V_{PP}
High-level Input Voltage	Except fi_n and OSC_{IN}	V_{IH}		V_{CC}x0.7			V
Low-level Input Voltage		V_{IL}				V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}			1.0		µA
Low-level Input Current		I_{IL}			−1.0		µA
Input Current	OSC_{IN}	I_{OSC}			±50		µA
	LE, FC	I_{LE}			−60		µA
High-level Output Current	Except D_o and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4			V
Low-level Output Current		V_{OL}				0.4	V
N-channel Open Drain Cutoff Current	D_o, ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$			1.1	µA
Output Current	Except D_o and OSC_{OUT}	I_{OH}		−1.0			mA
		I_{OL}		1.0			mA
Analog Switch On Resistor		R_{ON}			25		Ω

NOTE 1: f_{in}=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT



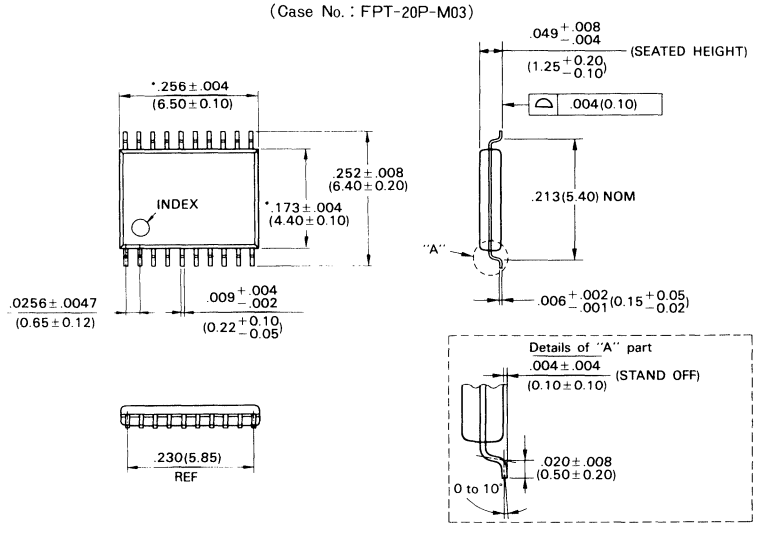
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

PACKAGE DIMENSIONS

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



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* : This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

3

FUJITSU

DATA SHEET

MB1513

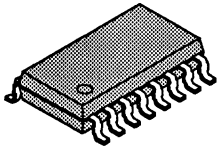
Serial Input PLL Frequency Synthesizer

The Fujitsu MB1513 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.

The MB1513 is configured with a 1.1 GHz dual-modulus prescaler with a 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and intermittent operation control circuit that selects the operating or stand-by mode depending on the power-save control input state (PS).

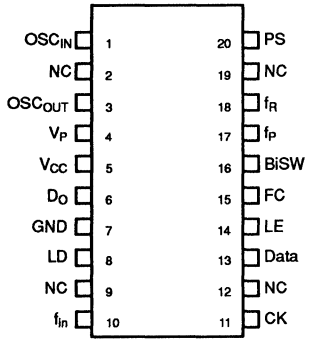
The MB1513 operates from a single +5 V supply. Fujitsu's advanced technology achieves an I_{CC} of 8 mA, typical. The stand-by mode current consumption is just 100 µA.

- High operating frequency: f_{IN} = 1.1 GHz (V_{IN} = −10 dBm)
- Pulse-swallow function: high-speed dual-modulus prescaler with 128/129 divide ratio
- Low supply current: I_{CC} = 8 mA typ. at 5 V
- Power-saving stand-by mode: 100 µA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 16 to 2,047
- Serial input, 15-bit programmable reference divider consisting of binary 14-bit programmable reference counter: 8 to 16,383 1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lock-up
- On-chip charge pump minimizes system component count
- Wide operating temperature range: −40 to +85 °C
- Plastic 20-pin shrink small outline package (Suffix: PFV)



FPT-20P-M03

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
	V_P	$V_{CC} \leq V_P \leq 10.0$	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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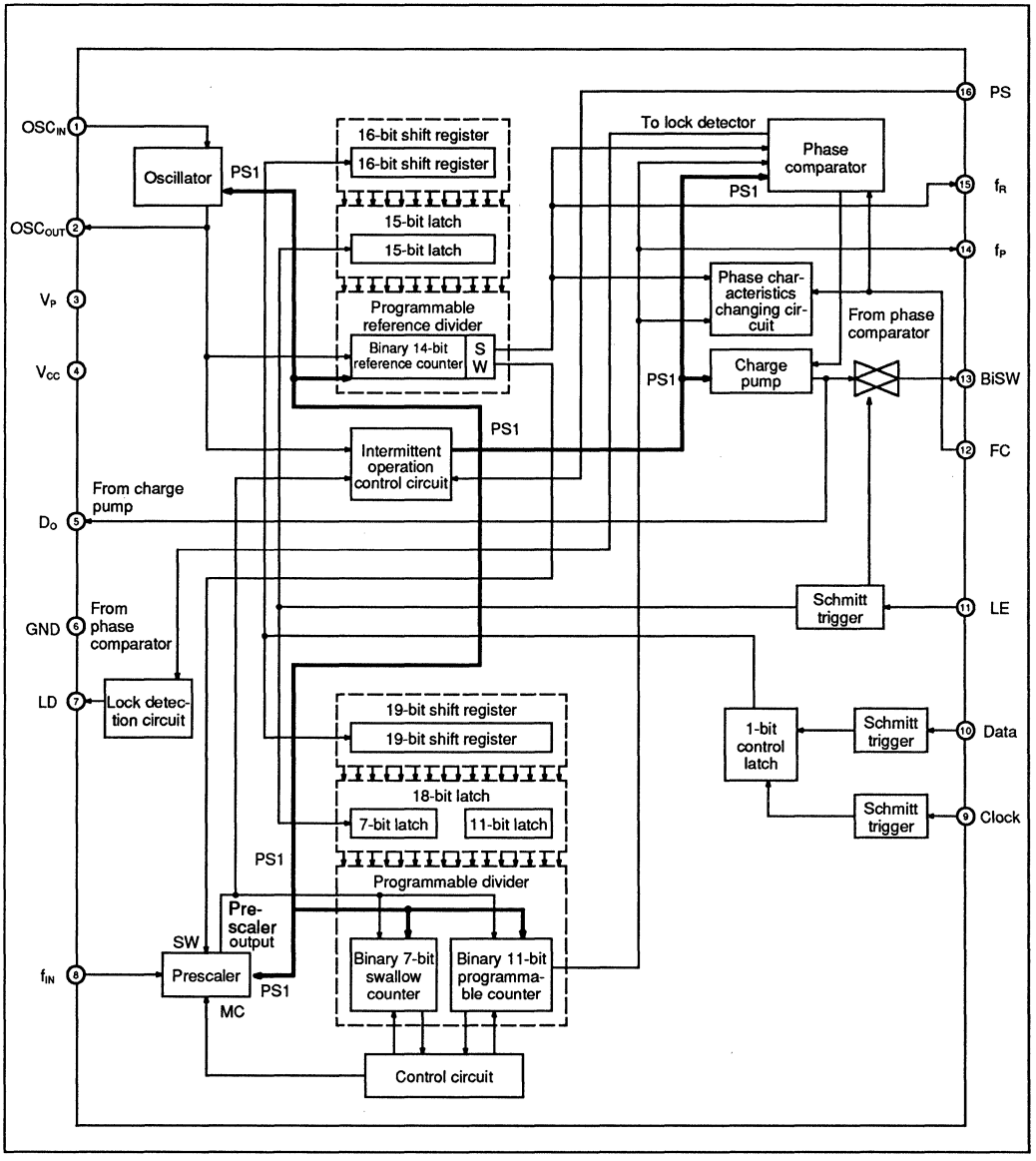
BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin
2	NC	–	No connection
3	OSC_{OUT}	O	Oscillator output An external crystal is connected to this pin
4	V_P	–	Power supply input for charge pump and analog switch
5	V_{CC}	–	Power supply
6	D_O	O	Charge pump output The phase of charge pump is reversed depending on FC input
7	GND	–	Ground
8	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked
9	NC	–	No connection
10	f_{IN}	I	Prescaler input An external VCO should be AC-coupled to this pin
11	Clock	I	Clock input for 19-bit and 16-bit shift registers One bit of data is shifted into the registers on the rising edge of the clock Schmitt trigger circuit is involved
12	NC	–	No connection
13	Data	I	Binary serial data input The last bit of the data is a control bit When the control bit is high, data is transmitted to the 15-bit latch When the control bit is low, data is transmitted to the 18-bit latch Schmitt trigger circuit is involved
14	LE	I	Load enable signal input When LE is high, the contents of the shift register are transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin Schmitt trigger circuit is involved
15	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of charge pump and phase comparator are reversed FC input signal is also used to control the f_{out} pin (test pin) of f_R or f_P
16	BiSW	O	Analog switch output Usually, BiSW is in the high-impedance state. When the switch is on (LE is high), the charge pump is connected to the BiSW pin
17	f_P	O	Programmable counter output monitor pin
18	f_R	O	Reference counter output monitor pin
19	NC	–	No connection
20	PS	I	Power save signal input Set low when the system is operating (Never use pin 20 as it is opened) PS = High : Operation mode PS = Low : Stand-by mode

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

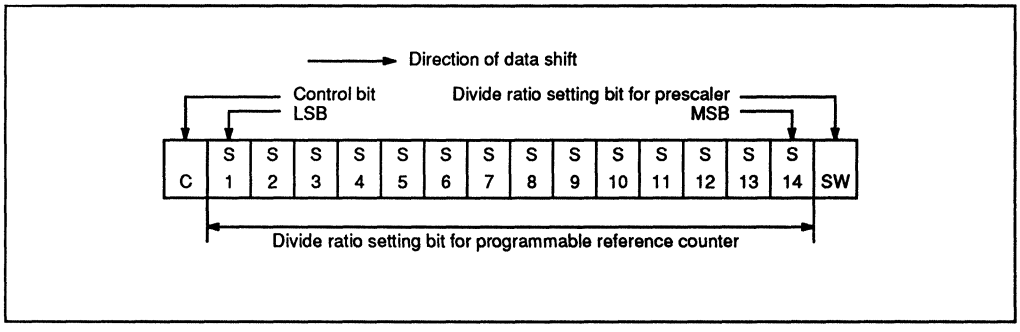
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of prescaler (128)

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched, depending on the control as follows:

Control data	Destination of serial data
H	15 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The 16-bit serial data format is shown below:



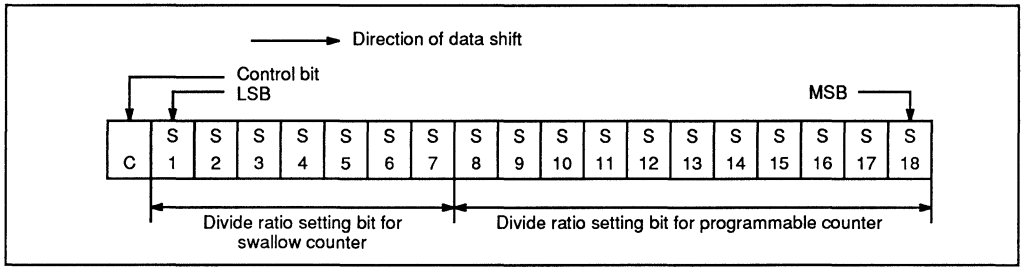
- 14-bit programmable reference counter divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited.
2. SW: This bit selects the divide ratio of the prescaler
SW Low: 128 or 129
(SW must be always be low.)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383).
4. C: Control bit: Set high.
5. Input data MSB first.

(b) Programmable divider divide ratio
The programmable divider consists of a 19-bit shift register, an 18-bit latch, a 7-bit swallow counter, and an 11-bit programmable counter. The 19-bit serial data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

- 11-bit programmable counter divide ratio

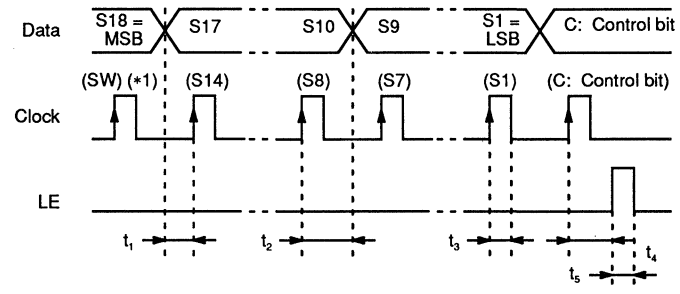
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 16 to 2,047)

Notes: 1. Divide ratios less than 16 are prohibited for 11–bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (16 to 2,047).
4. C: Control bit: (Set low)
5. Input data MSB first.

Serial data input timing

- t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
  t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or starting the internal circuits according to its necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost.
To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enters the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS = High)
  All circuits are operating, and PLL operation is normal.

- Stand-by mode (PS = Low)
  Circuits that do not affect operation are powered-down to save power.
  The current in the power save state is typically 100 µA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage-controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

Relationship between FC input and phase characteristics

The FC pin controls the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

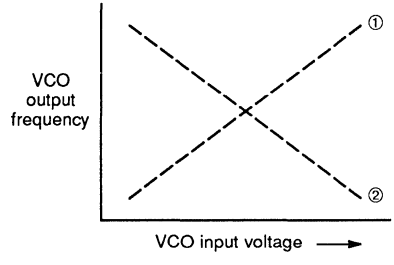
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (*1)	Z (*1)

*1: High impedance

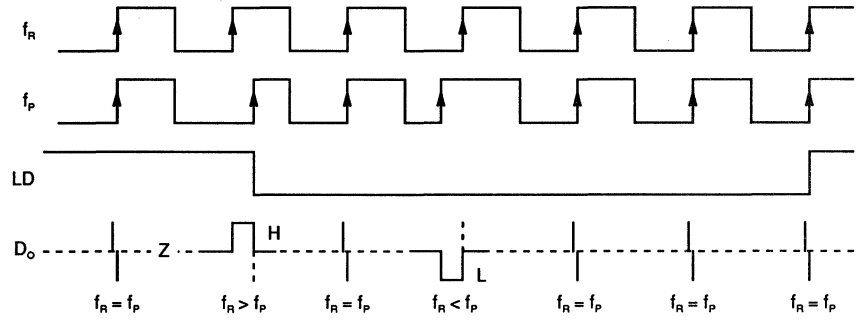
When designing a synthesizer, the FC pin setting depends on the VCO characteristics.

*: When the VCO characteristics are similar to ①, set FC high or open.

*: When the VCO characteristics are similar to ②, set FC low.



Phase comparator output waveform (FC = High)



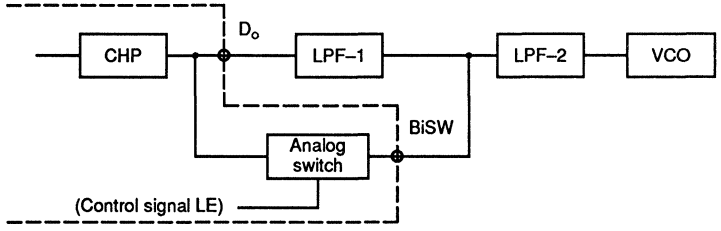
Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. The spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, spike might not appear, depending on the charge pump characteristics.
4. LD is low when the phase difference is two or more. LD is high when the phase difference is two or less for three or more continuous cycles (when f_{OSCIN} = 12.8 MHz, tw = 625 to 1,250 ns).

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (D_O) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$			V
Input voltage	V_I	GND	–	V_{CC}	V
Operating temperature	T_A	–40	–	+85	°C

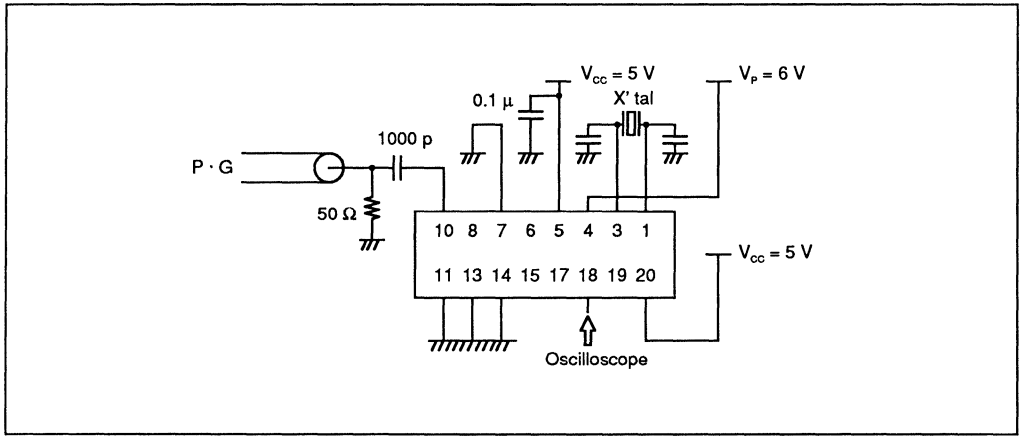
Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device from a socket.
- When handling PC boards on which devices are mounted, protect leads of the device using conductive sheet.

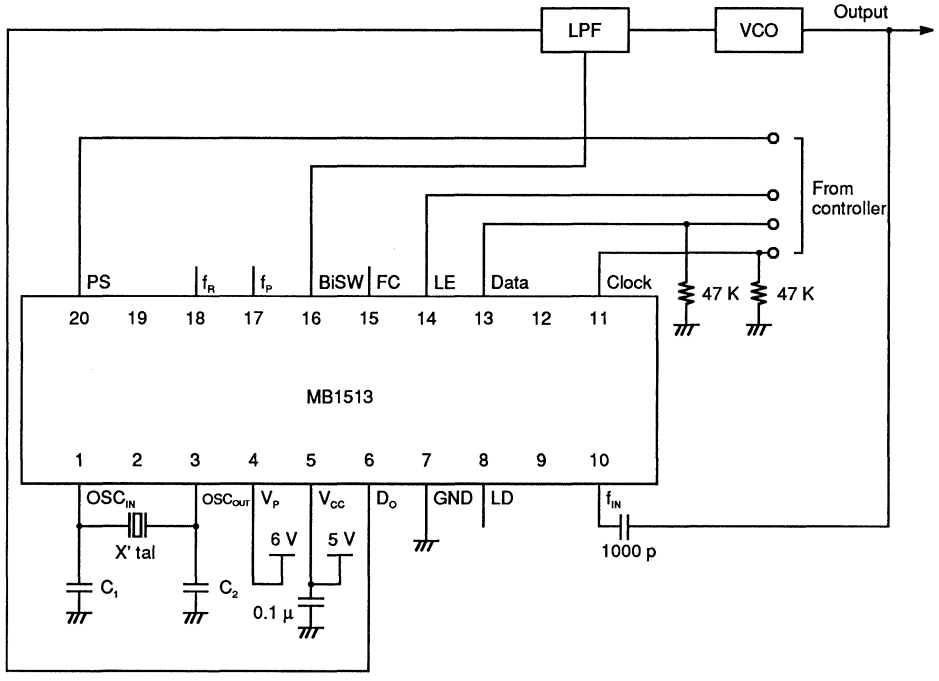
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply current		I_{CC}	–	8.0		mA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5.0 V. Inputs are at V_{CC} and outputs are open
Stand-by current		IPS	–	100	–	µA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5.0 V. The PS pin is grounded, remaining inputs are at V_{CC}, and outputs are open
Operating frequency	f_{IN}	f_{IN}	10	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 100-pF capacitor connected
	OSC_{IN}	f_{OSC}	–	12	20	MHz	
Input sensitivity	f_{IN}	V_{fIN}	–10	–	6	dBm	
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data Clock LE	I_{IH}	–	1.0	–	µA	
Low-level input current		I_{IL}	–	–1.0	–	µA	
	FC	I_{FC}	–	–60	–	µA	
Input current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	–	–	V	V_{CC} = 5 V
Low-level output voltage		V_{OL}	–	–	0.4	V	
High-impedance Cut off current	D_O	I_{OFF}	–	–	1.1	µA	V_{DO} = GND to 8 V $V_{CC} \leq V_P \leq 8$ V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	
		I_{OL}	1.0	–	–	mA	
Analog switch ON resistance		R_{ON}	–	25	–	Ω	

TEST CIRCUIT
(FOR MEASURING PRESCALER INPUT SENSITIVITY)

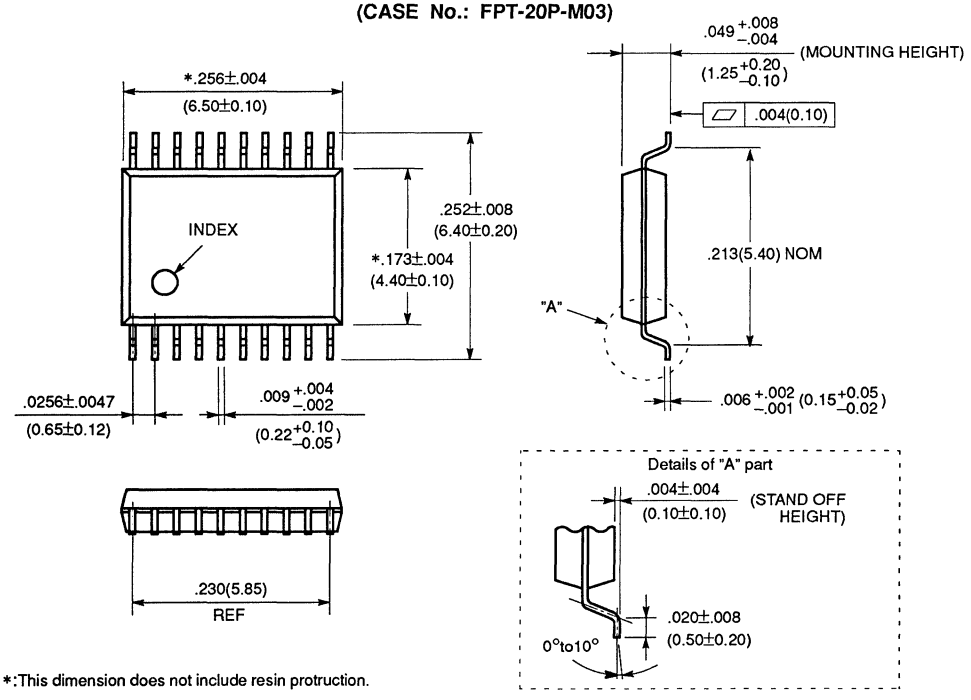


APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8 V
C_1, C_2 : Depend on the crystal parameters

PACKAGE DIMENSIONS



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May 1991
Edition 1.0

FUJITSU

DATA SHEET

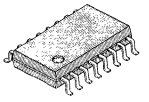
MB1518
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

SERIAL INPUT PLL FREQUENCY SYNTHESIZER ON CHIP 2.5GHz PRESCALER

The Fujitsu MB1518 on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system applications.

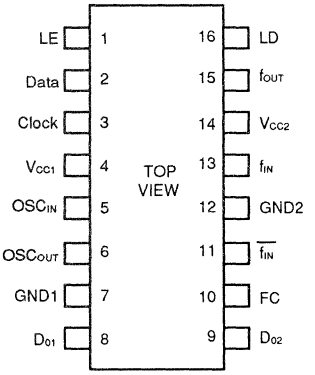
It operates supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- Power supply voltage: V_{CC} = 4.5 to 5.5V
- High operating frequency: f_{in} = 2.5GHz (V_{in} = −4dBm)
- 2.5GHz dual modulus prescaler: P = 512/528
- Low power supply current: I_{CC} = 16mA typ.
- Programmable reference divider : R = 512
- Programmable divider consisting of:
  Binary 5-bit swallow counter (A = 0 to 31)
  Binary 9-bit programmable counter (N = 32 to 511)
- Wide operating temperature: T_A = −40 to +85°C
- Plastic 16-pin flat package (Suffix: −PF)



PLASTIC PACKAGE
FPT-16P-M06

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0	V
Output Voltage	V_O	0.5 to V_{CC} +0.5	V
Output Current	I_O	±10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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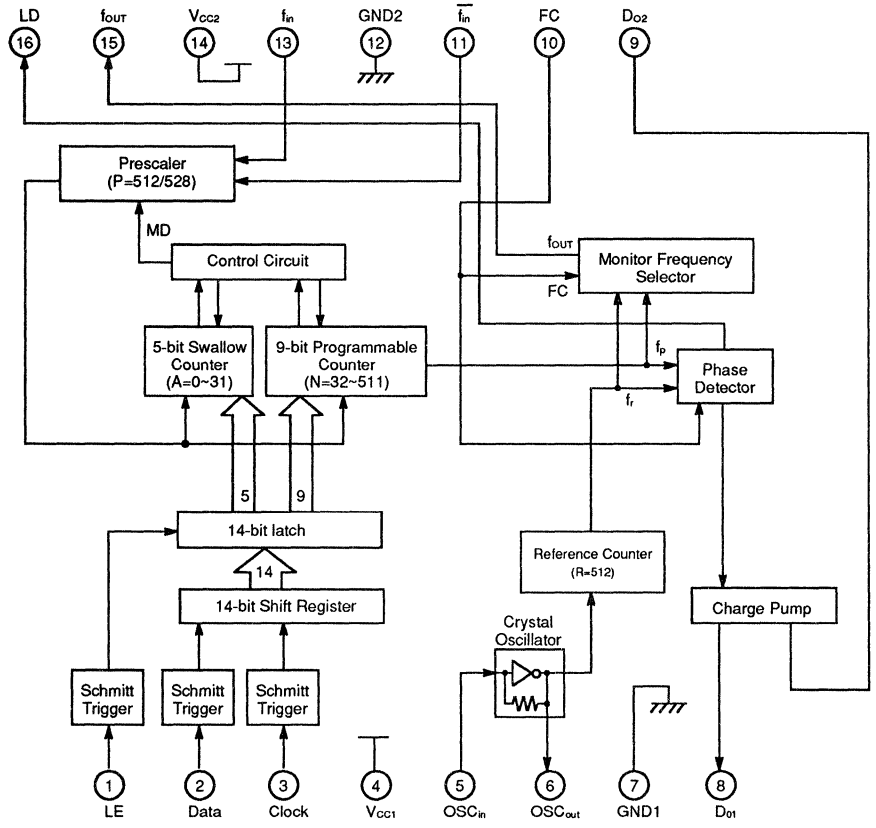
3

MB1518 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.
2	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.
3	Clock	I	Clock input pin of the 14–bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of the data into the shift register.
4	V_{CC1}	–	PLL power supply voltage input pin.
5 6	OSC_{IN} OSC_{OUT}	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.
7	GND1	–	PLL ground pin.
8 9	D_{O1} D_{O2}	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.
10	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f_{OUT} pin output level, either fr or fp. Please see on page 6.
11	$\overline{f_{in}}$	I	Complementary input pin of f_{in}. Please connect to GND through a capacitor.
12	GND2	–	Prescaler ground pin.
13	f_{in}	I	Prescaler input pin, This signal is input with AC coupled.
14	V_{CC2}	–	Prescaler power supply voltage input pin.
15	f_{OUT}	O	Monitor pin of the phase detector input. f_{OUT} pin outputs either of the programmable reference divider output frequency fr or programmable divider output frequency fp depending upon the FC pin input level. FC pin: H → fout output signal: fr; FC pin: L → fout output signal: fp
16	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.

FUNCTIONAL DESCRIPTIONS

DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

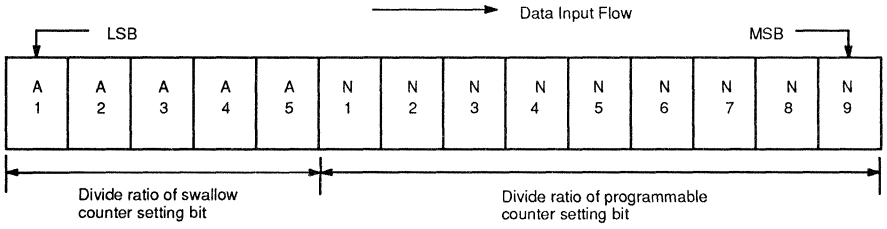
$f_{vco} = \{(P \times N) + (16 \times A)\} \times f_{osc} \div R$

f_{vco}: Output frequency of an external voltage controlled oscillator (VCO)
P: Preset divide ratio of an internal dual modulus prescaler (512)
N: Preset divide ratio of binary 9-bit programmable counter (32 to 511)
A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)
f_{osc}: Reference oscillator frequency
R: Preset divide ratio of reference counter (512)

SERIAL DATA I NPUT

On rising edge of the clock shifts one bit of the data into the shift register.
When the load enable is high, the data stored in the shift register is transferred to the latch.

14 bit of serial data formit is shown below.



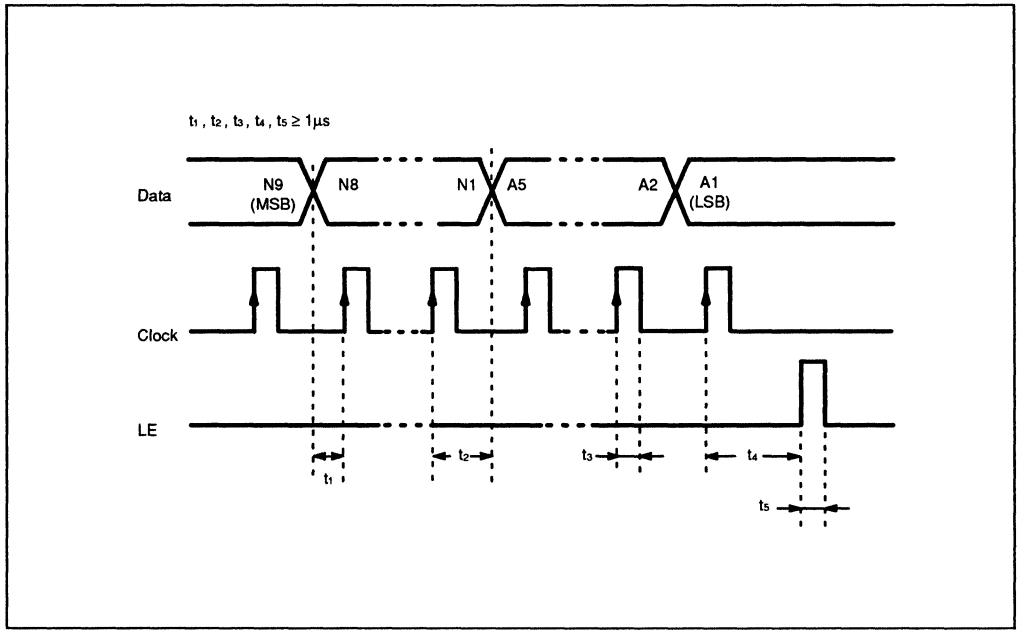
5-bit swallow counter divide ratio (A1 to A5)

Divide ratio A	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

9-bit programmable counter divide ratio (N1 to N9)

Divide ratio	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
32	0	0	0	1	0	0	0	0	0
33	0	0	0	1	0	0	0	0	1
34	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:
511	1	1	1	1	1	1	1	1	1

SERIAL DATA INPUT TIMING



Note: On rising edge of the clock shifts one bit of the data into the shift register.
When LE is high, the data stored the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC pin input level. Monitor pin (fout) output level is selected by the FC pin input level as well.

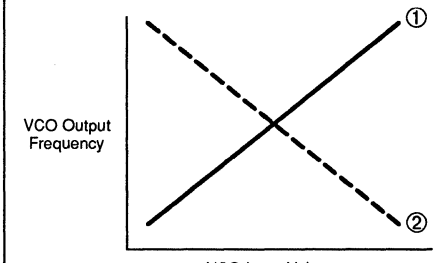
	FC = H (or open)		FC = L	
	D_{01}, D_{02}	fout	D_{01}, D_{02}	fout
fr > fp	H	Outputs programmable reference divider output frequency fr.	L	Outputs programmable divider output frequency fp.
fr = fp	Z		Z	
fr < fp	L		H	

Note:
Z: High-impedance

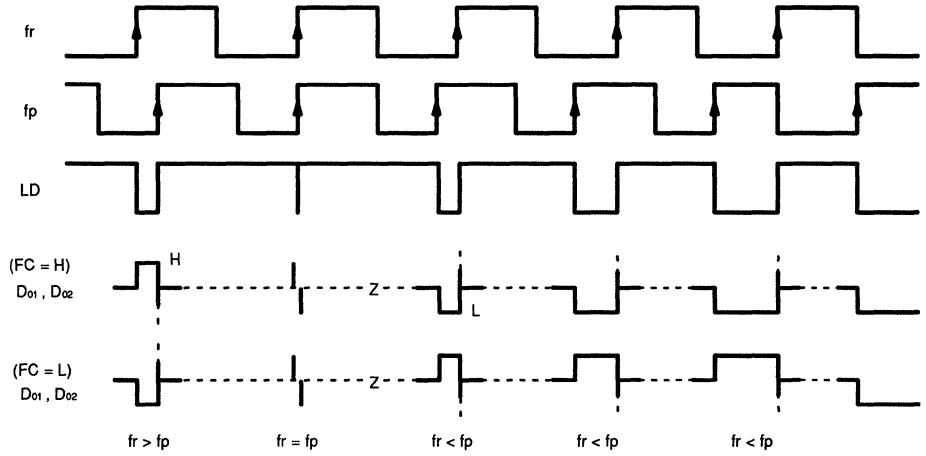
Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like 1,
FC should be set high or open.
When VCO polarity is like 2,
FC should be set low.

VCO POLARITY



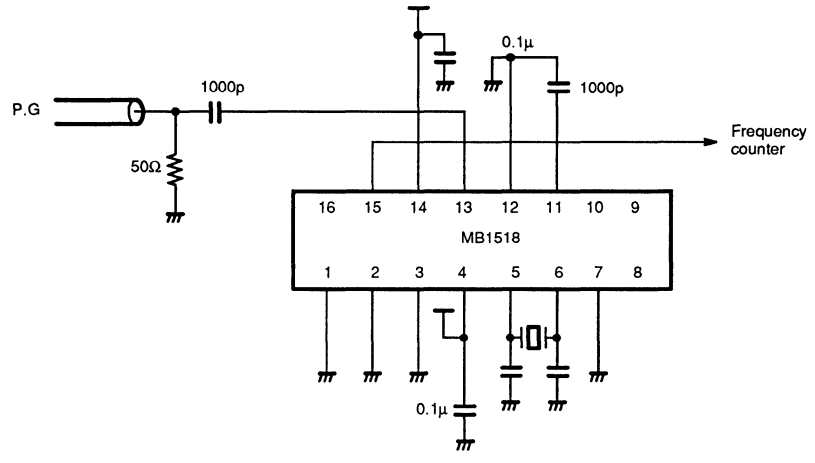
PHASE DETECTOR WAVEFORM



Note: Phase difference detection range : -2π to $+2\pi$

Spike shape depends on the charge pump characteristics.
The spike is output to diminish the dead band.

TEST CIRCUIT (FOR PRESCALER INPUT SENSITIVITY)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

HANDLING PRECAUTIONS

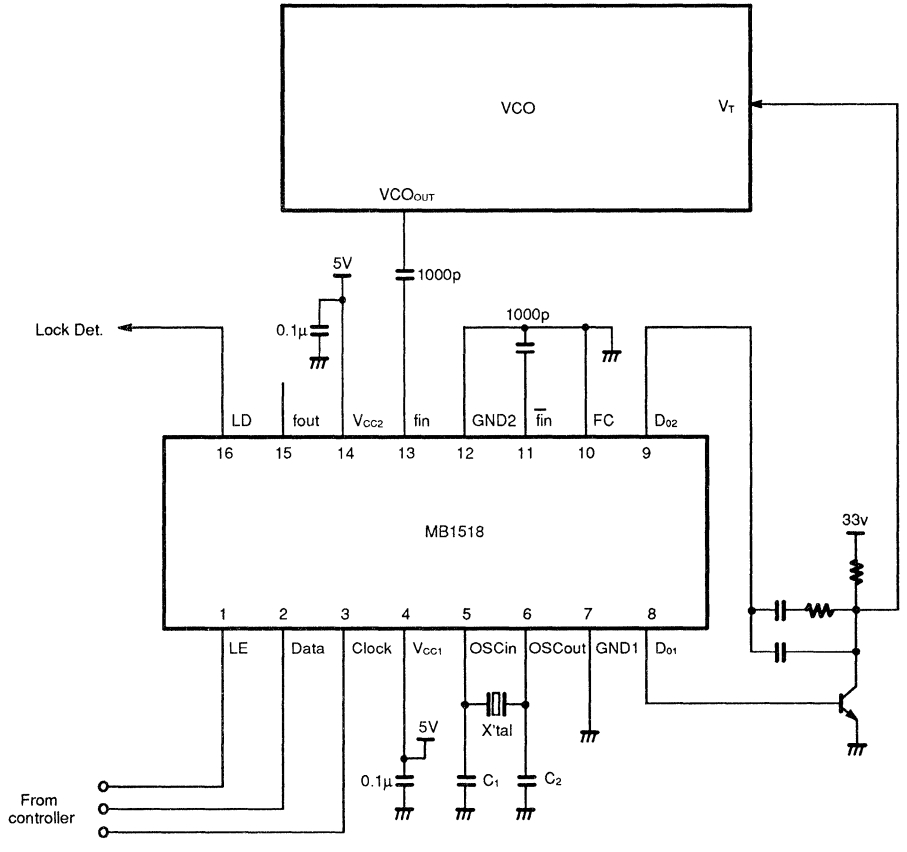
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note1	–	16.0	–	mA
Operating Frequency	f_{in}	f_{in}	Note2	10	–	2500	MHz
	OSC_{IN}	f_{OSC}	–	–	4	10	
Input Sensitivity	f_{in}	Vfin	2300 to 2500MHz	–4	–	6	dBm
			1900 to 2300MHz	–7	–	6	
			10 to 1900MHz	–10	–	6	
	OSC_{IN}	V_{OSC}	–	0.5	–	–	V_{PP}
High–level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}	–	V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}	–	–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock, LE	I_{IH}	–	–	1.0	–	µA
Low-level Input Current		I_{IL}	–	–	–1.0	–	
	FC	I_{ILFC}	–	–	–60	–	
Input Current	OSC_{IN}	I_{IOSC}	–	–	±50	–	
High–level Output Voltage	Except D_O	V_{OH}	V_{CC} = 5.0V	4.4	–	–	V
Low-level Output Voltage		V_{OL}	–	–	–	0.4	
High–impedance Cutoff Current	D_{01},D_{02}	I_{OFF}	–	–	–	1.1	µA
High-level Output Current	Except D_O	I_{OH}	–	–1.0	–	–	mA
Low-level Output Current		I_{OL}	–	1.0	–	–	

Note1: f_{in}=2.5GHz, OSC_{IN}=4.0MHz, V_{cc}=5.0V. Input pins are grounded and output pins are open.
Note2: AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

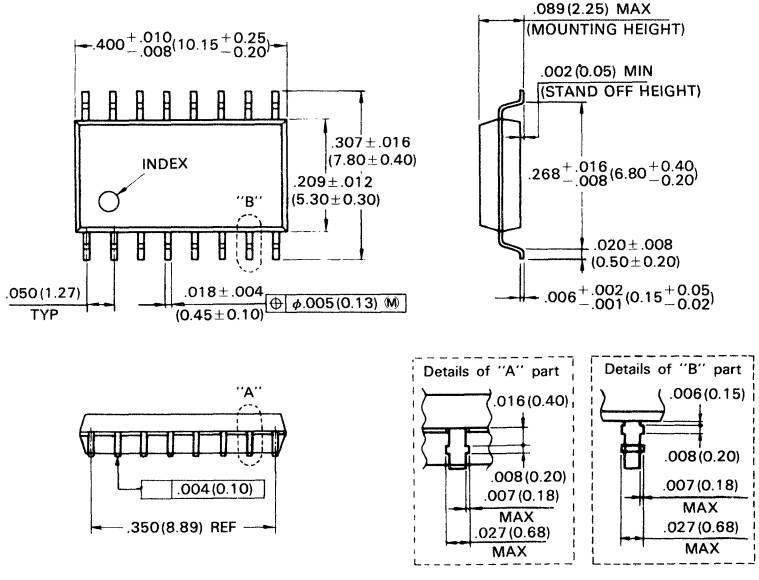
MB1518 APPLICATION CIRCUIT



C_1, C_2 : depends on the crystal oscillator.
FC : with internal pull up resistor.

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)



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Dimensions in inches (millimeters)

January 1991
Edition 1.0

FUJITSU

DATA SHEET

MB1519

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER

3

DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 600MHz PRESCALER

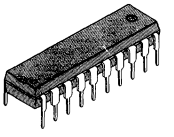
The Fujitsu MB1519 is a 600MHz dual serial input PLL (Phase Locked) frequency synthesizer designed for cellular telephone and cordless telephone applications.

The MB1519 has two PLL circuits on a single chip: one for transmit and the other for reception. Separate power supply pins are provided for the transmit and reception PLL circuits. Transmit PLL contains a low sensitivity charge pump for ease of modulation and reception PLL contains a high sensitivity charge pump for faster lock up time.

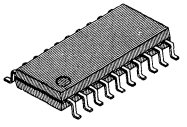
600 MHz dual modulus prescalers are on chip and enables a pulse swallow function.

It operates supply voltage of 3.0V typ. and dissipates 11mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- High operating frequency: fin = 600MHz
- Low power supply voltage: V_{CC} = 2.7 to 5.5V
- Low power supply current: I_{CC} = 11mA typ, @3V.
- Wide operating temperature: T_A = –40 to 85°C
- Two charge pumps
  Low sensitivity charge pump for transmit
  High sensitivity charge pump for reception
- Plastic 20-pin dual in line package (Suffix: -P)
  Plastic 20-pin flat package (Suffix: -PF)

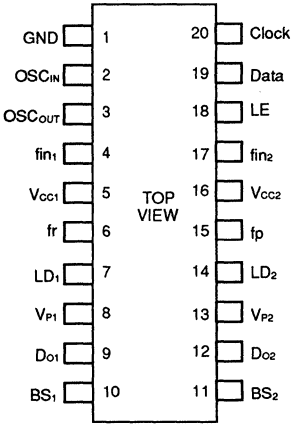


PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
	V_P	V_{CC} to 10.0	
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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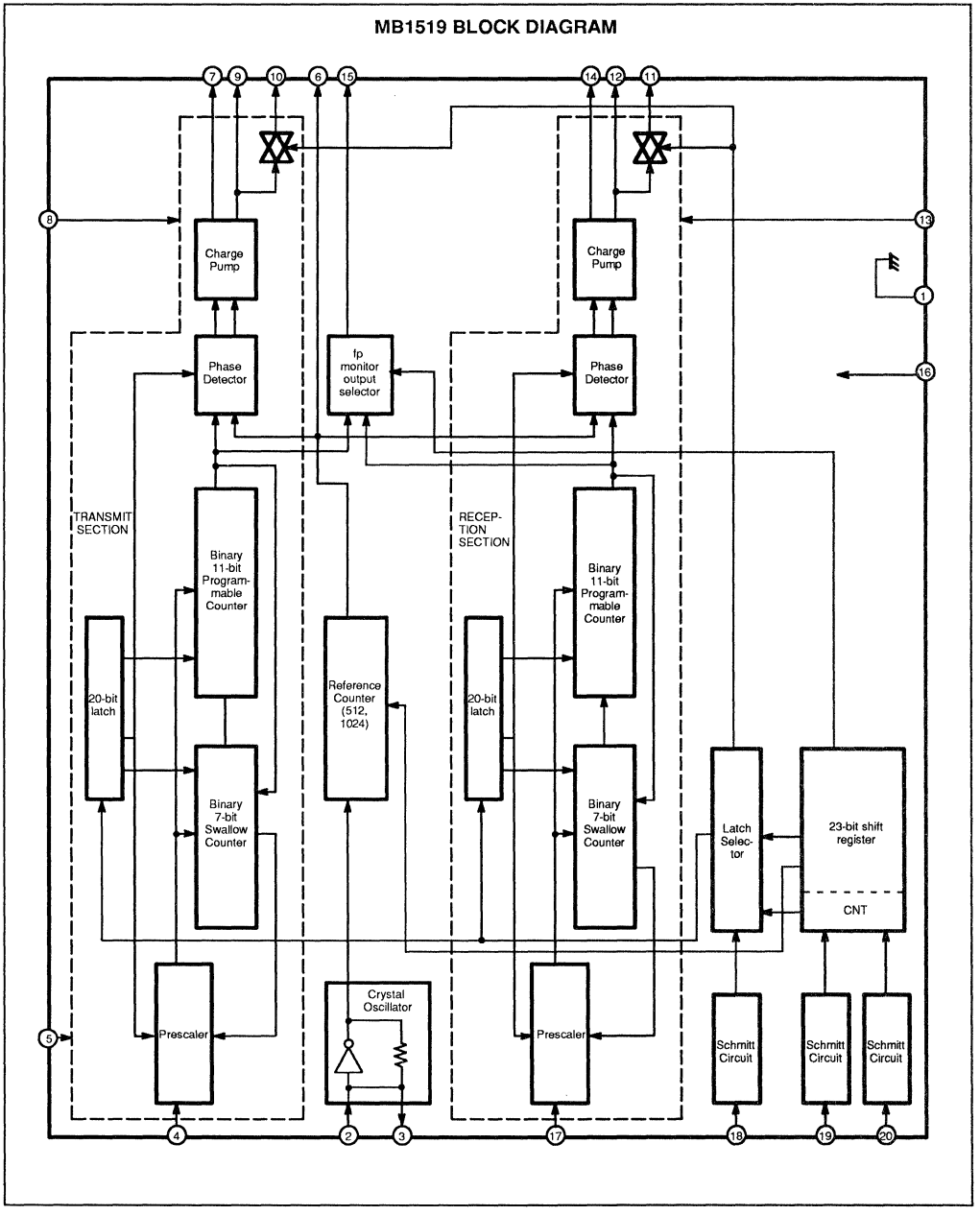
3

MB1519 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

TRANSMIT/RECEPTION BLOCK

- 20-bit latch
- Programmable divider consisting of:
  Binary 7-bit swallow counter (Divide ratio: 0 to 127)
  Binary 11-bit programmable counter (Divide ratio: 16 to 2047)
- Phase detector with phase polarity change function
- 600MHz dual modulus prescaler (Divide ratio: 64/65)
- Charge pump

COMMON BLOCK

- 23-bit shift register
- Programmable divider consisting of:
  Reference counter (Divide ratio: 512, 1024)
  (Divide frequency = 25kHz, 12.5kHz (Crystal oscillator frequency = 12.8MHz)
- Crystal oscillator
- fp monitor output selector
- Latch selector
- Schmitt circuits
- Analog switches

PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSC_{IN}
OSC_{OUT}</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSC_{IN} pin and OSC_{OUT} pin.</td></tr>
<tr><td>4</td><td>fin_1</td><td>I</td><td>Prescaler input pin of transmit section.
The connection with VCO should be AC connection.</td></tr>
<tr><td>5</td><td>V_{CC1}</td><td>–</td><td>Power supply voltage input pin of transmit section.
When power is OFF, latched data of transmit section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output.</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of transmit section.
<table><tr><th>Condition</th><th>LD pin output level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>8</td><td>V_{P1}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of transmit section.</td></tr>
<tr><td>9</td><td>D_{O1}</td><td>O</td><td>Charge pump output pin of transmit section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of transmit section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of reception section.
Usually this pin is high-impedance state. During SW is ON (LE = high), charge pump output is connected to this pin.</td></tr>
<tr><td>12</td><td>D_{O2}</td><td>O</td><td>Charge pump output pin of reception section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>V_{P2}</td><td>–</td><td>Power supply voltage input for charge pump and analog switch of reception section.</td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detect signal output pin of reception section.
<table><tr><th>Condition</th><th>LD pin output level</th></tr><tr><td>Lock</td><td>H</td></tr><tr><td>Unlock</td><td>L</td></tr></table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output.
This pin outputs divided frequency of transmit section or reception section depending upon FP bit setting.
<table><tr><th>FP bit</th><th>Output</th></tr><tr><td>H</td><td>Transmit section (fp1)</td></tr><tr><td>L</td><td>Reception section (fp2)</td></tr></table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for reception section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of reception section and reference counter is cancelled.
17	fin_2	I	Prescaler input pin of reception section. The connection with VCO should be AC conneciton.
18	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data. At this moment, charge pump output signal is output from BS pin since internal analog swith becomes ON.
19	Data	I	Serial data input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. The stored data in the shift register is transferred to either transmit section or reception section depending upon a control data. Control bit data: H → The destination of data: Latch of transmit section Control bit data: L → The destination of data: Latch of reception section
20	Clock	I	Clock input pin of 23-bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of data into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

M: Preset divide ratio of dual modulus prescaler (64)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillator frequency

R: Preset divide ratio of reference counter (512 or 1024)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is input using three pins, Data pin, Clock pin, and LE pin. Programmable divider of transmit section and programmable divider of reception section are controlled individually.
Serial data of binary data is input into Data pin.
On rising edge of clock shifts one bit of serial data into the shift register. When load enable signal is high, the data stored in the shift register is transferred to either the latch of transmit section or the latch of reception section depending upon the control bit data setting.

Control data	Destination of serial data
H	Latch of transmit section
L	Latch of reception section

SHIFT REGISTER CONFIGURATION

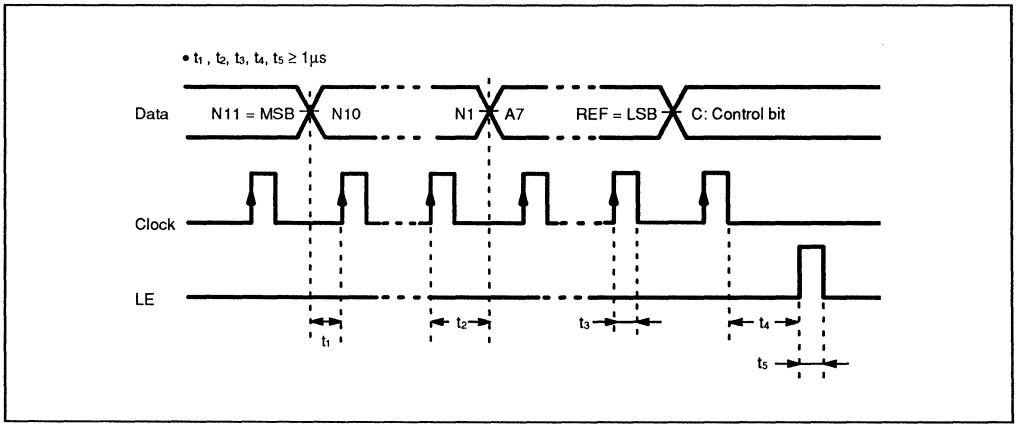
Control bit

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
C	R	F	D	F	A	A	A	A	A	A	A	N	N	N	N	N	N	N	N	N	N	N
N	E	P	M	C	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	9	10	11
T	F		Y																			

N1 to N11 : Divide ratio of the programmable counter setting bit (16 to 2047)
A1 to A7 : Divide ratio of the swallow counter setting bit (0 to 127)
FC : Phase control bit of the phase detector
DMY : Dummy bit (sets to low)
FP : Output of the programmable divider control bit (fp1 or fp2)
REF : Divide ratio of the reference counter setting bit (512 to 1024)
CNT : Control bit

SERIAL DATA INPUT TIMING



On rising edge of the clock shifts one bit of the data into the shift register.

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
·	·	·	·	·	·	·	·	·	·	·	·
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 16 is prohibited.
Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
·	·	·	·	·	·	·	·
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

DMY : DUMMY BIT INPUT
This bit is set to low in operation.

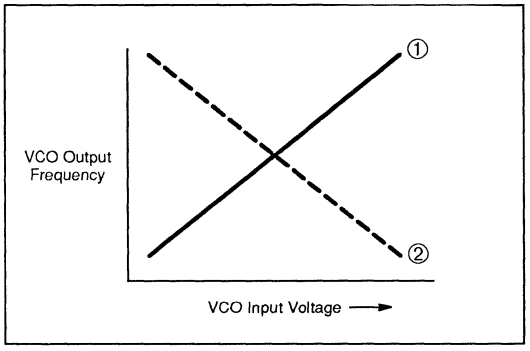
REF : DIVIDE RATIO (R) OF THE REFERENCE COUNTER SETTING BIT
H = 512 (fr = 25.0 kHz)
L = 1024 (fr = 12.5 kHz)

FP : OUTPUT OF THE PROGRAMMABLE DIVIDER SETTING BIT
H = fp pin (15 pin) outputs programmable divider output frequency (fp1) of transmit section.
L = fp pin (15 pin) outputs programmable divider output frequency (fp2) of reception section.

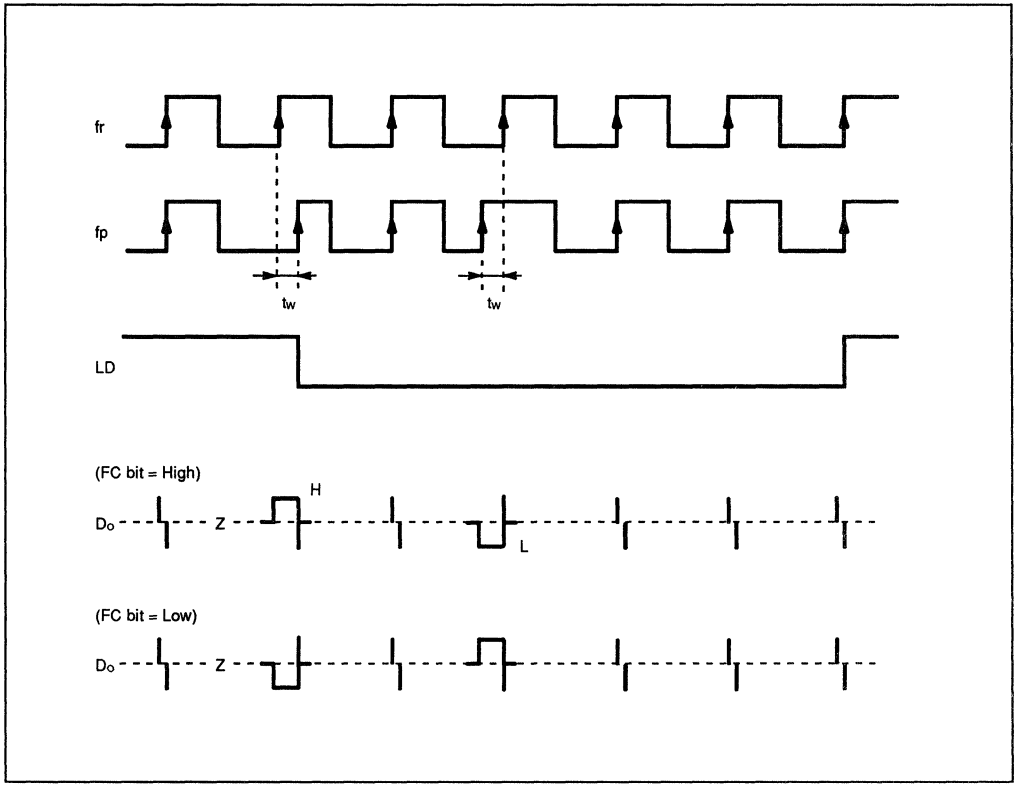
FC : PHASE CONTROL BIT OF THE PHASE DETECTOR
Output of charge pump is selected by FC pin.

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: Z = High-impedance
Depending upon the VCO porality, FC bit should be set.



PHASE DETECTOR OUTPUT WAVEFORM



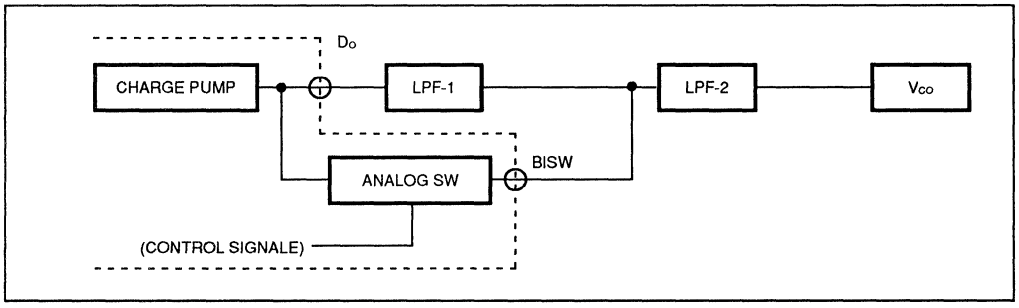
Note:
- Phase difference detection range = -2π to $+2\pi$
- LD output becomes low when phase difference is t_w or more.
  LD output becomes high when phase difference less than t_w is reperated 3 times or more.
  (e. g. t_w = 625 to 1250 ns, foscin = 12.8 MHz)
- Spike apperance depends on the charge pump characteristics. The spike is output to diminish the dead band.
- When fr > fp or fr < fp, spike might not generate depending up the VCO characteristics.

ANALOG SWITCH

ON/OFF of the analog switch is controlled by the combination of the control data and LE signal. When the analog switch is ON, BS1, BS2 pin output the charge pump output (D_{O1}, D_{O2}). When analog switch is OFF, BS pin is set to high impedance.

	Control data = H Divide ratio of transmit section is set		Control data = L Divide ratio of reception section is set	
	LE = H	LE = L	LE = H	LE = L
Analog switch of transmit section	ON	OFF	OFF	OFF
Analog switch of reception section	OFF	OFF	ON	OFF

When a analog switch is inserted between LP1 and LP2, faster lock up time is achieved to reduce LPF time constant during PLL channel switching.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V	$V_{CC1} = V_{CC2}$
	V_P	V_{CC}	–	8.0	V	
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	T_A	–40	–	+85	°C	

HANDLING PRECAUTIONS

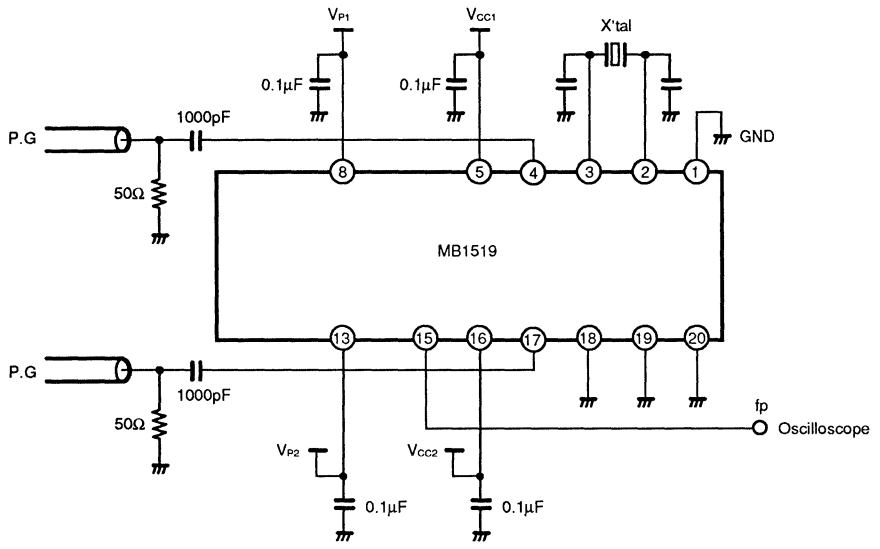
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

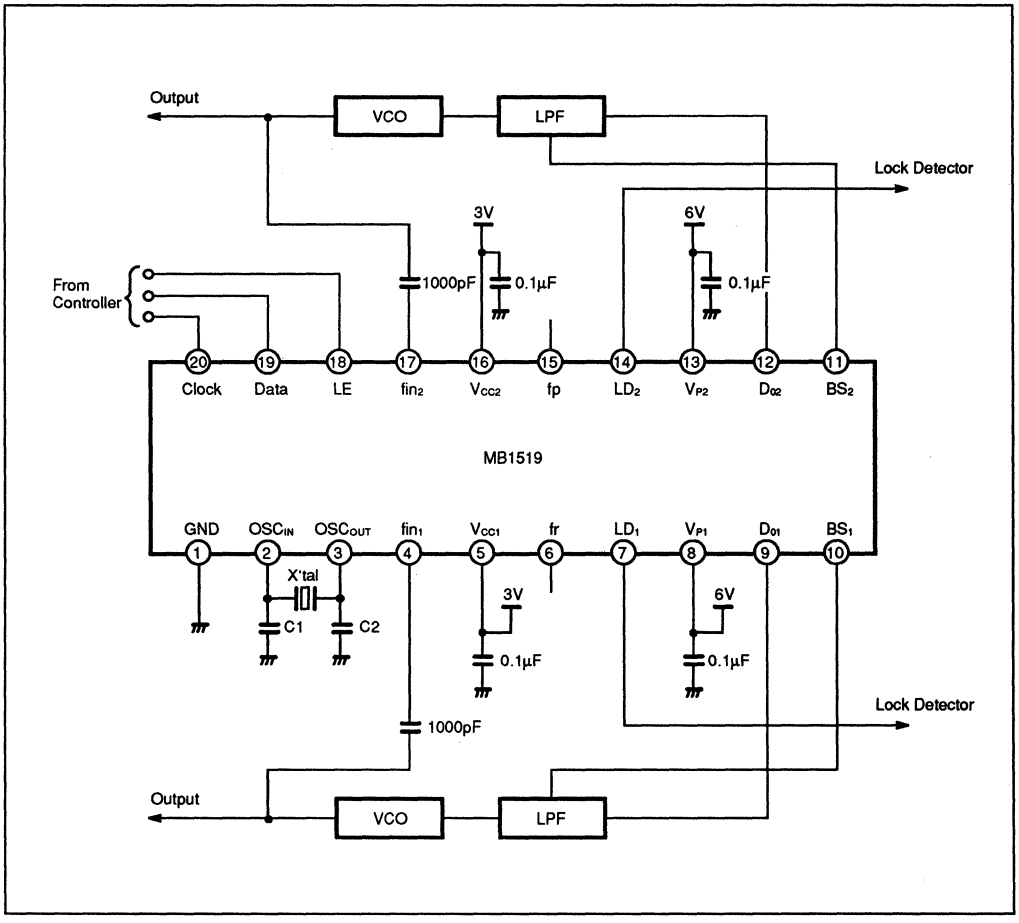
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current*		I_{CC1}	Reception section is active.	–	5.5	–	mA
		I_{CC2}	Transmit/reception section are active.	–	11.0	–	
Operating Frequency**	fin	fin		10	–	600	MHz
	OSC_{IN}	f_{OSC}		–	12.8	20	
Input Sensitivity	fin	Vfin	V_{CC} = 2.7 to 4.0V, 50Ω	–8	–	0	dBm
			V_{CC} = 4.0 to 5.5V, 50Ω	–4	–	2	
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High-level Input Current	Data, Clock LE	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
	FC	I_{FC}		–	–60	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level Output Voltage	Except D_O and OSC_{OUT}	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}		–	–	0.4	
High-impedance Cutoff Current	D_O, ϕP	I_{OFF}	V_P = V_{CC} to 8.0V V_{OOP} = GND to 8.0V	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	
	D_{O1}	I_{OH}	V_P = 6V	–	–1	–	
		I_{OL}	V_{CC} = 3V	–	12	–	
	D_{O2}	I_{OH}	V_P = 6V	–	–3	–	
		I_{OL}	V_{CC} = 3V	–	6	–	
Analog Switch ON Resistance		R_{ON}		–	25	–	Ω

Notes: *: fin = 600MHz, OSC_{IN} = 12.8MHz, V_{CC1} = V_{CC2} = 3.0V. The remaining input pins are grounded and output pins are open.
**: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



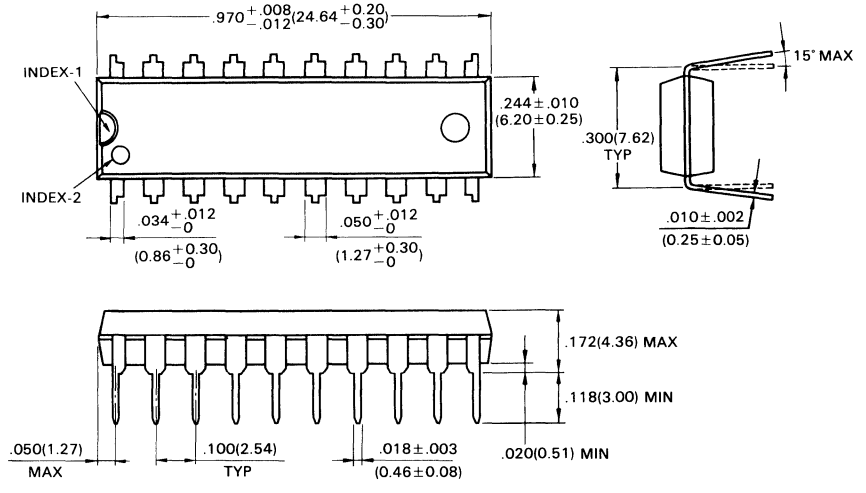
APPLICATION EXAMPLE



Note: V_{P1}, V_{P2} : 8 V max.
C1, C2 : depends on the crystal oscillator.
Clock, Data, LE : involve the schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent the oscillation.
X'tal : 12.8MHz

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)

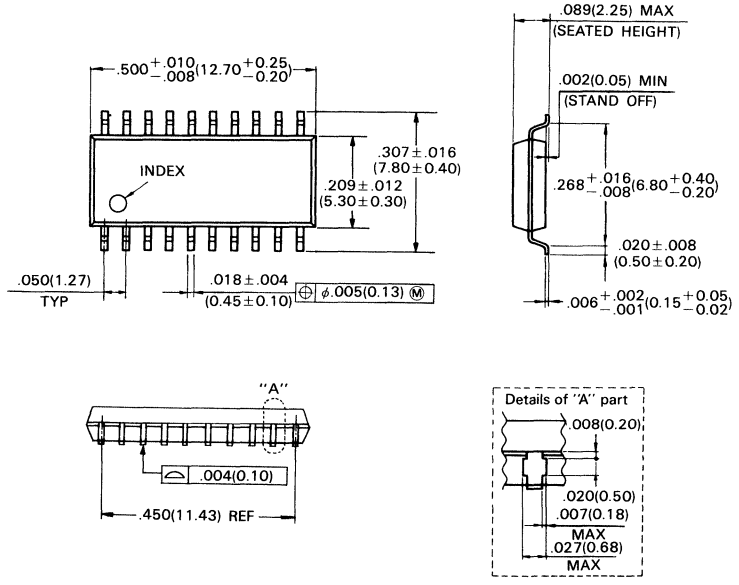


©1988 FUJITSU LIMITED D20003S-3C

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M01)



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Dimensions in inches (millimeters)

Section 4

Single-Chip VCOs/Prescalers — *At a Glance*

Page	Device	Maximum Frequency	Divide Ratio	Supply I_{CC}	Supply V_{CC}
4–3	MB551	1 GHz	128 or 129	16 mA (typ)	5 V (typ)

NOTE: The MB551 is available in an 8-pin Plastic FPT package.

4

DATA SHEET

FUJITSU

MB551
1 GHz Dual Modulus Prescaler

The Fujitsu MB551 is a dual modulus prescaler with low supply current and a VCO (voltage controlled oscillator). It is used in a frequency synthesizer in the 1 GHz region.

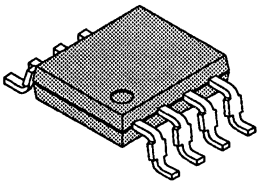
The MB551 contains a Colpitts oscillator with a grounded base capacitor, an open-collector output buffer amplifier, a prescaler interface circuit, and a dual modulus prescaler that can select divide ratios of 128 or 129.

The VCO oscillator section can be constructed with external components such as a capacitor, dieletric oscillator (resonator), and variable capacitor.

The on-chip VCO and prescaler are connected on internal control circuit. Thus, the influence caused by carrier to noise by deviation of prescaler input load is suppressed.

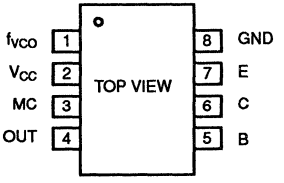
The MB551 operates on a supply voltage of 5 V typical and has a 16 mA supply current typical.

- Oscillator frequency: 1 GHz max.
- Low supply current: I_{CC} = 16 mA typ.
- Oscillator output voltage: 0 dBm typ.
- Carrier to noise ratio:
  70 dB typ. (Δf = 50 kHz, BW = 15 kHz
  65 dB typ. (Δf = 25 kHz, BW = 15 kHz
- Pulse swallow method: Divide ratio of 128 or 129
- Prescaler output contains termination circuit: V1 = 1.6 Vp–p typ.
- Signal to noise ratio: 45 dB typ. (BW = 0.3 to 3 kHz, 3 kHz Dev, 1 kHz tone)
- Stable oscillator output
- Supply voltage dependence: ±200 kHz/V typ.
- Frequency stability: 35 ppm/°C (Referenced to 25°C)
- Load regulation: ±2 MHz VSWR = 2 typ.
- Plastic 8-pin flat package: Suffix –PF



Plastic Package
FPT-08P-M01

Pin Assignment



Pin assignment to be determined

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Oscillator Transistor Base, Emitter Input Voltage	V_B V_E	DC voltage is not input from outside.	
Input Voltage for MC and OUT (3, 4 pins)	V_{P1}	–0.5 to V_{CC} +0.5	V
Input Voltage for f_{VCO} and C (1, 6 pins)	V_{P2}	$V_{CC} \leq V_{P2} < +7.0$	V
Input Current	I_P	±10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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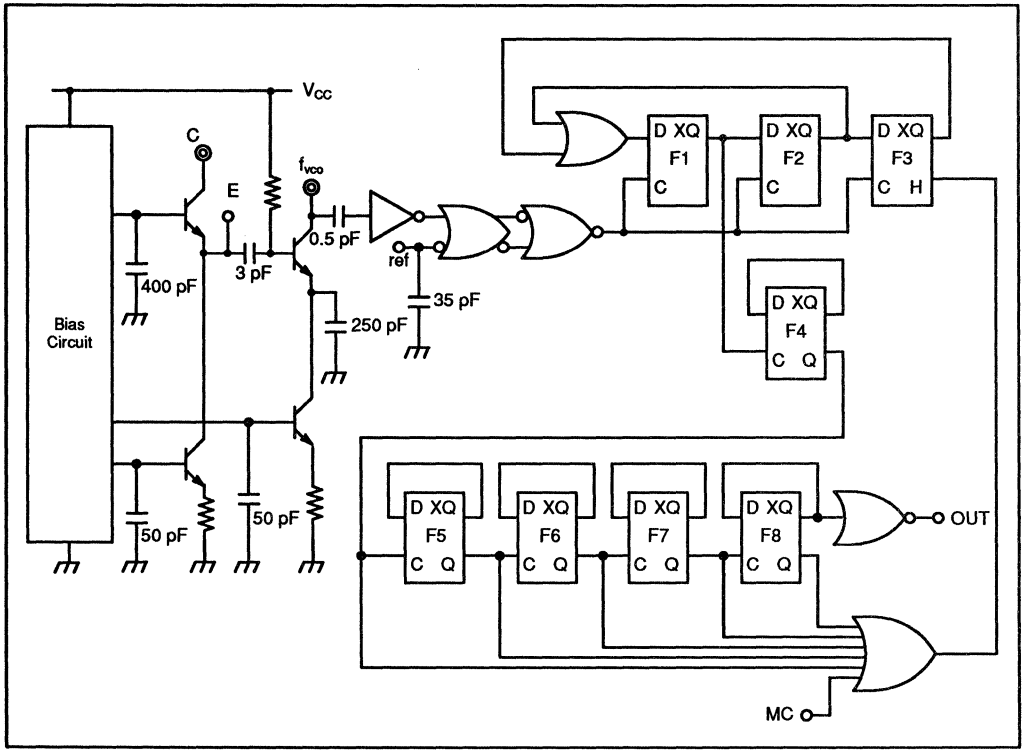
Figure 1. MB551 Equivalent Circuit



PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Description
1	f_{VCO}	O	Voltage controlled oscillator output
2	V_{CC}	–	Supply voltage input, +5V
3	MC	I	Modulus control input
4	OUT	O	Prescaler output
5	B	–	Oscillator transistor base pin
6	C	–	Oscillator transistor collector pin
7	E	–	Oscillator transistor emitter pin
8	GND	–	Ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
External Variable Capacitor Control Voltage	V_T	1.5		4.5	V
Operating Temperature	T_A	–40		+85	°C
Prescaler Output Load	C_L			8	pF

4

VCO ELECTRICAL CHARACTERISTICS[1,2]

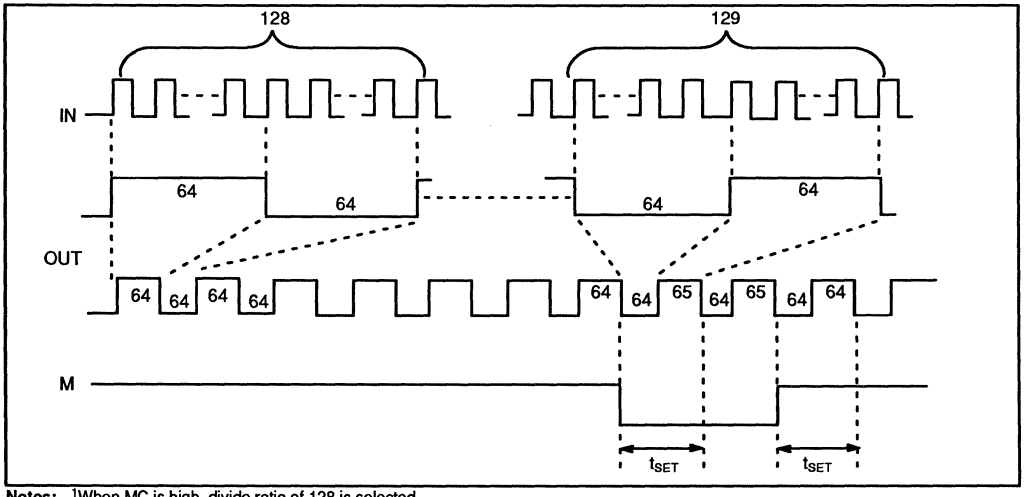
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Oscillator Frequency	f_{OSC}		–TBD–		900	MHz
Oscillator output	P_{OUT}	–To be supplied–		0		dBm
Carrier to Noise Ratio	C/N	Δf=25kHz, BW=15kHz		65		dB
Signal to Noise Ratio	S/N	BW = 0.3 – 3kHz, 3kHz Dev. Tone 1kHz		45		dB
Fundamental to 1st Harmonic Ratio	SP–1			–10		dB
Frequency Stability	Δf_t	T_A = –40 – 85°C Referenced to 25°C		35		ppm/°C
Supply Deviation	Δf_V	V_{CC} = 5V ±10%		±100		kHz/V
Conversion Gain	Δf_{OSC}	Control range: 1.5 – 4.5V		4.3		MHz/V
Load Regulation	Δf_{SWR}	V_{SWR} = 2.0 All phase Referenced to 50 Ω		±2		MHz

Notes: [1]These values depend on external components.
[2]These values are measured under the test circuit shown in Figure 2.

PRESCALER ELECTRICAL CHARACTERISTICS

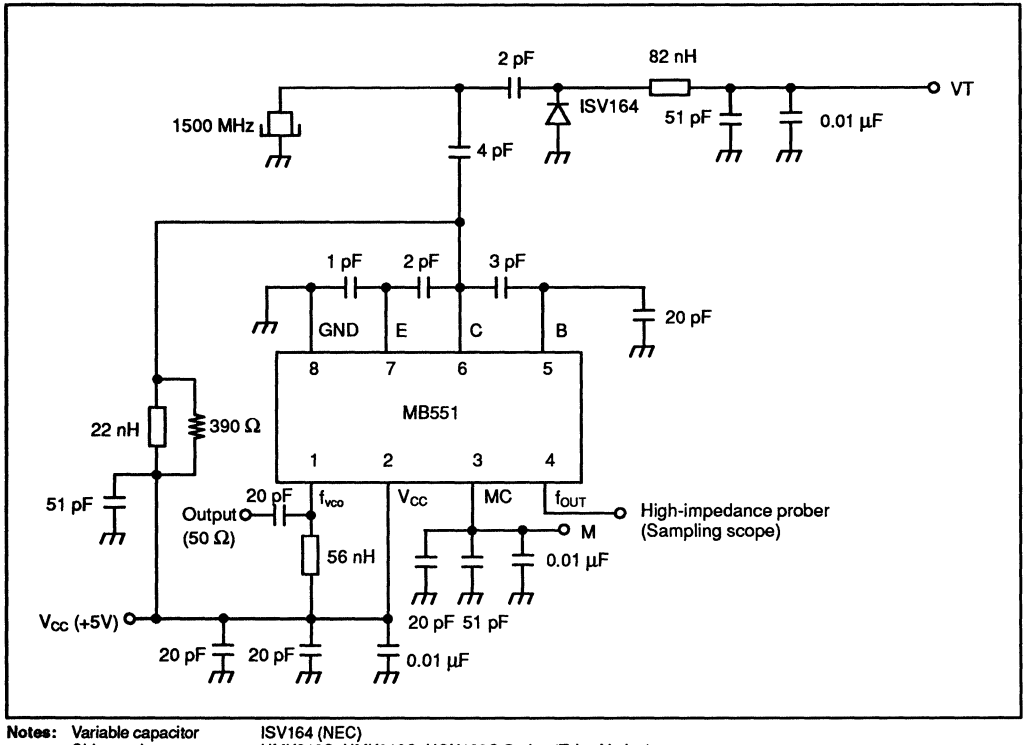
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Current	I_{CC}			16.0		mA
Output Amplitude	V_{OUT}	Internal termination resistor is used. Load capacitor is less than 8 pF.	1.0	1.6		Vp–p
Input Frequency	fin	Minimum value is measured with input coupling capacitor 1000 pF.	10		900	MHz
Input Signal Amplitude	Vin		–4		6	dBm
High-level Input Voltage for MC	V_{IH}		2.0			V
Low-level Input Voltage for MC	V_{IL}				0.8	V
High-level Input Current for MC	I_{IH}				0.4	mA
Low-level Input Current for MC	I_{IL}		–0.2			mA
Modulus Setup Time	$t_{SE}T$			16	26	ns

DUAL MODULUS FUNCTION



Notes: [1]When MC is high, divide ratio of 128 is selected.
[2]When MC is low, divide ratio of 129 is selected.
(V_{IH} = 2.0 V min., V_{IL} = 0.8 V max.)
[3]When divide ratio of 129 is selected, positive pulse is added by 1 to 65.
[4]The typical setup time is 16 ns from the MC signal input to the timing of change of prescaler divide ratio.

Figure 2. Test Circuit Example–I

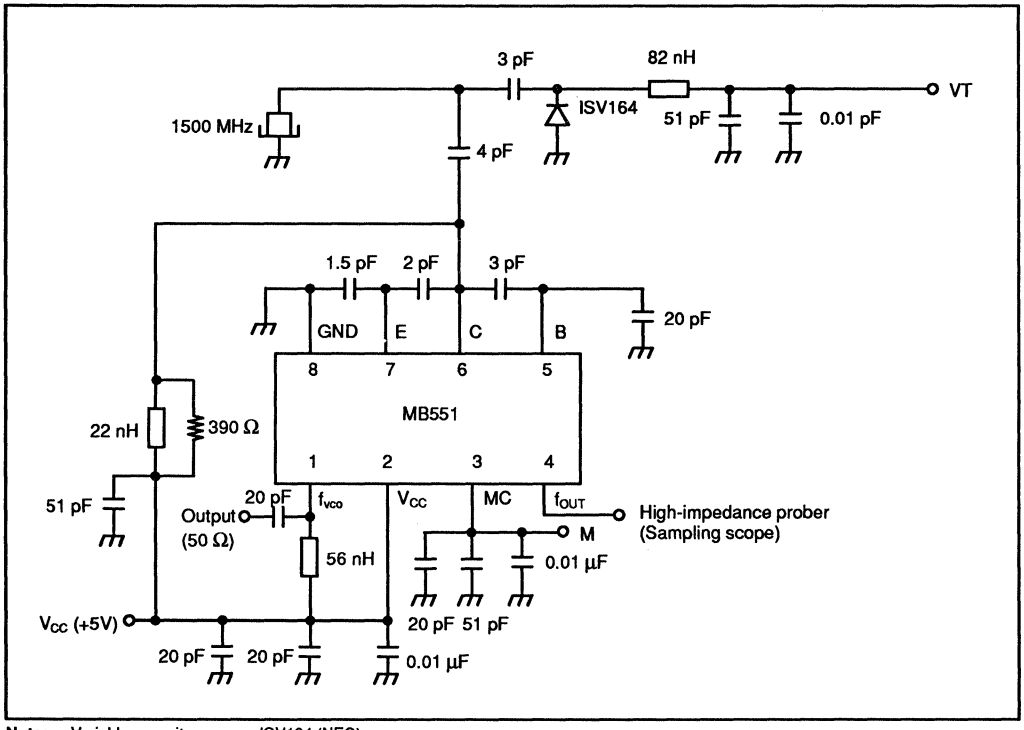


Notes:

Variable capacitor	ISV164 (NEC)
Chip condenser	UMK316C, UMK212C, UCN103C Series (Taiyo Yuden)
Chip coil	LQN2A Series (Murata)
Dielectric Oscillator	DRR060UE (Murata)

4

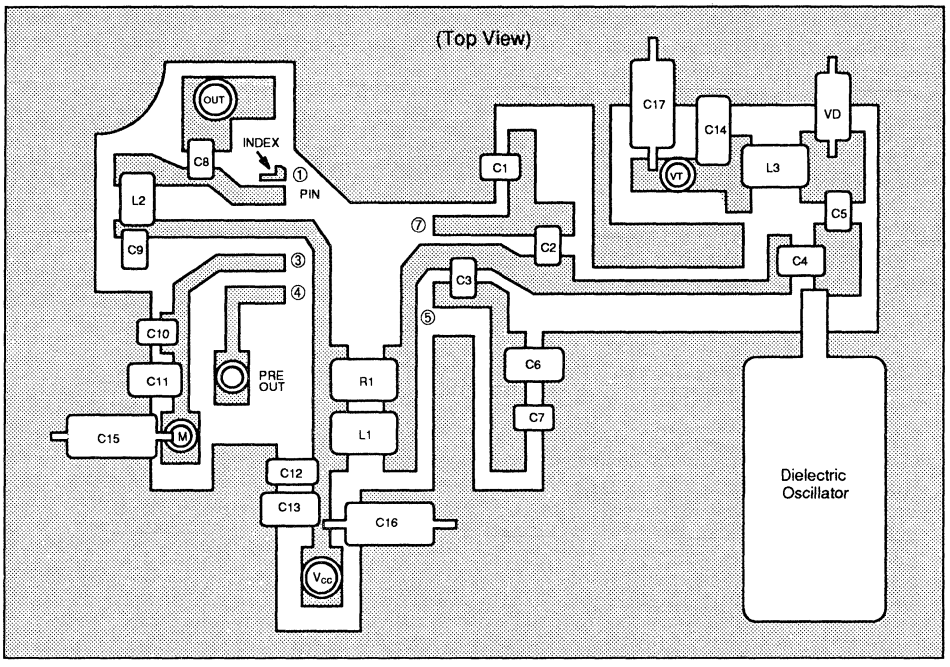
Figure 3. Test Circuit Example–II



Notes:

	Variable capacitor	ISV164 (NEC)
	Chip condenser	UMK316C, UMK212C, UCN103C Series (Taiyo Yuden)
	Chip coil	LQN2A Series (Murata)
	Dielectric Oscillator	DRR060UE (Murata)

Fig. 4 – RECOMMENDED PRINT CIRCUIT BOARD PATTERN



(Parts List)

C1	: 1pF	(Taiyo Yuden UMK212C)	C15	: 0.01μF	(Film condenser)
C2	: 2pF	(Taiyo Yuden UCN103C)	C16	: 0.01μF	(Film condenser)
C3	: 3pF	(Taiyo Yuden UMK212C)	C17	: 0.01μF	(Film condenser)
C4	: 4pF	(Taiyo Yuden UMK212C)			
C5	: 2pF	(Taiyo Yuden UMK212C)			
C6	: 20pF	(Taiyo Yuden UMK316C)	R1	: 390Ω	(Rohm MCR25)
C7	: 51pF	(Taiyo Yuden UMK212C)			
C8	: 20pF	(Taiyo Yuden UMK316C)			
C9	: 20pF	(Taiyo Yuden UMK316C)	L1	: 22nH	(Murata LQN2A)
C10	: 51pF	(Taiyo Yuden UMK212C)	L2	: 56nH	(Murata LQN2A)
C11	: 20pF	(Taiyo Yuden UMK316C)	L3	: 82nH	(Murata LQN2A)
C12	: 51pF	(Taiyo Yuden UMK212C)			
C13	: 20pF	(Taiyo Yuden UMK316C)			
C14	: 51pF	(Taiyo Yuden UMK212C)	VD	: 1SV164	(NEC)

Dielectric oscillator : (Murata DRR060 Serise, 1.5GHz)

TYPICAL CHARACTERISTICS CURVES

Fig. 5 – Supply Current vs. Supply Voltage

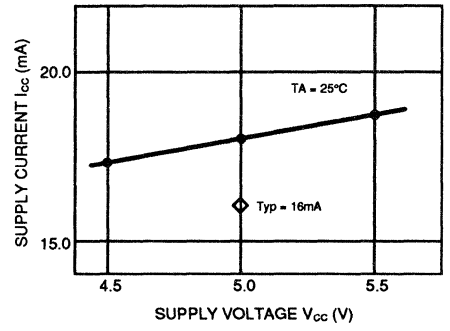
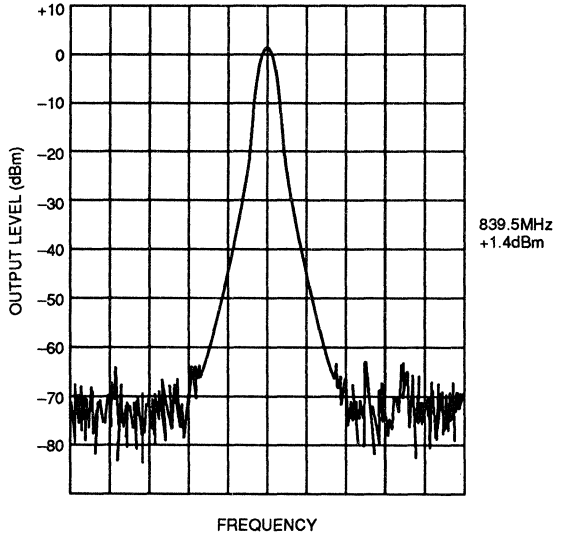


Fig. 6 – Oscillator Waveform (Span = 50kHz)



(TEST CIRCUIT – I, RECOMMENDED PRINTED CIRCUIT BOARD USED)

Fig. 7 – Conversion Gain

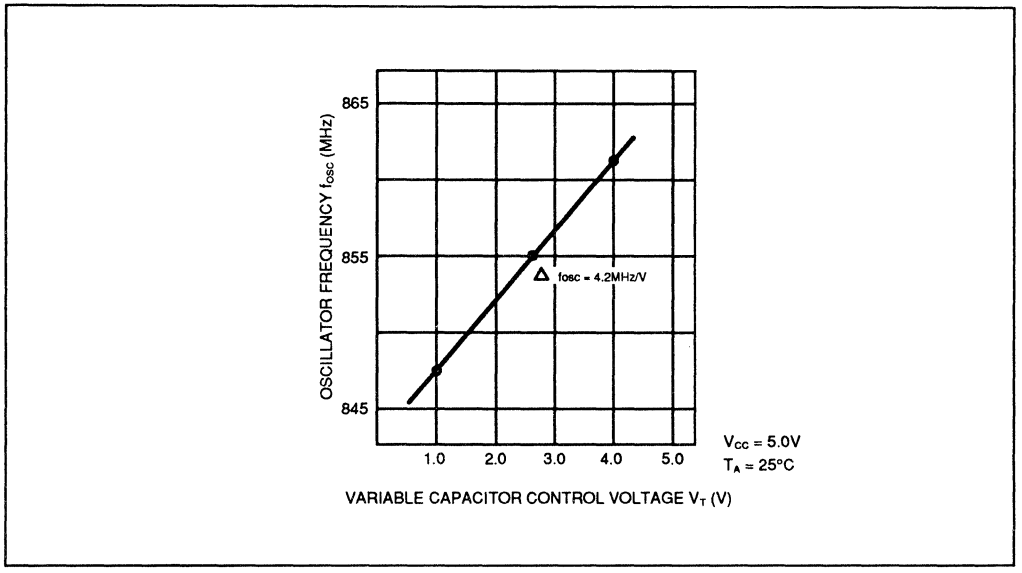
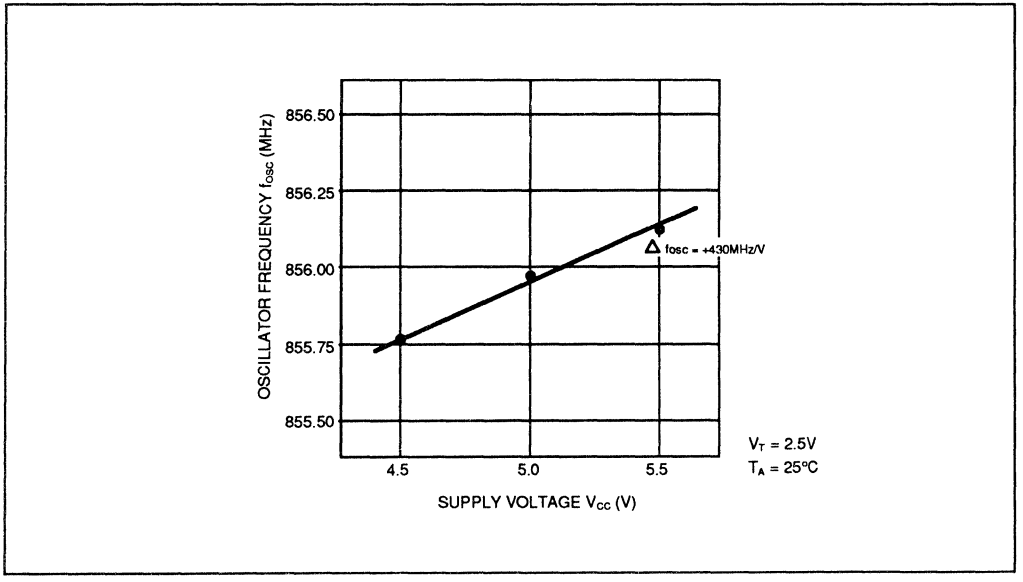


Fig. 8 – Supply Voltage Dependence



(TEST CIRCUIT – I, RECOMMENDED PRINTED CIRCUIT BOARD USED)

Fig. 9 – C/N, S/N vs. Variable Capacitor Control Voltage

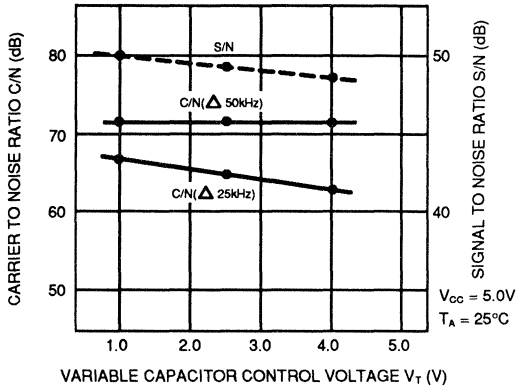


Fig. 10 – Supply Voltage Dependence

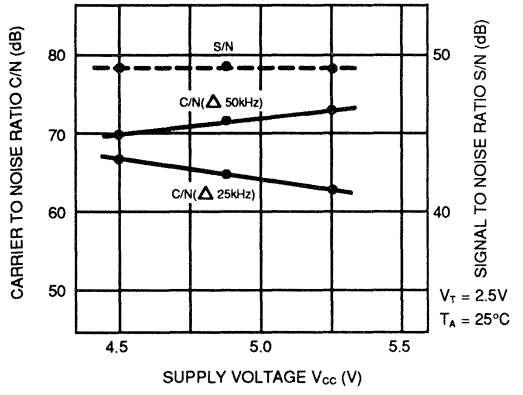


Fig. 11– Prescaler Input Sensitivity Curve (Supply Voltage Dependence) (T_A = 25°)

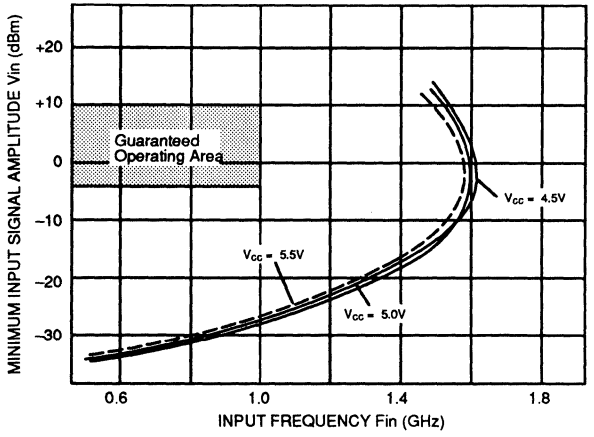
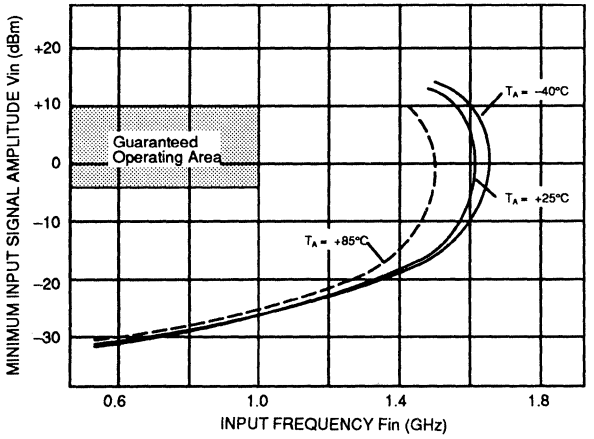


Fig. 12– Prescaler Input Sensitivity Curve (Temperature Dependence) (V_{CC} = 5V))



(TEST CIRCUIT – II)

Fig. 13 – Conversion Gain

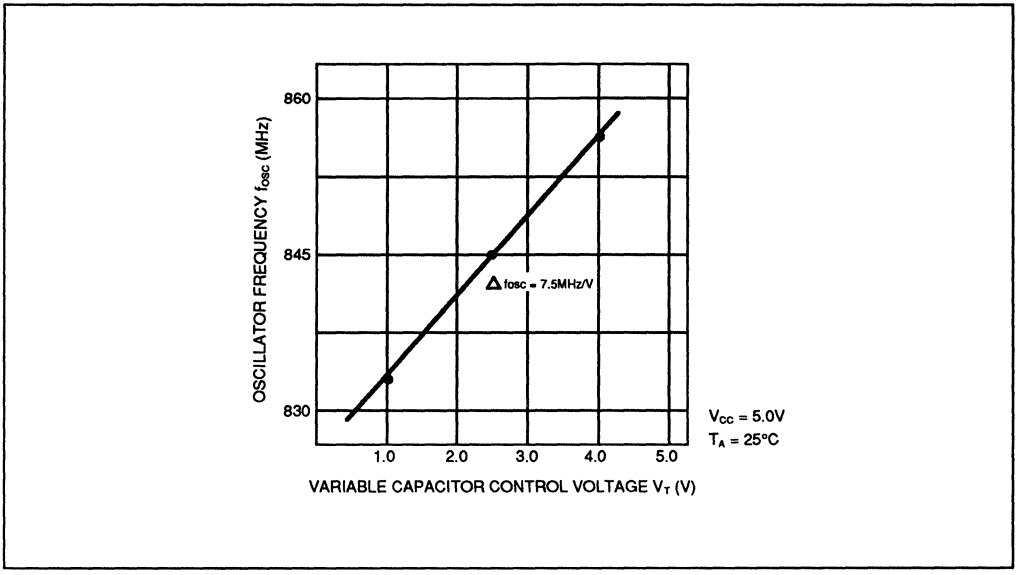


Fig. 14 – C/N, S/N vs. Variable Capacitor Control Voltage

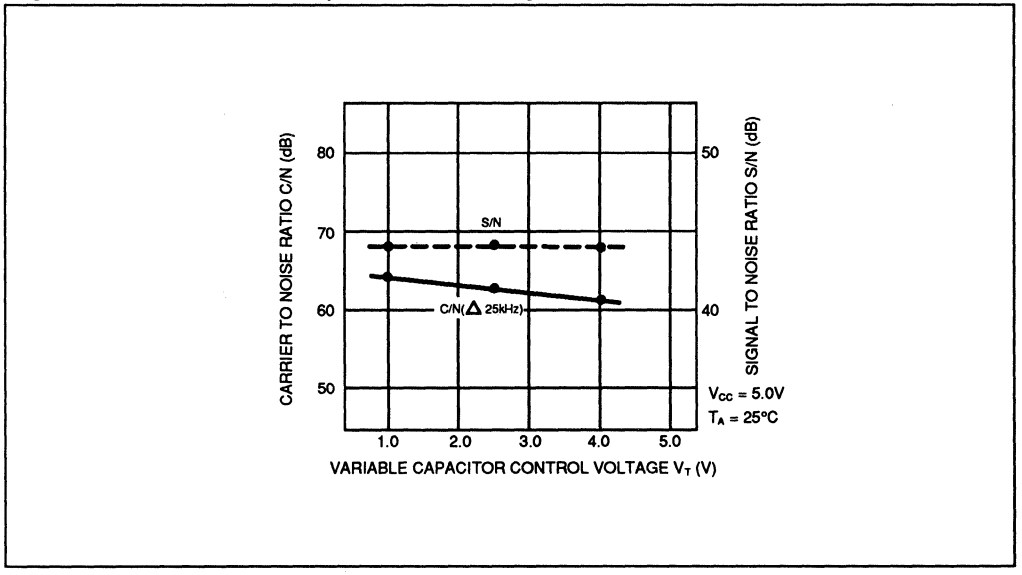
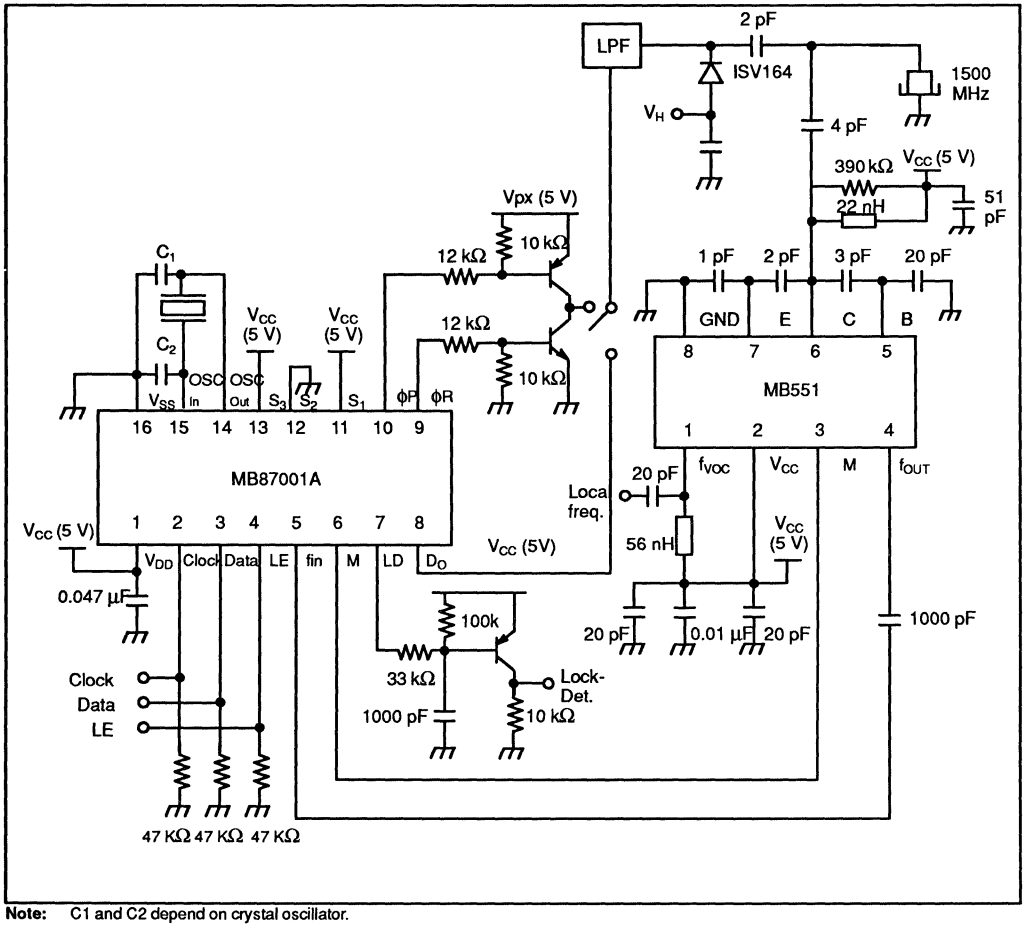
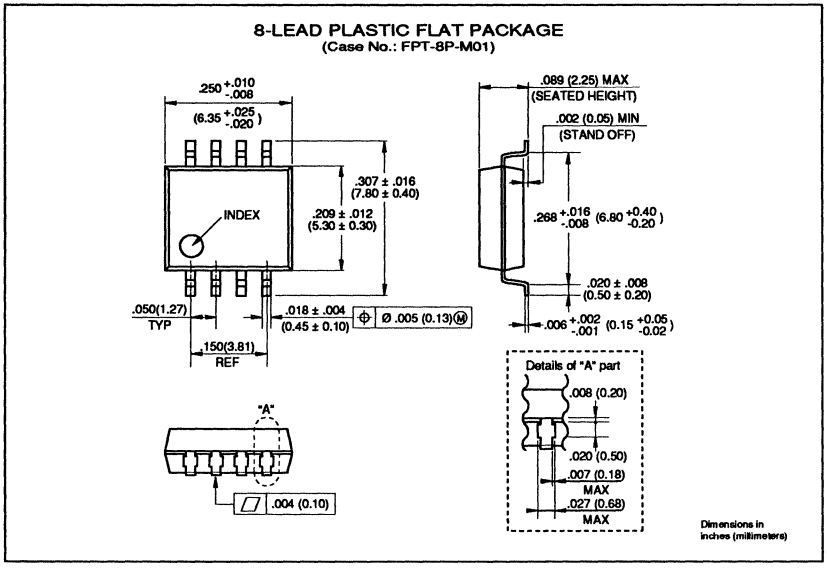


Figure 15. Application Example



Note: C1 and C2 depend on crystal oscillator.

PACKAGE DIMENSIONS



Section 5

Piezoelectric Devices — *At a Glance*

Page	Device	Description	Frequency Range	Package Option	
5–3	F5CB Series	SAW-Bandpass Filter	700-1000 MHz	8-pin	LCC
5-17	M2 Series	VCO (D100)	4–30 MHz	14-pin	DIP
5-25	M2 Series	VCO (D300)	4–30 MHz	16-pin	SIP
5-35	M3 Series	VCO (D001)	50–300 MHz	16-pin	DIP
5-39	M3 Series	VCO (D101)	50–300 MHz	14-pin	DIP

5

FUJITSU

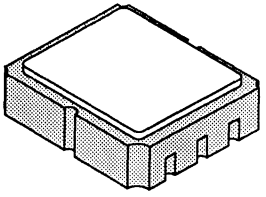
DATA SHEET

F5CB Series
Piezoelectric Filters

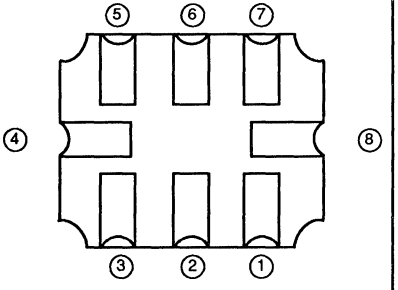
SAW-BPF, 700 MHz to 1000 MHz

The F5 series are wide bandpass filters for use in the 700 MHz to 1000 MHz range. The F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has a high electromechanical coupling coefficient. The $LiTaO_3$ also provides wide bandwidths and exceptional stability. Fujitsu's exclusive mounting technique makes the F5 series very compact and surface mountable. The F5 is suitable for use in handheld phones.

- Considerably smaller and lighter than the ceramic filter (volume and weight are reduced by 1/30)
- Surface mount package (SMT)
- Wide variety of bandwidths
- Low insertion loss
- High power rating: 0.2 W guaranteed
- 8-pad ceramic package (LCC)



(Bottom View)



Pin No.	Pin Name	Description
1	GND	Ground Pin
2	IN	Input Pin
3	GND	Ground Pin
4	GND	Ground Pin
5	GND	Ground Pin
6	OUT	Output Pin
7	GND	Ground Pin
8	GND	Ground Pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Operating Temperature	T_a	–30 to 70	°C
Storage Temperature	T_{STG}	–40 to 100	°C
Maximum Input Level	P_{IN}	200	mW
Frequency Range		700 to 1000	MHz

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Operating Temperature	T_a	–30 to 70	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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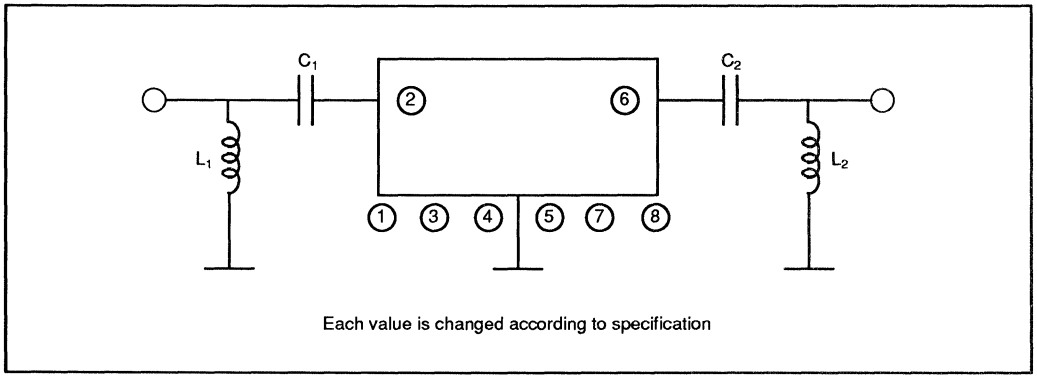
STANDARD FREQUENCIES

Number	Model	System	Use*	Center Frequency (MHz)	Bandwidth (MHz)
1	F5CB-836M50-G201	AMPS/EAMPS	Tx	836.5	25
2	F5CB-881M50-G201	AMPS/EAMPS	Rx	881.5	25
3	F5CB-888M50-G201	ETACS	Tx	888.5	33
4	F5CB-933M50-G202	ETACS	Rx	933.5	33
5	F5CB-902M50-G201	NMT	Tx	902.5	25
6	F5CB-947M50-G201	NMT	Rx	947.5	25
7	F5CB-911M50-G201	NTACS	Tx	911.5	27
8	F5CB-856M50-G201	NTACS	Rx	856.5	27

*Tx = Transmitter; Rx = Receiver

5

TEST CIRCUIT



Each value is changed according to specification

ELECTRICAL CHARACTERISTICS – EXAMPLES

Example 1. AMPS Specification (Tx)
Part Number F5CB-836M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	824 to 849 MHz	—	3.5	4.2	dB
In-band Ripple		824 to 849 MHz	—	1.0	1.5	dB
Absolute Out-of-band Attenuation		DC to 800 MHz	20	25	—	dB
		869 to 894 MHz	20	25	—	dB
		894 to 3000 MHz	15	20	—	dB
In-band VSWR		824 to 849 MHz	—	1.7	2.0	
Matching Constants	C_1			7	—	pF
	L_1			9	—	nH
	C_2			6	—	pF
	L_2			11	—	nF

Example 2. AMPS Specification (Rx)
Part Number F5CB-881M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	869 to 894 MHz	—	—	4.5	dB
In-band Ripple		824 to 849 MHz	—	—	1.5	dB
Absolute Out-of-band Attenuation		DC to 824 MHz	20	—	—	dB
		824 to 849 MHz	20	—	—	dB
		917 to 939 MHz	18	—	—	dB
		947 to 1049 MHz	30	—	—	dB
		1049 to 3000 MHz	15	—	—	dB
In-band VSWR		869 to 894 MHz	—	1.8	2.0	
Matching Constants	C_1			6	—	pF
	L_1			7	—	nH
	C_2			7	—	pF
	L_2			9	—	nF

Continued on next page

ELECTRICAL CHARACTERISTICS – EXAMPLES (Continued)

Example 3. ETACS Specification (Tx)
Part Number F5CB-888M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	872 to 900 MHz	—	4.5	5.0	dB
		900 to 905 MHz	—	5.5	6.5	dB
In-band Ripple		872 to 905 MHz	—	—	2.5	dB
Absolute Out-of-band Attenuation		DC to 847 MHz	20	25	—	dB
		847 to 860 MHz	8	12	—	dB
		917 to 920 MHz	10	13	—	dB
		920 to 922 MHz	13	15	—	dB
		922 to 950 MHz	20	23	—	dB
		962 to 995 MHz	30	33	—	dB
		995 to 3000 MHz	15	20	—	dB
In-band VSWR		872 to 905 MHz	—	2.0	2.5	
Matching Constants	C_1			7	—	pF
	L_1			7	—	nH
	C_2			6	—	pF
	L_2			9	—	nF

Continued on next page

ELECTRICAL CHARACTERISTICS – EXAMPLES (Continued)

Example 4. ETACS Specification (Rx)
Part Number F5CB-933M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	917 to 947 MHz	—	4.5	5.0	dB
		947 to 950 MHz	—	5.5	6.5	dB
In-band Ripple		917 to 950 MHz	—	1.0	2.5	dB
Absolute Out-of-band Attenuation		DC to 872 MHz	20	25	—	dB
		872 to 900 MHz	15	18	—	dB
		900 to 902 MHz	13	15	—	dB
		902 to 905 MHz	8	13	—	dB
		962 to 965 MHz	10	15	—	dB
		965 to 970 MHz	15	18	—	dB
		970 to 995 MHz	20	25	—	dB
		1005 to 1040 MHz	30	33	—	
		1040 to 3000 MHz	15	20	—	
In-band VSWR		917 to 950 MHz	—	20	2.5	
Matching Constants	C_1			6	—	pF
	L_1			6	—	nH
	C_2			7	—	pF
	L_2			8	—	nF

Example 5. NMT Specification (Tx)
Part Number F5CB-902M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	890 to 915 MHz	—	4.0	4.5	dB
In-band Ripple		890 to 915 MHz	—	1.3	2.0	dB
Absolute Out-of-band Attenuation		DC to 850 MHz	20	25	—	dB
		850 to 870 MHz	15	22	—	dB
		935 to 960 MHz	20	28	—	dB
		1012 to 1058 MHz	30	33	—	dB
		1058 to 3000 MHz	15	20	—	dB
In-band VSWR		890 to 915 MHz	—	1.5	2.0	
Matching Constants	C_1			5	—	pF
	L_1			6	—	nH
	C_2			6	—	pF
	L_2			9	—	nF

Continued on next page

ELECTRICAL CHARACTERISTICS – EXAMPLES (Continued)

Example 6. NMT Specification (Rx)
Part Number F5CB-947M50-G201

T_a = –30 to 70°C

Item	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	935 to 960 MHz	—	4.0	4.5	dB
In-band Ripple		935 to 960 MHz	—	1.3	2.0	dB
Absolute Out-of-band Attenuation		DC to 890 MHz	20	25	—	dB
		890 to 915 MHz	18	22	—	dB
		980 to 1005 MHz	18	30	—	dB
		1012 to 1058 MHz	28	32	—	dB
		1089 to 1115 MHz	30	32	—	dB
		1115 to 3000 MHz	15	20	—	dB
In-band VSWR		935 to 960 MHz	—	1.5	2.0	
Matching Constants	C_1	—	—	6	—	pF
	L_1	—	—	6	—	nH
	C_2	—	—	7	—	pF
	L_2	—	—	9	—	nF

Example 7. NTACS Specification (T_X)
Part Number F5CB-911M50-G201

T_a = –30 to 70°C

Parameter	Symbol	Condition	Specification			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	898-925 MHz	—	4.0	4.5	dB
In-band Ripple		898-925 MHz	—	1.5	2.0	dB
Absolute Out-of-Band Attenuation		DC-815 MHz	25	27	—	dB
		815-870 MHz	22	25	—	dB
		1008-1100 MHz	30	33	—	dB
		1100-3000 MHz	15	20	—	dB
In-band VSWR		898-925 MHz	—	1.8	2.0	
Matching Constants	C_1	—	—	6	—	pF
	L_1	—	—	7	—	nH
	C_2	—	—	5	—	pF
	L_2	—	—	10	—	nH

Continued on next page

ELECTRICAL CHARACTERISTICS – EXAMPLES (Continued)

Example 8. NTACS Specification (R_X)
Part Number F5CB-856M50-G201

T_a = –30 to 70°C

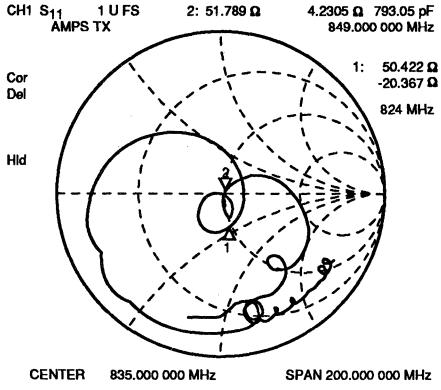
Parameter	Symbol	Condition	Specification			Unit
			Minimum	Typical	Maximum	
Insertion Loss	I_L	843-870 MHz	—	4.0	4.5	dB
In-band Ripple		843-870 MHz	—	1.5	2.0	dB
Absolute Out-of-Band Attenuation		DC-814 MHz	22	25	—	dB
		898-935 MHz	22	25	—	dB
		935-1100 MHz	30	33	—	dB
		1100-3000 MHz	15	20	—	dB
In-band VSWR		843-870 MHz	—	1.8	2.0	
Matching Constants	C_1	—	—	7	—	pF
	L_1	—	—	8	—	nH
	C_2	—	—	7	—	pF
	L_2	—	—	9	—	nH

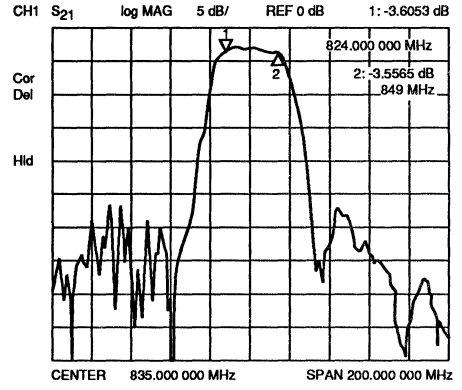
5

Below is an example of the AMPS-Tx filter input and output characteristics with compensating L&C components.

Input with L and C in 50 Ω environment

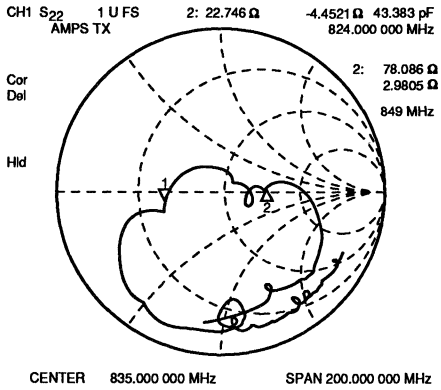
F5CB-836M50-G201

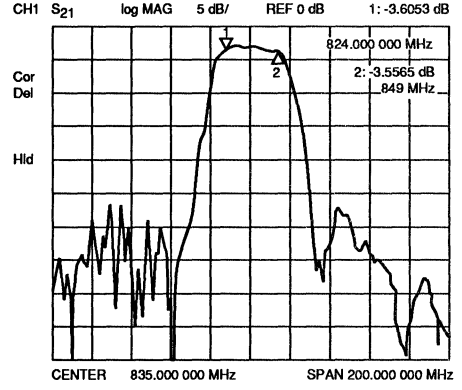




Output with L and C in 50 Ω environment

F5CB-836M50-G201





PART NUMBER DESIGNATION

Designation Example

F5CB – □□□□□□ – G□□□ – □
① ② ③

① Frequency Designation: Specifies the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to STANDARD FREQUENCIES. Example: For an 836.5 MHz device, the frequency designation would show "836M50."

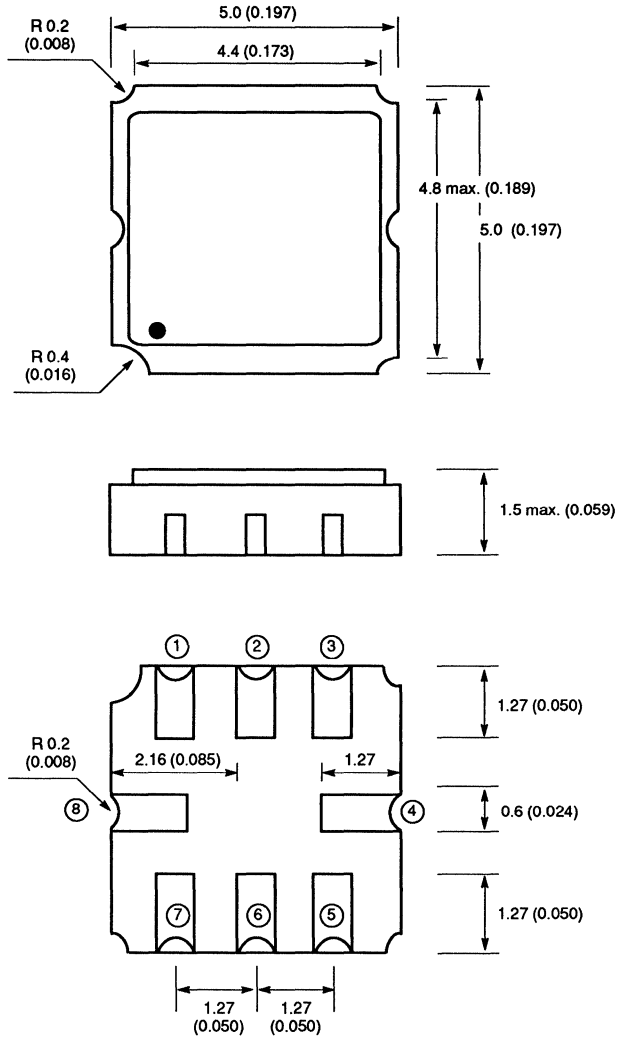
② Serial Number: Specifies a number from 201 to 299 (with 201 as the standard)

③ Packaging (Reeled tape)

Designation	Contents
T	1K pcs/reel
R	3K pcs/reel

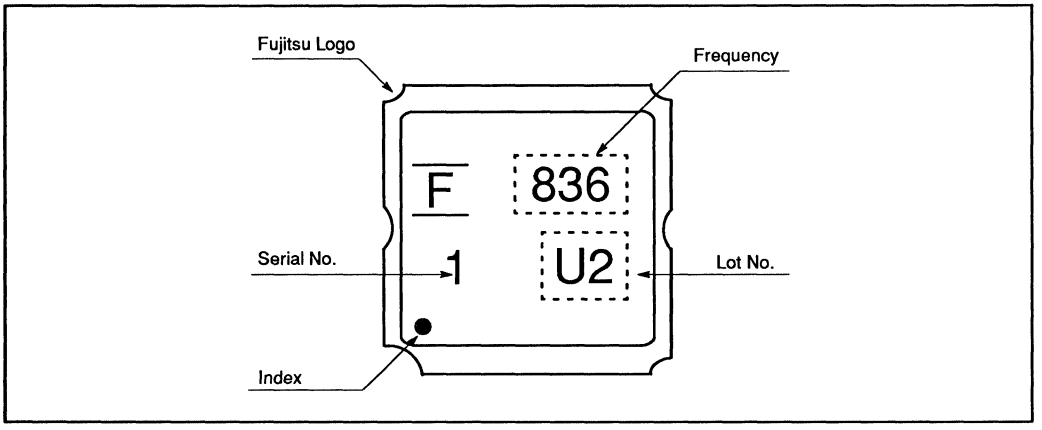
5

PACKAGE DIMENSIONS



Unit: mm (inches)

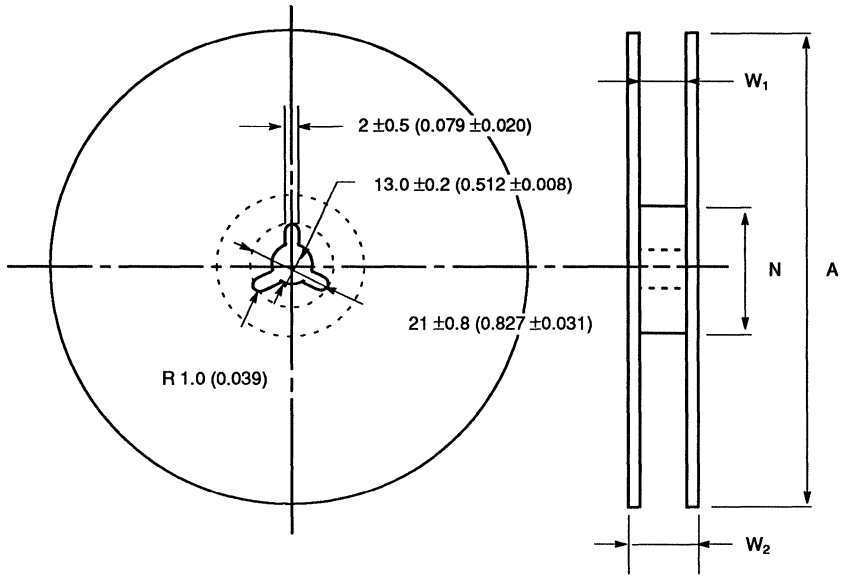
PACKAGE MARKING



PACKAGING: Reel Type

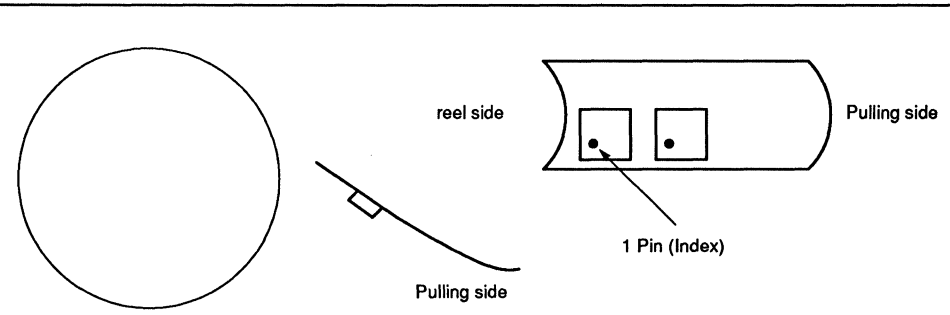
1. Reel Dimension

Unit: mm (inches)



Designation	A	N	W_1	W_2
–T	250 (9.843)	80 (3.150)	$12.4 \pm^{2.0}_{0.0}$ ($0.488 \pm^{0.079}_{0.00}$)	18.4 or less (0.724)
–R	330 (12.972)	80 (3.150)	$12.4 \pm^{2.0}_{0.0}$ ($0.488 \pm^{0.079}_{0.00}$)	18.4 or less (0.724)

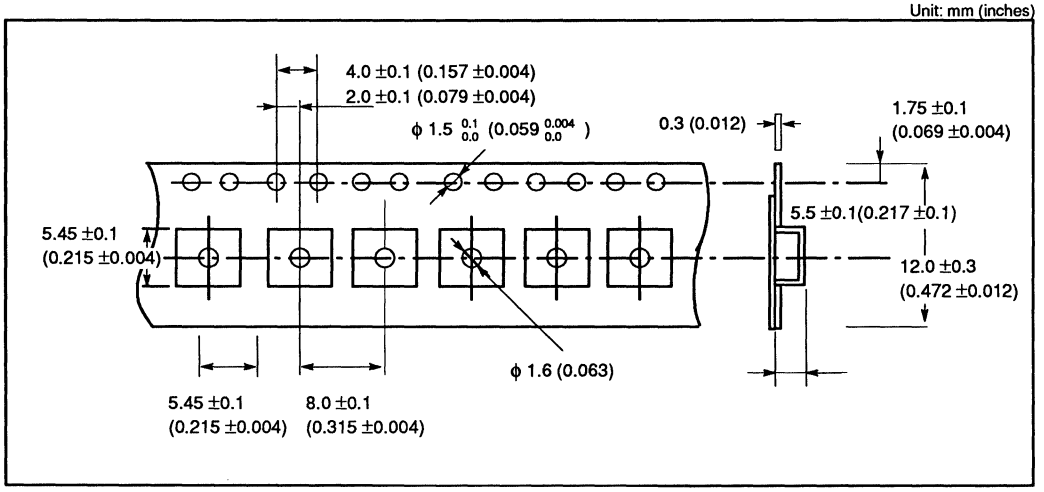
2. Package Style



PACKAGING: Reel Type (Continued)

3. Tape Dimension

Unit: mm (inches)



FUJITSU

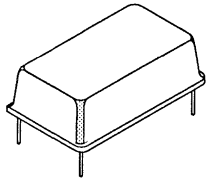
DATA SHEET

M2 Series (D100)
Piezoelectric Device (Voltage Controlled Oscillator)

The M2 series (D100) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz.

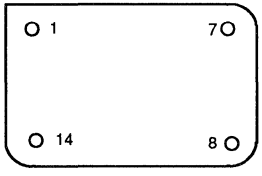
The M2 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient for stable and wide variable frequency width.

- Wider variable frequency width than quartz crystals: ±0.2% or more
- High stability (100 times more stable than LC configuration)
- Excellent carrier noise ratio
- Hermetically sealed in a metal case for high reliability in severe environmental conditions
- Compatible with 14-pin DIP IC packages



Metal Case
DIP-14

(Bottom View)



Terminal No.	Terminal Name	Description
1	V_{IN1}	Control Voltage Input Terminal
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
14	V_{CC}	Power Supply Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0	V
Input Control Voltage	V_{IN}	−0.5 to 10	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±25	mA
Operating Temperature	T_a	−30 to +85	°C
Storage Temperature	T_{STG}	−40 to +100	°C
Oscillation Frequency Range		4 to 30	MHz

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
Input Control Voltage	V_{IN}	0.5 to 5.0	V
Operating Temperature	T_a	−30 to +85	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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STANDARD FREQUENCIES

8.192 MHz	14.318 MHz	17.734 MHz	21.053 MHz	25.175 MHz
9.408 MHz	16.000 MHz	18.432 MHz	21.477 MHz	27.338 MHz
11.290 MHz	16.257 MHz	18.816 MHz	22.579 MHz	28.224 MHz
11.580 MHz	16.384 MHz	20.480 MHz	24.576 MHz	28.636 MHz
12.288 MHz	16.934 MHz			

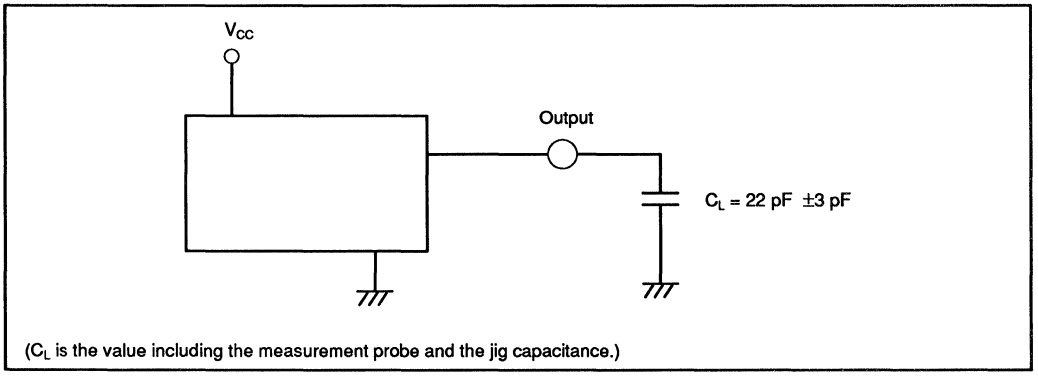
ELECTRICAL CHARACTERISTICS

DC Characteristics

Item	Symbol	Condition	Ratings		Unit
			Minimum	Maximum	
Output Level	V_{OUT}	See the measuring circuit diagram	0.5	—	V_{P-P}
Power Supply Current	I_{CC}	Load open	—	15	mA

5

Measuring Circuit Diagram



(C_L is the value including the measurement probe and the jig capacitance.)

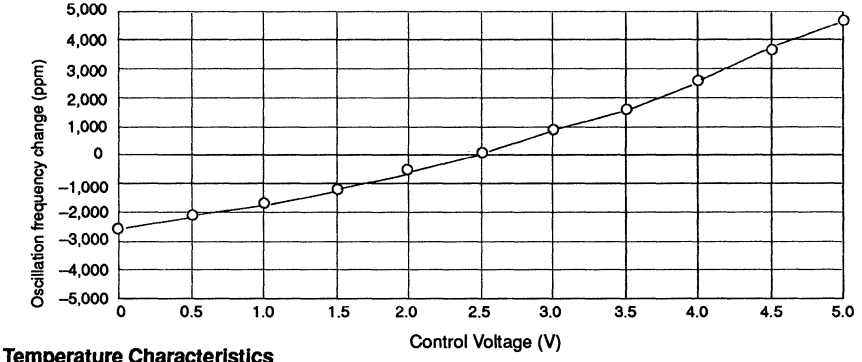
AC Characteristics

Item	Symbol	Condition	Ratings		Unit	Remarks
			Minimum	Maximum		
Oscillation Frequency	f_{OSC}	V_{IN} = 2.5 V	–0.05	+0.05	%	Nominal frequency reference V_{CC} = 5 V, T_a = 25°C
	f_H	V_{IN} = 4.5 V	+0.15	—	%	
	f_L	V_{IN} = 0.5 V	—	–0.15	%	
Frequency Voltage Stability	$\Delta f, V_{CC}$	V_{CC} = 4.75 V V_{CC} = 5.25 V	–200	200	ppm	5 V reference, V_{IN} = 2.5 V
Frequency Temperature Stability	$\Delta f, T_a$	V_{IN} = 0.5 V V_{IN} = 4.5 V	–500	500	ppm	25°C reference –10° to 70°C, T_A = 25°C

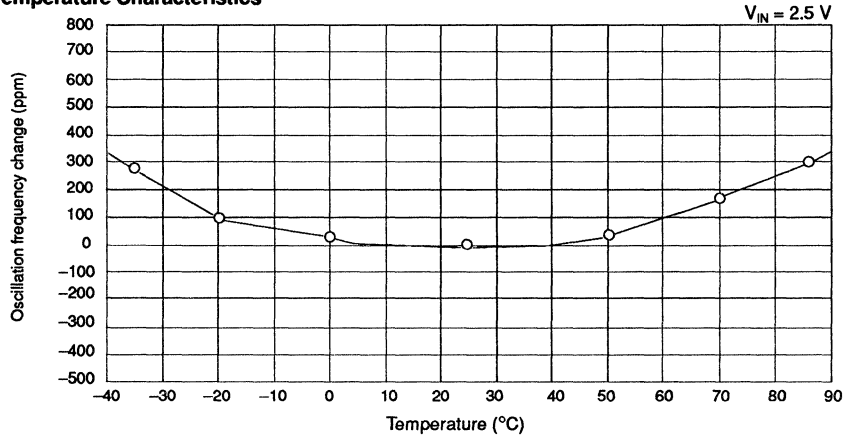
STANDARD CHARACTERISTICS:

Part Number: M2DA-8M1920-D100

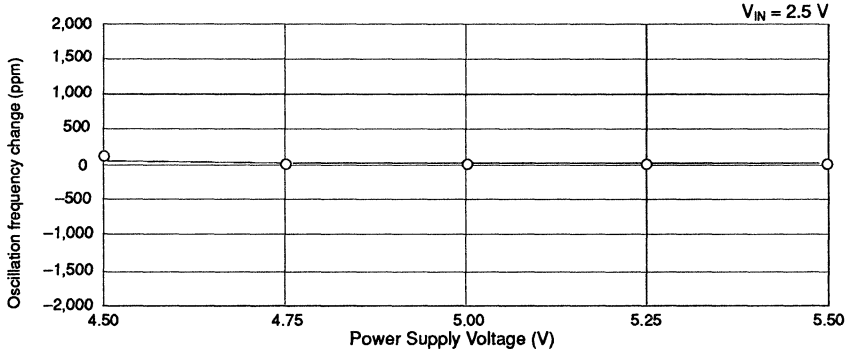
Control Voltage and Oscillation Frequency



Temperature Characteristics



Power Supply Voltage Characteristics



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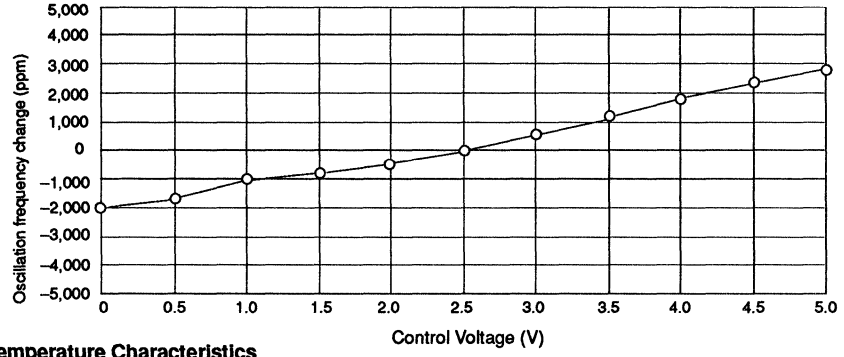
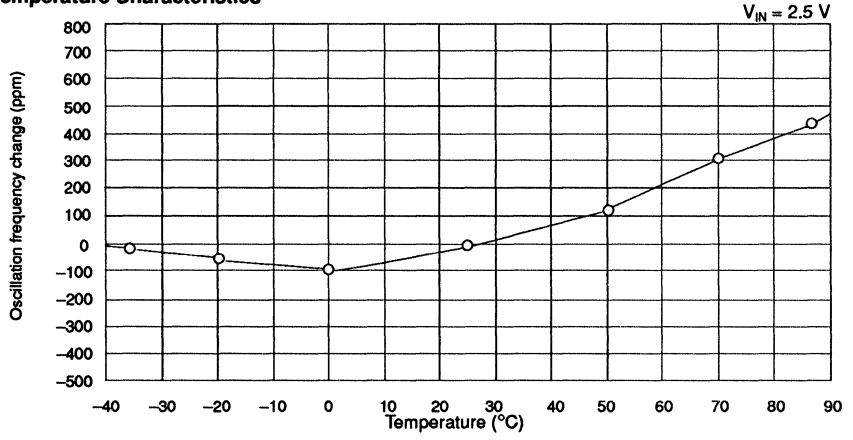
STANDARD CHARACTERISTICS:

Part Number: M2DA-12M288-D100

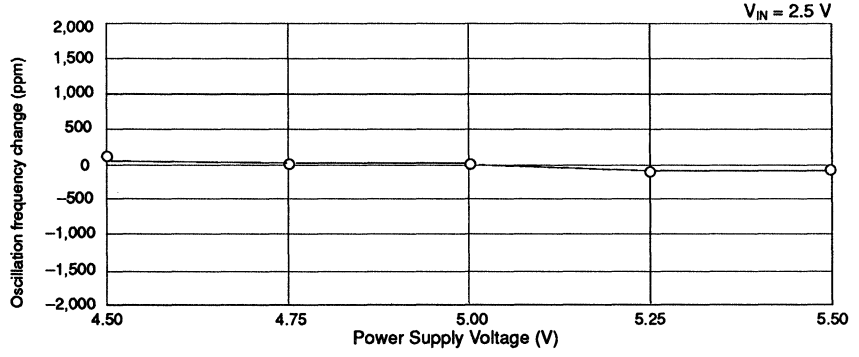
Control Voltage and Oscillation Frequency



Temperature Characteristics



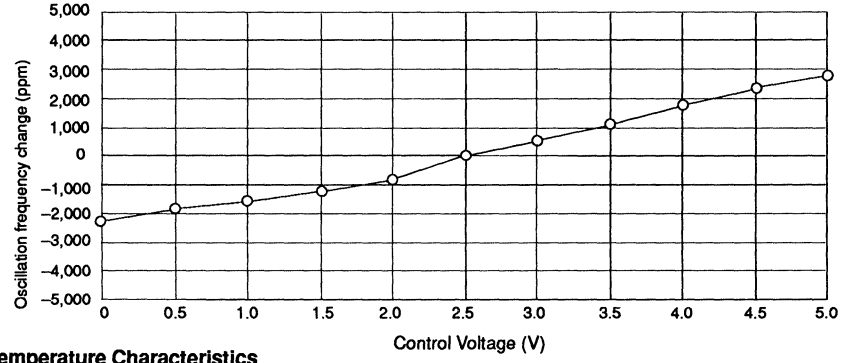
Power Supply Voltage Characteristics



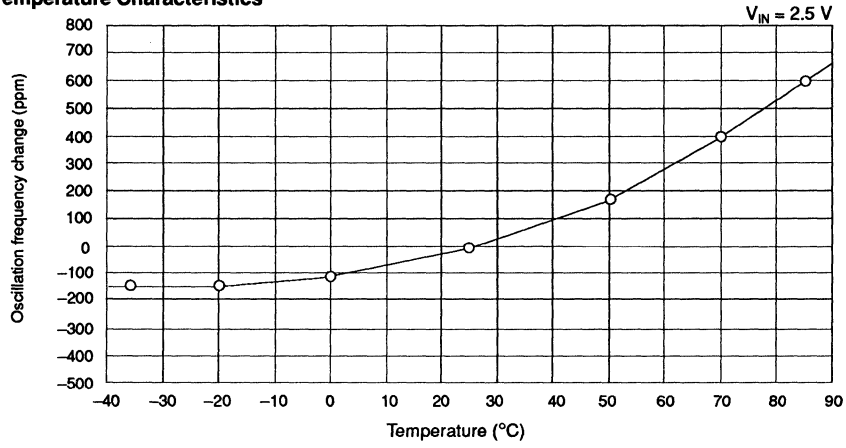
STANDARD CHARACTERISTICS:

Part Number: M2DA-28M636-D100

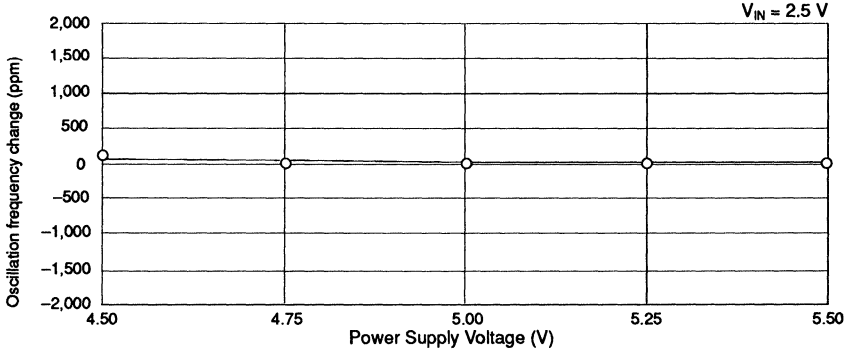
Control Voltage and Oscillation Frequency



Temperature Characteristics



Power Supply Voltage Characteristics



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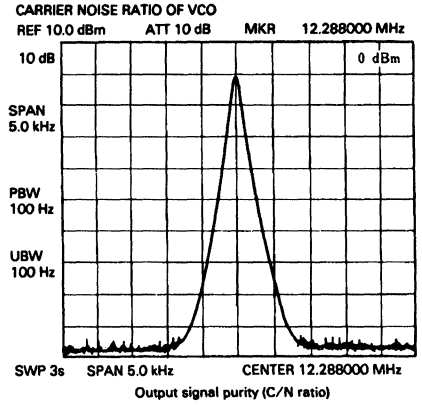
Oscillation Spectrum

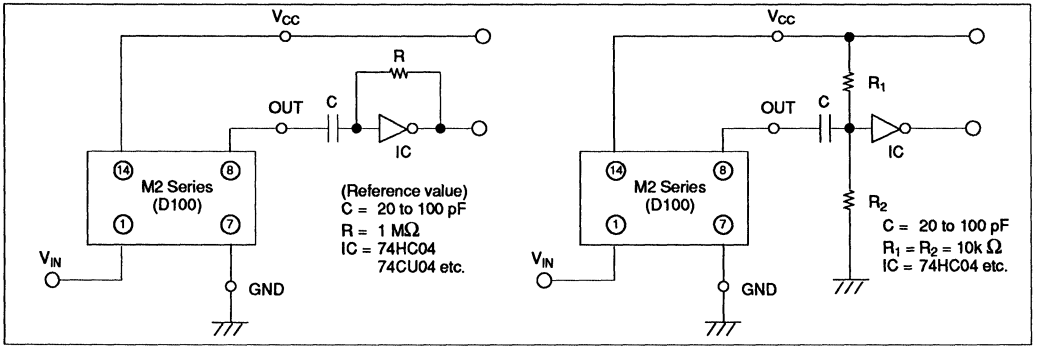


Output signal purity (C/N ratio)

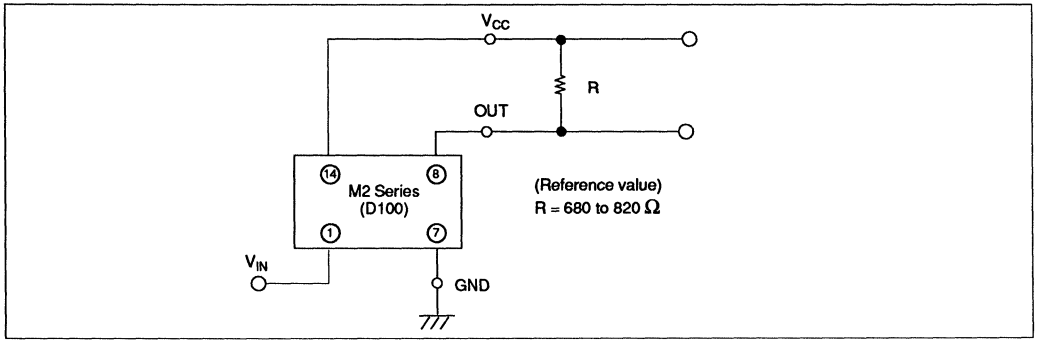
5

APPLICATION CIRCUIT EXAMPLES

Example 1. Connection to CMOS



Example 2. Connection to LS TTL (or CMOS)



PART NUMBERING SYSTEM

[Part Number Example]

M2DA-□□□□□□ -D□□□
① ②

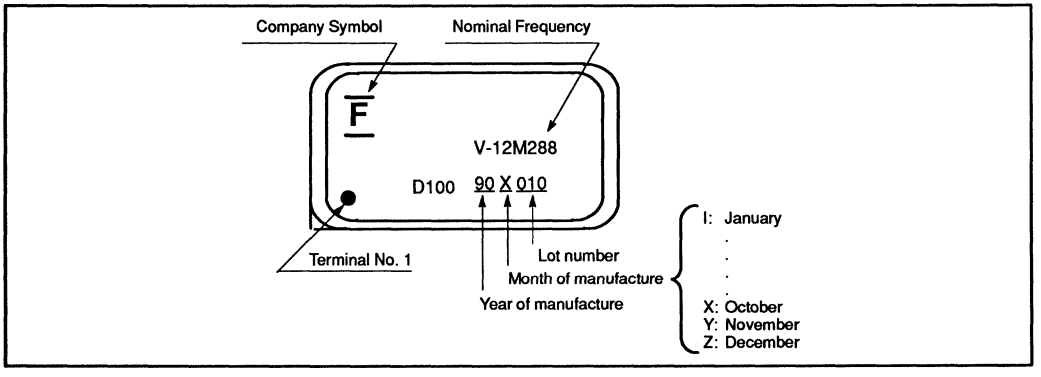
① Frequency designation: Designates the nominal frequency in six alphanumeric characters. M indicates the decimal point in MHz.

Frequency	Designation
8.192 MHz	8M1920
9.408 MHz	9M4080
11.290 MHz	11M290
11.580 MHz	11M580
12.288 MHz	12M288
14.318 MHz	14M318
16.000 MHz	16M000
16.257 MHz	16M257
16.384 MHz	16M384
16.934 MHz	16M934
17.734 MHz	17M734

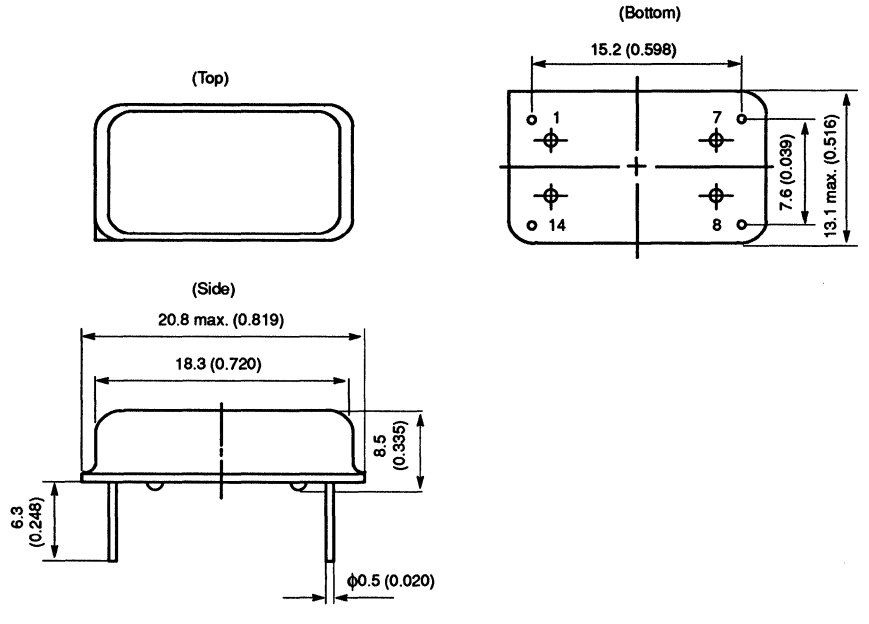
Frequency	Designation
18.432 MHz	18M432
18.816 MHz	18M816
20.480 MHz	20M480
21.053 MHz	21M053
21.477 MHz	21M477
22.579 MHz	22M579
24.576 MHz	24M576
25.175 MHz	25M175
27.338 MHz	27M338
28.224 MHz	28M224
28.636 MHz	28M636

② Serial Number (of the Series):
Standard: 100
Non-standard products: 001 to 099

MARKING



DIMENSIONS



Units: mm (in.)

5

FUJITSU

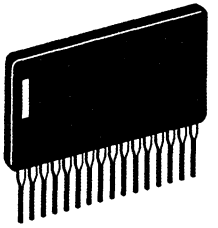
DATA SHEET

M2 Series (D300)
Piezoelectric Device (Voltage Controlled Oscillator)

The M2 series (D300) voltage controlled oscillators (VCO) operate in the frequency range of 4 to 30 MHz. The M2 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient for stable and wide variable frequency width.

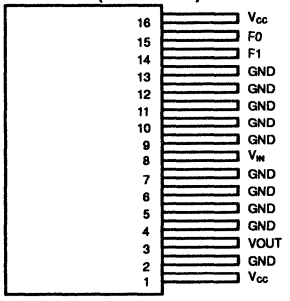
This module incorporates three VCOs for the three sampling frequencies used in digital audio equipment (32, 44.1, and 48 kHz). The frequencies are selected by external signals.

- Clock replay in response to three sampling frequencies (32, 44.1 and 48 kHz), is contained in one module
- Wider variable frequency width than in quartz crystals: ±0.1% or more
- Excellent stability for signal noise reproduced by high quality of the lithium tantalate
- 100 times more stable than VCOs of LC and TTL-IC configuration
- Three sampling frequencies controlled at CMOS logic level
- SIP packaged for high-density mounting of devices
- Compatible with the Electronic Industry Association of Japan (EIAJ) digital I/O Standard Type II (consumer digital audio equipment), Level I (high-resolution mode) and Level II (standard resolution mode)



Metal Case
SIP-16

(Front View)



Terminal No.	Terminal Name	Description
1, 16	V_{CC}	Power Supply Terminal
3	V_{OUT}	Output Terminal
8	V_{IN}	Control Voltage Intput Terminal
2, 4, 5, 6, 7, 9, 10, 11, 12,13	GND	Grounding Terminal[1]
14	F1	Frequency Switching Terminal[2]
15	F0	Frequency Switching Terminal[2]

1 The GND terminal and the V_{CC} terminals are not connected inside the module. So be sure to route them on the PC board.

2 The F1 and F0 bits switch the oscillation frequencies. The F1 and F0 bits are equivalent to bits 25 and 24 of the EIAJ Digital I/O Standard.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	−0.5 to 7.0	V
Input Control Voltage	V_{IN}	−0.5 to 10	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	±25	mA
Operating Temperature	T_a	−30 to +85	°C
Storage Temperature	T_{STG}	−40 to +100	°C

Negative value of current means that the current flows from the device.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
Input Control Voltage	V_{IN}	0.5 to 5.0	V
Operating Temperature	T_a	−20 to +70	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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5

STANDARD COMBINATION OF FREQUENCIES

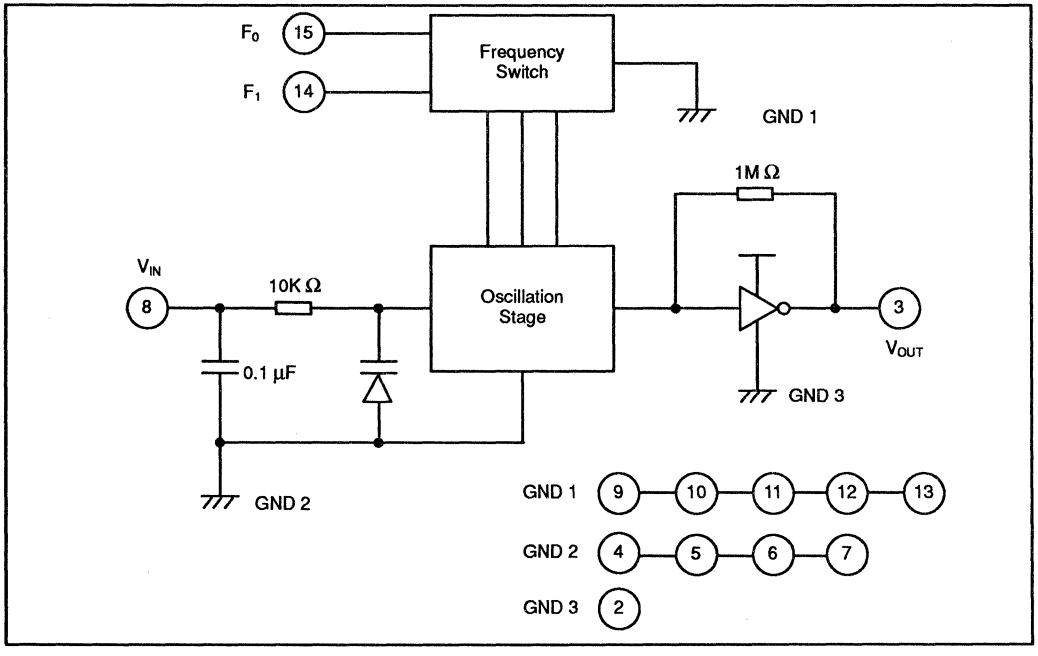
Type A (n = 256)	f_{01} (L)	8.192 MHz	32 kHz x 256
	f_{02} (M)	11.290 MHz	44.1 kHz x 256
	f_{03} (H)	12.288 MHz	48 kHz x 256
Type B (n = 384)	f_{01} (L)	12.288 MHz	32 kHz x 384
	f_{02} (M)	16.934 MHz	44.1 kHz x 384
	f_{03} (H)	18.432 MHz	48 kHz x 384
Type C (n = 512)	f_{01} (L)	16.384 MHz	32 kHz x 512
	f_{02} (M)	22.579 MHz	44.1 kHz x 512
	f_{03} (H)	24.576 MHz	48 kHz x 512

SWITCHING BIT DESIGNATION

F1	F0	Oscillation Frequency
H	H	f_{01} (L): 32 kHz x n
L	L	f_{02} (M): 44.1 kHz x n
H	L	f_{03} (H): 48 kHz x n
L	H	Stop

Note: n = 256, 384, 512

BLOCK DIAGRAM

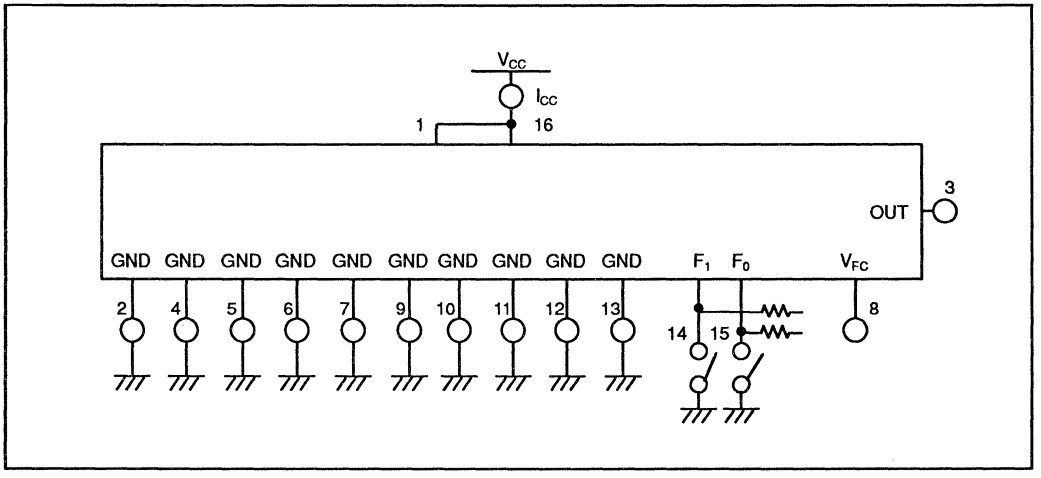


ELECTRICAL CHARACTERISTICS

DC Characteristics

Item		Symbol	Condition	Ratings			Unit
				Minimum	Normal	Maximum	
Output Voltage	H	V_{OH}	I_{OH} = –20 µA	V_{CC} –0.5	5.0	—	V
	L	V_{OL}	I_{OL} = 20 µA	—	0.0	0.5	V
Power Supply Current		I_{CC}	Not Loaded	—	4.6	15	mA

Measuring Circuit Diagram



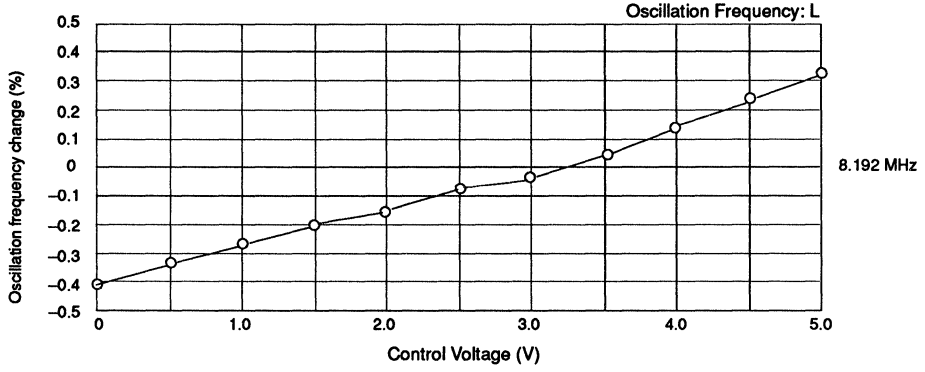
AC Characteristics

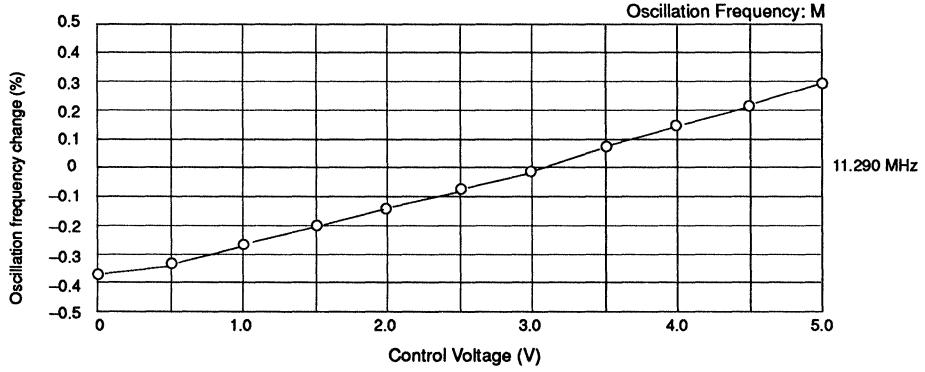
Item	Symbol	Condition	Ratings		Unit	Remarks
			Minimum	Maximum		
Oscillation Frequency One	f_{H1}	V_{IN} = 4.5 V	1.0015f_{01}	—	MHz	Nominal frequency F_0 reference
	f_{L1}	V_{IN} = 0.5 V	—	0.9985f_{01}	MHz	
Oscillation Frequency Two	f_{H2}	V_{IN} = 4.5 V	1.0015f_{02}	—	MHz	
	f_{L2}	V_{IN} = 0.5 V	—	0.9985f_{02}	MHz	
Oscillation Frequency Three	f_{H3}	V_{IN} = 4.5 V	1.0015f_{03}	—	MHz	
	f_{L3}	V_{IN} = 0.5 V	—	0.9985f_{03}	MHz	
Frequency Voltage Stability	Δf (V_{CC})	V_{CC} = 4.75 to 5.25 V	–100	100	ppm	5 V reference, V_{IN} = 0.5, 4.5 V
Frequency Temperature Stability	Δf (T_a)	T_a = –20 to +70°C	–500	500	ppm	25°C reference V_{IN} = 0.5, 4.5 V

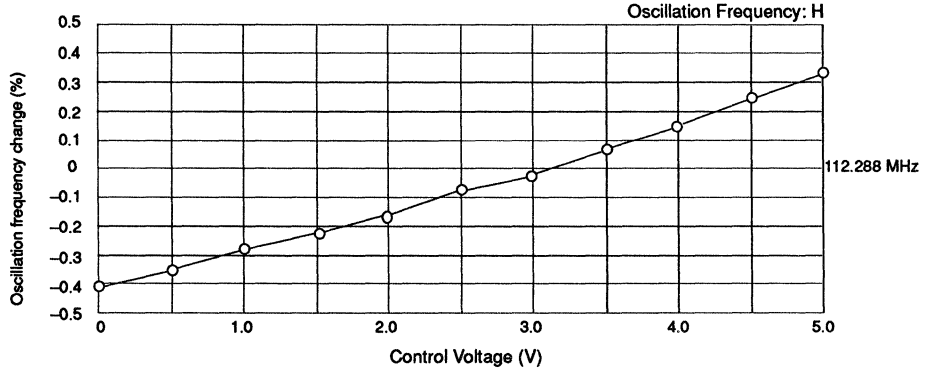
STANDARD CHARACTERISTICS

1A. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-12M288-D300



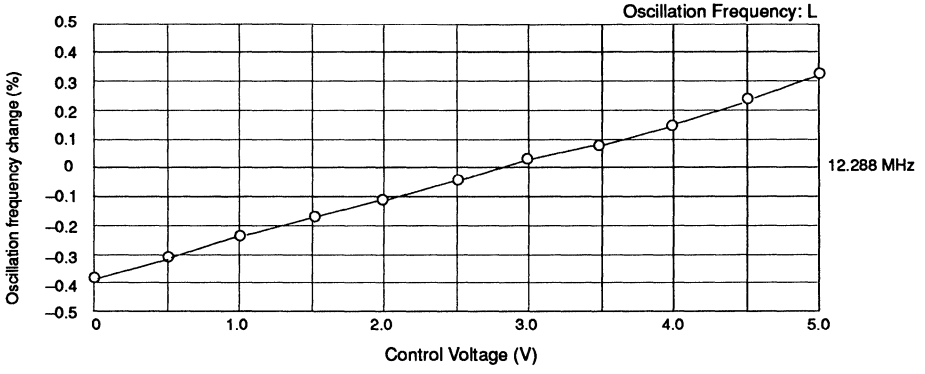


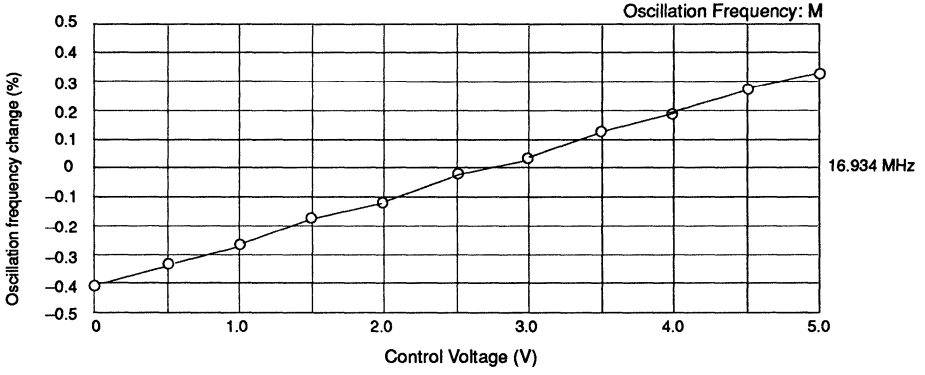


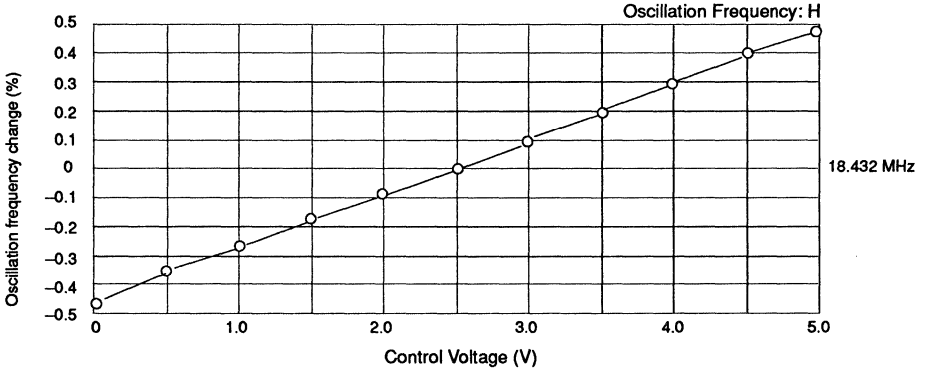
STANDARD CHARACTERISTICS

1B. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-18M432-D300







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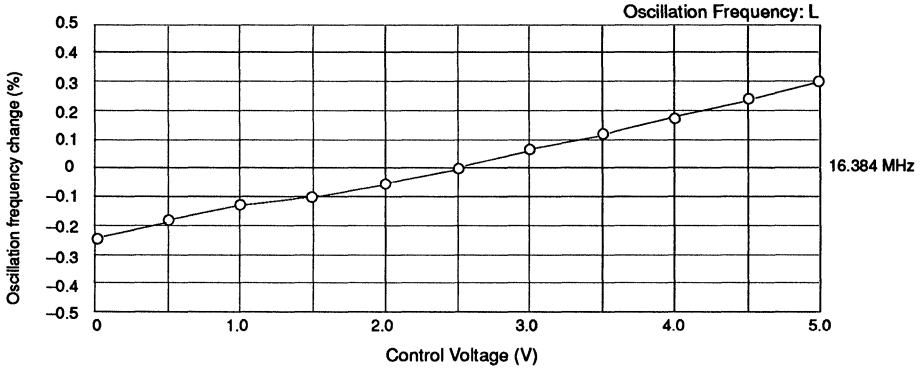
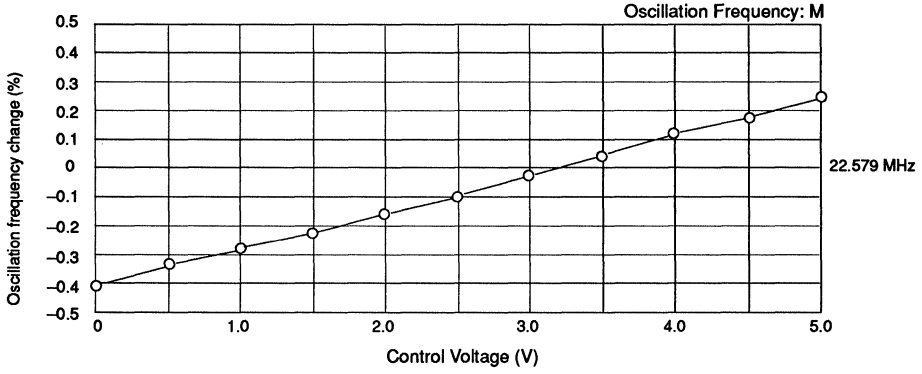
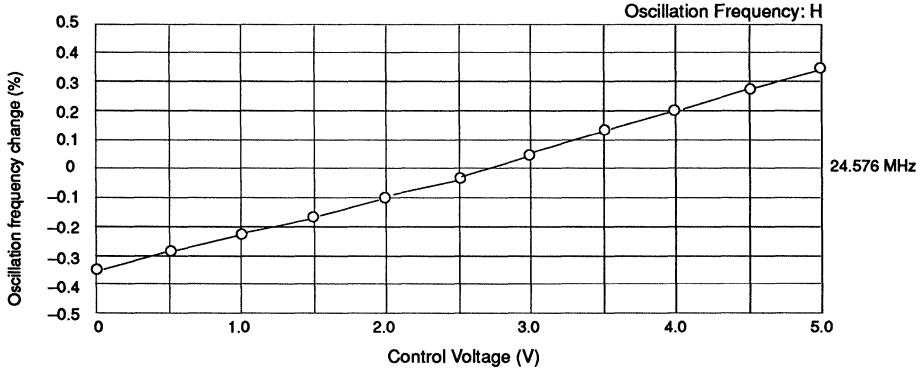
STANDARD CHARACTERISTICS

1C. Control Voltage and Oscillation Frequency Changes

Part Number: M2SC-24M576-D300

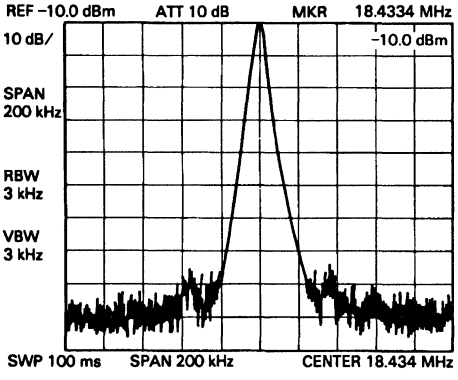


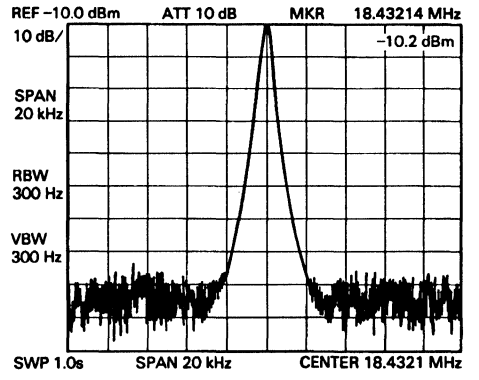




2. Oscillation Spectrum

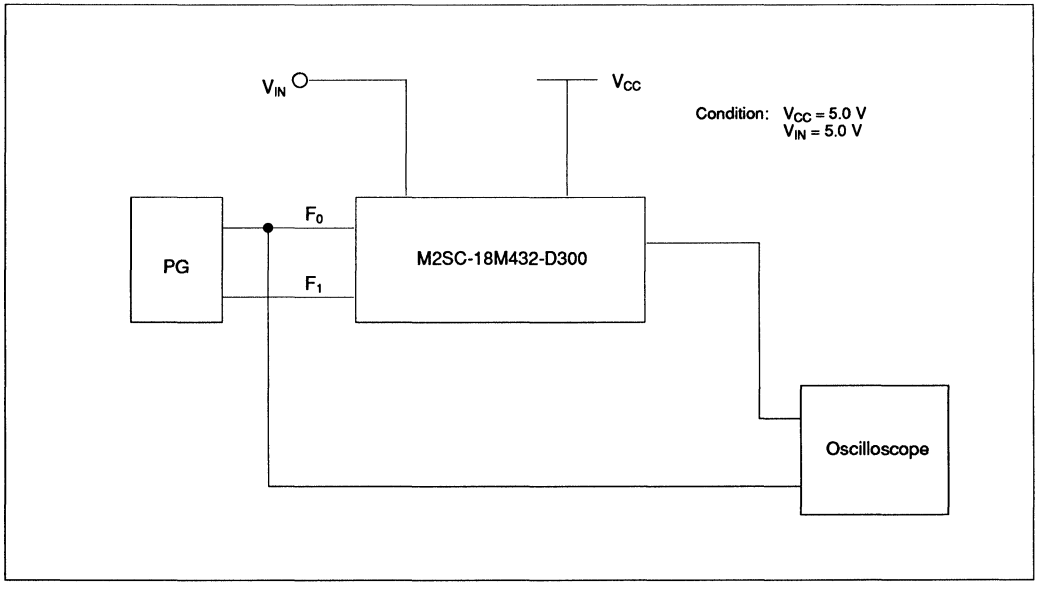
Part Number: M2SC-18M432-D300
Example of f_{03} = 18.432 MHz





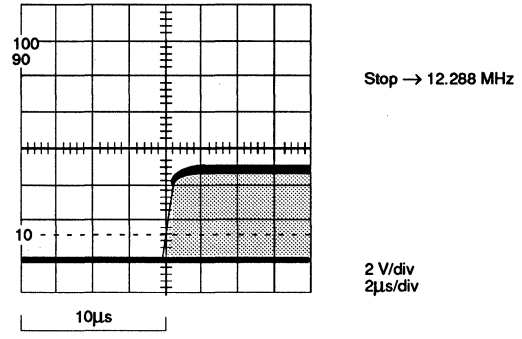
3. Frequency Switch Oscillation Startup Characteristics

The characteristics in the circuit below were measured with V_{CC} = 5.0 V and V_{FC} = 5.0 V.

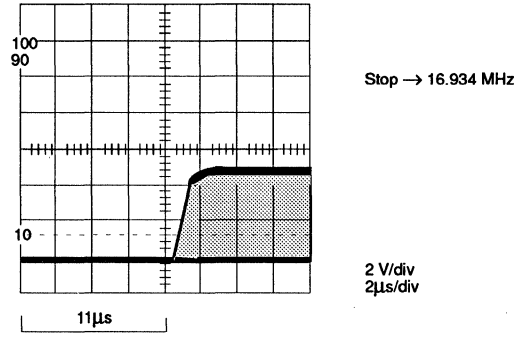


4. Frequency and Switching Oscillation Startup Characteristics

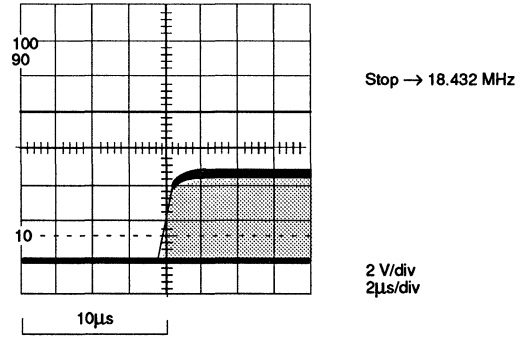
A. Condition: Stop → 12.288 MHz



B. Condition: Stop → 16.934 MHz



C. Condition: Stop → 18.432 MHz



PART NUMBERING SYSTEM

[Part Number Example]

M2SC-□□□□□□ - D □□□
① ②

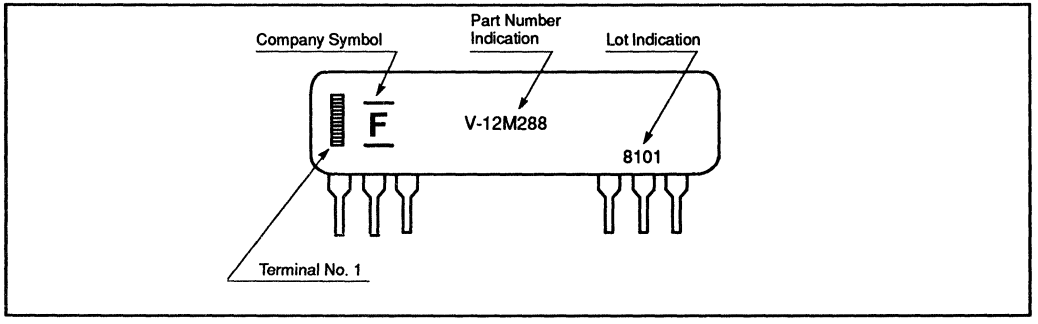
① Frequency designation: Designates the highest frequency of the combined nominal frequency types in six alphanumeric characters. M indicates the decimal point in MHz.

Frequency	Designation
(12.288 MHz)	Type A: 12M288
(18.432 MHz)	Type B: 18M432
(24.576 MHz)	Type C: 24M576

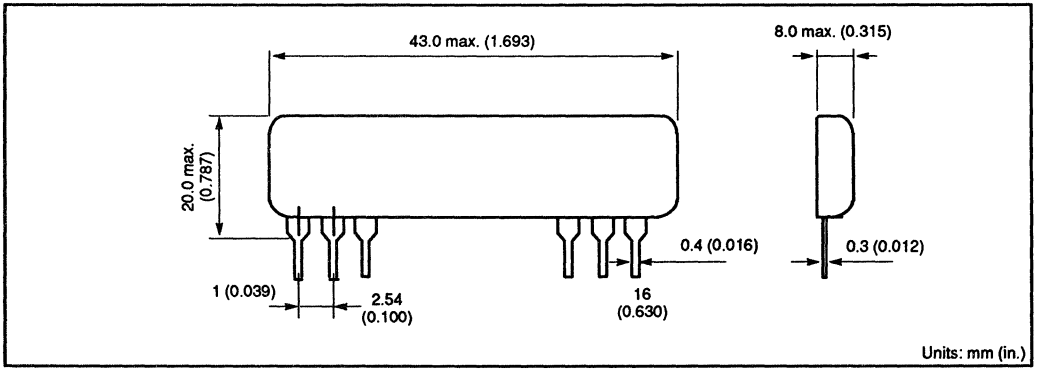
② Serial numbers of the series:
Standard for the M2 series (D300): D300

5

MARKING



DIMENSIONS



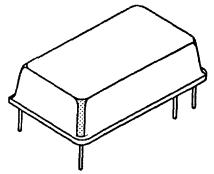
FUJITSU

DATA SHEET

M3 Series (D001)
Piezoelectric Device (Voltage Controlled Oscillator)

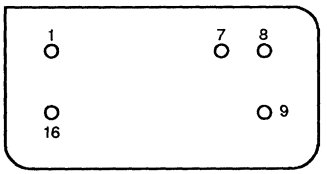
The M3 series voltage controlled oscillators (VCO) operate in the frequency range of 50 to 300 MHz. The M3 series VCOs use a single $LiTaO_3$ (lithium tantalate) piezoelectric crystal with a high electromechanical coupling coefficient and a SAW resonator that has an original configuration. The M3 series VCOs oscillate directly in the VHF band up to 300 MHz, and have a wide variable frequency width and high temperature stability.

- Direct oscillation at high frequencies: 50 to 300 MHz
- Wide variable frequency width: 800 ppm/V minimum (0.5 to 4.5 V)
- Superb temperature characteristics: Within ±200 ppm (0 to 60°C)
- High-precision oscillation frequency, ready for use without adjustment
- High reliability due to hermetically sealed package
- High carrier noise ratio: –90 dB or less (12.5 kHz detuning, 8 kHz band)
- Compact size: Compatible with 16-pin DIP IC packages
- Frequency offset by built-in offset terminal
- Three types of standard frequencies available



Metal Case
DIP-16

(Bottom View)



Terminal No.	Terminal Name	Description
1	V_{IN1}	Offset Terminal
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
9	V_{CC}	Power Supply Terminal
16	V_{IN2}	Control Voltage Input Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
Input Control Voltage	V_{IN2}	–0.5 to 7.0	V
Operating Temperature	T_a	0 to 60	°C
Storage Temperature	T_{STG}	–40 to 85	°C
Control Polarity		Positive Polarity	
Oscillation Frequency Range		50 to 300	MHz

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	5.0	V
Input Control Voltage	V_{IN2}	0.5 to 4.5	V
Operating Temperature	T_a	0 to 60	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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5

STANDARD FREQUENCIES

Frequency	Application	Part Number
74.25 MHz	Professional HDTV	M3DA-74M250-D001
97.2 MHz	Transmission Standard HDTV	M3DA-97M200-D001
115.52 MHz	Broad-band ISDN	M3DA-155M52-D001

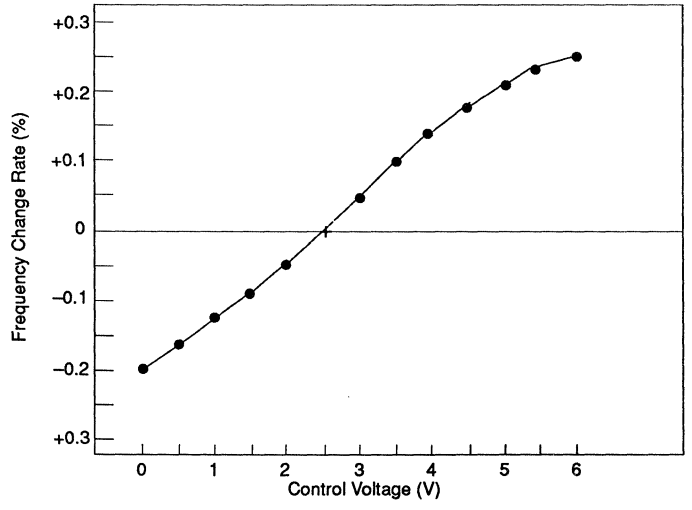
ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Ratings			Unit	Remarks
			Minimum	Typical	Maximum		
Oscillation Frequency Deviation	Δf_o	V_{IN2} = 2.5 V	–500	—	+500	ppm	f_o reference
Variable Width of Oscillation Frequency	$\frac{(f_H - f_L)}{f_o}$	V_{IN2} = 0.5 V V_{IN2} = 4.5 V	800	—	—	ppm/V	
Temperature Stability of Oscillation Frequency	Δf (T_a)	V_{IN2} = 2.5 V	–200	—	+200	ppm	25°C reference, T_a = 0 to 60°C
Output Level	P_{OUT}	V_{IN2} = 2.5 V	0	5	7	dBm	50 Ω termination
Output Level Stability	ΔP (V_F)	V_{IN2} = 0.5 V V_{IN2} = 4.5 V	–2	—	+2	dB	V_{IN2} = 2.5 V reference
Output Level Temperature Stability	ΔP (T_a)	V_{IN2} = 2.5 V	–2	—	+2	dB	25°C reference, T_a = 0 to 60°C
Current Consumption	I_{CC}	—	—	—	30	mA	
Oscillation Frequency Power Supply Voltage Fluctuation	Δf (V_{CC})	V_{IN2} = 2.5 V	–50	—	+50	ppm	V_{CC} = 5 V reference, ±5%

STANDARD CHARACTERISTICS

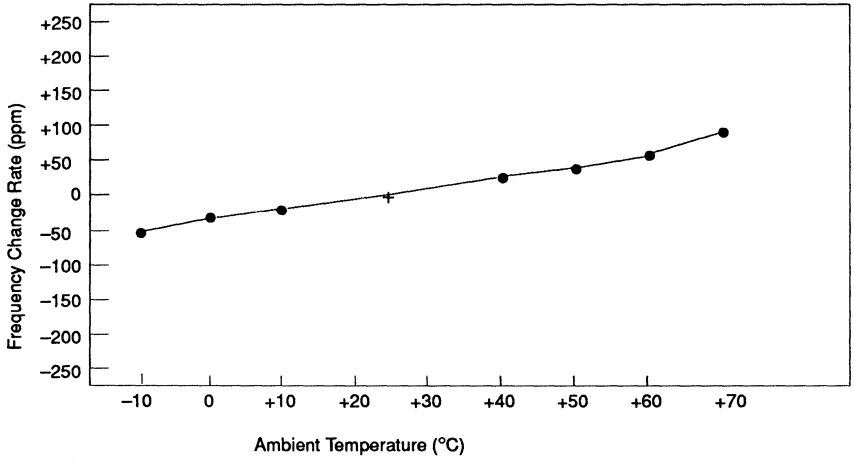
The examples below show characteristics of the M3 VCO devices at 155.52 MHz.

Example 1. Frequency Variable Characteristics

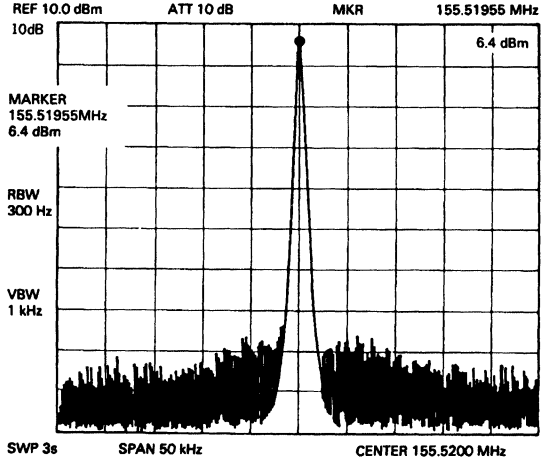


STANDARD CHARACTERISTICS (Continued)

Example 2. Temperature Characteristics



Example 3. Oscillation Spectrum



PART NUMBERING SYSTEM

(Part Number Example)

M3DA-□□□□□□ -D □□□
① ②

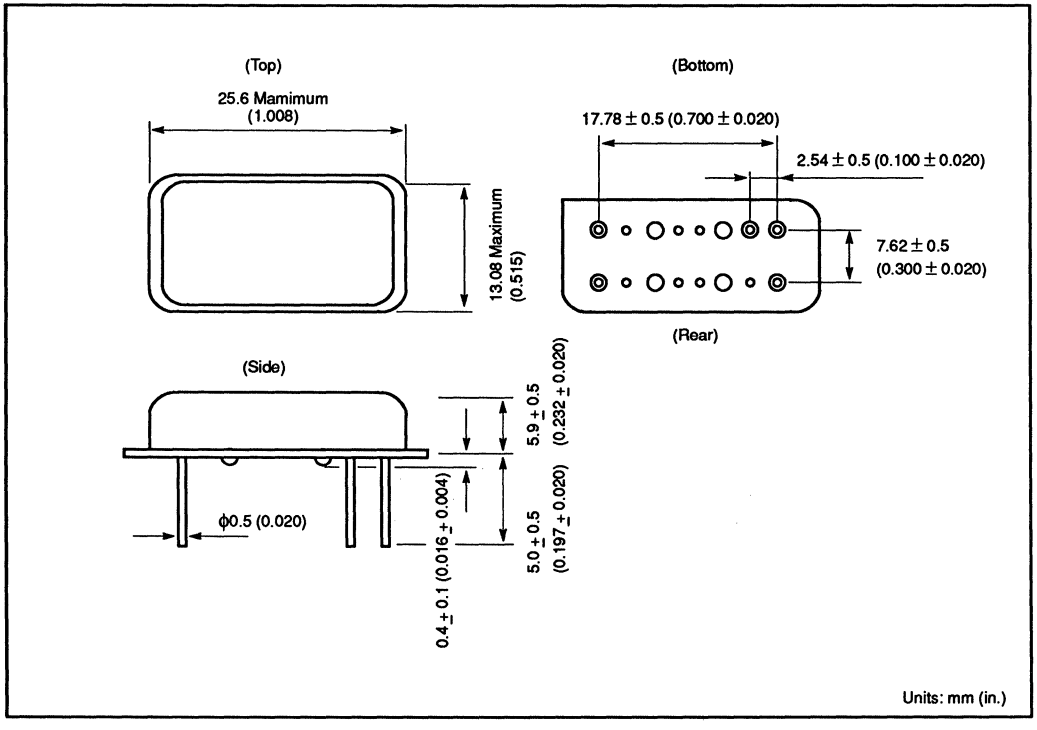
① Frequency designation: Designates the nominal frequency in six alphanumeric characters. M indicates the decimal point in MHz.

Frequency	Designation
74.25 MHz	74M250
97.2 MHz	97M200
115.52 MHz	115M52

5

② Serial Number (of the series):
Standard: 001
Non-standard products: 001 to 099

PACKAGE DIMENSIONS



FUJITSU

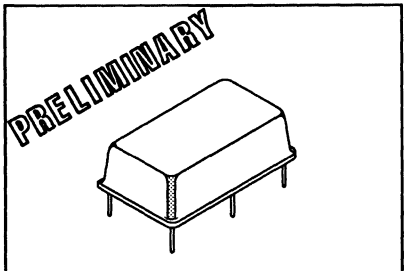
DATA SHEET

M3 Series (D101)
Piezoelectric Device

Modulator, 50 MHz to 300 MHz

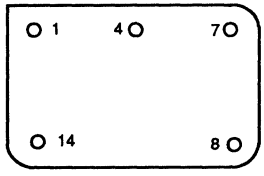
These piezoelectric modulators feature direct oscillators (50 MHz to 300 MHz). The piezoelectric modulator uses a lithium tantalate piezoelectric single crystal ($LiTaO_3$) with a high electromechanical coupling coefficient. The piezoelectric modulator employs an exclusive SAW resonator. The piezoelectric modulator can be used in direct modulation applications needing high modulation sensitivity and a high signal-to-noise ratio in the VHF band (up to 300 MHz).

- High frequency direct modulation: 50 to 300 MHz
- High modulation sensitivity: 800 ppm/V min. (0.5 to 4.5 V)
- Excellent modulation distortion ratio: 40 dB max. (1 kHz to 1.75 kHz dev.)
- Excellent signal noise ratio: –50 dB max.
- Excellent temperature characteristic: ±200 ppm max. (–20 to 70°)
- Highly reliable hermetically sealed package
- Compatible with 14-pin DIP IC packages



Metal Case
DIP-14

(Bottom View)



Terminal No.	Terminal Name	Description
1	ML	Control Voltage Input Terminal
4	MM	Modulation Input
7	GND	Grounding Terminal
8	V_{OUT}	Oscillation Output Terminal
14	V_{CC}	Power Supply Terminal

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	–0.5 to 7.0	V
ML Pin Input Voltage	V_{ML}	–0.5 to 10	V
MM Pin Input Voltage	V_{MM}	–0.5 to 7.0	V
ML Pin Modulation Polarity		Positive	
MM Pin Modulation Polarity		Negative	
Operating Temperature	T_a	–20 to +85	°C
Storage Temperature	T_{STG}	–40 to +100	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
ML Pin Input Voltage	V_{ML}	2.5	V
Operating Temperature	T_a	–20 to 70	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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STANDARD FREQUENCY

Standard Frequency	Application	Part Number
145.0 MHz	Mobile Phone	M3DA-145M00-D101

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V)

Item		Symbol	Condition	Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Remarks
Oscillation Frequency Deviation		Δf_o	V_{ML} = 2.5 V	–300	—	+300	ppm	f_o reference
Variable Width of Oscillation Frequency		$\frac{(f_H - f_L)}{f_o}$	V_{ML} = 0.5 V V_{ML} = 4.5 V	800	—	—	ppm/V	
Temperature Stability of Oscillation Frequency		$\Delta f (T_a)$	V_{ML} = 2.5 V	–200	—	+200	ppm	25°C reference, T_a = –20 to 70°C
Output Level		P_{OUT}	V_{ML} = 2.5 V	–5	–3	–1	dBm	50 Ω termination
Output Level Stability		$\Delta P (V_F)$	V_{ML} = 0.5 V V_{ML} = 4.5 V	–2	—	+2	dB	V_{ML} = 2.5 V reference
Output Level Temperature Stability		$\Delta P (T_a)$	V_{ML} = 2.5 V	–2	—	+2	dB	25°C reference, T_a = –20 to 70°C
Current Consumption		I_{CC}	—	—	—	10	mA	
Oscillation Frequency Power Supply Voltage Fluctuation		$\Delta f (V_{CC})$	V_{ML} = 2.5 V	–50	—	+50	ppm	±5% at V_{CC} = 5 V reference
Modulation Characteristic	Modulation Distortion (1 KHz tone)		1.75 kHz DEV	—	—	–40	dB	15 kHz LPF
			3.5 kHz DEV	—	—	–40	dB	
			5.0 kHz DEV	—	—	–40	dB	
	Signal to Noise Ratio		1.75 kHz DEV	—	—	–50	dB	300 to 3 kHz
	Modulator Input Impedance			10			KΩ	

PART NUMBERING SYSTEM

Designation Example

M3DA - □□□□□□ – D□□□

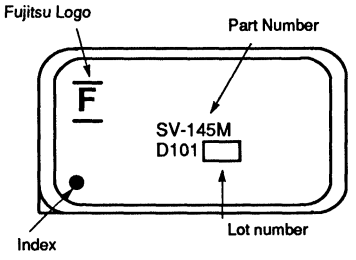
① ②

① Frequency Designation: The standard frequency is designated in six alphanumeric characters. M is used to designate the decimal point in MHz. Refer to STANDARD FREQUENCY. Example: 145.0 MHz device is designated as 145M00.

② Serial Number: The serial number is assigned from 101 to 199 (with 101 as the standard).

PACKAGE MARKING

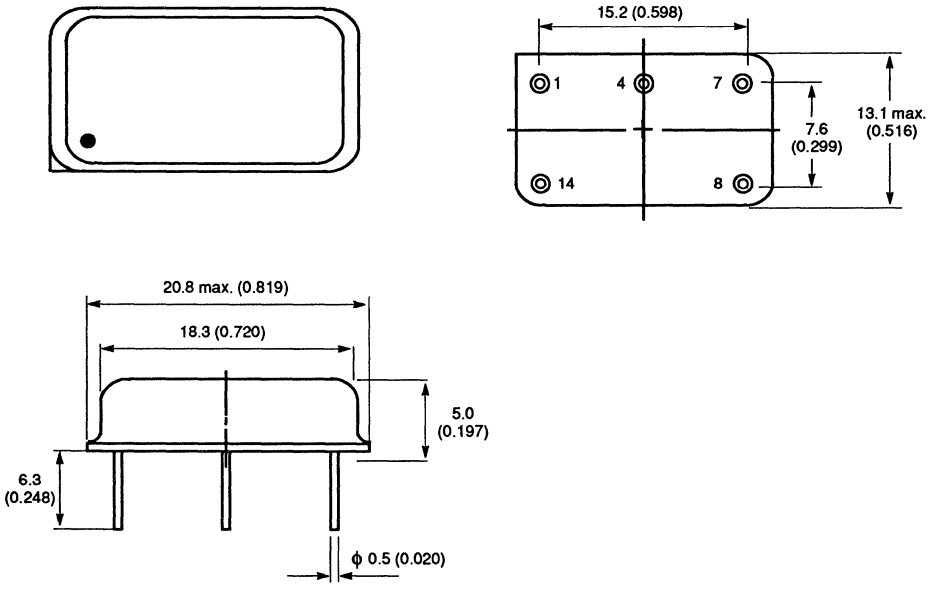
(Bottom View)



5

PACKAGE DIMENSIONS

Units: mm (in.)



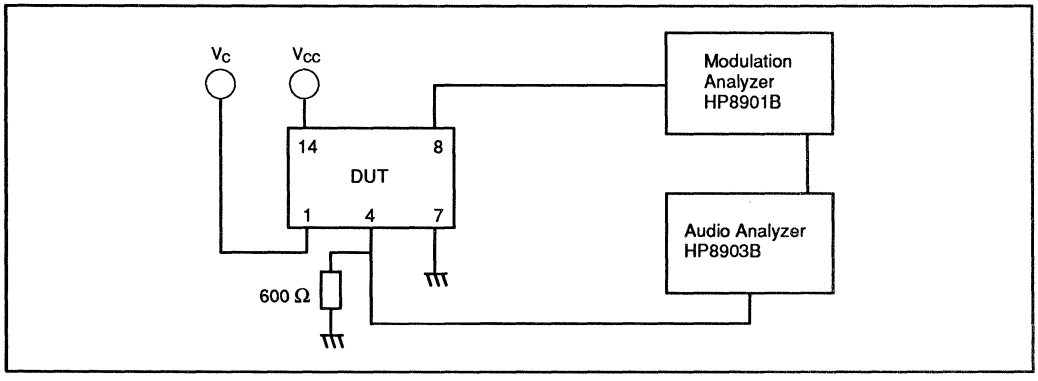
SAW MODULATOR CHARACTERISTICS

M3DA-145M00-D101

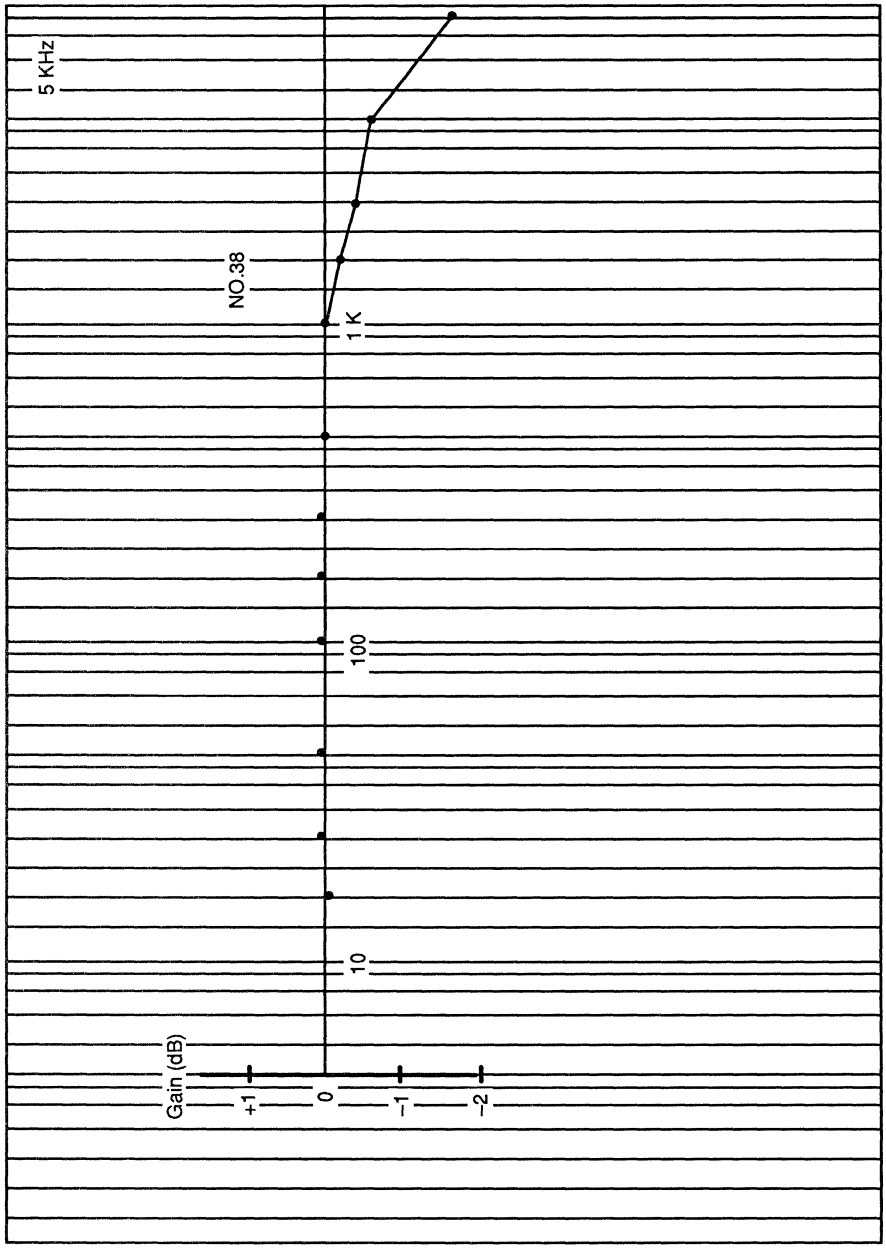
Item		Rating	Characteristics	Remarks
Output Frequency		145.0 MHz	144.997 MHz	V_C = 2.5 V
Current Consumption		10 mA or less (with buffer)	7.3 mA	
Output Level		–3 dBm ±2 dB	–2.00 dBm	V_C = 2.5 V
Spurious Response Ratio		Higher harmonic < 4 dB at 2 f_0 (290 MHz)	–7.3 dB	
Frequency Stability	Power Supply Fluctuation	Within ±50 ppm for 5 V ±0.25 V	+6.00 ppm –5.80 ppm	
	AFC-F-F Characteristic	±550 ppm or more for 2.5 V ±1 V	–789 ppm +1016 ppm	
	Temperature Characteristic	Within ±300 ppm for –35 to +85	+66 ppm +41 ppm	
AFC Voltage Versus Output Frequency Characteristics		At 25 ±5°C, the AFC voltage for the output frequency of 145 MHz is V_C = 2.5 V ±0.3 V	2.501 V	
		At –20 +85°C, the AFC voltage for the output frequency of 145 MHz is V_C = 2.5 V ±0.3 V	2.476 V 2.459 V	–20°C +85°C
Modulation Characteristic	Modulation Input Level	–28 dBm ±3 dB (600 W) 1 KHz ±3.5 kHz DEV*	–26.1 dB	15 kHz LPF
	Modulation Distortion Ratio	–35 dB or less 1 kHz (±1.75 kHz DEV)* –30 dB or less 1 kHz (±3.5 kHz DEV)* –20 dB or less 1 kHz (±5.0 kHz DEV)*	–46 dB –49 dB –48 dB	15 kHz LPF
	Modulation Characteristic	< ±1 dB/20 Hz to 5 kHz ±5 kHz DEV*		
	Signal Noise Characteristic	< –50 dB ±1.75 kHz DEV*	–55 dB	300 to 3 kHz

*Adjust the control voltage for an oscillation frequency of 145 MHz for the modulation characteristic.

Test Circuit

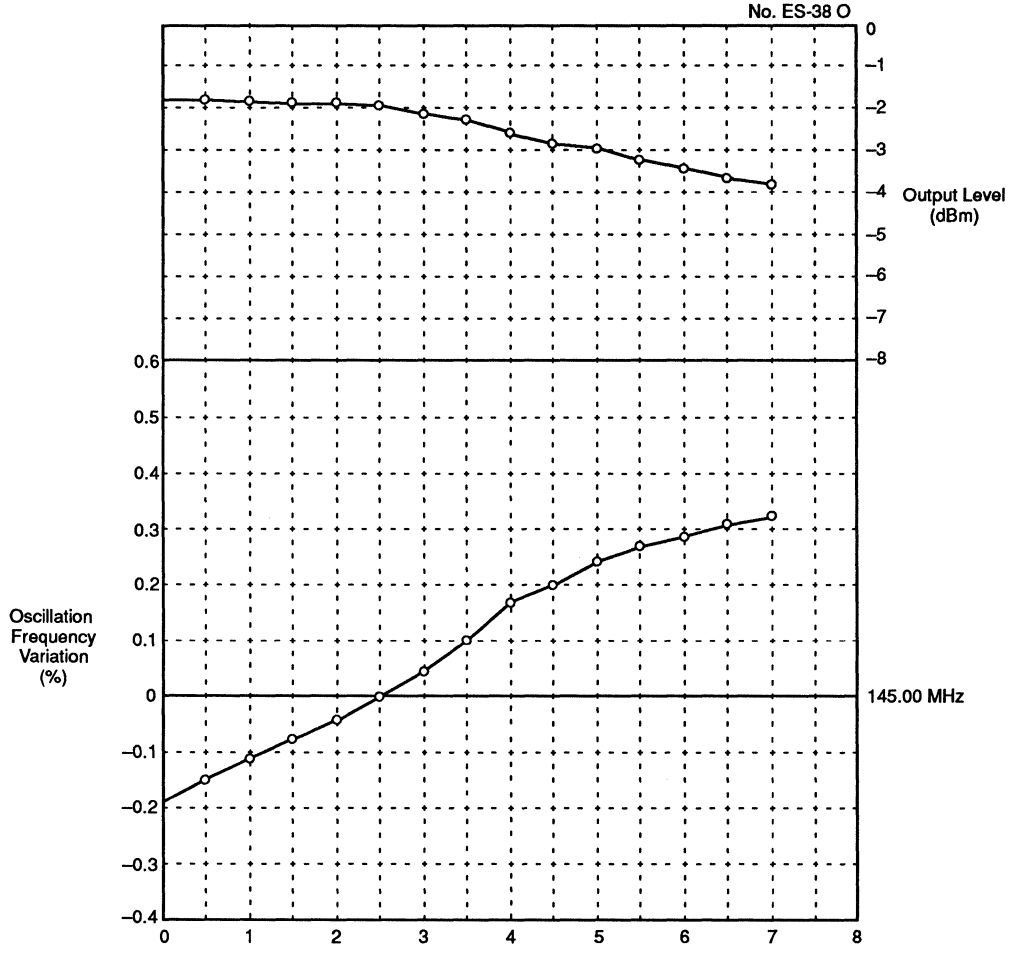


M30A-145M00-D101 MODULATION FREQUENCY CHARACTERISTICS



SAW MODULATOR CHARACTERISTIC DATA

M3DA-145M00-D101

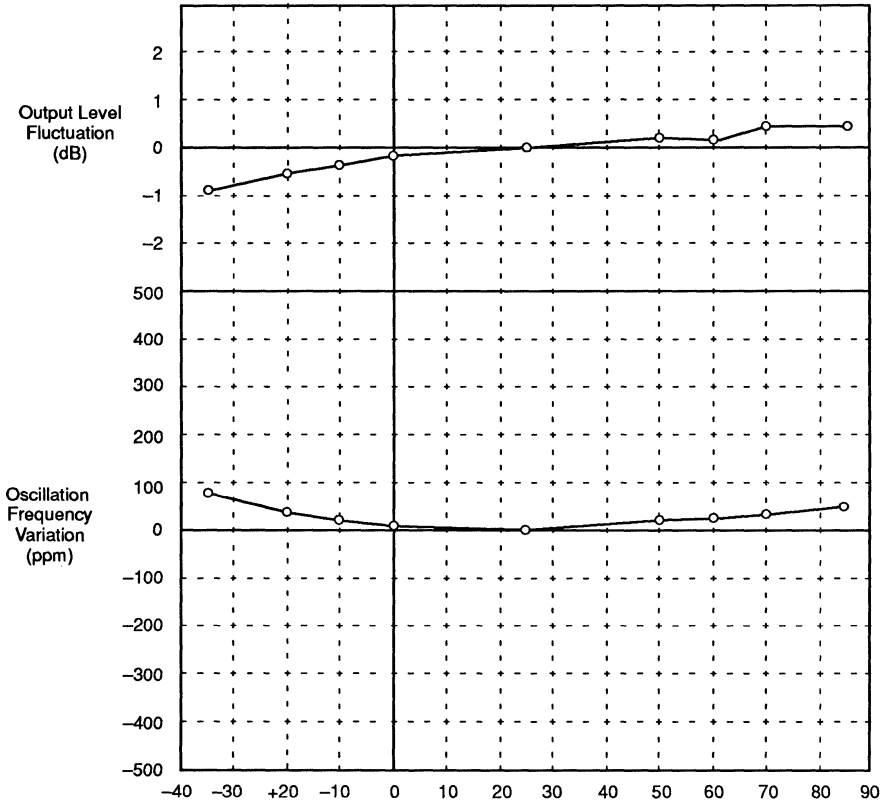


V–F Characteristic

SAW MODULATOR CHARACTERISTIC DATA (Continued)

M3DA-145M00-D101

No. ES-38 O



Section 6

Cordless Telephone Integrated Circuits — *At a Glance*

Page	Device	Description	Package Options		
6–3	MB86460A	Modem with Internal Voice-Band Filters	48-pin	Plastic	FPT
6–25	MB87002	CMOS 1200 bps MSK Modem	16-pin	Plastic	DIP, FPT

May 1991
Edition 1.0

FUJITSU

DATA SHEET

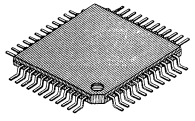
MB86460A

MODEM WITH INTERNAL VOICE-BAND FILTERS

CMOS MODEM CIRCUIT WITH INTERNAL VOICE-BAND FILTERS FOR CORDLESS TELEPHONES

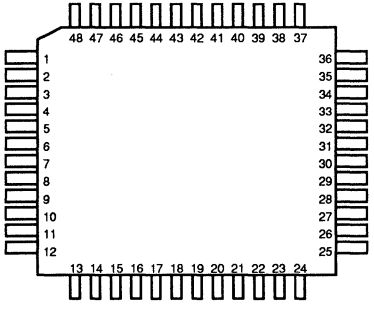
The MB86460 MSK (Minimum Shift Keying) modem IC contains a 1200-band MSK modem and voice-band filters.
The voice-band filter consists of transmit and receive bandpass filters, pre-emphasis/de-emphasis, and splatter filters arranged in an SCF configuration. In addition, a limiter circuit is included.
The MB86460 operates at low voltage (3.0 to 5.5 V) and is suitable for cordless telephone applications.

- On-chip voice-band filters and 1200-band MSK modem
- Low supply voltage requirements (3.0 to 5.5 V)
- Wide operating temperature range (T_A = –20°C to 70°C)
- Standby function for low power consumption
- MSK frame detection
- Frame synchronization selectable
- Full-duplex MSK modem
- Transmit/receive muting
- Externally adjustable receive and transmit gain
- Externally adjustable limiter level
- Carrier/interference detection circuit
- The on-chip oscillator operates with 3.6864 or 3.456 MHz crystal (selectable).
- The on-chip serial interface reduces the number of signal lines
- CMOS I/O interface



PLASTIC PACKAGE
(FPT-48P-M02)

PIN ASSIGNMENT
(TOP VIEW)



Pin No.	I/O	Pin name	Pin No.	I/O	Pin name	Pin No.	I/O	Pin name
1	O	EMP_{OUT}	17	O	CC_1	33	I	SD
2	I	CMP_{OUT}	18	I	CC_2	34	O	SCK
3	O	CMP_{IN}	19	–	V_{DDA}	35	I	SEND
4	O	AF_{IN2}	20	O	C_{OUT}	36	I	RST
5	I	AF_{IN1}	21	I	DET_{IN}	37	I	OSC_{IN}
6	O	1/2 V_{DDOUT}	22	O	DET_{OUT}	38	O	OSC_{OUT}
7	I	1/2 V_{DDIN}	23	I	$\overline{TEST}$	39	O	TD_{OUT}
8	I	CC_4	24	I	$F/\overline{M}$	40	–	DG
9	O	CC_3	25	O	D_{OUT}	41	–	AG
10	I	DEM_1	26	I	DSTB	42	O	MOD
11	O	DEM_2	27	I	DCK	43	–	V_{DDD}
12	O	EXP_{IN}	28	I	D_{IN}	44	O	LIM_{OUT}
13	I	EXP_{OUT}	29	I	FCL	45	I	LIM
14	O	AF_{OUT}	30	O	FD_{OUT}	46	O	$SAMP_{OUT}$
15	I	$RAMP_{IN}$	31	O	RCK	47	I	$SAMP_{IN}$
16	O	$RAMP_{OUT}$	32	O	RD	48	O	S_{OUT}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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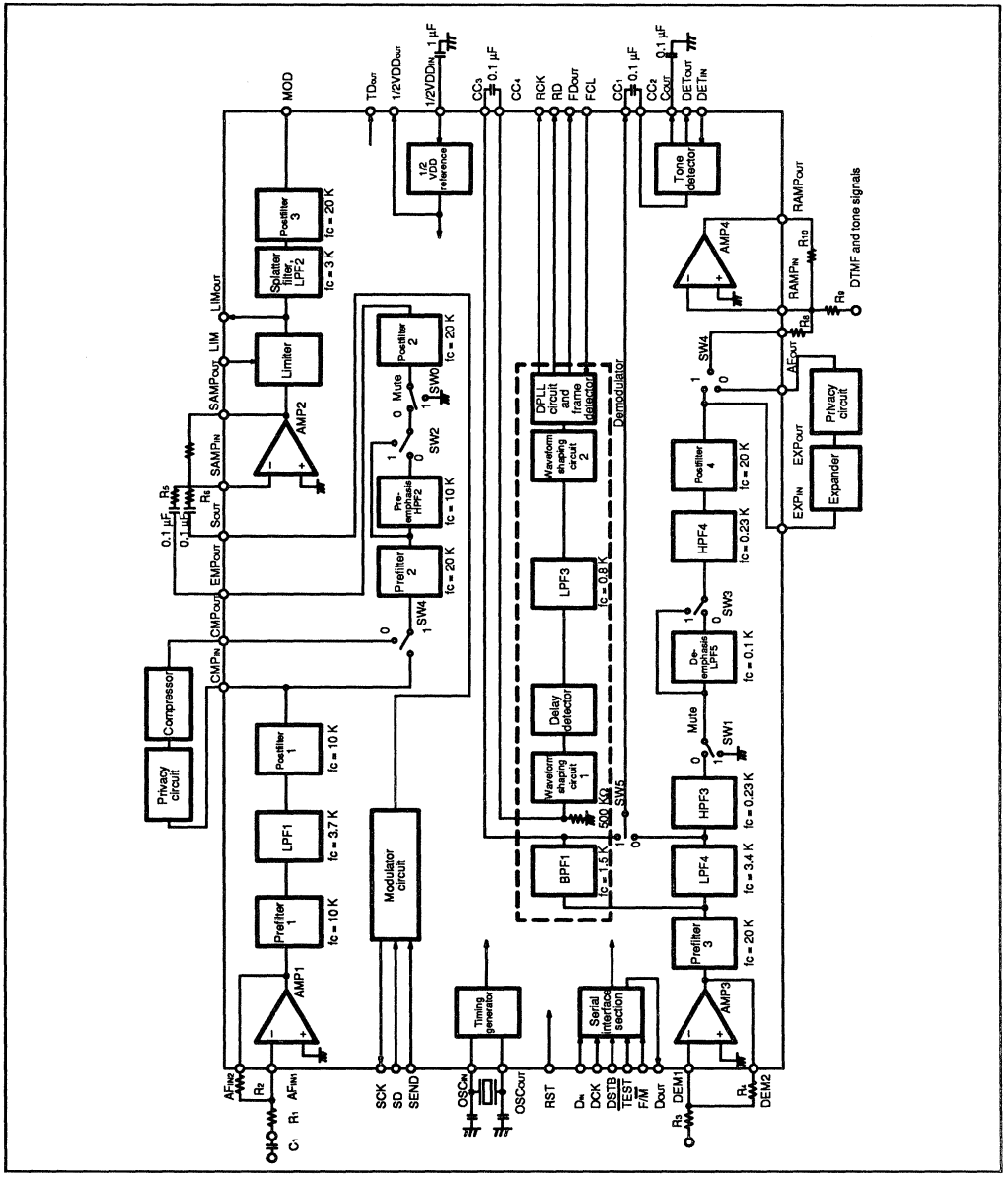
PIN DESCRIPTION

	Pin No.	Pin name	Function
Power supply pins	19	V_{DDA}	Analog supply voltage (3.0 to 5.5 V).
	40	DG	Digital ground
	41	AG	Analog ground
	43	V_{DDD}	Digital supply voltage (3.0 V to 5.5 V). $V_{DDD} = V_{DDA}$ is recommended.
Input pins	2	$COMP_{OUT}$	Input from external compressor
	5	AF_{IN1}	Inverting input of the input transmit amplifier The transmit input amplifier gain is adjusted by two external resistors, R1 and R2. R1 is connected to this pin and R2 connected between this pin and pin 4 (AF_{IN2}).
	7	1/2 V_{DDIN}	Input to the 1/2 V_{DD} generator. A 1 µF bypass capacitor is usually connected from this pin to analog ground (pin 41)
	10	DEM_1	Inverting input of the receive input amplifier The receiver input amplifier gain is adjusted by two external resistors, R3 and R4. R3 is connected to this pin and R4 is connected between this pin and pin 11 (DEM_2).
	13	EXP_{OUT}	Input from external expander
	15	$RAMP_{IN}$	Inverting input of the receive summing amplifier
	21	DET_{IN}	Reference voltage input to the tone detector. With this pin open, the reference voltage level is 1/100 V_{DD}.
	23	$\overline{TEST}$	Input for pattern check mode selection When $\overline{TEST}$ is low, an internal pattern is loaded into the shift register on the rising edge of DCK. When $\overline{TEST}$ is high, data at DIN is loaded into the shift register ans data in the shift register is shifted out to D_{OUT} on the rising edge of DCK. This pin is pulled by up a high resistance.
	24	F/$\overline{M}$	Mode selection input. When F/$\overline{M}$ is low, the mode selection pattern is set and checked. When F/$\overline{M}$ is high, the frame synchronization pattern is set and checked.
	26	DSTB	Input serial signal strobe. An input serial signal is validated on the rising edge of DSTB.
	27	DCK	Input serial signal clock. Serial data at D_{IN} is read in on the rising edge of DCK. (When $\overline{TEST}$ is high)
	28	D_{IN}	Input for serial signals from the microprocessor
	29	FCL	Frame detection latch clear input. When FCL is low, FD_{OUT} goes low. This pin is pulled up by a high resistance. FCL is pulled low to pull FD_{OUT} low after the frame synchronization pattern is set.
	33	SD	MSK modem data input
	35	SEND	Mutes transmit data to the MSK modem. A high on the SEND line enables data transmission.
	36	RST	Reset input. A low on RST resets all circuits. This pin is pulled up by a high resistance.

	Pin No.	Pin name	Function
Input pins	37	OSC_{IN}	Internal oscillator inputs. A 3.6864 or 3.456 MHz crystal is connected between OSC_{IN} and OSC_{OUT}.
	38	OSC_{OUT}	
	45	LIM	Limiter level adjustment input. The limiter level is set to 0.05 V_{DD} (V) when this pin is left open.
	47	$SAMP_{IN}$	Inverting input of the transmit summing amplifier
Input pin	8	CC_4	For demodulator external coupling capacitor. A 0.1 µF capacitor is connected between CC_3 and CC_4.
Output pin	9	CC_3	
Output pin	17	CC_1	For tone detector input external coupling capacitor. A 0.1 µF capacitor is connected between CC_1 and CC_2.
Input pin	18	CC_2	
Output pins	1	EMP_{OUT}	Pre-emphasis output
	3	$COMP_1$	Output to external compressor
	4	AF_{IN2}	Output of input transmit amplifier. The transmit input gain is adjusted with external registors connected to this pin and pin 5 (AF_{IN1}).
	6	1/2 VDD_{OUT}	Output of the 1/2 V_{DD} reference. Internal circuit operation is referenced to the voltage on this pin.
	11	DEM_2	Output of receive input amplifier. The receive input amplifier gain is adjusted with external resistors connected to this pin and pin 10 (DEM_1).
	12	EXP_{IN}	Output to external expander
	14	AF_{OUT}	Output to external expander or de-emphasis
	16	$RAMP_{OUT}$	Output of receive summing amplifier
	20	C_{OUT}	Output of tone detector. An external 0.1 µF capacitor is connected from this pin to ground complete the internal primary LPF configuration.
	22	DET_{OUT}	Tone detector output. DET_{OUT} is high when the input to the tone detector (rms value) exceeds the reference voltage.
	25	D_{OUT}	Pattern check setting output When TEST is high, the rising edge of DCK triggers output of the pattern.
	30	FD_{OUT}	Frame detection circuit output. FD_{OUT} goes high when a signal matching the frame synchronization pattern is output from RD after a reset.
	31	RCK	MSK modem receive clock output. RD data is output on the rising edge of RCK.
	32	RD	MSK modem receive data output
	34	SCK	MSK modem transmit clock output. SD data is read in on the rising edge of SCK.
	39	TD_{OUT}	Test digital output
	42	MOD	Transmit output
	44	LIM_{OUT}	Limiter output
	46	$SAMP_{OUT}$	Output of the transmit summing amplifier
	48	S_{OUT}	MSK modulated signal output

BLOCK DIAGRAM



CIRCUIT FUNCTIONS

The MB86460 consists of the transmit filters, receive filters, MSK modulator, MSK demodulator, digital circuits, and tone detector.

1. Transmit filters

The input amplifier AMP1 controls the gain of the transmitted VF signal. Gain is adjusted with external resistors R1 and R2. The input signal is then band-limited to 3.7 kHz or less by the transmit filter LPF1. The signal is then output at CMP_{IN} to an external compressor. We recommend forming an RC filter using external resistor R1, and external capacitor C1.
The compressor output signal is input to filter HPF2 at CMP_{OUT} for 6 dB/octave pre-emphasis. The pre-emphasis filter can be bypassed externally.
The pre-emphasis filter output is brought out at EMP_{OUT} to the external summing network of summing amplifier AMP2, where the signal is summed with the MSK modulating signal. The signal then enters the limiter. The limiter level can be adjusted externally at the LIM pin.
The output of the limiter is then band-limited to 3 kHz by splatter filter LPF2 and output at the MOD pin. the transmitted VF signal can be muted externally.

2. Receive filters

Input amplifier AMP3 controls the gain of the received VF signal. Gain is adjusted by external resistors R3 and R4. The input signal is then band-limited to 0.23 kHz to 3.4 kHz by receive filters LPF4 and HPF3. The signal then enters filter LPF5, where the 6 dB/octave pre-emphasis is removed. The de-emphasis filter can be bypassed externally.
The output of the de-emphasis filter is brought out to the EXP_{IN} pin to an external expander. The expander output is then input to summing amplifier AMP4, where the signal is summed with tone, DTMF, or other signal. The signal is then output at $RAMP_{OUT}$. The receive VF signal can be muted externally.

3. MSK modulator

In the MSK modulator, a 1200-Hz (data 1) or 1800-Hz (data 0) sine-wave signal is generated for data input to pin SD in synchronization with transmit clock SCK. The MSK modulator signal then passes through pin S_{OUT} and enters summing amplifier AMP2, where the signal is summed with the transmit VF signal.

4. MSK demodulator

The received MSK signal passes through receive input amplifier AMP3. The signal then enters BPF1, where frequencies other than 1200 and 1800 Hz are eliminated. The signal passes through waveform-shaping circuit 1 and is A/D converted. The signal then enters the delay detector, where data is regenerated. The noise components in the regenerated data are filtered out by LPF3 and then the signal enters waveform-shaping 2, where A/D conversion is done again.
The digital phase-locked loop (DPLL) circuit recovers receive clock RCK from the regenerated data signal and outputs the regenerated data at the RD pin.
The MB86460 has a built-in frame-detection function for reducing microprocessor load. When the regenerated data output from pin RD matches the frame synchronization pattern, FD_{OUT} goes high. The frame synchronization pattern can be set externally.

5. Digital circuits

The digital circuits consist of the timing generator and serial interface. The timing generator generates basic clocks for the MSK modulator and demodulator, transmit filters, and receive filters, and consists of a 3.6864-MHz crystal and an on-chip oscillator and divider circuits.
The signal interface is used to set the standby mode, the bypass mode, and the frame synchronization pattern, and to enable or and disable the transmit/receive mute function. These operations are microprocessor-controllable through serial signal lines D_{IN}, DCK, DSTB, and $F/\overline{M}$.

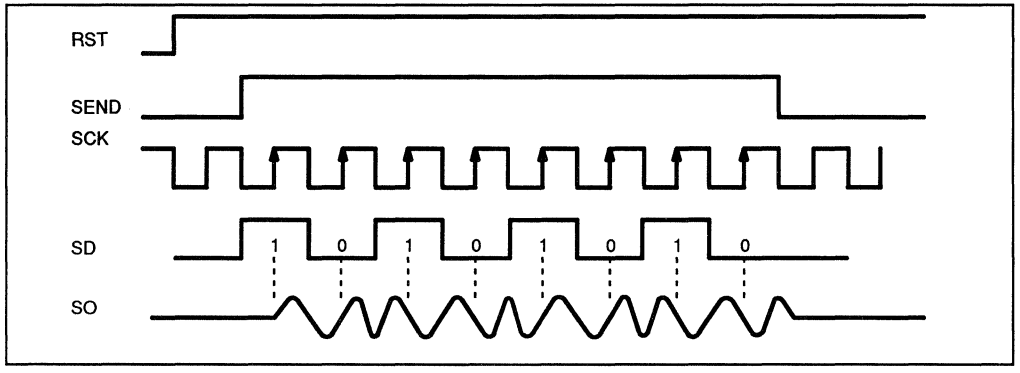
6. Tone detector

The tone detector is used for interference or carrier detection during demodulation. The tone detector full-wave-rectifies the output of the receive LPF or demodulator BPF, smoothes the signal, and compares it with the reference to check for interference or carrier presence.

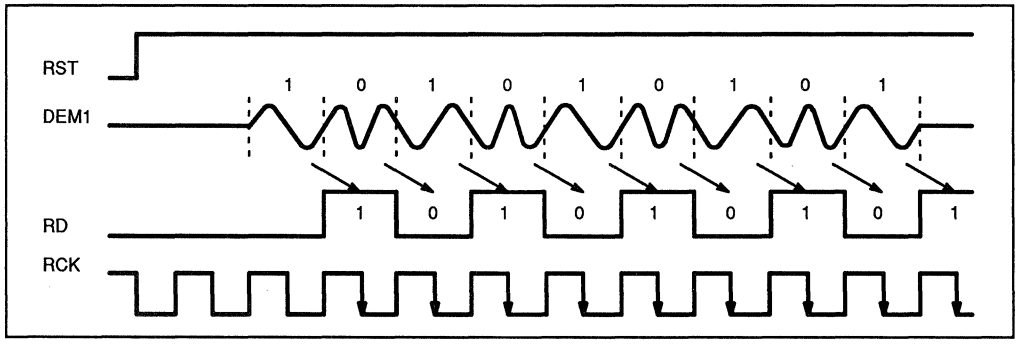
FUNCTION DESCRIPTIONS

1. Timing chart for the 1200-bps MSK modem

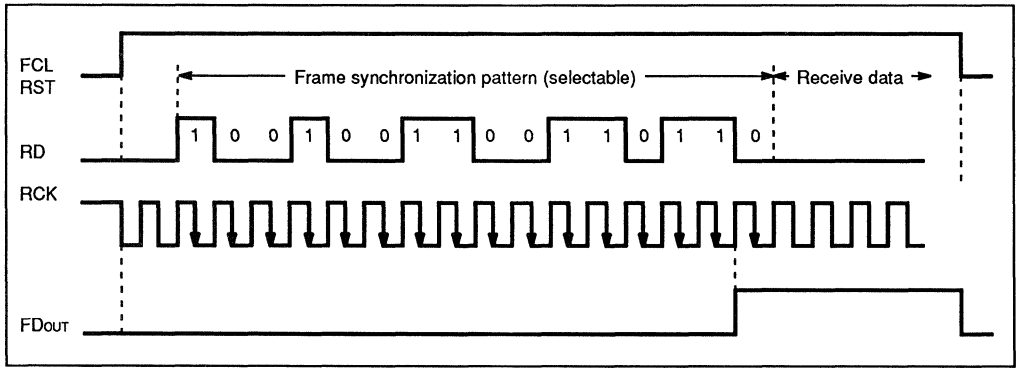
1. Modulation



2. Demodulation



3. Frame detection



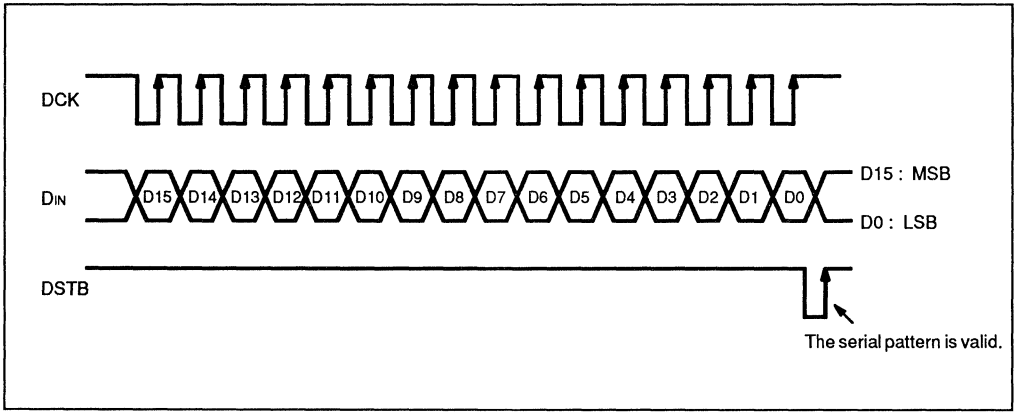
2. Limiter

$SAMP_{OUT}$ input level (V_i)	LIM_{OUT} output level (V_o)	Condition
$\frac{V_{DD}}{2} - 0.25 > V_i$	$\frac{V_{DD}}{2} - 0.25$	LIM pin is open. V_{DD} = 5.0 V
$\frac{V_{DD}}{2} - 0.25 \leq V_i \leq \frac{V_{DD}}{2} + 0.25$	V_i	
$\frac{V_{DD}}{2} + 0.25 < V_i$	$\frac{V_{DD}}{2} + 0.25$	
$V_{LIM} > V_i$	V_{LIM}	LIM pin = V_{LIM}
$V_{LIM} \leq V_i \leq V_i - V_{LIM}$	V_i	
$V_{DD} - V_{LIM} < V_i$	$V_{DD} - V_{LIM}$	

3. Microprocessor interface (mode selection)

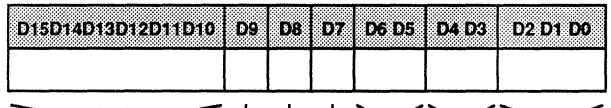
The serial interface selects the standby mode and mute mode.

① Data input timing ($\overline{TEST}$ is high, F/$\overline{M}$ is low)



FUNCTION DESCRIPTIONS

② Data setting



Function	Explanation
Selects the standby mode.	See the standby mode.
Selects the mute mode.	See the mute mode.
Selects the pre-emphasis/ de-emphasis bypass mode.	See the pre-emphasis/ de-emphasis bypass mode.
Selects the compander bypass mode.	See the compander bypass mode.
Selects the tone detector mode.	See the tone detector mode.
Selects the crystal oscillator mode.	See the crystal oscillator mode.
Selects the test mode.	See the test mode.

On reset, D15 to D3, D1, and D0 are set to 0, and D2 is set to 1.

- Standby mode
  (D2, D1, D0)

D2	D1	D0

→ Mode selection (Mn): n indicates values in binary notation for D2 (MSB) to D0 (LSB).

Block		Circuit	Mode						Remarks
			M0	M1	M2	M3	M4	M5	
Transmit system	Voice-band filters	AMP1	O	O	X	X	X	X	
		Prefilter 1	O	O	X	X	X	X	
		LPF1	O	O	X	X	X	X	
		Postfilter 1	O	O	X	X	X	X	
		Prefilter 2	O	O	X	X	X	X	
		HPF2	O	O	X	X	X	X	
		Postfilter 2	O	O	X	X	X	X	
		AMP2	O	O	X	X	X	X	
		Limiter	O	O	X	X	X	X	
		LPF2	O	O	X	X	X	X	
		Postfilter 3	O	O	X	X	X	X	
	MODEM	Modulator circuit	O	X	X	X	X	X	
Receive system	Voice-band filters	AMP3	O	O	O	O	X	X	
		Prefilter 3	O	O	O	O	X	X	
		LPF4	O	O	O	X	X	X	
		HPF3	O	O	O	X	X	X	
		HPF4	O	O	O	X	X	X	
		LPF5	O	O	O	X	X	X	
		Postfilter 4	O	O	O	X	X	X	
		AMP4	O	O	O	X	X	X	
		Tone detector	O	O	O	O	X	X	
	MSK MODEM	BPF1	O	X	O	O	X	X	
		Waveform-shaping circuit 1	O	X	O	O	X	X	
		LPF3	O	X	O	O	X	X	
		Waveform-shaping circuit 2	O	X	O	O	X	X	
Others		OSC	O	O	O	O	O	X	
		1/2 V_{DD} reference	O	O	O	O	X	X	

O .... Active X .... Powered down

Note: During reset, mode M4 is set.

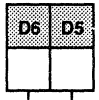
6

FUNCTION DESCRIPTIONS

- Mute mode
  (D4, D3)

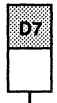
	"0"	"1"	Remarks
Transmit mute selection	Active	Muted	SW0
Receive mute selection	Active	Muted	SW1

- Pre-emphasis/de-emphasis bypass mode
  (D6, D5)



	"0"	"1"	Remarks
Pre-emphasis bypass selection	Used	Bypassed	SW2
De-emphasis bypass selection	Used	Bypassed	SW3

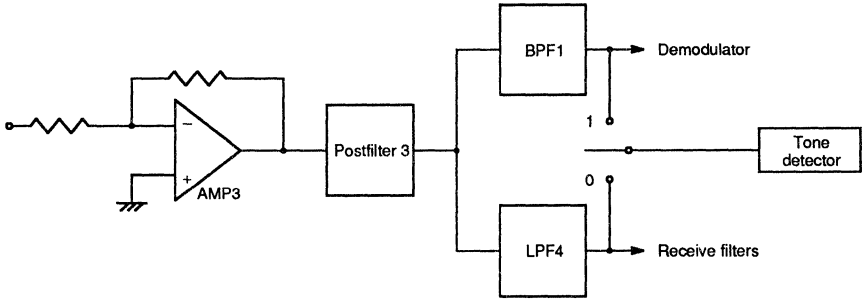
- Compander bypass mode
  (D7)



	"0"	"1"	Remarks
Compander bypass selection	Used	Bypassed	SW4

- Tone detector mode
  (D8)

D8		"0"	"1"	Remarks
	Tone detector mode selection	Interference detection	Carrier detection	SW5



- Crystal oscillator mode
  (D9)

D9		"0"	"1"	Remarks
	Crystal oscillator mode selection	3.6864 MHz	3.456 MHz	

Note: The internal dividing ratio depends on the frequency of the crystal.

- Test mode
  (D15 to D10)

D15	D14	D13	D12	D11	D10		"0"	"1"	Remarks
						Digital output selection	"00" : Modulator (normal) "01" : Waveform-shaping circuit 1 "10" : Deley detector "11" : Waveform-shaping circuit 2		Output from TD_{OUT} (In test mode)
						Digital test selection	Normal	Test	
						Analog test selection	Normal	Test	
							don't care		For expansion

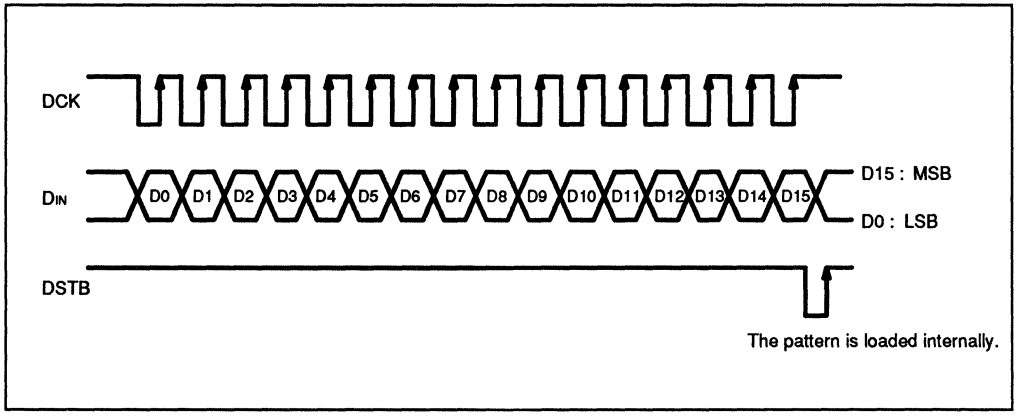
Note: In no-test (normal operation) mode, set D12 and D13 to 0.

FUNCTION DESCRIPTIONS

4. Setting the frame synchronization pattern

The frame synchronization pattern is set via the serial interface pins. (16 bits)
For strobe, use DSTB and set F/$\overline{M}$ to high.

Data input timing ($\overline{TEST}$ is high, F/$\overline{M}$ is high)



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ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Pin name	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	V_{DD}	GND–0.3	–	7	V
Input voltage	V_{IN}	All input pins	GND–0.3	–	V_{DD}+0.3	V
Output voltage	V_{OUT}	All output pins	GND–0.3	–	V_{DD}+0.3	V
Output current	I_{OUT}	All output pins	–10	–	10	mA
Storage temperature	T_{stg}		–40	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	V_{DD}	3.0 *	5.0	5.5	V
Input voltage	V_{IN}	All input pins	0	–	V_{DD}	V
Analog output load resistance	R_L	All analog output pins	50	–	–	kΩ
Analog output load capacitance	C_L	All analog output pins	–	–	30	pF
OSC pin load capacitance	C_{OSC}	OSC_{IN}, OSC_{OUT}	20	30	50	pF
Operating temperature	T_A		–20	25	70	°C

* The MB86460A operates down to 2.7 V, but electrical characteristics are not guaranteed from 2.7 V to 3.0 V.

ELECTRICAL CHARACTERISTICS

1. Transmit characteristics

V_{DD} = 3.0 to 5.5 V, T_A = –20 to 70 °C

Parameter	Symbol	Pin name	Condition	Minimum	Typical	Maximum	Unit
Transmit gain 1	T_{GAIN1}	AF_{IN1}–MOD	Input: –27 dBV, 1 kHz $R_1 = R_2$, $R_5 = R_7$ With pre-emphasis. Compander bypassed.	7.0	9.0	11.0	dB
Transmit mute	T_{MUTE}	AF_{IN1}–MOD	Input: –27 dBV, 1 kHz $R_1 = R_2$, $R_5 = R_7$ With pre-emphasis. Compander bypassed. Transmit muted.	45	–	–	dB
Transmit signal-to-noise ratio	$T_{S/N}$	AF_{IN1}–MOD	Input: –27 dBV, 1 kHz $R_1 = R_2$, $R_5 = R_7$ With pre-emphasis. Compander bypassed. Band: 50 Hz to 20 kHz	40	–	–	dB
Transmit distortion	$T_{S/D}$	AF_{IN1}–MOD	Same as above	–	–	–40	dB
Receive gain	R_{GAIN1}	DEM_1–$RAMP_{OUT}$	Input: –26 dBV, 1 kHz $R_3 = R_4$, $R_8 = R_{10}$ With de-emphasis. Compander bypassed.	–1.0	0.0	1.0	dB
Receive mute	R_{MUTE}	DEM_1–$RAMP_{OUT}$	Input: –18 dBV, 1 kHz $R_3 = R_4$, $R_8 = R_{10}$ With de-emphasis. Compander bypassed. Receive muted.	45	–	–	dB
Receive signal-to-noise ratio	$R_{S/N}$	DEM_1–$RAMP_{OUT}$	Input: –18 dBV, 1 kHz $R_3 = R_4$, $R_8 = R_{10}$ With de-emphasis. Compander bypassed. Band: 50 Hz to 20 kHz	40	–	–	dB
Receive distortion	$R_{S/D}$	DEM_1–$RAMP_{OUT}$	Same as above	–	–	–40	dB
Transmit gain 2	T_{GAIN2}	AF_{IN1}–EMP_{OUT}	Input: –27 dBV, 1 kHz $R_1 = R_2$ With pre-emphasis. Compander bypassed.	–1.0	0.0	1.0	dB
Transmit gain 3	T_{GAIN3}	EMP_{OUT}–MOD	Input: –27 dBV, 1 kHz $R_5 = R_7$	8.0	9.0	10.0	dB
Transmit frequency characteristics	T_{FA}	AF_{IN1}–MOD	Input: –27 dBV $R_1 = R_2$, $R_5 = R_7$ With pre-emphasis. Compander bypassed.	Shown in Figure 1.			

V_{DD} = 3.0 to 5.5 V, T_A = –20 to 70 °C

Parameter	Symbol	Pin name	Condition		Minimum	Typical	Maximum	Unit
Receive frequency characteristics	R_{FA}	DEM_1–$RAMP_{OUT}$	Input: –26 dBV $R_3 = R_4$, $R_5 = R_7$ With de-emphasis. Compander bypassed.		Shown in Figure 2.			
Demodulator BPF gain	B_{GAIN}	DEM_1–CC_1	Input: –18 dBV, 1.5 kHz $R_3 = R_4$		–1.5	0	1.5	dB
Demodulator LPF gain	L_{GAIN}	CC_4–CC_3	Input: –18 dBV, 300 Hz In test mode		–	–6.0	–	dB
Demodulator BPF frequency characteristics	B_{FA}	DEM_1–CC_1	Input: –18 dBV, $R_3 = R_4$	0-300Hz 900-1200Hz 1200-1800Hz 1800-2100Hz 3000-5000Hz	– –3.5 –1.0 –3.5 –	– – – – –	–30.0 – – – –30.0	dB
Demodulator LPF frequency characteristics	L_{FA}	CC_4–CC_3	Input: –18 dBV, In test mode Reduced by 3 dB		–	800	–	Hz

6

ELECTRICAL CHARACTERISTICS

2. DC characteristics

V_{DD} = 3.0 to 5.5 V, T_A = –20 to 70 °C

Parameter	Symbol	Pin name	Condition	Minimum	Typical	Maximum	Unit
Supply current	I_{DD0}	V_{DD}	Standby mode 0	3	8	14	mA
	I_{DD1}		Standby mode 1	2	6	11	mA
	I_{DD2}		Standby mode 2	1.5	5	8.5	mA
	I_{DD3}		Standby mode 3	1.3	4.5	8.0	mA
	I_{DD4}		Standby mode 4	0.1	1.0	2.0	mA
	I_{DD5}		Standby mode 5	–	25	100	µA
Low-level input voltage	V_{IL}	All digital input pins	–	0	–	0.3 x V_{DD}	V
High-level input voltage	V_{IH}		–	0.7 x V_{DD}	–	V_{DD}	V
Low-level input current	I_{IL}	SD, SEND, D_{IN} DCK, DSTB, F/$\overline{M}$	V_I = 0 V	–10	–	10	µA
High-level input current	I_{IH}		V_I = V_{DD}	–10	–	10	µA
Low-level output voltage	V_{OL}	All digital output pins	I_{OL} = 0.5 mA	0	–	0.2 x V_{DD}	V
High-level output voltage	V_{OH}		I_{OH} = –0.5 mA	0.8 x V_{DD}	–	V_{DD}	V
Pull-up resistance	R_{LU}	RST, $\overline{TEST}$	–	50	100	200	kΩ
Oscillation frequency	f_{OSC}	OSC_{IN}, OSC_{OUT}	Mode 0	–	3.6864	–	MHz
			Mode 1	–	3.456	–	
Analog input resistance 1	R_{AIN1}	1/2 VDD_{IN}	–	50	100	200	kΩ
Analog input resistance 2	R_{AIN2A}	DET_{IN} Operating	Between this pin and 1/2 V_{DD}	25	50	100	kΩ
	R_{AIN2B}	DET_{IN} At power down	Between this pin and ground	225	450	900	
Analog input resistance 3	R_{AIN3A}	LIM_{IN} Operating	Between this pin and 1/2 V_{DD}	10	20	40	kΩ
	R_{AIN3B}	LIM_{IN} At power down	Between this pin and ground	90	180	360	
Analog output load resistance	R_L	AF_{IN2}, CMP_{IN}, EMP_{OUT}, S_{OUT}, $SAMP_{OUT}$, MOD, DEM_2, LIM_{OUT}, EXP_{IN}, $RAMP_{OUT}$	Between this pin and 1/2 V_{DD}	50	–	–	kΩ
Analog output load capacitance 1	C_{L1}	AF_{IN2}, CMP_{IN}, EMP_{OUT}, S_{OUT}, $SAMP_{OUT}$, MOD, DEM_2, LIM_{OUT}, EXP_{IN}, $RAMP_{OUT}$	–	–	–	100	pF
Analog output load capacitance 2	C_{L2}	C_{OUT}	–	–	0.1	–	µF

V_{DD} = 3.0 to 5.5 V, T_A = –20 to 70 °C

Parameter	Symbol	Pin name	Condition		Minimum	Typical	Maximum	Unit
Analog input voltage range	V_{IA}	CMP_{OUT}	–		$\frac{1}{4}V_{DD}$	–	$\frac{3}{4}V_{DD}$	V
Analog output voltage range	V_{OA}	AF_{IN2}, CMP_{IN}, EMP_{OUT}, $SAMP_{OUT}$, MOD, DEM_2, EXP_{IN}, $RAMP_{OUT}$, LIM_{OUT}	–		$\frac{1}{4}V_{DD}$	–	$\frac{3}{4}V_{DD}$	V
Modulator output voltage	V_{MOT1}	S_{OUT}	Operating		0.16 x V_{DD}	0.2 x V_{DD}	0.24 x V_{DD}	V_{p-p}
	V_{MOT2}		Operating Offset voltage		$1/2V_{DD}$–0.3	$1/2V_{DD}$	$1/2V_{DD}$+0.3	V
	V_{MOT3}		SEND = "L"		$1/2V_{DD}$–0.3	$1/2V_{DD}$	$1/2V_{DD}$+0.3	V
Limiter high voltage	V_{DLH}	$SAMP_{OUT}$–LIM_{OUT}	The LIM pin is open.		$1/2V_{DD}$ +0.04V_{DD}	$1/2V_{DD}$ +0.05V_{DD}	$1/2V_{DD}$ +0.06V_{DD}	V
			LIM pin = V_{LIM}		$1/2V_{DD}$+0.8 x ($1/2V_{DD}$–V_{LIM})	$1/2V_{DD}$+1.0 x ($1/2V_{DD}$–V_{LIM})	$1/2V_{DD}$+1.2 x ($1/2V_{DD}$–V_{LIM})	V
Limiter low voltage	V_{DLL}	$SAMP_{OUT}$–LIM_{OUT}	The LIM pin is open.		$1/2V_{DD}$ –0.06V_{DD}	$1/2V_{DD}$ –0.05V_{DD}	$1/2V_{DD}$ –0.04V_{DD}	V
			LIM pin = V_{LIM}		$1/2V_{DD}$–1.2 x ($1/2V_{DD}$–V_{LIM})	$1/2V_{DD}$–1.0 x ($1/2V_{DD}$–V_{LIM})	$1/2V_{DD}$–0.8 x ($1/2V_{DD}$–V_{LIM})	V
Tone detection level	V_{DET}	DET_{IN}	$R_3 = R_4$	The DET_{IN} pin is open.	$\frac{1}{125}V_{DD}$	$\frac{1}{100}V_{DD}$	$\frac{1}{80}V_{DD}$	V_{rms}
				DET_{IN} pin = V_{DT}	1/12.5x ($1/2V_{DD}$–V_{DT})	1/10x ($1/2V_{DD}$–V_{DT})	1/8x ($1/2V_{DD}$–V_{DT})	V_{rms}

6

ELECTRICAL CHARACTERISTICS

3. AC characteristics

V_{DD} = 3.0 to 5.5 V, T_A = −20 to 70 °C

Parameter	Symbol	Pin name	Condition	Minimum	Typical	Maximum	Unit
SCK delay time 1	td_{sc1}	SCK	–	0	150	417	µs
SCK delay time 2	td_{sc2}	SCK	–	417	570	834	µs
SCK delay time 3	td_{sc3}	SCK	–	0	150	417	µs
FDO delay time 1	td_{FD1}	FD_{OUT}	–	0	–	1	µs
FDO delay time 2	td_{FD2}	FD_{OUT}	–	0	–	1	µs
SCK low width	tw_{LS}	SCK	–	390	417	444	µs
SCK high width	tw_{HS}	SCK	–	390	417	444	µs
SEND setup time	ts_{SE}	SEND	–	1	–	–	µs
SEND hold time	th_{SE}	SEND	–	1	–	–	µs
SD setup time	ts_{SD}	SD	–	1	–	–	µs
SD hold time	th_{SD}	SD	–	1	–	–	µs
S_{OUT} delay time 1	td_{SO1}	S_{OUT}	–	0	–	20	µs
S_{OUT} delay time 2	td_{SO2}	S_{OUT}	–	0	–	20	µs
S_{OUT} delay time 3	td_{SO3}	S_{OUT}	–	0	–	10	µs
MSK input invalid time	td_{RI}	DEM_1, DEM_2	–	0	–	10	ms
Number of fetched bits	N	–	DEM_1, DEM_2 No noise	–	–	15	bit
Demodulator delay time	td_{BD}	RD	N ≥ 15 DEM_1, DEM_2 No noise	1483	1900	2317	µs
RD timimg	td_{RD}	RD	–	−1	–	1	µs
RCK low width	tw_{LR}	RCK	N ≥ 15 DEM_1, DEM_2 No noise	338	417	496	µs
RCK high width	tw_{HR}	RCK	N ≥ 15 DEM_1, DEM_2 No noise	338	417	496	µs
RST low width	tw_{LC}	RST	–	20	–	–	µs
Digital input rise time	t_r	RST, SEND, SD, D_{IN}, DCK, DSTB, $\overline{TEST}$, F/$\overline{M}$	–	–	–	100	ns
Digital input fall time	t_f	RST, SEND, SD, D_{IN}, DCK, DSTB, $\overline{TEST}$, F/$\overline{M}$	–	–	–	100	ns

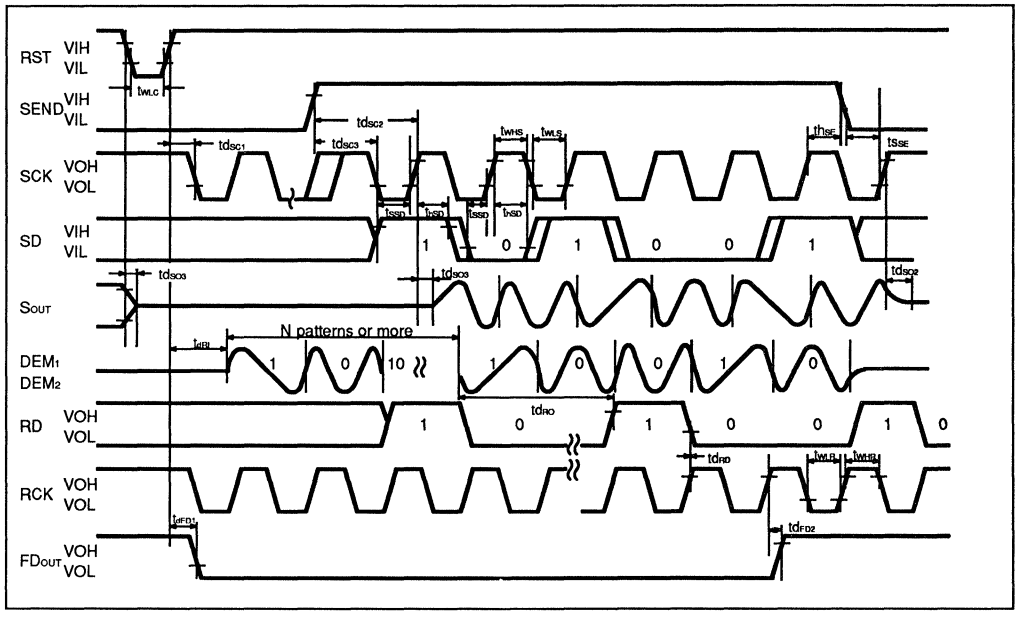
V_{DD} = 3.0 to 5.5 V, T_A = –20 to 70 °C

Parameter	Symbol	Pin name	Condition	Minimum	Typical	Maximum	Unit
D_{IN} setup time	ts_D	D_{IN}	–	100	–	–	ns
D_{IN} hold time	th_D	D_{IN}	–	100	–	–	ns
Strobe setup time	ts_T	DSTB	–	100	–	–	ns
DCK low width	tw_{LD}	DCK	–	100	–	–	ns
DCK period	tw_{WD}	DCK	–	2	–	–	µs
Strobe low width	tw_{LT}	DSTB	–	100	–	–	ns
$\overline{TEST}$ setup time	ts_{TE}	$\overline{TEST}$	–	100	–	–	ns
$\overline{TEST}$ hold time	th_{TE}	$\overline{TEST}$	–	100	–	–	ns
F/$\overline{M}$ setup time	ts_{FM}	F/$\overline{M}$	–	100	–	–	ns
F/$\overline{M}$ hold time	th_{FM}	F/$\overline{M}$	–	100	–	–	ns
D_{OUT} delay time	td_O	D_{OUT}	–	0	–	1	µs

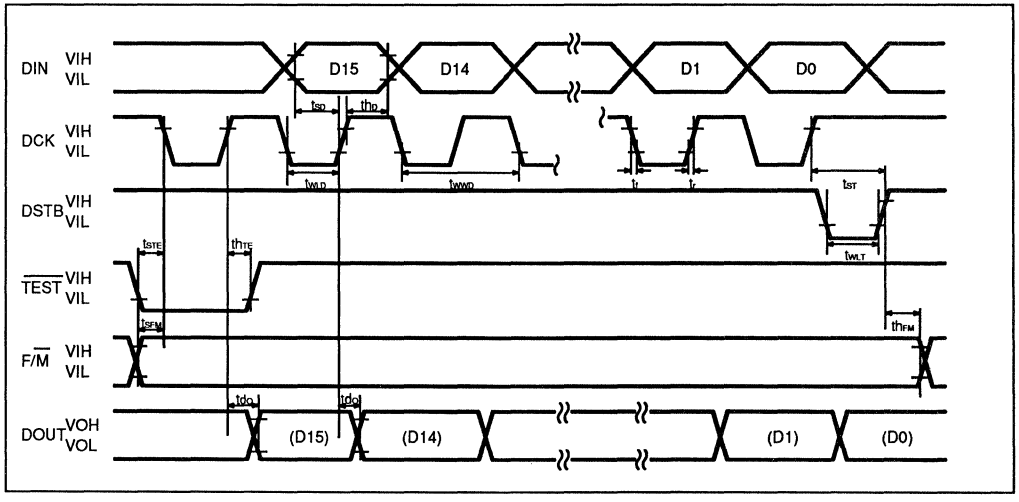
6

TIMING CHART

① MSK modem timing



② Serial interface timing



TRANSMIT RECEIVE CHARACTERISTICS

Figure 1 Transmit frequency characteristics

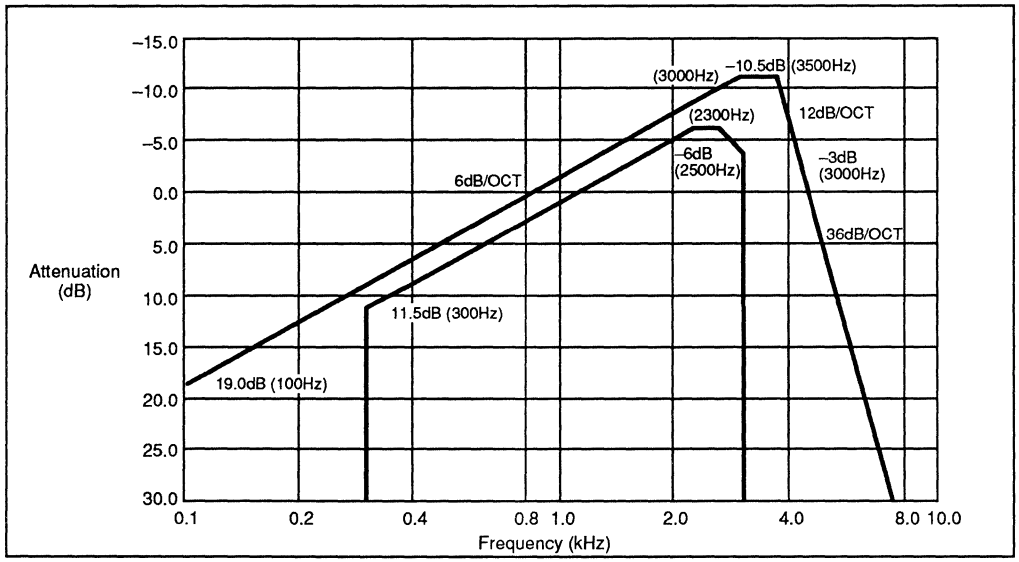
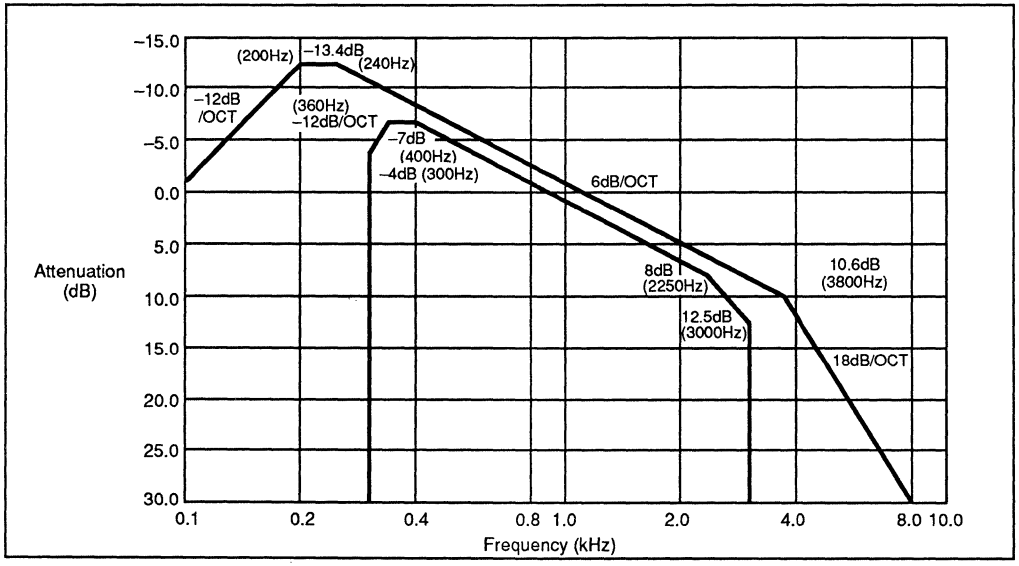


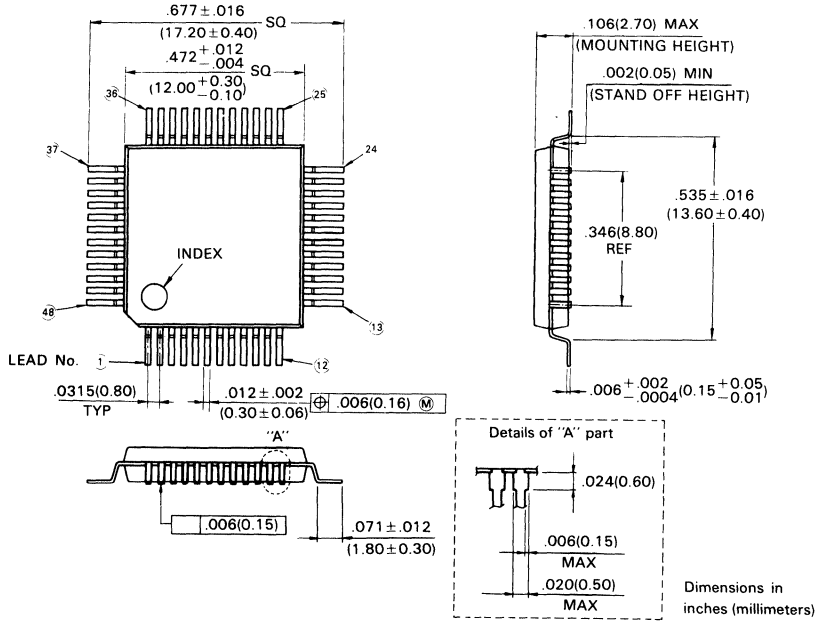
Figure 2 Receive frequency characteristics



6

DIMENSIONS

48-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-48-M02)



November 1990
Edition 3.0

FUJITSU

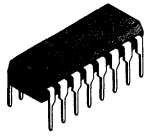
DATA SHEET

MB87002
1200 BPS MSK MODEM

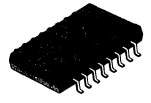
1200 BPS MSK (Minimum Shift Keying) MODEM

The MB87002 is a 1200–bps CMOS minimum shift keying (MSK) single–chip modem for multichannel access (MCA) and radio communication application. Its operation at low supply voltages and low power consumption is especially suitable for portable application.

- Data rate: 1200–bps
- Low power consumption (20 mW with 5 V power supply)
- Low supply voltage operation: 3.0 to 5.5 V (5 V typical)
- On–chip crystal oscillator: 3.6864 MHz
- Switched–capacitor filter (SCF)
- Selectable timing regenerator pull–in characteristic (within 15 bits for high–speed, and within 25 bits for low–speed operation)
- Low external component count
- TTL compatible inputs and outputs



PLASTIC PACKAGE
(DIP-16P-M03)

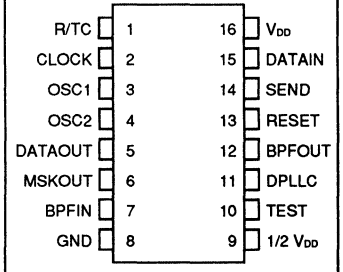


PLASTIC PACKAGE
(FPT-16P-M03)

6

PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	GND – 0.3	–	7	V
Input Voltage	V_{IN}	All input pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Voltage	V_{OUT}	All output pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Current	I_{OUT}	All output pins	–10	–	10	mA
Storage Temperature	T_{STG}	–	–55	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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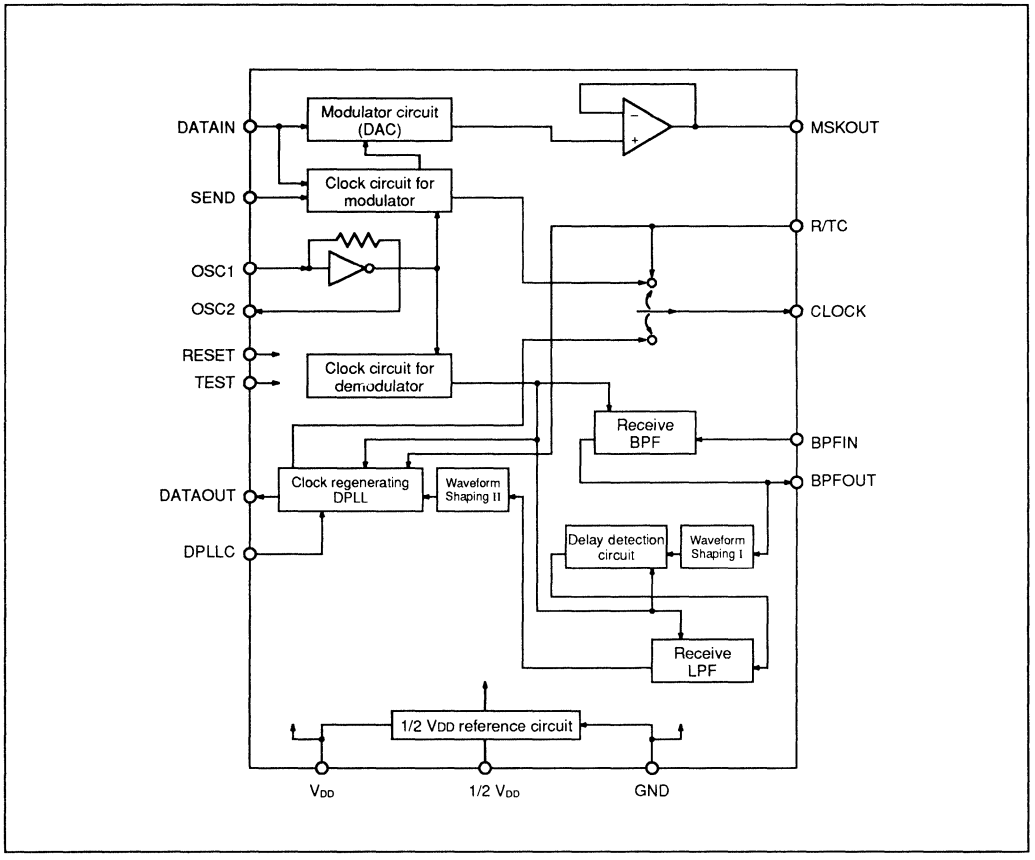
PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Functional descriptions
1	R/TC	I	Transmit–receive clock output control. When pulled high, the 1.2 kHz transmit clock is output from the CLOCK pin and DATAOUT becomes low. When pulled low, the 1.2 kHz receive clock is output from the CLOCK pin.
2	CLOCK	O	Transmit–receive clock output pin. When R/TC pin is pulled high, 1.2 kHz transmit clock is output. When R/TC pin is pulled low, the 1.2 kHz receive clock is output.
3	OSC1	I	Pin for external crystal (3.6864 MHz) connection.
4	OSC2	O	Pin for external crystal (3.6864 MHz) connection.
5	DATAOUT	O	Regenerated data output signal.
6	MSKOUT	O	Modulated signal output pin. $V_{DD}/2$ is output when the RESET pin is pulled low.
7	BPFIN	I	Demodulated signal input to the receive band–pass filter (BPF).
8	GND	–	Ground
9	1/2 V_{DD}	O	$V_{DD}/2$ reference voltage output
10	TEST	I	Test function control signal input. In the normal mode, this pin is pulled high or left open. In the test mode, it is pulled low. In the test mode, the BPF IN pin directly accepts Waveform Shaping I and receive LPF input signals, and the DATA IN pin directly accepts Waveform Shaping II input signals. In this mode, the delay detection circuit signal is output from BPFOUT and the receive LPF signal is output from MSKOUT.
11	DPLLC	I	DPLL pull–in time control signal input. When pulled low, high–speed operation is selected. When pulled high, low–speed operation is selected.
12	BPFOUT	O	Receive BPF output pin.
13	RESET	I	Device reset signal input. A low on this pin resets all circuits. Pulled high or left open to enable device operation.
14	SEND	I	Data transmit enable. With the reset high or open, transmit signals are output when this pin is pulled low to high.
15	DATAIN	I	Transmit data input to the receive BPF.
16	V_{DD}	–	Supply voltage pin (+3.0 to +5.5 V).

MB87002 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The timing generating section generates the clock signals required by the modulator and demodulator. The basic clock is generated by an internal oscillator and external crystal (3.6864 MHz).
Modulator uses a programmable DAC with a 6 bit resistor string. The MSKOUT output is 1200 Hz for input 1 and 1800 Hz for input 0 synchronized with transmit clock. Before the transmit signal is output, a fixed level of 1/2 V_{DD} is output by pulling the SEND pin low. The demodulator is composed of a band-pass filter (BPF), a delay detection circuit, a low-pass filter (LPF), and a digital phase-locked loop (DPLL). The BPF removes noise components from the 1,200 Hz and 1,800 Hz receive signals from the BPFIN pin and consists of a 10th-order Chebyshev switched-capacitor filter (SCF). The delay detection circuit, after conversion of the BPF output from analog to digital in the waveform shaping circuit, regenerates data by delay detection. The noise components in the regenerated data are removed by the LPF. The LPF is a third-order Butterworth filter and removes noise components of 800 Hz or higher. The DPLL extracts the receive clock from the regenerated data. The regenerated data is output from the DATAOUT pin synchronized with the receive clock. The DPLL has a tendency to degrade the bit error rate when the pull-in time is shortened. This IC allows users to choose between two pull-in times. When the DPLLC pin is pulled low, the high-speed mode is selected. When pulled high, the low-speed mode is selected.
The on-chip 1/2 V_{DD} circuit supplies the reference voltage required by BPF, LPF, and waveform shaping circuits and reduces external circuitry and component count.

NOTE: Devices consisting of mixed analog and digital signal processing circuits are usually difficult to test. The MB87002 **incorporates a test circuit which simplifies independent testing of the BPF, delay detection circuit, LPF and DPLL.**

RECOMMENDED OPERATING CONDITIONS

6

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	3.0	5.0	5.5	V
Input Voltage	V_{IN}	All input pins	0	–	V_{DD}	V
OSC1 Pin Load Capacitance	C_{OSC1}	OSC1	25	–	50	pF
OSC2 Pin Load Capacitance	C_{OSC2}	OSC2	25	–	50	pF
Analog Output Load Resistance	R_{MO}	MSKOUT	10	–	–	kΩ
Analog Output Load Capacitance	C_{MO}	MSKOUT	–	–	30	pF
Operating Temperature	T_A	–	–10	–	70	°C

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD} = 4.5 ~ 5.5 V)

T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	4	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.8	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull–up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 2.0 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 1.0 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog Input Voltage 1	V_{AIN1}	BPFIN		0.5	–	2.5	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	0.8	1.0	1.2	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–1.0	0	1.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 – 	– – – – – 	–40.0 – – – –30.0 	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

6

DC characteristics (V_{DD} = 3.0 ~ 4.5 V)

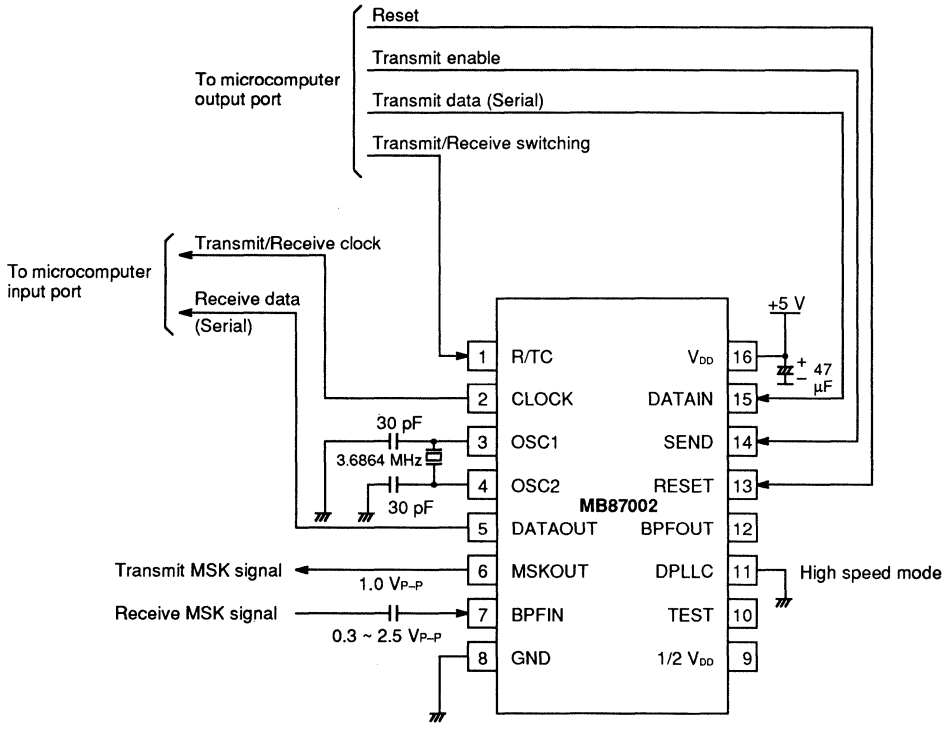
T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	–	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.6	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull-up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 0.5 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 0.5 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog Input Voltage 1	V_{AIN1}	BPFIN		0.5	–	V_{DD} – 2.0	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	V_{DD} x 0.16	V_{DD} x 0.2	V_{DD} x 0.24	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–2.0	0	2.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 – 	– – – – – 	–30.0 – – – –25.0 	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

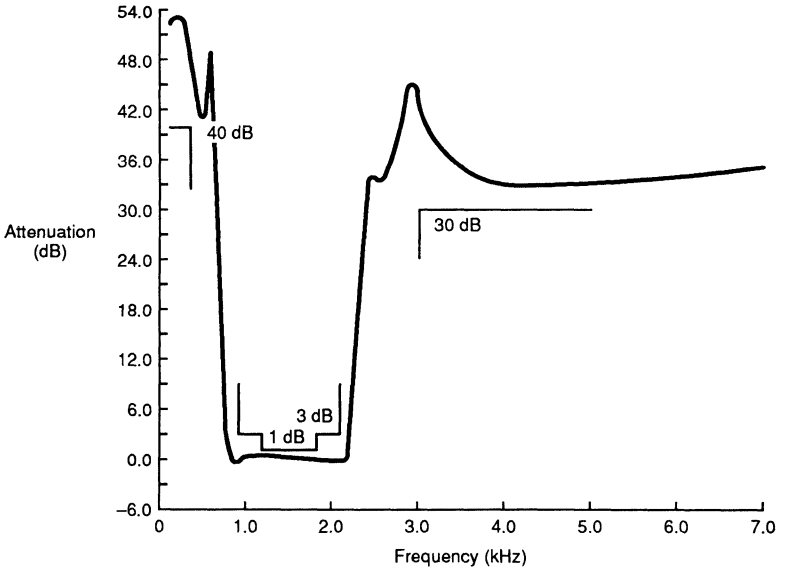
AC characteristics (V_{DD} = 3.0 ~ 5.5 V)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Transmit Clock Delay Time 1	t_{dRCH}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock Delay Time 2	t_{dSCH}	CLOCK	R/TC = "H"	417	570	834	µs
Transmit Clock Delay Time 3	t_{dSCL}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock High Width	t_{wHC1}	CLOCK	R/TC = "H"	390	417	444	µs
Transmit Clock Low Width	t_{wLC1}	CLOCK	R/TC = "H"	390	417	444	µs
SEND Setup Time	t_{SSC}	SEND	R/TC = "H"	1	–	–	µs
SEND Hold Time	t_{hSC}	SEND	R/TC = "H"	1	–	–	µs
DATAIN Setup Time	t_{SDC}	DATAIN	R/TC = "H"	1	–	–	µs
DATAIN Hold Time	t_{hDC}	DATAIN	R/TC = "H"	1	–	–	µs
MSKOUT Output Delay Time 1	t_{dCM1}	MSKOUT	R/TC = "H"	–	–	10	µs
MSKOUT Output Delay Time 2	t_{dCM2}	MSKOUT	R/TC = "H"	–	–	10	µs
BPFIN Invalid Time	t_{dRB}	BPFIN		0	–	10	ms
Pull–in Bit Number	N	–	R/TC = "L", DPLLC = "L", BPFIN: No noise	–	–	15	bit
Demodulator Delay Time	t_{dBD}	DATAOUT	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	1483	1900	2317	µs
DATAOUT Timing	t_{dCD}	DATAOUT	R/TC = "L"	–1	–	1	µs
Receive Clock High Width	t_{wHC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
Receive Clock Low Width	t_{wLC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
RESET Low Width	t_{wLR}	RESET		20	–	–	µs
MSKOUT Output Delay Time 3	t_{dRM}	MSKOUT		0	–	10	µs
Transmit Clock Delay Time 4	t_{dTC4}	CLOCK		0	–	2	µs
Receive Clock Delay Time 1	t_{dRC1}	CLOCK		0	–	2	µs

TYPICAL CONNECTION EXAMPLE

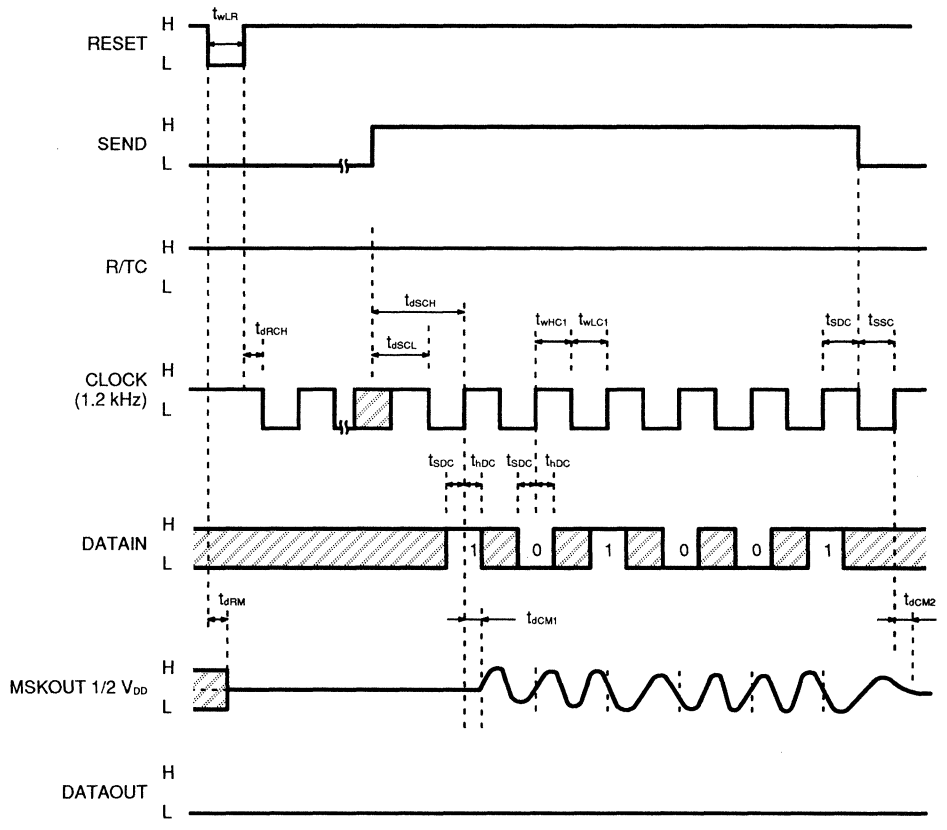


BPF FREQUENCY CHARACTERISTICS



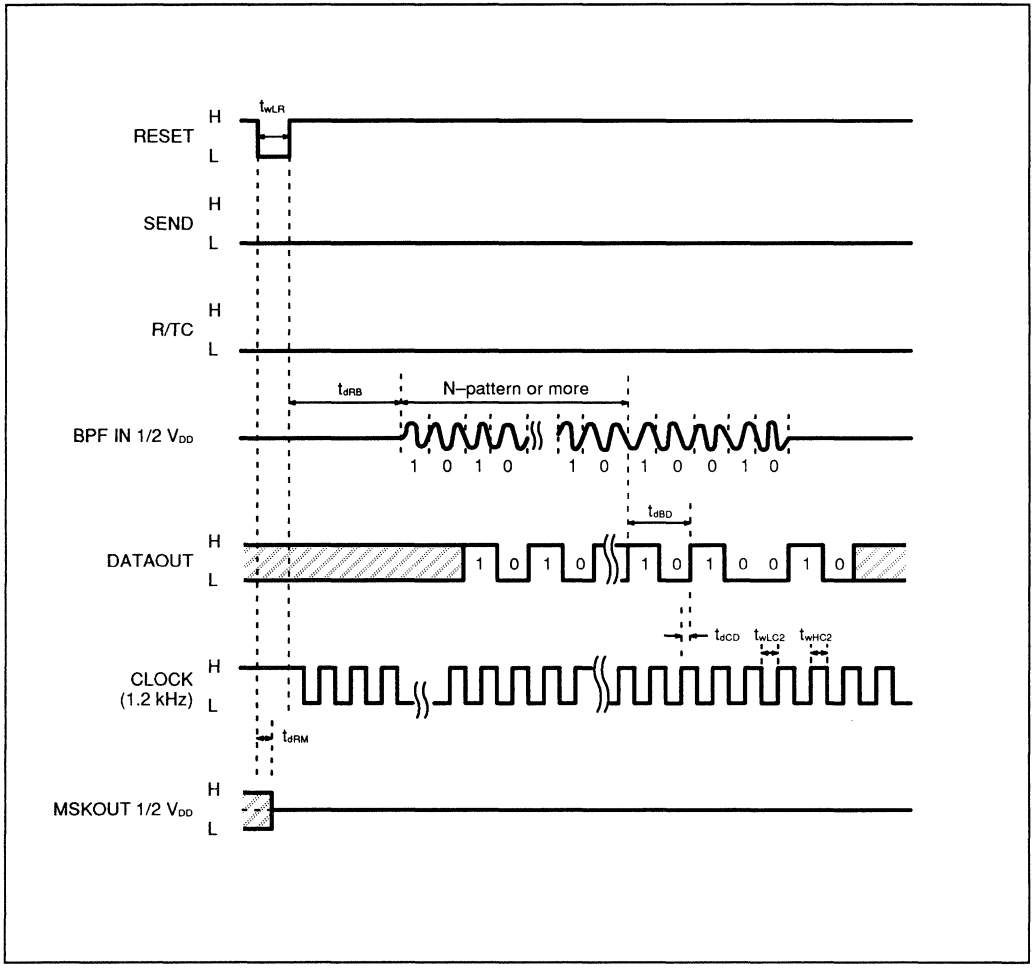
TIMING CHART

Modulator timing chart (TEST pin = High or Open)



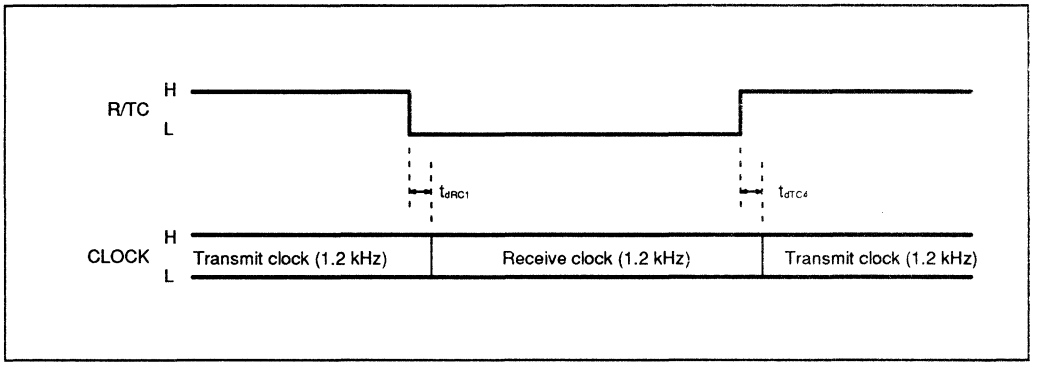
NOTE: 1. SEND pin is pulled high after low–to–high transition of the RESET pin.
2. DATAIN signal is read at the rising edge of the CLOCK.
3. When SEND pin changes from low to high, the CLOCK pin is pulled high once. Then 1.2 kHz clock is output.
4. When R/TC pin is pulled high, DATAOUT pin outputs low.
5. When power is first applied, RESET pin must be set to low to reset all circuits before use.

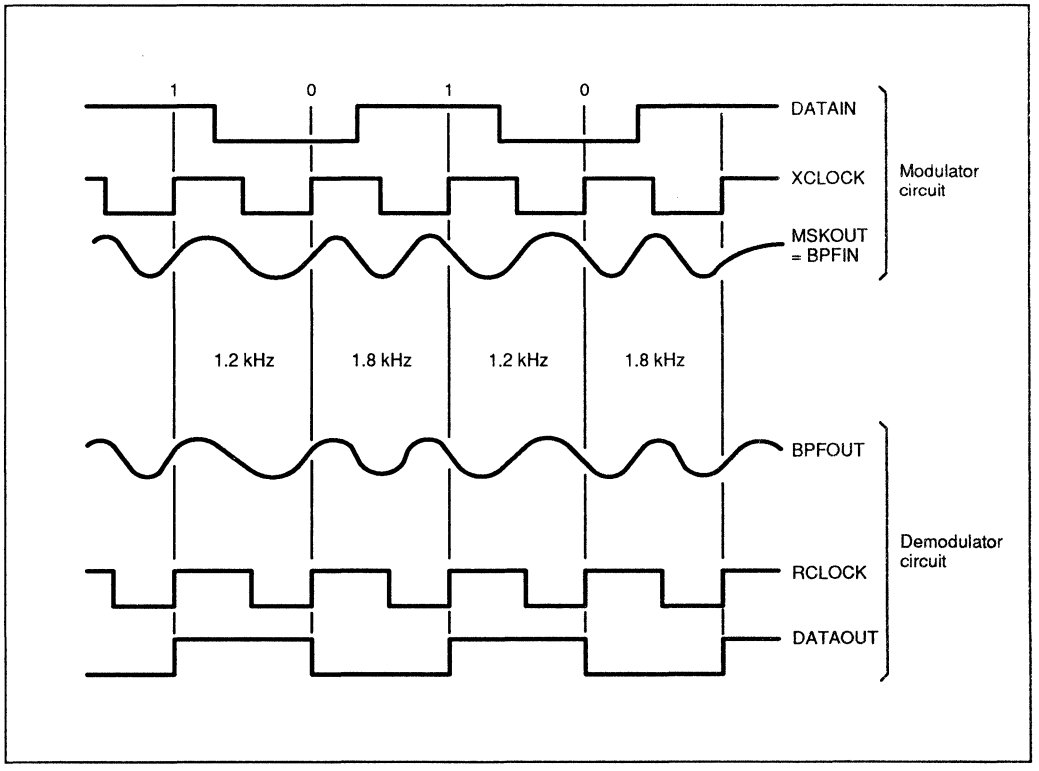
Demodulator timing chart (TEST pin = High or Open)



NOTE: 1. DATAOUT is output synchronized with the rising edge of the CLOCK.
2. When demodulator section is used, SEND pin must be set to high or low. When SEND pin is set to low, MSKOUT is fixed to 1/2 V_{DD}.
3. When power is first applied, RESET pin must be set to low to reset all circuits before use.

Clock output timing chart

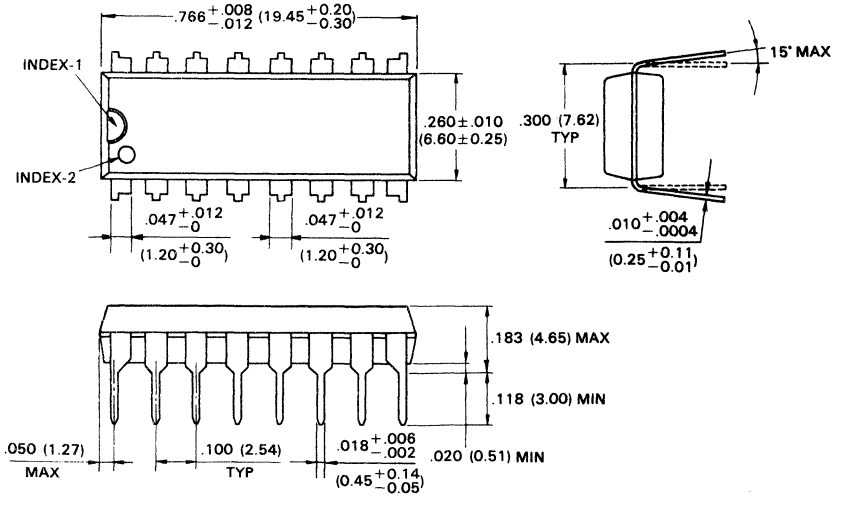




6

PACKAGE DIMENSIONS

Plastic DIP, 16 pins
(DIP–16P–M03)



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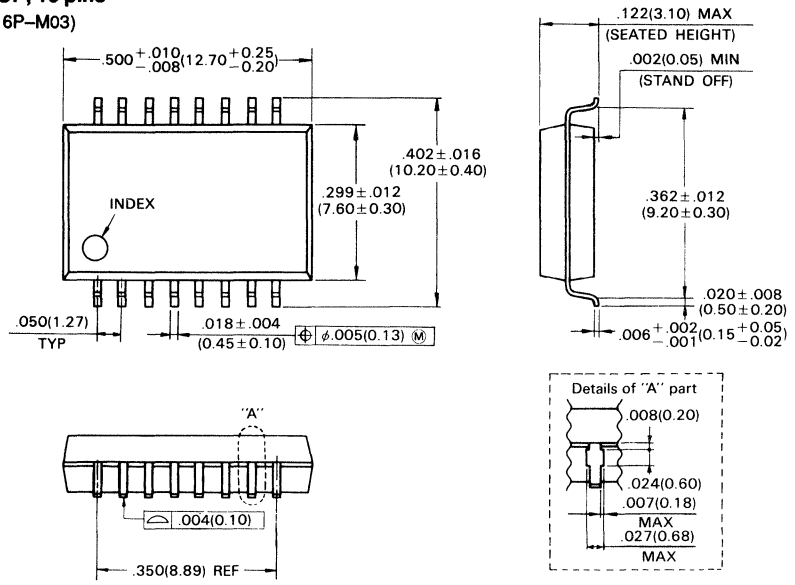
Units: mm (inches)

6

Plastic SOP, 16 pins
(FPT–16P–M03)



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Units: mm (inches)

6

Section 7

Telephone Integrated Circuits — *At a Glance*

Page	Device	Description	Package Options		
7–3	MB3120	Compandor IC	16-pin 17-pin	Plastic Plastic	FPT ZIP
7–15	MB3121	Compandor IC	28-pin	Plastic	FPT
7–19	MB4513	Telephone Amplifier/Tone Ringer	48-pin	Plastic	DIP, FPT
7–31	MB4518	Telecommunication Circuit	28–pin	Plastic	DIP, FPT
7–47	MB4752A	Subscriber Line Interface IC	28-pad	Ceramic	LCC
7–57	MB87007A MB87008A	Dual Tone Multifrequency Pulse Dialer	18-pin 24-pin	Plastic Plastic	DIP FPT
7–83	MB87009	Dual Tone Multifrequency Pulse Dialer	20-pin	Plastic	FPT
7–111	MB87017B	Dual Tone Multifrequency Receiver	18-pin 24-pin	Plastic Plastic	DIP FPT
7–123	MB87029	Dual Tone Multifrequency Pulse Dialer	22-pin 24-pin	Plastic Plastic	DIP FPT
7–149	MB87057	Dual Tone Multifrequency Receiver	18-pin 24-pin	Plastic Plastic	DIP FPT

7

April 1990
Edition 2.0

FUJITSU

DATA SHEET

MB3120
COMPANDOR IC

COMPANDOR IC

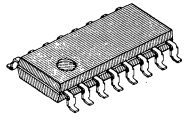
The Fujitsu MB3120 is a compandor IC to expand dynamic range at transmission/reception systems and to improve the tone quality by means of restricting noise.

Two functions are loaded on one IC, the one is the compressor which has the 2/1 ratio of input/output ratio by logarithm, and the expandor which has the 1/2 ratio of input/output ratio by logarithm.

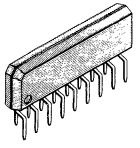
The MB3120 is encapsulated in a small package. This enables high density mounting.

The MB3120 is well suitable for a mobile radio system like as cellular radio, MCA and handy telephone set.

- Wide power supply voltage range (3.2V to 10.0V)
- Low power supply current
- On-chip both compressor and expandor
- Wide dynamic range
- Less external elements
- Inhibit function with compression/expantion ratio of one
- Equipped with mute function which cut off the output signal
- 16-pin Flat Package
  17-pin Zig-zag In-line Package

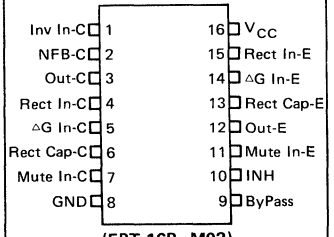


PLASTIC PACKAGE
FPT-16P-M04



PLASTIC PACKAGE
ZIP-17P-M01

PIN ASSIGNMENT
(TOP VIEW)



(FPT-16P–M02)

ZIP-17P-M01 Pin Assignment
Please See Page 12

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_A = 25°C)

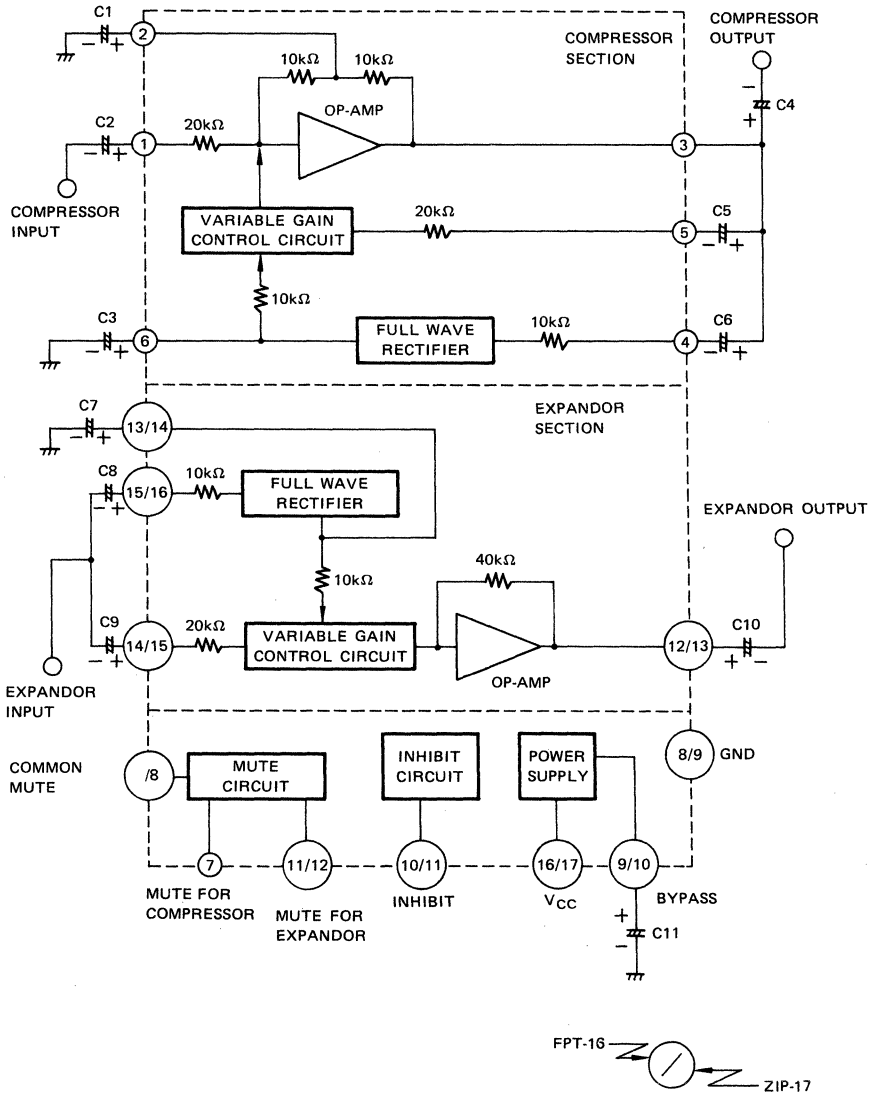
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	V
Mute Control Voltage	V_{MUTE}	5*	V
Inhibit Control Voltage	V_{INH}	5*	V
Power Dissipation	P_D	560	mW
Operating Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +125	°C

*: This value takes V_{CC} when V_{CC} is less than 5V.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB3120 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

C_1 : C_1 determines the low cut off frequency of compressor section.

$$fc = \frac{1}{2\pi R \cdot C_1}$$

R is on chip feed back resistor (10kΩ typ.)

C_2, C_8, C_9 : Input coupling condenser

C_3, C_7 : Smooth capacitor of full wave rectifier. Atack time and recovery time are determined by C_3 and C_7.
Time constant T_C can be calculated.
T_C (ms) ≒ 10 x C_3 (μF)

C_4, C_{10} : Output coupling condenser

C_5, C_6 : Coupling condenser for internal feed back of compressor section.

C_{11} : Ripple filter condenser

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.2		10	V
Operating Temperature	T_A	-20		75	°C

7

ELECTRICAL CHARACTERISTICS

(V_{CC} = 8V, T_A = 25°C, f = 1kHz, R_L = 10kΩ)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			3.0	4.5	mA

Compressor

Input Resistance	R_{INC}		14	20		kΩ
Input Reference Level	V_{OCO}	V_{IN} = -6dBm	-10.5	-9.0	-7.5	dBm
		V_{IN} = -6dBm, T_A = -20 to 75°C*2	-2.5	0	2.5	dB
Output Level*1	V_{OC1}	V_{IN} = -20dB	-10.5	-10.0	-9.5	dB
	V_{OC2}	V_{IN} = -40dB	-20.7	-20.0	-19.3	dB
	V_{OC3}	V_{IN} = -60dB	-31.5	-30.0	-29.0	dB
		V_{IN} = -60dB, T_A = -20 to 75°C*2	-4.0	0	3.0	dB
	V_{OC4}	V_{IN} = -80dB		-40.0		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Expandor						
Input Resistance	R_{INE}		4.7	6.7		kΩ
Input Reference Level	V_{OE0}	V_{IN} = -9dBm	-1.5	0	1.5	dBm
		V_{IN} = -9dBm, T_A = -20 to 75°C*2	-2.5	0	2.5	dB
Output Level*1	V_{OE1}	V_{IN} = -10dB	-20.5	-20.0	-19.5	dB
	V_{OE2}	V_{IN} = -20dB	-40.7	-40.0	-39.3	dB
	V_{OE3}	V_{IN} = -30dB	-61.0	-60.0	-58.5	dB
		V_{IN} = -30dB, T_A = -20 to 75°C*2	-3.0	0	4.5	dB
	V_{OE4}	V_{IN} = -40dB		-80.0		dB
Compandor						
Total Harmonic Distortion	THD	V_O = 0dBm		0.5	2.0	%
Output Noise Voltage	V_{ON}	BW = 100Hz to 5kHz			-80.0	dBm
Voltage Gain	A_V	V_{IN} = -6dBm	4.5	6.0	7.5	dB
Gain Deviation 1	ΔA_{V1}	V_{IN} = -6dBm, T_A = -20 to 75°C*2	-3.0	0	3.0	dB
Gain Deviation 2	ΔA_{V2}	f = 200Hz to 5kHz, V_{OI} = 0dBm	-0.5	0	0.5	dB
Voltage Gain at Inhibit	A_{VINH}	V_{IN} = -6dBm, V_{ININH} = 0.4V	4.5	6.0	7.5	dB
Compressor Mute Attenuation*3	V_{OCMUTE}	V_{IN} = -6dBm, $V_{INCMUTE}$ = 2.7V		-50		dBm
Expandor Mute Attenuation*3	V_{OEMUTE}	V_{IN} = -9dBm, $V_{INEMUTE}$ = 2.7V		-70		dBm
High-level Control Voltage for Mute and Inhibit Pins*3	V_{IH}		2.7			V
Low-level Control Voltage for Mute and Inhibit Pins*3	V_{IL}				0.4	V

Notes:

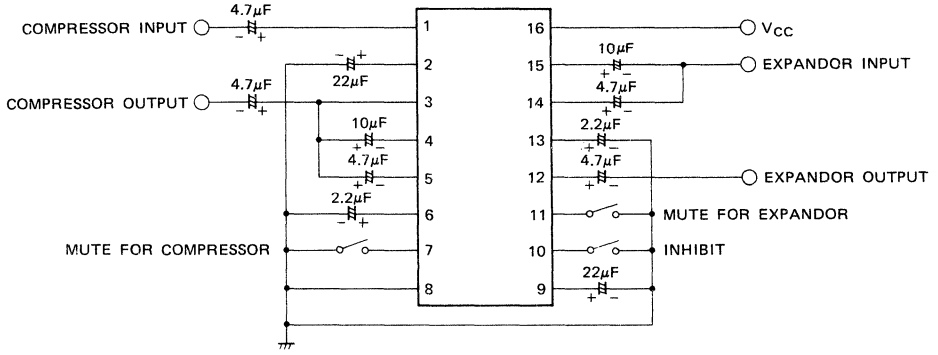
*1 Measured at input reference level of 0dB.

*2 Gain deviation with temperature when output level of 25°C is specified as 0dB.

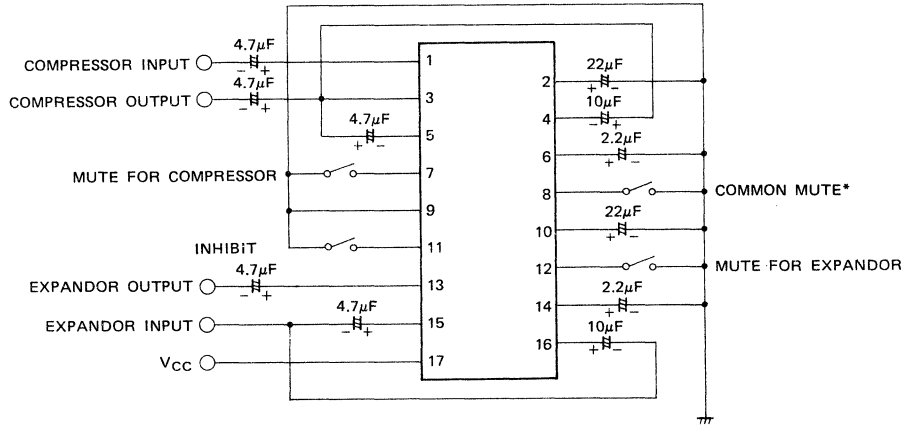
*3 As for Zip-17 pin, both compressor and expandor circuit enter mute function depending on 8 pin input.

TYPICAL CONNECTION EXAMPLE

FPT-16



ZIP-17



*: Both the mute of Compressor and Expandor can be controlled by this terminal.

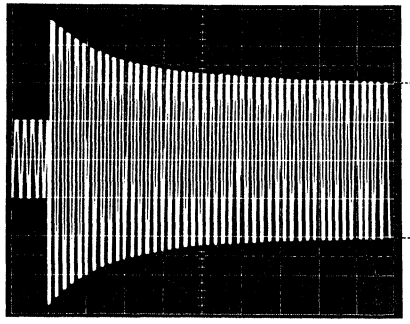
7

OUTPUT TRANSITION RESPONSE CHARACTERISTICS

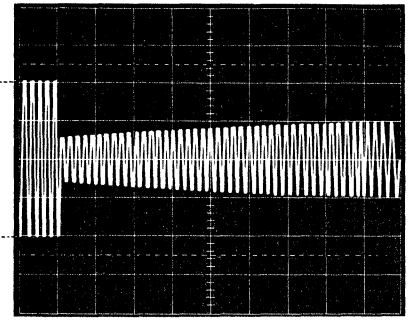
Condition: V_{CC} = 8V, f = 1kHz, R_L = 10kΩ, Mute OFF, INH OFF, Typ. connection

COMPRESSOR (Y: 0.2V/div, X: 5msec/div)

V_{IN} = −18dBm → −6dBm (V_O = −15dBm → −9dBm)

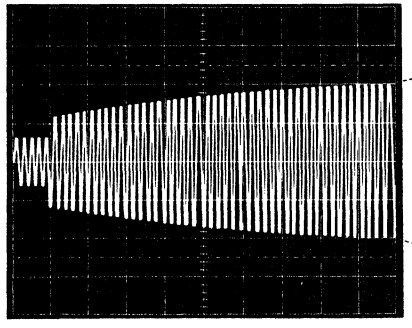


V_{IN} = −6dBm → −18dBm (V_O = −9dBm → −15dBm)

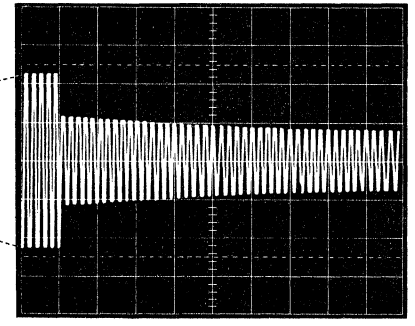


EXPANDOR (Y: 0.5V/div, X: 5msec/div)

V_{IN} = −15dBm → −9dBm (V_O = −12dBm → 0dBm)

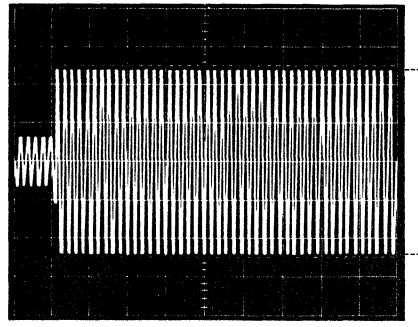


V_{IN} = −9dBm → −15dBm (V_O = 0dBm → −12dBm)

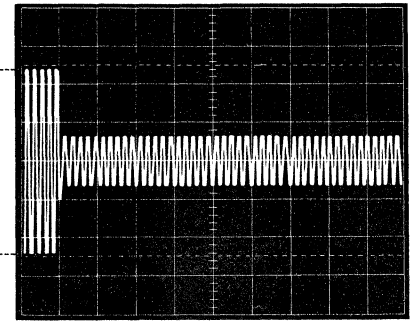


COMPANDOR (Y: 0.5V/div, X: 5msec/div)

V_{IN} = −18dBm → −6dBm (V_O = −12dBm → 0dBm)



V_{IN} = −6dBm → −18dBm (V_O = 0dBm → −12dBm)



7

TYPICAL CHARACTERISTICS CURVES

Fig. 1 – INPUT VOLTAGE vs. OUTPUT LEVEL

f = 1kHz
Mute OFF
INH OFF
Rg = 600Ω
R_L = 10kΩ
TYP. CONNECTION

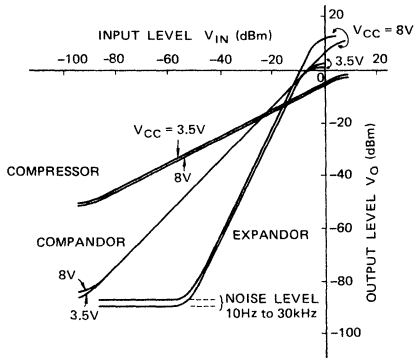


Fig. 2 – INPUT VOLTAGE vs. OUTPUT LEVEL (INHIBIT COND.)

f = 1kHz
Mute OFF
INH ON
Rg = 600Ω
R_L = 10kΩ
TYP. CONNECTION

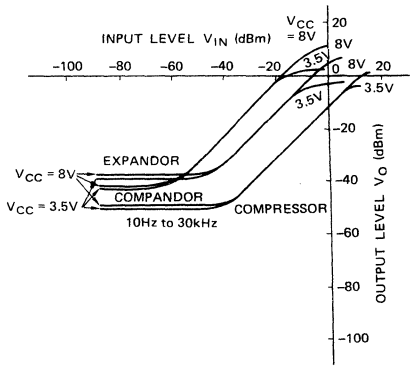


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Fig. 3 – INPUT REFERENCE LEVEL vs. VOLTAGE SUPPLY

f = 1kHz
Mute OFF
INH OFF ------ R_L = 600Ω
Rg = 600Ω —— R_L = 10kΩ

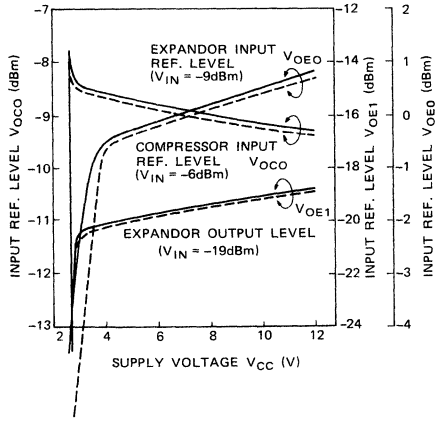
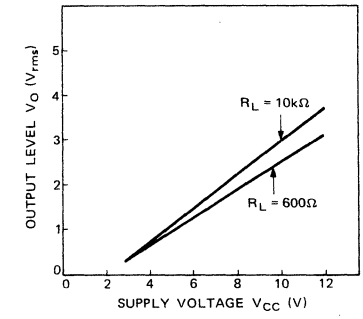


Fig. 4 – MAX. OUTPUT LEVEL vs. SUPPLY VOLTAGE (COMPANDOR)

LPF: 100kHz
THD = 1% INH OFF
Mute OFF Rg = 600Ω



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 5 – FREQUENCY vs. VOLTAGE GAIN (COMPANDOR)

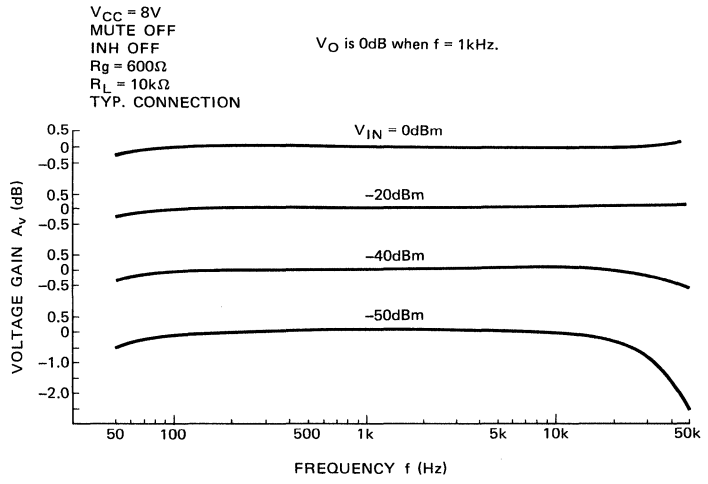


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Fig. 6 – INPUT REFERENCE LEVEL vs. TEMPERATURE

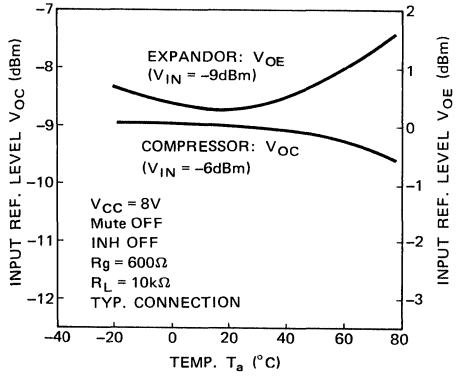
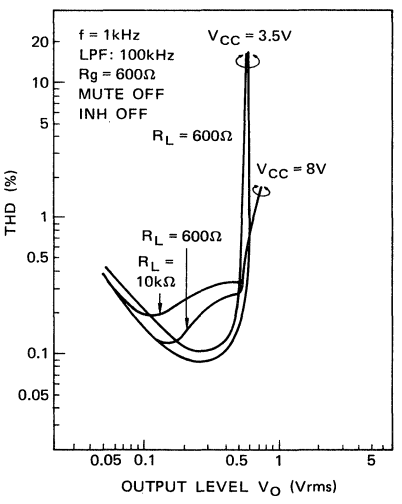


Fig. 7 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPRESSOR)



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 8 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (EXPANDOR)

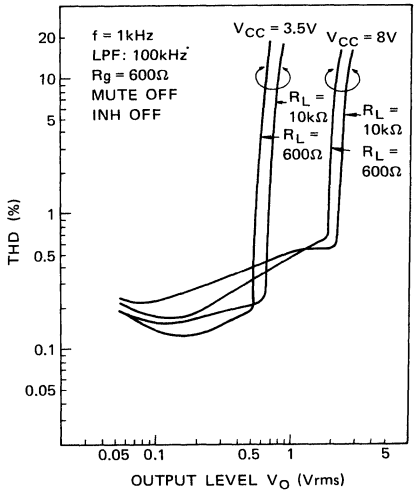


Fig. 9 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPANDOR)

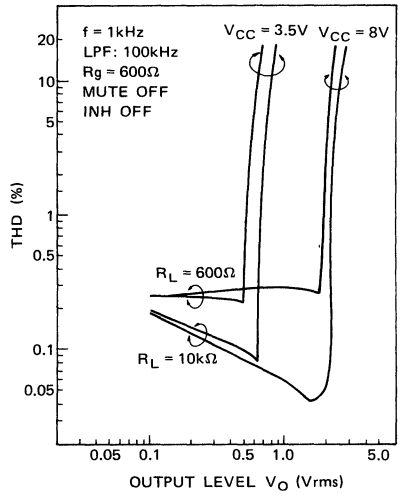


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Fig. 10 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (EXPANDOR INHIBIT COND.)

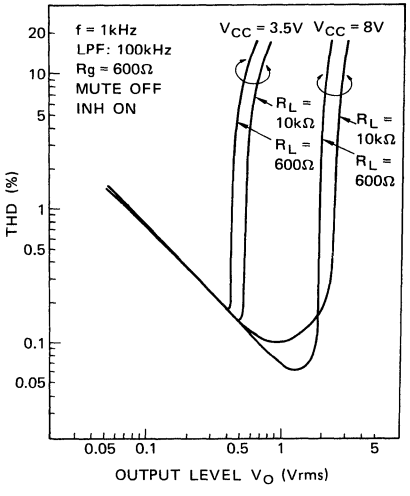
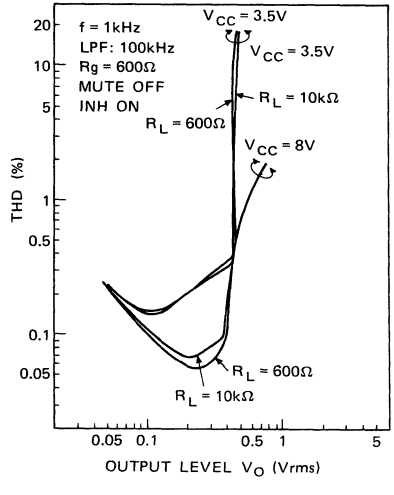


Fig. 11 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPRESSOR INHIBIT COND.)



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 12 – FREQUENCY vs. TOTAL HARMONIC DISTORTION (COMPANDOR)

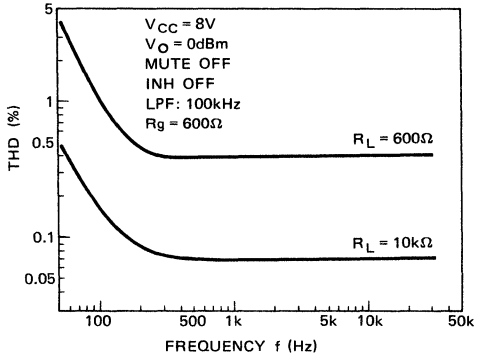


Fig. 13 – EXAPNDOR MUTE ATTENUATION

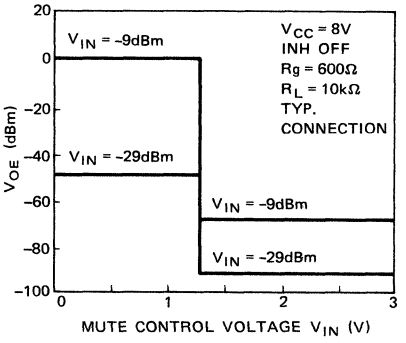
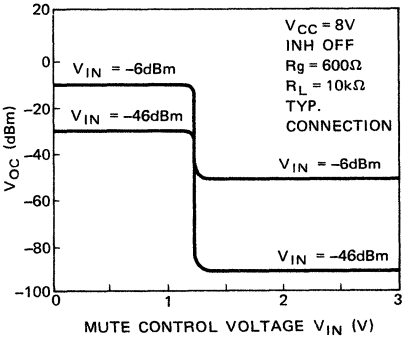
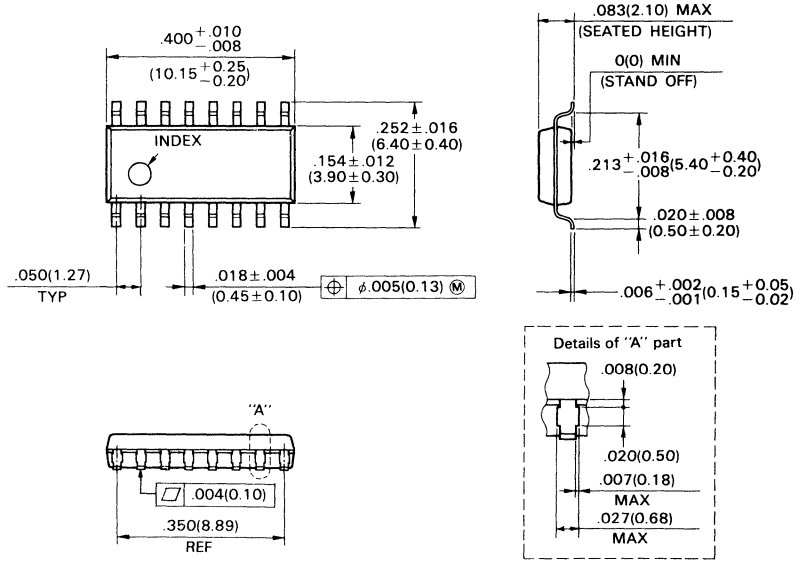


Fig. 14 – COMPRESSOR MUTE ATTENUATION



PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M04)



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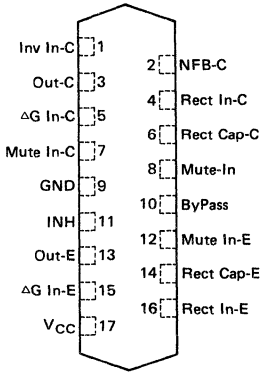
Dimensions in
inches (millimeters)

7

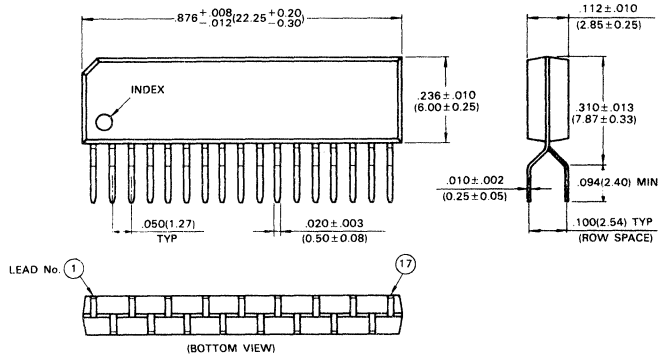
PACKAGE DIMENSIONS (Continued)

(TOP VIEW)



(ZIP-17P-M01)

17-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-17P-M01)



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Dimensions in
inches (millimeters)

7

DATA SHEET

FUJITSU

MB3121
Compandor IC

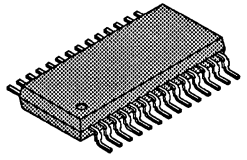
The Fujitsu MB3121 is a highly functional compandor IC with on-chip support circuitry that includes a microphone amplifier, input amplifier, and a splatter filter amplifier. It also features low operating voltage and low power consumption.

The MB3121 is designed to improve the sound quality in transceiver systems by increasing the dynamic range of the voice signal and suppressing noise. This device incorporates a signal compression circuit having an input/output compression ratio of 1/2*log (I/O) and an expandor circuit with an input/output expansion ratio of 2*log (I/O).

The MB3121 is the ideal choice for application in portable/mobile equipment such as car phones and cordless telephones.

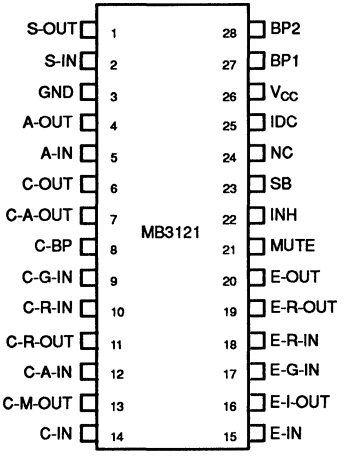
- Low voltage operation: 1.8 to 7 V
- Compressor and expandor circuitry
- Adjustable voltage gain (0 to 40 dB)
- Limiter circuit
- Amplifier circuit for use with a splatter filter
- Data input and output pins
- Output signal muting function
- INHIBIT function that sets the compression and expansion ratio to 1:1
- STANDBY mode
- 28-pin plastic SOP

PRELIMINARY



FPT-28P-M01

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	1.8 to 7 (Typical = 3)	V
Operating Temperature	T_a	−20 to +75	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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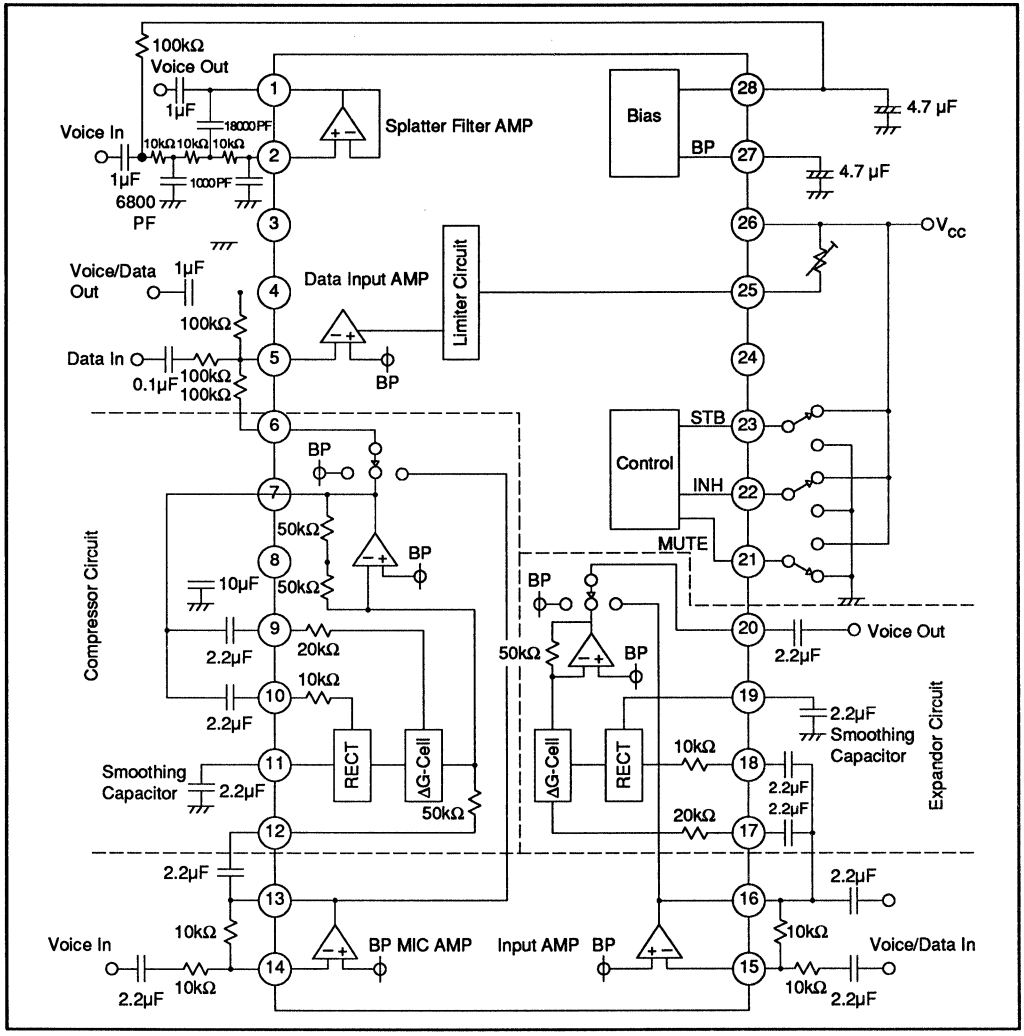
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply Current		I_{CC}	No Signal Applied	—	3.3	5.0	mA
Supply Current, STANDBY Mode		I_{SB}	V_{SB} = 0 V	—	0.1	10.0	µA
Compressor	Input/Output Reference Level	V_{OC1}	V_{in} = 100 mV_{rms}	–20.8	–17.8	–14.8	dBm
	Output Level	V_{OC11}	V_{in} = –20 dB	–10.5	–10.0	–9.5	dB
	Output Level	V_{OC12}	V_{in} = –40 dB	–21.0	–20.0	–19.0	dB
	Input Limiting Voltage	V_{LIM}	V_{in} = +14 dB	—	550	—	mV_{P-P}
	MUTE Attenuation	ATT_C	V_{in} = 0 dB BW = 200 Hz to 5 kHz	60	80	—	dB
Expandor	Input/Output Reference Level	V_{OC1}	V_{in} = 100 mV_{rms}	–20.8	–17.8	–14.8	dBm
	Output Level	V_{OC11}	V_{in} = –20 dB	–41.0	–40.0	–39.0	
	Output Level	V_{OC12}	V_{in} = –40 dB	–65.0	–63.0	–60.0	dB
	Maximum Output Voltage	V_{0m1}	THD = 2%	500	700	—	mV
	MUTE Attenuation	ATT_C	V_{in} = 0 dB BW = 200 Hz to 5 kHz	60	80	—	dB
Compandor	Output Noise Voltage	V_{OX}	R_L = 0Ω BW = 200 Hz to 5 kHz	—	10	—	µV
	Total Harmonic Distortion	THD	V_{OC1} = 100 mV_{rms}	—	0.5	1.5	%
	Voltage Gain	A_V	V_{in} = 100 mV_{rms}	–1.5	0.0	1.5	dB
Amplifiers	Open Circuit Voltage Gain	A_{VO}	—	40	50	—	dB
	Maximum Output Voltage	A_{OM2}	THD = 2%	500	700	—	mV
Filter	Filter Gain	AVF1	V_{in} = 100 mV_{rms} (typ) f = 1 kHz	–0.5	0.0	0.5	dB
	Filter Gain	AVF2	f = 3 kHz	–3.5	–3.0	–2.5	dB
	Filter Gain	AVF3	f = 30 kHz	–65.0	–60.0	–55.0	dB
STANDBY (SB)		V_{SBH}	Normal	1.0	—	V_{CC}	V
Pin Control Voltage		V_{SBL}	In STANDBY	0.0	—	0.3	V
MUTE		V_{MUTED}	Muted	0.8	—	V_{CC}	V
Pin Control Voltage		V_{MUTEL}	Normal	0.0	—	0.2	V
INHIBIT (INH)		V_{INHH}	Normal	0.8	—	V_{CC}	V
Pin Control Voltage		V_{INHL}	Compression/Expansion Inhibited	0.0	—	0.2	V

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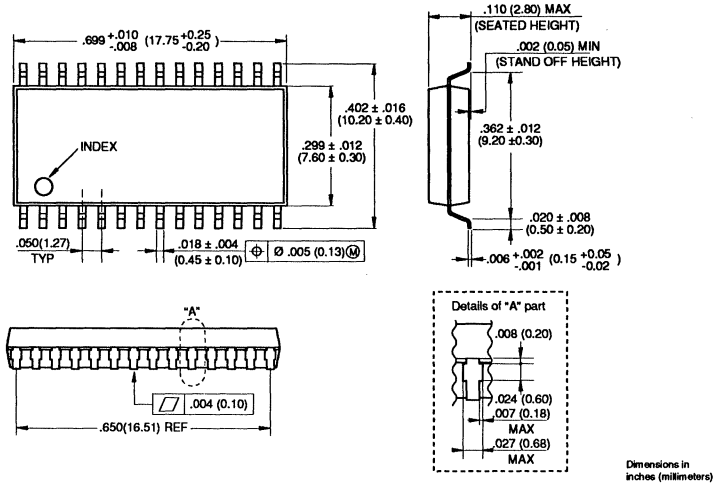
28-Lead Plastic Flat Package
(Case No.:FPT-28P-M01)



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June 1990
Edition 2.0

FUJITSU

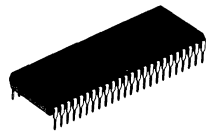
DATA SHEET

MB4513
TELEPHONE IC

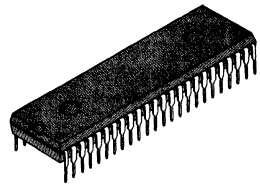
TELEPHONE IC
(SPEECH NETWORK, TONE RINGER, FILTER)

The Fujitsu MB4513 has an on–chip speech network circuit, filter circuit, and toneringer circuit. The MB4513 is intended to be used with dialer IC's (MB87003/4, MB87007A/8A, MB87029) to produce a telephone which can be connected to a rotary dial line or push button line.

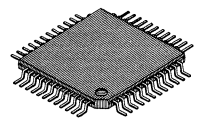
- On-chip speech network circuit, filter circuit and tone ringer circuit
- Uses a ceramic piezoelectronic transmitter and receiver
- Reception amplifier adopts BTL (Balanced Transformer Less) circuit
- Three selections of tone by the external switches
- Connectable to pulse or DTMF lines



PLASTIC PACKAGE
DIP–48P–M01



PLASTIC PACKAGE
DIP–48P–M02



PLASTIC PACKAGE
FPT–48P–M02

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Speech	Supply Voltage	V_L	20	V
	Supply Current	I_L	150	mA
Tone Ringer	Supply Voltage	V_{TR}	20	V
	Supply current	I_{TR}	7	mA
Operating Ambient Temperature		T_A	–30 to 60	°C
Storage Temperature		T_{STG}	–55 to 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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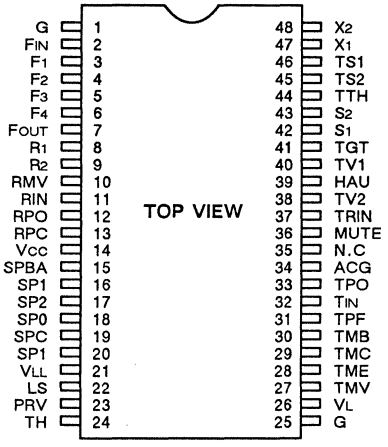
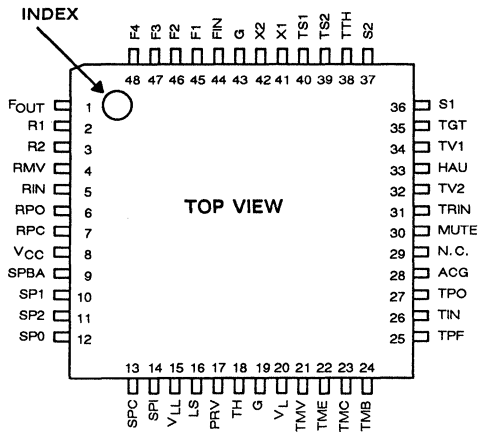
PIN ASSIGNMENT



(DIP-48P-M01)
(DIP-48P-M02)



(FPT-48P-M02)

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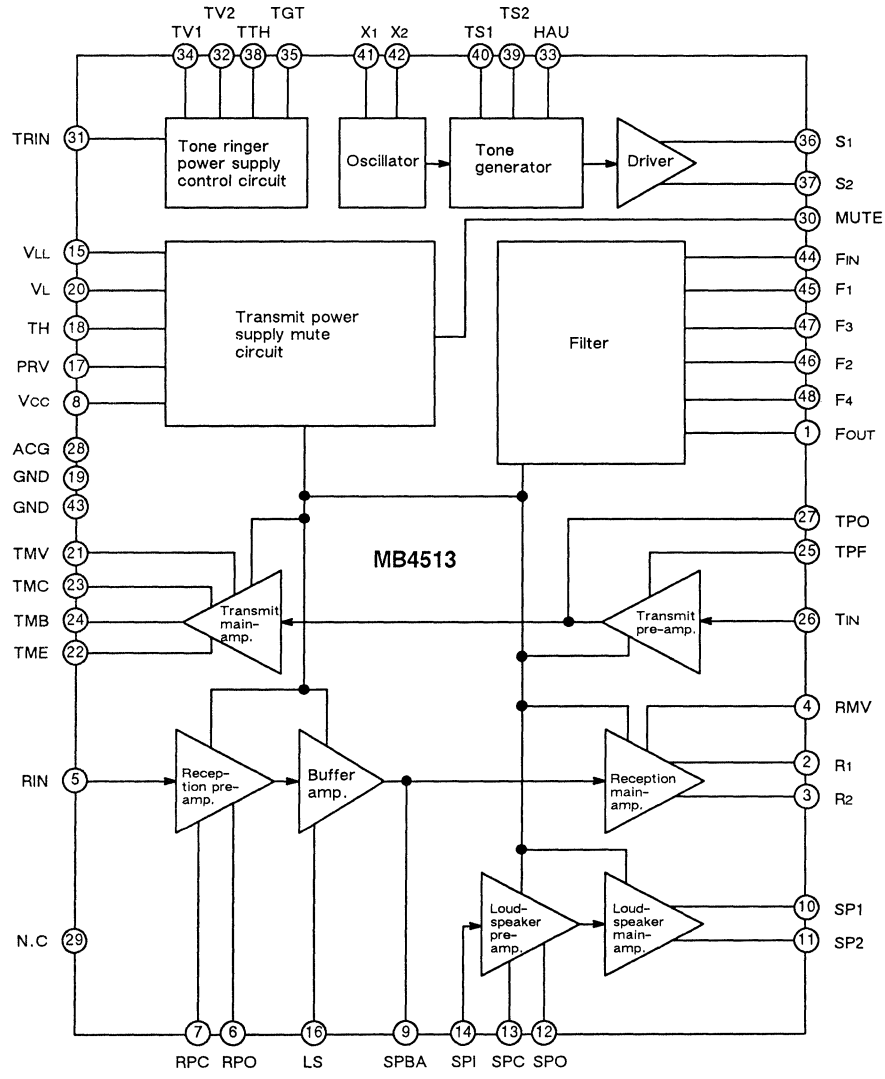
BLOCK DIAGRAM



Note : The pin numbers correspond to QFP package.

7

DC CHARACTERISTICS

(T_A = 25 °C)

Parameter	Symbol	Condition		Values			Unit
			I_L (mA)	Min	Typ	Max	
V_L Voltage	V_L	MUTE: OFF	20	1.9	2.7	3.9	V
			90	5.0	6.2	7.5	V
V_L Voltage	V_L	MUTE: ON	20	2.2	3.2	4.4	V
			90	5.3	6.5	8.0	V
Supply Voltage	V_{CC}	During Speech	20	1.4	1.7	2.0	V

AC CHARACTERISTICS

(T_A = 25 °C)

Parameter	Symbol	Condition			Values			Unit
			I_L (mA)	Freq (kHz)	Min	Typ	Max	
AC Impedance	Z_{TEL}		30	1.0	400	600	800	Ω
			90	1.0				
Transmit Voltage Gain	G_{TV}	V_{IN} = -50 dBm	30	1.0	42	45	48	dB
Transmit Dynamic Range	V_{TD}	DIS > -20 dB	30	1.0	-2	2.5		dBV
			90	1.0	0	8		
Reception Voltage Gain	G_{RV}	V_{IN} = -50 dBm	30	1.0	38	43	46	dB
Reception Dynamic Range	V_{RD}	DIS > -20 dB	30	1.0	-3	4		dBV
			90	1.0	-1.0	7		
Reception Pad Loss	L_{RP}	V_{IN} = -50 dBm $L_{RP} = G_{RV}$ (30mA) $-G_{RV}$ (90mA)	30	1.0	3	6	9	dB
			90	1.0				
Speaker Gain	G_{SV}	V_{IN} = -70 dBm	30	1.0	61	67	73	dB
Speaker Dynamic Range	V_{SD}	DIS > -20 dB	30	1.0	3	8		dBV

AC CHARACTERISTICS (Cont'd)

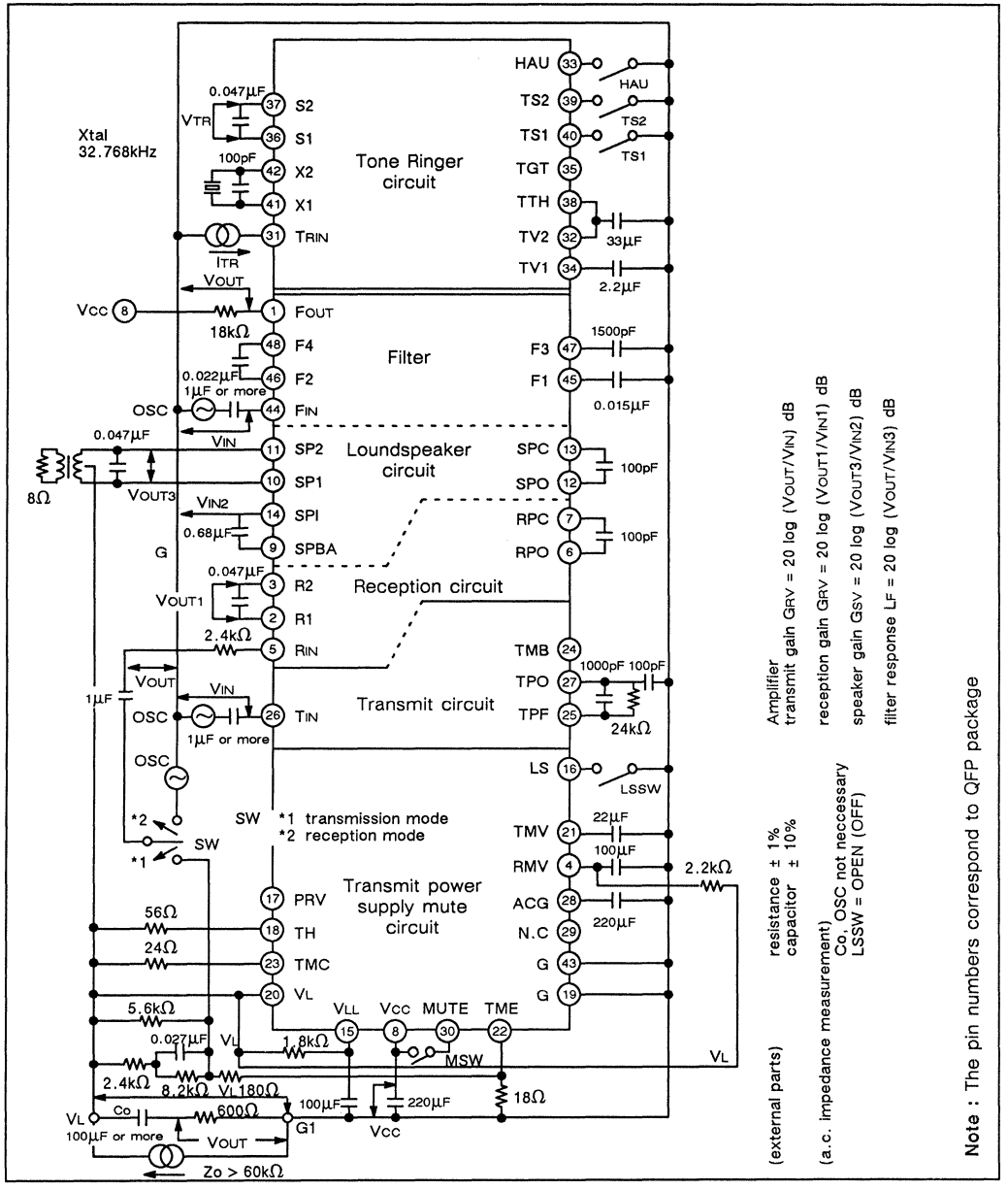
Parameter	Symbol	Condition			Values			Unit
			I_L (mA)	Freq (kHz)	Min	Typ	Max	
Filter Input * Output Characteristics	LF1	V_{IN} = -40 dBm	30	0.5	17	20	23	dB
	LF2			1.0	17	20	23	
	LF3			3.0		12	20	
	LF4			6.0		-7	5	
	LF5			12.0		-21	-9	
Tone Ringer Start Current	I_{TR}	Load = 47 nF			1.0	1.7	30	mA
Tone Ringer Output Voltage	V_{TR}	Load = 47 nF I_{TR} = 5 mA			19	21		dBV

Tone Ringer Tone **		Load = 47 nF I_{TR} = 5mA	HAU	TS1	TS2	Tone
	F1		Open	Open	Open	(1024, 819) 8Hz warble frequency
	F2			Close	Open	(1024, 819) 16Hz warble frequency
	F3			Open	Close	(1024, 1365) 8Hz warble frequency
	F4			Close	Close	1024
	F5		Close			(1024, 1365) 8Hz warble frequency

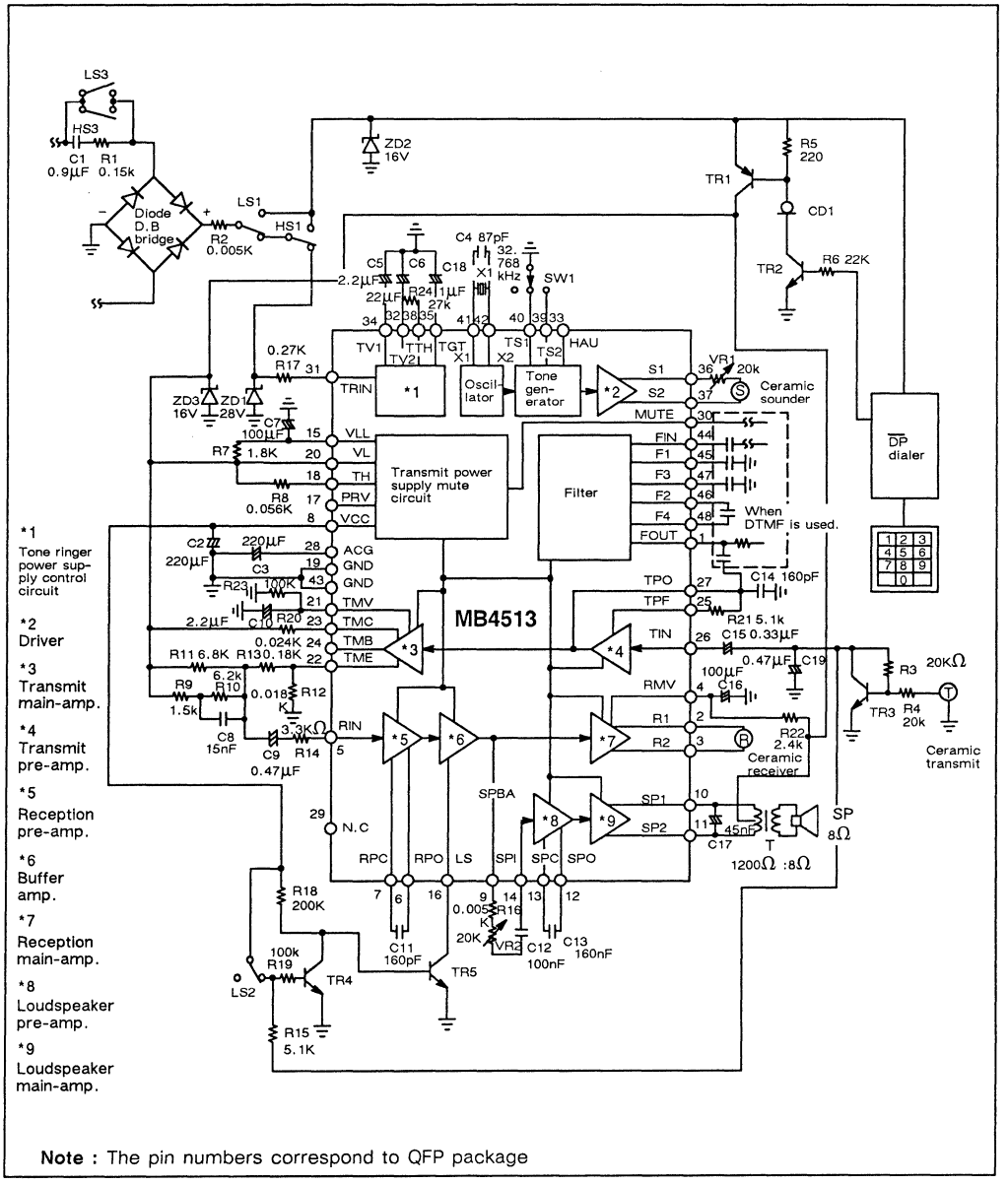
Note : * LF VOUT - VIN
: ** Provides a tone signal that shifts between warble frequency at 8Hz or 16Hz.

7

MEASUREMENT CIRCUIT



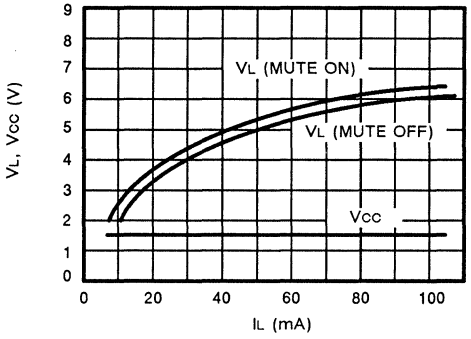
APPLICATION CIRCUIT



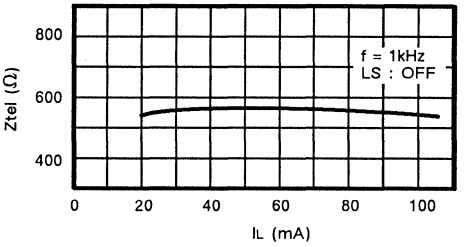
Note : The pin numbers correspond to QFP package

TYPICAL CHARACTERISTICS CURVES

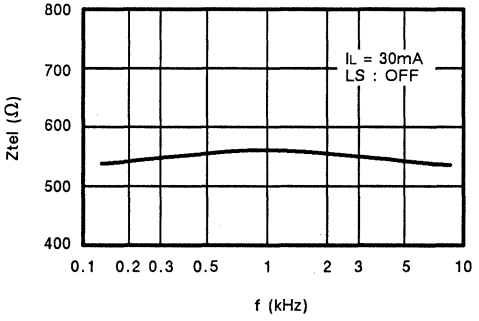
SUPPLY VOLTAGE VS. SUPPLY CURRENT



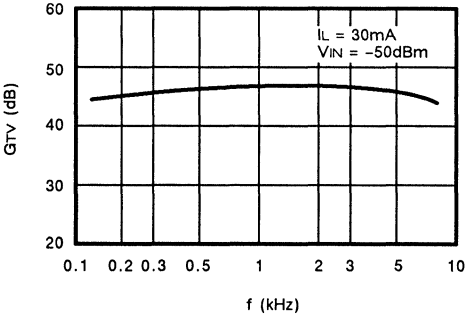
AC IMPEDANCE VS. SUPPLY CURRENT



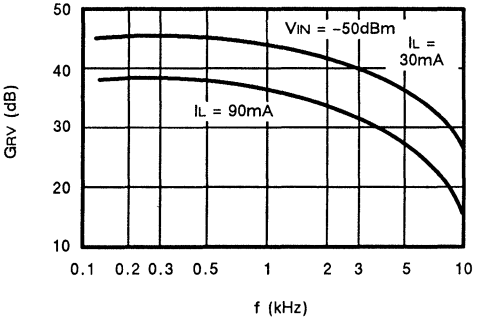
AC IMPEDANCE VS. FREQUENCY



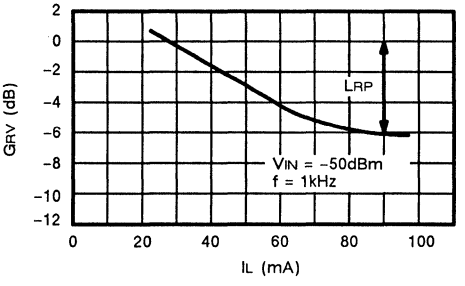
TRANSMIT GAIN VS. FREQUENCY



RECEPTION GAIN VS. FREQUENCY



RECEPTION GAIN VS. SUPPLY CURRENT



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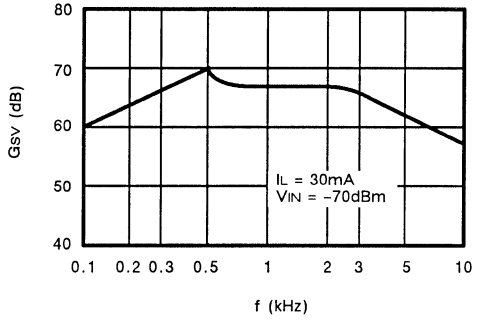
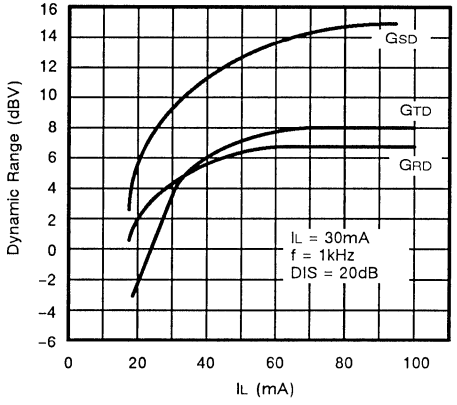
TYPICAL CHARACTERISTICS CURVES

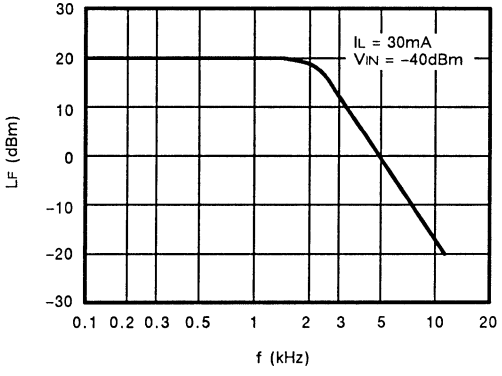
SPEAKER GAIN VS. FREQUENCY



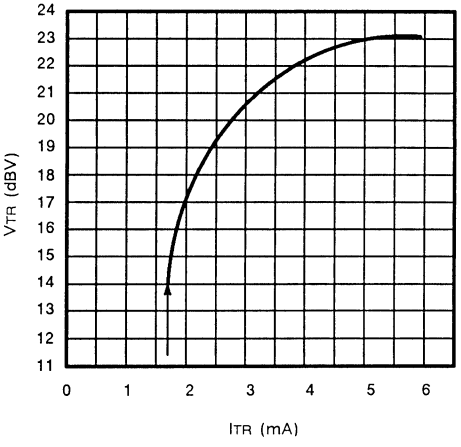
DYNAMIC RANGE VS. SUPPLY CURRENT



FILTER RESPONSE



TONE RINGER OUTPUT VOLTAGE VS. TONE RINGER INPUT CURRENT



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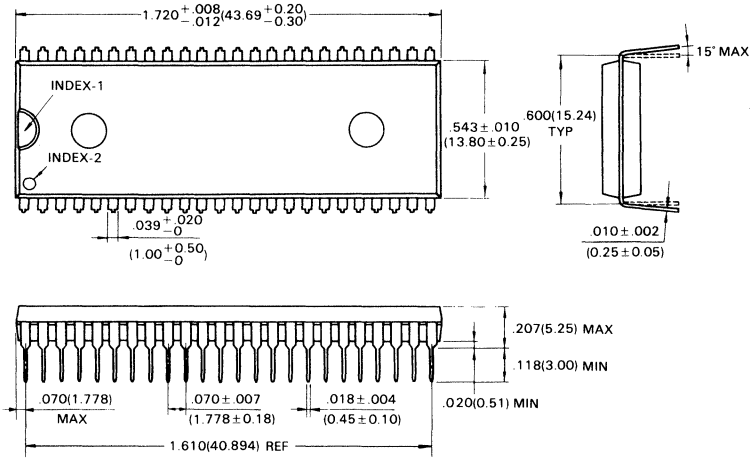
PACKAGE DIMENSIONS

48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M01)



©1988 FUJITSU LIMITED D48002S-3C

Dimensions in inches (millimeters)

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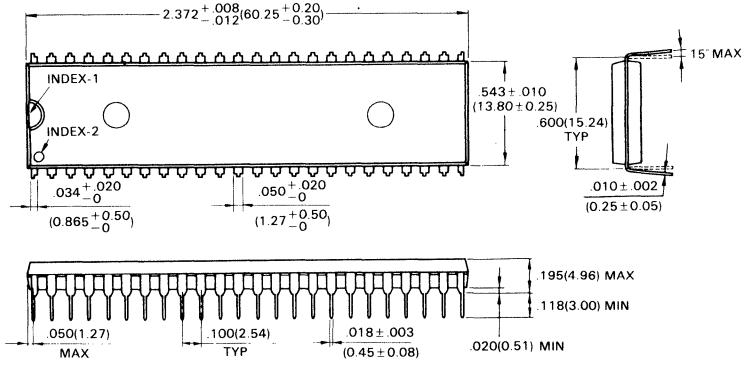
48-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-48P-M02)



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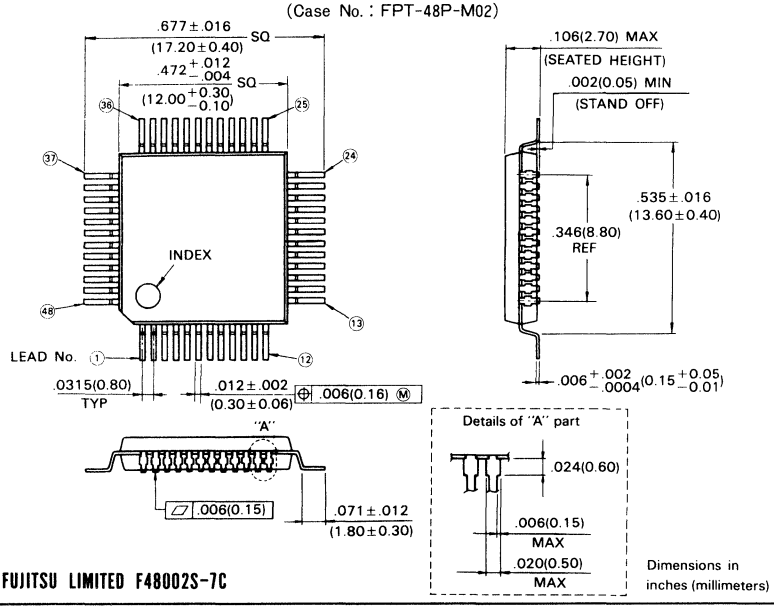
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

48-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-48P-M02)



Dimensions in inches (millimeters)

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April 1991
Edition 1.0

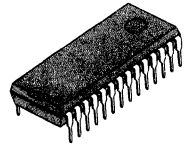
FUJITSU

DATA SHEET

MB4518
TELECOMMUNICATION CIRCUIT

The MB4518 provides many of the major speech circuit functions of the telephone handset. Additional features include a level expander circuit to minimize ambient acoustic noise interference and an on-chip amplifier with speaker-drive capability. Combined with general-purpose dialer and tone-ringer ICs, the MB4518 provides all of the basic handset functions.
The MB4518 easily interfaces with microprocessors designed for telephone handset control to provide microprocessor-controlled speaker level, transmitter muting, and side-tone level adjustments. The sidetone level adjustment circuit detects loop current levels and switches between two balance networks for proper sidetone level.

- On-chip power amplifier drives an 8 Ω speaker
- Transmit level expander
- Simple receive level boost
- Balanced transmitter input for improved noise rejection
- Drives low-impedance receiver (dynamic receiver)
- Switchable balance network for optimum side-tone level
- Loop-current monitoring automatic gain control (automatic pad function)
- Low loop current drain ($I_L \fallingdotseq 5$ mA)
- Superior branching properties
- Gain and frequency characteristics adjustable by external resistor and capacitor.
- Simple telephone microcomputer interface
- Available in 28-pin shrink dip and flat packages



PLASTIC PACKAGE
(DIP-28P-M03)

PLASTIC PACKAGE
(FPT-28P-M01)

ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = +25°C)

Rating	Symbol	Value	Unit
Supply voltage	V_L	18	V
Supply current	I_L	120	mA
Operating temperature range	Top	–30 to +60	°C
Storage temperature range	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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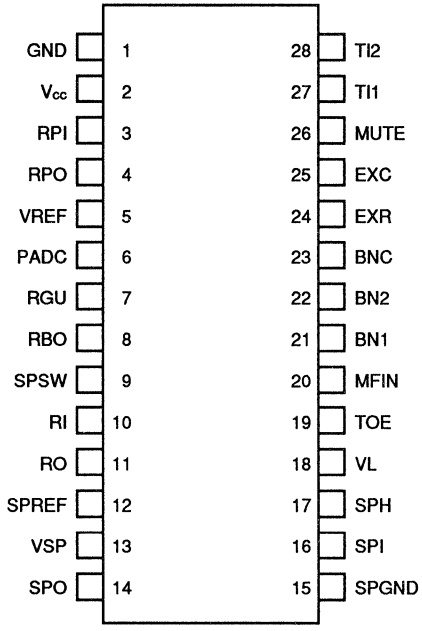
PIN ASSIGNMENT

(TOP VIEW)

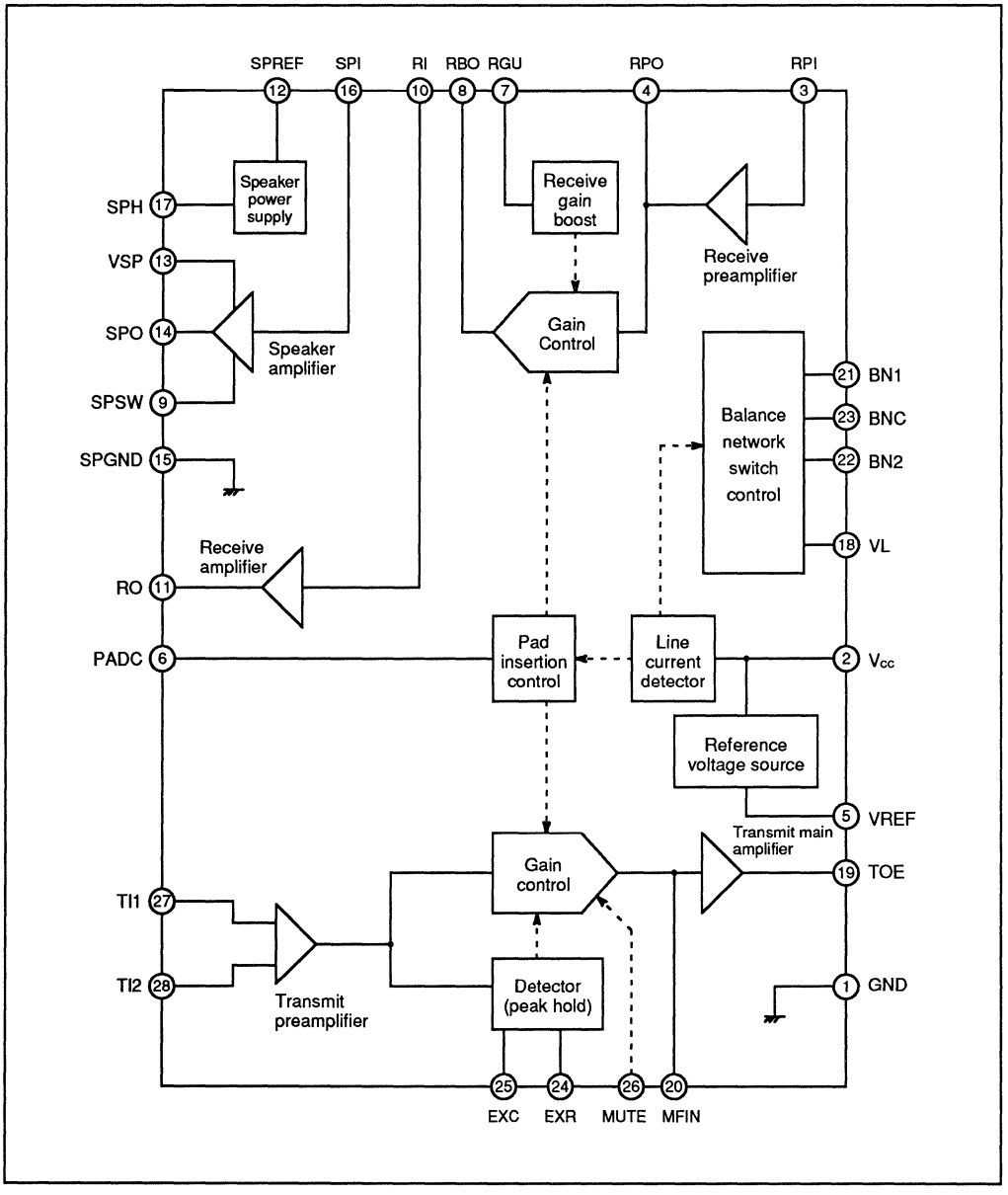


PIN FUNCTIONS

Pin No.	Symbol	I/O	Description
1	GND	–	Chip ground. Connected to the (–) side of an external diode bridge connected to the subscriber loop.
2	V_{CC}	–	Power supply pin. Supplies power to the chip circuits. Coupled from the loop (AC-grounded) by an external capacitor.
3	RPI	I	Receive preamplifier input. Connected to the receive input through an external coupling capacitor.
4	RPO	O	Receive preamplifier output. The receive preamplifier gain and frequency compensation are externally adjusted with a resistor and capacitor connected between this pin and the RPI pin.
5	VREF	–	Reference voltage pin. Connected to the internal reference voltage and AC-grounded through an external capacitor.
6	PADC	–	Pad insertion control. Start-up current for the pad insertion control is adjusted by connecting an external resistor to this pin.
7	RGU	I	Simple receive gain control. Grounding this pin increases the receive preamplifier gain by about 6 dB. Normally left open.
8	RBO	O	Receive buffer output. Connected to the RI and SPI pins through external coupling capacitors.
9	SPSW	I	Speaker defeat switch. When this pin is open, the speaker is connected; when grounded, the speaker is disconnected.
10	RI	I	Receive main amplifier input. The receive signal is coupled to this pin from the RBO pin by an external capacitor.
11	RO	O	Receive main amplifier output. Connected to a low-impedance receiver by an external coupling capacitor. Some receivers may require a shunt capacitor to prevent oscillation.
12	SPREF	–	Speaker circuit reference voltage pin. Reference voltage pin for the speaker and receive output circuit. AC-grounded through an external capacitor.
13	VSP	–	Speaker amplifier power supply pin. The speaker amplifier receives power from this pin. The speaker power supply can be coupled at this point by an external capacitors.
14	SPO	O	Speaker output. Connected to an 8 Ω speaker through an external capacitor. Some applications may require a speaker shunt capacitor to prevent oscillation.

Pin No.	Symbol	I/O	Description
15	SPGND	–	Speaker amplifier ground. This pin must be connected to the circuit network ground.
16	SPI	I	Speaker amplifier input. Connected to the RBO pin through an external capacitor and resistor for adjustment of speaker amplifier gain and frequency compensation.
17	SPH	–	Speaker circuit power control. The speaker power supply circuit is connected to the speaker amplifier input (VSP) through an external network which can be adjusted to control chip power consumption.
18	VL	I	Line input. Connected to the (+) side of an external diode bridge connected to the subscriber loop.
19	TOE	O	Transmit main amplifier output. Connected to the emitter of the transmit transistor.
20	MFIN	I	DTMF signal input. Connected to the base of the transmit output transistor. The input impedance is about 24 kΩ. During voice transmission this pin must be open.
21, 22	BN1, BN2	–	Balance network pins. Used for connection of external balance networks. BN1: Short loop, BN2: Long loop
23	BNC	–	Balance network switching control. An external resistor is connected between this pin and V_{CC} or ground to adjust the BN1 and BN2 switching current.
24	EXR	–	Level expander reference voltage pin. Reference voltage pin for the control of the level expander. Connecting an external capacitor holds the positive peak voltage level.
25	EXC	–	Level expander control. Control pin for the level expander. Connecting an external capacitor holds the negative peak voltage level. When grounded, this pin disables the expander function.
26	MUTE	–	Muting. Grounding this pin suppresses output to the loop. During communication this pin must be left open.
27, 28	TI1, TI2	I	Transmit preamplifier input. Connected to the transmitter through external coupling capacitors. The input is balanced. TI1 is the noninverting input and TI2 is the inverting input.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(T_A = +25°C)

Parameter	Symbol	Value	Unit
Supply voltage	V_L	12	V
Supply current	I_L	20 to 120	mA

ELECTRICAL CHARACTERISTICS

(T_A = +25°C)

Parameter	Symbol	Measurement conditions (f = 1 kHz)	IL (mA)	Value Min	Value Typ	Value Max	Unit
Handset DC voltage	V_{L1}	–	20	2.9	3.2	3.5	V
	V_{L2}		90	6.0	6.5	7.0	V
Supply voltage	V_{CC}	–	20	1.3	1.6	1.9	V
Handset AC impedance	Z_{TEL1}	–	30	500	600	700	Ω
	Z_{TEL2}		90	500	600	700	Ω
Transmit circuit gain	G_{TV1}	V_{IN} = –50 dBV	30	38.0	41.0	44.0	dB
	G_{TV2}	V_{IN} = –50 dBV	90	36.5	39.5	42.5	dB
	ΔG_{TV}	$\Delta G_{TV} = G_{TV}$ (V_{IN} = –50 dBV) – G_{TV} (V_{IN} = –65 dBV)	30	4.0	7.0	10.0	dB
Transmit circuit dynamic range	D_{T1}	Distortion attenuation: ≥ 20 dB	30	–0.5	2.5	–	dBV
	D_{T2}		90	4.5	7.5	–	dBV
Transmit circuit residual noise	NT *	–	–	–	–	–56	dBV
Receive circuit gain	G_{RV1}	V_{IN} = –30 dBV	30	–8.0	–5.0	–2.0	dB
	G_{RV2}	V_{IN} = –30 dBV	90	–13.0	–10.0	–7.0	dB
Receive circuit gain increase	G_{RUP}	V_{IN} = –30 dBV	30	4.0	6.0	8.0	dB
Receive circuit dynamic range	D_{R1}	Distortion attenuation: ≥ 20 dB	30	–15.0	–12.0	–	dBV
	D_{R2}		90	–10.5	–7.5	–	dBV
Speaker circuit gain	G_{SV1}	V_{IN} = –30 dBV	30	4.0	7.0	10.0	dB
	G_{SV2}	V_{IN} = –30 dBV	90	0.0	3.0	6.0	dB
Speaker circuit dynamic range	D_{S1}	Distortion attenuation: ≥ 20 dB	30	–22.0	–19.0	–	dBV
	D_{S2}		90	–11.5	–8.5	–	dBV
Balance network switching	I_{FN}	Far → near	–	43.0	55.0	70.0	mA
	I_{NF}	Near → far	–	32.5	42.5	52.5	mA
	I_H	Hysteresis width	–	9.0	12.5	27.5	mA

* : Design guaranteed

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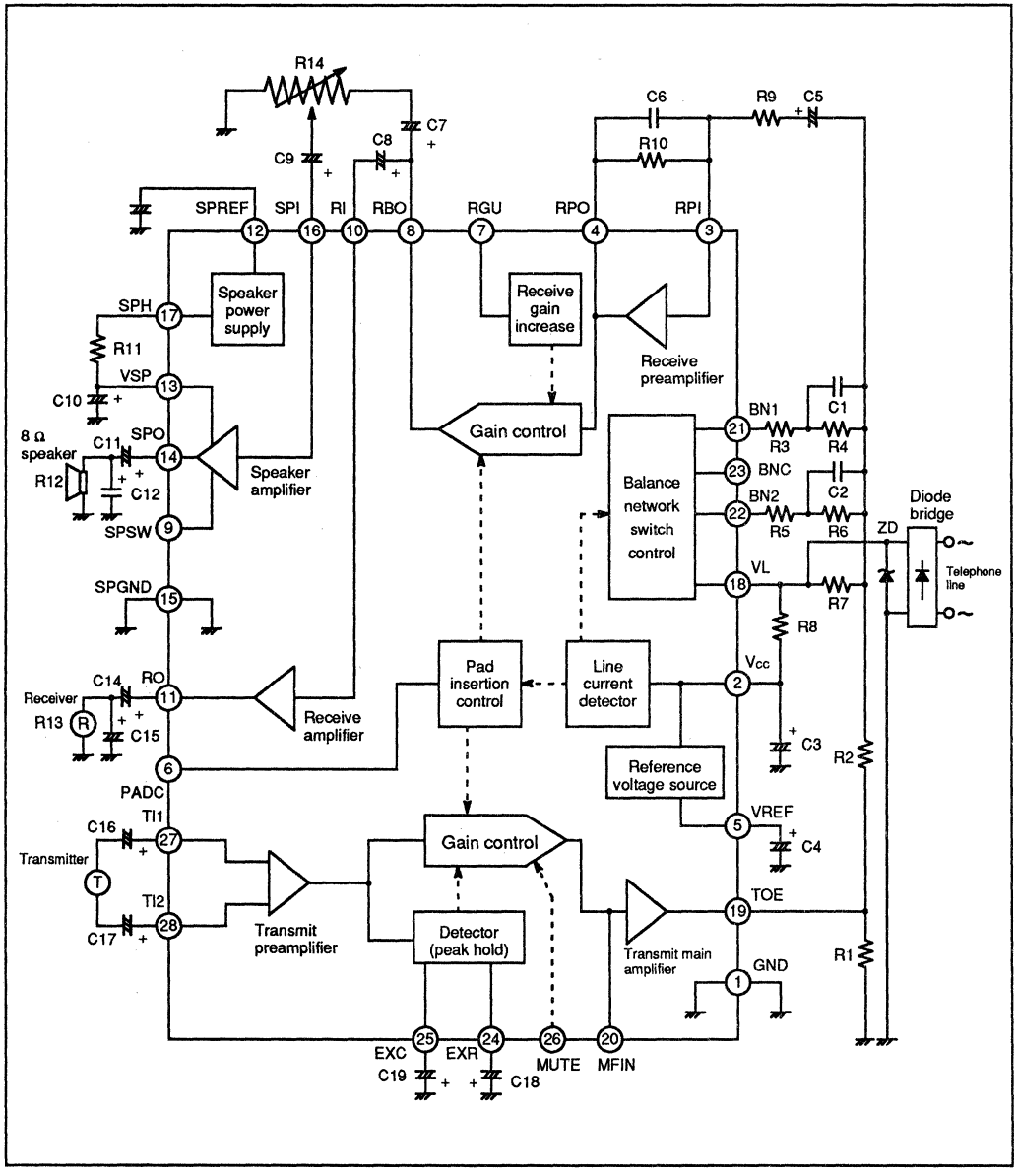
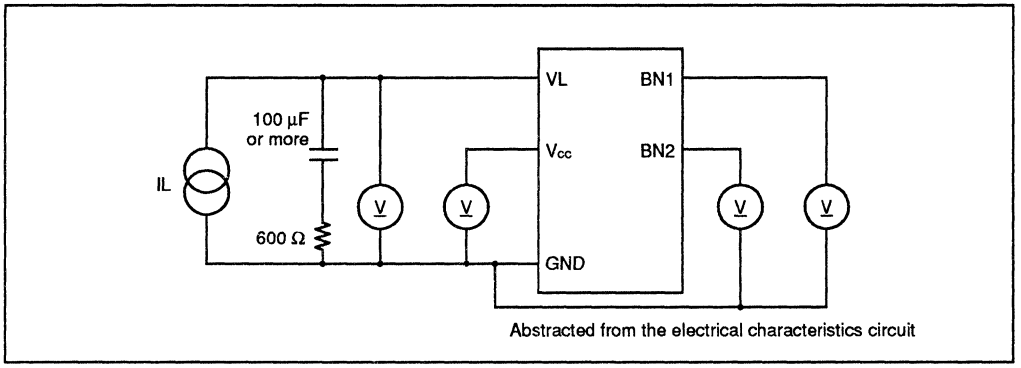
TEST CIRCUITS

- **Test circuit**



- **DC characteristics test circuit**

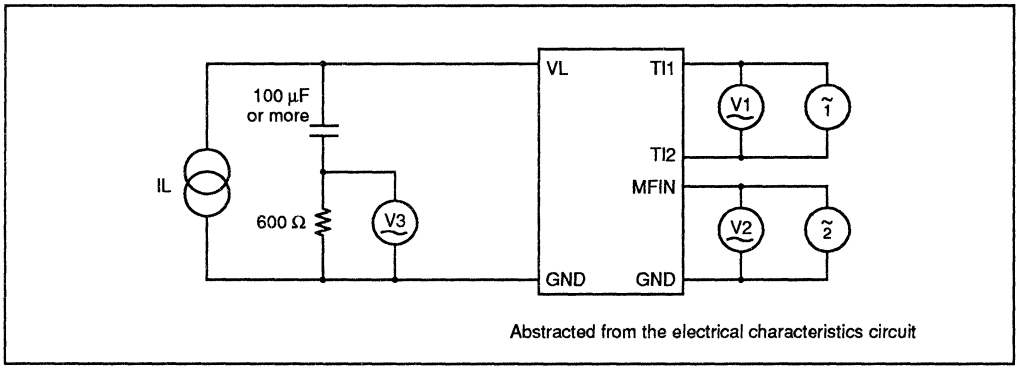


IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
Ⓥ : DC voltmeter

- Balance network switching I_{FN} : When IL increases from 30 mA to 70 mA
  IL (mA) for which VBN2 increases from 1.5 V to 3.5 V or more
  I_{NF} : When IL decreases from 70 mA to 30 mA
  IL (mA) for which VBN1 decreases from 3.5 V to 1.5 V or less

Note: The tolerance of the load impedance for each pin shall be ±1%. (All test circuits)

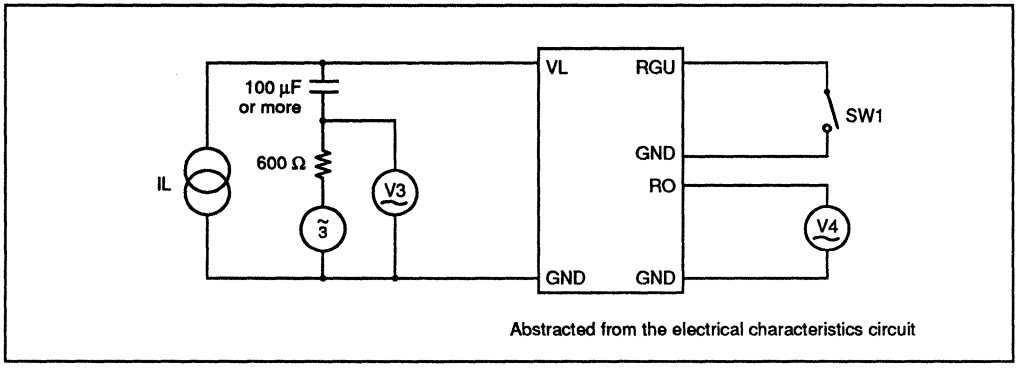
- **Transmission characteristics test circuit**



Ⓒ : Oscillator (Output impedance and DC resistance ≤ 4 Ω at 1 kHz)
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
Ⓥ : AC voltmeter
Transmit circuit gain: G_{TV} (dB) = 20 Log V3/V1 (oscillator 1)
G_{MFV} (dB) = 20 Log V3/V2 (oscillator 2)

- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.
- Residual noise : Measure the transmit output signal level with no transmit input signal.

- **Receive characteristics test circuit**



~ : Oscillator (Output impedance and DC resistance ≤ 4 Ω, f = 1 kHz)
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
V : AC voltmeter
Receive circuit gain: G_{RV} (dB) = 20 Log V4/V3

- Gain boost : Measure the V3 AC signal level boost when SW1 is closed.
- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.

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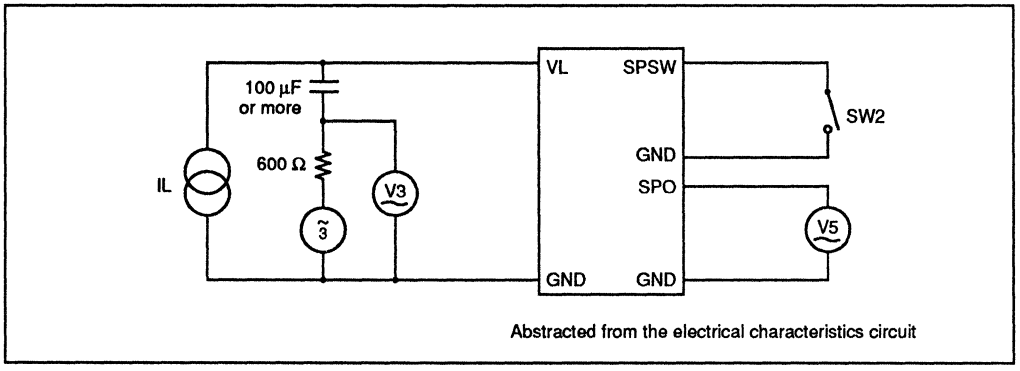
- **Speaker characteristics test circuit**



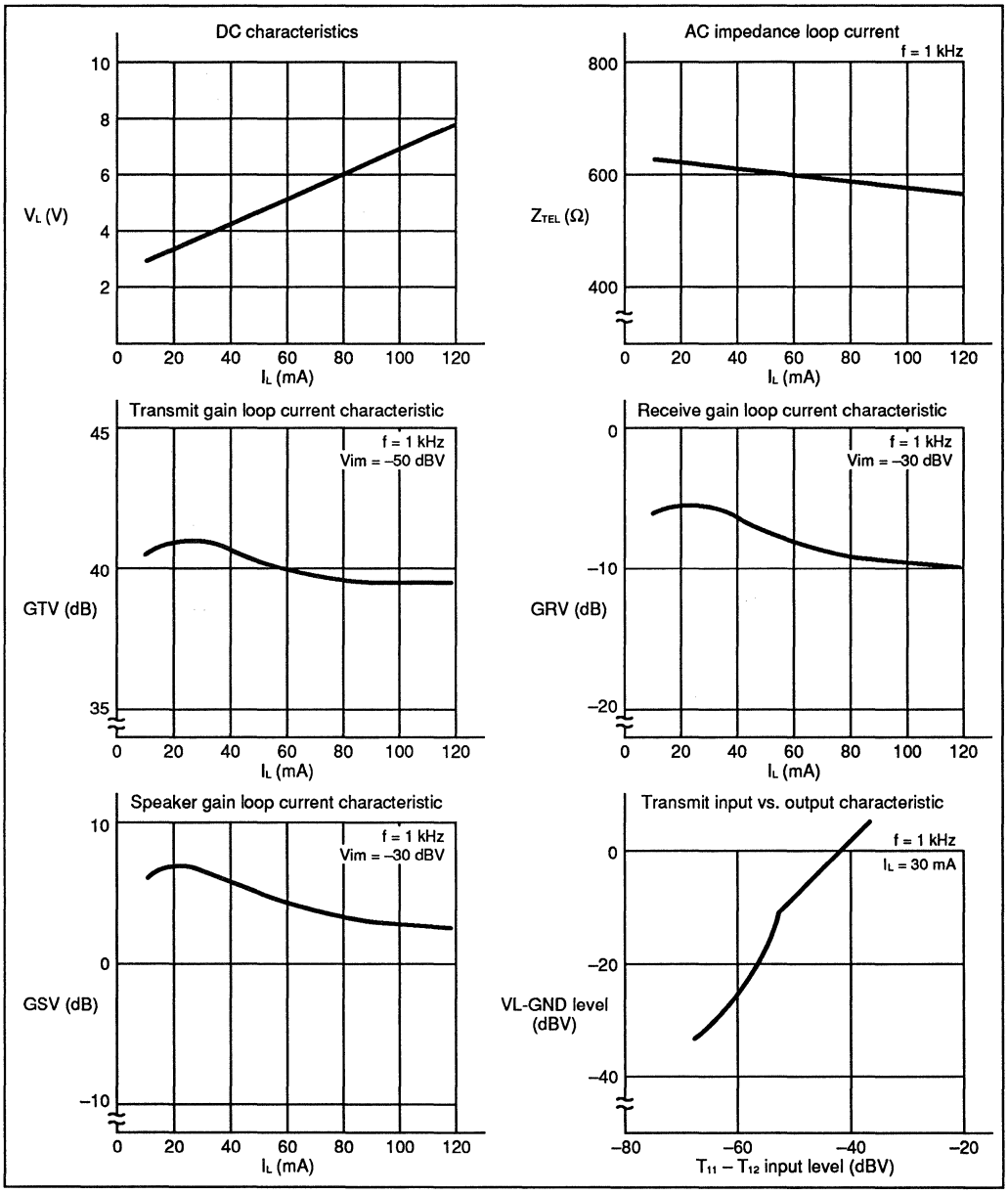
~ : Oscillator (Output impedance and DC resistance ≤ 4 Ω, f = 1 kHz)
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
V : AC voltmeter
Speaker system gain: G_{SV} (dB) = 20 Log V5/V3 (SW2 open)

- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.

- **Test circuit components**

Reference Designation	Component	Values	Remarks
R1	Resistor	82 Ω F, 1/8 W or more	
R2	Resistor	820 Ω F, 1/16 W or more	
R3	Resistor	2.4 kΩ F, 1/16 W or more	
R4	Resistor	8.2 kΩ F, 1/16 W or more	
R5	Resistor	1.5 kΩ F, 1/16 W or more	
R6	Resistor	6.2 kΩ F, 1/16 W or more	
R7	Resistor	5.6 kΩ F, 1/16 W or more	
R8	Resistor	680 Ω F, 1/16 W or more	
R9	Resistor	5.6 kΩ F, 1/16 W or more	
R10	Resistor	27 kΩ F, 1/16 W or more	
R11	Resistor	10 Ω F, 1/8 W or more	
R12	Resistor	8 Ω F, 1/8 W or more	Speaker
R13	Resistor	150 Ω F, 1/16 W or more	Receiver
R14	Resistor	20 kΩ or more F, 1/16 W or more	
C1	Capacitor	0.027 µF, 16 V or more, ±1%	
C2	Capacitor	0.015 µF, 16 V or more, ±1%	
C3	Capacitor	220 µF, 5 V or more, ±5%	
C4	Capacitor	100 µF, 3 V or more, ±5%	
C5	Capacitor	2.2 µF, 3 V or more, ±1%	
C6	Capacitor	2000 PF, 3 V or more, ±1%	
C7	Capacitor	2.2 µF, 5 V or more, ±5%	
C8	Capacitor	2.2 µF, 5 V or more, ±5%	
C9	Capacitor	2.2 µF, 5 V or more, ±5%	
C10	Capacitor	1000 µF, 5 V or more, ±5%	
C11	Capacitor	220 µF, 3 V or more, ±5%	
C12	Capacitor	2.2 µF, 3 V or more, ±5%	
C13	Capacitor	100 µF, 3 V or more, ±5%	
C14	Capacitor	100 µF, 3 V or more, ±5%	
C15	Capacitor	0.47 µF, 3 V or more, ±5%	
C16	Capacitor	2.2 µF, 3 V or more, ±1%	
C17	Capacitor	2.2 µF, 3 V or more, ±1%	
C18	Capacitor	2.2 µF, 5 V or more, ±1%	
C19	Capacitor	2.2 µF, 5 V or more, ±1%	

TYPICAL CHARACTERISTIC CURVES



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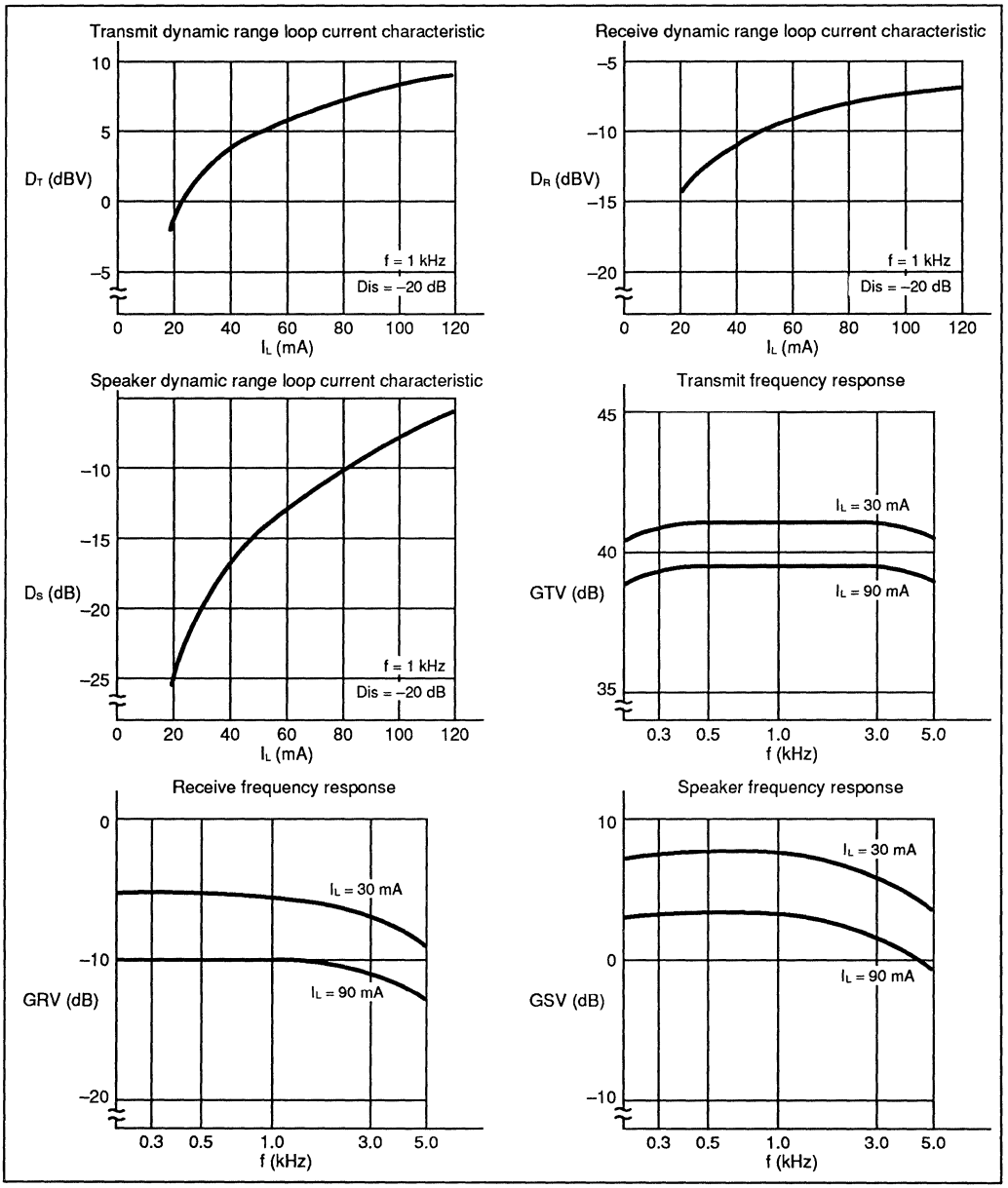
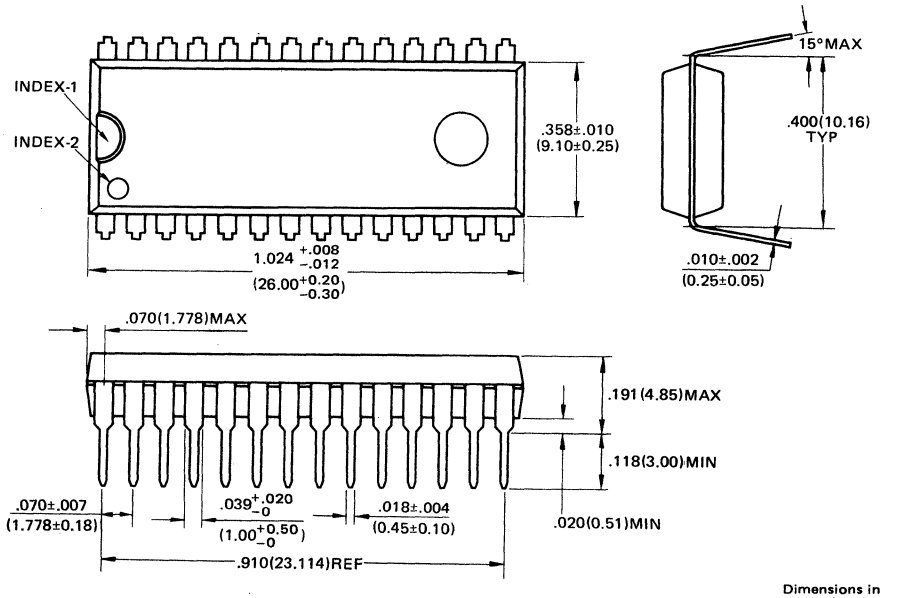

Transmit dynamic range loop current characteristic
D_T (dBV)
10
5
0
−5
f = 1 kHz
Dis = −20 dB
0 20 40 60 80 100 120
I_L (mA)
Receive dynamic range loop current characteristic
D_R (dBV)
−5
−10
−15
−20
f = 1 kHz
Dis = −20 dB
0 20 40 60 80 100 120
I_L (mA)
Speaker dynamic range loop current characteristic
D_S (dB)
−10
−15
−20
−25
f = 1 kHz
Dis = −20 dB
0 20 40 60 80 100 120
I_L (mA)
Transmit frequency response
GTV (dB)
45
40
35
I_L = 30 mA
I_L = 90 mA
0.3 0.5 1.0 3.0 5.0
f (kHz)
Receive frequency response
GRV (dB)
0
−10
−20
I_L = 30 mA
I_L = 90 mA
0.3 0.5 1.0 3.0 5.0
f (kHz)
Speaker frequency response
GSV (dB)
10
0
−10
I_L = 30 mA
I_L = 90 mA
0.3 0.5 1.0 3.0 5.0
f (kHz)

7

PACKAGE DIMENSIONS

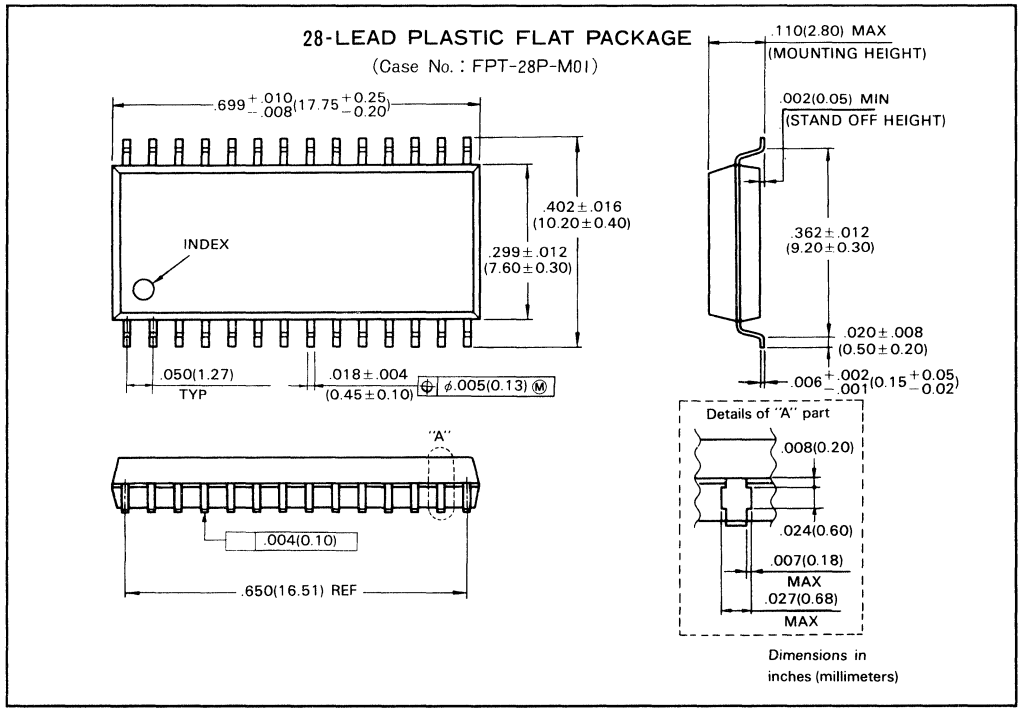
28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M03)



Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS



DATA SHEET

FUJITSU

MB4752A
Subscriber Line Interface IC

The Fujitsu MB4752A is designed for PBX (Private Branch Exchange), and has battery feed, supervision, and 4-wire-to-2-wire conversion functions.

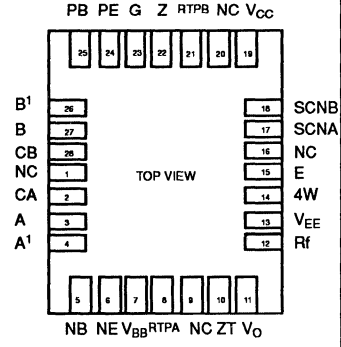
The battery feed mode can be set to a 200 x 2 or 440 x 2 constant feed resistor by using the terminal connection.

The subscriber line interface circuit is used for digital PBX and CO. This device can be used worldwide to achieve high longitudinal balance with 4W-to-2W gain and characteristics by adjusting the external resistor.

LCC-28C-F01

- 440 Ω x 2/200 Ω x 2 feeding resistance
- Loop detection function
- Line fault protection
- Hybrid function (4-wire to 2-wire conversion function)
- Ring trip comparator
  Balancing impedance is selected by external parts
- Digital output terminal has open-collector output with a pull up resistor
- 28-pad LCC package: (Suffix: –TV)

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Note
Power Supply Voltage	V_{BB}	–60 to +0.5	V	Referenced to GND
	V_{CC}	–0.5 to +7	V	Referenced to E
	V_{EE}	–7 to +0.5	V	
	V_{EG}	–7.5 to +0.5	V	Referenced to GND
Input Voltage	V_A	V_{BB} –0.5 to +0.5	V	Referenced to GND
	V_B	V_{BB} –0.5 to +0.5	V	
	RTPA	V_{BB} –0.5 to V_{BB} +30	V	
	RTPB	–30 to +0.5	V	
	V_{4W}	V_{EE} –0.5 to V_{CC} +0.5	V	Referenced to E
Storage Temperature	T_{STG}	–55 to +150	°C	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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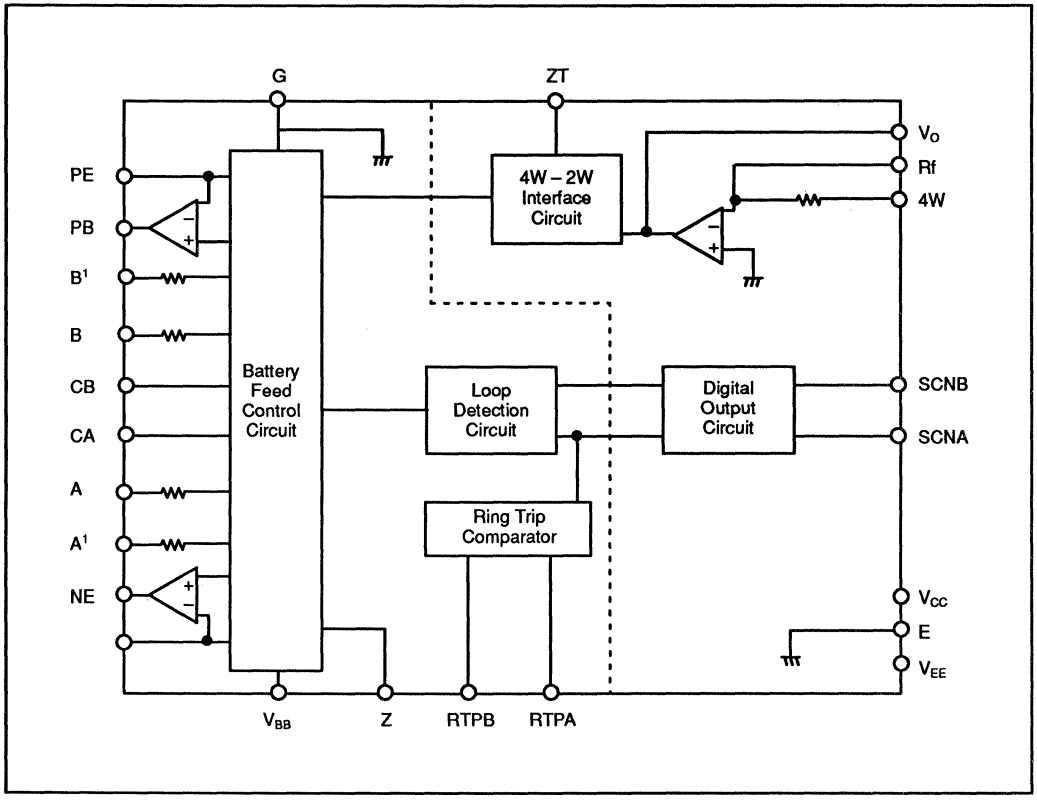
Figure 1. MB4752A Block Diagram



7

PIN DESCRIPTION

Pin No.	Symbol	Description
1	NC	No Connection
2	CA	High-impedance capacitor pin. A capacitor is connected between this terminal and CB terminal. AC impedance of Battey Feed circuit is made up to high impedance by this external capacitor.
3	A	440 Ω battery feed for line A
4	A^1	200 Ω battery feed for line A
5	NB	Base drive output for the NPN power transistor
6	NE	Emitter current sensing input for the NPN power transistor
7	V_{BB}	Most negative voltage supply, –48 V
8	RTPA	Ring-trip input for line A
9	NC	No Connection
10	ZT	4 W to 2 W transformation impedance
11	V_O	4 W to 2 W gain setting resistor input
12	R_f	4 W to 2 W gain setting resistor input
13	V_{EE}	Negative voltage supply, –5 V
14	4W	4-wire input
15	E	Ground
16	NC	No Connection
17	SCNA	SCN detecting output for line A
18	SCNB	SCN detecting output for line B
19	V_{CC}	Positive voltage supply, +5 V
20	NC	No Connection
21	RTPB	Ring trip input for line B
22	Z	Compensation capacitor input
23	G	Ground
24	PE	Emitter current sensing input for the PNP power transistor
25	PB	Base drive output for the PNP power transistor
26	B^1	200 Ω battery feed for line B
27	B	440 Ω battery feed for line B
28	CB	High-impedance capacitor pin. A capacitor is connected between this terminal and CB terminal. AC impedance of Battery Feed circuit is made up to high impedance by this external capacitor.

FUNCTIONAL DESCRIPTION

Battery Feed

By selecting connection A, B or A^1, B^1, balanced feeding resistance of 440 Ω for PBX or 200 Ω for CO application is selected.

Loop Detection

The digital signal output indicates the handset condition as off the hook, both the SCNA and SCNB terminals simultaneously, by detecting the current that is generated when the handset is off the hook.

Line Fault Protection

Line fault protection outputs the signals when line A or B is short circuited to SCNA and SCNB, respectively.

When excess current flows, arrester provides system protection, and DC feeding resistance becomes six times as large as the normal value. As a result, current decreases.

Hybrid (Four-to-two wire conversion)

As for the communication channel, the telephone switching system has a four-wire line internally, and the telephone set system has a two-wire line. This device also has a built-in four-wire to two-wire converter. The two-wire to four-wire converter contains external common industrial operational amplifier.

Ring Trip Comparator

It is necessary for the electrical telephone switching system to detect that the receiver is on the hook during a calling signal.

Ring trip detection is performed by connecting external low pass filter to the input RTPA or RTPB terminal. The output signal is superimposed on the trip supervise SCA when the handset is on the hook.

7

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Unit	Note
Power Supply Voltage		V_{BB}	−48 ± 5	V	Referenced to GND
		V_{CC}	5.0 ± 0.25	V	Referenced to E
		V_{EE}	−5.0 ± 0.25	V	
		V_{EG}	−0.5 to +0.5	V	Referenced to GND
2 W	440 Ω Feeding Loop Resistor	R_L	0 to 1200	Ω	Line resistor +
	200 Ω Feeding Loop Resistor	R_L	0 to 1900	Ω	terminal resistor
	Low Frequency Inductive Current	I_{AC}	0 to 6.4	mArms	Single line current f = 50/60 Hz
4 W	Input Offset Voltage	V_{RCS}	−0.2 to 0.2	V	
	Input Voltage	S_{4W}	7.0	dBm	
Operating Temperature		T_{OP}	5 to 70	°C	

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted.)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	On-Hook	I_{BB1}	V_B = 0 V	V_{BB} = −53 V V_{CC} = 5.25 V V_{EE} = −5.25 V V_{EG} = 0 V	−6.4	−3.8	—	mA
		I_{CC1}			—	2.5	6.6	mA
		I_{EE1}	$V_A = V_{BB}$		−2.2	−1.1	—	mA
440 Ω Feeding Mode	Off-Hook R_L = 0 Ω	I_{BB2}	V_B = −26.5 V		−13	−8	—	mA
		I_{CC2}	$V_A = V_{BB}$		—	2.5	6.4	mA
		I_{EE2}	+26.5 V		−2.2	−1.2	—	mA
Power Supply Current	On-Hook	I_{BB3}	V_B = 0 V		−7.5	−4	—	mA
		I_{CC3}			—	2.5	6.6	mA
		I_{EE3}	$V_A = V_{BB}$		−2.2	−1.1	—	mA
200 Ω Feeding Mode	Off-Hook R_L = 0 Ω	I_{BB4}	V_B = −26.5 V		−15.6	−9.5	—	mA
		I_{CC4}	$V_A = V_{BB}$		—	2.5	6.4	mA
		I_{EE4}	+26.5 V		−2.2	−1.2	—	mA

DC CHARACTERISTICS (Continued)

(Recommended operating condition unless otherwise noted.)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current 440 Ω Feeding Mode		I_{A1}	V_B = –24 V		47.5	54	65	mA
		I_{B1}	$V_A = V_{BB}$ +24 V		–65	–54	–47.5	mA
		I_{A2}	V_B = –10 V	V_{BB} = –48 V	16.8	21	26.5	mA
		I_{B2}	$V_A = V_{BB}$ +10 V	V_{CC} = 5.0 V	–26.5	–21	–16.8	mA
Loop Supply Current 200 Ω Feeding Mode		I_{A3}	V_B = –24 V	V_{EE} = –5.0 V	72.5	83	91.4	mA
		I_{B3}	$V_A = V_{BB}$ +24 V	V_{EG} = 0 V	–91.4	–83	–72.5	mA
		I_{A4}	V_B = –10 V		35.7	45	58	mA
		I_{B4}	$V_A = V_{BB}$ +10 V		–58	–45	–35.7	mA
Line-Fault Drooping Current 440 Ω Feeding Mode		I_{PG1}	V_A = GND	V_{BB} = –53 V	—	22	28	mA
		I_{PB1}	$V_B = V_{BB}$	V_{CC} = 5.0 V	–28	–22	—	mA
Line-Fault Drooping Current 200 Ω Feeding Mode		I_{PG2}	V_A = GND	V_{EE} = –5.0 V	—	29	36	mA
		I_{PB2}	$V_B = V_{BB}$	V_{EG} = 0 V	–36	–29	—	mA
Loop Detection Current	Detection	I_{ON1}	V_{BB} = –43 V	V_{CC} = 5.0 V	11.1	12.4	14.2	mA
	Release	I_{OFF1}		V_{EE} = –5.0 V	10.4	11.5	13.4	mA
	Detection	I_{ON2}	V_{BB} = –53 V	V_{EG} = 0 V	14.4	16.0	18.1	mA
	Release	I_{OFF2}			13.4	14.8	16.6	mA
Ring Trip Detection Volt.	RTPA	V_{RD1}	On-hook		–44	–43.3	–42.5	V
	RTPB	V_{RD2}	On-hook		–5	–4.4	–4	V
Line-Fault Detection Volt. 200 Ω Feeding Mode	Line A to GND	V_{GD1}	V_B = Open	V_{BB} = –48 V	24	26.5	30	V
	Line B to V_{BB}		V_A = Open	V_{CC} = 5.0 V	24	26.5	30	V
Line-Fault Detection Volt. 440 Ω Feeding Mode	Line A to GND	V_{GD2}	V_B = Open	V_{EE} = –5.0 V	11	15.5	21	V
	Line B to V_{BB}		V_A = Open	V_{EG} = 0 V	11	15.5	21	V
Line-Fault SCN Mask Current	SCNA	I_{MA}	$V_B = V_{BB}$		3.3	4.4	5.9	mA
	SCNB	I_{MB}	V_A = 0 V		–5.9	–4.4	–3.3	mA
SCN Output Low Voltage	SCNA	V_{OLA}	I = 1.2 mA		—	0.02	0.4	V
	SCNB	V_{OLB}	V_{CC} = 5.25 V On-hook	V_{BB} = –48 V	—	0.02	0.4	V
SCN Output High Voltage	SCNA	V_{OHA}	I = –50 µA	V_{EE} = –5.0 V	2.4	3.8	—	V
	SCNB	V_{OHB}	V_{CC} = 4.75 V Off-hook	V_{EG} = 0 V Ref. to E	2.4	3.8	—	V

Note: Unless RTPA terminal is in use, it must be connected to V_{BB}.

AC CHARACTERISTICS

(Recommended operating condition unless otherwise noted.)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
4 W to 2 W Gain		G_{42}	L = +4dBm, f = 1kHz		–5.4	–4.4	–3.4	dB
4 W to 2 W Gain Frequency Response		G_{f42}	f = 0.2 kHz	Referenced to output at f = 1 kHz L = –10 dBr	–0.1	+0.07	—	dB
			f = 0.3 kHz		–0.1	+0.04	+0.2	dB
			f = 0.4 kHz		–0.1	+0.02	+0.2	dB
			f = 0.6 kHz		–0.1	0	+0.2	dB
			f = 2.4 kHz		–0.1	–0.01	+0.2	dB
			f = 3.0 kHz		–0.1	–0.01	+0.2	dB
			f = 3.4 kHz		–0.1	–0.01	+0.2	dB
4 W to 2 W Gain Level Linearity		G_{L42}	L = +3 dBr	Referenced to output at L = –10 dBr f = 1 kHz	–0.1	0	+0.1	dB
			L = –40 dBr		–0.1	0	+0.1	dB
			L = –50 dBr		–0.2	0	+0.2	dB
Idle Channel Noise		N_{I2}			—	–94	–76	dB
4 W to 2 W Signal/Noise Ratio		SN_{42}	L = 0 dBr	f = 1 kHz	50	57	—	dB
			L = –30 dBr		46	61	—	dB
			L = –40 dBr		36	52	—	dB
			L = –45 dBr		31	47	—	dB
Longitudinal Balance		L_{B2W}	f = 0.3 kHz	Adjust REA 48 to 53 Ω	43	60	—	dB
			f = 1.0 kHz		43	60	—	dB
			f = 3.4 kHz		43	60	—	dB
Power Supply Noise Rejection	V_{BB} to 2 W	P_{SRB}	L = 0.24 Vrms f = 1 kHz		20	39	—	dB
	V_{CC} to 2 W	P_{SRC}			20	41	—	dB
	V_{EE} to 2 W	P_{SRE}			20	55	—	dB
	V_{EG} to 2 W	P_{SRR}			20	43	—	dB

Note: Unless RTPA terminal is in use, it must be connected to V_{BB}.

7

SCN Logical Table

Input Condition			SCNA	SCNB	Note
Loop Detection	Loop Detection (Off-hook to On-hook)	$I_L < I_{ON}$	L	L	I_L: Loop Current
		$I_L > I_{ON}$	H	H	I_{ON}: I_{ON1}, I_{ON2}
	Loop Release (On-hook to Off-hook)	$I_L < I_{OFF}$	H	H	I_{OFF}: I_{OFF1}, I_{OFF2}
		$I_L > I_{OFF}$	L	L	See DC Characteristics
Ring Trip Detection	RTPA input	$V_{RTPA} < V_{RD1}$	L	L	V_{RTPA}: RTPA Input Volt.
		$V_{RTPA} > V_{RD1}$	H	L	V_{RTPB}: RTPB Input Volt.
	RTPB input	$V_{RTPB} < V_{RD2}$	L	L	V_{RD1}: See DC Char.
		$V_{RTPB} > V_{RD2}$	H	L	V_{RD2}:
Line-Fault Detection	Line A to Ground	IA + IB < ION *2	L	L	IA: Line A Current IB: Line B Current IMA: See DC Char. IMB: See DC Char.
		IA + IB > ION *2 and IB < IMB	H	L	
		IA + IB > ION *2 and IB > IMB	H	H	
	Line B to Ground	IA + IB < ION *2	L	L	
		IA + IB > ION *2 and IA < IMA	L	H	
		IA + IB > ION *2 and IA > IMA	H	H	

Note: Unless RTPA terminal is in use, it must be connected to V_{BB}.

Line Fault Protection

2 W State		Feed Mode	Note
Line to Ground/V_{BB}	| VB + (VA – V_{BB} | < VGD	Normal Feeding (No Protection)	VA: Line A Voltage VB: Line B Voltage
	| VB + (VA – V_{BB} | > VGD	Feeding Resistor (6 times that of normal value)	VGD, VGD1, VGD2: See DC Char.

Figure 2. Power Supply Mode (440 Ω)

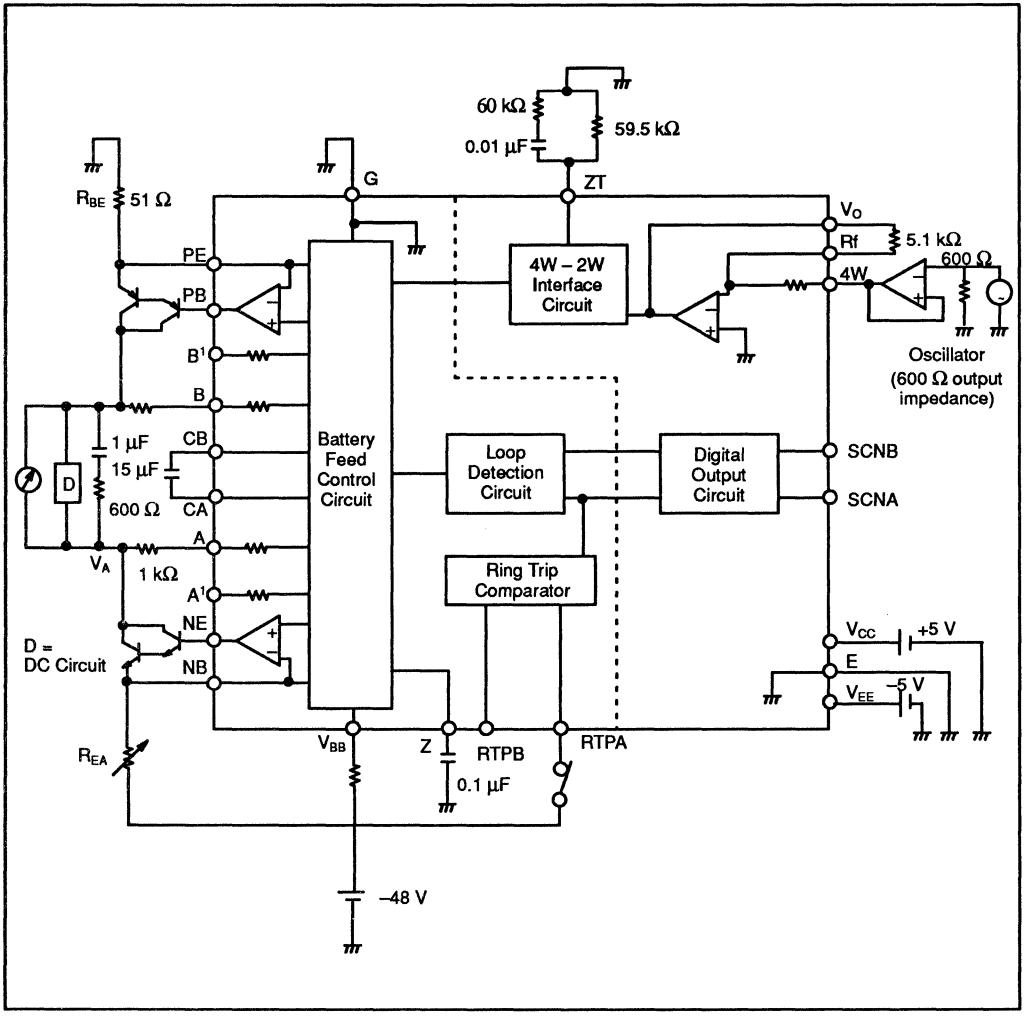
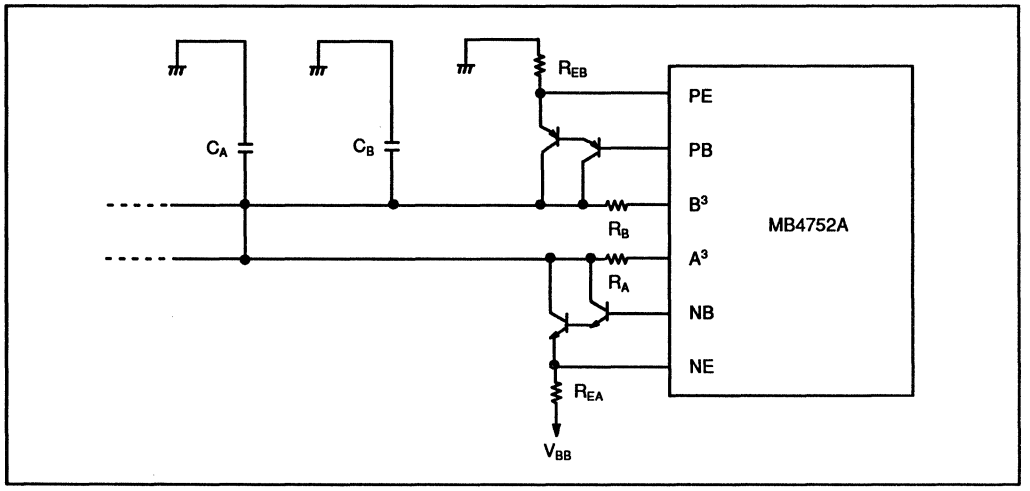
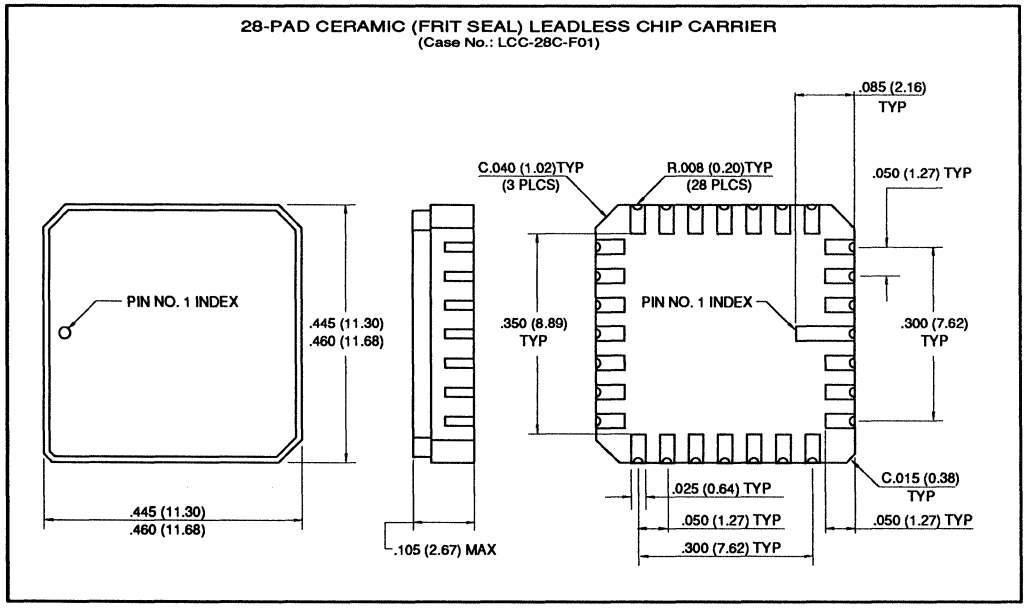


Figure 3. Power Supply Mode (200 Ω)





7

FUJITSU

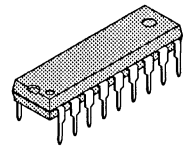
DATA SHEET

MB87007A/MB87008A
DTMF Pulse Dialer

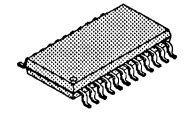
The Fujitsu MB87007A/MB87008A is a Dual Tone Multifrequency (DTMF) pulse dialer for pushbutton telephone sets. It uses the Si-Gate CMOS process and is suitable for both DTMF and PULSE modes. The MB87007A/MB87008A can be switched from a PULSE mode to a DTMF mode by a mode selection entry or by an input from the keyboard. It has a 26-digit redial memory that permits the coexistence of PULSE and DTMF modes and enables mixed redialing in both PULSE and DTMF modes by a signal key entry.

- Pulse 10 pps, 20 pps, or DTMF operation that is selected by the mode switch pin (MODEIN)
- On-chip 26 digits of redial memory (up to 25 digits can be written into the memory)
- MB87007A has a make ratio of 39% and MB87008A has a make ratio of 33%
- LDT function is provided (switching from PULSE mode to DTMF mode by key entry)
- Beep tone for input confirmation can be output (for all effective key entry independently PULSE/DTMF modes)
- Mixed redialing of both PULSE and DTMF modes is possible
- Redial inhibit function is included for redial memory overflow
- PAUSE function is provided and pause accumulation is possible
- FLASH function is provided (ONHOOK mode is selected by keyboard input)
- Crystal or ceramic oscillator (3.579545 MHz) can be used
- Pause release function is provided (two or more consecutive pauses can be released)
- Operating voltages:
  PULSE mode: 2.0 V to 6.0 V
  DTMF mode: 2.5 V to 6.0 V
  (TA = −30 to 60°C)

PRELIMINARY

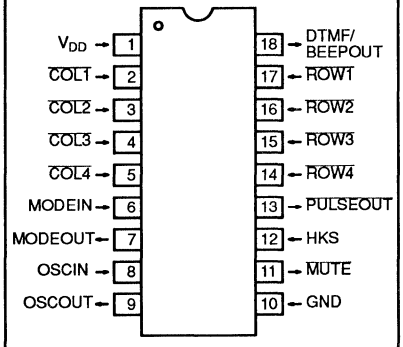


PLASTIC PACKAGE
DIP–18P–M02



PLASTIC PACKAGE
FPT–24P–M02

PIN ASSIGNMENT



(DIP–18P–M02)

FPT PIN ASSIGNMENT
See Page 6–88

7

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Pin Name	Value	Unit
Power Supply Voltage	V_{DD}	V_{DD}	GND – 0.3 to 7.0	V
Input Voltage	VI	All inputs	GND – 0.3 to V_{DD} + 0.3	V
Ouput Voltage	VO	All outputs	GND – 0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}		−55 to +150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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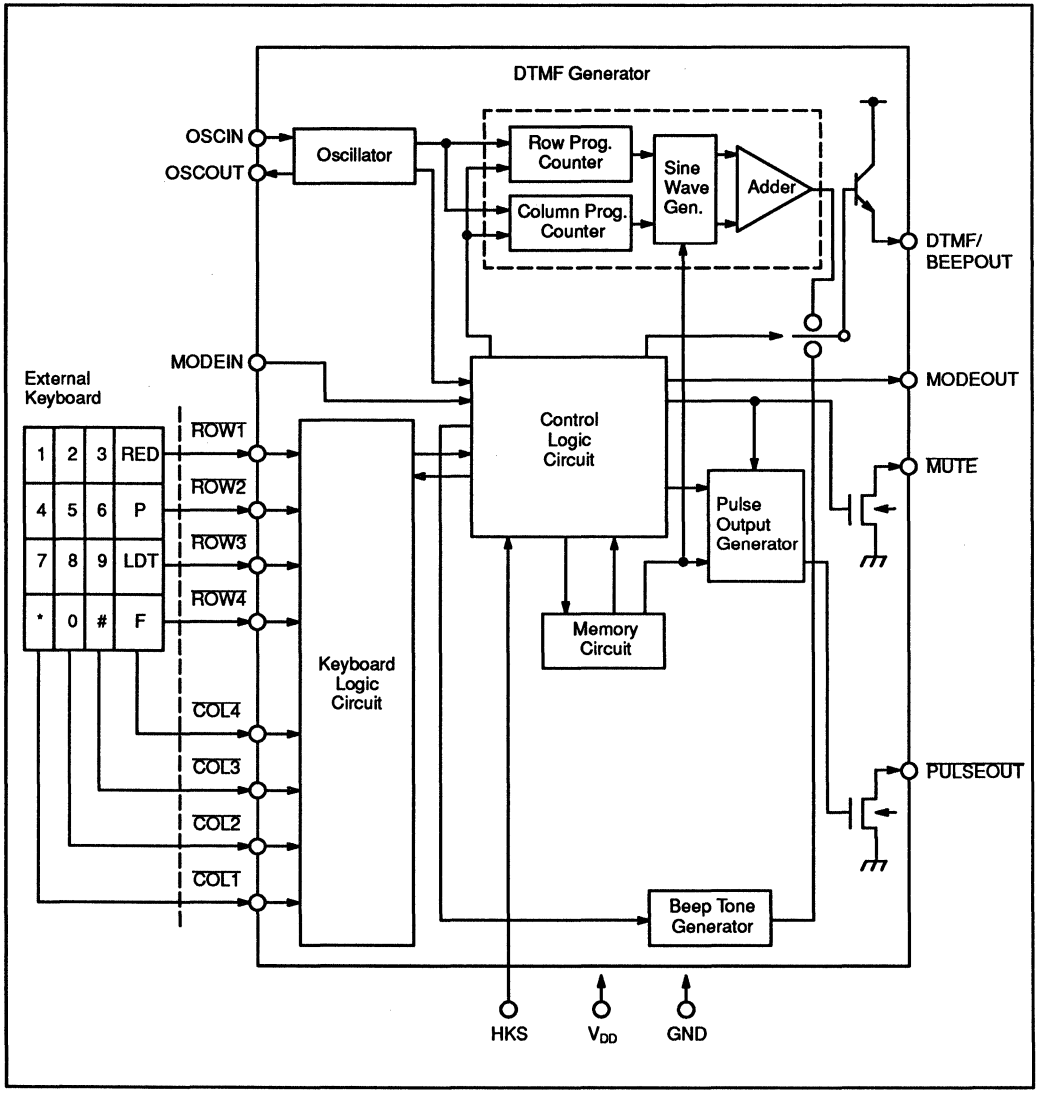
Figure 1. MB87007A/MB87008A Block Diagram



PIN DESCRIPTIONS

<table>
<tr><th rowspan="2">I/O</th><th colspan="2">Pin No.</th><th rowspan="2">Symbol</th><th rowspan="2">Description</th></tr>
<tr><th>DIP</th><th>FPT</th></tr>
<tr><td rowspan="2">Power Supply</td><td>1</td><td>1</td><td>V_{DD}</td><td>Power supply voltages: Pulse mode 2.0 V to 6.0 V
DTMF mode 2.5 V to 6.0 V
Memory Retention mode 2.0 V min.</td></tr>
<tr><td>10</td><td>12</td><td>GND</td><td>Ground</td></tr>
<tr><td rowspan="2">Input</td><td>2
3
4
5
17
16
15
14</td><td>2
3
4
5
23
22
21
20</td><td>$\overline{COL1}$
$\overline{COL2}$
$\overline{COL3}$
$\overline{COL4}$
$\overline{ROW1}$
$\overline{ROW2}$
$\overline{ROW3}$
$\overline{ROW4}$</td><td>Uses key entries from 2 of 7 or 2 of 8 keyboard with common GND. This IC is available with a single contact from A type key board and electronic input (Low entry).
Key input debouncing time is 23 ms typ. for both PULSE and DTMF modes.
Key input release guard time is 23 ms typ. for both PULSE and DTMF modes.
Key entry is accepted in PULSE/DTMF mode only when a single key (one key on the keyboard) is pressed longer than the debouncing time. If two or more keys are pressed, they are not accepted unless they are released one-by-one and the last key is held closed longer than the debouncing time, after all other keys are released.
Key entry is accepted in DTMF mode only when either a single key (dual-tone key) is pressed, or two or more keys in the same $\overline{COL}$ or $\overline{ROW}$ (single-tone keys) are pressed longer than the debouncing time. If even one key is pressed in $\overline{COL4}$, the single-tone keys are ineffective. When multiple single-tone keys are pressed, if they are released one-by-one, and the last key is held closed longer than the debouncing time (after all other keys are released), the key is effective as the dual-tone key.
Hereafter, key entries are described with the premise that keys are held closed longer than the debouncing time.
Pauses between key entries in PULSE and DTMF modes must be 50 ms or more. However, up to 50 ms is necessary from key entry to output start for a single-tone output.
Key switch contact resistance up to 5kΩ is allowable.</td></tr>
<tr><td>6</td><td>8</td><td>MODEIN</td><td>This pin selects the pulse 10 pps, 20 pps and DTMF mode.
<table>
<tr><th colspan="2">Mode</th><th>Setting</th></tr>
<tr><td rowspan="2">PULSE mode</td><td>10 pps</td><td>Open (1 MΩ or more)</td></tr>
<tr><td>20 pps</td><td>V_{DD}</td></tr>
<tr><td colspan="2">DTMF mode</td><td>GND</td></tr>
</table>
When mode switching is requested by MODEIN during PULSE or TONE transmission, the request will not be accepted.
The request is accepted by key entry after data entry transmission is completed.
In ONHOOK mode, MODEIN is set to a high impedance state.</td></tr>
</table>

Continued on next page

7

PIN DESCRIPTIONS

I/O	Pin No. DIP	Pin No. FPT	Symbol	Description
Input	12	15	HKS	Hook switch input pin. ONHOOK Mode: Open or V_{DD} OFFHOOK Mode: GND Output is inhibited in ONHOOK mode and $\overline{\text{PULSEOUT}}$, DTMF/BEEPOUT, $\overline{\text{MUTE}}$, and MODEOUT are set at a high impedance state. All key entries are set to HZ and the on-chip operational amplifier and oscillator (OSCIN = L, OSCOUT = L) become power down states. This pin is pulled up by a high resistance internally. The input level is in the CMOS level.
	8	10	OSCIN	Oscillator input pin. This pin is pulled up by a high resistance in ONHOOK mode.
Output	9	11	OSCOUT	Oscillator output pin. This pin is pulled down by a high resistance in ONHOOK mode.
	7	9	MODEOUT	The output level is in the CMOS level and set to a high impedance state in ONHOOK mode. Low level is output in the PULSE mode and high level is output in the DTMF mode, including the LDT function. MODEOUT blinks on and off at a frequency of 2.5Hz typ., if there is no pause before and after mode switching in redial function. Independent of PULSE/DTMF modes, the beep tone is output at the BEEPOUT when the FLASH key is pressed. The MODEOUT pin is output low level during the beep tone output. High impedance of 0.6 second typ. is output following the beep tone output. The key acceptance state (OFFHOOK mode) is now entered.
	11	13	$\overline{\text{MUTE}}$	N-channel open drain output. The following are $\overline{\text{MUTE}}$ pin HZ conditions during PULSE/DTMF modes. 1. There is no key entry. 2. When the FLASH key is pressed, HZ of 0.6 typ. second is output after the beep tone is output. 3. During pause output state. (However, when a key is pressed, $\overline{\text{MUTE}}$ is low level while beep tone is being output.) 4. During MODEOUT blinking. After key entries become effective in the PULSE or DTMF modes, the output level is low during the beep tone transmission, pulse transmission in accordance with effective key entries, and DTMF output transmission.
	13	16	$\overline{\text{PULSEOUT}}$	N-channel open drain output. High impedance (HZ) is set in ONHOOK or DTMF modes. In PULSE mode, this pin is set low for pulse brakes, according to numerical key entries. When the FLASH key is pressed in either the PULSE or DTMF mode, a low level is output for 600 milliseconds typ. after the beep tone is sent (even during a PULSE/DTMF send). The key acceptance state (OFFHOOK state) then returns. The make ratio for PULSE output is 39% for MB87007A and 33% for MB87008A.

Continued on next page

PIN DESCRIPTIONS

I/O	Pin No. DIP	Pin No. FPT	Symbol	Description
	18	24	DTMF/ BEEPOUT	The DTMF/BEEPOUT pin is a bipolar emitter follower that can drive a 100 Ω load between pin and GND. In the DTMF mode (exclude $\overline{COL4}$) when a single key (numeric, [*] or [#]) is pressed, a dual tone is output. Pressing two or more keys in the same $\overline{ROW}$ or $\overline{COL}$ on the keyboard outputs the signal tone in the $\overline{ROW}$ or $\overline{COL}$. However, if a key in $\overline{COL4}$ is pressed, DUAL TONE or single tone in the $\overline{ROW}$ or $\overline{COL}$ is not output (see Electrical Characteristics). If the FLASH key is pressed during DTMF sending, the beep tone is output at BEEPOUT and subsequent DTMF tones are not output. The ONHOOK mode is entered for 600 milliseconds typ. after which, MODEIN and key entries are placed in the acceptance state (OFFHOOK mode). Beep tone (key entry confirmation tone) is output in PULSE mode. The 41 ms typ. beep tone (1kHz square wave) is output when the following keys are pressed. 1. Numerical key entry. 2. First LDT key entry (subsequent LDT key entries are ineffective). 3. Pause key entries: [*] or [P] key. (However, if the first key after OFFHOOK is the PAUSE key, the key entry is ineffective or not accepted.) 4. Redial key entries: [#] or [RED]* key. (They are effective only when the redial key is the first key after OFFHOOK.) 5. PAUSE release key entries: [*], [P], or [RED] key. (They are accepted only during redialing and effective only when MODEOUT is blinking or at a pause time during redialing.) 6. FLASH key entry: [F] key. (For FLASH key entry, the beep tone is output in PULSE and DTMF modes.) When two or more keys are pressed simultaneously, that is, double or multiple key entries, the key entries are ineffective and the beep tone is not output. If DTMF mode tone request is received during a beep tone transmission, the beep tone is terminated even though the duration is 41 ms or shorter and DTMF tone is output. DUAL TONE output time conditions are as follows: 1. 80 ms typ. for redial output. 2. 80 ms typ. when the key entry time is within 130 ms typ. and more than the debouncing time. 3. DUAL TONE output is stopped at once if a key is pressed over 130 ms typ. and released. 4. Signal tone is output from the end of debouncing time until the key is released. 5. When a beep or DTMF tone is not being output, this pin is placed in a high impedance state.

* [RED] = Redial key

7

FUNCTIONAL DESCRIPTIONS

Ordinal Dialing

In the OFFHOOK mode, PULSE/DTMF signals are output according to the key input, regardless of number of key input figures. For the PULSE mode, any number of digital entries with keys 0 to 9. For the DTMF mode, any number of digital entries with keys 0 to 9, [*] and [#].

Up to 26 digits can be stored in the redial memory. In the PULSE mode, a redial digit is counted for any numeric, pause, and LDT entry. In the DTMF mode, a redial digit is counted for any numeric, [*], [#], and [P] entry.

In both the PULSE and DTMF modes, one digit is counted as mode information when MODEIN is used for mode switching. After OFFHOOK, the first numeric entry is counted as mode digit. In the PULSE mode the numeric key is counted as a mode digit. In the DTMF mode, a numeric key, [*], and [#] entry is counted as a mode digit. In either the OFFHOOK or PULSE modes, the mode-information digit is written into the redial memory.

Redialing Function

The redial memory is read out to execute the redialing operation when a redial key is the first key pressed in OFFHOOK state. In the PULSE mode, the redial keys are [#] and [*]. In the DTMF mode, only the [RED] key is accepted for redial.

When 27 or more digits are written into the redial memory, PULSE or DTMF signals that correspond to the key entries are output, but the redialing operation is ineffective because of memory overflow. At this time, even if the first key pressed after the state change from ONHOOK to OFFHOOK is the redial key, the entry is not accepted and the beep tone is not output in either mode of operation.

7

After OFFHOOK, if a numeric or LDT key is the first entry in PULSE mode, or the first entry in the DTMF mode is a numeric, [*], [#] or a single-tone key entry (excluding $\overline{COL4}$), the redial memory is cleared and data is written into memory according to key entry information.

Mixed Redialing

Mixed redialing is executed when the mode is changed from the PULSE to DTMF mode (done by pressing the LDT key), or when MODE is changed during key entries.

If, at redialing, there is a pause before or after mode switching (including LDT), PULSE/DTMF is sent and PULSE/DTMF signals are transmitted after the pause. To redial when there is no pause before or after mode switching (including LDT), all operations must cease after mode switching and a HALT state is enabled. MODEOUT blinks (indicates that mode switching has no automatic pause) and prompts a pause release.

The pause release keys in PULSE mode are [*], [RED], and the [P] key. In the DTMF mode, the [RED] and the [P] keys are used for pause release. PULSE and DTMF signals can now be sent by key entry. The FLASH key, is the only other acceptable entry.

During redial output, the [F] key is the only key entry accepted. The pause release key is only accepted when MODEOUT is blinking or during a pause at redialing.

Mode Switching

During PULSE or TONE transmissions, mode switching by MODEIN is not permitted; after transmission is complete, MODEIN can be used for mode switching.

When PULSE or DTMF modes are switched by MODEIN, one digit is stored into redial memory as mode information. After OFFHOOK, if the first key entry is numeric in the PULSE mode, or a numeric [*] or [#] in the DTMF mode, the mode-information digit is written into redial memory.

In the PULSE mode, after the LDT key is accepted only one time, the DTMF mode is selected (regardless of MODEIN pin switching). The LDT key is not accepted in the DTMF mode. The MODEIN pin switching enables the desired mode of operation to be selected.

Line Dial Tone (LDT) Function

If the LDT key is pressed in the PULSE mode, the DTMF mode is selected and DTMF tones can be output. In PULSE mode, only the first LDT key is accepted after key acceptance state (OFFHOOK mode) is entered. Once the LDT key is accepted, the following LDT key entries are ignored.

When the LDT key is used to enter the DTMF mode, all keys (excluding $\overline{COL4}$ keys) provide dual-tone and single-tone outputs. (Note: If even one $\overline{COL4}$ key is pressed, neither dual nor single tones are output.) The mode after that is not switched. If mode switching by LDT from memory is done during redialing, key entries after redialing are executed in DTMF mode regardless of the MODEIN state and the data is written into the redial memory. However, for effective keys (not the redial key) after ONHOOK changes to OFFHOOK, memory is reset and written in the current mode.

Pause Function

A pause state can be entered by pause key entry.

In the PULSE mode, a pause is introduced by pressing the [#] or [P] keys; in the DTMF mode (including LDT) only the [P] key is effective. If a pause key is the first key pressed after changing from ONHOOK to OFFHOOK, the entry is not accepted. One pause key entry introduces a pause state that is typically 4 seconds; contiguous pause (N X 4 seconds) can be executed by making consecutive key entries. The pause can be reduced by entering [P] or [RED] during a redialing pause time.

In the PULSE mode, the [*] key is used as a pause release key. Multiple pauses can be sent up to 500 times faster by entering a pause release key, that is, N X 4 seconds becomes N X 800 milliseconds.

Flash Function

Keyboard entries enable ONHOOK mode. Only the [F] key is used as a FLASH key in both PULSE and DTMF modes (including LDT).

When the [F] key is pressed, the ONHOOK mode is entered for 600 milliseconds (typical), after beep tone is sent. During this time, the key entry pin is not accepted. MODEIN, $\overline{MUTE}$, MODEOUT, and DTMF/BEEPOUT pins are placed in the high-impedance state and the PULSEOUT pin is set low level. After 600 milliseconds (typical), the return of OFFHOOK is automatic and key entries can again be accepted.

Test (High-speed Mode)

A test mode circuit is built into the IC. In the ONHOOK state, pins OSCIN and OSCOUT are pulled down by a high resistance. To activate the test mode, tie the OSCIN high and apply clock signal to OSCOUT. The internal circuit operates up to 128 times faster than normal operation.

Figure 1. Keyboard Configuration

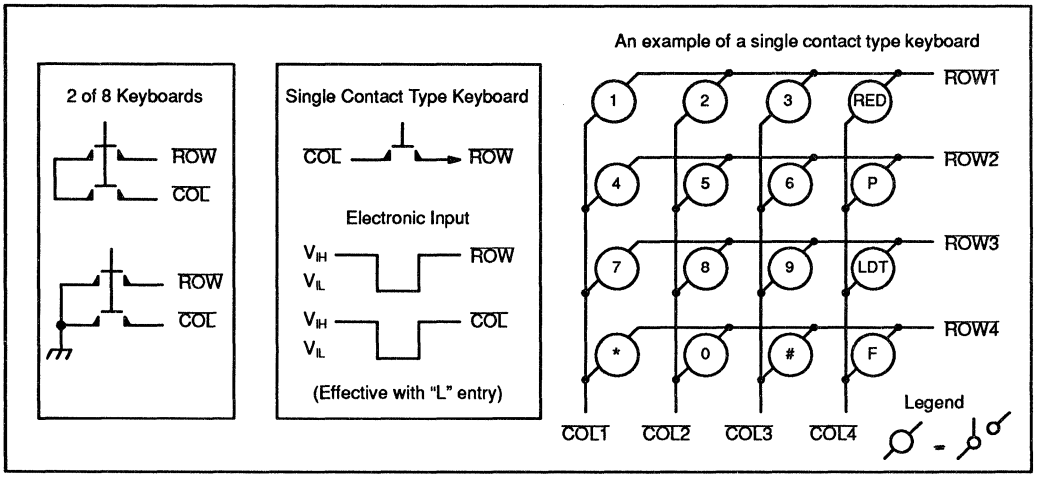
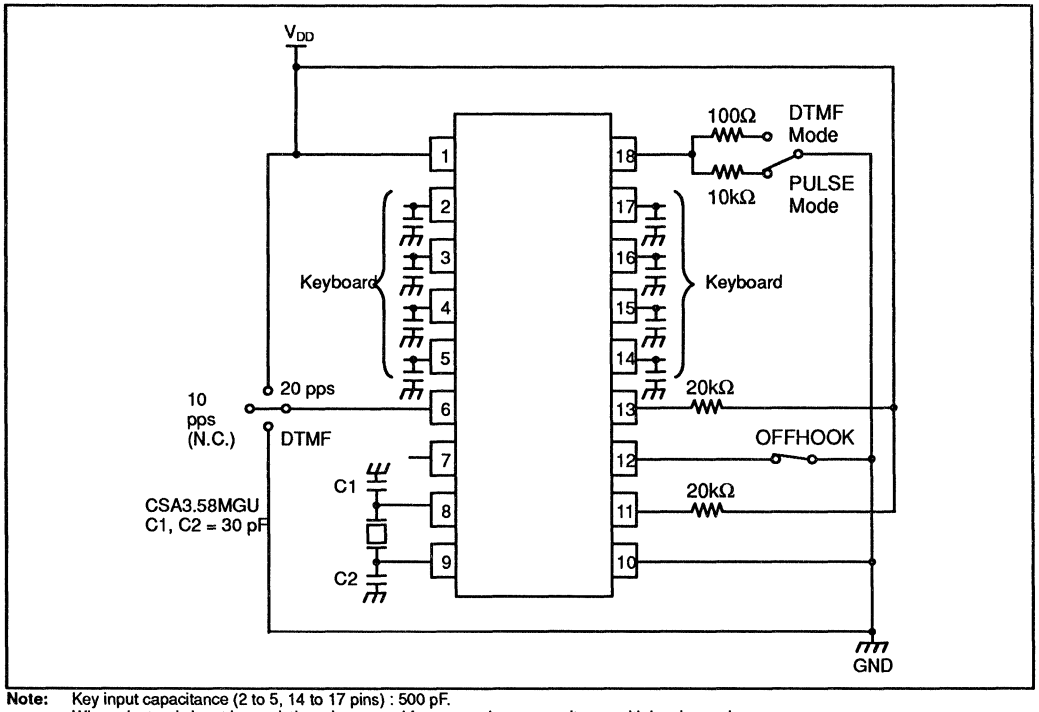


Figure 2. Reference Circuit



Note: Key input capacitance (2 to 5, 14 to 17 pins) : 500 pF.
When electronic input is used, there is no need for connecting a capacitance with key input pins.

KEY OPERATION DIAGRAM

Redial key for PULSE mode	:	[RED (P)] = [RED] or [#]
Redial key for DTMF mode	:	[RED (D)] = [RED]
Pause key for PULSE mode	:	[P (P)] = [P] or [#]
Pause key for DTMF mode	:	[P (D)] = [P]
Pause release key of PULSE mode	:	[PR (P)] = [RED], [P], or [*]
Pause release key of DTMF mode	:	[PR (D)] = [RED] or [P]
Pause output	:	(P) = Pause

KEY ENTRIES IN PULSE MODE

When MODEIN is set to 10 pps

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1] [2]	1–2		
ON					
OFF	OPEN	[RED (P)]	1–2		
		[3]	3		
ON					
OFF	OPEN	[RED (P)]	1–2–3		
ON					
OFF	V_{DD}	[RED (P)]	1–2–3		
ON					
OFF	GND	[RED (D)]	1–2–3		
		[4]			4

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7

KEY ENTRIES IN PULSE MODE

When MODEIN is set to 20 pps

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	V_{DD}	1 2		1–2	
ON					
OFF	V_{DD}	RED (P)		1–2	
		3		3	
ON					
OFF	V_{DD}	RED (P)		1–2–3	
ON					
OFF	OPEN	RED (P)		1–2–3	
ON					
OFF	GND	RED (D)		1–2–3	
		4			4

7

KEY ENTRIES IN DTMF MODE

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	GND	1 2			1–2
ON					
OFF	GND	RED (D)			1–2
		3			3
ON					
OFF	GND	RED (D)			1–2–3
ON					
OFF	OPEN	RED (P)			1–2–3
ON					
OFF	GND	RED (P)			1–2–3
		4		4	

Continued on next page

KEY ENTRIES WHEN THE LDT KEY IS USED

When there is a pause before LDT

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1] [2] [P (P)]	1–2–(P)		3
ON		[LDT] [3]			
OFF	GND	[RED (P)]	1–2–(P)		3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1–2–(P)		3–4
ON					
OFF	GND	[RED (D)]	1–2–(P)		3–4

KEY ENTRIES WHEN THE LDT KEY IS USED

When there is a pause after LDT

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1] [2] [LDT]	1–2		(P)–3
ON		[P (D)] [3]			
OFF	GND	[RED (P)]	1–2		(P)–3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1–2		(P)–3–4
ON					
OFF	GND	[RED (D)]	1–2		(P)–3–4

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7

KEY ENTRIES WHEN THE LDT KEY IS USED

When there is no pause before and after LDT

HOOK	MODEIN	Key Entry	PULSE Output 10pps	PULSE Output 20pps	DTMF Output
ON					
OFF	OPEN	[1] [2]	1–2		
		[LDT] [3]			3
ON					
OFF	OPEN	[RED (P)]	1–2–MODEOUT blinks		
		[PR (D)]			3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1–2–MODEOUT blinks		
		[PR (D)]			3–4
ON					
OFF	GND	[RED (D)]	1–2–MODEOUT blinks		
		[PR (D)]			3–4

7

KEY ENTRIES WHEN PULSE/DTMF MODE IS SWITCHED (MIXED REDIAL)

When there is a pause before mode switching

HOOK	MODEIN	Key Entry	PULSE Output 10pps	PULSE Output 20pps	DTMF Output
ON					
OFF	OPEN	[1] [2] [P (P)]	1–2–(P)		
	V_{DD}	[3] [4] [P (P)]		3–4–(P)	
	GND	[5] [*] [P (D)]			5–*–(P)
	OPEN	[6] [7]	6-7		
ON					
OFF	OPEN	[RED (P)]	1–2–(P) 6-7	3–4–(P)	5–*–(P)
ON					
OFF	V_{DD}	[RED (P)]	1–2–(P) 6–7	3–4–(P)	5–*–(P)
ON					
OFF	GND	[RED (D)]	1–2–(P) 6-7	3–4–(P)	5–*–(P)

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KEY ENTRIES WHEN PULSE/DTMF MODE IS SWITCHED (MIXED REDIAL)

When there is a pause after mode switching

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	1 2	1–2		
	V_{DD}	P (P) 3 4		(P)–3–4	
	GND	P (D) 5 *			(P)–5–*
	OPEN	P (P) 6 7	(P)–6–7		
ON					
OFF	OPEN	RED (P)	1–2 (P)–6–7	(P)–3–4	(P)–5–*
ON					
OFF	V_{DD}	RED (P)	1–2 (P)–6–7	(P)–3–4	(P)–5–*
ON					
OFF	GND	RED (D)	1–2 (P)–6–7	(P)–3–4	(P)–5–*

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7

KEY ENTRIES WHEN PULSE/DTMF MODE IS SWITCHED (MIXED REDIAL)

When there is no pause before and after mode switching

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1] [2]	1–2		
	V_{DD}	[3] [4]		3–4	
	GND	[5] [*]			5–*
	OPEN	[6] [7]	6–7		
ON					
OFF	OPEN	[RED (P)]	1–2–MODEOUT blinks		
		[PR (P)]		3–4–MODEOUT blinks	
		[PR (D)]			5–*–MODEOUT blinks
		[PR (P)]	6–7		
ON					
OFF	V_{DD}	[RED (P)]	1–2–MODEOUT blinks		
		[PR (P)]		3–4–MODEOUT blinks	
		[PR (D)]			5–*–MODEOUT blinks
		[PR (P)]	6–7		
ON					
OFF	GND	[RED (D)]	1–2–MODEOUT blinks		
		[PR (P)]		3–4–MODEOUT blinks	
		[PR (D)]			5–*–MODEOUT blinks
		[PR (P)]	6–7		

7

REDIAL MEMORY INHIBIT FUNCTION

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1][1] ··· [1][1] (25)	1 – 1·····1 – 1 (25)		
ON					
OFF	OPEN	[RED (P)]	1 – 1·····1 – 1 (25)		
ON					
OFF	OPEN	[1][1] ··· [1][1] (26)	1 – 1·····1 – 1 (26)		
ON					
OFF	OPEN	[RED (P)]	No output		
		[2]	2		
ON					
OFF	OPEN	[RED (P)]	2		
ON					
OFF	V_{DD}	[RED (P)]	2		
ON					
OFF	GND	[RED (D)]	2		
		[3]			3
ON					
OFF	OPEN	[LDT] [1][1] ··· [1][1] (25)			1 – 1·····1 – 1 (25)
ON					
OFF	OPEN	[RED (P)]			1 – 1·····1 – 1 (25)
ON					
OFF	OPEN	[1][1] [LDT] [1][1] ··· [1][1] (23)	1 – 1		1 – 1·····1 – 1 (23)
ON					
OFF	OPEN	[RED (P)]	No output		No output

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Condition		Value			Unit
					Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	PULSE mode and memory retention mode		2.0		6.0	V
			DTMF mode		2.5		6.0	V
Input Voltage	V_I	All Inputs			0		V_{DD}	V
Output Load Resistance	R_O	DTMF/ BEEPOUT	Between output pin and GND	DTMF mode	0.1		20	kΩ
				PULSE mode	0.1	10	100	kΩ
Operating Temperature	T_A				–30		60	°C

7

ELECTRICAL CHARACTERISTICS

V_{DD}: PULSE mode = 2.0 to 6.0 V, V_{DD}: DTMF mode = 2.5 to 6.0 V,TA = –30 to 60°C

Parameter	Symbol	Pin Name	Condition		Value Min	Value Typ	Value Max	Unit
Power Supply Current	I_{DD}	V_{DD}	All output pins are open in DTMF mode			2.5	5.0	mA
	I_{DP}		All output pins are open in PULSE mode			1.0	2.0	mA
	I_{DST}		All output pins, HKS pin open in Standby			1.5	10	µA
	I_{DD1}		V_{DD} = 2.5 V	All output pins open in DTMF		1.0	2.0	mA
	I_{DD2}			All output pins open in PULSE		0.3	0.6	mA
	TDST1		TA = 25°C	All output pins HKS open in Standby		0.2	1.0	µA
Digital Input Voltage 1	V_{Ih1}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ to $\overline{ROW4}$			0.8 V_{DD}		V_{DD}	V
	VIL1				0		$\frac{1}{5}$ V_{DD}	V
Digital Input Voltage 2	V_{IH2}	HKS, MODEIN			0.8 V_{DD}		V_{DD}	V
	V_{Il2}				0		$\frac{1}{5}$ V_{DD}	V
Digital Input Current 1	I_{IH1}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$	$V_I = V_{DD}$		–0.01		$\frac{1}{5}$ V_{DD}	mA
	I_{Il1}		V_I = GND		–0.01 V_{DD}		0.01	mA
Digital Input Leakage Current 1	I_{IZ1}		Key entry HZ GND ≤ VI ≤ V_{DD}		–10		10	µA
Digital Input Current 2	I_{IH2}	MODEIN	VI = V_{DD}		–0.01		$\frac{1}{75}$ V_{DD}	mA
	I_{IL2}		VI = GND		–1/75 V_{DD}		0.01	mA
Digital Input Leakage current 2	I_{IZ2}		MODEIN HZ GND ≤ VI ≤ V_{DD}		–10		10	µA
Digital Input Current 3	I_{IH3}	HKS	VI = V_{DD}		–10		10	µA
Pull-up Resistor	R_{PLU}				100	200	400	kΩ

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7

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Digital Output Voltage	V_{OH}	MODEOUT	I_{OH} = –0.2 mA	V_{DD} –0.5		V_{DD}	V
	V_{OL}	MODEOUT, PULSEOUT, MUTE	I_{OL} = 0.5 mA	0		0.5	V
BEEP TONE High Output Voltage	V_{BTOH}	DTMF/BEEPOUT	PULSE mode 100Ω is placed between output pin and GND	V_{DD} –1.0		V_{DD}	V
Digital Output Off Leakage Current	I_{OL}	MUTE, PULSEOUT, MODEOUT	GND ≤ V_O ≤ V_{DD}	–10		10	µA
External Resistance when digital input is open	R_{DIO}	ROW1 TO ROW4 COL1 to COL4 HKS, MODEIN	Resistance connected to external circuit when input is open. The other end of the resistance must be between 0V and V_{DD}.	1			MΩ
Pull-down Resistance	R_{PLD}	OSCIN, OSCOUT	ONHOOK mode	75	150	300	kΩ
Oscillator Frequency	O_{SCIN}				3.579545		MHz
DTMF Output Voltage 100Ω placed between output pin and GND.	A_{OUT}	DTMFOUT	No signal is output		0		V
			Offset voltage when signals are output		0.63 V_{DD} –0.75		V
			DTMF TONE output voltage		1.44		Vp–p
			ROW single tone output voltage		0.64		Vp–p
			COLUMN single tone output voltage		0.80		Vp–p
			COLUMN/ROW tone ratio		2.0		dB
Redial Memory Digit	N_{RKEY}	COL1 to COL4 ROW1 TO ROW4				26	digits
Make Ratio	W_{MAKE}	PULSEOUT	MB87007A		39		%
			MB87008A		33		%
Oscillation Start time	t_{OSS}	OSCIN, OSCOUT		0	8	16	ms
Oscillation Stop time	t_{OSSP}			0	8	16	ms
Key Entry HZ Hold time	t_{HZKH}	COL1 to COL4 ROW1 TO ROW4		0		5	ms

Continued on next page

7

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
MODEIN HZ Hold time	t_{HZMIH}	MODEIN		0		5	ms
MODEOUT HZ Hold time	t_{HZMOH}	MODEOUT		0		5	ms
Key Entry HZ Start time	t_{HZKS}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$		0		5	ms
MODEIN HZ Start time	t_{HZMIS}	MODEIN		0		5	ms
MODEOUT HZ Start time	t_{HZMOS}	MODEOUT		0		5	ms
Pause Time	t_{PAS}	$\overline{PULSEOUT}$, DTMF/BEEPOUT		3.85	4.0	4.15	s
MODEOUT Switch Start time 1	t_{MOC1}	MODEOUT			12		ms
MODEOUT Switch Start time 2	t_{MOC2}			2	5	8	ms
MODEOUT HZ Start Time by F key entry	t_{MOFS}				72		ms
MODEOUT HZ Hold Time by F key entry	t_{MOFH}			0.59	0.6	0.61	s
MODEOUT Blinking Period	t_{MOSI}			0.39	0.4	0.41	s
MODEOUT Change Start time by pause release key entry	t_{MOPS}				28		ms
DTMFOUT Output Start time when mode is switched	t_{MST}	DTMF/BEEPOUT		2	10	15	ms
DTMF Output Start time by pause release key entry	t_{PDT}				39		ms
$\overline{PULSEOUT}$ Output Hold time by F key entry	t_{PUFH}	$\overline{PULSEOUT}$		0.59	0.6	0.61	s
$\overline{PULSEOUT}$ OUTPUT Start time by F key entry	t_{PUFS}				72		ms

Continued on next page

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition		Value Min	Value Typ	Value Max	Unit
Key Entry Width1	t_{WK1}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$			50			ms
Key Entry Width2	t_{WK2}				50			ms
Key Input Pause Time	t_{PK}				50			ms
Key Entry Debouncing time	t_{CH}				21	23	25	ms
Key Entry Release Guard time	t_{RE}				21	23	25	ms
BEEP TONE Output Start time	t_{BES}	DTMF/BEEPOUT				31		ms
BEEP TONE Output Width	t_{WBE}				39	41	43	ms
$\overline{MUTE}$ LOW Output Start time	t_{MUS}	$\overline{MUTE}$				31		ms
$\overline{MUTE}$ LOW Output Hold time 1	t_{MUSP1}		10 pps		26	30	34	ms
			20 pps		13	15	17	
			Dual Tone Output		100	110	120	
Pulse Predigital Pause Time	t_{PDP}	$\overline{PULSEOUT}$	MB87007A	10 pps mode	950	980	1016	ms
				20 pps mode	480	510.5	556	
			MB87008A	10 pps mode	950	974	1016	ms
				20 pps mode	480	507.5	556	
Pulse Make Width	t_{WMA}		MB87007A	10 pps mode	38	39	40	ms
				20 pps mode	19	19.5	20	
			MB87008A	10 pps mode	32	33	34	ms
				20 pps mode	16	16.5	17	
Pulse Break Width	t_{WBR}		MB87007A	10 pps mode	60	61	62	ms
				20 pps mode	30	30.5	31	
			MB87008A	10 pps mode	66	67	68	ms
				20 pps mode	33	33.5	34	
Pulse Interdigital Pause Time	t_{IDP}		MB87007A	10 pps mode	900	939	960	ms
				20 pps mode	450	469.5	480	
			MB87008A	10 pps mode	900	933	960	ms
				20 pps mode	450	466.5	480	

Continued on next page

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
$\overline{\text{MUTE}}$ LOW Output Hold time 2	t_{MUSP2}	$\overline{\text{MUTE}}$	Single Tone Output	0		8	ms
DUAL TONE Output Time	t_{WDT}	DTMF/BEEPOUT		78	80	82	ms
DTMF Interpause Time	t_{DTP}			78	80	82	ms
Single Tone Output start time	t_{SIS}				31		ms
Single Tone Output stop time	t_{SISP}			0		8	ms
DUAL TONE Output start time	t_{DTS}				39		ms
DUAL TONE Output stop time	t_{DTSP}			0		5	ms
$\overline{\text{MUTE}}$ Hold Time 1 by PAUSE key entry	t_{PSM1}	$\overline{\text{MUTE}}$		0	10	20	ms
$\overline{\text{MUTE}}$ Hold Time 2 by PAUSE key entry	t_{PSM2}			75	90	105	ms
MODEOUT Blinking Start time	t_{MOST}	MODEOUT		0	5	10	ms

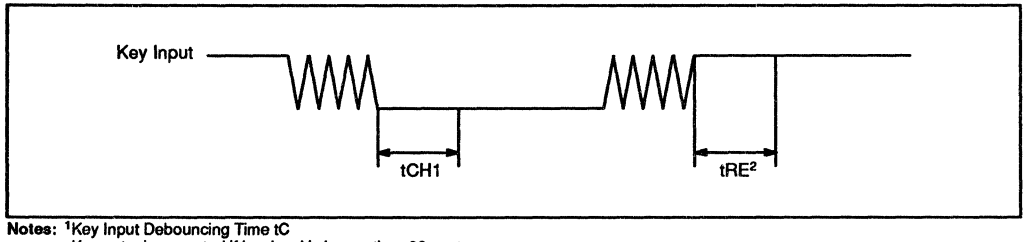
7

DTMF OUTPUT SIGNALS

Item	Symbol	Standard DTMF (Hz)	DTMF Output Signal* (Hz)	Error to Standard TDMF (%)
ROW1	FR1	697	696.95	–0.01
ROW2	FR2	770	770.13	+0.02
ROW3	FR3	852	852.27	+0.03
ROW4	FR4	941	940.99	–0.01
COL1	FC1	1209	1209.31	+0.03
COL2	FC2	1336	1335.65	–0.03
COL3	FC3	1477	1476.71	–0.02

Note: *Oscillation frequency 3.579545 MHz

Figure 4. Key Input Timing



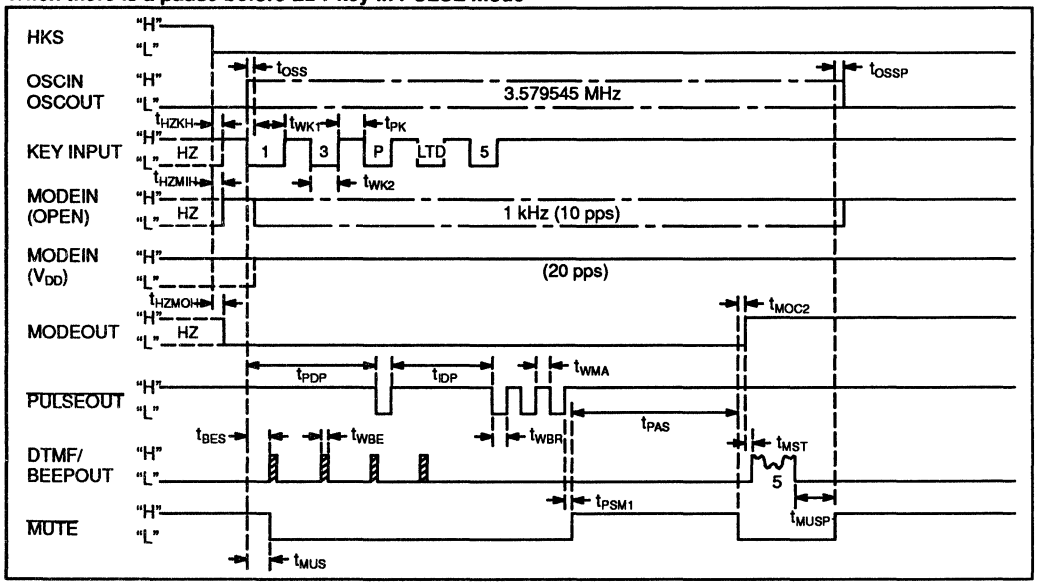
Notes: [1]Key Input Debouncing Time tC
Key entry is accepted if low level is longer than 23 ms typ.

[2]Key Input Release Guard Time tRE
Key release is recognized if low level is longer than 23 ms typ.

7

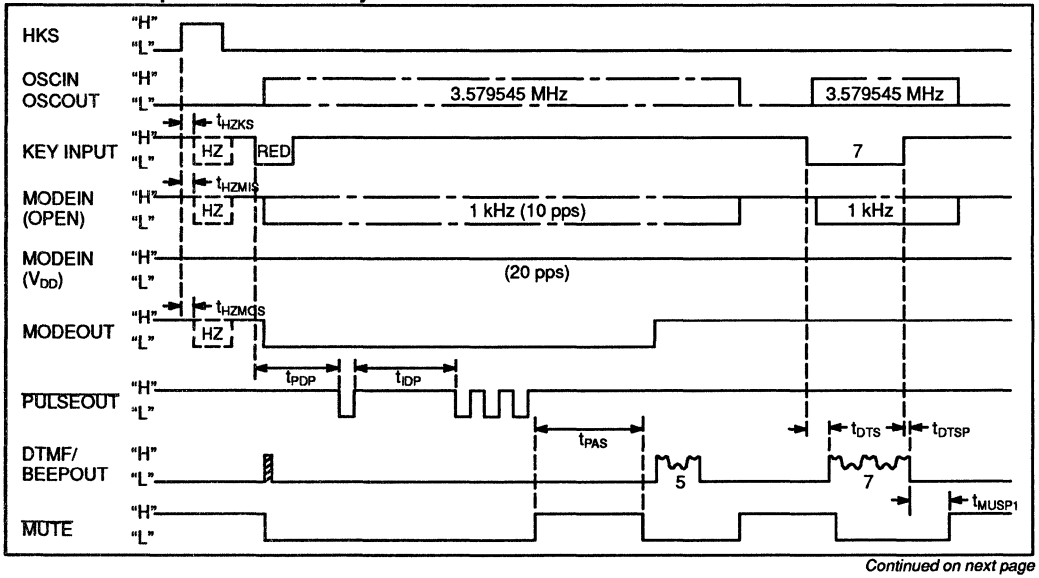
TIMING CHART 1–A

When there is a pause before LDT key in PULSE mode



TIMING CHART 1–B

When there is a pause before LDT key in PULSE mode



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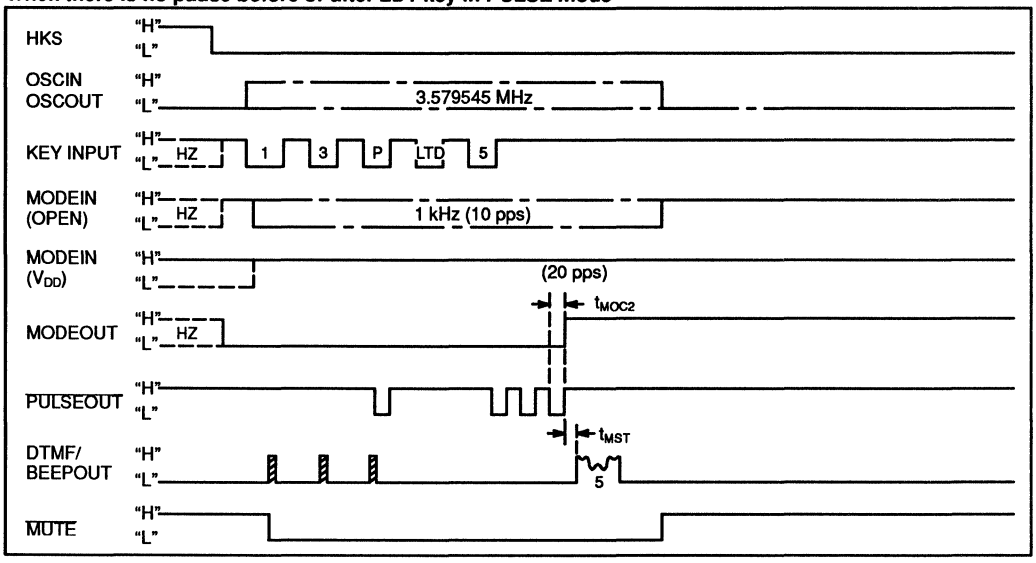
7

TIMING CHART 2–A

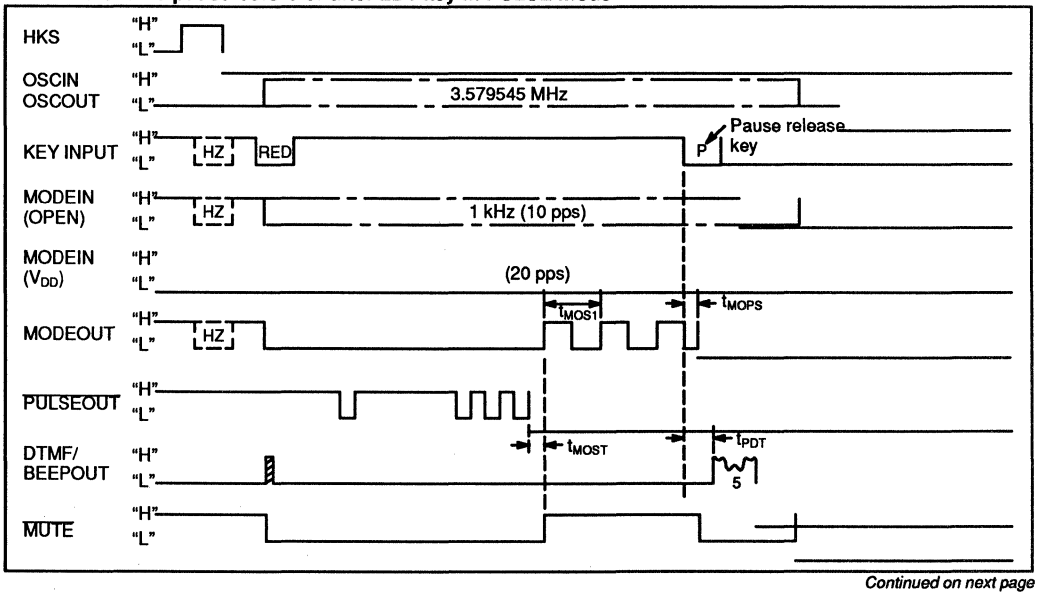
When there is no pause before or after LDT key in PULSE mode



7

TIMING CHART 2–B

When there is no pause before or after LDT key in PULSE mode



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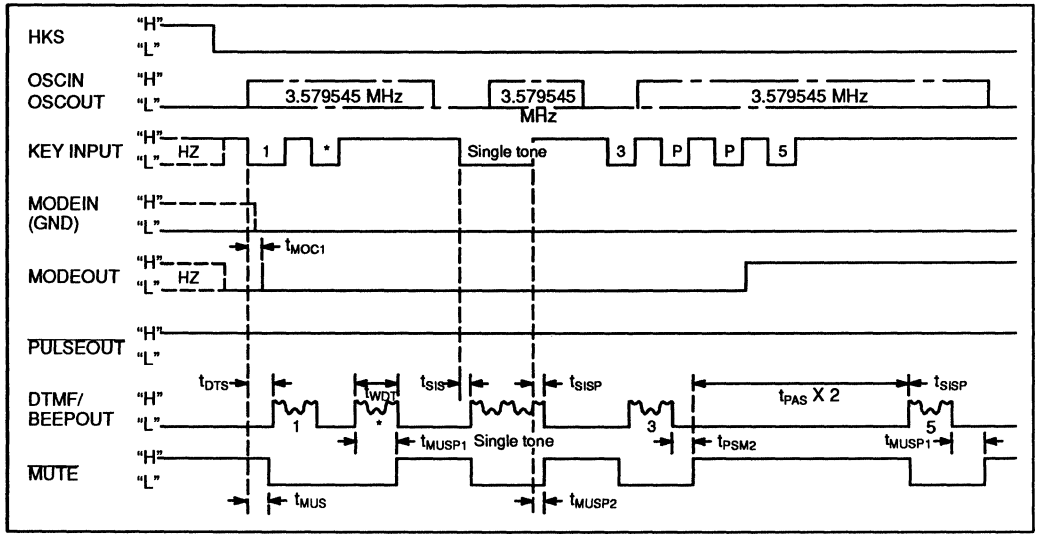
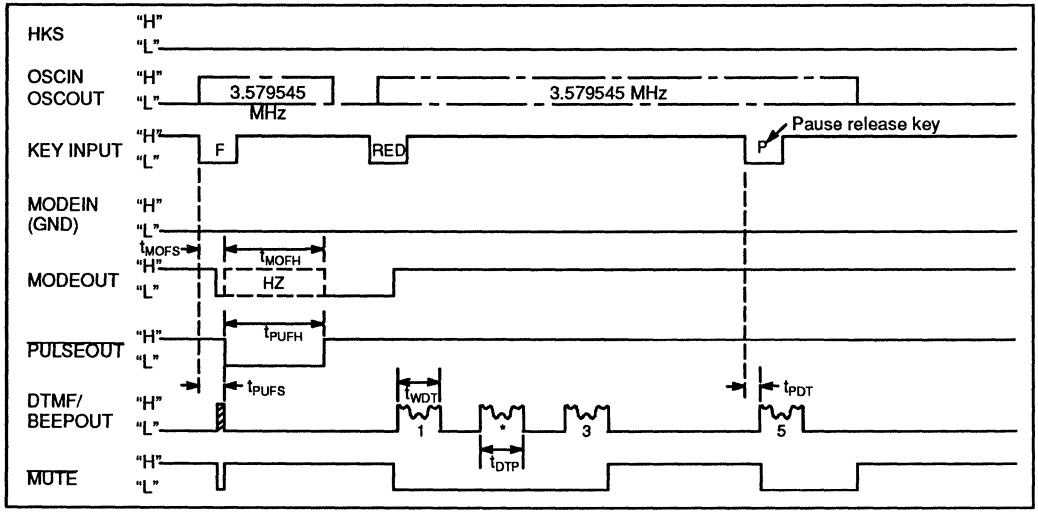
TIMING CHART 3–A

In DTMF mode



TIMING CHART 3–B

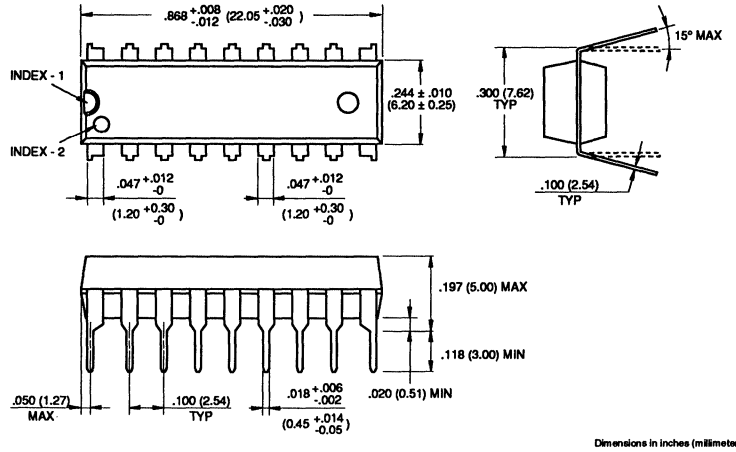
In DTMF mode



7

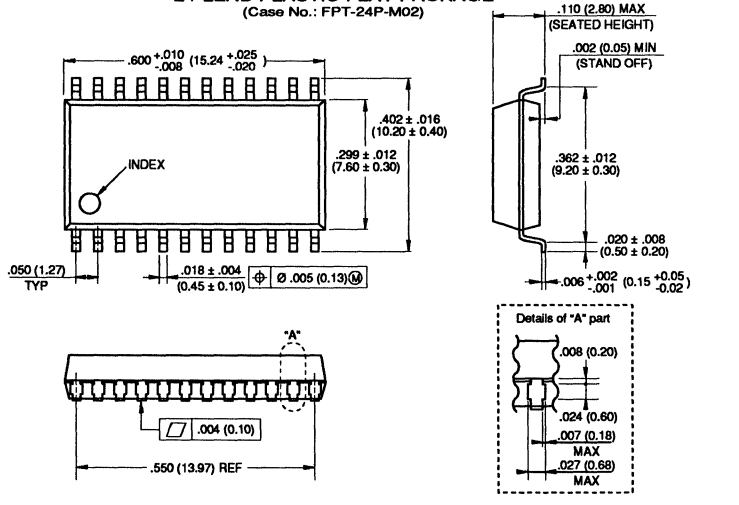
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-18P-M02)



Dimensions in inches (millimeters)

24-LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-24P-M02)



Dimensions in inches (millimeters)

7

June 1991

DATA SHEET

FUJITSU

MB87009

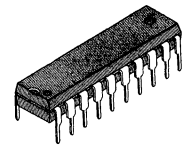
Dual Tone Multi-Frequency/Pulse Dialer

The Fujitsu MB 87009 is an IC for pushbutton telephone sets using Si gate CMOS process and can be used for both DTMF and PULSE modes.

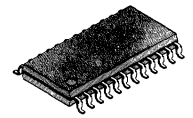
The MB 87009 can be switched from PULSE mode to DTMF mode by mode selection entry or by input from the keyboard.

The MB 87009 contains a 26-digit redial memory, permitting coexistence of PULSE and DTMF modes, enabling mixed redialing in both PULSE and DTMF modes by a single key entry.

- Pulsed 10 pps, 20 pps, or DTMF operation can be selected by the mode switch pin (MODEC).
- 26-digit redial memory is built in (up to 25 digits can actually be written in the memory).
- Selectable make ratio by MA/BR: 39% or 33%.
- LDT function is provided (key entry enables switching from PULSE mode to DTMF mode).
- Beep tone for input confirmation can be output (for all effective key entry independently of PULSE/DEMF mode.
- Redial inhibit function is included for redial memory overflow.
- Mixed redialing of both PULSE and DTMF modes is possible.
- PAUSE function is provided and pause accumulation is possible.
- FLASH function is provided (ONHOOK mode is entered by keyboard entry).
- Crystal or ceramic oscillator (3.579545 MHz) can be used.
- PAUSE release function is provided (two or more consecutive pauses can be released).
- Operating voltage (-30°C to 60°C)
  PULSE mode : 2.0 to 6.0 V
  DTMF mode : 2.5 to 6.0 V

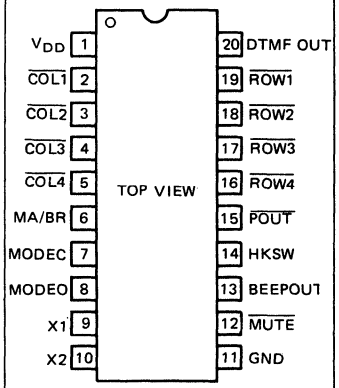


PLASTIC PACKAGE
DIP-20P-M01



PLASTIC PACKAGE
FPT-24P-M02

PIN ARRANGEMENT



ABSOLUTE RATINGS

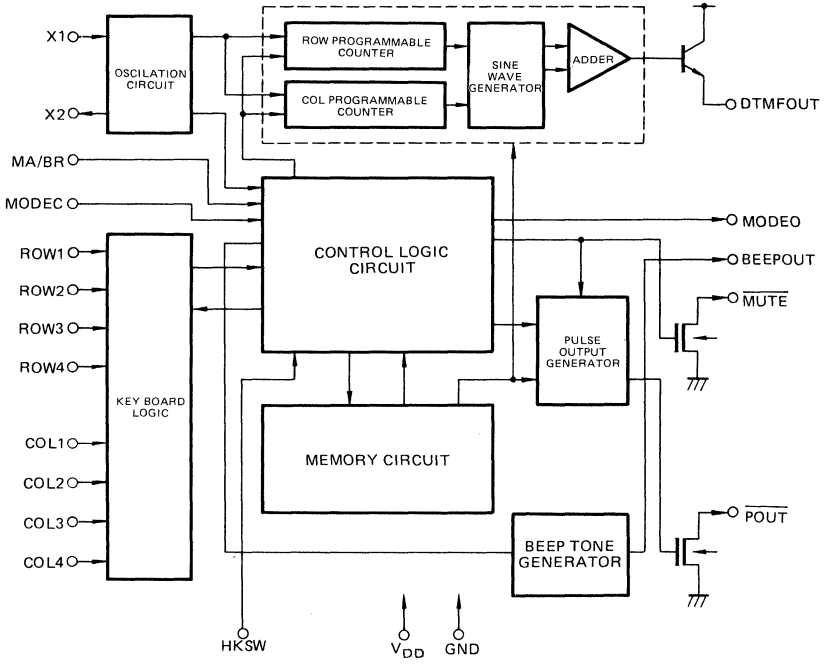
Rating	Symbol	Value	Unit
Power voltage	V_{DD}	GND-0.3 to 7.0	V
Input voltage	V_{IN}	GND-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	GND-0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	-55 to 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

MB 87009 BLOCK DIAGRAM



EXPLANATION OF THE BLOCK DIAGRAM

Setting the HKSW pin from "H" to "L" changes the mode from ONHOOK to OFFHOOK, activating the 3.579545 MHz oscillator and entering a key entry accepting state.

MODEC pin entry in OFFHOOK mode enables selection of PULSE mode 10 pps or 20 pps or DTMF mode. In PULSE mode, DTMF mode can be set by pressing the LDT key.

The keyboard logic circuit discriminates key entry information on $\overline{ROW1}$ to $\overline{ROW4}$ and $\overline{COL1}$ to $\overline{COL4}$ pins, and transmits key information to the control logic circuit after a time interval for debouncing, for effective key entry.

The control logic circuit controls the memory circuit, beep tone generator, pulse output generator, and DTMF output

generator according to key entry information.

The memory circuit contains a 26-digit redial memory. One-touch redialing is possible after mode and key entry information is stored.

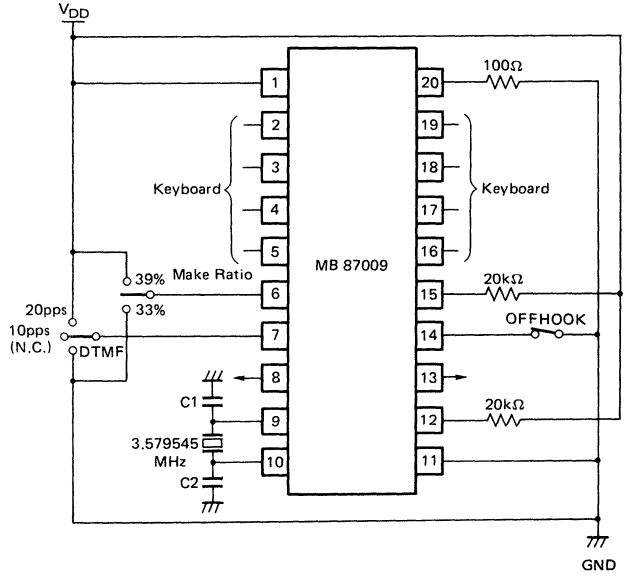
Independently of PULSE/DTMF mode, the beep tone generator operates to output beep tone to the BEEPOUT pin for all effective key entries.

The pulse output generator detects the memory output when the PULSE mode is selected, and outputs to the $\overline{POUT}$ pin as many PULSE signals "L" as the number depending on effective memory data in PULSE mode.

The make rate is 39% when MA/BR is "H", and 33% when "L."

When the DTMF mode is selected, the DTMF output generator outputs DTMF tones from the DTMF OUT pin according to effective memory data output. Row and column program counters and DA converter generate row and column sine wave signals, which are added by the analog adder to generate DTMF tones.

REFERENCE CIRCUIT



7

PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>1</td><td>V_{DD}</td><td rowspan="2">Power supply</td><td rowspan="2">– Voltages
2.0 to 6.0 V in PULSE mode
2.5 to 6.0 V in DTMF mode
2.0 V min. for maintaining memory</td></tr>
<tr><td>11</td><td>GND</td></tr>
<tr><td>2
3
4
5
19
18
17
16</td><td>$\overline{COL1}$
$\overline{COL2}$
$\overline{COL3}$
$\overline{COL4}$
$\overline{ROW1}$
$\overline{ROW2}$
$\overline{ROW3}$
$\overline{ROW4}$</td><td rowspan="2">Input pin</td><td>– Key entries to this IC are from the 2 of 7 or 2 of 8 keyboard using common GND. This IC is available with a single contact (FORM A) type keyboard and electronic input ("L" entry).
– Debouncing time is 34 ms typ. for both PULSE and DTMF.
– Key entry is accepted in PULSE mode only when a single key (one key on the keyboard) is pressed longer than the debouncing time. If two or more keys are pressed, they are not accepted unless they are released one by one and the last key is held closed longer than the debouncing time after all other keys are released.
– Key entry is accepted in DTMF mode only when either a single key (DUAL TONE key) is pressed or two or more keys in the same $\overline{COL}$ or $\overline{ROW}$ (single tone keys) are pressed longer than the debouncing time. However, if even one key is pressed in $\overline{COL4}$, single tone keys are ineffective. When multiple single tone keys are pressed, if they are released one by one and the last key is held closed longer than the debouncing time after all other keys are released, the key is effective as a DUAL TONE key. Hereafter, key entries are described with the premise that keys are held closed longer than the debouncing time.
– Pause between key entries in PULSE and DTMF mode is required to be 50 ms or more. However, for single tone outputs, up to 50 ms is necessary from key entry to output start.
– Key switch contact resistance up to 5 kΩ is allowable.</td></tr>
<tr><td>6</td><td>MA/BR</td><td>– Switch to select make rate as listed below:
<table><tr><th>MA/BR</th><th>Make Rate</th><th>Break Rate</th></tr><tr><td>"V_{DD}"</td><td>39</td><td>61</td></tr><tr><td>"GND"</td><td>33</td><td>67</td></tr></table>– Prohibited to switch it during PULSE/DTMF outputting.
– Input level is CMOS level.</td></tr>
</table>

PIN DESCRIPTION (Cont'd)

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>7</td><td>MODEC</td><td rowspan="4">Input pin</td><td>– Switch to select Pulse 10 pps, 20 pps, or DTMF operation.
The table below shows mode settings.
<table>
<tr><th colspan="2">Mode</th><th>Setting</th></tr>
<tr><td rowspan="2">PULSE mode</td><td>10 pps</td><td>Open (1 MΩ or more)</td></tr>
<tr><td>20 pps</td><td>V_{DD}</td></tr>
<tr><td colspan="2">DTMF mode</td><td>GND</td></tr>
</table>
– When mode switching is requested by MODEC during pulse or tone transmission, the request will not be accepted. The request is accepted by key entry after data transmission.
– In ONHOOK mode, a high impedance (HZ) is set.</td></tr>
<tr><td>14</td><td>HKSW</td><td>– Hook switch entry
<table>
<tr><td>ONHOOK mode</td><td>Open or V_{DD}</td></tr>
<tr><td>OFFHOOK mode</td><td>GND</td></tr>
</table>
– Output inhibit state is entered in ONHOOK mode and $\overline{POUT}$, DTMFOUT, BEEPOUT, MUTE, and MODEO are set to HZ. All key entries are set to HZ and the built-in operational amplifier and oscillator (X1 = "L", X2 = "L") enter power down states in ONHOOK mode.
– This pin is pulled up by a high resistance in the IC.
– The input level is CMOS level.</td></tr>
<tr><td>9</td><td>X1</td><td>– Resonator input pin.
– Pulled down to "L" by a high resistance in ONHOOK mode.
– Both crystal and ceramic resonators are available (3.579545 MHz).</td></tr>
<tr><td>10</td><td>X2</td><td rowspan="2">Output pin</td><td>– Resonator output pin.
– Pulled down to "L" by a high resistance in ONHOOK mode.
– Both crystal and ceramic resonators are availble (3.579545 MHz).</td></tr>
<tr><td>8</td><td>MODEO</td><td>– CMOS output pin which is set to HZ in ONHOOK mode.
– Outputs "L" level in PULSE mode, and "H" level in DTMF mode (including the LDT function).
– Blinks MODEO on and off at a frequency of 2.5 Hz typ. if there is no pause before and after mode switching in redialing function.</td></tr>
</table>

7

PIN DESCRIPTION (Cont'd)

Pin No.	Pin name	I/O	Description
8	MODEO	Output pin	– Independently of PULSE/DTMF mode, the beep tone is output at the BEEPOUT when the FLASH key is pressed. HZ of 0.6 second typ. is output after the beep tone is output. After that, key acceptance state (OFFHOOK mode) is entered.
12	$\overline{\text{MUTE}}$		– NCH open drain output pin. – The following are MUTE pin HZ conditions in PULSE and DTMF modes. (1) When there is no key entry. (2) After the beep tone is output when the FLASH key is pressed (0.6 s typ.) (3) During pause state However, $\overline{\text{MUTE}}$ is "L" while the beep tone is output. (4) During MODEO blinking. – After key entries become effective in PULSE and DTMF modes, the pin level is "L" during output of the beep tone, pulses, or DTMF according to effective key entries.
13	BEEPOUT		– CMOS Three-State Output. High-Impedance when the beep tone is not output. – Independently of PULSE/DTMF mode, the beep for input confirmation is output for all effective key entry. – BEEPTONE is output in 41 ms typ. at 1 kHz in rectangler pulse.
15	$\overline{\text{POUT}}$		– NCH open drain output pin. – HZ in ONHOOK and DTMF modes. – In PULSE mode, this pin is "L" for pulse breaks according to numerical key entries. – In PULSE and DTMF modes, when the FLASH key is pressed, "L" level is output for 0.6 second typ. after the beep tone is sent even during PULSE/DTMF sending, and a key acceptance state (OFFHOOK mode) returns.
20	DTMF OUT		– Bipolar type NPN emitter-follower pin. It can drive a load of 100Ω (between pin and GND). – When an ordinary single key is entered in DTMF mode, DUAL TONE of numerical, [*] , and [#] keys is output ($\overline{\text{COL4}}$ column is not allowed). Pressing two or more keys in the same $\overline{\text{ROW}}$ or $\overline{\text{COL}}$ on the keyboard outputs the single tone in the $\overline{\text{ROW}}$ or $\overline{\text{COL}}$. However, if a key in $\overline{\text{COL4}}$ is pressed, DUAL TONE or single tone in the $\overline{\text{ROW}}$ or $\overline{\text{COL}}$ is not output. – See Section 8.4 for single tone output frequencies.

PIN DESCRIPTION (Cont'd)

Pin No.	Pin name	I/O	Description
20	DTMF OUT	Output pin	– In the FLASH key is pressed during DTMF sending, the beep tone is output at BEEPOUT and subsequent DTMF tones are not output. After beep tone output, nearly ONHOOK mode of 0.6 second typ. is entered, and then, key acceptance state (OFFHOOK mode) is entered. – DUAL TONE output time conditions: 1) 80 ms TYP for redial output. 2) 80 ms TYP when the key entry time is within 130 ms typ. more than the debouncing time. 3) DUAL TONE output stops being generated at once if a key is pressed over 130 ms TYP and released. 4) Single tone is output from the end of debouncing time until the key is released. – HZ when the DTMF tone is not output.

7

OPERATION AND FUNCTION USE CONDITIONS

Ordinary dialing

Dialing is done by entering numerical keys (1 to 0 keys) in PULSE mode and numerical, [*], and [#] keys in DTMF mode regardless of the number of digits of key input in OFFHOOK, PULSE, or DTMF signals according to the key input are output.

The redial memory is 26 digits. A digit is counted for numerical, pause, and [LDT] keys in PULSE mode and for numerical, [*], [#], and [P] keys in DTMF mode.

One digit is counted as mode information for mode switching by MODEC for both PULSE and DTMF modes. The first key after OFFHOOK is counted as one digit as mode information for numerical keys in PULSE mode and numerical, [*], and [#] keys in DTMF mode, and is written into the redial memory.

Redial function

The redial memory is read to execute redialing only if the redial key is the first key pressed in OFFHOOK state.

The redial key, [*], and [RED] keys are used in PULSE mode and only the [RED] key in DTMF mode.

When 27 or more digits are written into the redial memory, PULSE or DTMF signals corresponding to the key entries are output, but the redialing operation is ineffective because of memory overflow. At this time, even if the first key pressed after the state changes from ONHOOK to OFFHOOK is the redial key, the redial key is not accepted and the beep tone is not output regardless of PULSE or DTMF mode.

If a numerical or [LDT] key is the first key entry in PULSE mode after OFFHOOK or a numerical, [*], [#], or single-tone key (excluding COL4) in DTMF mode, the memory is reset and data is written into the redial memory according to key entry information.

Mix redial function

If the mode is changed from PULSE to DTMF mode by pressing the [LDT] key, or MODEC is switched during key entries, mix redialing is executed.

If there is a pause before or after mode switching (including the LDT function) at redialing, PULSE/DTMF is sent and DTMF/PULSE signals are sent after the pause. However, for redialing in which there is no pause before or after mode switching (including the LDT function), the operation stops immediately after mode switching and a HALT state is entered. MODEO blinks to indicate that the mode switching has no auto pause, prompting pause release. The pause release key at this time is [*], [RED], and [P] keys in PULSE mode, and [RED] and [P] keys in DTMF mode. By key entry, the operation sending subsequent PULSE/DTMF signals is returned. Key entries other than the above are not accepted, except the [F] key.

Key entries are not accepted during redial output, except the [F] and pause release keys (only when MODEO is blinking or during a pause at redialing).

Mode switching
When mode switching is requested by MODEC during pulse or tone transmission, the request will not be accepted. The request becomes acceptable after data transmission.

One digit is used as mode information in both PULSE and DTMF modes when the mode is switched by MODEC. If the first key entry is a numerical in PULSE mode after OFFHOOK or a numerical, [*], [#] in DTMF mode, mode information is written into redial memory.

In PULSE mode, the [LDT] key is accepted only once. After that, DTMF mode is fixed regardless of MODEC pin switching.
In DTMF mode, the [LDT] key is not accepted. MODEC pin switching enables the desired mode to be selected.

LDT function
If the [LDT] key is pressed in PULSE mode, the mode changes to DTMF mode in which DTMF tones can be sent. "In PULSE mode, only first [LDT] key is accepted after key acceptance state (OFFHOOK mode) is entered. Once [LDT] key is accepted, the following [LDT] key entries are ignored.

When DTMF mode is entered by the [LDT] key, dual tones of keys, excepting $\overline{COL4}$ and single tones, can be output. (If even one $\overline{COL4}$ key is pressed, dual and single tones on the $\overline{ROW}$ or $\overline{COL}$ are not sent.) The mode after that is not switched. If mode switching by LDT from memory is done during redialing, key entries after redialing are executed in DTMF mode regardless of the MODEC state and the data is additionally written into the redial memory. However, for effective keys other than the redial key after ONHOOK changes to OFFHOOK memory is reset and written in the current mode.

PAUSE function
A pause state can be entered by pause key entry.

In PULSE mode, both [*] and [P] keys can be used as the pause key. In DTMF mode (including the LDT function), only the [P] key is used.

If the pause key is the first key pressed after ONHOOK changes to OFFHOOK, the key is not accepted.

One pause key entry can make a 4.0 second typ. pause state. N x 4.0 second typ. pauses can be made by multiple consecutive pause key entries.

Pause duration can be reduced by entering [P] and [RED] keys during redialing pause time. In PULSE mode, the [*] key can also be used as a pause release key.

When multiple consecutive pauses are written, the consecutive pauses are all sent fast by entering a pause release key. (N x 4.0 second typ. pause time becomes N x 8.0 ms pause time because the pauses are sent at a speed up to 500 times as fast.)

FLASH function
Keyboard entries enable ONHOOK mode. Only the [F] key is used as a FLASH key in both PULSE and DTMF modes (including the LDT function). When the [F] key is pressed, ONHOOK mode is entered for 0.6 second TYP after the beep tone is sent. The key entry pin, MODEC, $\overline{MUTE}$, DTMF-$\overline{OUT}$, and BEEPOUT during the time become HZ and the $\overline{POUT}$ pin outputs level "L". OFFHOOK mode returns after 0.6 second typ., and key entries can be accepted.

TEST MODE (High speed mode) function
TEST MODE circuit is built into the chip. At ONHOOK, X1 and X2 are pulled down by high resistances. By making the X1 pin "H" and entering a clock from the X2 pin, TEST MODE is enabled to operate internal circuits up to 128 times as fast.

KEY OPERATION DIAGRAM

Redial key: [RED (P)] = [RED] or [#]
[RED (D)] = [RED]

Pause key: [P (P)] = [P] or [*]
[P (D)] = [P]

Pause release key: [PR (P)] = [RED], [P], or [*]
[RED (D)] = [RED] or [P]

Ⓟ = Pause

Key Entries In PULSE Mode

When MODEC is set to 10 pps

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2]	1-2		
ON					
OFF	OPEN	[RED (P)]	1-2		
		[3]	3		
ON					
OFF	OPEN	[RED (P)]	1-2-3		
ON					
OFF	V_{DD}	[RED (P)]	1-2-3		
ON					
OFF	GND	[RED (D)]	1-2-3		
		[4]			4

7

When MODEC is set to 20 pps

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	V_{DD}	[1] [2]		1-2	
ON					
OFF	V_{DD}	[RED (P)]		1-2	
		[3]		3	
ON					
OFF	V_{DD}	[RED (P)]		1-2-3	
ON					
OFF	OPEN	[RED (P)]		1-2-3	
ON					
OFF	GND	[RED (D)]		1-2-3	
		[4]			4

7

Key Entries In DTMF Mode

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	GND	[1] [2]			1-2
ON					
OFF	GND	[RED (D)]			1-2
		[3]			3
ON					
OFF	GND	[RED (D)]			1-2-3
ON					
OFF	OPEN	[RED (D)]			1-2-3
ON					
OFF	V_{DD}	[RED (P)]			1-2-3
		[4]		4	

Key Entries When The LDT Key Is Used

When there is a pause before LDT

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2] [P (P)]	1-2-Ⓟ		
		[LDT] [3]			3
ON					
OFF	OPEN	[RED (P)]	1-2-Ⓟ		
					3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1-2-Ⓟ		
					3-4
ON					
OFF	GND	[RED (D)]	1-2-Ⓟ		
					3-4

When there is a pause after LDT

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2] [LDT]	1-2		
		[P (D)] [3]			Ⓟ-3
ON					
OFF	OPEN	[RED (P)]	1-2		
					Ⓟ-3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1-2		
					Ⓟ-3-4
ON					
OFF	GND	[RED (D)]	1-2		
					Ⓟ-3-4

7

When there is no pause before and after LDT

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2]	1-2		
		[LDT] [3]	MODEO blinks ↓		3
ON					
OFF	OPEN	[RED (P)]	1-2		
		[PR (D)]			3
		[4]	MODEO blinks ↓		4
ON					
OFF	V_{DD}	[RED (P)]	1-2		
		[PR (D)]	MODEO blinks ↓		3-4
ON					
OFF	GND	[RED (D)]	1-2		
		[PR (D)]			3-4

7

Key Entries When PULSE/DTMF Mode Is Switched (Mix Redial)

When there is a pause before mode switching

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2] [P (P)]	1-2-Ⓟ		
	V_{DD}	[3] [4] [P (P)]		3-4-Ⓟ	
	GND	[5] [*] [P (D)]			5-*-Ⓟ
	OPEN	[6] [7]	6-7		
ON					
OFF	OPEN	[RED (P)]	1-2-Ⓟ		
				3-4-Ⓟ	
			6-7		5-*-Ⓟ
ON					
OFF	V_{DD}	[RED (P)]	1-2-Ⓟ		
				3-4-Ⓟ	
			6-7		5-*-Ⓟ
ON					
OFF	GND	[RED (D)]	1-2-Ⓟ		
				3-4-Ⓟ	
			6-7		5-*-Ⓟ

When there is a pause after mode switching

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2]	1-2		
	V_{DD}	[P (P)] [3] [4]		Ⓟ-3-4	
	GND	[P (D)] [5] [*]			Ⓟ-5-*
	OPEN	[P (P)] [6] [7]	Ⓟ-6-7		
ON					
OFF	OPEN	[RED (P)]	1-2		
				Ⓟ-3-4	
					Ⓟ-5-*
			Ⓟ-6-7		
ON					
OFF	V_{DD}	[RED (P)]	1-2		
				Ⓟ-3-4	
					Ⓟ-5-*
			Ⓟ-6-7		
ON					
OFF	GND	[RED (D)]	1-2		
				Ⓟ-3-4	
					Ⓟ-5-*
			Ⓟ-6-7		

7

When there is no pause before and after mode switching

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON					
OFF	OPEN	[1] [2]	1-2		
	V_{DD}	[3] [4]		3-4	
	GND	[5] [*]			5-*
	OPEN	[6] [7]	6-7		
ON			MODEO blinks ↓		
OFF	OPEN	[RED (P)]	1-2	MODEO blinks ↓	
		[PR (P)]		3-4	MODEO blinks ↓
		[PR (D)]			5-*
		[PR (P)]	6-7		
ON			MODEO blinks ↓		
OFF	V_{DD}	[RED (P)]	1-2	MODEO blinks ↓	
		[PR (P)]		3-4	MODEO blinks ↓
		[PR (D)]			5-*
		[PR (P)]	6-7		
ON			MODEO blinks ↓		
OFF	GND	[RED (D)]	1-2	MODEO blinks ↓	
		[PR (P)]		3-4	MODEO blinks ↓
		[PR (D)]			5-*
		[PR (P)]	6-7		

7

Redial Memory Inhibit Function

Hook	MODEC	Key entry	PULSE output		DTMF output
			10 pps	20 pps	
ON → OFF	OPEN	[1] [1] ... [1] [1] (25)	1-1 ... 1-1 (25)		
ON → OFF	OPEN	[RED (P)]	1-1 ... 1-1 (25)		
ON → OFF	OPEN	[1] [1] ... [1] [1] (26)	1-1 ... 1-1 (26)		
ON → OFF	OPEN	[RED (P)]	Not output		
		[2]	2		
ON → OFF	OPEN	[RED (P)]	2		
ON → OFF	V_{DD}	[RED (P)]	2		
ON → OFF	GND	[RED (D)]	2		
		[3]			3
ON → OFF	OPEN	[LDT] [1] [1] ... [1] [1] (25)			1-1 ... 1-1 (25)
ON → OFF	OPEN	[RED (P)]			1-1 ... 1-1 (25)
ON → OFF	OPEN	[1] [1] [LDT] [1] [1] ... [1] [1] (23)	1-1		1-1 ... 1-1 (23)
ON → OFF	OPEN	[RED (P)]	No output		No output

7

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Condition	Value			Unit
			Min.	Typ	Max	
Power voltage	V_{DD}	In PULSE mode and when memory is maintained	2.0	–	6.0	V
		In DTMF mode	2.5	–	6.0	V
Input voltage	V_{IN}		0	–	V_{DD}	V
Output load condition	RO	Between output pin and GND	0.1	–	20	kΩ
Ambient temperature	T_A		-30	–	60	°C

7

Electrical Characteristics

(V_{DD} 2.0 to 6.0 V in PULSE mode, 2.5 to 6.0 V in DTMF mode; T_A = -30 to 60°C)

Parameter	Condition		Pin name	Symbol	Value			Unit
					Min	Typ	Max	
Supply Current	All output pins are OPEN in DTMF mode.		V_{DD}	I_{DD}	–	2.5	5.0	mA
	All output pins are OPEN in PULSE mode.			I_{DDP}	–	1.0	2.0	mA
	All output pins and HKSW pins are OPEN in standby state.			I_{DDSB}	–	1.5	10	μA
	V_{DD} = 2.5V, T_A = 25°C	Output pins are OPEN in DTMF mode.		I_{DDL}	–	1.0	2.0	mA
		Output pins are OPEN in PULSE mode.		I_{DDPL}	–	0.3	0.6	mA
		Output pins and HKSW pin are OPEN in stand-by state.		I_{DDSBL}	–	0.2	1.0	μA
Digital Input Voltage 1			$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	V_{IHI}	4/5 X V_{DD}	–	V_{DD}	V
				V_{ILI}	0	–	V_{DD} /5	V

Electrical Characteristics (Cont'd)

Parameter	Condition	Pin name	Symbol	Value Min	Value Typ	Value Max	Unit
Digital Input Voltage 2		HKSW, MODEC, MA/BR	V_{IH2}	4/5 X V_{DD}	–	V_{DD}	V
			V_{IL2}	0	–	V_{DD} /5	V
Digital Input Current 1	When $V_{IN} = V_{DD}$	$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	I_{IH1}	-0.01	–	V_{DD} /5	mA
	When V_{IN} = GND		I_{IL1}	$-V_{DD}$ /100	–	0.01	mA
Digital Input Leakage 1	When key entry is HZ $GND \leqq V_{IN} \leqq V_{DD}$		I_{ILK1}	-10	–	10	μA
Digital Input Current 2	When $V_{IN} = V_{DD}$	MODEC	I_{IH2}	-0.01	–	V_{DD} /75	mA
	When V_{IN} = GND		I_{IL2}	$-V_{DD}$ /75	–	0.01	mA
Digital Input Leakage 2	When MODEC is HZ $GND \leqq VIN \leqq V_{DD}$		I_{ILK2}	-10	–	10	μA
Digital Input Current 3	When $V_{IN} = V_{DD}$	HKSW, MA/BR	I_{IH3}	-10	–	10	μA
Pull-up Resistance		HKSW	R_{PLU}	100	200	400	kΩ
Digital Input Leakage 3	When V_{IN} = GND	MA/BR	I_{ILK3}	-10	–	10	μA
Digital Output Voltage	When I_{OH} = -0.2 mA	MODEO, BEEP OUT	V_{OH}	V_{DD} -0.5	–	V_{DD}	V
	When I_{OL} = 0.5 mA	$\overline{MODEO}$, $\overline{POUT}$, $\overline{MUTE}$, BEEP OUT	V_{OL}	0	–	0.5	V
Digital Output Off Leakage Current	$GND \leqq V_{OUT} \leqq V_{DD}$	$\overline{MUTE}$, $\overline{POUT}$, MODEO, BEEP OUT	I_{OFFLK}	-10	–	10	μA
External resistance when digital input is open	Resistance connected to external circuit when input is open. The other end of the resistance must be between 0 V and V_{DD}.	$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$, HKSW, MODEC	R_{DEXT}	1	–	–	MΩ

7

Electrical Characteristics (Cont'd)

Parameter	Condition	Pin name	Symbol	Value Min	Value Typ	Value Max	Unit
Pull-down Resistance	In ONHOOK mode	X1, X2	R_{PLD}	75	150	300	kΩ
Oscillator Frequency			f_{IN}	–	3.579545	–	MHz
DTMF output – When 100Ω is connected between output pin and GND	When no signal is output.	DTMF OUT	V_{AOUT}	–	0	–	V
	Offset voltage when signals are output.			–	$0.63 \times V_{DD}$ -0.75	–	V
	DTMF TONE output voltage			–	1.44	–	Vp-p
	ROW signal tone output voltage			–	0.64	–	Vp-p
	COLUMN single tone output voltage			–	0.80	–	Vp-p
	COLUMN/ROW TONE ratio			–	2.0	–	dB
Number of Redial Memory Digits		$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	N_{KEY}	–	–	26	digits
Make Ratio	MA/BR = V_{DD}	$\overline{POUT}$		–	39	–	%
	MA/BR = GND			–	33	–	%
Oscillation Start Time		X1, X2	t_{START}	0	8	16	ms
Oscillation Stop Time			t_{STOP}	0	8	16	ms
Key Entry HZ Hold Time		$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	t_{HZK}	0	–	5	ms
MODEC HZ Hold Time		MODEC	t_{HZMC}	0	–	5	ms
MODEO HZ Hold Time		MODEO	t_{HZMO}	0	–	5	ms
Key Entry HZ Start Time		$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	t_{ZKS}	0	–	5	ms
MODEC HZ Start Time		MODEC	t_{ZMCS}	0	–	5	ms

7

Electrical Characteristics (Cont'd)

Parameter	Condition	Pin name	Symbol	Value Min	Value Typ	Value Max	Unit
MODEO HZ Start Time		MODEO	t_{ZMOS}	0	–	5	ms
MODEO Switch Start Time 1			t_{MOSW1}	–	12	–	ms
MODEO Switch Start Time 2			t_{MOSW2}	–	5	–	ms
MODEO HZ Start Time by F Key Entry			t_{ZMOSF}	–	83	–	ms
MODEO HZ Hold Time by F Key Entry			t_{HZMOSF}	–	0.6	–	s
MODEO Blinking Period			t_{MOBLNK}	–	0.4	–	s
MODEO Switch Start Time by Pause Release Key			t_{MOSWPL}	–	39	–	ms
Pause Time		$\overline{POUT}$, DTMFOUT	t_{PAUSE}	–	4.0	–	s
DTMF Output Start Time by Pause Release Key		DTMFOUT	t_{OUTPL}	–	50	–	ms
$\overline{POUT}$ Output Hold Time by F Key Entry		$\overline{POUT}$	t_{HPH}	–	0.6	–	ms
$\overline{POUT}$ Output Start Time by F Key Entry			t_{POUTS}	–	83	–	ms
DTMFOUT Output Start Time when the Mode is Switched		DTMFOUT	t_{OUTSWS}	–	10	–	ms
Key Entry Width 1		$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	t_{WK1}	50	–	–	ms
Key Entry Width 2			t_{WK2}	50	–	–	ms
Pause Between Key Entries			t_{PK}	50	–	–	ms

7

ElectricalCharacteristics (Cont'd)

Parameter	Condition		Pin name	Symbol	Value Min	Value Typ	Value Max	Unit
Key Entry Debouncing Time			$\overline{COL1}$ to $\overline{COL4}$, $\overline{ROW1}$ to $\overline{ROW4}$	t_{ACHAT}	–	34	–	ms
BEEPTONE Output Start Time			BEEPOUT	t_{BEEPS}	–	42	–	ms
BEEPTONE Output Width				t_{WBEEP}	–	41	–	ms
$\overline{MUTE}$ LOW Output Start Time			$\overline{MUTE}$	t_{MS}	–	42	–	ms
$\overline{MUTE}$ LOW Output Hold Time 1	For 10 pps			t_{HML1}	26	30	34	ms
	For 20 pps				13	15	17	
	When DUAL TONE is output				100	110	120	
Pulse Pre-digital Pause	MA/BR = "VDD"	For 10 pps	$\overline{POUT}$	t_{PPDP}	950	990	1016	
		For 20 pps			480	520.5	566	
	MA/BR = "GND"	For 10 pps			950	984	1016	
		For 20 pps			480	517.5	556	
Pulse Make Width	MA/BR = "VDD"	For 10 pps		t_{WM}	–	39	–	ms
		For 20 pps			–	19.5	–	
	MA/BR = "GND"	For 10 pps			–	33	–	ms
		For 20 pps			–	16.5	–	
Pulse Break Width	MA/BR = "VDD"	For 10 pps		t_{WBRK}	–	61	–	ms
		For 20 pps			–	30.5	–	
	MA/BR = "GND"	For 10 pps			–	67	–	ms
		For 20 pps			–	33.5	–	
Pulse Inter-digital Pause	MA/BR = "VDD"	For 10 pps		t_{WIDP}	900	469.5	960	ms
		For 20 pps			450	469.5	480	
	MA/BR = "GND"	For 10 pps			900	933	960	ms
		For 20 pps			450	466.5	480	

7

Electrical Characteristics (Cont'd)

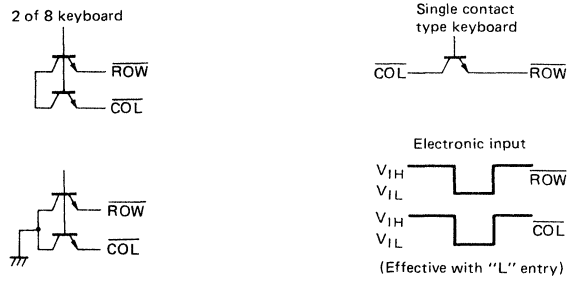
Parameter	Condition	Pin name	Symbol	Value			Unit
				Min	Typ	Max	
$\overline{\text{MUTE}}$ LOW Output Hold Time 2	When single tone is output	$\overline{\text{MUTE}}$	t_{HML2}	0	–	45	ms
DUALTONE Output Time		DTMFOUT	t_{WDT}	78	80	82	ms
DTMF Inter-pause			t_{INPS}	78	80	82	ms
Single Tone Output Start Time			t_{SINGS}	–	42	–	ms
Single Tone Output Stop Time			t_{SINGE}	0	–	5	ms
DUALTONE Output Start Time			t_{DUALS}	–	50	–	ms
DUALTONE Output Stop Time			t_{DUALE}	0	–	5	ms
$\overline{\text{MUTE}}$ Hold Time 1 by Pause Key		$\overline{\text{MUTE}}$	t_{PSM1}	0	10	20	ms
$\overline{\text{MUTE}}$ Hold Time 2 by Pause Key			t_{PSM2}	75	90	105	ms
MODEO Blinking Start Time		MODEO	t_{MOBS}	0	5	10	ms

7

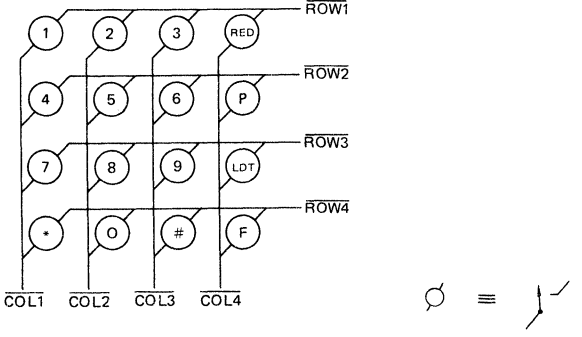
DTMF OUTPUT SIGNALS

Item	Symbol	Standard DTMF (Hz)	DTMF output signals (Hz) (Oscillator frequency 3.579545 MHz)	Error to standard DTmF (%)
ROW1	FR1	697	696.95	-0.01
ROW2	FR2	770	770.13	+0.02
ROW3	FR3	852	852.27	+0.03
ROW4	FR4	941	940.99	-0.01
COL1	FC1	1209	1209.31	+0.03
COL2	FC2	1336	1335.65	-0.03
COL3	FC3	1477	1476.71	-0.02

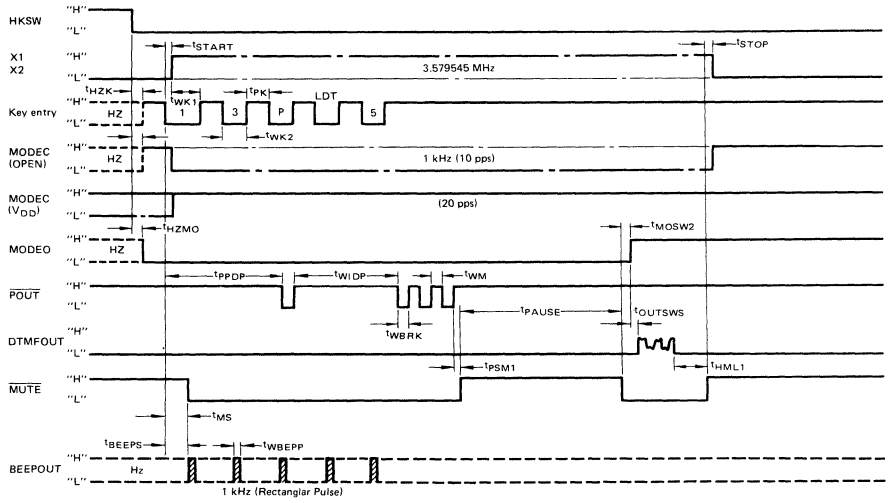
KEYBOARD CONFIGURATION



An example of a single contact type keyboard is shown below.

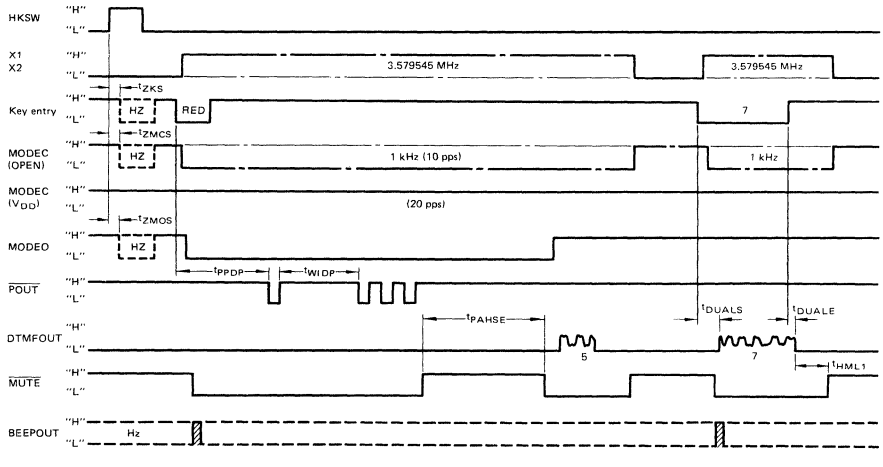


Timing chart 1-A (When there is a pause before LDT in PULSE mode)



NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

Timing chart 1-B (When there is a pause before LDT in PULSE mode)
Key entries in Timing chart 1-A are written as memory data.



NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

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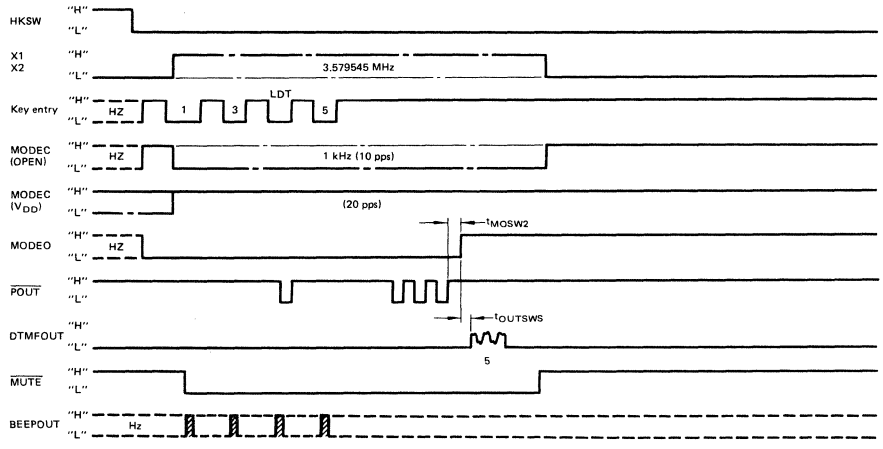
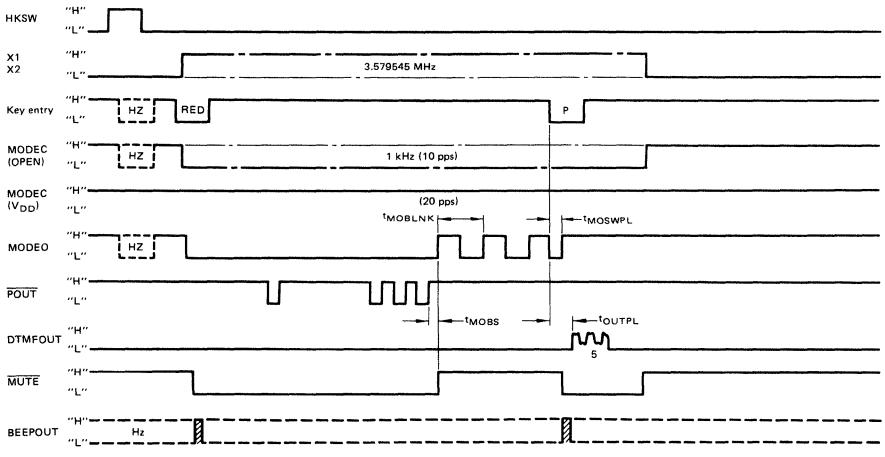
Timing chart 2-A (When there is no pause before or after LDT in PULSE mode)



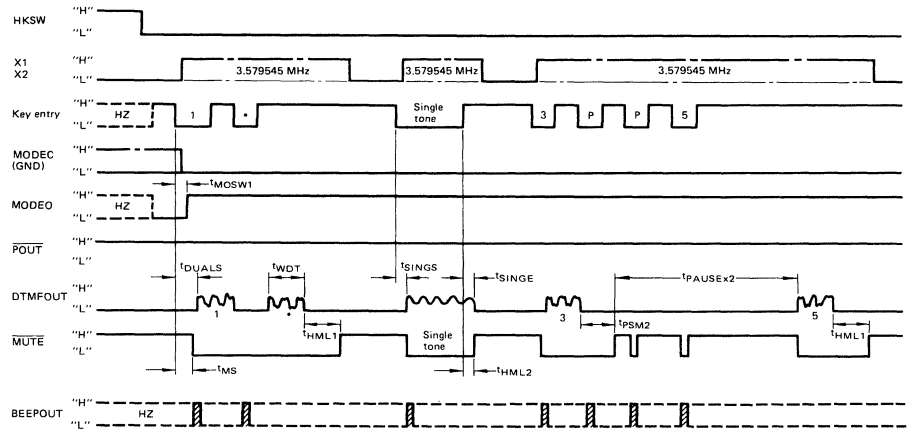
NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

Timing chart 2-B (When there is no pause before or after LDT in PULSE mode)
Key entries in Timing chart 2-A are written as memory data.



NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

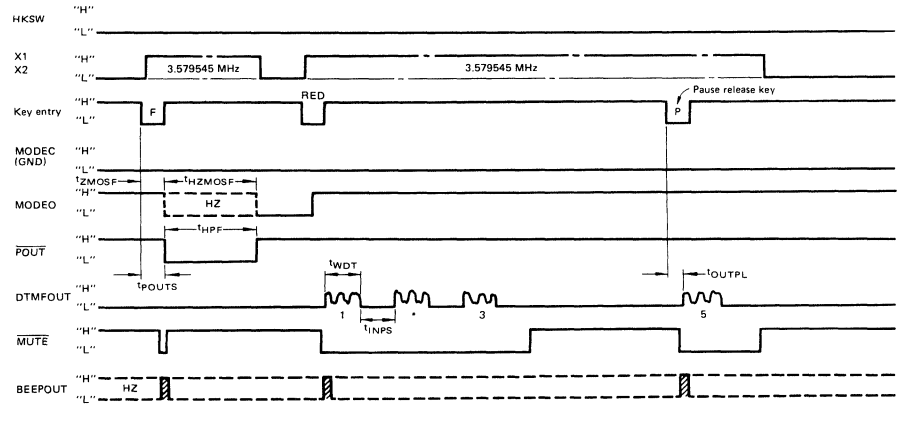
Timing chart 3-A (in DTMF mode)



NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

Timing chart 3-B (in DTMF mode)

Key entries in Timing chart 3-A are written as memory data.

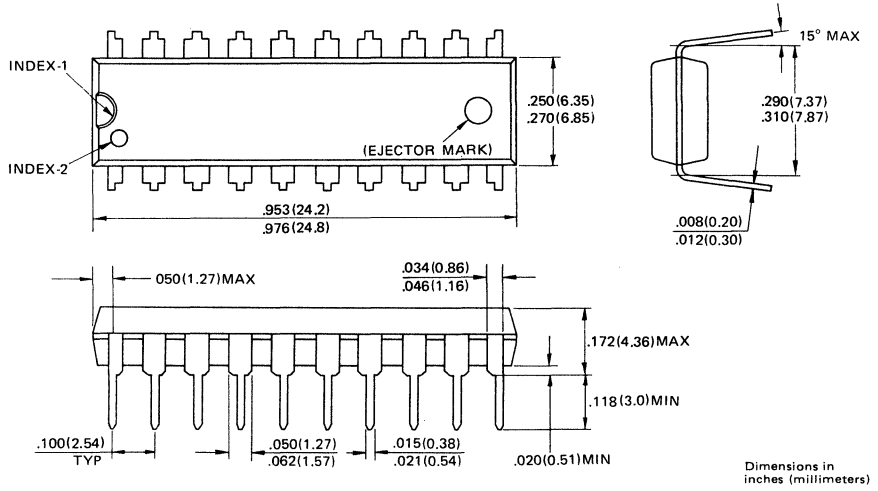


NOTE: MA/BR = "H" for make rate 39% and "L" for 33%.

7

PACKAGE DIMENSIONS (Suffix: P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



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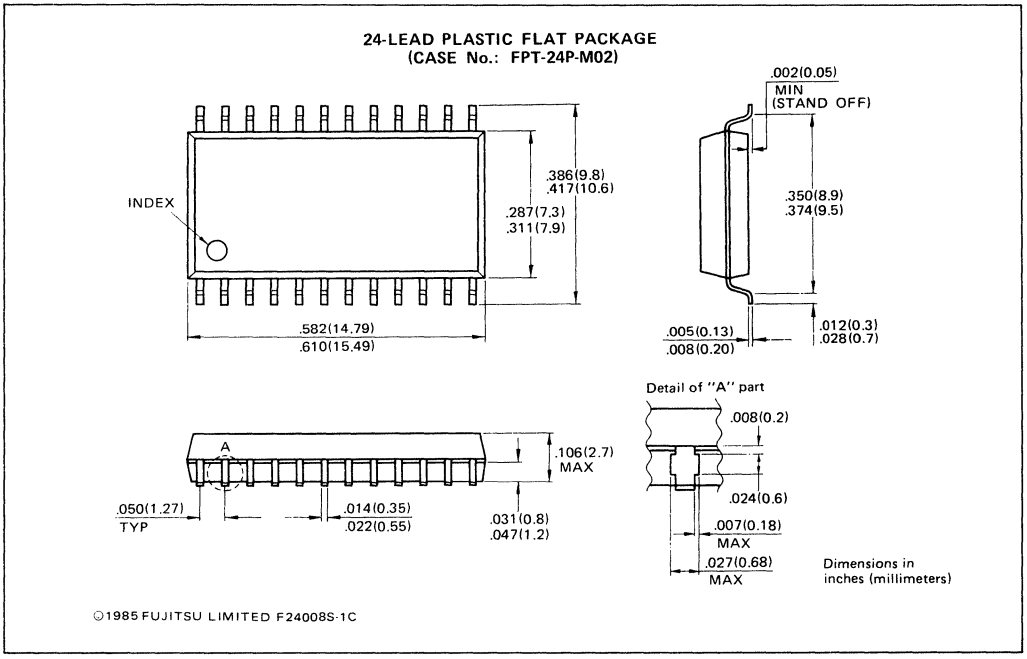
PACKAGE DIMENSIONS (Suffix: PF)



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

April 1991
Edition 2.0

FUJITSU

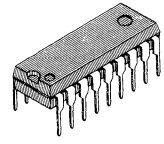
DATA SHEET

MB87017B
DTMF RECEIVER

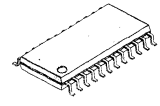
DUAL TONE MULTI FREQUENCY RECEIVER

The MB87017B is a one chip DTMF receiver with an input amplifier gain adjuster and low power consumption, integrating filter and decoder circuits. The MB87017B can select either automatic guard time setting mode or adjustable external guard time setting mode.
This circuit consists of SCFs (Switched Capacitor Filters) and decoders which convert 16 types of DTMF tone pairs into hexadecimal four-bit codes.

- All DTMF receiver functions are integrated on one chip.
- Low power consumption
- Built-in input amplifier gain adjustment circuit
- Selectable automatic or adjustable external guard time setting modes



PLASTIC PACKAGE
(DIP-18P-M02)



PLASTIC PACKAGE
(FPT-24P-M02)

7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	+6.0	V
Analog Input Voltage	V_{AIN}	−0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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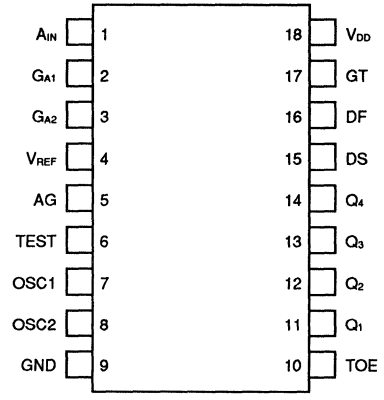
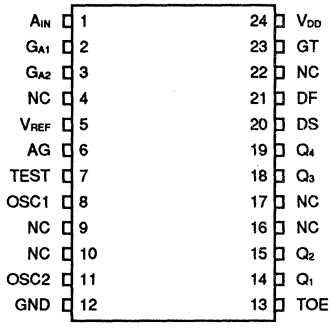
PIN ASSIGNMENT

PIN ASSIGNMENT
(TOP VIEW)



(DIP-18P-M02)

PIN ASSIGNMENT
(TOP VIEW)

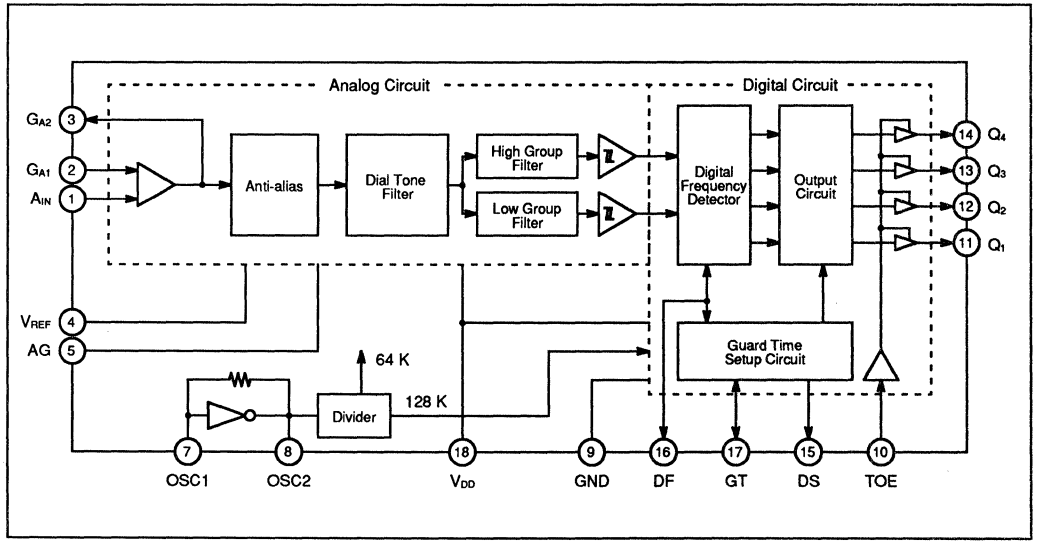


(FPT-24P-M02)

7

BLOCK DIAGRAM

(DIP PACKAGE)



PIN DESCRIPTIONS

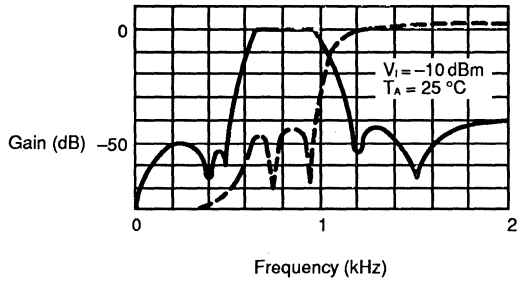
Pin Number DIP	Pin Number FPT	Symbol	I/O	Description
1	1	A_{IN}	I	Analog input pin (non-inverted operational amplifier input)
2	2	G_{A1}	I	Operational amplifier gain adjustment pin 1 (inverted operand amplifier input). Operational amplifier gain adjustment pin 2 (operand amplifier output pin). * These pins are provided for operational amplifier gain adjustment. The polarity of G_{A1} is opposite to that of G_{A2}.
3	3	G_{A2}	O	
4	5	V_{REF}	O	Reference voltage output pin. (1/2 V_{DD})
5	6	AG	–	Analog ground pin
6	7	TEST	–	Test pin. Usually set to ground level.
7	8	OSC1	I	Clock input pin. Clock output pin. * Connect a 3.5795 MHz crystal between OSC1 and OSC2 pins.
8	11	OSC2	O	
9	12	GND	–	Ground pin
10	13	TOE	I	Three-state output enable pin. * Data from Q_1 to Q_4 may be output when this pin is set to "High".
11 to 14	14, 15 18, 19	Q_1 to Q_4	O	Three-state data output pin.
15	20	DS	O	Signal detection pin. * This pin goes to "High" when an valid tone pair is received and decoded, and the data in the output data-bus is updated.
16	21	DF	O	Frequency detection pin. * This pin goes to "High" when a received tone pair is acknowledged as the valid DTMF signal frequency.
17	23	GT	O	Guard time mode select pin. * When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; Guard Time Present (GTP) and Guard Time Absent (GTA) are set to 20 milliseconds. * See functional descriptions on page 5. * When GT pin exceeds 1/2V_{DD}, DS pin outputs high level. When GT pin is less than 1/2V_{DD}, DS pin outputs low level.
18	24	V_{DD}	–	Positive supply voltage pin. * The voltage must be +5 V ±5%.
–	4, 9 10, 16 17, 22	NC	–	No connection

7

FUNCTIONAL DESCRIPTIONS

FILTER

The filters consist of 3 sixth-order SCFs. The dial tone removal filter (including the 60 Hz filter) output is connected to the individual hysteresis comparators through the low group and high group filters.
In the figure below, the solid line shows the characteristics of the low group filter while the broken line shows the characteristics of the high group filter. At a frequency of 770 Hz, it is assumed that 0 dB are lost. Therefore, this point is used for reference.



DECODER

7

1. Digital Frequency-detecting Circuit

The DF (Detect Frequency) pin goes to "High" when the detector circuit acknowledges the output signals from the two comparators as valid DTMF signal frequencies in the digital frequency detecting block.

2. Guard Time Setting Circuit

Automatic or adjustable external guard time setting modes are provided. Guard time has two types: GTP (Guard Time Present) and GTA (Guard Time Absent).

2.1 Automatic Guard Time Setting Circuit

When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; t_{GTP} and t_{GTA} are set to 20 milliseconds. The output signal from the filters may be acknowledged as a DTMF signal if:

① A signal with valid DTMF frequency lasts more than 40 milliseconds. This signal is decoded into a DTMF signal. These pulses correspond to the input signal enable period and disable period for alternative current characteristics.

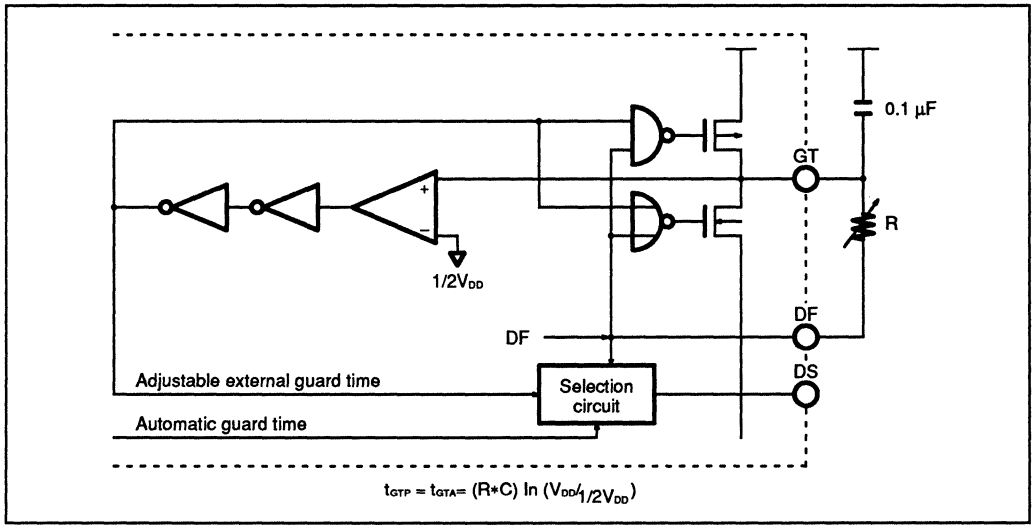
② A period of more than 40 milliseconds exists between DTMF signals n and (n + 1). If this is not the case the DTMF signal (n + 1) is disabled.
These pulses correspond to the inter-digit pauses for acceptance and rejection for alternative current characteristics.

In ①, it takes the DS (Detect Signal) pin GTP to acknowledge that the input signal is a DTMF signal after DF switches to "High". The DS pin switches to "High" when the input signal is acknowledged as a DTMF signal.
In ②, it takes the DS pin GTA to disable DTMF signal n after DF switches to "Low". The DS pin switches to "Low" when the signal is disabled. (See Page 10 for the timing chart.)

$$t_{SDA} > t_{GTP} + t_{PDF}$$
$$t_{IDA} > t_{ADF} + t_{GTA}$$

2.2 Adjustable External Guard Time Setting Circuit

The simplified adjustable external guard time setting circuit shown below enables any guard time present (GTP) or guard time absent (GTA) setting.
The guard time is adjusted by selecting external register R when the external capacitor is 0.1 µF.



2.3 Automatic Guard-time/Adjustable External Guard-time Setting Mode Selection Circuit

- Adjustable external guard time setting mode
  Adjustable external guard time setting mode (GT pin is set low) is selected on the rising edge of the detected frequency (DF).
- Automatic guard time setting mode
  The automatic guard time setting mode (GT pin is set high) is selected the power-on reset signal and on the rising edges of the DF.

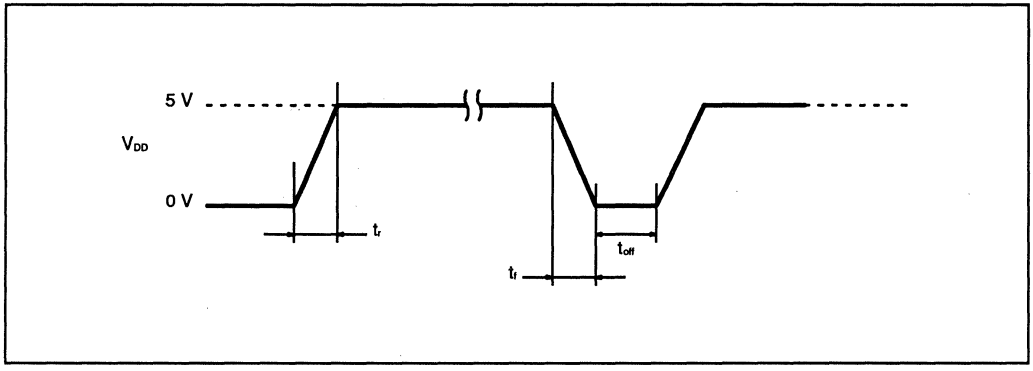
2.4 Power-on Reset Circuit

The power-on reset circuit generates a reset signal to initialize the automatic guard time or adjustable guard time setting circuit when power is applied.
The power-on reset circuit specifications and timing diagram are shown below.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Power supply rise time Power supply fall time	t_r t_f	0.1	–	50	ms	Power-on reset operation conditions
Power-off time	t_{off}	100	–	–	ms	

FUNCTIONAL DESCRIPTIONS

- Power-on reset timing diagram



NOTE: If the values of power supply rise time, fall time, and power off time shown in the table are not satisfied, the power-on reset signal will not be generated and the automatic guard time setting circuit may not recover from malfunction (receive disabled).
The adjustable external guard time setting circuit will not enter malfunction even if the power-on reset signal is not generated.
Therefore, if power supply conditions disable the power-on reset circuit, the adjustable external guard setting circuit can be used.

7

OUTPUT CIRCUIT

When the signal detector pin (DS) switches to "High", a received tone pair is stored in the output circuit register. The output latch status may be output on the output bus by setting the three state control input (TOE) to "High".

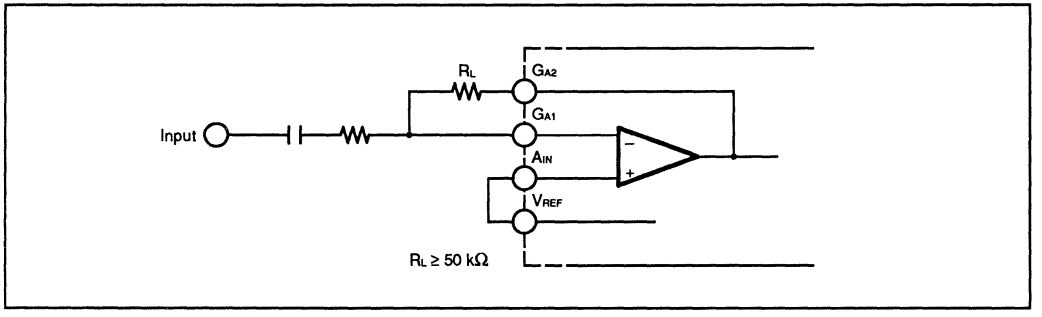
	COL0	COL1	COL2	COL3
ROW0	1	2	3	A
ROW1	4	5	6	B
ROW2	7	8	9	C
ROW3	*	0	#	D

DTMF Dial Matrix

Dial	A_{IN} Input		Input	Output			
	Low group: fo	High group: fo	TOE	Q_4	Q_3	Q_2	Q_1
1	697	1209	1	0	0	0	1
2	697	1336	1	0	0	1	0
3	697	1447	1	0	0	1	1
4	770	1209	1	0	1	0	0
5	770	1336	1	0	1	0	1
6	770	1477	1	0	1	1	0
7	852	1209	1	0	1	1	1
8	852	1336	1	1	0	0	0
9	852	1477	1	1	0	0	1
0	941	1336	1	1	0	1	0
*	941	1209	1	1	0	1	1
#	941	1477	1	1	1	0	0
A	697	1633	1	1	1	0	1
B	770	1633	1	1	1	1	0
C	852	1633	1	1	1	1	1
D	941	1633	1	0	0	0	0

SAMPLE DIFFERENCE INPUT CONFIGURATION

The MB87017B uses a difference input amplifier and provides for a bias power source (V_{REF}) to apply a bias voltage to the input signal. This also allows a pin to connect a gain adjustment resistor to the amplifier output.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Minimum	Typical	Maximum	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_I	0	–	V_{DD}	V
Oscillation Frequency	f_{OSC}	3.5759	3.5795	3.5831	MHz
OSC1 Pin Load Capacitance	C_{LDI}	10.0	–	50.0	pF
OSC2 Pin Load Capacitance	C_{LDO}	10.0	–	50.0	pF
GA2 Pin Load Resistance	R_{LA}	50	–	–	kΩ
GA2 Pin Load Capacitance	C_{LA}	–	–	100	pF
Operating temperature	T_A	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Power Consumption	P_D	f = 3.58 MHz, V_{DD} = 5 V	–	25	37	mW
Low Level Input Voltage	V_{IL}		0	–	0.8	V
High Level Input Voltage	V_{IH}		2.0	–	V_{DD}	V
Low Level Input Leak Current	I_{IL}	V_I = GND	–10	–	10	µA
High Level Input Leak Current	I_{IH}	V_I = V_{DD}	–10	–	10	µA
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA	0	–	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA	2.4	–	V_{DD}	V
V_{REF} Output Voltage	V_{REF}		–	2.5	–	V

AC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Signal Input Level *1		T_A = 25°C, V_{DD} = 5 V	−29	−10	−1	dBm
TWIST *2			–	±10	–	dB
Allowable Frequency Deviation			±1.5 ±2 Hz	–	–	%
Prohibited Frequency Deviation			±3.5	–	–	%
Allowable Noise Level *3			–	−12	–	dB
Allowable Dial Tone Level *4			–	22	–	dB
Input Signal Detection Timing (Present) *5	t_{PDF}		5	11	14	ms
Input Signal Detection Timing (Absent) *5	t_{ADF}		0.5	4	8.5	ms
Input Signal Enable Period (Accept) *5, 6	t_{SDA}		–	–	40	ms
Input Signal Enable Period (Reject) *5, 6	t_{SDR}		20	–	–	ms
Inter-digit Pause (Accept) *5, 6	t_{IPA}		–	–	40	ms
Inter-digit Pause (Reject) *5, 6	t_{IPR}		9	–	–	ms
Input Clock Frequency	f_{IN}		3.5759	3.5795	3.5831	MHz
Clock Rise Time	tr		–	–	110	ns
Clock Fall Time	tf		–	–	110	ns
Clock Duty	DR		–	50	–	%

*1 dBm: 600 ohm reference

*2 TWIST = High group tone voltage/Low group tone voltage

*3 Allowable noise = Total allowable noise within the range 300 Hz to 3.4 kHz/Minimum amplitude tone level in valid tone pairs

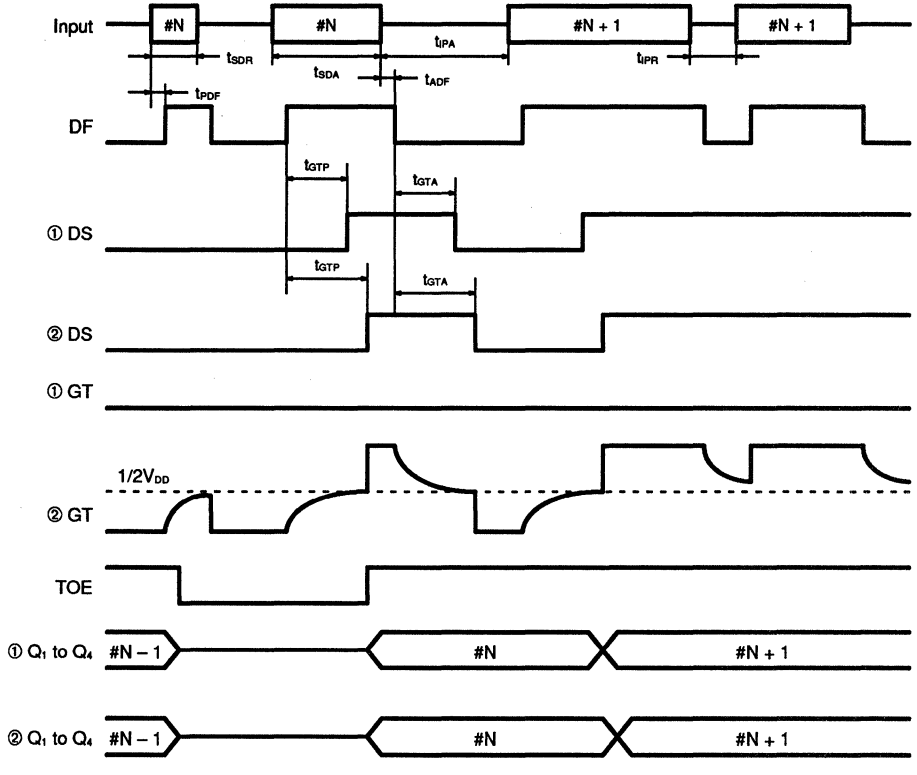
*4 Allowable dial tone level = Total allowable normal dial tone volume/Minimum amplitude tone in valid tone pairs

*5 See Timing Chart.

*6 Specified values are referenced to the automatic guard time setting mode.
See page 5 for t_{GTP}, and t_{GTA} in the adjustable external guard time setting mode.

7

TIMING CHART

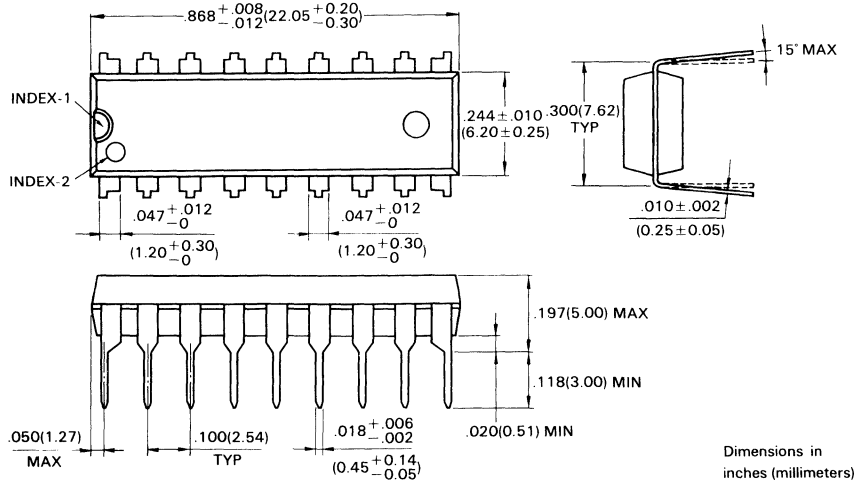


NOTE: ① Automatic guard time setting mode (GT pin is clamped to V_{DD})
② Adjustable external guard time setting mode (See circuit on page 5)

7

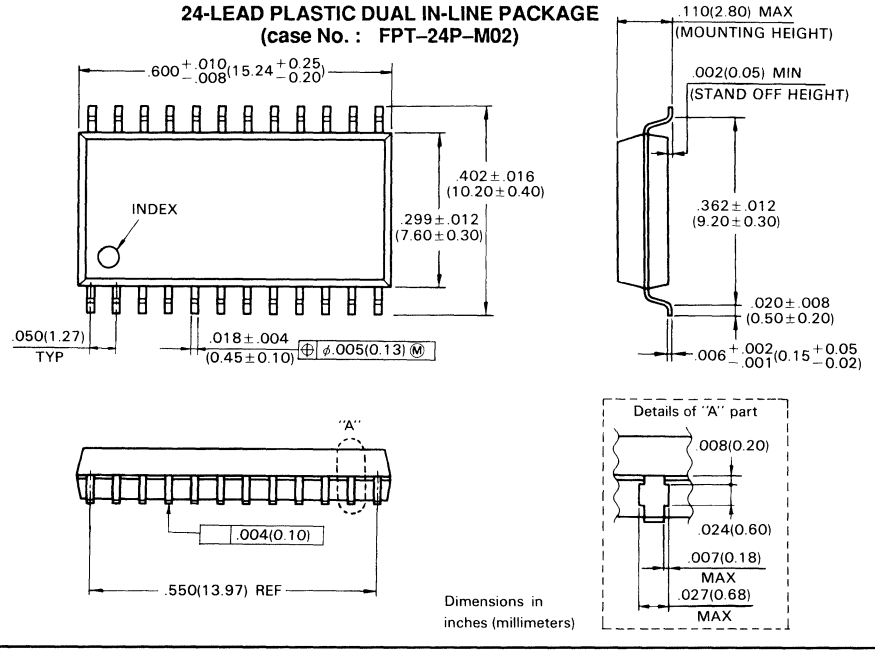
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(case No. : DIP–18P–M02)



Dimensions in inches (millimeters)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(case No. : FPT–24P–M02)



Dimensions in inches (millimeters)

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FUJITSU

DATA SHEET

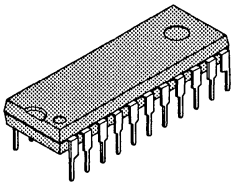
MB87029
DTMF Pulse Dialer

The Fujitsu MB87029 is a Dual Tone Multifrequency (DTMF) pulse dialer that is designed for pushbutton telephone sets and uses the Si-Gate CMOS process.

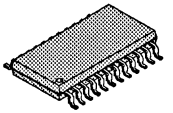
The MB87029 is used in both DTMF and PULSE modes and can be switched from PULSE mode to DTMF mode by a mode selection entry or by input from the keyboard. The MB87029 contains a 26-digit redial memory that permits the coexistence of PULSE and DTMF modes, enabling mixed redialing in both PULSE and DTMF modes by a signal key entry.

- Pulse 10 pps, 20 pps, or DTMF operation can be selected by the mode switch pin (MODEIN)
- On-chip 26 digits of redial memory (up to 25 digits can actually be written in the memory)
- Selectable make ratio by MA/BR: 39% or 33%
- Line Dial Tone (LDT) function is provided (switching from PULSE mode to DTMF mode by key entry)
- Output of a beep tone for input confirmation (for all effective key entry independently PULSE/DTMF modes)
- Redial inhibit function is included for redial memory overflow
- Mixed redialing of both PULSE and DTMF modes
- PAUSE function is provided and pause accumulation is possible
- Single-tone output is enabled by SCNT pin
- FLASH function is provided (ONHOOK mode is selected by keyboard input)
- FLASH output time, 0.1 second or 0.6 second, is selected by FCNT pin
- Crystal or ceramic oscillator (3.579545 MHz) can be used
- Pause release function is provided (two or more consecutive pauses can be released)
- Operating voltages:
  PULSE mode: 2.0 V to 6.0 V
  DTMF mode: 2.5 V to 6.0 V
  (TA = –30 to 60°C)

PRELIMINARY

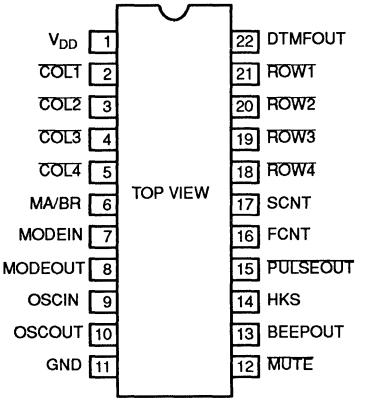


PLASTIC PACKAGE
DIP–22P–M03



PLASTIC PACKAGE
FPT–24P–M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Pin Name	Value	Unit
Positive Supply Voltage	V_{DD}	V_{DD}	GND – 0.3 to 7.0	V
Input Voltage	VI	All inputs	GND – 0.3 to V_{DD} + 0.3	V
Ouput Voltage	VO	All outputs	GND – 0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}		–55 to +150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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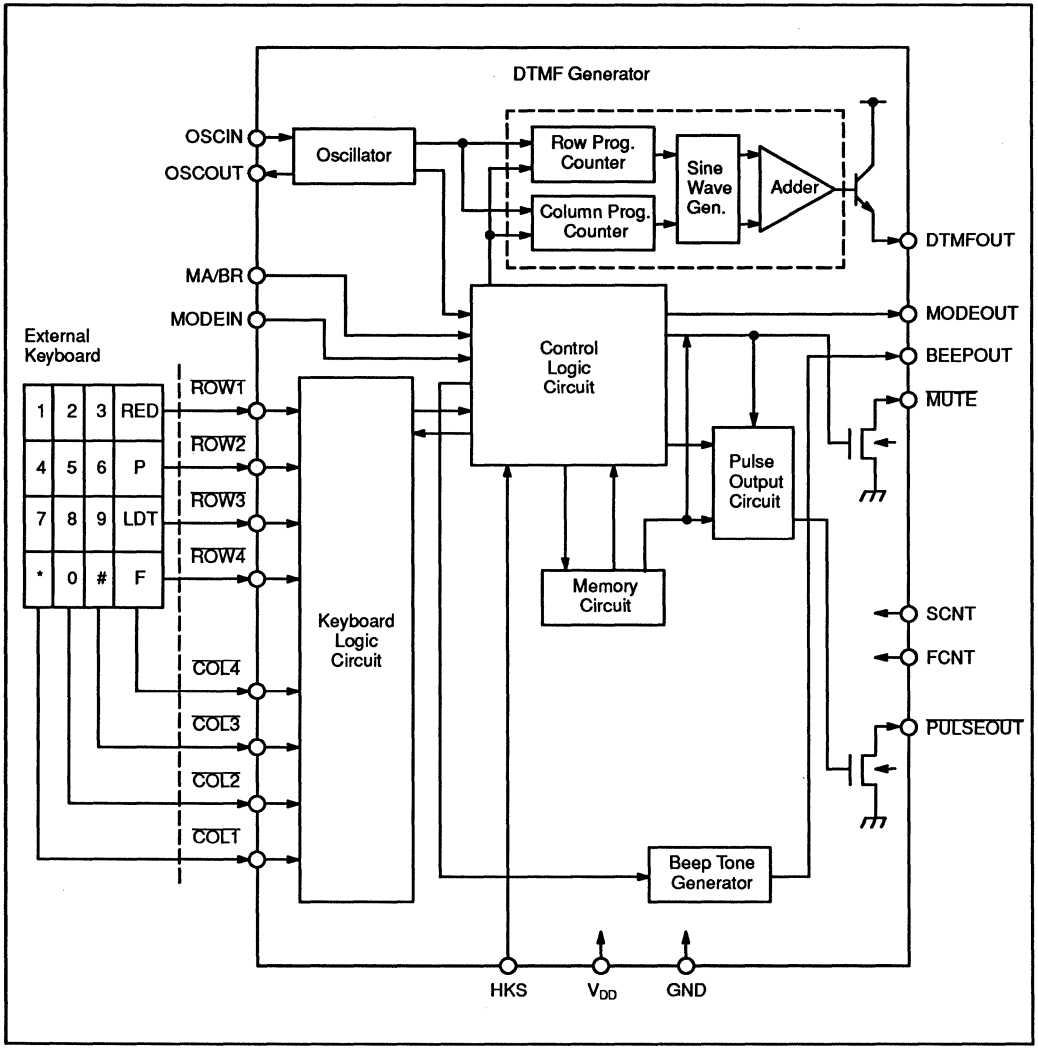
7

Figure 1. MB87029 Block Diagram



7

PIN DESCRIPTIONS

<table>
<tr><th rowspan="2">I/O</th><th colspan="2">Pin No.</th><th rowspan="2">Symbol</th><th rowspan="2">Description</th></tr>
<tr><th>DIP</th><th>FPT</th></tr>
<tr><td rowspan="2">Power Supply</td><td>1</td><td>1</td><td>V_D
D</td><td>Power supply voltages: Pulse mode 2.0 V to 6.0 V
DTMF mode 2.5 V to 6.0 V
Memory Retention mode 2.0 V min.</td></tr>
<tr><td>11</td><td>12</td><td>GND</td><td>Ground</td></tr>
<tr><td rowspan="3">Input</td><td>2
3
4
5
21
20
19
18</td><td>2
3
5
6
23
22
21
20</td><td>$\overline{COL1}$
$\overline{COL2}$
$\overline{COL3}$
$\overline{COL4}$
$\overline{ROW1}$
$\overline{ROW2}$
$\overline{ROW3}$
$\overline{ROW4}$</td><td>Uses key entries from 2 of 7 or 2 of 8 keyboards with common GND. This IC is available with a single contact from A type keyboard and electronic input (Low entry).
Key input debouncing time is 23 ms typ. for both PULSE and DTMF modes.
Key input release guard time is 23 ms typ. for both PULSE and DTMF modes.
Key entry is accepted in PULSE/DTMF modes only when a single key (one key on the keyboard) is pressed longer than the debouncing time. If two or more keys are pressed, they are not accepted unless they are released one-by-one and the last key is held closed longer than the debouncing time, after all other keys are released.
Key entry is accepted in DTMF mode only when either a single key (dual-tone key) is pressed or two or more keys in the same $\overline{COL}$ or $\overline{ROW}$ (single-tone keys) are pressed longer than the debouncing time. If one key in $\overline{COL4}$ is pressed, the single-tone keys are ineffective. If multiple single-tone keys are pressed, and the last key is held closed longer than the debouncing time, after all other keys are released, the key is effective as the dual-tone key.
Hereafter, key entries are described with the premise that keys are held closed longer than the debouncing time.
Pauses between key entries in PULSE and DTMF modes must be 50 ms or more. However, up to 50 ms is necessary from key entry to output start for single-tone outputs.
Key switch contact resistance up to 5kΩ is allowable.</td></tr>
<tr><td>6</td><td>7</td><td>MA/BR</td><td>This pin selects the make rate.
<table><tr><th>MA/BR</th><th>Make Rate (%)</th><th>Break Rate (%)</th></tr><tr><td>V_{DD}</td><td>39</td><td>61</td></tr><tr><td>GND</td><td>33</td><td>67</td></tr></table>Make ratio switching by MA/BR is inhibited during PULSE/DTMF transmission. The input level is in the CMOS level.</td></tr>
<tr><td>6</td><td>7</td><td>MODEIN</td><td>This pin selects the pulse mode, 10 pps, 20 pps, or the DTMF mode.
<table><tr><th>MODEIN</th><th>Mode</th></tr><tr><td>V_{DD}</td><td>Pulse Mode 20 pps</td></tr><tr><td>Open (1 MΩ or more)</td><td>Pulse Mode10 pps</td></tr><tr><td>GND</td><td>DTMF Mode</td></tr></table>Mode switching is not accepted by MODEIN. After data transmission is completed, mode switching is honored by key entry.
In the ONHOOK mode, this pin is set to a high impedance state.</td></tr>
</table>

continued on next page

7

PIN DESCRIPTIONS

I/O	Pin No. DIP	Pin No. FPT	Symbol	Description
Input	14	15	HKS	Hook switch input pin. ONHOOK Mode: Open or V_{DD} OFFHOOK Mode: GND Output is inhibited in ONHOOK mode, and $\overline{PULSEOUT}$, DTMFOUT, BEEPOUT, $\overline{MUTE}$, and MODEOUT are set at a high impedance state. All key entries are set to HZ and the on-chip operational amplifier and oscillator (OSCIN = L, OSCOUT = L) become power down states. This pin is pulled up by a high resistance internally. The input level is in the CMOS level.
	9	10	OSCIN	Oscillator input pin. In the ONHOOK mode, this pin is pulled to a low level by a high resistance.
	16	17	FNCT	This pin selects FLASH time period. FNCT: V_{DD} → FLASH output time: 0.6 second; FNCT: GND → FLASH output time: 0.2 second Switching is prohibited during PULSE/DTMF transmission. Input level is in the CMOS level.
	17	18	SCNT	This input enables a single-tone output. SCNT: V_{DD} → Single tone output: Output; SCNT: GND → Single tone output: Not output Switching is prohibited during a PULSE/DTMF transmission. Input level is in the CMOS level.
Output	10	11	OSCOUT	Oscillator output pin. In the ONHOOK mode, this pin is pulled to a low level by a high resistance.
	8	9	MODEOUT	The output is in the CMOS level and set to a high impedance state in the ONHOOK mode. Low level is output in the PULSE mode and high level is output in the DTMF mode, including the LDT function. MODEOUT blinks on and off at a frequency of 2.5 Hz typ., if there is no pause before and after mode switching in redial function. When the FLASH key is pressed in either PULSE or DTMF mode, High impedance is output for a 0.6 second (typical) following the BEEP tone output. The key acceptance state (OFFHOOK mode) is now entered.

continued on next page

7

PIN DESCRIPTIONS

I/O	Pin No. DIP	Pin No. FPT	Symbol	Description
Output	12	13	$\overline{\text{MUTE}}$	N-channel open drain output. In both PULSE and DTMF modes, the $\overline{\text{MUTE}}$ pin is in a high impedance state for the following conditions: 1. There is no key entry. 2. After the beep tone is output and the FLASH key is pressed, HZ is output for 0.6 second (typical). 3. During pause output state. (However, when key is pressed, $\overline{\text{MUTE}}$ is low level while beep tone is being output.) 4. During MODEOUT blinking. After key entries become effective in the PULSE or DTMF modes, the $\overline{\text{MUTE}}$ pin is low during output of the beep tone, pulse output (according to numeric key entry), and output of DTMF.
	13	14	BEEPOUT	The output is in CMOS level and the pin is set to a high impedance state unless beep tone is output. In PULSE/DTMF modes, the beep tone is output according to effective key entries. Beep tone is output in 41 ms typ. at 1 kHz in rectangular pulse.
	13	14	$\overline{\text{PULSEOUT}}$	N-channel open drain output. This pin is in a high impedance state in the ONHOOK mode or DTMF mode. In PULSE mode, this pin is at low for brakes (according to numerical key entries). When the FLASH key is pressed in the PULSE or DTMF mode, a low level is output for 600 ms typ. after the beep tone is sent (even during a PULSE/DTMF send). The key acceptance state (OFFHOOK mode) then returns.
	22	24	DTMFOUT	This DTMFOUT output pin is a bipolar follower that can drive a 100 Ω load between pin and GND. When a single key (numerical, [*] or [#]) is pressed in the DTMF modes, dual tone is output. Pressing two or more keys in the same $\overline{\text{ROW}}$ or $\overline{\text{COL}}$ on the keyboard outputs the signal tone in the $\overline{\text{ROW}}$ or $\overline{\text{COL}}$. If a key in $\overline{\text{COL4}}$ is pressed, then the DUAL TONE or single tone in the $\overline{\text{ROW}}$ or $\overline{\text{COL}}$ is not output. (Please see Electrical Characteristics.) If the FLASH key is pressed during DTMF sending, the beep tone is output at BEEPOUT and subsequent DTMF tones are not output. The ONHOOK mode is entered for 600 ms typ. after the key acceptance state (OFFHOOK mode) is entered. DUAL TONE output time conditions are as follows: 1. 80 ms typ. for redial output 2. 80 ms typ. when the key entry time is within 130 ms typ. and more than the debouncing time 3. DUAL TONE output is stopped at once if a key is pressed longer than 130 ms typ. and released. 4. Signal tone is output from the end of debouncing time until the key is released. This pin is set to a high impedance state unless DTMF tone is output.

7

FUNCTIONAL DESCRIPTIONS

Ordinal Dialing

In OFFHOOK mode, PULSE/DTMF signals are output according to the key input, regardless of the number of key input figures. For the PULSE mode, any number of digital entries with keys 0 to 9. For the DTMF mode, any number of digital entries with keys 0 to 9, [*] and [#].

Up to 26 digits can be stored in the redial memory. In the PULSE mode, a redial digit is counted for any numeric, pause, and LDT entry. In the DTMF mode, a redial digit is counted for any numeric, [*], [#], and [P] entry.

In both the PULSE and DTMF modes, one digit is counted as mode information when MODEIN is used for mode switching. After OFFHOOK, the first numeric entry is counted as a mode digit. In the PULSE mode the numeric key is counted as a mode digit. In the DTMF mode, a numeric key, [*], and [#] entry is counted as a mode digit. In either OFFHOOK or PULSE modes, the mode-information digit is written into the redial memory.

Redialing Function

The redial memory is read out to execute the redialing operation when a redial key is the first key pressed in OFFHOOK state. In the PULSE mode, the redial keys are [#] and [*]. In the DTMF mode, only the [RED] key is accepted for redial.

When 27 or more digits are written into the redial memory, PULSE or DTMF signals that correspond to the key entries are output, but the redialing operation is ineffective because of memory overflow. At this time, even if the first key pressed after the state change from ONHOOK to OFFHOOK is the redial key, the entry is not accepted and the beep tone is not output in either mode of operation.

7

After OFFHOOK, if a numeric or LDT key is the first entry in PULSE mode, or the first entry in the DTMF mode is a numeric, [*], [#] or a single-tone key entry (excluding $\overline{COL4}$), the redial memory is cleared and data is written into memory according to key entry information.

Mixed Redialing

Mixed redialing is executed when the mode is changed from the PULSE to DTMF mode (done by pressing the LDT key), or when MODE is changed during key entries.

If, at redialing, there is a pause before or after mode switching (including LDT), PULSE/DTMF is sent and PULSE/DTMF signals are transmitted after the pause. To redial when there is no pause before or after mode switching (including LDT), all operations must cease after mode switching and a HALT state is enabled. MODEOUT blinks (indicates that mode switching has no automatic pause) and prompts a pause release.

The pause release keys in PULSE mode are [*], [RED], and the [P] key. In the DTMF mode, the [RED] and the [P] keys are used for pause release. PULSE and DTMF signals can now be sent by key entry. The FLASH key is the only other acceptable entry.

During redial output, the [F] key is the only key entry accepted. The pause release key is only accepted when MODEOUT is blinking or during a pause at redialing.

Mode Switching

During PULSE or TONE transmissions, mode switching by MODEIN is not permitted; after transmission is complete, MODEIN can be used for mode switching.

When PULSE or DTMF modes are switched by MODEIN, one digit is stored into redial memory as mode information. After OFFHOOK, if the first key entry is numeric in the PULSE mode, or a numeric [*] or [#] in the DTMF mode, the mode-information digit is written into redial memory.

In the PULSE mode, after the LDT key is accepted only one time, the DTMF mode is selected (regardless of MODEIN pin switching). The LDT key is not accepted in the DTMF mode. The MODEIN pin switching enables the desired mode of operation to be selected.

Line Dial Tone (LDT) Function

If the LDT key is pressed in the PULSE mode, the DTMF mode is selected and DTMF tones can be output. In PULSE mode, only the first LDT key is accepted after key acceptance state (OFFHOOK mode) is entered. Once LDT key is accepted, the following LDT key entries are ignored.

When the LDT key is used to enter the DTMF mode, all keys (excluding $\overline{COL4}$ keys) provide dual-tone and single-tone outputs. (Note: If even one $\overline{COL4}$ key is pressed, neither dual nor single tones are output.) The mode after that is not switched. If mode switching by LDT from memory is done during redialing, key entries after redialing are executed in DTMF mode regardless of the MODEIN state and the data is written into the redial memory. However, for effective keys (not the redial key) after ONHOOK changes to OFFHOOK, memory is reset and written in the current mode.

Pause Function

A pause state can be entered by pause key entry.

In the PULSE mode, a pause is introduced by pressing the [#] or [P] keys; in the DTMF mode (including LDT) only the [P] key is effective. If a pause key is the first key pressed after changing from ONHOOK to OFFHOOK, the entry is not accepted.
One pause key entry introduces a pause state that is typically 4 seconds; contiguous pause (N X 4 seconds) can be executed by making consecutive key entries. The pause can be reduced by entering [P] or [RED] during a redialing pause time.

In the PULSE mode, the [*] key is used as a pause release key. Multiple pauses can be sent up to 500 times faster by entering a pause release key, that is, N X 4 seconds becomes N X 800 milliseconds.

Flash Function

Keyboard entries enable ONHOOK mode. Only the [F] key is used as a FLASH key in both PULSE and DTMF modes (including LDT).

When the [F] key is pressed, the ONHOOK mode is entered for 600 milliseconds (typical) after beep tone is sent. During this time, the key entry pin is not accepted. MODEIN, $\overline{MUTE}$, MODEOUT, and DTMF/BEEPOUT pins are placed in the high-impedance state and the PULSEOUT pin is set low level. After 600 milliseconds (typical), the return of OFFHOOK is automatic and key entries can again be accepted.

Test (High-speed Mode)

A test mode circuit is built into the IC. In the ONHOOK state, pins OSCIN and OSCOUT are pulled down by a high resistance. To activate the test mode, tie the OSCIN high and apply clock signal to OSCOUT. The internal circuit operates up to 128 times faster than normal operation.

Figure 2. Keyboard Configuration

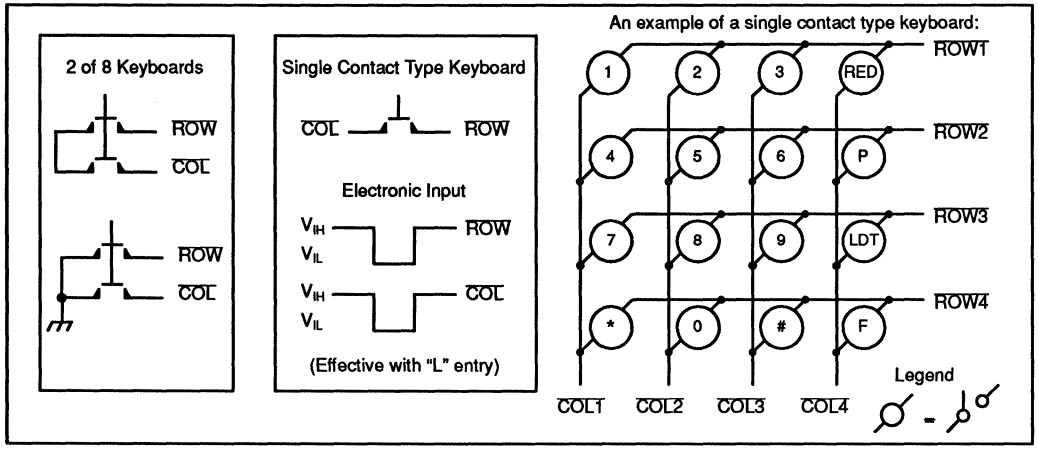
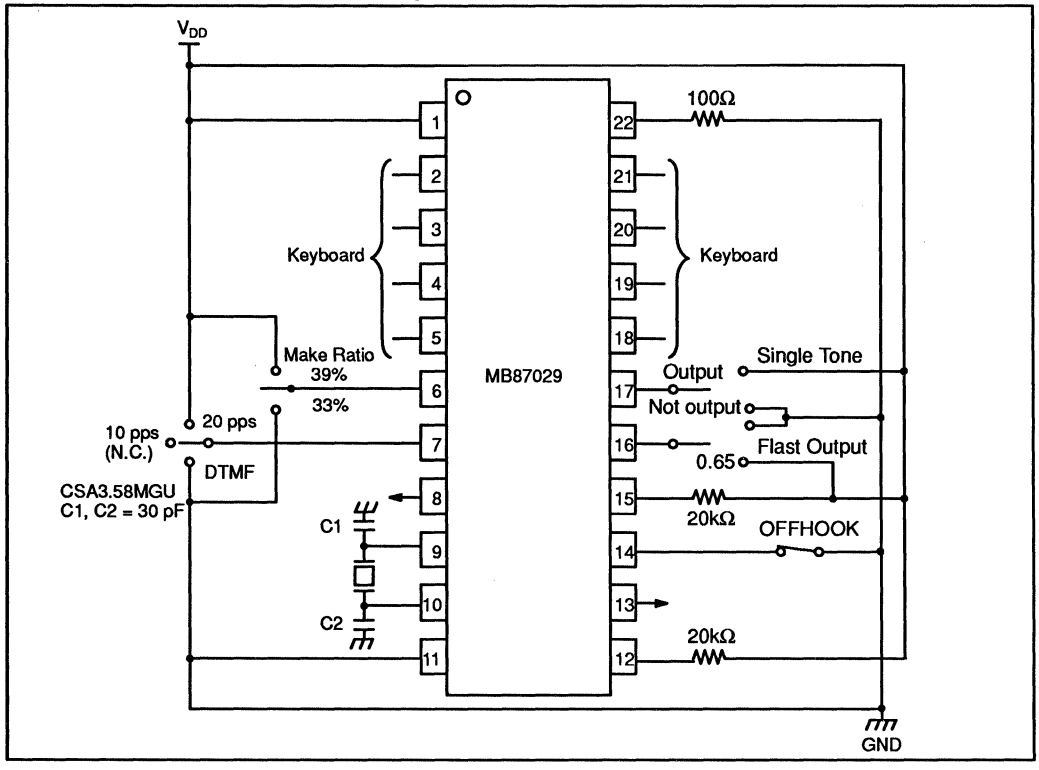


Figure 3. Reference Circuit



7

KEY OPERATION DIAGRAM

Redial key for PULSE mode	:	[RED (P)] = [RED] or [#]
Redial key for DTMF mode	:	[RED (D)] = [RED]
Pause key for PULSE mode	:	[P (P)] = [P] or [#]
Pause key for DTMF mode	:	[P (D)] = [P]
Pause release key of PULSE mode	:	[PR (P)] = [RED], [P], or [*]
Pause release key of DTMF mode	:	[PR (D)] = [RED] or [P]
Pause output	:	(P) = Pause

KEY ENTRIES IN PULSE MODE

When MODEIN is set to 10 pps

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	[1] [2]	1–2		
ON					
OFF	OPEN	[RED (P)]	1–2		
		[3]	3		
ON					
OFF	OPEN	[RED (P)]	1–2–3		
ON					
OFF	V_{DD}	[RED (P)]	1–2–3		
ON					
OFF	GND	[RED (D)]	1–2–3		
		[4]			4

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7

KEY ENTRIES IN PULSE MODE

When MODEIN is set to 20 pps

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	V_{DD}	1 2		1–2	
ON					
OFF	V_{DD}	RED (P)		1–2	
		3		3	
ON					
OFF	V_{DD}	RED (P)		1–2–3	
ON					
OFF	OPEN	RED (P)		1–2–3	
ON					
OFF	GND	RED (D)		1–2–3	
		4			4

7

KEY ENTRIES IN DTMF MODE

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	GND	1 2			1–2
ON					
OFF	GND	RED (D)			1–2
		3			3
ON					
OFF	GND	RED (D)			1–2–3
ON					
OFF	OPEN	RED (P)			1–2–3
ON					
OFF	GND	RED (P)			1–2–3
		4		4	

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KEY ENTRIES WHEN THE LDT KEY IS USED

When there is a pause before LDT

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON OFF	OPEN	1 2 P (P) LDT 3	1–2–(P)		3
ON OFF	GND	RED (P) 4	1–2–(P)		3 4
ON OFF	V_{DD}	RED (P)	1–2–(P)		3–4
ON OFF	GND	RED (D)	1–2–(P)		3–4

KEY ENTRIES WHEN THE LDT KEY IS USED

When there is a pause after LDT

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON OFF	OPEN	1 2 LDT P (D) 3	1–2		(P)–3
ON OFF	GND	RED (P) 4	1–2		(P)–3 4
ON OFF	V_{DD}	RED (P)	1–2		(P)–3–4
ON OFF	GND	RED (D)	1–2		(P)–3–4

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KEY ENTRIES WHEN THE LDT KEY IS USED

When there is no pause before and after LDT

HOOK	MODEIN	Key Entry	PULSE Output 10pps	PULSE Output 20pps	DTMF Output
ON					
OFF	OPEN	[1] [2]	1–2		
		[LDT] [3]			3
ON					
OFF	OPEN	[RED (P)]	1–2–MODEOUT blinks		
		[PR (D)]			3
		[4]			4
ON					
OFF	V_{DD}	[RED (P)]	1–2–MODEOUT blinks		
		[PR (D)]			3–4
ON					
OFF	GND	[RED (D)]	1–2–MODEOUT blinks		
		[PR (D)]			3–4

7

KEY ENTRIES WHEN PULSE/DTMF MODE IS SWITCHED (MIXED REDIAL)

When there is a pause before mode switching

HOOK	MODEIN	Key Entry	PULSE Output 10pps	PULSE Output 20pps	DTMF Output
ON					
OFF	OPEN	[1] [2] [P (P)]	1–2–(P)		
	V_{DD}	[3] [4] [P (P)]		3–4–(P)	
	GND	[5] [*] [P (D)]			5–*–(P)
	OPEN	[6] [7]	6-7		
ON					
OFF	OPEN	[RED (P)]	1–2–(P) 6-7	3–4–(P)	5–*–(P)
ON					
OFF	V_{DD}	[RED (P)]	1–2–(P) 6–7	3–4–(P)	5–*–(P)
ON					
OFF	GND	[RED (D)]	1–2–(P) 6-7	3–4–(P)	5–*–(P)

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KEY ENTRIES WHEN PULSE/DTMF MODE IS SWITCHED (MIXED REDIAL)

When there is a pause after mode switching

HOOK	MODEIN	Key Entry	PULSE Output 10pps	PULSE Output 20pps	DTMF Output
ON					
OFF	OPEN	1 2	1–2		
	V_{DD}	P (P) 3 4		(P)–3–4	
	GND	P (D) 5 *			(P)–5–*
	OPEN	P (P) 6 7	(P)–6–7		
ON					
OFF	OPEN	RED (P)	1–2 (P)–6–7	(P)–3–4	(P)–5–*
ON					
OFF	V_{DD}	RED (P)	1–2 (P)–6–7	(P)–3–4	(P)–5–*
ON					
OFF	GND	RED (D)	1–2 (P)–6–7	(P)–3–4	(P)–5–*
ON					
OFF	OPEN	1 2	1–2		
	V_{DD}	3 4		3–4	
	GND	5 *			5–*
	OPEN	6 7	6–7		
ON					
OFF	OPEN	RED (P)	1–2–MODEOUT blinks		
		PR (P)		3–4–MODEOUT blinks	
		PR (D)			5–*–MODEOUT blinks
		PR (P)	6–7		
ON					
OFF	V_{DD}	RED (P)	1–2–MODEOUT blinks		
		PR (P)		3–4–MODEOUT blinks	
		PR (D)			5–*–MODEOUT blinks
		PR (P)	6–7		
ON					
OFF	GND	RED (D)	1–2–MODEOUT blinks		
		PR (P)		3–4–MODEOUT blinks	
		PR (D)			5–*–MODEOUT blinks
		PR (P)	6–7		

7

REDIAL MEMORY INHIBIT FUNCTION

HOOK	MODEIN	Key Entry	PULSE Output		DTMF Output
			10pps	20pps	
ON					
OFF	OPEN	(1)(1) ··· (1)(1) (25)	1 – 1·····1 – 1 (25)		
ON					
OFF	OPEN	RED (P)	1 – 1·····1 – 1 (25)		
ON					
OFF	OPEN	(1)(1) ··· (1)(1) (26)	1 – 1·····1 – 1 (26)		
ON					
OFF	OPEN	RED (P)	No output		
		(2)	2		
ON					
OFF	OPEN	RED (P)	2		
ON					
OFF	V_{DD}	RED (P)	2		
ON					
OFF	GND	RED (D)	2		
		(3)			3
ON					
OFF	OPEN	LDT (1)(1) ··· (1)(1) (25)			1 – 1·····1 – 1 (25)
ON					
OFF	OPEN	RED (P)			1 – 1·····1 – 1 (25)
ON					
OFF	OPEN	(1)(1) LDT (1)(1) ··· (1)(1) (23)	1 – 1		1 – 1·····1 – 1 (23)
ON					
OFF	OPEN	RED (P)	No output		No output

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	PULSE mode and memory retention mode	2.0		6.0	V
			DTMF mode	2.5		6.0	V
Input Voltage	V_I	All Inputs		0		V_{DD}	V
Output Load Resistance	R_O	DTMFOUT	Between output pin and GND	0.1		20	kΩ
Operating Temperature	T_A			–30		60	°C

7

ELECTRICAL CHARACTERISTICS

V_{DD}: PULSE mode = 2.0 to 6.0 V, V_{DD}: DTMF mode = 2.5 to 6.0 V, TA = –30 to 60°C

Parameter	Symbol	Pin Name	Condition		Value Min	Value Typ	Value Max	Unit
Power Supply Current	I_{DD}	V_{DD}	All output pins are open in DTMF mode			2.5	5.0	mA
	I_{DP}		All output pins are open in PULSE mode			1.0	2.0	mA
	I_{DST}		All output pins, HKS pin open in Standby			1.5	10	µA
	I_{DD1}		V_{DD} = 2.5V	All output pins open in DTMF		1.0	2.0	mA
	I_{DP1}			All output pins open in PULSE		0.3	0.6	mA
	TDST1		TA = 25°C	All output pins HKS open in Standby		0.2	1.0	µA
Digital Input Voltage 1	V_{IH1}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ to $\overline{ROW4}$			0.8 V_{DD}		V_{DD}	V
	V_{IL1}				0		$\frac{1}{5}$ V_{DD}	V
Digital Input Voltage 2	V_{IH2}	HKS, FCNT MODEIN, SCNT MA/BR			0.8 V_{DD}		V_{DD}	V
	V_{IL2}				0		$\frac{1}{5}$ V_{DD}	V
Digital Input Current 1	I_{IH1}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$	$V_I = V_{DD}$		–0.01		$\frac{1}{5}$ V_{DD}	mA
	I_{IL1}		V_I = GND		–0.01 V_{DD}		0.01	mA
Digital Input Leakage Current 1	I_{IZ1}		Key entry HZ GND ≤ V_I ≤ V_{DD}		–10		10	µA
Digital Input Current 2	I_{IH2}	MODEIN	$V_I = V_{DD}$		–0.01		$\frac{1}{75}$ V_{DD}	mA
	I_{IL2}		V_I = GND		–1/75 V_{DD}		0.01	mA
Digital Input Leakage Current 2	I_{IZ2}		MODEIN HZ GND ≤ V_I ≤ V_{DD}		–10		10	µA
Digital Input Current 3	I_{IL3}	MA/BR, SCNT, FCNT	V_I = GND		–10		10	µA
	I_{IH3}	HKS, MA/BR, SCNT, FCNT	$V_I = V_{DD}$		–10		10	µA

continued on next page

7

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Pull-up Resistor	RPLU	HKS		100	200	400	kΩ
Digital Output Voltage	V_{OH}	MODEOUT BEEPOUT	I_{OH} = –0.2mA	V_{DD} –0.5		V_{DD}	V
	V_{OL}	MODEOUT, PULSEOUT, MUTE, BEEPOUT	I_{OL} = 0.5mA	0		0.5	V
Digital Output Off Leakage Current	I_{OL}	MUTE, PULSEOUT, MODEOUT, BEEPOUT	GND ≤ V_O ≤ V_{DD}	–10		10	µA
External Resistance when digital input is open	R_{DIO}	ROW1 TO ROW4 COL1 to COL4 HKS, MODEIN	Resistance connected to external circuit when input is open. The other end of the resistance must be between O V and V_{DD}.	1			MΩ
Pull-down Resistance	R_{PLD}	OSCIN, OSCOUT	ONHOOK mode	75	150	300	kΩ
Oscillator Frequency	O_{SCIN}				3.579545		MHz
DTMF Output Voltage 100Ω placed between output pin and GND.	A_{OUT}	DTMFOUT	No signal is output		0		V
			Offset voltage when signals are output		0.6 V_{DD} –0.75		V
			DTMF TONE output voltage		1.44		Vp–p
			ROW single tone output voltage		0.64		Vp–p
			COLUMN single tone output voltage		0.80		Vp–p
			COLUMN/ROW tone ratio		2.0		dB
Redial Memory Digit	N_{RKEY}	COL1 to COL4 ROW1 TO ROW4				26	digits
Make Ratio	W_{MAKE}	PULSEOUT	MA/BR = V_{DD}		39		%
			MA/BR = GND		33		%
Oscillation Start time	t_{OSS}	OSCIN, OSCOUT		0	8	16	ms
Oscillation Stop time	t_{OSSP}			0	8	16	ms

continued on next page

7

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
Key Entry HZ Hold time	t_{HZKH}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$		0		5	ms
MODEIN HZ Hold time	t_{HZMIH}	MODEIN		0		5	ms
MODEOUT HZ Hold time	t_{HZMOH}	MODEOUT		0		5	ms
Key Entry HZ Start time	t_{HZKS}	$\overline{COL1}$ to $\overline{COL4}$ $\overline{ROW1}$ TO $\overline{ROW4}$		0		5	ms
MODEIN HZ Start time	t_{HZMIS}	MODEIN		0		5	ms
MODEOUT HZ Start time	t_{HZMOS}	MODEOUT		0		5	ms
Pause Time	t_{PAS}	$\overline{PULSEOUT}$, DTMFOUT		3.85	4.0	4.15	s
MODEOUT Switch Start time 1	t_{MOC1}	MODEOUT			12		ms
MODEOUT Switch Start time 2	t_{MOC2}			2	5	8	ms
MODEOUT HZ Start Time by F key entry	t_{MOFS}				72		ms
MODEOUT HZ Hold Time by F key entry	t_{MOFH}		FCNT = V_{DD}	0.59	0.6	0.61	s
			FCNT = GND	0.09	0.1	0.11	
MODEOUT Blinking Period	t_{MOSI}			0.39	0.4	0.41	s
MODEOUT Change Start time by pause release key entry	t_{MOPS}				28		ms
DTMFOUT Output Start time when mode is switched	t_{MST}	DTMFOUT		2	10	15	ms
DTMF Output Start time by pause release key entry	t_{PDT}				39		ms
$\overline{PULSEOUT}$ Output Hold time by F key entry	t_{PUFH}	PULSEOUT	FCNT = V_{DD}	0.59	0.6	0.61	s
			FCNT = GND	0.09	0.1	0.11	
$\overline{PULSEOUT}$ OUTPUT Start time by F key entry	t_{PUFS}				72		ms

continued on next page

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition		Value Min	Value Typ	Value Max	Unit
Key Entry Width1	t_{WK1}	COL1 to COL4 ROW1 TO ROW4			50			ms
Key Entry Width2	t_{WK2}				50			ms
Key Input Pause Time	t_{PK}				50			ms
Key Entry Debouncing time	t_{CH}				21	23	25	ms
Key Entry Release Guard time	t_{RE}				21	23	25	ms
BEEP TONE Output Start time	t_{BES}	DTMF/BEEPOUT				31		ms
BEEP TONE Output Width	t_{WBE}				39	41	43	ms
$\overline{\text{MUTE}}$ LOW Output Start time	t_{MUS}	MUTE				31		ms
$\overline{\text{MUTE}}$ LOW Output Hold time 1	t_{MUSP1}		10 pps		26	30	34	ms
			20 pps		13	15	17	
			Dual Tone Output		100	110	120	
Pulse Predigital Pause Time	t_{PDP}	PULSEOUT	MA/BR = V_{DD}	10 pps mode	950	980	1016	ms
				20 pps mode	480	510.5	556	
			MA/BR = GND	10 pps mode	950	974	1016	ms
				20 pps mode	480	507.5	556	
Pulse Make Width	t_{WMA}		MA/BR = V_{DD}	10 pps mode	38	39	40	ms
				20 pps mode	19	19.5	20	
			MA/BR = GND	10 pps mode	32	33	34	ms
				20 pps mode	16	16.5	17	
Pulse Break Width	t_{WBR}		MA/BR = V_{DD}	10 pps mode	60	61	62	ms
				20 pps mode	30	30.5	31	
			MA/BR = GND	10 pps mode	66	67	68	ms
				20 pps mode	33	33.5	34	
Pulse Interdigital Pause Time	t_{IDP}		MA/BR = V_{DD}	10 pps mode	900	939	960	ms
				20 pps mode	450	469.5	480	
			MA/BR = GND	10 pps mode	900	933	960	ms
				20 pps mode	450	466.5	480	

continued on next page

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min	Typ	Max	
$\overline{\text{MUTE}}$ LOW Output Hold time 2	t_{MUSP2}	$\overline{\text{MUTE}}$	Single Tone Output	0		8	ms
DUAL TONE Output Time	t_{WDT}	DTMF/BEEPOUT		78	80	82	ms
DTMF Interpause Time	t_{DTP}			78	80	82	ms
Single Tone Output start time	t_{SIS}		SCNT = V_{DD}		31		ms
Single Tone Output stop time	t_{SISP}			0		45	ms
DUAL TONE Output start time	t_{DTS}				39		ms
DUAL TONE Output stop time	t_{DTSP}			0		5	ms
$\overline{\text{MUTE}}$ Hold Time 1 by PAUSE key entry	t_{PSM1}	$\overline{\text{MUTE}}$		0	10	20	ms
$\overline{\text{MUTE}}$ Hold Time 2 by PAUSE key entry	t_{PSM2}			75	90	105	ms
MODEOUT Blinking Start time	t_{MOST}	MODEOUT		0	5	10	ms

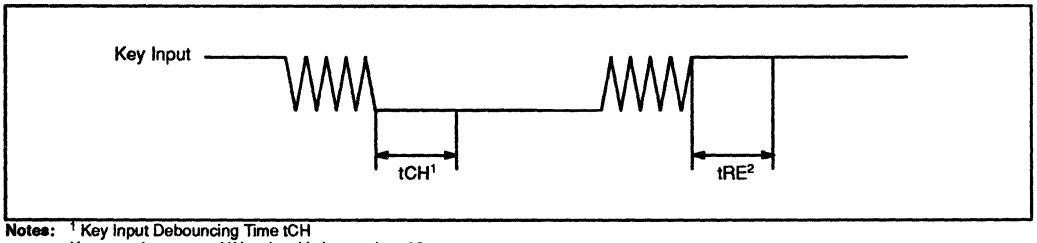
DTMF OUTPUT SIGNALS

Item	Symbol	Standard DTMF (Hz)	DTMF Output Signal* (Hz)	Error to standard TDMF (%)
ROW1	FR1	697	696.95	–0.01
ROW2	FR2	770	770.13	+0.02
ROW3	FR3	852	852.27	+0.03
ROW4	FR4	941	940.99	–0.01
COL1	FC1	1209	1209.31	+0.03
COL2	FC2	1336	1335.65	–0.03
COL3	FC3	1477	1476.71	–0.02

Note: *Oscillation frequency 3.579545 MHz

7

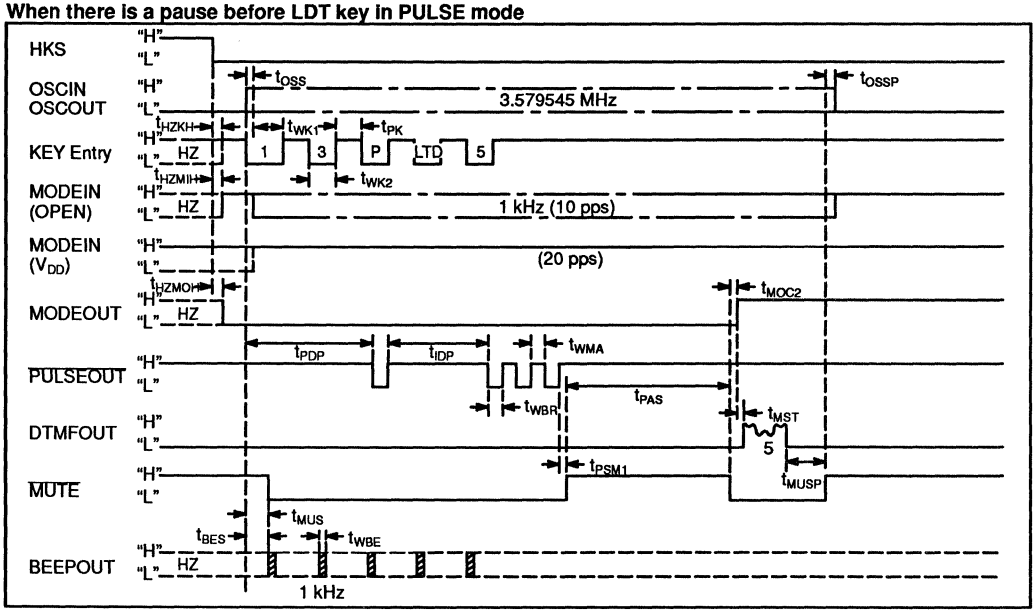
Figure 4. Key Input Timing



Notes: [1] Key Input Debouncing Time tCH
Key entry is accepted if low level is longer than 23 ms typ.
[2]Key Input Release Guard Time tRE
Key release is recognized if low level is longer than 23 ms typ.

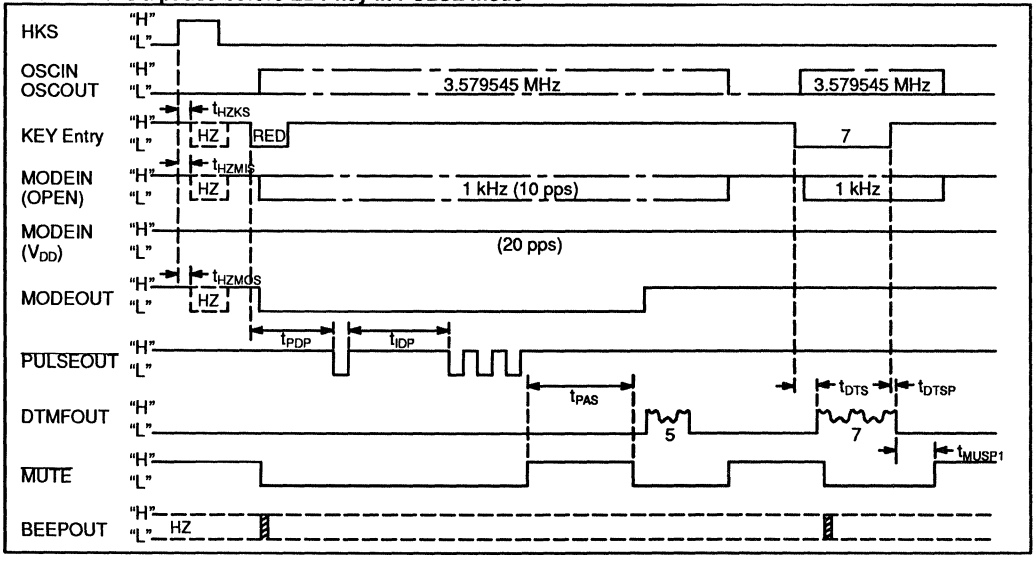
TIMING CHART 1–A

When there is a pause before LDT key in PULSE mode



TIMING CHART 1–B

When there is a pause before LDT key in PULSE mode



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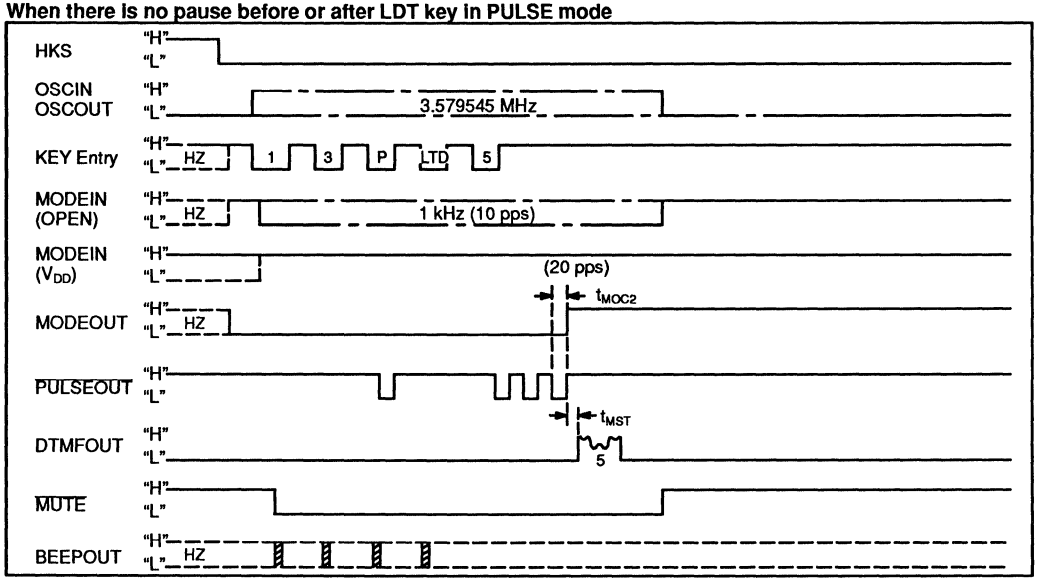
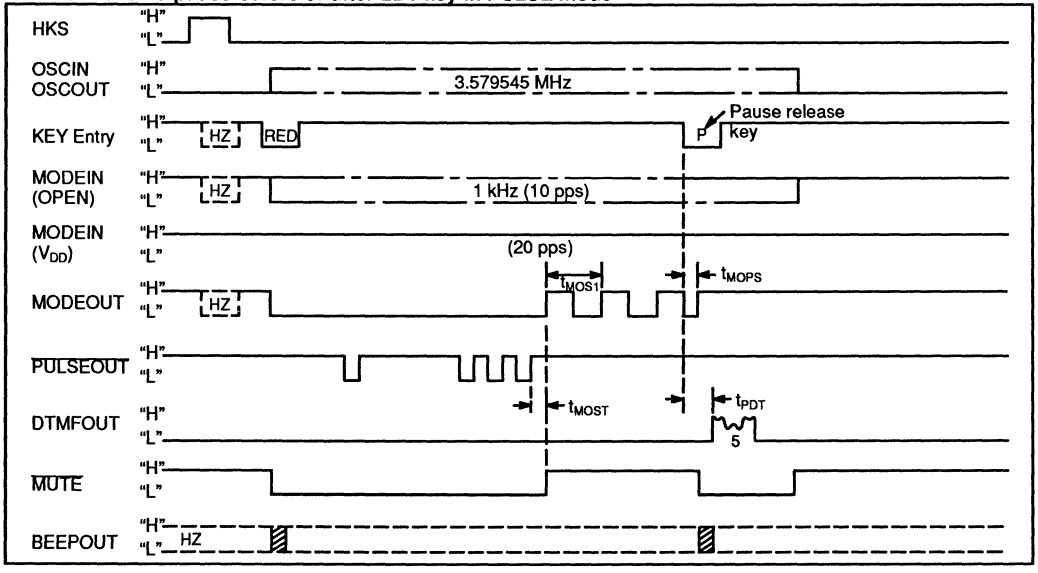
TIMING CHART 2–A

When there is no pause before or after LDT key in PULSE mode



TIMING CHART 2–B

When there is no pause before or after LDT key in PULSE mode



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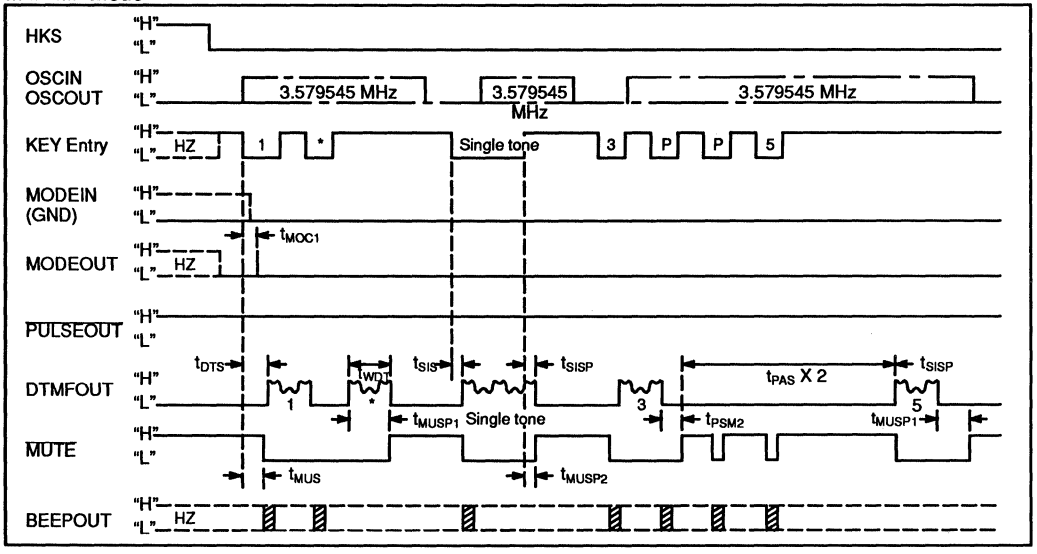
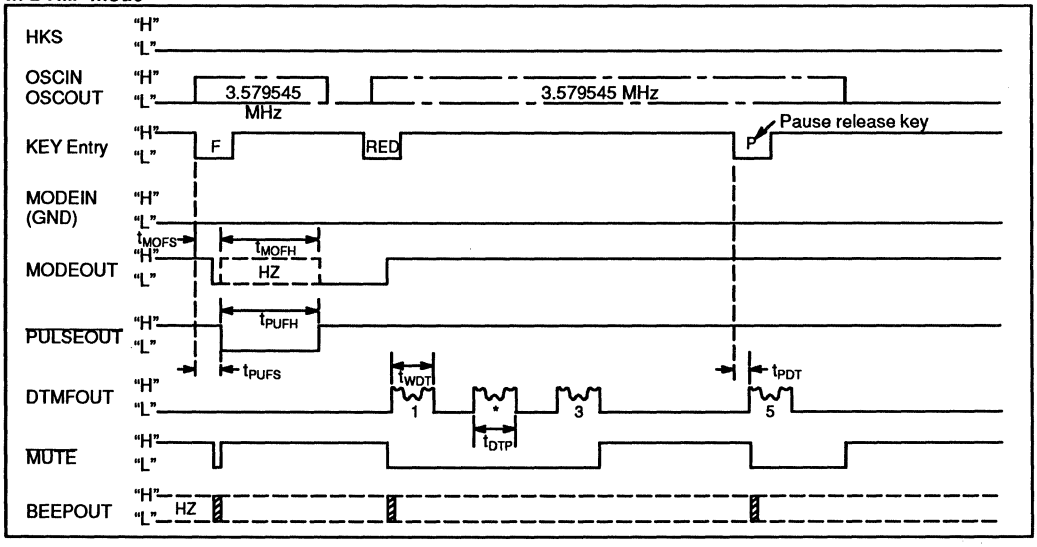
TIMING CHART 3–A

In DTMF mode

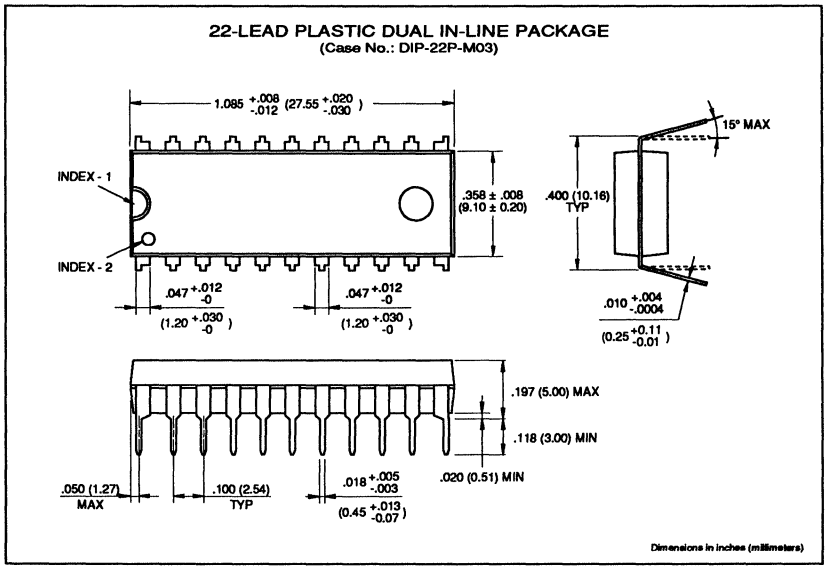


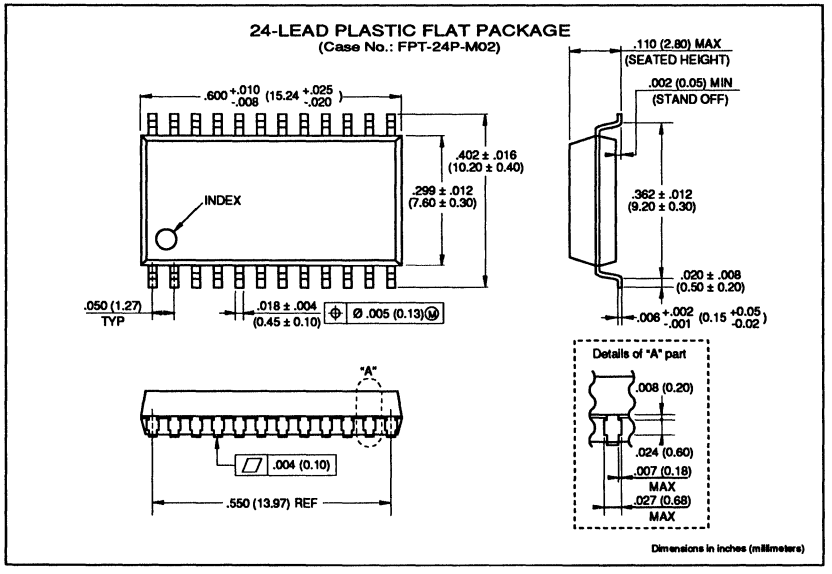
TIMING CHART 3–B

In DTMF mode



PACKAGE DIMENSIONS





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May 1991
Edition 2.0

FUJITSU

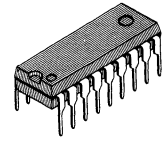
DATA SHEET

MB87057
DTMF RECEIVER

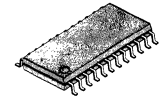
DUAL TONE MULTI FREQUENCY RECEIVER

The MB87057 is a one chip DTMF receiver with an input amplifier gain adjuster and low power consumption, integrating filter and decoder circuits. The MB87057 can automatically set guard times.
This circuit consists of SCFs (Switched Capacitor Filters) and decoders which convert 16 types of DTMF tone pairs into hexadecimal four-bit codes.

- All DTMF receiver functions are integrated on one chip.
- Low power consumption
- Built-in input amplifier gain adjustment circuit
- Automatic guard time setup



PLASTIC PACKAGE
(DIP-18P-M02)



PLASTIC PACKAGE
(FPT-24P-M02)

7

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	+6.0	V
Analog Input Voltage	V_{AIN}	−0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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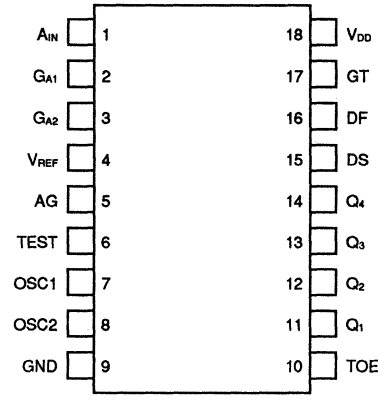
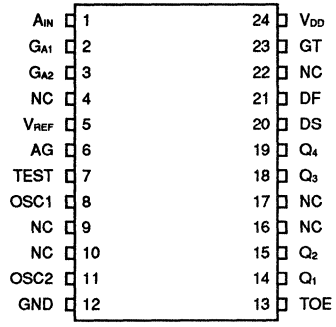
PIN ASSIGNMENT

PIN ASSIGNMENT
(TOP VIEW)



(DIP-18P-M02)

PIN ASSIGNMENT
(TOP VIEW)

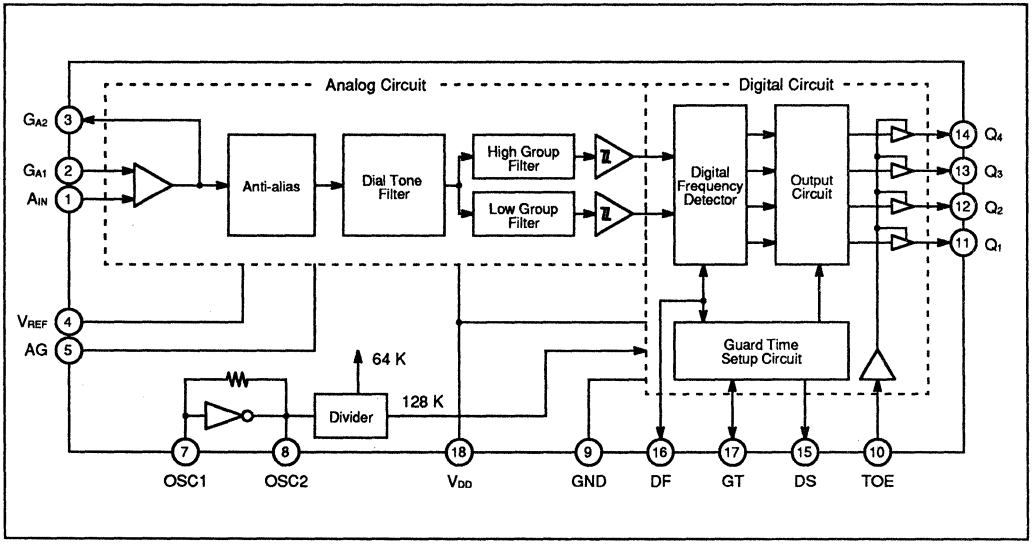


(FPT-24P-M02)

7

BLOCK DIAGRAM

(DIP PACKAGE)



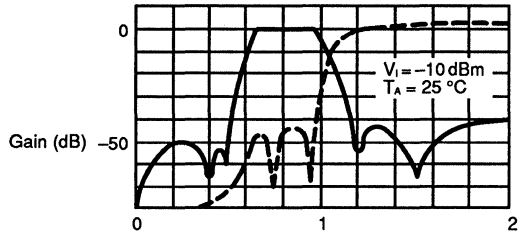
PIN DESCRIPTIONS

Pin Number DIP	Pin Number FPT	Symbol	I/O	Description
1	1	A_{IN}	I	Analog input pin (non-inverted operational amplifier input)
2	2	G_{A1}	I	Operational amplifier gain adjustment pin 1 (inverted operand amplifier input). Operational amplifier gain adjustment pin 2 (operand amplifier output pin). * These pins are provided for operational amplifier gain adjustment. The polarity of G_{A1} is opposite to that of G_{A2}.
3	3	G_{A2}	O	
4	5	V_{REF}	O	Reference voltage output pin. (1/2 V_{DD})
5	6	AG	–	Analog ground pin
6	7	TEST	–	Test pin. Usually set to ground level.
7	8	OSC1	I	Clock input pin. Clock output pin. * Connect a 3.5795 MHz crystal between OSC1 and OSC2 pins.
8	11	OSC2	O	
9	12	GND	–	Ground pin
10	13	TOE	I	Three-state output enable pin. * Data from Q_1 to Q_4 may be output when this pin is set to "High".
11 to 14	14, 15 18, 19	Q_1 to Q_4	O	Three-state data output pin.
15	20	DS	O	Signal detection pin. * This pin goes to "High" when an available tone pair is received and decoded, and the data in the output data-bus is updated.
16	21	DF	O	Frequency detection pin. * This pin goes to "High" when a received tone pair is acknowledged as the valid DTMF signal frequency.
17	23	GT	O	Since "H" has been output, secure the pin in the "Open" or V_{DD} position.
18	24	V_{DD}	–	Positive supply voltage pin. * The voltage must be +5 V ±5%.
–	4, 9 10, 16 17, 22	NC	–	No connection

FUNCTIONAL DESCRIPTIONS

1. FILTER

The filters consist of 3 sixth-order SCFs. The dial tone removal filter (including the 60 Hz filter). Output is connected to the individual hysteresis comparators through the low group and high group filters.
In the figure below, the solid line shows the characteristics of the low group filter while the broken line shows the characteristics of the high group filter. At a frequency of 770 Hz, it is assumed that 0 dB are lost. Therefore, this point is used for reference.



2. DECODER

2.1 Digital Frequency-detecting Circuit

The DF (Detect Frequency) pin goes to "High" when the detector circuit acknowledges the output signals from the two comparators as valid DTMF signal frequencies in the digital frequency detecting block.

2.2 Guard Time Setup Circuit

The automatic setup mode is provided for guard time setup. Guard time has two types: GTP (Guard Time Present) and GTA (Guard Time Absent).

2.2.1 Automatic guard-time setup circuit

The automatic guard time setup circuit sets both t_{GTP} and t_{GTA} to 20 ms. The output signal from the filters may be acknowledged as a DTMF signal if:

① A signal with valid DTMF frequency lasts more than 40 ms. This signal is decoded into a DTMF signal.
These pulses correspond to the input signal enable period and disable period for alternative current characteristics.

② A period of more than 40 ms exists between DTMF signals n and (n + 1). If this is not the case the DTMF signal (n + 1) is disabled.
These pulses correspond to the inter-digit pauses for acceptance and rejection for alternative current characteristics.

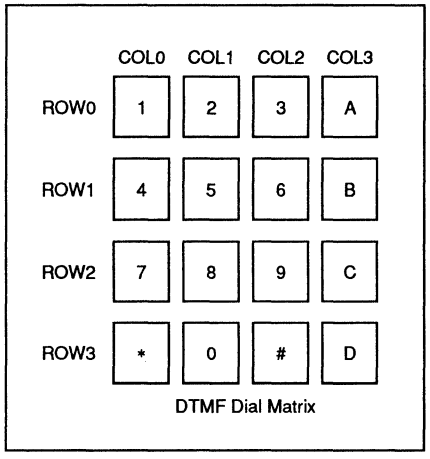
In ①, it takes the DS (Detect Signal) pin GTP to acknowledge that the input signal is a DTMF signal after DF switches to "High". The DS pin switches to "High" when the input signal is acknowledged as a DTMF signal.
In ②, it takes the DS pin GTA to disable DTMF signal n after DF switches to "Low". The DS pin switches to "Low" when the signal is disabled. (See Page 8 for the timing chart.)

$$t_{SDA} > t_{GTP} + t_{PDF}$$
$$t_{IDA} > t_{ADF} + t_{GTA}$$

FUNCTIONAL DESCRIPTIONS

3. OUTPUT CIRCUIT

When the signal detector pin (DS) switches to "High", a received tone pair is stored in the output circuit register. The output latch status may be output on the output bus by setting the three state control input (TOE) to "High".

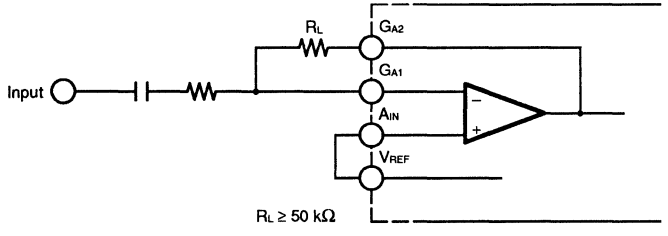


DTMF Dial Matrix

Dial	A_{IN} Input		Input	Output			
	Low group: fo	High group: fo	TOE	Q_4	Q_3	Q_2	Q_1
1	697	1209	1	0	0	0	1
2	697	1336	1	0	0	1	0
3	697	1447	1	0	0	1	1
4	770	1209	1	0	1	0	0
5	770	1336	1	0	1	0	1
6	770	1477	1	0	1	1	0
7	852	1209	1	0	1	1	1
8	852	1336	1	1	0	0	0
9	852	1477	1	1	0	0	1
0	941	1336	1	1	0	1	0
*	941	1209	1	1	0	1	1
#	941	1477	1	1	1	0	0
A	697	1633	1	1	1	0	1
B	770	1633	1	1	1	1	0
C	852	1633	1	1	1	1	1
D	941	1633	1	0	0	0	0

4. SAMPLE DIFFERENCE INPUT CONFIGURATION

The MB87057 uses a difference input amplifier and provides for a bias power source (V_{REF}) to apply a bias voltage to the input signal. This also allows a pin to connect a gain adjustment resistor to the amplifier output.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Minimum	Typical	Maximum	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_I	0	–	V_{DD}	V
Oscillation Frequency	f_{OSC}	3.5759	3.5795	3.5831	MHz
OSC1 Pin Load Capacitance	C_{LDI}	10.0	–	50.0	pF
OSC2 Pin Load Capacitance	C_{LDO}	10.0	–	50.0	pF
GA2 Pin Load Resistance	R_{LA}	50	–	–	kΩ
GA2 Pin Load Capacitance	C_{LA}	–	–	100	pF
Operating temperature	T_A	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Supply Voltage	V_{DD}		4.75	5.0	5.25	V
Power Consumption	P_D	f = 3.58 MHz, V_{DD} = 5 V	–	25	37	mW
Low Level Input Voltage	V_{IL}		0	–	0.8	V
High Level Input Voltage	V_{IH}		2.0	–	V_{DD}	V
Low Level Input Leak Current	I_{IL}	V_I = GND	–10	–	10	µA
High Level Input Leak Current	I_{IH}	$V_I = V_{DD}$	–10	–	10	µA
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA	0	–	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA	2.4	–	V_{DD}	V
V_{REF} Output Voltage	V_{REF}		–	2.5	–	V

AC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Signal Input Level *1		T_A = 25°C, V_{DD} = 5 V	–29	–10	–1	dBm
TWIST *2			–	±10	–	dB
Allowable Frequency Deviation			±1.5 ±2 Hz	–	–	%
Prohibited Frequency Deviation			±3.5	–	–	%
Allowable Noise Level *3			–	–12	–	dB
Allowable Dial Tone Level *4			–	22	–	dB
Input Signal Detection Timing (Present) *5	t_{PDF}		5	11	14	ms
Input Signal Detection Timing (Absent) *5	t_{ADF}		0.5	4	8.5	ms
Input Signal Enable Period (Accept) *5	t_{SDA}		–	–	40	ms
Input Signal Enable Period (Reject) *5	t_{SDR}		20	–	–	ms
Inter-digit Pause (Accept) *5	t_{IPA}		–	–	40	ms
Inter-digit Pause (Reject) *5	t_{IPR}		9	–	–	ms
Input Clock Frequency	f_{IN}		3.5759	3.5795	3.5831	MHz
Clock Rise Time	tr		–	–	110	ns
Clock Fall Time	tf		–	–	110	ns
Clock Duty	DR		–	50	–	%

*1 dBm: 600 ohm reference

*2 TWIST = High group tone voltage/Low group tone voltage

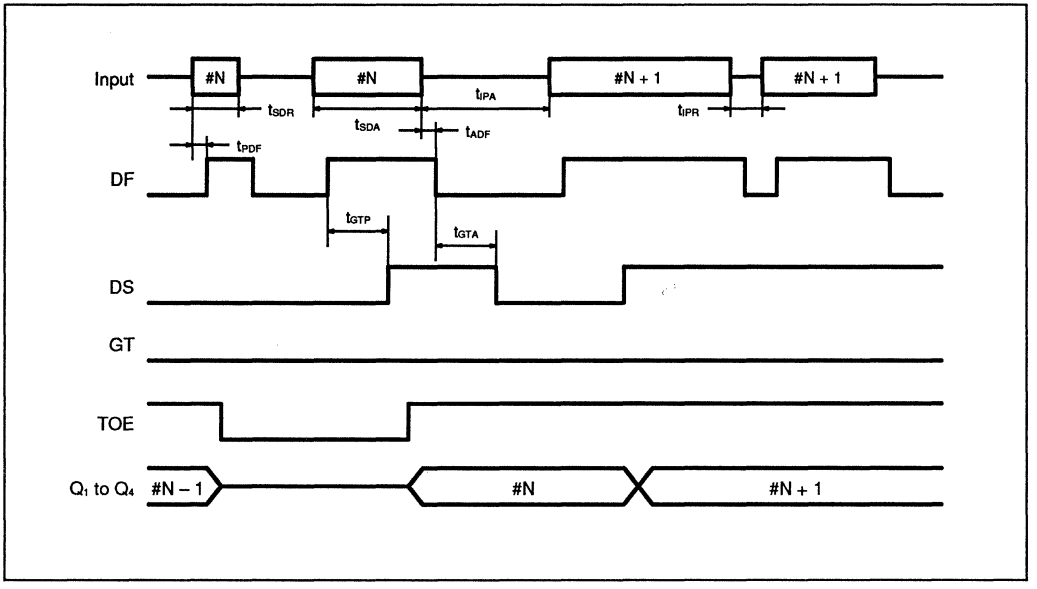
*3 Allowable noise = Total allowable noise within the range 300 Hz to 3.4 kHz/Minimum amplitude tone level in valid tone pairs

*4 Allowable dial tone level = Total allowable normal dial tone volume/Minimum amplitude tone in valid tone pairs

*5 See Timing Chart.

7

TIMING CHART



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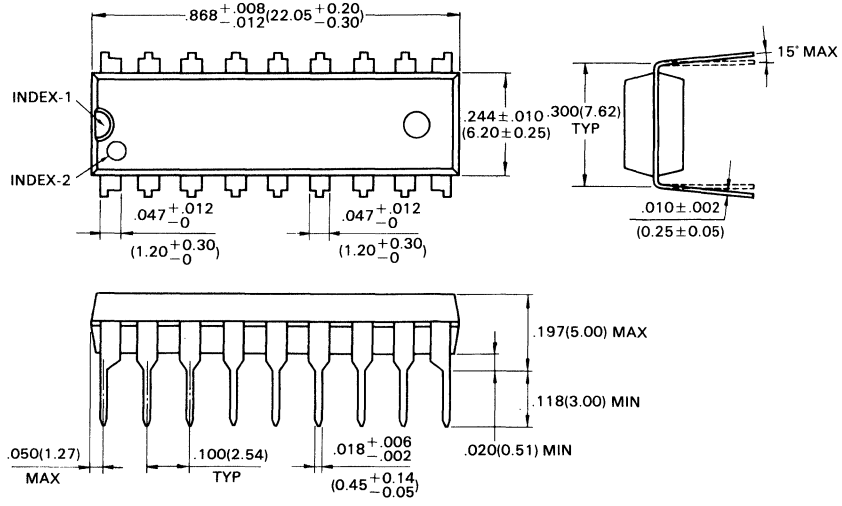
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(case No. : DIP–18P–M02)



Dimensions in inches (millimeters)

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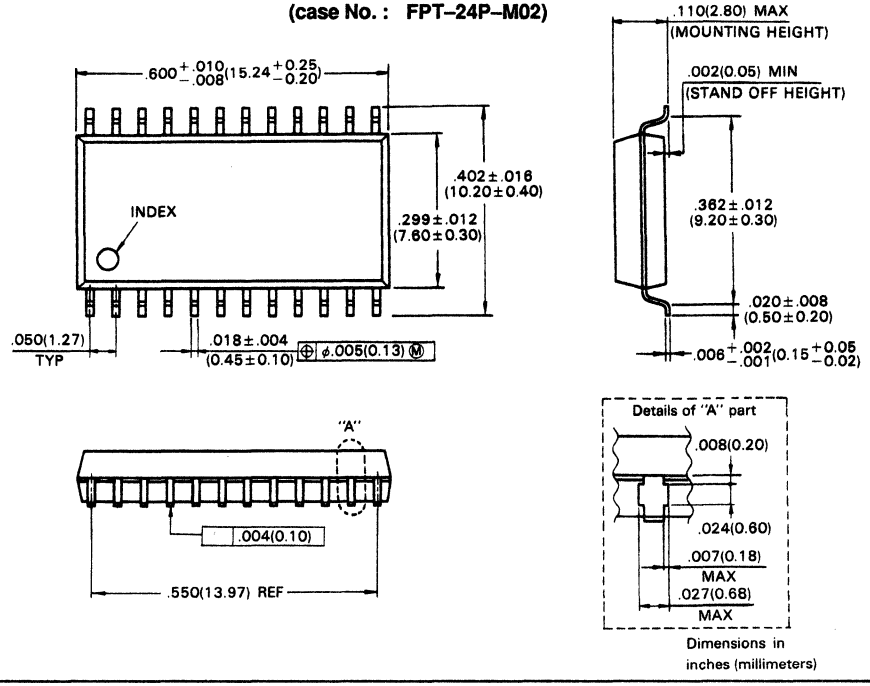
PACKAGE DIMENSIONS

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(case No. : FPT–24P–M02)



Dimensions in inches (millimeters)

7

Section 8

Coders/Decoders (CODECs) — *At a Glance*

Page	Device	Companding Law	Operation	Package Options		
8–3	MB6021A*	μ-Law	Sync/Async	16-pin	Plastic	DIP
	6022A	A-Law	Sync/Async	18-pad	Plastic	LCC

*Available in North America only

8

8

October 1991

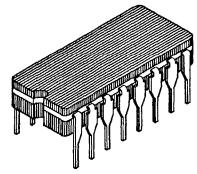
DATA SHEET

FUJITSU

MB6021/6022
PCM CODEC

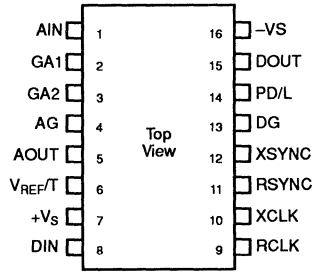
The Fujitsu CMOS BD6020 series consists of both μ-law and A-law single-chip codec/filter ICs for either synchronous-only or sync/async operation. These monolithic, single-channel, voice-frequency codecs incorporate both transmit and receive circuitries that are used for PCM (pulse coded modulation) systems.

- Transmit high-pass and low-pass filters
- Receive low-pass filter with SinX/X Correction
- Anti-aliasing filter
- Conforms to CCITT and AT&T specifications
- Synchronous and asynchronous operation: MB6021, MB6022
- Serial data rates of 64 kHz to 3.152 MHz
- PLL circuits as internal clock generator
- Internal voltage reference
- Internal auto-zero circuit
- TTL compatible digital interface
- Input gain adjust amplifier
- Pin selectable on-chip analog loopback
- μ-law: MB6021
  A-law: MB6022
- Package: 16-pin ceramic DIP package (Suffix: -CZ)



Ceramic Package
CERDIP
DIP-16C-C04

Pin Assignment



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Pin MB6021 MB6022	Min.	Max.	Unit
Positive Supply Voltage	$+V_S$	7	–0.3	7	V
Negative Supply Voltage	$-V_S$	16	–7	0.3	V
Reference Supply Voltage	V_{REF}	6	$-V_S$	$+V_S$	V
Analog Input Voltage	V_{AIN}	1	$-V_S$–0.3	$+V_S$+0.3	V
Digital Input Voltage	V_{DIN1}	8, 9, 10, 11, 12	–0.3	$+V_S$+0.3	V
Digital Input Voltage	V_{DIN2}	14	$-V_S$–0.3	$+V_S$+0.3	V
Storage Temperature	T_{STG}		–55	150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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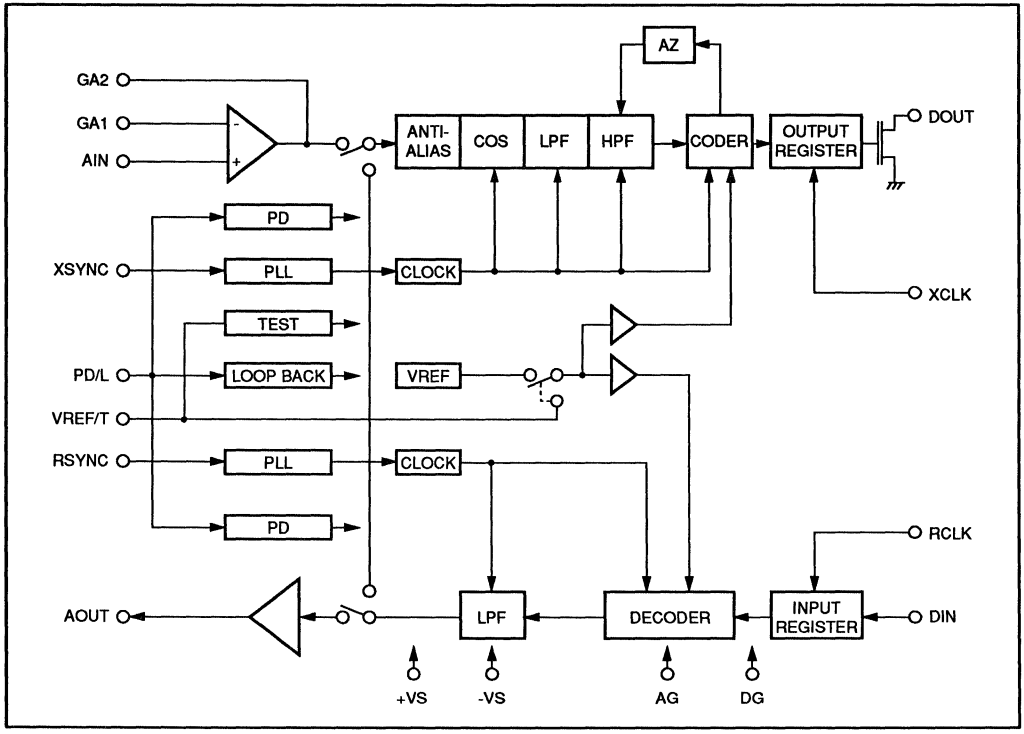
8

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The transmit section in the upper-half of the block diagram is composed of an input gain amplifier, an anti-aliasing filter (ANTI-ALIAS), a band-pass filter (COS, LPT, and HPF), and a compressing coder (CODER). An auto-zero circuit (AZ) is also included in this section. The receive section (lower half) is composed of an expanding decoder (DECODER) and a low-pass filter (LPF).

TRANSMIT SECTION

Analog signals are input to an operational amplifier to provide gain adjustment. This amplifier is followed by a 2nd order analog anti-aliasing filter (ANTI-ALIAS). This filter provides attenuation of 40 dB (typical) at the 256 kHz effective clock frequency of the following switched capacitor cosine filter (COS). From the cosine filter, the signals enter a 5th order low-pass (LPF) clocked at 128 kHz, followed by a 3rd order high-pass filter (HPF) clocked at 128 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCITG.712 recommendation. The output of the high-pass filter is then sampled by the coder (CODEC) at 8 kHz. This coder transforms the analog signals into 8-bit words using compressing law. The encoded PCM data is then output serially from the OUTPUT REGISTER at a frequency determined by the external clock, 64 kHz to 3.152 MHz. An auto-zero circuit (AZ) is utilized for DC offset correction.

RECEIVE SECTION

This filter smooths the decoded signals and corrects for SinX/X attenuation caused by the 8 kHz sample and hold operation. The decoder (DECODER) reconstructs the analog signals from the PCM data using expanding law. The decoder is followed by a 5th order low pass filter (LPF). This filter smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

INTERNAL CLOCK

Two independent phase locked loops (PLL) generate internal clocks for the transmit and receive sections from the respective synchronization clocks (XSYNC and RSYNC).

ANALOG LOOPBACK MODE

The analog loopback mode allows all decoding and coding functions to be exercised without using the analog input (AIN) and analog output (AOUT). In this mode, a digital input signal is decoded and internally routed to the transmit filters.

The output is available from the digital output (DOUT). The analog output (AOUT) is forced to the analog ground (AG) level. The analog loopback mode is selected by connecting the PD/L input to the negative supply voltage (–VS).

POWER DOWN MODE

Two power down modes are provided. The transmit and receive sections independently go into power down operation in the absense of the respective synchronization clock (XSYNC and RSYNC). If the external power down input (PD/L) is connected to a TTL low level, both the transmit and receive section are powered down regardless of the synchronization clocks. During power down operation, AOUT is forced to the level of AG, and DOUT goes into a high-impedance state.

TEST MODE

The VREF/T pin is connected to –VS, test mode allows independent evaluation of the coder and decoder. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. Also, the output of the decoder is made available on pin AOUT.

PIN DESCRIPTION

MB6021, MB6022		
Pin Name	Pin No.	Description
AIN	1	Analog Input. This is an input pin for analog signals to be filtered and coded.
GA1 GA2	2 3	Gain Adjust 1 Gain Adjust 2 These pins are provided for adjusting the gain of transmit section. GA1 and GA2 are the inverting input and output of the amplifier, respectively. GA2 can drive a load impedance of 10 to 20 kΩ and 50 pF or less.
AG	4	Analog Ground. All analog signals are referenced to this pin.
AOUT	5	Analog Output. This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 3 kΩ or greater, and 100 pF or less. This output is forced to AG level in the analog loopback mode and power down mode.
VREF/T	6	Reference Voltage Supply/Test. This pin is provided for the supply of an external voltage reference, for the selection of an internal reference, or for the selection of test mode. If VREF/T is greater than 2 V, the external voltage reference is selected. In this mode, a 2.5 V reference is recommended. If this pin is at the TTL low level or left open, the internal reference (2.5 V) is selected. If this pin is connected to –VS, the test mode with the internal reference results. In this mode, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. Also, the output of the decoder is directly available on the AOUT pin.
+VS	7	Positive Voltage Supply, +5 V ± 5%.
DIN	8	Digital Input. This is a TTL compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK.
RCLK	9	Receive Clock. This TTL compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rates of 64 kHz to 3.152 MHz. The digital PCM codes are accepted on the falling edge of the clock.
XCLK	10	Transmit Clock. This TTL compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (DOUT) pin on the rising edge of the XCLK.
RSYNC	11	Receive Synchronization Clock. This TTL compatible input defines the beginning of the receive timeslot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one RCLK cycle.
XSYNC	12	Transmit Synchronization Clock. This TTL compatible input defines the beginning of the transmit timeslot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one XCLK cycle.
DG	13	Digital Ground. All digital signals are reference to this pin.
PD/L	14	Power Down/Analog Loopback. This three level input is provided for the selection of power down mode or analog loopback mode. If this pin is at the TTL high level, the normal operation is selected. If this pin is at the TTL low level, the device is powered down regardless of the synchronization clocks. If this pin is connected to –VS, the analog loopback mode is selected. In this mode, the output of the receive filter in internally connected to the input of the transmit filter and AOUT is forced to AG level.
DOUT	15	Digital Output. This is a TTL compatible open-drain output. A pull-up resistor greater than 0.5 kΩ must be connected to +VS. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
–VS	16	Positive Voltage Supply, –5 V ± 5%.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value			Unit
			Min.	Typ.	Max.	
Positive Supply Voltage	7	+VS	+4.75	+5.0	+5.25	V
Negative Supply Voltage	16	–VS	–5.25	–5.0	–4.75	V
External Reference Voltage	6	V_{REF}	—	2.5	—	V
Internal Reference Voltage*	6	V_{IREF}	–0.8	0	0.8	V
Digital Output Load Resistance	15	R_{DL}	0.5	—	—	kΩ
Digital Output Load Capacitance	15	C_{DL}	—	—	144	pF
Analog Output Load Resistance	5	R_L	3	—	—	kΩ
Analog Output Load Capacitance	5	C_L	—	—	100	pF
Operating Temperature	—	T_{OP}	0	25	70	°C

Note: *VREF/T pin (pin No. 6) may be left open to select Internal Reference Voltage

8

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin MB6021/22	Symbol	Value			Unit
				Min.	Typ.	Max.	
Positive Supply Current	Operating	7	$+I_{VS}$		7.0	10.0	mA
Negative Supply Current	Operating	16	$-I_{VS}$	–10.0	–5.0	—	mA
Positive Supply Current	XSYNC = RSYNC = VIL SYNC = VIL	7	$+I_{VSST}$	—	1.0	2.0	mA
Power Down Mode	PD/L = VIL			—	0.3	1.0	mA
Negative Supply Current	XSYNC = RSYNC = VIL SYNC = VIL	16	$-I_{VSST}$	–0.5	–0.1	—	mA
Power Down Mode	PD/L = VIL			–0.5	–0.1	—	mA
Reference Supply Current	VREF/T = 2.5 V	6	I_{VREF}	10	40	100	µA
Digital Input High Voltage		8, 9, 10, 11, 12, 14	V_{IH}	2.0	—	+VS	V
Digital Input Low Voltage		8, 9, 10, 11, 12, 14	V_{IL}	0	—	0.8	V
Digital Input High Current		8, 9, 10, 11, 12, 14	I_{IH}	—	—	10	µA
Digital Input Low Current		8, 9, 10, 11, 12, 14	I_{IL}	—	—	10	µA
Digital Input Capacitance		8, 9, 10, 11, 12, 14	C_{DIN1}	—	—	10	pF
Digital Input Capacitance		—	C_{DIN2}	—	—	20	pF
Digital Output Low Voltage	R_{DL} = 0.5 kΩ $+I_{OL}$ = 0.4 mA	15	V_{OL1}	—	—	0.4	V
Digital Output Leakage Current		15	I_{LO}	—	—	10	µA
Digital Output Capacitance		15	C_{DOUT}	—	—	12	pF
Analog Input Offset Voltage		1	A_{INOFF}	–200	0	200	mV
Analog Input Resistance		1	R_{AIN}	300	—	—	kΩ
Analog Input Capacitance		1	C_{AIN}	—	—	10	pF
Analog Output Offset Voltage		5	A_{OUTOFF}	–150	—	150	mV
Analog Output Resistance		5	R_{AOUT}	—	10	30	Ω

8

AC CHARACTERISTICS (MB6021, MB6022)

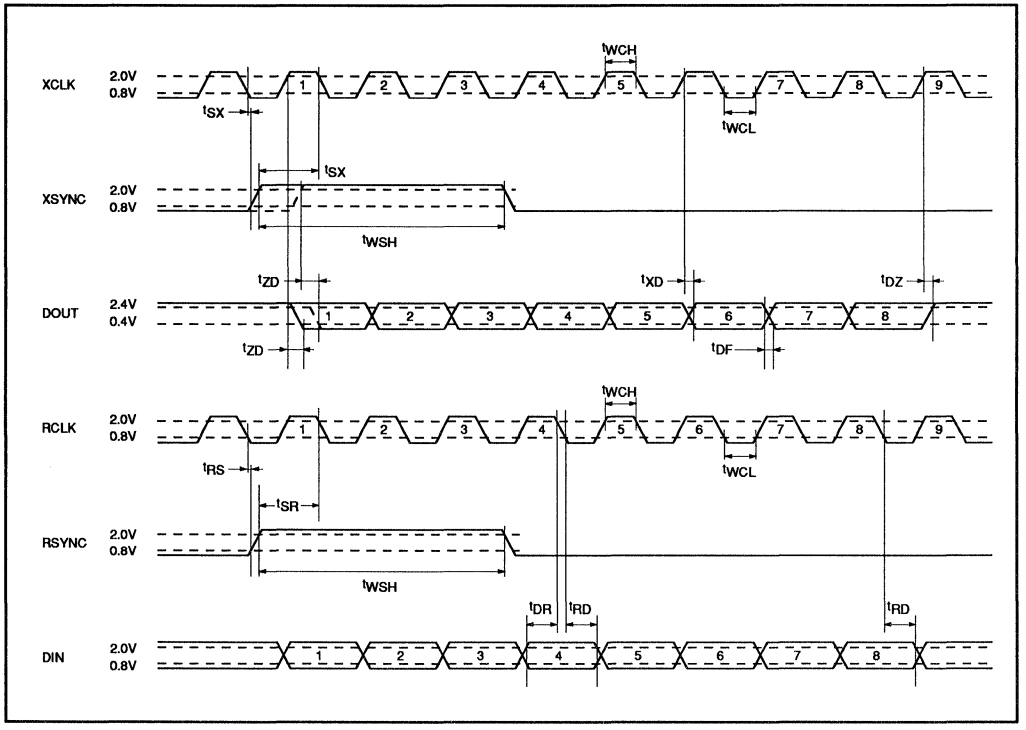
(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Pin MB6021/22	Symbol	Value			Unit
				Min.	Typ.	Max.	
Digital Input Rise Time	0.8 V → 2.0 V	8, 9, 10, 11, 12	t_r	—	—	50	ns
Digital Input Fall Time	2.0 V → 0.8 V	8, 9, 10, 11, 12	t_f	—	—	50	ns
Shift Clock Frequency	—	9, 10	F_C	64	—	3152	kHz
Shift Clock High Width	V_{IH} = 2.0 V	9, 10	t_{WCH}	140	—	—	ns
Shift Clock Low Width	V_{IL} = 0.8 V	9, 10	t_{WCL}	140	—	—	ns
Synchronization Frequency	—	11, 12	F_S	—	8	—	kHz
Synchronization High Width	V_{IH} = 2.0 V	11, 12	t_{WSH}	1/Fc Fc: MHz)	—	117	µA
XSYNC to XCLK Delay	—	10, 12	t_{SX}	100	—	—	ns
XCLK to XSYNC Delay	—	10, 12	t_{XS}	50	—	—	ns
RSYNC to RCLK Delay	—	9, 11	t_{SR}	100	—	—	ns
RCLK to RSYNC Delay	—	9, 11	t_{RS}	50	—	—	ns
RCLK to DIN Delay	—	8, 9	t_{RD}	50	—	—	ns
DIN to RCLK Delay	—	8, 9	t_{DR}	50	—	—	ns
XCLK or XSYNC to DOUT Delay	Note 1, Bit 1	10, 12, 15	t_{ZD}	30	—	200	ns
XCLK to DOUT Delay	Note 1, Bit 2 – 8	10, 15	t_{XD}	30	—	—	ns
XCLK to DOUT Disable Time	High-Z	10, 15	t_{DZ}	30	—	—	ns
DOUT Fall Time	—	15	t_{DF}	10	—	100	ns

Note: DOUT Load Conditions: R_{DL} = 0.5 kΩ, C_{DL} = 144 pF, $+I_{OL}$ = 0.4 mA

8

TIMING DIAGRAM



8

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min.	Typ.	Max.	
Signal to Distortion (A to A)	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDA	35.0 30.0 25.0	—	—	dB dB dB
Signal to Distortion (A to D)	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDX	36.0 31.0 26.0	—	—	dB dB dB
Signal to Distortion (D to A)	1020 Hz tone (C message)	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDR	36.0 31.0 26.0	—	—	dB dB dB
Gain Tracking (A to A)	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTX	–0.4 –0.8 –2.0	—	0.4 0.8 2.0	dB dB dB
Gain Tracking (A to D)	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTX	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Gain Tracking (D to A)	1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTR	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
Frequency Response (A to A)	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		FRA	24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6 	dB dB dB dB dB dB
Frequency Response (A to D)	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		FRX	24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB
Frequency Response (D to A)	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0 dBm0, 820 Hz		FRR	–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB

Notes: 1. $29\,(1 - \mathrm{Sin}\,\frac{\pi(4000 - f)}{1200})$

2. $29\,(1 - \mathrm{Sin}\,\frac{\pi(4000 - f)}{1200})$

8

TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021) (Continued)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Idle Channel Noise (A to A)	C message	ICNA	—	–80	–72.0	dBm0c
Idle Channel Noise (A to D)	C message	ICNX	—	–83	–74.0	dBm0c
Idle Channel Noise (D to A)	C message	ICNR	—	–83	–78.0	dBm0c
Crosstalk (A to A)	1020 Hz, 0dBm0	CTA	—	—	–66	dB
Crosstalk (D to D)	1020 Hz, 0dBm0	CTD	—	—	–66	dB
Absolute Level	Overload Level 3.17 dMb0	VABS	—	2.500	—	V_{OP}
Analog Input Level	1020 Hz, 0dBm0 ±VS = ±5.0 V, T_A = 25 °C	AIL	—	1.227	—	V_{rms}
Analog Output Level	1020 Hz, 0dBm0 ±VS = ±5.0 V, T_A = 25 °C	AOL	1.206	1.227	2.248	V_{rms}
Gain Accuracy (A to A)	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C	GAA	–0.5 –0.3	0 0	+0.5 +0.3	dB dB
Gain Accuracy (A to D)	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C Variation with power supply Variation with temperature	GAX	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Gain Accuracy (D to A)	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A = 25 °C Variation with power supply Variation with temperature	GAR	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/°C
Propagation Delay (A to A)	FC ≥ 1544 kHz	PDA	—	—	540	μs

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TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021) (Continued)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Delay to Distortion (A to A)	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to minimum delay	DDA	—	—	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	0 < f ≤ 50 kHz Idle Channel Noise (C Message) +VS +50 m V_{OP} AIN = AG	PSRRA+	25	30	—	dB
PSRR (–VS) (A to A)	0 < f ≤ 50 kHz Idle Channel Noise (C Message) –VS +50 m V_{OP} AIN = AG	PSRRA–	35	40	—	dB
Intermoduration (A to A)	AIN a. 0.47 kHz, – 10 dBm0 b. 0.32 kHz, – 10 dBm0 AOUT (a – b)	IMA1	—	—	–38	dB
Intermoduration (A to A)	AIN a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 AOUT (2a – b)	IMA2	—	—	–52	dBm0
Signal Frequency Noise (A to A)	0 to 4 kHz 4 to 200 kHz AIN = AG	SFNA	—	—	–70 –50	dBm0 dBm0
Discrimination (A to A)	AIN = 0dBm0 4.6 to 200 kHz	DISA	30	—	—	dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN = 0dBm0, 700 – 1100 Hz	IBSA	43	—	—	dB

8

TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022)

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions		Symbol	Value			Unit
				Min.	Typ.	Max.	
Signal to Distortion (A to A)	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDA	35.0 30.0 25.0	—	—	dB dB dB
	CCITT G.712 Method 1	–3 dBm0 –6 to –27 dBm0 –34 dBm0 –40 dBm0 –55 dBm0		28.0 35.5 33.5 28.5 13.5	—	—	dB dB dB dB dB
Signal to Distortion (A to D)	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDX	36.0 31.0 26.0	—	—	dB dB dB
	CCITT G.712 Method 1	–3 dBm0 –6 to –27 dBm0 –34 dBm0 –40 dBm0 –55 dBm0		30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB
Signal to Distortion (D to A)	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to –30 dBm0 –40 dBm0 –45 dBm0	SDR	36.0 31.0 26.0	—	—	dB dB dB
	CCITT G.712 Method 1	–3 dBm0 –6 to –27 dBm0 –34 dBm0 –40 dBm0 –55 dBm0		30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB

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TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022) (Continued)

Parameter	Conditions		Symbol	Value			Unit
				Min.	Typ.	Max.	
Gain Tracking (A to A)	CCITT G.712 Method 2 1020 Hz tone	+3 to –30 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTA	–0.4 –0.8 –2.0	—	0.4 0.8 2.0	dB dB dB
	CCITT G.712 Method 1	–10 to –50 dBm0 –55 to –60 dBm0		–0.5 –1.0	—	0.5 1.0	dB dB
Gain Tracking (A to D)	CCITT G.712 Method 2 1020 Hz tone	+3 to –30 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTX	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
	CCITT G.712 Method 1	–10 to –50 dBm0 –50 to –55 dBm0 –55 to –60 dBm0		–0.25 –0.4 –0.8	—	0.25 0.4 0.8	dB dB dB
Gain Tracking (D to A)	CCITT G.712 Method 2 1020 Hz tone	+3 to –40 dBm0 –40 to –50 dBm0 –50 to –55 dBm0	GTR	–0.2 –0.4 –0.8	—	0.2 0.4 0.8	dB dB dB
	CCITT G.712 Method 1	–10 to –50 dBm0 –50 to –55 dBm0 –55 to –60 dBm0		–0.25 –0.4 –0.8	—	0.25 0.4 0.8	dB dB dB
Frequency Response (A to A)	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		FRA	24.0 –0.2 –0.2 –0.2 Note 1 64.0	—	 0.3 1.6 	dB dB dB dB dB dB
Frequency Response (A to D)	0 to 60 Hz 60 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		FRX	24.0 –0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB dB
Frequency Response (D to A)	0 to 300 Hz 300 to 3000 Hz 3000 to 3400 Hz 3400 to 4600 Hz 4.6 to 12 kHz Relative to 0dBm0, 820 Hz		FRR	–0.1 –0.1 –0.1 Note 2 32.0	—	 0.15 0.8 	dB dB dB dB dB

Notes: 1. $29\,(1 - \mathrm{Sin}\,\frac{\pi(4000 - f)}{1200})$

2. $14.5\,(1 - \mathrm{Sin}\,\frac{\pi(4000 - f)}{1200})$

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TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022) (Continued)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Idle Channel Noise (A to A)	P Message	ICNA	—	–80	–72.0	dBm0p
Idle Channel Noise (A to D)	P Message	ICNX	—	–83	–74.0	dBm0p
Idle Channel Noise (D to A)	P Message	ICNR	—	–83	–78.0	dBm0p
Crosstalk (A to A)	1020 Hz, 0dBm0	CTA	—	—	–66	dB
Crosstalk (D to D)	1020 Hz, 0dBm0	CTD	—	—	–66	dB
Absolute Level	Overload Level 3.14 dBm0	VABS	—	2.500	—	V_{OP}
Analog Input Level	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A 25 °C	AIL	—	1.231	—	V_{rms}
Analog Output Level	1020 Hz, 0dBm0 Internal VREF ±VS = ±5.0 V, T_A 25 °C	AOL	1.210	1.231	1.252	V_{rms}
Gain Accuracy (A to A)	1020 Hz, 0dBm0 Internal VREF ± VS = ± 5.0 V, T_A 25 °C	GAA	–0.5 –0.3	0 0	+0.5 +0.3	dB dB
Gain Accuracy (A to D)	1020 Hz, 0dBm0 Internal VREF ± VS = ± 5.0 V, T_A 25 °C Variation with Power Supply Variation with Temperature	GAX	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/ °C
Gain Accuracy (D to A)	1020 Hz, 0dBm0 Internal VREF ± VS = ± 5.0 V, T_A 25 °C Variation with Power Supply Variation with Temperature	GAR	–0.25 –0.15	0 0 ±0.02 ±0.001	+0.25 +0.15	dB dB dB dB/ °C
Propagation Delay (A to A)	FC ≥ 1544 kHz	PDA	—	—	540	µs

8

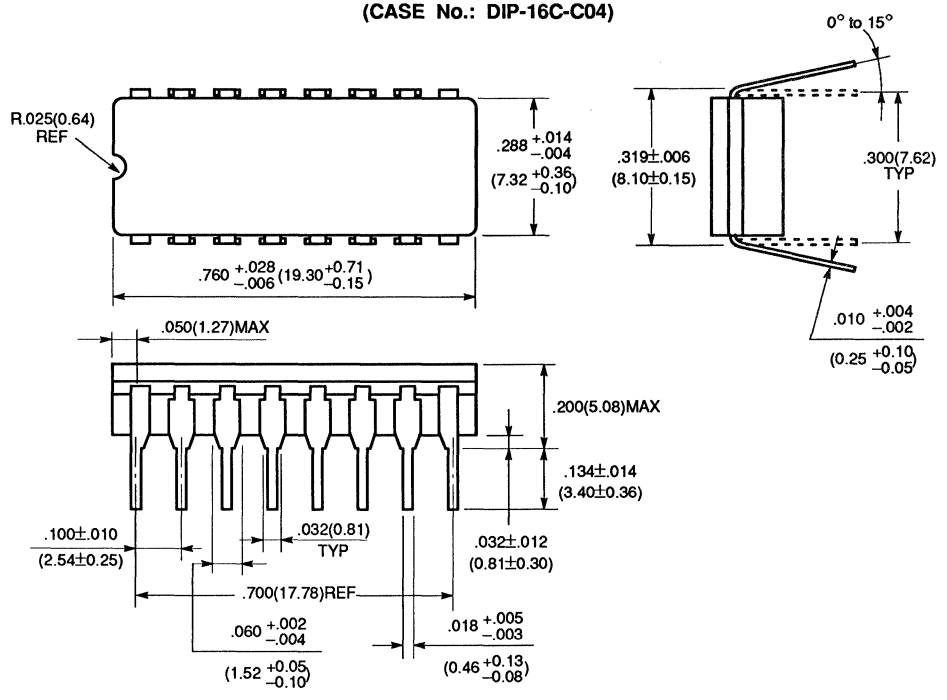
TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022) (Continued)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Delay to Distortion (A to A)	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to Minimum Delay	DDA	—	—	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	$0 < f \leq 50$ kHz Idle Channel Noise (P Message) +VS +50 m V_{OP} AIN = AG	PSRRA+	25	30	—	dB
PSRR (–VS) (A to A)	$0 < f \leq 50$ kHz Idle Channel Noise (P Message) +VS +50 m V_{OP} AIN = AG	PSRRA–	35	40	—	dB
Intermoduration (A to A)	AIN a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 AOUT (2a–b)	IMA1	—	—	–38	dB
Intermoduration (A to A)	AIN a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 AOUT (a–b)	IMA2	—	—	–52	dBm0
Single Frequency Noise (A to A)	0 to 4 kHz 4 kHz to 200 kHz AIN = AG	SFNA	—	—	–70 –50	dBm0 dBm0
Discrimination (A to A)	AIN = dBm0 4.6 kHz to 200 kHz	DISA	30	—	—	dB
In Band Spurious (A to A)	2nd, 3rd Harmonic AIN = dBm0, 700 to 1100 kHz	IBSA	43	—	—	dB

8

PACKAGE DIMENSIONS

16-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C04)



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Dimensions in
inches (millimeters)

8

Section 9

Quality and Reliability — *At a Glance*

Page
9–3 Quality Control at Fujitsu 9–4 Quality Control Processes at Fujitsu

9

Quality Control at Fujitsu

Built-in Quality and Reliability

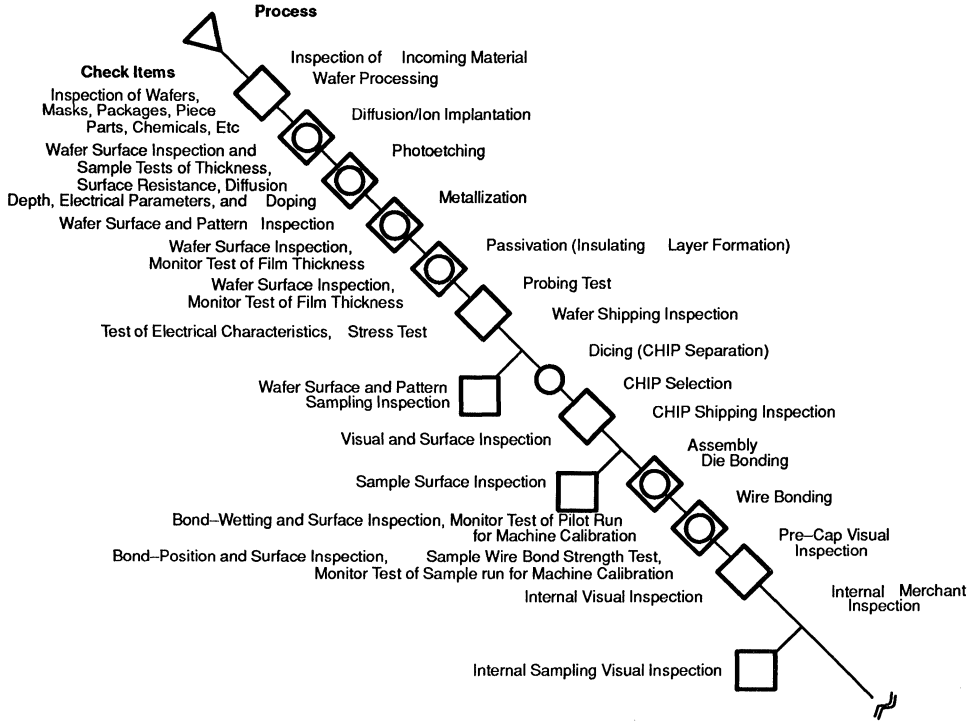
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Processes at Fujitsu



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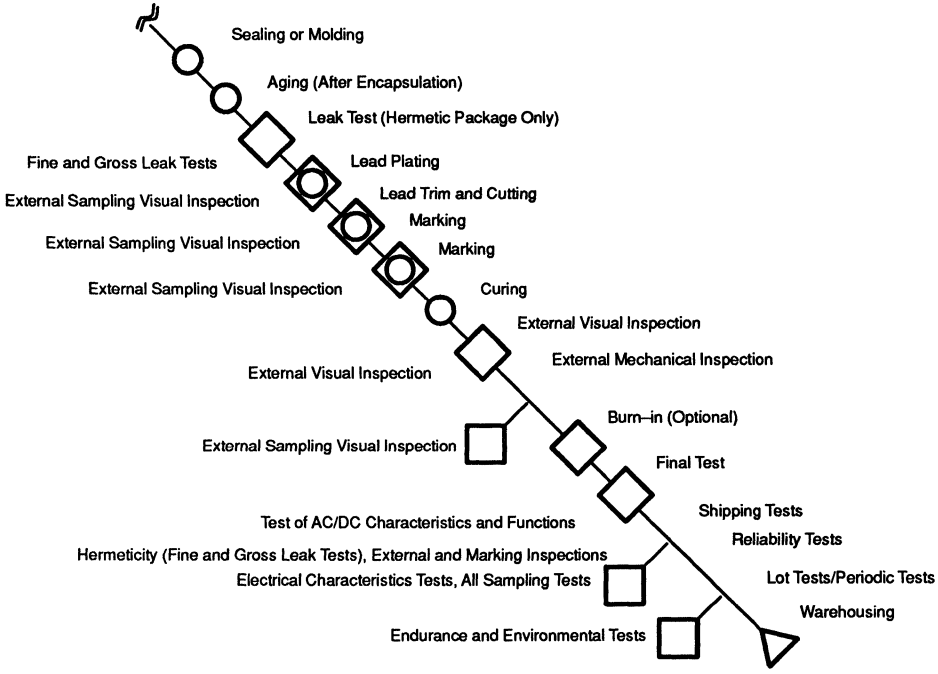
9

Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

9

Section 10

Ordering Information — *At a Glance*

Page	Title
10–3	IC Packages, Inserted Types
10–4	IC Packages, Surface Mounted Types
10–6	Part Number System

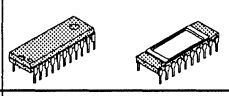
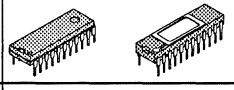
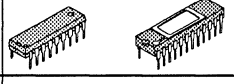
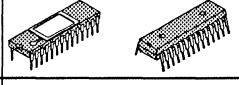
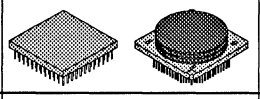
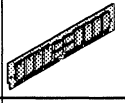
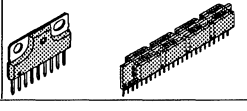
IC Packages

This section on Fujitsu packages is arranged as follows:

1. Package technology: inserted or surface mount types.
2. Package types within the technology.
3. Package type illustration and description with (a) package width(s) and (b) lead pitch (when applicable).
4. Package material.
5. Package ordering code. This code appears as a suffix to the product part number. See Part Number System in this section.

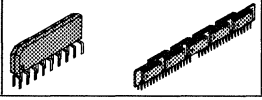
For the most up-to-date device and packaging information, including available packages and exact ordering code, please contact your nearest Fujitsu Sales Office, Sales Representative, or Distributor. (See the Sales Information section of this book.)

Inserted Packages

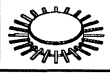
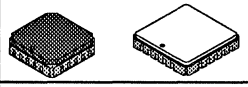
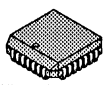
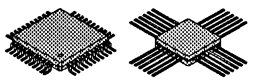
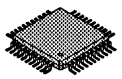
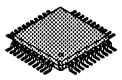
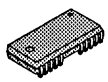
Package Type		Description	Package Material	Fujitsu Ordering Code (Suffix)
DIP		Dual In-line Package Package widths: 300, 400, 600, 900 mil Lead pitch: 100 mil	Plastic	P or M[1]
			CerDIP	Z
			Ceramic with frit seal	T
			Ceramic with metal seal	C
SH DIP		Shrink Dual In-line Package Lead pitch: 70 mil	Plastic	PSH
			CerDIP	ZSH
			Ceramic with frit seal	TSH
			Ceramic with metal seal	CSH
SK DIP		Skinny Dual In-line Package Package width: 300 mil Lead pitch: 100 mil	Plastic	PSK
			CerDIP	ZSK
			Ceramic with frit seal	TSK
			Ceramic with metal seal	CSK
SL DIP		Slim Dual In-line Package Package width: 400 mil Lead pitch: 100 mil	Plastic	PSL
			CerDIP	ZSL
			Ceramic with frit seal	TSL
			Ceramic with metal seal	CSL
PGA		Pin Grid Array Package Lead pitch: 50/100 mil	Plastic	PR
			Ceramic with metal seal	CR
SIM		Single In-line Packag (For modules only.)	Plastic	PS
SIP		Single In-line Package Lead pitch: 100 mil	Plastic	PL

Continued on next page

Inserted Packages (Continued)

Package Type		Description	Package Material	Fujitsu Ordering Code (Suffix)
ZIP		Zig-zag In-line Package Package width: 100 mil Lead pitch:50 mil 100 mil (modules)	Plastic	PSZ

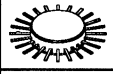
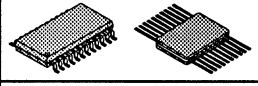
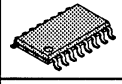
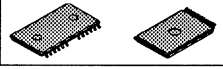
Surface Mount Packages

Package Type		Description	Package Material	Fujitsu Ordering Code (Suffix)
FPT		Flat (Disk Button type) Package	Ceramic	CF
LCC		Leadless Chip Carrier Lead pitch: 40, 50 mil	Ceramic with Frit seal	TV
			Ceramic with metal seal	CV
PLCC		(Plastic) Leaded Chip Carrier Lead pitch: 50 mil	Plastic	PD or PV
QFP		Quad Flat Package Lead pitch: 0.65, 0.80, 1.00 mm; 0.50 mm for straight leads	Plastic	PFQ
			Ceramic	CFQ
SQFP		Shrink Quad Flat Package Lead pitch: 0.50 mm	Plastic	PFQV or PFV
TQFP		Thin Quad Flat Package (Thin profile) Lead pitch: 0.50 mm	Plastic	PFT
SOJ		Small Outline Package with J-leads Lead pitch: 50 mil	Plastic	PJ
			Ceramic	CJ

Continued on next page

10

Surface Mount Packages (Continued)

Package Type		Description	Package Material	Fujitsu Ordering Code (Suffix)
FPT		Flat (Disk Button type) Package	Ceramic	CF
SOP		Small Outline Package Lead pitch: 50 mil	Plastic	PF
			Ceramic	CF
			Cerpack with gullwing leads	ZFL
			Ceramic with metal seal and gullwing leads	CFL
SSOP		Shrink Small Outline Package Lead Pitch: 0.65, 0.80, 1.00 mm	Plastic	PFV
TSOP		Thin Small Outline Package (Thin profile) Lead pitch: 0.50, 0.55, 0.60 mm	Plastic with normal leads	PFTN
			Plastic with reverse bend leads	PFTR

Memory Cards

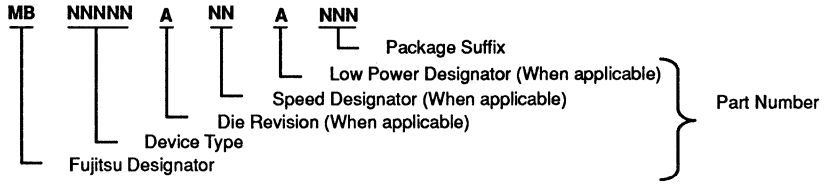
Package Type		Description	Package Material	Fujitsu Ordering Code (Suffix)
68-Pin Card		68-Pin Card	Plastic	—

10

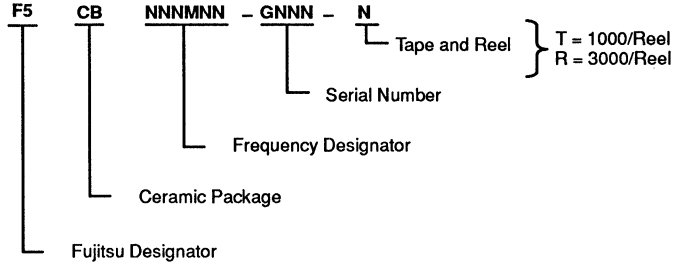
Part Number System

Standard Products Part Number

Found on most Standard Products: Memory, Analog, Logic, Telecommunications, Microprocessor, and Special Controller Products



8-Pin SMT Piezoelectric SAW Filter



Examples:

Memory Product, MB81C1001A–60 PFTN

MB	Fujitsu
81C1001	DRAM Device
A	Die Revision
60	Access Speed (60 ns)
L	Low Power Feature
PFTN	Plastic SOP (Package) with normal leads

Telecommunications Product, MB87086AP

MB	Fujitsu
87086	PLL Device
A	Die Revision
P	Plastic DIP (Package)

Analog Product, MB3731PS

MB	Fujitsu
3731	Audio Power Amplifier
PS	Plastic SIP (Package)

Controller Product, MB8876AC

MB	Fujitsu
8876	Floppy Disk Controller
A	Die Revision
C	Ceramic DIP (Package) with metal seal

10

Section 11

Sales Information — *At a Glance*

Page	Title
11–3	Introduction to Fujitsu
11–3	Fujitsu Limited (Japan)
11–4	Fujitsu Microelectronics, Inc. (U.S.A.)
11–6	Fujitsu Electronic Devices Europe
11–8	Fujitsu Microelectronics Asia PTE Ltd. (Singapore)
11–9	Integrated Circuits Corporate Headquarters – Worldwide
11–10	FMI Sales Offices for North and South America
11–11	FMI Representatives – USA
11–14	FMI Representatives – Canada, Mexico, and Puerto Rico
11–15	FMI Distributors – USA
11–17	FMI Distributors – Canada
11–18	FMG, FML, and FMIL Sales Offices for Europe
11–19	FMG, FML, and FMIL Distributors – Europe
11–20	FMAP Sales Offices for Asia, Australia and Oceania
11–21	FMAP Representatives – Asia and Australia
11–21	FMAP Distributors – Asia

Introduction to Fujitsu

Fujitsu Limited (Japan)

Fujitsu Limited was founded as a telecommunications equipment manufacturer in 1935, and today is not only one of Japan's leading telecommunications companies, but also one of the world's largest computer manufacturers.

This leadership has resulted, at least in part, from the superb quality of the company's semiconductors and electronic components. Manufactured by the company's Electronics Devices Operations Group, these vital electronic devices also contribute to the high reliability and performance of products made by many other manufacturers around the world.

Today, Fujitsu is one of the world's top manufacturers of semiconductors and electronic components. In Japan, Fujitsu's R&D laboratories for semiconductor and electronic components are situated in Kawasaki and Mie, and manufacturing works are located in Iwate, Aizu, Wakamatsu and Suzaka. Fujitsu also has six affiliated manufacturing works in the country. Overseas facilities in the U.S, Europe, and Asia also help to meet the growing global demand for Fujitsu semiconductors and electronic components.

Fujitsu enforces strict quality control at all stages of production, from materials selection through manufacturing to final testing. As a result, Fujitsu's electronic devices are known for their extremely high reliability and excellent cost-to-performance ratio.

Fujitsu manufactures a full line of semiconductors and electronic components to meet the diverse applications of a wide variety of customers. Backed by Fujitsu's extensive R&D commitment equal to over 10 percent of annual sales, Fujitsu's electronic devices stay on the cutting edge of electronics technology.

Introduction to Fujitsu

Fujitsu Microelectronics, Inc. (U.S.A.)

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to four marketing divisions and two manufacturing divisions. FMI offers a complete array of components including semiconductor products for its customers throughout North and South America.

The Advanced Products Division (APD) is responsible for designing and selling a full line of SPARC processors, peripheral chips, and the EtherStar™ LAN controller that it designed. The EtherStar LAN controller is the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of a cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs FETs and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The Electronic Components Division (ECD) markets connectors, keyboards, thermal printers, plasma displays, and relays.

The largest FMI marketing division is the Integrated Circuits Division (ICD) which markets the following standard devices, components, and ASICs.

Memory Products	BiCMOS SRAMs Bipolar PROMs CMOS Masked ROMs CMOS SRAMs DRAMs ECL RAMs EEPROMs EPROMs NOVRAMs STRAMs (self-timed RAMs)
Memory Module Products	DRAM modules
Memory Card Products	Memory Cards: EPROM, Flash, OTPROM, and SRAM Controller Design kits Programming adaptors
Telecommunication Products	CODECs Modems Piezoelectric devices PLLs Prescalers Telephone ICs VCOs

Introduction to Fujitsu

Microprocessor Products	4-bit microcontrollers DSPs
Logic Products	Interface devices Translator circuits Ultra high-speed ECL
Analog Products	Audio ICs Comparators Converters, A/D and D/A Darlington transistor arrays Disk drive ICs Linear devices MOSFET arrays Motor drivers Operational amps Power supply control ICs RETs VCOs
Hybrid Products	Custom modules Multi-chip modules Thick- and Thin-film T^2
Special Purpose Controller Products	SCSI controllers Data communication controllers: ECC, Ethernet, Floppy disk, Multiprotocol, and DMA Video controllers: CRT, PIP, and TV display
ASIC Products	CMOS gate arrays (channeled and channelless) ECL gate arrays BiCMOS gate arrays GaAs gate arrays CMOS standard cells ASIC Gallery™ (SuperMacros™, Compiled Cells) CAD Reference Environment that integrates with third-party CAD tools

Introduction to Fujitsu

Design and customer support for ASIC products are available throughout the country and at FMI Sales Offices located in Atlanta, Boston, Chicago, Dallas, Denver, Irvine, Minneapolis, Portland, and San Jose,

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division (SMD) assembles and tests memory devices. The Gresham Manufacturing Division (GMD) began manufacturing in 1988. GMD fabricates wafers, and produces ASIC products and DRAM memories.

Introduction to Fujitsu

Fujitsu Electronic Devices Europe:

Fujitsu Mikroelektronik GmbH (FMG), West Germany
Fujitsu Microelectronics Limited (FML), U.K.
Fujitsu Microelectronics Italia S.R.L (FMIL), Italy
Fujitsu Microelectronics Ireland, Ltd. (FME), Ireland

Fujitsu Mikroelektronik GmbH (FMG) was established in June 1980 in Frankfurt, West Germany, as Fujitsu's European headquarters and is a totally owned subsidiary of Fujitsu Limited, Tokyo. Fujitsu Microelectronics Limited (FML) is a sister company based in Maidenhead, England and dedicated to serving the U.K., Ireland, and Scandanavia. Fujitsu Microelectronics Italia (FMIL) is based in Milan, Italy and serves Italy, Spain, Portugal, and the rest of Southern Europe. Together, FMG, FML, and FMIL supply the European market with a full range of semiconductors and electronic components. Sales offices are located in Munich, Frankfurt, Stuttgart, Paris, Eindhoven, Milan, Maidenhead, and Stockholm.

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in Dublin, Ireland, as Fujitsu's European Assembly Center for integrated circuits. FME produces DRAMs, EPROMs, and other LSI memory products.

Fujitsu has two European VLSI design centers, both in the U.K. The Manchester Design Center, in operation since 1983, is equipped with two mainframe computers and is linked by satellite to production plants in Japan and the U.S. Staffed with a team of experienced engineers, the center is involved in the design of VLSI standard products, SuperMacros, CAD tools and ASICs. A second design center was set up in London in 1990 for designing telecommunication ICs. Additionally, Fujitsu offers a network of 17 ASIC design centers in eight European countries.

Fujitsu has further demonstrated its commitment to the European market by commencing construction of a full wafer fabrication plant in Durham in the North of England. The new plant is due to start production of 4 megabyte DRAMs and ASICs in 1991.

Introduction to Fujitsu

The range of semiconductor products offered by FMG, FML, and FMIL for the European market includes:

Memory Products	DRAMs SRAMs EPROMs EEPROMs Mask ROMs Bipolar PROMs Video RAMs ECL RAMs Memory modules Memory cards
ASIC Products	CMOS gate arrays BiCMOS gate arrays Bipolar (ECL) gate arrays Gallium Arsenide gate arrays CMOS standard cells ECL gate masterslice devices Wide range of ASIC design software
Microprocessor Products	4-Bit Microcontrollers 4- 8- and 16-bit F^2MC flexible Microcontrollers 32-Bit SPARC™ RISC microprocessors 32-Bit GMICRO™ TRON-based CISC microprocessors
Telecommunication Products	Prescalers PLLs CODECs LAN devices DSPs SCSI and LAN devices ISDN products Telecom devices for the GSM Pan-European digital cellular telephone system.
Analog Products	OP Amps Comparators A/D and D/A Converters Application Specific ICs

The range of electronic components offered by FMG, FML, and FMIL incudes relays, connectors, keyboards, thermal printers, plasma displays, liquid crystal displays, hybrid ICs, and piezoelectric devices.

Introduction to Fujitsu

Fujitsu Microelectronics Asia PTE Ltd. (Singapore)

Fujitsu Microelectronics Asia PTE Ltd. (FMAP) opened in August 1986, in Hong Kong, as a wholly-owned Fujitsu subsidiary for sales of electronic devices to the Asian, Australian, and Southwest Pacific markets. In 1990, FMAP moved to a new location in Singapore.

FMAP offers memory, ASIC, microprocessor, and telecommunication products along with Fujitsu's wide range of electronic components.

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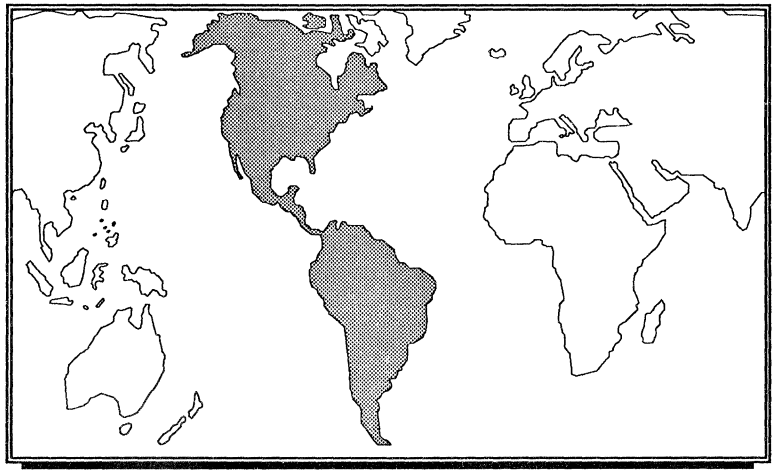

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For product information, contact your nearest Fujitsu representative.

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Reptron Electronics
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Lenexa, KS
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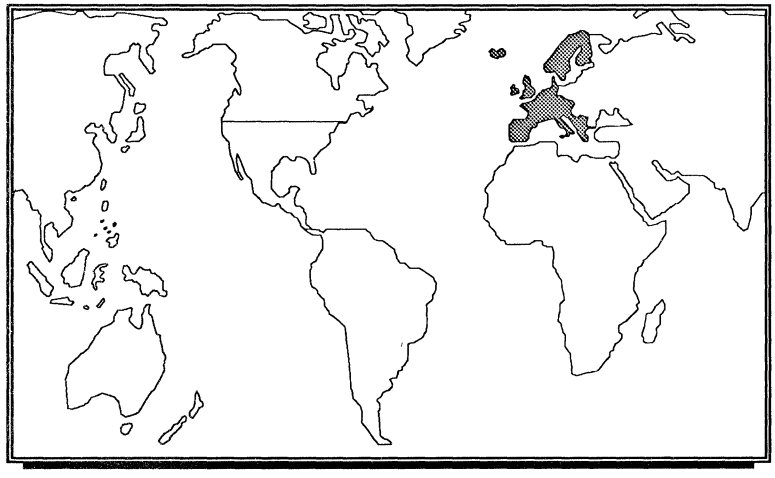

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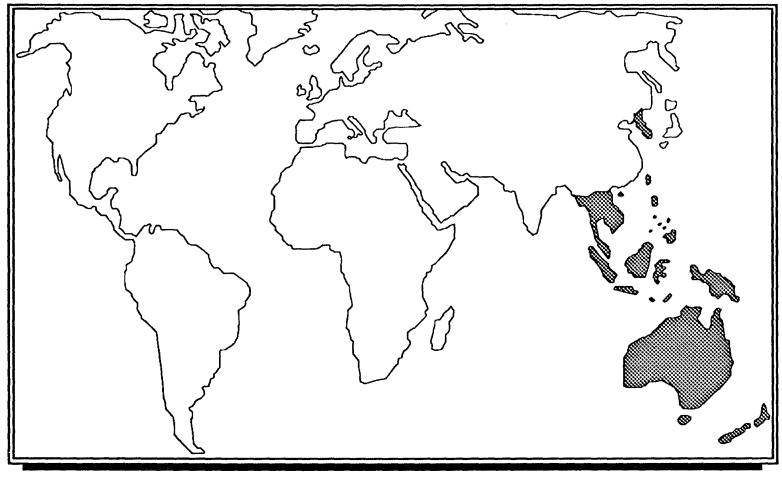

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Section 12

Telecommunication Products Design Information — *At a Glance*

Page	Title
12–3	Application Note. Prescalers and PLLs: *Fujitsu Prescalers and Phase-Locked Loops for VHF and UHF Frequency Synthesis.* A Tutorial with Selection Guides

12

12

March 1991

FUJITSU

APPLICATION NOTE

Prescalers and PLLs

Fujitsu Prescalers and Phase-Locked Loops for VHF and UHF Frequency Synthesis

A Tutorial with Selection Guides

Fujitsu Microelectronics, Inc.
Field Applications Engineering

Abstract

This Application Note includes a broad introduction to the relevant high frequency synthesis theory and its application areas, a description of prescaler and phase-locked loop (PLL) components, and guidelines for selecting and designing with Fujitsu's extensive selection of prescaler and PLL IC products.

12

Contents

Introduction 13–9

PLL Tuning Systems 13–9

What is a PLL? 13–11

Frequency Synthesis With PLLs and Prescalers 13–12

The Pulse Swallow Method 13–13

Stand-alone PLLs and Integrated PLLs 13–14

Selecting the Right PLL IC 13–16

Selecting a PLL 13–17

- Width of the counters 13–17
- Selecting the N and A counters 13–18
- PLL Counter Selection Guide 13–18

A Practical Example: Selecting the PLL IC for an FM Receiver 13–18

- Example 13–18
- Programming of the counters 13–19
- Set-up and switching times of the counters and modulus control logic 13–19
- Positive or negative edge triggering of counters 13–19
- Phase detector 13–20
- Charge pump 13–20
- Charge pump waveforms and fr and fv 13–21

4-bit Microcontrollers with PLLs 13–22

What is a Prescaler? 13–22

- Dual modulus prescalers 13–23
- Single modulus prescalers 13–23
- Microwave Prescalers 13–24

Stand-alone Prescaler Application 13–24

Selecting the Right Prescaler 13–25

- Toggling speed 13–25
- Termination resistor internal/external 13–26
- Stability of Vout 13–26
- Flexibility of the input voltage 13–27
- ECL level 13–27
- Flexibility of Vcc 13–27

Contents (Continued)

Modulus set-up time 13–27
Input impedance and reactance 13–27
Smith chart 13–27
Packaging 13–28
Signal propagation delay through the prescaler 13–30
Balanced inputs 13–30
Output duty cycles 13–30
Power dissipation 13–30
Conclusion 13–31
References 13–32
Books 13–32
Articles 13–32

Illustrations

Figures **Page**

1. A Typical Heterodyne FM Receiver Tuned to the 88.1 MHz Signal 3–10
2. A Typical Heterodyne (Audio) Sender 3–11
3. A Basic PLL Configuration 3–11
4. Frequency Synthesis with a Programmable Counter 3–12
5. Prescaler Accommodating for a Slow Program Counter 3–12
6. Pulse Swallow 3–13
7. System Blocks 3–14
8. Fujitsu's Integrated PLL ICs 3–14
9. Varactor Diode in a VCO or a VCXO 3–15
10. A Varactor Diode Acting as a Voltage-controlled Variable Capacitance 3–16
11. PLL Program Counter Triggered by Opposite Edge 3–19
12. PLL Program Counter Triggered by Same Edge 3–20
13. Active Low Pass Filter 3–21
14. External Charge Pump Example 3–21
15. Frequency Division 3–22
16. Selection Guide to the Fujitsu Bipolar Prescaler Family 3–24
17. A Stand-alone Application of a Prescaler: Clock Rate Reduction 3–24
18. Input Signal Amplitude Versus Input Frequency for MB509 Dual Modulus Prescaler ... 3–26
19. Smith Chart Constant Resistance 3–28
20. Smith Chart Constant Reactance 3–28
21. Input Impedance of Fujitsu's MB501L Dual Modulus Prescaler as a Function of Frequency Shown on a Smith Chart 3–29

Tables **Page**

1. Fujitsu's Low Power CMOS PLLs 3–16
2. Fujitsu's Super PLLs 3–17
3. Fujitsu Prescalers 3–31

Introduction

Phase-locked loops (PLLs) and prescalers are used for synthesizing and controlling frequencies in a multitude of high frequency systems. These systems range from radio and television broadcasting, cellular phones, computer local area networks (LANs), and measurement instrumentation to satellite and microwave systems.

Dedicated PLL integrated circuits (ICs) are manufactured in CMOS technology and typically operate in the 20-30 MHz range (maximum). Prescalers manufactured in bipolar ECL or GaAs technologies are considered interface ICs that allow the relatively slower PLLs to accurately control and select frequencies well into the microwave range (>1 GHz).

Fujitsu manufactures a broad range of high frequency telecommunication ICs that includes prescalers, PLLs, integrated PLLs, as well as microcontrollers with onboard PLL and prescaler circuits.

PLL Tuning Systems

Tuning of telecommunication senders and receivers is, by far, the largest application area for today's PLLs and prescalers. High frequency PLLs have largely replaced older methods such as direct tuning an RC or LC oscillator to the desired local oscillator frequency.

At the expense of a quantized (instead of a continuous frequency) resolution, PLLs and the so-called digital tuning circuits into which they are incorporated provide a cheaper, faster, more compact and reliable solution to tuning circuitry. The fact that PLLs only allow selection of frequencies in discrete steps, rather than over a continuous range, is not a concern because the available frequencies (for airwaves, long distance telephone cables, satellites, microwave links, ISDN etc.) are heavily regulated and limited to preassigned channel frequencies.

The frequency position and spacing between channels depends on the physical carrier medium and the program material involved. For example, U.S. airwaves regulations of the Federal Communications Commission (FCC) specify that:

AM radio must be broadcast at 530, 540, 550 to 1610, or 1620 kHz

FM radio must be broadcast at 87.9, 88.1 to 107.7, 107.9 MHz

TV (channels 2–69) must be broadcast at 55.25, 61.25, 67.25, 77.25, 83.25 to 795.25, 801.25 MHz.

These frequencies represent the center frequencies of each channel. The spacing of 10 KHz between assigned AM channels, 200 kHz between assigned FM channels, and 6 MHz between assigned TV channels reflects the progressively higher bandwidths necessary for FM and TV.

Other regulated frequencies worth mentioning within the VHF (30 - 300 MHz) and UHF (300 MHz – 3 GHz) bands include: 46/49 MHz for cordless telephones, 800-900 MHz for cellular phones (also known as land mobile radio services), 0.1-1.5 GHz for cable TV and >2 GHz for emerging Digital TV standards and Integrated Services Digital Network (ISDN). Fujitsu prescalers and PLL ICs are appropriate for most of these applications.

Figure 1 shows a superheterodyne FM broadcast receiver and some of the involved spectra and frequencies. For an example, let us examine the steps involved in tuning to the FM station at 88.1 MHz.

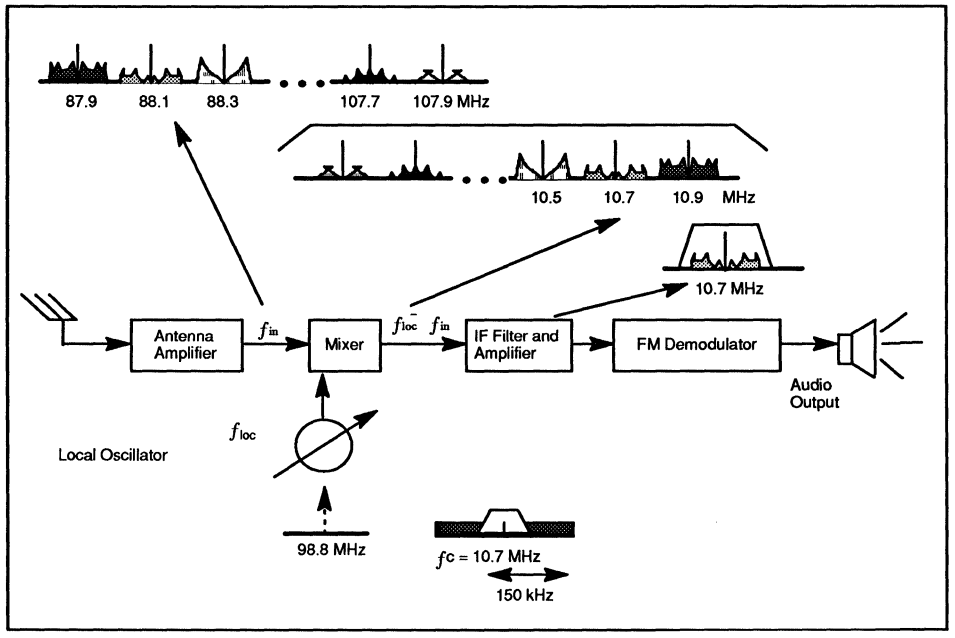

Figure 1. A Typical Heterodyne FM Receiver Tuned to the 88.1 MHz Signal

The antenna is exposed to a multitude of transmission frequencies. In order to retrieve the desired signal, several stages of amplification and progressive selective filtration must be applied. In FM broadcasting each radio station is allowed to use up to 150 kHz around the assigned center frequency. Since the spacing between the assigned channels is 200 kHz, this leaves a 50-kHz wide isolation gap between the stations to avoid a spectral overlap. Thus, a 150-kHz wide filter can be used in the final stage to isolate the desired station from all the others. Accurate tuning of such a narrow filter over the 20-MHz wide FM frequency range is not an easy task. To achieve accurate tuning, the filter is kept at a constant frequency, the so-called Intermediate Frequency (IF), and the desired radio signal is shifted in frequency to fall exactly within the filter passband. 10.7 MHz is the broadly used value for IF in commercial FM tuners.

The antenna signal is converted to a lower frequency by mixing (or heterodyning) with an appropriately chosen local oscillator frequency f_{loc}. A PLL is employed for synthesizing f_{loc}. In order to place the desired radio station (originally located at f_{in}) exactly at the center of the IF bandpass filter, the PLL frequency f_{loc} must be set so that IF = $f_{loc} - f_{in}$. In other words, to tune to the 88.1 MHz signal, a f_{loc} of 88.1+10.7 MHz = 98.8 MHz is necessary. Tuning to another signal is accomplished by selecting a different f_{loc}.

An appropriate FM demodulator working at the IF provides the final restoration of the original signal.

On the sender side (see Figure 2) the sequence is reversed: a modulated IF signal is mixed with the local frequency oscillator up to the appropriate channel-frequency and broadcast.

12

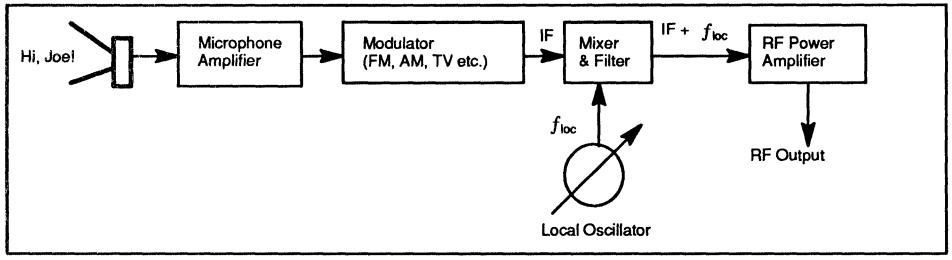

Figure 2. A Typical Heterodyne (Audio) Sender

Near-ideal PSK, PM, or FM demodulators can be implemented with PLLs as well as local oscillators.

What is a PLL?

A PLL is a control loop consisting of a phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO), program counter(s), and, as necessary, single- or dual-modulus prescalers. (See Figure 3.)

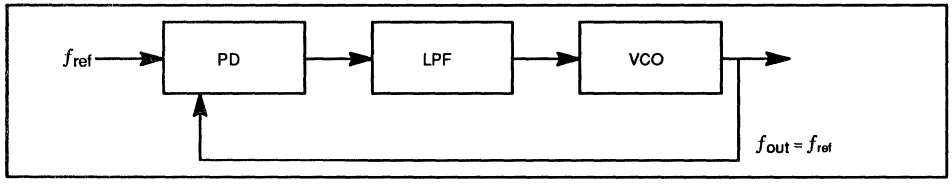

Figure 3. A Basic PLL Configuration

The output of the PD is a voltage indicating the phase difference between its two inputs.

The LPF smooths the PD output and determines the dynamic performance of the loop. The dynamic performance includes general servo loop issues, such as the capture and lock ranges, the noise suppression bandwidth and the transient response.

When the loop is out of lock, the PD voltage changes the frequency of the VCO in a direction that reduces the phase difference between the input signal and the local oscillator signal. When the loop is locked, the signals at both inputs are in phase and have the same frequency.

Generally speaking, the output of the VCO is considered the desired PLL output. It should be mentioned, however, that in some instances (such as when a PLL is used as an FM de-modulator), the filtered output of the PD, rather than the output of the VCO, can be viewed as the system output.

The bandwidth of the low-pass loop filter is crucial to the dynamic- and noise-filtering performance of the loop. The two performance requirements are conflicting, since faster lock-up times require wider LP filters while better noise characteristics are achieved with narrower filters. Therefore, a reasonable compromise has to be met for each application.

Narrow filter bandwidths provide long-loop averaging times and are useful in applications where a noisy, intermittent, or varying reference source must be cleaned up.

For example, in digital LANs, a PLL is used to regenerate a local clock rate from frame synchronization bits, which appear intermittently on most asynchronous communications networks.

In a similar way, the "flywheel synchronizers" for vertical and horizontal scan in today's TV receivers, are operated using PLL circuits. In both cases the "slow" lowpass filter maintains a relatively constant VCO frequency between occurrences of synchronization patterns on the input.

In frequency synthesis applications, the reference frequency source will typically be a high quality, relatively noise-free, crystal oscillator. The loop filter can be extensively wide to provide for fast switching times without compromising noise performance.

A novel approach to PLL design is to electronically bypass the loop filter during the bulk of a frequency switching period and then to activate it back into the loop for final lock-in.

As previously mentioned, the loop filter is the single most important factor in determining the dynamic performance of the servo loop. A thorough theoretical treatment of servo loop analysis is beyond the scope of this publication. References 1 through 4 listed in the back of this note are recommended for more in-depth information.

Frequency Synthesis With PLLs and Prescalers

Figure 4 shows a simple frequency-synthesizing configuration employing a PLL and a single program counter.

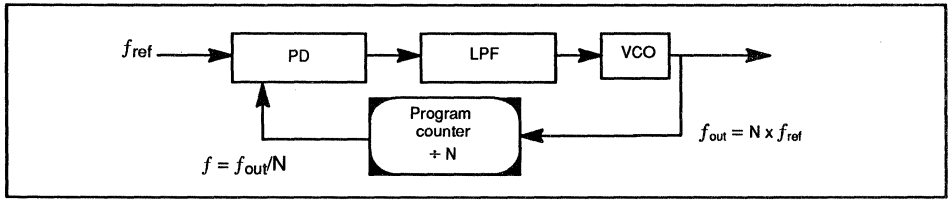

Figure 4. Frequency Synthesis with a Programmable Counter

When the loop is in lock, the two input frequencies of the PD are equal, hence:

$$f_{ref} = f_o/N <=> f_o = N \bullet f_{ref}$$

A reprogramming of "*N*" by +1 or –1 will result in selection of a new output frequency with channel separation of f_{ref}.

The scheme of Figure 4, although attractive in its simplicity, is only applicable to output frequencies below 40 MHz, since higher VCO frequencies will exceed the program counter's toggling rate.

Figure 5 shows a widely used remedy to the high frequency problem: a *1/M* prescaler is inserted in the feedback loop as a buffer between the VCO and the program counter. This lowers the program counter's input frequency to f_{out}/M instead of f_{out}.

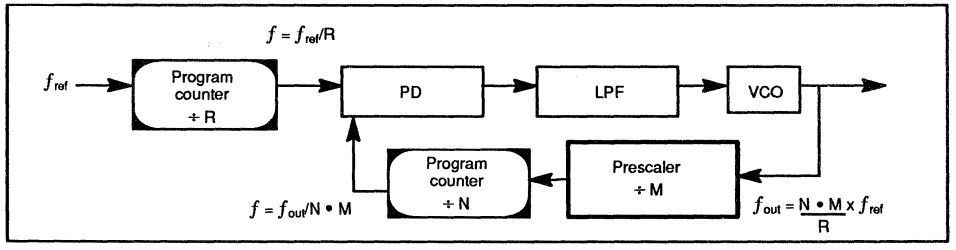

Figure 5. Prescaler Accommodating for a Slow Program Counter

Figure 5 also shows a reference frequency divider, 1/R, inserted in the reference frequency path to allow more flexibility in output frequency programming. Without the reference frequency divider, the presence

of the prescaler would result in broadening the channel separation to $M \bullet f_{ref}$. A resolution of f_{ref} is maintained by setting R equal to M.

In many cases, the scheme of Figure 5 is a satisfactory solution, with one drawback. Compared to Figure 4, the operational frequency of the phase detector is lowered by the prescaling factor M. A lowered PD frequency necessitates use of a narrower low-pass filter to suppress spurious output signals from the phase detector at the comparison frequency and its harmonics. Especially in very high frequency synthesizers, where the divide ratio of the prescaler becomes substantial, the loop's lock-in and switching speed characteristics will be severely degraded as a result of narrowing the lowpass filter.

The Pulse Swallow Method

The widely used "multi-modulus division", also known as pulse swallowing (see Figure 6), offers a solution to previously mentioned problems. This method employs two programmable counters and a dual modulus prescaler inside the loop. (For simplicity the reference frequency divider is not shown.)

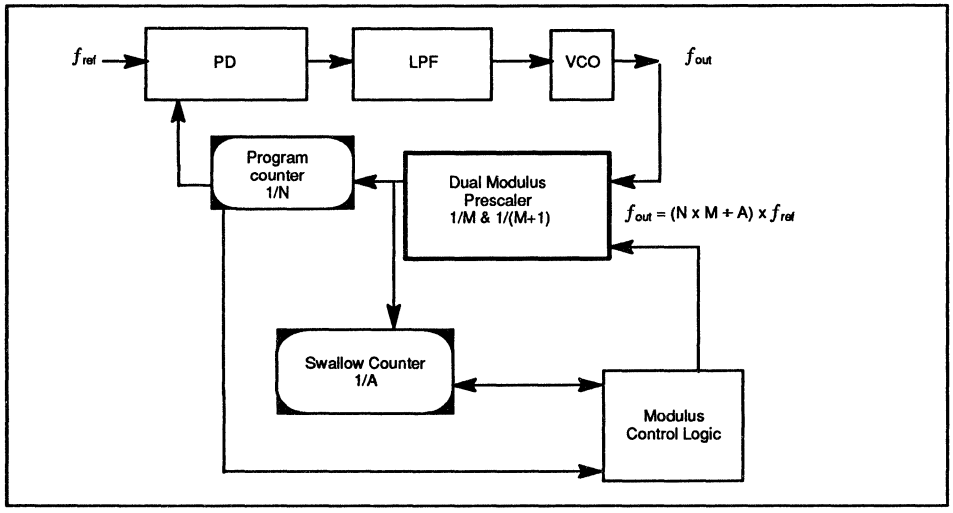

Figure 6. Pulse Swallow

A description of the pulse swallow method is as follows:

N must be larger than A ($N>A$). The dual modulus prescaler is initially set to divide by $M+1$. After "A" pulses out of the prescaler, the swallow counter is full and changes the prescaler modulus to M. After additional (N-A) pulses out of the prescaler, the program counter changes the prescaler modulus back to $M+1$, restarts the swallow counter and the cycle repeats.

In this way each cycle of the $1/N$ counter is a result of:

$$A \bullet (M+1) + (N-A) \bullet M = N \bullet M+A$$

cycles of the f_{pit}.

In other words:

$$f_{out} = (N \bullet M + A) \bullet f_{ref}$$

12

Since *M* is multiplied by *N*, but not *A*, the frequency will change by f_{ref} when *A* is changed by 1. In this way both the channel separation and the PD frequencies are maintained at f_{ref} to provide for an uncompromised loop performance.

As previously mentioned, more complex variations of the multi-modulus theme include: *N*/*N*+*Z* prescalers (as in MB508 with 128/130, 256/258 and 512/514) and quad-modulus schemes involving multiple swallow counters and special prescalers.

Stand-alone PLLs and Integrated PLLs

Figure 7 shows a general purpose high frequency synthesizer and the functional blocks. These blocks are: the PD, the reference counter, the A and the N counters and modulus control logic. The MB87014, manufactured entirely in CMOS, includes an onboard 180 MHz prescaler.

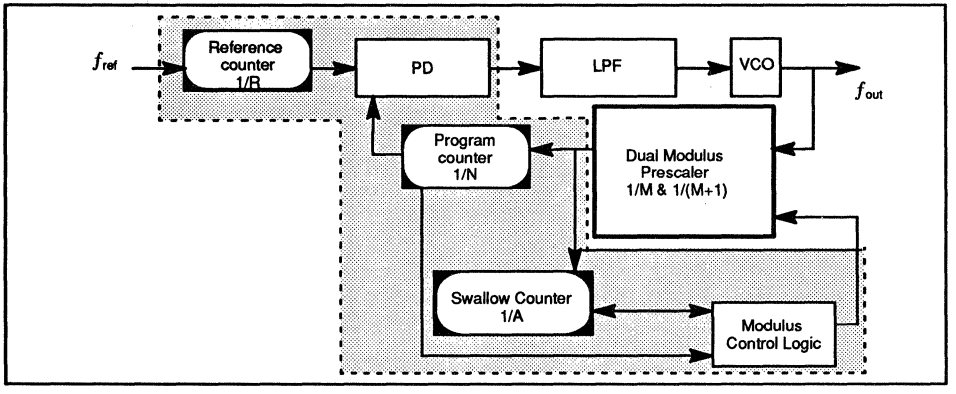

Figure 7. System Blocks

Advances in recent years in CMOS and BiCMOS (combined ECL and CMOS on one chip) have allowed integration of gigahertz prescalers on the same chip as the PLL. The architecture of these integrated PLL BiCMOS devices is illustrated in Figure 8.

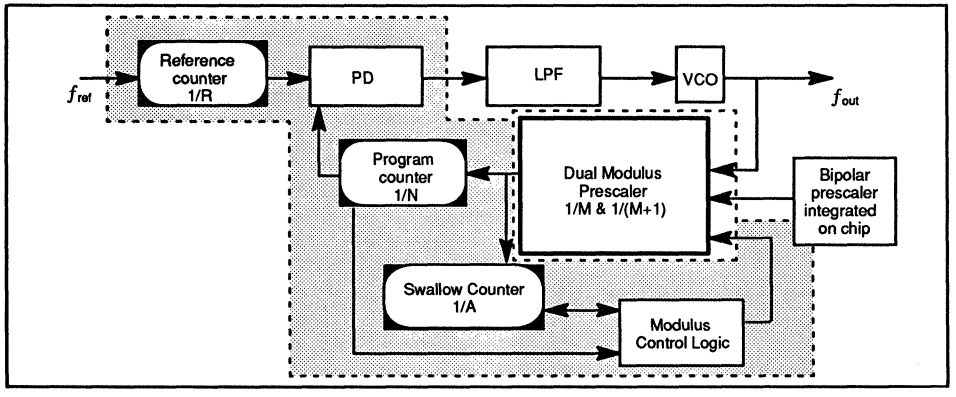

Figure 8. Fujitsu's Integrated PLL ICs

Before discussing the blocks on the PLL chip, let us briefly mention the circuits not found on it. As stated earlier, the low-pass filter must yield a good compromise between accommodating the desired noise and switching characteristics on one side and removing spurious components from the phase detector output on the other side. A charge pump output (see Figure 14) from the PLL is provided in most cases, allowing direct connection of an external passive RC filter. The charge pump output is simply a very high impedance output ($Z_{out} \geq 400k\ \Omega$) well suited to drive high-Q resonant circuits found in the VCO. Optionally, an unbuffered PD output is often also made available for connection of custom external active filter configurations. Typical filter bandwidths for frequency synthesis are 1-10 kHz.

The prescaler and the VCO are the only two devices actually operating at the high output frequency f_{out}.

The VCO is frequently custom made for a specific application. Some popular oscillator types, in order of decreasing phase and frequency-stability, but increasing frequency coverage and linearity, are as follows:

- PLL IC with an on-chip inverter/buffer for an external reference frequency oscillator
- Voltage controlled crystal oscillator with varactor diode (also known as VCXO)
- LC oscillator with a varactor diode
- RC multivibrator

A list of crystal oscillator and VCXO manufacturers can be found in reference 11.

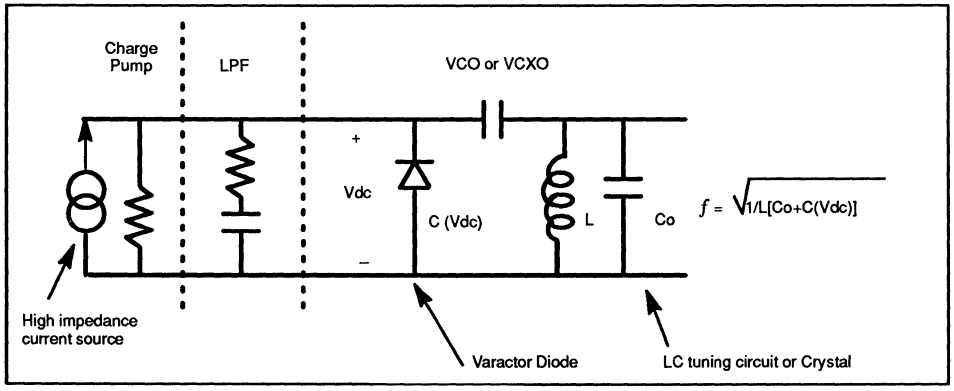

Figure 9. Varactor Diode in a VCO or a VCXO

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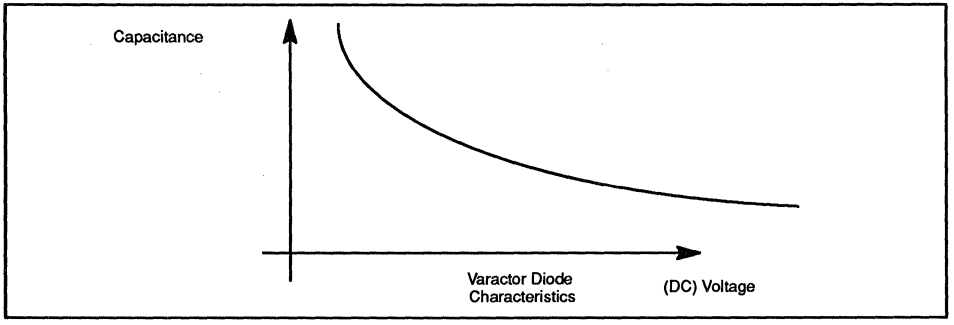

Figure 10. A Varactor Diode Acting as a Voltage-controlled Variable Capacitance

Selecting the Right PLL IC

Table 1 lists Fujitsu's family of CMOS PLL ICs and Table 2 lists the BiCMOS integrated PLL ICs.

Table 1. Fujitsu's Low Power CMOS PLLs

P/N	Max Frequency (3 V/5 V)	Divide Ratio N[1]	A[2]	Prescaler	R[3]	Super Voltage	I_{DD} (Typ.) 3 V/5 V	Package
MB87001A	10/13 MHz	5-1023	0-127	—	8-ldnd[4]	2.7-5.5 V	2.0/3.0 mA	16 Pin DIP/FPT
MB87006A	10/17 MHz	5-1023	0-127	—	5-16383	3.0-6.0 V	2.5/3.5 mA	16 Pin DIP/FPT
MB87014A	–/180 MHz	5-1023	0-63	64/65	5-65535	4.5-5.5 V	–/8.0 mA	16 Pin DIP/FPT
MB87073	10/13 MHz	5-2047	0-127	—	8-ldnd	2.7-5.5 V	2.0/3.0 mA	16 Pin DIP/FPT
MB87076	10/15 MHz	5-2047	0-127	—	8-16383	3.0-6.0 V	2.5/3.0 mA	16 Pin DIP/FPT
MB87086A	–/95 MHz	5-1023	—	—	5-65535	4.5-5.5 V	–/8.0 mA	16 Pin DIP/FPT
MB87087	10/13 MHz	5-1023	0-127	—	5-16383	3.0-6.0 V	2.5/3.5 mA	16 Pin DIP/FPT
MB87090	10/13 MHz	5-1023	0-127	—	8-ldnd	2.7-5.5 V	3.0/4.0 mA	16 Pin DIP/FPT

Notes: [1]N = Program counter divide factor.
[2]A = Swallow counter divide factor.
[3]R = Programmable reference counter.
[4]ldnd = 8 programmable combinations of 1/8, 1/16, 1/64, 1/128, 1/512, 1/1024, and 1/2048.

12

Table 2. Fujitsu's Super PLLs

P/N	Prescaler			Program Counter Divide Ratio	Swallow Counter Divide Ratio	Reference Counter Divide Ratio	I_{CC} (TYP)	Sypply Voltage	Package
	F_{IN} (MAX)	V_{IN} (MIN)	Divide Ratio						
MB1501	1100 MHz	200 mVp-p	64/65 128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	15 mA	2.7-5.5 V	16-Pin SOP
MB1502	1100 MHz	200 mVp-p	64/65 128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	8 mA	5 v ± 10%	16- Pin SOP
MB1503	1100 MHz	100 mVp-p	128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	8 mA	4.5-5.5 V	16-Pin SOP
MB1504	520 MHz	200 mVp-p	32/33 64/65	Binary 16-2047	Binary 0-127	Binary 8-16383	10 mA	2.7-5.5 V	16-Pin SOP
MB1505	600 MHz	200 mVp-p	32/33 64/65	Binary 16-2047	Binary 0-127	Binary 8-16383	6 mA	5 v ± 10%	16-Pin SOP
MB1507	2000 MHz	400 mVp-p	128/129 256/257	Binary 16-2047	Binary 0-255	Binary 8-16383	18 mA	5 v ± 10%	16-Pin SOP
MB1508	2400 MHz	200 mVp-p	64/128 256	Binary 16-2047	—	Binary 256, 512 1024, 2048	14 mA	5 v ± 10%	20-Pin SOP
MB1509*	400 MHz	200 mVp-p	32/33	Binary 16-2047	Binary 0-127	512 1024	12 mA	2.7-5.5 V	20-Pin SOP
MB1511	1100 MHz	200 mVp-p	64/65 128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	8 mA	2.7-5.5 V	20-Pin SSOP
MB1512	1100 MHz	100 mVp-p	64/65 128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	8 mA	4.5-5.5 V	20-Pin SSOP
MB1513	1100 MHz	100 mVp-p	128/129	Binary 16-2047	Binary 0-127	Binary 8-16383	8 mA	4.5-5.5 V	20-Pin SSOP
MB1518	2500 MHz	100 to 200 mVp-p	512/528	Binary 32-511	Binary 0-31	512	16 mA	4.5-5.5 V	16-Pin SSOP
MB1519*	600 MHz	200 mVp-p	128/129	Binary 16-2047	Binary 0-127	512, 1024	16.5 mA	2.7-5.5 V	20-Pin SOP

*Dual Device

Selecting a PLL

The specifications to consider when selecting a PLL are as follows:

Width of the counters

The most significant feature of the various PLL devices (since operating speed is practically the same for all), is the width of their counters. In general, the width (in bits) of the reference counter determines the frequency resolution ($\Delta f_{channel} = f_{ref}/R$) obtainable from the system. The width of the programmable counter, ($1/N$) (see Figure 7) and the swallow counter ($1/A$) determine the number of channels that can be covered. Fujitsu devices are available with up to 18-bit wide combined program and swallow counters, and 16-bit wide reference counters.

Selecting the N and A counters

It is easily observed from the dual-modulus equation [$f_{out} = (N \bullet M+A) \bullet \Delta f_{channel}$] that A need not assume values higher than the prescaler modulus M, since setting A equal to $M+X$ is equivalent to setting A equal to X and increasing N by 1. Hence, all possible channels can be covered in a dual modulus configuration if the programmable swallow counter number (A) is allowed to assume all values from 0 to $M-1$, where M is the modulus of the $M/M+1$ prescaler:

$$\bullet\ 0 \leq A \leq M-1$$

Under all circumstances the condition N≥A must be satisfied:

$$\bullet\ N_{min} = A_{max} = M-1.$$

To select the right PLL counters for your application, supply the information that is requested in the following guide.

PLL Counter Selection Guide

1. Identify maximum and minimum output frequency desired, $f_{out,\,max}$ and $f_{out,\,min}$.
2. Select a $M/M+1$ prescaler, so that $f_{out,\,max}/M$ can be accommodated by the PLL (<20 MHz typically).
3. Identify desired channel spacing(s), $\Delta f_{channel}$.
4. Let $A = 0$, then $N_{min} = f_{out,\,min}/\Delta f_{channel}$ and $N_{max} = f_{out,\,max}/\Delta f_{channel}$.
5. Verify that $N_{min} \geq M-1$; if not, select a bigger prescaling modulus and go back to step 3.
6. Select an N program counter with enough bit-width to accommodate the value of N_{max}.
7. Select an A swallow counter with enough bit-width to accommodate the value $M-1$; set all higher bits to 0.
8. Select the reference frequency divider (R) and a crystal reference frequency so that $f_{ref}/R = \Delta f_{channel}$.

A Practical Example: Selecting the PLL IC for an FM Receiver

We are going to select the appropriate PLL IC and prescaler for the local oscillator of the superheterodyne FM receiver shown earlier in Figure 1. In order to receive an FM station at f_{in}, the local oscillator must be set to $f_{loc} = f_{in}$ + 10.7 MHz. For receiving all FM stations, f_{loc} has to be selectable between 98.6 MHz and 118.6 MHz in 0.2 MHz steps; that is 101 positions in total.

To select a PLL for our example FM Receiver, we used the PLL Selection Guide, supplied the required information (see Example), and selected the appropriate PLL.

Example

1. $f_{out,\,max}$ = 118.6 MHz f_{out} = 98.6 MHz
2. Choose the MB503 prescaler ($M=16$)
   $f_{out,\,max}/M$ = 7.4 MHz < 20 MHz
3. $\Delta f_{channel}$ = 0.2 MHz
4. $N_{min} = f_{out,min}/\Delta f_{channel}$ = 493
   $N_{max} = f_{out,max}/\Delta f_{channel}$ = 593
5. N_{max} > 16, OK
6. N_{max} of 593 requires a 10-bit wide N-counter

- A 4-bit wide (swallow) counter
- Either an MB87001A or an MB87006A
- Choose MB87001A

8. Choose an f_{ref} of 3.2 MHz and set the R-counter to 16 to yield $\Delta f_{channel}$ = 0.2 MHz

Programming of the counters

In order to preserve board space, all Fujitsu PLLs have serially programmable counters. The divisor values are fed through a serial pin to a shift register and latched-in with a control pulse. This allows 16-pin packaging to be used for all devices.

Set-up and switching times of the counters and modulus control logic

These delays are important and can become a limiting factor, especially when operating in pulse swallow mode. When the circuit has counted down so that the N program counter is full, the whole counter system is reset. The reset function must be completed within the next cycle of the *M/M+1* prescaler or,

$$t_{reset} < M/f_{out,max}$$

Where t_{reset} equals the sum of propagation delays through the *A* and *N* counters, (the required modulus set-up time of the prescaler and release time of the modulus control logic).

Positive or negative edge triggering of counters

As previously mentioned, when the modulus of a dual-modulus prescaler is changed from 64 to 65, one half-cycle of the output (output low) will be extended to 33 input cycles. The other half-cycle will remain unchanged at 32 input cycles.

Therefore, modulus set-up time of the prescaler will be expressed relative to an edge of the affected half-cycle (in this case the negative-going edge). If the program counters and the modulus control logic are triggered on an opposite edge, valuable set-up time margin will be lost. (See Figures 11 and 12).

When necessary, insertion of a fast inverter between the prescaler and the program counter may provide some timing relief.

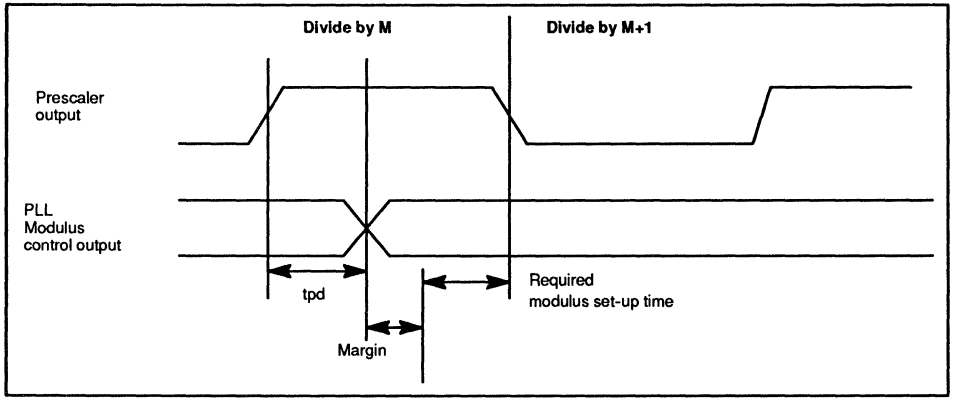

Figure 11. PLL Program Counter Triggered by Opposite Edge

12

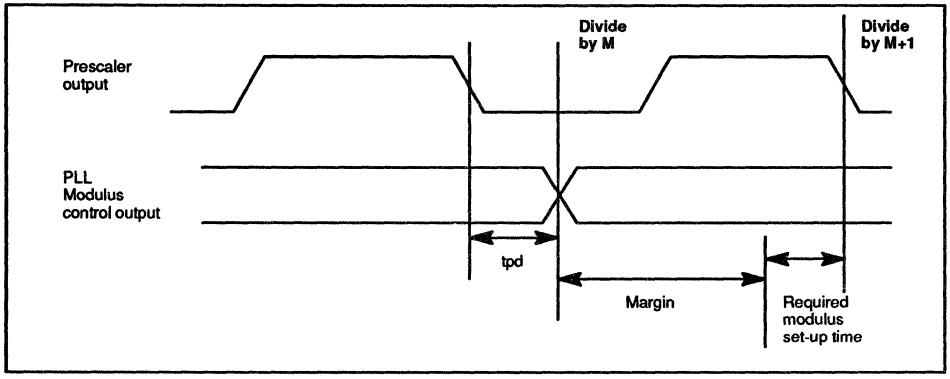

Figure 12. PLL Program Counter Triggered by Same Edge

Phase detector

There are some differences between analog and digital phase detectors.

An analog phase detector works on a so-called integrating multiplier principle (Gilbert Cell multiplier is one example) and reflects not only timing differences, but also (if the signals are not purely sinusoidal or square) differences in the shape of the input signals. Analog phase detectors can offer superior signal-to-noise (S/N) ratios and can react almost instantaneously to minute changes in input waveforms. However, they are relatively complex and lend themselves poorly to high speed CMOS integration.

The digital phase-frequency detector is a simple and extremely fast sequential circuit (4 flip-flops). The circuit detects only positive-going threshold crossings and indicates which of the two inputs is ahead of the other one. It is not dependent on the shape of the signals. The digital phase-frequency detector is in all Fujitsu PLLs.

Charge pump

The single-ended output from the phase detector is called the internal charge pump. The three-state charge pump output goes high when $f_{ref} > f_{vco}$, low when $f_{ref} < f_{vco}$ and high-impedance state when $f_{ref} = f_{vco}$. This output can be connected directly to an active or passive external filter. The MB87014 provides an inverted charge pump output as well.

The charge pump output is derived from two flip-flops out of the phase detector, ϕr and ϕv. In the case of MB87006A, MB87014 and the MB87086[1] when the loop is unlocked, the appropriate output terminal, ϕr or ϕv, pulls low to indicate which of the two inputs f_{ref} or f_{vco} is at a higher frequency.

The signals ϕr and ϕv would normally be considered an intermediate result; however, they are also made accessible on two output terminals allowing construction of an external charge pump.

A charge pump combines the two digital outputs (ϕr and ϕv) into one output. (See Figure 13.) The external configuration shown here also directly implements the lowpass filter. Note that due to different polarity assignments, this configuration is not appropriate for MB87001A, 87073, 87076, and the integrated PLLs. Also note that often a large resistor is inserted following the op-amp output to increase the output impedance.

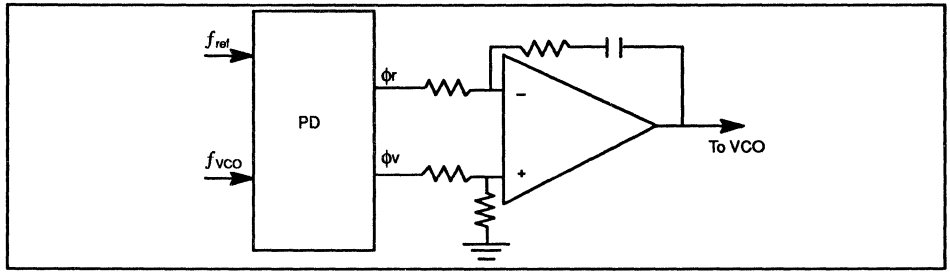

Figure 13. Active Low Pass Filter

A fast external charge pump implementation appropriate for the MB87001A, 87073, 87076 PLLs, ICs, and an integrated PLL is shown in Figure 14. The φr and φv outputs on these devices are of the open-drain type. (The rest of the PLL family provides push-pull outputs for φr and φv.)

[1]Note that the remaining Fujitsu PLL ICs (MB87001A, 87073, and 87076), as well as the single-chip PLL/Prescaler family (MB1500), have a different phase detector design and a different truth table for φr and φv:

	φr	φv
$f_r > f_v$:	Low	Low
$f_r = f_v$:	Low	High-Impedance
$f_r < f_v$:	High	High-Impedance

The φ-outputs of these devices are open drain.
An external charge pump allows use of faster transistors or op-amps (higher slew rates) and may offer improvement in lock-in performance.

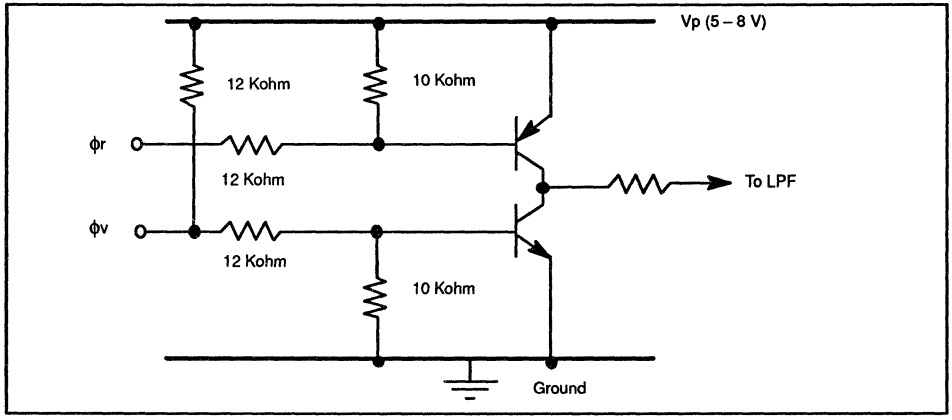

Figure 14. External Charge Pump Example

Charge pump waveforms and φr and φv

As previously mentioned, in the case of MB87006A, 87014 and 87086 (see footnote[1] on the preceeding page), when the loop is unlocked, the appropriate output terminal, φr or φv, pulls low to indicate which of the two inputs f_{ref} or f_{vco} is at a higher frequency. This active terminal, φr or φv, will not stay at a steady low but will occasionally toggle to a high state. Basically, its output provides a pulse-width modulated representation of the frequency difference between the inputs.

12

When the loop is in lock, ϕr and ϕv will both be in the "high" state. However, synchronously with the phase comparison frequency, a short spurious negative pulse will occur at both outputs.

The same pulse anomalies will also appear on the output from the internal charge pump. One of the tasks of the loop lowpass filter is to remove all spurious signals (pulses) from the PD output. The loop filter bandwidth must, therefore, always be below the phase comparison frequency. Conversely the phase comparison frequency should be kept as high as possible.

4-bit Microcontrollers with PLLs

Fujitsu also offers a family of 4-bit microcontrollers, the MB88560 family with an on-chip PLL.The MB88560 family consists of two 4-bit CMOS microcomputers: the MB88561 with a liquid crystal display (LCD) controller/driver and the MB88562 with a vacuum fluorescent display (VFD) driver. Both devices contain 21 I/O lines, an 8-bit timer/counter, an A/D converter with 6-bit resolution, display drivers, and a PLL with prescalers suitable for all broadcast and shortwave frequencies. Each device has independent AM (up to 32 MHz) and FM (up to 120 MHz) inputs. Up to 4 K by 8-bit ROM space and 256 K by 4-bit static RAM space is available on-chip.

Both chips allow extremely compact designs of car radios, personal stereos, personal communication equipment, etc.

A two-part MB88560 design guide and a demo board are both available from Fujitsu.

What is a Prescaler?

A prescaler is an integrated circuit that divides the frequency of an incoming signal by an integer M (see Figure15). The divisor, *M*, is called the Modulus.

Internally, a prescaler is a specialized ripple counter, which counts incoming pulses and performs one output cycle for every *M* received input cycle. If *M* is an even number the output is toggled following every *M*/2 input pulse. For *M* odd, one of the toggles is delayed an extra input cycle (e.g., 6 input pulses for output high and 5 input pulses for output low for $M = 11$).

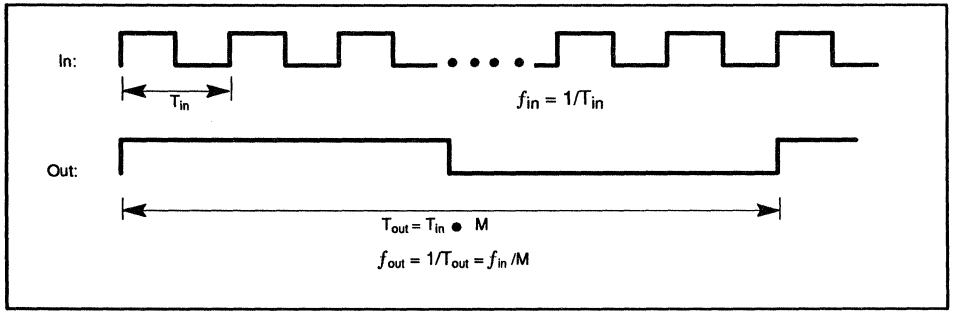

Figure15. Frequency Division

There are distinct differences between prescalers and general purpose divide-by-N counters. We will refer to the latter as program counters and substitute the letter N when referring to them for the remainder of this text.

12

Prescalers are comparatively simple devices. They contain a minimal amount of logic (less than approximately 100 gates) and offer a few, well chosen modulus numbers. This streamlined architecture allows implementation in the fastest bipolar and GaAs technologies without excessive power consumption or expense. For example, the MB510 dual modulus prescaler from Fujitsu offers a choice of four divide ratios

(128, 144, 256 and 272). Manufactured in 0.8 µm bipolar technology, this 8-pin device is ECL compatible, accepts input frequencies up to 2.7 GHz, and dissipates only 0.05 watts of power.

Program counters, on the other hand, contain a fair amount of programming and decoding logic in order to allow a wide selection of N (any value of N between 0 and $2_q{}^{-1}$ is made selectable using a q-bit wide program input). The relatively high internal gate count generally limits program counters to TTL or CMOS technology with toggling speeds of less than 40 MHz.

The important point to be made is that there is no need to make program counters faster, or prescalers more programmable. The distinction between the two types of devices is intentional. Once the frequency is brought down sufficiently by a prescaler, sophisticated frequency manipulation is performed with CMOS program counters and a PLL. Prescalers are generally classified as either single or dual modulus.

Dual modulus prescalers

Dual modulus prescalers allow a very rapid transition from a divide-by-M mode to a divide-by-$M+1$ mode (e.g., from 64 to 65); hence, they are often also called $M/M+1$ prescalers (64/65). In conjunction with PLLs and the pulse swallow method (discussed on page 14), dual modulus prescalers allow finer frequency resolution than single modulus prescalers.

Single modulus prescalers

Single modulus prescalers are fixed, or semi-fixed dividers that only divide by a fixed number M. A semi-fixed single modulus prescaler allows a choice of more than one modulus (e.g., 32, 64 and 128), but is not necessarily optimized for fast switching between moduluses, and the modulus choices are not spaced one apart.

Less common varieties of prescalers include:

- $M/M+Z$ (where $Z \neq 1$) dual modulus prescalers
- Four modulus prescalers
- Decimal single modulus prescalers

Figure 16 shows Fujitsu's bipolar prescaler ICs.

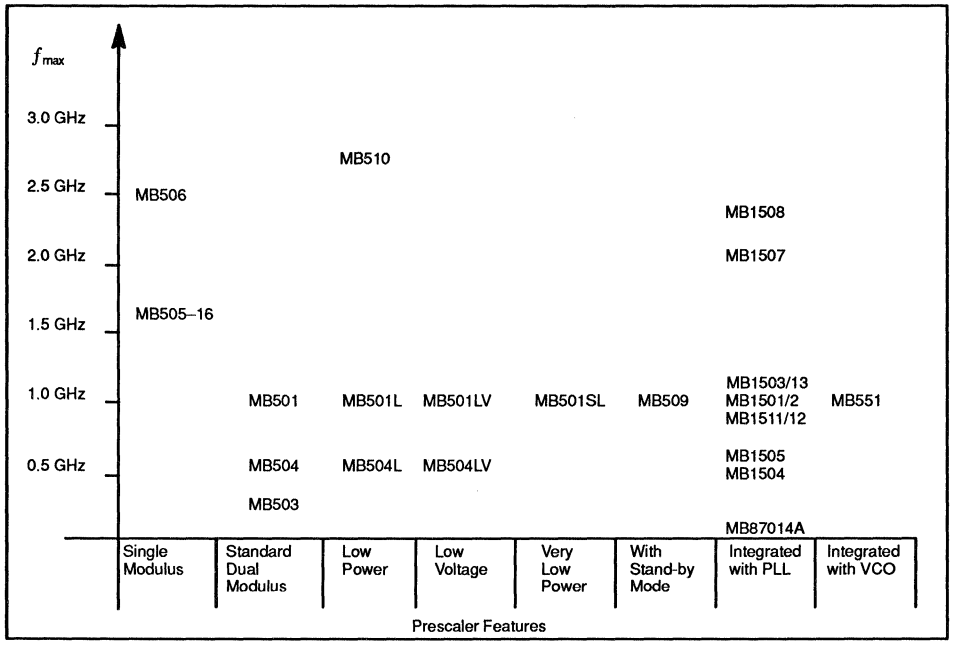

Figure 16. Selection Guide to the Fujitsu Bipolar Prescaler Family

Microwave Prescalers

Microwave prescalers manufactured in GaAs technology are available from specialized vendors, including Fujitsu. The microwave prescalers have frequencies above 3 GHz (microwave range) and toggle speeds of up to 10 GHz. The cost of GaAs parts, however, is considered high when compared to ECL bipolar parts.

Stand-alone Prescaler Application

Prescalers can be used as stand-alone components without a PLL.

A stand-alone application does not involve feedback of signals around the prescaler. The most common stand-alone application for a prescaler is in digital clock distribution networks, where a prescaler simply reduces an incoming clock rate and distributes it to slower analog or digital circuitry. (See Figure17.)

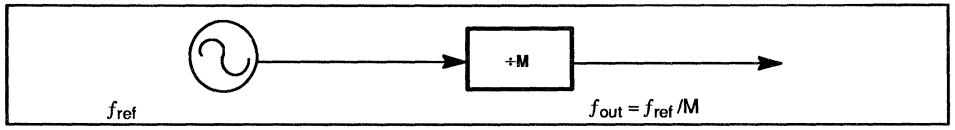

Figure 17. A Stand-alone Application of a Prescaler: Clock Rate Reduction

Prescalers offer several advantages as stand-alone elements. For example, consider an application that requires a high quality 1-MHz reference signal. For this application, a straightforward, high quality 1-MHz crystal oscillator might seem the most obvious choice; however, the highest quality will be

achieved with a higher frequency reference signal (10 MHz) followed by a prescaler (1/10). This application is preferred because of the following reasons:

- Crystal resonators with higher oscillation frequency tend to have smaller dimensions, shorter oscillation stabilization times and narrower characteristic variations.
- A prescaler will clean up the incoming high frequency signal in two ways:
  - It will totally remove variations in the amplitude noise (amplitude envelope of the incoming signal), since its output amplitude is independent of the input.
  - It will reduce the phase noise (jitter of zero-crossings) of the incoming signal by approximately a factor of M since its output only switches synchronously with one out of every M/2 input pulses.

The above reasons apply up to a certain point, or as long as the prescaling factor is moderate. The frequency of the crystal should not be increased to the point where RF shielding or board layout has to be changed. Increasingly small dimensions or the price of the crystal can also become a problem.

Numerous digital LSI ICs take advantage of the beneficial properties of prescaling; e.g., they have on-board prescalers that allow a direct connection of high frequency crystal clocks to slower internal logic. For example, Fujitsu's line of 4-bit microprocessors offers a built-in, divide-by-2 prescaler as a recommended option. This option allows the user to drive the 2-MHz internal logic with a 4-MHz crystal rather than a 2-MHz crystal. With this option, the 4-MHz crystal clock will turn on and be fully operational (as well as recover from any external disturbances) in half the time required for a 2-MHz crystal.

Selecting the Right Prescaler

To select the appropriate prescaler, first determine the necessary modulus choices and input toggling speeds.

Toggling speed

One should be aware that a 1-GHz ($f_{in,max}$ typically) prescaler does not abruptly stop functioning when fed frequencies above 1 GHz. The 1-GHz prescaler will typically require higher input levels to trigger, and it may deliver a smaller output swing, but typically it will function up to a 20-50 percent higher frequency. See Figure 18.

These characteristics are important, since frequency switching in a PLL is normally accompanied by a fair amount of overshoot. A VCO intended to stabilize at 1 GHz may reach, for example, 1.4 GHz before settling down. It is important that the loop (including the prescaler) remains functional during that period. Charts like Figure 18 can be helpful in verifying such cases.

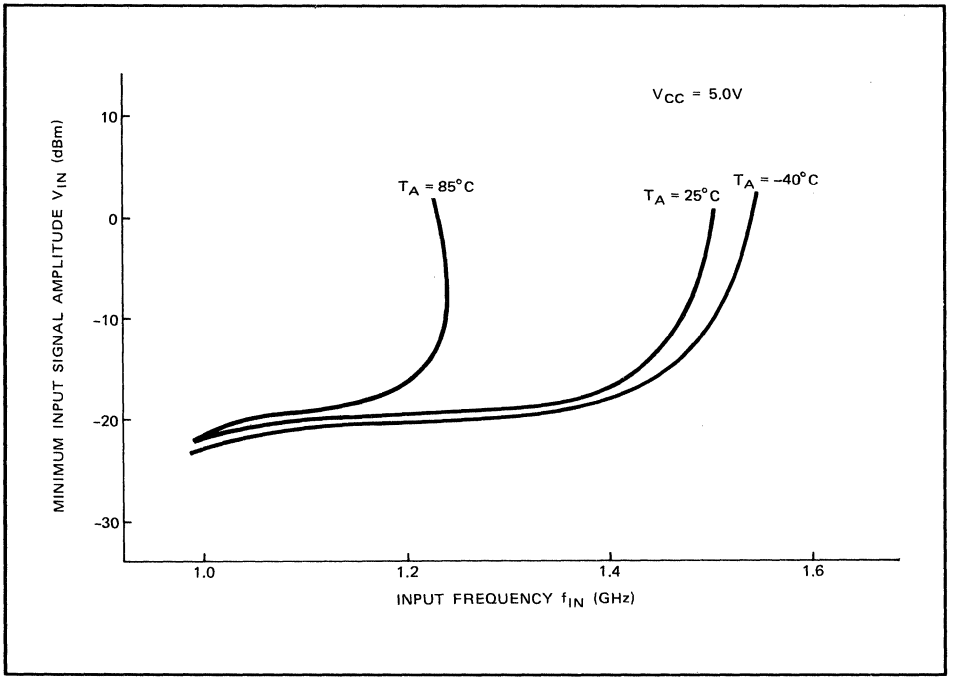

Figure 18. Input Signal Amplitude Versus Input Frequency for MB509 Dual Modulus Prescaler

Prescalers with higher frequency ratings will typically be associated with higher power dissipation and higher switching noise. For example, measurements of gallium arsenide dividers suggest noise performances 20 to 30 dB worse than for ECL dividers (reference 10).

Also note that the input coupling capacitance of a prescaler will limit the lowest useful frequency.

Termination resistor internal/external

All Fujitsu prescalers, except MB501LV, MB504LV, MB501SL, MB509, and MB510 have an open emitter output. Typically a 2.2k Ω resistor to ground for a load capacitance of 12 pF is recommended. By choosing a smaller or a larger external resistor, the prescaler's output can be tailored to drive higher or lower loads, respectively.

The prescalers with on-chip termination can drive output load capacitances of up to 8 pF undistorted. A shunt resistance can be added for driving larger loads.

In some situations it is desirable to "overdesign" the termination resistor. The limited current driving ability will tend to smooth the output signal, thus reducing its harmonic content and switching noise induced into supply lines.

Stability of V_{out}

One of the purposes of prescaling is to eliminate amplitude modulation from the output of the VCO. Therefore, it is absolutely mandatory that the output high and low are stable and guaranteed over a wide range of V_{in}, V_{cc}, and temperature.

Flexibility of the input voltage

A prescaler should be able to toggle properly with relatively widely varying input voltage levels (anywhere between 0.15 to 2 Vp-p for the Fujitsu MB 504), while maintaining a constant output level.

ECL level

For most Fujitsu prescalers the maximum allowable input voltage swing is 2 Vp-p. This means that a typical TTL voltage swing of 3 V will overload the prescaler, whereas ECL voltage levels can be accommodated without problems. The outputs of the prescaler are ECL compatible, too.

The statement "The outputs are 1.6 V peak on ECL level" found on the data sheet for MB501, 503, 504 etc. means that Fujitsu prescalers do not require negative supply voltages. In this sense they are not "true" ECL devices.

Flexibility of V_{cc}

A wide operational range of V_{cc} is essential (2.7 V to 4.5 V, 3.0 V typical for MB501LV), if a prescaler is to be used in a battery-powered system. Most Fujitsu prescalers, except the low voltage (LV-suffix) types which operate from a 3 V supply, operate from a single 5 V supply. The integrated PLLs, MB1501 and MB1504, however, operate from a 3 V supply (a higher supply voltage between V_{cc} and 8 V is required for the charge pump circuit).

Modulus set-up time

The time from application of appropriate voltage to the modulus select pin to appearance of the correctly prescaled waveform at the output is 10-50 ns. As previously discussed in the PLL section, fast modulus set-up times are necessary for correct implementation of the pulse swallow method.

Input impedance and reactance

Excessive reactance may affect performance of the VCO and require buffer circuitry between it and the prescaler. For very high frequencies (> 500 MHz), the input impedance should be given on a Smith chart. The nominal input impedance of Fujitsu's high frequency prescalers is 50Ω.

Smith chart

Signals on a printed circuit board travel at approximately 2/3 the speed of light. This means that at frequencies above 500 MHz, the signal wavelengths become less than 0.4 m and comparable in size to the board itself. At this point, circuit board traces start acting as transmission lines; i.e., the RMS voltage level will vary along the trace unless impedances of the termination and the trace are matched.

A Smith chart is a graphical impedance representation widely used in transmission theory. It is a tool allowing an easy assessment of impedance mismatch.

The chart consists of two sets of circles: the constant resistance circles (see Figure 19) and the constant reactance circles (see Figure 20). The values of these circles are normalized to the characteristic impedance of the system by dividing the actual value of resistance or reactance by the characteristic impedance, for example, in a 50 Ω system, a resistance of 100W is normalized to a value of 2.0.

A further series of circles may be plotted on the chart; these are the circles of constant voltage standing wave ratio (VSWR) and represent the degree of mismatch in the system. The VSWR is the ratio of the device impedance to the characteristic impedance. It is always expressed as a ratio greater than 1 (a 25 Ω device in a 50 Ω system gives rise to a 2:1 VSWR). See Figure 21.

Packaging

All Fujitsu prescalers are available in 8-pin DIP or surface mountable 8-pin plastic flat packages. Space saving and better stray capacitance performance are obtained with surface mounting.

CMOS PLLs and BiCMOS integrated PLLs are available in 16-pin DIP and Flatpacks.

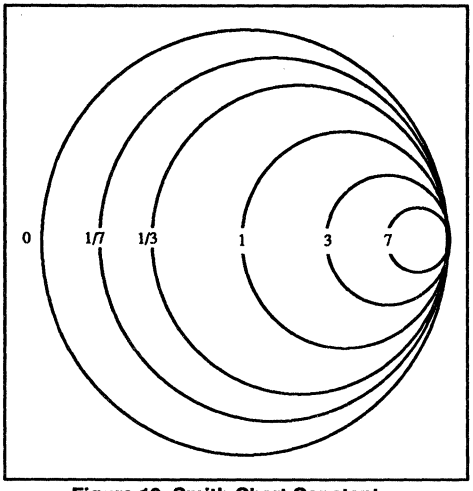

Figure 19. Smith Chart Constant Resistance

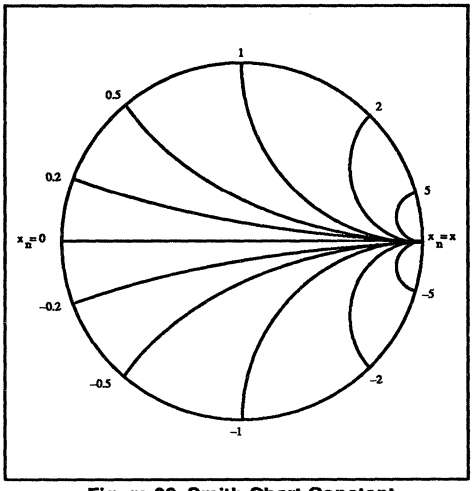

Figure 20. Smith Chart Constant Reactance

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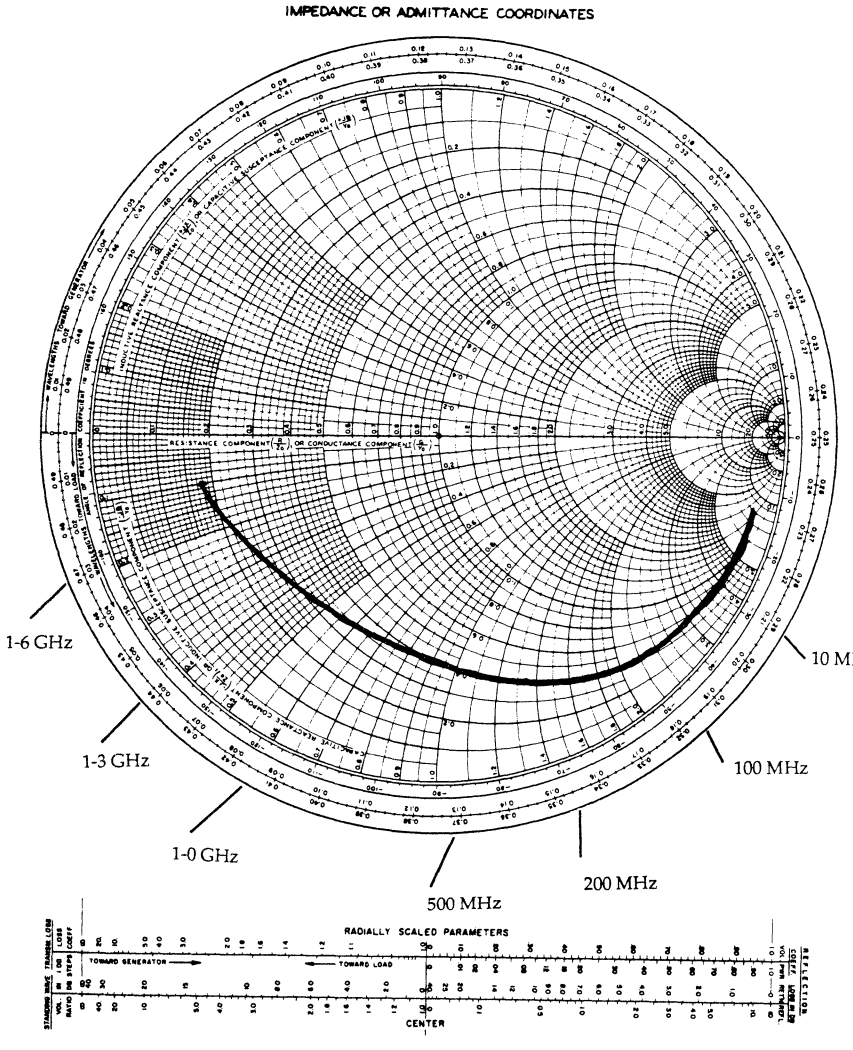

A standard commercially available form of Smith chart graph paper. Copyrighted 1949 by Philip Smith, Analog Instruments, New Providence, NJ, and reprinted with their permission.

Note: The nominal Z_{in} is 50 Ω.

Figure 21. Input Impedance of Fujitsu's MB501L Dual Modulus Prescaler as a Function of Frequency Shown on a Smith Chart

12

Signal propagation delay through the prescaler

Although a signal delay through the prescaler will affect the lock-in times of the loop, the prescaler is, in this respect, of little importance relative to the loop lowpass filter. Extensive phase shifts between the input and the output of the prescaler may, however, affect the PLL stability.

High capacitive loading will typically be the main cause for delays. This situation can be remedied by decreasing the output termination resistor value, thereby improving drive performance.

Self-oscillation problems can be caused by poor grounding, lack of decoupling, or cross-talk due to board layout. Fujitsu prescalers are guaranteed to be non-oscillatory under most conditions.

Balanced inputs

The ability to drive balanced inputs can be beneficial at high frequencies. All Fujitsu prescalers offer complementary inputs. The prescaler outputs, however, are single ended as they are intended to drive single-ended PLL inputs.

Output duty cycles

The output duty cycle should be 50 percent when the modulus is an even number (such as three input clock periods high and three input clock periods low for division with modulus 6). Division by an odd number should cause minimal deviation from 50 percent duty cycle (such as four input clocks high and three input clocks low for division with modulus 7). Rise and fall times are, of course, load dependent and deviations from idealized waveforms will occur. Also, clearly specify which of the output half-cycles (output low or output high) is the one that is extended in the M+1 mode of a dual modulus prescaler.

Power dissipation

Thanks to a proprietary, "third generation," 0.8 µm emitter self-align and polysilicon electrode and resistor (ESPER) manufacturing technology, Fujitsu can offer bipolar prescalers with the most beneficial frequency rating/power dissipation ratio available. See Table 3.

Table 3. Fujitsu Prescalers

P/N	F_{IN} (MAX)	V_{IN} (MIN)	Divide Ratio	I_{CC} (TYP)	Supply Voltage	Package
MB467	200 MHz	150 mVp-p	10/20	6 mA	5 V ± 10%	8 Pin DIP/FPT
MB501	1.0 GHz	400 mVp-p	64/65 128/129	30 mA	5 V ± 10%	8 Pin DIP/FPT
MB501L	1.1 GHz	400 mVp-p	64/65 128/129	10 mA	5 V ± 10%	8 Pin DIP/FPT
MB501LV	1.1 GHz	150 mVp-p	64/65 128/129	12 mA	3 V –10 – +50%	8 Pin DIP/FPT
MB501SL	1.1 GHz	100 mVp-p	64/65 128/129	5 mA	5 V ± 10%	8 Pin DIP/FPT
MB503	200 MHz	150 mVp-p	32/33	8 mA	5 V ± 10%	8 Pin DIP/FPT
MB504	520 MHz	150 mVp-p	32/33 64/65	10 mA	5 V ± 10%	8 Pin DIP/FPT
MB504L	520 MHz	150 mVp-p	32/33 64/65	5 mA	5 V ± 10%	8 Pin DIP/FPT
MB504LV	520 MHz	150 mVp-p	32/33 64/65	6 mA	3 V –10 – +50%	8 Pin DIP/FPT
MB505-16	1.6 GHz	150 mVp-p	128/129	9 mA	5 V ± 10%	8 Pin DIP/FPT
MB506	2.4 GHz	400 mVp-p	64/128 256	18 mA	5 V ± 10%	8 Pin DIP/FPT
MB507	1.6 GHz	400 mVp-p	128/129 256/257	18 mA	5 V ± 10%	8 Pin DIP/FPT
MB508	2.3 GHz	400 mVp-p	128/130 256/258 512/514	24 mA	5 V ± 10%	8 Pin DIP/FPT
MB509	1.1 GHz	400 mVp-p	64/65 128/129	11 mA	5 V ± 10%	8 Pin DIP/FPT
MB510	2.7 GHz	400 mVp-p	128/144 256/272	10 mA	5 V ± 10%	8 Pin FPT
MB511	1.0 GHz	60 mVp-p	1/2/8	23 mA	5 V ± 10%	8 Pin DIP/FPT

Conclusion

For further technical assistance and product information, including updates, please contact your nearest Fujitsu Microelectronics Sales Office. You will find a listing of the offices at the back of this paper.

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Glossary

CATV Cable Television.

CB RADIO Citizen Band Radio. The frequency bands allocated for short-distance personal or business radio communication. Present USA bands are 26.965 to 17.405 kHz, 72 to 76 MHz, and 462.550 to 467.425 MHz.

CMOS Complimentary Metal Oxide Semiconductor. A technology that is used for the manufacturing of low power consumption devices.

CODEC COder/DECoder.

DTMF Dual Tone Multifrequency

DIP Dual In-line Package.

ECL Emitter Coupled Logic. A technology that is used for the manufacturing of devices that operate at high frequencies.

Frequency The number of oscillations or cycles per unit of time.

FPT Flat Package Technology, usually referred to as Surface Mount Technology (SMT).

FSK Frequency shift keying. The form of frequency modulation in which the modulating wave shifts the output frequency between or among pre-determined values, and the output wave has no phase discontinuity.

GaAs Gallium Arsinide.

GHz Gigahertz. A unit of frequency equal to one billion cycles per second.

ISDN Integrated System Digital Network. A digital network in which all forms of communications, such as voice, data, and video, are converted to digital code and manipulated by computers serving as intelligent switching devices.

MHz Megahertz. A unit of frequency equal to one million cycles per second.

MSK Minimum shift keying.

Modem MOdulator/DEModulator. An equipment that connects data terminal equipment to a communication line.

Modulus The divide-by ratio of a prescaler counter.

PLL A device that locks onto a particular frequency. It is typically used in applications that require the tuning or selecting of communication channels.

Prescaler A device that divides the frequency of an incoming signal by a factor of N. N is the divide-by ratio of the counter and is called the modulus.

PSK Phase shift keying. The form of phase modulation in which the modulating function shifts the instantaneous phase of the modulated wave among pre-determined discrete values.

RF Radio Frequency. A frequency in the electromagnetic spectrum that is useful for radio transmission. Presently this refers to the limits of 10 kHz to 100,000 MHz.

UHF Ultra High Frequency. This range is 300 MHz to 3 GHz.

VHF Very High Frequency. This range is 30 MHz to 300 MHz.

1 Prescalers

2 Phase-Locked Loops (PLLs)

3 Single-Chip PLLs/Prescalers

4 Single-Chip VCOs/Prescalers

5 Piezoelectric Devices

6 Cordless Telephone Integrated Circuits

7 Telephone Integrated Circuits

8 Coders/Decoders (CODECs)

9 Quality and Reliability

10 Ordering Information

11 Sales Information

12 Appendix: Design Information

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