DRAM DATA BOOK



MCRON TECHNOLOGY, INC.

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DYNAMIC RAMS	1
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	g



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DRAM DATA BOOK

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ABOUT THE COVER:

Front — Clockwise from left, 1) Micron's 16 Meg DRAM wafer; 2) More than 4,000 Micron team members give painstaking attention to every step of the production process; 3) Scanning electron microscope (SEM) photograph of Micron's DRAM mini-stack process; and 4) Micron's Triple Port, Dual Port and 4 Meg DRAMs in SOJ, ZIP and TSOP packages.

Back — Micron's Boise, Idaho, corporate headquarters including three fabrication facilities.

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B. CRITICAL COMPONENT IS ANY COMPONENT OF A LIFE SUPPORT DEVICE OR SYSTEM WHOSE FAILURE TO PERFORM CAN BE REASONABLY EXPECTED TO CAUSE THE FAILURE OF THE LIFE SUPPORT DEVICE OR SYSTEM OR TO AFFECT ITS SAFETY OR EFFECTIVENESS.



Dear Customer:

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high quality, highly reliable memory components. Our corporate mission is

"To be a world class team developing advantages for our customers"

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs, VRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX™, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And, when you have a design or application question, you can get the answers you need from the source through one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team



ADVANTAGES

Micron Technology brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds and smallest die sizes. And we establish delivery standards based on your expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron Technology entered the memory market 14 years ago first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (VRAM and Triple Port DRAM), and a variety other memory products.

As we bring progressive memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. In 1990, Micron's Triple Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple Port's tradition. From FIFOs to processors, Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin IC DRAM Card. Ideal for laptop, notebook and other portable systems, Micron's IC DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

MILITARY CERTIFIED PRODUCTS

As one of the few manufacturers of military-grade memory in North America, Micron is proud to provide a documented source inspection from wafer start to finished product. We've earned recognition from U.S. and European space agencies as well as Joint Army/Navy

certification for both our NMOS and CMOS process technologies.

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for commercial and military use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers addedvalue services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

OUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with every Micron shipment. That's because we believe that quality must be internalized consistently at every level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX[™] intelligent burn-in and test system** gives Micron a unique edge in product reliability.

^{*}See NOTE, page v.

^{**}For more information on Micron's AMBYX™, see Section 7.



ABOUT THIS BOOK

CONTENT

The 1992 *DRAM Data Book* from Micron Technology provides complete specifications on all standard DRAMs and DRAM modules as well as specialty and derivative products based on our DRAM production process.

The *DRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *SRAM Data Book* and *Military Data Book*.

SECTION ORGANIZATION

Micron's 1992 *DRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The Data Book is organized into nine sections:

- Sections 1–5: Individual product families. Each contains a product selection guide followed by data sheets.
- Section 6: Application/technical notes.
- Section 7: Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX™ intelligent burn-in and test system.*
- · Section 8: Packaging information.
- Section 9: Product ordering information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the DRAM section begins with the 1 Meg x 1 followed by 4 Meg x 1 and all other x1 configurations in order of ascending depth. Next come the x4 products, followed by x8, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either **Advance**, **Preliminary** or **Final**. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of the front page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact

Micron Technology, Inc. 2805 East Columbia Road Boise, ID 83706 Phone: (208) 368-3900 FAX: (208) 368-4431 Customer Comment Line: 800-932-4992 (USA) 01-208-368-3410 (Intl.)

DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
"Advance"	This data sheet contains initial descriptions of products still under development.
"Preliminary"	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking (Final)	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
"New"	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the Data Book.

NOTE: Micron's DRAM Data Book uses acronyms to refer to certain industry-standard-setting bodies. These are defined below for your reference:

EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council.

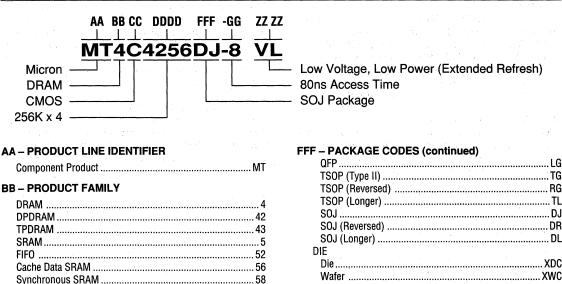
JEIDA—Japanese Electronics Industry Development Association.

PCMCIA—Personal Computer Memory Card International Association.

*Micron's Quality/Reliability Handbook is available by calling (208) 368-3900.



EXPANDED COMPONENT NUMBERING SYSTEM



CC - PROCESS TECHNOLOGY

CMOS	 	 	C
Low Voltage CMOS			1.0

DDDD - DEVICE NUMBER

(Can be modified to indicate variations)

DRAM	Width, Density
DPDRAM	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
CACHE	Density, Width
Latched SRAM	Total Bits, Width
FIFO	Width, Total Bits
Synchronous SRAM	

E - DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required)

Errata on Base PartQ

FFF - PACKAGE CODES

PLASTIC

DIP	Blank
DIP (Wide Body)	
ZIP	
LCC	
SOP/SOIC	Se Se

1001 (Type II)	
TSOP (Reversed)	RG
TSOP (Reversed) TSOP (Longer) SOJ	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Reversed)	DL
DIE	
Die	XDC
Wafer	XWC
Military Die	XD
Die	XW
DIP	C
DIP DIP (Narrow Body)	
DIP (Wide Body)	CW
LCC	EC
LCC (Narrow Body)	
LCC (Wide Body)	
SOP/SOIC	
00170010	

GG - ACCESS TIME

	8NS 0
	12ns or
	15ns or
2 (1.5 c) 1 (1.5	
(CDAM and a	
(SRAM only)	

SOJDCJ PGACA

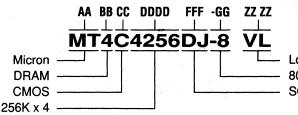
FLAT PACKF

-5 5ns or 50ns

ane or anne



EXPANDED COMPONENT NUMBERING SYSTEM (continued)



Low Voltage, Low Power (Extended Refresh) 80ns Access Time SOJ Package

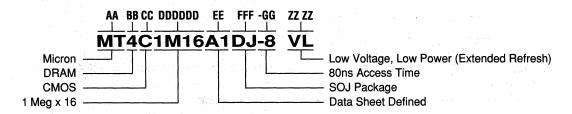
GG – ACCESS TIME (continued) -5555ns
-70 (SRAM only)70ns
ZZ ZZ – PROCESSING CODES (Multiple processing codes are separated by a space and are listed in hierarchical order).
Example: A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: V L IT
InterimI
Low VoltageV
DRAMS
Low Power (Extended Refresh)L
Low Voltage, Low Power (Extended Refresh)VL
Low Power (Self Refresh)S
Low Voltage, Low Power (Self Refresh)VS
SRAMS
Low Volt Data RetentionL
Low PowerP
Low Power, Low Volt Data RetentionLP
Low Voltage, Low PowerVP

ZZ ZZ - PROCESSING CODES (continued) Low Voltage, Low Volt Data RetentionVL Low Voltage, Low Volt Data Retention. Low PowerVB EPI Wafer E Commercial Testing 0°C to +70°C Blank -55°C to +125°CXT MIL-STD-883C Testing -55°C to +125°C883C -55°C to +110°C (DRAMs)883C Special Processing Engineering Sample ES Mechanical Sample MS Sample Kit*SK Tape and Reel*TR Bar Code* BC

^{*} Used in device order codes; this code is not marked on device.



NEW COMPONENT NUMBERING SYSTEM

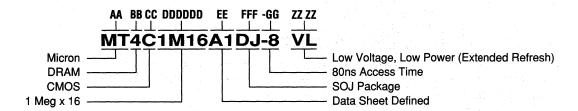


AA – PRODUCT LINE IDENTIFIER	
Component Product	Τ
BB - PRODUCT FAMILY	
DRAM 4 DPDRAM 4 TPDRAM 4 Synchronous DRAM 4 SRAM 5 Latched SRAM 5 Synchronous SRAM 5	12 18 5 16
CC - PROCESS TECHNOLOGY	
CMOSLow Voltage CMOSL	C .C
DDDDDD - DEVICE NUMBER	
Depth, Width	
Example: 1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory	
No LetterBi	
K	ts
EE – DEVICE VERSIONS	
(The first character is an alphabetic character only; the second character is a numeric character only.) Specified by individual data sheet	
FFF - PACKAGE CODES	
Plastic DIP Blar DIP (Wide Body) Y ZIP C E SOB/SQIC SOB/SQIC	W Z EJ

FFF – PACKAGE CODES (continued) QFPLG
TSOP (Type II)
TSOP (Reversed)RG
TSOP (Longer)TL
SOJDJ
SOJ (Reversed)DR
SOJ (Longer)DL
DIE GERMANNEN EINE GERMANNEN EINE AUS AUGUST DER GERMANNEN EINE GERMANNEN EINE GERMANNEN EINE GERMANNEN EINE G
DieXDC
WaferXWC
Military DieXD
Military WaferXW
CERAMIC
DIPC
DIP (Narrow Body)CN
DIP (Wide Body)CW
LCC (Narrow Body) ECN
LCC
LCC (Wide Body)
SOJDCJ
PGA
FLAT PACKF
TEAT FAON
GG – ACCESS TIME
-55ns or 50ns
-66ns or 60ns
-77ns or 70ns
-8
-10
-15
-17
-17
-25
-35
-45
-50 (SRAM only)50ns



NEW COMPONENT NUMBERING SYSTEM (continued)

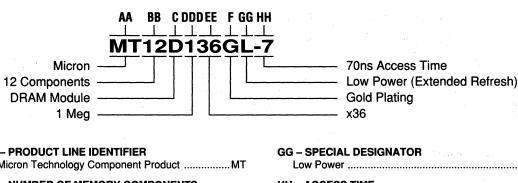


GG - ACCESS TIME (continued)	
-53	53ns
-55	55ns
-5570 (SRAM only)	70ns
ZZ ZZ – PROCESSING CODES	
(Multiple processing codes are separated by a space at all listed in hierarchical order.)	nd are
Example: A DRAM supporting low power, extended refresh (L); low vo (V) and the industrial temperature range (IT) would be indica V L IT	
Interim	1
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Voltage, Low Power (Extended Refresh)	
Low Power (Self Refresh)	
Low Voltage, Low Power (Self Refresh)	
SRAMs	
Low Volt Data Retention	1
Low Power	
Low Power, Low Volt Data Retention	I P
Low Voltage, Low Power	LF VD
LOW VOILAGE, LOW I OWEI	V F

ZZ ZZ – PROCESSING CODES (continued) Low Voltage, Low Volt Data Retention	VL
Low Voltage, Low Volt Data Retention, Low Power	VB
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	
-55°C to +125°C	
MIL-STD-883C Testing	
-55°C to +125°C	883C
-55°C to +110°C (DRAMs)	883C
0°C to +70°C	M070
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape and Reel*	TR
Bar Code*	BC



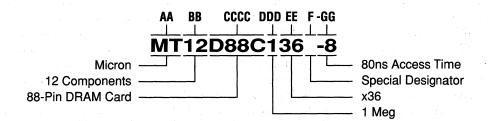
MODULE NUMBERING SYSTEM



- ACCESS TIME		
10	• • • • • • • • • • • • • • • • • • • •	10ns or 1
15	· · · · · · · · · · · · · · · · · · ·	
20		
25		
30		
35		
15	1.00	5 44 5.59
S		
,		



IC DRAM CARD NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER Micron Technology Component Product	MT
BB - NUMBER OF MEMORY COMPONENT	S
CCCC - DRAM CARD DESIGNATOR AND F	IN COUNT
88-Pin DRAM Card	D88C
60-Pin DRAM Card	D60C
DDD - DEPTH	

F - SPECIAL DESIG		×.
3.3 Volts		v
-5	 	
•	 	,

EE - WIDTH



DYNAMIC RAMS			PAGE
MT4C1024	1 Meg x 1	FP	1-1
MT4C1024 L		FP, LP	1-13
MT4C1026	1 Meg x 1	SC	1-25
MT4C1004J		FP	1-37
MT4C1004J L		FP, LP	1-49
MT4C1006J		SC	1-61
MT4C16M1A1		FP, 4KR	1-73
MT4LC16M1A1		FP, 4KR, LV	1-73
MT4C16M1D1		SC, 4KR	1-85
MT4C4256	256K x 4	FP	
MT4C4256 L	256K x 4	FP, LP	1-97
MT4C4256 VL		FP, LP, LV	1-109
MT4C4258	256K x 4	SC	1-121
MT4C4001J	1 Meg x 4	FP	1-133
MT4C4001J L		FP, LP	1-145
MT4C4003J		SC	1-157
MT4C4004J		FP, QCP	
MT4C4M4A1		FP, 4KR	1-183
MT4C4M4B1	O	FP, 2KR	1-183
MT4LC4M4A1	4 Meg x 4	FP, 4KR, LV	1-195
MT4LC4M4B1		FP, 2KR, LV	1-195
MT4C4M4D1		SC, 4KR	
FP	FAST PAGE MODE	LV	Low Voltage
SCLP		2KR4KR	
QCP	Quad CAS Parity		•
WIDE DRAMS			PAGE
MT4C8512	512K x 8	FP	2-1
MT4C8513		FP, WPB	2-1
MT4C8512 L	512K x 8	FP, LP	2-15
MT4C8513 L	512K x 8	FP, WPB, LP	
MT4(L)C2M8A1	2 Meg x 8	FP, 4KR	2-31
MT4(L)C2M8A2		FP, 4KR, WPB	2-31
MT4(L)C2M8B1	2 Meg x 8	FP, 2KR	2-47
MT4(L)C2M8B2	2 Meg x 8	FP, 2KR, WPB	2-47
MT4(L)C2M8A1 S	2 Meg x 8	FP, 4KR, S, LP	2-63
MT4(L)C2M8A2 S		FP, 4KR, WPB, S, LP	2-63
MT4(L)C2M8B1 S		FP, 2KR, S, LP	
MT4(L)C2M8B2 S	2 Meg x 8	FP, 2KR, WPB, S, LP	2-81
MT4C1664	64K x 16	FP, DW	2-99



V	VIDE DRAMS (continued)			PAGE
	MT4C1665	64K x 16	FP, WPB	. 2-99
	MT4C1664 L	64K x 16	FP, DW, LP	. 2-115
	MT4C1665 L	64K x 16	FP, WPB, LP	. 2-115
	MT4C1670	64K x 16	SC, DW	. 2-133
	MT4C1671	64K x 16	SC, WPB	
	MT4C1670 L	64K x 16	SC, DW, LP	
	MT4C1671 L		SC, WPB, LP	
	MT4C16256		FP, DW	
	MT4C16257		FP, DC	
	MT4C16258		FP, DW, WPB	
	MT4C16259		FP, DC, WPB	
	MT4C16256 L		FP, DW, LP	
	MT4C16257 L		FP, DC, LP	
	MT4C16258 L		FP, DW, WPB, LP	
	MT4C16259 L		FP, DC, WPB, LP	
	MT4C16260		FP, ASY, DW	
	MT4C16261		FP, WPB, ASY	
	MT4(L)C1M16C3		FP, DC	
	MT4(L)C1M16C5		FP, DW	
	MT4(L)C1M16C6		FP, DC, WPB	
	MT4(L)C1M16C7		FP, DW, WPB	
	MT4(L)C1M16C3 S		FP, DC, S, LP	
	MT4(L)C1M16C5 S		FP, DW, S, LP	
	MT4(L)C1M16C6 S		FP, DC, WPB, S, LP	
	MT4(L)C1M16C7 S		FP, DW, WPB, S, LP	
			11, DVV, VVI D, O, LI	. 2 201
	FP	FAST PAGE MODE	SCSTATIC	
	LP Low		WPBWRI'	
	2KR	2,048 Refresh	4KR 4, Asymmetrical	096 Refresh
		Seir Kerresn	AS1 Asymmetrical	Addressing
L	DRAM MODULES			
	MT2D2568	256K x 8	LP, LV*	. 3-1
	MT2D18	1 Meg x 8	LP, LV*	. 3-11
	MT8D18	1 Meg x 8	LP	. 3-21
	MT2D48	4 Meg x 8		. 3-31
	MT8D48	4 Meg x 8	LP	. 3-41
	MT8D168	16 Meg x 8		. 3-51
	MT3D2569		LP	
	MT3D19		LP	
	MT9D19		LP	
	MT3D49			
		O	요즘 그 아이들 이 이번 이번 하는 하는 것이 되는 것이 되었다. 이 사람들이 하는 생각이 되었다.	





DRAM MODULES (con	ntinued)	$oldsymbol{I}_{ij}$, which is a substitute of $oldsymbol{I}_{ij}$	PAGE
MT9D49	4 Meg x 9	LP	3-101
MT9D169	16 Meg x 9		3-111
MT8D25632	512K x 16	LP, LV*	3-121
MT16D51232	1 Meg x 16	LP, LV*	3-133
MT8D132	2 Meg x 16	LP, LV*	3-145
MT16D232	4 Meg x 16	LP, LV*	3-157
MT8D432	8 Meg x 16		3-169
MT16D832	16 Meg x 16		3-179
MT10D25636	512K x 18		3-199
MT6D118	1 Meg x 18		3-209
MT20D51236	1 Meg x 18	•	3-229
MT12D136	2 Meg x 18	LP	3-249
MT24D236		LP	3-271
MT12D436	8 Meg x 18	<u> </u>	3-283
MT24D836	16 Meg x 18		3-293
MT8D25632	256K x 32	LP, LV*	3-121
MT16D51232	512K x 32	LP, LV*	3-133
MT8D132	1 Meg x 32	LP, LV*	3-145
MT16D232	2 Meg x 32	LP, LV*	3-157
MT8D432	4 Meg x 32		3-169
MT16D832	8 Meg x 32		3-179
MT9D25636	256K x 36		3-189
MT10D25636	256K x 36		3-199
MT18D51236	512K x 36		3-219
MT20D51236	512K x 36	•••••	3-229
MT9D136	1 Meg x 36		3-239
MT12D136	1 Meg x 36	LP	3-249
MT18D236	2 Meg x 36		3-261
MT24D236	2 Meg x 36	LP	3-271
MT12D436	4 Meg x 36		3-283
MT24D836	8 Meg x 36		3-293
MT10D25640	256K x 40	LP, LV*	3-303
MT20D51240	512K x 40	LP, LV*	3-315
MT10D140	1 Meg x 40	LP, LV*	3-327
MT20D240	2 Meg x 40	LP, LV*	3-339
LP NOTE: All modules include FAST PAGE I	MODE cycle.	LV L *Contact factory regarding availability of low voltage versions.	ow Voltage



IC DRAM CARDS			PAGE
MT8D88C25632	512K x 16	•••••	4-1
MT16D88C51232	1 Meg x 16	•••••	4-17
MT8D88C132	2 Meg x 16		4-33
MT16D88C232		**************************************	4-49
MT12D88C25636	512K x 18		4-65
MT24D88C51236	1 Meg x 18		4-79
MT12D88C136	2 Meg x 18		4-93
MT24D88C236	4 Meg x 18		4-107
MT12D88C25640	512K x 20	#	4-121
MT24D88C51240	1 Meg x 20		4-137
MT12D88C140	2 Meg x 20	F	4-153
MT24D88C240	4 Meg x 20	92	4-169
MT8D88C25632	256K x 32	a y films a film of the second	4-1
MT16D88C51232	512K x 32		4-17
MT8D88C132	1 Meg x 32	•••••	4-33
MT16D88C232	2 Meg x 32		4-49
MT12D88C25636	256K x 36	•	4-65
MT24D88C51236	512K x 36		4-79
MT12D88C136	1 Meg x 36		4-93
MT24D88C236	2 Meg x 36	• • • • • • • • • • • • • • • • • • • •	4-107
MT12D88C25640			4-121
MT24D88C51240	512K x 40		4-137
MT12D88C140			
MT24D88C240	2 Meg x 40		4-169
MULTIPORT DRAM	S		PAGE
MT42C4255	256K x 4	FP	5-1
MT42C4256	256K x 4	FP, BW, LP	5-3
MT42C8127	128K x 8	FP	5-39
MT42C8128	128K x 8	FP, BW, LP	5-41
MT42C8255	256K x 8	FP, BW	5-79
MT42C8256	256K x 8	FP, BW	5-111
MT42C256K16A1	256K x 16	FP, BW	5-153
MT43C4257	256K x 4	FP, BW, QSF pin	5-155
MT43C4258	256K x 4	FP, BW, SSF pin	5-155
MT43C8128	128K x 8	FP, BW, QSF pin	
MT43C8129	128K x 8	FP, BW, SSF pin	
MT43C256K8A1	256K x 8	FP, BW,	
FP	FAST PAGE MODE	BW	BLOCK WRITE
ALL	LOW I OWEL, EXICHUEU REHESH		



APPLICATION/TECHNICAL INFO	RMATION	
TN-00-01 Moisture Absorption is	n Plastic Packages	6-1
	Procedures	
TN-04-01DRAM Power-up and	Refresh Constraints	6-9
TN-04-02MT4C1664 and MT4C1	1665 Compatibilities	6-11
TN-04-03MT4C1664: 256 Kiloby	te Memory System with Four RAS Lines	6-13
TN-04-04MT4C1664: 256 Kiloby	te Memory System with Four CAS Lines	6-15
TN-04-06DRAM OE Controlled	/LATE-WRITE Cycles	6-17
TN-04-08DRAM Timimg Param	neters	6-19
	nt vs. RAS Active Time (1 Meg)	
TN-04-12LPDRAM BBU Curren	nt vs. RAS Active Time (4 Meg)	6-23
TN-04-14Low Voltage (3V) DRA	AM Design Issues	6-25
TN-43-01MT43C4257/MT43C42	258 Comparison	6-27
	ls	
AN-04-01Chips & Technologies'	'82C456 VGA Controller Using MT4C1664	6-35
PRODUCT RELIABILITY Overview		7-1 7-12
Trocess frow Chart		7-12
PACKAGE INFORMATION		
Package Drawings		8-3
SALES INFORMATION		
SALES INFORMATION		
Customer Service Notes		9-1
Product Numbering System		9-5
	Distributors	
International Sales Representatives and Dis	stributors	9-25



J	UMERICAL INDEX		${f r}=({f r},{f r},{f r})$, where ${f r}$	AGE
	Part #, MT:			
	10D140	DRAM Modules		3-327
	10D25636			
	10D25640		() () () () () () () () () ()	
	12D136			
	12D436			
	12D88C136			
	12D88C140			
	12D88C25636		<u> </u>	
	12D88C25640			
	16D232			
	16D51232			
	16D832			
	16D88C232			
	16D88C51232			
	18D236			
	18D51236			
	20D240			
	20D51236			
	20D51240			
	24D236			
	24D836			
	24D88C236			
	24D88C240		<u> </u>	
	24D88C51236			
	24D88C51240			
	2D18			
10	2D2568			
	2D48		<u> </u>	
	3D19			
	3D2569			
	3D49			
	42C256K16A1			
	42C4255			
	42C4256			
	42C8127			
	42C8128			
	42C8255			
	42C8256			
	43C256K8A1			
	43C4257	TPDKAM		5-155



NUMERICAL INI Part #, MT:	DEX (continued)		PAGE
•	TPDRAM		E 155
	TPDRAM		
	TPDRAM	24	
	DRAM		
	DRAM		
	DRAM		
_	DRAM		
	DRAM		
	DRAM		
	Wide DRAM		
	Wide DRAM		
	Wide DRAM		
	Wide DRAM		2-191
	Wide DRAM		2-169
4C16258 L	Wide DRAM		2-191
4C16259	Wide DRAM		2-169
4C16259 L	Wide DRAM		2-191
4C16260	Wide DRAM	***************************************	2-213
4C16261	Wide DRAM	•	2-213
4C1664	Wide DRAM		2-99
4C1664 L	Wide DRAM		2-115
4C1665	Wide DRAM		2-99
	Wide DRAM		2-115
	Wide DRAM		2-133
	Wide DRAM		2-151
	Wide DRAM		2-133
	Wide DRAM		
	DRAM		
	DRAM		
	DRAM		
	DRAM		
	DRAM		
•	DRAM		
	DRAM		11
	DRAM		
	DRAM		
	DRAM		
	DRAM		
	DRAM		
4C4M4D1	DRAM		1-207



ľ	NUMERICAL INDEX	(continued)		PAGE
	Part #, MT:			
	4C8512	Wide DRAM		2-1
	4C8512 L	Wide DRAM		2-15
	4C8513	Wide DRAM		2-1
	4C8513 L	Wide DRAM		
	4LC16M1A1	DRAM		1-73
	4(L)C1M16C3	Wide DRAM		2-229
	4(L)C1M16C3 S	Wide DRAM		2-251
	4(L)C1M16C5			2-229
	4(L)C1M16C5 S			
	4(L)C1M16C6			2-229
	4(L)C1M16C6 S			2-251
	4(L)C1M16C7			2-229
	4(L)C1M16C7 S			
	4(L)C2M8A1			2-31
	4(L)C2M8A2	Wide DRAM		2-31
	4(L)C2M8B1			2-47
	4(L)C2M8B2	Wide DRAM	· · · · · · · · · · · · · · · · · · ·	2-47
	4(L)C2M8A1 S			2-63
	4(L)C2M8A2 S			2-63
	4(L)C2M8B1 S			2-81
	4(L)C2M8B2 S	Wide DRAM		
	4LC4M4A1			1-195
	4LC4M4B1	DRAM		1-195
	6D118	DRAM Modules		3-209
	8D132	DRAM Modules		
	8D168	DRAM Modules		3-51
	8D18	DRAM Modules		3-21
	8D25632	DRAM Modules		3-121
	8D432	DRAM Modules		3-169
	8D48	DRAM Modules	, , , , , , , , , , , , , , , , , , ,	3-41
	8D88C132	IC DRAM Cards		4-33
	8D88C25632	IC DRAM Cards		4-1
	9D136	DRAM Modules		3-239
	9D169	DRAM Modules		
	9D19	DRAM Modules		3-81
	9D25636	DRAM Modules		3-189
	9D49	DRAM Modules		3-101



PREFACE



DRAM PRODUCT SELECTION GUIDE

Memory	Optional	Part Access	Access	Typical Power Dissipation		Package and Number of Pins				
Configuration	Access Cycle	Number	Time (ns)	Standby	Active	PDIP	ZIP	SOJ	TSOP	Page
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20	20	1-1
1 Meg x 1	FP, LP	MT4C1024 L	70, 80, 100	0.3mW	150mW	18	20	20	20	1-13
1 Meg x 1	SC	MT4C1026	70, 80	3mW	175mW	18	20	20	- 1	1-25
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	- 1	20	20	20	1-37
4 Meg x 1	FP, LP	MT4C1004J L	60, 70, 80	1mW	225mW	-	20	20	20	1-49
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20	-	1-61
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70, 80	3mW	325mW	-	-	24	24	1-73
16 Meg x 1	FP, 4KR, LV	MT4LC16M1A1	60, 70, 80	1mW	125mW	- 1	-	24	24	1-73
16 Meg x 1	SC, 4KR	MT4C16M1D1	60, 70, 80	3mW	330mW	- 1	_	24	-	1-85
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20	20	1-87
256K x 4	FP, LP	MT4C4256 L	70, 80, 100	0.3mW	150mW	20	20	20	20	1-97
256K x 4	FP, LP, LV	MT4C4256 VL	100, 120	0.1mW	100mW	-	20	20	20	1-109
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20	-	1-121
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20	20	1-133
1 Meg x 4	FP, LP	MT4C4001J L	60, 70, 80	1mW	225mW	- 1	20	20	20	1-145
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20	- 1	1-157
1 Meg x 4	FP, QCP	MT4C4004J	70, 80, 100	3mW	225mW	-		24	- 1	1-169
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70, 80	3mW	325mW	- 1	-	24	24	1-183
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70, 80	3mW	400mW		-	24	24	1-183
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70, 80	1mW	125mW	- 1	- 1	24	24	1-195
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70, 80	1mW	175mW	- 1	-	24	24	1-195
4 Meg x 4	SC, 4KR	MT4C4M4D1	60, 70, 80	3mW	325mW	-	-	24	- 1	1-207

FP = Fast Page Mode, SC = Static Column Mode, LP = Low Power, Extended Refresh; QCP = Quad CAS Parity, LV = Low Voltage, 2KR = 2,048 Row Refresh, 4KR = 4,096 Row Refresh



WIDE DRAM PRODUCT SELECTION GUIDE

Memory	Optional	Part	Access	Typical Pow	er Dissipation	Packag	e/Number	of Pins	Terah.	
Configuration	Access Cycle	Number*	Time (ns)	Standby	Active	ZIP	SOJ	TSOP	Page	
512K x 8	FP	MT4C8512	70, 80, 100	3mW	350mW	28	28	28	2-1	
512K x 8	FP, WPB	MT4C8513	70, 80, 100	3mW	350mW	28	28	28	2-1	
512K x 8	FP, LP	MT4C8512 L	70, 80, 100	1mW	350mW	28	28	28	2-15	
512K x 8	FP, WPB, LP	MT4C8513 L	70, 80, 100	1mW	350mW	28	28	28	2-15	
2 Meg x 8	FP, 4KR	MT4(L)C2M8A1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31	
2 Meg x 8	FP, 4KR, WPB	MT4(L)C2M8A2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31	
2 Meg x 8	FP, 2KR	MT4(L)C2M8B1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47	
2 Meg x 8	FP, 2KR, WPB	MT4(L)C2M8B2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47	
2 Meg x 8	FP, 4KR, S, LP	MT4(L)C2M8A1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63	
2 Meg x 8	FP, 4KR, WPB, S, LP	MT4(L)C2M8A2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63	
2 Meg x 8	FP, 2KR, S, LP	MT4(L)C2M8B1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81	
2 Meg x 8	FP, 2KR, WPB, S, LP	MT4(L)C2M8B2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81	
64K x 16	FP, DW	MT4C1664	70, 80, 100	3mW	225mW	40	40	40	2-99	
64K x 16	FP, WPB	MT4C1665	70, 80, 100	3mW	225mW	40	40	40	2-99	
64K x 16	FP, DW, LP	MT4C1664 L	70, 80, 100	1mW	225mW	40	40	40	2-115	
64K x 16	FP, WPB, LP	MT4C1665 L	70, 80, 100	1mW	225mW	40	40	40	2-115	
64K x 16	SC, DW	MT4C1670	70, 80, 100	3mW	225mW	40	40	40	2-133	
64K x 16	SC, WPB	MT4C1671	70, 80, 100	3mW	225mW	40	40	40	2-133	
64K x 16	SC, DW, LP	MT4C1670 L	70, 80, 100	1mW	225mW	40	40	40	2-151	
64K x 16	SC, WPB, LP	MT4C1671 L	70, 80, 100	1mW	225mW	40	40	40	2-151	
256K x 16	FP, DW	MT4C16256	70, 80, 100	3mW	500mW	40	40	40	2-169	
256K x 16	FP, DC	MT4C16257	70, 80, 100	3mW	500mW	40	40	40	2-169	
256K x 16	FP, DW, WPB	MT4C16258	70, 80, 100	3mW	500mW	40	- 40	40	2-169	
256K x 16	FP, DC, WPB	MT4C16259	70, 80, 100	3mW	500mW	40	40	40	2-169	
256K x 16	FP, DW, LP	MT4C16256 L	70, 80, 100	1mW	500mW	40	40	40	2-191	
256K x 16	FP, DC, LP	MT4C16257 L	70, 80, 100	1mW	500mW	40	40	40	2-191	
256K x 16	FP, DW, WPB, LP	MT4C16258 L	70, 80, 100	1mW	500mW	40	40	40	2-191	
256K x 16	FP, DC, WPB, LP	MT4C16259 L	70, 80, 100	1mW	500mW	40	40	40	2-191	
256K x 16	FP, ASY, DW	MT4C16260	70, 80, 100	1mW	500mW	40	40	40	2-213	
256K x 16	FP, WPB, ASY	MT4C16261	70, 80, 100	1mW	500mW	40	40	40	2-213	
1 Meg x 16	FP, DC	MT4(L)C1M16C3	60, 70, 80	5mW	500mW	-	42	44	2-229	
1 Meg x 16	FP, DW	MT4(L)C1M16C5	60, 70, 80	5mW	500mW	 -	42	44	2-229	
1 Meg x 16	FP, DC, WPB	MT4(L)C1M16C6	60, 70, 80	5mW	500mW	-	42	44	2-229	
1 Meg x 16	FP, DW, WPB	MT4(L)C1M16C7	60, 70, 80	5mW	500mW	1 -	42	44	2-229	
1 Meg x 16	FP, DC, S, LP	MT4(L)C1M16C3 S	60, 70, 80	2mW	500mW	·	42	44	2-251	
1 Meg x 16	FP, DW, S, LP	MT4(L)C1M16C5 S	60, 70, 80	2mW	500mW	-	42	44	2-251	
1 Meg x 16	FP, DC, WPB, S, LP	MT4(L)C1M16C6 S	60, 70, 80	2mW	500mW	-	42	44	2-251	
1 Meg x 16	FP, DW, WPB, S, LP	MT4(L)C1M16C7 S	60, 70, 80	2mW	500mW	T -	42	44	2-251	

FP = Fast Page Mode, SC = Static Column, LP = Low Power, Extended Refresh; WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing

*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions



DRAM MODULE PRODUCT SELECTION GUIDE

Memory	Part	Optional Access Power Dissipation		issipation	Paci			
Configuration	Number	Access Cycle	Time (ns)	Standby	Active	SIMM	SIP	Page
256K x 8	MT2D2568	LP, LV*	60, 70, 80	6mW	350mW	30	30	3-1
1 Meg x 8	MT2D18	LP, LV*	60, 70, 80	6mW	450mW	30	30	3-11
1 Meg x 8	MT8D18	LP	60, 70, 80	24mW	1,400mW	30	30	3-21
4 Meg x 8	MT2D48		60, 70, 80	10mW	550mW	30	30	3-31
4 Meg x 8	MT8D48	LP	60, 70, 80	24mW	1,800mW	30	30	3-41
16 Meg x 8	MT8D168		60, 70, 80	24mW	2,200mW	30	30	3-51
256K x 9	MT3D2569	LP	60, 70, 80	9mW	625mW	30	30	3-61
1 Meg x 9	MT3D19	LP	60, 70, 80	9mW	625mW	30	30	3-71
1 Meg x 9	MT9D19	LP	60, 70, 80	27mW	1,575mW	30	30	3-81
4 Meg x 9	MT3D49		60, 70, 80	12mW	775mW	30	30	3-91
4 Meg x 9	MT9D49	LP	60, 70, 80	27mW	2,025mW	30	30	3-101
16 Meg x 9	MT9D169		60, 70, 80	27mW	2,475mW	30	30	3-111
512K x 16	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72		3-121
1 Meg x 16	MT16D51232	LP, LV*	60, 70, 80	48mW	2,800mW	72	-	3-133
2 Meg x 16	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
4 Meg x 16	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
8 Meg x 16	MT8D432		60, 70, 80	40mW	2,200mW	72	· -	3-169
16 Meg x 16	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
512K x 18	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
1 Meg x 18	MT6D118		60, 70, 80	18mW	1,250mW	72		3-209
1 Meg x 18	MT20D51236		60, 70, 80	60mW	1,780mW	72		3-229
2 Meg x 18	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
4 Meg x 18	MT24D236	LP	60, 70, 80	72mW	2,536mW	72		3-271
8 Meg x 18	MT12D436	30.12	60, 70, 80	52mW	3,100mW	72	-	3-283
16 Meg x 18	MT24D836	1 3 3 3 3	60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 32	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	- ÷	3-121
512K x 32	MT16D51232	LP, LV*	60, 70, 80	48mW	1,424mW	72	-	3-133
1 Meg x 32	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
2 Meg x 32	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
4 Meg x 32	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
8 Meg x 32	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
256K x 36	MT9D25636		60, 70, 80	27mW	1,575mW	72	-	3-189
256K x 36	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
512K x 36	MT18D51236		60, 70, 80	54mW	1,600mW	72		3-219
512K x 36	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
1 Meg x 36	MT9D136		60, 70, 80	27mW	2,175mW	72	-	3-239
1 Meg x 36	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
2 Meg x 36	MT18D236		60, 70, 80	54mW	2,052mW	72	-	3-26
2 Meg x 36	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	- 1 - 1	3-271
4 Meg x 36	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
8 Meg x 36	MT24D836	Jan San	60, 70, 80	104mW	3,152mW	72		3-293
256K x 40	MT10D25640	LP, LV*	60, 70, 80	30mW	1,750mW	72	-	3-303
512K x 40	MT20D51240	LP, LV*	60, 70, 80	60mW	1,780mW	72	-	3-315
1 Meg x 40	MT10D140	LP, LV*	60, 70, 80	30mW	2,250mW	72	-	3-327
2 Meg x 40	MT20D240	LP, LV*	60, 70, 80	60mW	2,280mW	72	_	3-339

LP = Low Power, Extended Refresh; LV = Low Voltage **NOTE:** All modules include FAST PAGE MODE cycle.

*Contact factory regarding availability of low voltage versions.



IC DRAM CARD SELECTION GUIDE

Memory		Part	Access	Number of Pins	
Configuration		Number	Time (ns)	Card	Page
512K x 16	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
1 Meg x 16	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
2 Meg x 16	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
4 Meg x 16	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
512K x 18	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
1 Meg x 18	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
2 Meg x 18	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
4 Meg x 18	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
512K x 20	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
1 Meg x 20	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
2 Meg x 20	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
4 Meg x 20	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169
256K x 32	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
512K x 32	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
256K x 36	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
512K x 36	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
1 Meg x 36	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
2 Meg x 36	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
256K x 40	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
512K x 40	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
1 Meg x 40	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
2 Meg x 40	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169



DUAL PORT DRAM (VRAM) PRODUCT SELECTION GUIDE

Memory Access		ss Part Access		Power Di	issipation	Package and Number of Pins				-
Configuration	Cycle	Number	Time (ns)	Standby	Active	SOJ	SOG	TSOP	ZIP	Page
256K x 4	FP	MT42C4255	80, 100	15mW	275mW	28	-	-	28	5-1
256K x 4	FP, BW, LP	MT42C4256	70, 80, 100	15mW	275mW	28	-	-	28	5-3
128K x 8	FP	MT42C8127	80, 100	15mW	275mW	40	-	-	-	5-39
128K x 8	FP, BW, LP	MT42C8128	70, 80, 100	15mW	275mW	40		40/44	-	5-41
256K x 8	FP, BW	MT42C8255	70, 80	10mW	300mW	40	- :	40/44	-	5-79
256K x 8	FP, BW	MT42C8256	70, 80	10mW	300mW	40	-	40/44	•	5-111
256K x 16	FP, BW	MT42C256K16A1	60, 70, 80	10mW	350mW	- 1 , 1	64		-	5-153

FP = Fast Page Mode, BW = Block Write, LP = Low Power, Extended Refresh

TRIPLE PORT DRAM PRODUCT SELECTION GUIDE

Memory	Access	Part	Access	Power Di	ssipation	Package/Number of P		Pins		
Configuration	Cycle	Number	Time (ns)	Standby	Active	SOJ	SOG	TSOP	PLCC	Page
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	5-155
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44		5-155
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	5-201
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	5-201
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW		64	-	-	5-247

FP = Fast Page Mode, BW = Block Write



APPLICATION/TECHNICAL NOTE SELECTION GUIDE

Technical Note	Title	Page
TN-00-01	Moisture Absorption in Plastic Packages	6-1
TN-00-02	Micron Tape and Reel Procedures	6-3
TN-04-01	DRAM Power-Up and Refresh Constraints	6-9
TN-04-02	MT4C1664 and MT4C1665 Compatibilities	6-11
TN-04-03	MT4C1664: 256 Kilobyte Memory System with Four RAS Lines	6-13
TN-04-04	MT4C1664: 256 Kilobyte Memory System with Four CAS Lines	6-15
TN-04-06	DRAM OE Controlled/LATE-WRITE Cycles	6-17
TN-04-08	DRAM Timing Parameters	6-19
TN-04-09	LPDRAM BBU Current vs. RAS Active Time (1 Meg)	6-21
TN-04-12	LPDRAM BBU Current vs. RAS Active Time (4 Meg)	6-23
TN-04-14	Low Voltage (3V) DRAM Design Issues	6-25
TN-43-01	MT43C4257/MT43C4258 Comparison	6-27
TN-88-01	88-Pin IC DRAM Cards	6-29
AN-04-01	Chips & Technologies' 82C456 VGA Controller Using MT4C1664	6-35

MICHON

DYNAMIC RAMS			1
WIDE DRAMS	**********		2
DRAM MODULES			3
IC DRAM CARDS		MI 600 NR NR NR NR NR NR NR NR	4
MULTIPORT DRAMS		医骶韧带 医腹膜 医血	5
APPLICATION/TECHNICAL	NOTES	MI 200 OM 200 OM 200 OM 500 OM 500 OM	
PRODUCT RELIABILITY		NNE (003 NNE 1986 NNE (NNE NNE NNE NNE	7.1
PACKAGE INFORMATION.		新新報服服期期	8
SALES INFORMATION			9



DRAM PRODUCT SELECTION GUIDE

Memory	Optional	Part	Access	Typical Powe	er Dissipation	Package and Number of Pins				
Configuration	Access Cycle	Number	Time (ns)	Standby	Active	PDIP	ZIP	SOJ	TSOP	Page
1 Meg x 1	FP	MT4C1024	60, 70, 80	3mW	175mW	18	20	20	20	1-1
1 Meg x 1	FP, LP	MT4C1024 L	70, 80, 100	0.3mW	150mW	18	20	20	20	1-13
1 Meg x 1	SC	MT4C1026	70, 80	3mW	175mW	18	20	20	-	1-25
4 Meg x 1	FP	MT4C1004J	60, 70, 80	3mW	225mW	-	20	20	20	1-37
4 Meg x 1	FP, LP	MT4C1004J L	60, 70, 80	1mW	225mW	-	20	20	20	1-49
4 Meg x 1	SC	MT4C1006J	70, 80	3mW	225mW	-	20	20	-	1-61
16 Meg x 1	FP, 4KR	MT4C16M1A1	60, 70, 80	3mW	325mW	-	-	24	24	1-73
16 Meg x 1	FP, 4KR, LV	MT4LC16M1A1	60, 70, 80	1mW	125mW	-	-	24	24	1-73
16 Meg x 1	SC, 4KR	MT4C16M1D1	60, 70, 80	3mW	330mW	-	-	24	-	1-85
256K x 4	FP	MT4C4256	60, 70, 80	3mW	175mW	20	20	20	20	1-87
256K x 4	FP, LP	MT4C4256 L	70, 80, 100	0.3mW	150mW	20	20	20	20	1-97
256K x 4	FP, LP, LV	MT4C4256 VL	100, 120	0.1mW	100mW	-	20	20	20	1-109
256K x 4	SC	MT4C4258	70, 80 ,100	3mW	175mW	20	20	20	-	1-121
1 Meg x 4	FP	MT4C4001J	60, 70, 80	3mW	225mW	-	20	20	20	1-133
1 Meg x 4	FP, LP	MT4C4001J L	60, 70, 80	1mW	225mW	-	20	20	20	1-145
1 Meg x 4	SC	MT4C4003J	70, 80	3mW	225mW	-	20	20	-	1-157
1 Meg x 4	FP, QCP	MT4C4004J	70, 80, 100	3mW	225mW	-	-	24	-	1-169
4 Meg x 4	FP, 4KR	MT4C4M4A1	60, 70, 80	3mW	325mW	-	-	24	24	1-183
4 Meg x 4	FP, 2KR	MT4C4M4B1	60, 70, 80	3mW	400mW	-	+	24	24	1-183
4 Meg x 4	FP, 4KR, LV	MT4LC4M4A1	60, 70, 80	1mW	125mW	-	-	24	24	1-195
4 Meg x 4	FP, 2KR, LV	MT4LC4M4B1	60, 70, 80	1mW	175mW	-	-	24	24	1-195
4 Meg x 4	SC, 4KR	MT4C4M4D1	60, 70, 80	3mW	325mW	1 -	-	24	-	1-207

 $FP = Fast\ Page\ Mode,\ SC = Static\ Column\ Mode,\ LP = Low\ Power,\ Extended\ Refresh;\ QCP = Quad\ CAS\ Parity,\ LV = Low\ Voltage,\ 2KR = 2,048\ Row\ Refresh,\ 4KR = 4,096\ Row\ Refresh$



DRAM

1 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS

MARKING

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8

Packages

Plastic DIP (300 mil)	 None
Plastic ZIP (350 mil)	\mathbf{Z}^{-}
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)***	TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

Operating Temperature, T_A
 Commercial (0°C to +70°C)
 Industrial (-40°C to +85°C)
 IT

GENERAL DESCRIPTION

The MT4C1024 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ and WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin, data out (Q), remains open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pin, Q is activated and

PIN ASSIGNMENT (Top View)

18-Pin DIP (N-1)	20-Pin ZIP (O-1)
D 1	*A9 1 = 1 2 CAS Q 3 = 1 2 4 Vss D 5 = 1 6 WE RAS 7 = 1 6 WE NC 9 = 1 10 NC A0 11 = 1 12 A1 A2 13 = 1 14 A3 Vcc 15 = 1 14 A3 Vcc 15 = 1 18 A6 A7 19 = 1 2 0 A8
20-Pin SOJ (Q-1)	20-Pin TSOP (R-1)
D 1 26 Vss WE 12 25 Q RAS 13 24 CAS "TF 14 23 NC	D 🗆 1 26 🗆 Vss WE 🗆 2 25 🗀 Q RAS 🗆 3 24 🗀 CAS **TF 🖂 4 23 🗀 NC NC 🗵 5 22 🗀 A9*
NC 5 22 A9*	NC □ 5 22 □ A9*

*Address not used for RAS-ONLY refresh

**TF = Test Function, Vin must not exceed Vcc+1V for normal operation
***Consult factory on availability of reverse pinout TSOP packages

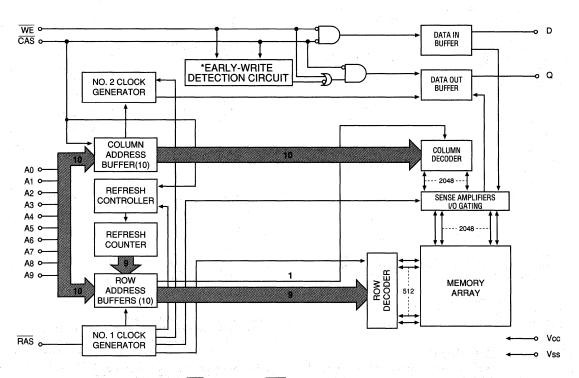
retains the selected cell data as long as \overline{CAS} remains LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed in by CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle

(READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



TRUTH TABLE

					ADDRESSES		DATA		
FUNCTION		RAS	CAS	WE	^t R	tC .	D (Data In)	Q (Data Out)	
Standby		Н	H→X	Х	Х	Х	Don't Care	High-Z	
READ		L	, , , , L , ,	Н	ROW	COL	Don't Care	Data Out	
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z	
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Don't Care	Data Out	
READ	2nd Cycle	L	H→L	Н	n/a	COL	Don't Care	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z	
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out	
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out	
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	Don't Çare	High-Z	
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Don't Care	Data Out	
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z	
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	Don't Care	High-Z	

I DRAN

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss1V to +	-7V
Operating Temperature, T _A (Ambient)0°C to +70)°C
Storage Temperature (Plastic)55°C to +150)°C
Power Dissipation600n	αW
Soldering Temperature (Soldering 10 Seconds) 260)°C
Short Circuit Output Current50r	nΑ

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le VIN \le 6.5V$ (All other pins not under test = $0V$)	lı	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (IouT = 4.2mA)	Vol		0.4	V	

		MAX]		
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{\text{IH}})$	lcc1	2	2	2	mA		
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	1	1	1	mA		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	90	80	70	mA	3, 4	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS, Address Cycling: [†] PC = [†] PC (MIN))	Icc4	70	60	50	mA	3, 4	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling; CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	90	80	70	mA	3	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icce	90	80	70	mA	3, 5	



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂		7	pF	2
Output Capacitance: Q	Co		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5.0V \pm 10\%$)

AC CHARACTERISTICS		Y	-6		-7		-8		4 37
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	135		155		175		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	60		65		70		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	†CAC		20		20		20	ns	15
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA	. 1	35		40		45	ns	
RAS pulse width	tRAS	60	100,000	. 70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20	a fagitiva	20	N . 1 . 14 (15	20	- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70	100000	80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0	1.8 27 . 27	ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	k. 1. 1
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20
WE command setup time	twcs	0		0	Transition (0		ns	21



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6		7		8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	^t WP	10	141 T. F. F.	15		15	Property of	ns	
Write command to RAS lead time	tRWL	20		20	5 1. 4	20		ns	
Write command to CAS lead time	tCWL	20		20		20	S	ns	
Data-in setup time	tDS	0		0	1	0		ns	22
Data-in hold time	tDH	15		15		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45	×1	55		60		ns	
RAS to WE delay time	tRWD	60		70		80		ns	21
Column address to WE delay time	tAWD	30		35	: "	40		ns	21
CAS to WE delay time	tCWD	15		20		20		ns	21
Transition time (rise or fall)	ŀΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	†REF		8		8		8	ms	N
RAS to CAS precharge time	tRPC	0	177	0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	[†] CHR	10		15		15		ns	5

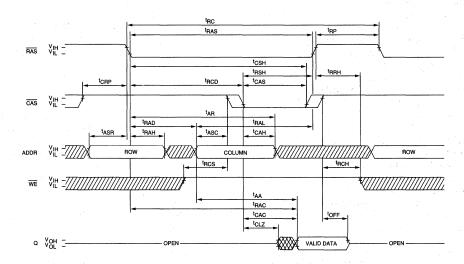


NOTES

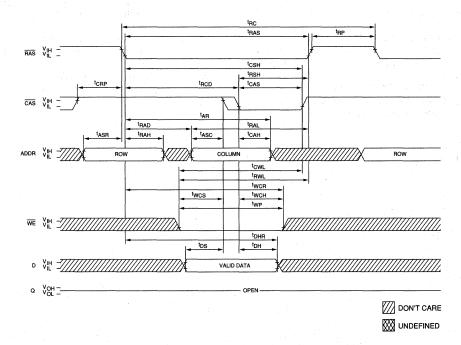
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. VCC = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a

- new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until CAS goes back to Vih).
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.

READ CYCLE



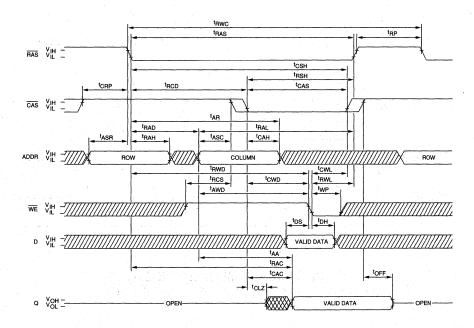
EARLY-WRITE CYCLE



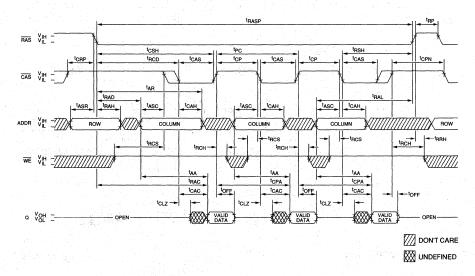
1-8



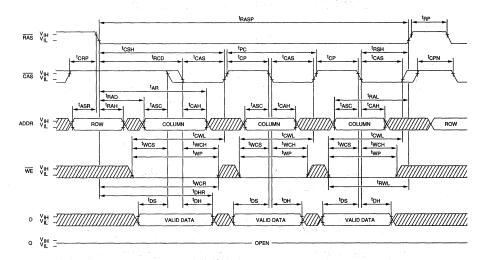
READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



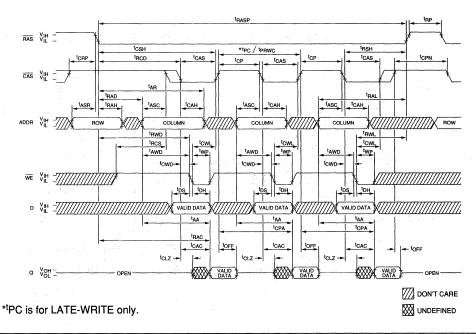
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



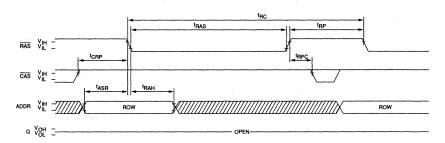
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





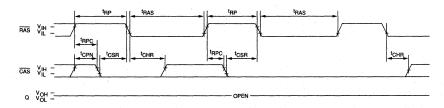
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and \overline{WE} = DON'T CARE)

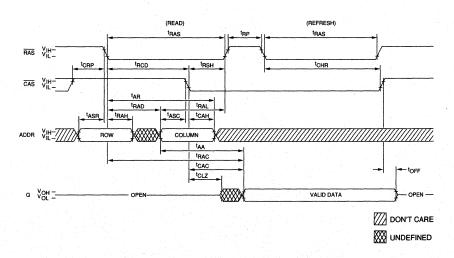


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 and $\overline{WE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 23 (WE = HIGH)





DRAM

1 MEG x 1 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, .3mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- 512-cycle extended refresh in 64ms
- Low CMOS STANDBY CURRENT, 200µA maximum

OPTIONS

MARKING

None

Timing	
70ns access	(S - 7
80ns access	- 8
100ns access	-10

 Packages Plastic DIP (300 mil) Plastic SOJ (300 mil)

Plastic SOJ (300 mil)
Plastic TSOP (300 mil)***
TG
Plastic ZIP (350 mil)
Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

Operating Temperature, T_A
 Commercial (0°C to +70°C)
 Industrial (-40°C to +85°C)
 IT

• Part Number Example: MT4C1024DJ-7 L

GENERAL DESCRIPTION

The MT4C1024 L is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ and WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin, data out (Q), remains open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pin, Q is activated and

PIN ASSIGNMENT (Top View)

18-Pin DIP (N-1)	20-Pi (O	n ZIP -1)
D [1 18] VS WE [2 17] Q RAS [3 16] C/ "TF [4 15] AS A0 [5 14] AS A1 [6 13] A7 A2 [7 12] A6 A3 [8 11] A5 Vcc [9 10] A4	Q 3 = 1	= 6 WE = 8 TF** = 10 NC = 12 A1 = 14 A3 = 16 A4
20-Pin SOJ	20-Pin	TSOP
(Q-1)	(R	-1)
WE d2 25 D RAS d3 24 D RAS d3 24 D RAS d3 24 D RAS d3 24 D RAS d3 D RAS d5	Q WE □ 2 DAS RAS □ 3 NC **TF □ 4	26 D Vss 25 D Q 24 D CAS 23 D NC 22 D A9*
A0 Q9 18 4 A1 Q10 17 D A A2 Q11 16 D A	A7 A1 □ 10	18 ⊞ A8 17 ⊞ A7 16 ⊞ A6

*Address not used for RAS-ONLY refresh

**TF = Test Function, Vin must not exceed Vcc+1V for normal operation
***Consult factory on availability of reverse pinout TSOP packages

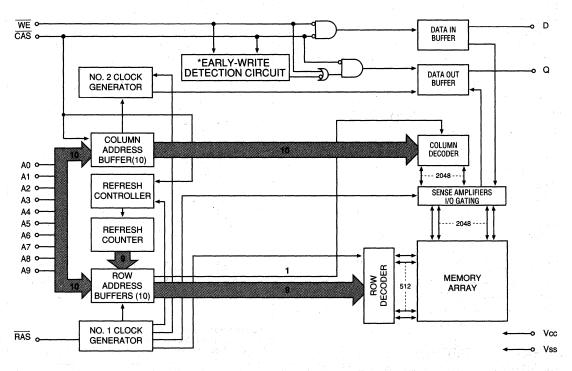
retains the selected cell data as long as \overline{CAS} remains LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle

(READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAMLOW POWER, FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



TRUTH TABLE

	17 15 15 15 15 15 15 15 15 15 15 15 15 15				ADDRI	ESSES	DA	TA
FUNCTION		RAS	CAS	WE	^t R	tC	D (Data In)	Q (Data Out)
Standby		Н	H→X	Х	Х	Х	Don't Care	High-Z
READ		L	L	Н	ROW	COL	Don't Care	Data Out
EARLY-WRITE	1.17	L	L	L	ROW	COL	Data In	High-Z
READ-WRITE	. a sastani	L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	Don't Care	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Х	Х	Х	Don't Care	High-Z

ABSOLUTE MAXIMUM RATINGS*

7V
°C
°C
W
°C
ιA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le VIN \le 6.5V$ (All other pins not under test = $0V$)	lı	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

		MAX]	
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μА	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: tRC = tRC (MIN))	lcc3	75	65	60	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS, Address Cycling: ¹PC = ¹PC (MIN))	Icc4	55	45	40	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling; CAS = V _{IH} : ^t RC = ^t RC (MIN))	lcc5	75	65	60	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC (MIN))	Icce	75	65	60	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = †RAS (MIN) to 1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), †RC = 125µs (512 rows at 125µs = 64ms)	lcc7	200	200	200	μА	3, 5, 7, 24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	Cit		5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂		7	pF	2
Output Capacitance: Q	Co		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		150		180	-	ns	
READ-WRITE cycle time	tRWC	155		175		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	65		70		85		ns	
Access time from RAS	†RAC		70		80		100	ns	14
Access time from CAS	†CAC		20		20		25	ns	15
Access time from column address	†AA		35		40		50	ns	
Access time from CAS precharge	^t CPA		40		45		50	ns	24%
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	TREE FOR
RAS hold time	†RSH	20		20		25		ns	
RAS precharge time	^t RP	50		60		70		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	^t CSH	70		80		100		ns	
CAS precharge time	[†] CPN	10		10	1	15		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10	1	10		ns	
RAS to CAS delay time	†RCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0	1	0		ns	
Row address hold time	†RAH	10		10		15		ns	
RAS to column- address delay time	†RAD	15	35	15	40	20	50	ns	18
Column address setup time	¹ ASC	0		0		0		ns	¥
Column address hold time	¹ CAH	15	1	15		20		ns	
Column address hold time (referenced to RAS)	^t AR	55		60		70		ns	
Column address to RAS lead time	^t RAL	35		40		50		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	1
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20
WE command setup time	twcs	0	1	0	1	0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-7			-8	Τ -	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		15		20		ns	
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15	8.7	15		20		ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25		ns	
Data-in setup time	†DS	0		0		0		ns	22
Data-in hold time	^t DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	tRWD	70		80		100		ns	21
Column address to WE delay time	^t AWD	35		40		50		ns	21
CAS to WE delay time	tCWD	20		20		25		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		64	1	64		64	ms	
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5



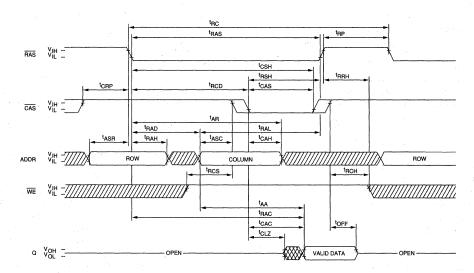
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $VCC = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.

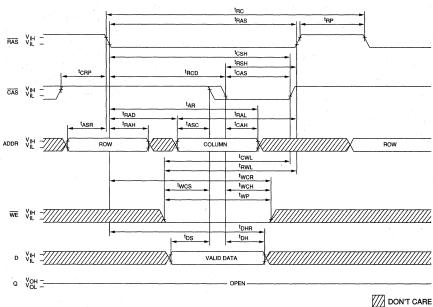
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until CAS goes back to VIH).
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 24. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.



READ CYCLE



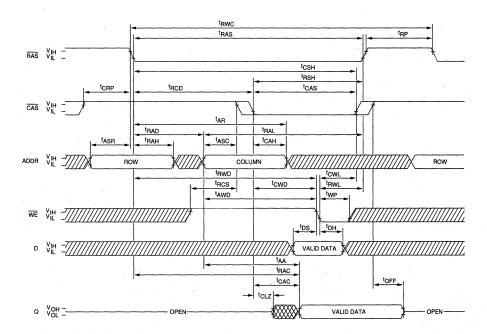
EARLY-WRITE CYCLE



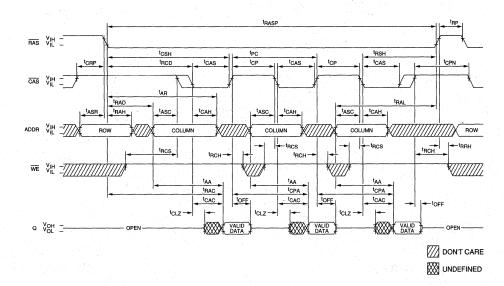




READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

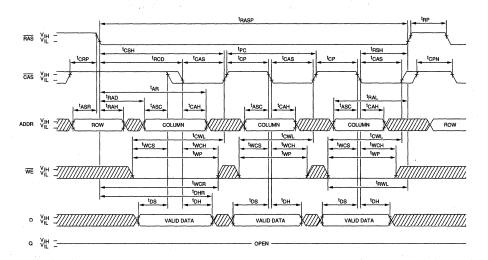


FAST-PAGE-MODE READ CYCLE

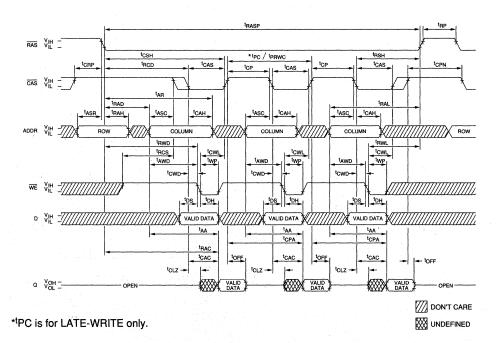




FAST-PAGE-MODE EARLY-WRITE CYCLE



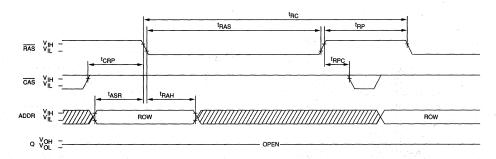
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





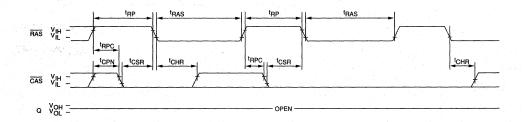
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and \overline{WE} = DON'T CARE)



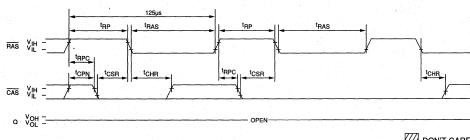
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 and $\overline{WE} = DON'T CARE$)



BATTERY BACKUP REFRESH CYCLE

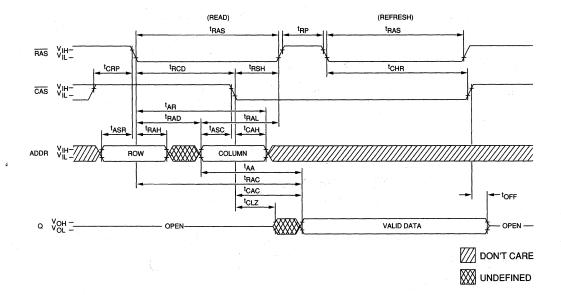
(A0-A9 and $\overline{WE} = DON'T CARE$)



DON'T CARE

W UNDEFINED

HIDDEN REFRESH CYCLE ²³ (WE = HIGH)





DRAM

1 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms

Plastic SOJ (300 mil)

Plastic ZIP (350 mil)

- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), and HIDDEN
- Optional STATIC COLUMN access cycle

OPTIONS	M	ARKIN	G
• Timing 70ns access		7	
80ns access		- 8	
100ns access		-10	
 Packages Plastic DIP (300 mil) 		None	

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

DI

GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin, data out (Q), remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first

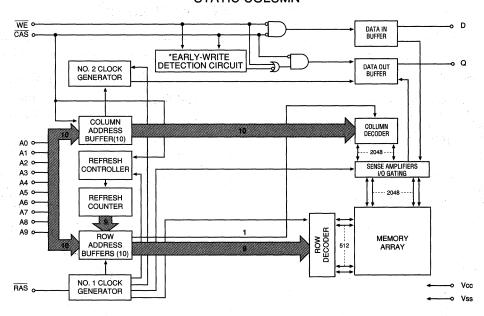
18-Pin (N-		20-Pin ZIF (O-1)
D [1 WE [2 RAS [3 3 **TF [4 4 A0 [5 A1 [6 A2 [7 A3 [8 Vcc [9		'A9 1 = 2 CA Q 3 = 2 CA Q 3 = 4 Vst
	D (1 WE (2 FAS (3 **TF (4 NC (15	26 D Vss 25 D Q 24 D CAS 23 D NC 22 D A9*

read, any column address transition will result in new data out. Unlike the page-mode part, which requires \overline{CAS} to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows \overline{CAS} to be left LOW for successive STATIC COLUMN accesses. Returning \overline{RAS} HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.



FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

					ADDRESSES DATA			TA
FUNCTION		RAS	CAS	WE	^t R	tC	D (Data In)	Q (Data Out)
Standby		Н	H→X	Х	Х	Х	Don't Care	High-Z
READ		L	' L	Н	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L'	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
STATIC COLUMN	1st Cycle	L	L	Н	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	L	Н	n/a	COL	Don't Care	Data Out
STATIC COLUMN	1st Cycle	L	L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	Ļ	L	H→L	n/a	COL	Data In	High-Z
STATIC COLUMN	1st Cycle	L	L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		. L	Н	Х	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	Don't Care	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient).	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	600mW
Soldering Temperature (Soldering 10 Sec	conds) 260°C
Short Circuit Output Current	50m A

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	į V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)		-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	٧	

지수 병원에 가는 그 가는 것이 그렇게 된 하지 않았다.		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	Icc2	1	1	1	mA		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	80	70	60	mA	3, 4	
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL; CAS, Address Cycling: tSC = tSC (MIN))	Icc4	60	50	40	mA	3, 4	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling; CAS = Vih: TRC = TRC (MIN))	lcc5	80	70	60	mA	3	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	80	70	60	mA	3, 5	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂		7	pF	2
Output Capacitance: Q	Со		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS	-7		-7	-8			10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	1.
READ-WRITE cycle time	^t RWC	155		175		205		ns	
STATIC-COLUMN READ	tSC	40		45		55		ns	
or WRITE cycle time									
STATIC-COLUMN READ-WRITE cycle time	tSRWC	70		80		100	14.2	ns	
Access time from RAS	†RAC		70		80		100	ns	14
Access time from CAS	†CAC		20		20		25	ns	15
Access time from column address	^t AA		35		40		50	ns	
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (STATIC COLUMN)	†RASC	70	100,000	80	100,000	100	100,000	ns	100
RAS hold time	^t RSH	20		20		25		ns	
RAS precharge time	^t RP	50		60		70		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	tCSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		15		ns	16
CAS precharge time (STATIC COLUMN)	^t CP	10		10		10		ns	i
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	^t ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		15		ns	
RAS to column address delay time	tRAD	15	35	15	40	20	50	ns	18
Column address setup time	tASC	0		0	2.00	0		ns	
Column address hold time	^t CAH	15		15		20		ns	
Column address hold time (referenced to RAS)	^t AR	80		90		100		ns	
Column address to RAS lead time	^t RAL	35		40		50		ns	
Read command setup time	†RCS	0		0		0	T Page 1	ns	- 41 1 1
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	^t CLZ	0		0	1	0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-7	•	-8	3	-1	0		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Column address hold time EARLY-WRITE (referenced to RAS)	tAWR	55		60		70		ns	
WE command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	15		15		20		ns	
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH.	15	····	15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	tRWD	70		80	7 7 7 7 7 7	100		ns	21
Column address to WE delay time	^t AWD	35		40		50		ns	21
CAS to WE delay time	tCWD	20		20		25		ns	21
Transition time (rise or fall)	^t T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^t REF		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	1
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
Write inactive time	tWI	10		10	Salar I	10		ns	
Previous WRITE to column address delay time	^t LWAD	20	30	20	35	25	45	ns	
Previous WRITE to column address hold time	tAHLW	65		75		95		ns	
Output data hold time from column address	^t AOH	5		5		5		ns	
Output data enable from WRITE	tOW	tAA + 5		tAA + 5		tAA + 5		ns	
Access time from last WRITE	^t ALW	65		75		95		ns	
Column address hold time referenced to RAS HIGH	tAH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	tcsc	^t CAS		†CAS		tCAS		ns	
Output data hold from WRITE	tWOH	0		0		0		ns	

DRAM

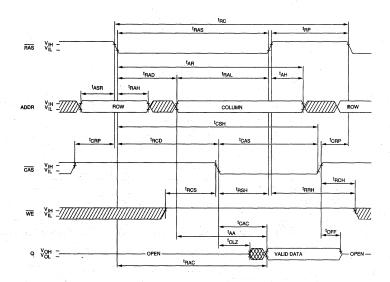
NOTES

- All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a

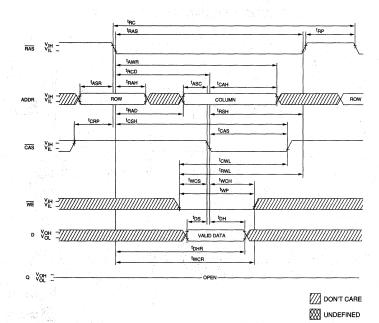
- new cycle and clear the data out buffer, \overline{CAS} must be pulsed HIGH for ${}^{t}CPN$.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until CAS goes back to V_{IH}).
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.



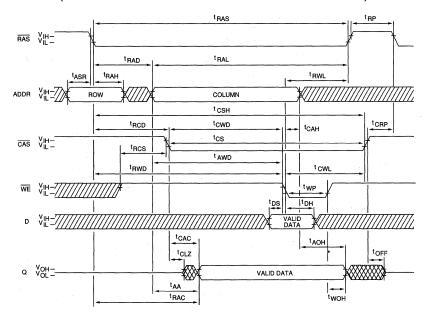
READ CYCLE



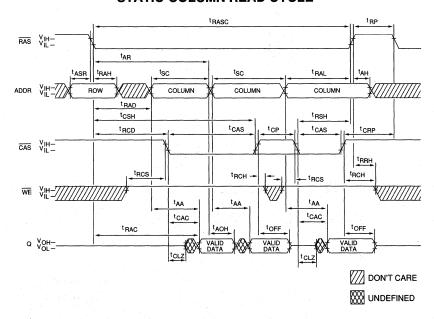
EARLY-WRITE CYCLE



READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

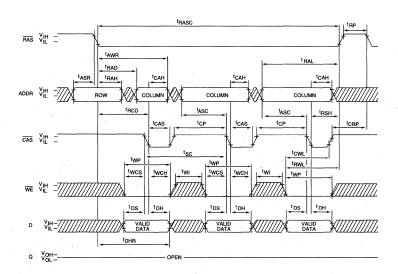


STATIC-COLUMN READ CYCLE

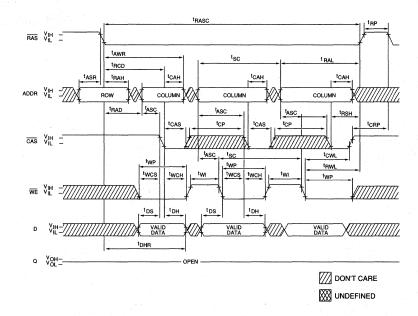




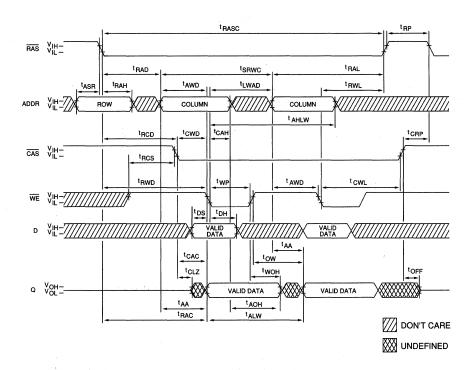
STATIC-COLUMN EARLY-WRITE CYCLE (CAS Controlled)



STATIC-COLUMN EARLY-WRITE CYCLE (WE Controlled)



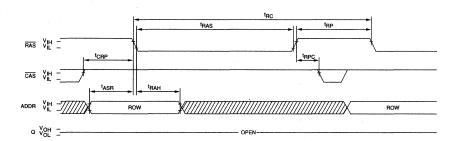
STATIC-COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





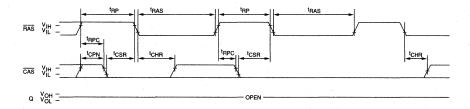
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and WE = DON'T CARE)

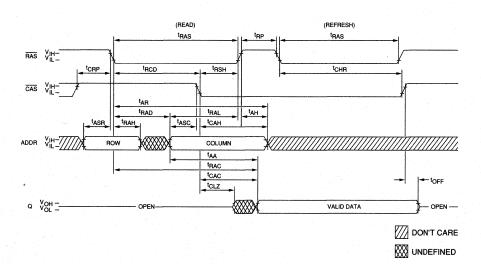


CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9 \text{ and } \overline{WE} = DON'T CARE)$



HIDDEN REFRESH CYCLE ²³ (WE = HIGH)





DRAM

4 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycle

OPTIONS • Timing 60ns access 70ns access 70ns access -6 70ns access -7 80ns access -8 • Packages Plastic SOJ (300 mil) Plastic TSOP (300 mil)** TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

Z

- Operating Temperature, T_A Commercial (0°C to +70°C) None Industrial (-40°C to +85°C) IT
- Part Number Example: MT4C1004JDJ-6

GENERAL DESCRIPTION

Plastic ZIP (350 mil)

The MT4C1004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. \overline{RAS} is used to latch the first 11 bits and \overline{CAS} the latter 11 bits. READ and WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin remains open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} remains LOW

PIN ASSIGNMENT (Top View) 20-Pin ZIP 20-Pin SOJ (Q-1) (0-1)D 1 WE 2 RAS 3 NC 4 <u>26</u> □ Vss 25 □ Q CAS Q 5 = 4 Vss 24 CAS 23 NC D WE 7 = 1 8 A10 9 = 1 10 NC RAS 22 A9 *A10 d 5 A10* NC A0 11 =1 ⊏ 12 A1 Vcc 15 = 14 A3
A5 17 = 16 A4
A7 19 = 1 18 A8 17 A7 16 A6 A0 49 A1 | 10 A2 | 11 A3 4 12 15 A5 Vcc 🖒 13 14 A4 20-Pin TSOP (R-1)DIII 1 26 P Vss WE = 2 25 □ Q 24 □ CAS RAS = 3 NC = 4 23 PNC 22 A9 *A10 🖂 5 A0 = 9 18 PA8 17 PA7 A1 10 16 - A6 15 - A5 A2 11 A3 4 12 14 P A4 Vcc 4 13 *Address not used for RAS-ONLY REFRESH *Consult factory on availability of reverse pinout TSOP packages

(regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

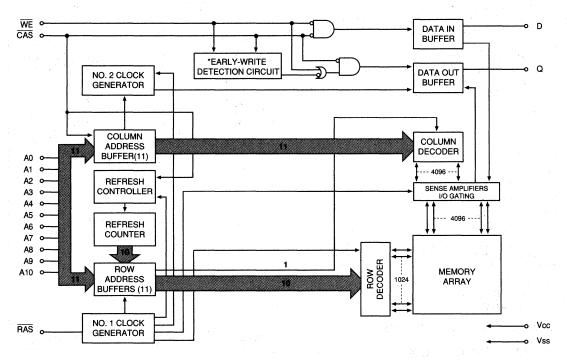
Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the



RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 1,024 combinations of RAS

addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic \overline{RAS} addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



TRUTH TABLE

		Street lands			ADDRESSES		DATA	
FUNCTION		RAS	CAS	WE	^t R	tC	D (Data In)	Q (Data Out)
Standby		Н	H→X	Х	Х	Х	Don't Care	High-Z
READ		L	L	Н	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	Lys	H→L	Н	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS REFRESH		H→L	L	Н	Х	Х	Don't Care	High-Z



■ DRAN

ABSOLUTE MAXIMUM RATINGS*

11 100
1V to +7V
0°C to +70°C
55°C to +150°C
1W
50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	, 1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	li'	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	loc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	80	70	60	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V _{IH} : ^t RC = ^t RC (MIN))	lcc5	110	100	90	mA	3
REFRESH CURRENT: CAS -BEFORE- RAS Average power supply current (RAS, CAS, Address Cycling: the table to the table to the table to the table to the table table to the table table	Icc6	110	100	90	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	Cit		5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂		7	pF	2
Output Capacitance: Q	Co		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	-7		-8		1. At 1.	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	†RWC	135	1-2-4	155		175		ns	
FAST-PAGE-MODE	^t PC	40		40		45		ns	
READ or WRITE cycle time								5 5445	
FAST-PAGE-MODE	^t PRWC	60	Tall to the second	65		70		ns	Art .
READ-WRITE cycle time			1 1						
Access time from RAS	tRAC	4.	60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	tAA .		30		35		40	ns	
Access time from CAS precharge	^t CPA		35	1 / 14	40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	. 10
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	3-9/1 F
RAS hold time	tRSH	15		20		20	The services	ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	†CSH	60		70		80		ns	
CAS precharge time	[†] CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	1	ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	10		10		10		ns	er er
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	†RAD	15	30	15	35	15	40	ns	18
address delay time			1					Pro Depart	
Column address setup time	†ASC	0		0	4.25	0		ns	
Column address hold time	^t CAH	10		15		15	T	ns	
Column address hold time	†AR	50		55		60		ns	
(referenced to RAS)									
Column address to	†RAL	30		35		40		ns	
RAS lead time								1.5	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	tRCH	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	†RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	†CLZ	0		0		0	1	ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0	1	0	1 1 1 1 1 1	ns	21



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6	-	7		-8	100	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	†DH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	60		70		80		ns	21
Column address to WE delay time	^t AWD	30		35		40		ns	21
CAS to WE delay time	tCWD	15		15		20		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	tREF :		16		16		16	ms	
RAS to CAS precharge time	tRPC	. 0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10	n	ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	24, 25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24, 25
WE hold time (WCBR test cycle)	^t WTH	10		10		10		ns	24, 25
WE setup time (WCBR test cycle)	twts	10		10		10		ns	24, 25



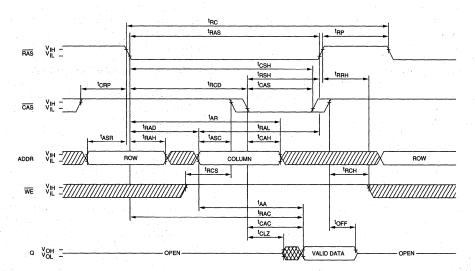
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{\rm IL}$ and $V_{\rm IL}$ (or between $V_{\rm IL}$ and $V_{\rm IH}$) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.

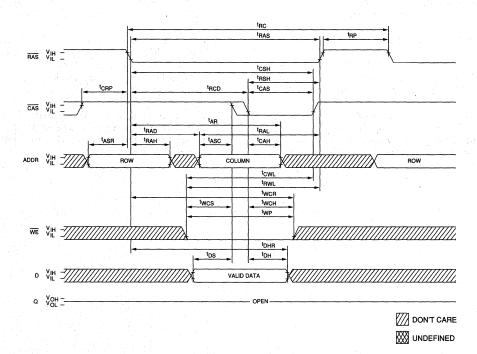
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the 'RAD (MAX) limit ensures that 'RAC (MIN) and 'CAC (MIN) can be met. 'RAD (MAX) is specified as a reference point only; if 'RAD is greater than the specified 'RAD (MAX) limit, then access time is controlled exclusively by 'AA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until CAS goes back to VIH).
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 24. tWTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 25. JEDEC test mode only.



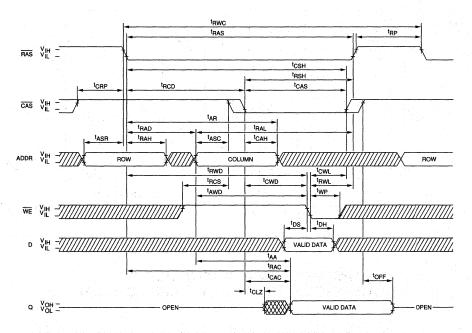
READ CYCLE



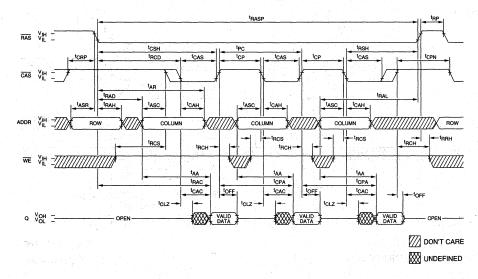
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



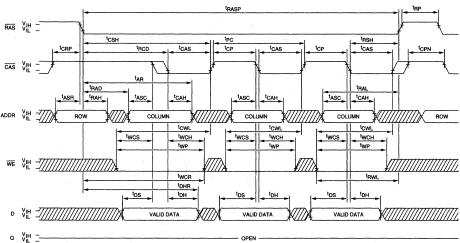
FAST-PAGE-MODE READ CYCLE



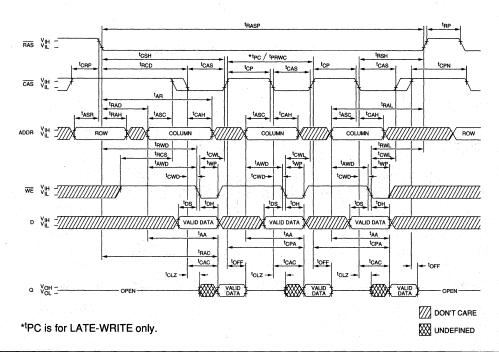
MICRON



FAST-PAGE-MODE EARLY-WRITE CYCLE

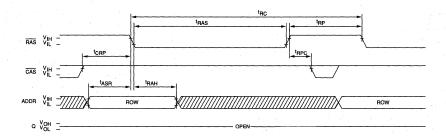


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



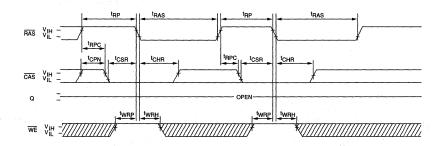


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; A10 and WE = DON'T CARE)



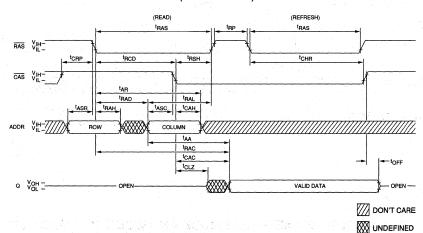
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

(WE = HIGH)



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

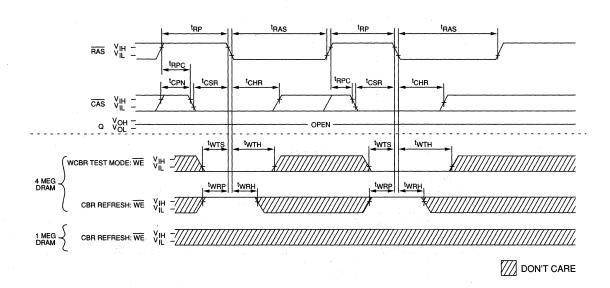
A CBR cycle with WE LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight \overline{RAS} cycles. The 4 Meg POWER-UP is more restrictive in that eight \overline{RAS} -ONLY or CBR REFRESH (\overline{WE} held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a \overline{RAS} -ONLY or a CBR REFRESH cycle (\overline{WE} held HIGH).

SUMMARY

- The 1 Meg CBR REFRESH allows the WE pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
- The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

4 MEG x 1 DRAM

LOW POWER. EXTENDED REFRESH

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single $+5V \pm 10\%$ power supply
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- 1,024-cycle extended refresh distributed across 128ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
80ns access	-8
Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)**	TG
Plastic ZIP (350 mil)	\mathbf{Z}
NOTE: Available in die form (comm	nercial or military) or military ceramic

packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

• Part Number Example: MT4C1004JDJ-6 L

GENERAL DESCRIPTION

The MT4C1004J L is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 pits (A0-A10) at a time. RAS is used to latch the first 11 bits ınd CAS the latter 11 bits. READ and WRITE cycles are elected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE node. During a WRITE cycle, data in (D) is latched by the alling edge of WE or CAS, whichever occurs last. If WE goes .OW prior to CAS going LOW, the output pin remains open High-Z) until the next CAS cycle. If WE goes LOW after ata reaches the output pin, data out (Q) is activated and etains the selected cell data as long as CAS remains LOW regardless of WE or RAS). This late WE pulse results in a EAD-WRITE cycle.

FAST PAGE MODE operations allow faster data operaons (READ, WRITE or READ-MODIFY-WRITE) within a w address (A0-A10) defined page boundary. The FAST

PIN ASSIGNMENT (Top View)

20-Pin	20-Pin ZIP	
(Q-	(O-1)	
D 1 WE 2 2 RAS 13 NC 14 *A10 15 A1 11 10 A2 11 A3 112 Vec 13 13	26) Vss 25] Q 24] CAS 23] NC 22] A9 18] A8 17] A7 16] A6 15] A6 14] A4	A9 1 2 2 CAS Q 3 2 5 4 Vss D 5 7 1 6 WE NC 9 1 6 NC A0 11 1 1 1 10 NC A0 11 1 1 1 12 A1 A2 13 2 11 14 A3 Voc 15 2 1 16 A4 A5 17 2 1 16 A6 A7 19 1 1 8 A6 A7 19 1 2 0 A8

20-Pin TSOP

(R-1)

		,	
ME CE RAS CE NC CE *A10 CE	2 3 4	25 24 23	⊞ Vss ⊞ Q ⊞ CAS ⊞ NC ⊞ A9
A0 == A1 == A2 == A3 == Vcc ==	10 11 12	17 16 15	⊞ A8 ⊞ A7 ⊞ A6 ⊞ A5 ⊞ A4

*Address not used for RAS-ONLY REFRESH

PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RASHIGH terminates the FAST PAGE MODE operation.

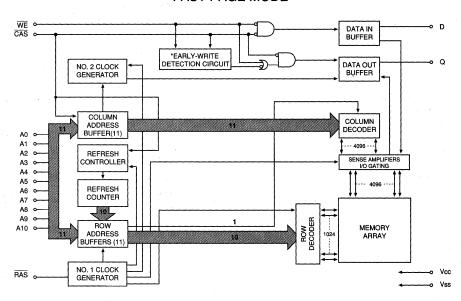
Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), BATTERY BACKUP or HIDDEN refresh) so that all 1.024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR and BATTERY BACKUP cycles will invoke the internal refresh counter for automatic RAS addressing.

The MT4C1004I L contains the EIA/JEDEC defined test mode.

^{**}Consult factory on availability of reverse pinout TSOP packages



FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

					ADDRESSES		DA	TA
FUNCTION		RAS	CAS	WE	^t R	tC.	D (Data In)	Q (Data Out)
Standby		Н	H→X	Х	Х	Х	Don't Care	High-Z
READ		L	L	Н	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L.	L'	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Don't Care	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRESH		L	Н	X	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Don't Care	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	X	X	Don't Care	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	lı .	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μΑ	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lссз	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	80	70	60	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: tRC = tRC (MIN))	lcc5	110	100	90	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (WE = VIH, RAS, CAS, Address Cycling: tRC = tRC (MIN))	Icc6	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = [†] RAS (MIN) to 300ns; WE = Vcc -0.2V, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), [†] RC = 125μs (1,024 rows at 125μs = 128ms)	lcc7	300	300	300	μА	3, 5, 7, 25

MICHON TECHNOLOGY, INC.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	Cıı	5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂	7	pF	2
Output Capacitance: Q	Co	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-67		-7	-8		<u> </u>		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	100
READ-WRITE cycle time	tRWC	135		155		175		ns	
FAST-PAGE-MODE	^t PC	40		40		45		ns	
READ or WRITE cycle time									
FAST-PAGE-MODE	^t PRWC	60		65		70		ns	
READ-WRITE cycle time									
Access time from RAS	^t RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	25
RAS pulse width (FAST PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	25
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	-
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	. 10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	^t ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column	tRAD	15	30	15	35	15	40	ns	18
address delay time									1 1 1 1 1 1
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time	tAR	50		55		60		ns	P 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
(referenced to RAS)						1 3 6 7			
Column address to	tRAL	30		35		40		ns	
RAS lead time							1		
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	tRCH.	0		0		0		ns	19
(referenced to CAS)				M. 19					and the
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)			Section 1						
CAS to output in Low-Z	tCLZ	0		0		0	1 1 1 1 1 1 1 1	ns	100
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0	1 1 2 3	0		ns	21



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10	31	15	N. 1.11 (2.14)	15	1000	ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15	1 1 1 1 1 1	ns	an well
Write command to RAS lead time	tRWL	15	- 1	20	1.19.0	20	1 40	ns	
Write command to CAS lead time	tCWL	15	1	20	100	20	1000	ns	75. S.V.
Data-in setup time	tDS .	0		0	142 5 166	0	100	ns	22
Data-in hold time	tDH	10		15	Part For The	15	1 2 2	ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	†RWD	60		70		80		ns	21
Column address to WE delay time	^t AWD	30		35		40	early of the	ns	21
CAS to WE delay time	tCWD	15		15		20		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	†REF		128		128		128	ms	
RAS to CAS precharge time	†RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10	and the second	10		10		ns	24
WE hold time (WCBR test cycle)	tWTH	10		10	19-38 (13.6 43.6 (13.6	10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24



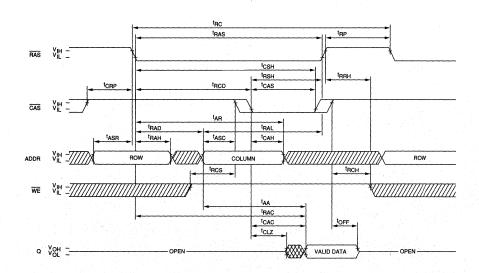
NOTES

- All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VII. (or between VII. and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that

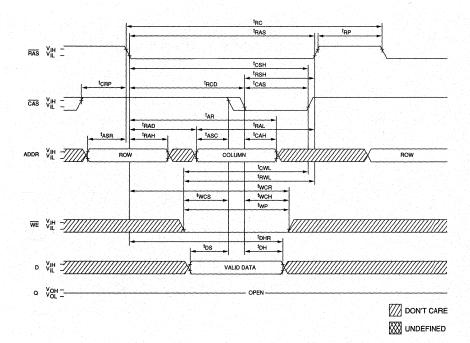
- ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the 'RAD (MAX) limit ensures that 'RAC (MIN) and 'CAC (MIN) can be met. 'RAD (MAX) is specified as a reference point only; if 'RAD is greater than the specified 'RAD (MAX) limit, then access time is controlled exclusively by 'AA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until CAS goes back to VIH).
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 24. WTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 25. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.



READ CYCLE

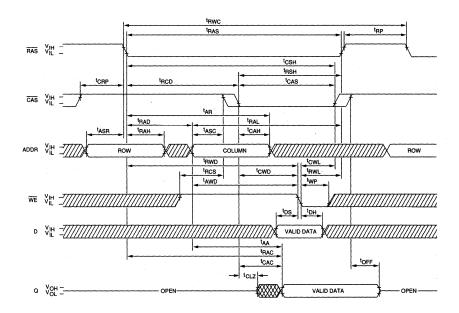


EARLY-WRITE CYCLE

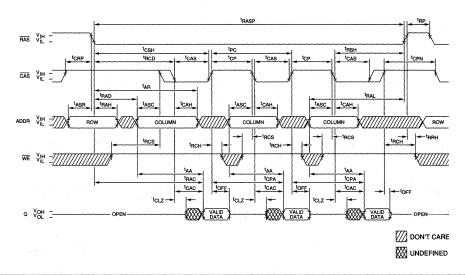




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

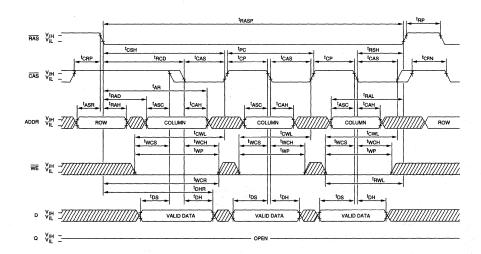


FAST-PAGE-MODE READ CYCLE

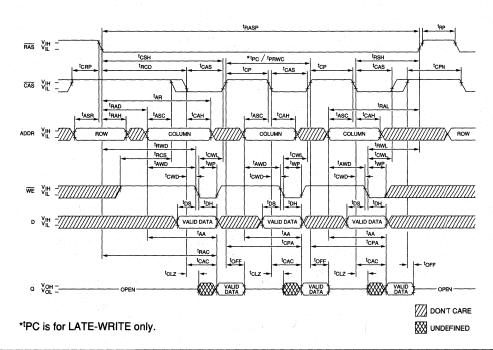




FAST-PAGE-MODE EARLY-WRITE CYCLE

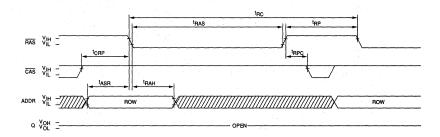


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



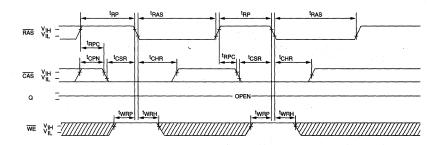


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; A10 and WE = DON'T CARE)



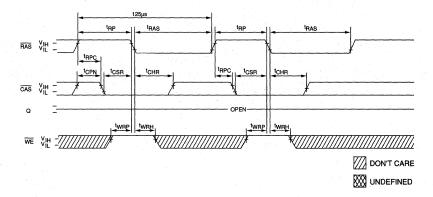
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DONTCARE)



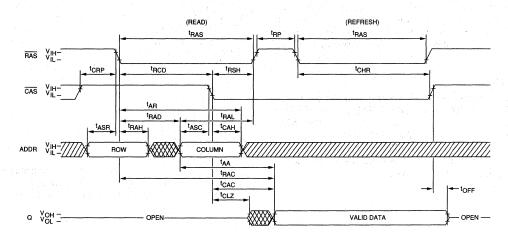
BATTERY BACKUP REFRESH CYCLE

(A0-A10 = DON'T CARE)





HIDDEN REFRESH CYCLE 23 (WE = HIGH)



DON'T CARE



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

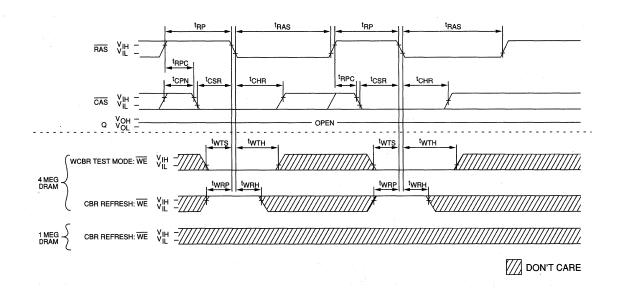
A CBR cycle with $\overline{\text{WE}}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight \overline{RAS} cycles. The 4 Meg POWER-UP is more restrictive in that eight \overline{RAS} -ONLY or CBR REFRESH (\overline{WE} held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a \overline{RAS} -ONLY or a CBR REFRESH cycle (\overline{WE} held HIGH).

SUMMARY

- The 1 Meg CBR REFRESH allows the WE pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
- The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

4 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- STATIC COLUMN access cycle

OPTIONS	MARKING
• Timing	
70ns access	-7
80ns access	-8
Packages	
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

Part Number Example: MT4C1006JDJ-7

GENERAL DESCRIPTION

The MT4C1006I is a randomly accessed solid-state nemory containing 4,194,304 bits organized in a x1 configuation. During READ or WRITE cycles, each bit is uniquely ddressed through the 22 address bits, which are entered 11 its (A0-A10) at a time. \overline{RAS} is used to latch the first 11 bits nd CAS the latter 11 bits. READ and WRITE cycles are elected with the WE input. A logic HIGH on WE dictates EAD mode while a logic LOW on WE dictates WRITE node. During a WRITE cycle, data in (D) is latched by the ılling edge of WE or CAS, whichever occurs last. If WE goes OW prior to CAS going LOW, the output pin remains open -ligh-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after ata reaches the output pin, data out (Q) is activated and tains the selected cell data as long as CAS remains LOW egardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a EAD-WRITE cycle.

STATIC COLÚMN operations allow faster data operaons (READ, WRITE or READ-MODIFY-WRITE) within a

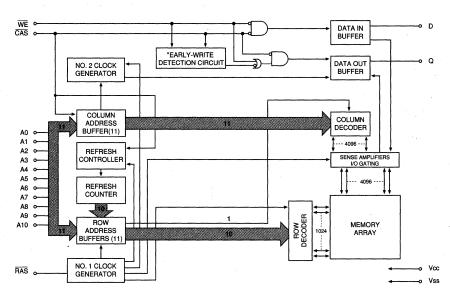
PIN ASSIGN	IMENT (Top View)
20-Pin SOJ (Q-1)	20-Pin ZIP (O-1)
WE 2 25 26 27 27 28 29 29 29 29 29 29 29	NC RAS 7 = 6 WE NC 9 = 10 NC A0 11 = 10 NC A2 13 = 12 A1
*Address not used for RAS-ON	ILY REFRESH

row address (A0-A10) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires \overline{CAS} to be toggled for each successive page-mode access, the STATIC COLUMN part allows \overline{CAS} to be left LOW for successive STATIC COLUMN accesses. Returning \overline{RAS} HIGH terminates the STATIC COLUMN operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR), or HIDDEN refresh) so that all 1,024 combinations of \overline{RAS} addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic \overline{RAS} addressing.



FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

					ADDRI	ESSES	DA	TA
FUNCTION		RAS	CAS	WE	^t R	tC.	D (Data In)	Q (Data Out)
Standby	4 4 4	н	H→X	Х	X	X	Don't Care	High-Z
READ		L	L	Н	ROW	COL	Don't Care	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In	High-Z
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out
STATIC COLUMN	1st Cycle	L.	L	Н	ROW	COL	Don't Care	Data Out
READ	2nd Cycle	e, L	L	Н	n/a	COL	Don't Care	Data Out
STATIC COLUMN	1st Cycle	L	L	L	ROW	COL	Data In	High-Z
EARLY-WRITE	2nd Cycle	L	Ĺ	H→L	n/a	COL	Data In	High-Z
STATIC COLUMN	1st Cycle	L	L	H→L	ROW	COL	Data In	Data Out
READ-WRITE	2nd Cycle	L	L	H→L	n/a	COL	Data In	Data Out
RAS-ONLY REFRES	SH	L	Н	Х	ROW	n/a	Don't Care	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Don't Care	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In	High-Z
CAS-BEFORE-RAS	REFRESH	H→L	L	Н	Х	Х	Don't Care	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	Vih	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	l II	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol	e a se	0.4	٧	

		MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	Icc2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	Іссз	100	90	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ^t SC = ^t SC (MIN))	Icc4	70	60	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: ^t RC = ^t RC (MIN))	lcc5	100	90	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc6	100	90	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	Cıı		5	pF	2
Input Capacitance: RAS, CAS, WE	C ₁₂		7	pF	2
Output Capacitance: Q	Co		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-7			-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		150	1	ns	21
READ-WRITE cycle time	tRWC	155		175		ns	. 1
STATIC-COLUMN	tSC	40		45		ns	·.
READ or WRITE cycle time			1				
STATIC-COLUMN	tSRWC	70		75		ns	
READ-WRITE cycle time					1	40 mm m	
Access time from RAS	tRAC		70		80	ns	14
Access time from CAS	^t CAC		20		20	ns	15
Access time from column address	tAA .		35	100	40	ns	
RAS pulse width	tRAS	70	100,000	80	100,000	ns	
RAS pulse width (STATIC COLUMN)	tRASC	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	20		20		ns	
RAS precharge time	t _{RP}	50		60		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	70		80		ns	
CAS precharge time	^t CPN	10		10		ns	16
CAS precharge time (STATIC COLUMN)	^t CP	10		10		ns	
RAS to CAS delay time	tRCD	20	50	20	60	ns	. 17
CAS to RAS precharge time	^t CRP	10		10		ns	
Row address setup time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
RAS to column	tRAD	15	35	15	40	ns	18
address delay time				- N		1.1	1000
Column address setup time	tASC	0		0		ns	
Column address hold time	^t CAH	15		15		ns	
Column address hold time	^t AR	80		90		ns	447.7
(referenced to RAS)							11/2
Column address to	†RAL	35		40		ns	
RAS lead time						Section Section	
Read command setup time	tRCS	0		0		ns	
Read command hold time	tRCH	0		0		ns	19
(referenced to CAS)							
Read command hold time	tRRH	0		0		ns	19
(referenced to RAS)							
CAS to output in Low-Z	†CLZ	0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	ns	20
Column address hold time	tAWR	55		60		ns	
(referenced to RAS)							



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5.0V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		+	
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0	ku Tetali.	0		ns	21
Write command hold time	tWCH	15		15		ns	
Write command hold time (referenced to RAS)	twcR	55		60		ns	
Write command pulse width	tWP	15		15	1.0540	ns	
Write command to RAS lead time	tRWL	20	11.	20		ns	
Write command to CAS lead time	tCWL	20	25 100	20		ns	
Data-in setup time	t _{DS}	0		0		ns	22
Data-in hold time	^t DH	15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		ns	
RAS to WE delay time	tRWD	70		80		ns	21
Column address to WE delay time	t _{AWD}	35		40	over et en	ns	21
CAS to WE delay time	tCWD	20	1000	20		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	¹REF	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	16		16	ms	
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time	tCSR	10	7.75	10		ns	5
(CAS-BEFORE-RAS refresh)							
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10	1.00	ns	24
WE setup time (CAS-BEFORE-RAS refresh)	[†] WRP	10,		10		ns	24
WE hold time (WCBR test cycle)	tWTH	10	NGAN 1 43	10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		ns	24
Write inactive time	twi	10		10		ns	
	tLWAD	20	30	20	35	ns	Albana ing
Previous WRITE to column address hold time	^t AHLW	65		75		ns	
Output data hold time from column address	tAOH	5		5		ns	
Output data enable from WRITE	tow	tAA + 5		tAA + 5		ns	
Access time from last WRITE	†ALW	65		75		ns	
Column address hold time referenced to RAS HIGH	^t AH	5		10		ns	
CAS pulse width in STATIC-COLUMN mode	†csc	^t CAS		†CAS		ns	
Output data hold from WRITE	HOW!	0		0		ns	

DRAM

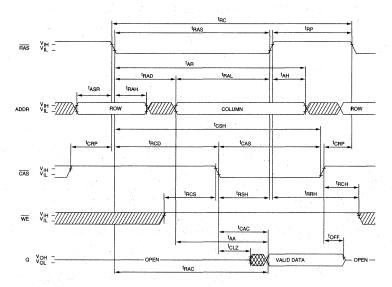
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If CAS = ViH, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.

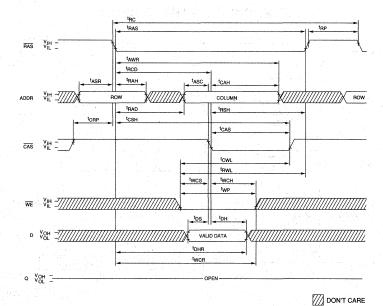
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until CAS goes back to VIH).
- These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 24. WTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.



READ CYCLE



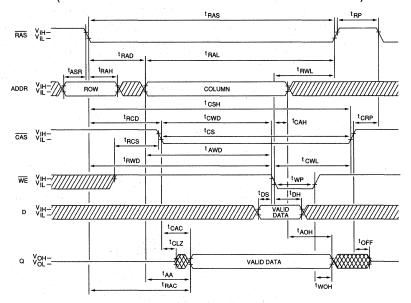
EARLY-WRITE CYCLE



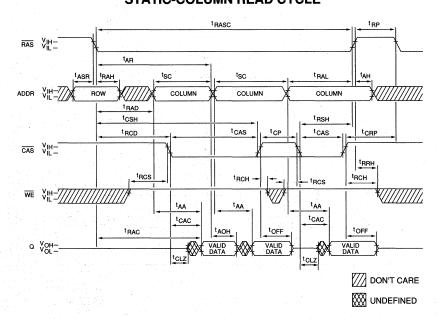
₩ UNDEFINED

DRAM

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



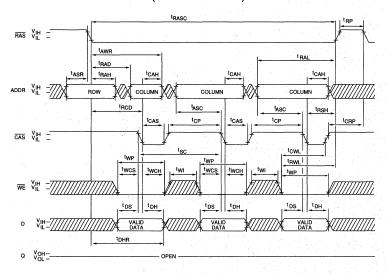
STATIC-COLUMN READ CYCLE





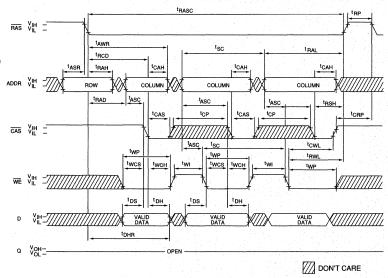
STATIC-COLUMN EARLY-WRITE CYCLE

(CAS controlled)

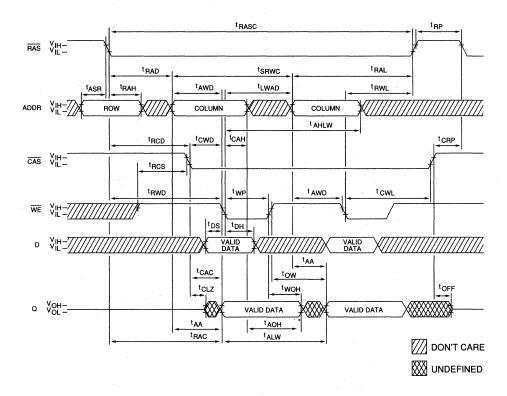


STATIC-COLUMN EARLY-WRITE CYCLE

(WE controlled)



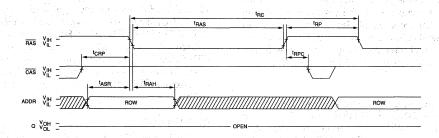
STATIC-COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





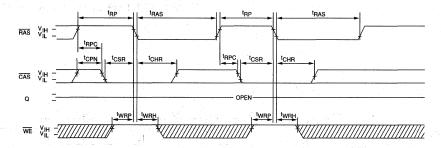
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; A10 and WE = DON'T CARE)



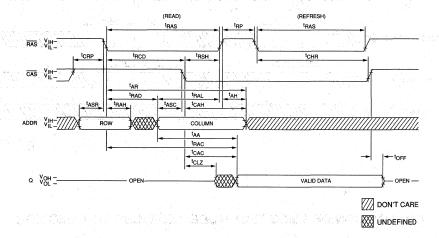
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

 $(\overline{WE} = HIGH)$



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

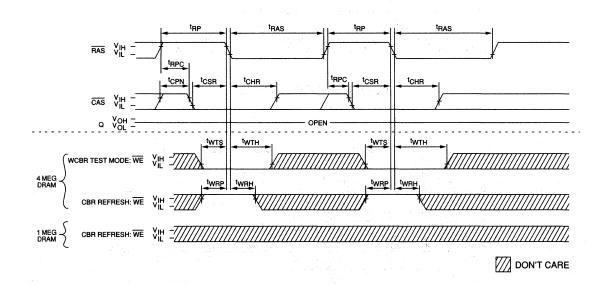
A CBR cycle with $\overline{\text{WE}}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight \overline{RAS} cycles. The 4 Meg POWER-UP is more restrictive in that eight \overline{RAS} -ONLY or CBR REFRESH (\overline{WE} held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a \overline{RAS} -ONLY or a CBR REFRESH cycle (\overline{WE} held HIGH).

SUMMARY

- The 1 Meg CBR REFRESH allows the WE pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
- The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

16 MEG x 1 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: $+5V \pm 10\%$ only or $+3.3V \pm 10\%$
- Low power, 3mW standby; 325mW active, typical (5V)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS	MARKING
• Timing 60ns access 70ns access 80ns access	-6 -7 -8
Packages Plastic SOJ (400 mil) Plastic TSOP (400 mil)	DJ TG
NOTE: Available in die form (commercial o packages. Please consult factory for die data Military Data Book.	

•	Operating Temperature, T _A
	Commercial (0°C to +70°C)

None

•	Power Supply
	+5V ±10%
	+3.3V ±10%

MT4C16M1A1 MT4LC16M1A1

GENERAL DESCRIPTION

The MT4(L)C16M1A1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. The MT4C16M1A1 and MT4LC16M1A1 are the same DRAM versions except that the MT4LC16M1A1 is a low voltage version of the MT4C16M1A1. The MT4LC16M1A1 is designed to operate in a 3.3+/-10% memory system. All further references made for the MT4C16M1A1 also apply to the MT4LC16M1A1 unless specifically stated otherwise. During READ and WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. RAS is used to latch the first 12 bits and CAS the latter 12 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE

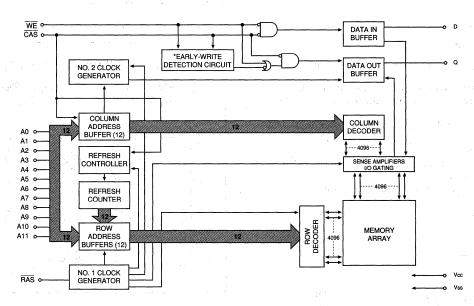
24-Pi (Q	24-Pin TSOP (R-2)			
Vcc 1 D 2 NC 3 WE 4	28 D Vss 27 D Q 26 D NC 25 D CAS	Vcc H D H NC H WE H RAS H	2 3 4	28 🖽 Vss 27 🖽 Q 26 🖽 NC 25 🖽 CAS
RAS 0 5 A11 0 6	24 D NC 23 D A9	A11 ==	·	24 PNC 23 A9
A10 1 9	20 D A8	A10 □	0	20 🗆 A8
A0 10	19 A7	A0 III	-	19 \boxplus A7
A1 11	18 A6	A1 =		18 🗆 A6
A2 c 12	17 🗅 A5	A2 □		17 ID A5
A3 🗆 13	16 🗅 A4	A3 □	13	16 🖾 A4
Vcc 🛘 14	15 D Vss	Vcc □	14	15 🎞 Vss

cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

and the state of the same	Min to History	- 17 Qu		ADDRESSES		DATA			
FUNCTION		RAS	CAS	WE	^t R	t _C	D (Data In)	Q (Data Out)	
Standby		Н	H→X	X	X	Х	Don't Care	High-Z	
READ	gradina in Ta	-3 L -35	sar E.A	Н	ROW	COL	Don't Care	Data Out	
EARLY-WRITE	3.1 (4.8 m) - 1 m	L	L	L	ROW	COL	Data In	High-Z	
READ-WRITE		L	L	H→L	ROW	COL	Data In	Data Out	
FAST-PAGE-MODE	1st Cycle	ns ##L + +	H→L	H.4.	ROW	COL	Don't Care	Data Out	
READ	2nd Cycle	L	H→L	Н	n/a	COL	Don't Care	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In	High-Z	
EARLY-WRITE	2nd Cycle	, L	H→L	L	n/a	COL	Data In	High-Z	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data In	Data Out	
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data In	Data Out	
RAS-ONLY REFRESH	V 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	a e La v	Н	Х	ROW	n/a	Don't Care	High-Z	
HIDDEN	RÉAD	L→H→L	- L'	Н	ROW	COL	Don't Care	Data Out	
REFRESH	WRITE	L→H→L	L	L	RÓW	COL	Data In	High-Z	
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	X	Х	Don't Care	High-Z	



MT4(L)C16M1A1 16 MEG x 1 DRAM

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1-1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	lı .	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

(Notes: 1, 3, 4, 6, 7) (Vcc = 3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V cc	3.0	3.6	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1-
INPUT LEAKAGE CURRENT Any input 0V ≤ Vin ≤ 3.6V (All other pins not under test = 0V)		-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -2mA)	V OH	2.4		٧	
Output Low Voltage (lout = 2mA)	Vol		0.4	٧	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)	and the second second		MAX	:]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	70	60	50	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	90	80	70	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcce	90	80	70	mA	3, 5

Notes: 1, 3, 4, 6, 7) (Vcc = 3.3V ±10%)			MAX			
PARAMETER/CONDITION	SYMBOL	-6 -7 -8		-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	400	400	400	μА	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	60	55	50	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ¹ PC = ¹ PC (MIN))	lcc4	40	35	30	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih.: ^t RC = ^t RC (MIN))	lcc5	60	55	50	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc6	60	55	50	mA	3, 5



MT4(L)C16M1A1 16 MEG x 1 DRAM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11, D	C ₁₁		5	pF	2
Input Capacitance: RAS, CAS, WE	CI2		7	pF	2
Output Capacitance: Q	Со		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13)

AC CHARACTERISTICS			-6		-7		-8		135-1-1-4
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	130		155		175		ns	100
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	60		70		75		ns	
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Access time from column address	†AA		30	11 110	35	:	40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20	1 1	ns	
RAS precharge time	†RP	40	75.14.17.1	50		60		ns	
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10	331	10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	9 F 2 5
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0	10000	0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	†RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0	1	0		0		ns	21





ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			6	-	7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	^t WP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20	100	ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	tDH	10		15		15		· ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60	i si	ns	1 1 1
RAS to WE delay time	†RWD	60		70		80		ns	21
Column address to WE delay time	^t AWD	30		35		40	A	ns	21
CAS to WE delay time	tCWD	-15		20		20		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF -	:	64		64		64	ms -	11.5
RAS to CAS precharge time	^t RPC	0		0		0		ns	1.
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15	: -1 · · ·	15	,	15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10	*	10		ns	24
WE hold time (WCBR test cycle)	¹WTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24



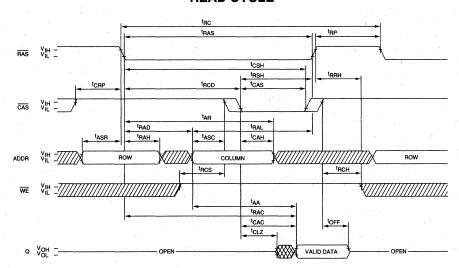
MT4(L)C16M1A1 16 MEG x 1 DRAM

NOTES

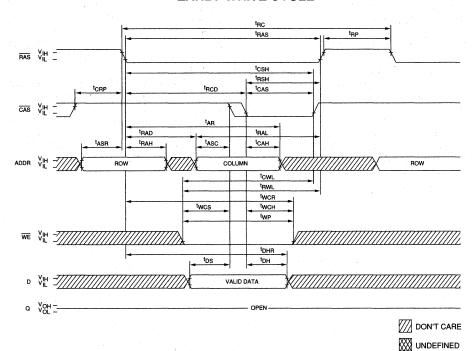
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VII and VII (or between VII and VIII) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.

- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE-WRITE and the state of data out is indeterminate (at access time and until CAS goes back to VIH).
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 24. tWTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.

READ CYCLE

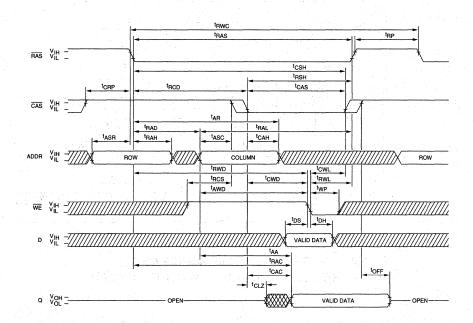


EARLY-WRITE CYCLE

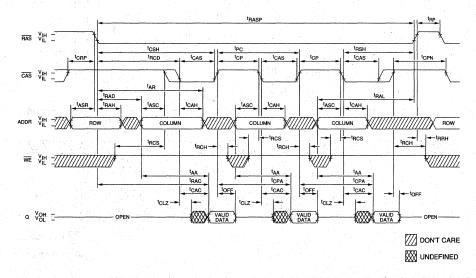




READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

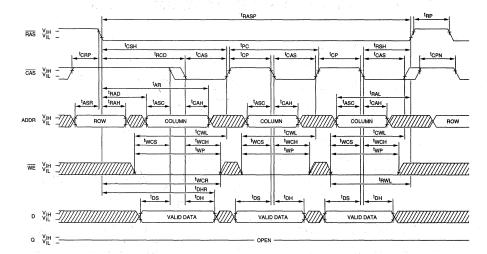


FAST-PAGE-MODE READ CYCLE

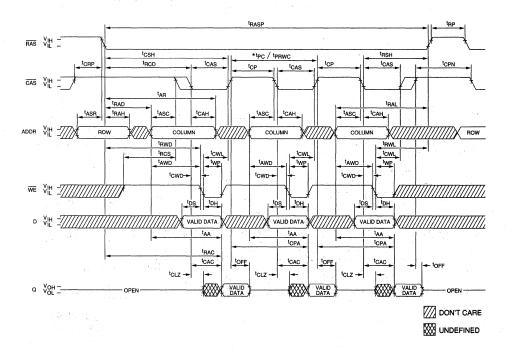


JEW **I** DRA

FAST-PAGE-MODE EARLY-WRITE CYCLE



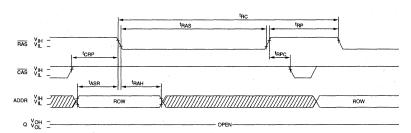
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





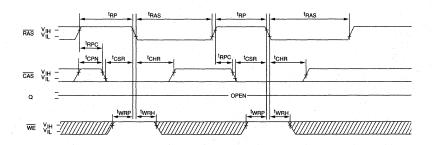
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; A11 and \overline{WE} = DON'T CARE)



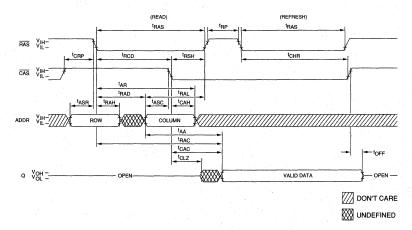
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

 $(\overline{WE} = HIGH)$



MT4(L)C16M1A1 REV. 4/92

16 MEG x 1 DRAM

STATIC COLUMN

FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 3mW standby; 330mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

MARKING OPTIONS Timing 60ns access -6 -7 70ns access 80ns access -8 Packages Plastic SOI (400 mil) DI

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

- Operating Temperature, T_A Commercial (0°C to +70°C) None
- Part Number Example: MT4C16M1D1DJ-6

GENERAL DESCRIPTION

The MT4C16M1D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. \overline{RAS} is used to latch the first 12 bits and CAS the latter 12 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS

PIN ASSIGNMENT (Top View) 24-Pin SOJ (Q-3)

Vcc D D D D D D D D D D D D D D D D D D	1 2 3 4 5	28 27 26 25 24 23	Vss Q NC CAS NC A9
71111			_ ,
A10 0 A0 0 A1 0 A2 0 A3 0 Vcc 0	9 10 11 12 13 14	19 18 17	A8 A7 A6 A5 A4 Vss

remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires CAS to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HID-DEN refresh) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.



256K x 4 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8 ·
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	, where TG is the property
Plastic ZIP (350 mil)	we have a ${f Z}$ in the liquid for

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

•	Operating Temperature, T _A	
	Commercial (0°C to +70°C)	None
	Industrial (-40°C to +85°C)	IT

GENERAL DESCRIPTION

The MT4C4256 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW orior to CAS going LOW, the output pin(s) remain open High-Z) until the next CAS cycle. If WE goes LOW after lata reaches the output pin, data out (Q) is activated and etains the selected cell data as long as CAS remains LOW regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and four data

PIN A	SSIGNI	MENI	(lob A	iew)
20-Pin	DIP		20-Pii	n ZIP

(N-2) ,				(C)-1)		
DQ1 [DQ2] WE [RAS] NC [A0 [A1 [A2]	3 18 4 17 5 16 6 15 7 14 8 13	DQ4 DQ3 CAS OE A8			OE DQ3 Vss DQ2 RAS A0 A2 Vcc A5	1 3 5 7 9 11 13 15 17	2 2 4 6 5 6 10 8 5 10 12 14 15 16 18 18	A1 A3	4
Voc F	10 11	h 🗚			~	10	= 20	A8	

20-Pin SOJ	20-Pin	n TSOP				
(Q-1)	(R-	R-1)				
DQ1 d1 26 D Vss	DQ1 cc 1	26 D Vss				
DQ2 d2 25 D DQ4	DQ2 cc 2	25 D DQ4				
WE d3 24 D DQ3	WE cc 3	24 D DQ3				
RAS d4 23 D CAS	RAS cc 4	23 D CAS				
NC d5 22 D OE	NC cc 5	22 D OE				
A0 0 9 18 A8	A0 = 9	18 m A8				
A1 0 10 17 A7	A1 = 10	17 m A7				
A2 0 11 16 A6	A2 = 11	16 m A6				
A3 0 12 15 A5	A3 = 12	15 m A5				
Vcc 0 13 14 A4	Vcc = 13	14 m A4				

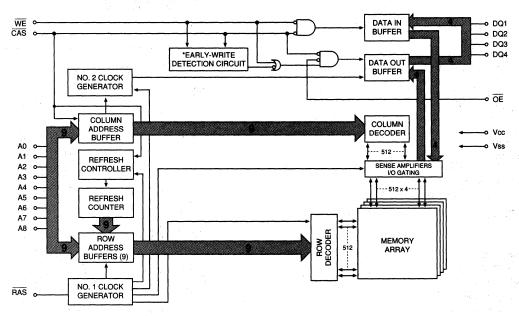
*Consult factory on availability of reverse pinout TSOP packages

outputs are routed through four pins using common I/O, and pin direction is controlled by \overline{WE} and \overline{OE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE cycle.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

	a a h	1. J. 1.				ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	OE	^t R	tC .	DQ1-DQ4
Standby		Н	H→X	Χ	Х	Х	Х	High-Z
READ	and the state of	L	ik L	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L L	∖H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	Sea Labe	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	WELL 2	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	н	X	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	(L	Н	ja L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS R	EFRESH	H→L	L	Х	Х	Х	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	1W
Short Circuit Output Current	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	in	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS	Vон	2.4		٧	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 4.2mA)	Vol		0.4	٧	

			MAX	J. 1			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	2	2	2	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	. 1	1	mA	•	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcca	90	80	70	mA	3, 4	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC (MIN))	lcc4	70	60	50	mA	3, 4	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: ¹RC = ¹RC (MIN))	lcc5	90	80	70	mA	3	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	90	80	70	mA	3, 5	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _I 1		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		.7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	. 110		130		150		ns	
READ-WRITE cycle time	†RWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90	V	95		100	ago, s	ns	
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		20		20		20	ns	15
Output Enable	^t OE		20		20		20	ns	
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	100
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	V 100	ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5	1	ns	
Row address setup time	^t ASR	0		0		0	1 2	ns	2. 14. 15.
Row address hold time	^t RAH	10		10		10	March.	ns	
RAS to column address delay time	^t RAD	15	30	15	35,	15	40	ns	18
Column address setup time	†ASC	0		0	or yearing	0		ns	100
Column address hold time	tCAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35	o produce	40		ns	
Read command setup time	tRCS	0		0		0	4.47	ns	
Read command hold time (referenced to CAS)	^t RCH	0		0	3884	0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0	fly 19 Jack	0	000 0050 03(8) 0060	ns	19
CAS to output in Low-Z	^t CLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 26
Output disable	tOD		15		20		20	ns	26
WE command setup time	tWCS	0		0		0	9.4.1.9	ns	21
Write command hold time	tWCH	10		15	1	15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	^t RWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	4.1
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		100		110		ns	21
Column address to WE delay time	tAWD	60		65		70		ns	21
CAS to WE delay time	tCWD	40		50		55		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0	1 1 1 1 1 1	0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	†ORD	0		0		0	ing grade Transport	ns	24

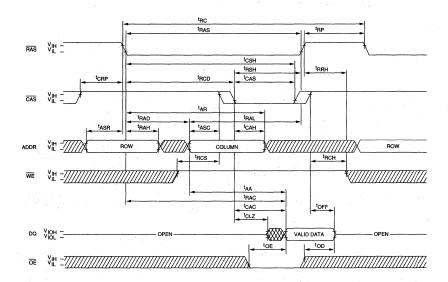
NOTES

- All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VII. (or between VII. and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD

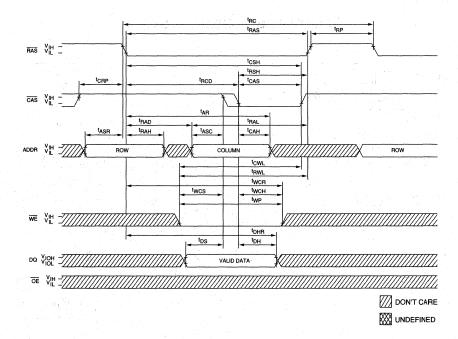
- is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to Voн or Vol.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are not restrictive operating parameters. ¹WCS applies to EARLY-WRITE cycles. ¹RWD, ¹AWD and ¹CWD apply to READ-MODIFY-WRITE cycles. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), †AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. ¹WCS, ¹RWD, ¹CWD and ¹AWD are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



READ CYCLE

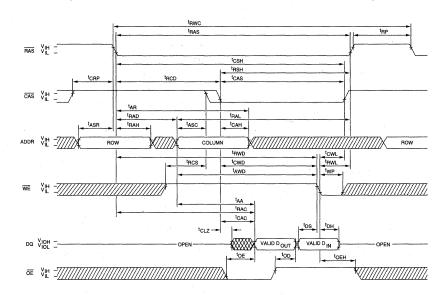


EARLY-WRITE CYCLE

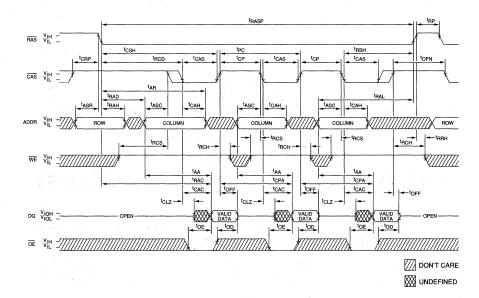




READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

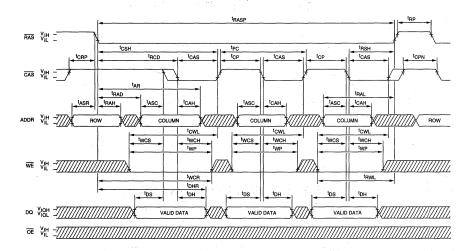


FAST-PAGE-MODE READ CYCLE

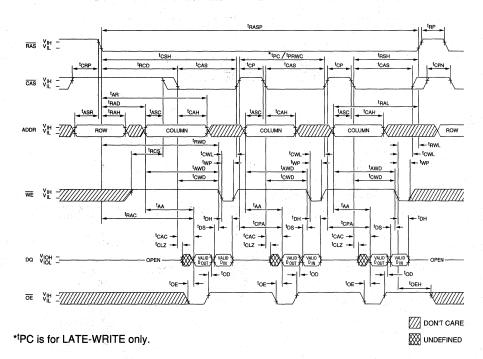




FAST-PAGE-MODE EARLY-WRITE CYCLE

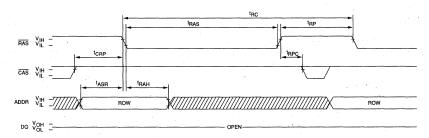


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



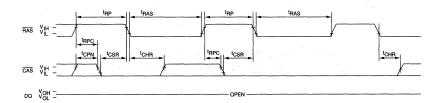
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; WE = DON'T CARE)



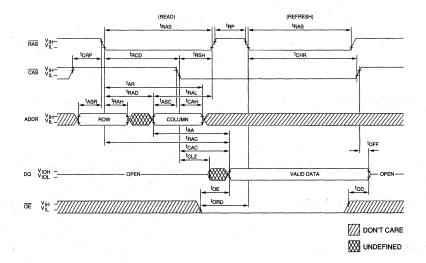
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$





256K x 4 DRAM

LOW POWER. **EXTENDED REFRESH**

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, .3mW standby; 150mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- 512-cycle extended refresh in 64ms
- Low CMOS STANDBY CURRENT, 200µA Maximum

OPTIONS MARKING Timing 70ns access 80ns access 100ns access

 Packages Plastic DIP (300 mil) Plastic SOJ (300 mil)

Plastic TSOP (300 mil)*

Plastic ZIP (350 mil)

None DI TG Z

- 7

- 8 -10

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

 Operating Temperature, T_A Commercial (0°C to +70°C) Industrial (-40°C to +85°C)

None IT

Part Number Example: MT4C4256DJ-7 L

GENERAL DESCRIPTION

The MT4C4256 L is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after

PIN ASSIGNM	IENT (Top View)
20-Pin DIP (N-2)	20-Pin ZIP (O-1)
DO1 [1 20] Vss DO2 [2 19] DO4 WE [3 18] DO3 RAS [4 17] CAS NC [5 16] OE AD [6 15] AS AT [7 14] A7 A2 [8 13] AS A3 [9 12] AS Vcc [10 11] A4	OE 1 1 2 CAS DO3 3 2 2 CAS VSS 5 2 4 DO4 VSS 5 2 6 DO1 DO2 7 2 8 WE RAS 9 1 2 10 NC A0 11 2 12 A1 Vcc 15 2 14 A3 Vcc 15 2 16 A4 A5 17 2 2 18 A6 A7 19 2 2 A8
20-Pin SOJ (Q-1)	20-Pin TSOP (R-1)
DO1 (1 26) Vss DQ2 (2 25) DQ4 WE (3 24) DQ3 RAS (4 23) CAS NC (5 22) OE	DQ1 cd 1 26 m Vss DQ2 cd 2 25 m DQ4 WE cd 3 24 m DQ3 RAS cd 4 23 m CAS NC cd 5 22 m OE
A0 0 9 18 0 A8 A1 0 10 17 0 A7 A2 0 11 16 0 A6 A3 0 12 15 0 A5 Voc 0 13 14 0 A4	A0 = 9 18 = A8 A1 = 10 17 = A7 A2 = 11 16 = A6 A3 = 12 15 = A5 Voc = 13 14 = A4

data reaches the output pin, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

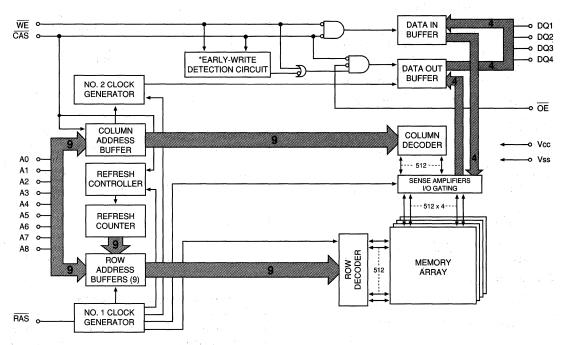
*Consult factory on availability of reverse pinout TSOP packages

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE cycle.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle

(READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR), or HIDDEN refresh) so that all 512 combinations of \overline{RAS} addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic \overline{RAS} addressing.

FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)

CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



TRUTH TABLE

			1 34 V			ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	^t C	DQ1-DQ4
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ	Lugher oxigin	L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	Н	Х	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	X	Х	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Х	Х	Х	Х	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	11
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	111	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	loc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	Icc2	200	200	200	μА	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: ^t RC = ^t RC (MIN))	lcc3	75	65	55	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	55	45	40	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	75	65	55	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC (MIN))	lcc6	75	65	60	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = [†] RAS (MIN) to 1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), [†] RC = 125µs (512 rows at 125µs = 64ms)	lcc7	200	200	200	μА	3, 5, 7, 27



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Ci1		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂	1.41	7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 5V ±10%)

AC CHARACTERISTICS PARAMETER		-7		-8		-10		1 1 1 1 1 1 1 1 1	45, 15,20,47
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	
READ-WRITE cycle time	^t RWC	185		205		245		ns	A ST
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		45		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	95		100		115		ns	
Access time from RAS	tRAC		70		80		100	ns	14
Access time from CAS	†CAC		20	100	20		25	ns	15
Output Enable	^t OE	4 5	20	1.44	20		25	ns	
Access time from column address	^t AA		35		40		50	ns	
Access time from CAS precharge	^t CPA		40		45		50	ns	40 () 44
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	Comment
RAS hold time	tRSH	20	38.55	20		25	100	ns	
RAS precharge time	tRP	50		60		70		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	9-49-100
CAS hold time	tCSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		15		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	1 4 4 5 5	ns	
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	^t CRP	5	18 18	5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		15		ns	
RAS to column address delay time	^t RAD	15	35	15	40	20	50	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		20		ns	
Column address hold time (referenced to RAS)	^t AR	55		60		70		ns	
Column address to RAS lead time	^t RAL	35		40		50		ns	
Read command setup time	†RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0	1	0		ns	



(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS	-7		-8		-10				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 26
Output disable	_tOD		20		20		20	ns	26
WE command setup time	twcs	0		0		0		ns	21
Write command hold time	†WCH	15		15		20		ns	
Write command hold time (referenced to RAS)	tWCR	55	153. in	60		75	1 48 1 7 1	ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	tRWD	100		110		130		ns	21
Column address to WE delay time	tAWD	65		70		80		ns	21
CAS to WE delay time	tCWD:	50		55		60		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	†REF		64		64		64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	20		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0	1	0		ns	24

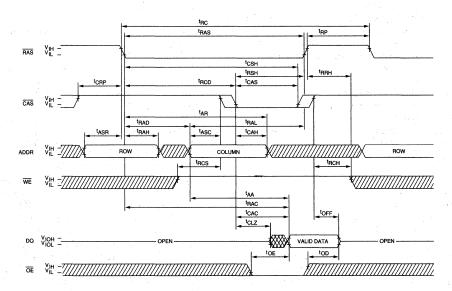


NOTES

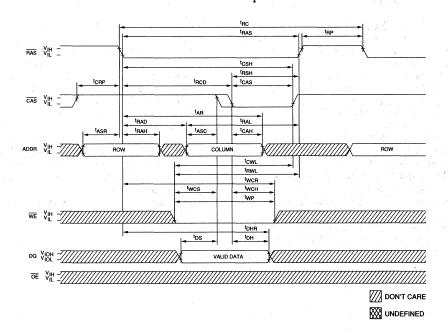
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- If CAS = Vπ, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
 - 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY-WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE-WRITE cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care," and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 27. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.

READ CYCLE

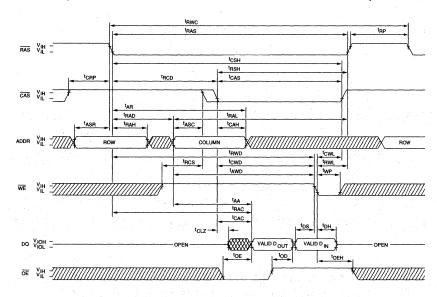


EARLY-WRITE CYCLE

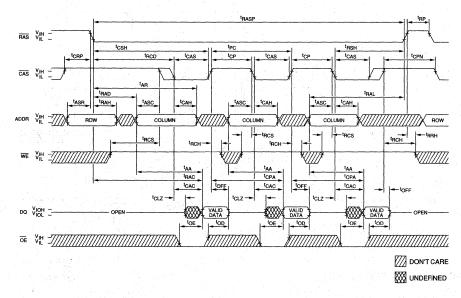




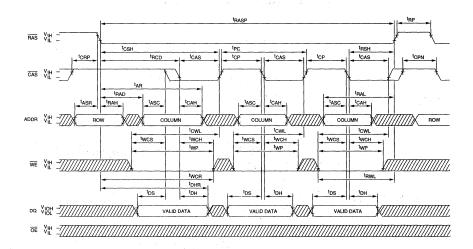
READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



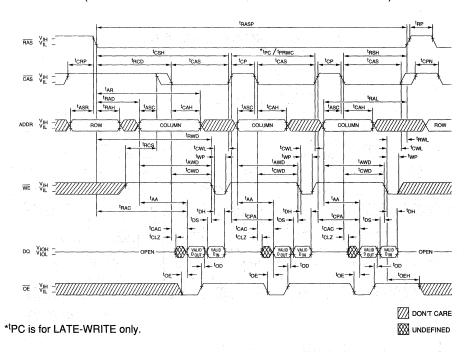
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

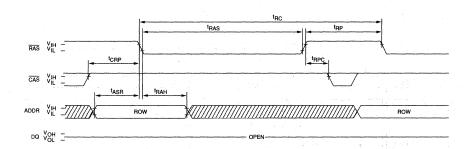


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



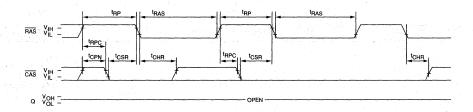


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



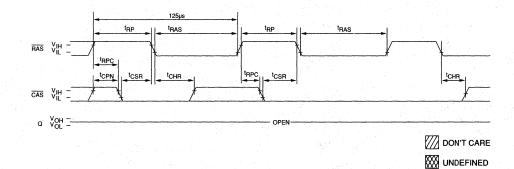
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)

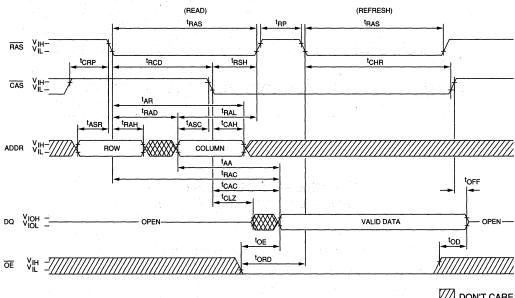


BATTERY BACKUP REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE 24 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



DON'T CARE

₩ undefined

DRAM 256k

256K x 4 DRAM

3.3V, EXTENDED REFRESH

FEATURES

- Best memory solution for 3.3V flat-panel controllers
- Single +3.3V ±5% power supply
- TSOP and SOJ compatible with 1 Meg x 4 TSOP
- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- All inputs and outputs are TTL compatible
- Optional FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Low power, 0.1mW standby; 100mW active, typical
- 512-cycle extended refresh distributed across 64ms
- Low BBU current, 60μA typical, 90μA (MAX)
- Low STANDBY CURRENT, 25μA typical, 60μA (MAX)

OPTIONS	MARKING
Timing	
100ns access	ыр ым уч ы түү - -10
120ns access	-12
Packages Plastic SOJ (300 n Plastic SOJ (300 n Plastic SOJ (300 n) Plastic SOJ (3	
Plastic TSOP (300 Plastic ZIP (350 n	mil) TG nil) Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

• Part Number Example: MT4C4256DJ-10 VL

GENERAL DESCRIPTION

The MT4C4256 VL is specially processed to operate at 3.3 volts allowing for maximum power savings. It is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ and WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pin, data out (Q) is activated and retains the selected cell data as

PIN A	SSIGNMI	ENT (Top View	')
20-Pir (Q-		20-Pin ZII (O-1)	P
DQ1 d1 DQ2 d2 WE d3 RAS d4 NC d5		DQ3 3 3 - 4 L Vss 5 - 1 - 4 L DQ2 7 1 - 8 V	OQ1 VE IC 11 3 4
	(H	-1)	
	DQ1 # 1 DQ2 # 2 WE # 3 RAS # 4 NC # 5	26 DVss 25 DQ4 24 DQ3 23 DGAS 22 DOE	
	A0 = 9 A1 = 10 A2 = 11 A3 = 12 Vcc = 13	18 □ A8 17 □ A7 16 □ A6 15 □ A5 14 □ A4	

long as \overline{CAS} remains LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by \overline{WE}

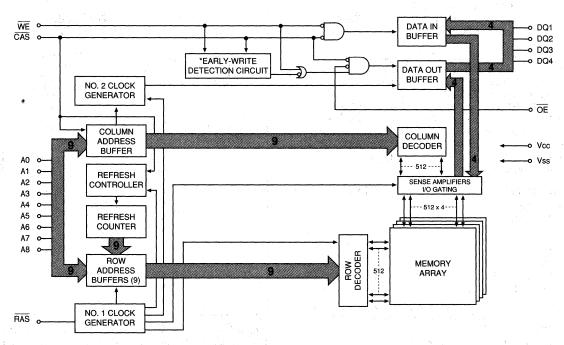
FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE cycle.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle

(READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regard-

less of sequence. The CBR and BATTERY BACKUP (BBU) refresh cycles will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



MT4C4256 VL 256K x 4 DRAM

TRUTH TABLE

					1 1 1 1	ADDRESSES		DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	tC	DQ1-DQ4
Standby		Н	H→X	Х	Χ	Χ	Х	High-Z
READ	1 4 to 4 32 W 4	L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L.	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	Ļ	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	Н	Х	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	Χ	Х	Χ	Χ	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	X	Х	Χ	Х	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vs	ss1V to +6V
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = $3.3V \pm 5\%$, $T_A = 0$ °C to 70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.15	3.45	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	. 1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 4.6V$ (All other pins not under test = $0V$)	lı	-2	2	μА	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -1mA)	Vон	2.0		V	
Output Low Voltage (lout = 2.0mA)	Vol		0.4	V	

		M	AX		
PARAMETER/CONDITION	SYMBOL	-10	-12	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	Icc1	1	1	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	60	60	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: tRC = tRC (MIN))	lcc3	40	35	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	30	25	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	40	35	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	40	35	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = †RAS (MIN) to 300ns; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQIN may be left OPEN), †RC = 125µs (512 rows at 125µs = 64ms)	lcc7	90	90	μА	3, 5, 7, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	Cı2		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 3.3V \pm 5\%$, $T_A = 0$ °C to 70°C)

AC CHARACTERISTICS		-10			-12		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC tRC	180		210		ns	
READ-WRITE cycle time	tRWC	245		255		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	55		60		ns	
FAST-PAGE-MODE READ-WRITE cycle time	[†] PRWC	115		140		ns	
Access time from RAS	^t RAC		100		120	ns	14
Access time from CAS	tCAC		30		40	ns	15
Output Enable	^t OE		25		30	ns	
Access time from column address	^t AA		50		60	ns	
Access time from CAS precharge	^t CPA	- 1	50		60	ns	
RAS pulse width	†RAS	100	100,000	120	100,000	ns	44.1.5
RAS pulse width (FAST PAGE MODE)	tRASP	100	100,000	120	100,000	ns	
RAS hold time	tRSH	25		35		ns	
RAS precharge time	t _{RP}	70		80		ns	1
CAS pulse width	†CAS	25	100,000	35	100,000	ns	
CAS hold time	tCSH	100		120		ns	
CAS precharge time	^t CPN	10		15	erfolg type	ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		15		ns	
RAS to CAS delay time	tRCD	25	75	25	90	ns	17
CAS to RAS precharge time	tCRP	5		10		ns	
Row address setup time	tASR	0		0		ns	Ş
Row address hold time	^t RAH	15		15		ns	
RAS to column address delay time	[†] RAD	20	50	20	60	ns	18
Column address setup time	†ASC	0		0		ns	
Column address hold time	^t CAH	20		25		ns	
Column address hold time (referenced to RAS)	^t AR	70		85		ns	
Column address to RAS lead time	^t RAL	50		60		ns	
Read command setup time	tRCS	0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		ns	19
CAS to output in Low-Z	tCLZ	0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = 3.3V $\pm 5\%$, T_A = 0°C to 70°C)

AC CHARACTERISTICS		-10		-1	2		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	25	0	35	ns	20, 26
Output disable	tOD.		25	6.	35	ns	26
WE command setup time	twcs	0		0		ns	21
Write command hold time	†WCH	20		25		ns	
Write command hold time (referenced to RAS)	tWCR	75		85	, 4	ns	
Write command pulse width	tWP	20		25		ns	
Write command to RAS lead time	^t RWL	25		30		ns	
Write command to CAS lead time	tCWL -	25		30		ns	- 11 - 1
Data-in setup time	tDS ·	0		0		ns	22
Data-in hold time	tDH .	20		25		ns	22
Data-in hold time (referenced to RAS)	^t DHR	75		90		ns	
RAS to WE delay time	^t RWD	130		160		ns	21
Column address to WE delay time	^t AWD	80		100		ns	21
CAS to WE delay time	tCWD	60		75		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF.		64		64	ms	
RAS to CAS precharge time	tRPC	0		0 5		ns	1 1
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	[†] CHR	20		20		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		ns	24

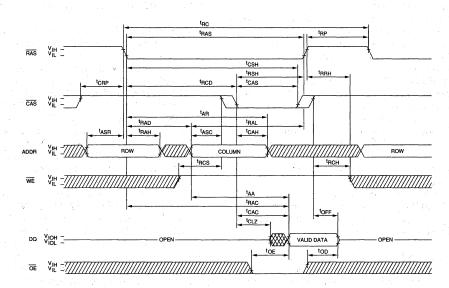
MT4C4256 VL 256K x 4 DRAM

NOTES

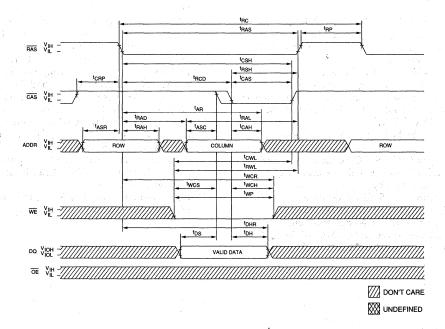
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If CAS = Vін, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 500F
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are not restrictive operating parameters. ¹WCS applies to EARLY-WRITE cycles. ¹RWD, ¹AWD and ¹CWD apply to READ-MODIFY-WRITE cycles. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. ¹WCS, ¹RWD, ¹CWD and ¹AWD are not applicable in a LATE-WRITE cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care," and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.

READ CYCLE

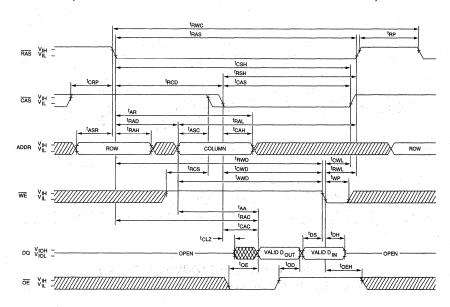


EARLY-WRITE CYCLE

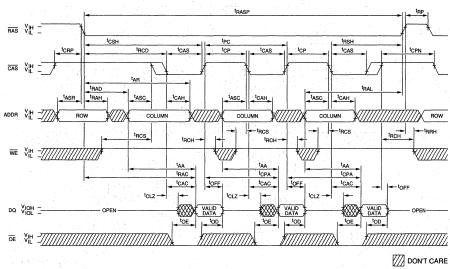




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

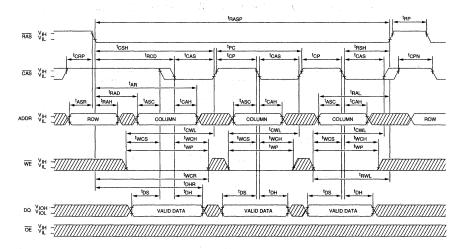


FAST-PAGE-MODE READ CYCLE

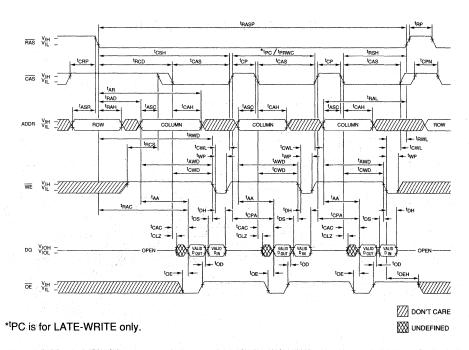




FAST-PAGE-MODE EARLY-WRITE CYCLE

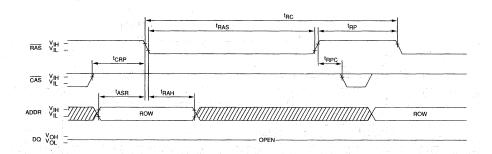


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



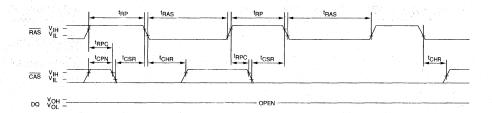


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



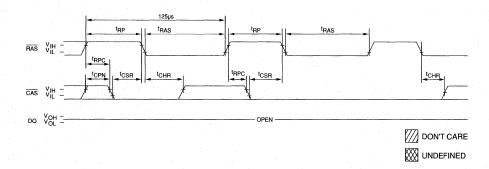
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)

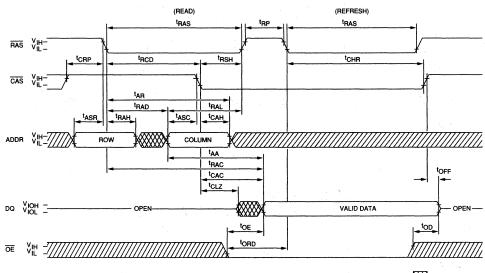


BATTERY BACKUP REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE 24 (WE = HIGH; OE = LOW)





DRAM

256K x 4 DRAM

STATIC COLUMN

FEATURES

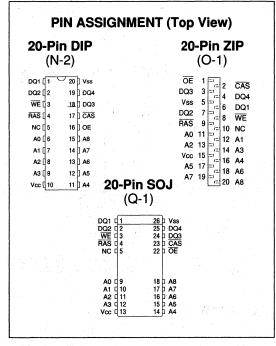
- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 512-cycle refresh in 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional STATIC COLUMN access cycle

OPTIONS	MARKING
Timing	
70ns access	- 7 (基準)
80ns access	- 8
100ns access	-10
• Packages	
Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic ZIP (350 mil)	\mathbf{z}

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

GENERAL DESCRIPTION

The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WEinput. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by \overline{WE} and \overline{OE} .

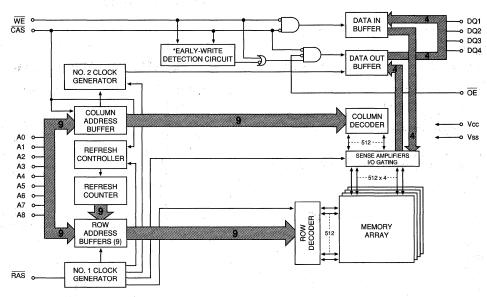


STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires \overline{CAS} to be toggled for each successive page-mode access, the STATIC COLUMN part allows \overline{CAS} to be left LOW for successive STATIC COLUMN accesses. Returning \overline{RAS} HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.



FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	^t C	DQ1-DQ4
Standby	1 20 1	Н	H→X	Х	X	Х	Х	High-Z
READ		- College	L	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE	V. S. S. S. M. S. S.	. L	L	H→L	L→H	ROW	COL	Data Out, Data In
STATIC COLUMN	1st Cycle	R HL V	r3 o L °	H	L	ROW	COL	Data Out
READ	2nd Cycle	L	L	Н	L	n/a	COL	Data Out
STATIC COLUMN	1st Cycle	i L	, L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	eg Late	44.4 L 5	H→L	Х	n/a	COL	Data In
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		Z . Lps	. H	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	A. L.	Х	Х	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under." Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	11	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Voн	2.4		V	
Output Low Voltage (IouT = 4.2mA)	Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL, CAS, Address Cycling: 'SC = 'SC (MIN))	lcc4	60	50	40	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ¹RC = ¹RC (MIN))	lcc5	80	70	60	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	80	70	60	mA	3, 5

CAPACITANCE

PARAMETER	124 - 127 - 124	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8		CI1		5	pF	2
Input Capacitance: RAS, CAS, WE, OE		C ₁₂		7	pF	2
Input/Output Capacitance: DQ		Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-7		-8	-	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		180		ns	43.45
READ-WRITE cycle time	tRWC	185		205		245		ns	
STATIC-COLUMN READ or WRITE	tSC	40		45		55		ns	
cycle time						#		174	
STATIC-COLUMN READ-WRITE	tSRWC	100		110		135		ns	
cycle time									
Access time from RAS	†RAC		70		80	9 E C	100	ns	14
Access time from CAS	^t CAC		20	154	20	1.81	25	ns	15
Output Enable	^t OE		20		20		25	ns	
Access time from column address	†AA		35		40	2.50	50	ns	
RAS pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (STATIC COLUMN)	tRASC	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		20		25		ns	
RAS precharge time	tRP	50		60		70		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	^t CSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		15		ns	16
CAS precharge time (STATIC COLUMN)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	tCRP	5		5.		5	N 197	ns	
Row address setup time	tASR .	0		0		0		ns	
Row address hold time	tRAH .	10		10		15	10.14	ns	
RAS to column address delay time	^t RAD	15	35	15	40	20	50	ns	18
Column address setup time	†ASC	0		0		0	5, 1 - 5	ns	
Column address hold time	^t CAH	15		15	1000	20	200	ns	
Column address hold time (referenced to RAS)	^t AR	80		90	, e syê ji bû.	100	11,1114	ns	
Column address to RAS lead time	^t RAL	35		40	Salasia.	50		ns	
Read command setup time	†RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0	1,939	0	N. C.	ns	-19
Read command hold time (referenced to RAS)	^t RRH	0		0		0	# 1	ns	19
CAS to output in Low-Z	tCLZ	0		0	1125, THV	0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		+	-7		-8		0		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 26
Output disable	tOD	. 137No - 1	20		20		20	ns	26
Column address hold time EARLY-WRITE (referenced to RAS)	^t AWR		55) (1816)	60		70	ns	A.
WE command setup time	twcs	0		0	er individual	0	41 15 27	ns	21
Write command hold time	tWCH	15		15		20		ns	1.34
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15	y (70.10.2)	20	197, 1	ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25	- 14.4 E	ns	
Data-in setup time	†DS	0		0		0	11.47.1.11.	ns	22
Data-in hold time	^t DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	tRWD	100		110		130		ns	21
Column address to WE delay time	^t AWD	65		70		80		ns	21
CAS to WE delay time	tCWD	50		55	- (1)	60		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15	Tartey Life Named No.	15		ns	5
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	20		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	24
Write inactive time	tWI	10		10	11 17 24 14	10	1. 2. 4.	ns	1.5
Previous WRITE to column address delay time	^t LWAD	20	30	20	35	25	45	ns	
Previous WRITE to column address hold time	^t AHLW	65		75		95		ns	
RAS hold time referenced to OE	^t ROH	10		10	128 457	10	1000	ns	esta , sa
Output data hold time from column address	^t AOH	5		5		5	C SAV	ns	
Output data enable from WRITE	tOW	tAA + 5		tAA+5		tAA + 5	7	ns	ALC: U
Access time from last WRITE	tALW	65		75	*	95		ns	
Column address hold time referenced to RAS HIGH	tAH .	5		5	s :	10		ns	
CAS pulse width in STATIC-COLUMN mode	tcsc	†CAS		†CAS		†CAS		ns	

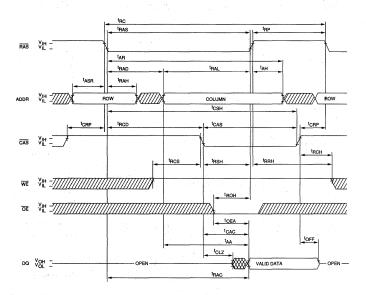
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is High-Z.
- 12. If CAS = Vπ, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (max) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD

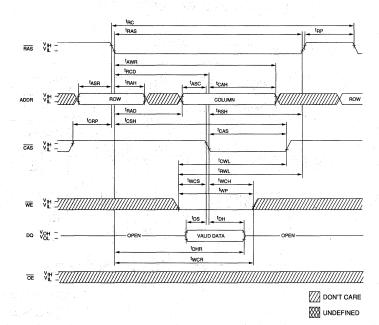
- is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY-WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If ^tWCS ≥ ^tWCS (MiN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE-WRITE cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If \overline{OE} is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a don't care. If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



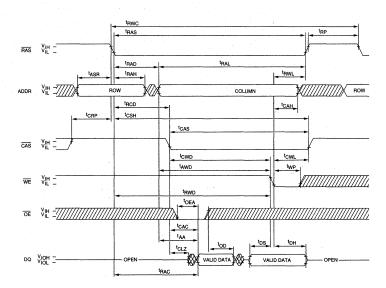
READ CYCLE



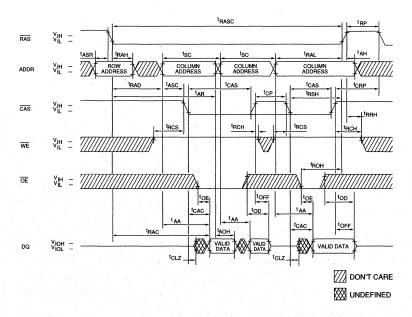
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



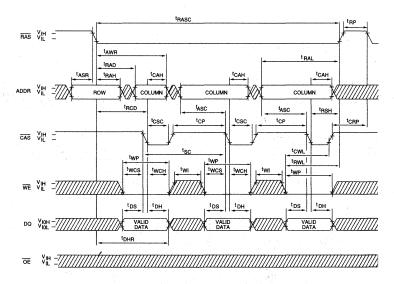
STATIC-COLUMN READ CYCLE



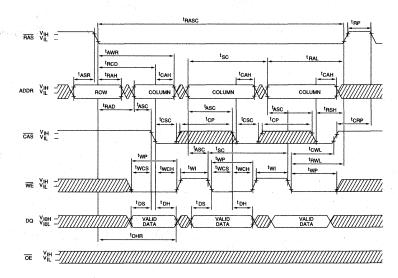


STATIC-COLUMN EARLY-WRITE CYCLE

(CAS controlled)



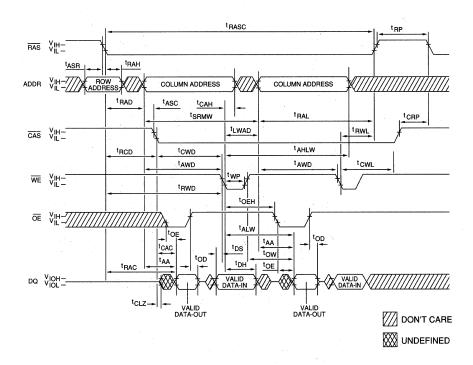
STATIC-COLUMN EARLY-WRITE CYCLE (WE controlled)





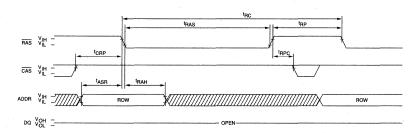


STATIC-COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



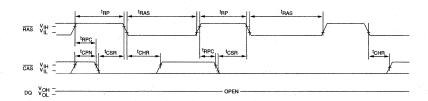


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



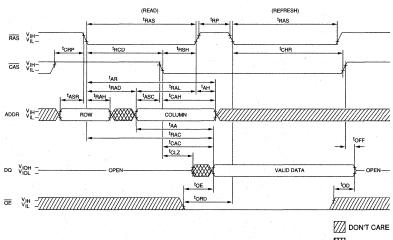
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

1 MEG x 4 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycle

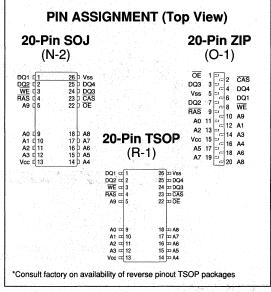
OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's *Military Data Book*.

- Operating Temperature, T_A
 Commercial (0°C to +70°C)
 Industrial (-40°C to +85°C)
 IT
- Part Number Example: MT4C4001JDJ-6

GENERAL DESCRIPTION

The MT4C4001J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ and WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pin(s), The Qs are activated and retain the selected cell data as long as \overline{CAS} remains low

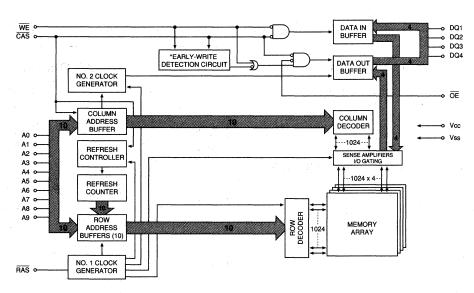


(regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR) or HIDDEN refresh) so that all 1,024 combinations of \overline{RAS} addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic \overline{RAS} addressing.

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

	× - × -		1 34			ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	, ·tR	tC t	DQ1-DQ4
Standby		Н	H→X	Х	Х	Х	X	High-Z
READ		L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE	god kolkka	.,L	L	L	Х	ROW	COL	Data In
READ-WRITE	MAGE	L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L L	, H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRES	H	L	Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H. H.	Tay L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	TO Face	L	X	ROW	COL	Data In
CAS-BEFORE-RAS	REFRESH	H→L	Y L	Н	Х	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	li li	-2	2	μΑ	11.5
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4	i a	V	
Output Low Voltage (IouT = 4.2mA)	Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC (MIN))	lcc4	80	70	60	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	110	100	90	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcce	110	100	90	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	, Ci1		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	145		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Output Enable	†OE		15		20		20	ns	23
Access time from column address	tAA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60	1	ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	¹ CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	41 1 5
Column address hold time	^t CAH	10		15		15	Tak Silv	ns	1.00
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0	100	ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		again to	-6	-	7		-8	1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0		0		0		ns	21, 27
Write command hold time	†WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	^t RWL	15		20		20		ns	The Election
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	t _{DS}	0		0		0		ns	22
Data-in hold time	^t DH	10		15		15	1	ns	22
Data-in hold time (referenced to RAS)	†DHR	45		55		60	la part	ns	
RAS to WE delay time	†RWD	85	†	100		110		ns	21
Column address to WE delay time	^t AWD	60		65	The second second	70		ns	21
CAS to WE delay time	tCWD	ં45		50		50	T	ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^t REF		16		16		16	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10	y ni iliya	ns 🎸	25, 28
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10	1 22-3	ns	25, 28
WE hold time (WCBR test cycle)	™TH	10		10		10		ns	25, 28
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25, 28
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0	17.14 1 - 18.71	0		ns	
Output disable	tOD		15		20		20	ns	27
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		20		20		ns	26

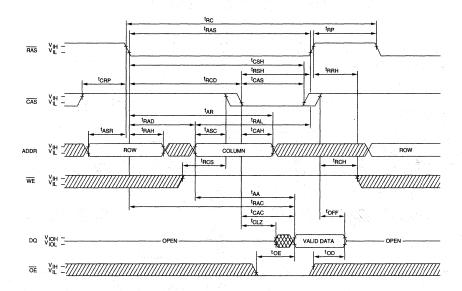
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

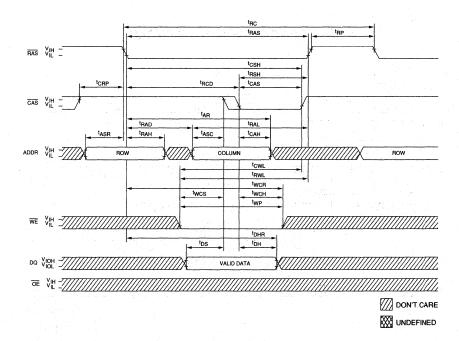
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY-WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 28. JEDEC test version only.



READ CYCLE

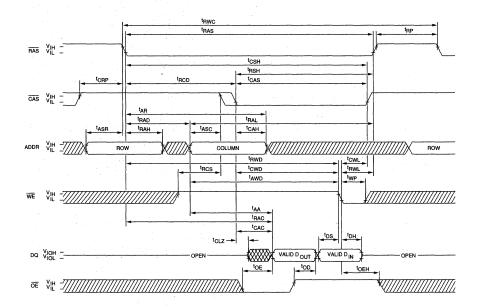


EARLY-WRITE CYCLE

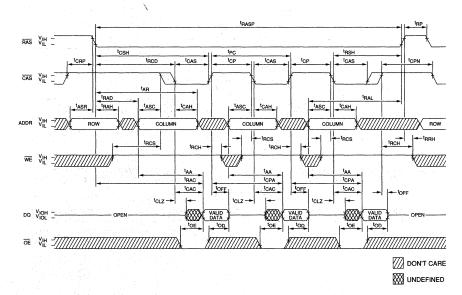




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

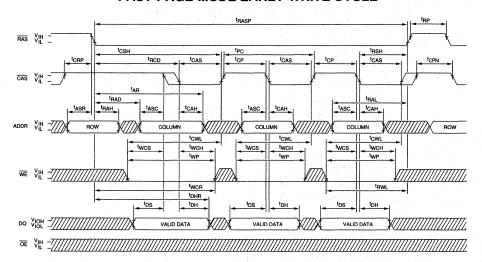


FAST-PAGE-MODE READ CYCLE

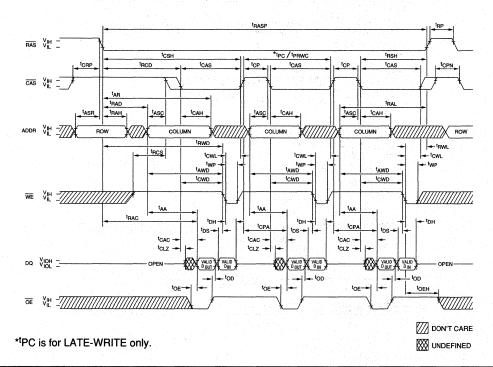




FAST-PAGE-MODE EARLY-WRITE CYCLE

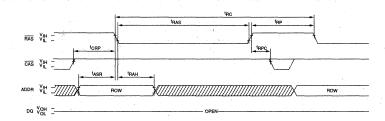


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



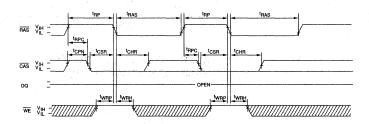


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



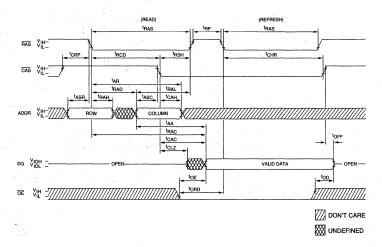
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$





4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

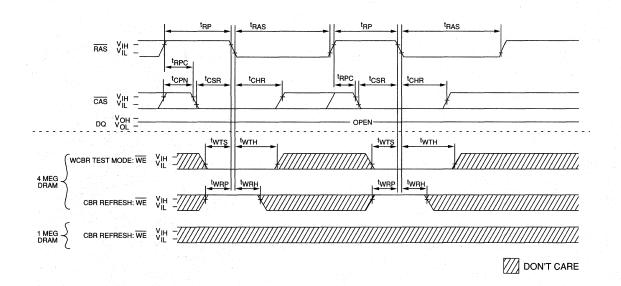
A CBR cycle with WE LOW will put the 4 Meg into the IEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight \overline{RAS} cycles. The 4 Meg POWER-UP is more restrictive in that eight \overline{RAS} -ONLY or CBR REFRESH (\overline{WE} held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a \overline{RAS} -ONLY or a CBR REFRESH cycle (\overline{WE} held HIGH).

SUMMARY

- 1. The 1 Meg CBR REFRESH allows the $\overline{\text{WE}}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{\text{WE}}$ to be HICH
- 2. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

1 MEG x 4 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- 1,024-cycle extended refresh distributed across 128ms
- · Low power, 1mW standby; 225mW active, typical

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
80ns access	-8
Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (350 mil)	Z

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

Part Number Example: MT4C4001JDJ-6 L

GENERAL DESCRIPTION

The MT4C4001J L is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates $READ mode while a logic LOW on \overline{WE} dictates WRITE mode. \\$ During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output pins, the outputs (Qs) are activated and retain the selected cell data as long as CAS remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by \overline{WE} and \overline{OE} .

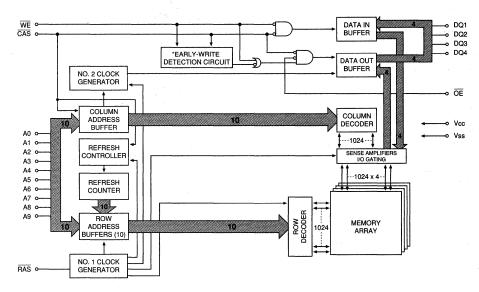
	Pin SOJ (N-2)	20-Pin ZII (O-1)	•
DQ1 d1 DQ2 d2 WE d3 RAS d4 A9 d5	26 J Vss 25 J DO4 24 J DO3 23 J CAS 22 J OE 18 J A8 17 J A7 16 J A6 15 J A5	OE 1 = 2 CA DQ3 3 = 2 CA Vss 5 = 2 GA DQ2 7 = 6 DQ RAS 9 = 12 A A0 11 = 12 A Vcc 15 = 14 A3 A5 17 = 18 A6 A7 19 = 2 0 A8)4)1
		1 TSOP (-1)	
	DQ1 == 1 DQ2 == 2 WE == 3 RAS == 4 A9 == 5	26 TO Vss 25 TO DQ4 24 TO DQ3 23 TO GAS 22 TO OE	
	A0 = 9 A1 = 10 A2 = 11 A3 = 12 Vcc = 13	18 ™ A8 17 ™ A7 16 ™ A6 15 ™ A5 14 ™ A4	

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), BATTERY BACKUP or HIDDEN refresh) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.



FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)

CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	tC	DQ1-DQ4
Standby		Н	H→X	Х	Х	X	Х	High-Z
READ		L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE		Г	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	Н	Х	Χ	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L.	Н	Χ	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:continuous_problem} \begin{tabular}{lll} Voltage on Any Pin Relative to Vss $$\dots$$ -1V to +7V \\ Operating Temperature, T_A (Ambient) $$\dots$$ 0°C to +70°C \\ Storage Temperature (Plastic) $$\dots$$ -55°C to +150°C \\ Power Dissipation $$\dots$$ 1W \\ Short Circuit Output Current $$\dots$$ 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1 1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	i i	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		٧	
Output Low Voltage (lout = 4.2mA)	Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = \text{Other Inputs} = \text{Vcc -0.2V})$	lcc2	200	200	200	μА	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	110	100	90	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	80	70	60	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	110	100	90	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc6	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE = Vcc -0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	300	300	300	μА	3, 5, 7, 28



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cii		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Cio		7	рĖ	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	-	7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	145		185	V.0	205		ns	10 12 1
FAST-PAGE-MODE	^t PC	40		40		45		ns	
READ or WRITE cycle time					1				
FAST-PAGE-MODE	^t PRWC	90		95		100		ns	
READ-WRITE cycle time			1		1				
Access time from RAS	†RAC		60		70		. 80	ns	14
Access time from CAS	^t CAC		15		20	-	20	ns	15
Output Enable	^t OE		15		20		20	ns	23
Access time from column address	t _{AA}		30		35	,	40	ns	
Access time from CAS precharge	^t CPA		35		40	7	45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17.
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10	1	10		ns	
RAS to column	^t RAD	15	30	15	35	15	40	ns	18
address delay time									
Column address setup time	†ASC	0		0		0		ns	12.5
Column address hold time	^t CAH	10		15		15		ns	1.5,0
Column address hold time	^t AR	50		55		60	1 1 1 1 1 1 1	ns	de Ma
(referenced to RAS)				1.1			14.14.14.1		nga jaka
Column address to	†RAL	30		35		40		ns	
RAS lead time				11.3					6.2780
Read command setup time	†RCS	0		0		0	135	ns	1.34.4.4
Read command hold time	^t RCH	0		0		0	1. 17 1. 4	ns	19
(referenced to CAS)				32					
Read command hold time	^t RRH	0		0	8.0	0		ns	19
(referenced to RAS)	-		Harris A	seld of					
CAS to output in Low-Z	†CLZ	0		0		0		ns	Terretti.
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	-7			-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0		0		0	1	ns	21, 27
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10.		15	1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1	15		ns	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Write command to RAS lead time	tRWL	15		20		20	12.5	ns	11 Table 1
Write command to CAS lead time	tCWL	15		20		20		ns	Baring R.
Data-in setup time	t _{DS}	0		0	1000	0		ns	22
Data-in hold time	tDH.	10		15	- 2 j.	15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	90		100		110		ns	21
Column address to WE delay time	^t AWD	60		65		70		ns	21
CAS to WE delay time	tCWD	45		50		50		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (1024 cycles)	†REF		128		128		128	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	10		ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD	Jaky H.A.	15		20		20	ns	27
OE hold time from WE during READ-MODIFY-WRITE cycle	†OEH	15		20		20		ns	26

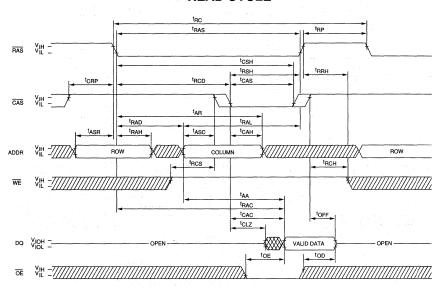
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for CPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

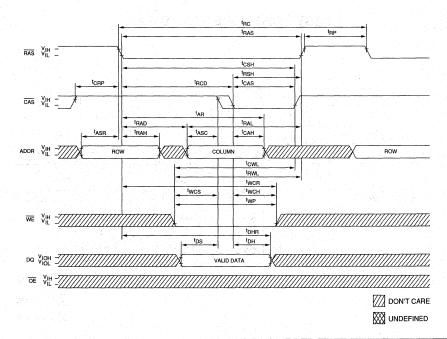
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY-WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 28. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.



READ CYCLE

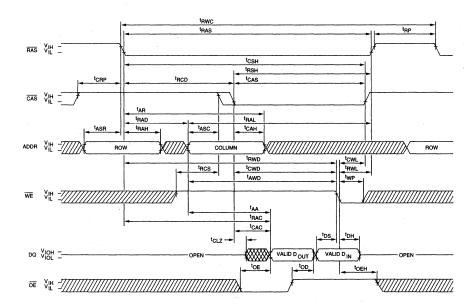


EARLY-WRITE CYCLE

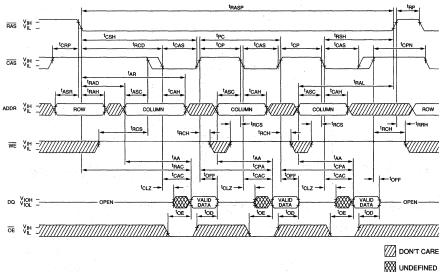




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

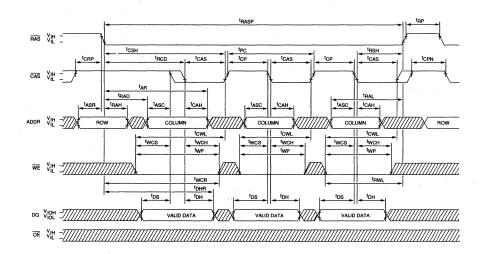


FAST-PAGE-MODE READ CYCLE

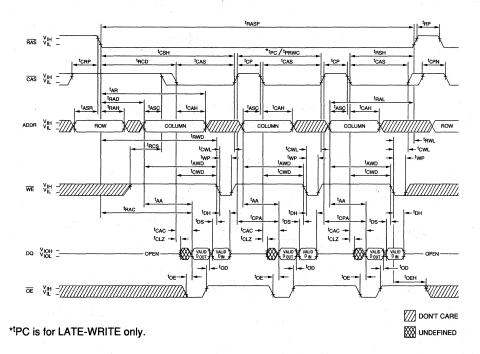




FAST-PAGE-MODE EARLY-WRITE CYCLE

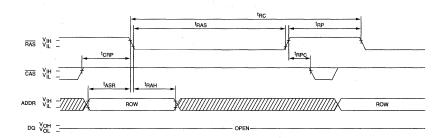


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



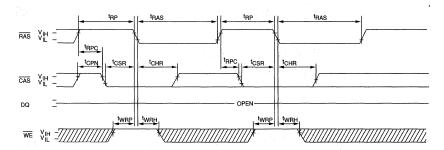


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



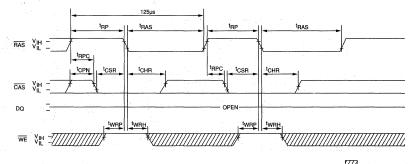
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



BATTERY BACKUP REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)

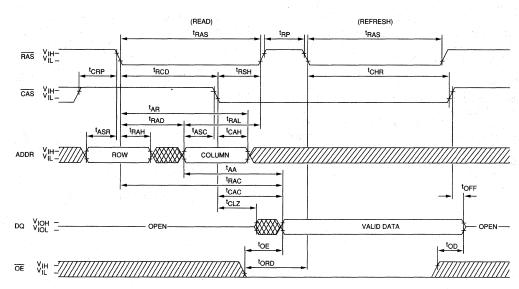


DON'T CARE





HIDDEN REFRESH CYCLE ²⁴ (WE = HIGH; OE = LOW)



DON'T CARE

₩ undefined

4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

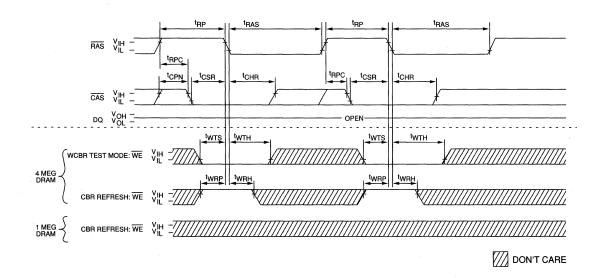
A CBR cycle with $\overline{\text{WE}}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100 μ s delay followed by any eight RAS cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS-ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a RAS-ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

- 1. The 1 Meg CBR REFRESH allows the $\overline{\text{WE}}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{\text{WE}}$ to be HIGH.
- The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

1 MEG x 4 DRAM

STATIC COLUMN

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), and HIDDEN
- STATIC COLUMN access cycle

OPTIONS	M	ARKING
 Timing 		
70ns access	The service of the service of	-7
80ns access		-8
• Packages		
Plastic SOJ (300	mil)	DJ
Plastic ZIP (350) mil)	Z
		military) or military ceran

• Part Number Example: MT4C4003JDJ-7

GENERAL DESCRIPTION

Military Data Book.

The MT4C4003J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

М	N A	221	лN.	MEN	н (ıop	vie	W)
α	D:	00				α	n:	715

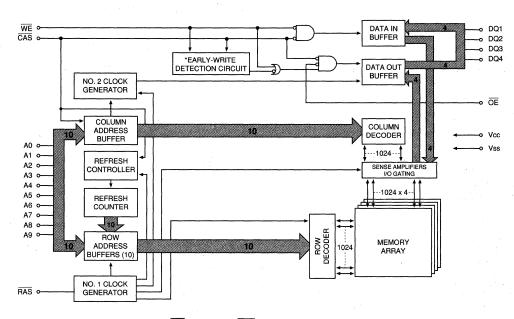
20-Pin SOJ 20-Pin ZIP (O-1)

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first read, any column address transition will result in new data out. Unlike the page-mode part, which requires \overline{CAS} to be toggled for each successive page-mode access, the STATIC COLUMN part allows \overline{CAS} to be left low for successive STATIC COLUMN accesses. Returning \overline{RAS} HIGH terminates the STATIC COLUMN operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR) or HIDDEN refresh) so that all 1,024 combinations of \overline{RAS} addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic \overline{RAS} addressing.



FUNCTIONAL BLOCK DIAGRAM STATIC COLUMN



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	ŌE	^t R	tC	DQ1-DQ4
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ		- 'E :	L	Н	.a.L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	A. L.	L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	je L "⊸	L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	Х	. X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	X	Х	Χ,	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	
Power Dissipation	
Short Circuit Output Current	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ 6.5V (All other pins not under test = 0V)	lı,	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	٧	

		M	IAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	1	1	mA		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	100	90	mA	3, 4	
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = V _I L, CAS, Address Cycling: [†] SC = [†] SC (MIN))	lcc4	70	60	mA	3, 4	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: tRC = tRC (MIN))	lcc5	100	90	mA	3	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc6	100	90	mA	3, 5	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	Cı2		-7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5.V \pm 10\%$)

AC CHARACTERISTICS			-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		150		ns	
READ-WRITE cycle time	^t RWC	185		205		ns	
STATIC-COLUMN	tSC	40		45		ns	
READ or WRITE cycle time	ľ		1				
STATIC-COLUMN	tSRWC	100		110		ns	
READ-WRITE cycle time	1 1				4,		
Access time from RAS	^t RAC		70		80	ns	14
Access time from CAS	^t CAC		20		20	ns	15
Output Enable	^t OE		20		20	ns	23
Access time from column address	†AA		35		40	ns	
RAS pulse width	tRAS	70	100,000	80	100,000	ns	4
RAS pulse width (STATIC COLUMN)	†RASC	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		ns	
RAS precharge time	^t RP	50		60		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	70		80		ns	
CAS precharge time	tCPN	10		10		ns	16
CAS precharge time (STATIC COLUMN)	^t CP	10		10		ns	
RAS to CAS delay time	tRCD	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	10		10		ns	
Row address setup time	tASR	0		0	4.45	ns	
Row address hold time	^t RAH	10		10		ns	
RAS to column	tRAD	15	35	15	40	ns	18
address delay time							
Column address setup time	†ASC	0		0		ns	
Column address hold time	^t CAH	15		. 15		ns	
Column address hold time	†AR	75		85		ns	,
(referenced to RAS)							satti i bil
Column address to	†RAL	35		40		ns	
RAS lead time					The state of		
Read command setup time	tRCS	0		0		ns	
Read command hold time	tRCH	0		0	1.5	ns	19
(referenced to CAS)					1 1 1 1		127 1
Read command hold time	tRRH	0		0		ns	19
(referenced to RAS)			1 100		- Jan 198	1 1 1	
CAS to output in Low-Z	tCLZ	0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	ns	20
Column address hold time	tAWR	55		60		ns	
(referenced to RAS)		<u> 4. j.</u>					
WE command setup time	twcs	0		0		ns	21, 27
Write command hold time	tWCH	15		15		ns	
Write command hold time	tWCR	55		60		ns	with spiriture
(referenced to RAS)							
Write command pulse width	tWP	15		15	100	ns	
Write command to RAS lead time	†RWL	20		20	1	ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-7			8 .		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command to CAS lead time	tCWL	20	5.57	20		ns	
Data-in setup time	tDS	0		0		ns	22
Data-in hold time	^t DH	15		15		ns	22
Data-in hold time	^t DHR	55		60		ns	
(referenced to RAS)							N - 1
RAS to WE delay time	tRWD	100		110	Marinetting.	ns	21
Column address	tAWD	65		70	1.3	ns	21
to WE delay time		1.00		Mark Color			11 A 1211
CAS to WE delay time	tCMD	50	1 Kalin	50		ns	21
Transition time (rise or fall)	T [†]	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16		16	ms	
RAS to CAS precharge time	tRPC	0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		ns	25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10	. y ¥ 4.	10		ns	25
WE hold time (WCBR test cycle)	tWTH.	10	Jan Jest	10		ns	25
WE setup time (WCBR test cycle)	twts	10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	†ORD	0		0	yan yang Sanggala	ns	
Output disable	tOD		20		20	ns	27
OE hold time from WE during READ-MODIFY-WRITE cycle	†OEH	20		20		ns	26
Write inactive time	tWI	10		10		ns	
Previous WRITE to column address delay time	tLWAD	20	30	20	35	ns	
Previous WRITE to column address hold time	tAHLW	65		75		ns	
RAS hold time referenced to OE	†ROH	10	September 1	10	Selection 1	ns	Array Prince
Output data hold time from column address	tAOH	5		5		ns	
Output data enable from WRITE	tow	tAA + 5		tAA + 5		ns	
Access time from last WRITE	†ALW	65		75		ns	
Column address hold time referenced to RAS HIGH	†AH	5		10		ns	
CAS pulse width in STATIC-COLUMN mode	tcsc	^t CAS		tCAS		ns	

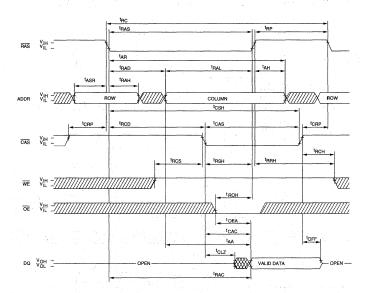
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $CAS = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

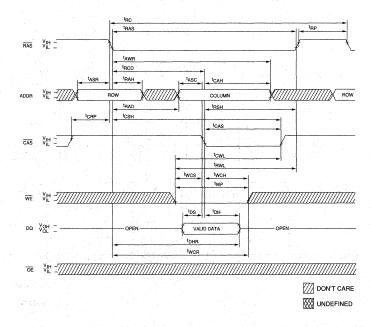
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY-WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit through out the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. WTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 27. The DQs open during READ cycles once ^tOD or ^tOFF occur. If \overline{CAS} goes HIGH first, \overline{OE} becomes a "don't care." If \overline{OE} goes HIGH and \overline{CAS} stays LOW, \overline{OE} is not a "don't care;" and the DQs will provide the previously read data if \overline{OE} is taken back LOW (while \overline{CAS} remains LOW).



READ CYCLE

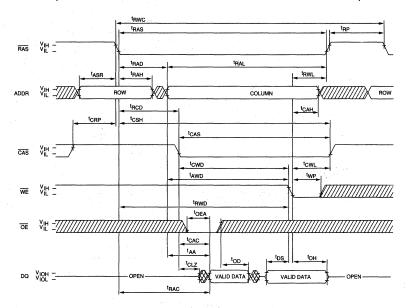


EARLY-WRITE CYCLE

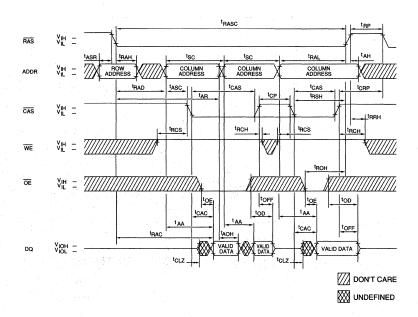




READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

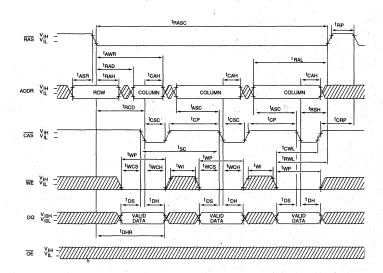


STATIC-COLUMN READ CYCLE

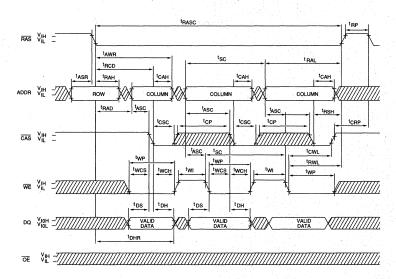




STATIC-COLUMN EARLY-WRITE CYCLE (CAS Controlled)



STATIC-COLUMN EARLY-WRITE CYCLE (WE Controlled)

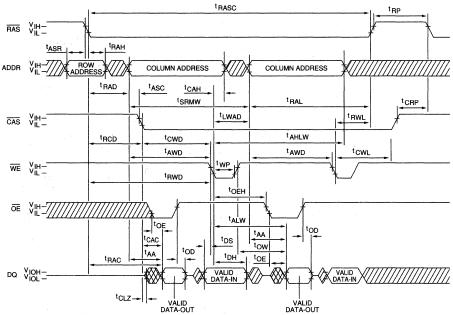


DON'T CARE





STATIC-COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

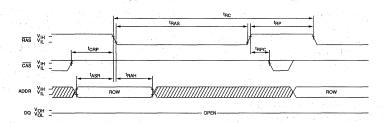


DON'T CARE

₩ undefined

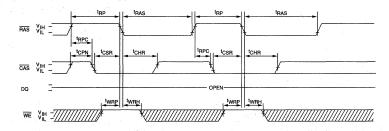


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



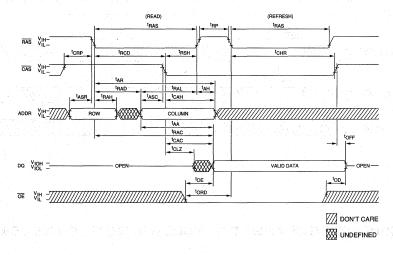
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR (CAS-BEFORE-RAS) REFRESH cycle. The CBR for the 1 Meg specifies the WE pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level.

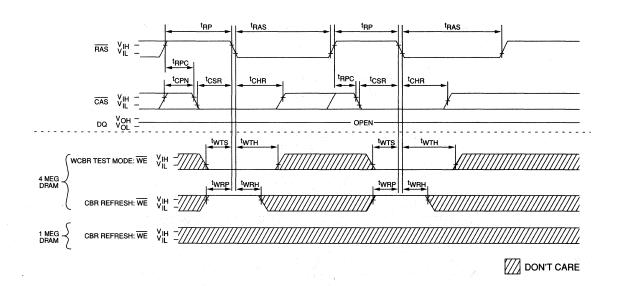
A CBR cycle with WE LOW will put the 4 Meg into the IEDEC specified test mode (WCBR).

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The 4 Meg POWER-UP is more restrictive in that eight RAS-ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the IEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a RAS-ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

- 1. The 1 Meg CBR REFRESH allows the $\overline{\text{WE}}$ pin to be "don't care" while the 4 Meg CBR requires WE to be HIGH.
- 2. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR



DRAM

1 MEG x 4 DRAM

QUAD CAS PARITY, FAST PAGE MODE

FEATURES

- Four independent CAS controls, allowing individual manipulation to each of the four data Input/Output ports (DQ1 through DQ4).
- Offers a single chip solution to byte level parity for 36bit words when using 1 Meg x 4 DRAMs for memory
- Emulates write-per-bit, at design-in level, with simplified timing constraints
- High-performance, CMOS silicon-gate process
- Single $+5V \pm 10\%$ power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

OPTIONS MARKING Timing 70ns access - 7 80ns access - 8 100ns access - 10 Packages Plastic SOJ (300 mil) NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

Part Number Example: MT4C4004JDJ-7 GENERAL DESCRIPTION

The MT4C4004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each CAS (CAS1 through CAS4) controls its corresponding data I/O port in conjunction with OE (eg. CAS1 controls DQ1 I/O port, CAS2 controls DQ2, CAS3 controls DQ3 and CAS4 controls DQ4).

The best way to view the Quad \overline{CAS} function is to imagine the \overline{CAS} inputs going into an AND gate to obtain an internally generated \overline{CAS} signal functioning in an identical manner to the single \overline{CAS} input on a standard 1 Meg x 4 DRAM device. The key difference is each \overline{CAS} controls its corresponding DQ tristate logic (in conjunction with \overline{OE} and \overline{WE}) on the Quad CAS DRAM.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits, and the first CAS is used to latch the latter 10 bits. READ and

PIN ASSIGNMENT (Top View) 24-Pin SOJ (Q-2)



WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode.

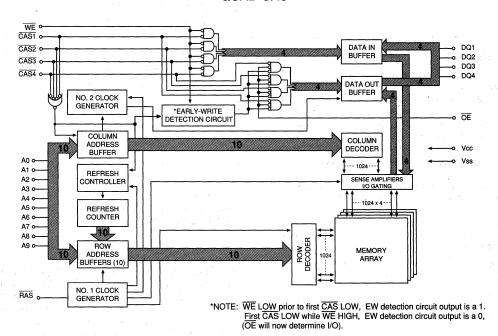
During a WRITE cycle, data-in (Dx) is latched by the falling edge of \overline{WE} or the first \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to the first \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after data reaches the output buffer, data out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding \overline{CAS} occurs (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle (\overline{OE} switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by \overline{WE} and \overline{OE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed in by the first CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and all four CAS controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.



FUNCTIONAL BLOCK DIAGRAM QUAD CAS



TRUTH TABLE

		· · · · · ·					ADDRE	SSES	DQx
FUNCTION		RAS	CASx	CASy	WE	ŌĒ	^t R	1C	(DQy always High-Z)
Standby		Н	H→X	H→X	X	X	X	Х	High-Z
READ	*,15	L	~L	Н	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	Н	L	X	ROW	COL	Data In
READ-WRITE		s y Lais	L C	Н	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	i se L esse	H→L	H to	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	r r Lass	H→L	H	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	Н	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	H	Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	PAR	Н	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	Н	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	⊢→L	L.	H	Χ	×	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	li.	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (Iout = -3.11A)	Vol	***	0.4	V	

		MAX						
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES		
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	2.5	2.5	2.5	mA			
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	1	1 2	mA	26		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC= ^t RC (MIN))	lcc3	100	90	80	mA	3, 4		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS, Address Cycling: ¹ PC= ¹ PC (MIN))	lcc4	70	60	50	mA	3, 4		
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: tRC= tRC (MIN))	lcc5	100	90	80	mA	3		
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC= ^t RC (MIN))	lcc6	100	90	80	.mA	3, 5		

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cı1		5	pF	2
Input Capacitance: RAS, CAS1-4, WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS			-7		-8		10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130	ł ·	150		180		ns	
READ-WRITE cycle time	^t RWC	185		205		220		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		45		55		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	95		100		115		ns	31
Access time from RAS	†RAC		70		80		100	ns	14
Access time from CAS	†CAC	- ' -	20		20		25	ns	15, 29
Output Enable	^t OE		20		20		25	ns	33
Access time from column address	†AA		35		40		50	ns	
Access time from CAS precharge	^t CPA		40		45		50	ns	29
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	4.40
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		20		25		ns	27
RAS precharge time	tRP	50		60		70		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	25	100,000	ns	34
CAS hold time	^t CSH	70		80		100		ns	28
CAS precharge time	^t CPN	10		10		15		ns	16, 32
CAS precharge time (FAST PAGE MODE)	t _{CP}	10		10		10		ns	32
RAS to CAS delay time	^t RCD	20	50	20	60	25	75	ns	17, 27
CAS to RAS precharge time	^t CRP	5		5		5		ns	28
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
RAS to column address delay time	†RAD	15	35	15	40	20	50	ns	18
Column address setup time	†ASC	0		0		0		ns	27
Column address hold time	^t CAH	15		15		20		ns	27
Column address hold time (referenced to RAS)	^t AR	55		60		70		ns	
Column address to RAS lead time	^t RAL	35		40		50		ns	
Read command setup time	tRCS	0		0		0		ns	27
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 28
Read command hold time (referenced to RAS)	^t RRH	0		0		0	1 16 14 15 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns	19
CAS to output in Low-Z	^t CLZ	0		0		0		ns	29



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

		100		10 mm	100	100		100	
AC CHARACTERISTICS		-7	7	-	3	-	10		1 1 1 1
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 29, 38
Output disable	tOD		20		20		20	ns	34, 38
WE command setup time	twcs	0		0	rees st	0		ns	21, 27
Write command hold time	tWCH	15		15	1,37 - 1, 1, 1,	20	1.12	ns	36
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to RAS lead time	tRWL	20		20		25		ns	
Write command to CAS lead time	tCWL	20		20		25		ns	28
Data-in setup time	tDS	0		0		0		ns	22, 29
Data-in hold time	tDH	15		15		20	N. 1514	ns	22, 29
Data-in hold time (referenced to RAS)	tDHR	55		60		75		ns	
RAS to WE delay time	^t RWD	100		110		130		ns	21
Column address to WE delay time	tAWD	65		70		80		ns	21
CAS to WE delay time	tCMD	50		55		60		ns	21, 27
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	†REF		16		16		16	ms	
RAS to CAS precharge time	tRPC	0		0		0	100	ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5, 27
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5, 28
Last CAS going LOW to first CAS to return HIGH	tCLCH	10		10		10		ns	30
OE hold time from WE during READ-MODIFY-WRITE cycle	†OEH	20		20	na e i i i i i i i i i i i i i i i i i i	20		ns	37
OE setup prior to RAS during HIDDEN refresh cycle	^t ORD	0		0		0		ns	

NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial 100µs pause is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH)
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CASx} = V_{IH}$, data output (Qx) is High-Z.
- If CASx = VIL, Qx may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If at least one CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four CAS controls must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in EARLY-WRITE and READ-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle (at access time and until CAS or OE goes back to Vih).
- 22. These parameters are referenced to CASx leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-WRITE cycles.
- If OE is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. One to three CAS controls may be HIGH throughout any given CAS cycle, even though the timing waveforms show all CAS controls going LOW. If any one goes LOW, it must meet all the timing requirements listed, or the data for that I/O buffer may be invalid. At least one of the four CAS controls must be LOW for a valid CAS cycle to occur.
- 26. All other inputs at Vcc -0.2V.
- 27. The first CASx edge to transition LOW.
- 28. The last CASx edge to transition HIGH.
- Output parameters (DQx) are referenced to corresponding CASx input; DQ1 by CAS1, DQ2 by CAS2, etc.
- 30. Last falling CASx edge to first rising CASx edge.
- Last rising CASx edge to next cycle's last rising CASx edge.
- 32. Last rising CASx edge to first falling CASx edge.
- 33. First DQx controlled by the first $\overline{CAS}x$ to go LOW.
- 34. Last DQx controlled by the last \overline{CASx} to go HIGH.
- 35. Each CASx must meet minimum pulse width.
- 36. Last CASx to go LOW.

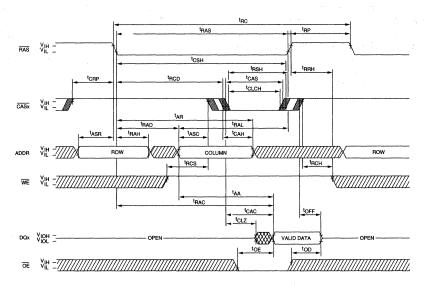


NOTES (continued)

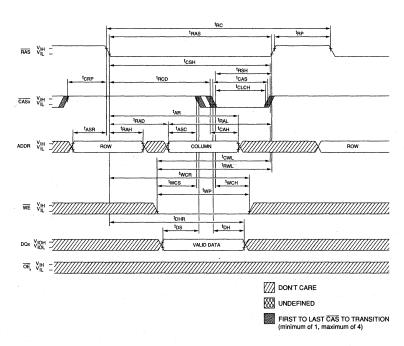
- 37. LATE-WRITE and READ-MODIFY-WRITE cycles must meet both ^tOD and ^tOEH (OE HIGH during WRITE cycle) to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If the last CASx goes HIGH prior to OE going back LOW, the DQs will remain open.
- 38. The DQs will open during READ cycles once ^tOD or ^tOFF occur. If the last CASx goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CASx stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CASx remains LOW).



READ CYCLE

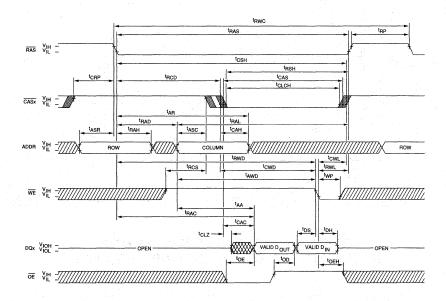


EARLY-WRITE CYCLE

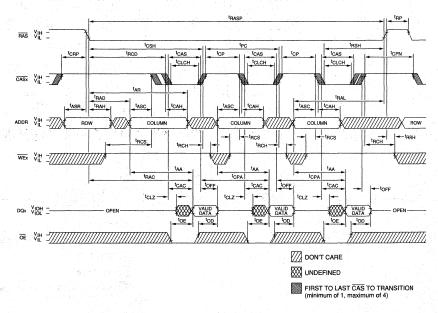




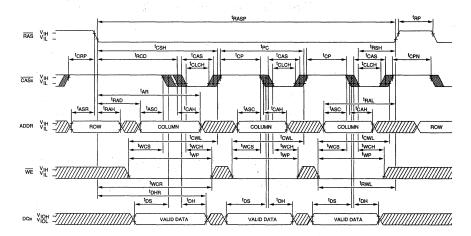
READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



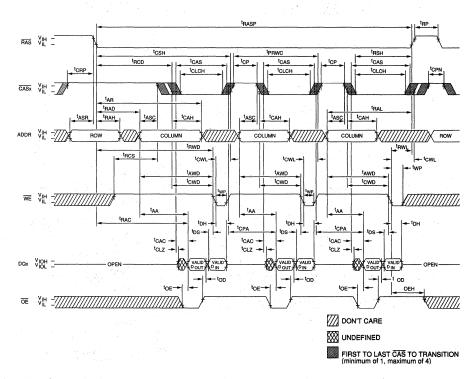
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



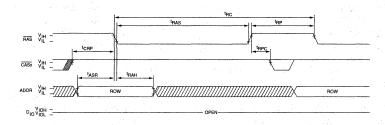
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





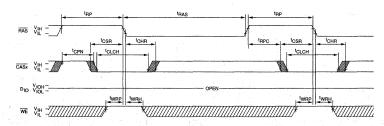
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; $\overline{\text{WE}}$ and $\overline{\text{OE}}$ = DON'T CARE)



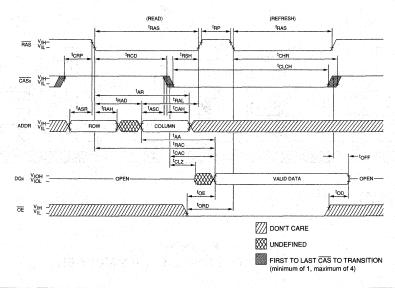
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9, \overline{OE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH, \overline{OE} = LOW)$

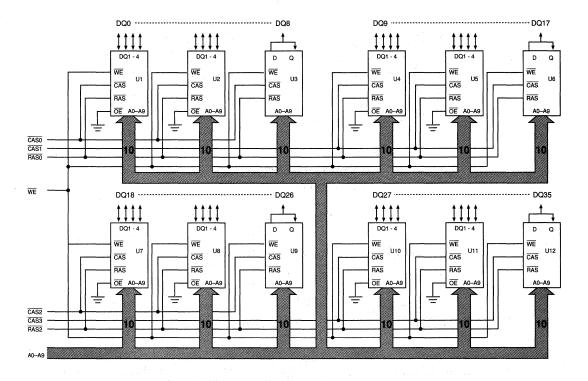


OUAD CAS MODULE UPGRADE

The MT4C4004J (Quad CAS DRAM) was developed to supersede the 1 Meg DRAMs used in the current 1 Meg and 2 Meg x 36 DRAM modules and to add leading-edge CMOS performance. The MT4C4004J is a 1 Meg x 4 CMOS FAST-PAGE-MODE DRAM with four CAS input controls. The four individual CAS inputs allow each I/O buffer (DQ) to be separately controlled, just as if there were four separate 1 Meg x 1 DRAMs. Most 1 Meg x 1 DRAMs use older CMOS technology and do not have the access speeds of the newer CMOS 4 Meg (1 Meg x 4).

The MT4C4004J reduces chip count on x36 modules; improving reliability, reducing power consumption and lowering cost. In the 1 Meg x 36, four 1 Meg x 1 DRAMs are replaced by either one or two Quad CAS DRAMs, depending on whether RAS0 and RAS1 must be separate or connected. In the 2 Meg x 36, eight 1 Meg x 1 DRAMs are replaced by either two or four Quad CAS DRAMs, depending on whether RASO, RAS1, RAS2, and RAS3 must be split or connected.

The current 1 Meg x 36 DRAM Module is shown with 256K x 1 DRAMs in Figure 1 below. Figures 2 and 3 show how the same module will be realized with the Quad CAS DRAM for both the split \overline{RAS} (Figure 2) and the common RAS (Figure 3) modules.

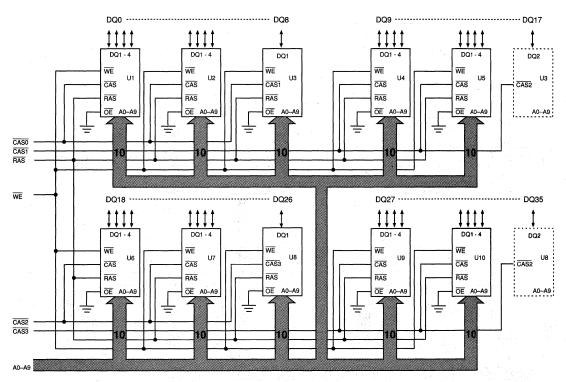


U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4001JDJ U3, U6, U9, U12 = MT4C1024DJ

Figure 1 1 MEG x 36 WITH 1 MEG x 1 FOR PARITY BIT



QUAD CAS ENHANCED x36 MODULES

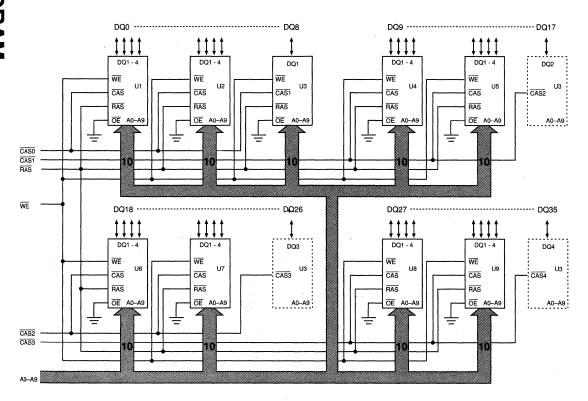


U1, U2, U4, U5, U6, U7, U8, U9 = MT4C4001JDJ U3 = MT4C4004JDJ

Figure 2

1 MEG x 36 WITH QUAD CAS FOR PARITY BIT AND SPLIT RAS CONTROL

QUAD CAS ENHANCED x36 MODULES



U1, U2, U4-U9 = MT4C4001JDJ U3 = MT4C4004JDJ

Figure 3

1 MEG x 36 WITH QUAD CAS FOR PARITY BIT AND COMMON RAS CONTROL



DRAM

4 MEG x 4 DRAM

5.0V FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 3mW standby; 325mW active, typical (A1)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
 Packages Plastic SOJ (400 mil) Plastic TSOP (400 mil) 	DJ TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

Refresh Period	
2,048 cycles @ 32ms,	MT4C4M4B1
11 Row Addresses	
4,096 cycles @ 64ms,	MT4C4M4A1
12 Row Addresses	

• Operating Temperature, T Commercial (0°C to +70°C) None

GENERAL DESCRIPTION

The MT4C4M4A1/B1 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. The MT4C4M4A1 and MT4C4M4B1 are the same DRAM versions except that the MT4C4M4B1 has 2,048 cycle refresh instead of 4,096 cycle refresh. All further references made for the MT4C4M4A1 also apply to the MT4C4M4B1 unless specifically stated otherwise. For a device with 2,048 cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a device with 4,096 cycle refresh, RAS is used to latch the first 12 bits and CAS the latter 10 bits (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the WE input. A logic

PIN ASSIGNMENT (Top View)						
24-Pin SOJ (Q-3)	24-Pin TSOP (R-2)					
Vcc 1	04 DQ1 □ 2 27 □ DQ4 03 DQ2 □ 3 26 □ DQ3 05 WE □ 4 25 □ CAS 07 RAS □ 5 24 □ OE					
A10 0 9 20 A8 A0 0 10 19 A7 A1 0 11 18 A6 A2 0 12 17 A5 A3 0 13 16 A4 Vcc 0 14 15 D Vs	A0 = 10					

HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

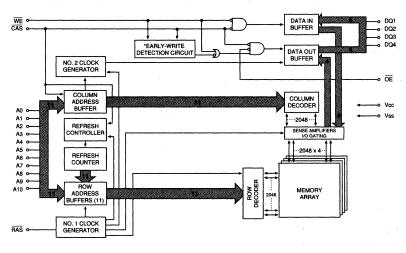
FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9/10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} (CBR) or HIDDEN refresh) so that all 2,048/4,096 combinations of \overline{RAS}

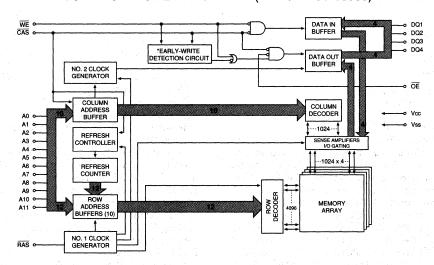
addresses (A0-A10/A11) are executed at least every 32ms/64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic \overline{RAS} addressing.

If CBR refresh is used, the number of cycles is a "don't care."

FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE MT4C4M4B1 (11 Row Addresses)



FUNCTIONAL BLOCK DIAGRAM FAST PAGE MODE MT4C4M4A1 (12 Row Addresses)



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE)

CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)

MT4C4M4A1/B1 4 MEG x 4 DRAM

TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	t _R	tC .	DQ1-DQ4
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ		L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	Н	X	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z

MT4C4M4A1/B1 4 MEG x 4 DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss (5.0	OV)1.0V to +7.0V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION	The state of the s	4,11	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage			Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	A		VIH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs			VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)			lı	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disable	ed, 0V ≤ Vout ≤	5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)			Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)			Vol		0.4	V	

(Notes: 1, 3, 4, 6, 7) (Vcc = 5V ±10%), 2,048 cycle refresh

(RAS, CAS, Address Cycling: tRC = tRC (MIN))

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 5V \pm 10\%$), 4,096 cycle refresh MAX PARAMETER/CONDITION -7 NOTES SYMBOL -6 -8 UNITS STANDBY CURRENT: (TTL) Icc1 2 2 2 mA $(\overline{RAS} = \overline{CAS} = V_{IH})$ STANDBY CURRENT: (CMOS) lcc2 1 1 1 mA $(\overline{RAS} = \overline{CAS} = Other Inputs = Vcc -0.2V)$ OPERATING CURRENT: Random READ/WRITE Average power supply current Іссз 90 80 70 mΑ 3, 4, 28 (RAS, CAS, Address Cycling: ^tRC = ^tRC (MIN)) OPERATING CURRENT: FAST PAGE MODE Average power supply current 70 60 50 3, 4, 28 ICC4 mΑ $(\overline{RAS} = V_{IL}, \overline{CAS}, Address Cycling: {}^{t}PC = {}^{t}PC (MIN))$ REFRESH CURRENT: RAS-ONLY Average power supply current Icc5 90 80 70 mΑ 3, 28 $(\overline{RAS} \text{ Cycling}, \overline{CAS} = V_{IH}: {}^{t}RC = {}^{t}RC (MIN))$ REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current Icc6 90 80 70 mΑ 3, 5, 28 (RAS, CAS, Address Cycling: ^tRC = ^tRC (MIN))

PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = \text{Other Inputs} = \text{Vcc -0.2V})$	lcc2	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	120	110	100	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	90	80	70	mA	3, 4, 27
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	120	110	100	mA	3, 27
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current	Icce	120	110	100	mA	3, 5, 27

MAX

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11	Ci1		- 5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		. 7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS			-6 , ,		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	150		180		200		ns	
FAST-PAGE-MODE	tPC	40		45		50		ns	
READ or WRITE cycle time									
FAST-PAGE-MODE	^t PRWC	85	1.	95		100		ns	
READ-WRITE cycle time									
Access time from RAS	^t RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Output Enable	†OE	7.7	15		20		20	ns	23
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10	1	10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	†RAD	15	30	15	35	15	40	ns	18
address delay time	1,11								B. 1
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time	†AR	50		55		60		ns	1 11 1
(referenced to RAS)			1 1						
Column address to	^t RAL	30		35		40		ns	
RAS lead time									3
Read command setup time	†RCS	0		0		0		ns	
Read command hold time	tRCH	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	^t CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS			-6		-7	1	-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		0		ns	21, 27
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55	1.41.21	60	o grada Salakan ng	ns	
Write command pulse width	tWP	10		15		15	1 10000	ns	19 11 1 1 1 4.
Write command to RAS lead time	tRWL	15		20		20		ns	29-00-00-0
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	^t DS	0		0	The second	0	A + 2/11	ns	22
Data-in hold time	^t DH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65	1 2 2 3 4 3	ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	^t REF		32/64		32/64		32/64	ms	26
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	[†] CHR	15		15		15	Fur 1, 51 413	ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10	Taley (10		ns	25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	25
WE hold time (WCBR test cycle)	™TH	10		10		10	Terison (i	ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD		15		20		20	ns	79310
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		15		15		ns	

MT4C4M4A1/B1 4 MEG x 4 DRAM

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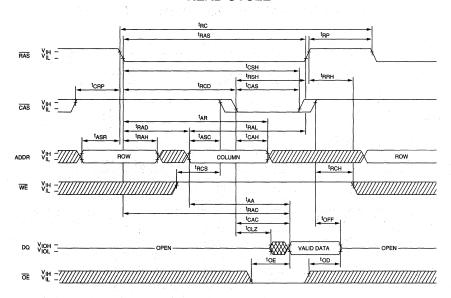
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{I\!H}$ and $V_{I\!H}$ (or between $V_{I\!L}$ and $V_{I\!H}$) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.

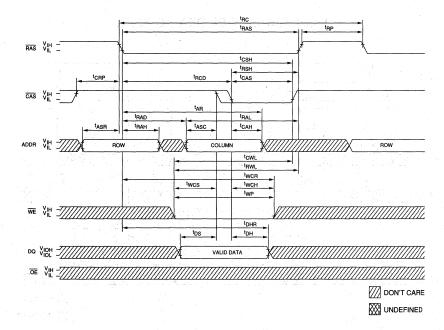
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
- 21. WCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY-WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. 32ms is 2,048 refresh, 64ms is 4,096 refresh.
- 27. 2,048 row refresh.
- 28. 4,096 row refresh.



READ CYCLE

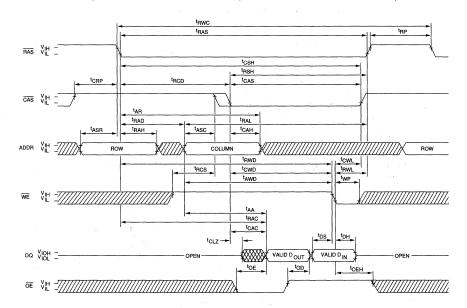


EARLY-WRITE CYCLE

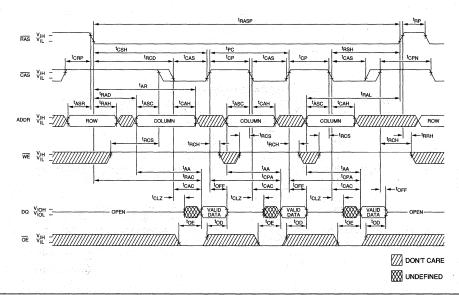


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READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

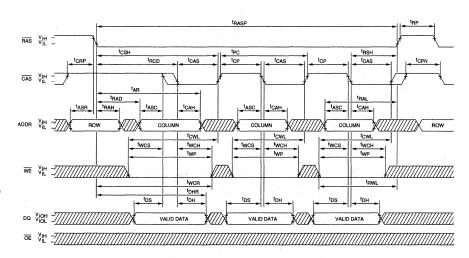


FAST-PAGE-MODE READ CYCLE

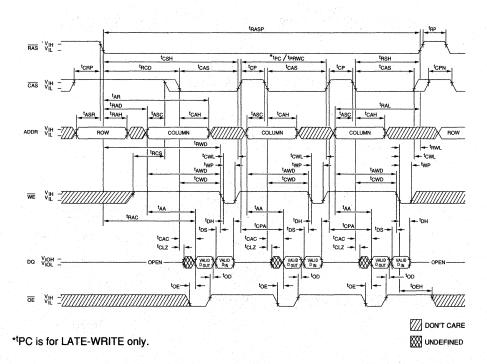




FAST-PAGE-MODE EARLY-WRITE CYCLE

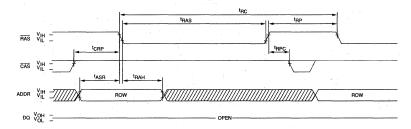


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



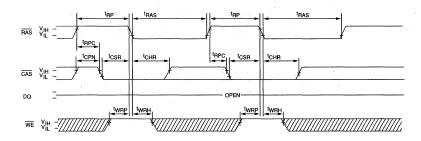


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



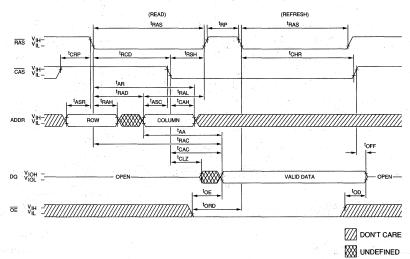
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

4 MEG x 4 DRAM

3.3V FAST PAGE MODE

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +3.3V ±10%
- Low power, 1mW standby; 125mW active, typical (A1)
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms or 4,096-cycle refresh distributed across 64ms

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Plastic SOJ (400 mil)	DI
Plastic TSOP (400 mil)	TG

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

Refresh Period	
2,048 cycles @ 32ms,	MT4LC4M4B1
11 Row Addresses	
4,096 cycles @ 64ms,	MT4LC4M4A1
12 Row Addresses	

 Operating Temperature, T_A Commercial (0 $^{\circ}$ C to +70 $^{\circ}$ C) None

GENERAL DESCRIPTION

The MT4LC4M4A1/B1 are randomly accessed solidstate memories containing 16,777,216 bits organized in a x4 configuration. The MT4LC4M4A1 and MT4LC4M4B1 are the same DRAM versions except that the MT4LC4M4B1 has 2,048 cycle refresh instead of 4,096 cycle refresh. All further references made for the MT4LC4M4A1 also apply to the MT4LC4M4B1 unless specifically stated otherwise. For a device with 2,048 cycle refresh, RAS is used to latch the first 11 bits and CAS the latter 11 bits. For a device with 4,096 cycle refresh, \overline{RAS} is used to latch the first 12 bits and \overline{CAS} the latter 10 bits (A10 and A11 are "don't care" bits). READ

9	·											
PIN ASSIGNMENT (Top View)												
24-Pin (Q-3		24-Pin TSOP (R-2)										
Vcc 1 1	28 Vss 27 DQ4 26 DQ3 25 CAS 24 DOE 23 A9	Vcc = 1 DQ1 = 2 DQ2 = 3 WE = 4 RAS = 5 A11/NC = 6	28									
A10 0 9 A0 0 10 A1 0 11 A2 0 12 A3 0 13 Vcc 0 14	20	A10 \(\psi \) 9 A0 \(\psi \) 10 A1 \(\psi \) 11 A2 \(\psi \) 12 A3 \(\psi \) 13 Vcc \(\psi \) 14	20 ^{□□} A8 19 ^{□□} A7 18 ^{□□} A6 17 ^{□□} A5 16 ^{□□} A4 15 ^{□□} Vss									

and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next \overline{CAS} cycle. If WE goes LOW after data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late WE pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9/10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

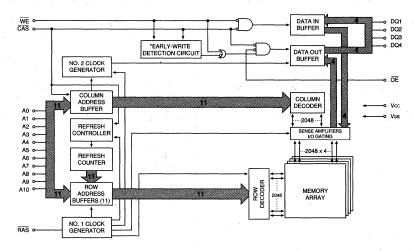
Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR) or HIDDEN refresh) so that all 2,048/4,096 combinations of RAS

addresses (A0-A10/A11) are executed at least every 32ms/ 64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic RAS addressing.

If CBR refresh is used, the number of cycles is a "don't

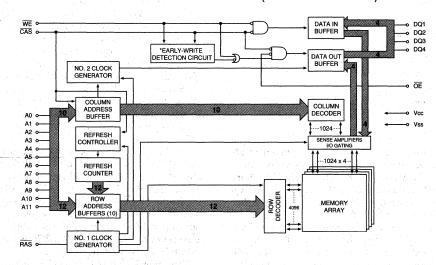
FUNCTIONAL BLOCK DIAGRAM

FAST PAGE MODE MT4LC4M4B1 (11 Row Addresses)



FUNCTIONAL BLOCK DIAGRAM

FAST PAGE MODE MT4LC4M4A1 (12 Row Addresses)



*NOTE: WE LOW prior to CAS LOW, EW detection circuit output is a HIGH (EARLY-WRITE) CAS LOW prior to WE LOW, EW detection circuit output is a LOW (LATE-WRITE)



MT4LC4M4A1/B1 4 MEG x 4 DRAM

TRUTH TABLE

The state of the s		100 \$100	1.74			ADDRE	SSES	DATA IN/OUT
FUNCTION	14 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	RAS	CAS	WE	0E	^t R	¹C	DQ1-DQ4
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ	esin kalif	,L	L	Н	L	ROW	COL	Data Out
EARLY-WRITE	1	L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
RAS-ONLY REFRESH		L	Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L.	Н	Х	Х	Х	High-Z

MT4LC4M4A1/B1 4 MEG x 4 DRAM

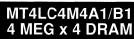
ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($Vcc = 3.3V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ 3.6V (All other pins not under test = 0V)	.lı	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 2mA)	Vol		0.4	V	





ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

Notes: 1, 3, 4, 6, 7) (Vcc = $3.3V \pm 10\%$), 4,096 cycle refresh			MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	1	1	1	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc2	400	400	400	μА		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	60	55	50	mA	3, 4, 28	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ¹PC = ¹PC (MIN))	ICC4	40	35	30	mA	3, 4, 2	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ¹RC = ¹RC (MIN))	lcc5	60	55	50	mA	3, 28	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: tRC = tRC (MIN))	lcc6	60	55	50	mA	3, 5, 2	

	 	 	1_	 		
(Notes: 1						

Notes: 1, 3, 4, 6, 7) (VCC = $3.3V \pm 10\%$), 2,048 cycle retresh			MAX			1 30 5 TO 1 A 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES		
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	1	1	1	mA			
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc2	400	400	400	μА			
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	80	70	60	mA	3, 4, 27		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC (MIN))	lcc4	60	50	40	mA	3, 4, 27		
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: tRC = tRC (MIN))	lcc5	80	70	60	mA	3, 27		
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	80	70	60	mA	3, 5, 27		



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APACITANCE					
APACITANCE PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
	1			T	NOTE 2
PARAMETER	SYMBOL		MAX	UNITS	NOTE 2 2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		-	-6		-7	-	8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	150		180		200		ns	
FAST-PAGE-MODE	^t PC	40		45		50		ns	
READ or WRITE cycle time									
FAST-PAGE-MODE	^t PRWC	85		95		100		ns	
READ-WRITE cycle time			1		4.				
Access time from RAS	†RAC		60		70	1	80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Output Enable	^t OE		15	:	20		20	ns	23
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		. 10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0	1	0		0		ns	N 150
Column address hold time	^t CAH	10		15		15		ns	1 ** Jan. 1
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35	1	40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0	100	0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		.0		ns	19
CAS to output in Low-Z	¹CLZ	0		0		0	4	ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23)

AC CHARACTERISTICS		1000	-6	-7			-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0		0		0		ns	21, 27
Write command hold time	^t WCH	10		15		15	A My Child	ns	15 10
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15	Para Sawara	15		ns	7
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	10,8
Data-in setup time	^t DS	0		0		0	Erre Value	ns	22
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	er jak sya
RAS to WE delay time	tRWD	85	1	95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65		ns	21
CAS to WE delay time	tCMD	40		45		45		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048/4,096 cycles)	†REF		32/64		32/64		32/64	ms	26
RAS to CAS precharge time	†RPC	0		0		0	7.7	ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	5		5	1.25 (3.0)	5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15	KI A	15	5.00	ns	5
WE hold time (CAS-BEFORE-RAS refresh)	†WRH	10		10	. (1) (3) (1) (1) (1) (2) (3) (1)	10		ns	25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		10	. Heljati i Konjenski	ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	^t OD	- 1978 THE	15		20		20	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	†OEH	15		15		15		ns	

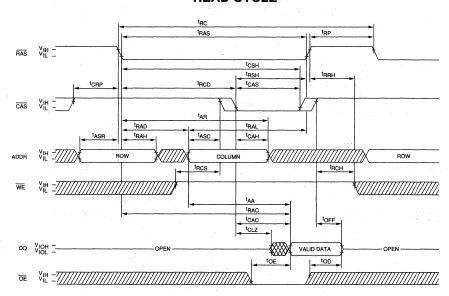
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ${}^{t}T = 5 ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If CAS = VIH, data output is High-Z.
- 12. If CAS = Vil, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.

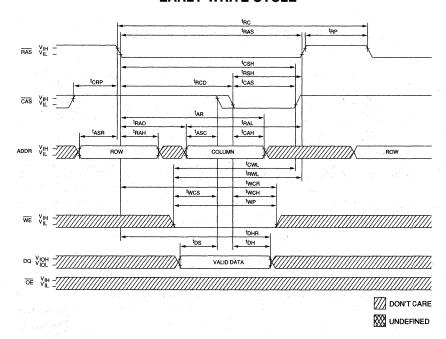
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cvcle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to Voh or Vol.
- 21. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY-WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge$ ${}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE-WRITE cycle.
- 22. These parameters are referenced to \overline{CAS} leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$ and \overline{OE}
- 25. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. 32ms is 2,048 refresh, 64ms is 4,096 refresh.
- 27. 2,048 row refresh.
- 28. 4.096 row refresh.



READ CYCLE

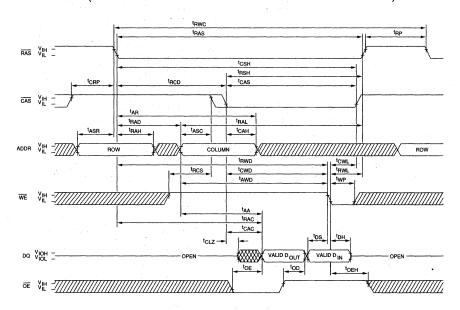


EARLY-WRITE CYCLE

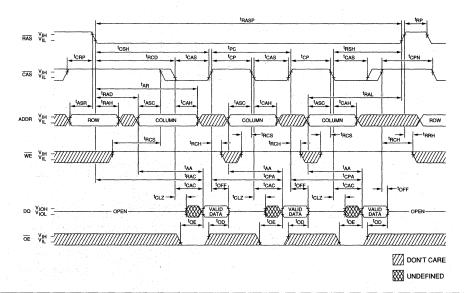


NEW I DRAM

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

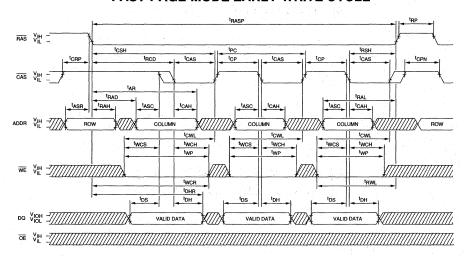


FAST-PAGE-MODE READ CYCLE

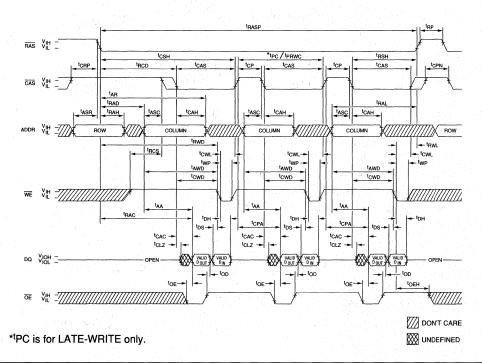




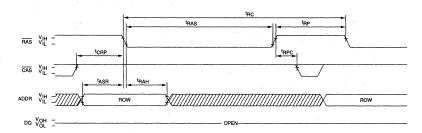
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

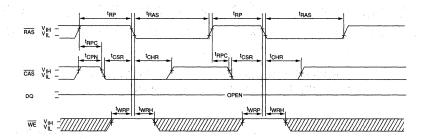


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)

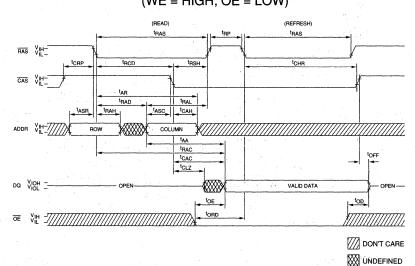


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24 (WE = HIGH; OE = LOW)



DRAM

4 MEG x 4 DRAM

STATIC COLUMN

FEATURES

- Industry standard x4 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 5mW standby; 275mW active, typical
- All inputs, outputs and clocks are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS

MARKING

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8

Packages

Plastic SOI (400 mil) DI

NOTE: Available in die form (commercial or military) or military ceramic packages. Please consult factory for die data sheets or refer to Micron's Military Data Book.

· Refresh Period 4,096 cycles @ 64ms,

MT4C4M4D1

12 Row Addresses

• Operating Temperature, TA Commercial (0°C to +70°C)

None

GENERAL DESCRIPTION

The MT4C4M4D1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 10-12 bits (A0-A11) at a time. RAS is used to latch the first 12 bits and CAS the latter 10 (A10 and A11 are "don't care" bits). READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the

PIN ASSIGNMENT (Top View)

24-Pin SOJ (Q-3)

Vcc C DQ1 C DQ2 C WE C RAS C A11/NC C	3 4 5	28 27 26 25 24 23	Vss DQ4 DQ3 CAS OE A9
A10 E A0 E A1 E A2 E A3 E Vcc E	10 11 12 13	17	A8 A7 A6 A5 A4 Vss

output pins, data out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by \overline{WE} and \overline{OE} .

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. After the first READ, any column address transition will result in new data out. Unlike the PAGE-MODE part, which requires CAS to be toggled for each successive PAGE-MODE access, the STATIC COLUMN part allows CAS to be left LOW for successive STATIC COLUMN accesses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), or HIDDEN refresh) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

MICHON

DYNAMIC RAMS	1
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9



WIDE DRAM PRODUCT SELECTION GUIDE

Memory	Optional	Part	Access	Typical Pow	er Dissipation	Packag	e/Number	of Pins	
Configuration	Access Cycle	Number*	Time (ns)	Standby	Active	ZIP	SOJ	TSOP	Page
512K x 8	FP	MT4C8512	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, WPB	MT4C8513	70, 80, 100	3mW	350mW	28	28	28	2-1
512K x 8	FP, LP	MT4C8512 L	70, 80, 100	1mW	350mW	28	28	28	2-15
512K x 8	FP, WPB, LP	MT4C8513 L	70, 80, 100	1mW	350mW	28	28	28	2-15
2 Meg x 8	FP, 4KR	MT4(L)C2M8A1	60, 70, 80	5mW	400mW		28, 32	28, 32	2-31
2 Meg x 8	FP, 4KR, WPB	MT4(L)C2M8A2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-31
2 Meg x 8	FP, 2KR	MT4(L)C2M8B1	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 2KR, WPB	MT4(L)C2M8B2	60, 70, 80	5mW	400mW	-	28, 32	28, 32	2-47
2 Meg x 8	FP, 4KR, S, LP	MT4(L)C2M8A1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 4KR, WPB, S, LP	MT4(L)C2M8A2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-63
2 Meg x 8	FP, 2KR, S, LP	MT4(L)C2M8B1 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
2 Meg x 8	FP, 2KR, WPB, S, LP	MT4(L)C2M8B2 S	60, 70, 80	2mW	400mW	-	28, 32	28, 32	2-81
64K x 16	FP, DW	MT4C1664	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, WPB	MT4C1665	70, 80, 100	3mW	225mW	40	40	40	2-99
64K x 16	FP, DW, LP	MT4C1664 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	FP, WPB, LP	MT4C1665 L	70, 80, 100	1mW	225mW	40	40	40	2-115
64K x 16	SC, DW	MT4C1670	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, WPB	MT4C1671	70, 80, 100	3mW	225mW	40	40	40	2-133
64K x 16	SC, DW, LP	MT4C1670 L	70, 80, 100	1mW	225mW	40	40	40	2-151
64K x 16	SC, WPB, LP	MT4C1671 L	70, 80, 100	1mW	225mW	40	40	40	2-151
256K x 16	FP, DW	MT4C16256	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC	MT4C16257	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, WPB	MT4C16258	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DC, WPB	MT4C16259	70, 80, 100	3mW	500mW	40	40	40	2-169
256K x 16	FP, DW, LP	MT4C16256 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, LP	MT4C16257 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DW, WPB, LP	MT4C16258 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, DC, WPB, LP	MT4C16259 L	70, 80, 100	1mW	500mW	40	40	40	2-191
256K x 16	FP, ASY, DW	MT4C16260	70, 80, 100	1mW	500mW	40	40	40	2-213
256K x 16	FP, WPB, ASY	MT4C16261	70, 80, 100	1mW	500mW	40	40	40	2-213
1 Meg x 16	FP, DC	MT4(L)C1M16C3	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW	MT4(L)C1M16C5	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, WPB	MT4(L)C1M16C6	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DW, WPB	MT4(L)C1M16C7	60, 70, 80	5mW	500mW	-	42	44	2-229
1 Meg x 16	FP, DC, S, LP	MT4(L)C1M16C3 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, S, LP	MT4(L)C1M16C5 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DC, WPB, S, LP	MT4(L)C1M16C6 S	60, 70, 80	2mW	500mW	-	42	44	2-251
1 Meg x 16	FP, DW, WPB, S, LP	MT4(L)C1M16C7 S	60, 70, 80	2mW	500mW	-	42	44	2-251

FP = Fast Page Mode, SC = Static Column, LP = Low Power, Extended Refresh; WPB = Write Per Bit, DW = Dual WE, DC = Dual CAS, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, S = Self Refresh, ASY = Asymmetrical Addressing
*(L)C means device is available in both 5V Vcc (MT4CXXXXX) and 3/3.3V Vcc (MT4LCXXXXX) versions

24 A5

== 26 A7

== 28 NC



DRAM

512K x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 10 row addresses, nine column addresses
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 350mW active, typical
- All device pins are fully TTL compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)

OPTIONS	MARKING
 Timing 	
70ns access	- 7
80ns access	- 8
100ns access	-10
Masked Write	
Not available	MT4C8512
Available	MT4C8513
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (375 mil)	\mathbf{Z}

NOTE: Available in die form. Please consult factory for die data sheets.

GENERAL DESCRIPTION

The MT4C8512/3 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by \overline{RAS} latching 10 bits (A0-A9) and then \overline{CAS} latching 9 bits (A0-A8).

The MT4C8513 has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.

28-Pin SOJ 28-Pin ZIP (Q-4)(O-3) ŌĒ Vcc ☐ 1 28 🛘 Vss CAS 2 DQ1 [2 27 DQ8 4 DQ6 DQ7 5 26 DQ7 DQ2 3 DQ8 DQ3 🛮 4 25 D DQ6 Vss 8 Vcc DQ4 🛮 5 24 DQ5 DQ1 10 DQ2 NC ☐ 6 23 CAS DQ3 11 12 DQ4 WE [7 22 D OE NC RAS [8 21 | NC 14 WE RAS 15 20 1 A8 A9 ☐ 9 16 A9 A0 19 🛭 A7 A0 10 18 A1 A2 19 A1 11 18 T A6 20 A3 A2 | 12 □ A5 Vcc 21 17 22 Vss A3 🛘 13 16 🛭 A4 A4 23

PIN ASSIGNMENT (Top View)

28-Pin TSOP (R-3)

15 🛭 Vss

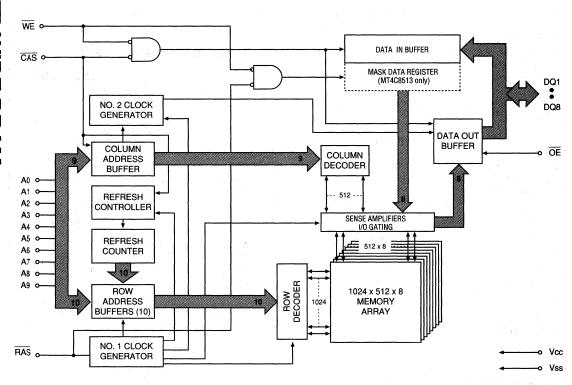
A6 25

A8

Vcc 14

Vcc	田	1		28	þ	Vss
DQ1	田	2		27	口	DQ8
DQ2	Ш	3		26	口	DQ7
DQ3	ш	4		25	口	DQ6
DQ4	田	5		24	口	DQ5
NC	Щ	6		23	Ы	CAS
WE	ш	7.		22	口	ŌĒ
RAS	Щ	8		21	田	NC
A9	Ш	9		20	b	A8
Α0		10		19	一	A7
A1	Ш	11		18	口	A6
A2	田	12		17	田	A5
A3		13		16	田	A4
Vcc	四	14		15	þ	Vss
	,		 			

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION			
8 4 h 33 h	15	RAS	Row Address Strobe: RAS is used to clock-in the 10 row-address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C8513 only).				
23	2	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.			
7 . : : : : : : : : : : : : : : : : : : :	14	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C8513).					
22		ŌĒ	Input	Output Enable: \overline{OE} enables the output buffers when taken LOW during a READ access cycle. \overline{RAS} and \overline{CAS} must be LOW and \overline{WE} must be HIGH before \overline{OE} will control the output buffers. Otherwise the output buffers are in a High-Z state.			
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 512K available words.			
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).			
6, 21	13, 28	NC	1	No Connect: These pins should be either left unconnected or tied to ground.			
1, 14	8, 21	V cc	Supply	Power Supply: +5V ±10%			
15, 28	7, 22	Vss	Supply	Ground			

WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First RAS is used to latch 10 bits (A0-A9) then CAS latches 9 bits (A0-A8).

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW.

READ or WRITE cycles are selected by \overline{WE} . A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-inby CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the

RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C8513 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when \overline{WE} is LOW at \overline{RAS} time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).



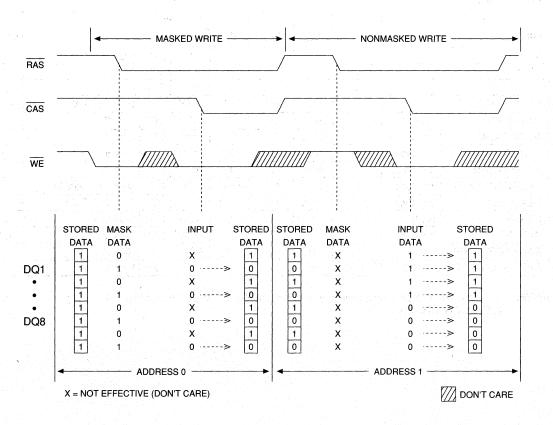


Figure 1
MT4C8513 MASKED WRITE EXAMPLE

TRUTH TABLE

·						ADDRE	SSES		
FUNCTION		RAS	CAS	WE	OE	^t R	¹C	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	X	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	

NOTE:

^{1.} Data in will be dependent on the mask provided (MT4C8513 only). Refer to Figure 1.

^{2.} EARLY WRITE only.



MT4C8512/3 512K x 8 DRAM

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ ViN ≤ Vcc (All other pins not under test = 0V)	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)	Vol		,0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: TTL (RAS = CAS = ViH)	Icc1	2	2	2	mA	
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹ RC = ¹ RC (MIN))	lcc3	110	100	90	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	Icc4	90	80	70	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: RC = RC (MIN))	lcc5	110	100	90	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	110	100	90	mA	3

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C ₁₁	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	*tRC	130		150		180		ns	
READ-WRITE cycle time	^t RWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE	^t PC	45		50		55		ns	
cycle time					4.7	1803			3
FAST-PAGE-MODE READ-WRITE	†PRWC	95		100		110		ns	
cycle time									
Access time from RAS	†RAC		70		80		100	ns,	14
Access time from CAS	tCAC		20		20		25	ns	15
Output Enable time	^t OE		20	7	20		25	ns	
Access time from column address	t AA		35		40		45	ns	
Access time from CAS precharge	^t CPA		40		45		55	ns	
RAS pulse width	^t RAS	70	100,000	80	100,000	100	100,000	ns	10
RAS pulse width (FAST PAGE MODE)	^t RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	^t RSH	20		20		25		ns	
RAS precharge time	tRP	50		60		70		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	^t CSH	70		80		100		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0	100 60 500	ns	
Row address hold time	^t RAH	10		10	1971	15	1.44.1.5	ns	1. 15.454
RAS to column	tRAD .	15	35	15	40	20	55	ns	18
address delay time									
Column address setup time	†ASC	0		0		0		ns	3
Column address hold time	^t CAH	15		15		20		ns	
Column address hold time (referenced to RAS)	^t AR	55		60		75		ns	
Column address to RAS lead time	^t RAL	35		40		55		ns	
Read command setup time	tRCS	0		. 0		0		ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0*		ns	19
CAS to output in Low-Z	†CLZ	0		0		0	<u> </u>	ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	1.52.1		-7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	15	0	20	ns	20, 29
Output disable time	tOD	Ē.	15		15		20	ns	29
Write command setup time	twcs	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to RAS)	tWCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20	7	ns	26
Write command to RAS lead time	tRWL	20		20		25	T	ns	26
Write command to CAS lead time	tCWL	20		20		25		ns	26
Data-in setup time	t _{DS}	0		0		0	1	ns	22
Data-in hold time	tDH.	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60		75	2.2.20	ns	
RAS to WE delay time	†RWD	95		105		135		ns	21
Column address to WE delay time	tAWD	60		65		80		ns	21
CAS to WE delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	tŢ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF	5.5	16		16		16	ms.	
RAS to CAS precharge time	tRPC	10		10		10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5
MASKED WRITE command to RAS setup time	†WRS	0		0	en en salar Por en salar	0		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	26
WE hold time to RAS (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
Mask data to RAS setup time	tMS	0		0		0		ns	26, 27
Mask data to RAS hold time	tMH	15		15		15		ns	26, 27
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	20		25		25		ns	28
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0	,	0	1,160	ns	

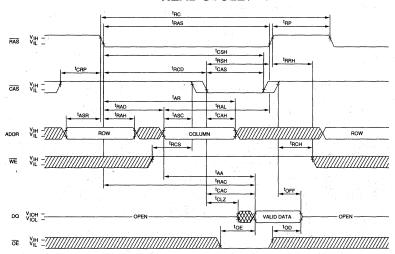
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS -ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IH} (or between V_{IL} and V_{IH}) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is high impedance.
- 12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gate and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

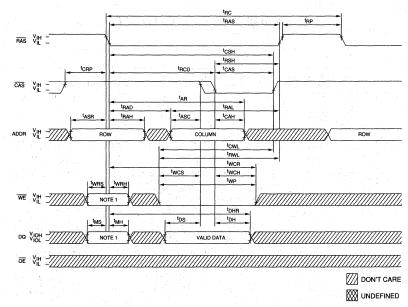
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as $\overline{\text{WE}}$ going LOW.
- 27. MT4C8513 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.



READ CYCLE

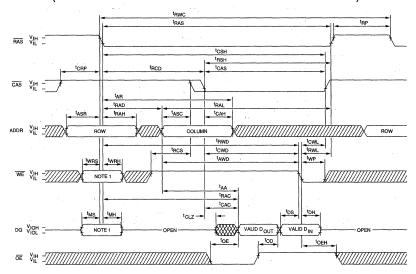


EARLY-WRITE CYCLE

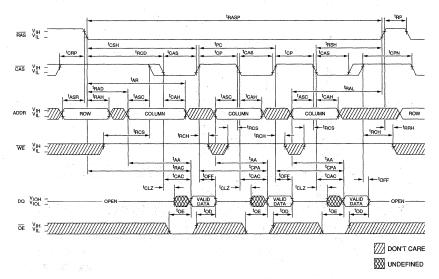


NOTE: 1. Applies to MT4C8513 only; WE and DQ inputs on MT4C8512 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE

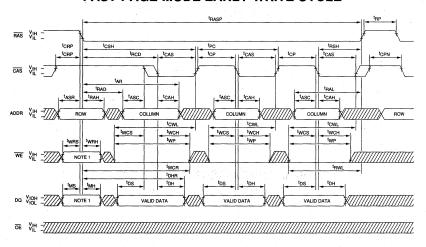


NOTE:

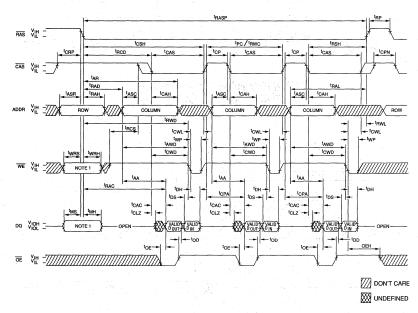
1. Applies to MT4C8513 only; WE and DQ inputs on MT4C8512 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE



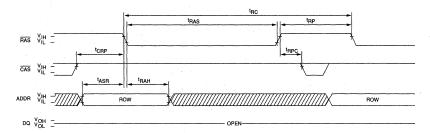
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



Applies to MT4C8513 only; WE and DQ inputs on MT4C8512 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

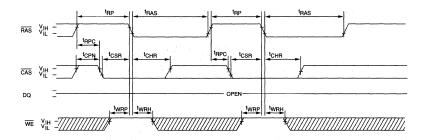


RAS-ONLY REFRESH CYCLE (OE and WE = DON'T CARE)



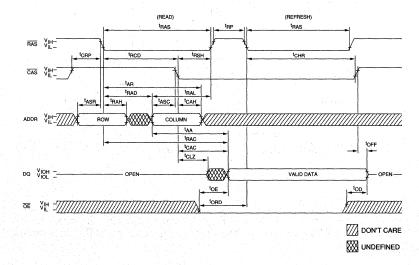
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9; \overline{OE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 24

 $\overline{\text{WE}} = \text{HIGH}; \overline{\text{OE}} = \text{LOW}$





DRAM

512K x 8 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 10 row addresses, nine column addresses
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C8513 only)
- 1,024-cycle refresh distributed accross 128ms
- Low-power, 1mW standby; 350mW active, typical

OPTIONS	MARKING
 Timing 	그는 그리다는 생활이 없다고 하셨다.
70ns access	- 7
80ns access	- 8
100ns access	-10
Masked Write	
Not available	MT4C8512 L
Available	MT4C8513 L
.	

 Packages Plastic SOJ (400 mil) DI Plastic TSOP (400 mil) TG Plastic ZIP (375 mil) Z

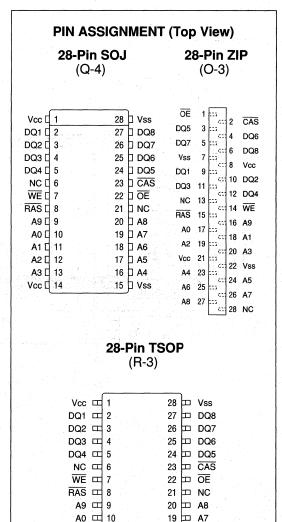
NOTE: Available in die form. Please consult factory for die data sheets.

Part number example: MT4C8512DJ-7 L

GENERAL DESCRIPTION

The MT4C8512/3 L are randomly accessed solid-state memories containing 4,194,304 bits organized in a x8 configuration. Each byte is uniquely addressed through the 19 address bits during READ or WRITE cycles. The address is entered first by \overline{RAS} latching 10 bits (A0-A9) and then CAS latching 9 bits (A0-A8).

The MT4C8513 L has NONPERSISTENT MASKED WRITE allowing it to perform WRITE-PER-BIT accesses.



18 🗆 A6

16 🗆 A4

15 🗆 Vss

17 □ A5

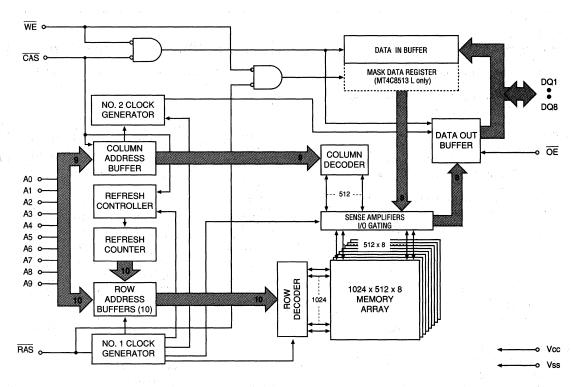
A1 四 11

A2 四 12

A3 🖂 13

Vcc 🖂 14

FUNCTIONAL BLOCK DIAGRAM





MT4C8512/3 L 512K x 8 DRAM

PIN DESCRIPTIONS

SOJ/TSOP PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
8	15	RAS	Input	Row Address Strobe: RAS is used to clock-in the 10 row- address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C8513 L only).
23	-2	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
7	14	WE	Input	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C8513 L).
22		ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WE must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-20, 9	17, 18, 19, 20, 23, 24, 25, 26, 27, 16	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 512K available words.
2-5, 24-27	9, 10, 11, 12, 3, 4, 5, 6	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
6, 21	13, 28	NC	. 11 <u>1</u> 8 90 	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	8, 21	V cc	Supply	Power Supply: +5V ±10%
15, 28	7, 22	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First RAS is used to latch 10 bits (A0-A9) then CAS latches 9 bits (A0-A8).

The CAS control also determines whether the cycle will be a refresh cycle (\overline{RAS} -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

READ or WRITE cycles are selected by WE. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle

(READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

MASKED WRITE ACCESS CYCLE (MT4C8513 L ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of WE at RAS time. A MASKED WRITE is selected when WE is LOW at RAS time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C8513 L MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).



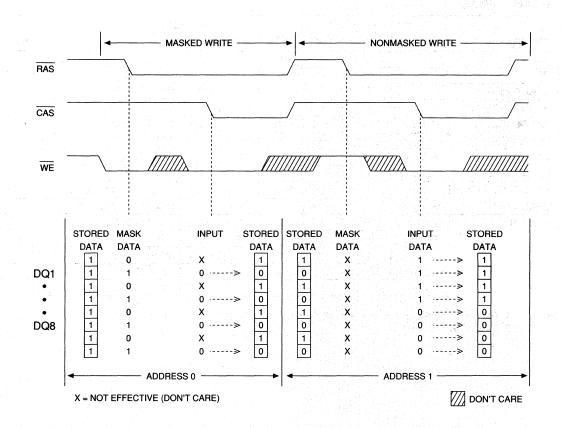


Figure 1
MT4C8513 L MASKED WRITE EXAMPLE

TRUTH TABLE

						ADDRESSES			
FUNCTION		RAS	CAS	WE	ŌĒ	^t R	tC.	DQs	NOTES
Standby		Н	H→X	X	Х	Х	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRES	Н	L	Н	X	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	X	Х	Х	High-Z	
BATTERY BACKUP I	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	

NOTE:

- 1. Data in will be dependent on the mask provided (MT4C8513 L only). Refer to Figure 1.
- 2. EARLY WRITE only.



MT4C8512/3 L 512K x 8 DRAM

ABSOLUTE MAXIMUM RATINGS*

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)		-2	့ 2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		٧	
Output Low Voltage (lout = 4.2mA)	Vol		0.4	V	

		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES	
STANDBY CURRENT: TTL (RAS = CAS = VIH)	lcc1	2	2	2	mA		
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μΑ	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	110	100	90	mA	3, 4, 31	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN); [†] CP, [†] ASC = 10ns)	Icc4	90	80	70	mA	3, 4, 31	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	110	100	90	mA	3, 31	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	110	100	90	mA	3	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE, A0-A9 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	300	300	300	μA	3, 5, 30	

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C ₁₁	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq $T_A \leq$ +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	130		150		180		ns	
READ-WRITE cycle time	tRWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	45		50		55		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	95		100		110		ns	
Access time from RAS	tRAC		70		80	111	100	ns	14
Access time from CAS	^t CAC		20		20		25	ns	15
Output Enable time	^t OE		20		20		25	ns	
Access time from column address	tAA.		35		40		45	ns	
Access time from CAS precharge	^t CPA		40		45		55	ns	
RAS pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		20		25		ns	
RAS precharge time	tRP	50		60		70	100	ns	4057
CAS pulse width	†CAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	^t CSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	1.1.2
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	tASR	0		0	4.5	. 0		ns	8 - F
Row address hold time	tRAH	10		10		15		ns	
RAS to column address delay time	^t RAD	15	35	15	40	20	55	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	15	100000	15		20		ns	
Column address hold time (referenced to RAS)	^t AR	55		60		75		ns	
Column address to RAS lead time	^t RAL	35		40		55		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^t RCH	/0		0		0	No. 1	ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	^t CLZ	0		0		0	1000	ns	



MT4C8512/3 L 512K x 8 DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le +70^{\circ}C$; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			2 2 3
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29
Output disable time	tOD	A.	15		15		20	ns	29
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15	1. 15.3.	20		ns	26
Write command hold time (referenced to RAS)	†WCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20	1.0	ns	26
Write command to RAS lead time	^t RWL	20		20		25		ns	26
Write command to CAS lead time	tCWL	20		20		25		ns	26
Data-in setup time	tDS	0		0	N 10 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60	11 - 12 - 12 1	75		ns	
RAS to WE delay time	tRWD	95		105		135		ns	21
Column address to WE delay time	^t AWD	60		65		80		ns	21
CAS to WE delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	ΙŢ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		128		128	- 17 A - 10	128	ms	
RAS to CAS precharge time	tRPC	10		10		10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	- 5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5
MASKED WRITE command to RAS setup time	tWRS	0		0	e William (1965) g The week in	0		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	26
WE hold time to RAS (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
Mask data to RAS setup time	tMS	0	Tuber 1	0		0		ns	26, 27
Mask data to RAS hold time	tMH	15		15		15		ns	26, 27
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	20		25		25		ns	28
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		О		0		ns	

TECHNOLOGY. If

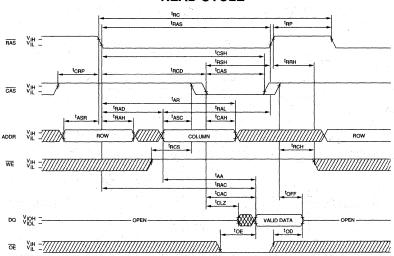
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS -ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5 \text{ns}$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gate and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

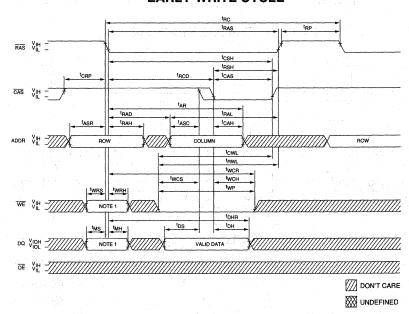
- OFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as $\overline{\text{WE}}$ going LOW.
- 27. MT4C8513 L only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
- 31. Column address changed once while RAS = VIL and CAS = VIH.



READ CYCLE



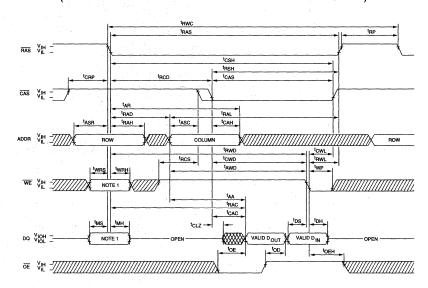
EARLY-WRITE CYCLE



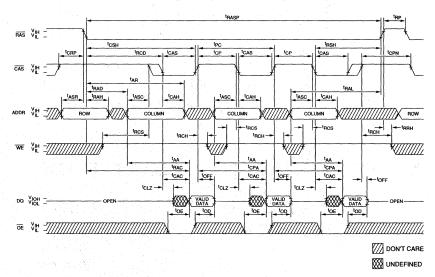
NOTE:

1. Applies to MT4C8513 L only; WE and DQ inputs on MT4C8512 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE

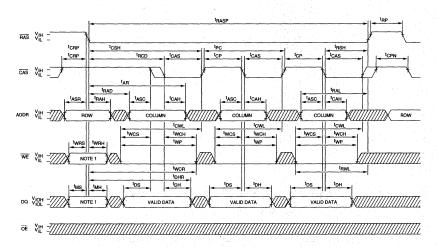


NOTE:

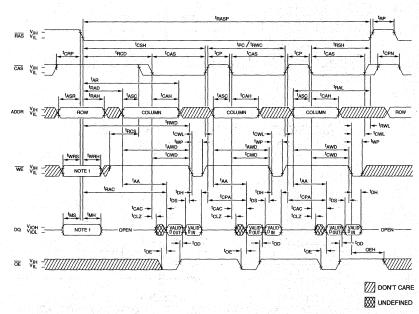
1. Applies to MT4C8513 L only; WE and DQ inputs on MT4C8512 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE

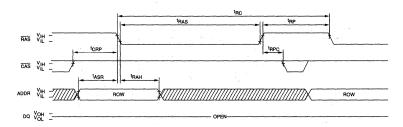


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



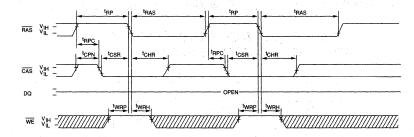
NOTE: 1. Applies to MT4C8513 L only; WE and DQ inputs on MT4C8512 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

RAS-ONLY REFRESH CYCLE (OE and WE = DON'T CARE)



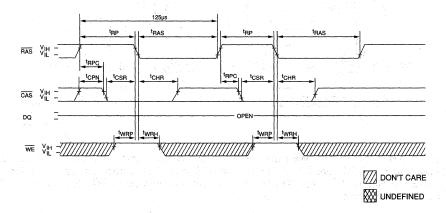
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9; \overline{OE} = DON'T CARE)$



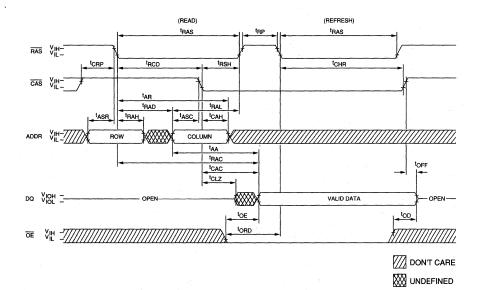
BATTERY BACKUP REFRESH CYCLE

 $(A0-A9; \overline{OE} = DON'T CARE)$



NEW WIDE DRAM

HIDDEN REFRESH CYCLE 24 $\overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

2 MEG x 8 DRAM

5.0V. FAST PAGE MODE (MT4C2M8A1/2) 3.0/3.3V, FAST PAGE MODE (MT4LC2M8A1/2)

FEATURES

OPTIONS

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 12 row, nine column addresses (64ms)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only $\pm 10\%$ power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are fully TTL compatible
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MADICINIC

- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 only)

OPTIONS	MAKKING
• Timing 60ns access 70ns access 80ns access	- 6 - 7 - 8
• Power Supply 5V ±10% only 3.0/3.3V ±10% only	4C 4LC
 Masked Write Not available Available 	A1 A2
Packages Plastic 28-pin SOJ (400 mil) Plastic 28-pin TSOP (400 mil) Plastic 32-pin SOJ (400 mil) Plastic 32-pin TSOP (400 mil)	DJ TG DL TL

NOTE: Available in die form. Please consult factory for die data sheets.

PART DESCRIPTION

MT4C2M8A1	5V, non-masked write
MT4C2M8A2	5V, masked write
MT4LC2M8A1	3.0/3.3V, non-masked write
MT4LC2M8A2	3.0/3.3V, masked write

GENERAL DESCRIPTION

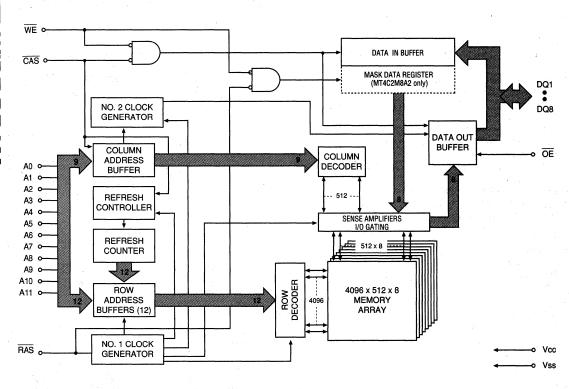
The MT4C2M8A1/2 and MT4LC2M8A1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8A1/2 and the MT4LC2M8A1/2 are the same DRAM versions except that the MT4LC2M8A1/2 are low voltage versions of the

28-Pi (Q	n SOJ -4)	28-Pin TSOP (R-3)			
(\alpha)		3)		
Vcc 🛘 1	28 D Vss	Vcc III 1	28 🗆 Vss		
Vcc [1 DQ1 [2	28 DQ8	DQ1 III 2	27 III DQ8		
DQ2 [] 3	26 DQ7	DQ2 III 3	26 H DQ		
DQ2 [] 3	25 D DQ6	DQ3 III 4	25 ED DQ		
DQ3 [] 4 DQ4 [] 5	24 DQ5	DQ4 III 5	24 ED DQ		
	24 DQ5 23 CAS	WE H 6	23 III CAS		
		RAS III 7	22 H OE		
RAS [7	22 D OE	*A11 = 8	21 III A9		
*A11 [8	21 A9	A10 🖽 9	20 H A9		
A10 [9	20 A8	A10 🖽 9	19 D A7		
A0 [10	19 D A7	A1 11	18 III A6		
A1 [] 11	18 A6	A2 11 12	17 T1 A5		
A2 [12	17 D A5	A2 112 A3 1113			
A3 🛘 13	16 A4				
Vcc 🛚 14	15 D Vss	Vcc □ 14	15 JU Vss		
32-Pi	n SOJ	32-Pir	TSOP		
(Q	-5)	(R	-4)		
Vcc [1	32 🛘 Vss	Vcc □ 1	32 🎞 Vss		
DQ1 [2	31 DQ8	DQ1 🞞 2	31 垣 DQ		
DQ2 [3	30 DQ7	DQ2 III 3	30 🞞 DQ		
DQ3 🛘 4	29 DQ6	DQ3 🕮 4	29 🞞 DQ		
DQ4 🛭 5	28 DQ5	DQ4 🖂 5	28 🞞 DQ		
NC 6	27 🗆 CAS	NC III 6	27 🖂 CA		
WE 0 7	26 DE	WE □ 7	26 🞞 OE		
RAS [8	25 D NC	RAS III 8	25 🞞 NC		
NC 9	24 DNC	NC III 9	24 🖽 NC		
*A11 🛭 10	23 A9	*A11 円 10	23 PA9		
A10 [11	22 A8	A10 円 11	22 🞞 A8		
A0 [12	21 A7	A0 🖂 12	21 PD A7 20 PD A6		
A1 [] 13	20 A6	A1 🖂 13			
A2 [14	19 A5	A2 II 14 A3 III 15	19 🖽 A5		
A3 🛘 15	18 🛭 A4	A3 LL 10	10 HJ A4		

MT4C2M8A1/2. The MT4LC2M8A1/2 are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8A1/ 2 also apply to the MT4LC2M8A1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS latching 12 bits (A0-11) and then CAS latching 9 bits (A0-A9).

The MT4C2M8A2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM 4,096 ROWS





MT4(L)C2M8A1/2 2 MEG x 8 DRAM

PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	3 8	RAS	Input	Row Address Strobe: RAS is used to clock-in the 12 row- address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C2M8A2 only).
23	27	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	WE	Input	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C2M8A2).
22	26	ŌĒ	Input	Output Enable: \overline{OE} enables the output buffers when taken LOW during a READ access cycle. \overline{RAS} and \overline{CAS} must be LOW and \overline{WE} must be HIGH before \overline{OE} will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V cc	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First RAS is used to latch 12 bits (A0-A11) then \overline{CAS} latches 9 bits (A0-A8).

The CAS control also determines whether the cycle will be a refresh cycle (RAS-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

READ or WRITE cycles are selected by WE. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-12) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-11) are executed at least every 64ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C2M8A2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of WE at RAS time. A MASKED WRITE is selected when WE is LOW at RAS time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2 MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

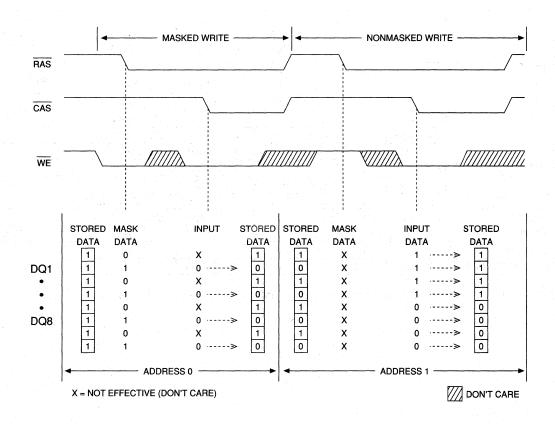


Figure 1 MT4C2M8A2 MASKED WRITE EXAMPLE

2-35

NEW WIDE DRAM

TRUTH TABLE

	:					ADDRE	SSES		
FUNCTION		RAS	CAS	WE	0E	t _R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	Х	High-Z	
READ		L	L	Н	L.	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRES	Н	L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	

NOTE:

- 1. Data in will be dependent on the mask provided (MT4C2M8A2 only). Refer to Figure 1.
- 2. EARLY WRITE only.



MT4(L)C2M8A1/2 2 MEG x 8 DRAM

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	li	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		V	
Output Low Voltage (IouT = 2.1mA)	Vol		0.4	٧	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C $\leq T_A \leq$ 70°C; Vcc = 3.0/3.3V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	٧	1, 31
Input High (Logic 1) Voltage, All Inputs	Vih	2.0	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VıL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ Vcc (All other pins not under test = 0V)	1.	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2mA)	Vон	2.4		V	
Output Low Voltage (lout = 2mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0° C $\leq T_{\Delta} \leq 70^{\circ}$ C; Vcc = 5V ±10%)

(Notes. 1, 3, 4, 0, 7, 30) (0.0 \leq 1 _A \leq 70.0, vcc = 3v \pm 10%)			MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: TTL $(\overline{RAS} = \overline{CAS} = V_{IH})$	lcc1	2	2	2	mA		
STANDBY CURRENT: CMOS $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	1	1	1	mA	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	110	100	90	mA	3, 4, 32	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC (MIN); tCP, tASC = 10ns)	lcc4	80	70	60	mA	3, 4, 32	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: ^t RC = ^t RC (MIN))	lcc5	110	100	90	mA	3, 32	
REFRESH CURRENT: CAS -BEFORE- RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	110	100	90	mA	3	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) $(0^{\circ}C < T_{*} < 70^{\circ}C \cdot V_{CC} = 3.0/3.3V + 10\%)$

(Notes: 1, 3, 4, 6, 7, 31) (0°C $\leq 1_A \leq 70$ °C; $\sqrt{6}$ C = 3.0/3.3 $\sqrt{10}$		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS} = \overline{CAS} = V_{IH}$)	lcc1	1	1	1	mA	
STANDBY CURRENT: CMOS $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	400	400	400	μΑ	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	80	70	60	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ¹PC = ¹PC (MIN); ¹CP, ¹ASC = 10ns)	lcc4	60	50	40	mA	3, 4, 32
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	80	70	60	mA	3, 32
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	80	70	60	mA	3



MT4(L)C2M8A1/2 2 MEG x 8 DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	Cıı	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_{A} \le +70^{\circ}C)$

AC CHARACTERISTICS	-6		-7		-8		100110	11	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	155	4	180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	35		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	85		95		100		ns	
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Output Enable	^t OE		15		15		15	ns	
Access time from column address	†AA		30		35	Y N. P	40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10	- 111 (ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	†RCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5	and and	5		5	The state of	ns	
Row address setup time	†ASR	0	272.0	0		0	1 1 1 (418)	ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	5
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	^t CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_A \le +70^{\circ}C)$

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN MAX		MIN MAX		MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0		0		0		ns	21, 26
Write command hold time	tWCH	10		15		15		ns	26
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	^t RWL	15		20		20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	^t DH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Column address to WE delay time	tAWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	^t T	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^t REF		64	16.00	64		64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		15		15		ns	28



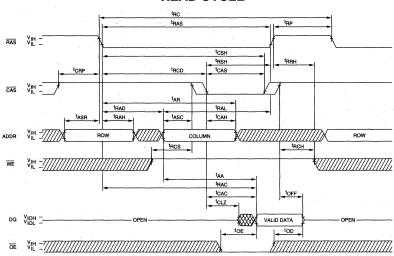
MT4(L)C2M8A1/2 2 MEG x 8 DRAM

NOTES

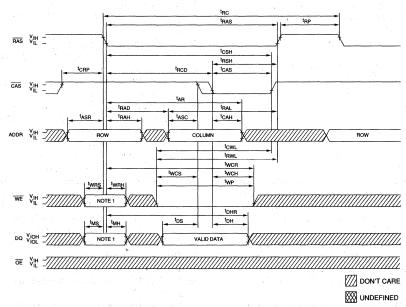
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is high impedance.
- 12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$ and $\overline{OE} = HICH$
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as WE going LOW.
- 27. MT4C2M8A2 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
- 31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 32. Column address changed once while $\overline{RAS} = VIL$ and $\overline{CAS} = VIH$.





EARLY-WRITE CYCLE

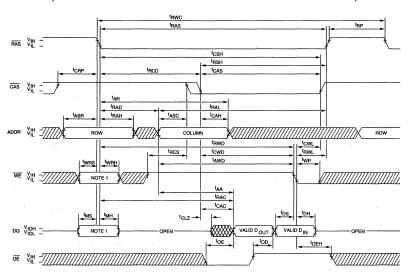


NOTE:

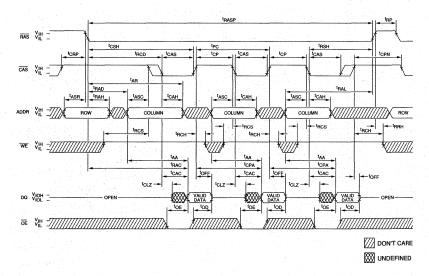
1. Applies to MT4C2M8A2 only; WE and DQ inputs on MT4C2M8A1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



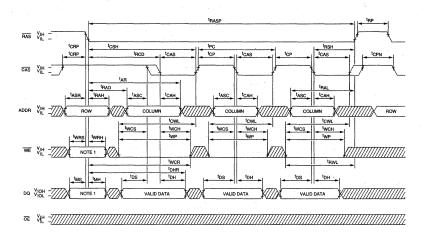
FAST-PAGE-MODE READ CYCLE



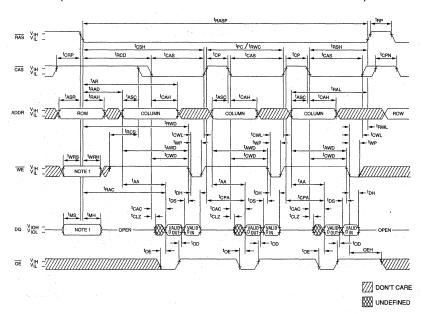
NOTE:

1. Applies to MT4C2M8A2 only; WE and DQ inputs on MT4C2M8A1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

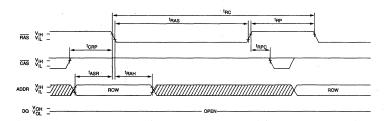


NOTE:

1. Applies to MT4C2M8A2 only; WE and DQ inputs on MT4C2M8A1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

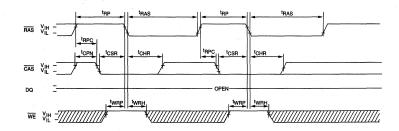
NEW WIDE DRAM

RAS-ONLY REFRESH CYCLE (OE and WE = DON'T CARE)

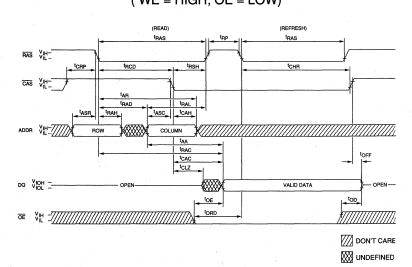


CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A11; \overline{OE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 24 (WE = HIGH; OE = LOW)





DRAM

2 MEG x 8 DRAM

5.0V FAST PAGE MODE (MT4C2M8B1/2) 3.0/3.3V, FAST PAGE MODE (MT4LC2M8B1/2)

FEATURES

- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 11 row, 10 column addresses (32ms);
- 2,048-cycle refresh (4,096-cycle refresh available as MT4(L)C2M8B1/2)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C2M8B2 only)

OPTIONS	MARKING
• Timing 60ns access 70ns access 80ns access	- 6 - 7 - 8
• Power Supply 5V ±10% only 3.0/3.3V ±10% only	4C 4LC
 Masked Write Not available Available 	B1 B2
Packages Plastic 28-pin SOJ (400 mil) Plastic 28-pin TSOP (400 mil) Plastic 32-pin SOJ (400 mil) Plastic 32-pin TSOP (400 mil)	DJ TG DL TL

NOTE: Available in die form. Please consult factory for die data sheets.

PART DESCRIPTION

MT4C2M8B1	5.0V, non-masked write
MT4C2M8B2	5.0V, masked write
MT4LC2M8B1	3.0V/3.3V, non-masked write
MT4LC2M8B2	3.0V/3.3V, masked write

GENERAL DESCRIPTION

The MT4C2M8B1/2 and MT4LC2M8B1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8B1/2 and the MT4LC2M8B1/2 are the same DRAM versions except that the MT4LC2M8B1/2 are low voltage versions of the

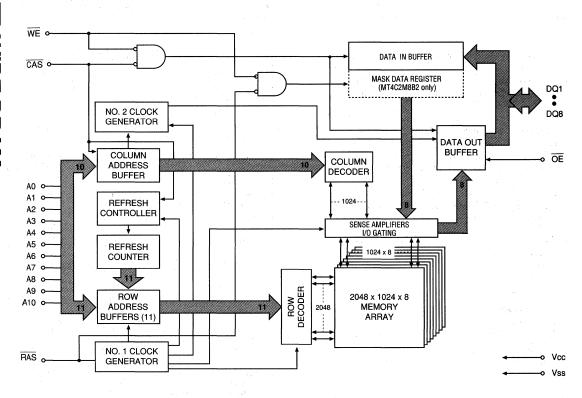
PIN ASSIGNM	ENT (Top View)
28-Pin SOJ (Q-4)	28-Pin TSOP (R-3)
Vcc □ 1 28 □ Vss DO1 □ 2 27 □ DQ8 DO2 □ 3 26 □ DQ7 DO3 □ 4 25 □ DQ6 DQ4 □ 5 24 □ DQ5 WE □ 6 23 □ CAS FIAS □ 7 22 □ OE *NC □ 8 21 □ A9 A10 □ 9 20 □ A8 A0 □ 10 19 □ A7 A1 □ 11 18 □ A6 A2 □ □ Z □ A5 A6 A2 □ □ Z □ A5 A6 A2 □ □ A □ A5 A6 A3 □ □ A5 A6 □ A5 A5 □ □ A5 □ A5 □ A5 A6 □ □ A5 □ A5 □ A5 A6 □ □ A5 □ A5 □ A5 A7 □ □ A5 □ A5 □ A5 A8 □ □ A5	VCC □ 1 28 □ Vss DO1 □ 2 27 □ DQ8 DQ2 □ 3 26 □ DQ7 DQ3 □ 4 25 □ DQ6 DQ4 □ 5 24 □ DQ5 WE □ 6 23 □ CAS RAS □ 7 22 □ OE **NC □ 8 21 □ A9 A10 □ 9 20 □ A8 A0 □ 10 19 □ A7 A1 □ 11 18 □ A6 A2 □ 12 17 □ A5 A3 □ 13 16 □ A4 VCC □ 14 15 □ Vss
32-Pin SOJ	32-Pin TSOP
Vcc 1 32 Vss DO1 2 31 DO8 DO2 3 30 DO7 D03 4 29 DO6 D04 5 28 DO5 NC 6 27 CAS WE 7 26 OE FAS 8 25 NC NC 9 24 NC NC 10 23 A8 A10 11 22 A8 A0 12 21 A7 A1 13 20 A6 A2 14 19 A5 A3 15 18 A4 Vcc 16 17 Vss	(R-4) Voc II 1 32 II Vss DQ1 III 2 31 II DQ8 DQ2 II 3 30 II DQ7 DQ3 III 4 29 III DQ6 DQ4 III 5 28 III DQ5 NG III 6 27 III GAS WE II 7 26 III OE RAS II 8 25 III NC NG II 9 24 III NC NG II 10 23 III A9 A10 II 11 22 III A7 A1 II 13 20 III A6 A2 II 14 19 A5 A3 II 15 18 III A4 Voc III 16 17 III Vss

MT4C2M8B1/2. The MT4LC2M8B1/2 are designed to operate in either a 3.0V $\pm 10\%$ or a 3.3V $\pm 10\%$ memory system. All further references made for the MT4C2M8B1/2 also apply to the MT4LC2M8B1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by \overline{RAS} latching 11 bits (A0-A10) and then \overline{CAS} latching 10 bits (A0-A10).

*A11 on 12 row address version

The MT4C2M8B2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM 2,048 ROWS





PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
	8	RAS	Input	Row Address Strobe: RAS is used to clock-in the 11 row- address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C2M8B2 only).
23	27	CAS	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6 16 16 16 16 16 16 16 16 16 16 16 16 16	7	WE	Input	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C2M8B2).
22	26	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WE must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9	12-15, 18-23, 11	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
8	6, 9, 24, 25, 10	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	Vcc	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	Vss	Supply	Ground

2 MEG x 8 DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First RAS is used to latch 11 bits (A0-A10) then CAS latches 10 bits (A0-A9).

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle ($\overline{\text{READ}}$, WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW.

READ or WRITE cycles are selected by \overline{WE} . A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High- Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct

state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

MASKED WRITE ACCESS CYCLE (MT4C2M8B2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when \overline{WE} is LOW at \overline{RAS} time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8B2 MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).

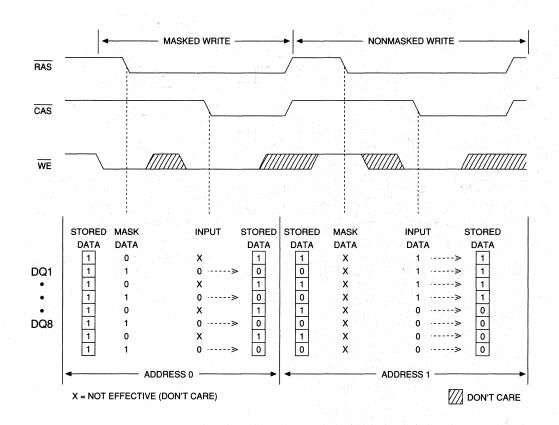


Figure 1
MT4C2M8B2 MASKED WRITE EXAMPLE

TRUTH TABLE

						ADDRE	SSES		
FUNCTION		RAS	CAS	WE	0E	^t R	tC	DQs	NOTES
Standby		Н	H→X	. X	Х	Х	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	٦	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	. L	H→L	L	Х	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRES	Н	L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	

2. EARLY WRITE only.

^{1.} Data in will be dependent on the mask provided (MT4C2M8B2 only). Refer to Figure 1.



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	, 1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	li	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (lout = 2.3mA)	Vol	A. A.	0.4	٧	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C \leq T_A \leq 70°C; Vcc = 3.0/3.3V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	Viн	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	. 1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ Vcc (All other pins not under test = 0V)		-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (laur 2mA)	Vон	2.4		V	
Output High Voltage (Ιουτ = -2mA) Output Low Voltage (Ιουτ = 2mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C $\le 1_A \le 70$ °C; Vcc = 5V ± 10 %)	en grand de la Agranda de La Carta de la Carta de la Agranda de la	MAX					
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: TTL (RAS = CAS = ViH)	Icc1	2	2	2	mA		
STANDBY CURRENT: CMOS $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	1	1	1	mA	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	140	130	120	mA	3, 4, 32	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN); [†] CP, [†] ASC = 10ns)	Icc4	100	90	80	mA	3, 4, 32	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	140	130	120	mA	3, 32	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	140	130	120	mA	3	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

2001 211/11110 01 2011 10/1110110 1 011 010/0101 1 211011						
(Notes: 1, 3, 4, 6, 7, 31) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 3.0/3.3V \pm 10\%)$		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL $(\overline{RAS} = \overline{CAS} = Vih)$	lcc1	1	1	1	mA	
STANDBY CURRENT: CMOS $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	400	400	400	μА	25
OPERATING CURRENT: Random READ/WRIT Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	Іссз	100	90	80	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ¹PC = ¹PC (MIN); ¹CP, ¹ASC = 10ns)	Icc4	75	65	55	mA	3, 4, 32
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: [†] RC = [†] RC (MIN))	lcc5	100	90	80	mA	3, 32
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	100	90	80	mA	3



CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	Cıı	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C ₁₂	7	pF	2
Input/Output Capacitance: DQ	Cio	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_{A} \le +70^{\circ}C)$

AC CHARACTERISTICS PARAMETER		-6			-7		-8	4 2	
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	†RWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	35		40		40		ns	en en san j
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	85		95		100		ns	
Access time from RAS	^t RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Output Enable	^t OE	· · · · · · · · · · · · · · · · · · ·	15		15		15	ns	
Access time from column address	^t AA		30	4 . *	35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	28
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	Sir sais.
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	1.02%
CAS hold time	^t CSH	60		70		80		ns	a service
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0	1.7	ns	19.00
Row address hold time	tRAH .	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10	1	15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		O		ns	19
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20, 29

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_A \le +70^{\circ}C)$

AC CHARACTERISTICS			6		-7		8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		0		ns	21, 29
Write command hold time	†WCH	10		15		15		ns	26
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	^t RWL	15		. 20		20		ns	26
Write command to CAS lead time	†CWL	15		20		20		ns	26
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	^t DH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	^t RWD	85		95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	·Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32		32	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	5		5		5	1 N. 1	ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15	4	15		15		ns	5
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	^t WRH	15	200	15		15		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		15		15		ns	28

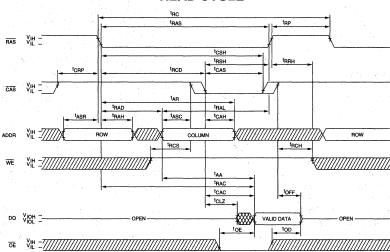


NOTES

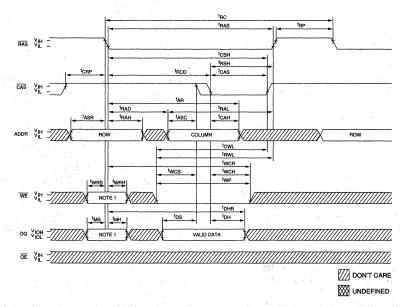
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If \overline{CAS} = VIH, data output is high impedance.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if \overline{OE} is LOW then taken HIGH before \overline{CAS} goes HIGH, Q goes open. If \overline{OE} is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as $\overline{\text{WE}}$ going LOW.
- 27. MT4C2M8B2 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
- 31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 32. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.

READ CYCLE



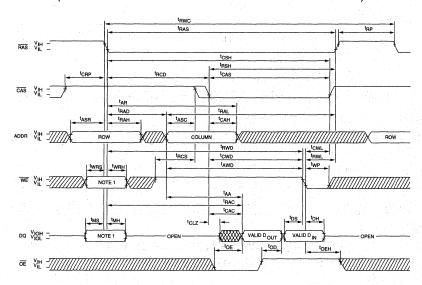
EARLY-WRITE CYCLE



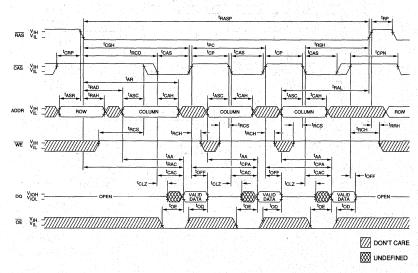
NOTE: 1. Applies to MT4C2M8B2 only; WE and DQ inputs on MT4C2M8B1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



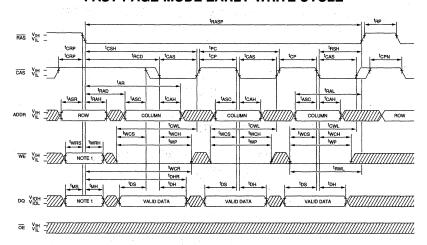
FAST-PAGE-MODE READ CYCLE



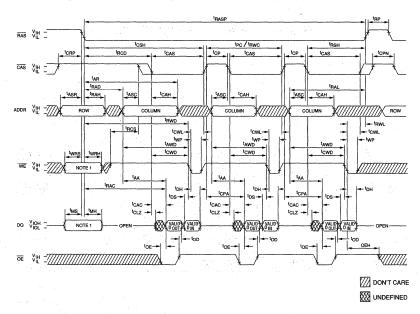
NOTE:

1. Applies to MT4C2M8B2 only; WE and DQ inputs on MT4C2M8B1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



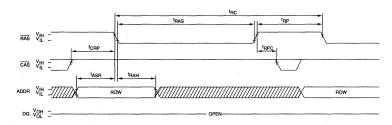
NOTE:

1. Applies to MT4C2M8B2 only; WE and DQ inputs on MT4C2M8B1 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



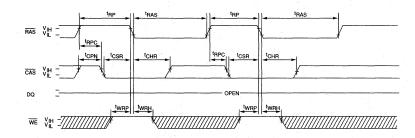
RAS-ONLY REFRESH CYCLE

 $(\overline{OE} \text{ and } \overline{WE} = DON'T CARE)$



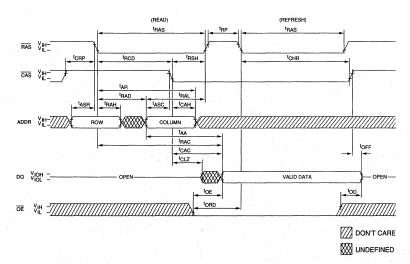
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A10; \overline{OE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 24

 $\overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

2 MEG x 8 DRAM

5.0V, SELF REFRESH (MT4C2M8A1/2 S) 3.0/3.3V, SELF REFRESH (MT4LC2M8A1/2 S)

FEATURES

- SELF REFRESH, i.e. "Sleep Mode"
- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 12 row, nine column addresses (512ms)
- High-performance, CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 S only)
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2 S)
- Low power, 2mW standby; 400mW active, typical (5V)

OPTIONS	MARKING
• Timing 60ns access 70ns access 80ns access	- 6 - 7 - 8
• Power Supply 5V ±10% only 3.0/3.3V ±10% only	4C 4LC
 Masked Write Not available Available 	A1 S A2 S
 Packages Plastic 28-pin SOJ (400 Plastic 28-pin TSOP (4 Plastic 32-pin SOJ (400 Plastic 32-pin TSOP (4 	00 mil) TG mil) DL

NOTE: Available in die form. Please consult factory for die data sheets.

Part Number Example: MT4C2M8A1DJ-7 S

PART DESCRIPTION

MT4C2M8A1S	5V, non-masked write
MT4C2M8A2 S	5V, masked write
MT4LC2M8A1 S	3.0/3.3V, non-masked write
MT4LC2M8A2 S	3.0/3.3V, masked write

GENERAL DESCRIPTION

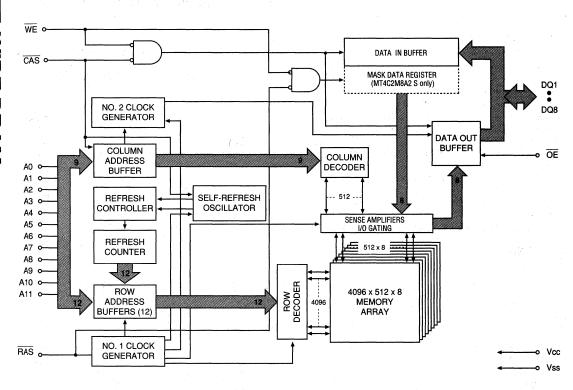
The MT4C2M8A1/2 S and MT4LC2M8A1/2 S are randomly accessed solid-state memories containing

PIN ASSIGNMI	ENT (Top View)
28-Pin SOJ (Q-4)	28-Pin TSOP (R-3)
Vcc	Vcc □ 28 □ Vss DO1 □ 27 □ DO8 DO2 □ 3 26 □ DO7 DO3 □ 4 25 □ DO6 DO4 □ 5 24 □ DO6 WE □ 6 23 □ CAS RAS □ 7 22 □ OE 'A11 □ 9 20 □ A8 A0 □ 10 19 □ A7 A1 □ 11 18 □ A6 A2 □ 12 17 □ A5 A3 □ 12 17 □ A5 A3 □ 13 16 □ A Vcc □ 14 15 Ji Ves
32-Pin SOJ (Q-5)	32-Pin TSOP
(Q-3)	(R-4)
Voc 0 1 32 Vss DQ1 0 3 30 DQ8 DQ2 0 3 30 DQ7 DQ3 0 4 29 DQ6 DQ4 0 5 28 DQ5 NC 0 6 27 DG5 WE 0 7 26 DG RAS 1 8 25 DNC NC 0 9 24 DNC 'A11 0 10 23 A9 A10 1 11 22 A8 A0 1 12 21 A7 A1 0 13 20 A6 A2 0 14 19 A5 A3 1 15 18 A4 Voc 0 6 17 Vss	Vcc □ 1 32 □ Vss DO1 □ 2 31 □ DO8 DO2 □ 3 30 □ DO7 DO3 □ 4 29 □ DO6 DO4 □ 5 28 □ DO5 WE □ 7 26 □ ŌE RAS □ 8 25 □ NC NC □ 9 24 □ NC □ 11 □ 22 □ A8 A1 □ □ 11 22 □ A8 A2 □ 14 □ 13 20 □ A6 A2 □ 14 □ 15 □ A5 A3 □ 15 18 □ A4 Vcc □ 16 17 □ Vss

16,777,216 bits organized in a x8 configuration. The MT4C2M8A1/2 S and the MT4LC2M8A1/2 S are the same DRAM versions except that the MT4LC2M8A1/2 S are low voltage versions of the MT4C2M8A1/2 S. The MT4LC2M8A1/2 S are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8A1/2 S also apply to the MT4LC2M8A1/2 S, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS latching 12 bits (A0-11) and then CAS latching 9 bits (A0-A9).

The MT4C2M8A2 S has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM 4,096 ROWS





PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8 , 6, 7	RAS	Input	Row Address Strobe: RAS is used to clock-in the 12 row- address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C2M8A2 S only).
23	27	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	WE	Input	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C2M8A2 S).
22	26	ŌĒ	Input	Output Enable: \overline{OE} enables the output buffers when taken LOW during a READ access cycle. \overline{RAS} and \overline{CAS} must be LOW and \overline{WE} must be HIGH before \overline{OE} will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	Vcc	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First RAS is used to latch 12 bits (A0-A11) then CAS latches 9 bits (A0-A8).

The CAS control also determines whether the cycle will be a refresh cycle (\overline{RAS} -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

READ or WRITE cycles are selected by WE. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-12) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-11) are executed at least every 512ms, regardless of sequence. The CAS-BEFORE-RAS refresh

cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 512ms.

MASKED WRITE ACCESS CYCLE (MT4C2M8A2 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of WE at RAS time. A MASKED WRITE is selected when \overline{WE} is LOW at \overline{RAS} time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2S MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

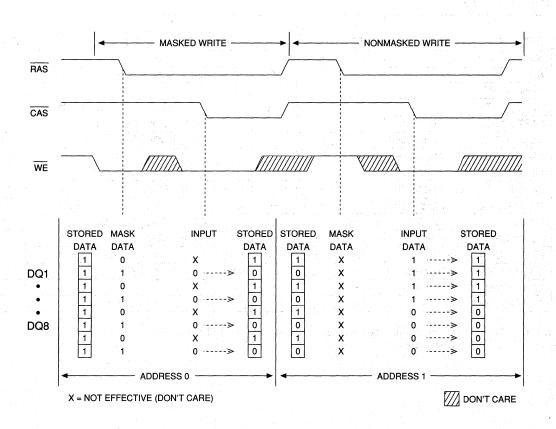


Figure 1
MT4C2M8A2 S MASKED WRITE EXAMPLE

NEW **W** WIDE DRAM

TRUTH TABLE

						ADDRESSES			
FUNCTION		RAS	CAS	WE	ŌĒ	t _R	tC	DQs	NOTES
Standby		Н	H→X	X	X	Х	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	· L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	-
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRES	Н	L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	X	Х	Х	High-Z	
BATTERY BACKUP	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	
SELF REFRESH		H→L	L	Н	. X	Х	Х	High-Z	

NOTE:

- 1. Data in will be dependent on the mask provided (MT4C2M8A2 S only). Refer to Figure 1.
- 2. EARLY WRITE only.



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0° C $\leq T_A \leq 70^{\circ}$ C; Vcc = 5V $\pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)		-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	YE.
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 2.3InA)	Vol		0.4	٧	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0° C $\leq T_{\Delta} \leq 70^{\circ}$ C; Vcc = 3.0/3.3V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = $0V$)	li.	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Ιουτ = -2mA)	Vон	2.4	0.4	V	
Output Low Voltage (Iout = 2mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

Notes: 1, 3, 4, 6, 7, 30) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$		г	BB 8 V		1 .	
	,	<u> </u>	MAX		ļ	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μΑ	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current (FAS = Vil., CAS, Address Cycling: tPC = tPC (MIN); tCP, tASC = 10ns)	Icc4	80	70	60	mA	3, 4, 32
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: tRC = tRC (MIN))	lcc5	110	100	90	mA	3, 32
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc6	110	100	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = [†] RAS (MIN) to 300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), [†] RC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	300	300	300	μА	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with RAS ≥ [†] RASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	lcc8	300	300	300	μА	5



DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C \leq T_A \leq 70°C; Vcc = 3.0/3.3V \pm 10%)

A = 1.5 °C, 1.			MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: TTL (RAS = CAS = Vih)	lcc1	1	1	1	mA		
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	80	80	80	μА	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	80	70	60	mΑ	3, 4, 32	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN); [†] CP, [†] ASC = 10ns)	lcc4	60	50	40	mA	3, 4, 32	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: tRC = tRC (MIN))	lcc5	80	70	60	mA	3, 32	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	80	70	60	mA	3, 5	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	100	100	100	μА	3, 30	
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with RAS ≥ tRASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	Icc8	100	100	100	μА	5	



CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C ₁₁	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	Cı2	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_A \le +70^{\circ}C)$

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	- 1 T
READ-WRITE cycle time	^t RWC	155		180		200		ns	
FAST-PAGE-MODE	^t PC	35		40		40		ns	
READ or WRITE cycle time			11						
FAST-PAGE-MODE	^t PRWC	85		95		100		ns	
READ-WRITE cycle time					1				
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15
Output Enable	^t OE		15		15		15	ns	
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40	-	45	ns	
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	^t RP	40	1	50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	,
RAS to CAS delay time	^t RCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5	-	5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10	1	ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0	<u> </u>	ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0	:	ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	0		0	1	0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20, 29



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_{A} \le +70^{\circ}C)$

AC CHARACTERISTICS PARAMETER		-6		-7		-8			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	twcs	0		0	N 4	0		ns	21, 26
Write command hold time	tWCH	10		. 15		15		ns	26
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	tRWL	15		20		20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26
Data-in setup time	^t DS	0		0	100	0	Part 1	ns	22
Data-in hold time	^t DH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	8
RAS to WE delay time	tRWD	85		95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	·Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^t REF		512		512		512	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15	* -	15		15	1000000	ns	5
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10) 1210 a	10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29
OE hold time from WE during READ-MODIFY-WRITE cycle	†OEH	15		15		15		ns	28
RAS pulse width during SELF REFRESH cycle	†RASS	100		100		100	6 ST	μs	
RAS precharge time during SELF REFRESH cycle	tRPS	150	. Biai	150		150		ns	
CAS hold time during SELF REFRESH cycle	tCHS	-70		-70		-70		ns	SECTION SECTION

.

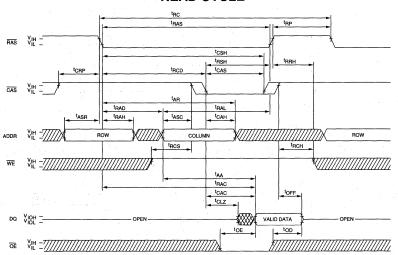
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS -ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF.
- 14. Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output

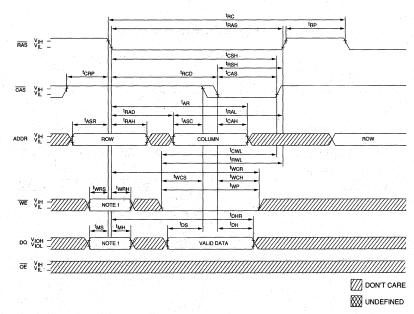
- achieves the open circuit condition, not a reference to Voh or Vol.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- .24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as $\overline{\text{WE}}$ going LOW.
- 27. MT4C2M8A2 S only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If <u>CAS</u> goes HIGH first, <u>OE</u> becomes a "don't care." If <u>OE</u> goes HIGH and <u>CAS</u> stays LOW, <u>OE</u> is not a don't care; and the DQs will provide the previously read data if <u>OE</u> is taken back LOW (while <u>CAS</u> remains LOW).
- 30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
- 31. The 5V version is restricted to operate between 4.5 V and 5.5V only.
- 32. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 33. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.



READ CYCLE

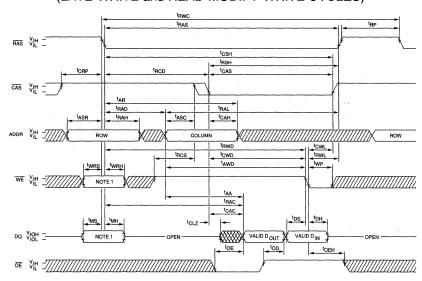


EARLY-WRITE CYCLE

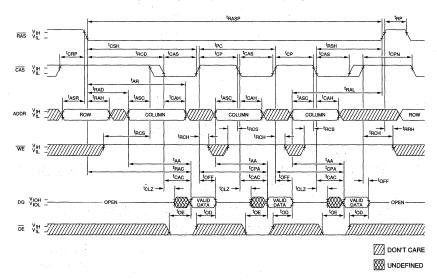


1. Applies to MT4C2M8A2 S only; WE and DQ inputs on MT4C2M8A1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



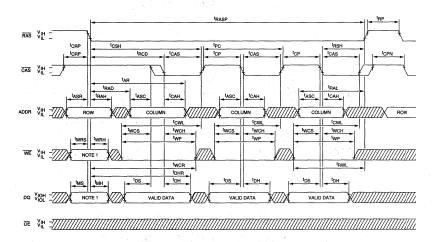
FAST-PAGE-MODE READ CYCLE



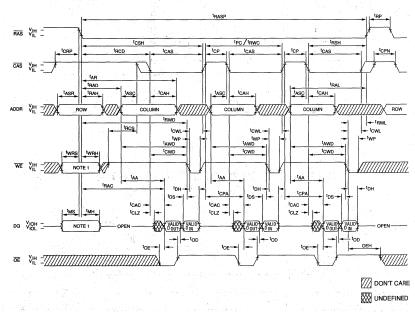
NOTE: 1. Applies to MT4C2M8A2 S only; WE and DQ inputs on MT4C2M8A1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE



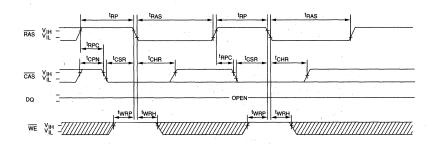
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C2M8A2 S only; WE and DQ inputs on MT4C2M8A1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

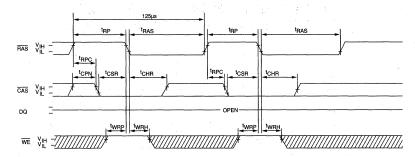
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A11; OE = DON'T CARE)



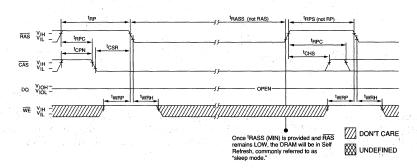
BATTERY BACKUP REFRESH CYCLE

(A0-A11; \overline{OE} = DON'T CARE)



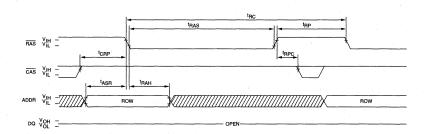
SELF REFRESH CYCLE ("SLEEP MODE")

 $(A0-A11; \overline{OE} = DON'T CARE)$



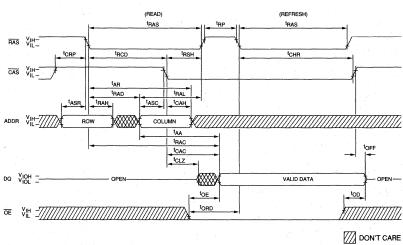


RAS-ONLY REFRESH CYCLE $(\overline{OE} \text{ and } \overline{WE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 24

 $\overline{WE} = HIGH; \overline{OE} = LOW)$



₩ UNDEFINED



DRAM

2 MEG x 8 DRAM

5.0V SELF REFRESH (MT4C2M8B1/2 S) 3.0/3.3V, SELF REFRESH (MT4LC2M8B1/2 S)

FEATURES

- SELF REFRESH, i.e. "Sleep Mode"
- Industry standard x8 pinouts, timing, functions and packages
- Address entry: 11 row, 10 column addresses (256ms);
- High-performance, CMOS silicon-gate process
- Single +5V only or 3/3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8B2 S only)
- 2,048-cycle refresh (4,096-cycle refresh available as MT4(L)C2M8A1/2 S)
- Low power, 2mW standby; 400mW active, typical (5V)

OPTIONS	MARKING	
Timing		
60ns access	- 6	
70ns access	ji ka - 7 - 4 - 1 - 4 - 4	
80ns access	- 8	
Power Supply		
5V ±10% only	4C	
3.0/3.3V ±10% only	4LC	
Masked Write		
Not available	B1 S	
Available	B2 S	
• Packages		
Plastic 28-pin SOJ (400 mil)	DI	
Plastic 28-pin TSOP (400 mil)	TĠ	
Plastic 32-pin SOJ (400 mil)	DL	
Plastic 32-pin TSOP (400 mil)	TL	
NOTE: Available in die form Please co	moult factory for die data cheete	

NOTE: Available in die form. Please consult factory for die data sheets

• Part Number Example: MT4C2M8B1DJ-7 S

PART DESCRIPTION

MT4C2M8B1 S	5.0V, non-masked write
MT4C2M8B2 S	5.0V, masked write
MT4LC2M8B1 S	3.0V/3.3V, non-masked write
MT4LC2M8B2 S	3.0V/3.3V, masked write

GENERAL DESCRIPTION

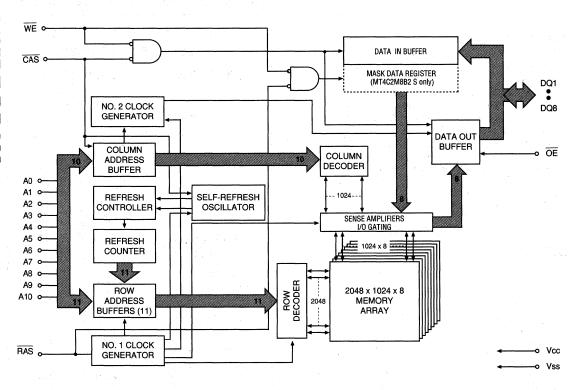
The MT4C2M8B1/2 S and MT4LC2M8B1/2 S are randomly accessed solid-state memories containing

	28-Pin SOJ (Q-4)		28-Pin TSOP (R-3)	
Vcc 1	28 J Vss	Vcc III 1	28 🖽 Vss	
DQ1 [2 DQ2 [3	27 DQ8	DQ1 == 2 DQ2 == 3	27 DQ8 26 DQ7	
DQ3 [] 4	25 DQ6	DQ3 == 4	25 III DQ6	
DQ4 🛘 5	24 DQ5	DQ4 III 5	24 DQ5	
WE [6	23 🗆 CAS	WE CC 6	23 🎞 CAS	
RAS [7	22 DE	RAS CC 7	22 🎞 ŌĒ	
*NC 🗆 8	21 A9	*NC === 8	21 🎞 A9	
A10 9	20 A8	A10 III 9	20 🞞 A8	
A0 🛘 10	19 🛘 A7 18 🗓 A6	A0 🖽 10	19 🖽 A7	
A2 [12	17 D A5	A1 III 11 A2 III 12	18 🞞 A6 17 🖾 A5	
A3 🛘 13	16 A4	A2 LL 12 A3 LL 13	16 TD A4	
Vcc [14	15 🛘 Vss	Vcc III 14	15 11 Van	
	n SOJ -5)	32-Pin TSOP (R-4)		
, α	0)	i ja seri	• • • • • • • • • • • • • • • • • • • •	
Vcc [1	32 J Vss	Vcc Ⅲ 1	32 TO Vss	
DQ1 🛭 2	31 DQ8	DQ1 III 2	31 DQ8	
DQ2 [] 3	30 DQ7	DQ2 == 3 DQ3 == 4	30 DQ7	
DQ3 [] 4 DQ4 [] 5	29 DQ6 28 DQ5	DQ3 11 4 DQ4 11 5	28 III DQ5	
NC [6	27 CAS	NC III 6	27 🞞 CAS	
WE 7	26 D OE	WE III 7	26 🞞 ŌE	
RAS [8	25 NC	RAS III 8	25 🞞 NC	
NC E 9	24 🗆 NC	NC III 9	24 🞞 NC	
*NC 🗆 10	23 🛘 A9	*NC 🖂 10	23 🞞 A9	
A10 🗆 11	22 A8	A10 🞞 11	22 🎞 A8	
A0 🛘 12	21 A7	A0 🕮 12	21 🎞 A7	
	20 🗎 A6	A1 == 13	20 🞞 A6	
A1 🛘 13				
A1 U 13 A2 U 14 A3 U 15	19 D A5 18 D A4	A2 == 14 A3 == 15	19 🞞 A5 18 🎞 A4	

16,777,216 bits organized in a x8 configuration. The MT4C2M8B1/2 S and the MT4LC2M8B1/2 S are the same DRAM versions except that the MT4LC2M8B1/2 S are low voltage versions of the MT4C2M8B1/2 S. The MT4LC2M8B1/2 S are designed to operate in either a 3.0V $\pm 10\%$ or a 3.3V $\pm 10\%$ memory system. All further references made for the MT4C2M8B1/2 S also apply to the MT4LC2M8B1/2 S, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{\rm RAS}$ latching 11 bits (A0-A10) and then $\overline{\rm CAS}$ latching 10 bits (A0-A10).

The MT4C2M8B2 S has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM 2,048 ROWS





PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
	8, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,	RAS	Input	Row Address Strobe: RAS is used to clock-in the 11 row- address bits and strobe the WE and DQs in the MASKED WRITE mode (MT4C2M8B2 S only).
23	27	CAS	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
6	7	WE	Input	Write Enable: WE is used to select a READ (WE = HIGH) or WRITE (WE = LOW) cycle. WE also serves as a Mask Enable (WE = LOW) at the falling edge of RAS in a MASKED-WRITE cycle (MT4C2M8B2 S).
22 (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A) (A)	26	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WE must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
10-13, 16-21, 9	12-15, 18-23, 11	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or Output masked data input (for MASKED WRITE cycle only).
44 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6, 9, 24, 25, 10	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	V cc	Supply	Power Supply: +5V ±10% (C), 3.0/3.3V ±10% (LC)
15, 28	17, 32	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

• Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First \overline{RAS} is used to latch 11 bits (A0-A10) then \overline{CAS} latches 10 bits (A0-A9).

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW.

READ or WRITE cycles are selected by \overline{WE} . A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by \overline{OE} and \overline{WE} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 256ms, regardless of sequence. The CAS-BEFORE-RAS refresh

cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 512ms.

MASKED WRITE ACCESS CYCLE (MT4C2M8B2 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when \overline{WE} is LOW at \overline{RAS} time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In nonpersistent MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8B2 S MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).



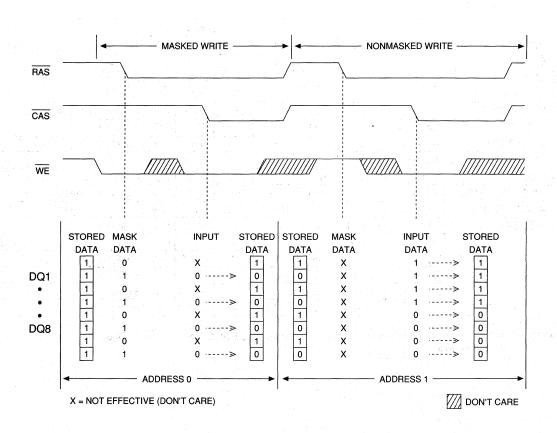


Figure 1
MT4C2M8B2 S MASKED WRITE EXAMPLE

TRUTH TABLE

						ADDRE	SSES		
FUNCTION		RAS	CAS	WE	OE .	tR.	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	X	Х	High-Z	
READ	READ		L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
MODE READ	2nd Cycle	L	H→L	Η	L	n/a	COL	Data Out	
FAST-PAGE-	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	1
MODE WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRES	H į	L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	Χ	Х	Х	High-Z	
BATTERY BACKUP	REFRESH	H→L	٦	Н	Х	Х	Х	High-Z	
SELF REFRESH		H→L	L	Н	Х	Х	Х	High-Z	

NOTE: 1. Data in will be dependent on the mask provided (MT4C2M8B2 S only). Refer to Figure 1.

2. EARLY WRITE only.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:control_volume} \begin{tabular}{lll} Voltage on Vcc supply relative to Vss (5V) & ... & -1V to +7V \\ Voltage on Vcc supply relative to Vss (3V) & ... & -1V to +4.6V \\ Operating Temperature, T_A (Ambient) & ... & 0°C to +70°C \\ Storage Temperature (Plastic) & ... & -55°C to +150°C \\ Power Dissipation & ... & 1W \\ Short Circuit Output Current & ... & ... & ... \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	li v	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (IouT = 2.1mA)	Vol	15.1	0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C \leq T_A \leq 70°C; Vcc = 3.0/3.3V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	lı	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	Vон	2.4		٧	
Output Low Voltage (IouT = 2mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)			MAX		1		
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: TTL (RAS = CAS = VIH)	lcc1	2	2	2	mA		
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μΑ	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	140	130	120	mA	3, 4, 32	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	Icc4	100	90	80	mA	3, 4, 32	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ¹RC = ¹RC (MIN))	lcc5	140	130	120	mA	3, 32	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: tRC = tRC (MIN))	lcc6	140	130	120	mA	3, 5	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ^t RAS (MIN) to 300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), ^t RC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	300	300	300	μА	3, 30	
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with RAS ≥ ¹RASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	lccs	300	300	300	μА	5	



DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0° C $\leq T_{A} \leq 70^{\circ}$ C: $V_{CC} = 3.0/3.3V \pm 10\%$)

Notes. 1, 3, 4, 6, 7, 31) (0 $C \le T_A \le 70 C$, $VCC = 3.0/3.3 V \pm 10\%)$			MAX		1972 1978 19	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL (RAS = CAS = VIH)	lcc1	1	1	10.	mA.	
STANDBY CURRENT: CMOS (RAS = CAS = Vcc -0.2V)	lcc2	80	80	80	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current. (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	90	90	80	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	Icc4	75	65	55	mA	3, 4, 32
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	100	90	80	mA	3, 32
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icce	100	90	80	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), tRC = 125μs (1,024 rows at 125μs = 128ms)	lcc7	100	100	100	μА	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with RAS ≥ ¹RASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9 and Din = Vcc - 0.2V or 0.2V (Din may be left open)	Icc8	100	100	100	μА	5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	Cıı	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C12	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C)

AC CHARACTERISTICS		-6		-7		8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	. 4
READ-WRITE cycle time	^t RWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	35		40		40	******	ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	85		95		100	1 1 1	ns	. 4 1
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Output Enable	^t OE		15		15		15	ns	
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	†CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100.000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100.000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15	1	20	1	20	100,000	ns	
RAS precharge time	tRP	40	 	50		60	1	ns	<u> </u>
CAS pulse width	tCAS	15	100,000	20	100.000	20	100,000	ns	
CAS hold time	tCSH	60	1	70	1	80	1	ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		- 5	<u> </u>	ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	†RAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0	1	0	<u> </u>	ns	
Column address hold time	^t CAH	10		15		15	-	ns	
Column address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20, 29



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) $(0^{\circ}C \le T_{A} \le +70^{\circ}C)$

AC CHARACTERISTICS	15.5		-6		-7	1	-8	5 5 25 5 5	fish y
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
WE command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	10		15		15		ns	- 26
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	tRWL	15		20	1000	20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	^t DH	10		15		15	1000	ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Column address to WE delay time	tAWD	55		60		65	T. H. Ma	ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^t REF		256		256		256	ms	
RAS to CAS precharge time	^t RPC	0		0	100 Tige.	0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	[†] OD		15		15	1977	15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		15		15		ns	28
RAS pulse width during SELF REFRESH cycle	†RASS	100		100		100		μs	34
RAS precharge time during SELF REFRESH cycle	^t RPS	150		150		150		ns	34
CAS hold time during SELF REFRESH cycle	[†] CHS	-70		-70		-70		ns	34

TECHNOLOGY. IN

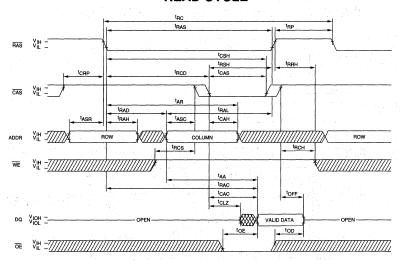
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS -ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the REF refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VII. (or between VII. and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.

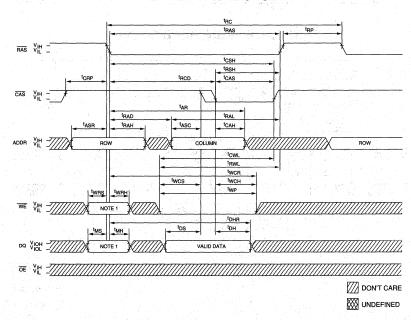
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CASgoes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as WE going LOW.
- 27. MT4C2M8B2 S only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a don't care; and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
- 31. The 5V version is restricted to operate between 4.5 V and 5.5V only.
- 32. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 33. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.
- 34. When exiting the SELF REFRESH mode, a complete set of row refreshes must be executed in order to ensure the DRAM will be fully refreshed.



READ CYCLE

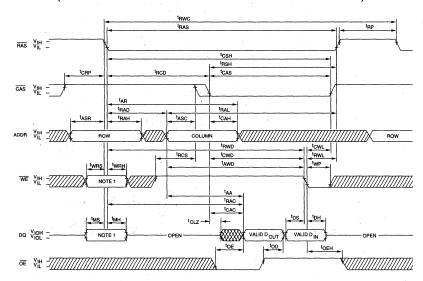


EARLY-WRITE CYCLE

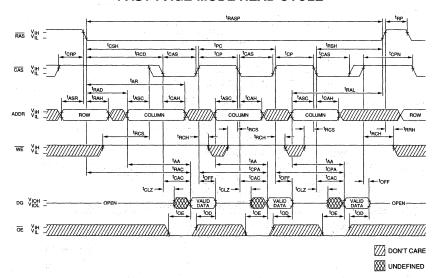


NOTE: 1. Applies to MT4C2M8B2 S only; WE and DQ inputs on MT4C2M8B1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



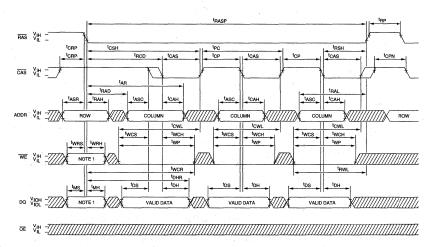
FAST-PAGE-MODE READ CYCLE



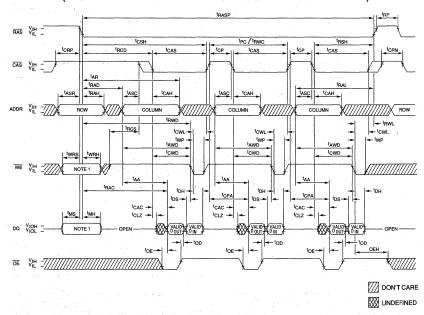
NOTE:

1. Applies to MT4C2M8B2 S only; WE and DQ inputs on MT4C2M8B1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



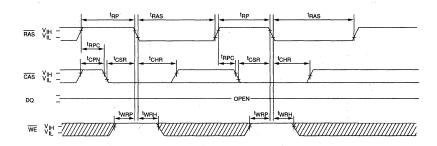
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C2M8B2 S only; WE and DQ inputs on MT4C2M8B1 S are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

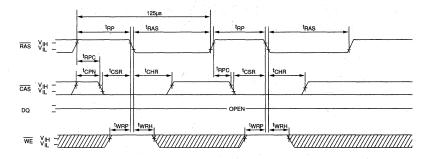
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A10; \overline{OE} = DON'T CARE)$



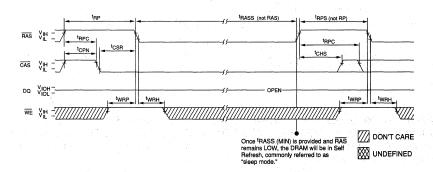
BATTERY BACKUP REFRESH CYCLE

 $(A0-A10; \overline{OE} = DON'T CARE)$



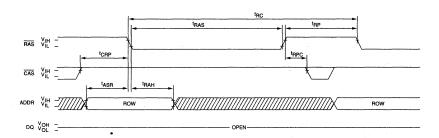
SELF REFRESH CYCLE ("SLEEP MODE")

 $(A0-A10; \overline{OE} = DON'T CARE)$



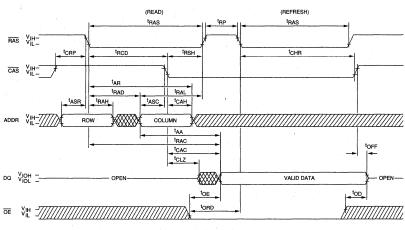


RAS-ONLY REFRESH CYCLE (OE and WE = DON'T CARE)



HIDDEN REFRESH CYCLE 24

 $\overline{\text{WE}} = \text{HIGH}; \overline{\text{OE}} = \text{LOW}$



DON'T CARE

₩ UNDEFINED



DRAM

64K x 16 DRAM

FAST PAGE MODE

FEATURES

ODTIONIC

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL compatible
- 256-cycle refresh in 4ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle (MT4C1664 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 only)

MADIZINIC

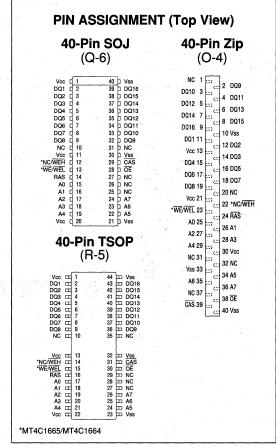
OPTIONS	MAKKING
Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
Write Enable	
Byte or Word	MT4C1664
Word only	MT4C1665
Mask Enable	
Not Available	MT4C1664
Always Available	MT4C1665
 Packages 	
Plastic SOJ (400mil)	DI
Plastic TSOP (400mil)	TG
Plastic ZIP (475mil)	Z
I MUSIC ZII (T/OIIII)	

NOTE: Available in die form Please consult factory for die data sheets.

GENERAL DESCRIPTION

The MT4C1664/5 are randomly accessed solid-state nemories containing 1,048,576 bits organized in a x16 onfiguration. The MT4C1664 has both BYTE and WORD VRITE access cycles while the MT4C1665 has only WORD VRITE access cycles.

The MT4C1664 functions in a similar manner to the MT4C1665 except that replacing \overline{WE} with \overline{WEL} and \overline{WEH} llows for BYTE WRITE access cycles. \overline{WEL} and \overline{WEH} unction in an identical manner to \overline{WE} : either \overline{WEL} or \overline{WEH}

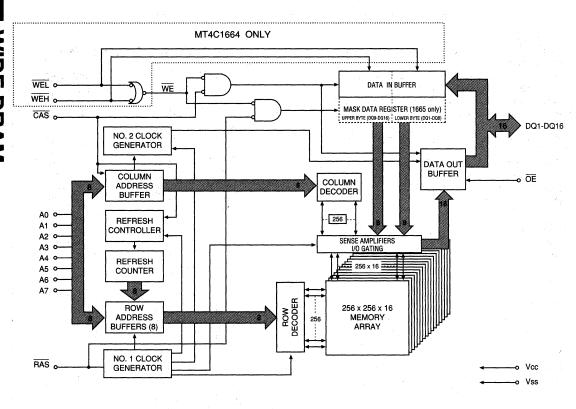


will generate an internal \overline{WE} through an AND gate (Inverted NOR gate).

The MT4C1664 "WE" function and timing are determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1665 has NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN Numbers	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	RAS	Input	ROW Address Strobe: RAS is used to clock-in the 8 row address bits and strobe the WEL, WEH and DQ inputs for the MASKED WRITE function.
29	39	31	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL and WEH must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	WE/WEL*	Input	WRITE Enable Lower Byte: WEL on MT4C1664 is WE control for the DQ1 through DQ8 inputs. WE on MT4C1665 controls DQ1 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/WEH*	Input	Write Enable Upper Byte: WEH on MT4C1664 is WE control for the DQ9 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL or WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25-27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1665/MT4C1664

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. RAS is used to latch the first 8 bits and CAS the latter 8 bits.

READ or WRITE cycles on the MT4C1665 are selected with the WE input while either WEL or WEH perform the "WE" on the MT4C1664. The MT4C1664 "WE" function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE, WEL and WEH (MT4C1664) or WE (MT4C1665).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 256 combinations of RAS addresses (A0-A7) are executed at least every 4ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also

invoke the refresh counter and controller for row address control.

BYTE WRITE DESCRIPTION (MT4C1664 ONLY)

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling WEH will select an upper BYTE WRITE (DQ9-DQ16). Enabling both WEL and WEH selects a WORD WRITE cycle.

The MT4C1664 can be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1664 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1665 is only word selectable when \overline{WE} is LOW at \overline{RAS} time (the MT4C1664 does not have MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665* MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).



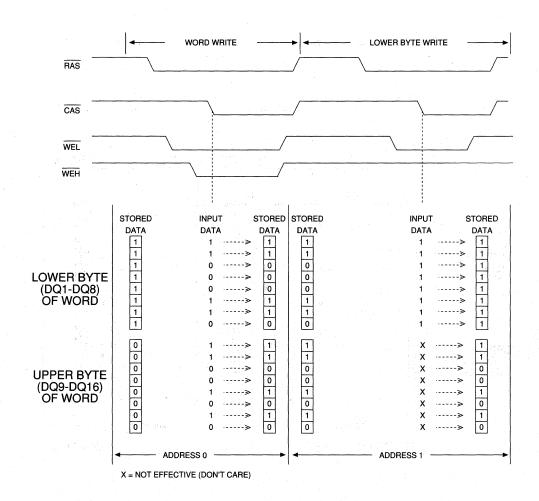


Figure 1
MT4C1664 WORD AND BYTE WRITE EXAMPLE

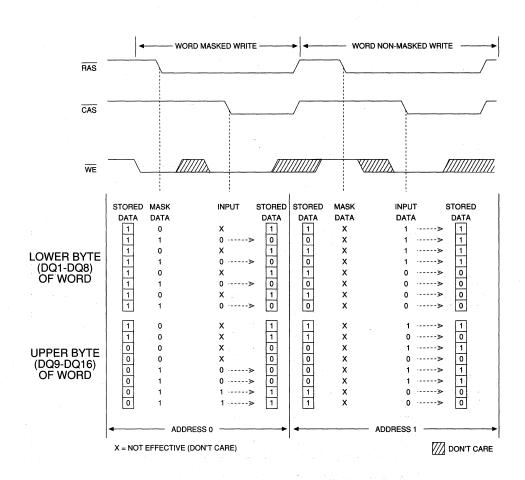


Figure 2
MT4C1665 MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C1664

							ADDRE	SSES		
FUNCTION		RAS	CAS	WEL	WEH	ŌĒ	t _R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	Χ	Х	Х	High-Z	
READ	31.7	L	L	Н	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	E L L Z T L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-R REFRESH	AS	H→L	L	Х	Х	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be byte WRITE cycles (either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ active).
- 2. EARLY-WRITE only.



TRUTH TABLE: MT4C1665

						ADDRESSES			
FUNCTION		RAS	CAS	WE	OE	t _R	tC	DQs	NOTES
Standby	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Н	H→X	X	Х	Х	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	4 1
WRITE: WORD (EARLY-WRITE)		L' ·	L ,	L	Х	ROW	COL	Data In	11 / 135
READ-WRITE		Ľ	L	H→L	L→H	ROW	ĊOL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1 .
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	Х	X-	Х	High-Z	

NOTE:

- 1. Data In will be dependent on the mask provided. Refer to Figure 2.
- 2. EARLY-WRITE only.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1.0V to +7.0V \\ Operating Temperature, T_A (Ambient) & 0°C to +70°C \\ Storage Temperature (Plastic) & -55°C to +150°C \\ Power Dissipation & 1W \\ Short Circuit Output Current & 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	Vıн	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	8.0	V	111
INPUT LEAKAGE CURRENT Any Input 0V ≤ ViN ≤ Vcc (All other pins not under test = 0V)	lı .	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -2.5mA)	Vон	2.4		V	
Output Low Voltage (lout = 2.1mA)	Vol		0.4	ν	

		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	2	2	2	mA		
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc -0.2V)$	lcc2	1	1	4 1 3	mA	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	120	110	100	mA	3, 4, 31	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	Icc4	80	70	60	mA	3, 4, 31	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS=ViH: tRC = tRC (MIN))	lcc5	120	110	100	mA	3, 31	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	Icc6	120	110	100	mA	3, 5	



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/ WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-	10		1 0
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	130		145		170		ns	
READ-WRITE cycle time	tRWC.	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE	tPC	45		50		60		ns	
cycle time							1		
FAST-PAGE-MODE READ-WRITE	^t PRWC	95		100		120		ns	
cycle time									
Access time from RAS	tRAC.		70	- "	80		100	ns	14
Access time from CAS	^t CAC		25	1	25		30	ns	15
Output Enable time	^t OE		25		25		30	ns	
Access time from column address	^t AA		40		45		50	ns	
Access time from CAS precharge	^t CPA		45		50		55	ns	1 1
RAS pulse width	tRAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		²⁰		25		ns	
RAS precharge time	tRP	45		45		60		ns	
CAS pulse width	^t CAS	25	100,000	25	100,000	30	100,000	ns	
CAS hold time	^t CSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		15		ns	16
CAS precharge time (FAST PAGE MODE)	[†] CP	10	1	10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	25	60	ns	17
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0	1	ns	
Row address hold time	tRAH .	10		10		10	1	ns	
RAS to column	^t RAD	15	35	15	40	15	50	ns	18
address delay time									
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	15	1	15		15	1.1.4	ns	
Column address hold time	^t AR	55	1	60		70		ns.	
(referenced to RAS)								6.	
Column address to	†RAL	35		40		50		ns	
RAS lead time			1			4.00			
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time	tRCH	0		0	5.15.1	0		ns	19, 26
(referenced to CAS)				The second of th	1 1 1 1 1 1 1 1 1				1.
Read command hold time	^t RRH	0		0	1 1 1	0		ns	19
(referenced to RAS)		•					1 1	Pikanen,	Bar Mil
CAS to output in Low-Z	tCLZ	0		0		0	120	ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	<u> </u>	-7		-8		-10		1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 30
Output disable time	tOD		15		15		20	ns	30
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		15		ns	26
Write command hold time (referenced to RAS)	tWCR	50		55		65		ns	26
Write command pulse width	tWP	15		15		15		ns	26
Write command to RAS lead time	tRWL	20		20	2.5	20		ns	26
Write command to CAS lead time	tCWL	20	1.	20		20		ns	26
Data-in setup time	tDS	0		0	1 1 1 1	0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	50		55		65		ns	ost in
RAS to WE delay time	^t RWD	90		100		125		ns	21
Column address to WE delay time	^t AWD	65		70		80		ns	21
CAS to WE delay time	tCWD	50		55		70		ns	21
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	tREF	0.00	4		4		4	ms	28
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
MASKED WRITE command to RAS setup time	†WRS	0		0		0		ns	26, 27
MASKED WRITE command to RAS hold time	^t WRH	15		15		15		ns	26, 27
Mask data to RAS setup time	tMS	0		0	1.17	0		ns	26
Mask data to RAS hold time	tMH	15		15		15		ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	10		10		20		ns	29
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	

WIDE DRAM

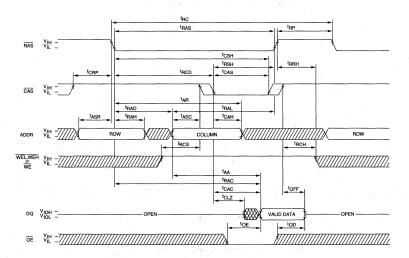
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIII and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gates and 50pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

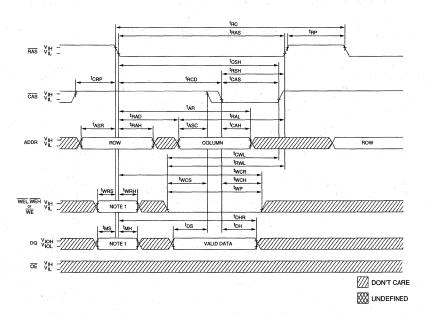
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as either WEL or WEH or both going LOW on the MT4C1664. Write command is defined as WE going LOW on the MT4C1665.
- Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
- The refresh period may be extended to 8ms without experiencing problems.
- 29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both 'OD and 'OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after 'OEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 31. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.



READ CYCLE



EARLY-WRITE CYCLE

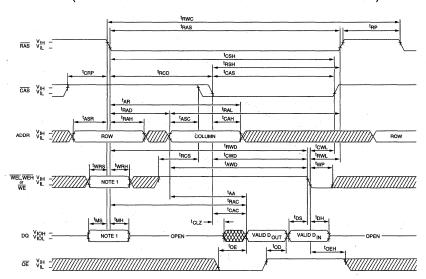


NOTE:

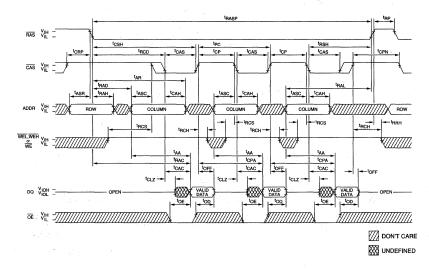
1. Applies to MT4C1665 only; WEL, WEH and DQ inputs on MT4C1664 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



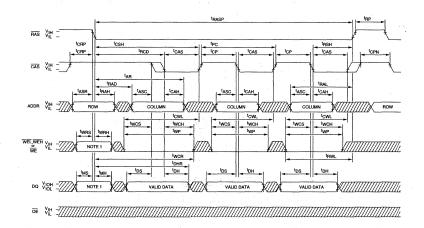
FAST-PAGE-MODE READ CYCLE



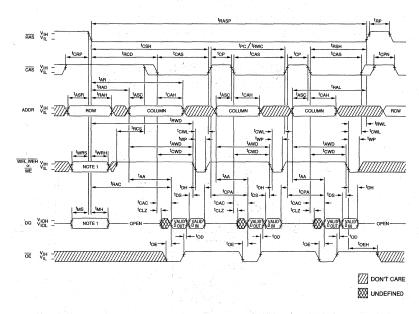
NOTE: 1. Applies to MT4C1665 only; WEL, WEH and DQ inputs on MT4C1664 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



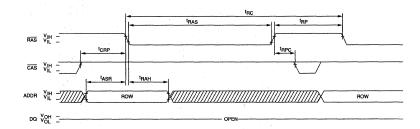
NOTE:

1. Applies to MT4C1665 only; WEL, WEH and DQ inputs on MT4C1664 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



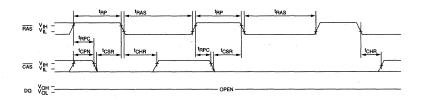
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, \overline{OE} ; \overline{WEL} , \overline{WEH} or \overline{WE} = DON'T CARE)



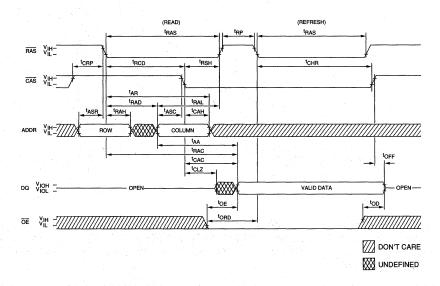
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; \overline{WEL} , \overline{WEH} or \overline{WE} , and \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE 24

 $(\overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

64K x 16 DRAM

LOW POWER EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle (MT4C1664 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1665 L only)
- Reduced CMOS STANDBY CURRENT
- Low power, 1mW standby; 225mW active, typical
- Extended refresh: 256 cycles over 32ms (125µs cycles)

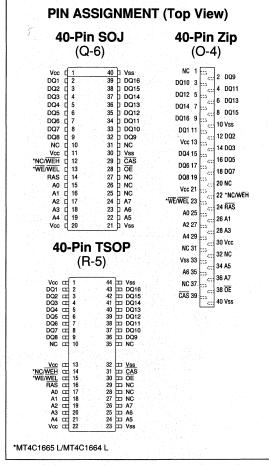
OPTIONS MARKING Timing 70ns access - 7 80ns access - 8 100ns access -10 • Write Enable Byte or Word MT4C1664 L MT4C1665 L Word only · Mask Enable Not available MT4C1664 L Always available MT4C1665 L Packages Plastic SOJ (400mil) DI Plastic TSOP (400mil) TG Plastic ZIP (475mil) Z NOTE: Available in die form Please consult factory for die data sheets.

• Part Number Example: MT4C1664DI-7 L

GENERAL DESCRIPTION

The MT4C1664/5 L are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1664 L has both BYTE and WORD WRITE access cycles while the MT4C1665 L has only WORD WRITE access cycles.

The MT4C1664 L functions in a similar manner to the MT4C1665 L except that replacing WE with WEL and WEH allows for BYTE WRITE access cycles. WEL and WEH function in an identical manner to WE: either WEL



or \overline{WEH} will generate an internal \overline{WE} through an AND gate (inverted NOR gate).

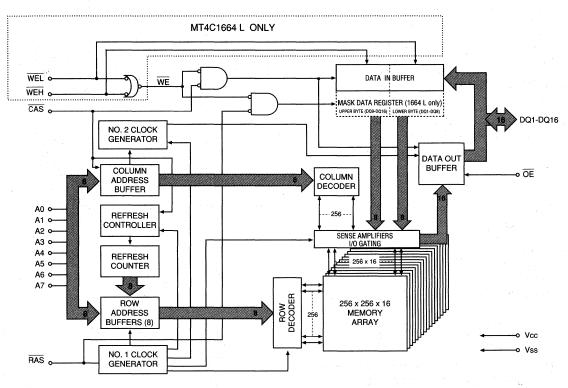
The MT4C1664 L "WE" function and timing are determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1665 L has NONPERSISTENT MASKED WRITE capability.

The extended refresh of the MT4C1664/5 L provides a factor-of-eight reduction of refresh intervals required, as compared to a standard 64K x 16 DRAM (MT4C1664/5).

The MT4C1664/5 L offers lower operating power as well as reduced refresh and standby currents. The MT4C1664/5 L are the same devices as the MT4C1664/5, but with low power capabilites.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	RAS	Input	ROW Address Strobe: RAS is used to clock-in the 8 row address bits and strobe the WEL, WEH and DQ inputs for the MASKED WRITE function.
29	39	31	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL and WEH must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	WE/WEL*	Input	WRITE Enable Lower Byte: WEL on MT4C1664 L is WE control for the DQ1 through DQ8 inputs. WE on MT4C1665 L controls DQ1 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/WEH*	Input	Write Enable Upper Byte: WEH on MT4C1664 L is WE control for the DQ9 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1665 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL or WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	- · · · · · · · · · · · · · · · · · · ·	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%

NOTE: *MT4C1665 L/MT4C1664 L

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. RAS is used to latch the first 8 bits and CAS the latter 8 bits.

READ or WRITE cycles on the MT4C1665 L are selected with the \overline{WE} input while either \overline{WEL} or \overline{WEH} perform the " \overline{WE} " on the MT4C1664 L. The MT4C1664 L " \overline{WE} " function is determined by the first BYTE WRITE (\overline{WEL} or \overline{WEH}) to transition LOW and the last one to transition back HIGH.

A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE, WEL and WEH (MT4C1664 L) or WE (MT4C1665 L).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 256 combinations of RAS addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

BYTE WRITE DESCRIPTION (MT4C1664 L ONLY)

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling WEH will select an upper BYTE WRITE (DQ9-DQ16). Enabling both WEL and WEH selects a WORD WRITE cycle.

The MT4C1664 L may be viewed as two 64K x 8 DRAMs which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1664 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1665 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1665 L is only word selectable when \overline{WE} is LOW at \overline{RAS} time (the MT4C1664 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1665 L MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).



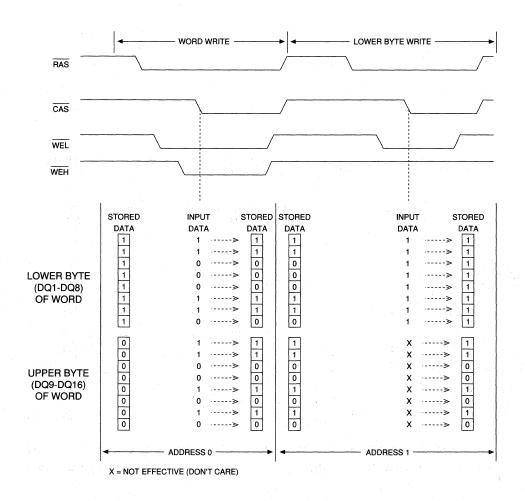


Figure 1
MT4C1664 L WORD AND BYTE WRITE EXAMPLE

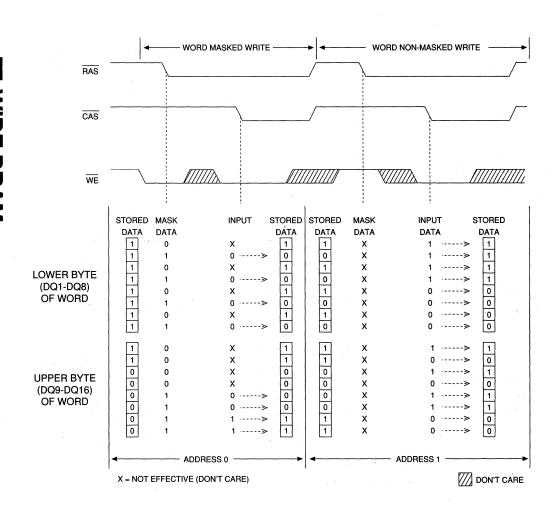


Figure 2
MT4C1665 L MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C1664 L

							ADDRE	SSES		
FUNCTION		RAS	CAS	WEL	WEH	ŌE	t _R	tC	DQs	NOTES
Standby		Н	H→X	X	Х	Х	Х	Х	High-Z	111111111111111111111111111111111111111
READ	1 1	L	L	Н	Н	L	ROW	COL	Data Out	145.44
WRITE: WORD (EARLY-WRITE)		L	L	L	L	Х	ROW	COL	Data In	1.4
WRITE: LOWER BYTE (EARLY)		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	jewa sa
READ	2nd Cycle	i L	H→L	Н	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	a Lara	H→L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	X	Х	ROW	n/a	High-Z	
CAS-BEFORE-R. REFRESH	AS	H→L	L	Х	X	Х	Х	Х	High-Z	
BATTERY BACK REFRESH	UP	H→L	L	Х	Х	Х	Х	Х	High-Z	

NOTE:

^{1.} These cycles may also be BYTE WRITE cycles (either WEL or WEH active).

^{2.} EARLY-WRITE only.

TRUTH TABLE: MT4C1665 L

						ADDRE	SSES		
FUNCTION		RAS	CAS	WE	ŌĒ	^t R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	1
WRITE: WORD (EARLY-WRITE)		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	1 W 1
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Η	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Х	Х	Х	Х	High-Z	
BATTERY BACKUP	REFRESH	H→L	L	X	Х	Х	Х	High-Z	

NOTE:

- 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
- 2. EARLY-WRITE only.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1V to +7V \\ Operating Temperature, T_A (Ambient) & 0°C to +70°C \\ Storage Temperature (Plastic) & ... -55°C to +150°C \\ Power Dissipation & ... 1W \\ Short Circuit Output Current & ... 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	lı .	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (lout = 2.1mA)	Vol		0.4	٧	

JANE BURE BERKER BERKER			MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	lcc2	300	300	300	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	120	110	100	mA	3, 4, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS, Address Cycling: ¹PC = ¹PC (MIN); ¹CP, ¹ASC = 10ns)	lcc4	80	70	60	mA	3, 4, 32
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	120	110	100	mA	3, 32
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc6	120	110	100	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current with $\overline{CAS} = 0.2V$ or CBR; $\overline{RAS} = \text{minimum}^{t} RAS$ to 1µs; A0-A7, \overline{WE} , \overline{OE} and DQs = Vcc -0.2V or 0.2V (DQs may float); ${}^{t} RC = 125 \mu s$	lcc7	400	400	400	μА	3, 31



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/ WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Cio		7	рF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		145		170		ns	
READ-WRITE cycle time	tRWC	175		185		220		ns	
FAST-PAGE-MODE READ or WRITE	^t PC	45		50		60		ns	
cycle time									
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	95		100		120		ns	
Access time from RAS	tRAC		70		80		100	ns	14
Access time from CAS	†CAC		25		25		30	ns	15
Output Enable time	†OE		25		25		30	ns	
Access time from column address	†AA		40		45		50	ns	
Access time from CAS precharge	†CPA		45		50		55	ns	
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20	100,000	20	100,000	25	100,000	ns	
RAS precharge time	tRP	45	 	45	-	60	 	ns	
CAS pulse width	†CAS	25	100,000	25	100,000	30	100,000	ns	
CAS hold time	†CSH	70	100,000	80	100,000	100	100,000		
CAS precharge time	tCPN	10	-	10	+	15	+	ns	16
CAS precharge time (FAST PAGE MODE)	¹ CP	10	 	10	+	10		ns	10
RAS to CAS delay time	tRCD	20	45	20	50	25	60	ns	17
CAS to RAS precharge time	tCRP	5	45	- 5	50	5	60	ns	. 17
Row address setup time	tASR	0	-	0		0		ns	-
Row address hold time	tRAH					10	1 1 1 1 1 1	ns	
RAS to column	tRAD	10 15		10	40	15		ns	10
address delay time	HAD	15	35	15	40	15	50	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time (referenced to RAS)	†AR	55		60		70		ns	
Column address to RAS lead time	^t RAL	35		40	14.19	50		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	0		0		0	1 100 1	ns	7/4° s. T.



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		. v	7	_	8	-1	0		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	. 0	20	0	20	0	20	ns	20, 30
Output disable time	tOD		15		15		20	ns	30
Write command setup time	tWCS	0		0	1- 1-	0	7.1	ns	21, 26
Write command hold time	tWCH	15		15		15		ns	26
Write command hold time (referenced to RAS)	^t WCR	50		55		65		ns	26
Write command pulse width	tWP	15		15		15		ns	26
Write command to RAS lead time	tRWL	20		20	100	20		ns	26
Write command to CAS lead time	tCWL	20		20	1.0	20		ns	26
Data-in setup time	t _{DS}	0		0		0		ns	22
Data-in hold time	^t DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	50		55		65		ns	
RAS to WE delay time	^t RWD	90		100	7	125		ns	21
Column address to WE delay time	^t AWD	65		70	•	80		ns	21
CAS to WE delay time	tCWD	50		55	1 1 1	70		ns	21
Transition time (rise or fall)	·Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	tREF		32		32		32	ms	28
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	-15		15		15		ns	5
MASKED WRITE command to RAS setup time	^t WRS	0		0		0		ns	26, 27
MASKED WRITE command to RAS hold time	tWRH	15		15		15	971.7 871.7	ns	26, 27
Mask data to RAS setup time	tMS	0		0		0		ns	26
Mask data to RAS hold time	^t MH	15		15	40%	15	1 1 1 1 1	ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	10		10		20		ns	29
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	

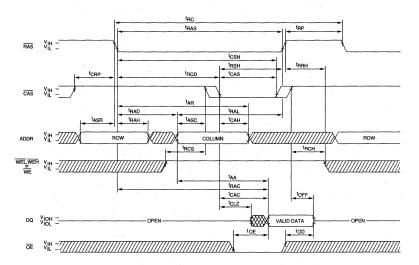
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VII. and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is high impedance.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gates and 50pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.

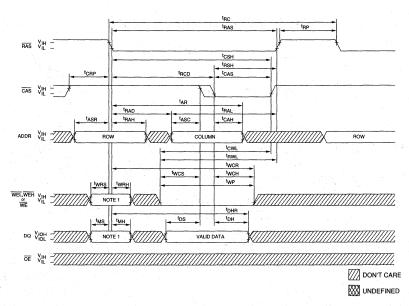
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If 'RWD ≥ 'RWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle
- These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. WRITE command is defined as either WEL or WEH or both going LOW on the MT4C1664 L. WRITE command is defined as WE going LOW on the MT4C1665 L.
- Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
- 28. The refresh period may be extended to 8ms without causing problems.
- 29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 31. BBU current does not significantly change when ^tRAS is reduced from its maximum specification during BBU cycle.
- 32. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH



READ CYCLE



EARLY-WRITE CYCLE

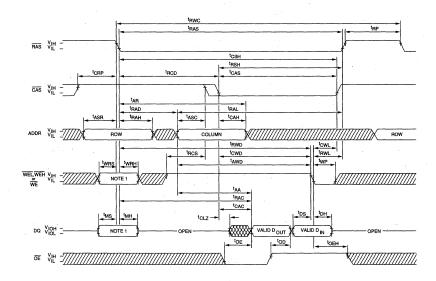


NOTE:

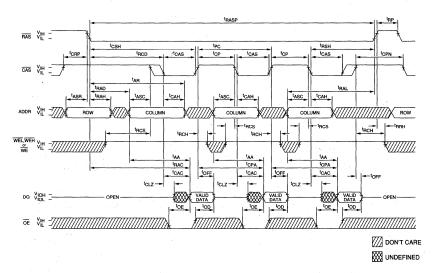
1. Applies to MT4C1665 L only; WEL, WEH and DQ inputs on MT4C1664 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE

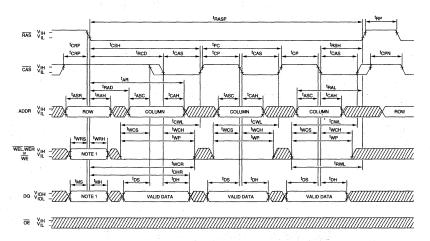


NOTE:

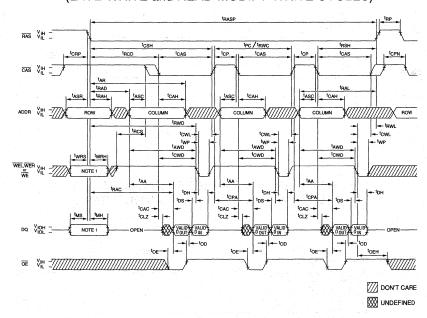
1. Applies to MT4C1665 L only; WEL, WEH and DQ inputs on MT4C1664 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

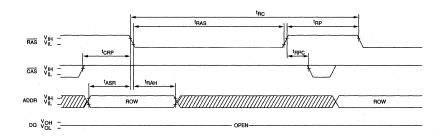


NOTE: 1. Applies to MT4C1665 L only; WEL, WEH and DQ inputs on MT4C1664 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



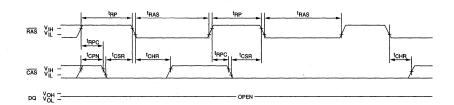
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



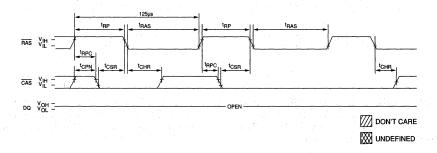
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7 \overline{WEL} , \overline{WEH} or \overline{WE} , and $\overline{OE} = DON'T CARE$)



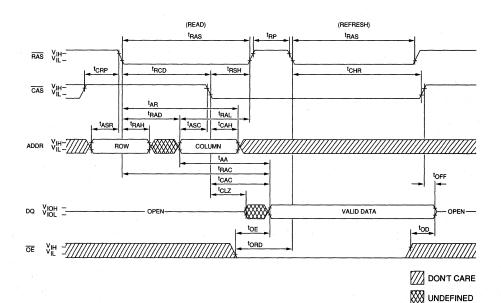
BATTERY BACKUP REFRESH CYCLE

(A0-A7 $\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$, and $\overline{\text{OE}} = \text{DON'T CARE}$)





HIDDEN REFRESH CYCLE ²⁴ $\overline{\text{WEL}}$, $\overline{\text{WEH}}$ or $\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)





DRAM

64K x 16 DRAM

STATIC COLUMN MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL compatible
- 256 cycle refresh in 4ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 only)

OPTIONS	MARKING
Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
Write Enable	
Byte or Word	MT4C1670
Word only	MT4C1671
Mask Enable	
Not Available	MT4C1670
Always Available	MT4C1671
Packages	
Plastic SOJ (400mil)	DJ
Plastic TSOP (400mil)	TĠ
Plastic ZIP (475mil)	Z

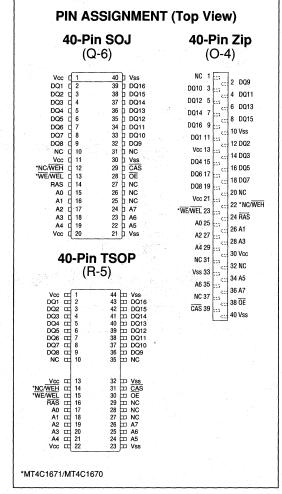
NOTE: Available in die form Please consult factory for die data sheets.

GENERAL DESCRIPTION

The MT4C1670/1 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 has both BYTE and WORD WRITE access cycles while the MT4C1671 has only WORD WRITE access cycles.

The MT4C1670 functions in a similar manner to the MT4C1671 except that replacing WE with WEL and WEH allows for BYTE WRITE access cycles. WEL and WEH function in an identical manner to WE: either WEL or WEH will generate an internal WE through an AND gate Inverted NOR gate).

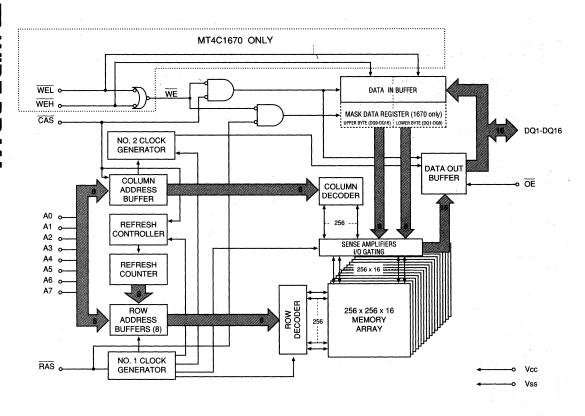
The MT4C1670 "WE" function and timing are determined by the first BYTE WRITE (WEL or WEH) to transition LOW



and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DO9-DQ16).

The MT4C1671 has NONPERSISTENT MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN Numbers	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	RAS	Input	ROW Address Strobe: RAS is used to clock-in the 8 row address bits and strobe the WEL, WEH and DQ inputs for the MASKED WRITE function.
29	39	31	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38 2004 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	30	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL and WEH must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	WE/WEL*	Input	Write Enable Lower Byte: WEL on MT4C1670 is WE control for the DQ1 through DQ8 inputs. WE on MT4C1671 controls DQ1 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/WEH*	Input	Write Enable Upper Byte: WEH on MT4C1670 is WE control for the DQ9 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL or WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671/MT4C1670

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 addressbits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. RAS is used to latch the first 8 bits and CAS the latter 8 bits.

READ or WRITE cycles on the MT4C1671 are selected with the \overline{WE} input while either \overline{WEL} or \overline{WEH} perform the " \overline{WE} " on the MT4C1670. The MT4C1670 " \overline{WE} " function is determined by the first BYTE WRITE (\overline{WEL} or \overline{WEH}) to transition LOW and the last one to transition back HIGH.

A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by \overline{OE} , \overline{WEL} and \overline{WEH} (MT4C1670) or \overline{WE} (MT4C1671).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have CAS or WE toggled strobing-in the different column addresses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} , or HID-DEN refresh) so that all 256 combinations of \overline{RAS} addresses (A0-A7) are executed at least every 4ms, regardless of

sequence. The $\overline{\text{CAS-BEFORE-RAS}}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE ACCESS CYCLE (MT4C1670 ONLY)

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling WEH will select an upper BYTE WRITE (DQ9-DQ16). Enabling both WEL and WEH selects a WORD WRITE cycle.

The MT4C1670 may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1671 is only word selectable when \overline{WE} is LOW at \overline{RAS} time (the MT4C1670 does not have a MASKED WRITE cycle function)

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

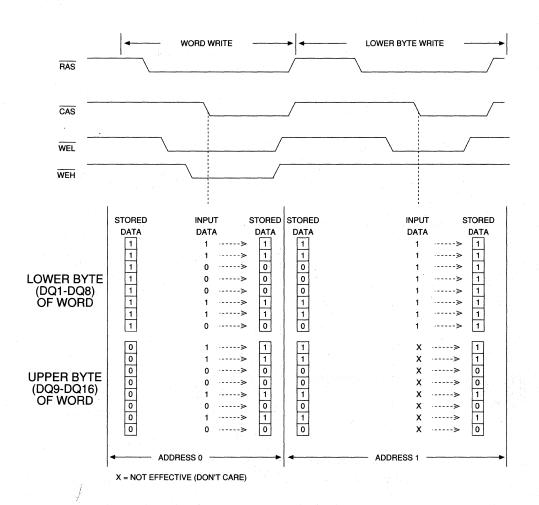


Figure 1 MT4C1670 WORD AND BYTE WRITE EXAMPLE

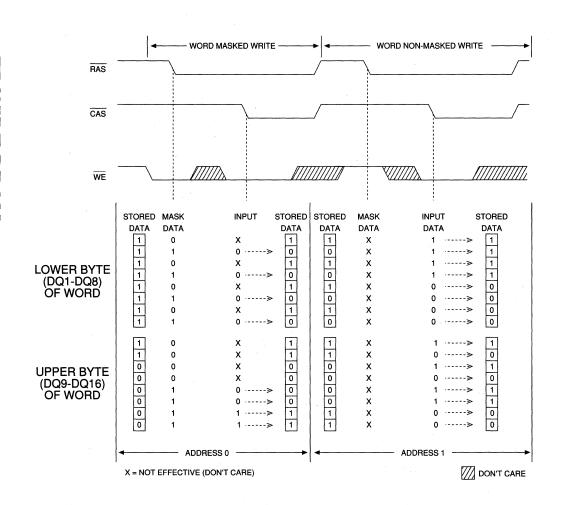


Figure 2
MT4C1671 MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C1670

							ADDRE	SSES		
FUNCTION		RAS	CAS	WEL	WEH	ŌĒ	^t R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	X	Х	Х	High-Z	
READ		L	L	Н	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	Х	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	Н	Н	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	100
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	X	Х	ROW	n/a	High-Z	
CAS-BEFORE-RA	45	H→L	L	Χ	Х	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ active).
- 2. EARLY-WRITE only.
- 3. Either CAS or WEL / WEH must latch in each additional column address and input data.



TRUTH TABLE: MT4C1671

						ADDRE	SSES		
FUNCTION		RAS	CAS	WE	0E	^t R	tC.	DQs	NOTES
Standby		Н	H→X	Х	Х	X	Х	High-Z	
READ		L	€ L	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	Н	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	/L	L	L	Х	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle /	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	Ly	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	Х	Х	X	High-Z	

NOTE:

- 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
- EARLY-WRITE only.
 Either CAS or WEL / WEH must latch in each additional column address and input data.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1.0V to +7.0V \\ Operating Temperature, T_A (Ambient) & -0^{\circ}C to +70^{\circ}C \\ Storage Temperature (Plastic) & -55^{\circ}C to +150^{\circ}C \\ Power Dissipation & 1W \\ Short Circuit Output Current & 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	Vıн	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	di di	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (lout = 2.1mA)	Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$	Icc2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL; CAS, Address Cycling: ^t SC = ^t SC (MIN))	lcc4	110	95	80	mA	3, 4, 31
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC (MIN))	lcc5	120	115	90	mA	3, 31
REFRESH CURRENT: CAS -BEFORE- RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	120	115	90	mA	3, 5



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	Cıı		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/ WE, OE	C ₁₂		7	pF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Input Capacitance: RAS, CAS,	Cız	2	7	pF						
Input/Output Capacitance: DQ	Cic)	7	pF						
ELECTRICAL CHARACTE Notes: 6, 7, 8, 9, 10, 11, 12, 13, 2						PERA	TING CO	ONDITIO	ONS	
AC CHARACTERISTICS			-7		-8	-8 -10				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NO	
Random READ or WRITE cycle time	^t RC	130		150		180	41	ns		
READ-WRITE cycle time	tRWC	175		185		220		ns		
STATIC-COLUMN READ or WRITE cycle time	tSC	45		50		55		ns		
STATIC-COLUMN READ-WRITE cycle time	^t SRWC	95		100		120		ns		
Access time from RAS	^t RAC		70		80		100	ns	. 1	
Access time from CAS	^t CAC		25		35		40	ns	1	
Output Enable time	^t OE		25		35		40	ns		
Access time from column address	^t AA		40		45		55	ns		
Access time from CAS precharge	^t CPA		45		50		55	ns		
RAS pulse width	^t RAS	70	100,000	80	100,000	100	100,000	ns		
RAS pulse width (STATIC COLUMN)	tRASC	70	100,000	80	100,000	100	100,000	ns		
RAS hold time	^t RSH	20		35		40		ns		
RAS precharge time	^t RP	50		60		70		ns		
CAS pulse width	^t CAS	25	100,000	35	100,000	40	100,000	ns		
CAS hold time	^t CSH	70		80		100		ns		
CAS precharge time	tCPN .	10		10		15		ns	1	
CAS precharge time (STATIC COLUMN)	^t CP	10		10		10		ns	1.75	
RAS to CAS delay time	^t RCD	20	45	20	45	25	60	ns	1	
CAS to RAS precharge time	^t CRP	5		10		10		ns		
Row address setup time	^t ASR	0		0		0		ns		
Row address hold time	^t RAH	10		12		15		ns		
RAS to column address delay time	^t RAD	15	35	17	40	20	55	ns	1	
Column address setup time	†ASC	0		0		0		ns		
Column address hold time	^t CAH	15		15		20		ns		
Column address hold time (referenced to RAS)	^t AR	55		60		70		ns		
Column address to RAS lead time	^t RAL	35		45		55		ns		
Read command setup time	†RCS	0		0		0		ns	2	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19,	
Read command hold time (referenced to RAS)	^t RRH	0		10		10		ns	1	
CAS to output in Low-Z	^t CLZ	0		0		0		ns		
Output buffer turn-off delay	†OFF	0	20	0	20	0	20	ns	20,	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS -7		7	-8		-10				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output disable time	đQt		15		20	3 2 5 6 6 8 6	20	ns	30
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to RAS)	^t WCR	50		55		70		ns	26
Write command pulse width	tWP	15		15		20		ns	26
Write command to RAS lead time	^t RWL	20		35	1	40		ns	26
Write command to CAS lead time	tCWL	20		35		40	100	ns	26
Data-in setup time	t _{DS}	0		0		0		ns	22
Data-in hold time	^t DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	tDHR .	50		60		70		ns	
RAS to WE delay time	tRWD	90		100		125		ns	21
Column address to WE delay time	^t AWD	65		70		80		ns	21
CAS to WE delay time	tCWD	50		55		70		ns	21
Transition time (rise or fall)	·Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	†REF		4		4		4	ms	28
RAS to CAS precharge time	tRPC	0		10		10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		25		30		ns	5
MASKED WRITE command to RAS setup time	tWRS	0		0		0		ns	26, 27
MASKED WRITE command to RAS hold time	tWRH	15		15		15		ns	26, 27
Mask data to RAS setup time	tMS	0		0		0		ns	26
Mask data to RAS hold time	tMH	15		15		15		ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	10		20		20	31	ns	29
OE setup prior to RAS during HIDDEN REFRESH cycle	[†] ORD	0		0		0		ns	
Last WRITE to column address delay	^t LWAD	20	30	20	35	25	45	ns	
Access time from last WRITE	^t ALW	65		75		95		ns	
Output data enable from WRITE	tow	^t AA		t _{AA}		t _{AA}		ns	
Output data hold time from column address	tAOH	5		5		5		ns	
RAS hold time referenced to OE	^t ROH	10		10		10		ns	
Column address hold time referenced to RAS HIGH	^t AH	5		5		10		ns	
CAS pulse width in STATIC-COLUMN mode	tcsc	^t CAS		†CAS		†CAS		ns	
Write command inactive time	tWI	10	 	10		10		ns	

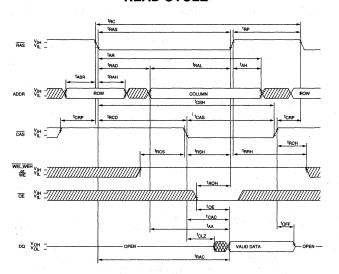
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{\text{CAS}} = \text{ViH}$, data output is High-Z.
- 12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gates and 50pF.
- 14. Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for CPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

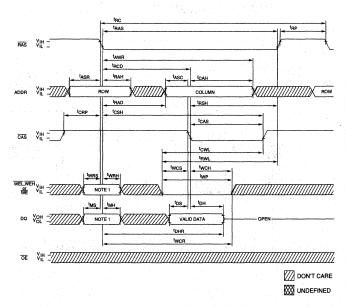
- 20. *OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case \overline{WE} = LOW and \overline{OE} =HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. WRITE command is defined as either WEL or WEH or both going LOW on the MT4C1670. WRITE command is defined as WE going LOW on the MT4C1671.
- Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
- 28. The refresh period may be extended to 8ms without experiencing problems.
- 29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 31. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.



READ CYCLE



EARLY-WRITE CYCLE

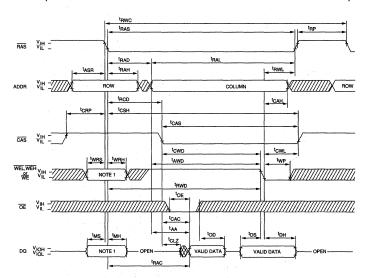


NOTE: 1. Applies to MT4C1671 only; WEL, WEH and DQ inputs on MT4C1670 are "don't care" at RAS time.

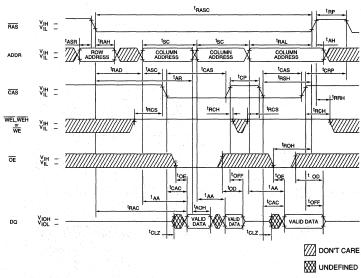
WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE



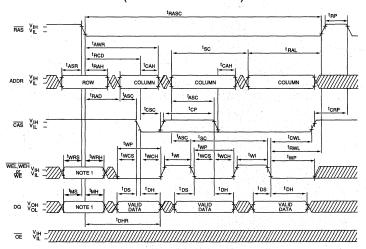
NOTE: 1. Applies to MT4C1671 only; WEL, WEH and DQ inputs on MT4C1670 are "don't care" at RAS time.

WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

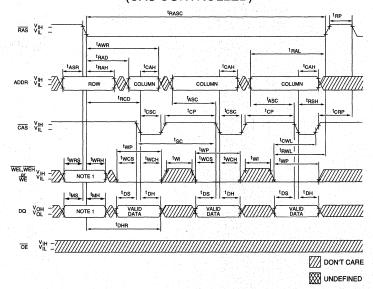
4.10



STATIC-COLUMN EARLY-WRITE CYCLE (WE CONTROLLED)



STATIC-COLUMN EARLY-WRITE CYCLE (CAS CONTROLLED)

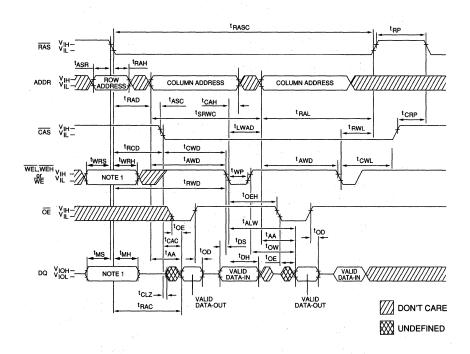


NOTE: 1. Applies to MT4C1671 only; WEL, WEH and DQ inputs on MT4C1670 are "don't care" at RAS time.

WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



STATIC COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

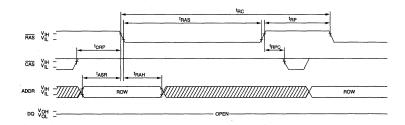


NOTE: 1. Applies to MT4C1671 only; WEL, WEH and DQ inputs on MT4C1670 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



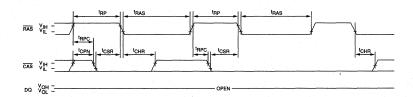
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



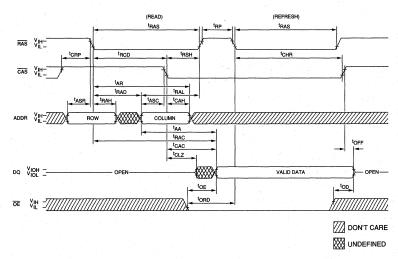
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; \overline{WEL} , \overline{WEH} or \overline{WE} , and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

64K x 16 DRAM

STATIC COLUMN MODE, LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- · All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 L only)
- 256 cycle extended refresh distributed across 32ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS	MARKING
Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
Write Enable	
Byte or Word	MT4C1670 L
Word only	MT4C1671 L
Mask Enable	
Not Available	MT4C1670 L
Always Available	MT4C1671 L
Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	\mathbf{z}
	lease consult factory for die data sheets

• Part Number Example: MT4C1670DJ-7 L

GENERAL DESCRIPTION

The MT4C1670/1 L are randomly accessed solid-state nemories containing 1,048,576 bits organized in a x16 coniguration. The MT4C1670 L has both BYTE and WORD WRITE access cycles while the MT4C1671 L has only WORD VRITE access cycles.

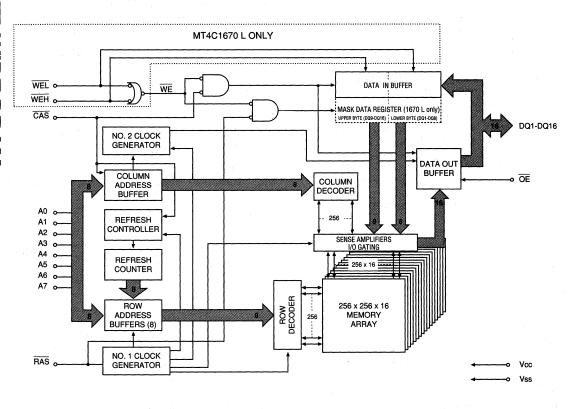
The MT4C1670 L functions in a similar manner to the MT4C1671 L except that replacing WE with WEL and VEH allows for BYTE WRITE access cycles. WEL and $\overline{\text{VEH}}$ function in an identical manner to $\overline{\text{WE}}$: either $\overline{\text{WEL}}$ or VEH will generate an internal WE through an AND gate Inverted NOR gate).

PIN	ASSIGNME	NT (Top View)
	Pin SOJ (Q-6)	40-Pin Zip (O-4)
Voc	30	NC 1 1 2 2 009 D010 3 3 4 4 D011 D012 5 6 6 D013 D014 7 6 8 D015 D016 9 7 12 10 10 Vs D01 11 7 12 10 10 Vs D01 11 7 16 D05 D06 17 16 D05 D08 19 17 16 D07 D08 19 17 10 16 D07 Vcc 21 17 12 20 NC Vcc 21 17 12 20 NC Vcc 21 17 12 24 RAS A0 25 17 12 8 A3 A4 29 17 17 28 A3 A4 29 17 17 28 A3 A4 29 17 17 30 Vcc NC 31 17 32 NC Vss 33 17 33 A4 5 A6 35 NC 37 17 36 A7 CAS 39 17 17 38 DE 11 10 10 11 11 11 11 11 11 11 11 11 11 1
*NC-WEH CI 1 *WE-WEH CI 1 *WE-WEH CI 1 *RAS CI 1 *A0 CI 1 *A1 CI 1 *A3 CI 2 *A4 CI 2 *Voc CI 2	31 H CAS 5 30 H OE 6 29 H NC 7 28 H NC 8 27 H NC 8 27 H NC 9 26 H A7 0 25 H A6 1 24 H A5	
*MT4C1671 L/M	T4C1670 L	

The MT4C1670 L "WE" function and timing are determined by the first BYTEWRITE (WEL or WEH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTEWRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 L has NONPERSISTENT MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	RAS	Input	ROW Address Strobe: RAS is used to clock-in the 8 row address bits and strobe the WEL, WEH and DQ inputs for the MASKED WRITE function.
29	39	31 A 16	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38 1	30	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL and WEH must be HIGH before OE will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	WE/WEL*	Input	Write Enable Lower Byte: WEL on MT4C1670 L is WE control for the DQ1 through DQ8 inputs. WE on MT4C1671 L controls DQ1 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/WEH*	Input	Write Enable Upper Byte: WEH on MT4C1670 L is WE control for the DQ9 through DQ16 inputs. If (WEL or WEH)/WE is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word out of the 64K available words.
2-9, 32-39,	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL or WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	13, 27-29, 35	NC		No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671 L/MT4C1670 L

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 addressbits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. RAS is used to latch the first 8 bits and CAS the latter 8 bits.

READ or WRITE cycles on the MT4C1671 L are selected with the WE input while either WEL or WEH perform the "WE" on the MT4C1670 L. The MT4C1670 L "WE" function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Taking $\overline{\text{WE}}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$ cose LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ remain LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE, WEL and WEH (MT4C1670 L) or WE (MT4C1671 L).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have CAS or WE toggled strobing-in the different column addresses. Returning RAS HIGH terminates the STATIC COLUMN operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 256 combinations of RAS addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS must be clocked by an external source during the BBU MODE or "SLEEP MODE".

BYTE WRITE ACCESS CYCLE (MT4C1670 L ONLY)

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling WEH will select an upper BYTE WRITE (DQ9-DQ16). Enabling both WEL and WEH selects a WORD WRITE cycle.

The MT4C1670 L may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1671 L is only word selectable when \overline{WE} is LOW at \overline{RAS} time (the MT4C1670 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at \overline{RAS} time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At \overline{CAS} time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 L MASKED WRITE operation (Note: \overline{RAS} or \overline{CAS} time refers to the time at which \overline{RAS} or \overline{CAS} transition from HIGH to LOW).



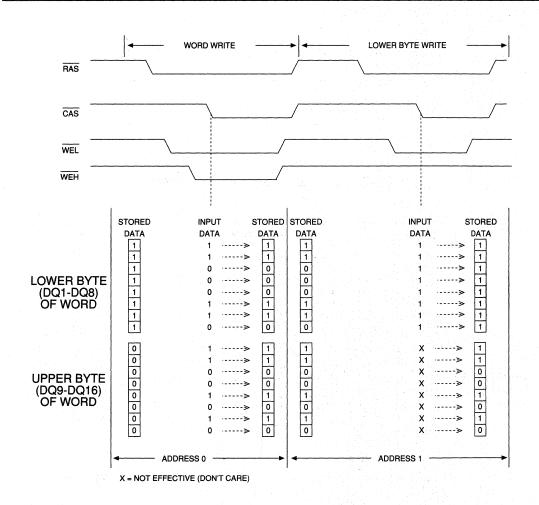


Figure 1
MT4C1670 L WORD AND BYTE WRITE EXAMPLE

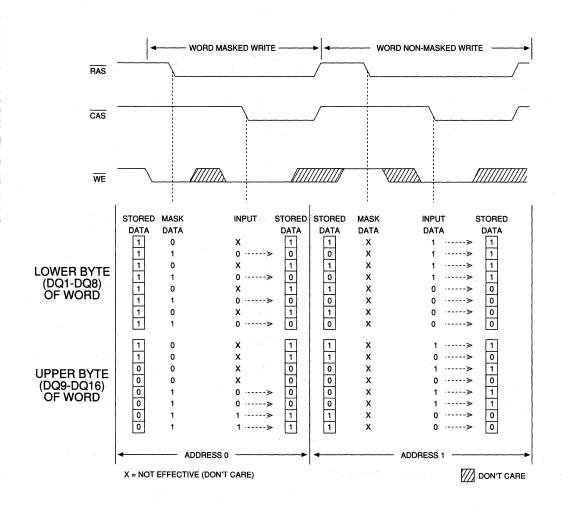


Figure 2
MT4C1671 L MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C1670 L

4.							ADDRE	SSES		
FUNCTION		RAS	CAS	WEL	WEH	OE	^t R	tC.	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	. X	Х	High-Z	
READ		L	L	Н	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	Х	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	, L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	Н	Н	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	L	Х	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	Н	Х	X	Х	ROW	n/a	High-Z	
CAS-BEFORE-RA	AS	H→L	L	Х	Х	Х	X	Х	High-Z	
BATTERY BACK	UP	H→L	L	Х	Х	Х	X	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Either CAS or WEL / WEH must latch in each additional column address and input data.

TRUTH TABLE: MT4C1671 L

	·					ADDRE	SSES		
FUNCTION		RAS	CAS	WE	0E	t _R	tC.	DQs	NOTES
Standby		Н	H→X	X	Х	Х	X	High-Z	
READ		L.	L	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	Х	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L .	L	Н	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	Х	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	Х	n/a	COL	Data In	1,3
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH	N	L	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	Х	X	Х	Х	High-Z	
BATTERY BACKUP REFRESH		H→L	L	Х	Х	Х	Х	High-Z	

NOTE:

- 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
- 2. EARLY-WRITE only.
- 3. Either CAS or WEL / WEH must latch in each additional column address and input data.



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss $^{-1.0V}$ to $^{+7.0V}$ Operating Temperature, T_A (Ambient) 0 °C to $^{+70}$ °C Storage Temperature (Plastic) $^{-55}$ °C to $^{+150}$ °C Power Dissipation 1 1W Short Circuit Output Current 50 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0° C $\leq T_A \leq 70^{\circ}$ C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	1 (4) (4) (4) (4) (4) (4) (4) (4) (4) (4)	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (IouT = -2.5mA)	Vон	2.4		· V	
Output Low Voltage (IouT = 2.3mA)	Vol		0.4	V	

			MAX		1	
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	Icc2	300	300	300	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	Іссз	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current (RAS = VIL; CAS, Address Cycling: [†] SC = [†] SC (MIN))	Icc4	110	95	80	mA	3, 4, 31
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ¹RC = ¹RC (MIN))	lcc5	120	115	90	mA	3, 31
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: tRC = tRC (MIN))	Icce	120	115	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1,000ns; WE, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	400	400	400	μΑ	3, 5, 28

CAPACITANCE

(Note: 2)

PARAMETER	 SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	 C _{l1}		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/WE, OE	Cı2		7	рF	2
Input/Output Capacitance: DQ	Сю		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			·7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		150		180		ns	
READ-WRITE cycle time	^t RWC	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	tSC	45		50		55		ns	
STATIC-COLUMN READ-WRITE cycle time	^t SRWC	95		100		120		ns	
Access time from RAS	^t RAC		70		80		100	ns	14
Access time from CAS	†CAC		25		35		40	ns	15
Output Enable time	^t OE		25		35		40	ns	
Access time from column address	†AA		40		45	-	55	ns	
Access time from CAS precharge	^t CPA		45		50		55	ns	
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (STATIC COLUMN)	†RASC	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20	1	35	1	40	1	ns	
RAS precharge time	tRP	50	· .	60		70		ns	
CAS pulse width	^t CAS	25	100,000	35	100,000	40	100,000	ns	
CAS hold time	tCSH	70		80		100		ns	
CAS precharge time	^t CPN	10		10		15		ns	16
CAS precharge time (STATIC COLUMN)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	45	25	60	ns	17
CAS to RAS precharge time	^t CRP	5		10		10		ns	
Row address setup time	^t ASR	0		0		0		ns	
Row address hold time	^t RAH	10		12		15		ns	
RAS to column address delay time	^t RAD	15	35	17	40	20	55	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		20		ns	
Column address hold time (referenced to RAS)	^t AR	55		60		70		ns	
Column address to RAS lead time	^t RAL	35		45		55		ns	
Read command setup time	†RCS	0		0		0	1844 J.	ns	26
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	^t RRH	0	Consider Environment	10		10		ns	19
CAS to output in Low-Z	tCLZ	0		0	1 1 1 1 1 1 1	0	4	ns	3447.5
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20, 30



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	24		7		8	-	10	1 1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output Disable time	tOD		15		20		20	ns	30
Write command setup time	twcs	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20	100	ns	26
Write command hold time (referenced to RAS)	tWCR	50		60		70		ns	26
Write command pulse width	^t WP	15		15		20	100	ns	26
Write command to RAS lead time	tRWL	20		35		40		ns	26
Write command to CAS lead time	tCWL	20		35		40		ns	26
Data-in setup time	^t DS	0		0		0		ns	22
Data-in hold time	†DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	50		60		70		ns	
RAS to WE delay time	tRWD	90		100		125		ns	21
Column address to WE delay time	^t AWD	65		70		80		ns	21
CAS to WE delay time	tCWD	50		55		70		ns	21
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	†REF		32	 	32	 	32	ms	28
RAS to CAS precharge time	tRPC	0		10		10	100	ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time	^t CHR	15		25		30		ns	5
(CAS-BEFORE-RAS refresh)	tWRS	0	<u> </u>	0		 	-		00.07
MASKED WRITE command to RAS	WHS	U		0		0		ns	26, 27
setup time MASKED WRITE command to RAS	tWRH	15		1.5		1.5			06.07
hold time	144			15		15	Target and the	ns	26, 27
Mask data to RAS setup time	tMS	0		0		0		ns	26
Mask data to RAS hold time	tMH	15		15		15	11.00 (4.00)	ns	26
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	10		20		20		ns	29
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0	in the second	ns	
Last WRITE to column address delay	^t LWAD	20	30	20	35	25	45	ns	
Access time from last WRITE	†ALW	65		75		95		ns	
Output data enable from WRITE	tow	†AA		tAA.		†AA		ns	
Output data hold time from column address	tAOH	5		5		5		ns	
RAS hold time referenced to OE	^t ROH	10		10		- 10	1	ns	
Column address hold time referenced to RAS HIGH	tAH	5		5		10	and the second	ns	
CAS pulse width in STATIC-COLUMN mode	tcsc	^t CAS		†CAS		†CAS		ns	
Write command inactive time	tWI	10		10		10		ns	

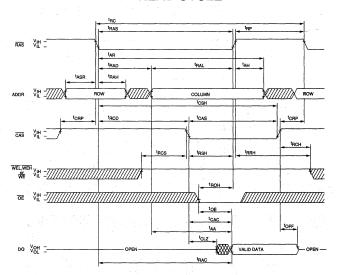
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{\rm IL}$ and $V_{\rm IL}$ (or between $V_{\rm IL}$ and $V_{\rm IH}$) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gates and 50pF
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

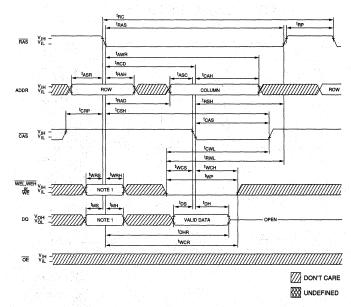
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case WE = LOW and OE=HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. WRITE command is defined as either WEL or WEH or both going LOW on the MT4C1670 L. WRITE command is defined as WE going LOW on the MT4C1671 L.
- Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
- BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.
- 29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 31. Column address changed once while \overline{RAS} = VIL and \overline{CAS} = VIH.



READ CYCLE



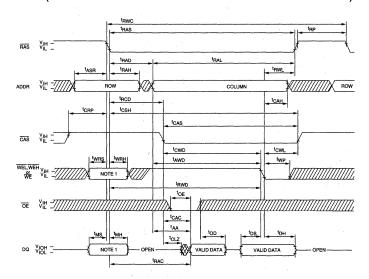
EARLY-WRITE CYCLE



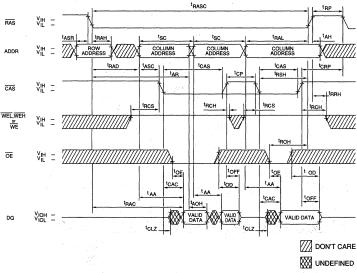
NOTE: 1. Applies to MT4C1671 L only; WEL, WEH and DQ inputs on MT4C1670 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE

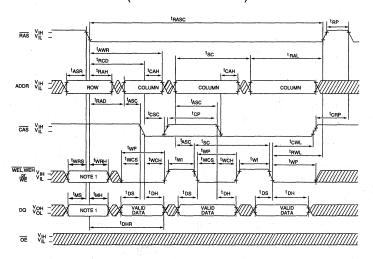


NOTE:

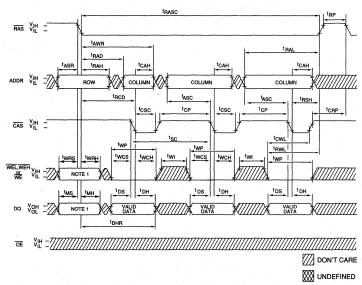
1. Applies to MT4C1671 L only; WEL, WEH and DQ inputs on MT4C1670 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



STATIC-COLUMN EARLY-WRITE CYCLE (WE CONTROLLED)



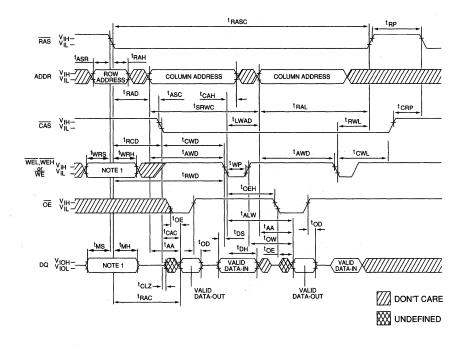
STATIC-COLUMN EARLY-WRITE CYCLE (CAS CONTROLLED)



NOTE:

1. Applies to MT4C1671 L only; WEL, WEH and DQ inputs on MT4C1670 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

STATIC-COLUMN READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

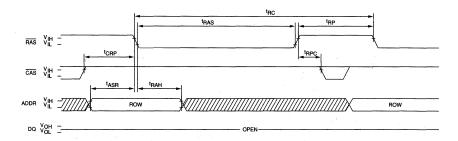


1. Applies to MT4C1671 L only; WEL, WEH and DQ inputs on MT4C1670 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.



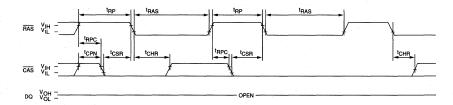
RAS-ONLY REFRESH CYCLE

 $(ADDR = A0-A7, \overline{OE}; \overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = DON'T CARE)$



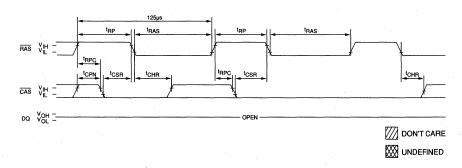
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; \overline{WEL} , \overline{WEH} or \overline{WE} , and $\overline{OE} = DON'T$ CARE)



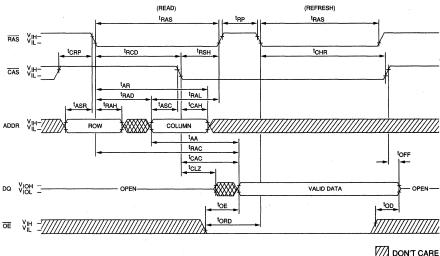
BATTERY BACKUP REFRESH CYCLE

(A0-A7; \overline{WEL} , \overline{WEH} or \overline{WE} , and $\overline{OE} = DON'T CARE$)





HIDDEN REFRESH CYCLE 24 $(\overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = HIGH; \overline{OE} = LOW)$



DON'T CARE

₩ undefined



DRAM

256K x 16 DRAM

FAST PAGE MODE

FEATURES

ODTIONIC

- Industry standard x16 pinouts, timing, functions and packages
- · High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL compatible
- 512 cycle refresh in 8ms (9 rows and 9 columns)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 only)

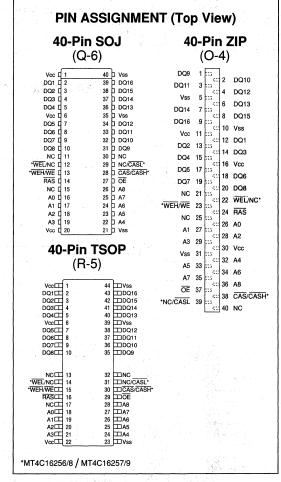
B & A DIZINIO

OPTIONS	MARKING
Timing	
70ns access	*
80ns access	- 8
100ns access	-10
Write Cycle Access	
BYTE or WORD via WE	MT4C16256
(non-maskable)	WITTC10250
BYTE or WORD via CAS	MT4C16257
(non-maskable)	, , , , , , , , , , , , , , , , , , ,
BYTE or WORD via WE	MT4C16258
(maskable)	
BYTE or WORD via CAS	MT4C16259
(maskable)	
Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	Ζ
NOTE: Assailable in die forme Dieses	

NOTE: Available in die form. Please consult factory for die data sheets.

GENERAL DESCRIPTION

The MT4C16256/7/8/9 are randomly accessed solidstate memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 and MT4C16258 have 20th BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 and MT4C16259 have 20th BYTE WRITE and WORD WRITE access cycles via 20th WRITE write and WORD WRITE access cycles via 21 wo CAS pins. The MT4C16258 and MT4C16259 are also able to perform WRITE-PER-BIT accesses.



The MT4C16256 and MT4C16257 function in the same manner except that \overline{WEL} and \overline{WEH} on MT4C16256 and \overline{CASL} and \overline{CASH} on MT4C16257 control the selection of byte WRITE access cycles. \overline{WEL} and \overline{WEH} function in an identical manner to \overline{WE} in that either \overline{WEL} or \overline{WEH} will generate an internal \overline{WE} . \overline{CASL} and \overline{CASH} function in an identical manner to \overline{CAS} in that either \overline{CASL} or \overline{CASH} will generate an internal \overline{CAS} .

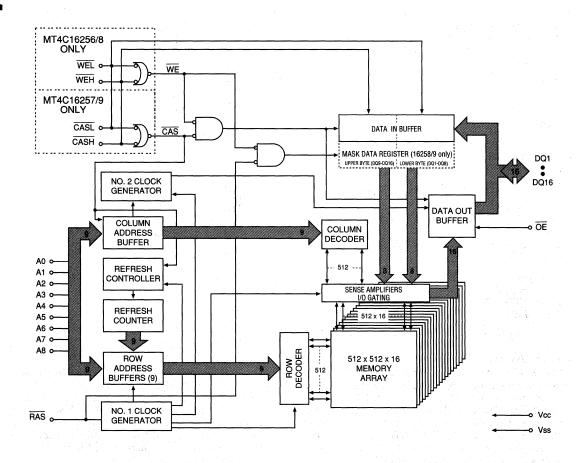
The MT4C16256 "WE" function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 "CAS" function and timing are determined by the first CAS (CASL or CASH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning

LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner during READ cycles for the MT4C16257.

The MT4C16258 and MT4C16259 function in the same manner as MT4C16256 and MT4C16257, respectively; and they have NONPERSISTENT MASKED WRITE cycles capabilities. This option allows the MT4C16258 and MT4C16259 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM





MT4C16256/7/8/9 256K x 16 DRAM

PIN DESCRIPTIONS

SOJ Pins	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
3. 14 (1.25)	16	24	RAS	Input	ROW Address Strobe: RAS is used to latch in the 9 row-address bits and strobe the WE and DQs on the MASKED WRITE option (MT4C16258 and MT4C16259 only).
28	28 30 38 CAS/ C				Column Address Strobe: CAS (MT4C16256/8) is used to latch-in the 9 column-address bits and enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. CAS controls DQ1 through DQ16.
					Column Address Strobe Upper Byte: CASH (MT4C16257/9) is the CAS control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	ŌĒ	Input	Output Enable: \overline{OE} enables the output buffers when taken LOW during a READ access cycle. \overline{RAS} and \overline{CAS} (MT4C16256/8) or \overline{CASL} / \overline{CASH} (MT4C16257/9) must be LOW and \overline{WEL} / \overline{WEH} (MT4C16256/8) or \overline{WE} (MT4C16257/9) must be HIGH before \overline{OE} will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	WEH/WE	Input	Write Enable Upper Byte: WEH (MT4C16256/8) is WE control for the DQ9 through DQ16 inputs. If WE or WEH is LOW, the access is a WRITE cycle. If either WE or WEH is LOW at RAS time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
					Write Enable: WE (MT4C16257/9) controls DQ1 through DQ16inputs. If WE is LOW, the access is a WRITE cycle. The MT4C16258/9 also use WE to enable the MASK register during RAS time.
12	14	22	WEL/NC	Input	Write Enable Lower Byte: WEL (MT4C16256/8) is the WE control for DQ1 through DQ8 inputs. If WEL is LOW, the access is a WRITE cycle. If WEL is LOW at RAS time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/CASL	Input	Column Address Strobe Low Byte: CASL (MT4C16257/9) is the CAS control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS (or CASL / CASH) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

PIN DESCRIPTIONS (continued)

SOJ Pins	TSOP PINS	ZIP Pins	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL / WEH (MT4C16256/8) or CASL / CASH (MT4C16257/8) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8). The MT4C16257/9 allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle ($\overline{\text{RAD}}$ -WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW. The MT4C16256 and MT4C16258 each have one $\overline{\text{CAS}}$ control while the MT4C16257 and MT4C16259 have two: $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$.

The $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ inputs internally generate a $\overline{\text{CAS}}$ signal functioning in an identical manner to the single $\overline{\text{CAS}}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{\text{CAS}}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{\text{OE}}$ and $\overline{\text{WE}}$). $\overline{\text{CASL}}$ controls DQ1 through DQ8, and $\overline{\text{CASH}}$ controls DQ9 through DQ16.

The MT4C16257 and MT4C16259 "CAS" function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C16257 and MT4C16259 both byte READ and byte WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 or MT4C16259 are selected with the \overline{WE} input while either \overline{WEL} or \overline{WEH} perform the " \overline{WE} " on the MT4C16256 or MT4C16258. The MT4C16256 and MT4C16258 " \overline{WE} " function is determined by the first BYTE WRITE (\overline{WEL} or \overline{WEH}) to transition LOW and the last one to transition back HIGH.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled

by $\overline{\text{OE}}$, $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ (MT4C16256 and MT4C16258) or $\overline{\text{WE}}$ (MT4C16257 and MT4C16259).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH or CASL and CASH. Enabling WEL/CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling WEH or CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH or CASL and CASH selects a WORD WRITE cycle.

The MT4C16256, MT4C16257, MT4C16258 and MT4C16259 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the WE or the CAS inputs. Figure 1 illustrates the MT4C16256 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles, since it uses two \overline{CAS} inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

WIDE DRAM

MASKED WRITE ACCESS CYCLE (MT4C16258/9 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{\text{WE}}$ at $\overline{\text{RAS}}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{\text{WE}}$ is LOW at $\overline{\text{RAS}}$ time. The MT4C16256 and MT4C16257 do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and

no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 MASKED WRITE operation and Figure 5 illustrates the MT4C16259 MASKED WRITE operation.

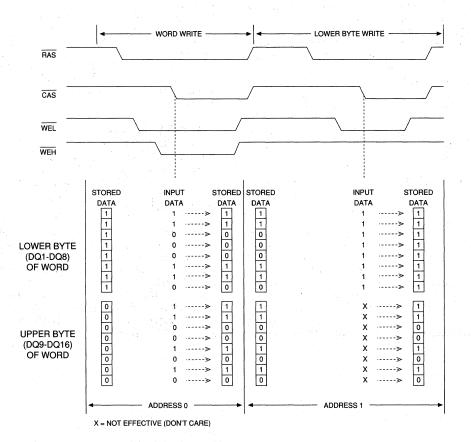


Figure 1
MT4C16256/8 WORD AND BYTE WRITE EXAMPLE

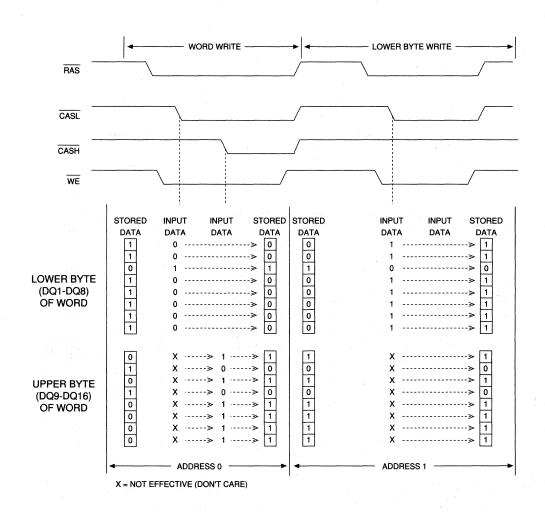


Figure 2
MT4C16257/9 WORD AND BYTE WRITE EXAMPLE

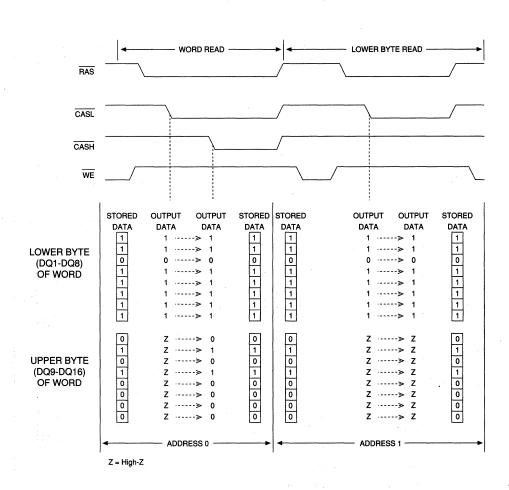


Figure 3
MT4C16257/9 WORD AND BYTE READ EXAMPLE

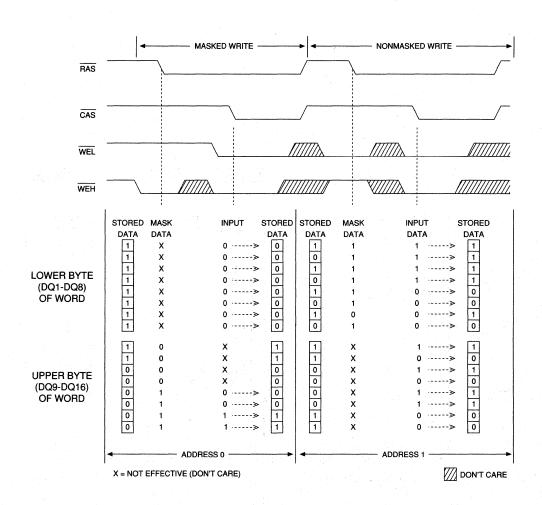


Figure 4
MT4C16258 MASKED WRITE EXAMPLE

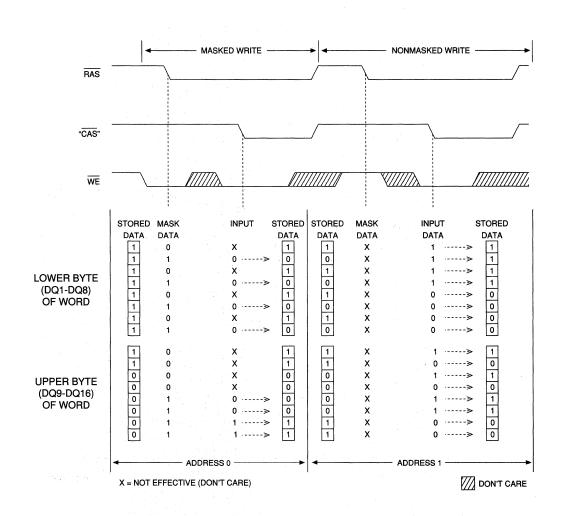


Figure 5
MT4C16259 MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C16256/8

			1 14 14				ADDR	ESSES		
FUNCTION		RAS	CAS	WEL	WEH	0E	^t R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	X	Х	High-Z	
READ		L,	L	Н	Н	L	ROW	COL	Data Out	1888
WRITE: WORD		L	L	L	L	Х	ROW	COL	Data In	3
WRITE: LOWE BYTE (EARLY)		L .	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPE BYTE (EARLY)		L) L 6	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE	iny agina a	L	on Line	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L L	H→L	L	L	Х	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L.	H→L	L	in Line	Х	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	Н	Н	H	Х	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	RAS	H→L	L	H	Н	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Data-in will be dependent on the mask provided (MT4C16258 only). Refer to Figure 4.

TRUTH TABLE: MT4C16257/9

							ADDRI	ESSES		
FUNCTION		RAS	CASL	CASH	WE	0E	^t R	t _C	DQs	NOTES
Standby		Н	H→X	H→X	Х	Χ	X	Х	High-Z	
READ: WORD		L	L	L	Н	L	ROW	COL	Data Out	
READ: LOWER	RBYTE	L	L	Н	Н	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER	BYTE	L	Н	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORE (EARLY-WRIT		L	L	L	L	Х	ROW	COL	Data In	5
WRITE: LOWE BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPE BYTE (EARLY)		L	Н	L	. L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	Н	L	ROW	COL	Data Out	2
READ	2nd Cycle	L	H→L	H→L	Н	L	n/a	COL	Data Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	Х	ROW	COL	Data In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L	Х	n/a	COL	Data In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	Н	L	ROW	COL	Data Out	2
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	Н	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	RAS	H→L	L L	L	Н	Х	Х	X	High-Z	4

NOTE:

- 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
- 2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
- 3. EARLY-WRITE only.
- 4. Only one of the two CAS must be active (CASL or CASH).
- 3. Data-in will be dependent on the mask provided (MT4C16259 only). Refer to Figure 5.



MT4C16256/7/8/9 256K x 16 DRAM

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1./
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ Vcc (All other pins not under test = 0V)	.	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		V	
Output Low Voltage (lout = -3.11A)	Vol		0.4	٧	

		MAX					
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	1	1	mA	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc3	160	140	120	mA	3, 4, 42	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN); [†] CP, [†] ASC = 10ns)	Icc4	120	110	100	mA	3, 4, 42	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS=VIH: ^t RC = ^t RC (MIN))	lcc5	160	140	120	mA	3, 5, 42	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc6	160	140	120	mA	3, 5	

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Ci1	5	pF	2
Input Capacitance: RAS, CAS/(CASL,CASH), (WEL, WEH)/ WE, OE	C12	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-10			1 4 4 4 4	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES	
Random READ or WRITE cycle time	tRC	130		150		180		ns		
READ-WRITE cycle time	tRWC	180		200		245		ns	1,17	
FAST-PAGE-MODE READ or WRITE	^t PC	45		50		55		ns	35	
cycle time										
FAST-PAGE-MODE READ-WRITE	^t PRWC	95		100		110		ns	35	
cycle time										
Access time from RAS	^t RAC		70		80		100	ns	14	
Access time from CAS	tCAC		20		20		25	ns	15, 33	
Output Enable time	^t OE		20		20		25	ns	33	
Access time from column address	^t AA		35		40		45	ns		
Access time from CAS precharge	^t CPA		40		45		55	ns	33	
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns		
RAS pulse width (PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns		
RAS hold time	tRSH	20		20		25		ns	40	
RAS precharge time	tRP	50		60		70		ns		
CAS pulse width	^t CAS	20	100,000	20	100,000	25	100,000	ns	39	
CAS hold time	^t CSH	70		80		100		ns	32	
CAS precharge time	tCPN	10		10		10		ns	16, 36	
CAS precharge time (PAGE MODE)	^t CP	10		10		10		ns	36	
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17, 31	
CAS to RAS precharge time	tCRP	10		10		10		ns	32	
Row address setup time	†ASR	0		0		0		ns		
Row address hold time	^t RAH	10		10		15	**	ns		
RAS to column	tRAD	15	35	15	40	20	55	ns	18	
address delay time										
Column address setup time	tASC	0		0		0		ns	31	
Column address hold time	[†] CAH	15		15		20	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns	31	
Column address hold time (referenced to RAS)	^t AR	55		60		75		ns		
Column address to RAS lead time	^t RAL	35		40		55		ns		
Read command setup time	^t RCS	0		0		0	1.73	ns	26, 31	
Read command hold time (referenced to CAS)	^t RCH	0	a salay a salay	0		0		ns	19, 26 ,32	
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19	
CAS to output in Low-Z	†CLZ	0		0		0	 	ns	33	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le +70^{\circ}C$; $Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	15	0	20	ns	20, 29, 33
Output disable time	tOD.	<i>y</i>	15		15		20	ns	29, 41
Write command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	15		15		20		ns	26, 40
Write command hold time (referenced to RAS)	^t WCR	55		60		75	1.5%	ns	26
Write command pulse width	tWP	10		10		20	13,75	ns	26
Write command to RAS lead time	tRWL	20		20	100	25		ns	26
Write command to CAS lead time	tCWL	20		20	and the second	25		ns	26, 32
Data-in setup time	†DS	0		0	1.1	0	100	ns	22, 33
Data-in hold time	tDH	15		15	11/2/3	20	1000	ns	22, 33
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	†RWD	95		105		135		ns	21
Column address to WE delay time	^t AWD	60		65		80		ns	21
CAS to WE delay time	tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	ŧΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	†REF		8		8		8	ms	28
RAS to CAS precharge time	^t RPC	10		10		10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5, 31
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 32
MASKED WRITE command to RAS setup time	twrs	0		0		0.		ns	26, 27
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	†WRH	15		15		15		ns	26
Mask data to RAS setup time	tMS	0		0	3.00	0		ns	26, 27
Mask data to RAS hold time	tMH	15		15	Je s	15	1	ns	26, 27
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	20		20	. 91.75	25		ns	28
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0	7. 4	0		ns	
Last CAS going LOW to first CAS to return HIGH	†CLCH	10		10	la elektri. Ligi yada	10		ns	34
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	

NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $VCC = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the TREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIIL and VIH) in a monotonic manner.
- 11. If CAS = VIH, data output is High-Z.
- 12. If CAS = Vπ, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gate and 100pF.
- 14. Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to VIH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if \overline{OE} is LOW then taken HIGH before \overline{CAS} goes HIGH, Q goes open. If \overline{OE} is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as either WEL or WEH or both going LOW on the MT4C16256/8. Write command is defined as WE going LOW on the MT4C16257/9.
- 27. MT4C16258/9 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).

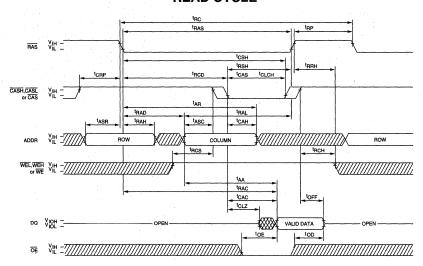


MT4C16256/7/8/9 <u>256K x 16</u> DRAM

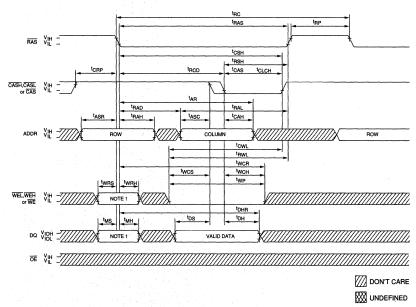
NOTES (continued)

- 30. Notes 31 through 41 apply to MT4C16257/9 only (*):
- 31. *The first CASx edge to transition LOW.
- 32. *The last CASx edge to transition HIGH.
- 33. *Output parameter (DQx) is referenced to corresponding $\overline{\text{CAS}}$ input; DQ1-DQ8 by $\overline{\text{CASL}}$ and DQ9-DQ16 by $\overline{\text{CASH}}$.
- 34. *Last falling CASx edge to first rising CASx edge.
- 35. *Last rising CASx edge to next cycle's last rising CASx edge.
- 36. *Last rising $\overline{\text{CAS}}$ x edge to first falling $\overline{\text{CAS}}$ x edge.
- 37. *First DQs controlled by the first CASx to go LOW.
- 38. *Last DQs controlled by the last CASx to go HIGH.
- 39. *Each CASx must meet minimum pulse width.
- 40. *Last CASx to go LOW.
- 41. *All DQs controlled, regardless CASL and CASH.
- 42. Column address changed once while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

READ CYCLE



EARLY-WRITE CYCLE

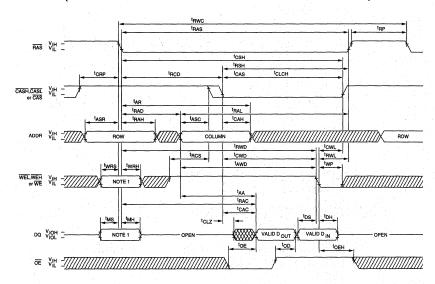


NOTE:

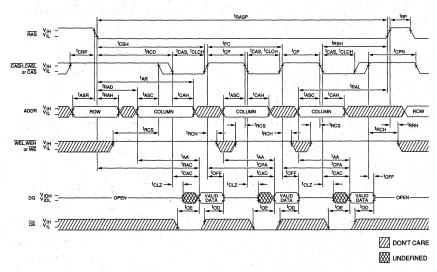
1. Applies to MT4C16258 and MT4C16259 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

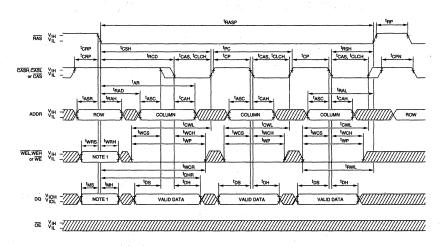


FAST-PAGE-MODE READ CYCLE

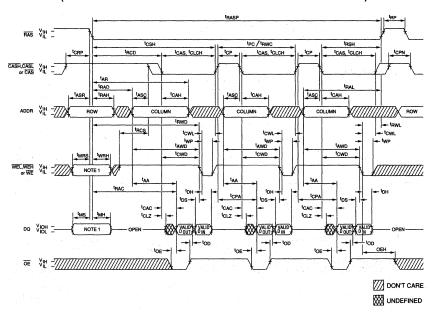


NOTE: 1. Applies to MT4C16258 and MT4C16259 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

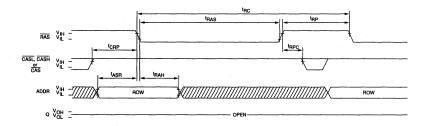


NOTE:
1. Applies to MT4C16258 and MT4C16259 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at RAS time.



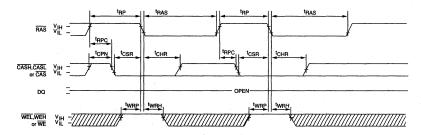
RAS ONLY REFRESH CYCLE

 $(ADDR = A0-A8, \overline{OE}; \overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = DON'T CARE)$



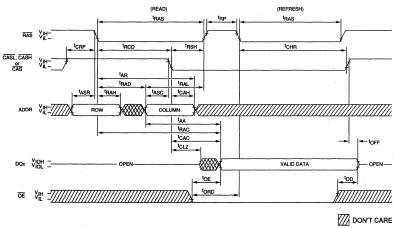
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8; and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

256K x 16 DRAM

LOW POWER, EXTENDED REFRESH

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 L only)
- 512 cycle refresh distributed across 64ms
- Low power, 1mW standby; 500mW active, typical

OPTIONS MARKING Timing - 7 70ns access - 8 80ns access 100ns access -10

Write Cycle Access	
BYTE or WORD via WE	MT4C16256 L
(non-maskable)	
BYTE or WORD via CAS	MT4C16257 L
(non-maskable)	
BYTE or WORD via WE	MT4C16258 L
(maskable)	
BYTE or WORD via CAS	MT4C16259 L
(maskable)	

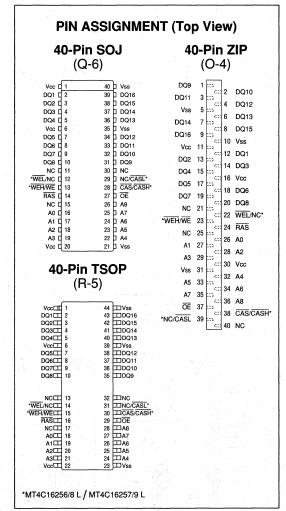
Packages	
Plastic SOJ (400 mil)	Dī
Plastic TSOP (400 mil)	ΤĠ
Plastic ZIP (475 mil)	Z

NOTE: Available in die form. Please consult factory for die data sheets.

Part Number Example: MT4C16256DJ-7 L

GENERAL DESCRIPTION

The MT4C16256/7/8/9 L are randomly accessed solidstate memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 L and MT4C16258 L have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 L and MT4C16259 L have both BYTE WRITE and WORD WRITE access cycles



via two CAS pins. The MT4C16258 L and MT4C16259 L are also able to perform WRITE-PER-BIT accesses.

The MT4C16256 L and MT4C16257 L function in the same manner except that WEL and WEH on MT4C16256 L and CASL and CASH on MT4C16257 L control the selection of byte WRITE access cycles. WEL and WEH function in an identical manner to \overline{WE} in that either \overline{WEL} or \overline{WEH} will generate an internal \overline{WE} . \overline{CASL} and \overline{CASH} function in an identical manner to \overline{CAS} in that either \overline{CASL} or \overline{CASH} will generate an internal \overline{CAS} .

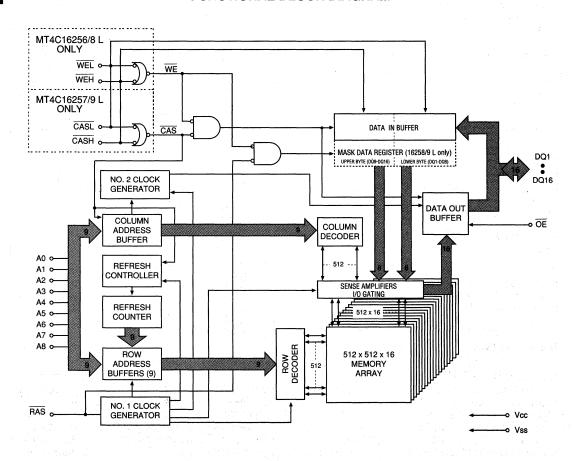
The MT4C16256 L "WE" function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 L "CAS" function and timing are determined by the first CAS (CASL or CASH) to transition LOW

and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL or CASH in the same manner during READ cycles for the MT4C16257 L.

The MT4C16258 L and MT4C16259 L function in the same manner as MT4C16256 L and MT4C16257 L, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C16258 L and MT4C16259 L to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ Pins	TSOP Pins	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	RAS	Input	ROW Address Strobe: RAS is used to latch in the 9 row- address bits and strobe the WE and DQs on the MASKED WRITE option (MT4C16258 L and MT4C16259 L only).
28	30	38	CAS/ CASH	Input	Column Address Strobe: CAS (MT4C16256/8 L) is used to latch-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. CAS controls DQ1 through DQ16.
					Column Address Strobe Upper Byte: $\overline{\text{CASH}}$ (MT4C16257/9 L) is the $\overline{\text{CAS}}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS (MT4C16256/8 L) or CASL / CASH (MT4C16257/9 L) must be LOW and WEL / WEH (MT4C16256/8 L) or WE (MT4C16257/9 L) must be HIGH before OE will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	WEH/WE	Input	Write Enable Upper Byte: WEH (MT4C1625L6/8 L) is WE control for the DQ9 through DQ16 inputs. If WE or WEH is LOW, the access is a WRITE cycle. If either WE or WEH is LOW at RAS time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
					Write Enable: \overline{WE} (MT4C16257/9 L) controls DQ1 through DQ16 inputs. If \overline{WE} is LOW, the access is a WRITE cycle. The MT4C16258/9 L also use \overline{WE} to enable the MASK register during \overline{RAS} time.
12	14	22	WEL/NC	Input	Write Enable Lower Byte: WEL (MT4C16256/8 L) is the WE control for DQ1 through DQ8 inputs. If WEL is LOW, the access is a WRITE cycle. If WEL is LOW at RAS time on MT4C16258 L, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/CASL	Input	Column Address Strobe Low Byte: CASL (MT4C16257/9 L) is the CAS control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS (or CASL / CASH) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

NEW WIDE DRAM

PIN DESCRIPTIONS (continued)

SOJ Pins	TSOP PINS	ZIP Pins	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL / WEH (MT4C16256/8L) or CASL / CASH (MT4C16257/8L) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8L). The MT4C16257/9L allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground



MT4C16256/7/8/9 L 256K x 16 DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle ($\overline{\text{READ}}$, WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW. The MT4C16256 L and MT4C16258 L each have one $\overline{\text{CAS}}$ control while the MT4C16257 L and MT4C16259 L have two: $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8, and CASH controls DQ9 through DQ16.

The MT4C16257 L and MT4C16259 L "CAS" function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C16257 L and MT4C16259 L both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 L or MT4C16259 L are selected with the $\overline{\text{WE}}$ input while either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ perform the " $\overline{\text{WE}}$ " on the MT4C16256L or MT4C16258 L. The MT4C16256 L and MT4C16258 L " $\overline{\text{WE}}$ " function is determined by the first BYTE WRITE ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking \overline{WE} LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High- Z) until the next \overline{CAS} cycle. If \overline{WE} goes LOW after \overline{CAS} goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE, WEL and WEH (MT4C16256 L and MT4C16258 L) or WE (MT4C16257 L and MT4C16259 L).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for ROW address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH or CASL and CASH. Enabling WEL/CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling WEH or CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH or CASL and CASH selects a WORD WRITE cycle.

The MT4C16256 L, MT4C16257 L, MT4C16258 L and MT4C16259 L can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{\text{WE}}$ or the $\overline{\text{CAS}}$ inputs. Figure 1 illustrates the MT4C16256 L BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 L BYTE WRITE and WORD WRITE cycles.

The MT4C16257 L also has BYTE READ and WORD READ cycles, since it uses two \overline{CAS} inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 L BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C16258/9 L Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{\text{WE}}$ at $\overline{\text{RAS}}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{\text{WE}}$ is LOW at $\overline{\text{RAS}}$ time. The MT4C16256 L and MT4C16257 L do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and

no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 L MASKED WRITE operation and Figure 5 illustrates the MT4C16259 L MASKED WRITE operation.

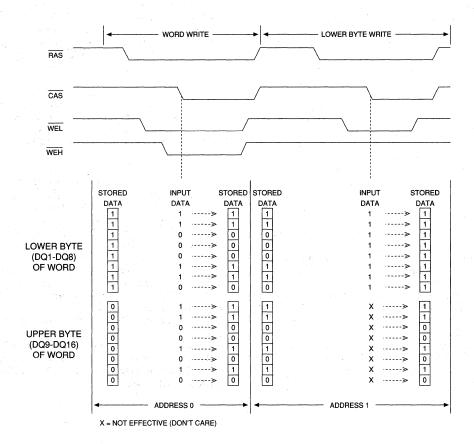


Figure 1
MT4C16256/8 L WORD AND BYTE WRITE EXAMPLE

NEW WIDE DRAM

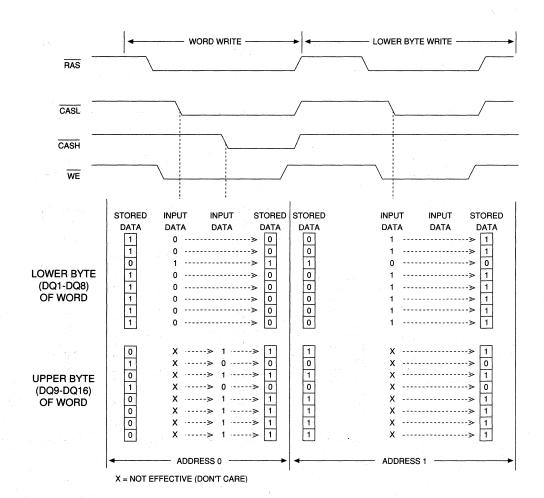


Figure 2 MT4C16257/9 L WORD AND BYTE WRITE EXAMPLE

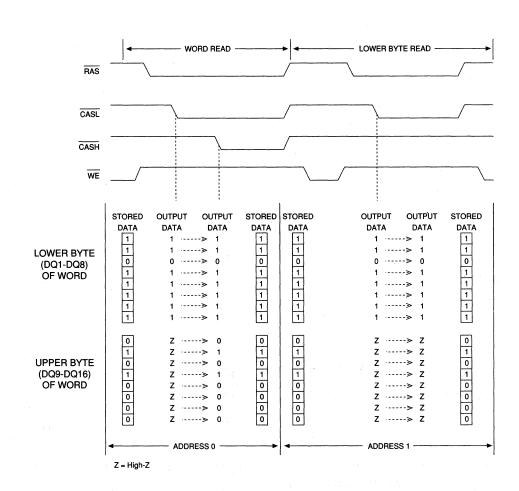


Figure 3
MT4C16257/9 L WORD AND BYTE READ EXAMPLE



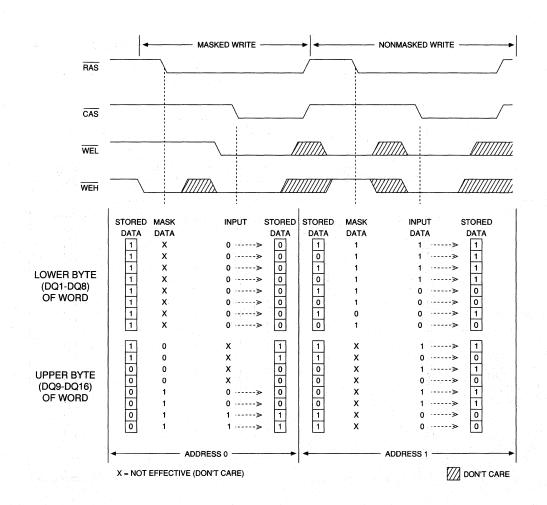


Figure 4
MT4C16258 L MASKED WRITE EXAMPLE

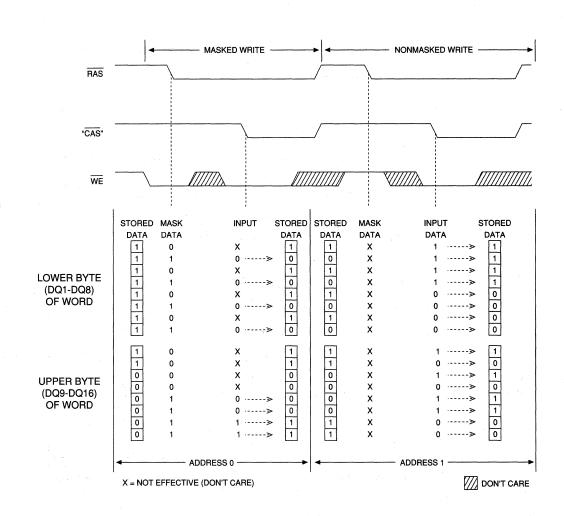


Figure 5 MT4C16259 L MASKED WRITE EXAMPLE

MT4C16256/7/8/9 L 256K x 16 DRAM

TRUTH TABLE: MT4C16256/8 L

			+15				ADDR	ESSES		
FUNCTION		RAS	CAS	WEL	WEH	0E	^t R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	X	Х	Х	High-Z	
READ		L	L	Н	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRIT	=	L	L	L	L	Х	ROW	COL	Data In	3
WRITE: LOWE BYTE (EARLY		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPE BYTE (EARLY		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		- L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	Х	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	Х	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	٦	Н	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	Н	Н	Н	Χ	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	RAS	H→L	L	Н	Н	Х	Х	Х	High-Z	
BATTERY BAC REFRESH	KUP	H→L	L	Н	Н	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Data-in will be dependent on the mask provided (MT4C16258 L only). Refer to Figure 4.

NEW WIDE DRAM

TRUTH TABLE: MT4C16257/9 L

							ADDRI	SSES		
FUNCTION		RAS	CASL	CASH	WE	ŌĒ	t _R	tC	DOs	NOTES
Standby		. Н	H→X	H→X	Х	Х	Х	Х	High-Z	
READ: WORD		L	L	L	Н	L	ROW	COL	Data Out	
READ: LOWER	RBYTE	. , L	L	Н	Н	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER	BYTE	L	Н	L	Н	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITI		L	L	L	L	Х	ROW	COL	Data In	5
WRITE: LOWE BYTE (EARLY)		L	L	. Н	L	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPEI BYTE (EARLY)	-	L	Н	L	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	Н	L	ROW	COL	Data Out	2
READ	2nd Cycle	L	H→L	H→L	Н	L	n/a	COL	Data Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L	Х	n/a	COL	Data In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	Н	L	ROW	COL	Data Out	2
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	Н	Н	Х	Х	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	-RAS	H→L	L	L	Н	Х	Х	Х	High-Z	4
BATTERY BAC REFRESH	KUP	H→L	L	L	Н	X	X	X	High-Z	4

NOTE:

- 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
- 2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
- 3. EARLY-WRITE only.
- 4. Only one of the two CAS must be active (CASL or CASH).
- 5. Data-in will be dependent on the mask provided (MT4C16259 L only). Refer to Figure 5.



MT4C16256/7/8/9 L 256K x 16 DRAM

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	lı	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	Vol		0.4	V	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	200	200	200	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	160	140	120	mA	3, 4 43
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN); [†] CP, [†] ASC = 10ns)	lcc4	120	110	100	mA	3, 4 43
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: RC = RC (MIN))	lcc5	160	140	120	mA	3, 5 43
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	160	140	120	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = †RAS (MIN) to 300ns; WE, A0-A9 and DIN = Vcc - 0.2V (DIN may be left open), †RC = 125µs (512 rows at 125µs = 64ms)	lcc7	300	300	300	μА	3, 5 42



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cit	5	pF	2
Input Capacitance: RAS, CAS/(CASL,CASH), (WEL, WEH)/ WE, OE	Cı2	7	pF	2
Input/Output Capacitance: DQ	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq $T_{A} \leq$ +70°C; Vcc = 5V $\pm 10\%$)

AC CHARACTERISTICS			-7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	130		150		180		ns	
READ-WRITE cycle time	^t RWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE	^t PC	45		50		55		ns	35
cycle time			1						ļ
FAST-PAGE-MODE READ-WRITE	^t PRWC	95		100		110		ns	35
cycle time									
Access time from RAS	^t RAC		70		80		100	ns	14
Access time from CAS	^t CAC		20		20		25	ns	15, 33
Output Enable time	^t OE		20		20		25	ns	33
Access time from column address	^t AA		35		40		45	ns	
Access time from CAS precharge	^t CPA		40		45		55	ns	33
RAS pulse width	†RAS	- 70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (PAGE MODE)	^t RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	^t RSH	20		20		25		ns	40
RAS precharge time	^t RP	50		60		70		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	25	100,000	ns	39
CAS hold time	^t CSH	70		80		100		ns	32
CAS precharge time	^t CPN	10		10		10		ns	16, 36
CAS precharge time (PAGE MODE)	^t CP	10		10		10		ns	36
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17, 31
CAS to RAS precharge time	tCRP	10		10		10		ns	32
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		15		ns	
RAS to column	^t RAD	15	35	15	40	20	55	ns	18
address delay time								20.00	
Column address setup time	†ASC	0		0		0		ns	31
Column address hold time	^t CAH	15		15		20		ns	31
Column address hold time	tAR	55		60		75		ns	
(referenced to RAS)	the term		1 1						
Column address to	^t RAL	35		40		55		ns	
RAS lead time	7				1			2.0	
Read command setup time	†RCS	0		0		0		ns	26, 31
Read command hold time	^t RCH	0	-	0		0		ns	19, 26 ,32
(referenced to CAS)						4.			
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	^t CLZ	0		0	1 2 2 2 2	0		ns	33



MT4C16256/7/8/9 L 256K x 16 DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	1	-	7		8		10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	15	0 1	20	ns	20, 29, 33
Output disable time	tOD		15		15		20	ns	29, 41
Write command setup time	twcs	0		0		0	144	ns	21, 26, 31
Write command hold time	tWCH	15		15		20		ns	26, 40
Write command hold time (referenced to RAS)	†WCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20		ns	26
Write command to RAS lead time	tRWL	20		20		25		ns	26
Write command to CAS lead time	tCWL	20		20		25		ns	26, 32
Data-in setup time	tDS	0		0		0		ns	22, 33
Data-in hold time	^t DH	15		15		20		ns	22, 33
Data-in hold time (referenced to RAS)	^t DHR	55		60		75		ns	
RAS to WE delay time	tRWD	95		105		135		ns	21
Column address to WE delay time	^t AWD	60		65		80		ns	21
CAS to WE delay time	tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	tT T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF	17.	64		64		64	ms	28
RAS to CAS precharge time	†RPC	10		10		10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5, 31
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 32
MASKED WRITE command to RAS setup time	tWRS	0		0		0		ns	26, 27
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26
Mask data to RAS setup time	tMS	0		0	7	0	1 - 7	ns	26, 27
Mask data to RAS hold time	^t MH	15		15		15	1000	ns	26, 27
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	20		20		25		ns	28
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Last CAS going LOW to first CAS to return HIGH	†CLCH	10		10		10		ns	34
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	10		10	tar a f	10		ns	

- TECHNOLO

NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gate and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

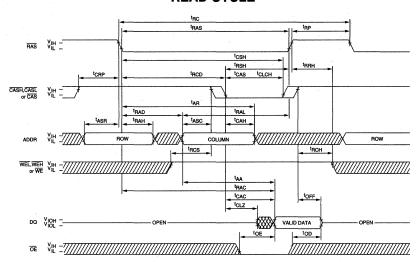
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VOH or VOL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to Vii) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if \overline{OE} is LOW then taken HIGH before \overline{CAS} goes HIGH, Q goes open. If \overline{OE} is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as either WEL or WEH or both going LOW on the MT4C16256/8 L. Write command is defined as WE going LOW on the MT4C16257/9 L.
- 27. MT4C16258/9 L only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).

MT4C16256/7/8/9 L 256K x 16 DRAM

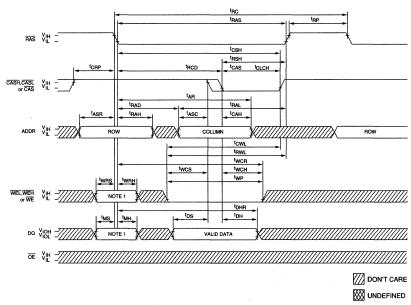
NOTES (continued)

- 30. Notes 31 through 41 apply to MT4C16257/9 L only (*):
- 31. *The first CASx edge to transition LOW.
- 32. *The last CASx edge to transition HIGH.
- 33. *Output parameter (DQx) is referenced to corresponding CAS input; DQ1-DQ8 by CASL and DQ9-DQ16 by CASH.
- 34. *Last falling CASx edge to first rising CASx edge.
- 35. *Last rising CASx edge to next cycle's last rising CASx
- 36. *Last rising \overline{CASx} edge to first falling \overline{CASx} edge.
- 37. *First DQs controlled by the first $\overline{CAS}x$ to go LOW.
- 38. *Last DQs controlled by the last CASx to go HIGH.
- 39. *Each CASx must meet minimum pulse width.
- 40. *Last CASx to go LOW.
- 41. *All DQs controlled, regardless CASL and CASH.
- 42. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.
- 43. Column address changed once while \overline{RAS} = VIL and $\overline{CAS} = V_{IH}$.

READ CYCLE



EARLY-WRITE CYCLE

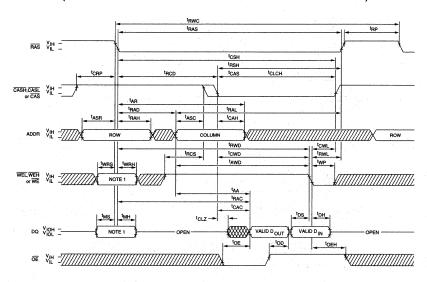


NOTE:

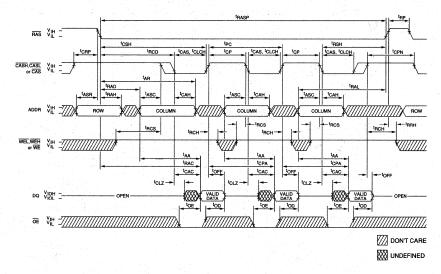
1. Applies to MT4C16258 L and MT4C16259 L only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256L and MT4C16257 L are "don't care" at RAS time.



READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

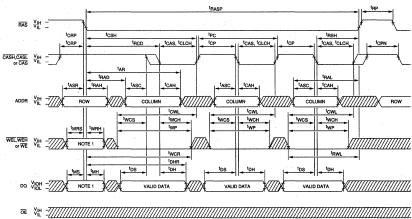


FAST-PAGE-MODE READ CYCLE

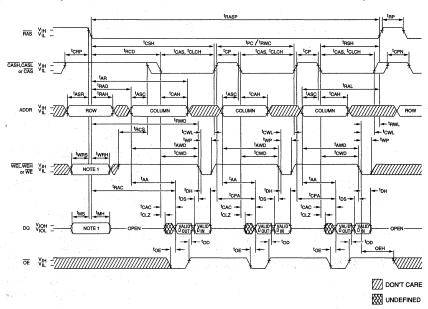


NOTE: 1. Applies to MT4C16258 L and MT4C16259 L only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



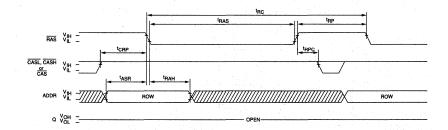
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE:
1. Applies to MT4C16258 L and MT4C16259 L only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C16256 L and MT4C16257 L are "don't care" at RAS time.

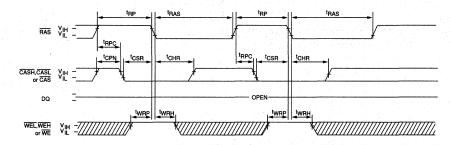


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



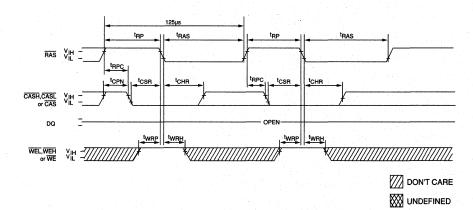
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8; and $\overline{OE} = DON'T CARE$)

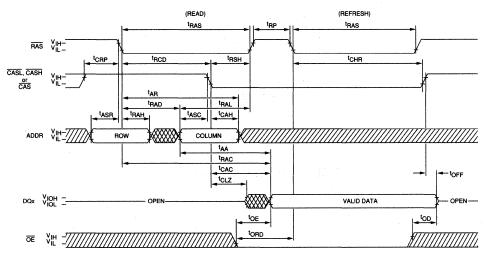


BATTERY BACKUP REFRESH CYCLE

(A0-A8; and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24 (WEL, WEH or WE = HIGH; OE = LOW)



DON'T CARE

₩ undefined



DRAM

256K x 16 DRAM

ASYMMETRICAL, FAST PAGE MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- Address entry: 10 row addresses, eight column addresses
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL compatible
- 1,024 cycle refresh in 16ms
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle, 256 locations wide
- BYTE WRITE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C16261 only)

OPTIONS	MARKING
Timing	
70ns access	- 7 D
80ns access	- 8
100ns access	-10
Masked Write	
Not Available	MT4C16260
Available	MT4C16261
Packages	
Plastic SOJ (400mil)	DJ
Plastic TSOP (400mil)	TG
Plastic ZIP (475mil)	Z

GENERAL DESCRIPTION

The MT4C16260 and MT4C16261 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. Each word or byte is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) first, then eight bits second (A0-A7). \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter eight bits.

The MT4C16260 and MT4C16261 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16261 is able to perform WRITE-PER-BIT accesses.

The MT4C16260 and MT4C16261 function in the same manner in that $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ control the selection of

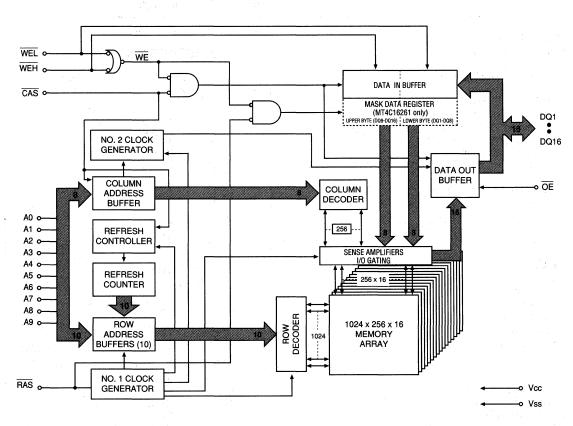
PIN ASSIG	NMEN	IT (Top	View)	
40-Pin SC (Q-6))J	4(0-Pin Z (O-4)	IP.
DO1 2 39 D02 3 38 D03 4 37 D04 0 5 6 VCC 0 6 35 D05 0 8 33 D07 0 9 32 D08 0 10 31 NC 0 11 29 WEH 0 12 29 WEH 0 15 26 A0 0 16 25 A1 0 17 24 A2 0 18 23	D Vss D Doil	DQ9 DQ11 Vss DQ14 DQ16 Vcc DQ2 DQ4 DQ5 DQ7 NC WEH NC A1	1 2 4 5 4 6 9 11 12 11 1	DQ10 DQ12 DQ13 DQ15 Vss DQ1 DQ3 Vcc DQ6 DQ8 WEL RAS A0 A2
DQ1 世 2 43 DQ2 世 3 42 DQ3 世 4 41 DQ4 世 5 40 VCC 世 6 39 DQ5 世 7 38 DQ6 世 8 37	☐ Vss ☐ DQ16 ☐ DQ15 ☐ DQ14 ☐ DQ13 ☐ VSS ☐ DQ12 ☐ DQ11 ☐ DQ10 ☐ DQ9	Vss A5 A7 ŌE *NC	31 32 33 32 35 34 37 36 39 38	A4 A6 A8 CAS NC
WEL 11 14 31 WEH 11 15 30 RAS 11 16 29 A9 II 17 28 A0 II 18 27 A1 II 19 26 A2 II 20 25 A3 II 22 24	NC N			

BYTE WRITE access cycles. \overline{WEL} and \overline{WEH} function identically to \overline{WE} in that either \overline{WEL} or \overline{WEH} will generate an internal \overline{WE} .

The WE function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16261 has NONPERSISTENT, MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ Pins	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	RAS	Input	ROW Address Strobe: RAS is used to latch in the 9 row- address bits and strobe the WE and DQs on the MASKED WRITE option.
28	30	38	CAS	Input	Column Address Strobe: CAS is used to latch-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. CAS controls DQ1 through DQ16.
2 7	29	37	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS must be LOW and WEL / WEH HIGH before OE will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	WEH	Input	Write Enable Upper Byte: WEH is WE control for the DQ9 through DQ16 inputs. If WE or WEH is LOW, the access is a WRITE cycle. If either WE or WEH is LOW at RAS time on MT4C16261, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
12.	14	22	WEL	Input	Write Enable Lower Byte: WEL is the WE control for DQ1 through DQ8 inputs. If WEL is LOW, the access is a WRITE cycle. If WEL is LOW at RAS time on MT4C16261, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS to select one 16-bit word (or 8-bit byte) out of the 256K available words.
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL / WEH to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles.
11, 15, 30, 29	13, 17, 31	21, 25, 40, 39	NC	* <u>-</u>	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. RAS is used to latch the first 10 bits (A0-A9) and CAS the latter 8 bits (A0-A7).

The CAS control also determines whether the cycle will be a refresh cycle (\overline{RAS} -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW.

A READ or WRITE cycle is selected with either $\overline{\text{WEL}}$ or WEH performing the "WE" function. The "WE" function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WELOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\mathsf{CAS}}$ cycle. If $\overline{\mathsf{WE}}$ goes LOW after $\overline{\mathsf{CAS}}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as CAS and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by \overline{OE} , \overline{WEL} and \overline{WEH} .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN refresh) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH. Enabling WEL will select a lower byte WRITE cycle (DQ1-DQ8) while Enabling WEH will select an upper byte WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH selects a word WRITE cycle.

The MT4C16260/1 may be viewed as two 256K x 8 DRAMS that have common input controls, with the exception of the WE inputs. Figure 1 illustrates the MT4C16260/1 BYTE and WORD WRITE cycles.

MASKED WRITE ACCESS CYCLE (MT4C16261 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of WE at RAS time. A MASKED WRITE is selected when \overline{WE} is LOW at \overline{RAS} time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ16 inputs at RAS time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

For NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle

Figure 2 illustrates the MT4C16261 MASKED WRITE operation (Note: RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).



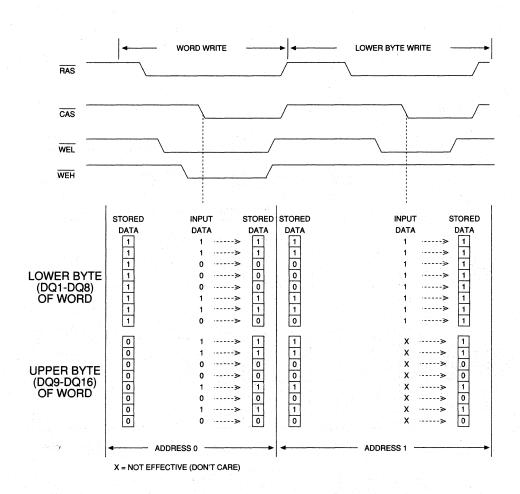


Figure 1
MT4C16260/1 WORD AND BYTE WRITE EXAMPLE

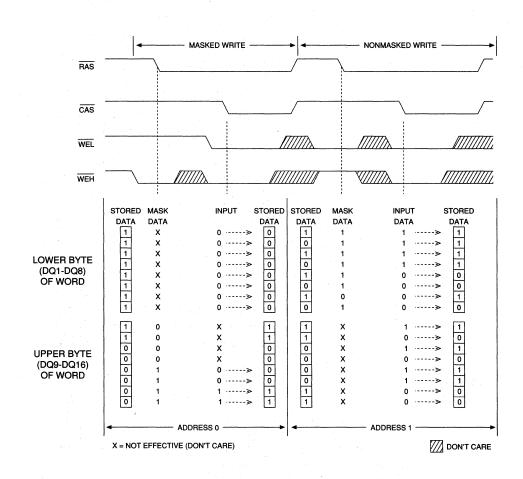


Figure 2 MT4C16261 MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C16260/1

			e a estada es	er e st.			ADDR	ESSES		
FUNCTION		RAS	CAS	WEL	WEH	0E	^t R	t _C	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	Х	Χ	High-Z	115000
READ		L	L	H ,	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)	- 1	L	L	L	L	Х	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L .	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	Н	L ,	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	ı L	H→L	Н	Н	L	n/a	COL	Data Out	tu i e
FAST-PAGE-MODE	1st Cycle	L	H→L	L	L	Х	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	Х	n/a	COL	Data In	1, 3
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	٦	L	L	Х	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	Н	X	X	Х	ROW	n/a	High-Z	1
CAS-BEFORE-R REFRESH	AS	H→L	L	Н	Н	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Data In will be dependent on the mask provided (MT4C16261 only). Refer to figure 2.



ABSOLUTE MAXIMUM RATINGS*

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0 V)	=	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)	V он	2.4		٧	
Output Low Voltage (lout = -3.mA)	Vol		0.4	V	

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

		IVIAA				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	.1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	140	130	120	mA	3, 4, 30
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN); CP, ASC = 10ns)	lcc4	100	90	80	mA	3, 4, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS=ViH: RC = RC (MIN))	lcc5	140	130	120	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	140	130	120	mA	3

MAY



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		5	pF	2
Input Capacitance: RAS, CAS, WEL, WEH, OE	Cı2		7	pF	2
Input/Output Capacitance: DQ	Сю	-	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	-7			-8		-10		5 5 55	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	130		150		180		ns	
READ-WRITE cycle time	^t RWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE	tPC	45		50		- 55		ns	
cycle time									
FAST-PAGE-MODE READ-WRITE	^t PRWC	95		100		110		ns	
cycle time									
Access time from RAS	tRAC		70		80		100	ns	14
Access time from CAS	†CAC		20		20		25	ns	15
Output Enable time	^t OE	7	20		20		25	ns	
Access time from column address	†AA		35		40		45	ns	
Access time from CAS precharge	¹ CPA		40	, , , , , , , , , , , , , , , , , , , 	45		55	ns	
RAS pulse width	†RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		20		25		ns	
RAS precharge time	tRP	50		60		70	10000000	ns	
CAS pulse width	†CAS	20	100,000	20	100,000	25	100,000	ns	
CAS hold time	tCSH	70		80		100		ns	and the same
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	50	20	60	25	75	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		15		ns	
RAS to column	tRAD .	15	35	15	40	20	55	ns	18
address delay time									
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		20		ns	
Column address hold time	tAR .	55		60		75		ns	*
(referenced to RAS)									
Column address to	tRAL	35	7-15-55	40		55		ns	
RAS lead time									
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time	tRCH	0		0		0		ns	19, 26
(referenced to CAS)									
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	†CLZ	0	1	0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	15	0	20	ns	20, 29
Output disable time	^t OD		15		15		20	ns	29
Write command setup time	twcs	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time	tWCR	55		60		75		ns	26
(referenced to RAS)									
Write command pulse width	tWP	10		10		20		ns	26
Write command to RAS lead time	^t RWL	20		20		25		ns	26
Write command to CAS lead time	tCML	20		20		25		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	^t DH	15		15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		60	-	75		ns	-
RAS to WE delay time	^t RWD	95		105		135		ns	21
Column address	tAWD	60		65		80	<u> </u>	ns	21
to WE delay time									
CAS to WE delay time	tCWD	45		45		60		ns	21
Transition time (rise or fall)	ŧΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	^t REF		16		16		16	ms	28
RAS to CAS precharge time	†RPC	10		10	·····	10		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time	^t CHR	10		10		10		ns	5
(CAS-BEFORE-RAS refresh)				·					
MASKED WRITE command to RAS setup time	twrs	0		0		0		ns	26, 27
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	10		10		15		ns	26
Mask data to RAS setup time	tMS	0		0		0		ns	26, 27
Mask data to RAS hold time	tMH	10		10		10	·	ns	26, 27
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	20		20		25		ns	28
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Last CAS going low to first CAS to return high	[†] CLCH	10		10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	†WRP	10		10		10		ns	

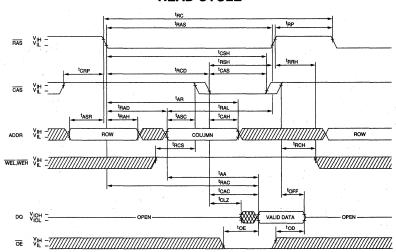


NOTES

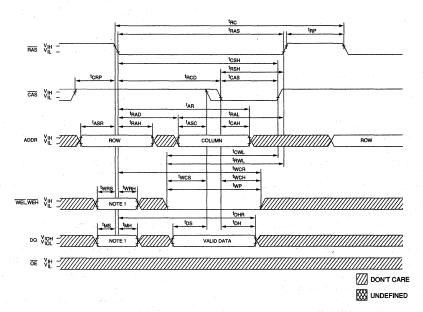
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by 8 RAS refresh cycles (RAS -ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tRAF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gate and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (max). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to VoH or VoL.
- 21. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until CAS goes back to VIH) is indeterminate. WE determines either EARLY-WRITE (WCS), LATE-WRITE (RWD, AWD and CWD) or an indeterminate (WCS or RWD, AWD and CWD not met) cycle when WE goes LOW in reference to CAS going LOW.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if \overline{OE} is LOW then taken HIGH before \overline{CAS} goes HIGH, Q goes open. If \overline{OE} is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- Write command is defined as either WEL or WEH or both going LOW.
- 27. MT4C16261 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 30. Column address changed once while $\overline{RAS} = VIL$ and $\overline{CAS} = VIH$.

READ CYCLE



EARLY-WRITE CYCLE



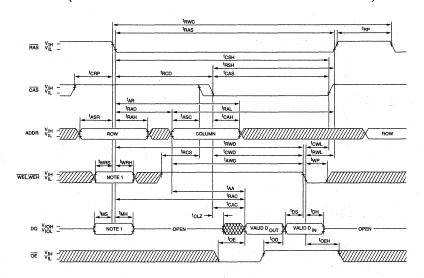
NOTE:

1. Applies to MT4C16261 only; WEL, WEH and DQ inputs on MT4C16260 are "don't care" at RAS time.

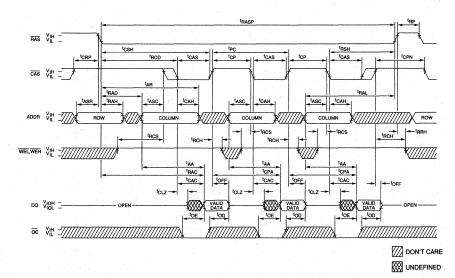
WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, with WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, with WE LOW at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

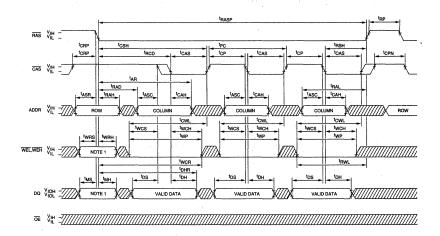


FAST-PAGE-MODE READ CYCLE

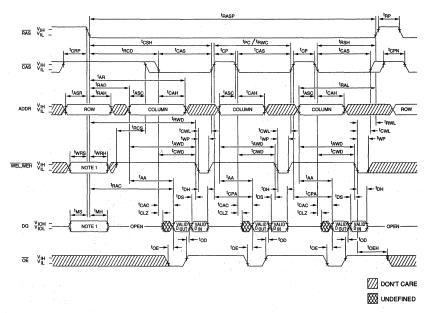


NOTE: 1. Applies to MT4C16261 only; WEL, WEH and DQ inputs on MT4C16260 are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, with WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, with WE LOW at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE:

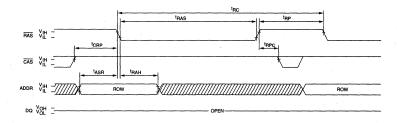
1. Applies to MT4C16261 only; WEL, WEH and DQ inputs on MT4C16260 are "don't care" at RAS time.

WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, with WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, with WE LOW at RAS time.



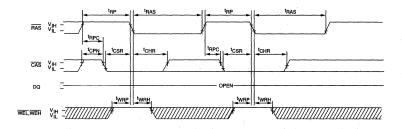
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9,, OE; WEL and WEH = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24 (WEL, WEH = HIGH; OE=LOW)

READ)

(REFRESH)

(REF

DON'T CARE

₩ UNDEFINED



DRAM

1 MEG x 16 DRAM

5.0V FAST PAGE MODE (MT4C1M16CX) 3.0/3.3V, FAST PAGE MODE (MT4LC1M16CX)

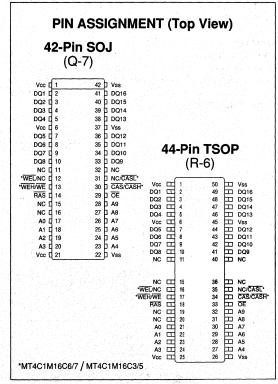
FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- · High-performance, CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- Low power, 5mW standby; 500mW active, typical (5V)
- All device pins are fully TTL compatible
- 1,024 cycle refresh in 16ms (10 rows and 10 columns)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 only)

OPTIONS	MARKING
Timing 60ns access	- 6
70ns access	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -
80ns access	- 8
Power Supply	
+5V ±10% only	4C
+3.0/3.3V ±10% only	4LC
Refresh Rate	
1,024 Rows	None
4,096 Rows	Contact Factory
Write Cycle Access	
BYTE or WORD via CAS	16C3
(non-maskable)	
BYTE or WORD via CAS	16C5
(maskable)	
BYTE or WORD via WE	16C6
(non-maskable)	
BYTE or WORD via WE	16C7
(maskable)	
Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

Part Number Example: MT4C1M16C3DJ-7

NOTE: Available in die form. Please consult factory for die data sheets.



GENERAL DESCRIPTION

The MT4C1M16CX and MT4LC1M16CX are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16CX and the MT4LC1M16CX are the same DRAM versions except that the MT4LC1M16CX is the low voltage version of MT4C1M16CX. The MT4LC1M16CX is designed to operate in either a 3.0V $\pm 10\%$ or a 3.3V $\pm 10\%$ memory system. All further references made for the MT4C1M16CX also apply to the MT4LC1M16CX, unless specifically state otherwise. The MT4C1M16C6 and MT4C1M16C7 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 and MT4C1M16C5 have both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. The MT4C1M16C5 and MT4C1M16C7 are also able to perform WRITE-PER-BIT accesses.

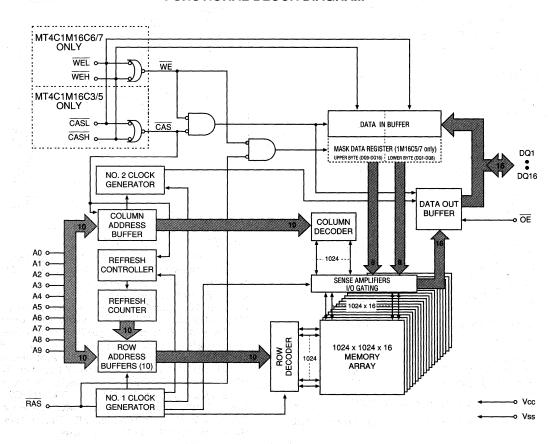
The MT4C1M16C3 and MT4C1M16C6 function in the same manner except that \overline{WEL} and \overline{WEH} on MT4C1M16C6 and \overline{CASL} and \overline{CASH} on MT4C1M16C3 control the selection of BYTE WRITE access cycles. \overline{WEL} and \overline{WEH} function in an identical manner to \overline{WE} in that either \overline{WEL} or \overline{WEH} will generate an internal \overline{WE} . \overline{CASL} and \overline{CASH} function in an identical manner to \overline{CASH} in that either \overline{CASL} or \overline{CASH} will generate an internal \overline{CAS} .

The MT4C1M16C6 "WE" function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 "CAS" function and timing are determined by the first CAS (CASL or CASH) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL or CASH in the same manner during READ cycles for the MT4C1M16C3.

The MT4C1M16C5 and MT4C1M16C7 function in the same manner as MT4C1M16C3 and MT4C1M16C6, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 and MT4C1M16C7 to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION		
14:	18	RAS	Input	ROW Address Strobe: RAS is used to latch-in the 10 row-address bits and strobe the WE and DQs on the MASKED WRITE option (MT4C1M16C5 and MT4C1M16C7 only).		
	34	CAS/ CASH	Input	Column Address Strobe: CAS (MT4C1M16C6/7) is used to latch-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles CAS controls DQ1 through DQ16.		
				Column Address Strobe Upper Byte: CASH (MT4C1M16C3/5) is the CAS control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.		
29						
13	13 17			Write Enable Upper Byte: WEH (MT4C1M16C6/7) is WE control for the DQ9 through DQ16 inputs. If WE or WEH is LOW, the access is a WRITE cycle. If either WE or WEH is LOW at RAS time on MT4C1M16C7, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).		
				Write Enable: \overline{WE} (MT4C1M16C3/5) controls DQ1 through DQ16 inputs. If \overline{WE} is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 also use \overline{WE} to enable the MASK register during \overline{RAS} time.		
12	16	WEL/NC	Input	Write Enable Lower Byte: WEL (MT4C1M16C6/7) is the WE control for DQ1 through DQ8 inputs. If WEL is LOW, the access is a WRITE cycle. If WEL is LOW at RAS time on MT4C1M16C3, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).		
31	to a transfer of the first of t					
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS (or CASL / CASH) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.		

PIN DESCRIPTIONS (continued)

SOJ Pins	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL / WEH (MT4C1M16C6/7) or CASL / CASH (MT4C1M16C3/7) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7). The MT4C1M16C3/5 allow for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	 	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 3.0/3.3V ±10% (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits.

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ -ONLY) or an active cycle ($\overline{\text{READ}}$, WRITE or READ-WRITE) once $\overline{\text{RAS}}$ goes LOW. The MT4C1M16C6 and MT4C1M16C7 each have one $\overline{\text{CAS}}$ control while the MT4C1M16C3 and MT4C1M16C5 have two: $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$.

The $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ inputs internally generate a $\overline{\text{CAS}}$ signal functioning in an identical manner to the single $\overline{\text{CAS}}$ input on the other 1 Meg x 16 DRAMs. The key difference is each $\overline{\text{CAS}}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{\text{OE}}$ and $\overline{\text{WE}}$). $\overline{\text{CASL}}$ controls DQ1 through DQ8, and $\overline{\text{CASH}}$ controls DQ9 through DQ16.

The MT4C1M16C3 and MT4C1M16C5 "CAS" function is letermined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C1M16C3 and MT4C1M16C5 both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 or MT4C1M16C5 are selected with the $\overline{\text{WE}}$ input while either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ perform the " $\overline{\text{WE}}$ " on the MT4C1M16C6 or MT4C1M16C7. The MT4C1M16C6 and MT4C1M16C7 $\overline{\text{WE}}$ " function is determined by the first BYTE WRITE $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$) to transition LOW and the last one to ransition back HIGH.

A logic HIGH on WE dictates READ mode while a logic .OW on WE dictates WRITE mode. During a WRITE cycle, lata-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a VRITE cycle, selecting DQ1 through DQ16. If WE goes .OW prior to CAS going LOW, the output pin(s) remain pen (High- Z) until the next CAS cycle. If WE goes LOW fter CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long is CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 6 pins using common I/O. Pin direction is controlled by

 $\overline{\text{OE}}$, $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ (MT4C1M16C6 and MT4C1M16C7) or $\overline{\text{WE}}$ (MT4C1M16C3 and MT4C1M16C5).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HID-DEN refresh) so that all 1024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH or CASL and CASH. Enabling WEL/CASL will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling WEH or CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH or CASL and CASH selects a WORD WRITE cycle.

The MT4C1M16C3, MT4C1M16C5, MT4C1M16C6 and MT4C1M16C7 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{\text{WE}}$ or the $\overline{\text{CAS}}$ inputs. Figure 1 illustrates the MT4C1M16C6 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 also has BYTE READ and WORD READ cycles, since it uses two CAS inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3 BYTE READ and WORD READ cycles.

MASKED WRITE ACCESS CYCLE (MT4C1M16C5/7 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1M16C3 and MT4C1M16C6 do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that

bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At CAS time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 MASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 MASKED WRITE operation.

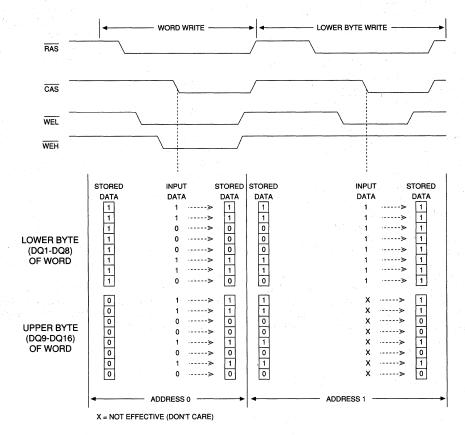


Figure 1
MT4C1M16C6/7 WORD AND BYTE WRITE EXAMPLE

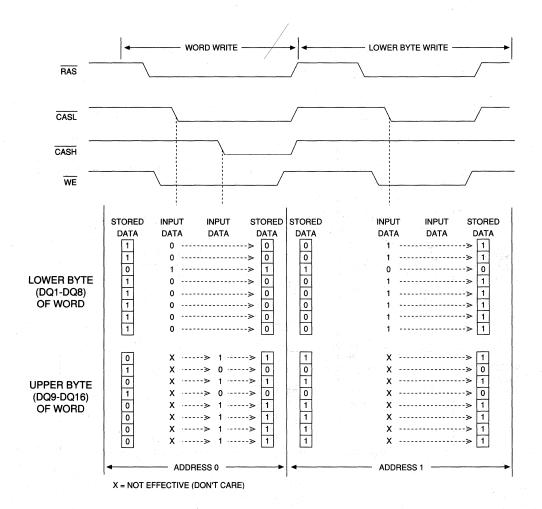


Figure 2
MT4C1M16C3/5 WORD AND BYTE WRITE EXAMPLE

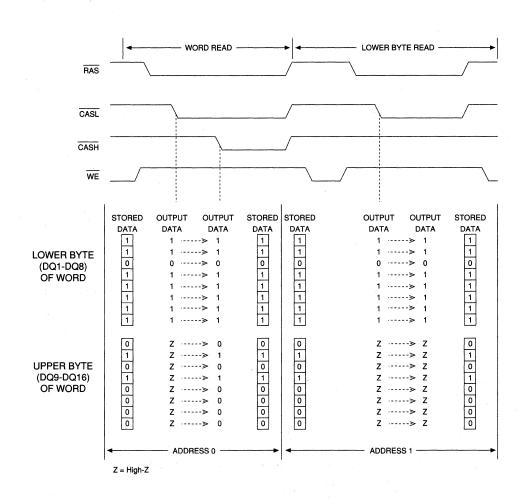


Figure 3
MT4C1M16C3/5 WORD AND BYTE READ EXAMPLE

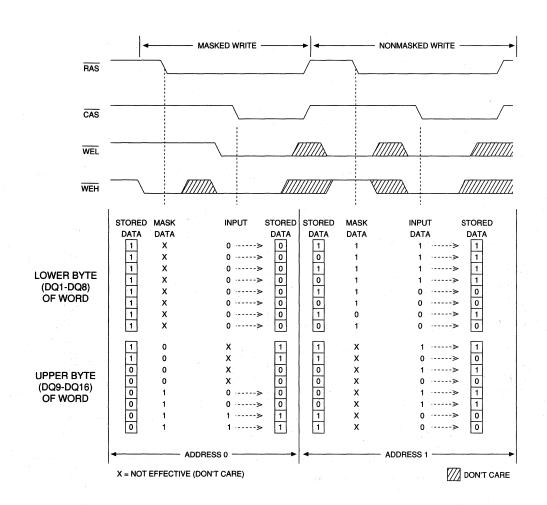


Figure 4
MT4C1M16C7 MASKED WRITE EXAMPLE

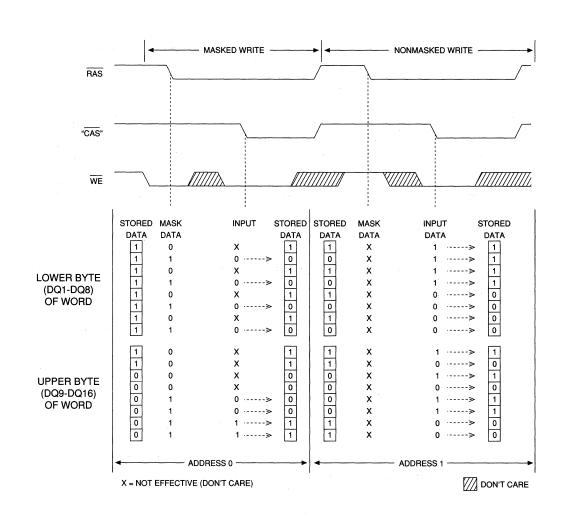


Figure 5
MT4C1M16C5 MASKED WRITE EXAMPLE



TRUTH TABLE: MT4C1M16C6/7

							ADDRI	ESSES		
FUNCTION		RAS	CAS	WEL	WEH	0E	^t R	t _C	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	Х	Х	High-Z	
READ		L	L	Н	Н	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE		L	L	L	L	Х	ROW	COL	Data In	3
WRITE: LOWE BYTE (EARLY)		14. L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPE BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	Х	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	Н	Н	Н	X	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	RAS	H→L	L	Н	Н	Х	Х	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Data-in will be dependent on the mask provided (MT4C1M16C7 only). Refer to Figure 4.

TRUTH TABLE: MT4C1M16C3/5

							ADDRI	ESSES		
FUNCTION		RAS	CASL	CASH	WE	0E	^t R	tC	DQs	NOTES
Standby		Н	H→X	H→X	Х	Х	Х	X	High-Z	
READ: WORD		L	L	L	Н	L	ROW	COL	Data Out	
READ: LOWER	RBYTE	L	L	Н	Н	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER	BYTE	L	Н	L	Н	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD		L	L	L	L	Х	ROW	COL	Data In	5
WRITE: LOWE BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPE BYTE (EARLY)	•	L	Н	L	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	.5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	Н	L	ROW	COL	Data Out	2
READ	2nd Cycle	L	H→L	H→L	Н	L	n/a	COL	Data Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	Х	ROW	COL	Data In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L ·	X	n/a	COL	Data In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	Ĥ	L	ROW	COL	Data Out	2
REFRESH	WRITE	L→H→L	L	L	L	Х	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	Н	H	X	Х	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	-RAS	H→L	L	L	Н	Х	Х	Х	High-Z	4

NOTE:

- 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
- 2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
- 3. EARLY-WRITE only.
- 4. Only one CAS must be active (CASL or CASH).
- 3. Data-in will be dependent on the mask provided (MT4C1M16C5 only). Refer to Figure 5.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:control_volume} \begin{tabular}{lll} Voltage on Vcc supply relative to Vss (5V) &-1V to +7V \\ Voltage on Vcc supply relative to Vss (3V) &-1V to +4.6V \\ Operating Temperature, T_A (Ambient) && 0°C to +70°C \\ Storage Temperature (Plastic) && -55°C to +150°C \\ Power Dissipation & ...& 1W \\ Short Circuit Output Current & ...& 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, All Inputs	Vıн	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)		-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 2.1mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 3.0/3.3V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	I	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -1.0mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 1.0mA)	Vol	194.8 1817.0	0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

Notes: 1, 3, 4, 6, 7, 42) $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 10\%)$			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	1	1	1	mA _.	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	Icc4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: **TRC = **TRC (MIN))	lcc5	170	160	140	mA	3, 5, 44
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: tBC = tBC (MIN))	lcc6	170	160	140	mA	3, 5

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 3.0/3.3V \pm 10\%)$			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = Vih)$	lcc1	1	1	1	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = Vcc -0.2V)$	lcc2	400	400	400	μА	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	130	120	100	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN); CP, ASC = 10ns)	lcc4	90	80	70	mA	3, 4, 44
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V _{IH} : ^t RC = ^t RC (MIN))	Icc5	130	120	100	mA	3, 4, 44
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	130	120	100	mA	3, 4



CAPACITANCE

(Note: 2)

PARAMETER				SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9				Ci1	5	pF	2
Input Capacitance: RAS, CAS/	(CASL,CASH), (WEL, WEH)	/ WE, OE		C ₁₂	7	pF	2
Input/Output Capacitance: DQ			a ing N	Сю	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V or 3.0/3.3V \pm 10%)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	35		40		40		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	85		95		100		. ns	35
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15, 33
Output Enable	^t OE		15		15		15	ns	23
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	33
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	40
RAS precharge time	tRP	40		50	1 34 1 344	60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	39
CAS hold time	^t CSH	60		70		80		ns	32
CAS precharge time	^t CPN	10		10		10		ns	16, 36
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	36
RAS to CAS delay time	tRCD	15	45	20	50	20	60	ns	17, 31
CAS to RAS precharge time	tCRP	5		5		5	N 15.5	ns	32
Row address setup time	tASR	0		0	10.000	0	1.7	ns	
Row address hold time	^t RAH	10		10		10		ns	1 7
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	31
Column address hold time	^t CAH	10		15		15		ns	31
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26, 32
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0	1 3 3 3	0		ns	33

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V or 3.0/3.3V \pm 10%)

AC CHARACTERISTICS		-6			7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	. 0	20	ns	20, 29, 33
WE command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to RAS)	tWCR	45		55		60	2.5	ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	tRWL	15		20		20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26, 32
Data-in setup time	tDS	0		. 0		0		ns	22, 33
Data-in hold time	^t DH	10		15		15		ns	22, 33
Data-in hold time (referenced to RAS)	tDHR	45	1	55		60		ns	
RAS to WE delay time	^t RWD	85		95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45		ns	21, 31
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	†REF		16		16		16	ms	28
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	5		5		5		ns	5, 31
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15	1 44	15		ns	5, 32
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	^t WRH	15		15		15		ns	26, 27
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26, 27
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	tOD		15		15		15	ns	29, 41
OE hold time from WE during HIDDEN REFRESH cycle	^t OEH	15		15		15		ns	28
Last CAS going LOW to first CAS to return HIGH	[†] CLCH	10		10		10	11.00	ns	34
Mask data to RAS setup time	tMS	0		0		0		ns	26, 27
Mask data to RAS setup time	tMH	15	<u> </u>	15		15	 	ns	26, 27



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = 5V or 3.0/3.3V $\pm 10\%$; f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{I\!H}$ and $V_{I\!L}$ (or between $V_{I\!L}$ and $V_{I\!H}$) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = Vπ, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF.
- 14. Assumes that 'RCD < 'RCD (MAX). If 'RCD is greater than the maximum recommended value shown in this table, 'RAC will increase by the amount that 'RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- *OFF (MAX) defines the time at which the output achieves the open circuit condition (not a reference to VOH or VOL).
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to VIH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if \overline{OE} is LOW then taken HIGH before CAS goes HIGH, Q goes open. If \overline{OE} is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as either WEL or WEH or both going LOW on the MT4C1M16C6/7. Write command is defined as WE going LOW on the MT4C1M16C3/5.
- 27. MT4C1M16C5/7 only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once ^tOF or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).

WIDE D

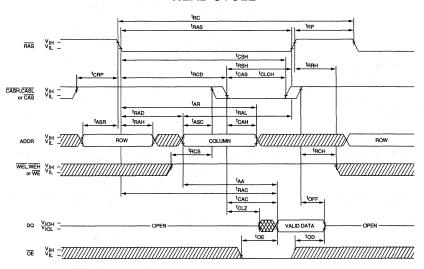
NOTES (continued)

- 30. Notes 31 through 41 apply to MT4C1M16C3/5 only (*).
- 31. *The first $\overline{CAS}x$ edge to transition LOW.
- 32. *The last CASx edge to transition HIGH.
- 33. *Output parameter (DQx) is referenced to corresponding CAS input; DQ1-DQ8 by CASL and DQ9-DQ16 by CASH.
- 34. *Last falling \overline{CASx} edge to first rising \overline{CASx} edge.
- 35. *Last rising CASx edge to next cycle's last rising CASx edge.
- 36. *Last rising CASx edge to first falling CASx edge.

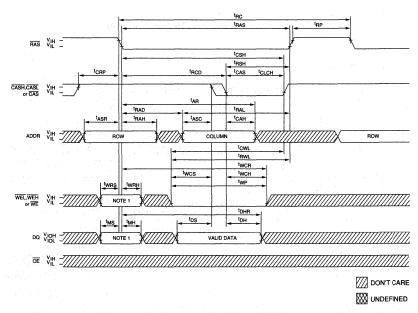
- 37. *First DQs controlled by the first CASx to go LOW.
- 38. *Last DQs controlled by the last \overline{CASx} to go HIGH.
- 39. *Each CASx must meet minimum pulse width.
- 40. *Last CASx to go LOW.
- 41. *All DQs controlled, regardless CASL and CASH.
- 42. The 5V version is restricted to operate between $4.5\,\mathrm{V}$ and $5.5\mathrm{V}$ only.
- 43. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 44. Column address changed once while \overline{RAS} = VII. and \overline{CAS} = VIII.



READ CYCLE

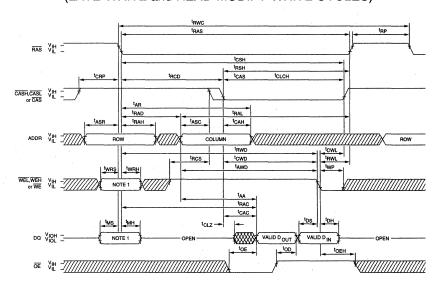


EARLY-WRITE CYCLE

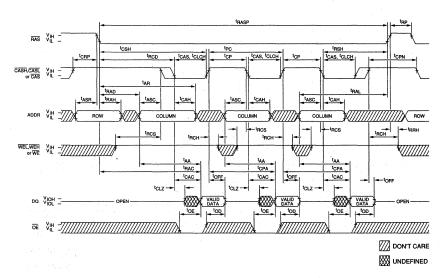


NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at RAS time.

READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



FAST-PAGE-MODE READ CYCLE

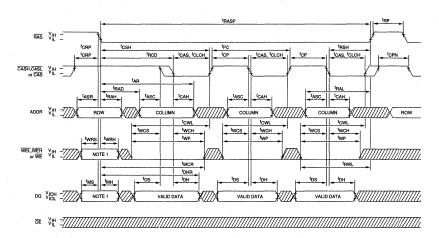


NOTE:

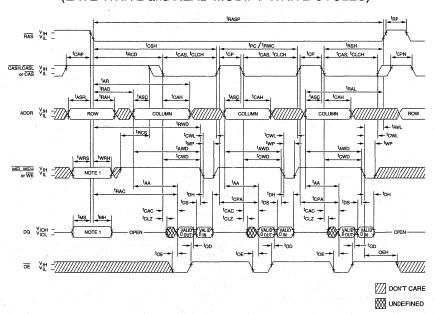
1. Applies to MT4C1M16C5 and MT4C1M16C7 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at RAS time.



FAST-PAGE-MODE EARLY-WRITE CYCLE



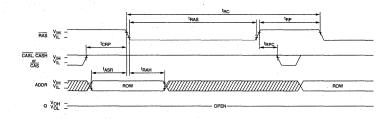
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1M16C5 and MT4C1M16C7 only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 and MT4C1M16C6 are "don't care" at RAS time.

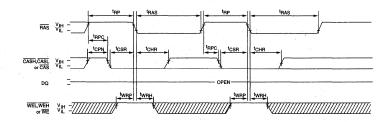
RAS-ONLY REFRESH CYCLE

 $(ADDR = A0-A9, \overline{OE}; \overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = DON'T CARE)$



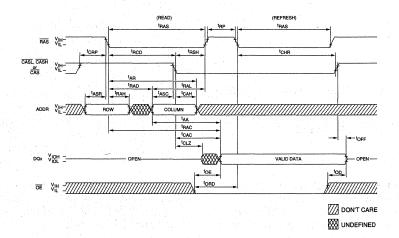
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9; and $\overline{OE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 24

 $(\overline{WEL}, \overline{WEH} \text{ or } \overline{WE} = HIGH; \overline{OE} = LOW)$





DRAM

1 MEG x 16 DRAM

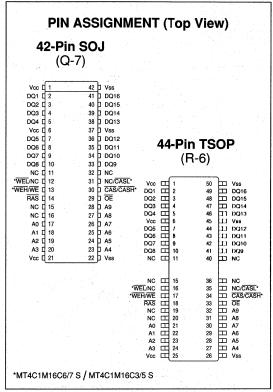
5.0V SELF REFRESH (MT4C1M16CX S) 3.0/3.3V, SELF REFRESH (MT4LC1M16CX S)

FEATURES

- Self Refresh, ie "Sleep Mode"
- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V only or +3.0/+3.3V only ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C1M16C3/5 S only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1M16C5/7 S only)
- 1,024 cycle refresh in 128ms (10 rows and 10 columns)
- Low power, 2mW standby; 500mW active, typical (5V)

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Power Supply	
+5V ±10% only	4C
+3.0/3.3V ±10% only	4LC
Refresh Rate	
1,024 Rows	None
4,096 Rows	Contact Factory
Write Cycle Access	
BYTE or WORD via CAS	16C3 S
(non-maskable)	
BYTE or WORD via CAS	16C5 S
(maskable)	
BYTE or WORD via WE	16C6 S
(non-maskable) BYTE or WORD via WE	16C7 S
(maskable)	1007.5
• Packages	
Plastic SOJ (400 mil) Plastic TSOP (400 mil)	DJ TC
Plastic Laur (400 mil)	TG

Part Number Example: MT4C1M16C3DJ-7 S
 NOTE: Available in die form. Please consult factory for die data sheets.



GENERAL DESCRIPTION

The MT4C1M16CX S and MT4LC1M16CX S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16CX S and the MT4LC1M16CX S are the same DRAM versions except that the MT4LC1M16CX S is the low voltage version of MT4C1M16CX S. The MT4LC1M16CX S is designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C1M16CX S also apply to the MT4C1M16CX S, unless specifically state otherwise. The MT4C1M16CA S and MT4C1M16C7 S have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C1M16C3 S and MT4C1M16C5 S have both BYTE WRITE and WORD WRITE access cycles via two CAS pins.

The MT4C1M16C5 S and MT4C1M16C7 S are also able to perform WRITE-PER-BIT accesses.

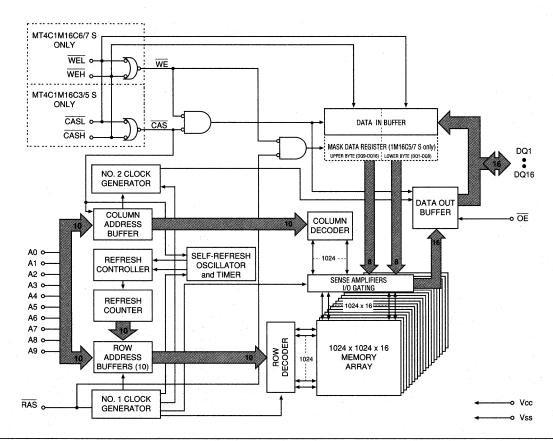
The MT4C1M16C3 S and MT4C1M16C6 S function in the same manner except that WEL and WEH on MT4C1M16C6 S and CASL and CASH on MT4C1M16C3 S control the selection of BYTE WRITE access cycles. WEL and WEH function in an identical manner to WE in that either WEL or WEH will generate an internal WE. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS.

The MT4C1M16C6 S "WE" function and timing are determined by the first WE (WEL or WEH) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8), and WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1M16C3 S "CAS" function and timing are determined by the first \overline{CAS} (\overline{CASL} or \overline{CASH}) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. \overline{CASL} transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and \overline{CASH} transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through \overline{CASL} or \overline{CASH} in the same manner during READ cycles for the MT4C1M16C3 S.

The MT4C1M16C5 S and MT4C1M16C7 S function in the same manner as MT4C1M16C3 S and MT4C1M16C6 S, respectively; and they have NONPERSISTENT MASKED WRITE cycle capabilities. This option allows the MT4C1M16C5 S and MT4C1M16C7 S to operate with either normal WRITE cycles or NONPERSISTENT MASKED WRITE cycles.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION					
14				ROW Address Strobe: RAS is used to latch-in the 10 row-address bits and strobe the WE and DQs on the MASKED WRITE option (MT4C1M16C5 S and MT4C1M16C7 S only).					
30	34	CAS/ CASH	Input	Column Address Strobe: CAS (MT4C1M16C6/7 S) is used to latch-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. CAS controls DQ1 through DQ16.					
				Column Address Strobe Upper Byte: CASH (MT4C1M16C3/5 S) is the CAS control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.					
29	33	ŌĒ	Input	Output Enable: OE enables the output buffers when taken LOW during a READ access cycle. RAS and CAS (MT4C1M16C6/7 S) or CASL / CASH (MT4C1M16C3/5 S) must be LOW and WEL / WEH (MT4C1M16C6/7 S) or WE (MT4C1M16C3/5 S) must be HIGH before OE will control the output buffers. Otherwise, the output buffers are in a High-Z state.					
13	17	WEH/WE	Input	Write Enable Upper Byte: WEH (MT4C1M16C6/7 S) is WE control for the DQ9 through DQ16 inputs. If WE or WEH is LOW, the access is a WRITE cycle. If either WE or WEH is LOW at RAS time on MT4C1M16C7 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).					
				Write Enable: WE (MT4C1M16C3/5 S) controls DQ1 through DQ16 inputs. If WE is LOW, the access is a WRITE cycle. The MT4C1M16C5/7 S also use WE to enable the MASK register during RAS time.					
12	16	WEL/NC	Input	Write Enable Lower Byte: WEL (MT4C1M16C6/7 S) is the WE control for DQ1 through DQ8 inputs. If WEL is LOW, the access is a WRITE cycle. If WEL is LOW at RAS time on MT4C1M16C3 S, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).					
31	35	NC/CASL	Input	Column Address Strobe Lower Byte: CASL (MT4C1M16C3/5 S) is the CAS control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.					
17-20, 23-28	21-24, 27-32	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS (or CASL / CASH) to select one 16-bit word (or 8-bit byte) out of the 1 Meg available words.					



PIN DESCRIPTIONS (continued)

SOJ PINS	TSOP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 33-36, 38-41	2-5, 7-10, 41-44, 46-49	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using WEL / WEH (MT4C1M16C6/7 S) or CASL / CASH (MT4C1M16C3/7 S) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All sixteen I/Os are active for READ cycles (MT4C1M16C6/7 S). The MT4C1M16C3/5 S allow for BYTE READ cycles.
11, 15, 16, 30-32	11, 15, 36, 40	NC	. -	No Connect: These pins should be left either unconnected or tied to ground.
1, 6, 21	1, 6, 25	Vcc	Supply	Power Supply: +5V ±10% (C) or 3.0/3.3V ±10% (LC)
22, 37, 42	26, 45, 50	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS goes LOW. The MT4C1M16C6 S and MT4C1M16C7 S each have one CAS control while the MT4C1M16C3 S and MT4C1M16C5 S have two: CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 1 Meg x 16 DRAMs. The key difference is each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8, and CASH controls DQ9 through DQ16.

The MT4C1M16C3 S and MT4C1M16C5 S "CAS" function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C1M16C3 S and MT4C1M16C5 S both BYTE READ and BYTE WRITE cycle capabilities.

READ or WRITE cycles on the MT4C1M16C3 S or MT4C1M16C5 S are selected with the \overline{WE} input while either WEL or WEH perform the "WE" on the MT4C1M16C6 S or MT4C1M16C7 S. The MT4C1M16C6 S and MT4C1M16C7 S "WE" function is determined by the first BYTE WRITE (WEL or WEH) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as \overline{CAS} and \overline{OE} remain LOW (regardless of \overline{WE} or \overline{RAS}). This late \overline{WE} pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE , WEL and WEH (MT4C1M16C6 S and MT4C1M16C7 S) or WE (MT4C1M16C3 S and MT4C1M16C5 S).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobedin by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN refresh) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence. The CAS-BEFORE-RAS refresh cycle will also invoke the refresh counter and controller for ROW address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. RAS or CAS time refers to the time at which RAS or CAS transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during "SLEEP MODE". Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 128ms.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of WEL and WEH or CASL and CASH. Enabling WEL/ CASL will select a lower BYTE WRITE cycle (DQ1-DQ8). Enabling WEH or CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both WEL and WEH or CASL and CASH selects a WORD WRITE cycle.

The MT4C1M16C3 S, MT4C1M16C5 S, MT4C1M16C6 S and MT4C1M16C7 S may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the WE or the CAS inputs. Figure 1 illustrates the MT4C1M16C6 S BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C1M16C3 S BYTE WRITE and WORD WRITE cycles.

The MT4C1M16C3 S also has BYTE READ and WORD READ cycles, since it uses two $\overline{\text{CAS}}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C1M16C3SBYTE READ and WORD READ cycles.

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MASKED WRITE ACCESS CYCLE (MT4C1M16C5/7 S Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of \overline{WE} at \overline{RAS} time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and \overline{WE} is LOW at \overline{RAS} time. The MT4C1M16C3 S and MT4C1M16C6 S do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at RAS time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that

bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At \overline{CAS} time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same.

Figure 4 illustrates the MT4C1M16C7 SMASKED WRITE operation and Figure 5 illustrates the MT4C1M16C5 S MASKED WRITE operation.

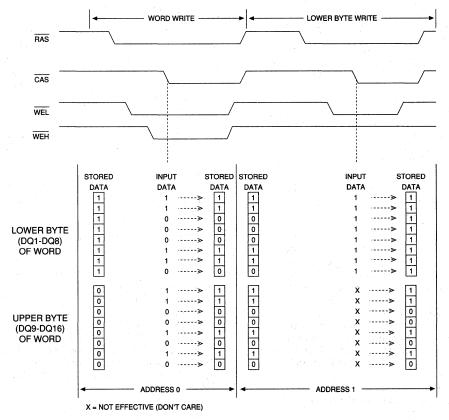


Figure 1
MT4C1M16C6/7 S WORD AND BYTE WRITE EXAMPLE

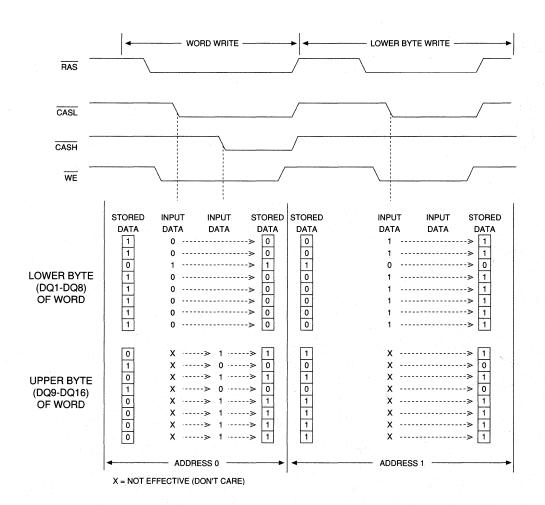


Figure 2
MT4C1M16C3/5 S WORD AND BYTE WRITE EXAMPLE

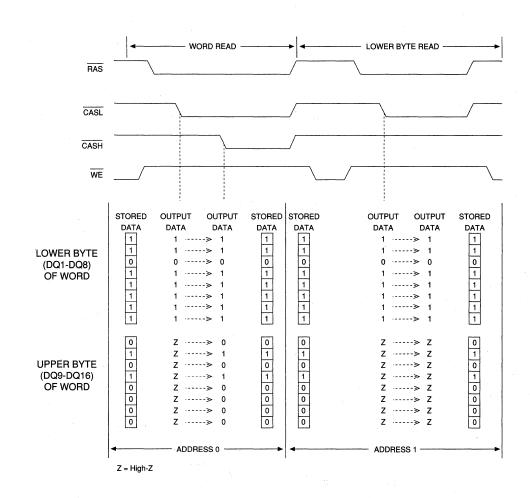


Figure 3
MT4C1M16C3/5 S WORD AND BYTE READ EXAMPLE

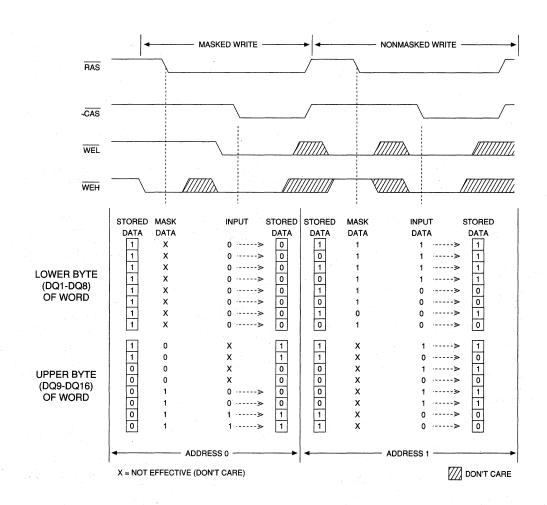


Figure 4
MT4C1M16C7 S MASKED WRITE EXAMPLE

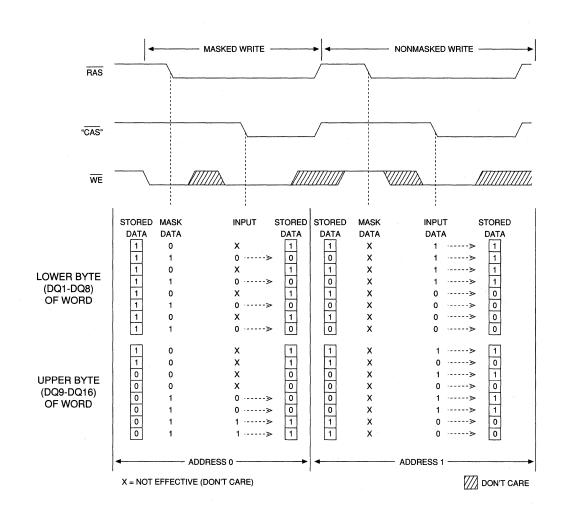


Figure 5 MT4C1M16C5 S MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1M16C6/7 S

							ADDRESSES			
FUNCTION		RAS	CAS	WEL	WEH	0E	^t R	tC	DQs	NOTES
Standby		Н	H→X	Х	Х	Х	Х	Х	High-Z	
READ		L	L	Н	Н	L	ROW	COL	Data Out	1 2
WRITE: WORD (EARLY-WRITE)		L	L	L	L	Х	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	Н	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPE BYTE (EARLY)	-	≓te L ine	L	Н	L	Х	ROW	COL	Lower Byte, High+Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	Н	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	Н	L	n/a	COL	Data Out	
PAGE-MODE	1st Cycle	L	H→L	L	L	Х	ROW	COL	Data In	1, 3
WRITE	2nd Cycle	L	H→L	L	L	Х	n/a	COL	Data In	1, 3
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN	READ	L→H→L	L.	Н	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		[*] L	T	Н	Н	Х	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	Н	Н	X	Х	Х	High-Z	
BATTERY BACKUP REFRESH		H→L	Land	Н	Н	Х	Х	Х	High-Z	
SELF REFRESH		H→L	L	Н	Н	Х	X	Х	High-Z	

NOTE:

- 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
- 2. EARLY-WRITE only.
- 3. Data-in will be dependent on the mask provided (MT4C1M16C7 S only). Refer to Figure 4.

TRUTH TABLE: MT4C1M16C3/5 S

			. 1.1.				ADDRI	ESSES		
FUNCTION		RAS	CASL	CASH	WE	OE	t _R	¹C	DQs	NOTES
Standby		Н	H→X	H→X	Х	Х	Х	X	High-Z	
READ: WORD		. L	L	L	Н	L	ROW	COL	Data Out	
READ: LOWER	RBYTE	L	L	Н	Н	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	4 ³ ×
READ: UPPER	BYTE	L	Н	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	20 Sec.
WRITE: WORD (EARLY-WRIT		L	L	L	L	Х	ROW	COL	Data In	5
WRITE: LOWE BYTE (EARLY)		L	L	Н	L	Х	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPE BYTE (EARLY)		L	Н	L	L	Х	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	Н	L	ROW	COL	Data Out	2
READ	2nd Cycle	L	H→L	H→L	Н	L	n/a	COL	Data Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	Х	ROW	COL	Data In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L	Х	n/a	COL	Data In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	Н	L	ROW	COL	Data Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		, - L	Н	Н	: X	Х	ROW	n/a	High-Z	
CAS-BEFORE REFRESH	-RAS	H→L	L	L	Н	X	Х	Х	High-Z	4
BATTERY BAC REFRESH	CKUP	H→L	L	L	Н	Х	Х	Х	High-Z	
SELF REFRES	SH	H→L	L	L	Н	Х	Χ	Х	High-Z	

- NOTE: 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
 - 2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
 - 3. EARLY-WRITE only.
 - 4. Only one CAS must be active (CASL or CASH).
 - 3. Data-in will be dependent on the mask provided (MT4C1M16C5 S only). Refer to Figure 5.



MT4(L)C1M16CX S 1 MEG x 16 DRAM

ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:control_volume} \begin{tabular}{lll} Voltage on Vcc supply relative to Vss (5V) &-1V to +7V \\ Voltage on Vcc supply relative to Vss (3V) &-1V to +4.6V \\ Operating Temperature, T_A (Ambient) && 0°C to +70°C \\ Storage Temperature (Plastic) && .55°C to +150°C \\ Power Dissipation && 1W \\ Short Circuit Output Current && .50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 44
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	e de la deservación de la defendación del defendación de la defendación de la defendación de la defendación del defendación de la defendac	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = 2.1mA)	Vol		0.4	٧	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 43) (0°C $\leq T_A \leq 70$ °C; Vcc = 3.0/3.3V ± 10 %)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 44
Input High (Logic 1) Voltage, All Inputs	ViH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ Vcc (All other pins not under test = 0V)	l	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ 3.6V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -1.0mA)	Vон	2.4		V	
Output Low Voltage (IouT = 1.0mA)	Vol		0.4	V	

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 42) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

(Notes. 1, 3, 4, 6, 7, 42) (0°C \leq 1 _A \leq 70°C, VCC = 5V \pm 10%)			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	300	300	300	μΑ	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	170	160	140	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	lcc4	130	120	110	mA	3, 4, 44
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC (MIN))	lcc5	170	160	140	mA	3, 5, 44
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC (MIN))	lcc6	170	160	140	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = [†] RAS (MIN) to 300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), [†] RC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	400	400	400	μА	3, 42
REFRESH CURRENT: SELF Average power supply current during SELF refresh: CBR cycle with RAS ≥ tRASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	Iccs	400	400	400	μΑ	5



DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

300ns; WE, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open),

Average power supply current during SELF refresh: CBR cycle with RAS ≥ tRASS (MIN) and CAS held LOW; WE = Vcc - 0.2V; A0-A9

^tRC = 125µs (1,024 rows at 125µs = 128ms)

and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)

REFRESH CURRENT: SELF

lotes: 1, 3, 4, 6, 7, 43) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 3.0/3.3V \pm 10\%)$			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	1	1	1	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	80	80	80	μΑ	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc3	130	120	100	mA	3, 4, 44
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN); ^t CP, ^t ASC = 10ns)	lcc4	90	80	70	mA	3, 4, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: ¹RC = ¹RC (MIN))	lcc5	130	120	100	mA	3, 4, 4
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc6	130	120	100	mA	3, 4
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to	lcc7	100	100	100	μА	3, 42

Icc8

100

100 100 μΑ

5



CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cii	5	pF	2
Input Capacitance: RAS, CAS/(CASL,CASH), (WEL, WEH)/ WE, OE	C ₁₂	7	pF	2
Input/Output Capacitance: DQ	Cio	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V or 3.0/3.3V \pm 10%)

AC CHARACTERISTICS			-6		-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	1.
READ-WRITE cycle time	^t RWC	155		180		200		ns	
FAST-PAGE-MODE	^t PC	35		40		40		ns	35
READ or WRITE cycle time	ł								
FAST-PAGE-MODE	^t PRWC	85		95		100		ns	35
READ-WRITE cycle time									
Access time from RAS	†RAC		60	2.5	70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15, 33
Output Enable	^t OE		15	1	15		15	ns	33
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		35	-	40		45	ns	33
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	1.55
RAS hold time	tRSH	15		20		20		ns	40
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	39
CAS hold time	^t CSH	60		70		80		ns	32
CAS precharge time	^t CPN	10		10		10		ns	16, 36
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	36
RAS to CAS delay time	tRCD	15	45	20	50	20	60	ns	17, 31
CAS to RAS precharge time	tCRP	5		5		5		ns	32
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	^t RAD	15	30	15	35	15	40	ns	18
address delay time									7
Column address setup time	†ASC	0		0		0		ns	31
Column address hold time	^t CAH	10		15		15		ns	31
Column address hold time	tAR	50		55		60		ns	
(referenced to RAS)			1						
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26, 31
Read command hold time	tRCH	0		0		0		ns	19, 26, 32
(referenced to CAS)					1		_	ļ	
Read command hold time (referenced to RAS)	trrh	0		0		0		ns	19
CAS to output in Low-Z	^t CLZ	0		0		0		ns	33



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le +70^{\circ}C$; Vcc = 5V or $3.0/3.3V \pm 10\%$)

AC CHARACTERISTICS	-6			-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20, 29, 33
WE command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	10		15		15		ns	26, 40
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command pulse width	tWP	10		15		15		ns	26
Write command to RAS lead time	^t RWL	15		20	Spirit in	20		ns	26
Write command to CAS lead time	tCWL	15		20		20		ns	26, 32
Data-in setup time	^t DS	0		0		0		ns	22, 33
Data-in hold time	†DH	10		15		15		ns	22, 33
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Column address to WE delay time	^t AWD	55		60		65		ns	21
CAS to WE delay time	tCWD	40		45		45	· · · · · · · · · · · · · · · · · · ·	ns	21, 31
Transition time (rise or fall)	T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF.		128		128		128	ms	28
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5, 31
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5, 32
WE hold time (MASKED WRITE and CAS-BEFORE-RAS refresh)	tWRH	15		15		15		ns	26, 27
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	26
WE setup time (MASKED WRITE)	tWRS	10		10		10		ns	26, 27
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	
Output disable	^t OD	7	15		15	Visit 1	15	ns	29, 41
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	15	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	15	Feet 18	15		ns	28
Last CAS going LOW to first CAS to return HIGH	[†] CLCH	10		10		10		ns	34
Mask data to RAS setup time	tMS	0		0		0		ns	26, 27
Mask data to RAS setup time	tMH	15		15		15	1	ns	26, 27
RAS pulse width during SELF REFRESH cycle	†RASS	100		100		100		μs	46
RAS precharge time during SELF REFRESH cycle	^t RPS	150		150		150		ns	46
CAS hold time during SELF REFRESH cycle	^t CHS	-70		-70		-70		ns	46



ZEW

WIDE DRAM

NOTES

- All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = 5V or 3.0/3.3V $\pm 10\%$; f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of $100\mu s$ is required after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} -ONLY or CBR) before proper device operation is assured. The eight \overline{RAS} cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 1 TTL gate and 50pF
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD ≥ {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition (not a reference to VOH or VOL).
- 21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), ^tAWD cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to ViH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE-WRITE and READ-MODIFY-WRITE operations are not possible.
- 24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
- 25. All other inputs at Vcc -0.2V.
- 26. Write command is defined as either WEL or WEH or both going LOW on the MT4C1M16C6/7 S. Write command is defined as WE going LOW on the MT4C1M16C3/5 S.
- 27. MT4C1M16C5/7 S only.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. The DQs open during READ cycles once 'OD or 'OFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



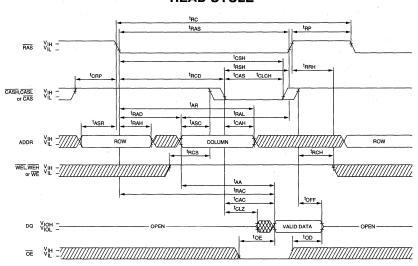
MT4(L)C1M16CX S 1 MEG x 16 DRAM

NOTES (continued)

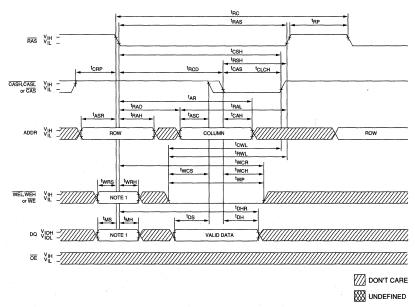
- 30. Notes 31 through 41 apply to MT4C1M16C3/5 S only (*).
- 31. *The first \overline{CASx} edge to transition LOW.
- 32. *The last \overline{CASx} edge to transition HIGH.
- *Output parameter (DQx) is referenced to corresponding CAS input; DQ1-DQ8 by CASL and DQ9-DQ16 by CASH.
- 34. *Last falling CASx edge to first rising CASx edge.
- 35. *Last rising CASx edge to next cycle's last rising CASx edge.
- 36. *Last rising \overline{CASx} edge to first falling \overline{CASx} edge.
- 37. *First DQs controlled by the first CASx to go LOW.
- 38. *Last DQs controlled by the last \overline{CASx} to go HIGH.
- 39. *Each CASx must meet minimum pulse width.

- 40. *Last CASx to go LOW.
- 41. *All DQs controlled, regardless CASL and CASH.
- 42. BBU current is reduced as tRAS is reduced from its maximum specification during BBU cycle.
- 43. The 5V version is restricted to operate between 4.5 V and 5.5V only.
- 44. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
- 45. Column address changed once while $\overline{RAS} = VIL$ and $\overline{CAS} = VIH$.
- 46. When exiting the SELF REFRESH mode, a complete set of row refreshes must be executed in order to ensure the DRAM will be fully refreshed.

READ CYCLE



EARLY-WRITE CYCLE

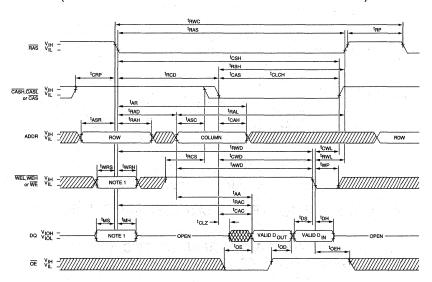


NOTE:

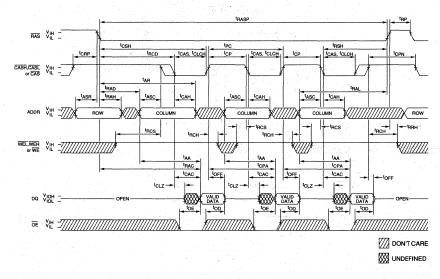
1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at RAS time.



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



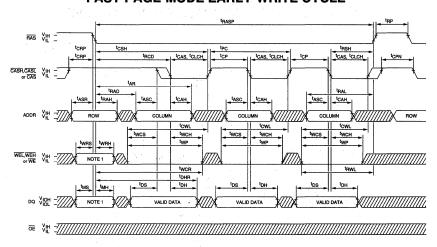
FAST-PAGE-MODE READ CYCLE



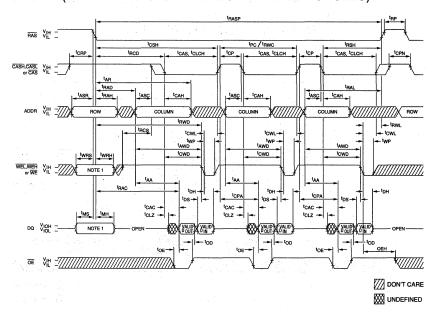
NOTE:

1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at RAS time.

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



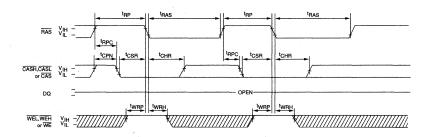
NOTE:

1. Applies to MT4C1M16C5 S and MT4C1M16C7 S only. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE (WE HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE (WE LOW at RAS time). WEL, WEH and DQ inputs on MT4C1M16C3 S and MT4C1M16C6 S are "don't care" at RAS time.



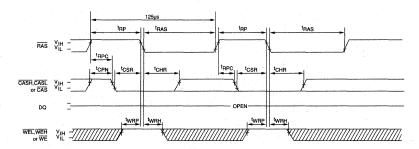
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9; and \overline{OE} = DON'T CARE)$



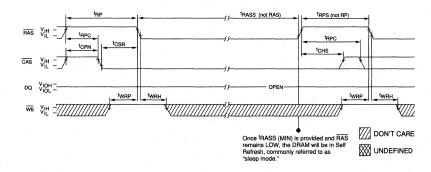
BATTERY BACKUP REFRESH CYCLE

 $(A0-A9; and \overline{OE} = DON'T CARE)$

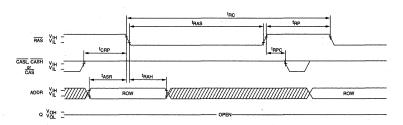


SELF REFRESH CYCLE ("SLEEP MODE")

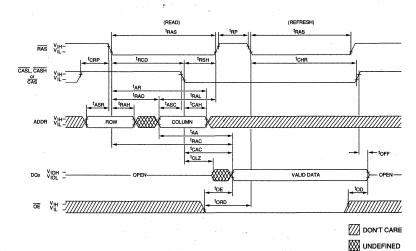
(A0-A9; and $\overline{OE} = \overline{DON'T} CARE$)



RAS-ONLY REFRESH CYCLE (ADDR = A0-A9, OE; WEL, WEH or WE = DON'T CARE)



HIDDEN REFRESH CYCLE ²⁴ (WEL, WEH or WE = HIGH; OE = LOW)



MICHON

DYNAMIC RAMS	
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9



DRAM MODULE PRODUCT SELECTION GUIDE

Memory	Part	Optional	Access	Power D	issipation		kage]
Configuration	Number	Access Cycle	Time (ns)	Standby	Active	SIMM	SIP	Page
256K x 8	MT2D2568	LP, LV*	60, 70, 80	6mW	350mW	30	30	3-1
1 Meg x 8	MT2D18	LP, LV*	60, 70, 80	6mW	450mW	30	30	3-11
1 Meg x 8	MT8D18	LP	60, 70, 80	24mW	1,400mW	30	30	3-21
4 Meg x 8	MT2D48		60, 70, 80	10mW	550mW	30	30	3-31
4 Meg x 8	MT8D48	LP	60, 70, 80	24mW	1,800mW	30	30	3-41
16 Meg x 8	MT8D168		60, 70, 80	24mW	2,200mW	30	30	3-51
256K x 9	MT3D2569	LP	60, 70, 80	9mW	625mW	30	30	3-61
1 Meg x 9	MT3D19	LP	60, 70, 80	9mW	625mW	30	30	3-71
1 Meg x 9	MT9D19	LP	60, 70, 80	27mW	1,575mW	30	30	3-81
4 Meg x 9	MT3D49		60, 70, 80	12mW	775mW	30	30	3-91
4 Meg x 9	MT9D49	LP	60, 70, 80	27mW	2,025mW	30	30	3-101
16 Meg x 9	MT9D169		60, 70, 80	27mW	2,475mW	30	30	3-111
512K x 16	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
1 Meg x 16	MT16D51232	LP, LV*	60, 70, 80	48mW	2,800mW	72	-	3-133
2 Meg x 16	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
4 Meg x 16	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
8 Meg x 16	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
16 Meg x 16	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
512K x 18	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
1 Meg x 18	MT6D118		60, 70, 80	18mW	1,250mW	72	-	3-209
1 Meg x 18	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
2 Meg x 18	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
4 Meg x 18	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
8 Meg x 18	MT12D436		60, 70, 80	52mW	3,100mW	72	-	3-283
16 Meg x 18	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 32	MT8D25632	LP, LV*	60, 70, 80	24mW	1,400mW	72	-	3-121
512K x 32	MT16D51232	LP, LV*	60, 70, 80	48mW	1,424mW	72	-	3-133
1 Meg x 32	MT8D132	LP, LV*	60, 70, 80	24mW	1,800mW	72	-	3-145
2 Meg x 32	MT16D232	LP, LV*	60, 70, 80	48mW	1,824mW	72	-	3-157
4 Meg x 32	MT8D432		60, 70, 80	40mW	2,200mW	72	-	3-169
8 Meg x 32	MT16D832		60, 70, 80	80mW	2,240mW	72	-	3-179
256K x 36	MT9D25636	1	60, 70, 80	27mW	1,575mW	72		3-189
256K x 36	MT10D25636		60, 70, 80	30mW	1,750mW	72	-	3-199
512K x 36	MT18D51236		60, 70, 80	54mW	1,600mW	72	-	3-219
512K x 36	MT20D51236		60, 70, 80	60mW	1,780mW	72	-	3-229
1 Meg x 36	MT9D136		60, 70, 80	27mW	2,175mW	72	-	3-239
1 Meg x 36	MT12D136	LP	60, 70, 80	36mW	2,500mW	72	-	3-249
2 Meg x 36	MT18D236		60, 70, 80	54mW	2,052mW	72		3-261
2 Meg x 36	MT24D236	LP	60, 70, 80	72mW	2,536mW	72	-	3-271
4 Meg x 36	MT12D436	10 · 10 · 10 · 10 · 10 · 10 · 10 · 10 ·	60, 70, 80	52mW	3,100mW	72	-	3-283
8 Meg x 36	MT24D836		60, 70, 80	104mW	3,152mW	72	-	3-293
256K x 40	MT10D25640	LP, LV*	60, 70, 80	30mW	1,750mW	72	-	3-303
512K x 40	MT20D51240	LP, LV*	60, 70, 80	60mW	1,780mW	72	-	3-315
1 Meg x 40	MT10D140	LP, LV*	60, 70, 80	30mW	2,250mW	72	-	3-327
2 Meg x 40	MT20D240	LP, LV*	60, 70, 80	60mW	2,280mW	72	-	3-339

LP = Low Power, Extended Refresh; LV = Low Voltage NOTE: All modules include FAST PAGE MODE cycle.



DRAM MODULE

256K x 8 DRAM

FAST PAGE MODE (MT2D2568) LOW POWER, EXTENDED REFRESH (MT2D2568 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW (.6mW L-version) standby; 350mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 400μA maximum (L-version)

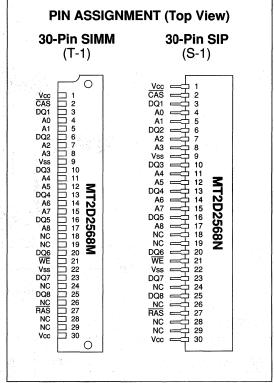
OPTIONS	MARKIN
• Timing 60ns access	- 6
70ns access	- 7
80ns access	- 8
 Packages Leadless 30-pin SIMM Leaded 30-pin SIP 	M N
 Power/Refresh Normal Power/8ms Low Power/64ms 	Blank L

• Part Number Example: MT2D2568ML-6

GENERAL DESCRIPTION

The MT2D2568 is a randomly accessed solid-state memory containing 262,144 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY-WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, and the output pins remain open (High-Z) until the next \overline{CAS} cycle.

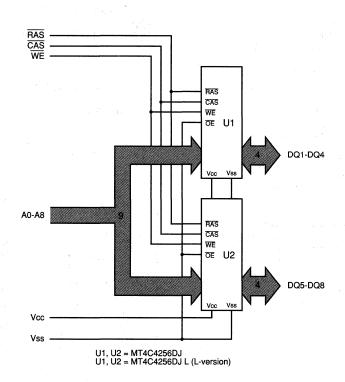
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8)



defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} or HIDDEN REFRESH) so that all 512 combinations of \overline{RAS} addresses (A0-A8) are executed at least every 8ms, (64ms on L-version) regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

					:		ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	ιC	DQ1-DQ8		
Standby		Н	H→X	Х	Х	X	High-Z		
READ		L	L	Н	ROW	COL	Data Out		
EARLY-WRITE		75 L	L	L	ROW	COL	Data In		
FAST-PAGE-MODE	1st Cycle	L i	H→L	Н	ROW	COL	Data Out		
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out		
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In		
WRITE	2nd Cycle		H→L	L	n/a	COL	Data In		
RAS-ONLY REFRESH		L	Н	X	ROW	n/a	High-Z		
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out		
REFRESH	WRITE	L→H→L	L	Ł	ROW	COL	Data In		
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	High-Z		
BATTERY BACKUP		H→L	L	X	Х	X X	High-Z		
REFRESH (L-version)				la de la la	with the	e ad the co	1964 our bar De Ger		



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)0°C to +70°C
Storage Temperature	
Power Dissipation	2W
Short Circuit Output Current	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	The state of the s	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1	0.8	V	1.
INPUT LEAKAGE Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	A0-A8, RAS, CAS, WE	li a	-4	4	μА	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ Vouт ≤ Vcc)	DQ1-DQ8	loz	-10	10	μА	
OUTPUT LEVELS Output High (Logic 1) Voltage (Iout = -5mA)		Vон	2.4		٧	
Output Low (Logic 0) Voltage (IOUT = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	4	4	4	mA	
STANDBY CURRENT: (CMOS)	lcc2	2	2	2	mA	23
$\overline{(RAS)} = \overline{CAS} = Vcc -0.2V$.4	.4	.4	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current	lссз	180	160	140	mA	2, 22
(RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	1 . A. (1984)	170	150	130	mA	2,22,25
OPERATING CURRENT: FAST PAGE MODE Average power supply current	lcc4	140	120	100	mA	2, 22
(RAS = V _I L, CAS, Address Cycling: ^t PC = ^t PC (MIN))		130	110	90	mA	2,22,25
REFRESH CURRENT: RAS-ONLY Average power supply current	lcc5	180	160	140	mA	2
(RAS Cycling, CAS = Vih: tRC = tRC (MIN))		170	150	130	mA	2, 25
REFRESH CURRENT: CAS-BEFORE-RAS		180	160	140	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	170	150	130	mA	2,19,25
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = †RAS (MIN) to 1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), †RC = 125µs (512 rows at 125µs = 64ms)	lcc7	.4	.4	.4	mA	25



CAPACITANCE

PARAMETER	Č.	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8		Cit		13	pF	17
Input Capacitance: RAS, CAS, WE		Cı2		17	pF	17
Input/Output Capacitance: DQ1-DQ8		Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0^{\circ}C \le T_{A} \le +70^{\circ}C$; $Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a	1 11	n/a		n/a	21
FAST-PAGE-MODE READ or WRITE	^t PC	40		40		40		ns	
cycle time		1.0							
FAST-PAGE-MODE READ-WRITE	^t PRWC	n/a		n/a		n/a		n/a	21
cycle time									
Access time from RAS	tRAC		60		70		80	ns	8
Access time from CAS	tCAC		20		20		20	ns	9
Output Enable	^t OE		20		20		20	ns	
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	tCPA .		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	.13
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0	14.30	0	1.1	0		ns	111
Row address hold time	†RAH	10	- 3.7	10		10		ns	
RAS to column	†RAD	15	30	15	35	15	40	ns	24
address delay time									
Column address setup time	tASC	0		0		0		ns	
Column address hold time	[†] CAH	15		15	17 . 19	15		ns	
Column address hold time	tAR take	45		55		60		ns	
(referenced to RAS)									
Column address to	^t RAL	30		35		40		ns	
RAS lead time						31 1 4			
Read command setup time	†RCS	0		0		0		ns	last in the
Read command hold time	†RCH	0		0	9.00	0		ns	14
(referenced to CAS)	a parameter ega				145,000	E SON	Leaf Mary		
Read command hold time	^t RRH	0		0		0	1	ns	14
(referenced to RAS)		1.7 g/h()			14.00	2 9 1 3	10/43		
CAS to output in Low-Z	tCLZ	0	tran da l	0	Harry Commercial	0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6 -7 -8		3					
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	^t WP	10		15		15		ns	
Write command to RAS lead time	^t RWL	20		20		20		ns	
Write command to CAS lead time	^t CWL	20		20		20	1.59	ns	
Data-in setup time	t _{DS}	0		0		0		ns	15
Data-in hold time	^t DH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	[†] DHR	45		55		60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^t REF		8/64		8/64		8/64	ms	3/25
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10	1 (1) (5) (1)	10		10		ns	19
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	10		15		15		ns	19

NOTES

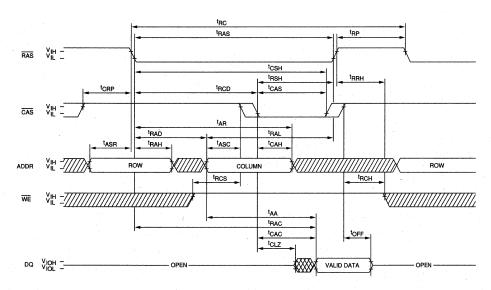
- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 4. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- Measured with a load equivalent to two TTL gates
- AC characteristics assume 1 5...
 VIH (MIN) and VIL (MAX) are referent measuring timing of input signals. Trans are measured between VIH and VIL.
 The minimum specifications are used cycle time at which proper operation temperature range (0°C ≤ T_A ≤ 70°C)
 Measured with a load equivalent to tand 100pF.
 Assumes that [†]RCD < [†]RCD (MAX). I than the maximum recommended vatable, [†]RAC will increase by the amore exceeds the value shown.
 Assumes that [†]RCD ≥ [†]RCD (MAX).
 If CAS = VIH, data output is High-Z. 8. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD

 - 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
 - 11. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
 - 12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
 - 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

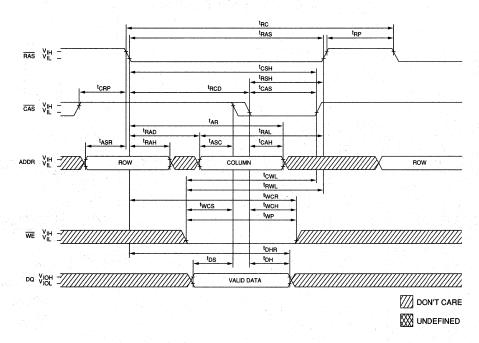
- a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to \overline{CAS} leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCP.
- On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1 and U2.
- 22. Icc is dependent on cycle rates.
- 23. All other inputs at Vcc -0.2V.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Applies to L-version only.



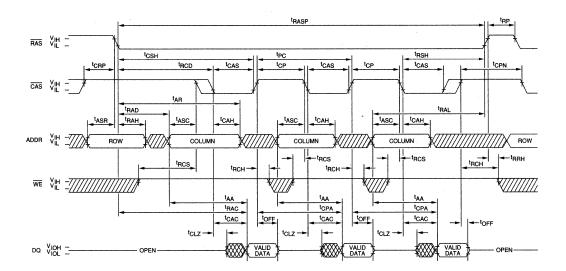
READ CYCLE



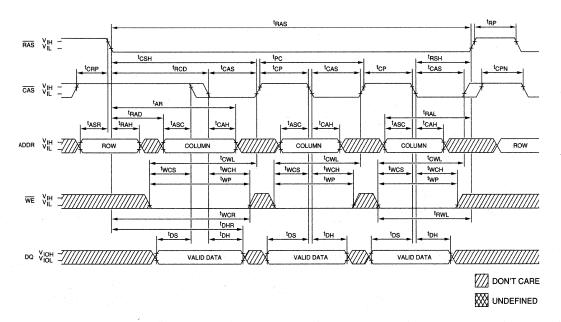
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

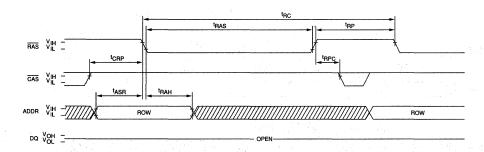


FAST-PAGE-MODE EARLY-WRITE CYCLE



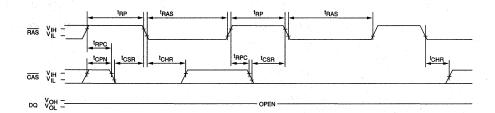


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



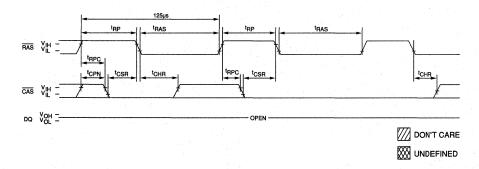
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8 and WE = DON'T CARE)

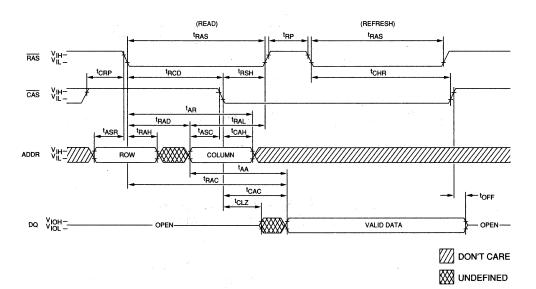


BATTERY BACKUP REFRESH CYCLE 25

 $(A0-A8 \text{ and } \overline{WE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 20 (WE = HIGH)







DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE (MT2D18) LOW POWER, EXTENDED REFRESH (MT2D18 L)

FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW (2mW L-version) standby; 450mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- Low CMOS standby current, 400μA maximum (L-version)

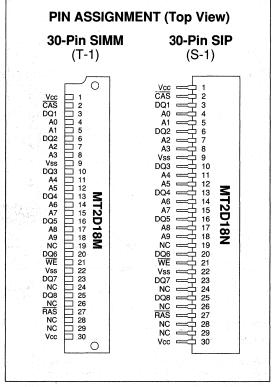
OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
 Power/Refresh 	
Normal power/16ms	Blank
Low power/128ms	

GENERAL DESCRIPTION

• Part Number Example: MT2D18ML-6

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. Early WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, and the output pins remain open (High-Z) until the next \overline{CAS} cycle.

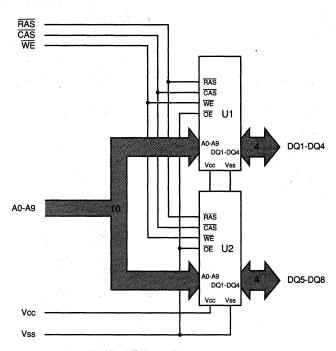
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A9)



defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} or HIDDEN REFRESH) so that all 1,024 combinations of \overline{RAS} addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4001JDJ U1, U2 = MT4C4001JDJ L (L-version)

TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC	DQ1-DQ8
Standby		н	H→X	Х	Χ	Х	High-Z
READ	t was on	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	· · · E	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	r sje L jij	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	24 H 14	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	all L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	X	X	. • X	High-Z



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & --1V to +7V \\ Operating Temperature, T_A (Ambient) & --0°C to +70°C \\ Storage Temperature & -55°C to +125°C \\ Power Dissipation & 2W \\ Short Circuit Output Current & 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0° C $\leq T_A \leq 70^{\circ}$ C; Vcc = 5V $\pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Viн	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	A0-A9, RAS, CAS, WE	li	-4	4	μА	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ Vouт ≤ Vcc)	DQ1-DQ8	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High (Logic 1) Voltage (IouT = -5mA) Output Low (Logic 0) Voltage (IouT = 5mA)		Vol		0.4	V	

			MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{IH})$	lcc1	4	4	4	mA		
STANDBY CURRENT: (CMOS)	lcc2	2	2	2	mA	25	
$\overline{(RAS)} = \overline{CAS} = Other Inputs = Vcc -0.2V$.4	.4	.4	mA	25	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	220	200	180	mA	2, 26	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	160	140	120	mA	2, 26	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	220	200	180	mA	2	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	220	200	180	mA	2, 19	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ^t RAS (MIN) to 300ns; WE = Vcc -0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), ^t RC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	.6	.6	.6	μΑ	27, 28	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Ci1		13	рF	17
Input Capacitance: RAS, CAS, WE	Ci2		17	рF	17
Input/Output Capacitance: DQ1-DQ8	Сю		10	рF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE	^t PC	40		40		45		ns	
cycle time								-	
FAST-PAGE-MODE READ-WRITE	^t PRWC	n/a		n/a		n/a		n/a	21
cycle time		1.					1		
Access time from RAS	^t RAC		60		70		80	ns	8
Access time from CAS	[†] CAC		15		20		20	ns	9
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	- 20	60	ns	13
CAS to RAS precharge time	tCRP	10		10		10	-	ns	
Row address setup time	tASR	0	,	0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	^t RAD	15	30	15	35	15	40	ns	22
address delay time				1.0					
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time	tAR	50		55		60		ns	
(referenced to RAS)									
Column address to	tRAL.	30		35		40	1111	ns	
RAS lead time			1						
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	^t RCH	0		0		0		ns	24
(referenced to CAS)	programme to				1	1.5%			
Read command hold time	^t RRH	0		0		0		ns	24
(referenced to RAS)					L 22		11/1		1
CAS to output in Low-Z	tCLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS	SYM	-6		-7		-8			
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15	2	ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	11.
Data-in setup time	tDS	0		0	1	0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	^t REF		16/128		16/128		16/128	ms	3/28
RAS to CAS precharge time	tRPC	2 0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	23
WE setup time (CAS-BEFORE-RAS refresh)	†WRP	10		10		10	See god.	ns	23
WE hold time (WCBR test cycle)	^t WTH	10		10		10		ns	23
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	23

DRAM MODULE

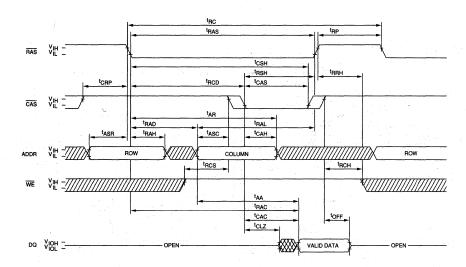
NOTES

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 4. AC characteristics assume ${}^{t}T = 5$ ns.
 - VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
 - The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. Measured with a load equivalent to 2 TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If \overline{CAS} = VIH, data output is High-Z.
- 11. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. ${}^{t}RCH$ is referenced to the first rising edge of \overline{RAS} or \overline{CAS} .

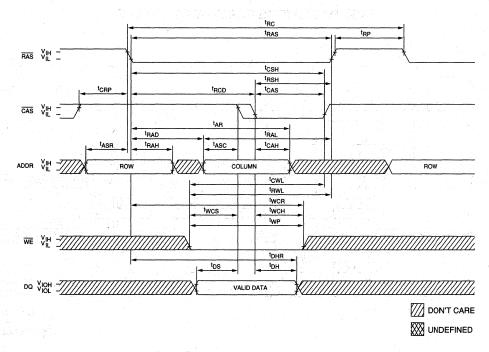
- 15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{\text{OE}}$ being grounded on U1 and U2.
- 22. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 23. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 24. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 25. All other inputs at Vcc -0.2V.
- 26. Icc is dependent on cycle rates.
- 27. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.
- 28. Applies to L-version only.



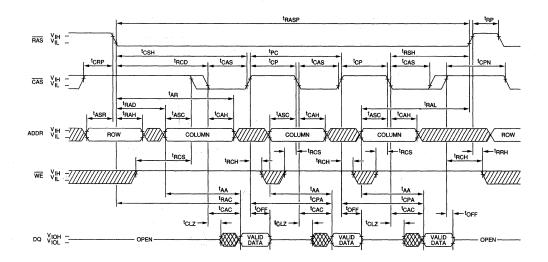
READ CYCLE



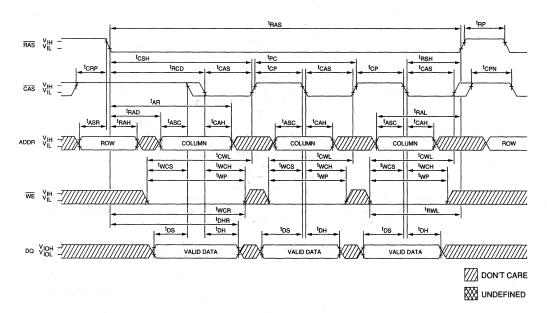
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

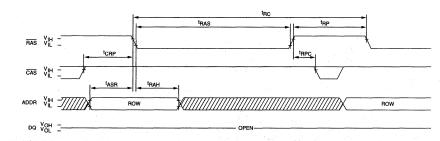


FAST-PAGE-MODE EARLY-WRITE CYCLE

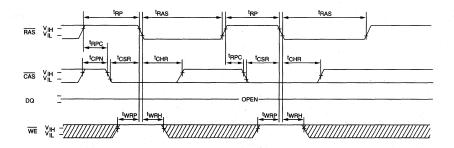




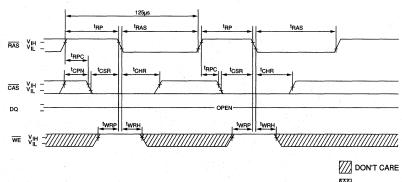
RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



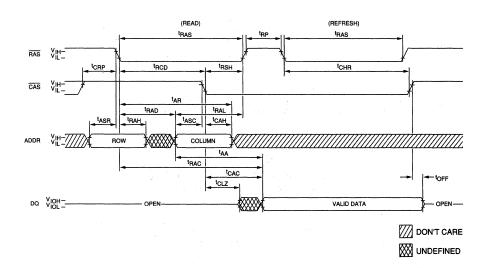
CAS-BEFORE-RAS REFRESH CYCLE (A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE ²⁸ (A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

1 MEG x 8 DRAM

FAST PAGE MODE (MT8D18) LOW POWER, EXTENDED REFRESH (MT8D18 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- · High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 24mW (2.4mW L-version) standby; 1,400mW active, typical
- · All device pins are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or
 512-cycle extended refresh distributed across 64ms
- · FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

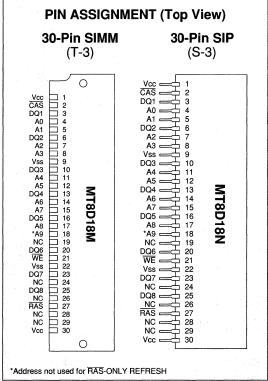
MARKING					

Part Number Example: MT8D18ML-6

GENERAL DESCRIPTION

The MT8D18 is a randomly accessed solid-state memory ontaining 1,048,576 words organized in a x8 configuration. Furing READ or WRITE cycles, each word is uniquely ddressed through the 20 address bits, which are entered 10 its (A0-A9) at a time. $\overline{\text{RAS}}$ is used to latch the first 10 bits nd $\overline{\text{CAS}}$ the latter 10 bits. READ or WRITE cycles are elected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates EAD mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE cycle, data-in (D) is latched by the Illing edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Early /RITE occurs when $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going OW, and the output pins remain open (High-Z) until the ext $\overline{\text{CAS}}$ cycle.

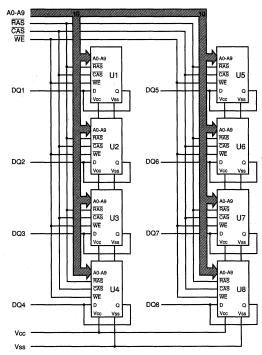
FAST PAGE MODE operations allow faster data operaons (READ or WRITE) within a row-address (A0-A9)



defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycles (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version only), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ U1 - U8 = MT4C1024DJ L (L-version)

TRUTH TABLE

	1			2	ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	τC	DQ1-DQ8
Standby		Н	H→X	Х	X	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	tan L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	es a Ling	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	i V <u>L</u>	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	e.∛e.j L	L. L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Χ	High-Z
BATTERY BACKUP		H→L _g et	L	X , .	Х	X ,	High-Z
REFRESH (L-version)		ALTERNATION OF THE				5 1 1997	



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1V to +7V \\ Operating Temperature, T_A (Ambient) & 0°C to +70°C \\ Storage Temperature (Plastic) & ... -55°C to +125°C \\ Power Dissipation & ... 8W \\ Short Circuit Output Current & ... 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		V _I H 2.4 V _{CC+1} V 1 V _I L -1.0 0.8 V 1 V _S S I _I -2 2 μA RAS, WE I _I -16 16 μA				1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE: Any Input 0V ≤ Vin ≤ Vcc,	D9, CAS9	lı lı	-2	2	μА	
(All other pins not under test = 0V)	A0-A9, RAS, WE	lı .	-16	16	μА	
OUTPUT LEAKAGE: (Q is disabled, 0V ≤ Vouт ≤ Vcc)	DQ1-8, Q9	loz	-10	10	μА	
OUTPUT LEVELS Output HighVoltage (lout = -5mA)		Vон	2.4		٧	
Output Low Voltage (IOUT = 5mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	16	16	16	mA	
STANDBY CURRENT: (CMOS)	lcc2	8	8	8	mA	23
$\overline{(RAS)} = \overline{CAS} = Vcc - 0.2V$		1.6	1.6	1.6	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current	Іссз	720	640	560	mA	3, 4
(RAS, CAS, Address Cycling: 'RC = 'RC (MIN)) OPERATING CURRENT: FAST PAGE MODE		560	480	520 400	mA mA	3, 4, 25
Average power supply current (RAS = VIL; CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	520	440	360	mA	3, 4, 25
REFRESH CURRENT: RAS-ONLY Average power supply current	lcc5	720	640	560	mA	3
(RAS Cycling; CAS = Vih: ^t RC = ^t RC (MIN))	1005	680	600	520	mA	3, 25
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current	Icc6	720	640	560	mA	3, 5
(RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	1000	680	600	520	mA	3, 5, 25
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ¹RAS (MIN) to 1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left	lcc7	1.6	1.6	1.6	mA	25
OPEN), ^t RC = 125μs (512 rows at 125μs = 64ms)						



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Ci1		51	pF	2
Input Capacitance: RAS, CAS, WE	Cı2		67	pF	2
Input/Output Capacitance: DQ1-DQ8	Cıo		16	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	†RWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		ns			
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		n/a	24
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		20		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns.	
Access time from CAS precharge	[†] CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	60.	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0.		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	tAR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40	and the control of th	ns	
Read command setup time	†RCS	0	1	0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq 75$ °C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6	3		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	^t CLZ	0		0		0		ns	3 T 3 H
Output buffer turn-off delay	¹OFF	0	20	0	20	0	20	ns	20
WE command setup time	twcs	0 0		0		0		ns	et sylv
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP.	10		15		15		ns	31. T.
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH	15		15		15	1 1 1 1	ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60	s in stars	ns	
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	†REF		8/64		8/64		8/64	ms	7/25
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	10		15		15		ns	5

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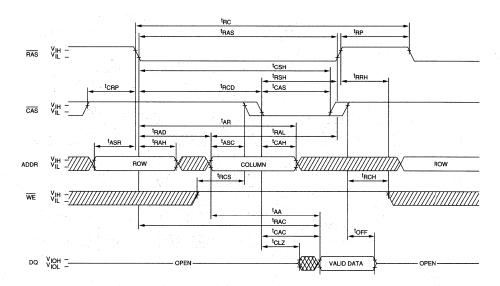
NOTES

- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this

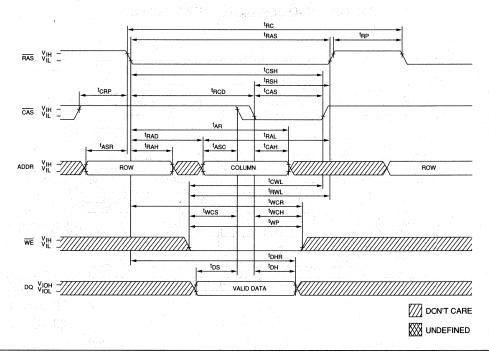
- table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 23. All other inputs equal Vcc -0.2V.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- 25. Applies to the L-version only.



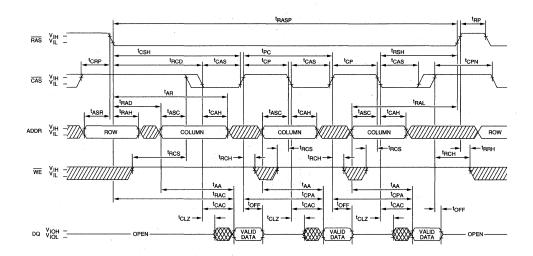
READ CYCLE



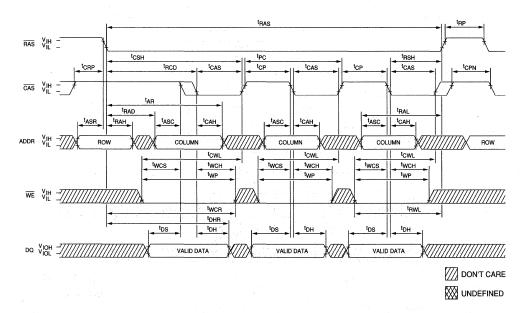
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



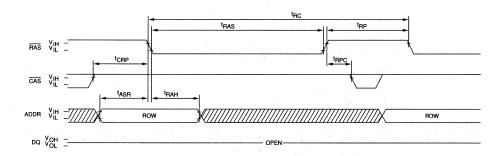
FAST-PAGE-MODE EARLY-WRITE CYCLE





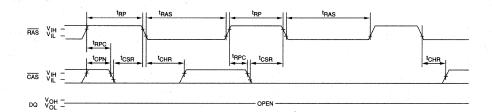
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and \overline{WE} = DON'T CARE)



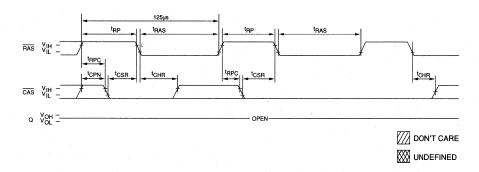
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 and $\overline{WE} = DON'T CARE$)

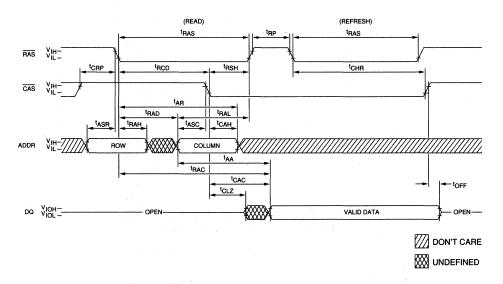


BATTERY BACKUP REFRESH CYCLE 25

(A0-A9 and $\overline{WE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 22 (WE = HIGH)





DRAM MODULE

4 MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 550mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

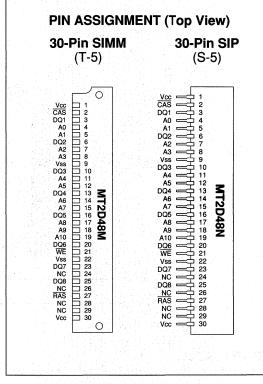
MARKING
- 6
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• Part Number Example: MT2D48M-6

GENERAL DESCRIPTION

The MT2D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next \overline{CAS} cycle.

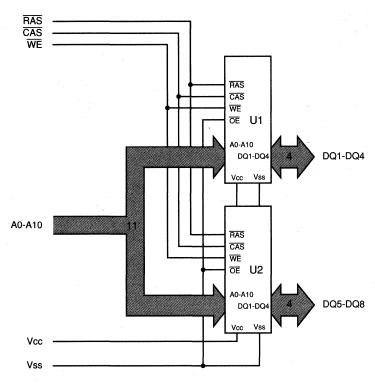
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS



followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST-PAGE-MODE operations.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



U1, U2 = MT4C4M4B1DJ

TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	^t C	DQ1-DQ8
Standby	and the second s	Н	H→X	Х	Χ	Х	High-Z
READ		L	· . L	Н , , ,	ROW	COL	Data Out
EARLY-WRITE		L V	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	. H	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L age	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH	1 20 2	L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss-1V to +7V Operating Temperature, TA (Ambient)0°C to +70°C Storage Temperature-55°C to +125°C Power Dissipation2W Short Circuit Output Current50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	٧	1
INPUT LEAKAGE Any Input 0V ≤ Vin ≤ Vcc (All other pins not under test = 0V)	-A10, RAS, CAS, WE	li	-4	4	μА	
OUTPUT LEAKAGE DC (Q is disabled, 0V ≤ Vouт ≤ Vcc)	11-DQ8	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High (Logic 1) Voltage (IouT = -5mA) Output Low (Logic 0) Voltage (IouT = 5mA)		Vol		0.4	V	

		12.5				
그렇게 하시다 아들이 있다면서 그리는 사람들에 되었다.			MAX	gari		
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	4	4	4	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc3	240	200	180	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL; CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	160	140	120	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling; CAS = Vin: tRC = tRC (MIN))	Icc5	240	200	180	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	240	200	180	mA	,3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	Cıı		13	pF	2
Input Capacitance: RAS, CAS, WE	Cı2		17	pF	2
Input/Output Capacitance: DQ1-DQ8	Сю		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE	^t PC	40		40		45		ns	
READ or WRITE cycle time			İ						
FAST-PAGE-MODE	†PRWC	n/a		n/a		n/a		ns	22
READ-WRITE cycle time								2.0	
Access time from RAS	tRAC	1.5	60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP:	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	1.
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP.	. 5		5		5		ns	11.14
Row address setup time	^t ASR	0		0	1 1	0		ns	
Row address hold time	^t RAH	10		10		10	100	ns	
RAS to column	tRAD .	15	30	15	35	. 15	40	ns	18
address delay time	: 11							4	
Column address setup time	tASC	0		0		0	1 1 1	ns	
Column address hold time	^t CAH	10		15		15	1000	ns	11.00
Column address hold time	^t AR	50		55		60	1.0	ns	esti care
(referenced to RAS)					46.5246		1 1 7 4 4		
Column address to	†RAL	30		35		40		ns	
RAS lead time									
Read command setup time	tRCS	0		0	71	0	la de la companya de	ns	2.5
Read command hold time	tRCH	. 0		0		0	A Property Company	ns	19
(referenced to CAS)									
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	†CLZ	0		0		0		ns	
Output buffer turn-off delay	¹OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

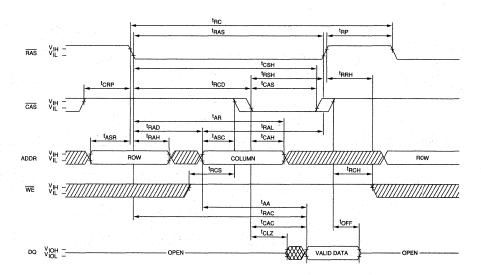
						<u> </u>			
AC CHARACTERISTICS			6		-7	1.1	-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20	174 T. Tes	20		ns	1000
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	t _{DS}	0		0	1 1	0		ns	21
Data-in hold time	tDH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	†REF		32		32		32	ms	
RAS to CAS precharge time	tRPC	0		0	1 1 1 1 1 1 1	0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	tWTH	10		10		10	- 19-20 S	ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24

NOTES

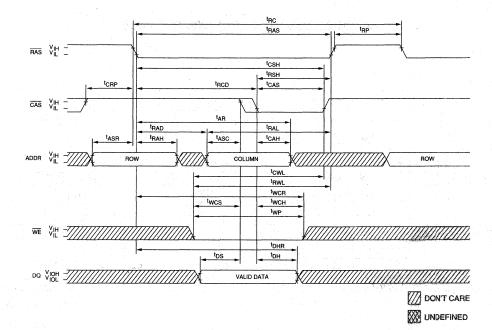
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{\rm IL}$ and $V_{\rm IL}$ (or between $V_{\rm IL}$ and $V_{\rm IH}$) in a monotonic manner.
- 11. If $\overline{CAS} = VIH$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this

- table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- OE is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE=HIGH.
- 24. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.

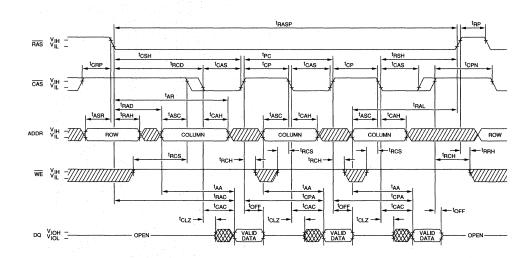
READ CYCLE



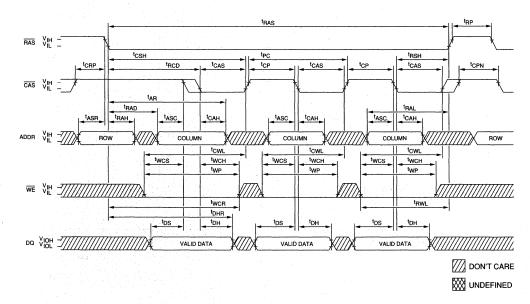
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

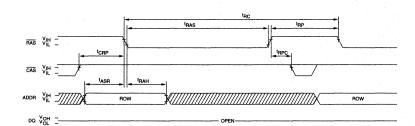


FAST-PAGE-MODE EARLY-WRITE CYCLE



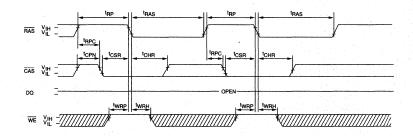


RAS-ONLY REFRESH CYCLE (ADDR = A0-A10; WE = DON'T CARE)

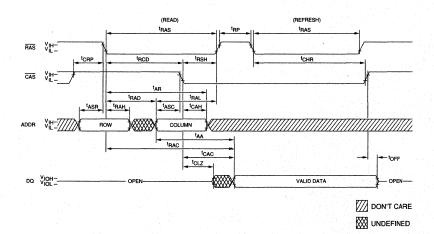


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE ²³ (WE = HIGH)





DRAM **MODULE**

4 MEG x 8 DRAM

FAST PAGE MODE (MT8D48) LOW POWER, EXTENDED REFRESH (MT8D48 L)

FEATURES

DTTONIC

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (8mW L-version) standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms FAST PAGE MODE access cycle

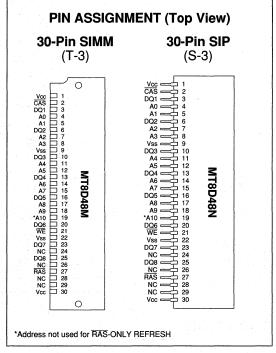
Low CMOS standby current, 1.6mA maximum (L-version)

PHONS	MAKKING
Timing	
60ns access	- 6
70ns access	-7
80ns access	-8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	Line in

Part Number Example: MT8D48ML-6

GENERAL DESCRIPTION

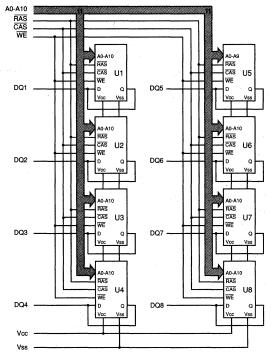
The MT8D48 is a randomly accessed solid-state memory ontaining 4,194,304 words organized in a x8 configuration. buring READ or WRITE cycles, each bit is uniquely adressed through the 22 address bits which are entered 11 its (A0-A10) at a time. RAS is used to latch the first 11 bits nd CAS the latter 11 bits. A READ or WRITE cycle is elected with the WE input. A logic HIGH on WE dictates EAD mode, while a logic LOW on WE dictates WRITE node. During a WRITE cycle, data-in (D) is latched by the ılling edge of WE or CAS, whichever occurs last. If WE oes LOW prior to CAS going LOW, the output pin(s) emain open (High-Z) until the next CAS cycle. EARLY-/RITE occurs when WE goes LOW prior to CAS going OW, and the ouput remains open (High-Z) until the next AS cycle.



FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C1004JDJ U1-U8 = MT4C1004JDJ L (L-version)

TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC	DQ1-DQ8
Standby		Н	H→X	Х	Х	X	High-Z
READ		L	L	н	ROW	COL	Data Out
EARLY-WRITE	san talah	L	alaa L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Ban H and	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	S Late III	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L.	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	133. L 201	X	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	8W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$) A0-A10, WE, CAS, RAS		-16	16	μА	
OUTPUT LEAKAGE CURRENT DQ1-DQ8 (Q is disabled, $0V \le Vout \le 5.5V$)	loz	-10	10	μА	
OUTPUT LEVELS	Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 4.2mA)	VoL		0.4	V	1

		MAX					
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	Icc1	16	16	16	mA		
STANDBY CURRENT: (CMOS)	lcc2	8	8	8	mA	23	
$\overline{(RAS} = \overline{CAS} = Vcc - 0.2V)$		1.6	1.6	1.6	mA	23, 26	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	880	800	720	mA	3, 4	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ¹PC = ¹PC (MIN))	lcc4	640	560	480	mA	3, 4	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	880	800	720	mA	3	
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	880	800	720	mA	3, 5	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ¹RAS (MIN) to 300ns; WE = Vcc -0.2V, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), ¹RC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	2.4	2.4	2.4	mA	26	



CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	Cıı	51	pF	2
Input Capacitance: RAS, WE	Cı2	67	pF	2
Input/Output Capacitance: DQ1-DQ8	Cio	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS	1000		6		-7		-8	1 1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	†RWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ	^t PC	40		40		45		ns	
or WRITE cycle time			,						
FAST-PAGE-MODE READ-WRITE	^t PRWC	n/a	1, 17	n/a	1	n/a		n/a	24
cycle time									
Access time from RAS	^t RAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	·
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20	<u> </u>	ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80	<u> </u>	ns	
CAS precharge time	^t CPN	10		10		10	1	ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		. 10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10	-	10		10		ns	
RAS to column	†RAD	15	30	15	35	15	40	ns	18
address delay time	Contract								
Column address setup time	†ASC	0		0		0	T	ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time	tAR .	50		55		60		ns	
(referenced to RAS)									
Column address to	†RAL	30		35		40		ns	
RAS lead time					18.44				
Read command setup time	tRCS	0		0	The second	0		ns	3
Read command hold time	^t RCH	0		0		0		ns	19
(referenced to CAS)				1.1		en la la	de Disert		
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)									in King kan sa
CAS to output in Low-Z	†CLZ	0	regard of	0		0	13166	ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0	1	0	1,000	0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		43.00	-6		-7	-8	3		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	^t RWL	15		20		20		ns	
Write command to CAS lead time	tCWL	20		20	1000	20		ns	
Data-in setup time	^t DS	0	* * * * * * *	0	1. 1. 1.	0		ns	21
Data-in hold time	tDH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF.		16/128		16/128	100	16/128	ms	7/26
RAS to CAS precharge time	^t RPC	0		0		0		ns	1 1 1 1 1 1
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	15		15		15		ns	5
WE setup time (CAS-BEFORE-RAS REFRESH)	^t WRP	10		10		10		ns	25
WE hold time (CAS-BEFORE-RAS REFRESH)	^t WRH	10		10		10	2/3) . 3	ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	25



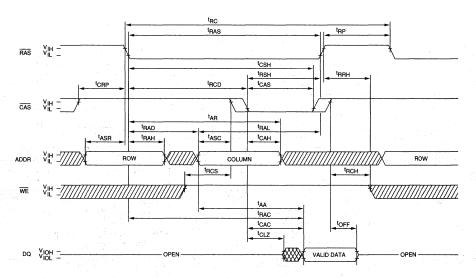
NOTES

- All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

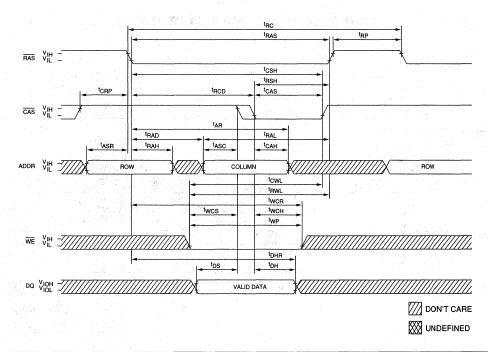
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if 'RAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 23. All other inputs equal Vcc -0.2V.
- 24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- 25. tWTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. Applies to L-version only.

DRAM MODULE

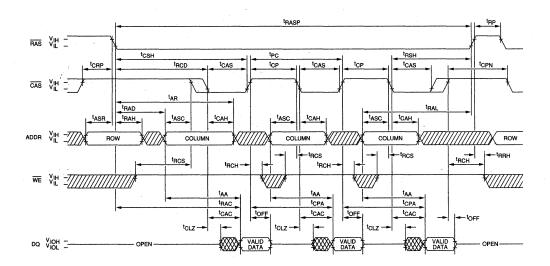
READ CYCLE



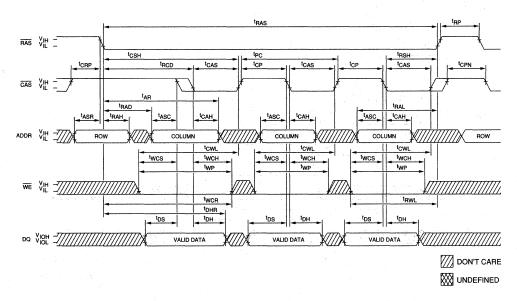
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



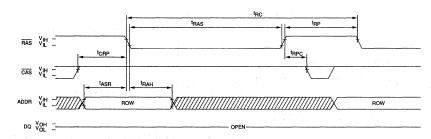
FAST-PAGE-MODE EARLY-WRITE CYCLE





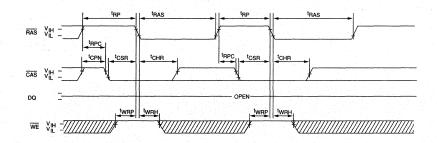
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; A10 and WE = DON'T CARE)



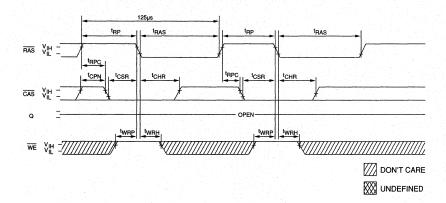
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)

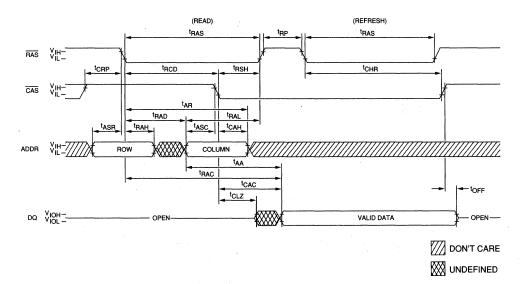


BATTERY BACKUP REFRESH CYCLE 26

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 22 (WE = HIGH)





DRAM MODULE

16 MEG x 8 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- · High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- · All device pins are fully TTL compatible
- Low power, 24mW standby; 2,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms
- FAST PAGE MODE access cycle

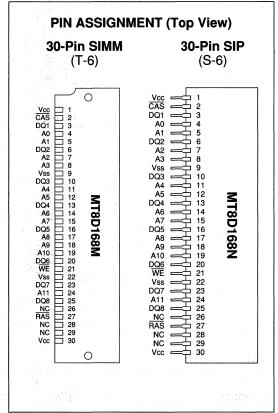
OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	\mathbf{N}

Part Number Example: MT8D168M-6

GENERAL DESCRIPTION

The MT8D168 is a randomly accessed solid-state memry containing 16,777,216 words organized in a x8 configuation. During READ or WRITE cycles, each bit is uniquely ddressed through the 24 address bits which are entered 12 its (A0-A11) at a time. \overline{RAS} is used to latch the first 12 bits nd \overline{CAS} the latter 12 bits. READ or WRITE cycles are elected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates EAD mode, while a logic LOW on \overline{WE} dictates WRITE rode. During a WRITE cycle, data-in (D) is latched by the alling edge of \overline{CAS} . Since \overline{WE} goes LOW prior to \overline{CAS} going OW, the output pin(s) remain open (High-Z) until the ext \overline{CAS} cycle.

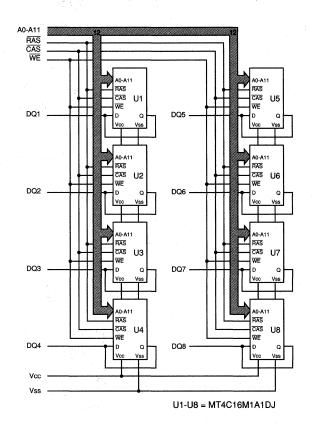
FAST PAGE MODE allows faster data operations (READ r WRITE) within a row-address (A0-A11) defined page oundary. The FAST PAGE MODE cycle is always initiated rith a row address strobed-in by RAS followed by a colmn address strobed-in by CAS. CAS may be toggled-in by



holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS, or HIDDEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

					ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC t	DQ1-DQ8
Standby		Н	H→X	Х	Х	Х	High-Z
READ	ed de que	L.	L	Н	ROW	COL	Data Out
EARLY-WRITE	14 may 1 m 1 m	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L L	Н	Х	Х	High-Z



MT8D168 16 MEG x 8 DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	A0-A11, WE, CAS, RAS		-16	16	μА	411.11.11 1
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	DQ1-DQ8	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (lout = -5mA)		Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)		Vol		0.4	V	A Delian Joseph

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) (RAS = CAS = ViH)	lcc1	16	16	16	mA	
STANDBY CURRENT (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: \(^1RC = ^1RC \)(MIN))	lcc3	720	640	560	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _I L, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	560	480	400	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS=VIH: [†] RC = [†] RC (MIN))	lcc5	720	640	560	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	720	640	560	mA	3



MT8D168 16 MEG x 8 DRAM MODULE

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	Cıı	51	pF	2
Input Capacitance: RAS, WE, CAS	C ₁₂	67	pF	2
Input/Output Capacitance: DQ1-DQ8	Сю	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	14.4
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		45		50		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	22
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		. 15		20		20	ns	15
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	¹RASP	60	100.000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15	1,	20		20		ns	-
RAS precharge time	tRP	40		50		60		ns	· · · · · · ·
CAS pulse width	tCAS	15	100,000	20	100,000	20	100.000	ns	
CAS hold time	tCSH	60	100,000	70	100,000	80	100,000	ns	
CAS precharge time	tCPN	10	1	10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	5	1	5	"	5		ns	
Row address setup time	†ASR	0		0	+	0		ns	10 m
Row address hold time	tRAH	10	 	10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0	1.0	ns	
Output buffer turn-off delay	†OFF	0	15	0	15	0	15	ns	20
WE command setup time	twcs	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

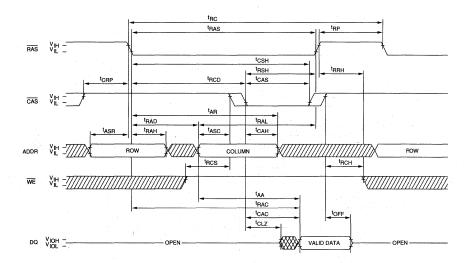
AC CHARACTERISTICS	-6		3	-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15	2.1	ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60	4247 (175) 44 (175)	ns	
Write command pulse width	tWP	10		15		15	pt - 15 c	ns	17.54
Write command to RAS lead time	tRWL	15		20	1000	20		ns	
Write command to CAS lead time	tCWL	15		20	1.22.	20		ns	
Data-in setup time	^t DS	0	4	0		0		ns	21
Data-in hold time	^t DH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	·Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	tREF		64	14.11	64	45	64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	e et e e
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5	T. W.	5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	^t WTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	twrs	10	gride in the con-	10		10		ns	24

MT8D168 16 MEG x 8 DRAM MODULE

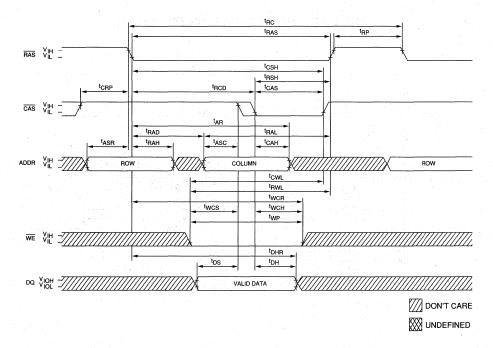
- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
 - 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 24. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). tWRP and tWRH are setup and hold specifications for the WE pin being held HIGH to enable the CBR refresh cycle.

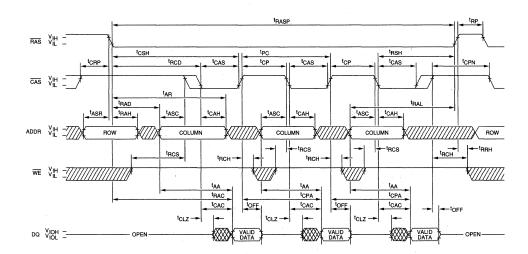
READ CYCLE



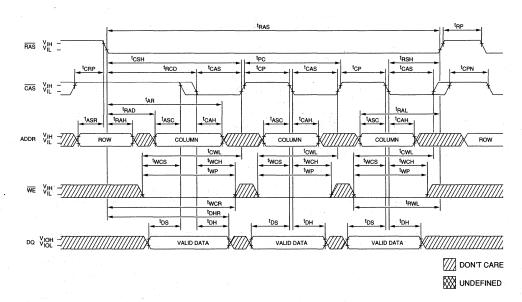
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



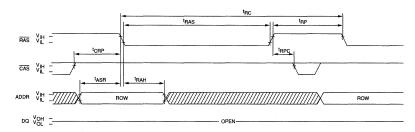
FAST-PAGE-MODE EARLY-WRITE CYCLE





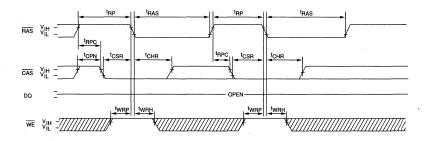
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; A11 and \overline{WE} = DON'T CARE)



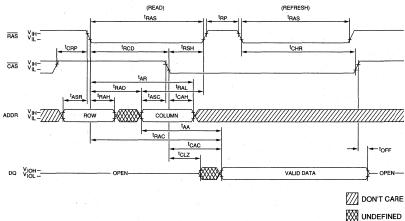
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

 $(\overline{WE} = HIGH)$





DRAM MODULE

256K x 9 DRAM

FAST PAGE MODE (MT3D2569) LOW POWER, EXTENDED REFRESH (MT3D2569 L)

FEATURES

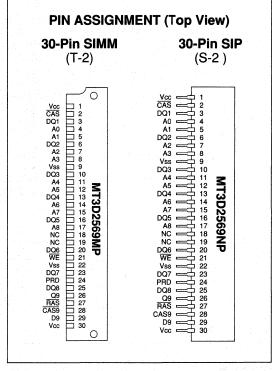
- Industry standard pinout in a 30-pin single-in-line memory module
- · High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW (.9mW L-version) standby; 625mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 60μA maximum (L-version)

60ns access 70ns access 80ns access Packages Leadless 30-pin SIMM Leaded 30-pin SIP Access Mode FAST PAGE MODE Power/Refresh Normal Power/8ms	MARKING
Timing	
60ns access	- 6
70ns access	-7
80ns access	- 8
and the second of the second o	M N
 Access Mode FAST PAGE MODE 	P
 Power/Refresh Normal Power/8ms Low Power/64ms 	Blank L

• Part Number Example: MT3D2569MPL-6

GENERAL DESCRIPTION

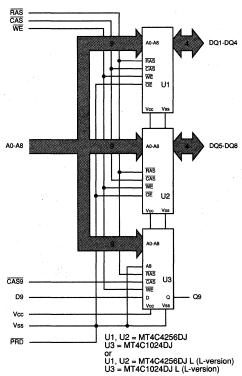
The MT3D2569 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered nine bits (A0-A8) at a time. \overline{RAS} is used to latch the first nine bits and \overline{CAS} the latter nine bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY-WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, and the output pins remain open (High-Z) until the next \overline{CAS} cycle.



FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE, \overline{RAS} -ONLY, \overline{CAS} -BEFORE- \overline{RAS} or HIDDEN REFRESH) so that all 512 combinations of \overline{RAS} addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

:	1 1					ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	^t R	tC	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	Х	Х	High-Z
READ		L	L	L	Н	ROW	COL	Data Out
EARLY-WRITE	Kalin Profesiona	L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	Toll 1	n/a	COL	Data In
RAS-ONLY REFRESI	H	L	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Х	Х	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	» b	L	Х	Х	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL -	-1.0	0.8	V	1
Input Low (Logic 0) Voltage, All Inputs INPUT LEAKAGE Any Input 0V ≤ VIN ≤ Vcc, (All other pins not under test = 0V) OUTPUT LEAKAGE (Q is disabled, 0V ≤ Vouт ≤ Vcc)	D9, CAS9	i li	-2	2	μΑ	
	A0-A8, RAS, WE	lı lı	-6	6	μΑ	
	DQ1-DQ8, Q9	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High (Logic 1) Voltage (Iout = -5mA) Output Low (Logic 0) Voltage (Iout = 5mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	6	6	6	mA	
STANDBY CURRENT: (CMOS)	lcc2	3	3	3	mA	24
$\overline{(RAS)} = \overline{CAS} = Vcc - 0.2V$.6	.6	.6	mA	24, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current	lcc3	270	240	210	mA	2, 22
(RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))		255	225	195	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE		210	180	150	mA	2, 22
Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	195	165	135	mA	2,22,26
REFRESH CURRENT: RAS-ONLY		270	240	210	mA	2
Average power supply current (RAS Cycling, CAS = V _I H: ^t RC = ^t RC (MIN))	Icc5	255	225	195	mA	2, 26
REFRESH CURRENT: CAS-BEFORE-RAS		270	240	210	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	255	225	195	mA	2,19,26
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1μs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125μs (512 rows at 125μs = 64ms)	lcc7	.6	.6	.6	mA	26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C ₁₁		19	pF	17
Input Capacitance: RAS, CAS, WE	C ₁₂		25	pF	17
Input Capacitance: D9	Сіз		10	pF	17
Input/Output Capacitance: DQ1-DQ8	Сю		15	pF	17
Output Capacitance: Q9	Со		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6 -7 -8		7 -8		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE	^t PC	40		40		45		ns	
cycle time									
PAGE-MODE READ or WRITE	^t PC	n/a		n/a		n/a		ns	
cycle time								it re	1.
Access time from RAS	^t RAC		60		70		80	ns	8
Access time from CAS (FAST PAGE MODE)	^t CAC		20		20		20	ns	9
Output Enable	^t OE		20		20		20	ns	
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	1
RAS precharge time	tRP	40		50		60	1	ns	
CAS pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	1
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	5		5	1,5	5		ns	1 N
Row address setup time	^t ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	^t RAD	15	30	15	35	15	40	ns	24
address delay time	ş						* 1 1 1	111	
Column address setup time	†ASC	0		0		0		ns	1.1
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time	tAR.	45		55		60		ns	100
(referenced to RAS)		i			Traff.		Again.	4/3/2009	
Column address to	tRAL.	30		35		40	1841 1960	ns	
RAS lead time			1 14.54				1 11 11 11	- K S	
Read command setup time	^t RCS	0	1902 : 18	0		0	i kawa P	ns	90.0
Read command hold time	^t RCH	0		0		0	- C. C. C.	ns	25
(referenced to CAS)			13.74						
Read command hold time	^t RRH	0	1346	0	1 2 2 2 2	0		ns	25
(referenced to RAS)			The second						11000



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6		- 1 - 1 -	7	-	В		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15	10.00	15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20	187.40	20		ns	
Data-in setup time	tDS	0		0	1000	0		ns	15
Data-in hold time	^t DH	15		15		15	100	ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	3/26
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS REFRESH)	tCHR	10		15		15		ns	19



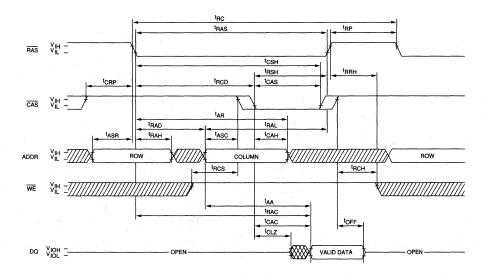
NOTES

- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight \overline{RAS} cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
 - 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
 - 11. If CAS = VIL, data output may contain data from the last valid READ cycle.
 - 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
 - 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the

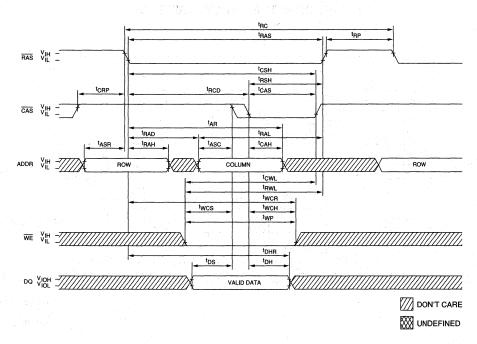
- specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. tRCH is referenced to the first rising edge of RAS or
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1 and U2.
- Icc is dependent on cycle rates.
- 23. All other inputs at Vcc -0.2V.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 25. Either ^tRCH or ^tRRH must be satisfied for a READ cvcle.
- 26. Applies to L-version only.



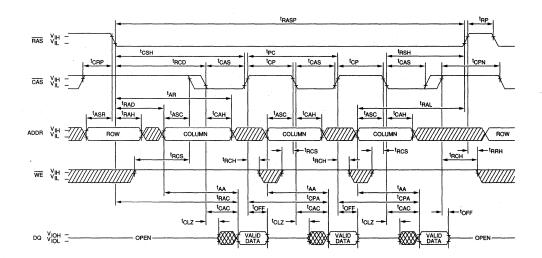
READ CYCLE



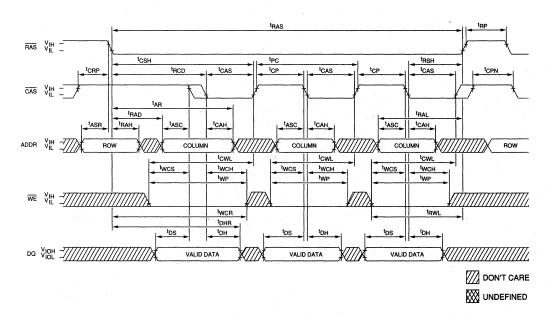
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

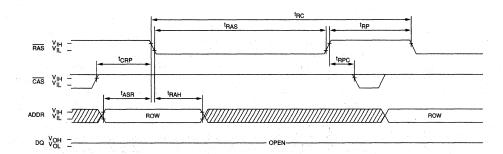


FAST-PAGE-MODE EARLY-WRITE CYCLE



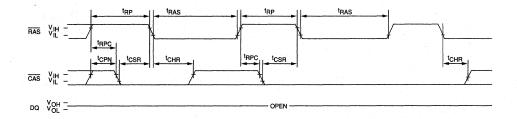


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



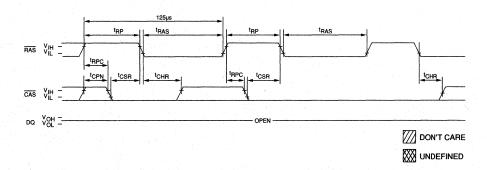
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8 and $\overline{WE} = DON'T CARE$)



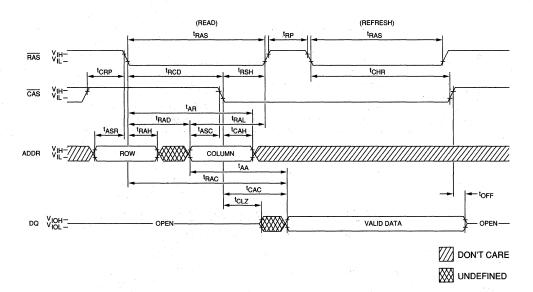
BATTERY BACKUP REFRESH CYCLE 26

(A0-A8 and $\overline{WE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 20

 $\overline{(WE = HIGH)}$





DRAM MODULE

1 MEG x 9 DRAM

FAST PAGE MODE (MT3D19) LOW POWER, EXTENDED REFRESH (MT3D19 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- · High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW (3mW L-version) standby; 625mW active, typical
- · All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile

ADTTONIC

- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- Low CMOS standby current, 600μA maximum (L-version)

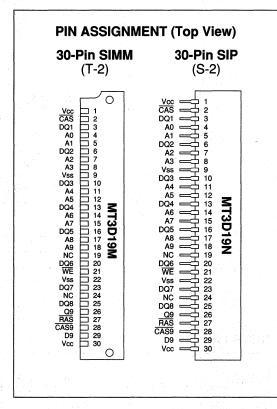
OPTIONS	MAKKIN
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

Part Number Example: MT3D19ML-6

GENERAL DESCRIPTION

The MT3D19 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, and the output pins remain open (High-Z) until the next \overline{CAS} cycle.

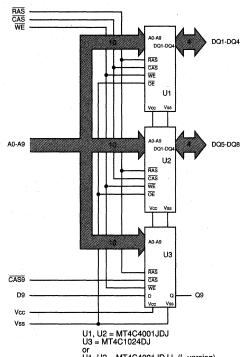
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9)



defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



or U1, U2 = MT4C4001JDJ L (L-version) U3 = MT4C1024DJ L (L-version)

TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	^t R	tC	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	Х	Х	High-Z
READ	1	L	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		i L	a ja L ij	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESI	+	L	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	Mou L 5	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	*, L	L	Х	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 7, 25) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1,
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ Vin ≤ Vcc	D9, <u>CAS9</u>	m, li	-2	2	μА	
(All other pins not under test = 0V)	A0-A9, RAS, WE	lı	-6	6	μА	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ Vout ≤ Vcc)	DQ1-DQ8, Q9	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High (Logic 1) Voltage (IouT = -5mA) Output Low (Logic 0) Voltage (IouT = 5mA)		Vol		0.4	V	

내려가 되는 그는 사람들이 살아 들어 먹는 이렇게 살아 되는 말을 했다.			MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	6	6	6	mA		
STANDBY CURRENT: (CMOS)	lcc2	3	3	3	mA	26	
$\overline{(RAS} = \overline{CAS} = Vcc -0.2V)$.6	.6	.6	mA	26, 27	
OPERATING CURRENT: Random READ/WRITE Average power supply current	lcc3	310	280	250	mA	2, 25	
(RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))		305	275	245	mA	2,25,27	
OPERATING CURRENT: FAST PAGE MODE Average power supply current	ICC4	230	200	170	mA	2, 25	
(RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))		225	195	165	mA	2,25,27	
REFRESH CURRENT: RAS-ONLY		310	280	250	mA	2	
Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	Icc5	305	275	245	mA	2, 27	
REFRESH CURRENT: CAS-BEFORE-RAS		310	280	250	mA	2, 19	
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	305	275	245	mA	2,19,27	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE = Vcc -0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	.8	.8	.8	mA	27	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}		19	pF	17
Input Capacitance: RAS, CAS, WE	C ₁₂		25	pF	17
Input Capacitance: D9	Сіз		10	pF	17
Input/Output Capacitance: DQ1-DQ8	Ci/o		10	pF	17
Output Capacitance: Q9	Co		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0^{\circ}C \le T_A \le +70^{\circ}C$; $Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			6	-	7	-8		4	3 N
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		- ns	-
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE	^t PC	40		40		45		ns	
cycle time									
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		n/a	21
Access time from RAS	tRAC	60	 		70		80	ns	8
Access time from CAS	†CAC		15	-	20		20	ns	9
Access time from column address	t _{AA}		30		35	<u> </u>	40	ns	
Access time from CAS precharge	†CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100.000	70	100,000	80	100,000	ns	†
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15	1,	20	1,	20	1	ns	†
RAS precharge time	tRP	40		50		60	1	ns	1
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80	1	ns	
CAS precharge time	tCPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10.		ns	1
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	10		10		10		ns	1
Row address setup time	tASR	0		0		0	1.	ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	22
Column address setup time	tASC	0		0	 	0	*	ns	-
Column address hold time	†CAH	10		15		15	1	ns	-
Column address hold time	tAR	50	1	55	+	60	 	ns	+
(referenced to RAS)		30				- 00	- CAT	113	
Column address to RAS lead time	†RAL	30		35		40		ns	
Read command setup time	tRCS	0	1 (31)	0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0	0 1/2 5 10 1	0		0		ns	24
Read command hold time (referenced to RAS)	†RRH	0		0	1 1 1 2 2	0		ns	24
	tCLZ	-		0		0		ne	+
CAS to output in Low-Z	CLZ	0		U		0	- P	ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		1,5 -€	3		-7	1 1 14 1	-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	twcs	0		0	19.00	0		ns	
Write command hold time	†WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	s especial Starte
Write command pulse width	tWP	10		15		15	10.2	ns	W-7
Write command to RAS lead time	tRWL	15		20		20	7 7 7 44 5	ns	
Write command to CAS lead time	tCWL	15		20		20		ns	1.42
Data-in setup time	^t DS	0		Ö		0	14.4	ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tT .	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	†REF	299	16/128		16/128		16/128	ms	3/27
RAS to CAS precharge time	tRPC	0		0		0	1.2	ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15	250	ns	19
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10	4.	10		10		ns	23
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10	tv. i	ns	23
WE hold time (WCBR test cycle)	^t WTH	10		10		10		ns	23
WE setup time (WCBR test cycle)	twrs	10		10		10	[Not Hays a	ns	23

DRAM MODULE

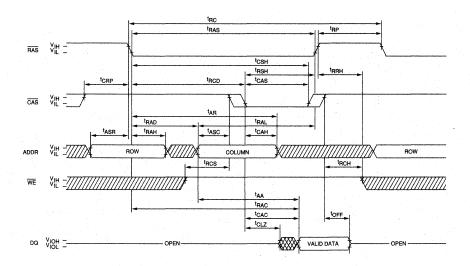
NOTES

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 4. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.

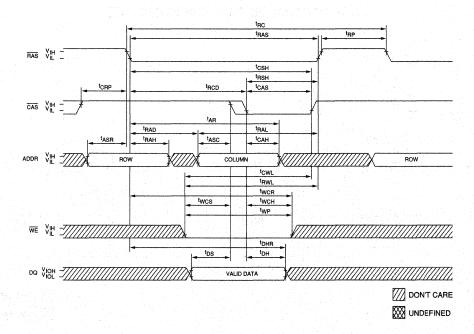
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1 and U2.
- 22. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 23. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 24. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 25. Icc is dependent on cycle rates.
- 26. All other inputs at Vcc 0.2V.
- 27. Applies to L-version only.



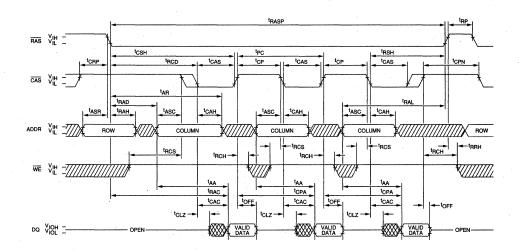
READ CYCLE



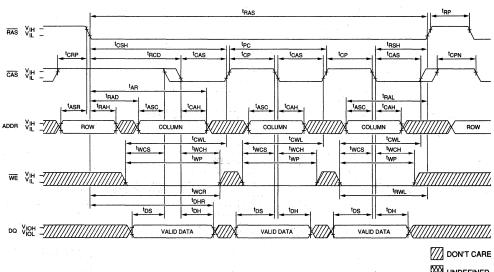
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



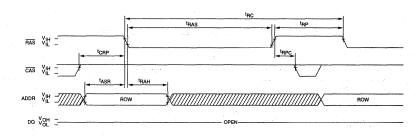
FAST-PAGE-MODE EARLY-WRITE CYCLE





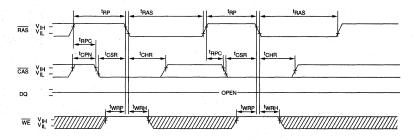
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; WE = DON'T CARE)



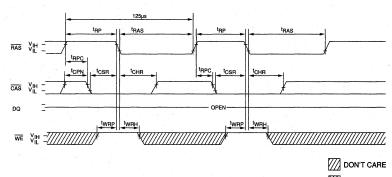
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



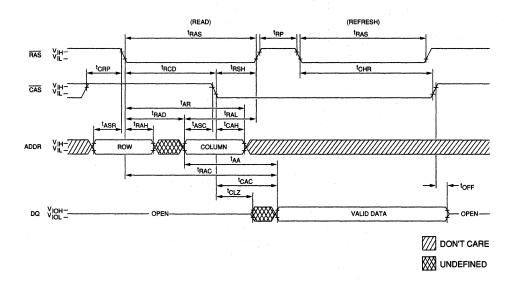
BATTERY BACKUP REFRESH CYCLE 27

(A0-A9 = DON'T CARE)





HIDDEN REFRESH CYCLE 20 (WE = HIGH)







MODULE

1 MEG x 9 DRAM

FAST PAGE MODE (MT9D19) LOW POWER. EXTENDED REFRESH (MT9D19 L)

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- · Single 5V ±10% power supply
- · All device pins are fully TTL compatible
- Low power, 27mW (2.7mW L-version) standby; 1,575mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

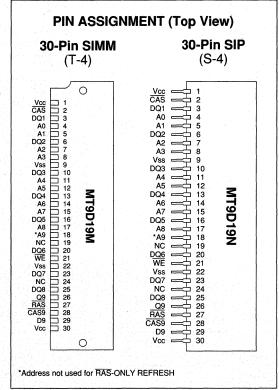
DPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
Power/Refresh	
Normal Power/8ms	Blank
Low Power/64ms	L

Part Number Example: MT9D19ML-6

GENERAL DESCRIPTION

The MT9D19 is a randomly accessed solid-state memory ontaining 1,048,576 words organized in a x9 configuration. buring READ or WRITE cycles, each word is uniquely ddressed through the 20 address bits, which are entered 10 its (A0-A9) at a time. RAS is used to latch the first 10 bits nd CAS the latter 10 bits. A READ or WRITE cycle is elected with the WE input. A logic HIGH on WE dictates EAD mode while a logic LOW on WE dictates WRITE 10de. During a WRITE cycle, data-in (D) is latched by the Illing edge of WE or CAS, whichever occurs last. EARLY-/RITE occurs when WE goes LOW prior to CAS going OW, and the output pins remain open (High-Z) until the ext CAS cycle.

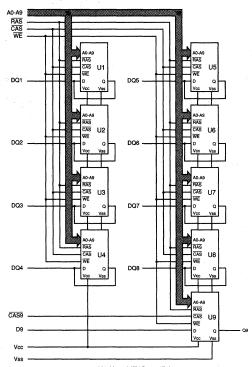
FAST PAGE MODE operations allow faster data operaons (READ or WRITE) within a row-address (A0-A9)



defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

U1-U9 = MT4C1024DJ U1-U9 = MT4C1024DJ L (L-version)

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	^t R	tC.	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	Х	Х	High-Z
READ		L	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESI	⊣	L	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	Lan	L	∠ H :	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Х	Х	Х	High-Z
BATTERY BACKUP		H→L	L	L	Х	Х	Х	High-Z
REFRESH (L-version)	<u>romainay kii.</u>	Georgia	Section 1					



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		 Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Vін	2.4	Vcc+1	V .	1.
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE: Any Input 0V ≤ ViN ≤ Vcc	D9, CAS9	i	-2	2	μΑ	
(All other pins not under test = 0V)	A0-A9, RAS, WE	lı	-18	18	μА	
OUTPUT LEAKAGE: (Q is disabled, 0V ≤ Vout ≤ Vcc)	DQ1-DQ8, Q9	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (IouT = -5mA) Output Low Voltage (IouT = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	18	18	18	mA	
STANDBY CURRENT: (CMOS)	lcc2	9	9	9	mA	23
$(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$		1.8	1.8	1.8	mA	23, 25
OPERATING CURRENT: Random READ/WRITE		810	.720	630	mA	3, 4
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	765	675	585	mA	3,4,25
OPERATING CURRENT: FAST PAGE MODE		630	540	450	mA	3, 4
Average power supply current (RAS = V _I L, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	585	495	405	mA	3,4,25
REFRESH CURRENT: RAS-ONLY		810	720	630	mA	3
Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	765	675	585	mA	3, 25
REFRESH CURRENT: CAS-BEFORE-RAS		810	720	630	mA	3, 5
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	765	675	585	mA	3,5,25
REFRESH CURRENT: BATTERY BACKUP (BBU)				. 10 Page		
Average power supply current during BATTERY BACKUP refresh: $\overline{\text{CAS}} = 0.2\text{V}$ or $\overline{\text{CAS}}$ -BEFORE-RAS cycling; $\overline{\text{RAS}} = {}^{\text{t}}\text{RAS}$ (MIN) to 1µs; $\overline{\text{WE}}$, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), ${}^{\text{t}}\text{RC} = 125\mu\text{s}$ (512 rows at $125\mu\text{s} = 64\text{ms}$)	lcc7	1.8	1.8	1.8	mA	25



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		58	pF	2
Input Capacitance: RAS, CAS, WE	Cı2		76	pF	2
Input Capacitance: D9	Сіз		10	pF	2
Input/Output Capacitance: DQ1-DQ8	Сю		15	pF	2
Output Capacitance: Q9	Co	4	10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS	-6		-7			-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC .	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		n/a	24
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	^t CAC		20		20		20	ns	15
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		. 10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	†RCD	20	40	20	60	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0.		0		ns	19



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 75°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6	-7		-8		100	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	†CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	.0	20	ns	20
WE command setup time	tWCS	0		0		0	1.00	ns	
Write command hold time	†WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	X 75.75
Write command to RAS lead time	†RWL	20		20		20		ns	14,71
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	^t DS	0		0		0		ns	21
Data-in hold time	^t DH	15		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	İΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	^t REF		8/64		8/64	7.7	8/64	ms	7/25
RAS to CAS precharge time	†RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	tCHR	10		15		15		ns	5

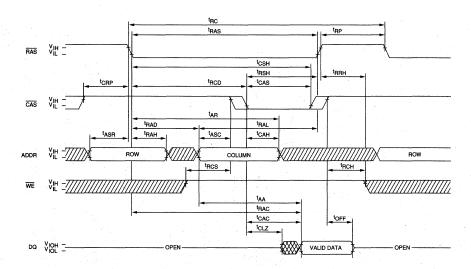
NOTES

- All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If CAS = VIH, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to two TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this

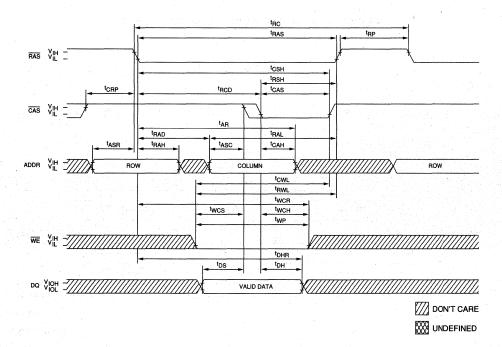
- table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 23. All other inputs equal Vcc -0.2V.
- 24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- 25. Applies to L-version only.



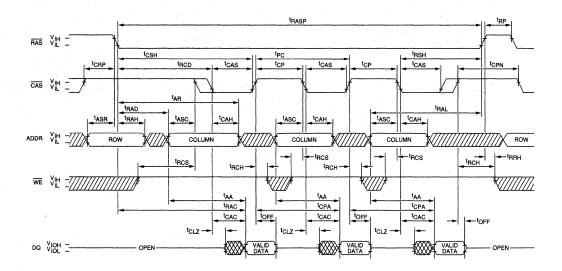
READ CYCLE



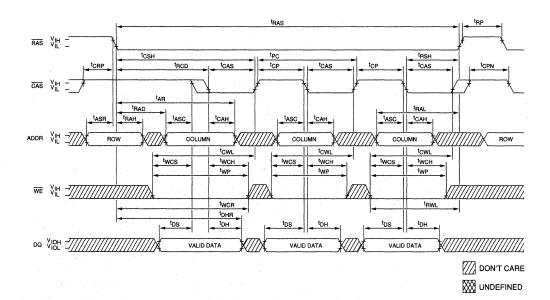
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



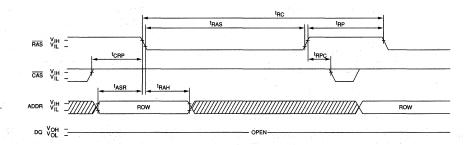
FAST-PAGE-MODE EARLY-WRITE CYCLE





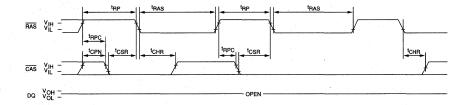
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; A9 and \overline{WE} = DON'T CARE)



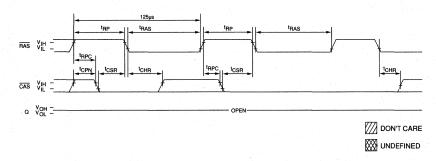
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 and $\overline{WE} = DON'T CARE$)

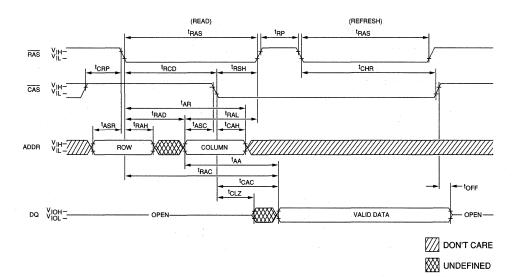


BATTERY BACKUP REFRESH CYCLE 25

(A0-A9 and $\overline{WE} = DON'T CARE$)



HIDDEN REFRESH CYCLE 22 (WE = HIGH)



DRAM MODULE

4 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin, single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 12mW standby; 775mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

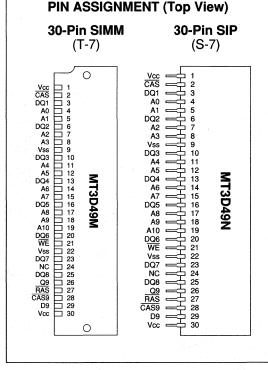
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Part Number Example: MT3D49M-6

GENERAL DESCRIPTION

The MT3D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. \overline{RAS} is used to latch the first 11 bits and \overline{CAS} the latter 11 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{CAS} . Since \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pins remain open (High-Z) until the next \overline{CAS} cycle.

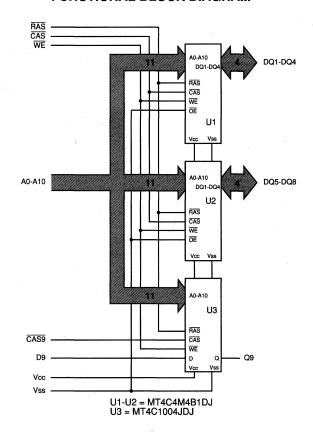
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$



followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST-PAGE-MODE operations.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	tR	tC t	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	Х	Х	High-Z
READ	<u> </u>	L	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L.	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L L L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESI	Η ;	L	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L = 6	H	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Н	X	Х	High-Z



MT3D49 4 MEG x 9 DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V 1 V 1 μΑ μΑ	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ Vin ≤ Vcc	D9, CAS9	li di	-2	2	μА	
(All other pins not under test = 0V)	A0-A10, RAS, WE	le le	-6	6	μА	
OUTPUT LEAKAGE (Q is disabled, 0V ≤ Vout ≤ Vcc)	DQ1-DQ8, Q9	loz	-10	10	μА	
OUTPUT LEVELS Output High (Logic 1) Voltage (Lour Em A)		Vон	2.4		٧	
Output High (Logic 1) Voltage (Ioυτ = -5mA) Output Low (Logic 0) Voltage (Ioυτ = 5mA)		Vol		0.4	٧	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL Input Levels (RAS = CAS = VIH)	lcc1	6	6	6	mA	
STANDBY CURRENT: CMOS Input Levels (RAS = CAS = Vcc -0.2V)	lcc2	3	3	3	mA	
OPERATING CURRENT (RAS and CAS = Cycling; ^t RC = ^t RC (MIN))	lccs	350	300	270	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling; ¹ PC = ¹ PC (MIN))	Icc4	240	210	180	mA	3, 4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vir; tRC = tRC (MIN))	lcc5	350	300	270	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS	Icc6	350	300	270	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C _{I1}		19	pF	2
Input Capacitance: RAS, CAS, WE	Cı2		25	pF	2
Input/Output Capacitance: DQ1-DQ8	Сю		10	pF	2
Input Capacitance: DQ9	Сіз		10	pF	2
Output Capacitance: Q9	Со		10	pF	2

NEW DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (Vcc = 5V ±10%)

AC CHARACTERISTICS			6	100	-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a	tris.	n/a		n/a		ns	22
FAST-PAGE-MODE	^t PC	40		40		45		ns	
READ or WRITE cycle time				347					
FAST-PAGE-MODE	†PRWC	n/a		n/a	1	n/a		ns	22
READ-WRITE cycle time									
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80	<u> </u>	ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	†RCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column	tRAD	15	30	15	35	15	40	ns	18
address delay time									
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time	†AR	50		55		60		ns	
(referenced to RAS)									
Column address to	tRAL	30		35		40		ns	
RAS lead time									
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	^t RCH	0		0		0	300	ns	19
(referenced to CAS)						1.56		Kara Sara	3.11
Read command hold time	tRRH	0		0		0		ns	19
(referenced to RAS)							kan a sa		
CAS to output in Low-Z	†CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7			8	Agree Afr	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45 . X,		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	100
Write command to RAS lead time	tRWL	15		20	1.795	20		ns	1,110
Write command to CAS lead time	tCWL	15		20	1 1 1 1 1 1 1 1	20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	†DH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	ΙT	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32		32	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	†WRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	†WRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	[†] WTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24

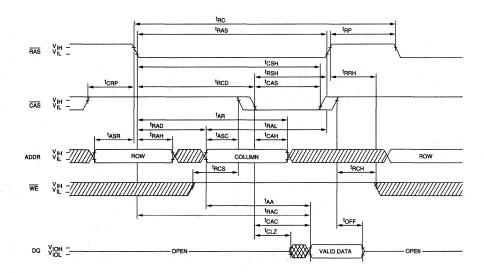
MT3D49 4 MEG x 9 DRAM MODULE

NOTES

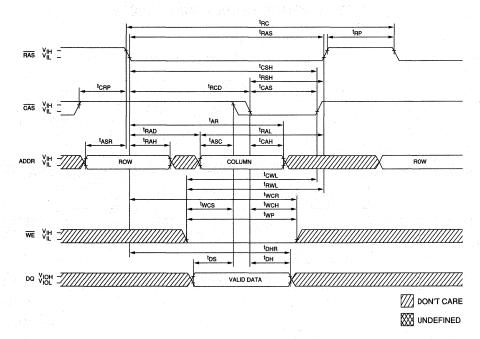
- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 22. OE is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 24. WTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.

READ CYCLE

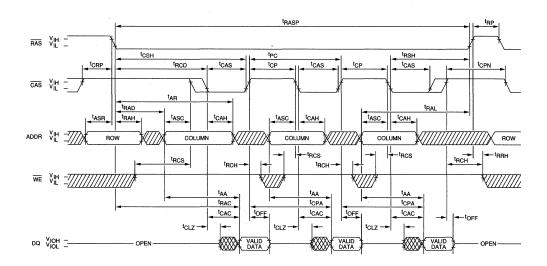


EARLY-WRITE CYCLE

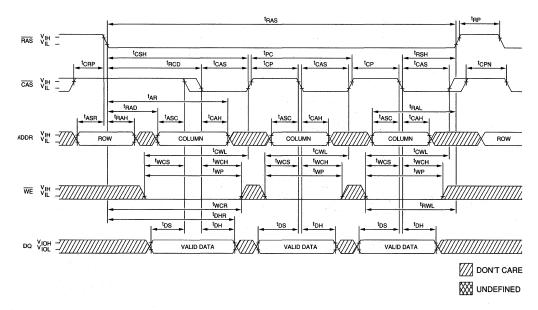


3-97

FAST-PAGE-MODE READ CYCLE



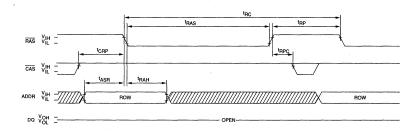
FAST-PAGE-MODE EARLY-WRITE CYCLE





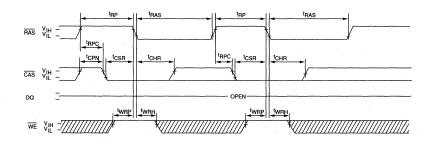
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; WE = DON'T CARE)



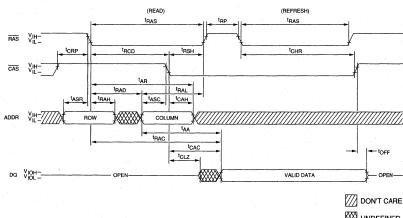
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

(WE = HIGH)





DRAM **MODULE**

4 MEG x 9 DRAM

FAST PAGE MODE (MT9D49) LOW POWER. EXTEDEND REFRESH (MT9D49 L)

FEATURES

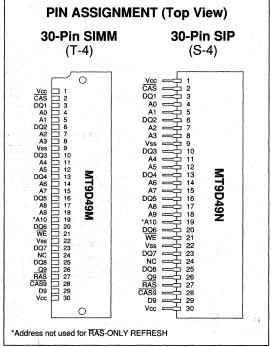
- Industry standard pinout in a 30-pin single-in-line
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW (9mW L-version) standby; 2,025mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.8mA maximum (L-version)

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	-8
• Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N
• Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

Part Number Example: MT9D49ML-6

GENERAL DESCRIPTION

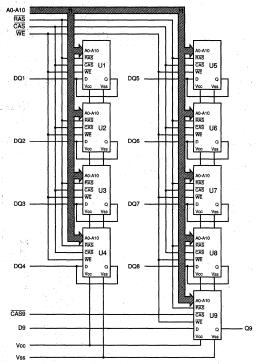
The MT9D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.



FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1004JDJ

TRUTH TABLE

or U1-U9 = MT4C1004JDJ L (L-version)

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	^t R	¹C	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	Х	Х	High-Z
READ		L	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	u Les	n/a	COL	Data In
RAS-ONLY REFRESI	1	L	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Н	X	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	> L	X	X	Х	High-Z



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1V to +7V \\ Operating Temperature, T_A (Ambient) & 0^{\circ}C to +70^{\circ}C \\ Storage Temperature (Plastic) & -55^{\circ}C to +125^{\circ}C \\ Power Dissipation & 9W \\ Short Circuit Output Current & 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	The state of the s	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	D9, CAS9	li li	-2	2	μА	2
Any Input: $0V \le V_{IN} \le 6.5V$ (All other pins not under test = $0V$)	A0-A10, WE, CAS, RAS	li di	-18	18	μА	
OUTPUT LEAKAGE CURRENT	Q9	loz	-10	10	μΑ	
(Q is disabled, $0V \le V_{OUT} \le 5.5V$)	DQ1-DQ8	loz	-12	12	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (IouT = -5mA) Output Low Voltage (IouT = 4.2mA)		Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	18	18	18	mA	
STANDBY CURRENT: (CMOS)	lcc2	9	9	9	mA	23
$\overline{(RAS)} = \overline{CAS} = Vcc -0.2V$		1.8	1.8	1.8	mA	23, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	990	900	810	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	ICC4	720	630	540	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: [†] RC = [†] RC (MIN))	lcc5	990	900	810	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icc6	990	900	810	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE = Vcc -0.2V, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	2.7	2.7	2.7	mA	26



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	.Ci1		58	pF	2
Input Capacitance: RAS, WE	C ₁₂		76	pF	2
Input Capacitance: D9	Сіз		10	pF	2
Input/Output Capacitance: DQ1-DQ8	Сю		15	pF	2
Output Capacitance: Q9	Со		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ	^t PC	40		40		45		ns	
or WRITE cycle time									
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		n/a	24
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60.	1	70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10	100	10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0	127.23	ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0	1	0	2.1	ns	
Write command hold time	tWCH.	. 10		15	1 V	15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15	1	ns	
Write command to RAS lead time	tRWL	15		20		20		ns	1.7
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	†DH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	7/26
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10		10		ns	25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	25
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	25
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	25

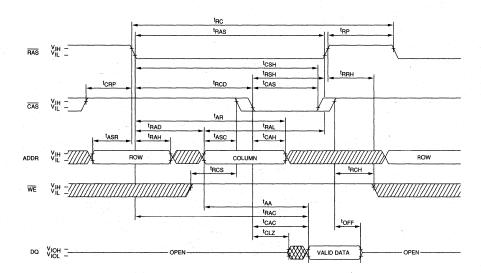
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to two TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

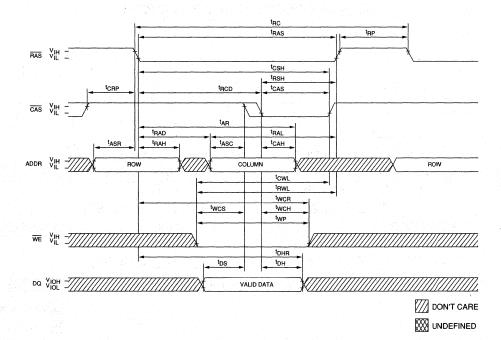
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 23. All other inputs equal Vcc -0.2V.
- 24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- 25. tWTS and tWTH are set up and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 26. Applies to L-version only.



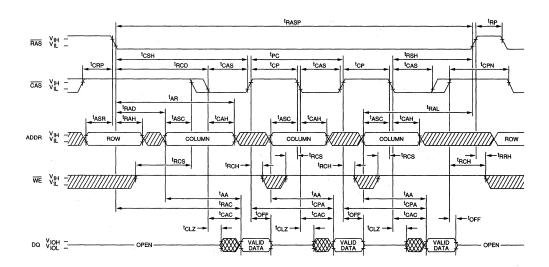
READ CYCLE



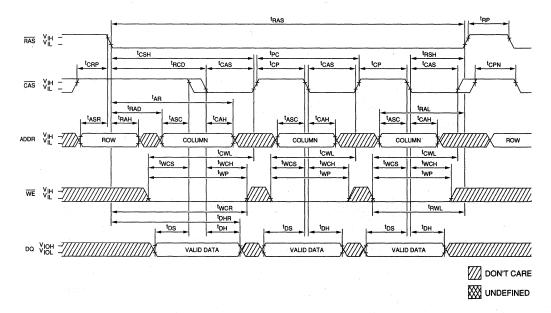
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE



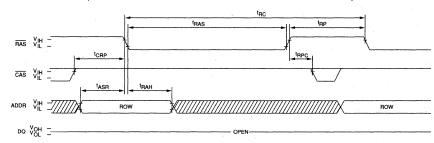
FAST-PAGE-MODE EARLY-WRITE CYCLE





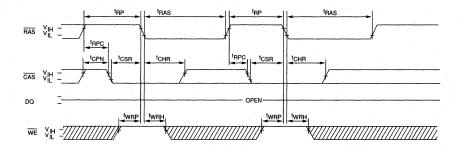
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; A10 and \overline{WE} = DON'T CARE)



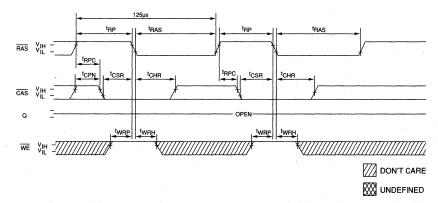
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



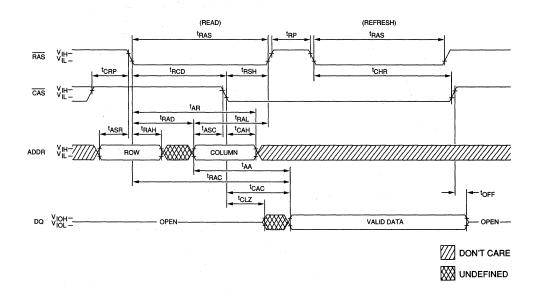
BATTERY BACKUP REFRESH CYCLE 26

(A0-A10 = DON'T CARE)



3-109

HIDDEN REFRESH CYCLE 22 (WE = HIGH)





DRAM MODULE

16 MEG x 9 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 30-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 2,475mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms
- FAST PAGE MODE access cycle

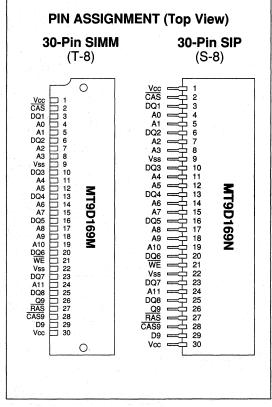
OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	-7
80ns access	-8
Packages	
Leadless 30-pin SIMM	M
Leaded 30-pin SIP	N

• Part Number Example: MT9D169M-6

GENERAL DESCRIPTION

The MT9D169 is a randomly accessed solid-state memory containing 16,777,216 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 24 address bits which are entered 12 bits (A0-A11) at a time. \overline{RAS} is used to latch the first 12 bits and \overline{CAS} the latter 12 bits. A READ or WRITE cycle is selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode, while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{CAS} . Since \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

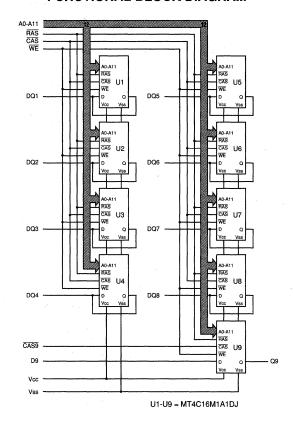
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A11) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may



be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 4,096 combinations of RAS addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR refresh cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	CAS9	WE	^t R	t _C	DQ1-DQ8, D9, Q9
Standby		Н	H→X	H→X	Х	X	X	High-Z
READ		L	L	Ŀ	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	. L	H→L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESI	H 1 - 1 - 1 - 1 - 1	L - L - 1	Н	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS F	REFRESH	H→L	L	L	Н	Х	X	High-Z



MT9D169 16 MEG x 9 DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & -1V to +7V \\ Operating Temperature, T_A (Ambient) & 0°C to +70°C \\ Storage Temperature (Plastic) & ... -55°C to +125°C \\ Power Dissipation & ... 9W \\ Short Circuit Output Current & ... 50mA \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0° C $\leq T_A \leq 70^{\circ}$ C; $V_{CC} = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	- 1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input: 0V ≤ ViN ≤ 6.5V	A0-A11, WE, RAS	h	-18	18	μΑ	
(All other pins not under test = 0V)	D9, CAS9	h h	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ 5.5V)	DQ1-DQ8, Q9	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (IouT = -5mA) Output Low Voltage (IouT = 4.2mA)		Vol		0.4	٧	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT (TTL) (RAS = CAS = ViH)	lcc1	18	18	18	mA	
STANDBY CURRENT (CMOS) (RAS = CAS = Vcc -0.2V)	Icc2	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	810	720	630	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ¹ PC = ¹ PC (MIN))	Icc4	630	540	450	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	810	720	630	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcce	810	720	630	mA	3

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	Cıı	58	pF	2
Input Capacitance: RAS, WE, CAS	C ₁₂	76	pF	2
Input/Output Capacitance: DQ1-DQ8	Cio	15	pF	2
Input Capacitance: D9, CAS9	Сіз	10	pF	2
Output Capacitance: Q9	Co	10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a	1	n/a	,	ns	22
FAST-PAGE-MODE	^t PC	35		40		40		ns	
READ or WRITE cycle time									
FAST-PAGE-MODE	^t PRWC	n/a		n/a	1	n/a		ns	22
READ-WRITE cycle time			1						
Access time from RAS	^t RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0	10.00	ns	
Row address hold time	^t RAH	10		10		10	1 1 1 1	ns	1800
RAS to column	†RAD	15	30	15	35	15	40	ns	18
address delay time									
Column address setup time	†ASC	0		0		0		ns	21.20
Column address hold time	^t CAH	10		15		15		ns	3,30
Column address hold time	tAR .	50		55		60		ns	
(referenced to RAS)								50,000 10,000 10,000	
Column address to	^t RAL	30		35	1 1000	40		ns	
RAS lead time			1						
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	^t RCH	0		0		0		ns	19
(referenced to CAS)					Tuestie.	\$441.5		rani eni	
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)						1000			



MT9D169 16 MEG x 9 DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = 5V ±10%)

AC CHARACTERISTICS	1 2 2 2		6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	¹OFF	5	15	-5	15	5	15	ns	20
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	3 1 1 1
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15	1	ns	
Write command to RAS lead time	tRWL	15		20		20		ns	Sept.
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH t	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55	in the state of th	60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	tREF		64		64		64	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5	1 2 2 2	ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	[†] WRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	[†] WTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24

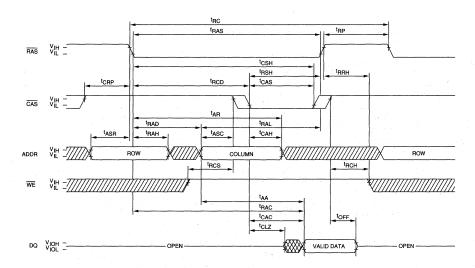
NOTES

- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.

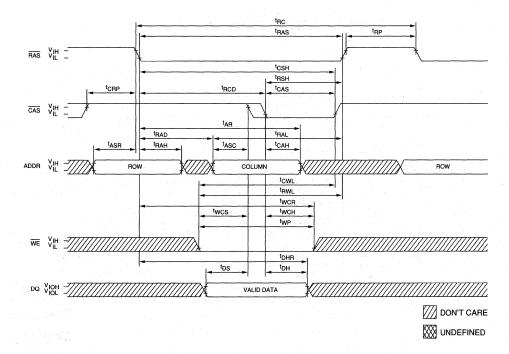
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 22. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$ and $\overline{OE} =$
- 24. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.



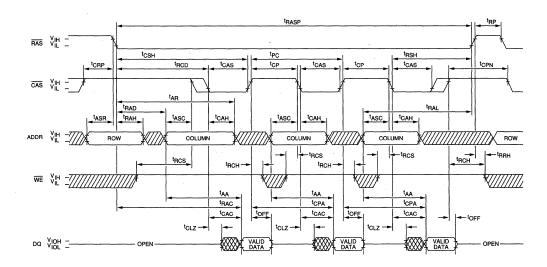
READ CYCLE



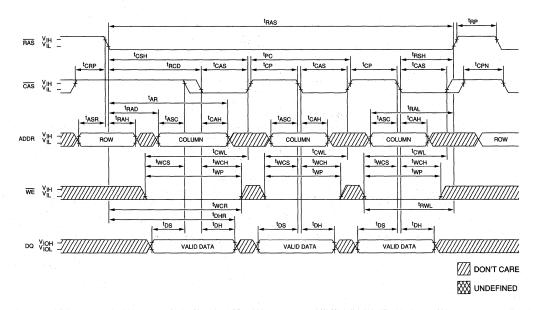
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

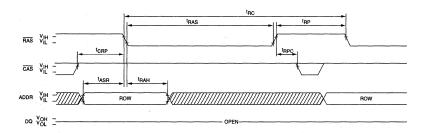


FAST-PAGE-MODE EARLY-WRITE CYCLE



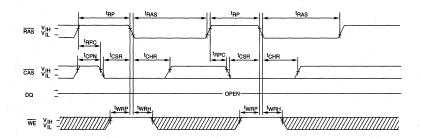


RAS-ONLY REFRESH CYCLE (ADDR = A0-A11; WE = DON'T CARE)

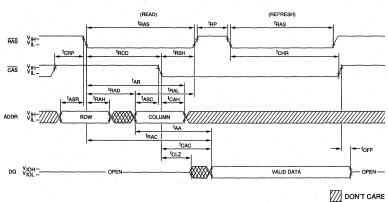


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE 23 $(\overline{WE} = HIGH)$



₩ undefined



DRAM **MODULE**

256K x 32, 512K x 16

FAST PAGE MODE (MT8D25632) LOW POWER. EXTENDED REFRESH (MT8D25632 L)

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (2.4mW L-version) standby; 1,400mW active, typical
- Multiple RAS lines offer x16 or x32 widths
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

MARKING OPTIONS Timing 60ns access - 6 70ns access - 7 80ns access - 8 Packages Leadless 72-pin SIMM M Leadless 72-pin SIMM (Gold) G Power/Refresh

Normal Power/8ms Blank Low Power/64ms L

• Part Number Example: MT8D25632ML-6

GENERAL DESCRIPTION

The MT8D25632 is a randomly accessed solid-state memory containing 262,144 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-9)

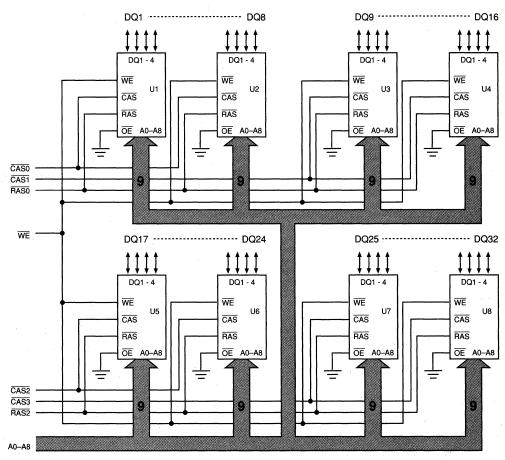


PIN#	SYMBOL	PIN#	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
-1	Vss	19	. NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ U1-U8 = MT4C4256DJ L (L-version)



TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC	DQ1-DQ32
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	<u>L</u>	Х	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L		X	Х	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	8W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C \leq $T_A \leq$ 70°C; Vcc = 5V $\pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	- /	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Vih	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	RASO, RAS2	lı1	-8	8	μΑ	
Any input: 0V ≤ VIN ≤ Vcc	A0-A8, WE	l ₁₂	-16	16	μΑ	
(All other pins not under test = 0V) For each package input	CAS0-CAS3	lıз	-4	4	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) For each package input	DQ1-DQ32	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 5mA)		Vol		0.4	v	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	16	16	16	mA	
STANDBY CURRENT: (CMOS)	lcc2	8	8	8	mA	
$\overline{(RAS} = \overline{CAS} = Vcc -0.2V)$		1.6	1.6	1.6	mA	24
OPERATING CURRENT: Random READ/WRITE		720	640	560	mA	2, 22
Average power supply current (RAS, CAS, Address Cycling: tRC = tRC (MIN))	lcc3	680	600	520	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE		560	480	400	mA	2, 22
Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	Icc4	520	440	360	mA	2,22,24
REFRESH CURRENT: RAS-ONLY		720	640	560	mA	2
Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	680	600	520	mA	2, 24
REFRESH CURRENT: CAS-BEFORE-RAS		720	640	560	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	680	600	520	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1μs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125μs (512 rows at 125μs = 64ms)	lcc7	1.6	1.6	1.6	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cıı		51	pF	17
Input Capacitance: WE	Cı2		67	pF	17
Input Capacitance: RAS0	Сіз		34	pF	17
Input Capacitance: CAS0-CAS3	C ₁₄		17	pF	17
Input/Output Capacitance: DQ1-DQ32	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7		-8	197	Mar New
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC		60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE		20		20		20	ns	
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20	1. * - 1	20		20		ns	
RAS precharge time	tRP	40		50	0.4	60		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	†RAH	10		10	12.5	10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	23
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	15		15	144	15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6		-7		-8		1.5	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0 .	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	^t RWL	20		20		20		ns	
Write command to CAS lead time	tCML	20		20		20		ns	
Data-in setup time	^t DS	0		0		0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	t T	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	3/24
RAS to CAS precharge time	tRPC	0		0		. 0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	19

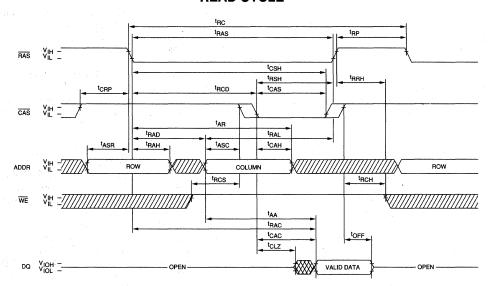


NOTES

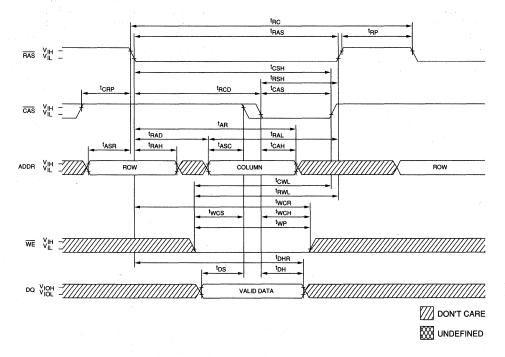
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- 5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U8.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 24. Applies to L-version only.

READ CYCLE

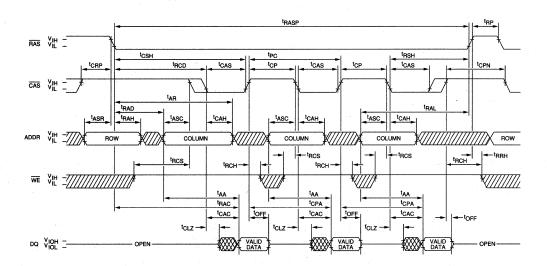


EARLY-WRITE CYCLE

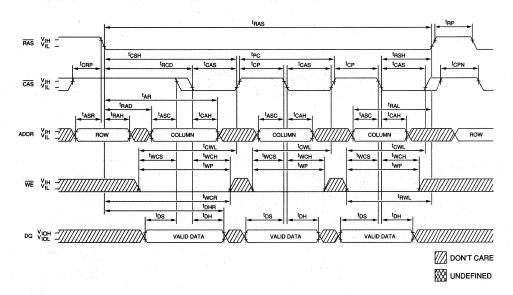




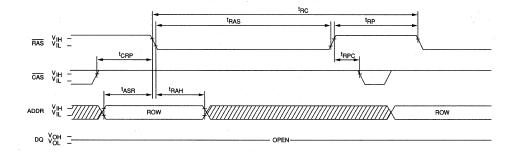
FAST-PAGE-MODE READ CYCLE



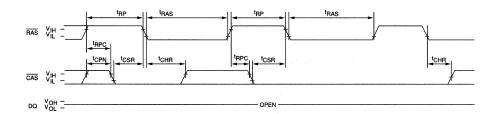
FAST-PAGE-MODE EARLY-WRITE CYCLE



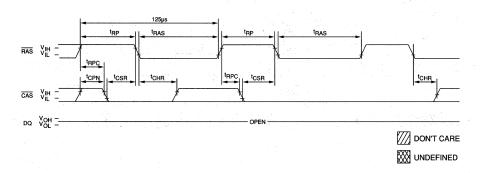
RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE (A0-A8, WE = DON'T CARE)

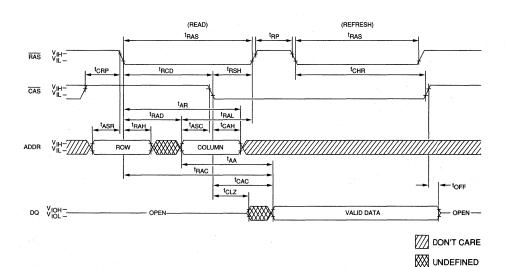


BATTERY BACKUP REFRESH CYCLE ²⁴ (A0-A8, WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

512K x 32, 1 MEG x 16

FAST PAGE MODE (MT16D51232) LOW POWER, EXTENDED REFRESH (MT16D51232 L)

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 48mW (4.8mW L-version) standby;
 1,424mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Multiple RAS lines offer x16 or x32 widths
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 3.2μA maximum (L-version)

OPTIONS • Timing 60ns access 70ns access 80ns access - 8 • Packages

- Power/Refresh
 Normal Power/8ms
 Blank
 Low Power/64ms
 L
- Part Number Example: MT16D51232G-6

GENERAL DESCRIPTION

Leadless 72-pin SIMM (Gold)

Leadless 72-pin SIMM

The MT16D51232 is a randomly accessed solid-state memory containing 524,288 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

M

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8)

PIN ASSIGNMENT (Top View)

72-Pin SIMM (T-10)

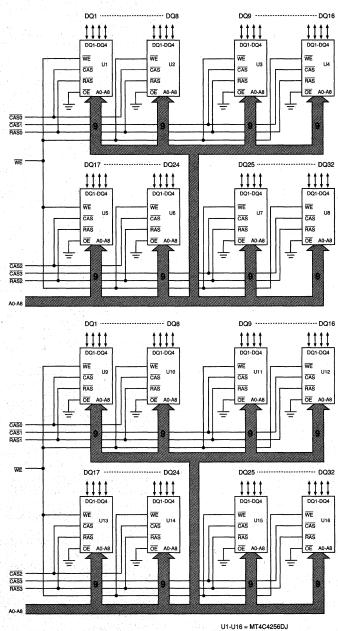


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4256DJ U1-U16 = MT4C4256DJ L (L-version)



TRUTH TABLE

				ADDR	ESSES	DATA IN/OUT	
FUNCTION		RAS	CAS	WE	^t R	tC	DQ1-DQ32
Standby		H	H→X	Х	Х	Х	High-Z
READ	17.1.1	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Χ	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H 1	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	Ľ	X	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L		X	Х	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss-1V to +7V Operating Temperature, T_A (Ambient)0°C to +70°C Storage Temperature (Plastic)-55°C to +125°C Power Dissipation16W Short Circuit Output Current50mA *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) ($0^{\circ}C \le T_{\Delta} \le 70^{\circ}C$; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1	
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1	
Input Low (Logic 0) Voltage, All Inputs		VIL	V	1		
INPUT LEAKAGE CURRENT	CAS0-CAS3	l ₁₁	-8	8	μΑ	
Any Input: 0V ≤ VIN ≤ Vcc	A0-A8, WE	l ₁₂	-32	32	μΑ	
(All other pins not under test = 0V) For each package input	RAS0-RAS3	lıз	-8	8	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) For each package input	DQ1-DQ32	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iouт = -5mA) Output Low Voltage (Iouт = 5mA)	Vol		0.4	v		

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = V_{\text{IH}})$	lcc1	32	32	32	mA	
STANDBY CURRENT: (CMOS)	lcc2	16	16	16	mA	
$\overline{(RAS} = \overline{CAS} = Vcc - 0.2V)$		3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE		736	656	576	mA	2, 22
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	684	604	524	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE		576	496	416	mA	2, 22
Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	ICC4	524	444	364	mA	2,22,24
REFRESH CURRENT: RAS-ONLY		736	656	576	mA	2
Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	684	604	524	mA	2, 24
REFRESH CURRENT: CAS-BEFORE-RAS		736	656	576	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	684	604	524	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1µs; WE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125µs (512 rows at 125µs = 64ms)	lcc7	3.2	3.2	3.2	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C ₁₁		102	pF	17
Input Capacitance: WE	Cı2		134	рF	17
Input Capacitance: CAS0-CAS3, RAS0-RAS3	C ₁₄		34	рF	17
Input/Output Capacitance: DQ1-DQ32	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C $\leq T_A \leq$ 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110	1	130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a	4.	n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC		. 60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE	1 1	20		20		20	ns	
Access time from column address	^t AA		30		35	:	40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP .	40		50		60		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	†CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10	7	10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	. 0	10 To 10 To 1	0		0		ns	1 - 1 -
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	23
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	†RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS.	0		0		0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tŢ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^t REF		8/64		8/64		8/64	ms	3/24
RAS to CAS precharge time	†RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	†CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	19

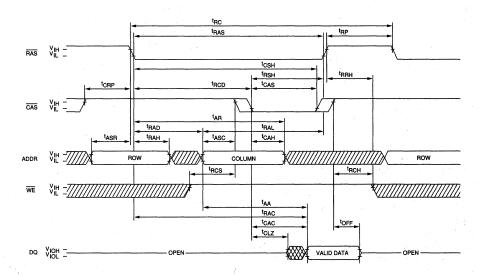


NOTES

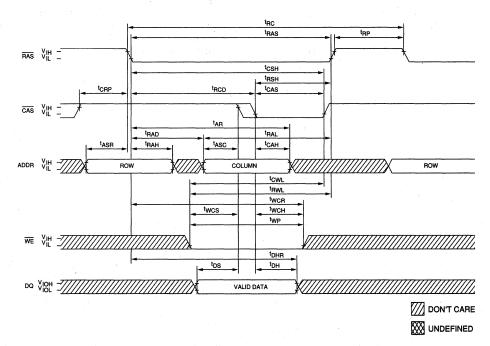
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If CAS = Vπ, data output may contain data from the last valid READ cycle.
- *OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U16.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 24. Applies to L-version only.

READ CYCLE

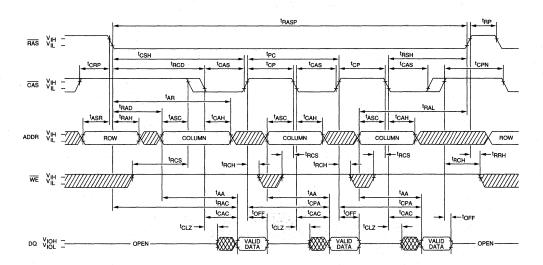


EARLY-WRITE CYCLE

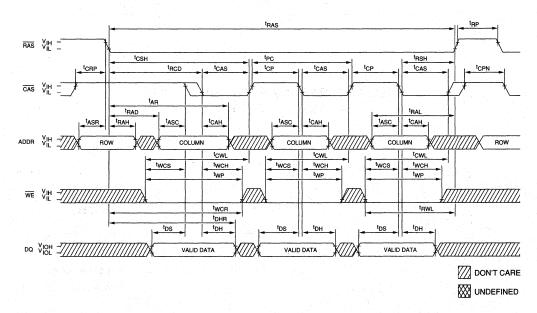




FAST-PAGE-MODE READ CYCLE

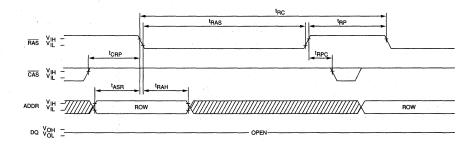


FAST-PAGE-MODE EARLY-WRITE CYCLE



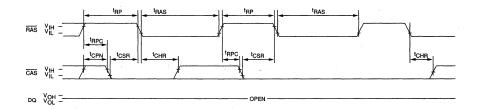
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7; A8 and \overline{WE} = DON'T CARE)



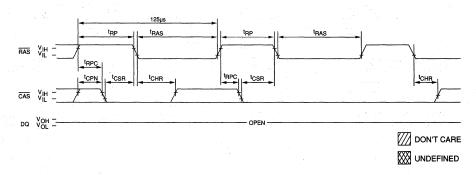
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A8, \overline{WE} = DON'T CARE)$



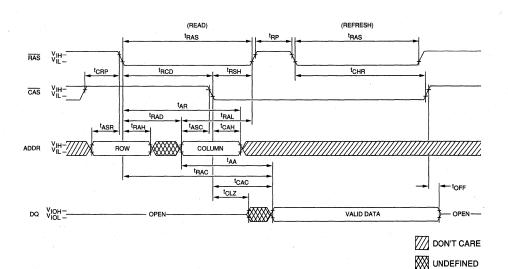
BATTERY BACKUP REFRESH CYCLE 24

(A0-A8, WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

1 MEG x 32, 2 MEG x 16

FAST PAGE MODE (MT8D132) LOW POWER, EXTENDED REFRESH (MT8D132 L)

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 24mW (8mW L-version) standby; 1,800mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms

MARKING

- FAST PAGE MODE access cycle
- Low CMOS standby current 1.6mA maximum (L-version)

01 110110	*****
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 72 -pin SIMM	M
Leadless 72-pin SIMM (Gold	l) G
Power/Refresh	
Normal Power/16ms	Blank
Low Power/128ms	L

GENERAL DESCRIPTION

• Part Number Example: MT8D132GL-6

The MT8D132 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. A READ or WRITE cycle is elected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates \overline{WE} and \overline{WE} while a logic LOW on \overline{WE} dictates WRITE node. During a WRITE cycle, data-in (D) is latched by the alling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} coes LOW prior to \overline{CAS} going LOW, the output pin(s) emain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) lefined page boundary. The FAST PAGE MODE cycle is lways initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-9)

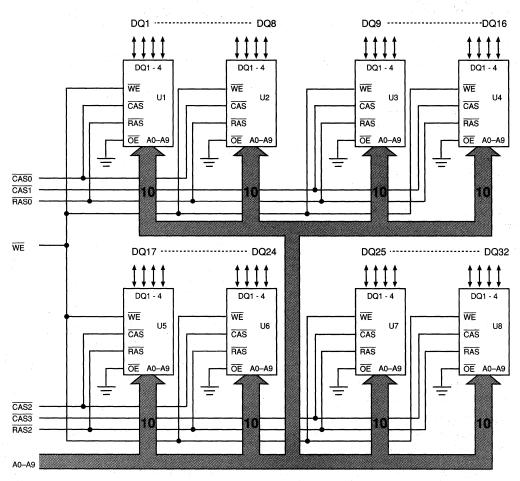
MT8D132M/G

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO CASO	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	-30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	. A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ U1-U8 = MT4C4001JDJ L (L-version)

DRAM MODULE

TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC	DQ1-DQ32
Standby		Н	H→X	Х	X	Х	High-Z
READ		L	, L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	CAS-BEFORE-RAS REFRESH		L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	Х	Х	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient).	
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	8W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

						
PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	RASO, RAS2	l ₁₁	8	8	μΑ	
Any Input: 0V ≤ Vin ≤ Vcc	A0-A9, WE	lı2	-16	16	μΑ	
(All other pins not under test = 0V) For each package input	CAS0-CAS3	lıз	-4	4	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) For each package input	DQ1-DQ32	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 5mA)		Vol		0.4	v	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	16	16	16	mA	
STANDBY CURRENT: (CMOS)	lcc2	8	8	8	mA	
$\overline{(RAS)} = \overline{CAS} = Vcc -0.2V$	and the second second	1.6	1.6	1.6	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	880	800	720	mA	2, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	Icc4	640	560	480	mA	2, 22
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	880	800	720	mΑ	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC (MIN))	Icc6	880	800	720	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300µs; WE = Vcc -0.2V; A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	2.4	2.4	2.4	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}		51	pF	17
Input Capacitance: WE	Cı2		67	pF	17
Input Capacitance: RAS0, RAS2	Сіз		34	pF	17
Input Capacitance: CASO, CASO, CASO, CASO, CASO	C ₁₄		17	pF	17
Input/Output Capacitance: DQ1-DQ32	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	^t RAC		60		70	. ;	80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Output Enable	†OE		15		20		20	ns	
Access time from column address	†AA	7777	30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	agarthyddia
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	200,000	70	200,000	80	200,000	ns	100
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40	1000	50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70	1. 1. 25	80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	23
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15	1	15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40	x 2	ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			6		-7		8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCML	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	İΤ	3	50	3	50	3 .	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/24
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	†CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	
WE setup time (WCBR test cycle)	twts	10		10		10		ns	



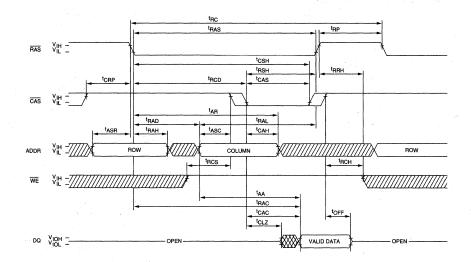
NOTES

- 1. All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ${}^{t}T = 5ns$.
- 5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

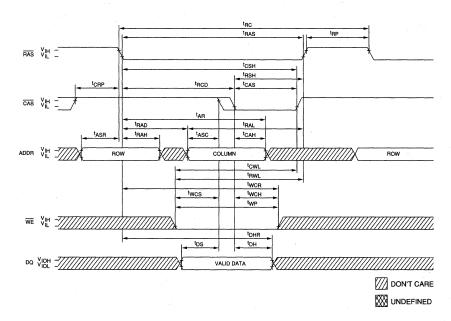
- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U8.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 24. Applies to L-version only.



READ CYCLE

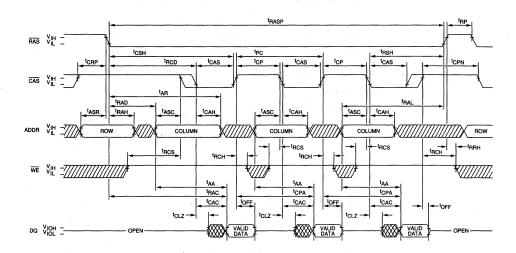


EARLY-WRITE CYCLE

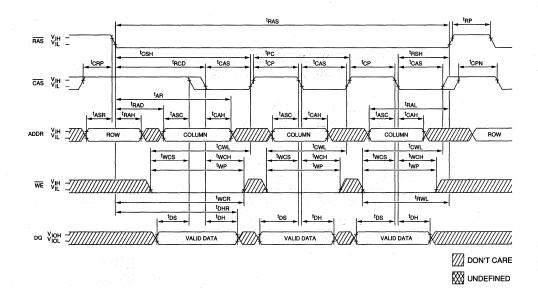




FAST-PAGE-MODE READ CYCLE

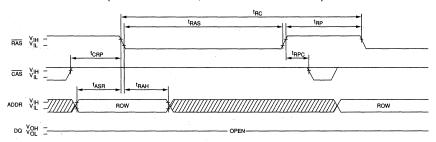


FAST-PAGE-MODE EARLY-WRITE CYCLE



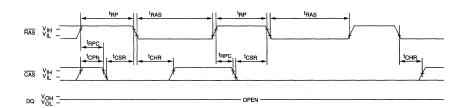
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; WE = DON'T CARE)



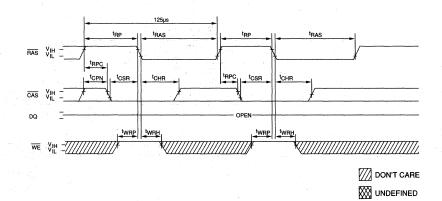
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9, \overline{WE} = DON'T CARE)$



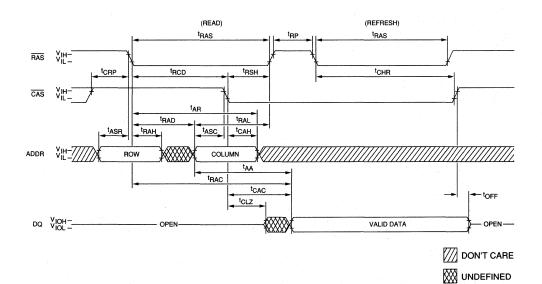
BATTERY BACKUP REFRESH CYCLE 24

(A0-A9, WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

2 MEG x 32, 4 MEG x 16

FAST PAGE MODE (MT16D232) LOW POWER. EXTENDED REFRESH (MT16D232 L)

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 48mW (16mW L-version) standby; 1,824mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Multiple RAS lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms

MARKING

- FAST PAGE MODE access cycle
- Low CMOS standby current, 3.2mA maximum (L-version)

•	Timing		
	60ns access	- 6	
	70ns access	- 7	
	80ns access	- 8	
•	Packages		
	Leadless 72-pin SIMM	M	
	Leadless 72-pin SIMM (Gold)	\mathbf{G}	
	Power/Refresh		
	Normal Power/16ms	Blank	
	Low Power/128ms	L	

Part Number Example: MT16D232GL-6

GENERAL DESCRIPTION

The MT16D232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY-WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-10)

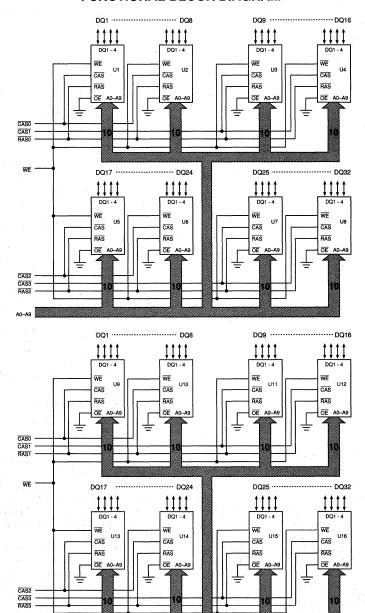


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combination of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001JDJ U1-U16 = MT4C4001JDJ L (L-version)



TRUTH TABLE

					ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC t	DQ1-DQ32
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L		X	X	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0° C $\leq T_A \leq 70^{\circ}$ C; Vcc = 5V $\pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	-	Vcc	4.5	5.5	· V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CASO-CAS3	lı1	-8	8	μΑ	11
Any Input 0V ≤ Vin ≤ Vcc	A0-A9, WE	l ₁₂	-32	32	μΑ	
(All other pins not under test = 0V) For each package input	RAS0-RAS3	lıз	-8	8	μΑ	4.0
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) For each package input	DQ1-DQ32	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 5mA)		Vol		0.4	v	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	32	32	32	mA	
STANDBY CURRENT: (CMOS)	lcc2	16	16	16	mA	
$\overline{(RAS} = \overline{CAS} = Vcc - 0.2V)$	* 1 2 2	3.2	3.2	3.2	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	896	816	736	mA	2, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	656	576	496	mA	2, 22
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	896	816	736	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	896	816	736	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE = Vcc -0.2V; A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	4.8	4.8	4.8	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı	1.00	102	pF	17.
Input Capacitance: WE	Cı2		134	pF	17
Input Capacitance: CASO-CAS3, RASO-RAS3	C ₁₄		34	pF	17
Input/Output Capacitance: DQ1-DQ32	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	-6			-7		-8			10000
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	- 17 J
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC		60	1.0	70		80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Output Enable	^t OE		15		20		20	ns	
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	1
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	200,000	70	200,000	80	200,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		- 80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	10		10		10		ns	10.00
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	23
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	†RCS	0		0		0		ns	1.00
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14
CAS to output in Low-Z	†CLZ	0		0		0	1	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55	: 14 V.	60		ns	
Write command pulse width	tWP	10		15	1.0	15		ns	
Write command to RAS lead time	^t RWL	15		20		- 20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	^t DS	0		0		0		ns	15
Data-in hold time	tDH t	10		15		15	100 100 104	ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT.	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/24
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10	 W	10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10	. "	10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10	7 74 3	10		10		ns	
WE hold time (WCBR test cycle)	tWTH	10		10	i (e.g.)	10		ns	
WE setup time (WCBR test cycle)	twts	10		10		10		ns	

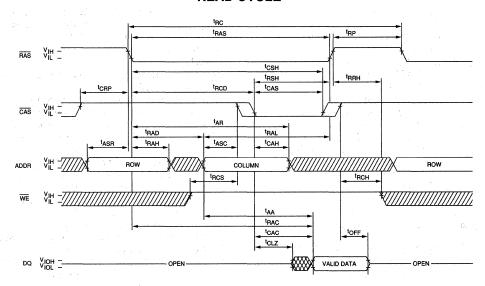


NOTES

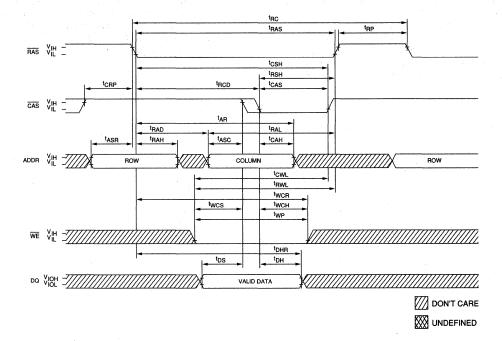
- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- 5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. Measured with a load equivalent to two TTL gates and 100pF.
- 8. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If $\overline{CAS} = VIH$, data output is High-Z.
- 11. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to \overline{CAS} leading edge in EARLY-WRITE cycles.
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U16.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 24. Applies to L-version only.

READ CYCLE

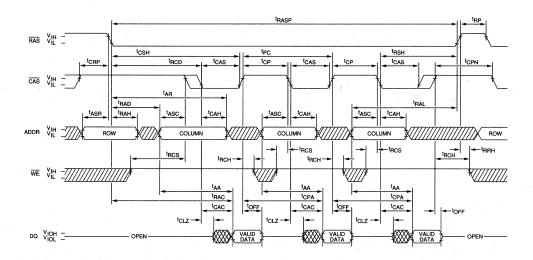


EARLY-WRITE CYCLE

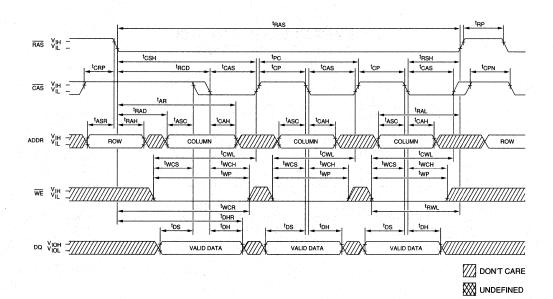




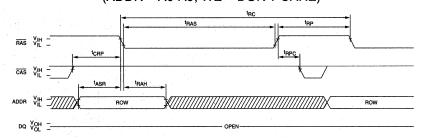
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

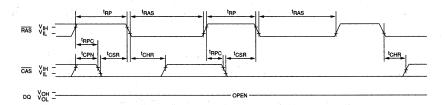


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



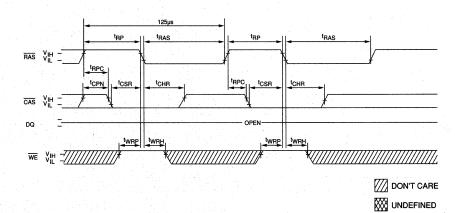
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9, $\overline{WE} = DON'T CARE$)



BATTERY BACKUP REFRESH CYCLE 24

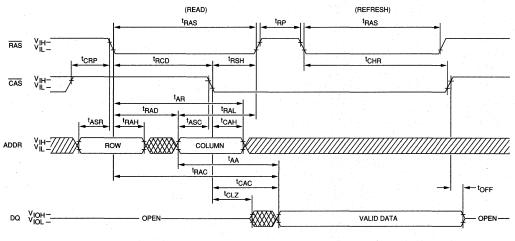
 $(A0-A9, \overline{WE} = DON'T CARE)$





HIDDEN REFRESH CYCLE 20

(WE = HIGH)



DON'T CARE

₩ UNDEFINED



DRAM MODULE

4 MEG x 32, 8 MEG x 16

FAST PAGE MODE

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 40mW standby; 2,200mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

- Multiple RAS lines allow x16 or x32 width
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle

• Timing	
60ns access	- 6
70ns access	· 7
80ns access	- 8
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G G

Part Number Example: MT8D432G-6

GENERAL DESCRIPTION

The MT8D432 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. \overline{RAS} is used to latch the first 11 bits and \overline{CAS} the latter 11 bits. A READ or WRITE cycle is selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{CAS} . Since \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-17)



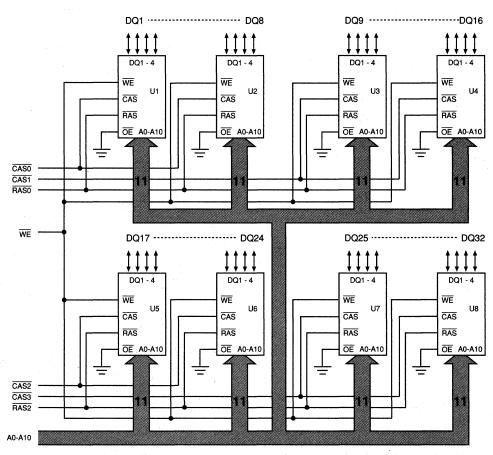
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO CASO	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	ÇAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

NEW **III** DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4A1DJ

TRUTH TABLE

			14.		ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	^t C	DQ1-DQ8
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Χ	X	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	8W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		• Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	RASO, RAS2	li1	-8	8	μΑ	
Any Input 0V ≤ VIN ≤ Vcc	A0-A10, WE	112	-16	16	μΑ	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	lıз	-4	4	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) for each package input	DQ1-DQ32	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4	1	V	
Output High Voltage (IouT = -5mA) Output Low Voltage (IouT = 5mA)		Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	16	16	16	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	8	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	960	800	680	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	640	560	480	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))	lcc5	960	800	680	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Icce	960	800	680	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C ₁₁		51	pF	2
Input Capacitance: WE	C ₁₂		67	pF	2
Input Capacitance: RAS0, RAS2	Сіз		34	pF	2
Input Capacitance: CASO, CAS1, CAS2, CAS3	C ₁₄		17	pF	2
Input/Output Capacitance: DQ1-DQ32	Сю		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	-
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	22
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	t _{AA}		30		35		40	ns	
Access time from CAS precharge	^t CPA		40		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20	1000000	ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	†CRP	5		5		5		ns	
Row address setup time	†ASR	0	1	0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0	1	ns	
Read command hold time (referenced to CAS)	[†] RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	^t CLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) (Vcc = 5V $\pm 10\%$)

AC CHARACTERISTICS		_	6		-7	-	8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	^t DH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	^t Τ	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	†REF		32		32		32	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	^t WTS	10		10	Mark Service	10		ns	24

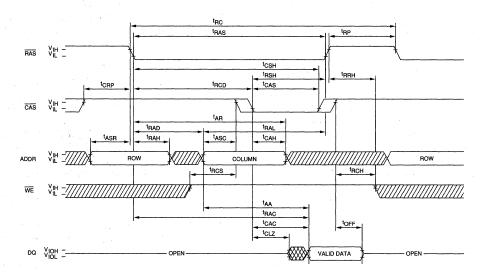


NOTES

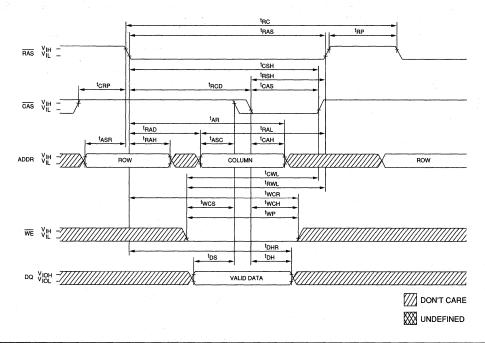
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ⁴OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 22. OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH
- 24. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.

READ CYCLE

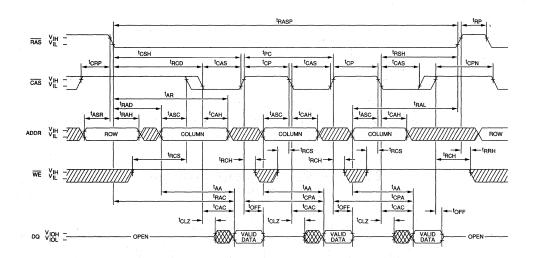


EARLY-WRITE CYCLE

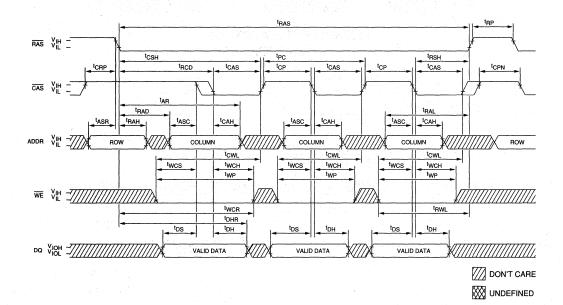


NEW DRAM MODULE

FAST-PAGE-MODE READ CYCLE



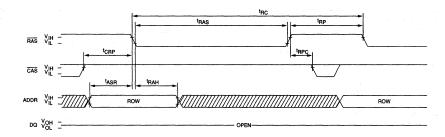
FAST-PAGE-MODE EARLY-WRITE CYCLE





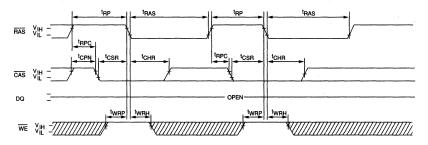
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; WE = DON'T CARE)

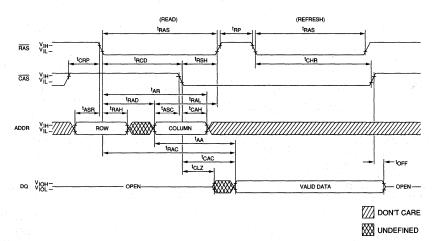


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23 (WE = HIGH)





DRAM MODULE

8 MEG x 32,16 MEG x 16 **FAST PAGE MODE**

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 80mW standby; 2,240mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x16 or x32 width

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM	G

Part Number Example: MT16D832G-6

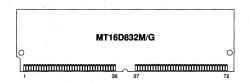
GENERAL DESCRIPTION

The MT16D832 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-18)

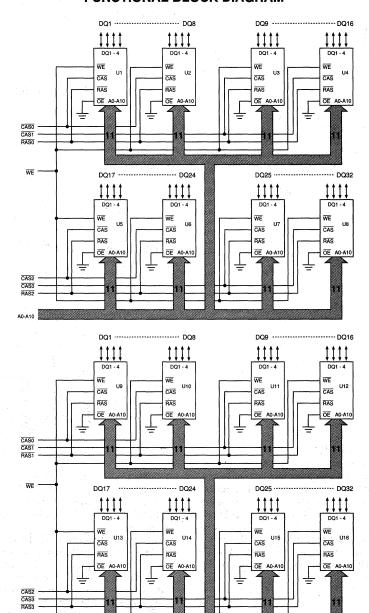


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	.71	NC
18	A6	36	NC	54	DQ27	72	Vss

followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4MA1DJ

TRUTH TABLE

		1.0			ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC .	DQ1-DQ32
Standby		Н	H→X	Х	X	Х	High-Z
READ		, L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L. L.	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	16W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT	RASO-RAS3	lii -	-8	8	μΑ	
Any Input 0V ≤ Vin ≤ Vcc	A0-A10, WE	l ₁₂	-32	32	μΑ	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	lıз	-8	8	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) for each package input	DQ1-DQ32	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 5mA)		Vol		0.4	V	

	MAX		l			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	32	32	32	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	16	16	16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	976	816	696	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	656	576	496	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: TRC = TRC (MIN))	lcc5	976	816	696	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹ RC = ¹ RC (MIN))	Icc6	976	816	696	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C ₁₁	-	102	pF	2
Input Capacitance: WE	C ₁₂		134	pF	2
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз	_	34	pF	2
Input Capacitance: CAS0, CAS1, CAS2, CAS3	CI4		34	pF	2
Input/Output Capacitance: DQ1-DQ32	Сю		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	100	-7		-8		3 N N
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	and the first
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	22
Access time from RAS	†RAC		60		70		80	ns	14
Access time from CAS	†CAC		15		20		20	ns	15
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		40		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	1.
RAS hold time	tRSH	15		20		20	1 1 1 1 1 1 1 1 1 1	ns	1,111
RAS precharge time	tRP	40		50	1 2 2 2 2	60		ns	44.14, 44.
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70	1 4 4	80		ns	1,54
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0	1 2 2 7	0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

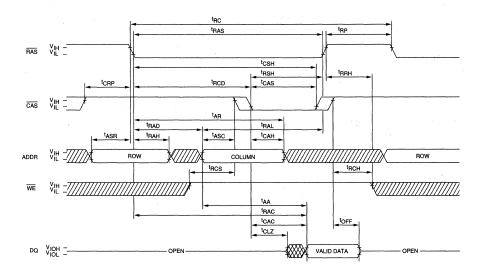
AC CHARACTERISTICS		-	6		-7		8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	20
WE command setup time	twcs	0		0		0		ns	
Write command hold time	†WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	†DHR	45		55		60		ns	
Transition time (rise or fall)	^t T	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	tREF		32		32		32	ms	
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	5		5		5		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	₩TH	10		10		10		ns	24
WE setup time (WCBR test cycle)	†WTS	10		10		10		ns	24

NOTES

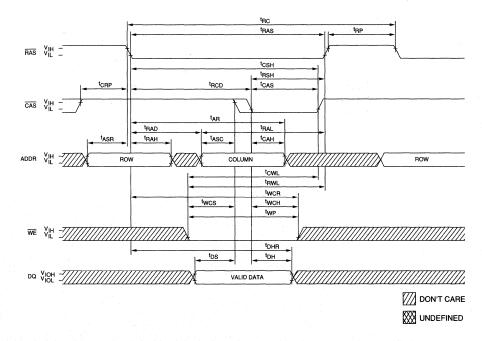
- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If \overline{CAS} = VIH, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

- 15. Assumes that ^tRCD ≥ ^tRCD (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 22. OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 24. ^tWTS and ^tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.

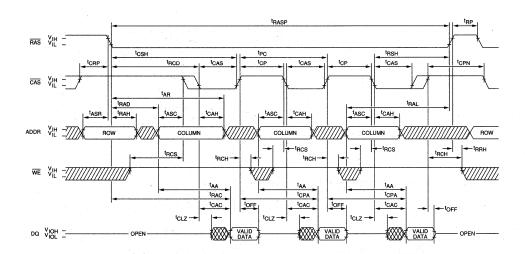
READ CYCLE



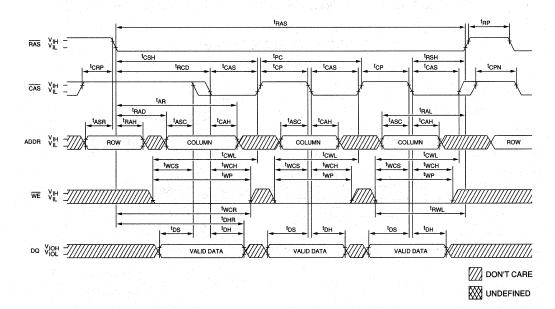
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

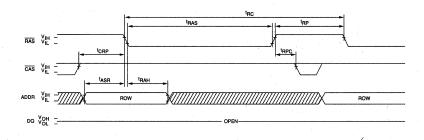


FAST-PAGE-MODE EARLY-WRITE CYCLE



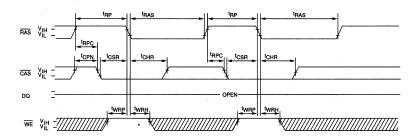


RAS-ONLY REFRESH CYCLE (ADDR = A0-A10; WE = DON'T CARE)



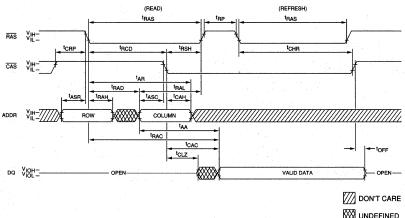
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE 23

 $(\overline{WE} = HIGH)$





DRAM MODULE

256K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common RAS control pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 1,575mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle

OPTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Part Number Example: MT9D)25636G-6

GENERAL DESCRIPTION

The MT9D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-11)

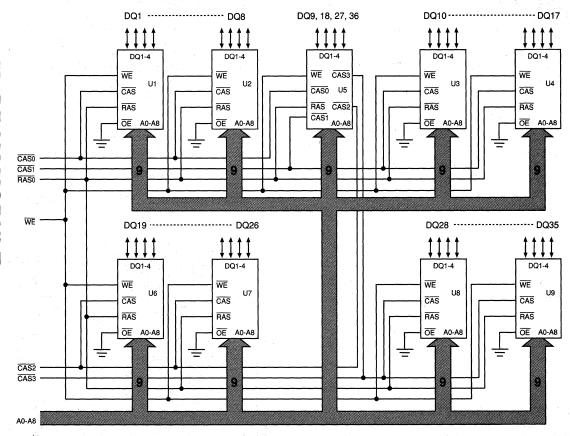
MT9D25636M/G

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC .	64	DQ35
.11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS0	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4256DJ U5 = MT4C4259DJ

NOTE: Due to the use of a Quad \overline{CAS} parity DRAM, \overline{RASO} is common to all devices.



TRUTH TABLE

			apariti de la compansión de la compansió		ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tc	DQ1-DQ36
Standby		Н,	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		A A L	Н	Χ	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	9W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6, 23) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1	
INPUT LEAKAGE CURRENT	CASO-CAS3	lı1	-6	6	μА	
Any Input 0V ≤ Vin ≤ Vcc	A0-A8, WE	lı2	-18	18	μΑ	
(All other pins not under test = 0V) For each package input	RAS0	lıз	-18	18	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) For each package input	DQ1-DQ36	loz	-10	10	μA	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Iout = -5mA)				-		1
Output Low Voltage (lout = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	18	18	18	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	lcc2	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	810	720	630	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	630	540	450	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	810	720	630	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	810	720	630	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C ₁₁		58	pF	17
Input Capacitance: WE	C ₁₂		76	pF	17
Input Capacitance: RASO	Сіз		76	pF	17
Input Capacitance: CAS0, CAS1, CAS2, CAS3	C ₁₄		25	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130	1 3	150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	tRAC		60		70	-	80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE		20		20	,	20	ns	5.5 S. T. N.
Access time from column address	tAA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	71. F. 37.0
RAS pulse width	†RAS	60	100,000	.70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18,22
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	24
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	15		15	14.	15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	^t REF		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	. 10		10		10	1 1	ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	19
Last CAS going LOW to first CAS to return HIGH	tCLCH	10		10		10		ns	22

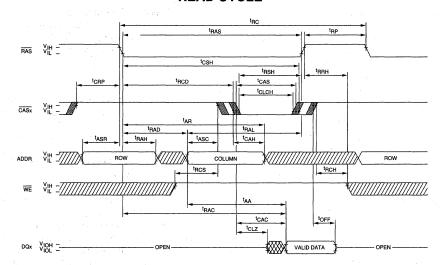


NOTES

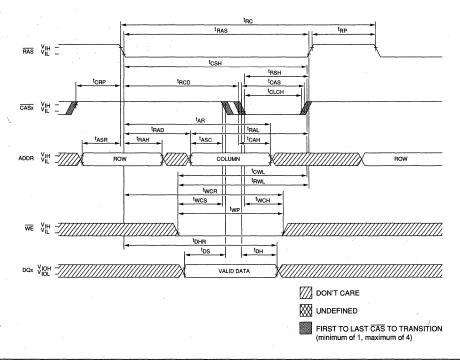
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 4. AC characteristics assume ${}^{t}T = 5ns$.
- 5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VII. (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U9.
- 22. Last falling \overline{CASx} edge to first rising \overline{CASx} edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

READ CYCLE

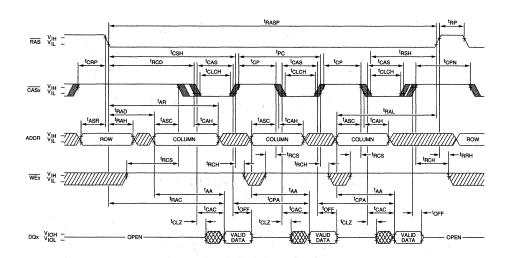


EARLY-WRITE CYCLE

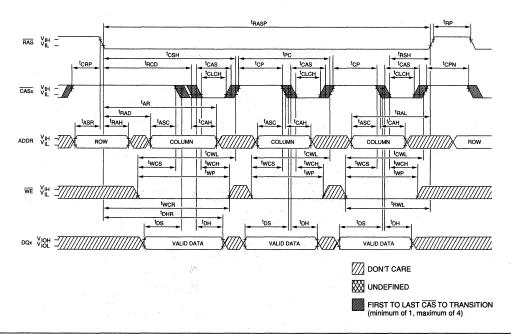




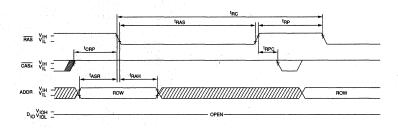
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

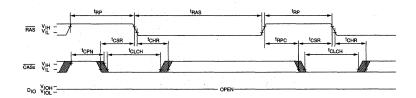


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



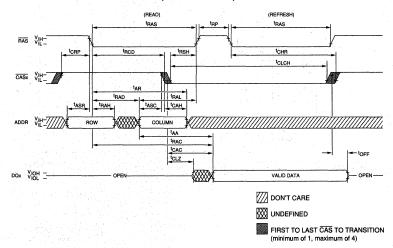
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, WE = DON'T CARE)



HIDDEN REFRESH CYCLE 20

 $(\overline{WE} = HIGH)$





DRAM MODULE

256K x 36, 512K x 18

FAST PAGE MODE

FEATURES

OPTIONS

Timing

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW standby; 1,750mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

MT10D25636G-6

- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 width

	60ns access			- 6	
	70ns access			- 7	
	80ns access			- 8	
•	Packages				
	Leadless 72-pin S	SIMM		M	
	Leadless 72-pin S		old)	G	

GENERAL DESCRIPTION

• Part Number Example:

The MT10D25636 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-13)

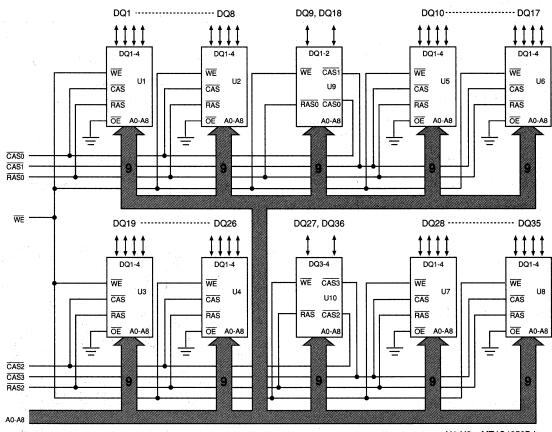
MT10D25636M/G

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3 .	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4256DJ U9, U10 = MT4C4259DJ



TRUTH TABLE

					ADDRESSES		DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC .	DQ1-DQ36
Standby		Н	H→X	Х	X	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	Н	ROW	COL	Data Out
READ	2nd Cycle	L L	H→L→H	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	X	Х	Χ	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss.	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	10W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) ($0^{\circ}C \le T_A \le 70^{\circ}C$; Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs		≠ ViL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CAS0-CAS3	l ₁₁	-6	6	μА	
Any Input 0V ≤ Vin ≤ Vcc	A0-A8, WE	112	-20	20	μΑ	
(All other pins not under test = 0V) for each package input	RASO, RAS2	lıз	-10	10	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ36	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iouт = -5mA) Output Low Voltage (Iouт = 5mA)		Vol		0.4	V	-

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(\overline{RAS} = \overline{CAS} = VIH)$	lcc1	20	20	20	mA	
STANDBY CURRENT: (CMOS)	lcc2	10	10	10	mA	
$\overline{(RAS)} = \overline{CAS} = Vcc -0.2V$						
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	900	800	700	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	700	600	500	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V _{IH} : ^t RC = ^t RC (MIN))	lcc5	900	800	700	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	900	800	700	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cıı		64	pF	17
Input Capacitance: WE	C ₁₂		84	pF	17
Input Capacitance: RASO, RAS2	Сіз		42	pF	17
Input Capacitance: CASO, CAS1, CAS2, CAS3	C14		25	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	-6		-7		-8			18614	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	The second
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC		60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE	1 (2)	20		20		20	ns	TARY TO
Access time from column address	^t AA		30		35		40	ns	1
Access time from CAS precharge	†CPA		35		40	1.	45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	5	- 1 - 1 - 12	5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	†RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	25
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15	100	15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-	6		-7		8	l .	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	†WCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH.	15		15		15		ns	. 15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	ŀΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF.		8		8		8	ms	
RAS to CAS precharge time	tRPC	. 0		0	,	0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15	. 43	15		ns	19
Last CAS going LOW to First CAS to return HIGH	[†] CLCH	10	1.41	10		10		ns	

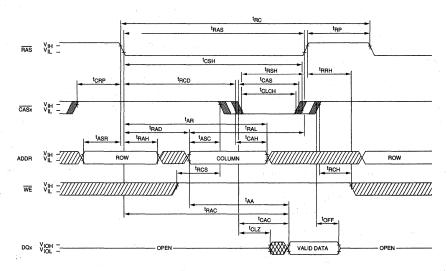


NOTES

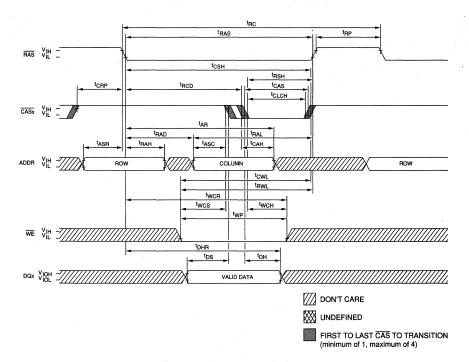
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1-U9.
- 22. Last falling CASx edge to first rising CASx edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

READ CYCLE

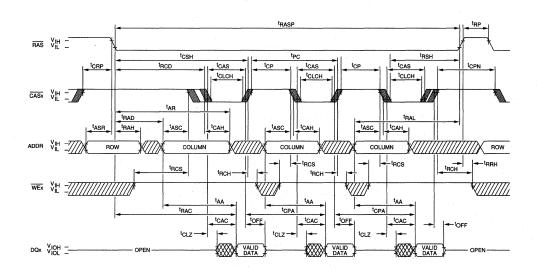


EARLY-WRITE CYCLE

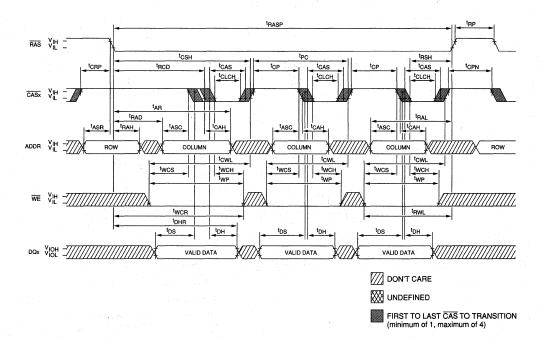




FAST-PAGE-MODE READ CYCLE

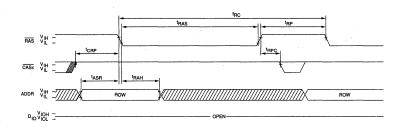


FAST-PAGE-MODE EARLY-WRITE CYCLE



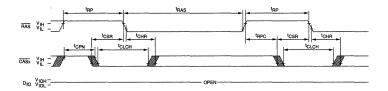


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)

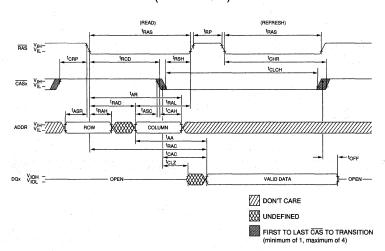


CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A8, \overline{WE} = DON'T CARE)$



HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

1 MEG x 18 DRAM

FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 18mW standby; 1,250mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS

MARKING

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8

 Packages Leadless 72-pin SIMM M Leadless 72-pin SIMM (Gold)

Part Number Example: MT6D118G-6

GENERAL DESCRIPTION

The MT6D118 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x18 configuration. During READ or WRITE cycles, each bit is uniquely $addressed\,through\,the\,20\,address\,bits, which are\,entered\,10$ bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View)

72-Pin SIMM (T-16)

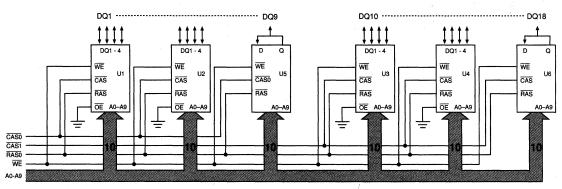


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	NC	56	NC
3	NC	21	NC	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	NC
5	NC	23	NC	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	NC
7	NC	25	NC	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	NC
9	NC	27	NC	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	NC
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	NC	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	NC	52	NC	70	PRD4
17	A5	35	NC	53	DQ12	71	NC
18	A6	36	DQ9	54	NC	72	Vss

followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR refresh cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT4C4001JDJ U5-U6 = MT4C1024DJ

TRUTH TABLE

					ADDRI	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC	DQ1-DQ18
Standby		Н	H→X	Х	Х	Χ	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	X	Χ	High-Z

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	X	Х	Х
PRD2	Х	Х	Х
PRD3	Х	Х	Х
PRD4	Х	Х	Х

X = "don't care"



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	6W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 25) (0° C $\leq T_{A} \leq 70^{\circ}$ C; Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ Vin ≤ Vcc	A0-A9, WE, RASO,	lit	-12	12	μА	
(All other pins not under test = 0V) for each package input	CAS0, CAS1	l ₁₂	-6	6	μΑ	<u> </u>
OUTPUT LEAKAGE CURRENT (Q is disabled, $0V \le Vout \le Vcc$) for each package input	DQ1-DQ18	loz	-10	10	μА	1 1 1 2 2 2 2 1
OUTPUT LEVELS Output High Voltage (lout = -5mA)		Vон	2.4		V	
Output Low Voltage (IOUT = 5mA)		Vol	1. 1.	0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	12	12	12	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc2	6	6	6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	620	560	500	mA	2, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: †PC = †PC (MIN))	lcc4	450	390	330	mA	2, 25
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: tRC = tRC (MIN))	lcc5	620	560	500	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icce	620	560	500	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Ci1		38	pF	17
Input Capacitance: WE	Cı2		50	pF	17
Input Capacitance: RAS0	Сіз		50	pF	17
Input Capacitance: CASO, CAS1	Cı4		25	pF	17
Input/Output Capacitance: DQ1-DQ18	Сю		15	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 9, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7	-	8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
FAST PAGE MODE cycle time	^t PC	40		40		45		ns	
Access time from RAS	^t RAC	60			70		80	ns	
Access time from CAS	^t CAC	15			20		20	ns	
Access time from column address	^t AA	30			30		35	ns	
Access time from CAS precharge	^t CPA	35	4		35		40	ns	
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	^t RSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	^t RCD	20	40	20	50	20	60	ns	13
CAS to RAS setup time	^t CRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	1.5
RAS to column	tRAD	15	30	15	30	15	35	ns	23
address delay time		:							
Row address hold time	^t RAH	.10		10		10		ns	
Column address setup time	tASC	0		0		0		ns	1. 1. 1.
Column address hold time	^t CAH	10		15		15		ns	
Column address to RAS lead time	^t RAL	30		30		35		ns	
Column address hold time referenced to RAS	^t AR	50		55		60		ns	
Read command setup time	tRCS	0		0		0		ns	1.0
Read command hold time referenced to CAS	^t RCH	0		0		0		ns	14
CAS to output in Low-Z	^t CLZ	0		0		0		ns	
Read command hold time referenced to RAS	^t RRH	0		0		0		ns	14
Output buffer turn-off delay	^t OFF	0 -	15	0	20	0 :	20	ns	12
WE command setup time	twcs	0		0		0		ns	raja dijela



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 9, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

A.C. CHARACTERISTICS			6		-7	· ·	8	1.0	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	^t WCR	45		55	1 4 5 5 5 5 6 5 6 5 6 5 6 5 6 5 6 6 6 6 6	60		ns	
Write command pulse width	†WP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20	7	ns	30 30 50
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	^t DH	10		15		15		ns	15
Data-in hold time referenced to RAS	^t DHR	45		55		60		ns	
Transition time (rise or fall)	t _T	3	50	3	50	3	50	ns	5, 16
Refresh period (1024 cycles)	†REF		16		16		16	ms	
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	15		15		15		ns	19
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		10		ns	19
RAS to CAS precharge time	^t RPC	0		0		0		ns	
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	10		10		10		ns	22
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10	A 4500 1	ns	22
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	22
WE setup time (WCBR test cycle)	tWTS	10		10	red at fact	10		ns	22



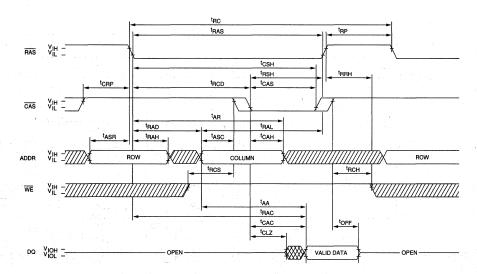
NOTES

- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR withWE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 4. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 12. [†]OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.

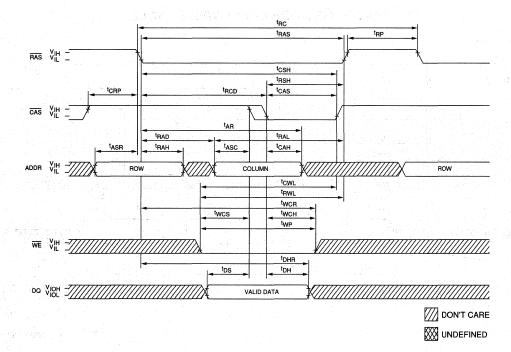
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for CP.
- 19. On-chip refresh and address counters are enabled.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on all 4 Meg DRAMs.
- 22. WTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.
- 23. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 24. All other inputs at Vcc -0.2V.
- Icc is dependent on cycle rates.



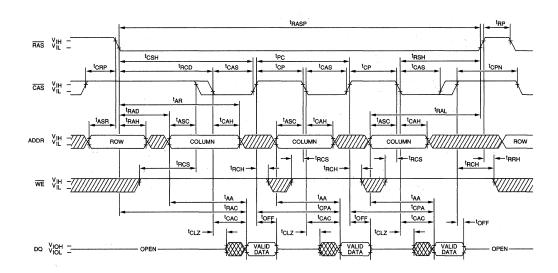
READ CYCLE



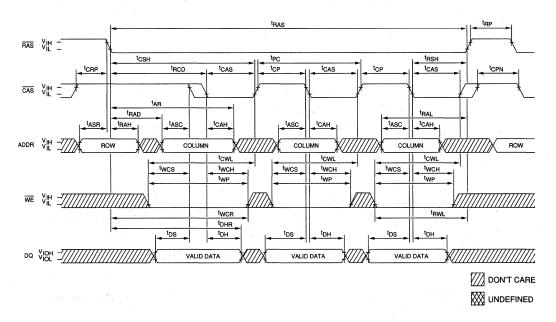
EARLY-WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

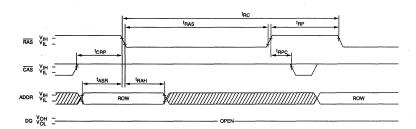


FAST-PAGE-MODE EARLY-WRITE CYCLE



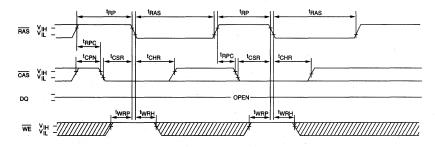


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)

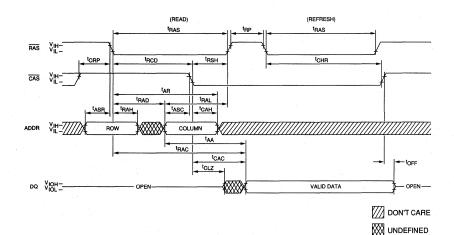


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE 20 (WE = HIGH)





DRAM MODULE

512K x 36 DRAM

FAST PAGE MODE

FEATURES

- Common RAS control per side pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 54mW standby; 1,602mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle

OPTIONS		\mathbf{M}_{I}	ARKI	NG
 Timing 				
60ns access			- 6	
70ns access			- 7	
80ns access			- 8	
• Paglagga				

Packages
 Leadless 72-pin SIMM
 M
 Leadless 72-pin SIMM (Gold)
 G

Part Number Example: MT18D51236G-6

GENERAL DESCRIPTION

The MT18D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0 -A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-12)

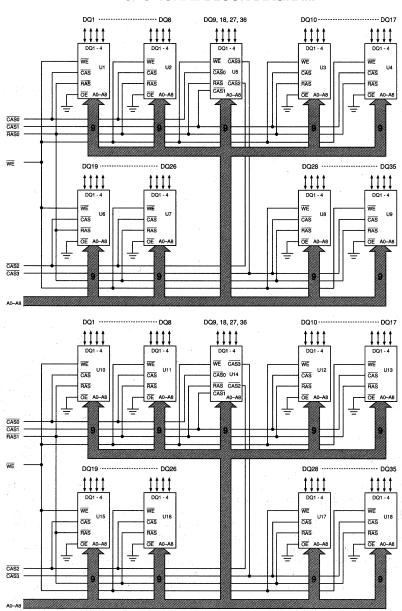


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CASO	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11:	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	50	DQ28	68	PRD2
15	A3	33	RAS1	51	DQ11	69	PRD3
16	A4	34	RAS0	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U13, U15-U18 = MT4C4256DJ U5, U14 = MT4C4259DJ

NOTE: Due to the use of a Quad \overline{CAS} parity DRAM, $\overline{RAS0}$ is common to side 1 and $\overline{RAS1}$ is common to side 2.



TRUTH TABLE

		1 24			ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC.	DQ1-DQ36
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		Ļ	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	19 L 13	H→L→H	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	, H : 1	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L L	H→L→H	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L L	H-A-A	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CASO-CAS3	lii .	-12	12	μΑ	
Any Input 0V ≤ VIN ≤ Vcc	A0-A8, WE	lı2	-36	36	μΑ	
(All other pins not under test = 0V) For each package input	RAS0, RAS1	lıз	-18	18	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) For each package input	DQ1-DQ36	loz	-20	20	μΑ	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iouт = -5mA) Output Low Voltage (Iouт = 5mA)		Vol		0.4	V	

	Leave to the		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc1	36	36	36	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	18	18	18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	828	738	648	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	648	558	468	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: [†] RC = [†] RC (MIN))	lcc5	828	738	648	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	828	738	648	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cıı		115	pF	17
Input Capacitance: WE	C ₁₂	4.0	151	pF	17
Input Capacitance: RASO, RAS1	Сіз		76	pF	17
Input Capacitance: CASO, CAS1, CAS2, CAS3	C ₁₄		50	pF	17
Input/Output Capacitance: DQ1-DQ36	Cio		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq $T_A \leq$ 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	tRAC		60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE		20	V. F. (195	20		20	ns	
Access time from column address	^t AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20	100	20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	. :
CAS hold time	^t CSH	60		70		80		ns	100
CAS precharge time	^t CPN	10		. 10		10		ns	18, 22
CAS precharge time (FAST PAGE MODE)	^t CP	10		10	14.10	10		ns	
RAS to CAS delay time	†RCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5	1.14) 1.14	5		ns	
Row address setup time	†ASR	0		0	1 - 7 - 1 - 1	0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	24
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS	-6 -7		-	8					
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	. 20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15	y 652.1	ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP.	10		15		15		ns	3.34
Write command to RAS lead time	t _{RWL}	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	t _{DS}	0		0		0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	^t T	3	50	3	50	. 3	50	ns	5, 16
Refresh period (512 cycles)	tREF		- 8		8		8	ms	1. 1. 1.
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	†CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	19
Last CAS going LOW to First CAS to return HIGH	[†] CLCH	10		10		10		ns	

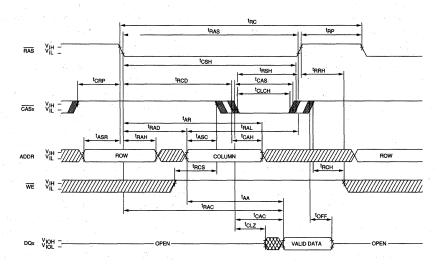


NOTES

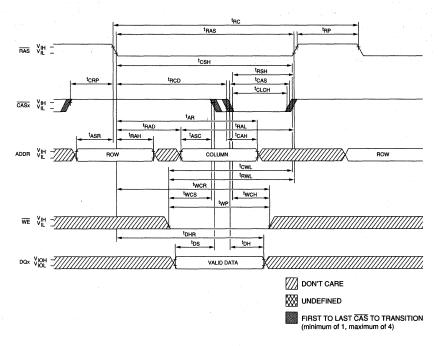
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U18.
- 22. Last falling \overline{CASx} edge to first rising \overline{CASx} edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

READ CYCLÉ

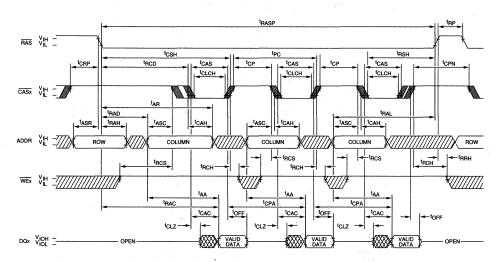


EARLY-WRITE CYCLE

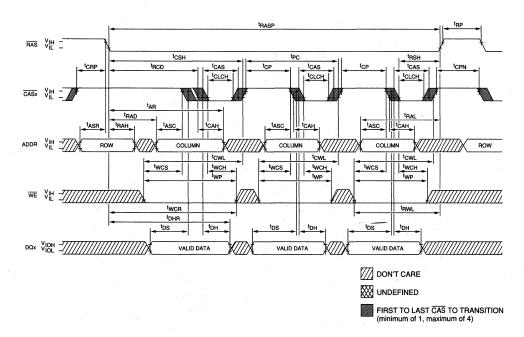




FAST-PAGE-MODE READ CYCLE

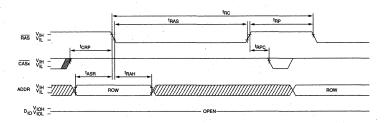


FAST-PAGE-MODE EARLY-WRITE CYCLE



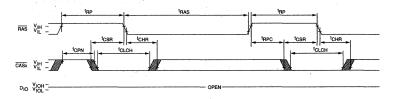
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; WE = DON'T CARE)



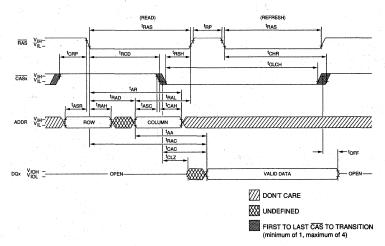
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, WE = DON'T CARE)



HIDDEN REFRESH CYCLE 20

 $\overline{(WE = HIGH)}$





DRAM MODULE

512K x 36, 1 MEG x 18 FAST PAGE MODE

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW standby; 1,780mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

M

- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x16 or x32 width

OPTIONS	MARKING
 Timing 	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	

• Part Number Example: MT20D51236G-6

GENERAL DESCRIPTION

Leadless 72-pin SIMM

Leadless 72-pin SIMM (Gold)

The MT20D51236 is a randomly accessed solid-state memory containing 524,288 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-14)

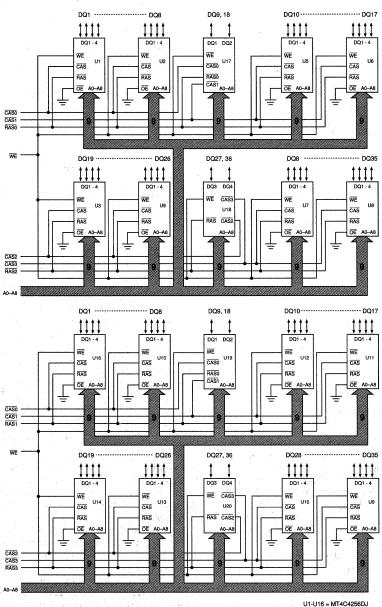


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CASO	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10.	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	AO	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	NC	- 50	DQ28	68	PRD2
15	A3	33	RAS3	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM





TRUTH TABLE

the state of the s					ADDRI	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC t	DQ1-DQ36
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L→H	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L→H	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L→H	Ĺ	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L→H	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Х	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) ($0^{\circ}C \le T_A \le 70^{\circ}C$; Vcc = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		Vih	2.4	Vcc+1	٧	1.
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT	RAS0-RAS3	lı1	-10	10	μΑ	
Any Input 0V ≤ VIN ≤ Vcc	A0-A8, WE	l ₁₂	-40	40	μΑ	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	lıз	-12	12	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ36	loz	-20	20	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Io∪τ = -5mA) Output Low Voltage (Io∪τ = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) $(RAS = \overline{CAS} = Vih)$	lcc1	40	40	40	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	20	20	20	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	Іссз	920	820	720	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN)) Average power supply current	lcc4	720	620	520	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	920	820	720	mA	2
REFRESH CURRENT: CAS -BEFORE- RAS Average power supply current (RAS , CAS , Address Cycling: ^t RC = ^t RC (MIN))	Icc6	920	820	720	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cıı		128	pF	17
Input Capacitance: WE	C ₁₂		168	pF	17
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз		42	pF	17
Input Capacitance: CAS0, CAS1, CAS2, CAS3	C14		50	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	A
READ-WRITE cycle time	tRWC	n/a		n/a	50 1	n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC		60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	^t OE		20		20		20	ns	4 000
Access time from column address	†AA		30	7.10	35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	^t CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70	1	80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18, 22
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	1.00
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5		5	100	ns	
Row address setup time	tASR .	0		0	1000	0		ns	19 1
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	24
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40	1	ns	
Read command setup time	tRCS	0	44	0		0		ns	N 1
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_{A} \leq 70°C; Vcc = 5V $\pm 10\%$)

AC CHARACTERISTICS	-6		-	7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0	+ 4.	0		ns	15
Data-in hold time	tDH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	^t T	3	50	3	50	. 3	50	ns	5, 16
Refresh period (512 cycles)	tREF.		8		8		8	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	19
Last CAS going LOW to First CAS to return HIGH	tCLCH	10		10		10		ns	22

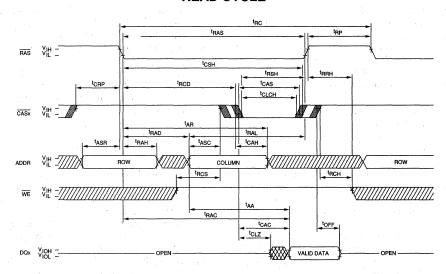


NOTES

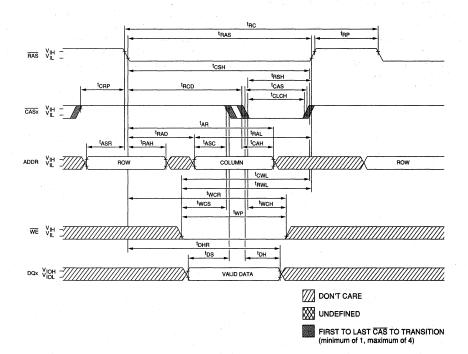
- 1. All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If CAS = Vπ, data output may contain data from the last valid READ cycle.
- *OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for CP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = 1.0W$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U18.
- 22. Last falling CASx edge to first rising CASx edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

READ CYCLE

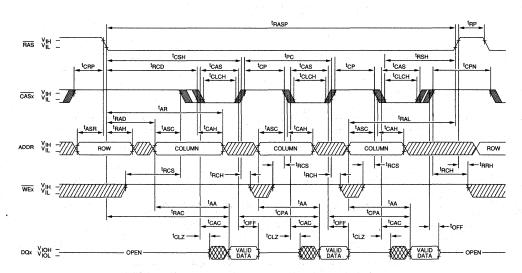


EARLY-WRITE CYCLE

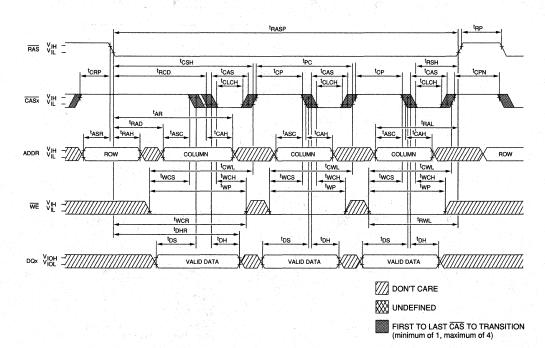




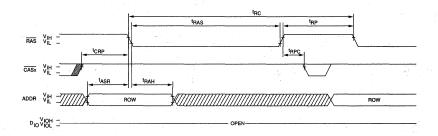
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

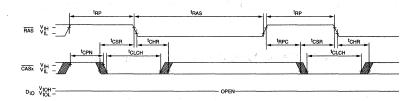


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



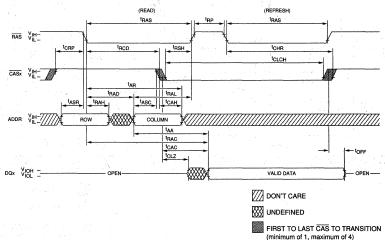
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, WE = DON'T CARE)



HIDDEN REFRESH CYCLE 20

 $\overline{(WE = HIGH)}$





DRAM MODULE

1 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

- Common RAS control pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 27mW standby; 2,175mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS	MARKING
• Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
 Packages 	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Go	ld) G

Part Number Example: MT9D136G-6

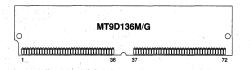
GENERAL DESCRIPTION

The MT9D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are elected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE node. During a WRITE cycle, data-in (D) is latched by the alling edge of \overline{WE} or \overline{CAS} , whichever occurs last. If \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) emain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operaions (READ or WRITE) within a row-address (A0-A9) lefined page boundary. The FAST PAGE MODE cycle is llways initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-11)

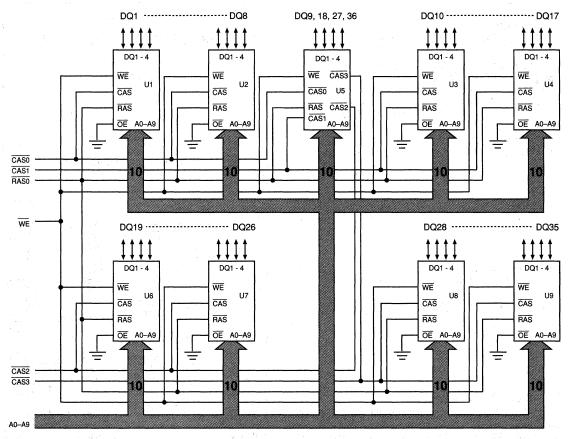


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS0	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U9 = MT4C4001JDJ U5 = MT4C4004JDJ

Due to the use of a Quad CAS DRAM, RASO is common to all devices.



TRUTH TABLE

					ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC	DQ1-DQ36
Standby		Н	H→X	Х	Х	Χ	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	EFRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CASO-CAS3	lı1	-6	6	μΑ	
Any Input 0V ≤ VIN ≤ Vcc	A0-A8, WE,	112	-18	18	μA	
(All other pins not under test = 0V) For each package input	RAS0					
OUTPUT LEAKAGE CURRENT	DQ1-DQ36	loz	-10	10	μA	
(Q is disabled, $0V \le V_{OUT} \le V_{CC}$) For each package input						
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iout = -5mA)				-		1
Output Low Voltage (louт = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	18	18	18	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	9	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	990	900	810	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	720	630	540	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	990	900	810	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	990	900	810	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	CI1		58	pF	17
Input Capacitance: WE	C ₁₂		76	pF	17
Input Capacitance: RAS0	Сіз		76	pF	17
Input Capacitance: CASO, CAS1, CAS2, CAS3	C ₁₄		25	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-	-6 -7			-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130	100	150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40	4 7	45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC	1.21	60		70		80	ns	8
Access time from CAS	^t CAC		15		20		20	ns	9
Output Enable	^t OE		15	1.7	20		20	ns	
Access time from column address	†AA		30		35		40	ns	and a second
Access time from CAS precharge	^t CPA		35		40	1	45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	1, 3,445
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	19
CAS hold time	^t CSH	60		70		80		ns	88
CAS precharge time	^t CPN	10		10		10		ns	18, 22
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	100	ns	11.4
RAS to CAS delay time	†RCD	20	45	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	tASR	0	1	0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	24
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	†RCS	0		0	1 2 2	0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	[†] RRH	0		0		0		ns	14



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

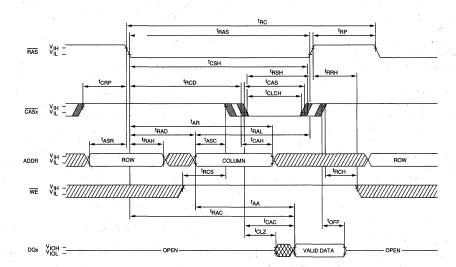
AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	0	20	ns	12
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45	ar, m	55	· · · · · · · · ·	60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	1.0
Data-in setup time	tDS .	0		0		0		ns	15
Data-in hold time	^t DH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45	-	55		60		ns	
Transition time (rise or fall)	t T	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	†REF		16		16		16	ms	
RAS to CAS precharge time	†RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	†WRH	10		10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	
WE hold time (WCBR test cycle)	tWTH	10		10		10		ns	
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	
Last CAS going LOW to First CAS to return HIGH	tCLCH	10		10		10		ns	22



NOTES

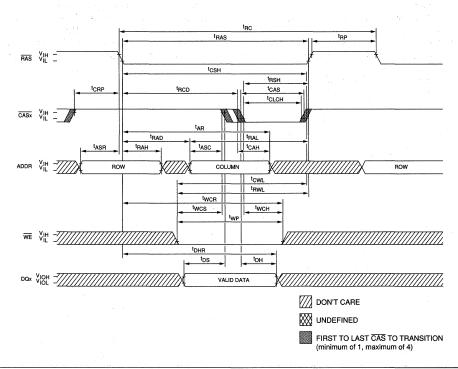
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR withWE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U9.
- 22. Last falling CASx edge to first rising CASx edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the [†]RAD (MAX) limit ensures that [†]RCD (MAX) can be met. [†]RAD (MAX) is specified as a reference point only; if [†]RAD is greater than the specified [†]RAD (MAX) limit, then access time is controlled exclusively by [†]AA.



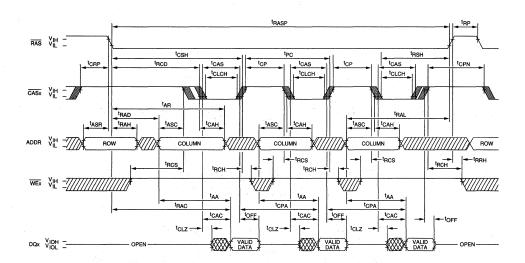
READ CYCLE

EARLY-WRITE CYCLE

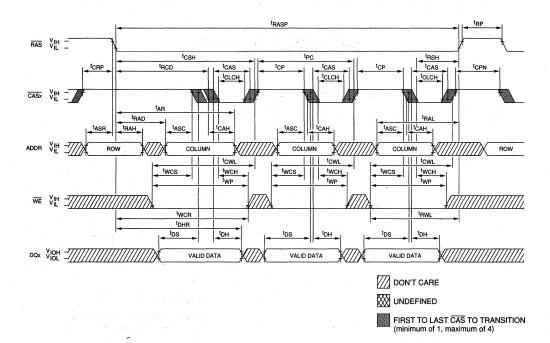




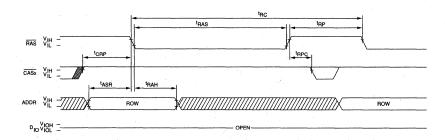
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

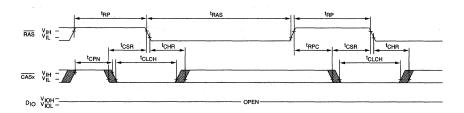


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



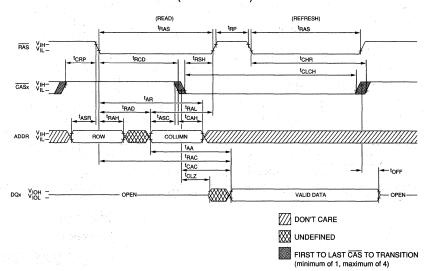
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE 20

(WE = HIGH)





DRAM MODULE

1 MEG x 36, 2 MEG x 18

FAST PAGE MODE (MT12D136) LOW POWER. EXTENDED REFRESH (MT12D136 L)

FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 36mW (9.2mW L-version) standby; 2,500mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE access cycle
- Low CMOS standby current, 2.4mA maximum (L-version)
- Multiple RAS lines allow x18 or x36 width

OPTIONS MARKING Timing 60ns access - 6 70ns access - 7 80ns access - 8 Packages

Leadless 72-pin SIMM M Leadless 72-pin SIMM (Gold) C Power/Refresh Normal Power/16ms Blank

• Part Number Example: MT12D136GL-6

GENERAL DESCRIPTION

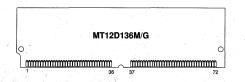
Low Power/128ms

The MT12D136 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-19)

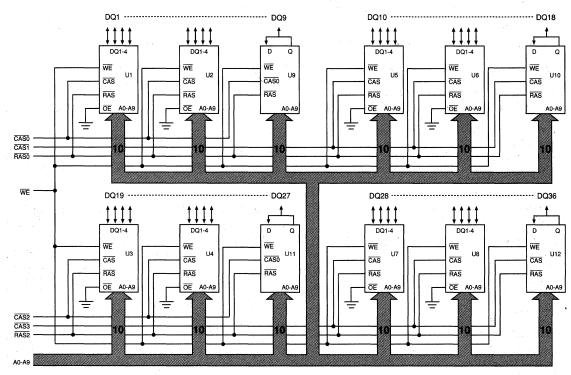


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	-71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4001JDJ U9-U12 = MT4C1024DJ

U1-U8 = MT4C4001JDJ L (L-version) U9-U12 = MT4C1024DJ L (L-version)



TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	tR t	tC .	DQ1-DQ36
Standby	- A	Н	H→X	Х	X	Х	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L 	X	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC .
PRD4	NC	NC	Vss

1 MEG x 36, 2 MEG x 18 DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss-1V to +7V Operating Temperature, TA (Ambient) 0°C to +70°C Storage Temperature (Plastic)-55°C to +150°C Power Dissipation12W Short Circuit Output Current50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION	The state of the s	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CASO-CAS3	lı1	-6	6	μΑ	
Any Input 0V ≤ Vin ≤ Vcc	A0-A9, WE	lı2	-24	24	μΑ	
(All other pins not under test = 0V) for each package input	RASO, RAS2	lıз	-12	12	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ36	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 5mA)		Vol		0.4	v	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	24	24	24	mA	
STANDBY CURRENT: (CMOS)	lcc2	12	12	12	mA	
$(\overline{RAS} = \overline{CAS} = Vcc - 0.2V)$		2.4	2.4	2.4	mA	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	Іссз	1240	1120	1000	mA	2, 22
(RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))		1220	1100	980	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE		920	800	680	mA	2, 22
Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	900	780	660	mA	2,22,24
REFRESH CURRENT: RAS-ONLY	1-1-	1240	1120	1000	mA	2
Average power supply current (RAS Cycling, CAS = V _{IH} : ^t RC = ^t RC (MIN))	lcc5	1220	1100	980	mA	2, 24
REFRESH CURRENT: CAS-BEFORE-RAS		1240	1120	1000	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	1220	1100	980	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 300ns; WE = Vcc -0.2; A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open), tRC = 125µs (1,024 rows at 125µs = 128ms)	lcc7	3.2	3.2	3.2	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cii		77	pF	17
Input Capacitance: WE	C ₁₂	n sáná.	101	pF	17
Input Capacitance: RASO, RAS2	Сіз		50	pF	17
Input Capacitance: CASO, CAS1, CAS2, CAS3	CI4		25	pF	17
Input/Output Capacitance: DQ1-DQ36	Cio	14	10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($0^{\circ}C \le T_A \le 70^{\circ}C$; $Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		1.3	-6	1	-7	10	-8	117 44 1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110	1	130		150		ns	
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40	, 11, 12. pri 1, 18	40		45	. See a	ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC	- 1	60		70	West of the	80	ns	8
Access time from CAS	tCAC		15		20		20	ns	9
Output Enable	^t OE		15		20		20	ns	
Access time from column address	t _{AA}		30		35		40	ns	Language Control
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	esta gradica e e
RAS hold time	tRSH	15		20		20	1.6%	ns	
RAS precharge time	tRP	40		50	1 1 1 1	60		ns	r Say I di
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	19.00
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	23
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	†RCS	0	0.1	0		0		ns	
Read command hold time (referenced to CAS)	[†] RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	[†] RRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq $T_A \leq$ 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-6		7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	twcs	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55	() (m)	60		ns	
Write command pulse width	tWP	10		15		15		ns	.51
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	t _{DS}	0		0		0		ns	15
Data-in hold time	tDH t	10		15		15		ns	15
Data-in hold time (referenced to RAS)	¹DHR	45		55		60		ns	
Transition time (rise or fall)	tΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	†REF		16/128		16/128		16/128	ms	3/24
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	
WE hold time (WCBR test cycle)	^t WTH	10		10	100 100 100	10		ns	
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	

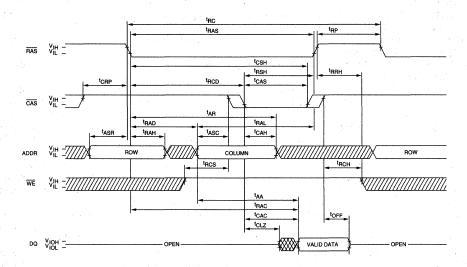


NOTES

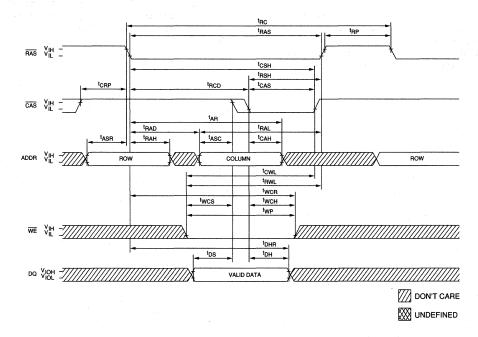
- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device. operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- 5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. Measured with a load equivalent to two TTL gates and 100pF.
- 8. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on all 4 Meg DRAMs.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 24. Applies to L-version only.

READ CYCLE

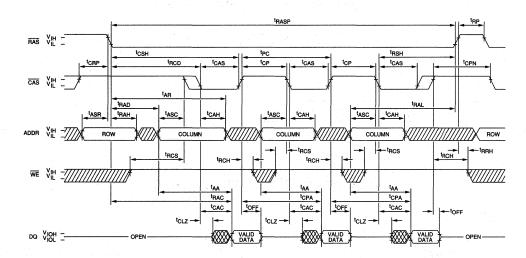


EARLY-WRITE CYCLE

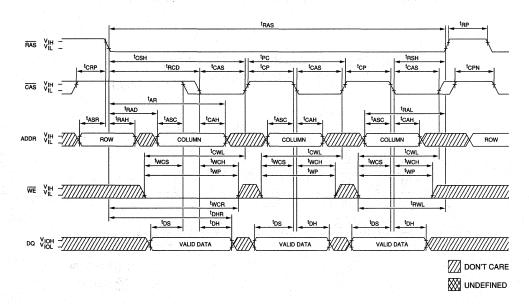




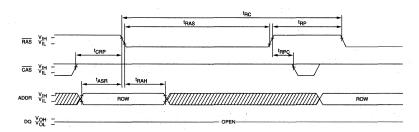
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

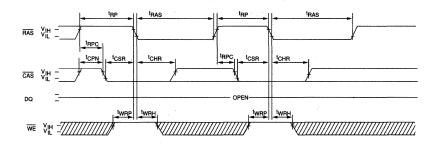


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



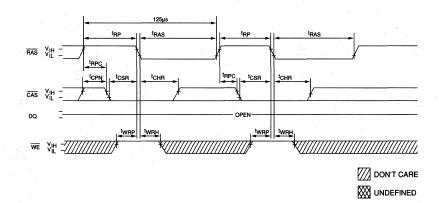
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



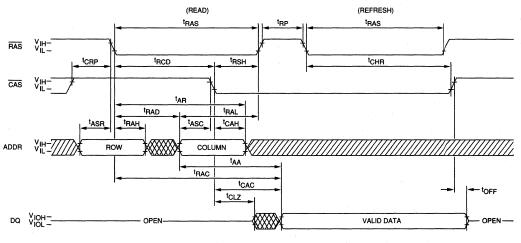
BATTERY BACKUP REFRESH CYCLE 24

(A0-A9 = DON'T CARE)





HIDDEN REFRESH CYCLE 20 (WE = HIGH)



DON'T CARE

₩ undefined



DRAM **MODULE**

2 MEG x 36 DRAM

FAST PAGE MODE

FEATURES

- Common RAS control per side pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 54mW standby; 2,052mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE access cycle

OPTIONS		MARKIN	10
 Timing 			
60ns access		- 6	
70ns access		- 7	
80ns access		- 8	
 Packages 			
Leadless 72-pin	SIMM	M	
Leadless 72-pin) G	
•			

Part Number Example: MT18D236G-6

GENERAL DESCRIPTION

The MT18D236 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-12)

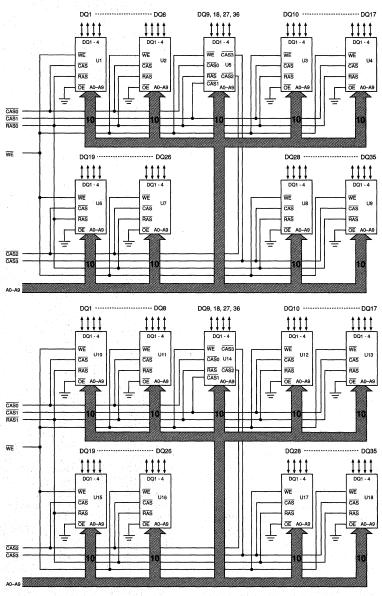
MT18D236M/G

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	RAS1	51	DQ11	69	PRD3
16	A4	34	RAS0	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U4, U6-U13, U15-U18 = MT4C4001JDJ U5, U14 = MT4C4004JDJ

Due to the use of a Quad CAS parity DRAM, RAS0 is common to side 1 and RAS1 is common to side 2.



TRUTH TABLE

					ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC	DQ1-DQ36
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	.:. L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	X	High-Z

PRESENCE DETECT

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SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

1V to +7V
0°C to +70°C
55°C to +125°C
18W
50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 23) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	. 1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	CAS0-CAS3	ln	-12	12	μΑ	
Any Input: 0V ≤ Vin ≤ Vcc	A0-A9, WE	l ₁₂	-36	36	μΑ	
(All other pins not under test = 0V) For each package input	RASO, RAS1	lıз	-18	18	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) For each package input	DQ1-DQ36	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 5mA)		Vol		0.4	ν	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	36	36	36	mA	
STANDBY CURRENT: (CMOS) $(\overline{RAS} = \overline{CAS} = \text{Other Inputs} = \text{Vcc} - 0.2\text{V})$	lcc2	18	18	18	mA	-
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: 'RC = 'RC (MIN))	lcc3	1008	918	828	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: [†] PC = [†] PC (MIN))	lcc4	738	648	558	mA	2, 23
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: **RC = **RC (MIN))	lcc5	1008	918	828	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: RC = RC (MIN))	Icce	1008	918	828	mA	2, 19



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		115	pF	17
Input Capacitance: WE	C ₁₂		151	pF	17
Input Capacitance: RASO, RAS1	Сіз		76	pF	17
Input Capacitance: CASO, CAS1, CAS2, CAS3	C ₁₄		50	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0° C $\leq T_{A} \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS	-6		-7			-8	1 1 2 2 2 2		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a	1 3 ATO 1 4 ATO	ns	21
Access time from RAS	†RAC		60		70		80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Output Enable	†OE	· · · · · · · · · · · · · · · · · · ·	15		20		20	ns	
Access time from column address	†AA		30		35		40	ns	Maria Na
Access time from CAS precharge	^t CPA		35		40		45	ns	45.5
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	90-80.
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	siden, din
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	1 (1)
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18, 22
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10	The state of the	ns	
RAS to CAS delay time	†RCD	20	45	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	24
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15	10.00	ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	†RAL	30		35		40		ns	
Read command setup time	†RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			6	-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	^t CLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	15	0	20	- 0	20	ns	12
WE command setup time	†WCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time	tWCR	45		55		60		ns	
(referenced to RAS)	1.0	The second secon		1.31.1.4.					4.53
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	1.5
Data-in setup time	^t DS	0		0		0		ns	15
Data-in hold time	^t DH	10		15		15		ns	15
Data-in hold time	tDHR	45		55		60		ns	100
(referenced to RAS)		1.0							
Transition time (rise or fall)	tT ·	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF	1 1	16		16		16	ms	
RAS to CAS precharge time	tRPC	0		0		0		ns	1.74
CAS setup time	tCSR	10	1	10		10		ns	19
(CAS-BEFORE-RAS refresh)									
CAS hold time	tCHR	15		15	-	15		ns	19
(CAS-BEFORE-RAS refresh)			4						
WE hold time	tWRH	10		10		10		ns	4.
(CAS-BEFORE-RAS refresh)								110	2.5
WE setup time	tWRP	10		10		10		ns	
(CAS-BEFORE-RAS refresh)				1					
WE hold time	tWTH	10		10		10		ns	
(WCBR test cycle)	V7 .		1 1						
WE setup time	tWTS	10		10		10		ns	
(WCBR test cycle)								4.44	
Last CAS going LOW to first	tCLCH	10		10		10		ns	
CAS to return HIGH	<u> </u>	l	L					J. C. 41	

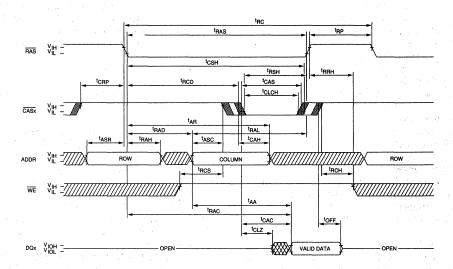


NOTES

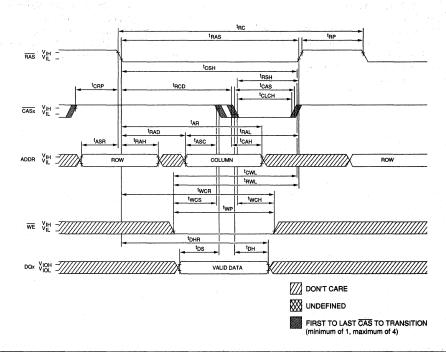
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U18.
- 22. Last falling \overline{CASx} edge to first rising \overline{CASx} edge.
- 23. Icc is dependent on cycle rates.
- 24. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

READ CYCLE

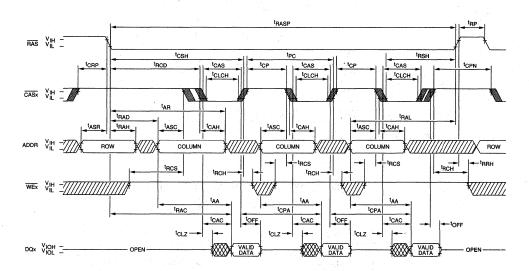


EARLY-WRITE CYCLE

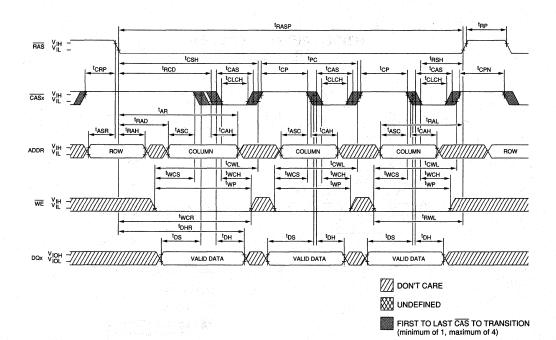




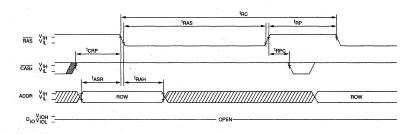
FAST-PAGE-MODE READ CYCLE



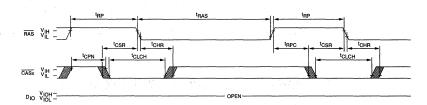
FAST-PAGE-MODE EARLY-WRITE CYCLE



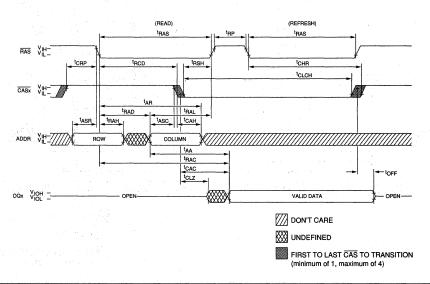
RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE (A0-A9 = DON'T CARE)



HIDDEN REFRESH CYCLE 20 (WE = HIGH)





ORAM MODULE

2 MEG x 36, 4 MEG x 18

FAST PAGE MODE (MT24D236) LOW POWER, EXTENDED REFRESH (MT24D236 L)

EATURES

Industry standard pinout in a 72-pin single-in-line package

High-performance, CMOS silicon-gate process

Single 5V ±10% power supply

All device pins are fully TTL compatible

Low power, 72mW (18.4mW L-version) standby;

2,536mW active, typical

Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR)

and HIDDEN

1,024-cycle refresh distributed across 16ms or

1,024-cycle extended refresh distributed across 128ms

FAST PAGE MODE access cycle

Low CMOS standby current, 4.8mA maximum (L-version)

Multiple RAS lines allow x18 or x36 width

PTIONS	MARKING
Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
Packages Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G
Power/Refresh Normal Power/16ms Low Power/128ms	Blank L
Part Number Example: MT24I	D236GL-6

ENERAL DESCRIPTION

The MT24D236 is a randomly accessed solid-state memory ntaining 2,097,152 words organized in a x36 configurant. During READ or WRITE cycles, each bit is uniquely dressed through the 20 address bits, which are entered 10 is (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits d \overline{CAS} the latter 10 bits. A READ or WRITE cycle is lected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates \overline{AD} mode while a logic LOW on \overline{WE} dictates WRITE ode. During a WRITE cycle, data-in (D) is latched by the ling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY RITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going DW, and the output pin(s) remain open (High-Z) until the xt \overline{CAS} cycle.

FAST PAGE MODE operations allow faster data operans (READ or WRITE) within a row-address (A0-A9)

PIN ASSIGNMENT (Top View) 72-Pin SIMM (T-20)

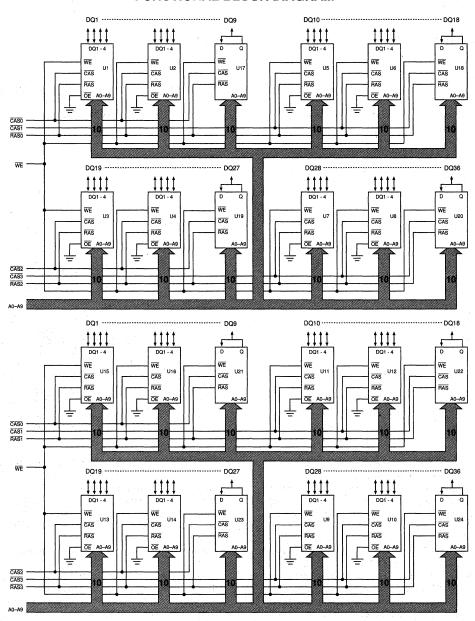


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CASO	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	RAS3	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U16 = MT4C4001JDJ U17-U24 = MT4C1024DJ

U1-U16 = MT4C4001JDJ L (L-version) U17-U24 = MT4C1024DJ L (L-version)



TRUTH TABLE

				<u> </u>			
					ADDRESSES		DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC.	DQ1-DQ36
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L.	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L. L.	Н	Х	Χ	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L		Х	X	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	24W
Short Circuit Output Current	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	. '	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1	
INPUT LEAKAGE CURRENT	CASO-CAS3	111	-12	12	μΑ	
Any Input: 0V ≤ Vin ≤ Vcc	A0-A9, WE	112	-48	48	μA	
(All other pins not under test = 0V) for each package input	RAS0-RAS3	lıз	-12	12	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ36	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iouт = -5mA) Output Low Voltage (Iouт = 5mA)		Vol		0.4	v	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	48	48	48	mA	
STANDBY CURRENT: (CMOS)	lcc2	24	24	24	mA	
$\overline{(RAS} = \overline{CAS} = Vcc -0.2V)$		4.8	4.8	4.8	mΑ	24
OPERATING CURRENT: Random READ/WRITE Average power supply current	lcc3	1264	1144	1024	mA	2, 22
(RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	1003	1225	1105	985	mA	2,22,24
OPERATING CURRENT: FAST PAGE MODE		944	824	704	mA	2, 22
Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	ICC4	905	785	665	mA	2,22,24
REFRESH CURRENT: RAS-ONLY		1264	1144	1024	mA	2
Average power supply current (RAS Cycling, CAS = V _{IH} : ^t RC = ^t RC (MIN))	lcc5	1225	1105	985	mA	2, 24
REFRESH CURRENT: CAS-BEFORE-RAS		1264	1144	1024	mA	2, 19
Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	1225	1105	985	mA	2,19,24
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = \frac{1}{1}RAS (MIN) to 300ns; WE = Vcc -0.2V; A0-A9 and Din = Vcc -0.2V or 0.2V (Din may be left open), \frac{1}{1}RC = 125\textit{\mu}s (1,024 rows at 125\textit{\mu}s = 128ms)	lcc7	6.4	6.4	6.4	mA	24



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		154	pF	17
Input Capacitance: WE	C ₁₂		202	pF	17
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз		50	pF	17
Input Capacitance: CAS0, CAS1, CAS2, CAS3	C ₁₄		50	pF	17
Input/Output Capacitance: DQ1-DQ36	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS			-6		-7		-8		100
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	1745
READ-WRITE cycle time	^t RWC	n/a		n/a		n/a		ns	21
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	21
Access time from RAS	†RAC	No.	60		70		80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Output Enable	^t OE		15		20		20	ns	
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	1.0
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	and the
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	10		10		-10		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	23
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	1. 1. A.
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	†RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-	6		-7		-8		1.0
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12
WE command setup time	tWCS	0		0	1 1	0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	†WP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCML	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	tŢ	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/24
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	[†] CHR	15		15		15		ns	19
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10		ns	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	
WE hold time (WCBR test cycle)	tWTH.	10		10		10		ns	
WE setup time (WCBR test cycle)	twts	10		10		10		ns	

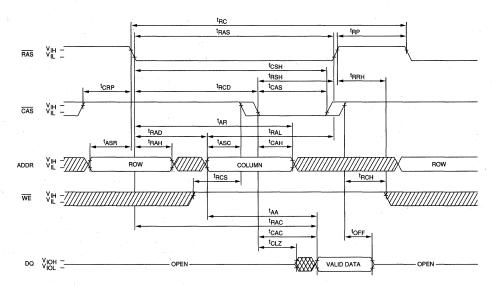


JOTES

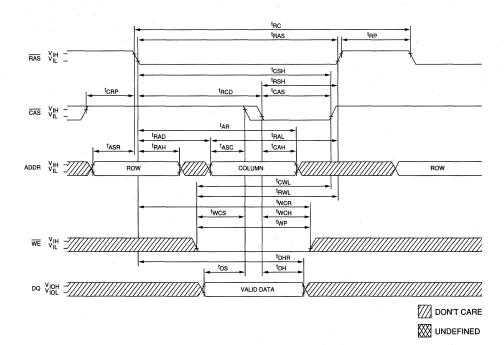
- All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- An initial pause of 100µs is required after power-up followed by any eight RAS REFRESH cycles (RAS-ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \le T_A \le 70^{\circ}C$) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ${}^{t}RCD < {}^{t}RCD$ (MAX). If ${}^{t}RCD$ is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
-). If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 1. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 2. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 3. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to \overline{CAS} leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on all 4 Meg DRAMs.
- 22. Icc is dependent on cycle rates.
- 23. Operation within the ^tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 24. Applies to L-version only.

READ CYCLE

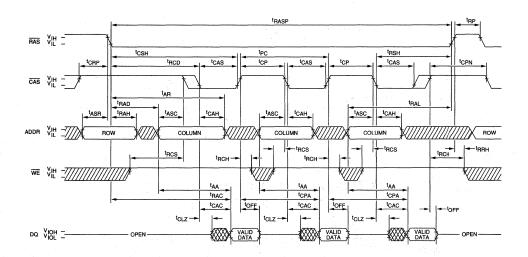


EARLY-WRITE CYCLE

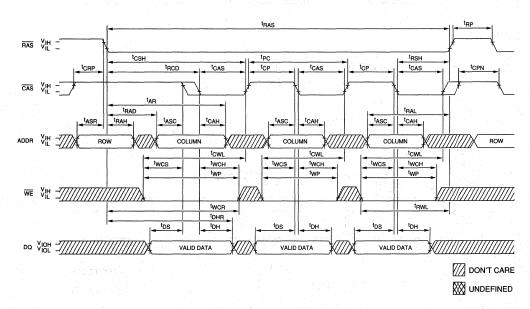




FAST-PAGE-MODE READ CYCLE



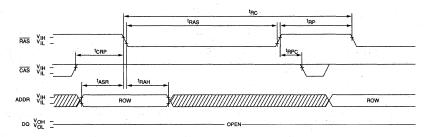
FAST-PAGE-MODE EARLY-WRITE CYCLE





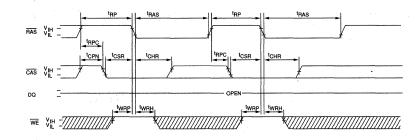
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; WE = DON'T CARE)



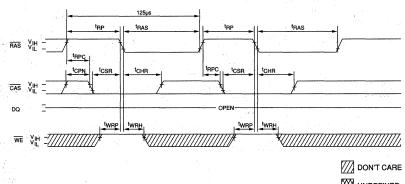
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE 24

(A0-A9 = DON'T CARE)

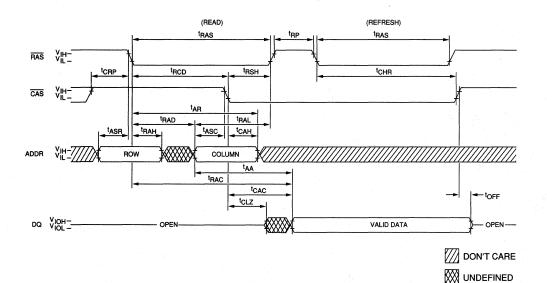






HIDDEN REFRESH CYCLE 20

(WE = HIGH)



DRAM MODULE

4 MEG x 36, 8 MEG x 18 **FAST PAGE MODE**

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 52mW standby; 3,100mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 width

 Timing 		
60ns access		- 6
70ns access		- 7
80ns access		- 8
 Packages 		
Leadless 72-pin	SIMM	M
Leadless 72-pin	SIMM (Gold)	G

• Part Number Example: MT12D436G-6

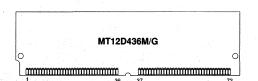
GENERAL DESCRIPTION

The MT12D436 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-21)

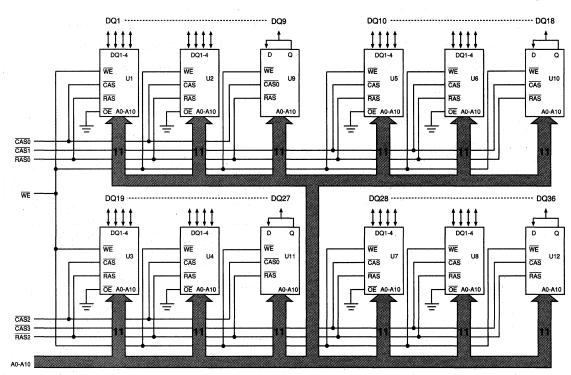


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	:38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CASO	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC .	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C4M4A1DJ U9-U12 = MT4C1004JDJ

MT12D436 4 MEG x 36, 8 MEG x 18 DRAM MODULE

TRUTH TABLE

	11.		3.1	72.44	ADDR	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	tR t	t _C	DQ1-DQ36
Standby		Н	H→X	X	X	Х	High-Z
READ		, 11 L 1	, L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	, L,	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L,	Н	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss



MT12D436 4 MEG x 36, 8 MEG x 18 DRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	12W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs		Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT	RASO, RAS2	ln	-12	12	μΑ	
Any Input 0V ≤ Vin ≤ Vcc	A0-A10, WE	lı2	-24	24	μΑ	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	lıз	-6	6	μA	•
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) for each package input	DQ1-DQ36	loz	-10	10	μΑ	
OUTPUT LEVELS	1,	Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 5mA)		Vol		0.4	v	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	24	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc2	12	12	12	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	1400	1200	1040	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	960	840	720	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	1400	1200	1040	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	1400	1200	1040	mA	3, 5

CAPACITANCE

PARAMETER	 1 181 Televisia 1 180 Televisia	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10		Cıı		77	pF	2
Input Capacitance: WE		Cı2		100	pF	2
Input Capacitance: RASO, RAS2		Сіз		51	pF	2
Input Capacitance: CAS0, CAS1, CAS2, CAS3		C ₁₄		25	pF	2
Input/Output Capacitance: DQ1-DQ36		Сю		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7	-8			d is
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	ENGLY.
READ-WRITE cycle time	tRWC	n/a	The State of the	n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	n/a		n/a		n/a		ns	22
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	^t CAC		15		20		20	ns	15
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		40		40		45	ns	ga i i i i i i i
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	^t RP	40		50		60		ns	
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	tCAH .	10		15		15		ns	
Column address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19



4 MEG x 36, 8 MEG x 18 DRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6		-7		8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	[†] OFF	0	20	0	20	0	20	ns	20
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		. 15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	^t RWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		- 0		ns	21
Data-in hold time	HQţ	10		15		15		ns	21
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
Transition time (rise or fall)	^t T	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^t REF		32		32		32	ms	
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15	-	ns	5
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	10		10		10	1.2	ns	24
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	^t WTH	10		10		10		ns	24
WE setup time (WCBR test cycle)	twts	10		10		10		ns	24



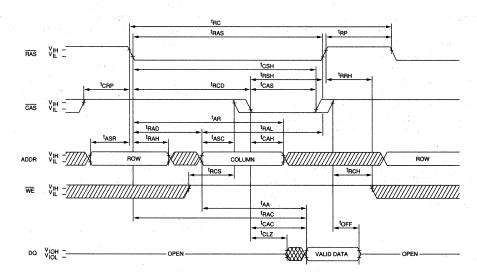
M112D436 4 MEG x 36, 8 MEG x 18 DRAM MODULE

NOTES

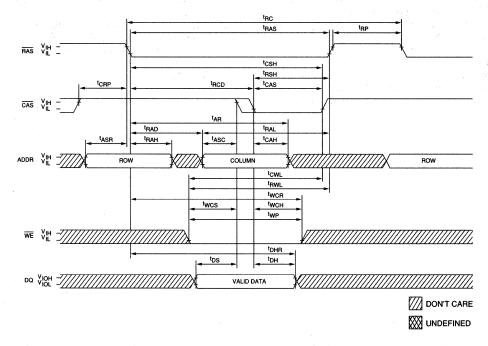
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.

- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 22. OE is tied permanently LOW; LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 24. ^tWTS and ^tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR refresh cycle.

READ CYCLE

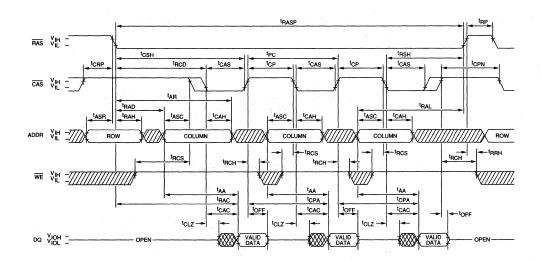


EARLY-WRITE CYCLE

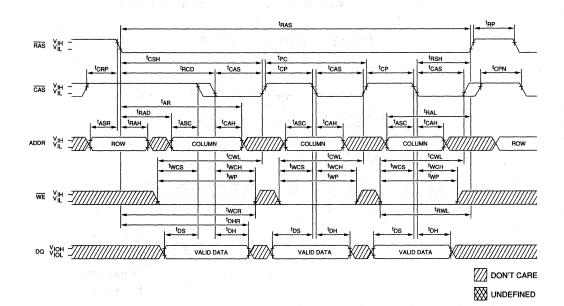


NEW DRAM MODULE

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

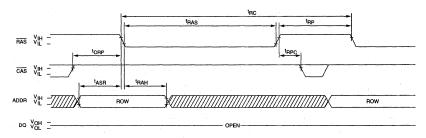


T12D436 EV. 4/92



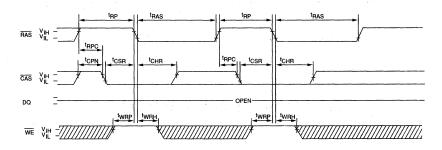
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A10; WE = DON'T CARE)



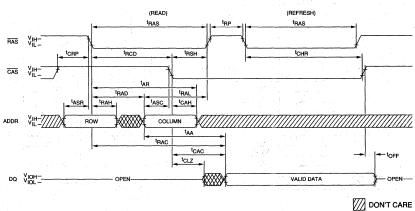
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DONTCARE)



HIDDEN REFRESH CYCLE 23

 $(\overline{WE} = HIGH)$



NEW **III** DRAM MODULE

DRAM MODULE

8 MEG x 36,16 MEG x 18 FAST PAGE MODE

FEATURES

OPTIONS

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 104mW standby; 3,152mW active, typical
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE access cycle
- Multiple RAS lines allow x18 or x36 widths

• Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Leadless 72-pin SIMM	M
Leadless 72-pin SIMM (Gold)	G

Part Number Example: MT24D836G-6

GENERAL DESCRIPTION

The MT24D836 is a randomly accessed solid-state memory containing 8,388,608 words organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{\text{RAS}}$ is used to latch the first 11 bits and $\overline{\text{CAS}}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{CAS}}$. Since $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open(High-Z) until the next $\overline{\text{CAS}}$ cycle.

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A10) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS

PIN ASSIGNMENT (Top View) 72-Pin SIMM

(T-22)

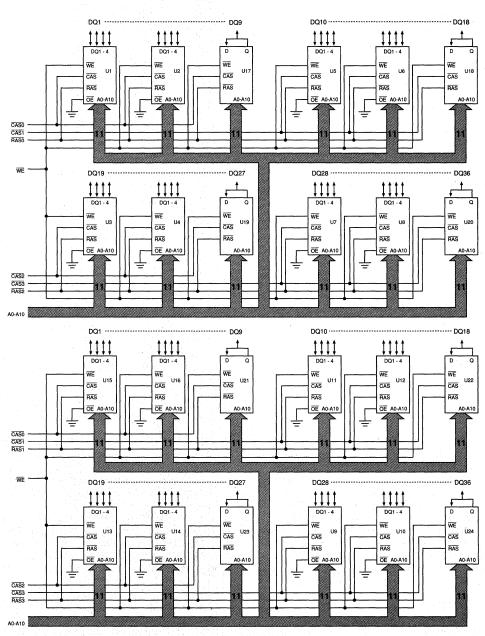


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	RAS1	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	RAS3	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM





TRUTH TABLE

					ADDRI	ESSES	DATA IN/OUT
FUNCTION	**************************************	RAS	CAS	WE	t _R	¹C	DQ1-DQ36
Standby		Н	H→X	Х	Х	Х	High-Z
READ		L	L L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
WRITE	2nd Cycle	L.	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	Н	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	LL	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C $\leq T_A \leq 70$ °C; Vcc = 5V ± 10 %)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	. 1 .
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	RAS0-RAS3	l ₁₁	-12	12	μΑ	
Any Input 0V ≤ ViN ≤ Vcc	A0-A10, WE	lı2	-48	48	μΑ	
(All other pins not under test = 0V) for each package input	CAS0-CAS3	lı3	-12	12	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) for each package input	DQ1-DQ36	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 5mA)		Vol		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	Icc1	48	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	24	24	24	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	1424	1224	1064	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	984	864	744	mA	3, 4
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: ^t RC = ^t RC (MIN))	lcc5	1424	1224	1064	mA	3
REFRESH CURRENT: CAS-BEFORE-RAS Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icce	1424	1224	1064	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	Cıı		154	pF	2
Input Capacitance: WE	Cı2		200	pF	2
Input Capacitance: RASO, RAS1, RAS2, RAS3	Сіз		51	pF	2
Input Capacitance: CASO, CAS1, CAS2, CAS3	C ₁₄	-	50	pF	2
Input/Output Capacitance: DQ1-DQ36	Сю		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 22) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		ar a tar
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		ns	22
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	[†] PRWC	n/a		n/a		n/a		ns	22
Access time from RAS	TRAC		60		70		80	ns	14
Access time from CAS	¹ CAC		15		20		20	ns	15
Access time from column address	tAA		30		35		40	ns	
Access time from CAS precharge	†CPA		40		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	The state of the
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15	1	20		20	1.5	ns	
RAS precharge time	tRP	40		50		60		ns	Carlos S
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	^t CSH	60	1	70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	16
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	<u> </u>	ns	
RAS to CAS delay time	†RCD	20	40	20	50	20	60	ns	17
CAS to RAS precharge time	^t CRP	5		5		5		ns	
Row address setup time	^t ASR	0		0		0		ns	A grant in
Row address hold time	tRAH .	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	18
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	†RAL	30		35		40		ns	
Read command setup time	†RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	19
CAS to output in Low-Z	†CLZ	0		0		0		ns	

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6	-	7	-	8	1.1	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	20
WE command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15	- qu	15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	†RWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH	10		15		15		ns	21
Data-in hold time (referenced to RAS)	tDHR	45		55	W . 1.	60		ns	
Transition time (rise or fall)	tΤ	3	- 50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	^t REF		32		32		32	ms	
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	5
WE hold time (CAS-BEFORE-RAS refresh)	WRH	10		10		10		ns	24
WE setup time (CAS-BEFORE-RAS refresh)	†WRP	10		10		10		ns	24
WE hold time (WCBR test cycle)	hTW [†]	10		10		10		ns	24
WE setup time (WCBR test cycle)	tWTS	10		10		10		ns	24



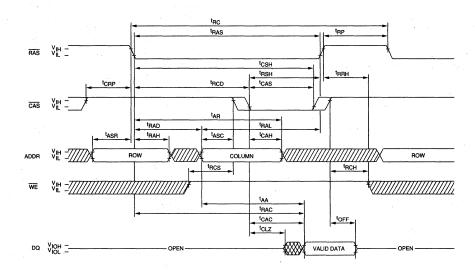
NOTES

- 1. All voltages referenced to Vss.
- This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS)
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates.
 Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this

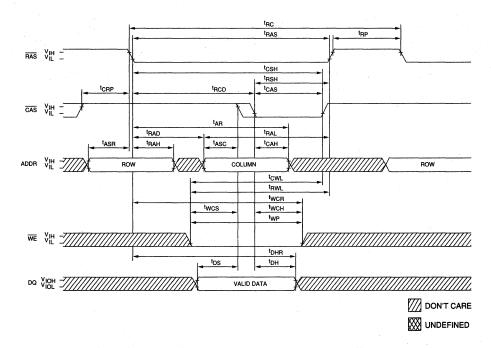
- table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles.
- 22. OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} =HIGH.
- 24. WTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR refresh cycle.

MICRON

READ CYCLE

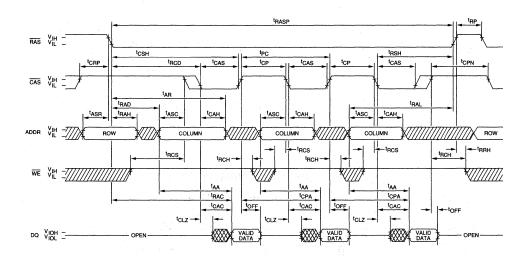


EARLY-WRITE CYCLE

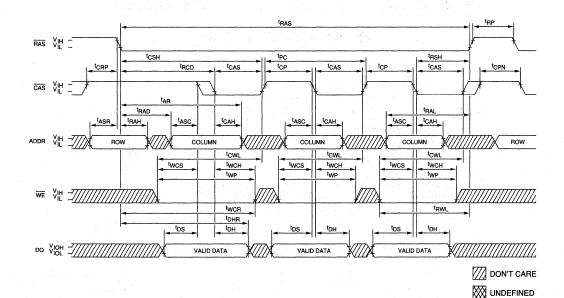


NEW DRAM MODULE

FAST-PAGE-MODE READ CYCLE

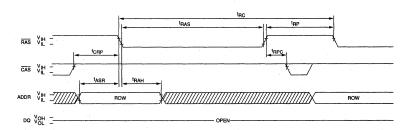


FAST-PAGE-MODE EARLY-WRITE CYCLE



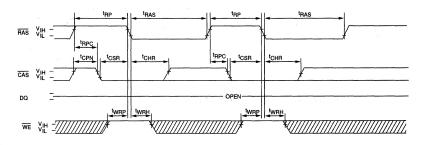
3-301

RAS-ONLY REFRESH CYCLE (ADDR = A0-A10; WE = DON'T CARE)

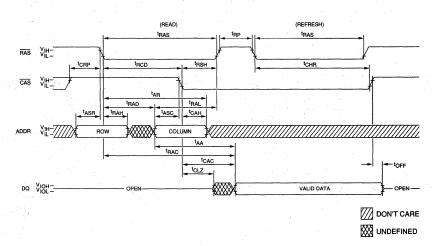


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A10 = DON'T CARE)



HIDDEN REFRESH CYCLE ²³ (WE = HIGH)





DRAM MODULE

256K x 40 DRAM

FAST PAGE MODE (MT10D25640) LOW POWER, EXTENDED REFRESH (MT10D25640 L)

FEATURES

- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW (3mW L-version) standby; 1,750mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 2mA maximum (L-version)

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	- 7
80ns access	- 8
• Packages Leadless 72-pin SIMM (Gold)	\mathbf{G}
 Presence Detect Industry standard Application specific 	Blank IB
• Power/Refresh Normal power/8ms Low power/64ms	Blank L

Part Number Example: MT10D25640GL-6 IB

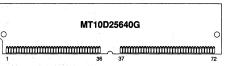
GENERAL DESCRIPTION

The MT10D25640 is a randomly accessed solid-state nemory containing 262,144 words organized in a x40 coniguration. During READ or WRITE cycles, each bit is iniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first bits and CAS the latter 9 bits. READ or WRITE cycles are elected with the WE input. A logic HIGH on WE dictates **EAD** mode while a logic LOW on WE dictates WRITE node. During a WRITE cycle, data-in (D) is latched by the alling edge of WE or CAS, whichever occurs last. EARLY VRITE occurs when WE goes LOW prior to CAS going .OW; the output pin(s) remain open (High-Z) until the next AS cycle.

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-13)

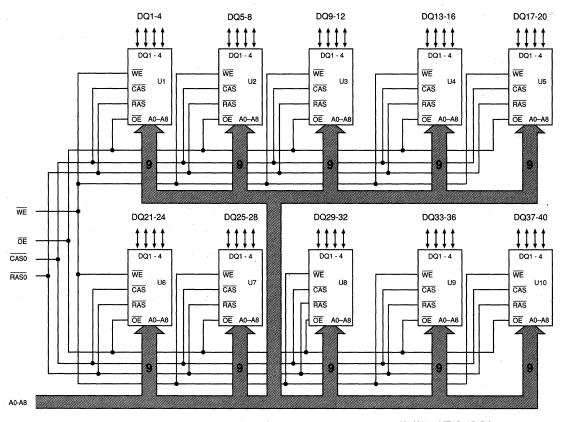


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	ŌĒ	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	WE	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4256DJ U1-U10 = MT4C4256DJ L (L-version)



TRUTH TABLE

						ADDRI	ESSES	DATA IN/OUT	
FUNCTION		RAS	CAS	WE	0E	^t R	t _C	DQ1-DQ40	NOTES
Standby	1	Н	H→X	Х	X	Х	Х	High-Z	
READ		L	· L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data In	
READ-WRITE	. Den	L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	The Control
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRES	H agarija i	L	Н	Х	Х	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	i L	L	Х	ROW	COL	Data In	
CAS-BEFORE-RAS	REFRESH	H→L	L	Х	Х	Х	Х	High-Z	
BATTERY BACKUP I	REFRESH	H→L	L	Х	Х	Х	Х	High-Z	2 2

PRESENCE DETECT-INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT-APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	Vss	NC	Vss
PRD2	NC	NC	NC
PRD3	Vss	Vss	NC
PRD4	NC	Vss	Vss



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss-1V to +7V Operating Temperature, TA (Ambient)0°C to +70°C Storage Temperature (Plastic)-55°C to +125°C Power Dissipation10W Short Circuit Output Current50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage			4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs			2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	-	VIL	-1.0	0.8	٧	1
INPUT LEAKAGE CURRENT	A0-A8, WE	lı lı	-20	20	μΑ	
Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = $0V$) for each package input	RAS, CAS	lı2	-10	10	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ40	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 4.2mA)	Vol		0.4	V		

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc3	20	20	20	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	Icc4	10 2	10 2	10 2	mA mA	27 22
OPERATING CURRENT: Random READ/WRITE Average power supply current	lcc1	900	800	700	mA	2, 26
(RAS, CAS, Single Address Cycling: RC = RC (MIN)) OPERATING CURRENT: FAST PAGE MODE	1	700	750 600	650 500	mA mA	22 2, 26
Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc2	650	550	450	mA	22
REFRESH CURRENT: RAS-ONLY Average power supply current	lcc5	900	800	700	mA	2
(RAS Cycling, CAS = ViH: tRC = tRC (MIN))	1000	850	750	650	mA	22
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current	lcc6	900	800	700	mA	2, 19
(RAS, CAS, Address Cycling: tRC = tRC (MIN))		850	750	650	mA	22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1μs; WE, A0-A8 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125μs (512 rows at 125μs = 64ms)	lcc7	2	2	2	mA	22



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Cıı		64	pF	17
Input Capacitance: WE, OE, RASO, CASO	C ₁₂		84	рF	17
Input/Output Capacitance: DQ1-DQ40	Сю		10	рF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = 5V ±10%)

AC CHARACTERISTICS			-6		-7		-8		14. T
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	^t RWC	165		185		205		ns	1 - 1 2 2 V
FAST-PAGE-MODE READ or WRITE cycle time	tPC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	
Access time from RAS	^t RAC		60		70		80	ns	8
Access time from CAS	^t CAC		20		20		20	ns	9
Output Enable	†OE		20		20		20	ns	
Access time from column address	tAA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35	- 1	40		45	ns	nazaju es
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	najoji k
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60	1.11 - 1.13	ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		10		ns	
RAS to column address delay time	†RAD	15	30	15	35	15	40	ns	21
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14
CAS to output in Low-Z	†CLZ	0	1 1 1	0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6	-	7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	†OFF	0	20	0	20	0	20	ns	12, 23
Output disable	†OD		15		20		20	ns	23
WE command setup time	twcs	0		0		0		ns	24
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45 ,	·	55	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20	1	20		ns	
Data-in setup time	t _{DS}	0		0		0		ns	15
Data-in hold time	^t DH	15		15		. 15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		100		110		ns	24
Column address to WE delay time	tAWD	60	,	65		70		ns	24
CAS to WE delay time	tCWD	40		50		55		ns	24
Transition time (rise or fall)	ŀΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	3/22
RAS to CAS precharge time	tRPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10	. 67 94	10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		15		15		ns	19
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	20

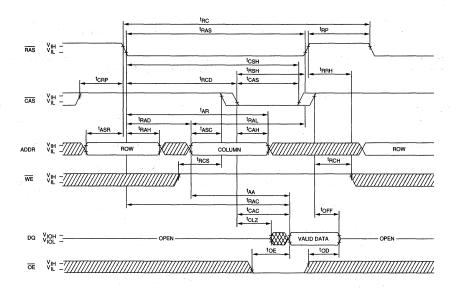


NOTES

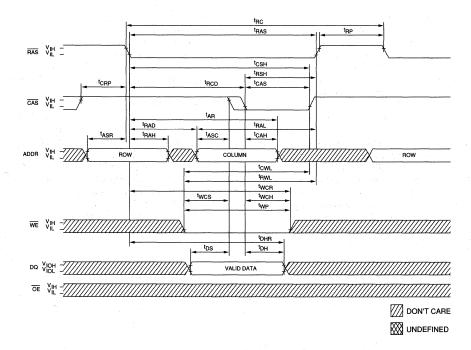
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 8ms (64ms L version) refresh requirement is exceeded.
- 4. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ¹RCD < ¹RCD (MAX). If ¹RCD is greater than the maximum recommended value shown in this table, ¹RAC will increase by the amount that ¹RCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If CAS = Vін, data output is High-Z.
- 11. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).

- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and \overline{OE} = HIGH.
- 21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 22. Applies to L-version only.
- 23. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 24. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. Icc is dependent on cycle rates.
- 27. All other inputs at Vcc -0.2V.

READ CYCLE

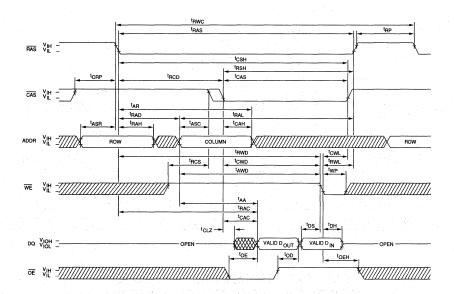


EARLY-WRITE CYCLE

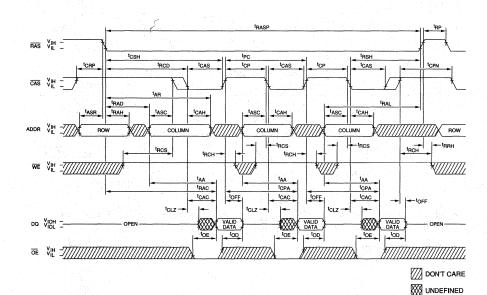




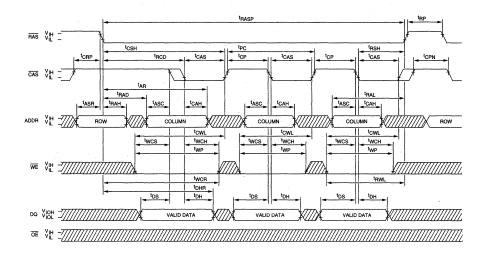
READ-WRITE CYCLE(LATE WRITE and READ-MODIFY-WRITE CYCLES)



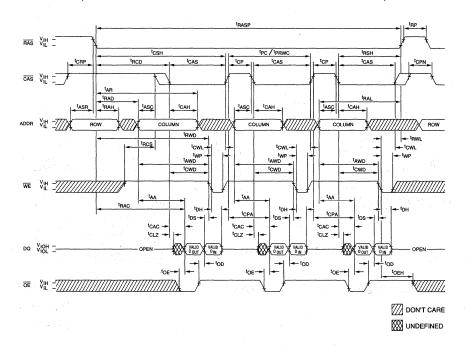
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



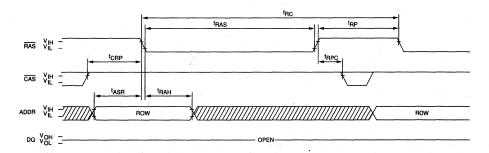
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





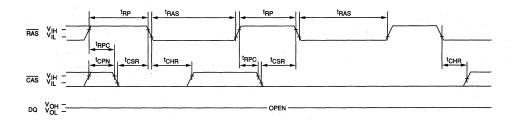
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; WE = DON'T CARE)



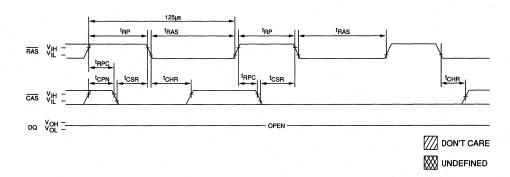
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



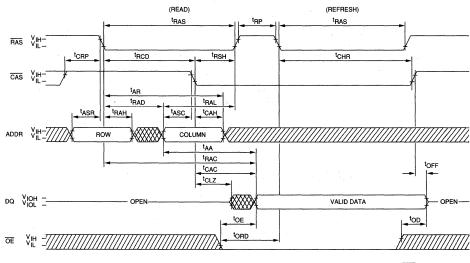
BATTERY BACKUP REFRESH CYCLE 22

(WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



DON'T CARE





DRAM MODULE

512K x 40 DRAM

FAST PAGE MODE (MT20D51240) LOW POWER. EXTENDED REFRESH (MT20D51240 L)

FEATURES

OPTIONS

- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW (6mW L-version) standby; 1,780mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

MARKING

- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 4mA maximum (L-version)

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages	
Leadless 72-pin SIMM (Gol	d) G
Presence Detect	
Industry standard	Blank
Application specific	IB
• Power/Refresh	
Normal power/8ms	Blank
Low power/64ms	L

GENERAL DESCRIPTION

• Part Number Example: MT20D51240GL-6 IB

The MT20D51240 is a randomly accessed solid-state memory containing 524,288 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW; the output pin(s) remain open (High-Z) until the next CAS cycle.

PIN ASSIGNMENT (Top View)

72-Pin SIMM

(T-15)

MT20D51240G **.....**

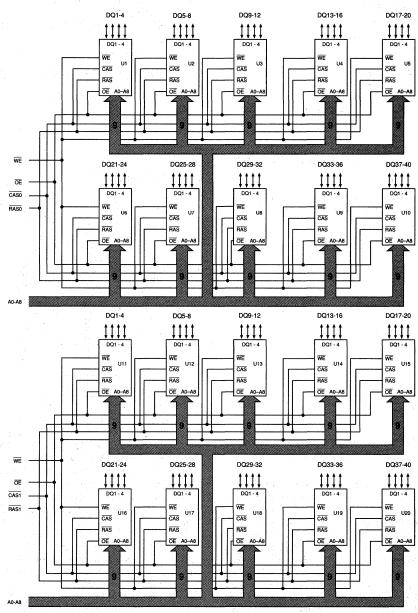
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
. 1	Vss	19	ŌĒ	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	WE	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms (64ms on L version), regardless of sequence.



FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4256DJ U1-U20 = MT4C4256DJ L (L-version)



TRUTH TABLE

						ADDRI	ESSES	DATA IN/OUT	
FUNCTION		RAS	CAS	WE	ŌĒ	^t R	^t C	DQ1-DQ40	NOTES
Standby		Н	H→X	Х	Х	Х	X	High-Z	1
READ		· L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	ı L	L	Х	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	14.4
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	A L	ROW	COL	Data Out	# A
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	Talka See
RAS-ONLY REFRES	H	, L	Н	Х	Х	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	
CAS-BEFORE-RAS	REFRESH	H→L	, L	Н	Х	Х	X	High-Z	
BATTERY BACKUP	REFRESH	H→L	L	Х	X	Х	Х	High-Z	22

PRESENCE DETECT-INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT-APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	NC	Vss	NC
PRD2	NC	Vss	Vss
PRD3	NC	NC	Vss
PRD4	Vss	NC	NC



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0° C $\leq T_A \leq 70^{\circ}$ C; Vcc = 5V ±10%)

PARAMETER/CONDITION	PARAMETER/CONDITION S				UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	- :	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	A0-A8, WE	lı lı	-40	40	μА	
Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = $0V$) for each package input	RAS, CAS	lı2	-20	20	μА	
OUTPUT LEAKAGE CURRENT	DQ1-DQ40	loz	-20	20	μΑ	
(Q is disabled, $0V \le V_{OUT} \le V_{CC}$) for each package input	l			7.5		
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (lout = -5mA) Output Low Voltage (lout = 4.2mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lссз	40	40	40	mA	
STANDBY CURRENT: (CMOS)	lcc4	20	20	20	mA	27
$\overline{(RAS} = \overline{CAS} = Vcc - 0.2V)$		4	4	4	mA	22
OPERATING CURRENT: Random READ/WRITE (RAS, CAS, Single Address Cycling: ^t RC = ^t RC (MIN))	lcc1	920	820	720	mA	2, 26
Average power supply current		854	754	654	mA	22
OPERATING CURRENT: FAST PAGE MODE Average power supply current	lcc2	720	620	520	mA	2, 26
(RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))		654	554	454	mA	22
REFRESH CURRENT: RAS-ONLY Average power supply current	lcc5	920	820	720	mA	2
(RAS Cycling, CAS = ViH: ^t RC = ^t RC (MIN))		854	754	654	mA	22
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current	lcc6	920	820	720	mA	2, 19
(RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))		854	754	654	mA	22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during battery backup refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = tRAS (MIN) to 1µs; WE, A0-A8 and DIN = Vcc -0.2V or 0.2V (DIN may be left OPEN), tRC = 125µs (512 rows at 125µs = 64ms)	lcc7	4	4	4	mA	22



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C ₁₁		128	pF	17
Input Capacitance: WE, OE	C ₁₂		168	pF	17
Input Capacitance: RAS0, RAS1, CAS0, CAS1	Сіз		84	pF	17
Input/Output Capacitance: DQ1-DQ40	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER -	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	V V V
Access time from RAS	^t RAC		60		70		80	ns	8
Access time from CAS	†CAC		20		20		20	ns	9
Output Enable	†OE		20		20		20	ns	
Access time from column address	tAA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	William P. C.
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	20		20		20		ns	
RAS precharge time	tRP	40		50		60	The state of	ns	
CAS pulse width	†CAS	20	100,000	20	100,000	20	100,000	ns	4-14
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	21
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	^t CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	45		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14
CAS to output in Low-Z	^t CLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			6		7		-8	1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	0	20	0	20	0	20	ns	12, 23
Output disable	tOD		15		20		20	ns	23
WE command setup time	twcs	0		0		0		ns	24
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45	: 2 x . v . ·	55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	†RWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns .	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	^t DH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	85		100		110		ns	24
Column address to WE delay time	tAWD	60		65		70		ns	24
CAS to WE delay time	tCWD	40		50		55		ns	24
Transition time (rise or fall)	ľΤ	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	3/22
RAS to CAS precharge time	tRPC	0	4	0	100	0	1. 1.	ns	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		15		15		ns	19
OE hold time from WE during READ-MODIFY-WRITE cycle	OEH	15		20		20		ns	25
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	20

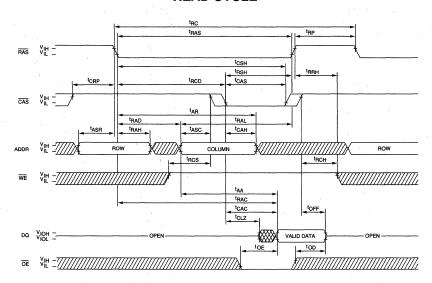


NOTES

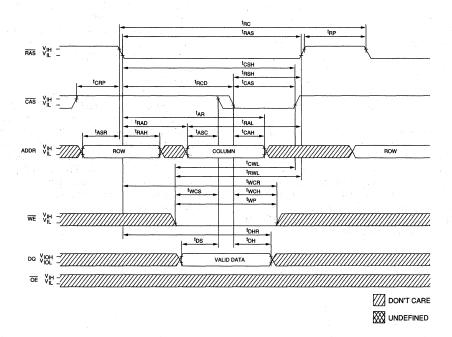
- 1. All voltages referenced to Vss.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 8ms (64ms L version) refresh requirement is exceeded.
- 4. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
- *OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).

- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW and \overline{OE} = HIGH.
- 21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 22. Applies to L-version only.
- 23. The DQs open during RÉAD cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).
- 24. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. Icc is dependent on cycle rates.
- 27. All other inputs at Vcc -0.2V.

READ CYCLE

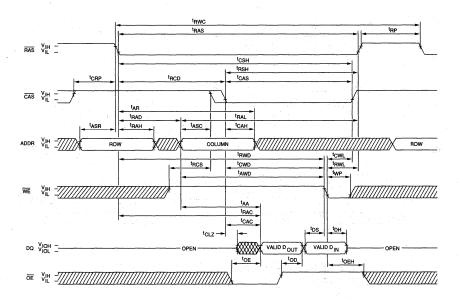


EARLY-WRITE CYCLE

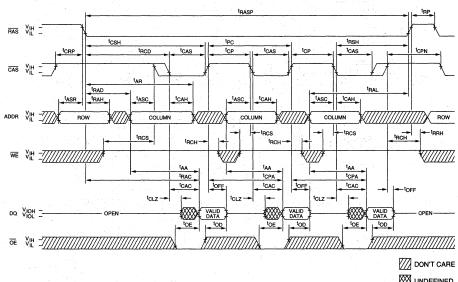




READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE CYCLES)

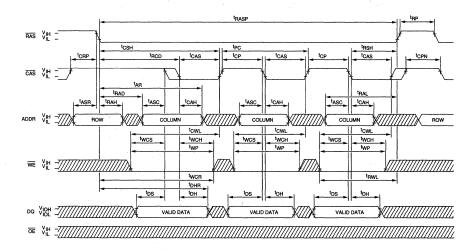


FAST-PAGE-MODE READ CYCLE

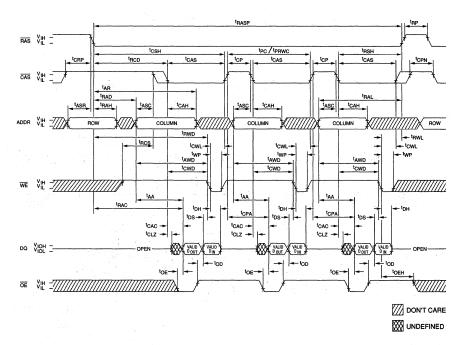




FAST-PAGE-MODE EARLY-WRITE CYCLE

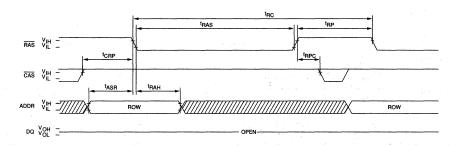


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



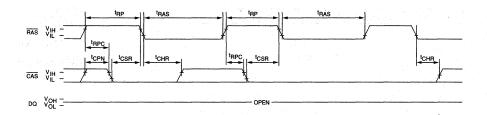


RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)

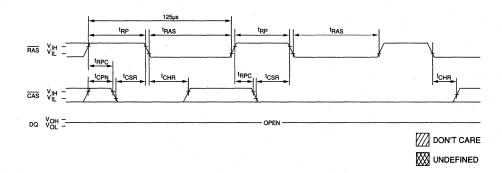


CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8, \overline{WE} and \overline{OE} = DON'T CARE)



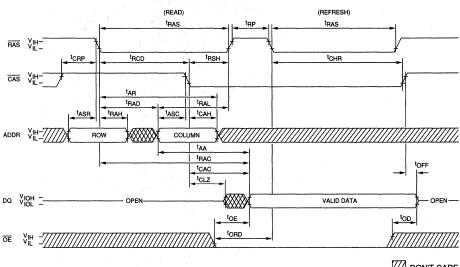
BATTERY BACKUP REFRESH CYCLE 22 (WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



DON'T CARE

₩ undefined



DRAM **MODULE**

1 MEG x 40 DRAM

FAST PAGE MODE (MT10D140) LOW POWER. EXTENDED REFRESH (MT10D140 L)

FEATURES

OPTIONS

- 72-pin single-in-line package
- High-performance, CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 30mW (10mW L-version) standby; 2,250mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- · 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms

MARKING

· Low CMOS standby current, 2mA maximum (L-version)

Timing	
60ns access	- 6
70ns access	- 7
80ns access	- 8
• Packages Leadless 72-pin SIMM (Gold)	G
Presence Detect Industry standard	Blank
Application specific	IB
Power/Refresh	
Normal power/16ms	Blank
Low power/128ms	L

Part Number Example: MT10D140GL-6 IB

GENERAL DESCRIPTION

The MT10D140 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW; the output pin(s) remain open (High-Z) until the next CAS cycle.

PIN ASSIGNMENT (Top View)

72-Pin SIMM (T-13)

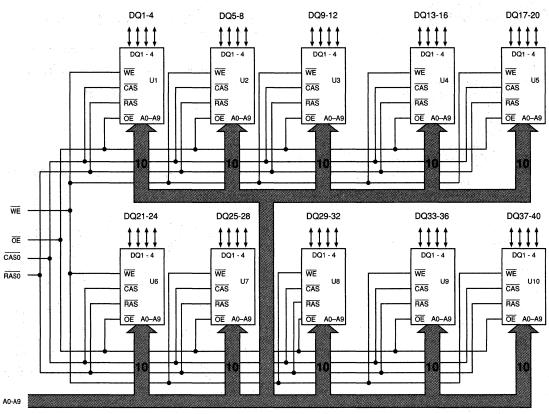
MT10D140G

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	ŌĒ	37	DQ34	55	DQ12
2	DQ1	20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	WE	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U10 = MT4C4001JDJ U1-U10 = MT4C4001JDJ L (L-version)



TRUTH TABLE

		4.5				ADDR	ESSES	DATA IN/OUT	
FUNCTION	FUNCTION		CAS	WE	0E	t _R	t _C	DQ1-DQ40	NOTES
Standby		Н	H→X	Х	Х	Х	Х	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	State Se
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	
RAS-ONLY REFRES	Н	Н	Х	Х	Х	ROW	n/a	High-Z	
HIDDEN	READ	L→H→L	L	Н	<u>L</u>	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In	
CAS-BEFORE-RAS	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	
BATTERY BACKUP I	REFRESH	H→L	L	Х	Х	Х	Х	High-Z	22

PRESENCE DETECT-INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	Vss	Vss	Vss
PRD3	NC	Vss	NC
PRD4	NC	- NC	Vss

PRESENCE DETECT-APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	Vss	Vss	Vss
PRD2	NC	Vss	Vss
PRD3	NC	NC	Vss
PRD4	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	10W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage		Vcc	4.5	5.5	V	1.
Input High (Logic 1) Voltage, All Inputs		ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	A0-A9, WE	lı lı	-20	20	μΑ	
Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = $0V$) for each package input	RAS, CAS	lı2	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ40	loz	-10	10	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 5mA)		Vol		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Vih after 8 RAS cycles (MIN))	lcc3	20	20	20	mA	
STANDBY CURRENT: CMOS INPUT LEVELS	1	10	10	10	mA	
Power supply standby current (RAS = CAS = Vcc -0.2V after 8 RAS cycles (MIN)). (All other inputs at Vcc -0.2V or Vss +0.2V)	lcc4	2	2	2	mA	22
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	lcc1	1100	1000	900	mA	2, 26
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL, CAS = Cycling: PC = PC (MIN))	lcc2	800	700	600	mA	2, 26
REFRESH CURRENT: RAS-ONLY (RAS = Cycling: CAS = Vih)	lcc5	1100	1000	900	mA	2
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	lcc6	1100	1000	900	mA	2, 19
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ^t RAS (MIN) to 300ns; WE, A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open), ^t RC = 125μs (1024 rows at 125μs = 128ms)	lcc7	3	3	3	mA	22



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı		64	pF	17
Input Capacitance: WE, OE, RASO, CASO	C ₁₂		84	pF	17
Input/Output Capacitance: DQ1-DQ40	Сю		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	i jaran
READ-WRITE cycle time	†RWC	165		185		205	21	ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	
Access time from RAS	†RAC		60	3.7.7.4	70		80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Access time from column address	†AA		30		35	1 1 2 1 1	40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	No. of the
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	asal Na
RAS hold time	tRSH	15		20		20	1000000	ns	
RAS precharge time	tRP	45		50		60		ns	
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	- 7.11 L
CAS hold time	^t CSH	60		70		80		ns	
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	tCRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	†RAH	10		10		10		ns	
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	21
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	†CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14
CAS to output in Low-Z	^t CLZ	0		0	1 1 1	0		ns	
Output buffer turn-off delay	[†] OFF	0	20	0	20	0	20	ns	12, 23
WE command setup time	twcs	0		0		0		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	†WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	†WCR	45		55		60		ns	
Write command pulse width	tWP	10		15	1 1 1	15		ns	
Write command to RAS lead time	^t RWL	15		20		20		ns	
Write command to CAS lead time	^t CWL	15		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	90		100		110		ns	24
Column address to WE delay time	^t AWD	60		65		70		ns	24
CAS to WE delay time	tCMD	45		50		50		ns	24
Transition time (rise or fall)	tŢ.	3	50	3	50	3	50	ns	5, 16
Refresh period (1024 cycles)	tREF		16/128		16/128		16/128	ms	3/22
RAS to CAS precharge time	tRPC	0		0		0		ns	19
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	10		10		10	:.	ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	15		15		15		ns	19
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	20
Output disable	tOD	15		20		20		ns	23
Output enable	†OE	15		20		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		20		20		ns	25

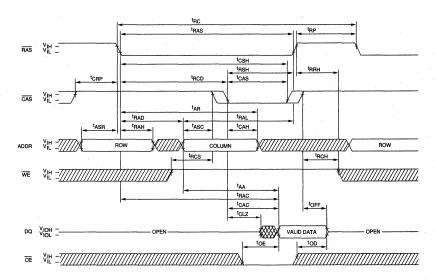


NOTES

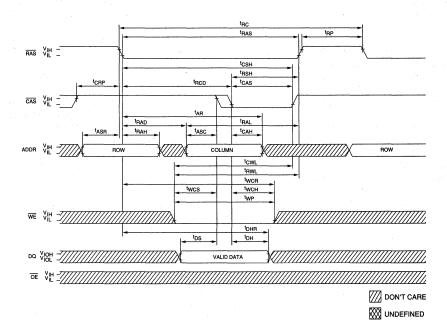
- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight \overline{RAS} cycle wake-up should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
- 4. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 9. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 10. If $\overline{CAS} = VIH$, data output is High-Z.
- 11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.

- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- L-version only.
- 23. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \ge {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 24. LATE-WRITE and READ-MODIFY-WRITE cycles must have both tOD and tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 25. Icc is dependent on cycle rates.
- 26. All other inputs at Vcc -0.2V.

READ CYCLE

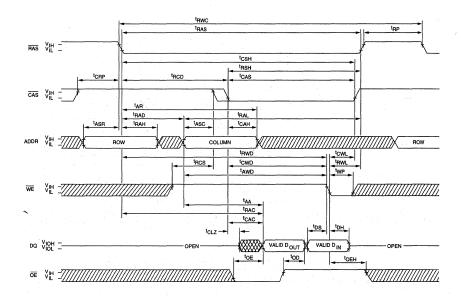


EARLY-WRITE CYCLE

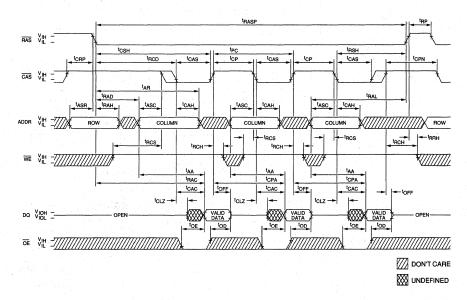




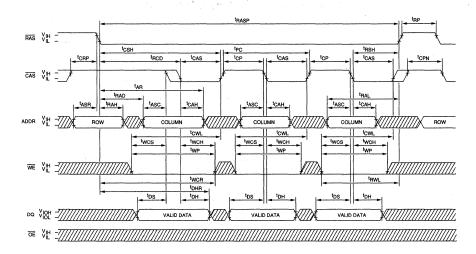
READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



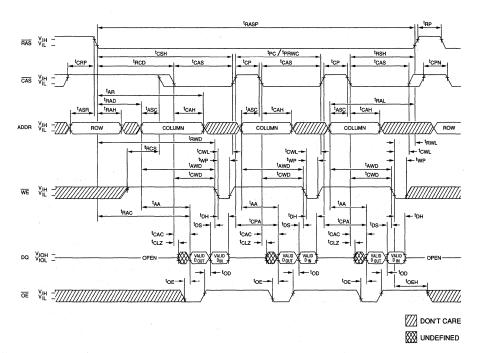
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



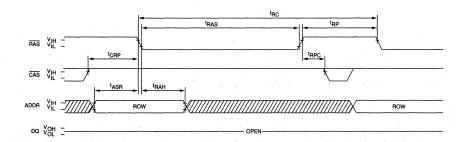
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





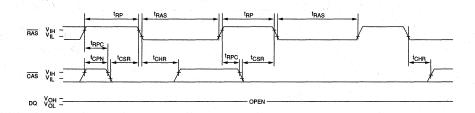
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; and \overline{WE} = DON'T CARE)



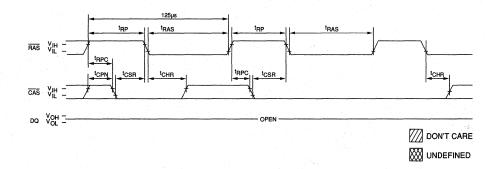
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9, \overline{OE} = DON'T CARE)$



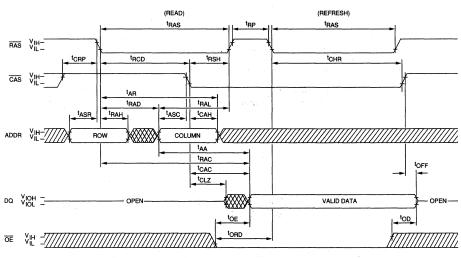
BATTERY BACKUP REFRESH CYCLE 22

(WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



DON'T CARE

W UNDEFINED



DRAM MODULE

2 MEG x 40 DRAM

FAST PAGE MODE (MT20D240) LOW POWER. EXTENDED REFRESH (MT20D240 L)

FEATURES

- 72-pin single-in-line package
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are fully TTL compatible
- Low power, 60mW (20mW L-version) standby; 2,280mW active, typical
- FAST PAGE MODE access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms (L-version)
- Low CMOS standby current, 4mA maximum (L-version)

OPTIONS	MARKING
• Timing 60ns access 70ns access 80ns access	- 6 - 7 - 8
• Packages Leadless 72-pin SIMM (Gold)	G
 Presence Detect Industry standard Application specific 	Blank IB
 Power/Refresh Normal power/16ms 	Blank

Part Number Example: MT20D240GL-6 IB

GENERAL DESCRIPTION

Low power/128ms

The MT20D240 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x40 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW; the output pin(s) remain open (High-Z) until the next CAS cycle.

PIN ASSIGNMENT (Top View)

72-Pin SIMM (T-15)

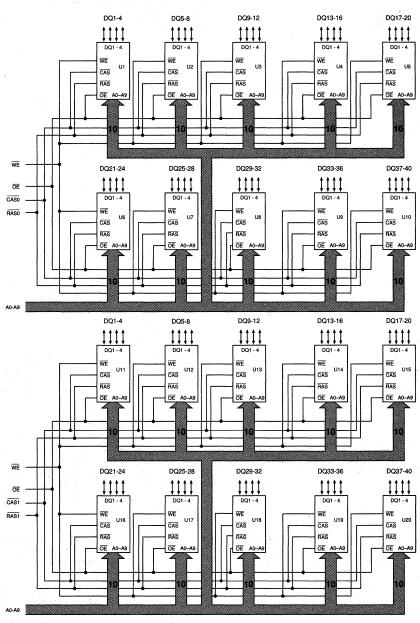


PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	OE .	37	DQ34	55	DQ12
2	DQ1	. 20	DQ5	38	DQ36	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CASO	58	DQ29
5	DQ18	23	DQ22	41	NC	59	Vcc
6	DQ3	24	DQ7	42	NC	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	DQ38	64	DQ32
11	NC	29	DQ37	47	WE	65	DQ16
12	A0	30	Vcc	48	Vss	66	DQ39
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	NC	52	DQ26	70	PRD4
17	A5	35	DQ35	53	DQ11	71	DQ40
18	A6	36	DQ33	54	DQ27	72	Vss

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS or HIDDEN REFRESH) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on L-version), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U20 = MT4C4001JDJ U1-U20 = MT4C4001JDJ L (L-version)



IRUTH TABLE

i i ka wa wa						ADDRI	ESSES	DATA IN/OUT	
FUNCTION		RAS	CAS	WE	0E	t _R	t _C	DQ1-DQ40	NOTES
Standby		Н	H→X	Х	Х	X	Х	High-Z	
READ		L	L	Н	L	ROW	COL	Data Out	
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In	
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L	ROW	COL	Data Out	
READ	2nd Cycle	L	H→L	Н	L	n/a	COL	Data Out	
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In	To the second
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In	
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	Magazina.
RAS-ONLY REFRES	Н	Н	Х	Х	Х	ROW	n/a	High-Z	with the
HIDDEN	READ	L→H→L	L	Н	L	ROW	COL	Data Out	
REFRESH WRITE		L→H→L	L	L	Х	ROW	COL	Data In	
CAS-BEFORE-RAS F	REFRESH	H→L	L	Н	Х	Х	Х	High-Z	
BATTERY BACKUP	REFRESH	H→L	L	Х	Х	Х	Х	High-Z	22

PRESENCE DETECT-INDUSTRY STANDARD

SYMBOL	-6	-7	-8
PRD1	NC	NC	NC
PRD2	NC	NC	NC
PRD3	NC	Vss	NC
PRD4	NC	NC	Vss

PRESENCE DETECT-APPLICATION SPECIFIC

SYMBOL	-6	-7	-8
PRD1	NC	NC	Vss
PRD2	Vss	NC	Vss
PRD3	NC	Vss	Vss
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	55°C to +125°C
Power Dissipation	20W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 26) (0° C $\leq T_A \leq 70^{\circ}$ C; $Vcc = 5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage	Vcc	4.5	5.5	V	1	
Input High (Logic 1) Voltage, All Inputs	Vıн	2.4	Vcc+1	V	1	
Input Low (Logic 0) Voltage, All Inputs		VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT	A0-A9, WE	lı	-40	40	μА	
Any Input $0V \le V_{IN} \le V_{CC}$ (All other pins not under test = 0V) for each package input	RAS, CAS	lı2	-20	20	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vouт ≤ Vcc) for each package input	DQ1-DQ40	loz	-20	20	μА	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Iout = -5mA) Output Low Voltage (Iout = 4.2mA)		Vol		0.4	V	Ī

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles (MIN))	Іссз	40	40	40	mA	
STANDBY CURRENT: CMOS INPUT LEVELS		20	20	20	mA	
Power supply standby current ($\overline{RAS} = \overline{CAS} = Vcc -0.2V$ after 8 \overline{RAS} cycles (MIN)). (All other inputs at $Vcc -0.2V$ or $Vss +0.2V$)	lcc4	4	4	4	mA	22
OPERATING CURRENT	lcc1	1120	1020	920	mA	2, 26
$(\overline{RAS} \text{ and } \overline{CAS} = \text{Cycling: } {}^{t}RC = {}^{t}RC \text{ (MIN))}$		1104	1004	904	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE	lcc2	820	720	620	mA	2, 26
$(\overline{RAS} = V_{IL}, \overline{CAS} = Cycling: {}^{t}PC = {}^{t}PC (MIN))$		804	704	604	mA	2,22,26
REFRESH CURRENT: RAS-ONLY	Icc5	1120	1020	920	mA	2
$(\overline{RAS} = Cycling: \overline{CAS} = V_{IH})$		1104	1004	904	mA	2, 22
REFRESH CURRENT: CAS-BEFORE-RAS	Icc6	1120	1020	920	mA	2, 19
(RAS and CAS = Cycling)		1104	1004	904	mA	2,19,22
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: CAS = 0.2V or CAS-BEFORE-RAS cycling; RAS = ^t RAS (MIN) to 300ns; WE, A0-A9 and Din = Vcc - 0.2V or 0.2V (Din may be left open), ^t RC = 125μs (1,024 rows at 125μs = 128ms)	lcc7	6	6	6	mA	22



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	Cıı	-	128	pF	17
Input Capacitance: WE, OE	Cı2		168	pF	17
Input Capacitance: RAS0, RAS1, CAS0, CAS1	Сіз		84	pF	17
Input/Output Capacitance: DQ1-DQ40	Сю		20	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS			-6	-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	- 11 - 1
READ-WRITE cycle time	^t RWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	
Access time from RAS	†RAC		60		70		80	ns	8
Access time from CAS	†CAC		15		20		20	ns	9
Access time from column address	†AA		30		35		40	ns	
Access time from CAS precharge	^t CPA		35		40		45	ns	
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	15, 14.1
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	^t RP	45		50		60	1 1 1 1 1 1 1	ns	10,130,00
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	#
CAS precharge time	^t CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	31.5	ns	1.42.11.2
RAS to CAS delay time	tRCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	^t CRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
RAS to column address delay time	^t RAD	15	30	15	35	15	40	ns	21
Column address setup time	tASC	0		0		0		ns	
Column address hold time	^t CAH	10		15		15		ns	
Column address hold time (referenced to RAS)	^t AR	50		55		60		ns	
Column address to RAS lead time	^t RAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to CAS)	^t RCH	0		0		0		ns	14
Read command hold time (referenced to RAS)	^t RRH	0		0		0		ns	14
CAS to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	^t OFF	0	20	0	20	0	20	ns	12, 23
WE command setup time	twcs	0		0		0		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($Vcc = 5V \pm 10\%$)

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	
Write command pulse width	^t WP	10		. 15		15		ns	
Write command to RAS lead time	tRWL	15		20		20		ns	
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in setup time	^t DS	0		. 0		0		ns	15
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	
RAS to WE delay time	tRWD	90		100		110		ns	24
Column address to WE delay time	^t AWD	60		65		70		ns	24
CAS to WE delay time	tCWD	45		50		50	1	ns	24
Transition time (rise or fall)	††T	3	50	3	50	3	50	ns	5, 16
Refresh period (1,024 cycles)	tREF		16/128		16/128		16/128	ms	3/22
RAS to CAS precharge time	tRPC	0		0		0		ns	19
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	15		15		15	'	ns	19
OE setup prior to RAS during HIDDEN REFRESH cycle	^t ORD	0		0		0		ns	20
Output disable	tOD	15		20		20		ns	23
Output enable	^t OE	15	1	20		20		ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	15		20		20		ns	25

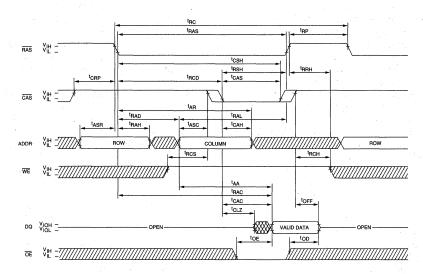


NOTES

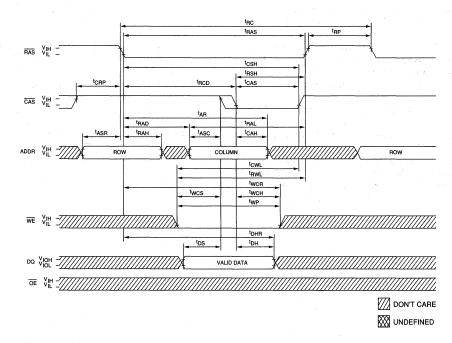
- All voltages referenced to Vss.
- 2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
- 3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 16ms (128ms L version) refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- 5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq T_A \leq 70°C) is assured.
- 7. Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- Assumes that ^tRCD ≥ ^tRCD (MAX).
- 10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 11. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 12. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 14. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 15. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles.
- 16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.

- 17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V @ 15mV RMS).
- 18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^tCP.
- 19. On-chip refresh and address counters are enabled.
- 20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 21. Operation within the ^tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 22. L version only.
- 23. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \ge {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.
- 24. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 25. Icc is dependent on cycle rates.
- 26. All other inputs at Vcc -0.2V.

READ CYCLE

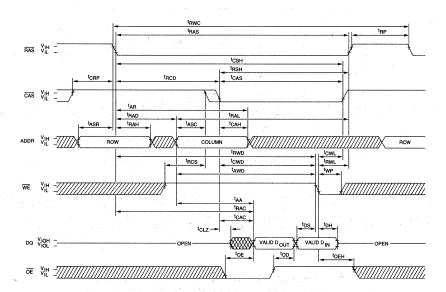


EARLY-WRITE CYCLE

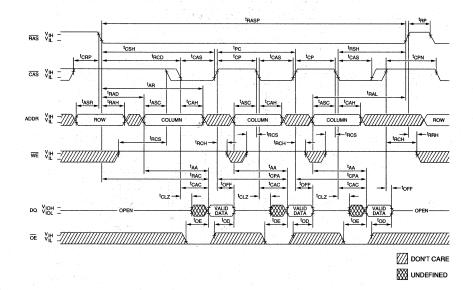




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

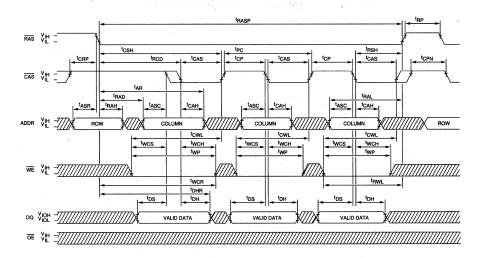


FAST-PAGE-MODE READ CYCLE

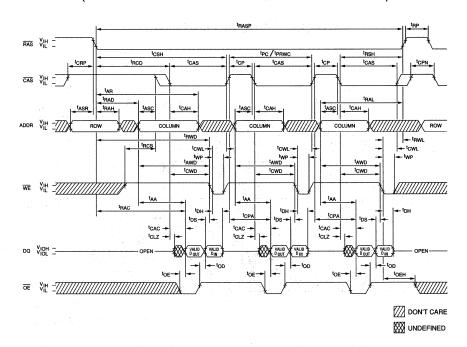




FAST-PAGE-MODE EARLY-WRITE CYCLE



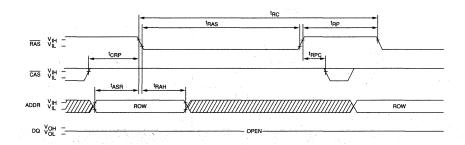
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)





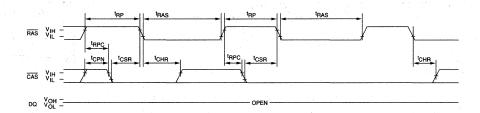
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; and \overline{WE} = DON'T CARE)



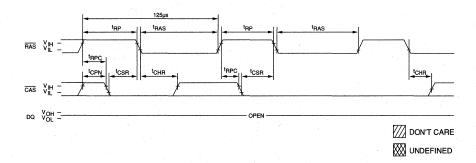
CAS-BEFORE-RAS REFRESH CYCLE

 $(A0-A9, \overline{OE} = DON'T CARE)$



BATTERY BACKUP REFRESH CYCLE 22

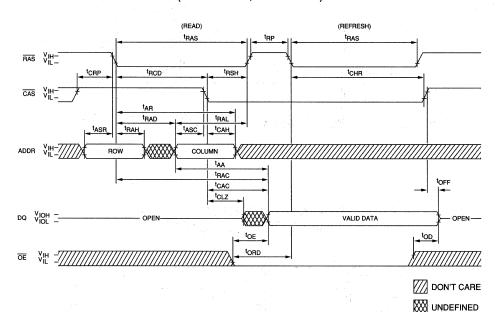
(WE = DON'T CARE)





HIDDEN REFRESH CYCLE 20

 $(\overline{WE} = HIGH; \overline{OE} = LOW)$



MCRON TECHNOLOGY, INC.

DYNAMIC RAMS	1
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9



IC DRAM CARD SELECTION GUIDE

Memory		Part	Access	Number of Pins	
Configuration		Number	Time (ns)	Card	Page
512K x 16	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
1 Meg x 16	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
2 Meg x 16	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
4 Meg x 16	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
512K x 18	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
1 Meg x 18	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
2 Meg x 18	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
4 Meg x 18	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
512K x 20	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
1 Meg x 20	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
2 Meg x 20	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
4 Meg x 20	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169
256K x 32	1 Megabyte	MT8D88C25632	60, 70, 80	88	4-1
512K x 32	2 Megabytes	MT16D88C51232	60, 70, 80	88	4-17
1 Meg x 32	4 Megabytes	MT8D88C132	60, 70, 80	88	4-33
2 Meg x 32	8 Megabytes	MT16D88C232	60, 70, 80	88	4-49
256K x 36	1 Megabyte	MT12D88C25636	60, 70, 80	88	4-65
512K x 36	2 Megabytes	MT24D88C51236	60, 70, 80	88	4-79
1 Meg x 36	4 Megabytes	MT12D88C136	60, 70, 80	88	4-93
2 Meg x 36	8 Megabytes	MT24D88C236	60, 70, 80	88	4-107
256K x 40	1 Megabyte	MT12D88C25640	60, 70, 80	88	4-121
512K x 40	2 Megabytes	MT24D88C51240	60, 70, 80	88	4-137
1 Meg x 40	4 Megabytes	MT12D88C140	60, 70, 80	88	4-153
2 Meg x 40	8 Megabytes	MT24D88C240	60, 70, 80	88	4-169



IC DRAM CARD

1 MEGABYTE

256K x 32, 512K x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- · Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16 or x32 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 8mW standby, 1.8W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS

MARKING

Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT8D88C25632 is a 1 megabyte, IC DRAM card organized as a 256K x 32 bit memory array. It may also be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{\text{CAS}}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT8D88C25632 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

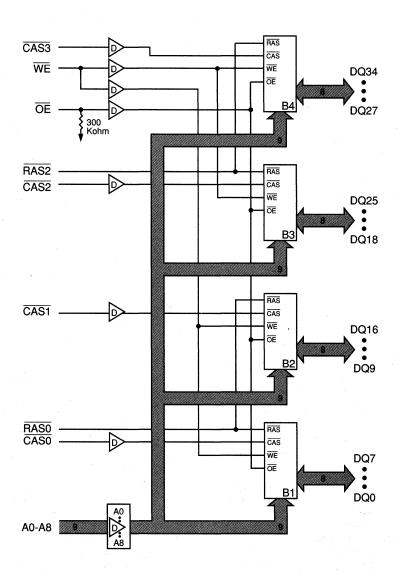


	\sqcap		PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	00	45	1	Vss	31	NC	61	NC
3		46	2	DQ0	32	NC	62	NC
4		47 48	3	DQ1	33	NC	63	Vss
4 5 6 7		49 50	4	DQ2	34	DQ9	64	NC
7	۱ Š	51	5	DQ3	35	NC	65	NC
9	80	52 53	6	DQ4	36	DQ10	66	CAS2
10	20	54	7	DQ5	37	Vcc	67	Vss
12	ŏ	55 56	8	DQ6	38	DQ11	68	CAS3
13 14	80	57	9	Vcc	39	DQ12	69	NC
15	ŏ	58 59	10	DQ7	40	DQ13	70	WE
16 17	000000000000000000000000000000000000000	60	11	NC	41	DQ14	71	PD1 (Vss
18 19	08 08	61 62	12	NC	42	DQ15	72	PD3 (Vss
20		63 64	13	A0	43	DQ16	73	Vss
21 22	88	65	14	A2	44	Vss	74	PD5 (NC
23	8	66 67	15	Vcc	45	Vss	75	PD7 (TBD
24 25	80	68	16	A4	46	DQ18	76	PD8 (NC
26	ŏ8	69 70	17	NC	47	DQ19	77	NC
27 28	80	71	18	A6	48	DQ20	78	NC
29	ŏö	72 73	19	A8	49	DQ21	79	NC
30 31		74	20	NC	50	DQ22	80	DQ27
32 33	Š	75 76	21	NC	51	DQ23	81	DQ28
34		77 78	22	RAS0	52	DQ24	82	DQ29
35 36	80	79	23	CASO CASO	53	DQ25	83	DQ30
37	ŏ	80 81	24	CAS1	54	NC	84	DQ31
38 39	80	82	25	NC	55	OE (Vss)	85	DQ32
40	ŏ8	83 84	26	RAS2	56	Vss	86	DQ33
41	88	85	27	Vcc	57	A1	87	DQ34
43	00000000000000000000000000000000000000	86 87	28	PD2 (Vss)	58	A3	88	Vss
44	00	88	29	PD4 (Vss)	59	A5		
		I	30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT8D88C25632 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT8D88C25632 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 through B4 = 256K x 8 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RASO, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits. Two RAS inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	CAS ₀₋₃	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	ŌĒ	Input	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 61, 62, 64, 65, 69, 77, 78, 79	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

The MT8D88C25632 is a 1 megabyte memory card structured as a 256K x 32 bit memory array ($\overline{RAS0} = \overline{RAS2}$). It also may be configured as a 512K x 16 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32 bit applications use the same signal to control the CAS inputs. RASO controls the lower 16 bits, and RAS2 controls the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the 512K x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of \overline{RAS} addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the $\overline{\mathrm{WE}}$ input. A logic HIGH on $\overline{\mathrm{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if \overline{WE} goes LOW after \overline{CAS} , the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT8D88C25632 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, eight thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT8D88C25632 operates reliably up to 55°C.



MEMORY TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	tC	DQ0-DQ34
Standby		Н	H→X	Х	×	X	Х	High-Z
READ	1 4 5	L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	X	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	5 - L 1-2	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	ő Ļu	X	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Χ	Χ	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	CTERISTICS	3				-	PRESE	NT DE	TECT P	IN (PD:	x)	
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	X	NC	NC	NC	NC	NC	Х	Х	Х
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NO	Х	Х	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	Х	X	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X X	X
Access Timi	ing .		10	0ns		Х	Х	Х	Х	Х	Vss	Vss	X
			80)ns		Х	Х	Х	X	Х	NC	Vss	Х
			70)ns	1. 1869	Х	Х	Х	Х	Х	Vss	NC	X
		11.00	60)ns		Х	Х	Х	X	Х	NC	NC	X
			50)ns		X	Х	Х	X	Х	Vss	Vss	Х
Refresh Con	itrol		Standard			Х	Х	Х	Х	Х	Х	Х	NC
			Auto			Х	х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = 0V)	Buffered	Ів	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	ουτ ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	1 1 1 1
Output High Voltage (lout = -5mA) Output Low Voltage (lout = 4.2mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	16	16	16	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	1.6	1.6	1.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	680	600	520	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _I L, CAS, Address Cycling: ¹PC = ¹PC (MIN))	lcc4	520	440	360	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih: tRC = tRC (MIN))	lcc5	680	600	520	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	680	600	520	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125μs; WE, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	1.6	1.6	1.6	mA	3,5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A8, OE	Cıı		9	pF	2
Input Capacitance: WE	Cı2		13	pF	2
Input Capacitance: RASO, RAS2	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110	7 7 7 7 7 7 8	130		150		ns	23
FAST-PAGE-MODE	tPC	40		40		45		ns	23
READ or WRITE cycle time									
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	†CAC		25	100	30		30	ns	15, 26
Access time from column address	tAA.		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	†RSH	25		30		30		ns	26
RAS precharge time	^t RP	40		50		60		ns	23
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65	A In Cathern	75	alisi bali	ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10	1. Fit 1, 12 1	10		10		ns	23
RAS to CAS delay time	^t RCD	10	35	15	40	15	- 50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	^t ASR	10		10		10		ns	26
Row address hold time	†RAH	5		5	Jack Park	5		ns	25
RAS to column address delay time	†RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	†ASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	†RAL	40		45		50		ns	26
Read command setup time	†RCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	tRRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5	1 1 1 1 1 1 1	5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to RAS)	tWCR	. 40		50		55		ns	25
Write command pulse width	^t WP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	^t CWL	20		25		25		ns	24
Data-in setup time	^t DS	5	1 40 0	5		5	3 A	ns	24, 32
Data-in hold time	^t DH	5		10		10	1 1 1 1	ns	25, 32
Data-in hold time (referenced to RAS)	†DHR	45		55	•	60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF.		128	100	128		128	ms	
RAS to CAS precharge time	^t RPC	10		10		10	A COL	ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20	:	20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5	;	5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	[†] WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	^t WTH	5		5	1 - 44 g	5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	†RWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100	(a. 8)	ns	23
RAS to WE delay time	^t RWD	80		90		100		ns	31, 27
Column Address to WE delay time	^t AWD	65		70	ala g	75	V 19 V 2	ns	31, 24
CAS to WE delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^t OE		25		30		30	ns	20, 33, 26
Output disable	^t OD		25		30	D	30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	5		10		10	44	ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	^t ORD	10		10		10	1.00	ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between $V_{\rm III}$ and $V_{\rm III}$ (or between $V_{\rm II}$ and $V_{\rm III}$) in a monotonic manner.
- 11. If $\overline{\text{CAS}} = \text{ViH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one half when used in the x16 mode.
- 31. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

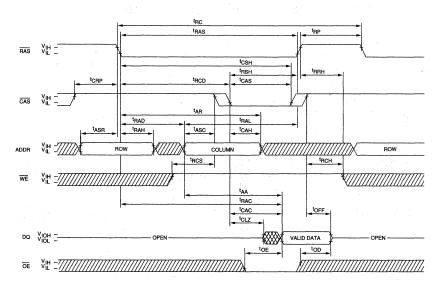


NOTES (continued)

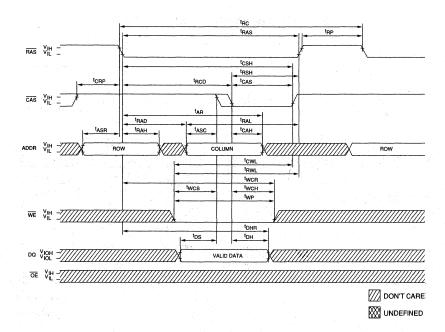
- 32. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 33. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If \overline{OE} goes HIGH and \overline{CAS} stays LOW, \overline{OE} is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while $\overline{\text{CAS}}$ remains LOW).



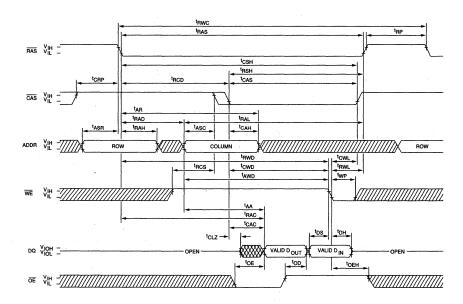
READ CYCLE



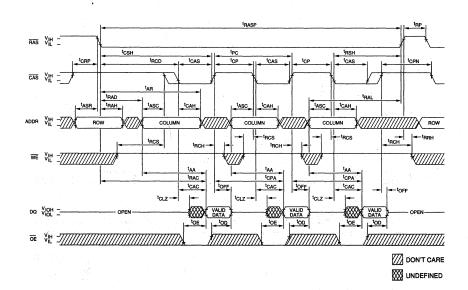
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

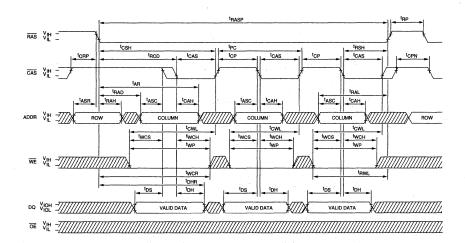


FAST-PAGE-MODE READ CYCLE

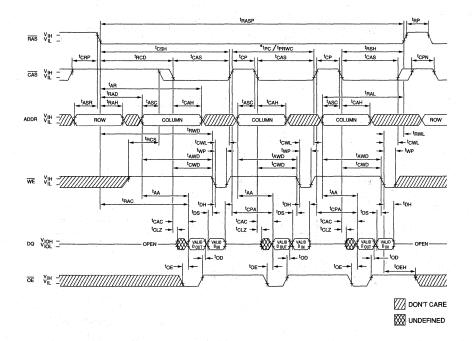




FAST-PAGE-MODE EARLY-WRITE CYCLE

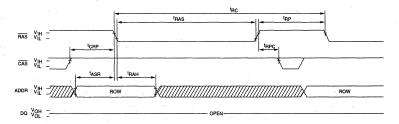


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



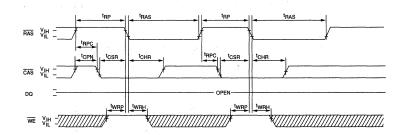
RAS-ONLY REFRESH CYCLE





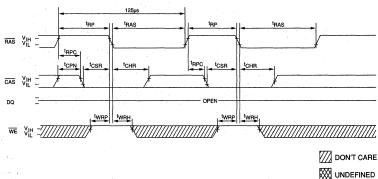
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8 = DON'T CARE)



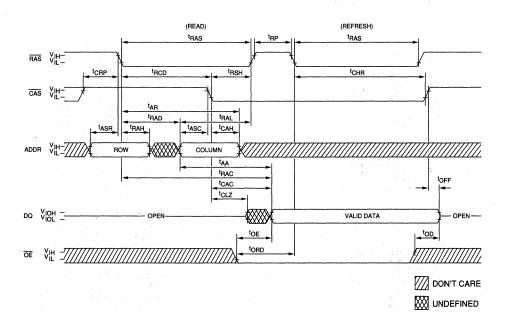
BATTERY BACKUP REFRESH CYCLE

(A0-A8 = DON'T CARE)





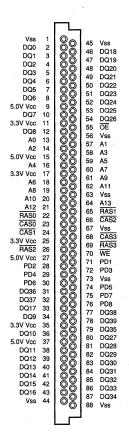
HIDDEN REFRESH CYCLE 21 (WE = HIGH)

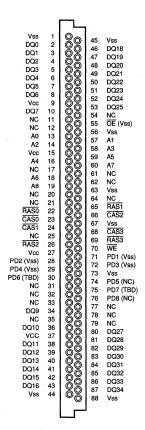


RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)

MT8D88C25632 PIN ASSIGNMENT (JEDEC Standard)







IC DRAM CARD

2 MEGABYTES

512K x 32, 1 MEG x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- · All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16 or x32 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 16mW standby, 1.8W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS

MARKING

•	Timing		
	60ns access		-6
	70ns access		-7
	80ns access		-8

GENERAL DESCRIPTION

The MT16D88C51232 is a 2 megabyte, IC DRAM card organized as a 512K x 32 bit memory array. It may also be configured as a 1 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT16D88C51232 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32 organization, the memory array may be divided into two banks, each with four separate bytes. In the x16 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

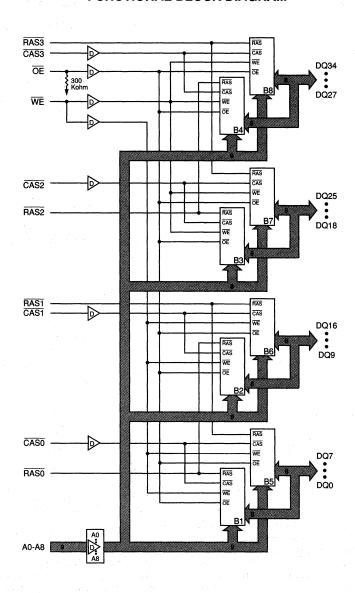


		Court of	01/11001	DIN #	OVIEDOL	DIN #	01/140.01
اما	Ė	PIN#	SYMBOL	PIN #	SYMBOL	PIN#	SYMBOL
2 0	0 45 0 46	1	Vss	31	NC	61	NC
3 Ø	O 46	2	DQ0	32	NC	62	NC
4 0	0 47 48 49 50 50 51	3	DQ1	33	NC	63	Vss
6 0	O 49 O 50	4	DQ2	34	DQ9	64	NC
5 0 6 0 7 0 8 0	Š 51	5	DQ3	35	NC	65	RAS1
. O	© 52 © 53	6	DQ4	36	DQ10	66	CAS2
10 0	O 54	7	DQ5	37	Vcc	67	Vss
12 0	O 55 O 56	- 8	DQ6	38	DQ11	68	CAS3
13 0	O 57	9	Vcc	39	DQ12	69	RAS3
15 0	O 58	10	DQ7	40	DQ13	70	WE
9 0 10 0 11 0 12 0 13 14 0 15 0 16 0 17 0 18 0 19 0 20 0	56 57 58 59 60 61 62 63 64 65 66 67	111	NC	41	DQ14	71	PD1 (Vss)
18 0	0 62	12	NC	42	DQ15	72	PD3 (Vss)
20 0	0 63 0 64	13	A0	43	DQ16	73	Vss
21 0	Ø 65	14	A2	44	Vss	74	PD5 (Vss)
23 0	0 66 0 67	15	Vcc	45	Vss	75	PD7 (TBD)
24 ©	O 68	16	A4	46	DQ18	76	PD8 (NC)
26 Ö	0 69 0 70	17	NC	47	DQ19	77	NC
27 0	Ď 71	18	A6	48	DQ20	78	NC
29 0	72 73	19	A8	49	DQ21	79	NC
30 ©	Ō 74	20	NC	50	DQ22	80	DQ27
32 0 33 0	0 75 0 76	21	NC	51	DQ23	81	DQ28
34 0	0 76 0 77 0 78	22	RAS0	52	DQ24	82	DQ29
35 0	D 79	23	CAS0	53	DQ25	83	DQ30
21	0 80 81 0 82 0 83 0 84 0 85	24	CAS1	54	NC	84	DQ31
38 ©	82	25	NC	55	OE (Vss)	85	DQ32
40 0	0 83 0 84	26	RAS2	56	Vss	86	DQ33
41 0 42 0	85	27	Vcc	57	A1	87	DQ34
43 0	0 86 0 87	28	PD2 (Vss)	58	A3	88	Vss
44 ©	Š 88	29	PD4 (Vss)	59	A5		
		30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT16D88C51232 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT16D88C51232 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 through B8 = 256K x 8 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION					
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 9 row- address bits. Four RAS inputs allow for two x32 banks or four x16 banks.					
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.					
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.					
55	ŌĒ	Input	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.					
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.					
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.					
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).					
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 61, 62, 64, 77, 78, 79	NC		No Connect: These pins should be left unconnected (reserved for future use).					
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%					
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground					

FUNCTIONAL DESCRIPTION

The MT16D88C51232 is a 2 megabyte memory card structured as a 512K x 32 bit memory array ($\overline{RAS0} = \overline{RAS2}$ RAS1 = RAS3). It also may be configured as a 1 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four RAS lines.

Most x32 bit applications use the same signal to control the CAS inputs. RASO and RAS1 control the lower 16 bits, and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding \overline{CAS} pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the 1 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if WE goes LOW after CAS, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE- WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the ICDRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems which use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT16D88C51232 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 16 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT16D88C51232 operates reliably up to 55°C.



MEMORY TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	OE	t _R	tC.	DQ0-DQ34
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ		L	: L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	⊶ H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L s	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	Х	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L (NC)	ROW	COL	Data Out
REFRESH WRITE		L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z
BATTERY BACKUP REFRESH		H→L	L	Н	Х	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	TERISTICS	3			PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	Х	Х	Χ
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	Х	Х	Х
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X	X X	X X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X X	X X	X X
Access Timi	ng in the second		10	0ns		Х	Х	Χ	Х	Х	Vss	Vss	Х
			80	ns		X	Х	Х	Х	X	NC	Vss	Х
			70)ns		Х	Х	Х	Х	Х	Vss	NC	Х
			60ns			Х	Х	Х	Х	Х	NC	NC	Х
		50ns				Х	Х	Х	Х	Х	Vss	Vss	Х
Refresh Con	trol		Standard				Х	Х	Х	Х	Х	Х	NC
		Auto				Х	Х	Х	Χ	Х	Х	Х	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss.	0.5V to +5.25V
Operating Temperature, T _A (Ambient)	0°C to +55°C
Storage Temperature	
Power Dissipation	
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = 0V)	Buffered	lв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	о́от ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Iouт = -5mA) Output Low Voltage (Iouт = 4.2mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	32	32	32	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	3.2	3.2	3.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	680	600	520	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	520	440	360	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: RC = RC (MIN))	lcc5	680	600	520	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icce	680	600	520	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR						
cycling; \overline{RAS} = ${}^{t}RAS$ (MIN) up to 300ns; ${}^{t}RC$ = 125 μ s; \overline{WE} , A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	Icc7	3.2	3.2	3.2	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A8, OE	Cii		9	pF	2
Input Capacitance: WE	Cı2		13	pF	2
Input Capacitance: RASO, RAS1, RAS2, RAS3	Сіз	1.1	50	pF	2
Input/Output Capacitance: DQ	Cio		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS	-6		-7			-8	1 1 1		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time									
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	†AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	^t RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	25		30		30		ns	26
RAS precharge time	^t RP	40		50		60		ns	23
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10		10	1	ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	tCRP	15		15		15		ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	†RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	tASC	5		5		5	100	ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50	Note that	ns	26
Read command setup time	†RCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	†CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5	1., 4.45	5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS	I	-	6	-	7		-8	1.	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time	tWCR	40		50		55		ns	25
(referenced to RAS)							10 133		
Write command pulse width	^t WP	10		15		15		ns	23
Write command to RAS lead time	tRWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	^t DH	5		10		10		ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tT.	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	7.5
RAS to CAS precharge time	^t RPC	10		. 10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20	·	20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^t RWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE: cycle time	^t PRWC	90		95		100		ns	23
RAS to WE delay time	tRWD	80		90		100		ns	31, 27
Column Address to WE delay time	^t AWD	65	, as	70		75		ns	31, 24
CAS to WE delay time	^t CWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^t OE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	5		10		10		ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	^t ORD	10	:	10		10		ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $VCC = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

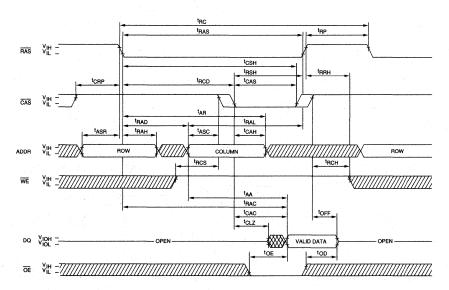
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- Timing between the DRAMs and the DRAM card did not change with addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM Card resulted from the addition of line drivers.
- 30. The maximum current ratings are based on one of the two banks operating or being refreshed (x32 mode). The stated maximums may be reduced by one half when used in the x16 mode. Standby currents of nonactive bank is not included.
- 31. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

NOTES (continued)

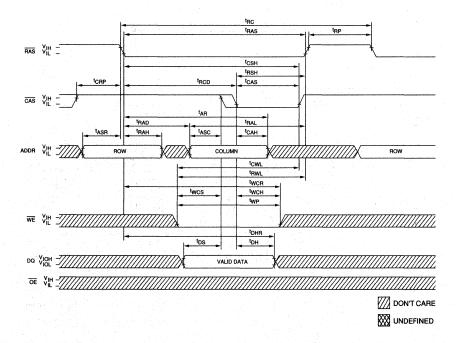
- 32. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and \overline{OE} is taken back LOW after ^tOEH is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



READ CYCLE

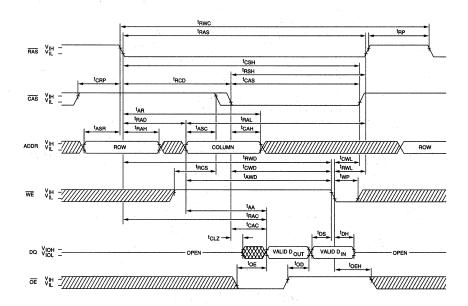


EARLY-WRITE CYCLE

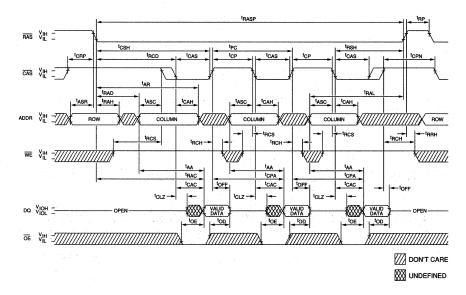




READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

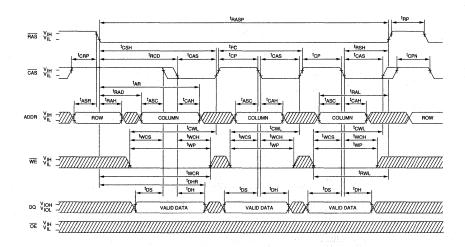


FAST-PAGE-MODE READ CYCLE

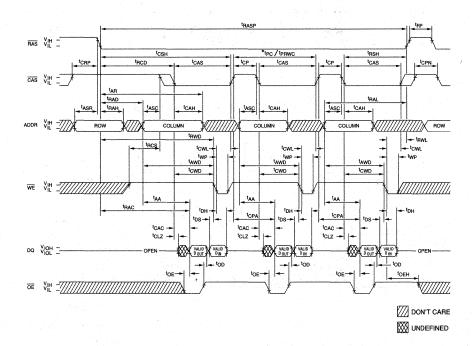




FAST-PAGE-MODE EARLY-WRITE CYCLE

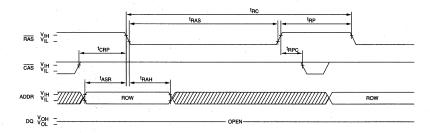


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



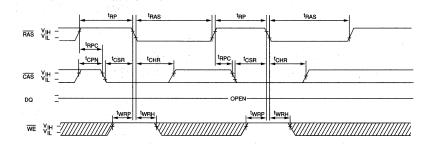
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A8; WE = DON'T CARE)



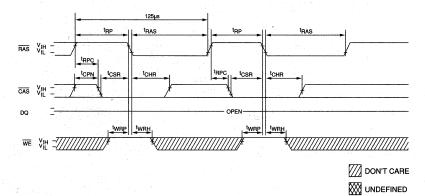
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8 = DON'T CARE)



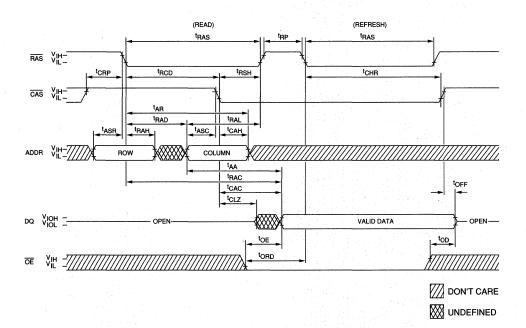
BATTERY BACKUP REFRESH CYCLE

(A0-A8 = DON'T CARE)





HIDDEN REFRESH CYCLE 21 (WE = HIGH)



RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)

45 Vss DQ0 46 47 DQ18 DQ1 DQ2 48 DQ20 DQ3 49 50 DQ21 DQ22 DQ4 DQ5 51 52 DQ23 DQ6 DQ24 5.0V Vcc DQ7 53 DQ25 10 54 55 56 57 58 59 DQ26 OE 3.3V Vcc 11 DQ8 Vss **A2** АЗ 5.0V Vcc A4 60 3.3V Vcc 61 62 63 64 Α9 A6 A8 A11 Vss A10 A12 RAS0 CAS0 21 22 23 65 CAS₂ 67 68 69 Vss CAS3 CAS1 3.3V Vcc RAS3 RAS2 70 27 28 29 5.0V Vcc PD2 72 73 74 75 76 PD3 PD4 Vss PD6 PD5 DQ36 PD7 DQ37 DQ17 DQ9 32 33 34 PD8 78 DQ39 3.3V Vcc 35 36 79 DQ35 DQ10 80 DQ27 5.0V Vcc 37 81 DQ28 DQ11 38 82 DQ29 DQ12 39 DQ13 40 83 40 41 DQ31 DQ14 85 DQ32 86 DO33 DQ16 43 87 DQ34

MT16D88C51232 PIN ASSIGNMENT

(JEDEC Standard)

	1			
Vss DQ0 DQ11 DQ2 DQ3 DQ3 DQ4 DQ5 DQ6 V6c DQ7 NC NC A0 A2 V6c CA4 NC RA50 CA50 CA51 NC NC RA50 CA51 NC NC RA50 CA51 NC NC DQ7 NC NC DQ1 DQ1 V6c DQ1 V6c DQ10 V6c DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 Vss	1 2 3 4 4 5 6 7 8 9 10 11 12 13 14 15 6 17 18 19 20 1 22 23 4 25 5 27 28 9 33 33 34 4 4 4 4 4 4 4 4 4 4 4 4 4 4	000000000000000000000000000000000000000	45 46 47 48 49 50 51 52 53 54 55 66 61 62 63 64 65 66 67 70 71 72 73 74 75 77 77 78 88 88 88 88 88 88 88 88 88 88	Vss D018 D0219 D0220 D0221 D0222 D0223 D0225 D025 D025 D025 D025 D025 D025 D02



IC DRAM CARD

4 MEGABYTES

1 MEG x 32, 2 MEG x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- · All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16 or x32 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 8mW standby, 2.2W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS

MARKING

• Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT8D88C132 is a 4 megabyte, IC DRAM card organized as a 1 Meg x 32 bit memory array. It may also be configured as a 2 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when as compared to standard DRAMs.

The MT8D88C132 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

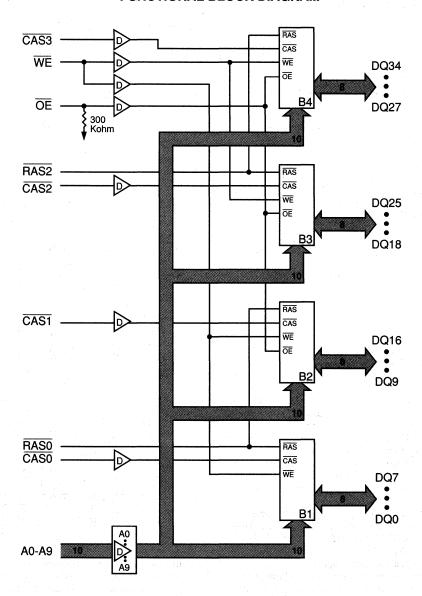


ᅩ	i	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
00	45	1	Vss	31	NC	61	A9
8	46 47	2	DQ0	32	NC	62	NC
88	48	3	DQ1	33	NC	63	Vss
000000	49 50	4	DQ2	34	DQ9	64	NC
	51	5	DQ3	35	NC	65	NC
	52 53	6	DQ4	36	DQ10	66	CAS2
₹ŏ	54	7	DQ5	37	Vcc	67	Vss
	55 56	8	DQ6	38	DQ11	68	CAS3
	57	9	Vcc	39	DQ12	69	NC
000000000000000000000000000000000000000	58 59	10	DQ7	40	DQ13	70	WE
Ø.	60 61	11	NC	41	DQ14	71	PD1 (Vss)
0	62	12	NC	42	DQ15	72	PD3 (Vss)
<u></u>	63 64	13	A0	43	DQ16	73	Vss
5	65	14	A2	44	Vss	74	PD5 (NC)
	66 67	15	Vcc	45	Vss	75	PD7 (TBD)
3	68	16	A4	46	DQ18	76	PD8 (NC)
	69 70	17	NC	47	DQ19	77	NC
5	71	18	A6	48	DQ20	78	NC
0	72 73	19	A8	49	DQ21	79	NC
ğ	74	20	NC	50	DQ22	80	DQ27
0	75 76	21	NC	51	DQ23	81	DQ28
Ŏ.	77	22	RAS0	52	DQ24	82	DQ29
0	78 79	23	CAS0	53	DQ25	83	DQ30
0	80 81	24	CAS1	54	NC	84	DQ31
ŏ	82	25	NC	55	OE (Vss)	85	DQ32
0	83 84	26	RAS2	56	Vss	86	DQ33
	85	27	Vcc	57	A1	87	DQ34
000	86 87	28	PD2 (NC)	58	A3	88	Vss
ŏ	88	29	PD4 (Vss)	59	A5		
_	ı	30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT8D88C132 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT8D88C132 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 through B4 = 1 Meg x 8 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION					
22, 26	RASO, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. TwoRAS inputs allow for a single x32 bank or two x16 banks.					
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.					
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.					
55	ŌĒ	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.						
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.					
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.					
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).					
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 62, 64, 65, 69, 77, 78, 79	NC		No Connect: These pins should be left unconnected (reserved for future use).					
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%					
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground					

FUNCTIONAL DESCRIPTION

The MT8D88C132 is a 4 megabyte memory card as a 1 Meg x 32 bit memory array ($\overline{RAS0} = \overline{RAS2}$). It also may be configured as a 2 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32 bit applications use the same signal to control the CAS inputs. RASO controls the lower 16 bits and RAS2 controls the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and CAS0 to CAS2 and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the 2 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (ICC7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the ICDRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems which use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT8D88C132 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, eight thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT8D88C132 operates reliably up to 55°C.



MEMORY TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	tC	DQ0-DQ34
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ		L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	e L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	Х	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	Х	X	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARA	CTERISTICS	3				11	PRESE	NT DE	TECT P	IN (PD	x)	
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6.	7	8
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
1MB 2MB	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18	18 18	9 9	9 9	512 512	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X X	X	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1.024	Vss	NO	Vss	Vss	NO	X	Х	
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	X	Х	Х
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Timi	ng, a la sasa, ti sa sa sa sa sa sa sa sa sa sa sa sa sa		10	0ns		Х	Х	Х	Х	Х	Vss	Vss	X
			80)ns		Х	Х	Х	Х	Х	NC	Vss	Х
			70)ns		Х	Х	Х	Х	Х	Vss	NC	X
			60	ns		Х	Х	Х	Х	Х	NC	NC.	Х
			50)ns		Х	Х	Х	Х	Х	Vss	Vss	Х
Refresh Con	trol		Star	ndard		Х	Х	Х	Х	Х	Х	Х	NC
			Αι	uto		Х	Х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss0.5	5V to +5.25V
Operating Temperature, T _A (Ambient)	0°C to +55°C
Storage Temperature20	0°C to +80°C
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)	10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 55^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		VIH	3.5	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	V	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = $0V$)	Buffered	Ів	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	о́от ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 4.2mA)		Vol		0.4	V	

			MAX		1	2	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	16	16	16	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	1.6	1.6	1.6	mA		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	840	760	680	mA	3, 4, 30	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ⁴PC = ⁴PC (MIN))	Icc4	600	520	440	mA	3, 4, 30	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: RC = RC (MIN))	lcc5	840	760	680	mA	3, 30	
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	Icc6	840	760	680	mA	3, 5, 30	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125μs; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	2.4	2.4	2.4	mA	3, 5	



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A9, OE	CI1	1.1	9	pF	2
Input Capacitance: WE	C ₁₂		13	pF	2
Input Capacitance: RASO, RAS2	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS			-6	-7			-8		1000
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time			1				No.		
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	tCAC		25		30		30	ns	15, 26
Access time from column address	†AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	tRP	45		50		60		ns	23
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	55	1.	65	1 9 14 1 3 4 1	75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10	1	10		10		ns	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15	7.	ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	†RAH	5		5		5		ns	25
RAS to column address delay time	^t RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	tASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	¹AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	†RCS	5	1	5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5	1	5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-	6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time	†WCR	40		50		55	1	ns	25
(referenced to RAS)					į		1		
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	†CWL	20		25		25		ns	24
Data-in setup time	^t DS	5		5		5		ns	24, 32
Data-in hold time	^t DH	5		10		10		ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	
RAS to CAS precharge time	^t RPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	[†] CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	[†] WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	^t WTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	†RWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	23
RAS to WE delay time	^t RWD	80		90		100		ns	31, 27
Column Address to WE delay time	^t AWD	65		70		. 75		ns	31, 24
CAS to WE delay time	†CWD	50		65		55		ns	31, 24
Output buffer turn-off delay	[†] OE		25		30		30	ns	20, 33, 26
Output disable	^t OD		25		30		30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	5		10		10		ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	^t ORD	10		10		10		ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

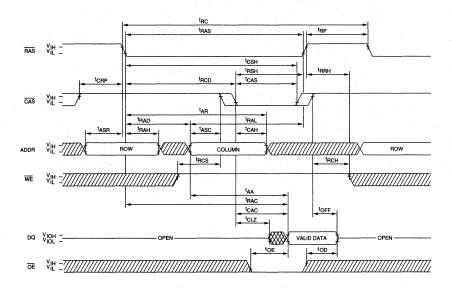
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one half when used in the x16 mode.
- 31. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \ge {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

NOTES (continued)

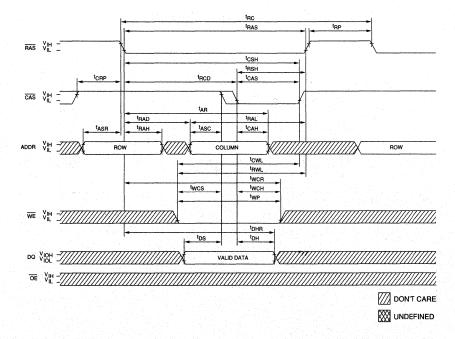
- 32. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and \overline{OE} is taken back LOW after ^tOEH is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



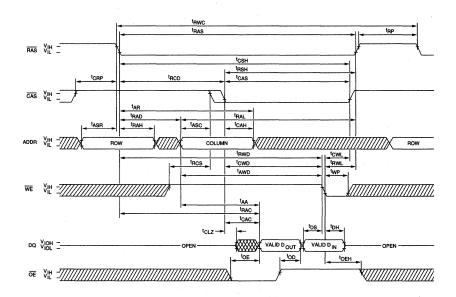
READ CYCLE



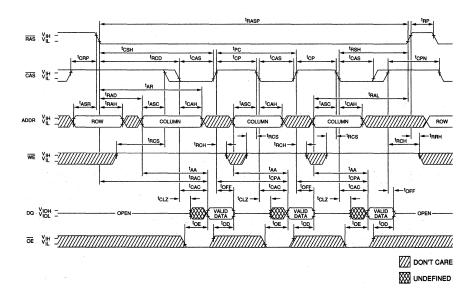
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

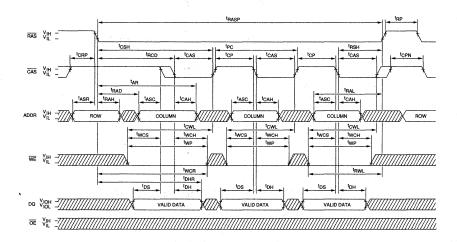


FAST-PAGE-MODE READ CYCLE

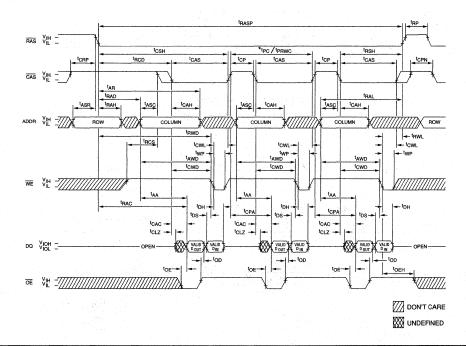




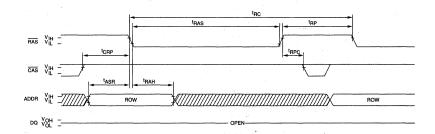
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

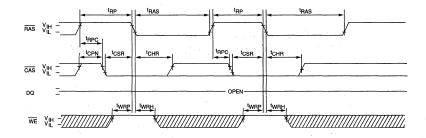


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



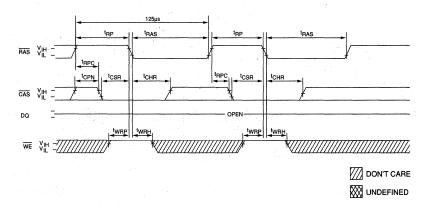
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE

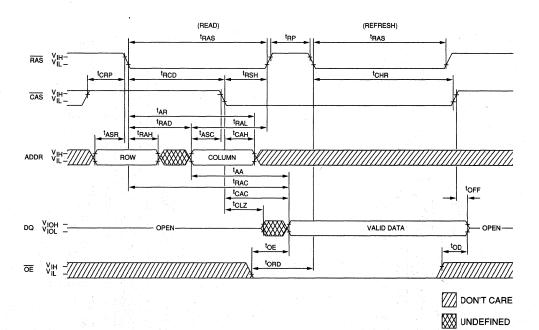
(A0-A9 = DON'T CARE)





HIDDEN REFRESH CYCLE 21

 $(\overline{WE} = HIGH)$



RESERVED JEDEC, JEIDA and PCMCIA **88-PIN ASSIGNMENT**

(All Possible Combinations)

Vss DQ0 DQ18 46 47 DQ1 DQ19 DQ20 48 DQ3 49 DQ21 DQ4 50 51 DQ22 DQ5 DQ6 52 53 54 55 56 57 58 59 60 61 DQ24 5.0V Vcc DQ25 DQ7 DQ26 OE 3.3V Vcc DQ8 12 Vss 13 14 A0 A2 A3 A5 A7 A9 15 5.0V Vcc 16 3.3V Vcc A6 18 19 20 21 22 23 24 25 26 62 A11 **A8** 63 64 65 66 67 68 A10 A12 RAS0 A13 RAS1 CAS2 CAS0 CAS1 Vss CAS3 RAS3 3.3V Vcc RAS2 69 70 71 72 73 74 75 WE 5.0V Vcc 27 PD1 PD2 28 PD3 PD4 PD6 29 30 31 32 33 Vss PD5 DQ36 DQ37 PD7 76 77 78 79 PD8 DQ17 DQ38 DQ9 34 DQ39 3.3V Vcc 35 DQ35 DQ10 36 5.0V Vcc 37 DQ11 38 80 DQ27 81 DQ28 82 83 84 85 DQ12 39 DQ30 DQ13 40 DQ31 DQ32 DQ14 41 DQ15 42 86 DQ33 DQ16 43 Vss 44

MT8D88C132 PIN ASSIGNMENT (JEDEC Standard)

| Vss DQ0 2 DQ1 3 DQ1 3 DQ1 4 DQ15 4 DQ16 4 DQ15 4 DQ16 000000000000000000000000000000000000000 | 56 Vsc
57 A1
58 A3
59 A5
60 A7
61 A9
62 NC
63 Vsc
64 NC
65 NC
66 CA
67 Vsc
68 CA
69 NC
70 WE
71 PD
72 PD
73 Vsc
74 PD | 118 119 120 121 121 121 121 121 121 121 121 121 | | | | | | | | |
|---|---|---|---|--|--|--|--|--|--|--|--|



IC DRAM CARD

8 MEGABYTES

2 MEG x 32, 4 MEG x 16

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16 or x32 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 16mW standby, 2.2W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS

MARKING

• Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT16D88C232 is an 8 megabyte, IC DRAM card organized as a 2 Meg x 32 bit memory array. It may also be configured as a 4 Meg x 16 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate $\overline{\text{CAS}}$ inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT16D88C232 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple \overline{RAS} inputs conserve power by allowing individual bank selection. In the x32 organization, the memory array may be divided into two banks, each with four separate bytes. In the x16 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each \overline{RAS} selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

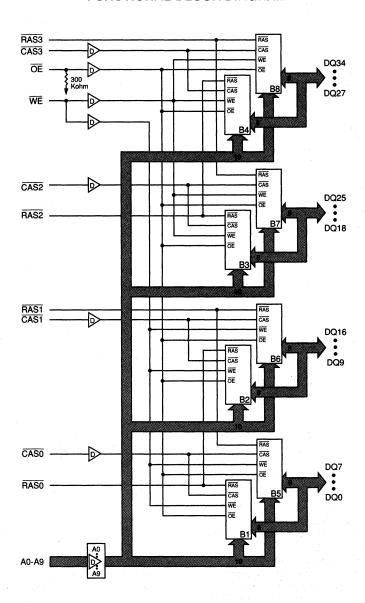


ا ب	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
Q _Q 45	1	Vss	31	NC	61	A9
00 46 00 47	2	DQ0	32	NC	62	NC
20 46 A	3	DQ1	33	NC	63	Vss
0 49 0 50	4	DQ2	34	DQ9	64	NC
20 51 B	5	DQ3	35	NC	65	RAS1
00 51 00 52 00 53	6	DQ4	36	DQ10	66	CAS2
00 54 00 54	7	DQ5	37	Vcc	67	Vss
© 55 0 56	8	DQ6	38	DQ11	68	CAS3
57	9	Vcc	39	DQ12	69	RAS3
0 58 0 59 0 60	10	DQ7	40	DQ13	70	WE
00 61 00 61	11	NC	41	DQ14	71	PD1 (Vss)
	12	NC	42	DQ15	72	PD3 (Vss)
0 62 0 63 0 64	13	A0	43	DQ16	73	Vss
65	14	A2	44	Vss	74	PD5 (Vss)
0 66 67	15	Vcc	45	Vss	75	PD7 (TBD)
Ø 66	16	A4	46	DQ18	76	PD8 (NC)
0 69 0 70	17	NC	47	DQ19	77	NC
71	18	A6	48	DQ20	78	NC
) 72) 73	19	A8	49	DQ21	79	NC
74	20	NC	50	DQ22	80	DQ27
76	21	NC	51	DQ23	81	DQ28
77 78	22	RAS0	52	DQ24	82	DQ29
79	23	CASO CASO	53	DQ25	83	DQ30
O 80 O 81	24	CAS1	54	NC	84	DQ31
0 80 81 0 82	25	NC.	55	OE (Vss)	85	DQ32
0 83 0 84	26	RAS2	56	Vss	86	DQ33
45	27	Vcc	57	A1	87	DQ34
O 87	28	PD2 (NC)	58	A3	88	Vss
Ö 88	29	PD4 (Vss)	59	A5		
_	30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT16D88C232 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT16D88C232 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installa-

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 through $B8 = 1 \text{ Meg } \times 8 \text{ memory blocks}$.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. Four RAS inputs allow for two x32 banks or four x16 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	ŌĒ	Input	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ34	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ34 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ34 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 62, 64, 77, 78, 79	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT16D88C232 is an 8 megabyte memory card structured as a 2 Meg x 32 bit memory array ($\overline{RAS0} = \overline{RAS2}$, $\overline{RAS1} = \overline{RAS3}$). It also may be configured as a 4 Meg x 16 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four \overline{RAS} lines.

Most x32 bit applications use the same signal to control the \overline{CAS} inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQs and the corresponding \overline{CAS} pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each \overline{RAS} is then a bank select for the 4 Meg x 16 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{CAS} . \overline{WE} must fall prior to \overline{CAS} (EARLY WRITE); if \overline{WE} goes LOW after \overline{CAS} , the outputs (Q) will be

activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of \overline{RAS} inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT16D88C232 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 16 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT16D88C232 operates reliably up to 55°C.



MEMORY TRUTH TABLE

J - 3 8 1						ADDRESSES		DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R	^t C	DQ0-DQ34
Standby		Н	H→X	X	Х	Х	Х	High-Z
READ		L	L ₁	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	Х	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	- L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	X	Χ	Χ	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARA	CTERISTICS	3 - 4				PRESENT DETECT PIN (PDx)						
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	X	X	X	NC	NC	NC	NC	NC	Х	Х	Х
1MB 2MB	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18	18 18	9 9	9 9	512 512	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB • 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X X	X	X X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Timi	ing	1,000	10	0ns		Х	Х	Х	Х	Х	Vss	Vss	Х
			80)ns		Х	Х	Х	Х	Х	NC	Vss	Х
			70)ns		Х	Х	Х	Х	Х	Vss	NC	Х
			60ns				Х	Х	Х	Х	NC	NC	Х
			50ns			Х	Х	Х	Χ	Х	Vss	Vss	Х
Refresh Con	itrol		Star	ndard		Χ	Х	Х	Х	Х	Х	Х	NC
			Aı	uto		Х	Х	Х	Х	Х	Х	Х	Vss

VSS = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss0.5V to +5.25V
Operating Temperature T _A (Ambient)0°C to 55°C
Storage Temperature20°C to +80°C
Power Dissipation15W
Short Circuit Output Current50mA
Card Insertions (Connector's Life Cycle)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0° C $\leq T_A \leq 55^{\circ}$ C; $V_{CC} = 5V \pm 5\%$)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		Vін	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μA	1.7
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = $0V$)	Buffered	lів	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	о́от ≤ 5.25V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)		Vон	2.4		٧.	
Output Low Voltage (IOUT = 4.2mA)		Vol	-	0.4	V	Programa Version

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	32	32	32	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	3.2	3.2	3.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc3	840	760	680	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	600	520	440	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: \textstyle RC = \textstyle RC (MIN))	lcc5	840	760	680	mA	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	840	760	680	mA	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125µs; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	4.8	4.8	4.8	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A9, OE	C _{I1}		9	pF	2
Input Capacitance: WE	C ₁₂		13	pF	2
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз		50	pF	2
Input/Output Capacitance: DQ	Cio		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS		-6		-7		1	-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC .	110		130		150		ns	23
FAST-PAGE-MODE	tPC	40		40		45		ns	23
READ or WRITE cycle time	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1.46			4.0			
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	tRP	45	A North Services	50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10	1	10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns :	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15	1	15		15		ns	26
Row address setup time	†ASR	10	1 11 1	10		10		ns	26
Row address hold time	^t RAH	5	i	5		5		ns	25
RAS to column	†RAD	10	20	10	25	10	30	ns	18, 28
address delay time									
Column address setup time	†ASC	5		5		5		ns	24
Column address hold time	tCAH.	15		20		20		ns	24
Column address hold time	tAR .	45		50		55		ns	25
(referenced to RAS)									
Column address to	^t RAL	40		45		50		ns	26
RAS lead time	24 1 1 1 1 1 1								
Read command setup time	†RCS	5		5		5		ns	25
Read command hold time	^t RCH	5		5		5		ns	19, 24
(referenced to CAS)		<u> </u>							
Read command hold time	^t RRH	-5		-5		-5		ns	19, 25
(referenced to RAS)								<u> </u>	
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	tOFF.	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5		5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

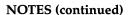
AC CHARACTERISTICS	-6		-7		-8				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20	İ	ns	24
Write command hold time	tWCR	40		50		55		ns	25
(referenced to RAS)									
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	^t DS	5		5		5		ns	24, 32
Data-in hold time	tDH	5		10		10		ns	25, 32
Data-in hold time (referenced to RAS)	tDHR.	45		55		60		ns	23
Transition time (rise or fall)	t _T	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	
RAS to CAS precharge time	tRPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10	¥".	10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	™TH	5		5	,	5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205	1	ns	
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	23
RAS to WE delay time	tRWD	80		90		100		ns	31, 27
Column Address to WE delay time	tAWD.	65		70	* /	75		ns	31, 24
CAS to WE delay time	tCWD	50		65		55		ns	31, 24
Output buffer turn-off delay	^t OE		25		30		30	ns	20, 33, 26
Output disable	^t OD	i syra i i	25		30		30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	5		10		10		ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	^t ORD	10		10		10		ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between V_{II} and V_{II} (or between V_{IL} and V_{IH}) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

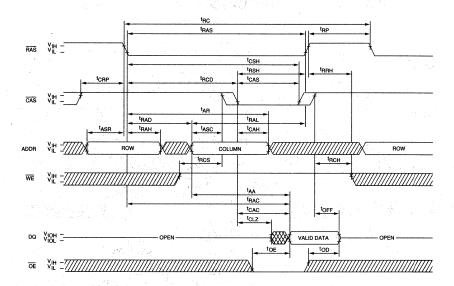
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based on one of the two banks operating or being refreshed (x32 mode). The stated maximums may be reduced by one half when used in the x16 mode. Standby currents of the non-active bank are not included.
- 31. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.



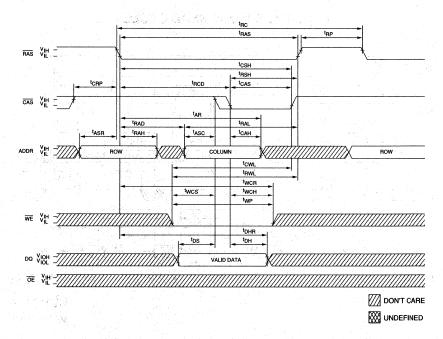
- 32. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 33. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



READ CYCLE

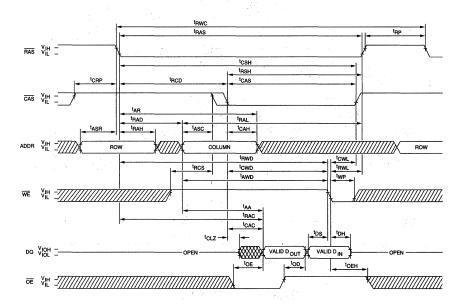


EARLY-WRITE CYCLE

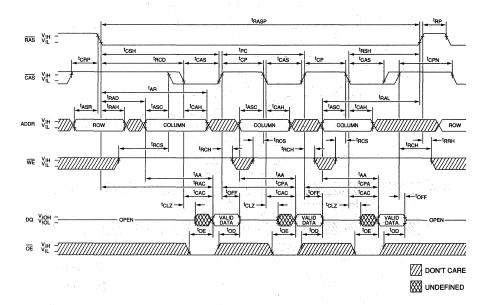




READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

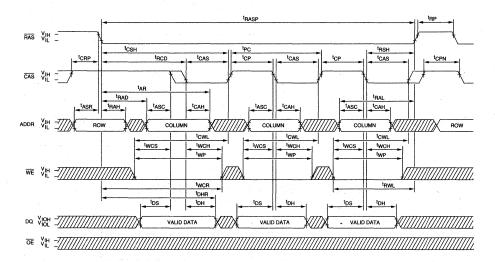


FAST-PAGE-MODE READ CYCLE

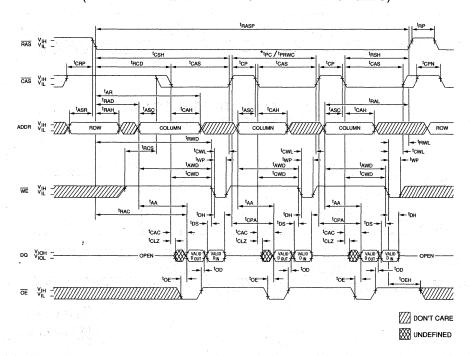




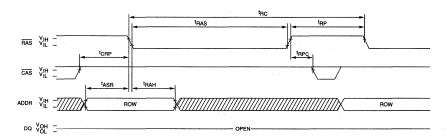
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

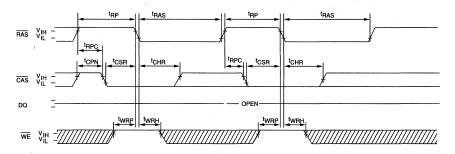


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



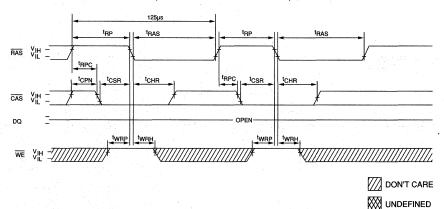
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



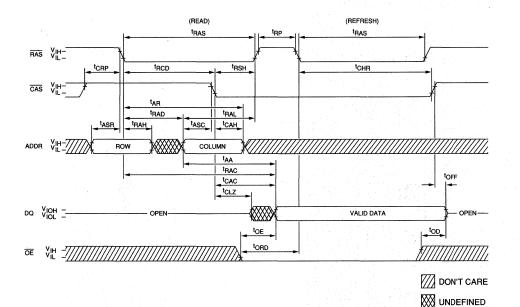
BATTERY BACKUP REFRESH CYCLE

(A0-A9 = DON'T CARE)



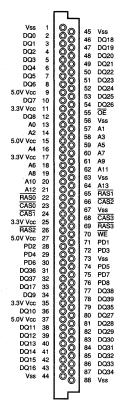


HIDDEN REFRESH CYCLE 21 (WE = HIGH)



RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)



MT16D88C232 PIN ASSIGNMENT

(JEDEC Standard)

			i	
Vss DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 Vcc DQ7 NC NC NC A0 A2 Vcc A4 NC A6 A8 NC NC FAS0 CAS0 CAS0 CAS0 CAS0 CAS0 CAS0 CAS0 C	1 2 3 4 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 6 27 28 29 30 31 32 33 34 40 44 44 44 44 44 44 44 44 44 44 44 44	000000000000000000000000000000000000000	45 46 47 48 49 50 51 52 53 55 56 60 61 62 63 64 65 66 67 71 72 73 74 75 77 78 78 78 78 78 78 78 78 78 78 78 78	Vss D018 D019 D020 D021 D022 D023 D024 D025 NC ODE (Vss) Vss A1 A3 A5 A7 A9 NC Vss CAS3 WE PD1 (Vss) PD5 (Vss) Vss WS QAS3 WE PD1 (Vss) PD5 (Vss) CAS3 D034 Vss D033 D034 Vss



IC DRAM CARD

1 MEGABYTE

256K x 36, 512K x 18

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- · Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x18 or x36 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS

MARKING

Timing		
60ns access		-6
70ns access		-7
80ns access		-8

GENERAL DESCRIPTION

The MT12D88C25636 is a 1 megabyte, IC DRAM card organized as a 256K x 36 bit memory array. It may also be configured as a 512K x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT12D88C25636 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x36 organization, the memory is a single array that may be divided into four separate bytes. In the x18 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

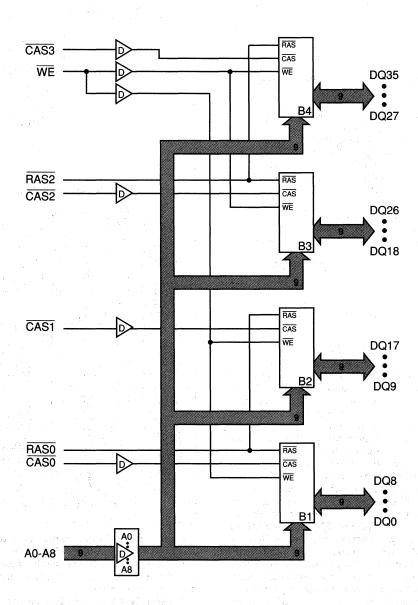


L [F	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
O 45	1	Vss	31	NC	61	NC
46	2	DQ0	32	NC	62	NC
0 47 -	3	DQ1	33	DQ17	63	Vss
49	4	DQ2	34	DQ9	64	NC
51	5	DQ3	35	NC	65	NC
52 53	6	DQ4	36	DQ10	66	CAS2
4	7	DQ5	37	Vcc	67	Vss
5	8	DQ6	38	DQ11	68	CAS3
57	9	Vcc	39	DQ12	69	NC
58 59	10	DQ7	40	DQ13	70	WE
60 61	11	NC	41	DQ14	71	PD1 (Vss)
12	12	DQ8	42	DQ15	72	PD3 (Vss)
33	13	A0	43	DQ16	73	Vss
64 - 65	14	A2	44	Vss	74	PD5 (NC)
66 67	15	Vcc	45	Vss	75	PD7 (TBD)
68 69	16	A4	46	DQ18	76	PD8 (NC)
. [17	NC	47	DQ19	77	NC
1	18	A6	48	DQ20	- 78	NC
72 73	19	A8	49	DQ21	79	DQ35
74	20	NC	50	DQ22	80	DQ27
75 76	21	NC	51	DQ23	81	DQ28
77	22	RAS0	52	DQ24	82	DQ29
79	23	CAS0	53	DQ25	83	DQ30
80 81	24	CAS1	54	DQ26	84	DQ31
82	25	NC	55	NC	85	DQ32
83	26	RAS2	56	Vss	86	DQ33
85	27	Vcc	57	A1	87	DQ34
86 87	28	PD2 (Vss)	58	A3	88	Vss
88	29	PD4 (Vss)	59	A5		
	30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT12D88C25636 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT12D88C25636 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.

2. B1 through $B4 = 256K \times 9$ memory blocks.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RASO, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits. Two RAS inputs allow for a single x36 bank or two x18 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is a WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 61, 62, 55, 64, 65, 69, 77, 78	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C25636 is a 1 megabyte memory card structured as a 256K x 36 bit memory array ($\overline{RAS0} = \overline{RAS2}$). It also may be configured as a 512K x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both \overline{RAS} lines.

Most x36 bit applications use the same signal to control the \overline{CAS} inputs. $\overline{RAS0}$ controls the lower 18 bits, and $\overline{RAS2}$ controls the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding \overline{CAS} pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each \overline{RAS} is then a bank select for the 512K x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and \overline{CAS} the latter 9 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{CAS} . \overline{WE} must fall prior to \overline{CAS} (EARLY WRITE); if \overline{WE} goes LOW after \overline{CAS} , the outputs (Q) will be activated

and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of \overline{RAS} inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C25636 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C25636 operates reliably up to 55°C.



MEMORY TRUTH TABLE

		2.34			ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	t _R	tC	DQ0-DQ35
Standby		Н	H→X	Х	Х	X	High-Z
READ		L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH	1	Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS R	EFRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP R	EFRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	TERISTICS	3			PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	X	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	Х	Х	Х
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	Х	Х	Х
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Timi	ing () () () () () () () ()		10	0ns		Х	Х	Х	Х	Х	Vss	Vss	Х
			80)ns		Х	Х	Х	Х	Х	NC	Vss	Х
			70)ns		Х	Х	Х	Х	Х	Vss	NC	Х
			60)ns		Х	Х	Х	Х	Х	NC	NC	Х
			50)ns	1 W 5	Х	Х	Х	Х	Х	Vss	Vss	Х
Refresh Con	ntrol		Star	ndard		Х	Х	Х	Х	Х	Х	Х	NC
			Aı	uto		Х	Х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	0.5V to +5.25V
Operating Temperature T _A (Ambient)	0°C to 55°C
Storage Temperature	20°C to +80°C
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle).	10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 55^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs		Vін	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-0.5	0.8	٧	1	
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = 0V)	Buffered	lв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	′о∪т ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)		Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)		Vol		0.4	٧	

			MAX].	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = ViH)	lcc1	24	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcc3	1.0	0.9	0.8	Α	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	lcc4	780	660	540	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: \text{*RC} = \text{*RC} (MIN))	lcc5	1.0	0.9	0.8	Α	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	1.0	0.9	0.8	А	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = ^t RAS (MIN) up to 300ns; ^t RC = 125μs; WE, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	2.4	2.4	2.4	mA	3,5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A8	Cıı		9	pF	2
Input Capacitance: WE	Cı2		13	pF	2
Input Capacitance: RASO, RAS2	Сіз	18.1	50	pF	2
Input/Output Capacitance: DQ	Сю		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS	-6		-7			-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time									
Access time from RAS	tRAC		60		70	44144	80	ns	14, 23
Access time from CAS	†CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	. 26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	^t RP	40		50		60		ns	23
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	tRCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	tCRP	15		15		15		ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	tRAH	5		5		5		ns	25
RAS to column	†RAD	10	20	10	25	10	30	ns	18, 28
address delay time									
Column address setup time	tASC	5		5		5		ns	24
Column address hold time	tCAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	tAR .	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29
WE command setup time	twcs	5		5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-6			-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to RAS)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24
Data-in hold time	^t DH	5		10		10		ns	25
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	ťΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	†REF		64		64		64	ms	
RAS to CAS precharge time	^t RPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	^t WTH	5		5	-	5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26

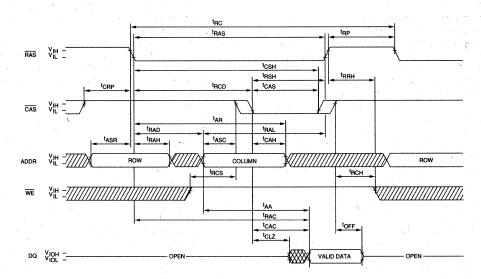


NOTES

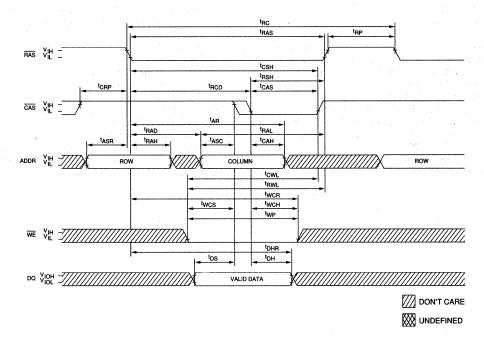
- All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = VIL, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 22. tWTS and tWTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x36 mode. The stated maximums may be reduced by one half when used in the x18 mode.

READ CYCLE

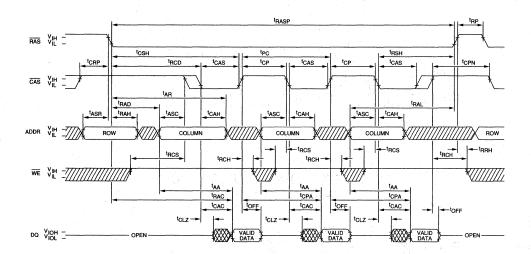


EARLY-WRITE CYCLE

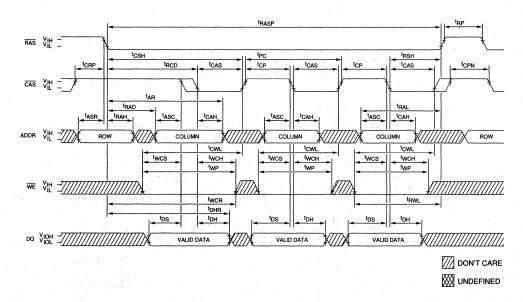




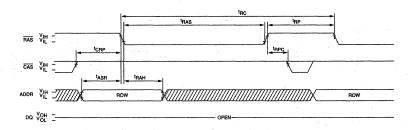
FAST-PAGE-MODE READ CYCLE



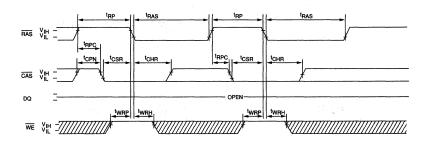
FAST-PAGE-MODE EARLY-WRITE CYCLE



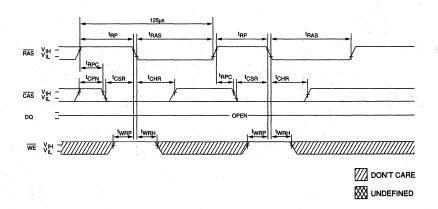
RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE (A0-A8 = DON'T CARE)

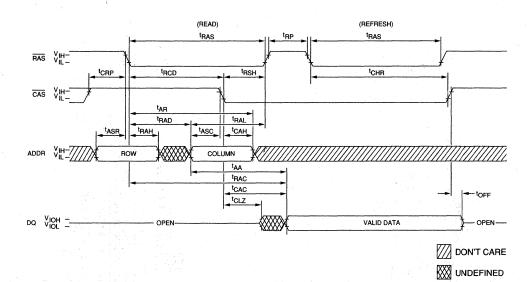


BATTERY BACKUP REFRESH CYCLE (A0-A8 = DON'T CARE)





HIDDEN REFRESH CYCLE 21 (WE = HIGH)



RESERVED JEDEC, JEIDA and PCMCIA **88-PIN ASSIGNMENT**

(All Possible Combinations)

Vss Vss DQ18 DQ19 DQ0 2 3 4 5 6 7 46 47 DQ2 48 DQ20 DQ3 DQ4 50 DQ22 DQ5 51 DQ23 DQ6 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 52 53 54 55 DQ24 DQ25 5.0V Vcc DQ7 DQ26 OE 3.3V Vcc DQ8 A0 56 57 58 59 60 Vss A1 A3 A5 A7 A2 5.0V Vcc A4 3.3V Vcc 61 A6 A8 62 63 64 65 Vss A10 A13 RAS1 RAS0 CAS0 CAS1 66 67 CAS3 68 3.3V Vcc RAS2 RAS3 WE PD1 69 70 71 72 5.0V Vcc 28 29 30 31 32 PD2 PD3 PD4 73 74 Vss PD6 DQ36 75 76 77 PD7 DQ37 PD8 DQ37 32 DQ17 33 DQ9 34 3.3V Vcc 35 DQ10 36 5.0V Vcc 37 DQ38 78 DQ39 DQ35 DQ27 81 DQ28 38 DQ11 82 83 84 DQ29 DQ12 DQ30 40 41 42 43 DQ13 DQ31 DQ14 DQ32 DQ15 86 DQ33 DQ16 87 DQ34 88

MT12D88C25636 PIN ASSIGNMENT (JEDEC Standard)

Vss DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 Vcc DQ7 NC DQ8 A0 A2 Vcc A4 A6 A8 NC NC RA50 CAS0 CAS0 CAS0 CAS0 CAS0 CAS0 CAS0 CAS	1 2 3 4 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 6 27 28 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44	000000000000000000000000000000000000000	45 46 47 48 49 50 152 53 54 55 56 66 67 71 72 73 74 75 67 77 78 81 82 83 84 85 86 87 88	Vss DO18 DO19 DO21 DO22 DO22 DO22 DO22 DO24 DO25 DO26 NC Vss A1 A3 A5 A7 NC NC Vss CAS3 NC WE WE CAS5 NC WS NC NC CAS5 NC WS NC NC NC CAS5 NC WS NC NC WS DO25 DO27 DO27 DO27 DO27 DO27 DO27 DO27 DO28 DO29 DO23 DO23 DO23 DO23 DO23 DO23 DO23 DO23



IC DRAM CARD

2 MEGABYTES

512K x 36, 1 MEG x 18

FEATURES

- IEIDA, IEDEC and PCMCIA standard 88-pin IC DRAM card
- · Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- · All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x18 or x36 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 2.7W active (typical)
- · Extended refresh standard: 512 cycles every 64ms

OPTIONS

MARKING

Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT24D88C51236 is a 2 megabyte, IC DRAM card organized as a 512K x 36 bit memory array. It may also be configured as a 1 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C51236 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x36 organization, the memory array may be divided into two banks, each with four separate bytes. In the x18 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

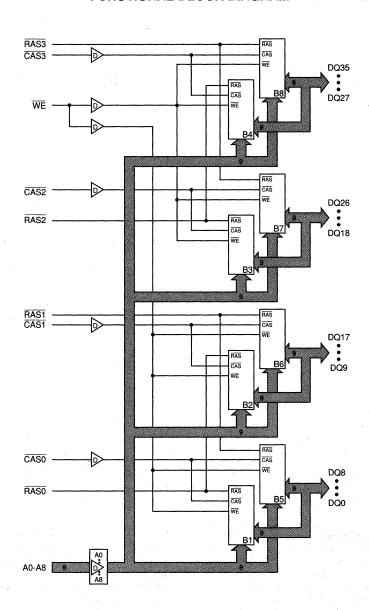


\sqcap	1	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
20	45	1	Vss	31	NC	61	NC
188	46 47	2	DQ0	32	NC	62	NC
180	48	3	DQ1	33	DQ17	63	Vss
188	49 50	4	DQ2	34	DQ9	64	NC
180	51	5	DQ3	35	NC	65	RAS1
l ŏ8	52 53	6	DQ4	36	DQ10	66	CAS2
180	54	7	DQ5	37	Vcc	67	Vss
§8	55 56	8	DQ6	38	DQ11	68	CAS3
188	57 58	9	Vcc	39	DQ12	69	RAS3
188	59	10	DQ7	40	DQ13	70	WE
l 🍇	60 61	11	NC	41	DQ14	71	PD1 (Vss)
188	62	12	DQ8	42	DQ15	72	PD3 (Vss)
188	63 64	13	A0	43	DQ16	73	Vss
180	65	14	A2	44	Vss	74	PD5 (Vss)
I ŏS	66 67	15	Vcc	45	Vss	75	PD7 (TBD)
180	68	16	A4	46	DQ18	76	PD8 (NC)
I ŏS	69 70	17	NC	47	DQ19	77	NC
80	71	18	A6	48	DQ20	78	NC
I ŠŠ	72 73	19	A8	49	DQ21	79	DQ35
188	74 75	20	NC .	50	DQ22	80	DQ27
I ŠŠ	76	21	NC	51	DQ23	81	DQ28
Iŏġ	77 78	22	RAS0	52	DQ24	82	DQ29
188	79	23	CAS0	53	DQ25	83	DQ30
188	80	24	CAS1	54	DQ26	84	DQ31
180	82	25	NC	55	NC	85	DQ32
100	83 84	26	RAS2	56	Vss	86	DQ33
180	85	27	Vcc	57	A1	87	DQ34
000000000000000000000000000000000000000	86 87	28	PD2 (Vss)	58	A3	88	Vss
100	88	29	PD4 (Vss)	59	A5		
	J	30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT24D88C51236 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT24D88C51236 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.

2. B1 through B8 = 256K x 8 memory blocks.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 9 row- address bits. Four RAS inputs allow for two x36 banks or four x18 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is a WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	, 28, 72, 29, PD1-PD8 - Presence Detect: These pins are read by the		
11, 17, 20, 21, 25, 31, 32, 35, 61, 62, 55, 64, 77, 78	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C51236 is a 2 megabyte memory card structured as a 512K \times 36 bit memory array (RAS0 = RAS2) RAS1 = RAS3). It also may be configured as a 1 Meg \times 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four RAS lines.

Most x36 bit applications use the same signal to control the $\overline{\text{CAS}}$ inputs. $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ control the lower 18 bits, and $\overline{\text{RAS2}}$ and $\overline{\text{RAS3}}$ control the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{\text{CAS}}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the 1 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (AO-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if WE goes LOW after CAS, the outputs (Q) will be activated and will

drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of the \overline{RAS} inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C51236 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C51236 operates reliably up to 55°C.



MEMORY TRUTH TABLE

					ADDRI	ESSES	DATA IN/OUT
FUNCTION	rettu searcus	RAS	CAS	WE	^t R	tC	DQ0-DQ35
Standby		Н	H→X	Х	Х	Χ	High-Z
READ	Paran in	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	High-Z
FAST-PAGE-MODE	1st Cycle	L.	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH	1	Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	th L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	i i <u>L</u> ERS	L	ROW	COL	Data In
CAS-BEFORE-RAS R	EFRESH	H→L	L	Н	Х	X	High-Z
BATTERY BACKUP R	EFRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	CTERISTICS	3			PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	Х	Χ	Х
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	VSS	Vss	Vss	Ves	V.S.S	Х	Х	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Timi	ing		10	0ns		Х	Х	Х	Х	Х	Vss	Vss	Х
			80)ns		Х	Х	Х	Х	Х	NC	Vss	Х
			70)ns		Х	Х	Х	Х	Х	Vss	NC	Х
			60ns			Х	Х	Х	Х	Х	NC	NC	Х
	50ns			Yel July	Х	Х	Х	Х	Х	Vss	Vss	Х	
Refresh Con	ntrol	100	Star	ndard		Х	Х	Х	Х	Х	X	Х	NC
	Auto			Х	Х	Х	Х	Х	X	Х	Vss		

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	0.5V to +5.25V
Operating Temperature T _A (Ambient)	0°C to 55°C
Storage Temperature	-20°C to +80°C
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)	10.000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 55^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	-	Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = 0V)	Buffered	lв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	ουτ ≤ 5.25V)	loz	-10	10	μΑ	- 1 to 1
OUTPUT LEVELS Output High Voltage (Iout = -5mA)		Vон	2.4		V	
Output Low Voltage (Iout = 4.2mA)		Vol	2.00	0.4	٧	

				MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES	
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	48	48	48	mA		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	Icc2	4.8	4.8	4.8	mA		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	1.0	0.9	0.8	А	3, 4, 30	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, Address Cycling: ¹ PC = ¹ PC (MIN))	lcc4	780	660	540	mA	3, 4, 30	
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vih.: ^t RC = ^t RC (MIN))	lcc5	1.0	0.9	0.8	A	3, 30	
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	1.0	0.9	0.8	А	3, 5, 30	
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = [†] RAS (MIN) up to 300ns; [†] RC = 125μs; WE, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	4.8	4.8	4.8	mA	3, 5	



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A8	Cıı		9	pF	2
Input Capacitance: WE	C ₁₂		13	pF	2
Input Capacitance: RASO, RAS1, RAS2, RAS3	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_{A} \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS			-6	-7			-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time							1 4		
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	†CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	^t RP	40		50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10	100	ns	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	^t RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	†ASC	5		5	1 2	5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	tCLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29
WE command setup time	twcs	5	1	5		5		ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-6		-	7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to RAS)	tWCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	^t DS	5		5		5		ns	24
Data-in hold time	tDH	5		10		10		ns	25
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		64		64		64	ms	
RAS to CAS precharge time	^t RPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	20		20		20	·	ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		· 20		ns	22, 26

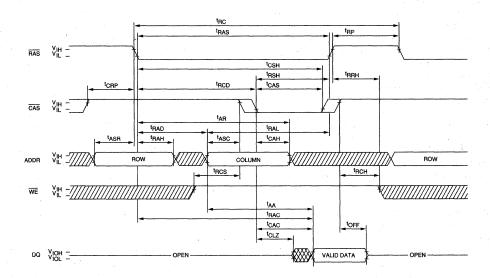


NOTES

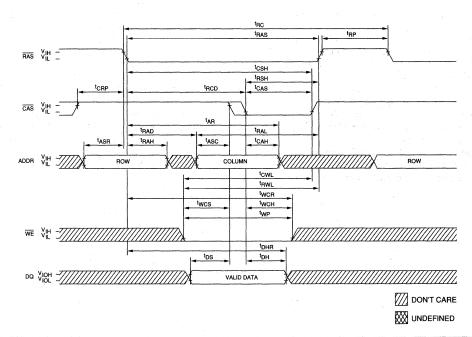
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight \overline{RAS} cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If CAS = Vін, data output is High-Z.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the

- specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cvcle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based on one of the two banks operating or being refreshed (x36 mode). The stated maximums may be reduced by one half when used in the x18 mode. Standby currents of the non-active bank are not included.

READ CYCLE

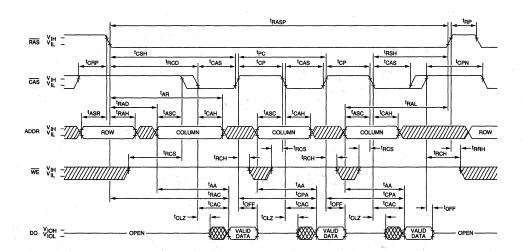


EARLY-WRITE CYCLE

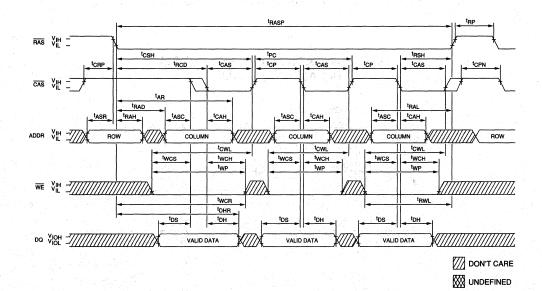




FAST-PAGE-MODE READ CYCLE



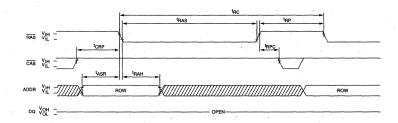
FAST-PAGE-MODE EARLY-WRITE CYCLE





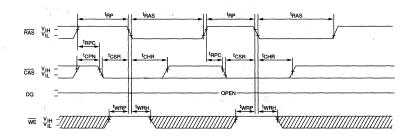
RAS-ONLY REFRESH CYCLE

 $(ADDR = A0-A8; \overline{WE} = DON'T CARE)$



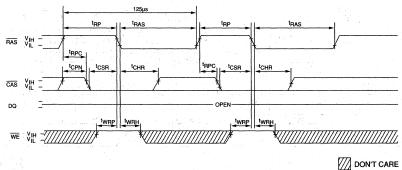
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE

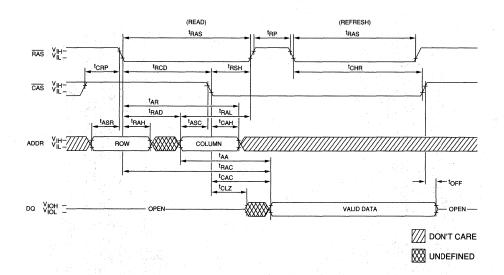
(A0-A8 = DON'T CARE)







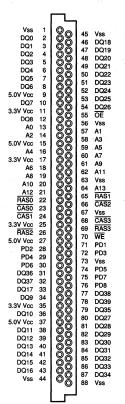
HIDDEN REFRESH CYCLE 21 $(\overline{WE} = HIGH)$



RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)

MT24D88C51236 PIN ASSIGNMENT (JEDEC Standard)



45 Vss DQ0 DQ1 DQ2 46 DQ18 48 DQ20 DQ3 49 DQ21 DQ4 DQ5 DQ6 Vcc 50 DQ22 51 DQ23 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 DQ25 DQ7 NC DQ8 A0 A2 Vcc A4 NC A6 A8 NC NC RASO CASO CASO NC RASO RASO 10 DQ26 11 NC Vss АЗ A5 A7 NC NC Vss NC RAS1 CAS2 Vss CAS3 RAS3 WE 67 68 69 70 71 72 Vcc PD1 (Vss) PD2 (Vss) PD3 (Vss) PD4 (Vss) 73 74 75 76 77 Vss PD6 (TBD) PD5 (Vss) PD7 (TBD) PD8 (NC) NC DQ17 NC DQ9 78 NC 79 DQ35 DQ10 80 81 82 DQ27 DQ28 Vcc DQ11 DQ29 DQ12 DQ13 DQ14 83 DQ30 84 85 86 DQ31 DQ32 DQ33 DQ16 DQ34



IC DRAM CARD

4 MEGABYTES

1 MEG x 36, 2 MEG x 18

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x18 or x36 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 3.1W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS

MARKING

•	Timing			
	60ns access			-6
	70ns access			-7
	80ns access			-8

GENERAL DESCRIPTION

The MT12D88C136 is a 4 megabyte, IC DRAM card organized as a 1 Meg x 36 bit memory array. It may also be configured as a 2 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when as compared to standard DRAMs.

The MT12D88C136 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple RAS inputs conserve power by allowing individual bank selection. In the x36 organization, the memory is a single array that may be divided into four separate bytes. In the x18 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)

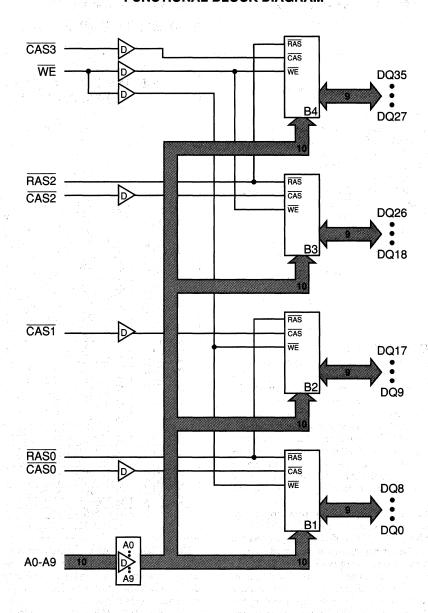


PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
45 1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	CAS2
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	CAS3
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	70	WE
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	RAS0	52	DQ24	82	DQ29
23	CAS0	53	DQ25	83	DQ30
24	CAS1	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	RAS2	56	Vss	86	DQ33
27	Vcc	57	A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT12D88C136 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT12D88C136 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.

2. B1 through B4 = 1 Meg x 9 memory blocks.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RASO, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. Two RAS inputs allow for a single x36 bank or two x18 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is a WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 62, 55, 64, 77, 78, 65, 69	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C136 is a 4 megabyte memory card as a 1 Meg x 36 bit memory array ($\overline{RAS0} = \overline{RAS2}$). It also may be configured as a 2 Meg x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both \overline{RAS} lines.

Most x36 bit applications use the same signal to control the $\overline{\text{CAS}}$ inputs. $\overline{\text{RAS0}}$ controls the lower 18 bits and $\overline{\text{RAS2}}$ controls the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding $\overline{\text{CAS}}$ pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the 2 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{CAS} . \overline{WE} must fall prior to \overline{CAS} (EARLY WRITE); if \overline{WE} goes LOW after \overline{CAS} , the outputs (Q) will be

activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C136 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C136 operates reliably up to 55°C.



MEMORY TRUTH TABLE

			100		ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	t _C	DQ0-DQ35
Standby		Н	H→X	Х	Х	Х	High-Z
READ	the second	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	. L (4)	H→L	- н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L.	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	. L	- H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	, HL	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH	1	Н	Χ	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS R	EFRESH	H→L	L	Н	Х	Х	High-Z
BATTERY BACKUP R	EFRESH	H→L	L	Н	Х	X	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	CTERISTICS	3			PRESENT DETECT PIN (PDx)									
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8		
0MB	No card installed	Х	. X	Х	X	NC	NC	NC	NC	NC	Х	Х	Х		
1MB 2MB	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18	18 18	9 9	9 9	512 512	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X		
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X		
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	Х	Х	Х		
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	Х	Х	Х		
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X		
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X X	X		
Access Timi	ng	17.504	10	0ns		Х	Х	X	Х	Х	Vss	Vss	Х		
			80)ns		Х	Х	Х	Х	Х	NC	Vss	Х		
			70)ns	- 48	Х	Х	Х	Х	Х	Vss	NC	Х		
			60ns			Х	Х	Х	Х	Х	NC	NC	Х		
			50	ns		Х	Х	X	Х	Х	Vss	Vss	Х		
Refresh Con	trol		Stan	ndard		X	X	Х	X	Х	X	Х	NC		
			Au	uto	none.	Х	Х	Х	Х	Х	Х	Х	Vss		

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs	* * * * * * * * * * * * * * * * * * *	VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = $0V$)	Buffered	Ів	-2	2	μА	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	ουτ ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		٧	
Output High Voltage (lout = -5mA) Output Low Voltage (lout = 4.2mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	24	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	1.2	1.1	1.0	Α	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^t PC = ^t PC (MIN))	Icc4	900	750	625	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: RC = RC (MIN))	lcc5	1.2	1.1	1.0	А	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: [†] RC = [†] RC (MIN))	lcce	1.2	1.1	1.0	Α	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125µs; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	3.2	3.2	3.2	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A9	CI1	. ,	9	pF	2
Input Capacitance: WE	C12		13	pF	2
Input Capacitance: RASO, RAS2	Сіз		50	pF	2
Input/Output Capacitance: DQ	Cio		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13,) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-6		-7			-8	nga mili	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time							7.55		
Access time from RAS	^t RAC		60		70	Sept. 17	80	ns	14, 23
Access time from CAS	†CAC	1	25		30	1.1	30	ns	15, 26
Access time from column address	^t AA		40		45	Service of	50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	^t RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	25		30		30		ns	26
RAS precharge time	^t RP	45		50		60		ns	23
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65		75		ns	25
CAS precharge time	¹ CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	tRCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	tASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	†ASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	[†] RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5	1	5	7 2 2	ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29
WE command setup time	twcs	5	1 7 7	5		5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_{A} \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS	1 × 1 × 1	-6		-7		-8				
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES	
Write command hold time	tWCH	15		20		20		ns	24	
Write command hold time (referenced to RAS)	†WCR	40		50	-	55	The Hart	ns	25	
Write command pulse width	tWP	10		15		15		ns	23	
Write command to RAS lead time	^t RWL	25		30		30		ns	26	
Write command to CAS lead time	tCWL	20		25		25		ns	24	
Data-in setup time	tDS	5		5		5		ns	24	
Data-in hold time	^t DH	5		. 10		10		ns	25	
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23	
Transition time (rise or fall)	ŧΤ	2	15	2	15	2	15	ns	9, 10, 23	
Refresh period (1,024 cycles)	^t REF	1 36	128		128		128	ms	244.	
RAS to CAS precharge time	^t RPC	10		10		10		ns	26	
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26	
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25	
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5		ns	22, 25	
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	20		20		20		ns	22, 26	
WE hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25	
WE setup time	tWTS	20		20		20		ns	22, 26	

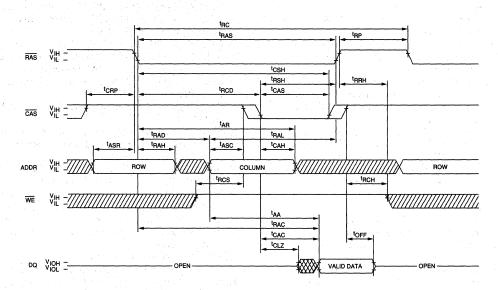


NOTES

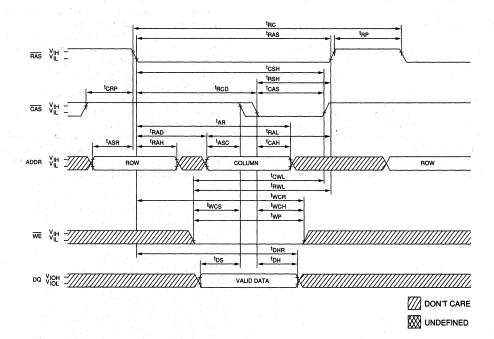
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- 4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
- 12. If $\overline{CAS} = VIL$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as

- a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cvcle.
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x36 mode. The stated maximums may be reduced by one half when used in the x18 mode.

READ CYCLE

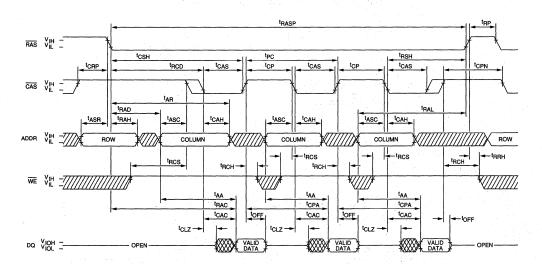


EARLY-WRITE CYCLE

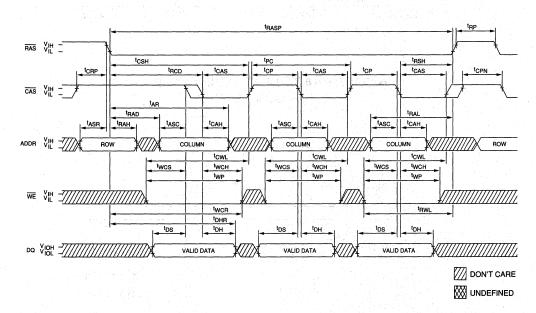




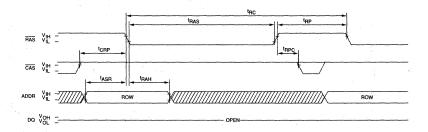
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

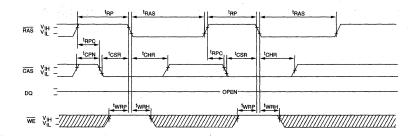


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



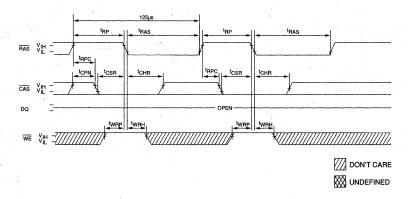
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



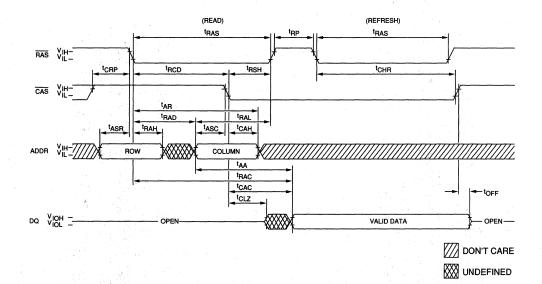
BATTERY BACKUP REFRESH CYCLE

(A0-A9 = DON'T CARE)





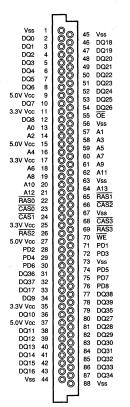
HIDDEN REFRESH CYCLE 21 (WE = HIGH)

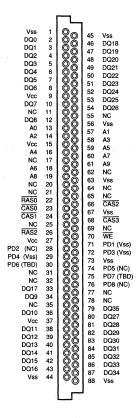


RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)

MT12D88C136 PIN ASSIGNMENT (JEDEC Standard)







IC DRAM CARD

8 MEGABYTES

2 MEG x 36, 4 MEG x 18

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- · Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x18 or x36 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 3.1W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS

MARKING

	 _
Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT24D88C236 is an 8 megabyte, IC DRAM card organized as a 2 Meg x 36 bit memory array. It may also be configured as a 4 Meg x 18 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C236 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

Multiple \overline{RAS} inputs conserve power by allowing individual bank selection. In the x36 organization, the memory array may be divided into two banks, each with four separate bytes. In the x18 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each \overline{RAS} selection; the others not selected remain in standby mode, drawing minimum power.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)



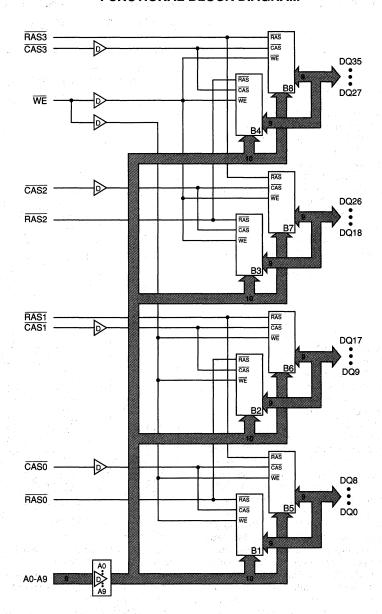
1 2 3 4	00000	45 46 47 48
5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23	000000000000000000000000000000000000000	49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66
23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44	000000000000000000000000000000000000000	59 60 61 62 63 64 65 66 67 70 77 77 77 77 77 80 81 82 83 84 85 86 87 88
1.5.	ٿا	

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	31	NC	61	A9
2	DQ0	32	NC	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	RAS1
6	DQ4	36	DQ10	66	CAS2
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	CAS3
9	Vcc	39	DQ12	69	RAS3
10	DQ7	40	DQ13	70	WE
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (Vss)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
.17	NC	47	DQ19	77	NC
18	A6	48	DQ20	78	NC
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	RAS0	52	DQ24	82	DQ29
23	CAS0	53	DQ25	83	DQ30
24	CAS1	54	DQ26	84	DQ31
25	NC	55	NC	85	DQ32
26	RAS2	56	Vss	86	DQ33
27	Vcc	57	. A1	87	DQ34
28	PD2 (NC)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Eight presence detect pins may be read by the host to identify the MT24D88C236 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power-saving features.

The MT24D88C236 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. D = 74AC11244 line drivers.

2. B1 through B8 = 1 Meg x 9 memory blocks.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. Four RAS inputs allow for two x36 banks or four x18 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is a WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79	DQ0-DQ35	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ35 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ35 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 31, 32, 35, 62, 55, 64, 77, 78	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C236 is an 8 megabyte memory card structured as a 2 Meg x 36 bit memory array ($\overline{RAS0} = \overline{RAS2}$, RAS1 = RAS3). It also may be configured as a 4 Meg x 18 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four RAS lines.

Most x36 bit applications use the same signal to control the CAS inputs. RASO and RASI control the lower 18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 18 bits to obtain a x36 memory array. For x18 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and CASO to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the 4 Meg x 18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if WE goes LOW after CAS, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C236 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C236 operates reliably up to 55°C.



MEMORY TRUTH TABLE

1		4.3.		14	ADDRI	ESSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	^t R	tC	DQ0-DQ35
Standby		Н	H→X	Х	Х	X	High-Z
READ	4.11 <u>1. 1. 1.</u>	L	L	Н	ROW	COL	Data Out
EARLY-WRITE		L	L	L	ROW	COL	Data In
READ-WRITE		L	L	H→L	ROW	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data Out
RAS-ONLY REFRESH		Н	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L L	Н	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	- 1 - L	ROW	COL	Data In
CAS-BEFORE-RAS R	EFRESH	H→L	L	Н	Х	X	High-Z
BATTERY BACKUP R	EFRESH	H→L	L	Н	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	Insity Organizations Address Address Address Address Depth OMB No card installed X X X X 1MB 256K x 1, 4, 16, 18 18 9 9 512 2MB 256K x 1, 4, 16, 18 18 9 9 512 2MB 512K x 8, 9 19 10 9 512 4MB 1 Meg x 1, 4, 16, 18 20 10 10 1,024							PRESE	NT DET	ECT P	IN (PD	x)	
Card Density		1				1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	w X	Х	NC	NC	NC	NC	NC	X	Х	Х
1MB 2MB		1			-	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
2MB 4MB		1				NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	Х	Х	Х
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Viss							
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Timi	ing	5 84,38	10	0ns		X	Х	Х	X	Х	Vss	Vss	Х
			80)ns		X	Х	Х	X	Х	NC	Vss	Х
			70)ns	and the gre	Х	Х	Х	Х	Х	Vss	NC	Х
			60)ns		Х	Х	Х	Х	Х	NC	NC	Х
			50ns			Х	Х	Х	Х	Х	Vss	Vss	Х
Refresh Con	itrol		Star	ndard		Х	X.	Х	Х	Х	Х	Х	NC
			A	uto	M .135	Х	Х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	0.5V to +5.25V
Operating Temperature T _A (Ambient)	0°C to 55°C
Storage Temperature	
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)	10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION	1 1	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	3.5	Vcc+0.5	٧	1	
Input Low (Logic 0) Voltage, All Inputs	VIL	-0.5	0.8	٧	1	
INPUT LEAKAGE CURRENT, Any input	CURRENT, Any input Non-buffered				μΑ	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = 0V)	Buffered	lв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	о∪т ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (lout = -5mA)		Vон	2.4		٧	
Output Low Voltage (Iout = 4.2mA)	e de la companya de la companya de la companya de la companya de la companya de la companya de la companya de	Vol		0.4	V	

			MAX	v		
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	48	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	1.2	1.1	1.0	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	860	740	620	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: TRC = TRC (MIN))	lcc5	1.2	1.1	1.0	A	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	1.2	1.1	1.0	А	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: $\overline{CAS} = 0.2V$ or CBR cycling; $\overline{RAS} = {}^{t}RAS$ (MIN) up to 300ns; ${}^{t}RC = 125\mu s$; \overline{WE} , A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	6.4	6.4	6.4	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A9	Cıı		9	pF	2
Input Capacitance: WE	C ₁₂		13	pF	2
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		24	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_{A} \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS			-6		-7		-8	. 0 0	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	110		130		150	100	ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time							1.5		
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	^t RP	45	100	50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	55		65		75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	tASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column	tRAD .	10	20	10	25	10	30	ns	18, 28
address delay time									
Column address setup time	^t ASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to \overline{RAS})	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5	1, 1	5		ns	25
Read command hold time (referenced to CAS)	tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5	1	5	1	ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29
WE command setup time	twcs	5	1	5		5	1	ns	24

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS	-6			-7	-	8	4		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time (referenced to RAS)	tWCR	40		50		55		ns	25
Write command pulse width	^t WP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	^t CWL	20		25		25		ns	24
Data-in setup time	^t DS	5		5		5		ns	24
Data-in hold time	^t DH	5		10		10		ns	25
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	ŀΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	
RAS to CAS precharge time	^t RPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	tWRH	5		5		5		ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	tWTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26

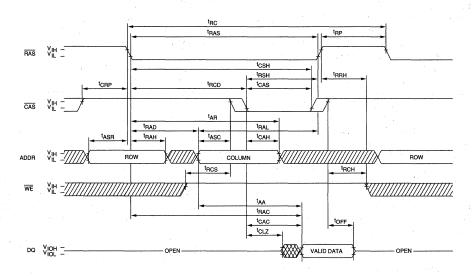


NOTES

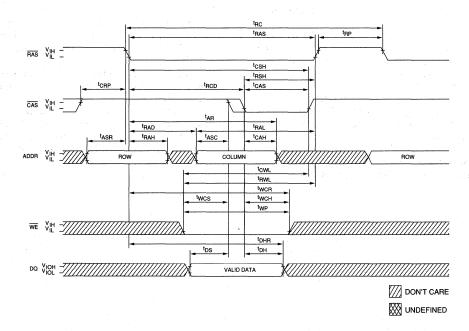
- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the

- specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. twTS and twTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of twRP and twRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based on one of the two banks operating or being refreshed (x36 mode). The stated maximums may be reduced by one half when used in the x18 mode. Standby currents of the non-active bank are not included.

READ CYCLE

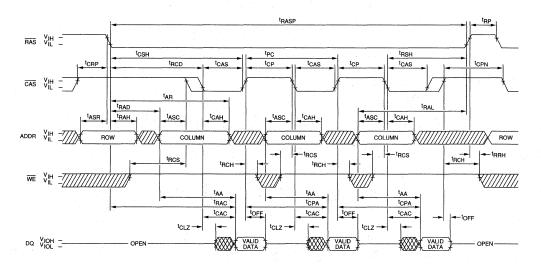


EARLY-WRITE CYCLE

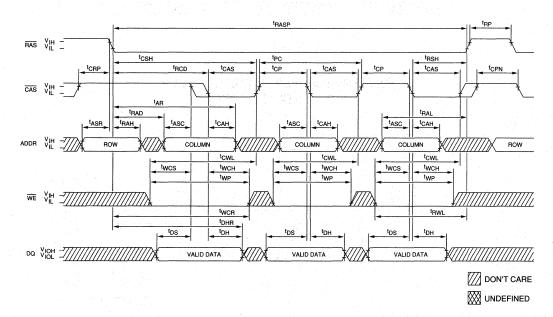




FAST-PAGE-MODE READ CYCLE

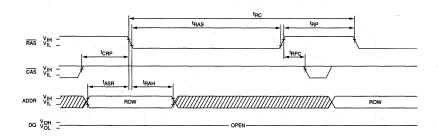


FAST-PAGE-MODE EARLY-WRITE CYCLE

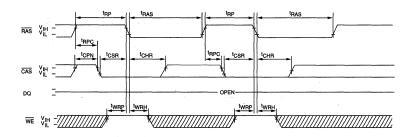


MICHON

RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)

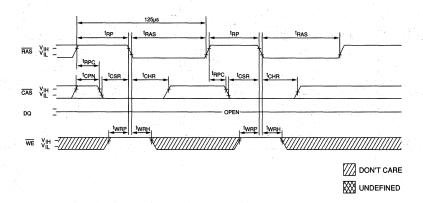


CAS-BEFORE-RAS REFRESH CYCLE (A0-A9 = DON'T CARE)



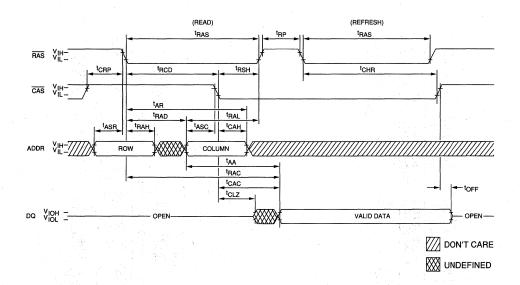
BATTERY BACKUP REFRESH CYCLE

(A0-A9 = DON'T CARE)





HIDDEN REFRESH CYCLE 21 (WE = HIGH)

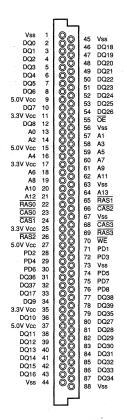


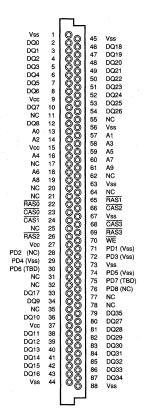
RESERVED JEDEC 88-PIN ASSIGNMENT

(All Possible Combinations)

MT24D88C236 PIN ASSIGNMENT

(JEDEC Standard)





I IC DRAM CARD

IC DRAM CARD

1 MEGABYTE

256K x 40, 512K x 20

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple \overline{RAS} inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS

MARKING

Timing	
60ns access	-6
70ns access	-7
80ns access	-8

GENERAL DESCRIPTION

The MT12D88C25640 is a 1 megabyte, IC DRAM card organized primarily as a 256K x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 512K x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT12D88C25640 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)



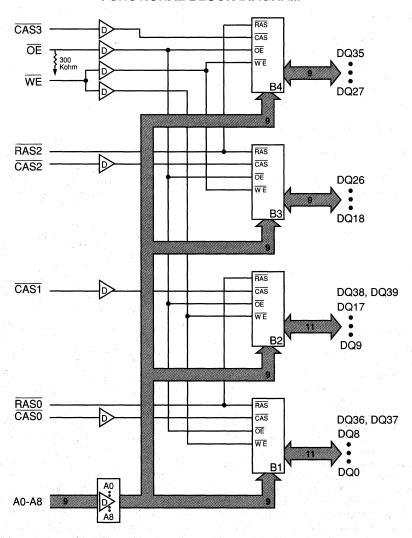
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	31	DQ36	61	NC
2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
4	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC .
6	DQ4	36	DQ10	66	CAS2
7	DQ5	37	Vcc	67	Vss
8	DQ6	38	DQ11	68	CAS3
9	Vcc	39	DQ12	69	NC
10	DQ7	40	DQ13	. 70	WE
11	NC	41	DQ14	71	PD1 (Vss)
12	DQ8	42	DQ15	72	PD3 (Vss)
13	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
15	Vcc	45	Vss	75	PD7 (TBD)
16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
19	A8	49	DQ21	79	DQ35
20	NC	50	DQ22	80	DQ27
21	NC	51	DQ23	81	DQ28
22	RAS0	52	DQ24	82	DQ29
23	CAS0	53	DQ25	83	DQ30
24	CAS1	54	DQ26	84	DQ31
25	NC	55	OE (Vss)	85	DQ32
33 26	RAS2	56	Vss	86	DQ33
5 27	Vcc	57	A1	87	DQ34
28	PD2 (Vss)	58	A3	88	Vss
29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory is a single array that may be divided into four separate bytes (x32/x36 only). In the x16/18/20 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT12D88C25640 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT12D88C25640 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 and B2 = 256K x 11 memory blocks; B3 and B4 = 256K x 9 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RAS0, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits. Two RAS inputs allow for a single x32/36/40 bank or two x16/18/20 banks.
23, 24, 66, 68	CAS ₀ -3	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	ŌĒ	Input	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 35, 61, 62, 64, 65, 69	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

The MT12D88C25640 is a 1 megabyte memory card structured as a 256K x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$). It also may be configured as a 512K x 16/18/20 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both \overline{RAS} lines.

Most x32/36/40 bit applications use the same signal to control the CAS inputs. RASO controls the lower 16/18 bits, and $\overline{RAS2}$ controls the upper 16/18 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{\text{CAS0}}$ to $\overline{\text{CAS2}}$ and $\overline{\text{CAS1}}$ to $\overline{\text{CAS3}}$). Each $\overline{\text{RAS}}$ is then a bank select for the 512K x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. \overline{RAS} is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$, the outputs (Q) will be activated

and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C25640 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 8 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C25640 operates reliably up to 55°C.



MEMORY TRUTH TABLE

	e a grandi				ADDRE	SSES	DATA IN/OUT	
FUNCTION	RAS	CAS	WE	0E	^t R	tC.	DQ0-DQ39	
Standby		Н	H→X	Х	Х	Χ	Х	High-Z
READ		L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH	Alberta (Ligh	L	Х	X	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	Ľ	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	Ĺ	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	CAS-BEFORE-RAS REFRESH		L	Н	X	Х	Х	High-Z
BATTERY BACKUP RE	H→L	L	Н	Х	Х	Х	High-Z	

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS							PRESENT DETECT PIN (PDx)						
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	X	NC	NC	NC	NC	NC	Х	Х	Х
• 1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	Х	X
2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	Х	X	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Tim	ing		10	0ns		Х	Х	Х	X	Х	Vss	Vss	Х
			80)ns		X	Х	Х	Х	Х	NC	Vss	Х
			70)ns	i Mayan	Х	Х	Х	Х	Х	Vss	NC	Х
		1.54	60)ns		Х	Х	Х	Х	Х	NC	NC	Х
			50ns				Х	Х	Х	Х	Vss	Vss	Х
Refresh Cor	ntrol		Standard			Х	Х	Х	Х	Х	Х	Х	NC
			Auto				Х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	0.5V to +5.25V
Operating Temperature, TA (Ambient)	0°C to +55°C
Storage Temperature	
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)	10.000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage	Vcc	4.75	5.25	٧	- 1	
Input High (Logic 1) Voltage, All Inputs		Vıн	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V \text{In} \le 5.25V$; all other pins not under test = 0V)	Buffered	lıв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	′ουτ ≤ 5.25 V)	loz	-10	10	μΑ	
OUTPUT LEVELS		Vон	2.4		V	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 4.2mA)		Vol	81 1	0.4	٧	

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PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	24	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Іссз	1.0	0.9	0.8	А	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	Icc4	780	660	540	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	1.0	0.9	0.8	Α	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc6	1.0	0.9	0.8	А	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125µs; WE, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	2.4	2.4	2.4	mA	3,5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CAS0, CAS1, CAS2, CAS3, A0-A8, OE	C _{I1}		9	pF	2
Input Capacitance: WE	Cı2		13	pF	2
Input Capacitance: RAS0, RAS2	Сіз		50	pF	2
Input/Output Capacitance: DQ	Cio		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-6			-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40	No. 18 Sec.	45		ns	23
READ or WRITE cycle time									
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	†CAC		25		30	***************************************	30	ns	15, 26
Access time from column address	tAA .		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	25		30		30		ns	26
RAS precharge time	tRP	40		50		60		ns	23
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65	9 11 12 14 2	75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	^t RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	tCRP	15		15		15		ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	tRAD .	10	20	10	25	10	30	ns	18, 28
Column address setup time	tASC	5		5		5	To Market	ns	24
Column address hold time	^t CAH	15		20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	†RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	tCLZ.	5		5		5		nş	24
Output buffer turn-off delay	¹OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5		5	1	ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS	-6		-7	·		8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	†WCH	15		20		20		ns	24
Write command hold time (referenced to RAS)	^t WCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	^t DH	5		10		10		ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	4 5 5
RAS to CAS precharge time	^t RPC	10		10		10		ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20	are ji	ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5	12.	5		5	- Se	ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	tWRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	^t WTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	^t RWC	165		185		205		ns	
FAST-PAGE-MODE READ-WRITE cycle time	[†] PRWC	90		95		100		ns	23
RAS to WE delay time	tRWD	80		90		100		ns	31, 27
Column Address to WE delay time	^t AWD	65		70		75		ns	31, 24
CAS to WE delay time	^t CWD	50		65		55	1.5%	ns	31, 24
Output buffer turn-off delay	†OE		25		30		30	ns	20, 33, 26
Output disable	tOD		25		30		30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	^t OEH	5		10		10	er kaja Kajawa	ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	[†] ORD	10		10		10	13 %	ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = \text{Vil.}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

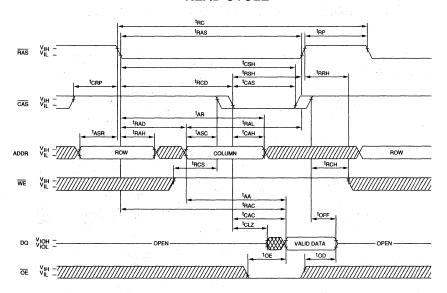
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voн or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
- 31. ¹WCS, ¹RWD, ¹AWD and ¹CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

NOTES (continued)

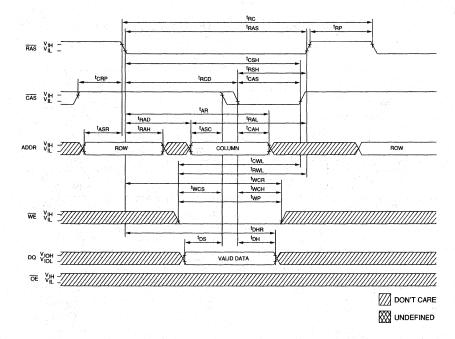
- 32. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 33. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and \overline{OE} is taken back LOW after 'OEH is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once 'OD or 'OFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



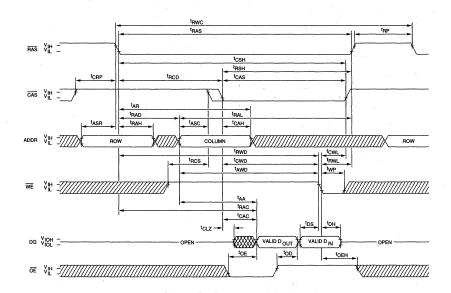
READ CYCLE



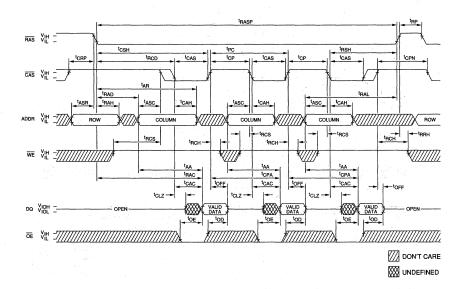
EARLY-WRITE CYCLE



READ-WRITE CYCLE(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

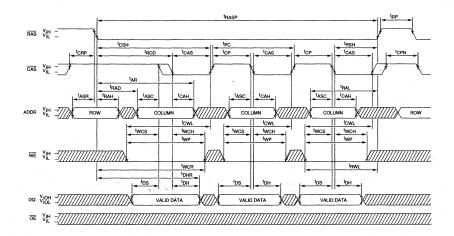


FAST-PAGE-MODE READ CYCLE

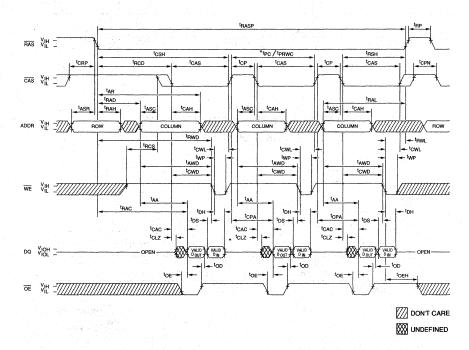




FAST-PAGE-MODE EARLY-WRITE CYCLE



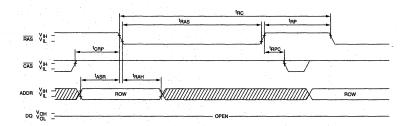
FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



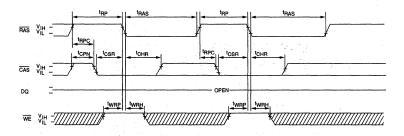
MICHON



RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)

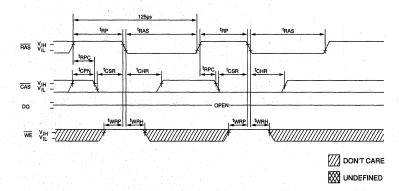


CAS-BEFORE-RAS REFRESH CYCLE (A0-A8 = DON'T CARE)



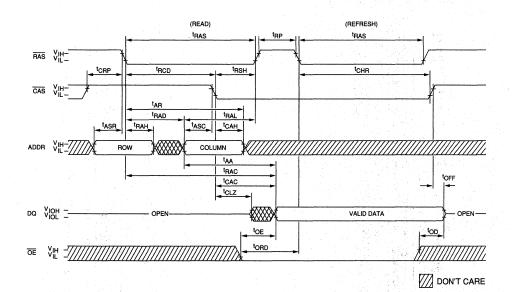
BATTERY BACKUP REFRESH CYCLE

(A0-A8 = DON'T CARE)





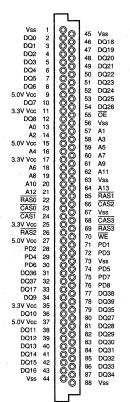
HIDDEN REFRESH CYCLE 21 (WE = HIGH)



₩ undefined

RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)



MT12D88C25640 PIN ASSIGNMENT (JEDEC Standard)

45 Vss DQ0 46 DQ18 47 DQ19 DQ2 48 DQ20 DQ3 49 DQ21 DQ4 DQ5 50 DQ22 51 DQ23 DQ6 52 53 54 DQ24 Vcc DO25 DQ7 10 DQ26 NC DQ8 A0 A2 11 12 13 OE (Vss) 57 Α1 14 58 59 60 A3 A5 A7 VCC A4 NC A6 A8 NC 15 17 61 18 19 20 NC RAS1 64 65 21 RAS0 CAS2 66 CAS0 CAS1 NC RAS2 23 24 25 26 67 Vss 68 CAS₃ RAS3 WE 70 71 Vcc 27 PD1 (Vss) PD2 (Vss) 72 PD3 (Vss) PD4 (Vss) 29 73 Vss 30 31 32 PD6 (TBD) PD5 (Vss) DQ36 PD7 (TBD) DQ37 76 77 PD8 (NC) DQ17 33 DQ38 DQ9 34 78 79 DQ39 NC 35 DQ35 DQ10 VCC 36 37 38 39 80 DQ27 DQ28 DQ11 DQ29 DQ12 83 DQ30 DQ13 40 84 DQ31 DQ14 41 85 DQ32 42 43 44 DQ15 86 DQ33 DQ16 Vss DQ34 88 Vss



IC DRAM CARD

2 MEGABYTES

512K x 40, 1 MEG x 20

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), BATTERY BACKUP (BBU) and HIDDEN
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 2.7W active (typical)
- Extended refresh standard: 512 cycles every 64ms

OPTIONS	MARKI	NG
 Timing 		
60ns access	-6	
70ns access	-7	
80ns access	-8	

GENERAL DESCRIPTION

The MT24D88C51240 is a 2 megabyte, IC DRAM card organized primarily as a 512K x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 1 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C51240 is designed for low power operation using 256K x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)



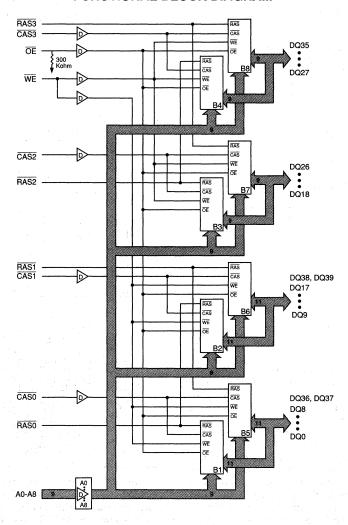
1 2 45 46 47 48 49 55 12 23 3 4 5 5 6 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	1 2 3 4 5 6 7 8 9	Vss DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6	31 32 33 34 35 36 37	DQ36 DQ37 DQ17 DQ9 NC DQ10	61 62 63 64 65	NC NC Vss NC RAS1
47 49 49 50 51 52 55 57 58 66 000000000000000000000000000000000	3 4 5 6 7 8 9	DQ1 DQ2 DQ3 DQ4 DQ5 DQ6	33 34 35 36	DQ17 DQ9 NC	63 64 65	Vss NC
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	4 5 6 7 8 9	DQ2 DQ3 DQ4 DQ5 DQ6	34 35 36	DQ9 NC	64 65	NC
6 50 50 50 50 50 50 50 50 50 50 50 50 50	5 6 7 8 9	DQ3 DQ4 DQ5 DQ6	35 36	NC	65	
7 8 9 9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	6 7 8 9	DQ4 DQ5 DQ6	36			DV61
9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	7 8 9 10	DQ5 DQ6		DQ10	CC	ונהטו
101 0000000000000000000000000000000000	8 9 10	DQ6	37		66	CAS2
12 55 13 57 14 55 58 16 60 00 00 61 17 18 00 00 00 62 20 00 00 00 63 21 00 00 00 64 22 00 00 66 23 00 00 67	9			Vcc	67	Vss
14 55 57 58 16 60 60 61 17 66 62 20 63 64 21 22 20 66 67	10		38	DQ11	68	CAS3
15 59 60 17 00 0 61 18 00 0 62 21 22 22 23 00 67		Vcc	39	DQ12	69	RAS3
17 80 61 18 000 62 20 000 63 21 22 000 65 22 23 000 67		DQ7	40	DQ13	70	WE
18 000 62 19 000 63 20 000 64 21 000 66 22 000 67	. 11	NC	41	DQ14	71	PD1 (Vss)
20 00 63 21 00 65 22 00 66 23 00 67	12	DQ8	42	DQ15	72	PD3 (Vss)
21 00 65 22 00 66 23 00 67	13	A0	43	DQ16	73	Vss
23 00 66	14	A2	44	Vss	74	PD5 (Vss)
	15	Vcc	45	Vss	75	PD7 (TBD)
24 00 68 25 00 68	16	A4	46	DQ18	76	PD8 (NC)
26 QQ 69 70	17	NC	47	DQ19	77	DQ38
26 0 70 27 0 71 28 0 72	18	A6	48	DQ20	78	DQ39
28 00 72 29 00 73 30 00 73	19	A8	49	DQ21	79	DQ35
31 OO 74 31 OO 75	20	NC	50	DQ22	80	DQ27
31 00 74 32 00 76 33 00 77 34 00 78 35 00 79 36 00 81	21	NC	51	DQ23	81	DQ28
34 QQ 77 78	22	RAS0	52	DQ24	82	DQ29
35 00 79 36 00 79	23	CAS0	53	DQ25	83	DQ30
37 OO 80 81	24	CAS1	54	DQ26	84	DQ31
38 OO 82 39 OO 82 40 OO 83	25	NC	55	OE (Vss)	85	DQ32
40 QQ 83 40 QQ 84	26	RAS2	56	Vss	86	DQ33
41 00 85 42 00 85	27	Vcc	57	A1	87	DQ34
42 00 86 43 00 87 44 00 88	28	PD2 (Vss)	58	A3	88	Vss
44 OO 88	29	PD4 (Vss)	59	A5		
	30	PD6 (TBD)	60	A7		

Multiple \overline{RAS} inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory array may be divided into two banks, each with four separate bytes (x32/36 only). In the x16/18/20 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each \overline{RAS} selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT24D88C51240 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT24D88C51240 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1, B2, B5 and B6 = 256K x 11 memory blocks; B3, B4, B7 and B8 = 256K x 9 memory blocks.
- OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION					
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 9 row address bits. Four RAS inputs allow for two x32/36/40 banks or four x16/18/20 banks.					
23, 24, 66, 68	CAS ₀₋₃	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration (not in x40 mode).					
70	70 WE Input Write Enable: WE is the READ/WRIT pins. If WE is LOW prior to CAS going is an EARLY-WRITE cycle. If WE is LOW, the access is a READ cycle, pr LOW. If WE goes LOW after CAS good cycle is a LATE-WRITE cycle. A LATT generally used in conjuction with a RI READ-MODIFY-WRITE cycle.							
55	ŌĒ	Input	Output Enable: \overline{OE} is the input/output control for the DQ pins. \overline{OE} is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.					
13, 57, 14, 58, 16, 59, 18, 60, 19	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.					
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.					
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).					
11, 17, 20, 21, 25, 35, 61, 62, 64	NC		No Connect: These pins should be left unconnected (reserved for future use).					
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%					
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground					

FUNCTIONAL DESCRIPTION

The MT24D88C51240 is a 2 megabyte memory card structured as a 512K x 32/36/40 bit memory array ($\overline{RAS0}$ = $\overline{RAS2}$, $\overline{RAS1} = \overline{RAS3}$). It also may be configured as a 1 Meg x 16/18/20 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four RAS

Most x32/36/40 bit applications use the same signal to control the CAS inputs. RASO and RAS1 control the lower 16/18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16/18 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each \overline{RAS} is then a bank select for the 1 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 64ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if WE goes LOW after CAS, the outputs (Q) will be activated and will drive invalid data to the inputs. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C51240 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, four thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C51240 operates reliably up to 55°C.



MEMORY TRUTH TABLE

						ADDRE	SSES	DATA IN/OUT
FUNCTION	r in the sign	RAS	CAS	WE	0E	^t R	tC	DQ0-DQ39
Standby	and the second of the second o	Н	H→X	Х	Х	Х	Х	High-Z
READ		L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L,	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L. L.	Х	Х	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	TERISTICS	3			PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
1MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	NC	X	Х	Х
• 2MB	256K x 1, 4, 16, 18	18	9	9	512	Vss	Vss	Vss	Vss	Vss	X	X	Х
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
4MB 8MB	1 Meg x 1, 4, 16, 18 1 Meg x 1, 4, 16, 18	20 20	10 10	10 10	1,024 1,024	Vss Vss	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Tim	ing		100ns			Х	Х	Х	Х	Х	Vss	Vss	X
			80)ns		X	Х	Х	Х	Х	NC	Vss	Х
			70)ns		Х	X	Х	Х	Х	Vss	NC	Х
			60)ns	and the second second	Х	X	X	Х	Х	NC	NC	Х
			50)ns		Х	Х	Х	Х	Х	Vss	Vss	Х
Refresh Cor	ntrol		Star	ndard		Х	Х	Х	Х	Х	Х	Х	NC
			Ai	uto		Х	Х	Х	Х	Х	Х	Х	Vss

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss0.5V to +	-5.25V
Operating Temperature, T _A (Ambient)0°C to	+55°C
Storage Temperature20°C to	
Power Dissipation	15W
Short Circuit Output Current	50mA
Card Insertions (Connector's Life Cycle)	10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	٧	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le V \text{In} \le 5.25V$; all other pins not under test = 0V)	Buffered	lв	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	/ouт ≤ 5.25V)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)		Vон	2.4		٧	
Output Fight Voltage (Iout = -5HA) Output Low Voltage (Iout = 4.2mA)		Vol		0.4	٧	

			MAX]	
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	lcc1	48	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	1.0	0.9	0.8	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	780	660	540	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = VIH: TRC = TRC (MIN))	lcc5	1.0	0.9	0.8	Α	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	1.0	0.9	0.8	Α	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125µs; WE, A0-A8 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	4.8	4.8	4.8	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A8, OE	Cii		9	pF	2
Input Capacitance: WE	C ₁₂		13	pF	2
Input Capacitance: RAS0, RAS1, RAS2, RAS3	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS			-6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time							The annual section		
Access time from RAS	^t RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25	1	30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	^t RSH	25		30		30		ns	26
RAS precharge time	tRP	40		50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55		65	1 2 200	75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	tCP	10		10		10		ns	23
RAS to CAS delay time	^t RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	†ASR	10		10		10		ns	26
Row address hold time	^t RAH	5		5		5	1	ns	25
RAS to column address delay time	tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	tASC	5		5		5		ns	24
Column address hold time	^t CAH	15		20		20	3-5-1	ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5	1	ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5	1	5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS			6		-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH.	15		20	1	20		ns	24
Write command hold time	tWCR	40		50		55		ns	25
(referenced to RAS)									
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	^t DS	5		5		5		ns	24, 32
Data-in hold time	^t DH	5		10		10	4.	ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	The second
RAS to CAS precharge time	tRPC	10		10		10		ns	26
CAS setup time	^t CSR	20		20		20		ns	5, 26
(CAS-BEFORE-RAS refresh)							974		
CAS hold time	tCHR	10		10		10		ns	5, 25
(CAS-BEFORE-RAS refresh)								1	
WE hold time	^t WRH	5		5		5	* -	ns	22, 25
(CAS-BEFORE-RAS refresh)	1.						<u> </u>		
WE setup time	tWRP	20)	20		20		ns	22, 26
(CAS-BEFORE-RAS refresh)								1	
WE hold time	tWTH	5	İ	5		5		ns	22, 25
(WCBR test cycle)									
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185	<u> </u>	205		ns	
FAST-PAGE-MODE	^t PRWC	90		95		100		ns	23
READ-WRITE cycle time	 			ļ		1			
RAS to WE delay time	tRWD	80	11	90		100		ns	31, 27
Column Address	tAWD	65	[70		75		ns	31, 24
to WE delay time					ļ				<u> </u>
CAS to WE delay time	tCWD	50		65	1	55		ns	31, 24
Output buffer turn-off delay	[†] OE		25		30		30	ns	20, 33, 26
Output disable	^t OD		25		30		30	ns	35, 26
OE hold time from WE during	tOEH	5	1	10		10	1.0	ns	34, 27
READ-MODIFY-WRITE cycle					122			1	1
OE hold time from RAS during	^t ORD	10		10	1	10	1	ns	21, 26
HIDDEN REFRESH cycle			1						- 114 M



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- .8. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

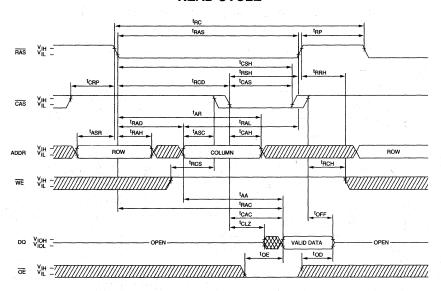
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, \overline{WE} = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
- 31. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

NOTES (continued)

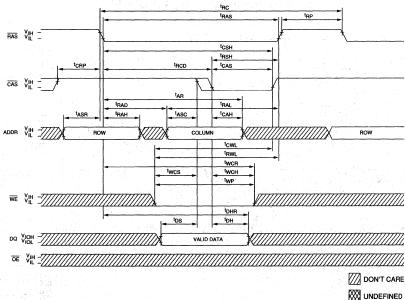
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 33. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and \overline{OE} is taken back LOW after 'OEH is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



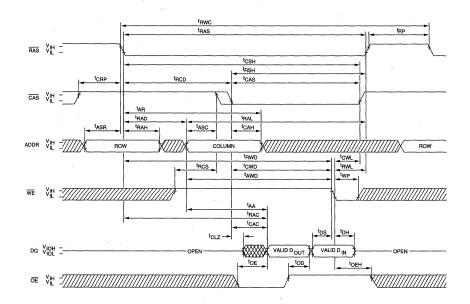
READ CYCLE



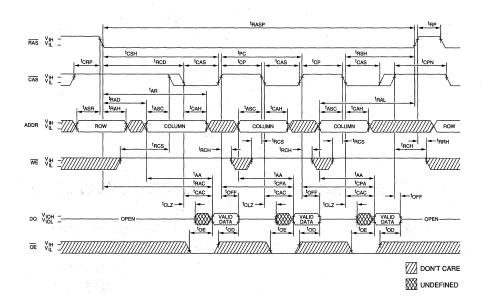
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

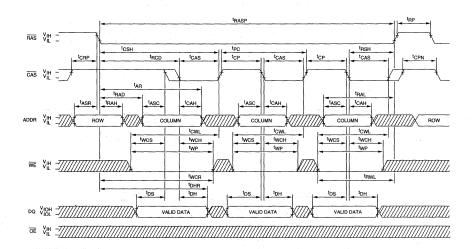


FAST-PAGE-MODE READ CYCLE

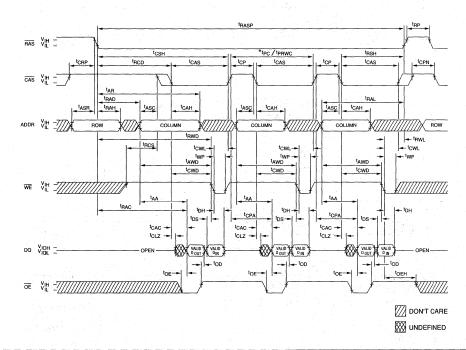




FAST-PAGE-MODE EARLY-WRITE CYCLE

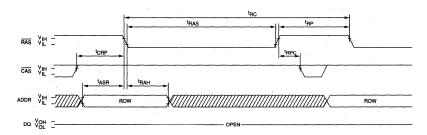


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

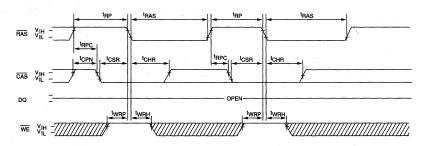


4-149

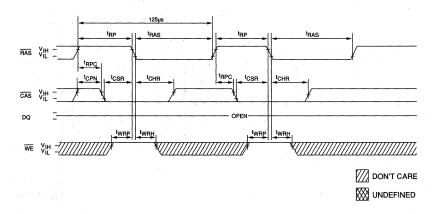
RAS-ONLY REFRESH CYCLE (ADDR = A0-A8; WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE (A0-A8 = DON'T CARE)

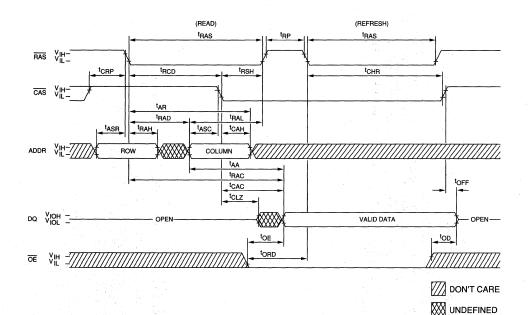


BATTERY BACKUP REFRESH CYCLE (A0-A8 = DON'T CARE)





HIDDEN REFRESH CYCLE 21 (WE = HIGH)



RESERVED JEDEC, JEIDA and PCMCIA 88-PIN ASSIGNMENT

(All Possible Combinations)

DQ0 DQ18 DQ19 DQ1 47 DQ2 48 DQ20 5 6 7 DQ3 DQ4 DQ22 DQ5 DQ23 DQ6 DQ24 52 53 DQ25 DQ7 54 DQ26 OE 3.3V Vcc DQ8 55 12 56 57 58 59 A0 13 A2 A3 A5 5.0V Vcc Α4 60 Α7 3.3V Vcc A6 17 18 62 A8 19 Vss A13 RAS1 A10 64 65 A12 RAS0 CAS0 CAS1 22 23 24 66 Vss CAS3 RAS3 WE 3.3V Vcc RAS2 25 69 70 5.0V Vcc 71 PD1 PD2 28 29 30 72 PD3 PD4 PD6 73 Vss DQ36 31 PD7 DQ37 76 77 PD8 DQ17 DQ38 DQ9 34 35 78 DQ39 3.3V Vcc DQ10 36 DQ27 5.0V Vcc 37 81 DQ28 DQ11 82 DQ29 DQ12 39 DQ30 83 DQ13 40 DQ14 41 DQ15 42 DQ31 84 DQ33 43 DQ16 87 DQ34 88 Vss

MT24D88C51240 PIN ASSIGNMENT

(JEDEC Standard)

		\Box		
Vss DQ0 DQ1 DQ1 DQ2 DQ3 DQ1 DQ3 DQ3 DQ4 DQ5 DQ7 NC DQ8 A0 A2 Vcc A6 A8 NC NC NC NC DQ8 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ7 DQ1 DQ3 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6 PQ6	1 2 3 4 4 5 6 7 8 9 10 11 12 13 14 15 6 17 18 9 20 1 12 22 23 24 25 26 27 28 29 30 31 22 25 30 31 32 33 34 4 4 24 34 44	000000000000000000000000000000000000000	45 46 47 48 49 50 51 52 53 54 55 66 66 67 68 69 77 77 77 78 79 80 81 82 83 84 84 86 86 87 88 88 88 88 88 88 88 88 88 88 88 88	Vss D018 D019 D020 D021 D022 D022 D022 D022 D022 D022



IC DRAM CARD

4 MEGABYTES

1 MEG x 40, 2 MEG x 20

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- · Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 12mW standby, 3.3W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS

MARKING

•	Timing
	60ns access
	70ns access
	80ns access

-6 -7

-8

GENERAL DESCRIPTION

The MT12D88C140 is a 4 megabyte, IC DRAM card organized primarily as a 1 Meg x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 2 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT12D88C140 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)



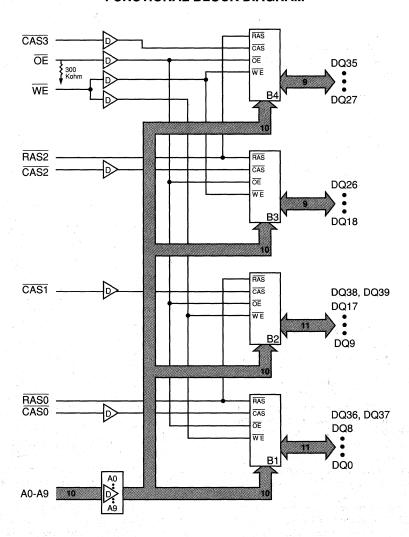
PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
45 1	Vss	31	DQ36	61	A9
6 2	DQ0	32	DQ37	62	NC
3	DQ1	33	DQ17	63	Vss
8 3	DQ2	34	DQ9	64	NC
5	DQ3	35	NC	65	NC
6	DQ4	36	DQ10	66	CAS2
4 7	DQ5	37	Vcc	67	Vss
5 8	DQ6	38	DQ11	68	CAS3
7 9	Vcc	39	DQ12	69	NC
58 59 10	DQ7	40	DQ13	70	WE
60 11	NC	41	DQ14	71	PD1 (Vss)
61 12	DQ8	42	DQ15	72	PD3 (Vss)
63 13 64	A0	43	DQ16	73	Vss
14	A2	44	Vss	74	PD5 (NC)
36 15	Vcc	45	Vss	75	PD7 (TBD)
67 16	A4	46	DQ18	76	PD8 (NC)
17	NC	47	DQ19	77	DQ38
18	A6	48	DQ20	78	DQ39
72 19	A8	49	DQ21	79	DQ35
4 20	NC	50	DQ22	80	DQ27
75 76 21	NC	51	DQ23	81	DQ28
77 22	RAS0	52	DQ24	82	DQ29
78 79 23	CASO	53	DQ25	83	DQ30
80 24	CAS1	54	DQ26	84	DQ31
82 25	NC .	55	OE (Vss)	85	DQ32
83 26	RAS2	56	Vss	86	DQ33
85 27	Vcc	57	A1	87	DQ34
86 87 28	PD2 (NC)	58	A3	88	Vss
88 29	PD4 (Vss)	59	A5		
30	PD6 (TBD)	60	A7		

Multiple \overline{RAS} inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory is a single array that may be divided into four separate bytes (x32/36 only). In the x16/18/20 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each \overline{RAS} selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT12D88C140 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT12D88C140 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1 and B2 = 1 Meg x 11 memory blocks; B3 and B4 = 1 Meg x 9 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to DRAM.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26	RASO, RAS2	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. Two RAS inputs allow for a single x32/36/40 bank or two x16/18/20 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjuction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	ŌĒ	Input	Output Enable: OE is the input/output control for the DQ pins. OE is connected to ground through a 300 Kohm resistor and is intended to be LOW allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36, 38-43, 33, 46-54, 80-87, 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25, 35, 62, 64, 65, 69	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT12D88C140 is a 4 megabyte memory card as a 1 Meg x 32/36/40 bit memory array (RAS0 = RAS2). It also may be configured as a 2 Meg x 16/18/20 bit memory array provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32/36/40 bit applications use the same signal to control the CAS inputs. RASO controls the lower 16/18 bits and RAS2 controls the upper 16 bits to obtain a x32/36 memory array. For x16/18 applications, the corresponding DQs and the corresponding CAS pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and CASO to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the 2 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BAT-TERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the penalty is the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE); if WE goes LOW after CAS, the outputs (Q) will be activated and will drive invalid data to the inputs, unless LATE-WRITE CYCLE timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by \overline{WE} .

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS followed by a column address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the ICDRAM card are buffered, with the exception of RAS inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system line drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and nonbuffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT12D88C140 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 12 thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT12D88C140 operates reliably up to 55°C.



MEMORY TRUTH TABLE

					144	ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	0E	^t R .	tC t	DQ0-DQ39
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ		L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	Х	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	· H - , ,	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	Х	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		L	Χ	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	L	L	Х	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	Н	Х	Χ	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	Х	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

	CHARAC	CTERISTICS	3				PRESENT DETECT PIN (PDx)						
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х
1MB 2MB	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18	18 18	9 9	9 9	512 512	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X
• 4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	Х	Х	Х
8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	Х	Х	X
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X
Access Tim	ing		100ns			X	Х	Х	Х	X	Vss	Vss	Х
			80)ns		X	Х	Х	Х	Х	NC	Vss	Х
		1	70)ns		Х	Х	Х	Х	Х	Vss	NC	Х
		ş m	60ns				Х	Х	Х	Х	NC	NC	Х
		50ns					Х	Х	Х	Х	Vss	Vss	Х
Refresh Cor	ntrol	Standard				X	Х	Х	Х	Х	Х	Х	NC
		3,111	Au	uto	x x x x x x x						Vss		

NOTE: Vss = Ground.

ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 55^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	٧	1
Input High (Logic 1) Voltage, All Inputs		ViH	3.5	Vcc+0.5	V	1
Input Low (Logic 0) Voltage, All Inputs		VIL	-0.5	0.8	٧,	1
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μА	
$(0V \le V_{IN} \le 5.25V$; all other pins not under test = $0V$)	Buffered	Ів	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	⁄оuт ≤ 5.25V)	loz	-10	10	μΑ	
OUTPUT LEVELS Output High Voltage (Iout = -5mA)		Vон	2.4		٧	
Output Low Voltage (lout = 4.2mA)		Vol	4	0.4	٧	

				1		
	<u> </u>		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	24	24	24	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	2.4	2.4	2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc3	1.26	1.14	1.02	Α	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	900	780	660	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = Vin: ^t RC = ^t RC (MIN))	lcc5	1.26	1.14	1.02	А	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ¹RC = ¹RC (MIN))	lcc6	1.26	1.14	1.02	А	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = tRAS (MIN) up to 300ns; tRC = 125µs; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	3.6	3.6	3.6	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CAS0, CAS1, CAS2, CAS3, A0-A9, OE	Cıı		9	pF	2
Input Capacitance: WE	C ₁₂	1. 1	13	ρF	2
Input Capacitance: RAS0, RAS2	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		12	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		, ** · · ·	-6		-7		-8	14/16	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE	^t PC	40		40		45		ns	23
READ or WRITE cycle time							garter.		-
Access time from RAS	†RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	25		30		30		ns	26
RAS precharge time	tRP	45		50		60		ns	23
CAS pulse width	^t CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	^t CSH	55	100000000000000000000000000000000000000	65		75		ns	25
CAS precharge time	^t CPN	10		10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	^t RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	^t CRP	15		15		15		ns	26
Row address setup time	†ASR	10		10	1.5.5,545.94	10		ns	26
Row address hold time	^t RAH	5		5		5		ns	25
RAS to column address delay time	^t RAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	†ASC	5		5		5		ns	24
Column address hold time	[†] CAH	15	1	20		20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	^t RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	tRCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	^t CLZ	5		5		5		ns	24
Output buffer turn-off delay	^t OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5		5		5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-(6		7		-8		100
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20	- 1944	ns	24
Write command hold time (referenced to RAS)	^t WCR	40		50		55		ns	25
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	tRWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5		5		5		ns	24, 32
Data-in hold time	^t DH	5	:	10		10		ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	tΤ	2	15	2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	†REF		128		128		128	ms	1 1
RAS to CAS precharge time	^t RPC	10		10		10	12.	ns	26
CAS setup time (CAS-BEFORE-RAS refresh)	^t CSR	20		20		20		ns	5, 26
CAS hold time (CAS-BEFORE-RAS refresh)	^t CHR	10		10		10		ns	5, 25
WE hold time (CAS-BEFORE-RAS refresh)	^t WRH	5		5		5	,	ns	22, 25
WE setup time (CAS-BEFORE-RAS refresh)	^t WRP	20		20		20		ns	22, 26
WE hold time (WCBR test cycle)	[†] WTH	5		5		5		ns	22, 25
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	7
FAST-PAGE-MODE READ-WRITE cycle time	^t PRWC	90		95		100		ns	23
RAS to WE delay time	tRWD	80		90		100		ns	31, 27
Column Address to WE delay time	^t AWD	65		70		75		ns	31, 24
CAS to WE delay time	^t CWD	50		65		55		ns	31, 24
Output buffer turn-off delay	†OE		25		30		30	ns	20, 33, 26
Output disable	^t OD		25		30		30	ns	35, 26
OE hold time from WE during READ-MODIFY-WRITE cycle	[†] OEH	5		10		10	1,44	ns	34, 27
OE hold time from RAS during HIDDEN REFRESH cycle	^t ORD	10		10		10	1 313	ns	21, 26



NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and 100pF.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

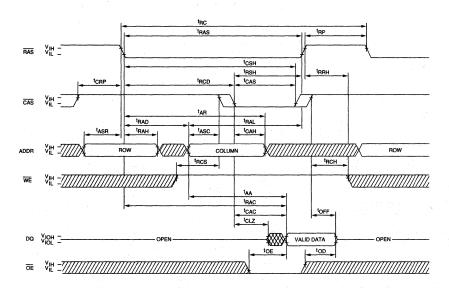
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
- 31. ¹WCS, ¹RWD, †AWD and ¹CWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ¹WCS ≥ ¹WCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ¹RWD ≥ ¹RWD (MIN), ¹AWD ≥ ¹AWD (MIN) and ¹CWD ≥ ¹CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.



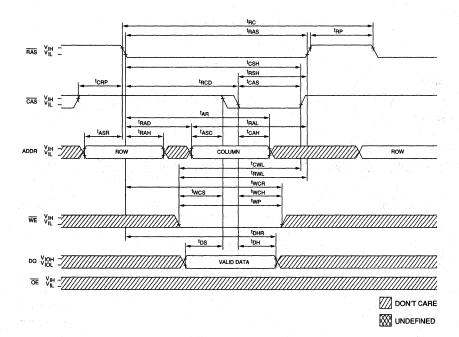
NOTES (continued)

- 32. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- 33. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both tOD and tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and OE is taken back LOW after 'OEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once tOD or tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).

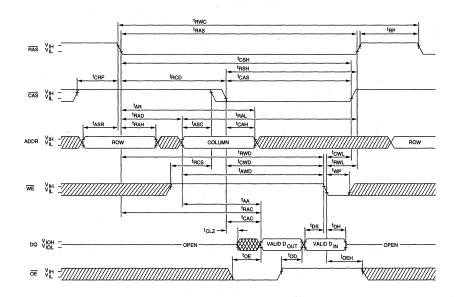
READ CYCLE



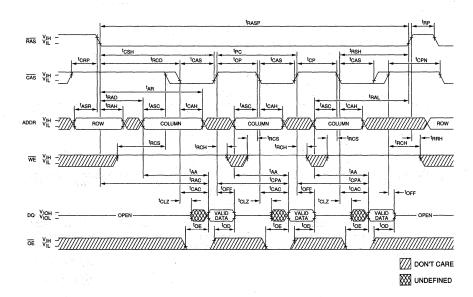
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

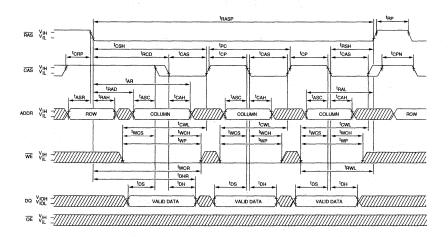


FAST-PAGE-MODE READ CYCLE

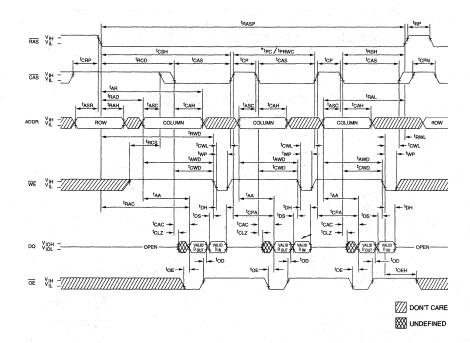




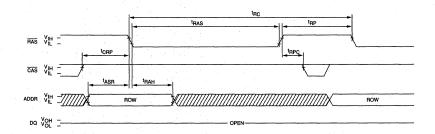
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

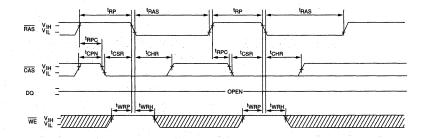


RAS-ONLY REFRESH CYCLE (ADDR = A0-A9; WE = DON'T CARE)



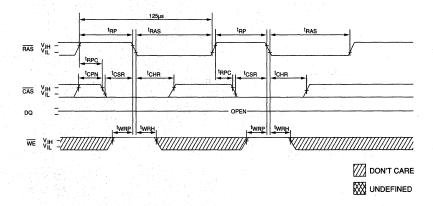
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



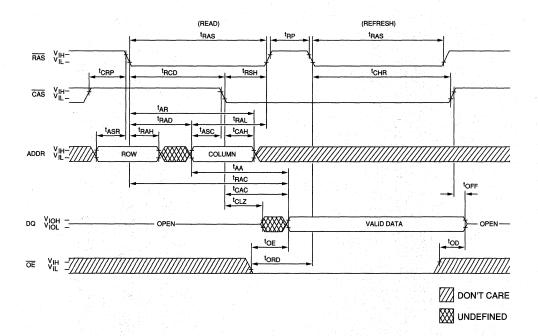
BATTERY BACKUP REFRESH CYCLE

(A0-A9 = DON'T CARE)





HIDDEN REFRESH CYCLE 21 (WE = HIGH)

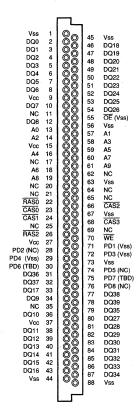


RESERVED JEDEC, JEIDA and PCMCIA **88-PIN ASSIGNMENT**

(All Possible Combinations)

Vss DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 5.0V Vcc DQ8 A0 0.3V Vcc A4 3.3V Vcc A8 A10 0.12 RAS0 CAS0 CAS0 3.3V Vcc RAS2 DQ7 0.3S V Vcc DQ10 0.3S V Vcc DQ10 0.3S V Vcc DQ10 0.3S V Vcc DQ10 0.3S V Vcc DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 Vss	1 2 3 4 4 5 6 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 3 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44	000000000000000000000000000000000000000	45 46 47 48 49 50 51 52 53 55 56 60 61 62 63 64 65 66 67 77 77 77 77 78 79 80 81 82 83 84 85 86 87 88 88 88 88 88 88 88 88 88 88 88 88	Vss D018 D019 D020 D021 D022 D022 D022 D022 D022 D022

MT12D88C140 PIN ASSIGNMENT (JEDEC Standard)





IC DRAM CARD

8 MEGABYTES

2 MEG x 40, 4 MEG x 20

FEATURES

- JEIDA, JEDEC and PCMCIA standard 88-pin IC DRAM card
- Polarized receptacle connector
- Industry standard DRAM functions and timing
- High-performance, CMOS silicon-gate process
- All outputs are fully TTL compatible
- All inputs buffered except RAS inputs
- Multiple RAS inputs for x16/18/20 or x32/36/40 selectability
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU)
- FAST PAGE MODE access cycle
- Single +5V ±5% power supply
- Low power; 24mW standby, 3.3W active (typical)
- Extended refresh standard: 1,024 cycles every 128ms

OPTIONS MARKING Timing 60ns access 70ns access -7 80ns access

GENERAL DESCRIPTION

The MT24D88C240 is an 8 megabyte, IC DRAM card organized primarily as a 2 Meg x 40 bit memory array for EDC applications. It may be used as a x32 or x36 bit memory array (the unused DQs should be tied to Vss or Vcc through current limiting resistors). It may also be configured as a 4 Meg x 20 bit memory array, provided the corresponding DQs on the host system are made common and memory bank control procedures are implemented. Separate CAS inputs allow byte accesses.

All inputs to the DRAMs are buffered, with the exception of RAS. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. At the same time, the line drivers add delays to the buffered input timings when compared to standard DRAMs.

The MT24D88C240 is designed for low power operation using 1 Meg x 4 low power, extended refresh DRAMs. These devices support BATTERY BACKUP (BBU) cycle refresh; a very low current, data retention mode. Standard component DRAM refresh modes are supported as well.

PIN ASSIGNMENT (End View) 88-Pin Card (U-1)



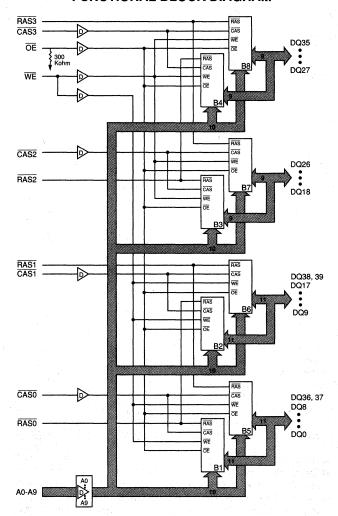
47.		PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
- 1	Q _Q 45	. 1	Vss	31	DQ36	61	A9
2		2	DQ0	32	DQ37	62	NC
4			DQ1	33	DQ17	63	Vss
5		14	DQ2	34	DQ9	64	NC
. 7	SO 50		DQ3	35	NC	65	RAS1
8		6	DQ4	36	DQ10	66	CAS2
10		. 7	DQ5	37	Vcc	67	Vss
12			DQ6	38	DQ11	68	CAS3
13	86 57	9	Vcc	39	DQ12	69	RAS3
15	O 58		DQ7	40	DQ13	70	WE
16		11	NC	41	DQ14	71	PD1 (Vss)
18			DQ8	42	DQ15	72	PD3 (Vss)
19		13	A0	43	DQ16	73	Vss
21 22	00 64 65		A2	44	Vss	74	PD5 (Vss)
23			Vcc	45	Vss	75	PD7 (TBD)
24 25		16	A4	46	DQ18	76	PD8 (NC)
26			NC	47	DQ19	77	DQ38
27	80 71	18	A6	48	DQ20	78	DQ39
29			A8	49	DQ21	79	DQ35
30	80 74		NC	50	DQ22	80	DQ27
32 33	00 75 76		NC	51	DQ23	81	DQ28
34			RAS0	52	DQ24	82	DQ29
35 36		23	CAS0	53	DQ25	83	DQ30
37			CAS1	54	DQ26	84	DQ31
38		25	NC	55	OE (Vss)	85	DQ32
40	00 44 00 44 00 45 00 55 00 55		RAS2	56	Vss	86	DQ33
41 42		27	Vcc	57	A1	87	DQ34
43 44			PD2 (NC)	58	A3	88	Vss
44	00 8		PD4 (Vss)	59	A 5		
	L	30	PD6 (TBD)	60	A7		

Multiple RAS inputs conserve power by allowing individual bank selection. In the x32/36/40 organization, the memory array may be divided into two banks, each with four separate bytes (x32/36 only). In the x16/18/20 organization, up to four banks, each with two separate bytes, may be independently selected. One bank is activated by each RAS selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence detect pins may be read by the host to identify the MT24D88C240 organization, number of banks, access time and refresh mode. These extensive presence detect functions allow systems to utilize the advanced power saving features.

The MT24D88C240 is built with a plastic frame covered by stainless steel panels. This package, containing an 88-pin receptacle connector, is keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM



NOTE:

- 1. D = 74AC11244 line drivers.
- 2. B1, B2, B5 and B6 = 1 Meg x 8 memory blocks; B3, B4, B7 and B8 = 1 Meg x 9 memory blocks.
- 3. OE is internally connected to ground via a 300 Kohm resistor and is also buffered to the DRAMs.



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	RAS0-3	Input	Row Address Strobe: RAS is used to clock-in the 10 row-address bits. Four RAS inputs allow for two x32/36/40 banks or four x16/18/20 banks.
23, 24, 66, 68	CAS0-3	Input	Column Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration (not in x40 mode).
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY-WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE-WRITE cycle. A LATE-WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
55	ŌĒ	Input	Output Enable: \overline{OE} is the input/output control for the DQ pins. \overline{OE} is connected to ground through a 300 Kohm resistor and is intended to be LOW, allowing for EARLY-WRITE cycles only. This signal may be driven, allowing for LATE-WRITE cycles.
13, 57, 14, 58, 16, 59 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 12, 34, 36 38-43, 33, 46-54, 80-87 79, 31, 32, 77, 78	DQ0-DQ39	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ39 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select (x32/36 mode only). For READ access cycles, DQ0-DQ39 act as outputs for the addressed DRAM location.
71, 28, 72, 29 74, 30, 75, 76	PD1-PD8		Presence Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or they will be grounded (Vss).
11, 17, 20, 21, 25 35, 62, 64	NC		No Connect: These pins should be left unconnected (reserved for future use).
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ± 5%
1, 44, 45, 56 63, 67, 73, 88	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT24D88C240 is an 8 megabyte memory card structured as a 2 Meg x 32/36/40 bit memory array ($\overline{RAS0} = \overline{RAS2}$, $\overline{RAS1} = \overline{RAS3}$). It also may be configured as a 4 Meg x 16/18/20 bit memory array, provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving all four \overline{RAS} lines.

Most x32/36/40 bit applications use the same signal to control the \overline{CAS} inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16/18 bits, and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16/18 bits, to obtain a x32/36/40 memory array. For x16/18 applications, the corresponding DQs and the corresponding \overline{CAS} pins must be connected together (DQ0 to DQ18, DQ1 to DQ19 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each \overline{RAS} is then a bank select for the 4 Meg x 16/18 memory organization.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle [READ, WRITE, RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN or BATTERY BACKUP (BBU) REFRESH] so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 128ms, regardless of sequence.

The implied method of choice for refreshing the memory card is the BBU cycle. This is a very low current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (ICC7).

The memory card may be used with the other refresh modes common in standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the BBU REFRESH cycle. However, the memory card will draw more current in the STANDBY mode. The CBR REFRESH mode is recommended when not using the BBU mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. READ or WRITE cycles are selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of \overline{CAS} . \overline{WE} must fall prior to \overline{CAS} (EARLY WRITE); if \overline{WE} goes LOW after \overline{CAS} , the outputs (Q) will be

activated and will drive invalid data to the inputs, unless LATE-WRITE cycle timing specifications are met. The data inputs and data outputs are routed through pins using common I/O, and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by \overline{RAS} followed by a column address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation. Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} high time.

DRAM TIMING

In accordance with JEDEC standard specifications, all inputs to the IC DRAM card are buffered, with the exception of \overline{RAS} inputs. The line drivers used for buffers reduce reflections on the card and ensure compatibility in a wide range of systems. The implementation of buffers on the card may relieve the need for additional host system lin drivers. Notes 23 though 29 indicate which parameters on the IC DRAM card are affected by the line drivers, and to what magnitude they are affected. The component DRAM timing specifications, rather than those of the IC DRAM card (in systems that use both), may cause timing incompatibilities.

All traces on the IC DRAM card (buffered and non-buffered) are approximately 50 ohms characteristic impedance. Matching impedance on the system board to 50 ohms characteristic impedance on traces to the IC DRAM card will decrease signal noise to the IC DRAM card, enhancing overall system reliability.

PHYSICAL DESIGN

The MT24D88C240 is constructed with a molded plastic frame and covered with stainless steel panels. Inside, 24 thin small-outline package (TSOP) DRAMs are mounted on both sides of an ultrathin printed circuit board. The board is attached to a high insertion, 88-pin receptacle connector. The package has a polarized key to prevent improper installation, including insertion into other types of IC card sockets. The MT24D88C240 operates reliably up to 55°C.



MEMORY TRUTH TABLE

in division with the con-		2 - 2 - 2 - 2	1.			ADDRE	SSES	DATA IN/OUT
FUNCTION		RAS	CAS	WE	OE	t _R	tC	DQ0-DQ39
Standby		Н	H→X	Х	Х	Х	Х	High-Z
READ	100	L	L	Н	L (NC)	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	Н	L (NC)	ROW	COL	Data Out
READ	2nd Cycle	L	H→L	Н	L (NC)	n/a	COL	Data Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
EARLY-WRITE	2nd Cycle	L	H→L	L	Х	n/a	COL	Data In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data In
RAS-ONLY REFRESH		Н	Х	Х	Х	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	Н	L (NC)	ROW	COL	Data Out
REFRESH	WRITE	L→H→L	· Line	L	X	ROW	COL	Data In
CAS-BEFORE-RAS RE	FRESH	H→L	L	Н	Н	Χ	Х	High-Z
BATTERY BACKUP RE	FRESH	H→L	L	Н	H	Х	Х	High-Z

PRESENCE DETECT TRUTH TABLE

CHARACTERISTICS							PRESENT DETECT PIN (PDx)							
Card Density	DRAM Organizations	Card Address	RAS Address	CAS Address	Page Depth	1	2	3	4	5	6	7	8	
0MB	No card installed	Х	Х	Х	Х	NC	NC	NC	NC	NC	Х	Х	Х	
1MB 2MB	256K x 1, 4, 16, 18 256K x 1, 4, 16, 18	18 18	9 9	9 9	512 512	Vss Vss	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X	
2MB 4MB	512K x 8, 9 512K x 8, 9	19 19	10 10	9 9	512 512	NC NC	Vss Vss	Vss Vss	Vss Vss	NC Vss	X	X	X	
4MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	NC	Х	Х	Х	
• 8MB	1 Meg x 1, 4, 16, 18	20	10	10	1,024	Vss	NC	Vss	Vss	Vss	Х	X	Х	
8MB 16MB	2 Meg x 8, 9 2 Meg x 8, 9	21 21	11 11	10 10	1,024 1,024	NC NC	NC NC	Vss Vss	Vss Vss	NC Vss	X	X	X	
16MB 32MB	4 Meg x 1, 4, 16, 18 4 Meg x 1, 4, 16, 18	22 22	12 12	11 11	1,024 1,024	Vss Vss	Vss Vss	NC NC	Vss Vss	NC Vss	X	X	X	
Access Timing		100ns				X	Х	Х	Х	Х	Vss	Vss	Х	
		80ns				Х	Х	Х	Х	Х	NC	Vss	Х	
		70ns				Х	Х	Х	Х	Х	Vss	NC	Х	
		60ns				Х	Х	Х	Х	Х	NC	NC	Х	
		50ns				Х	Х	Х	Х	Х	Vss	Vss	Х	
Refresh Control		Standard				Х	Х	Х	Х	Х	Х	X	NC	
			Auto				Х	Х	Х	Х	Х	Х	Vss	

NOTE: Vss = Ground.



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	0.5V to +5.25V
Operating Temperature TA (Ambient)	0°C to 55°C
Storage Temperature	
Power Dissipation	15W
Short Circuit Output Current	
Card Insertions (Connector's Life Cycle)	10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) $(0^{\circ}C \le T_A \le 55^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage	Vcc	4.75	5.25	٧	1	
Input High (Logic 1) Voltage, All Inputs	ViH	3.5	Vcc+0.5	٧	1	
Input Low (Logic 0) Voltage, All Inputs	VIL	-0.5	0.8	٧	- 1	
INPUT LEAKAGE CURRENT, Any input	Non-buffered	lin	-12	12	μΑ	
$(0V \le VIN \le 5.25V$; all other pins not under test = $0V$)	Buffered	Ів	-2	2	μΑ	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V	'ουτ ≤ 5.25V)	loz	-10	10	μΑ	2
OUTPUT LEVELS	:	Vон	2.4		٧	
Output High Voltage (Ιουτ = -5mA) Output Low Voltage (Ιουτ = 4.2mA)		Vol		0.4	٧	

			MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = Vih)	lcc ₁	48	48	48	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	lcc2	4.8	4.8	4.8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	lcc3	1.26	1.14	1.02	A	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: PC = PC (MIN))	lcc4	900	780	660	mA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = ViH: ¹RC = ¹RC (MIN))	lcc5	1.26	1.14	1.02	Α	3, 30
REFRESH CURRENT: CAS-BEFORE-RAS (CBR) Average power supply current (RAS, CAS, Address Cycling: ^t RC = ^t RC (MIN))	Icc6	1.26	1.14	1.02	Α	3, 5, 30
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BBU: CAS = 0.2V or CBR cycling; RAS = ^t RAS (MIN) up to 300ns; ^t RC = 125μs; WE, A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	lcc7	7.2	7.2	7.2	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CASO, CAS1, CAS2, CAS3, A0-A9, OE	Cit		9	pF	2
Input Capacitance: WE	Cı2		13	pF	2
Input Capacitance: RASO, RAS1, RAS2, RAS3	Сіз		50	pF	2
Input/Output Capacitance: DQ	Сю		20	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($0^{\circ}C \le T_A \le 55^{\circ}C$; $Vcc = 5V \pm 5\%$)

AC CHARACTERISTICS			-6		-7	-24	-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^t RC	110		130		150		ns	23
FAST-PAGE-MODE READ or WRITE cycle time	^t PC	40		40		45		ns	23
Access time from RAS	^t RAC		60		70		80	ns	14, 23
Access time from CAS	^t CAC		25		30		30	ns	15, 26
Access time from column address	^t AA		40		45		50	ns	26
Access time from CAS precharge	^t CPA		50		50		55	ns	26
RAS pulse width	†RAS	60	100,000	70	100,000	80	100,000	ns	23
RAS pulse width (FAST PAGE MODE)	†RASP	60	100,000	70	100,000	80	100,000	ns	23
RAS hold time	tRSH	25		30		30		ns	26
RAS precharge time	tRP	45		50		60		ns	23
CAS pulse width	†CAS	15	100,000	20	100,000	20	100,000	ns	23
CAS hold time	tCSH	55		65		75		ns	25
CAS precharge time	^t CPN	10	1	10		10		ns	16, 23
CAS precharge time (FAST PAGE MODE)	^t CP	10		10		10		ns	23
RAS to CAS delay time	†RCD	10	35	15	40	15	50	ns	17, 28
CAS to RAS precharge time	tCRP	15		15		15		ns	26
Row address setup time	^t ASR	10		10		10		ns	26
Row address hold time	tRAH	5		5		5		ns	25
RAS to column address delay time	tRAD	10	20	10	25	10	30	ns	18, 28
Column address setup time	tASC	5		5		5	1 2 2 2 2 2	ns	24
Column address hold time	†CAH	15	 	20	1	20		ns	24
Column address hold time (referenced to RAS)	^t AR	45		50		55		ns	25
Column address to RAS lead time	†RAL	40		45		50		ns	26
Read command setup time	tRCS	5		5		5		ns	25
Read command hold time (referenced to CAS)	^t RCH	5		5		5		ns	19, 24
Read command hold time (referenced to RAS)	^t RRH	-5		-5		-5		ns	19, 25
CAS to output in Low-Z	†CLZ	5		5		5		ns	24
Output buffer turn-off delay	[†] OFF	5	30	5	30	5	30	ns	20, 29, 35
WE command setup time	twcs	5	1	5	1	5		ns	24



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq 55°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-	6	T	7		-8	T	
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command hold time	tWCH	15		20		20		ns	24
Write command hold time	tWCR	40		50		55		ns	25
(referenced to RAS)									
Write command pulse width	tWP	10		15		15		ns	23
Write command to RAS lead time	^t RWL	25		30		30		ns	26
Write command to CAS lead time	tCWL	20		25		25		ns	24
Data-in setup time	tDS	5	1.5	5		5		ns	24, 32
Data-in hold time	^t DH	5		10		10		ns	25, 32
Data-in hold time (referenced to RAS)	^t DHR	45		55		60		ns	23
Transition time (rise or fall)	ŀΤ	2	15	. 2	15	2	15	ns	9, 10, 23
Refresh period (1,024 cycles)	^t REF		128		128		128	ms	
RAS to CAS precharge time	tRPC	10		10		10		ns	26
CAS setup time	^t CSR	20		20		20		ns	5, 26
(CAS-BEFORE-RAS refresh)									
CAS hold time	^t CHR	10		10		10		ns	5, 25
(CAS-BEFORE-RAS refresh)									
WE hold time	^t WRH	5		5		5		ns	22, 25
(CAS-BEFORE-RAS refresh)									
WE setup time	tWRP	20		20	j	20		ns	22, 26
(CAS-BEFORE-RAS refresh)					1				
WE hold time	^t WTH	5		5		5		ns	22, 25
(WCBR test cycle)									
WE setup time	tWTS	20		20		20		ns	22, 26
READ-WRITE cycle time	tRWC	165		185		205		ns	1
FAST-PAGE-MODE	^t PRWC	90		95		100		ns	23
READ-WRITE cycle time									
RAS to WE delay time	tRWD	80		90		100		ns	31, 27
Column Address	tAWD	65		70		75		ns	31, 24
to WE delay time					1 1			1	
CAS to WE delay time	tCMD	50		65	1.0	55		ns	31, 24
Output buffer turn-off delay	†OE		25		30		30	ns	20, 33, 26
Output disable	[†] OD		25		30		30	ns	35, 26
OE hold time from WE during	^t OEH	5		10		10		ns	34, 27
READ-MODIFY-WRITE cycle									100
OE hold time from RAS during	^t ORD	10		10		10		ns	21, 26
HIDDEN REFRESH cycle					1 1				



NOTES

- All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- 6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- 7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- 9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and Vін).
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
- 12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 13. Measured with a load equivalent to 2 TTL gates and
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by tAA.

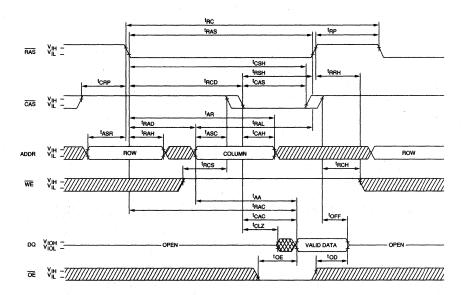
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ
- 20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to Voh or Vol.
- 21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
- 22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR refresh cycle.
- 23. Timing between the DRAMs and the DRAM card did not change with the addition of the line drivers.
- 24. A +5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 25. A -5ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 26. A +10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 27. A -10ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 28. A -5ns (MIN) and a -10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 29. A +5ns (MIN) and a +10ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
- 30. The maximum current ratings are based with the memory operating or being refreshed in the x32/36/ 40 mode. The stated maximums may be reduced by one half when used in the x16/18/20 mode.
- 31. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in late WRITE, and READ-MODIFY-WRITE cycles only. If ${}^{t}WCS \ge {}^{t}WCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle.

NOTES (continued)

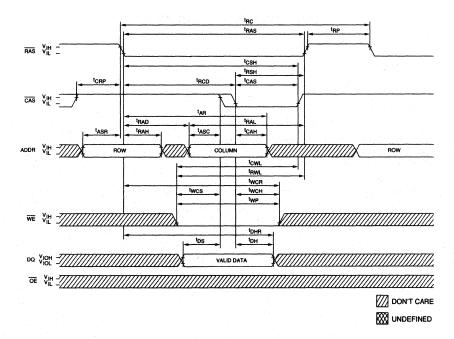
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- 34. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS
- remains LOW and \overline{OE} is taken back LOW after 'OEH is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
- 35. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



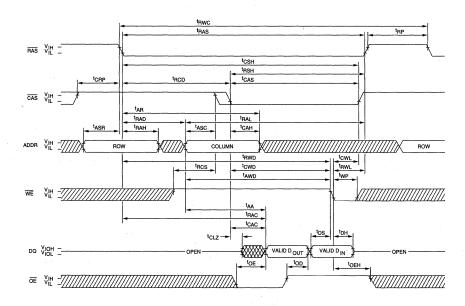
READ CYCLE



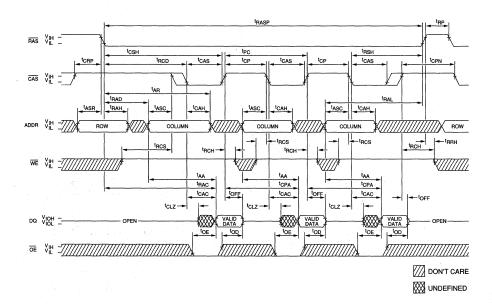
EARLY-WRITE CYCLE



READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

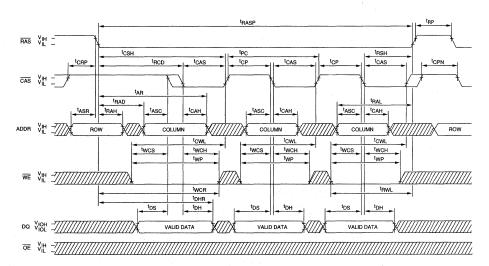


FAST-PAGE-MODE READ CYCLE

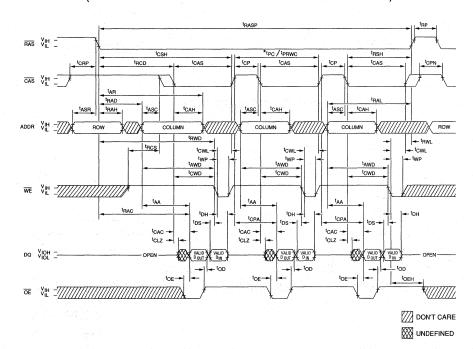




FAST-PAGE-MODE EARLY-WRITE CYCLE

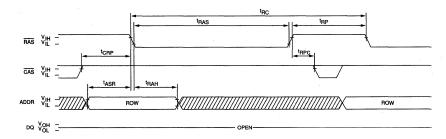


FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



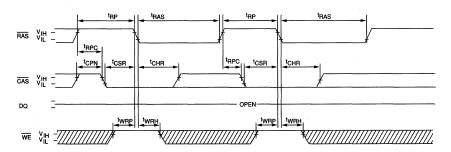
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A9; WE = DON'T CARE)



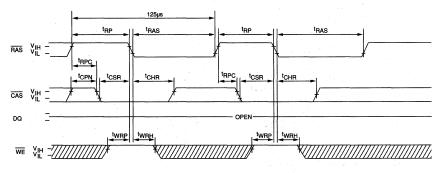
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A9 = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE

(A0-A9 = DON'T CARE)



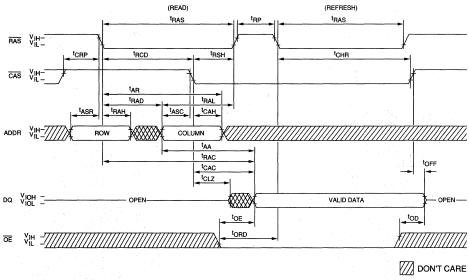
DON'T CARE





HIDDEN REFRESH CYCLE 21

 $(\overline{WE} = HIGH)$



₩ UNDEFINED



RESERVED JEDEC, JEIDA and PCMCIA **88-PIN ASSIGNMENT**

(All Possible Combinations)

Vss DQ0 DQ18 DQ1 DQ2 3 4 5 47 DQ19 48 DQ20 DQ3 49 50 DQ21 DO22 DQ5 51 DQ23 DQ6 52 DQ24 5.0V Vcc 53 DQ7 10 54 55 56 57 58 3.3V Vcc DQ8 A0 A1 **A**2 5.0V Vcc 15 A4 16 60 Α7 3.3V Vcc A9 A11 Vss 61 62 63 64 65 18 Α8 A10 A13 RAS1 21 22 23 A12 RAS0 66 CAS₂ CAS0 CAS1 67 68 Vss CAS3 3.3V Vcc RAS2 5.0V Vcc PD2 69 RAS3 26 27 28 70 72 PD3 PD4 29 73 74 75 76 Vss PD6 PD5 DQ36 PD7 DQ37 32 PD8 DQ17 33 DQ9 34 DQ39 3.3V Vcc 35 79 DQ35 DQ10 36 80 DQ27 5.0V Vcc 37 81 DQ28 DQ11 38 82 DQ29 DQ12 39 DQ13 40 83 DQ30 84 DQ31 DQ14 41 85 DQ32 DQ15 42 86 DQ33 DQ16 43

87 DQ34

88 Vss

Vss

MT24D88C240 PIN ASSIGNMENT

(JEDEC Standard)

Vss DQ0 DQ1 DQ2 DQ3 DQ3 DQ4 DQ5 DQ6 VCC DQ7 NC DQ8 A0 A2 Vcc A6 A8 NC NC RAS9 CAS9 PD2 (NC) PD4 (Vss) PD6 (TBD) DQ36 DQ37 DQ17 DQ9 NC DQ10 Vcc DQ10 Vcc DQ11 DQ12 DQ13 DQ14 SQ15 DQ15 SQ16 SQ16 SQ16 SQ16 SQ16 SQ16 SQ16 SQ16	1 2 3 4 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 11 12 22 23 24 25 26 27 28 29 30 31 32 33 34 53 63 73 83 94 04 14 24 34 44	000000000000000000000000000000000000000	45 46 47 48 49 50 51 52 53 55 56 61 62 63 64 66 67 70 77 78 77 78 77 78 77 78 77 78 78 78 78	Vss DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ26 DQ26 DQ26 DQ26 DQ26 DQ26 DQ27 A7 A9 NC Vss NC RAS1 CAS2 WE PD1 (Vss) PD5 (Vss) Vss DQ38 DQ39 DQ36 DQ39 DQ36 DQ29 DQ30 DQ31 DQ32 DQ31 DQ34 Vss

MICHON TECHNOLOGY, INC.

DYNAMIC RAMS
WIDE DRAMS2
DRAM MODULES
IC DRAM CARDS4
MULTIPORT DRAMS5
APPLICATION/TECHNICAL NOTES6
PRODUCT RELIABILITY
PACKAGEINFORMATION8
SALES INFORMATION 9



DUAL PORT DRAM (VRAM) PRODUCT SELECTION GUIDE

Memory	Access	Part	Access	Power Dissipation Package and		age and I	Number of	Pins		
Configuration	Cycle	Number	Time (ns)	Standby	Active	SOJ	SOG	TSOP	ZIP	Page
256K x 4	FP	MT42C4255	80, 100	15mW	275mW	28	-	-	28	5-1
256K x 4	FP, BW, LP	MT42C4256	70, 80, 100	15mW	275mW	28	-	, . -	28	5-3
128K x 8	FP	MT42C8127	80, 100	15mW	275mW	40	-	-	-	5-39
128K x 8	FP, BW, LP	MT42C8128	70, 80, 100	15mW	275mW	40	-	40/44	-	5-41
256K x 8	FP, BW	MT42C8255	70, 80	10mW	300mW	40	-	40/44	-	5-79
256K x 8	FP, BW	MT42C8256	70, 80	10mW	300mW	40	-	40/44	-	5-111
256K x 16	FP, BW	MT42C256K16A1	60, 70, 80	10mW	350mW	- "	64	-	-	5-153

FP = Fast Page Mode, BW = Block Write, LP = Low Power, Extended Refresh

TRIPLE PORT DRAM PRODUCT SELECTION GUIDE

Memory	Access	Part Access Power Dissipation		ssipation	Pack	age/Nu	mber of	Pins		
Configuration	Cycle	Number	Time (ns)	Standby	Active	SOJ	SOG	TSOP	PLCC	Page
256K x 4	FP, BW, QSF pin	MT43C4257	80, 100	15mW	500mW	40	-	40/44	-	5-155
256K x 4	FP, BW, SSF pin	MT43C4258	80, 100	15mW	500mW	40	-	40/44	-	5-155
128K x 8	FP, BW, QSF pin	MT43C8128	80, 100	15mW	550mW	-	-	-	52	5-201
128K x 8	FP, BW, SSF pin	MT43C8129	80, 100	15mW	550mW	-	-	-	52	5-201
256K x 8	FP, BW	MT43C256K8A1	60, 70, 80	15mW	400mW	-	64	-	-	5-247

FP = Fast Page Mode, BW = Block Write



VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- · High-performance, CMOS silicon-gate process
- Single $+5V \pm 10\%$ (-10), $+5V \pm 5\%$ (-8S) power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
 512 x 4 SAM port
- · No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times 80ns random, 25ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS

MARKING

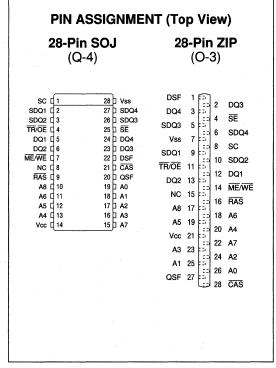
• Timing [DRAM, SAM (cycl	e/access)]
80ns, 25ns/25ns	-8S
100ns, 30ns/30ns	-10
 Packages 	

Plastic SOJ (400 mil) DJ Plastic ZIP (375 mil) Z

GENERAL DESCRIPTION

The MT42C4255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Four 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 4-bit random access I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.



Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4255 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, allow further enhancements to system performance.



VRAM

256K x 4 DRAM WITH 512 x 4 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms, with 32ms option
- Optional FAST PAGE MODE access cycles
- Dual port organization: 256K x 4 DRAM port
 512 x 4 SAM port
- No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times 70ns random, 22ns serial

SPECIAL FUNCTIONS

- IEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS

MARKING

Timing [DRAM, SAM (cycle/access)]	
70ns, 25ns/22ns	- 7
80ns, 30ns/25ns	- 8
100ns, 30ns/27ns	-10
Packages	
Plastic SOJ (400 mil)	DJ
Plastic ZIP (375 mil)	\mathbf{Z}
	70ns, 25ns/22ns 80ns, 30ns/25ns 100ns, 30ns/27ns Packages Plastic SOJ (400 mil)

GENERAL DESCRIPTION

Low power/extended refresh (32ms)

The MT42C4256 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed by a 4-bit wide DRAM port or by a 512 x 4-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM. An extended refresh (32ms), low power standby option is available as the MT42C4256 L.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K \times 4 DRAM). Four 512-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths; the 4-bit random access

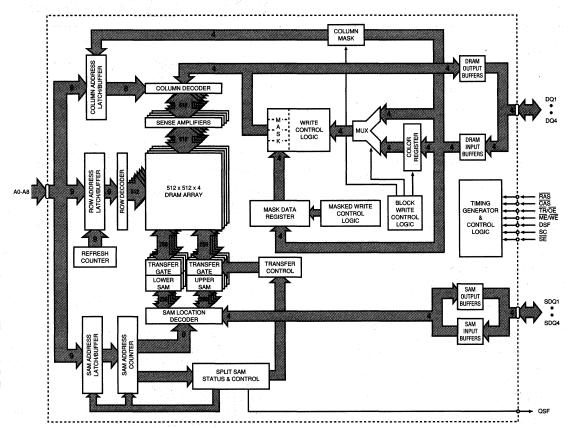
28-Pin		28-Pin ZIP						
(Q-	4)	((O-3)					
SC [1	28 Vss	DSF	1 2 DQ3					
SDQ1 [2	27 SDQ4	DQ4	3 =					
SDQ2 [3	26 SDQ3	SDQ3	5 = 4 SE					
TR/OE [4	25 D SE		== 6 SDQ4					
DQ1 [5	24 DQ4	Vss	7 = 8 SC					
DQ2 [6	23 DQ3	SDQ1	9 =					
ME/WE [7	22 DSF	TR/OE 1	10 SDQ2					
NC [8	21 🗆 CAS		== 12 DO1					
RAS [9	20 QSF	DQ2 1	13 = 14 ME/WE					
A8 ☐ 10	19 🗎 A0	NC 1	15 to					
A6 ☐ 11	18 🛭 A1	A8 1	17 == 16 RAS					
A5 🛘 12	17 🛘 A2	A5 1	19 == 18 A6					
A4 🛘 13	16 🗆 A3		== 20 A4					
Vcc [14	15 A7	Vcc 2	21 💷					
		A3 2	22 A7					
		A1 2	25 = 24 A2					
		AI Z	25 = 26 A0					

I/O port, the four internal 512 bit wide paths between the DRAM and the SAM, and the 4-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. Refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 8ms, or 32ms for the MT42C4256 L, (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C4256 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
	8	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
4	11	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at RAS (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a High-Z state.
7	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS a MASKED WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
25	4	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. SE is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
22		DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used on a particular access cycle.
9	16	RAS	Input	Row Address Strobe: RAS is used to clock-in the 9 row- address bits and strobe the ME/WE, TR/OE, DSF, SE, CAS and DQ inputs. It also acts as the master chip enable and must fall for initiation of any DRAM or TRANSFER cycle.
21	28	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe the DSF input.
19, 18, 17, 16, 13, 12, 11, 15, 10	26, 25, 24, 23, 20, 19, 18, 22, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and the SAM start address (when CAS goes LOW).
5, 6, 23, 24	12, 13, 2, 3	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2, 3, 26, 27	9, 10, 5, 6	SDQ1-SDQ4	Input/ Output	Serial Data I/O: Input, output, or High-Z.
20	27	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
8	15	NC		No Connect: This pin should be left either unconnected or tied to ground.
14	21	Vcc	Supply	Power Supply: +5V ±10%
28	7	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C4256 may be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note:

For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C4256 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C4256 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for \overline{RAS} -ONLY refresh cycles. The DQ pins remain in a High-Z state for both the \overline{RAS} -ONLY and \overline{CAS} -BEFORE- \overline{RAS} refresh cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C4256 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has several special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, \overline{RAS} and \overline{CAS} inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when \overline{RAS} transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when \overline{CAS} goes from HIGH-to-LOW.

Note:

 \overline{RAS} also acts as a "master" chip enable for the VRAM. If \overline{RAS} is inactive, HIGH, all other DRAM control pins (\overline{CAS} , $\overline{TR}/\overline{OE}$, $\overline{ME}/\overline{WE}$, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without \overline{RAS} falling.

For single port DRAMS, the \overline{OE} pin is a "don't care" when \overline{RAS} goes LOW. However, for the VRAM, when \overline{RAS} goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANS-FER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition for all DRAM operations (except \overline{CAS} -BEFORE- \overline{RAS}).

If $(\overline{\text{ME}})/\overline{\text{WE}}$ is HIGH when $\overline{\text{CAS}}$ goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The $(\overline{\text{TR}})/\overline{\text{OE}}$ input must transition from HIGH-to-LOW some time after $\overline{\text{RAS}}$ falls to enable the DRAM output port.

For single port normal DRAMs, \overline{WE} is a "don't care" when \overline{RAS} goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when \overline{RAS} goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the \overline{RAS} HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition. If $(\overline{ME})/\overline{WE}$ is LOW before \overline{CAS} goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells. If $(\overline{ME})/\overline{WE}$ goes LOW after \overline{CAS} goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.



NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within a 4-bit word. The MT42C4256 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF are LOW at the $\overline{\text{RAS}}$ HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and

allows normal WRITE operation to proceed. Note that \overline{CAS} is still HIGH. When \overline{CAS} goes LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every \overline{RAS} cycle) if DSF is LOW when \overline{RAS} goes LOW. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE \overline{RAS} cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

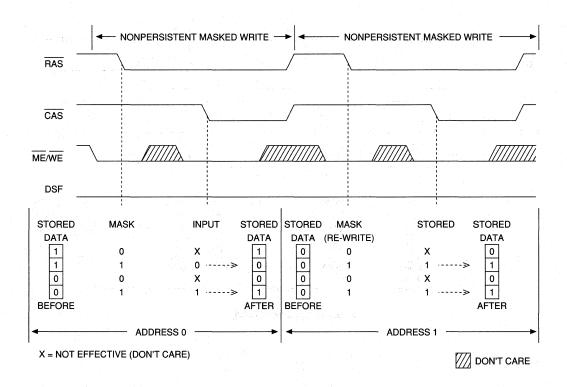


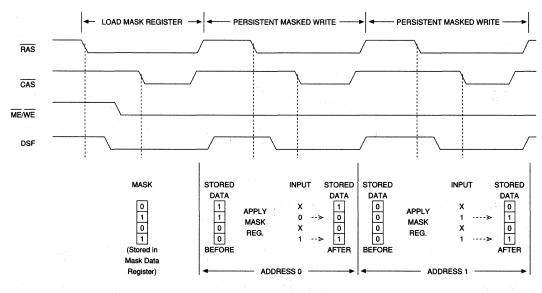
Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF HIGH when $\overline{\text{RAS}}$ goes LOW. The mask data is loaded into the internal register when $\overline{\text{CAS}}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF HIGH when $\overline{\text{RAS}}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask

register when \overline{RAS} falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at \overline{RAS} time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations may be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.



X = NOT EFFECTIVE (DON'T CARE)

Figure 2 PERSISTENT MASKED WRITE EXAMPLE

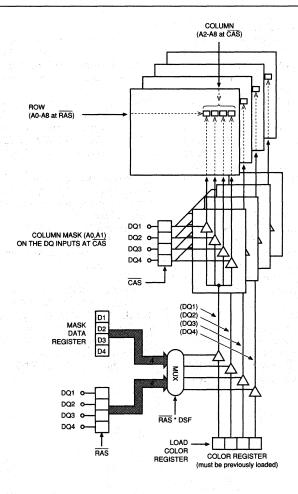


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when CAS goes LOW, the MT42C4256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle.

However, when $\overline{\text{CAS}}$ goes LOW only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs are then used to determine what combination of the four column locations will be changed. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0=1, A1=0; DQ3 controls A0=0, A1=1; and DQ4 controls A0=1, A1=1. The write enable controls are active HIGH; the WRITE function is enabled by a logic 1 and disabled by a logic 0.

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE, except that the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of ME/(WE) LOW and DSF LOW when RAS goes LOW initiates a NONPERSISTENT MASKED cycle. The DSF pin must be driven HIGH when CAS goes LOW, to perform the NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes or column locations may be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when CAS goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when \overline{RAS} goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when \overline{RAS} goes LOW indicates the cycle is a LOAD REGIS-

TER cycle. DSF is used when \overline{CAS} goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note:

For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSISTENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when CAS goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.



TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{\text{TR}}/(\overline{\text{OE}})$ is LOW then $\overline{\text{RAS}}$ goes LOW. The state of $(\overline{\text{ME}})/\overline{\text{WE}}$ when $\overline{\text{RAS}}$ goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If (ME)/WE is HIGH and DSF is LOW when RAS goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the four 512-bit DRAM row planes that are to be transferred to the four SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. CAS must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized

with SC (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after CAS goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), \overline{TR} / (OE) may go HIGH before CAS goes LOW (refer to the AC Timing Diagrams). The 2.048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 9-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 255), and HIGH if access is from the upper half (256 through 511). If \overline{SE} is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. SE enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of SE. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

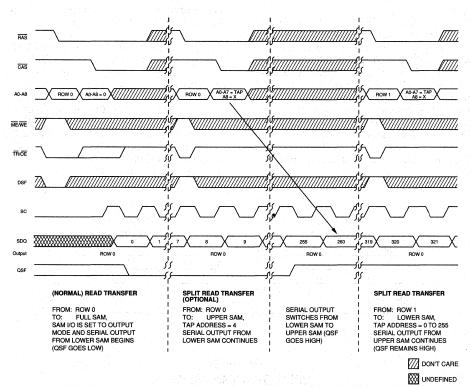


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of \overline{RAS} or \overline{CAS} . The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to set SAM I/O direction and provide a reference to which half of the SAM the access will begin. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when RAS goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of CAS. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half is \neq 0. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1), the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half a Tap address of "0" will be used. Access will start at 0 if going to the lower half, or 256 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously except $(\overline{ME})/\overline{WE}$ and \overline{SE} must be LOW when \overline{RAS} goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QFS is LOW if access is to the lower half of the SAM, and HIGH if access is to the upper half.

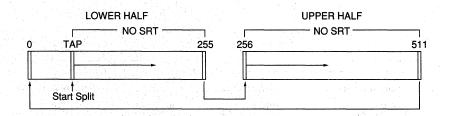


Figure 5
SPLIT SAM TRANSFER



PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with SE held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{ME})/\overline{WE}$ is LOW when \overline{RAS} goes LOW, allowing \overline{SE} to be a "don't care." This allows the outputs to be disabled using \overline{SE} during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUT-PUT are SC and \overline{SE} . The rising edge of SC increments the serial address counter and provides access to the next SAM location. \overline{SE} enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. SE is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether SE is HIGH or LOW. The address progresses through the SAM

and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. \overline{SE} acts as a write enable for serial input data and must be LOW for valid serial input. If \overline{SE} = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the \overline{SE} input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100 μ s minimum, eight RAS cycles must be executed to initialize the dynamic memory array. Micron recommends that RAS = $(TR)/OE \ge VIH$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C4256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High-Z, regardless of the state of $\overline{\text{SE}}$. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.



TRUTH TABLE

			RAS	FALLING	EDGE		CAS FALL	A0-A81		DQ1-DQ4 ²		REGISTERS	
CODE	FUNCTION	CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS	RAS	CAS,WE ³	MASK	COLOR
	DRAM OPERATIONS	····											
CBR	CAS-BEFORE-RAS REFRESH	0	X	х	х	х	X		X	_	х	×	Х
ROR	RAS-ONLY REFRESH	1	1	х	Х	×	I - "	ROW	_	х	T - T	×	х
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	х	0	ROW	COLUMN	Х	VALID	Х	Х
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	х	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	х	0	ROW	COLUMN	х	VALID DATA	USE	х
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1.3.	1	1	0	х	1	ROW	COLUMN (A2-A8)	, X	COLUMN MASK	x	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	Х	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD &	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	. 1	х	1	ROW	COLUMN (A2-A8)	х	COLUMN MASK	USE	USE
	REGISTER OPERATIONS												
LMR	LOAD MASK REGISTER	1	1	1	. 1	x	0	ROW ⁴	x	x	WRITE MASK	LOAD	×
LCR	LOAD COLOR REGISTER	1	1	- 1	1	Х	1	ROW ⁴	X	х	COLOR DATA	X	LOAD
	TRANSFER OPERATIONS												
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	, 1,	0	1	0	×	х	ROW	TAP ⁵	×	X	х	х
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	×	х	ROW	TAP ⁵	×	X	Х	x
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	х	ROW	TAP ⁵	х	Х	Х	х
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)	- 1	0	0	0	1	х	ROW ⁴	TAP ⁵	х	X	х	Х
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	1	Х	х	ROW	TAP ⁵	х	х	Х	х

NOTE:

- 1. These columns show what must be present on the A0-A8 inputs when RAS falls and when CAS falls.
- 2. These columns show what must be present on the DQ1-DQ4 inputs when RAS falls and when CAS falls.
- On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
- 4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
- 5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient).	0°C to +70°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{A} \leq 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V \leq Vin \leq Vcc); all other pins not under test = 0V	lL .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ Vouт ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS	Vон	2.4		V	
Output High Voltage (Iουτ = -2.5mA) Output Low Voltage (Ιουτ = 2.5mA)	Vol		0.4	v	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SC, SE, DSF	C ₁₂	Januar (A)	7	pF	2
Input/Output Capacitance: DQ, SDQ	Cı/o		9	pF	2
Output Capacitance: QSF	Co		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

· ·						
$0^{\circ}\text{C} \le \text{T}_{A} \le 70^{\circ}\text{C}$; $\text{Vcc} = 5\text{V} \pm 10\%$)			MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	lcc1	95	85	75	mA	3, 4 26
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: ¹ PC = ¹ PC (MIN))	lcc2	85	75	65	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Viн after 8 RAS cycles (MIN), other inputs ≥ Viн or ≤ Vil)	lcc3	8	8	8	mA	4
STANDBY CURRENT: CMOS INPUT LEVELS (MT42C4256 L only) $(\overline{RAS} = \overline{CAS} \ge Vcc -0.2V, other inputs \ge Vcc -0.2V or \le -0.2V)$	Icc4	500	500	500	μА	4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vih)	Icc5	95	85	75	mA	3, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	Icc6	95	85	75	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) MT42C4256 L only Average power supply current during BATTERY BACKUP refresh: $\overline{CAS} \leq 0.2V$ or \overline{CAS} -BEFORE- \overline{RAS} cycling; $\overline{RAS} = {}^{t}RAS$ (MIN) to 300ns; $\overline{ME/WE}$, A0-A8 and DQs $\geq Vcc$ - 0.2V or $\leq 0.2V$ (DQs may be left open), ${}^{t}RC = 62.5\mu s$ (512 rows at 62.5 $\mu s = 32ms$)	lcc7	600	600	600	μА	3, 5
SAM/DRAM DATA TRANSFER	Iccs.	105	95	95	mA	3

CURRENT DRAIN, SAM ACTIVE (tSC = MIN)

$0^{\circ}C \le I_A \le 70^{\circ}C$; $VCC = 5V \pm 10\%$)			MAX		1	
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ¹ RC = ¹ RC (MIN))	Icc9	150	130	120	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: PC = PC (MIN))	lcc10	140	120	110	mA	3, 4, 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Viн after 8 RAS cycles (MIN), other inputs ≥ Viн or ≤ Vil)	lcc11	55	45	45	mA	3, 4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vih)	lcc12	150	130	120	mA	3, 4, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	lcc13	150	130	120	mA	3, 4, 5
SAM/DRAM DATA TRANSFER	Icc14	160	130	125	mA	3, 4



DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-7		-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t _{RC}	130		150		180		ns	
READ-MODIFY-WRITE cycle time	^t RWC	175		190		230	- 1	ns	
FAST-PAGE-MODE READ or WRITE	t _{PC}	45		50		55		ns	
cycle time									
FAST-PAGE-MODE READ-MODIFY-WRITE	^t PRWC	90		95		110		ns	
cycle time								41.77	
Access time from RAS	^t RAC	30A.1	70		80		100	ns	14
Access time from CAS	¹ CAC		20		25		25	ns	15
Access time from (TR)/OE	^t OE		20	-	20		25	ns	
Access time from column address	t _{AA}	a produce	35		40		45	ns	
Access time from CAS precharge	^t CPA		40		45		50	ns	
RAS pulse width	†RAS	70	20,000	80	20,000	100	20,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		25		25		ns	Page 1
RAS precharge time	tRP	50	10000	60		70		ns	
CAS pulse width	†CAS	20	10,000	25	10,000	25	10,000	ns	10000
CAS hold time	^t CSH	70	133.1	80		100		ns	
CAS precharge time	^t CP	10	347.0	10		10	N. H. Marie	ns	
RAS to CAS delay time	tRCD	20	50	20	55	25	75	ns	17
CAS to RAS precharge time	tCRP	10		10		10		ns	1987
Row address setup time	†ASR	0	0.00	0		0		ns	
Row address hold time	†RAH	10		10		15		ns	
RAS to column	tRAD	15	35	15	40	20	50	ns	18
address delay time					1				To Black
Column address setup time	†ASC	0		0		0		ns	The service
Column address hold time	^t CAH	15	1.16	15		15		ns	To be
Column address hold time	tAR.	45		55		70		ns	
(referenced to RAS)							1.4		
Column address to	tRAL	35		40		50		ns	
RAS lead time									
Read command setup time	tRCS	0		0		0		ns	
Read command hold time	tRCH	0		0		0		ns	19
(referenced to CAS)									1 1 8
Read command hold time	tRRH	0		0		0		ns	19
(referenced to RAS)									
CAS to output in Low-Z	tCLZ	3		3		3		ns	
Output buffer	^t OFF	3	20	3	20	3	20	ns	20, 23
turn-off delay									
Output disable	tOD	3	10	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	^t OEH	10		10		20		ns	25
OE LOW to RAS HIGH delay time	†ROH	0		0	1 1	0	1	ns	



DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS			7		-8	-	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	twcs	0		0		0	4	ns	21
Write command hold time	†WCH	15		15		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		70		ns	
Write command pulse width	tWP	15		15		15		ns	
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	^t DS	0		.0		0		ns	22
Data-in hold time	^t DH	15	14.	15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45	-	55		65		ns	
RAS to WE delay time	tRWD	90		100		130		ns	21
Column address to WE delay time	^t AWD	55		65		75		ns	21
CAS to WE delay time	^t CWD	.40		45		55		ns	21
Transition time (rise or fall)	t _T	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF		8 (32)		8 (32)		8 (32)	ms	29
RAS to CAS precharge time	^t RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	tCSR	10		10		10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	[†] CHR	10		10	: '	10		ns	5
ME/WE to RAS setup time	tWSR	0		0		0		ns	
ME/WE to RAS hold time	tRWH	15		15	<u> </u>	15		ns	
Mask Data to RAS setup time	tMS	0		0		0	1 18 -	ns	
Mask Data to RAS hold time	tMH	15		15		15	1000	ns	



TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-7		-8	-	10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
TR/(OE) LOW to RAS setup time	†TLS	0		0		0		ns	
TR/(OE) LOW to RAS hold time	tTLH	15	10,000	15	10,000	15	10,000	ns	
TR/(OE) LOW to RAS hold time (REAL-TIME READ TRANSFER only)	^t RTH	65	10,000	70	10,000	80	10,000	ns	
TR/(OE) LOW to CAS hold time (REAL-TIME READ TRANSFER only)	^t CTH	25		25		25		ns	
TR/(OE) HIGH to SC lead time	^t TSL	5		, 5		5		ns	
TR/(OE) HIGH to RAS precharge time	^t TRP	50		60		70		ns	
TR/(OE) precharge time	^t TRW	20		20		30	1	ns	12.00
First SC edge to TR/(OE) HIGH delay time	^t TSD	15		15		15		ns	
Serial output buffer turn-off delay from RAS	^t SDZ	7	40	7	40	7	40	ns	
SC to RAS setup time	tSRS	25		30		30		ns	
Serial data input to SE delay time	†SZE	0		0		0		ns	
Serial data input delay from RAS	tSDD	50		50		50		ns	1,10
Serial data input to RAS delay time	tszs	0		0		0		ns	100
Serial-input-mode enable (SE) to RAS setup time	^t ESR	0		0		0		ns	
Serial-input-mode enable (SE) to RAS hold time	^t REH	15		15		15		ns	
TR/(OE) HIGH to RAS setup time	tYS	0		0		0		ns	
TR/(OE) HIGH to RAS hold time	tYH	15		15		15	1	ns	
DSF to RAS setup time	tFSR	0		0		0		ns	
DSF to RAS hold time	^t RFH	15		15		15		ns	
SC to QSF delay time	tSQD		30		30	· · · · · · · · · · · · · · · · · · ·	30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		0		ns	
RAS to QSF delay time	tRQD		75		75		75	ns	
DSF to RAS hold time	tFHR.	45		55		70		ns	
DSF to CAS setup time	tFSC	0		0		0		ns	
DSF to CAS hold time	^t CFH	15		15		20		ns	
TR/OE to QSF delay time	^t TQD		25		25		25	ns	
CAS to QSF delay time	tCQD		35		35		35	ns	
RAS to first SC delay	tRSD	80		80		80		ns	
CAS to first SC delay	tCSD	30		30		30		ns	



SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock-cycle time	tsc	25		30		30		ns	
Access time from SC	†SAC		22		25		27	ns	24, 28
SC precharge time (SC LOW time)	tSP	- 8		10		10		ns	
SC pulse width (SC HIGH time)	tSAS	8		10		10		ns	
Access time from SE	tSEA		15		15		15	ns	24
SE precharge time	^t SEP	20		20		20		ns	
SE pulse width	^t SE	20		20		20		ns	
Serial data-out hold time after SC high	†SOH	- 5		5		5		ns	24, 28
Serial output buffer turn-off delay from SE	†SEZ	3	12	3	12	3	12	ns	20, 24
Serial data-in setup time	tSDS	0		0		0		ns	
Serial data-in hold time	: tSDH	10		10		10		ns	
Serial input (Write) Enable setup time	tsws	0		0		0	-	ns	
Serial input (Write) Enable hold time	tSWH	15		15		15		ns	
Serial input (Write) disable setup time	tswis	0		0		0		ns	
Serial input (Write) disable hold time	tSWIH	15		15		15		ns	



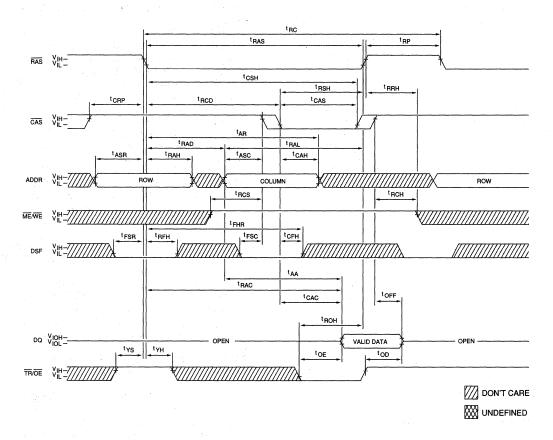
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5$ ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition between 0V and 3V for AC testing.
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{\text{CAS}} = \text{Vih}$, DRAM data output (DQ1-DQ4) is High-Z.
- 12. If $\overline{\text{CAS}} = V_{\text{IL}}$, DRAM data output (DQ1-DQ4) may contain data from the last valid READ cycle.
- 13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: VoH = 2.0V; VoL = 0.8V.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (VOH -200mV, VOL +200mV). This parameter is sampled and not 100 percent tested.
- tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \leq$ tWCS (MIN), the cycle is a LATE-WRITE and TR/OE must control the output buffers during the WRITE to avoid data contention. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate but the WRITE will be valid, if tOD and tOEH are met. See the LATE-WRITE AC Timing diagram.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and ME/WE leading edge in LATE-WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE or CAS, whichever goes HIGH first.
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. ^tOD and ^tOEH must be met in LATE-WRITE and READ-MODIFY-WRITE cycles (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if CAS remains LOW and OE is taken LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. Address (A0-A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
- 27. Address (A0-A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. ^tSOH = ^tSAC output transition time; this is guaranteed by design.
- Values in parenthesis apply to the "L" version.

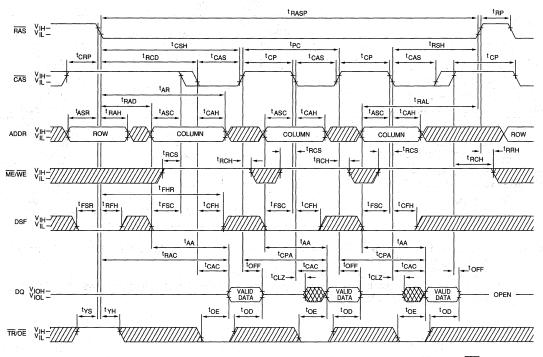


DRAM READ CYCLE





DRAM FAST-PAGE-MODE READ CYCLE



DON'T CARE

₩ UNDEFINED

NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

WRITE CYCLE FUNCTION TABLE 1

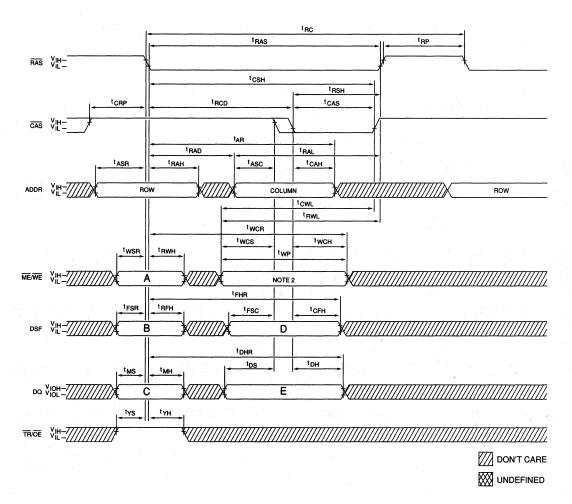
	LOGIC STATES							
		RAS Fall	ling Edge	T	CAS Falling Edge			
FUNCTION	ME/WE	B DSF	C DQ (Input)	D DSF	E ² DQ (Input)			
Normal DRAM WRITE	1	0	Х	0	DRAM Data			
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	. 0	0	Write Mask	0	DRAM Data (Masked)			
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0	DRAM Data (Masked)			
BLOCK WRITE to DRAM (No Data Mask)	1	0	Х	1	Column Mask ³			
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask ³			
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	X	1	Column Mask ³			
Load Mask Register	1.	1	X	0	Write Mask			
Load Color Register	1	1	X	1	Color Data			

NOTE:

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
- 2. CAS or ME/WE, whichever occurs later (Except Block Write).
- WE = "don't care" for Block Write. The DQ column-mask data will be latched at the falling edge of CAS, regardless of the state of ME/WE.



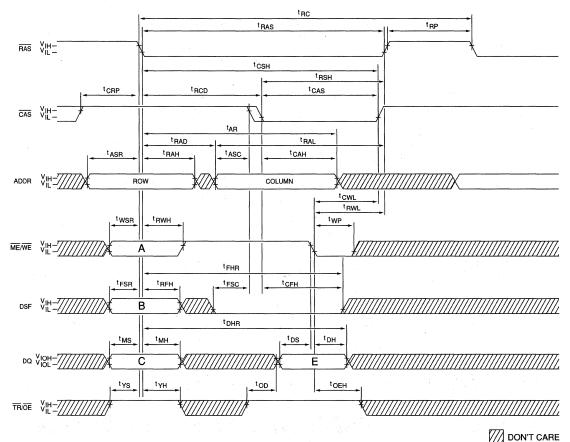
DRAM EARLY-WRITE CYCLE 1



NOTE:

- The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
- 2. For Block Write, ME/WE = "don't care." For all other EARLY-WRITE cycles, ME/WE = LOW.

DRAM LATE-WRITE CYCLE 1



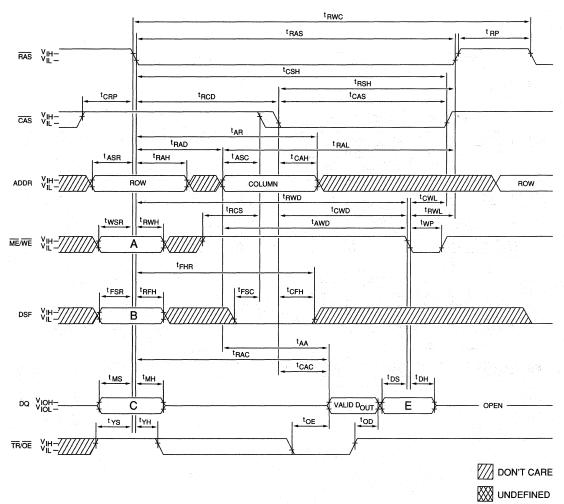
M ----

W UNDEFINED

NOTE: 1. The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

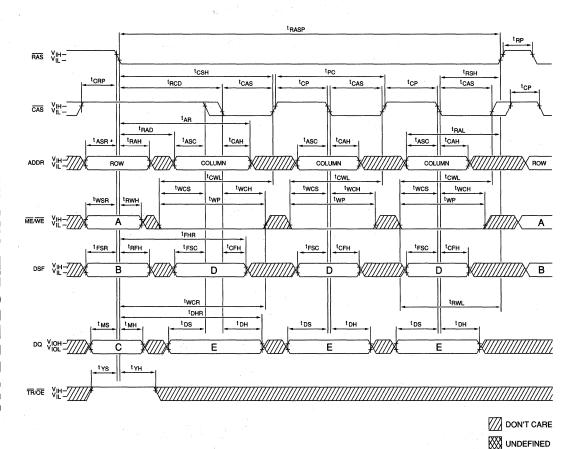


DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

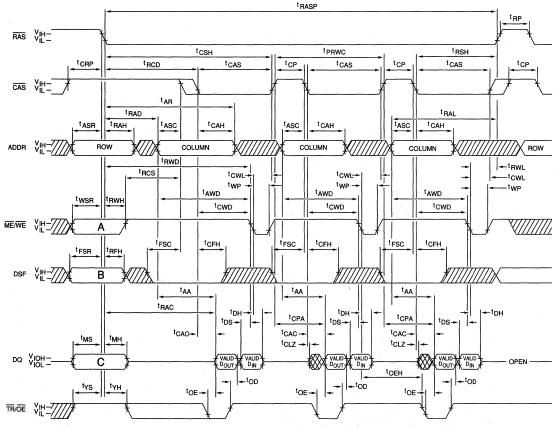
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



NOTE:

- READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
- The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



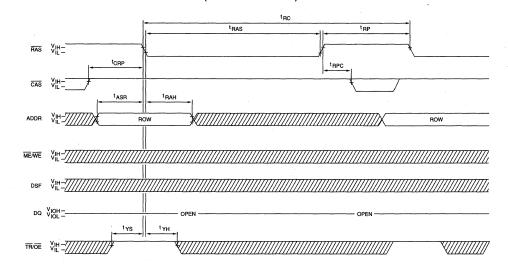
DON'T CARE

W UNDEFINED

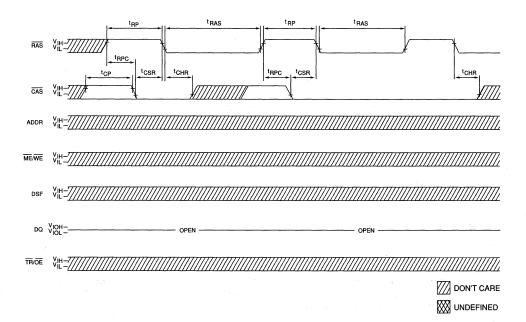
IOTE: 1. READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.

2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)

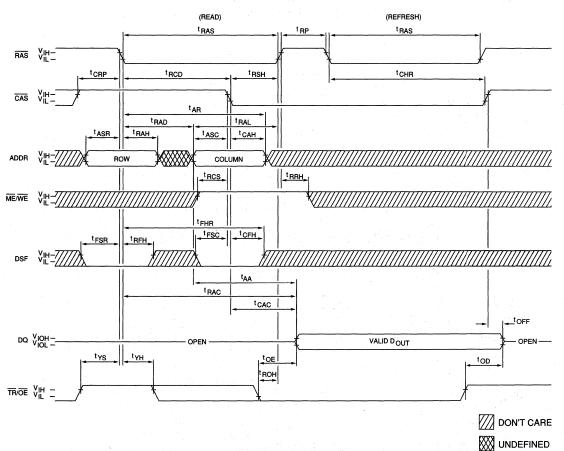


DRAM CAS-BEFORE-RAS REFRESH CYCLE





DRAM HIDDEN-REFRESH CYCLE

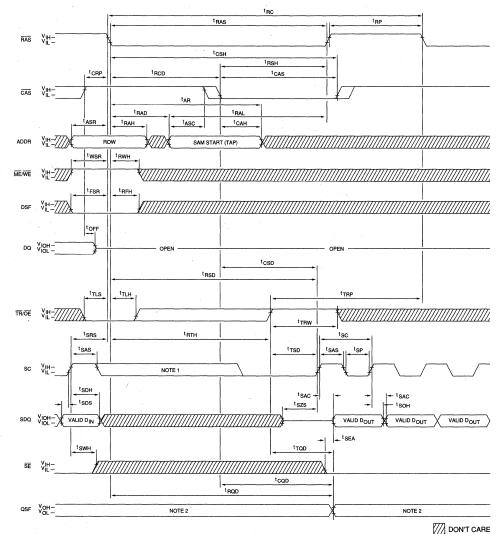


NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH and the DQ pins stay High-Z. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.



READ TRANSFER³ (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode or SC idle)



NOTE:

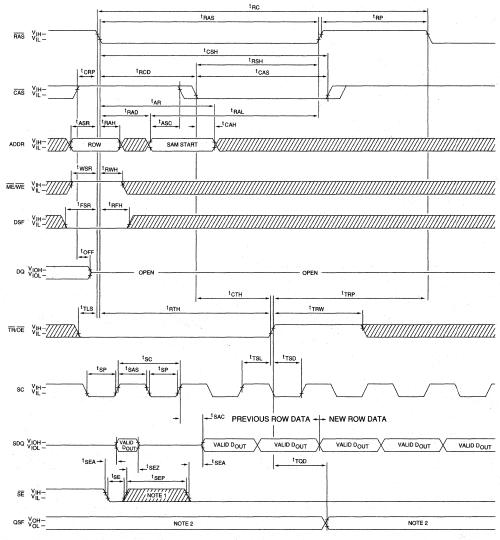
- 1. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
- 3. If ^tTLH is timing for the TR/(OE) rising edge, the transfer is self-timed and the ^tCSD and ^tRSD times must be met. If ^tRTH is timing for the TR/(OE) rising edge, the transfer is done off of the TR/(OE) rising edge and ^tTSD must be met.

₩ UNDEFINED



REAL-TIME READ-TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)

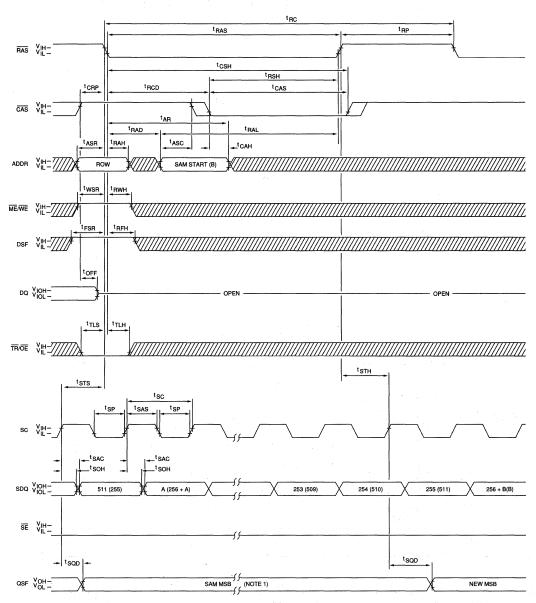


DON'T CARE

NOTE:

- 1. The SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)



NOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed.

QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

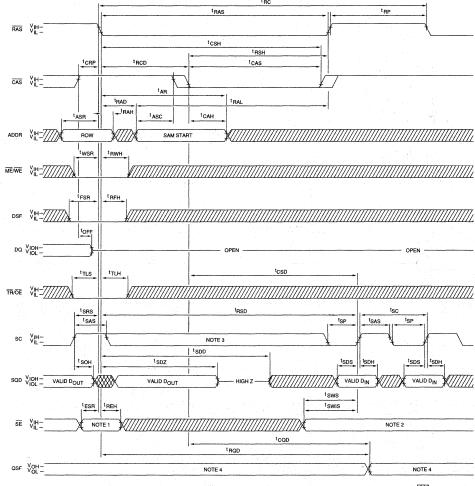
DON'T CARE

W UNDEFINED



WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



DON'T CARE

₩ undefined

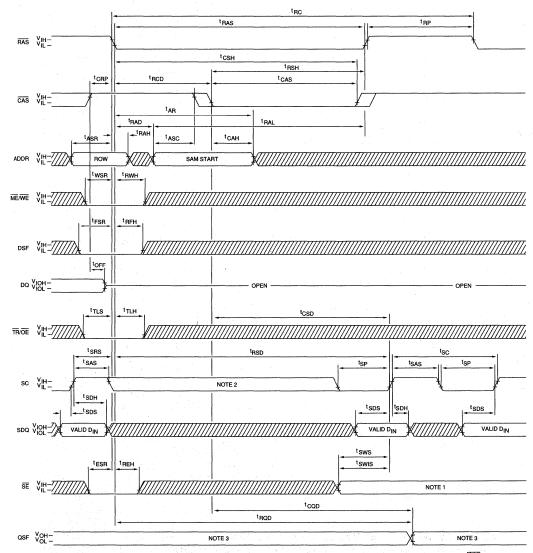
NOTE:

- 1. If SE is LOW, the SAM data will be transferred to the DRAM.
 - If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless
 of SE.
- 3. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.



WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL INPUT mode)



NOTE:

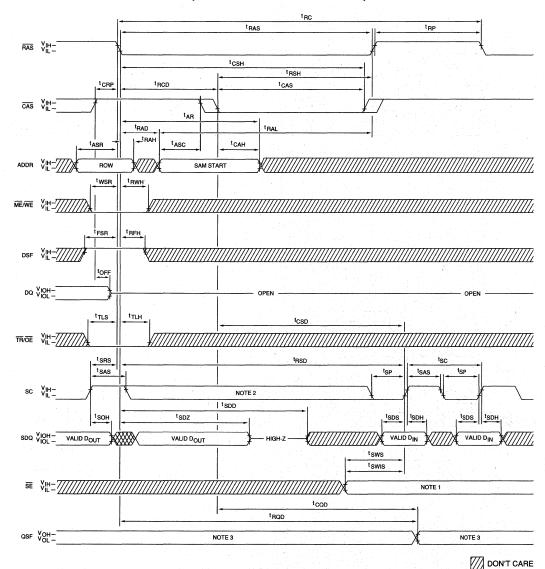
- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 2. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

DON'T CARE

₩ UNDEFINED



ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



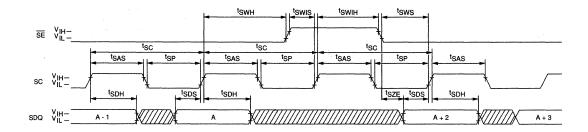
NOTE:

- 1. SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 2. There must be no rising edges on the SC input during this time period.
- 3. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.

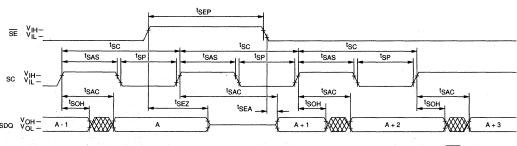
W UNDEFINED



SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

₩ UNDEFINED

MULTIPORT DRAN

VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% (-10), +5V ±5% (-8S) power supply
- · Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port 256 x 8 SAM port
- · No refresh required for serial access memory
- Low power: 15mW standby; 275mW active, typical
- Fast access times 80ns random, 25ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER

OPTIONS

MARKING

- Timing [DRAM, SAM (cycle/access)] 80ns, 25ns/25ns -8S 100ns, 30ns/30ns -10
- Packages Plastic SOJ (400 mil)

DI

GENERAL DESCRIPTION

The MT42C8127 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 1,048,576 bits. These bits may be accessed either by an 8-bit wide DRAM port or by a 256 x 8-bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM). Eight 256-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

PIN ASSIGNMENT (Top View) 40-Pin SOJ (Q-6)

sc	1	40 Vss1
SDQ1	2	39 🛘 SDQ8
SDQ2	d 3	38 🕽 SDQ7
SDQ3	□ 4	37 D SDQ6
SDQ4	[5	36 D SDQ5
TR/OE	4 6	35 SE
DQ1	d 7	34 🕽 DQ8
DQ2	4 8	33 DQ7
DQ3	d 9	32 DQ6
DQ4	[10	31 DQ5
Vcc1	[11	30 🕽 Vss2
ME/WE	[12	29 DSF
NC	[13	28 D NC
RAS	d 14	27 🕽 CAS
NC	[15	26 🕽 QSF
A8	□ 16	25 🗀 AO
A6	L 17	24 🛘 A1
A5	□ 18	23 🛘 A2
A4	□ 19	22 🕽 A3
Vcc2	디 20	21 🕽 A7

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8127 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in rastor graphics display, serial and parallel networking and data communications. Special features, such as SPLIT READ TRANSFER, allow further enhancements to system performance.



VRAM

128K x 8 DRAM WITH 256 x 8 SAM

FEATURES

- · Industry standard pinout, timing and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power: 15mW standby; 275mW active, typical
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- No refresh required for serial access memory
- Optional FAST PAGE MODE access cycles
- Dual port organization: 128K x 8 DRAM port 256 x 8 SAM port
- Fast access times 70ns random, 22ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Function set
- PERSISTENT MASKED WRITE
- SPLIT READ TRANSFER
- WRITE TRANSFER/SERIAL INPUT
- ALTERNATE WRITE TRANSFER
- BLOCK WRITE

OPTIONS

MARKING

L

 Timing [DRAM, SA 	M (cycle/access)]
70ns, 25ns/22ns	(1)
80ns, 30ns/25ns	- 8
100ns, 30ns/27ns	-10

Packages

Plastic SOJ (400 mil) DJ Plastic TSOP (400 mil) TG

32ms low power/extended refresh

GENERAL DESCRIPTION

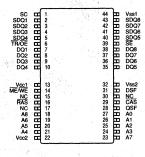
The MT42C8128 is a high-speed, dual port CMOS dynamic random access memory or video RAM (VRAM) ontaining 1,048,576 bits. These bits may be accessed either y an 8-bit wide DRAM port or by a 256 x 8-bit serial access nemory (SAM) port. Data may be transferred bidirectionly between the DRAM and the SAM. An extended refresh 32ms), low power option is available as the MT42C8128 L. The DRAM portion of the VRAM is functionally identical

PIN ASSIGNMENT (Top View)

40-Pin SOJ (Q-6)



40/44-Pin TSOP* (R-5)



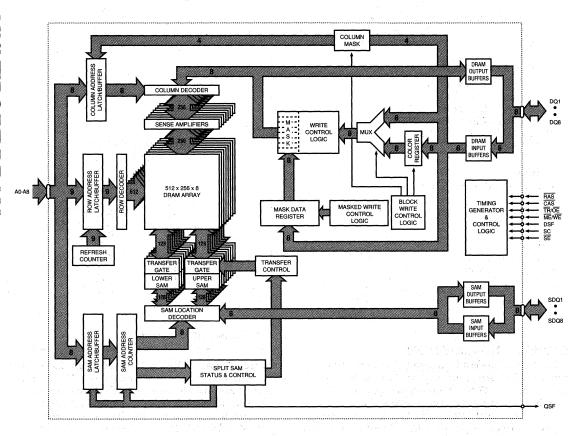
*Consult factory on TSOP availability.

to the MT4C4256 (256K x 4 DRAM). Eight 256-bit data registers make up the SAM portion of the VRAM. Data I/O and internal data transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 256 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 8ms, or 32ms for the MT42C8128 L, (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and requires no refresh.

The operation and control of the MT42C8128 is optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE, allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
* .1	1	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
6	6	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at \overline{RAS} (H \rightarrow L), or
				Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a High-Z state.
12	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or
				Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
35	39	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. SE is also used during a WRITE TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE cycle is performed.
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE vs. PERSISTENT MASKED WRITE, etc.) are used for a particular access cycle.
14	16	RAS	Input	Row Address Strobe: RAS is used to clock in the 9 row-address bits and strobe the ME/WE, TR/OE, DSF, SE, CAS and DQ inputs. It acts as master chip enable, and must fall to initiate any DRAM or TRANSFER cycle
27	29	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe the DSF input.
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and A0-A7 indicate the SAM start address (when CAS goes LOW). A7, A8 = "don't care" for the start address when during SPLIT TRANSFER.



PIN DESCRIPTIONS (continued)

SOJ PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7, 8, 9, 10, 31, 32, 33, 34	7, 8, 9, 10, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM cycles; inputs for Mask Data Register and Color Register load cycles, and DQ and Column Mask inputs for BLOCK WRITE.
2,3,4,5,36, 37,38,39	2, 3, 4, 5, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-127, HIGH if address is 128-255.
15, 28	17, 30	NC	-	No Connect: This pin should be either left unconnected or tied to ground.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±10%
30, 40	32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8128 may be divided into three functional blocks: the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note:

For dual-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8128 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8128 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM portion of the MT42C8128 is fully static and does not require any refreshing.

DRAM READ AND WRITE CYCLES

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on his part, several conditions that were undefined or in 'don't care" states for the DRAM are specified for the /RAM. These conditions are highlighted in the following liscussion. In addition, the VRAM has several special funcions that can be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when \overline{RAS} transitions from HIGH-to-LOW. Next, the 8 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note:

RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH; all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS

For single port DRAMS, the OE pin is a "don't care" when RAS goes LOW. For the VRAM, when RAS goes LOW, TR/ (OE) selects between DRAM access or TRANSFER cycles. TR/(OE) must be HIGH at the RAS HIGH-to-LOW transition for all DRAM operations (except \overline{CAS} -BEFORE- \overline{RAS}).

If $(\overline{ME})/\overline{WE}$ is HIGH when \overline{CAS} goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. To enable the DRAM output port, the $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after RAS falls.

For single port normal DRAMs, WE is a "don't care" when \overline{RAS} goes LOW. For the VRAM, $\overline{ME}/(\overline{WE})$ is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{\text{ME}}/(\overline{\text{WE}})$ is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any DRAM access cycle (READ or WRITE), $\overline{\text{ME}}/(\overline{\text{WE}})$ must be HIGH at the $\overline{\text{RAS}}$ HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed. Refer to the AC timing diagrams.

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.



NONPERSISTENT MASKED WRITE

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing only specific bits within an 8-bit word. The MT42C8128 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{ME}/(\overline{WE})$ and DSF are LOW at the \overline{RAS} HIGH-to-LOW transition, a NONPERSISTENT MASKED WRITE is performed and the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that CAS is still HIGH. When CAS goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The MASKED WRITE is nonpersistent (must be re-entered at every RAS cycle) if DSF is LOW when RAS goes LOW. The mask data register is cleared at the end of every NONPER-SISTENT MASKED WRITE. FAST PAGE MODE can be used with NONPERSISTENT MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE RAS cycle. An example NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

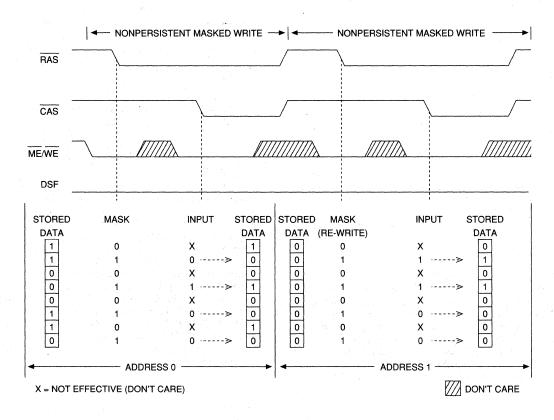


Figure 1 NONPERSISTENT MASKED WRITE EXAMPLE

MULTIPORT DRAM

PERSISTENT MASKED WRITE

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF HIGH when $\overline{\text{RAS}}$ goes LOW. The mask data is loaded into the internal register when $\overline{\text{CAS}}$ goes LOW.

PERSISTENT MASKED WRITE cycles may then be performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF HIGH when $\overline{\text{RAS}}$ goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present on the DQ inputs is not loaded into the mask

register when RAS falls, and the mask data register will not be cleared at the end of the cycle. Any number of PERSISTENT MASKED WRITE cycles, to any address, may be performed without having to reload the mask data register. Figure 2 shows the LOAD MASK REGISTER and two PERSISTENT MASKED WRITE cycles in operation. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow controllers that cannot provide mask data to the DQ pins at RAS time to perform MASKED WRITE operations. PERSISTENT MASKED WRITE operations can be performed during FAST PAGE MODE cycles and the same mask will apply to all addressed columns in the addressed row.

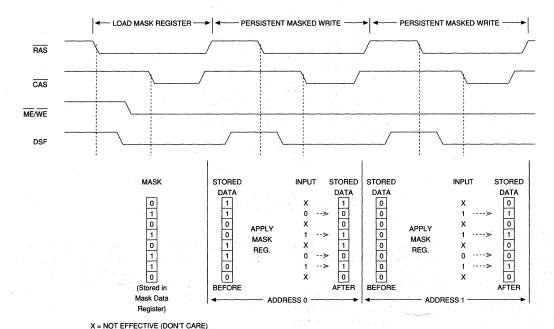


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

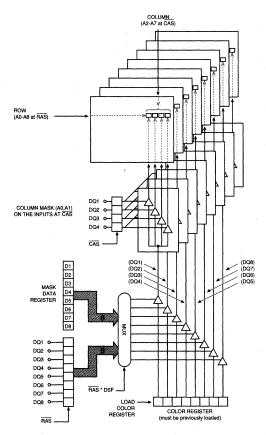


Figure 3
BLOCK WRITE EXAMPLE

BLOCK WRITE

If DSF is HIGH when $\overline{\text{CAS}}$ goes LOW, the MT42C8128 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However when CAS goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The table on this

page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

	COLUMN ADDRESS CONTROLLE					
INPUTS	A0	A1				
DQ1	0	0				
DQ2	1	0				
DQ3	0	1				
DQ4	1 1	1				

MULTIPORT DRAM

NONPERSISTENT MASKED BLOCK WRITE

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF LOW when $\overline{\text{RAS}}$ goes LOW initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{\text{CAS}}$ goes LOW, to perform a NONPERSISTENT MASKED BLOCK WRITE. Using the column mask input and MASKED WRITE function allows any combination of the eight bit planes or four column locations to be masked.

PERSISTENT MASKED BLOCK WRITE

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF is HIGH when $\overline{\text{CAS}}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

LOAD MASK DATA REGISTER

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF is HIGH when \overline{RAS} goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF being HIGH when \overline{RAS} goes LOW indicates the cycle is a LOAD REGIS-

TER cycle. DSF is used when \overline{CAS} goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note: For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The mask data register contents will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSIS-TENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER

The LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when CAS goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW then \overline{RAS} goes LOW. The state of $(\overline{ME})/\overline{WE}$ when \overline{RAS} goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER, SPLIT READ TRANSFER, and ALTERNATE WRITE TRANSFER cycles. Each of the TRANSFER cycles available is described below.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

If (ME)/WE is HIGH and DSF is LOW when RAS goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate the eight 256-bit DRAM row planes that are to be transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. CAS must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accom-

plished two ways. If the transfer is to be synchronized with SC (REAL-TIME READ TRANSFER), TR/(OE) is taken HIGH after CAS goes LOW. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before CAS goes LOW (refer to the AC Timing Diagrams). The 2,048 bits of DRAM data are written into the SAM data registers and the serial shift start address is stored in an internal 8-bit register. QSF will be LOW if access is from the lower half (addresses 0 through 127), and HIGH if access is from the upper half (128 through 255). If \overline{SE} is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. \overline{SE} enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of SE. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

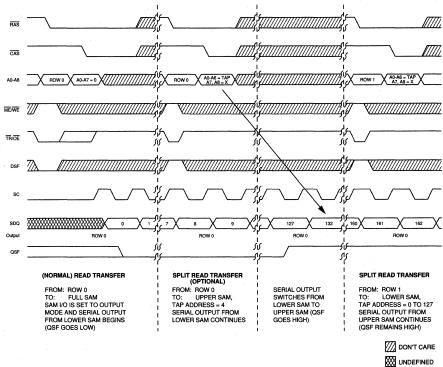


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

MULTIPORT DRAM

SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles, the REAL-TIME READ TRANSFER cycle has to occur immediately after the last bit of "old data" was clocked out of the SAM port.

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the rising edges of \overline{RAS} or \overline{CAS} . The transfer timing is generated internally for SPLIT TRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM port.

A normal, non-split READ TRANSFER cycle must precede any sequence of SPLIT READ TRANSFER cycles to provide a reference to which half of the SAM the access will begin, and to set SAM I/O direction. Then SPLIT READ TRANSFERS may be initiated by taking DSF HIGH when RAS goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A6, is used to input the SAM Tap address. Address pin A7 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of CAS. It is internally generated so that the SPLIT TRANSFER will be to the SAM half not currently being accessed.

Figure 4 shows a typical SPLIT READ TRANSFER initiation sequence. The normal READ TRANSFER is first performed, followed by a SPLIT READ TRANSFER of the same row to the upper half of the SAM. The SRT to the upper half is optional, it is only needed if the Tap for the upper half is \neq 0. Serial access continues, and when the SAM address counter reaches 127 ("A7" = 0, A0-A6 = 1) the new Tap address is loaded for the next half ("A7" = 1, A0-A6 = Tap) and the QSF output goes HIGH. Once the serial access has switched to the upper SAM, new data may be transferred to the lower SAM. The controller must wait for the state of QSF to change and then the new data may be transferred to the SAM half not being accessed. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and then transfer the upper half of row 1 to the upper SAM. If the half boundary is reached, before an SRT is done for the half, a Tap address of "0" will be used. Access will start at 0 if going to the lower half, and 128 if going to the upper half. See Figure 5.

WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the WRITE TRANSFER is identical to that of the READ TRANSFER described previously except (ME)/WE and SE must be LOW when RAS goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A WRITE TRANSFER changes the direction of the SAM I/O buffers to the input mode. QSF is LOW if access is to the lower half of the SAM, and HIGH if to access the upper half.

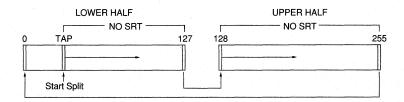


Figure 5
SPLIT SAM TRANSFER

PSEUDO WRITE TRANSFER (SERIAL-INPUT-MODE ENABLE)

The PSEUDO WRITE TRANSFER cycle is used to change the direction of the SAM port from output to input without performing a WRITE TRANSFER cycle. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with SE held HIGH instead of LOW. The DRAM data will not be disturbed and the SAM will be ready to accept input data.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

The operation of the ALTERNATE WRITE TRANSFER is identical to the WRITE TRANSFER except that the DSF pin is HIGH and $(\overline{\text{ME}})/\overline{\text{WE}}$ is LOW when $\overline{\text{RAS}}$ goes LOW, allowing $\overline{\text{SE}}$ to be a "don't care." This allows the outputs to be disabled using $\overline{\text{SE}}$ during a WRITE TRANSFER cycle. ALTERNATE WRITE TRANSFER will change the SAM I/O direction to an input condition.

SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUT-PUT are SC and $\overline{\text{SE}}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{\text{SE}}$ enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{\text{SE}}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{\text{SE}}$ is HIGH or LOW. The address progresses through the SAM

and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 255) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 8-bit word written. \overline{SE} acts as a write enable for serial input data and must be LOW for valid serial input. If \overline{SE} = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the \overline{SE} input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight \overline{RAS} cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = (\overline{TR})/\overline{OE} \ge V_{IH}$ during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8128 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of SE. The mask and color register will contain random data after power-up. QSF initializes in the LOW state.



TRUTH TABLE

		RAS FALLING EDGE			CAS FALL AO-A81			DQ1-DQ8 ²		REGISTERS			
CODE	FUNCTION	CAS	TR/OE	ME/WE	DSF	SE	DSF	RAS	CAS, A8=X	RAS	CAS,WE3	MASK	COLOR
	DRAM OPERATIONS												7
CBR	CAS-BEFORE-RAS REFRESH	0	×	х	х	х	X	_	X	_	X.	X	X
ROR	RAS-ONLY REFRESH	1	1	Х	Х	X	_	ROW	_	Х		X	Χ.
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	Х	0	ROW	COLUMN	Х	VALID	Х	Х
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	х	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	X
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	х	0	ROW	COLUMN	×	VALID DATA	USE	х
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	Х	1	ROW	COLUMN (A2-A7)	x	COLUMN MASK	X	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	х	1	ROW	COLUMN	WRITE MASK	COLUMN MASK	LOAD & USE	USE
вwом	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	. 1	1	0	1	X	1	ROW	COLUMN (A2-A7)	×	COLUMN	USE	USE
	REGISTER OPERATIONS				1								
LMR	LOAD MASK REGISTER	1	1	1	1	х	0	ROW ⁴	х	×	WRITE MASK	LOAD	X
LCR	LOAD COLOR REGISTER	1	1	1	1	Х	1	ROW ⁴	х	х	COLOR DATA	х	LOAD
	TRANSFER OPERATIONS												12
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	х	X	ROW	TAP ⁵	X	X	Х	Х
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	х	Х	ROW	TAP ⁵	х	X	Х	Х
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	Х	ROW	TAP ⁵	Х	Х	х	×
PWT	PSEUDO WRITE TRANSFER (SERIAL-INPUT- MODE ENABLE)	1	. 0	0	0	1	х	ROW ⁴	TAP ⁵	х	х	х	х
AWT	ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1.	0	0	1	X	x	ROW	TAP ⁵	x	×	×	X

NOTE:

- 1. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
- 2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
- On WRITE cycles (except BLOCK WRITE), the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is activated at the falling edge of CAS or TR/OE, whichever is later.
- 4. The ROW that is addressed will be refreshed, but no particular ROW address is required.
- 5. This is the SAM location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (127 for lower half, 255 for upper half).



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	Vін	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

DC ELECTRICAL CHARACTERISTICS

Cappiy Vollage	1 .00	10	0.0	1	ì
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1
O EL EGEDIO AL OLLA DA GEORGIOTICO					
°C ≤ T _A ≤ 70°C; Vcc = 5V ±10%)	SYMBOL	MIN	MAX	UNITS	NOTE
	SYMBOL	MIN -10	MAX 10	UNITS μΑ	NOTE
$^{\circ}$ C \leq T _A \leq 70 $^{\circ}$ C; Vcc = 5V \pm 10%) PARAMETER/CONDITION			+	 	NOTE
$^{\circ}$ C \leq T _A \leq 70 $^{\circ}$ C; Vcc = 5V \pm 10%) PARAMETER/CONDITION INPUT LEAKAGE CURRENT			+	 	NOTE
PARAMETER/CONDITION INPUT LEAKAGE CURRENT Any input (0V \leq Vin \leq Vcc); all other pins not under test = 0V	IL I	-10	10	μА	NOTE
PARAMETER/CONDITION INPUT LEAKAGE CURRENT Any input (0V \leq Vin \leq Vcc); all other pins not under test = 0V OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V \leq Vout \leq Vcc)	IL I	-10	10	μА	NOTE
INPUT LEAKAGE CURRENT Any input (0V \leq V _{IN} \leq V _{CC}); all other pins not under test = 0V OUTPUT LEAKAGE CURRENT	loz	-10	10	μΑ	NOTE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _{l1}		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SC, SE, DSF	 Cl2		7	pF	2
Input/Output Capacitance: DQ, SDQ	Cı/o		9	pF	2
Output Capacitance: QSF	Co		9	pF	2



CURRENT DRAIN, SAM IN STANDBY

0° C \leq T _A \leq 70°C; Vcc = 5V \pm 10%)	The State of the S	19.00	MAX			
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	lcc1	95	85	75	mA	3, 4 26
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: [†] PC = [†] PC (MIN))	Icc2	85	75	65	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Viн after 8 RAS cycles (MIN); other inputs ≥ Viн or ≤ ViL)	Іссз	8	8	8	mA	4
STANDBY CURRENT: CMOS INPUT LEVELS (MT42C8128 L only) $(\overline{RAS} = \overline{CAS} \ge Vcc -0.2V, other inputs \ge Vcc -0.2V or \le 0.2V)$	ICC4	500	500	500	μА	4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vih)	Icc5	95	85	75	mA	3, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	Icc6	95	85	75	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) MT42C8128 L only Average power supply current during BATTERY BACKUP refresh: $\overline{CAS} \leq 0.2V$ or \overline{CAS} -BEFORE- \overline{RAS} cycling; $\overline{RAS} = {}^{t}RAS$ (MIN) to 300ns; $\overline{ME/WE}$, A0-A8 and DQs $\geq Vcc$ - 0.2V or \leq 0.2V (DQs may be left open), ${}^{t}RC = 62.5\mu s$ (512 rows at 62.5 $\mu s = 32ms$)	lcc7	600	600	600	μА	3, 5
SAM/DRAM DATA TRANSFER	Icc8	105	95	90	mA	3

CURRENT DRAIN, SAM ACTIVE (*SC = MIN)

0° C \leq T _A \leq 70°C; Vcc = 5V \pm 10%)		MAX			1		
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES	
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	Icc9	150	130	120	mA	3, 4, 26	
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: PC = PC (MIN))	Icc10	140	120	110	mA	3, 4, 27	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles (MIN); other inputs ≥ VIH or ≤ VIL)	lcc11	55	45	45	mĄ	3, 4	
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = ViH)	lcc12	150	130	120	mA	3, 4, 26	
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	lcc13	150	130	120	mA	3, 4, 5	
SAM/DRAM DATA TRANSFER	Icc14	160	130	125	mA	3, 4	

DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS PARAMETER			-7	-8		-	-10		
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	†RC	130		150		180		ns	
READ-MODIFY-WRITE cycle time	†RWC	175		190		230		ns	
FAST-PAGE-MODE READ or WRITE	^t PC	45		50		55		ns	
cycle time			1 1						
FAST-PAGE-MODE READ-MODIFY-WRITE	†PRWC	90		95		110		ns	
cycle time									
Access time from RAS	†RAC	,	70		80		100	ns	14
Access time from CAS	†CAC		20		25		25	ns	15
Access time from (TR)/OE	^t OE		20		20		25	ns	
Access time from column address	tAA .		35		40		45	ns	
Access time from CAS precharge	[†] CPA		40		45		50	ns	i
RAS pulse width	†RAS	70	20,000	80	20,000	100	20,000	ns	
RAS pulse width (FAST PAGE MODE)	^t RASP	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		20		25		ns	
RAS precharge time	tRP	50		60		70		ns	
CAS pulse width	†CAS	20	10,000	20	10,000	25	10,000	ns	
CAS hold time	¹CSH	70		80		100		ns	
CAS precharge time	^t CP	10		10		10		ns	
RAS to CAS delay time	†RCD	20	50	20	55	20	75	ns	17
CAS to RAS precharge time	CRP	10		10		10		ns	
Row address setup time	†ASR	0		0		0		ns	
Row address hold time	^t RAH	10		10		15		ns	
RAS to column	tRAD	20	45	15	40	20	50	ns	18
address delay time							1		
Column address setup time	†ASC	0		0		0		ns	
Column address hold time	†CAH	15		15		15		ns	
Column address hold time	tAR.	45		55		70	T	ns	
(referenced to RAS)									
Column address to	†RAL	35		40		50		ns	
RAS lead time									
Read command setup time	tRCS	0		0		0		ns	1
Read command hold time	tRCH	0		0		0		ns	19
(referenced to CAS)									
Read command hold time	^t RRH	0		0		0		ns	19
(referenced to RAS)								Marie 1	
CAS to output in Low-Z	^t CLZ	3		3		3		ns	
Output buffer turn-off delay	†OFF	3	20	3	20	3	20	ns	20, 23
Output disable	dO [†]	3	10	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	tOEH	10		10		20	17.	ns	27
OE LOW to RAS HIGH delay time	^t ROH	0	1	0		0	1	ns	1



DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 10 %)

AC CHARACTERISTICS PARAMETER		-7			-8	-10			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	¹wcs	0		0		0		ns	21
Write command hold time	^t WCH	15		15		15		ns	
Write command hold time (referenced to RAS)	¹WCR	45		55	Sarra.	70		ns	
Write command pulse width	tWP	15		15		15		ns	100
Write command to RAS lead time	tRWL	20		20		20		ns	
Write command to CAS lead time	tCWL	20		20		20		ns	
Data-in setup time	t _{DS}	0		0		0		ns	22
Data-in hold time	tDH t	15		15		15		ns	22
Data-in hold time (referenced to RAS)	^t DHR	45		55		65		ns	
RAS to WE delay time	†RWD	90		100		130		ns	21
Column address to WE delay time	^t AWD	55		65		75		ns	21
CAS to WE delay time	tCWD	40		45		55		ns	21
Transition time (rise or fall)	'	3	35	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF		8(32)		8(32)	n especial	8(32)	ms	29
RAS to CAS precharge time	tRPC	0	F1 ()	0		0	Pari in	ns	1.00
CAS setup time (CAS-BEFORE-RAS REFRESH)	[†] CSR	10		10	7	10		ns	5
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	10		10		10	Year o	ns	5
ME/WE to RAS setup time	twsR	0		0		0		ns	
ME/WE to RAS hold time	tRWH	15		15		15	1000	ns	
Mask Data to RAS setup time	tMS	0	177	0		0		ns	1500
Mask Data to RAS hold time	t _{MH}	15		15		15	100000	ns	100



TRANSFER AND MODE CONTROL TIMING PARAMETERS ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
TR/(OE) LOW to RAS setup time	^t TLS	0		0		0		ns	
TR/(OE) LOW to RAS hold time	^t TLH	15	10,000	15	10,000	15	10,000	ns	
TR/(OE) LOW to RAS hold time (REAL-TIME READ-TRANSFER only)	^t RTH	65	10,000	70	10,000	80	10,000	ns	
TR/(OE) LOW to CAS hold time (REAL-TIME READ-TRANSFER only)	^t CTH	25		25		25		ns	
TR/(OE) HIGH to SC lead time	^t TSL	5		5		5		ns	
TR/(OE) HIGH to RAS precharge time	tTRP	50		60		70		ns	
TR/(OE) to precharge time	tTRW	20	145	20		30		ns	
First SC edge to TR/(OE) HIGH delay time	TSD	. 15	-	15		15		ns	
Serial output buffer turn-off delay from RAS	tSDZ	7	40	7	40	7	40	ns	
SC to RAS setup time	tSRS	25		30		30		ns	
Serial data input to SE delay time	tSZE	0		0		0		ns	
Serial data input delay from RAS	tSDD	50		50		50		ns	
Serial data input to RAS delay time	tSZS	0		0		. 0		ns	
Serial-input-mode enable (SE) to RAS setup time	tESR	0		0	-	0		ns	
Serial-input-mode enable (SE) to RAS hold time	^t REH	15		15		15		ns	
TR/(OE) HIGH to RAS setup time	tys	0		0		0	13	ns	
TR/(OE) HIGH to RAS hold time	tYH	15	7.1	15		15		ns	
DSF to RAS setup time	†FSR	0		0		0		ns	
DSF to RAS hold time	tRFH .	.15		15		15		ns	1
SC to QSF delay time	tSQD		30		30		30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		30	1	ns	
SPLIT TRANSFER hold time	^t STH	0		0		0		ns	
RAS to QSF delay time	†RQD		75		75		75	ns	
DSF to RAS hold time	^t FHR	45		60		65	1	ns	1
DSF to CAS setup time	†FSC	. 0		0		0		ns	
DSF to CAS hold time	^t CFH	15		15		20		ns	
TR/OE to QSF delay time	tTQD		25		25		25	ns	
CAS to QSF delay time	^t CQD		35		35		35	ns	
RAS to first SC delay	tRSD	80		80		80		ns	
CAS to first SC delay	tCSD	30		30		30		ns	



SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			7	-	8	-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	tSC	25		30		30		ns	
Access time from SC	†SAC		22		25		27	ns	24
SC precharge time (SC LOW time)	tSP	8	1,513	10		10		ns	
SC pulse width (SC HIGH time)	tSAS	8		10		10		ns	
Access time from SE	tSEA		15	11.11	15		15	ns	24
SE precharge time	^t SEP	20		20		20		ns	
SE pulse width	tSE.	20		20		20		ns	
Serial data-out hold time after SC high	tSOH	5		5		5	4.5	ns	24
Serial output buffer turn-off delay from SE	^t SEZ	3	12	3	12	3	12	ns	20, 24
Serial data-in setup time	tSDS	0		0		0		ns	1
Serial data-in hold time	tSDH	10		10		10	100	ns	
Serial input (Write) Enable setup time	tsws	0		0		0	The second	ns	
Serial input (Write) Enable hold time	tSWH	15		15		15		ns	
Serial input (Write) disable setup time	tswis	0		0		0		ns	
Serial input (Write) disable hold time	tSWIH	15		15		15		ns	

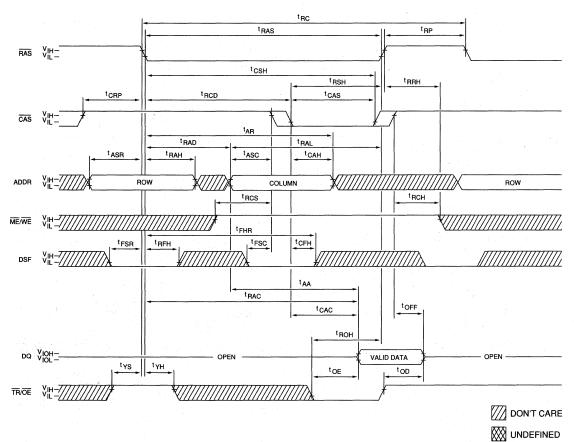
NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on I/O loading. Specified values are obtained with minimum cycle time and the I/Os open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition between 0V and 3V for AC testing.
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{CAS} = V_{IH}$, DRAM data output (DQ1-DQ8) is High-Z.
- If CAS = VIL, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
- DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: VOH = 2.0V; VOL = 0.8V.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCPN.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OD, OFF and SEZ define the time when the output achieves open circuit (VoH -200mV, Vol. +200mV). This parameter is sampled and not 100% tested.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \le$ tWCS (MIN), the cycle is a LATE-WRITE and TR/OE must control the output buffers during the write to avoid data contention. If ${}^{t}RWD \ge {}^{t}RWD$ (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate but the WRITE will be valid, if tOD and tOEH are met. See the LATE-WRITE AC Timing diagram.
- 22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and ME/WE leading edge in LATE-WRITE or READ-WRITE cycles.
- During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE or CAS, whichever goes HIGH first.
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if CAS remains LOW and OE is taken LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 26. Address (A0-A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
- 27. Address (A0-A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 28. 'SAC is MAX at 70° C and 4.5V Vcc; 'SOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature 'SOH = 'SAC output transition time, this is guaranteed by design.
- 29. Values in parenthesis apply to the "L" version.

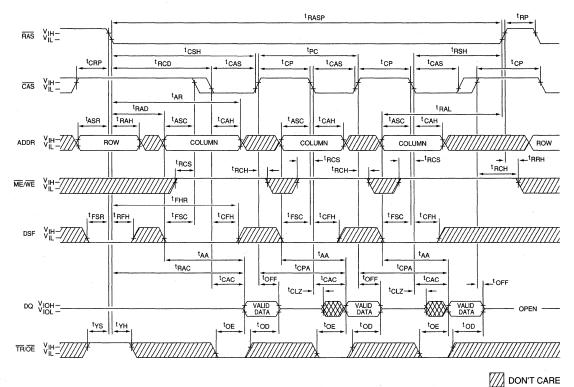


DRAM READ CYCLE



UNDEFINED

DRAM FAST-PAGE-MODE READ CYCLE



NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.



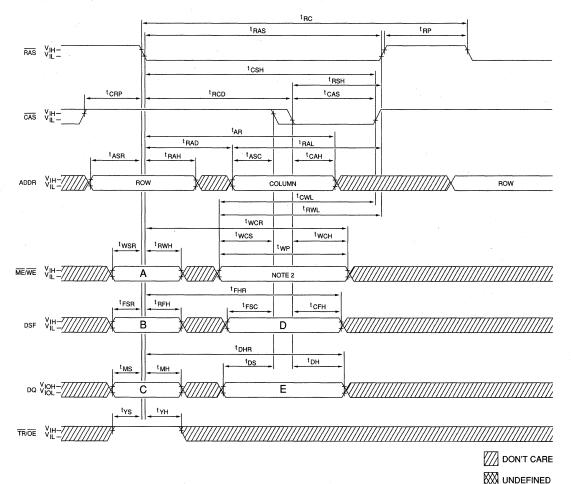
WRITE CYCLE FUNCTION TABLE 1

	LOGIC STATES							
		RAS Fall	ing Edge		CAS Falling Edge			
FUNCTION		B DSF	C DQ (Input)	D DSF	E ² DQ (Input)			
Normal DRAM WRITE (or READ)	1	0	X	0	DRAM Data			
NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)			
PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	Х	0	DRAM Data (Masked)			
BLOCK WRITE to DRAM (No Data Mask)	1	0	х	1	Column Mask ³			
NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask ³			
PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	Х	1	Column Mask ³			
Load Mask Register	1	1	х	0	Write Mask			
Load Color Register	1	1	X	1	Color Data			

NOTE:

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
- 2. CAS or ME/WE, whichever occurs later (except for BLOCK WRITE).
- 3. WE = "don't care" for BLOCK WRITE. The DQ column-mask data will be latched at the falling edge of CAS, regardless of the state of ME/WE.

DRAM EARLY-WRITE CYCLE 1

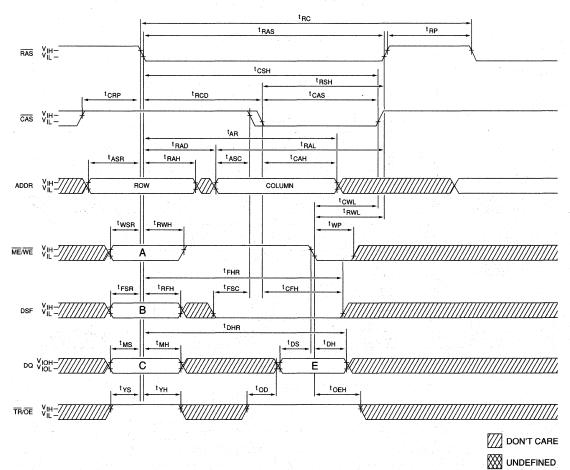


NOTE:

- 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.
- 2. For BLOCK WRITE, ME/WE = "don't care." For all other EARLY-WRITE cycles, ME/WE = LOW.

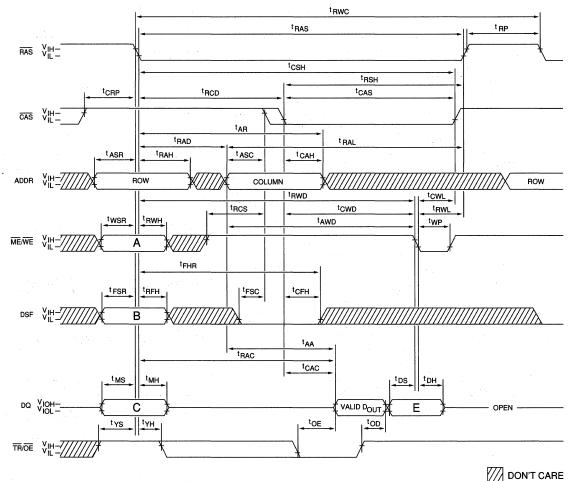


DRAM LATE-WRITE CYCLE



NOTE: The logic states of "A", "B", "C" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)

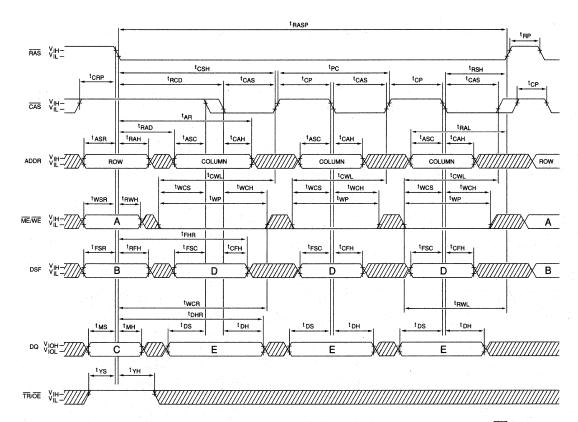


NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

W UNDEFINED



DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

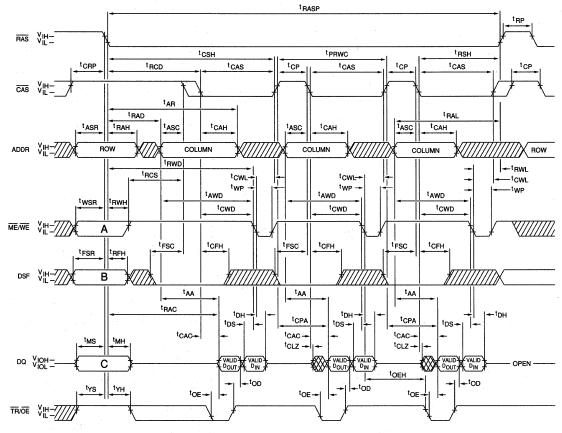
W UNDEFINED

NOTE:

- 1. READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
- 2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

MULTIPORT DRAM

DRAM FAST-PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



DON'T CARE

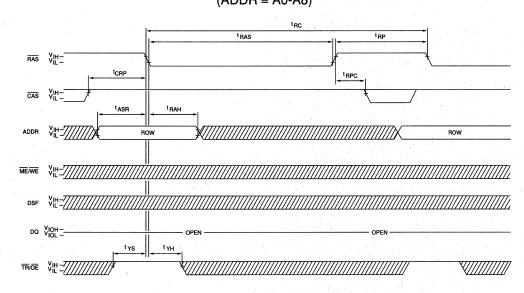
₩ undefined

NOTE:

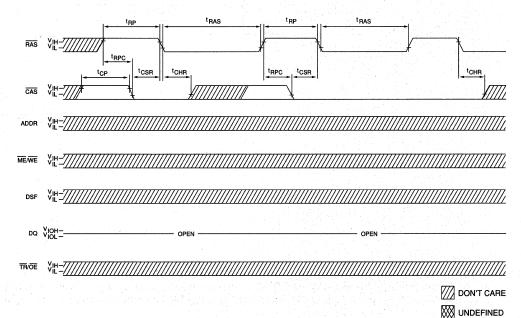
- READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use
 the Write Function Table to determine the proper DSF state for the desired WRITE operation.
- 2. The logic states of "A", "B" and "C" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.



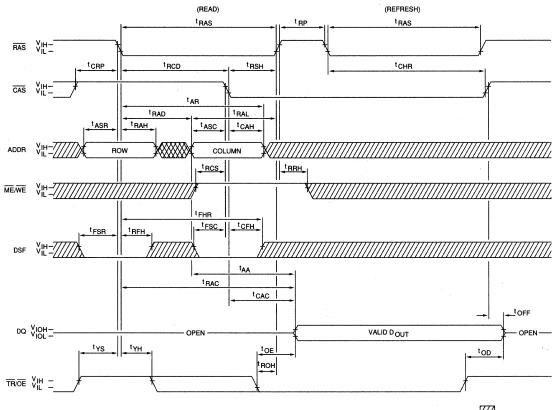
DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)



CAS-BEFORE-RAS REFRESH CYCLE



DRAM HIDDEN-REFRESH CYCLE



DON'T CARE

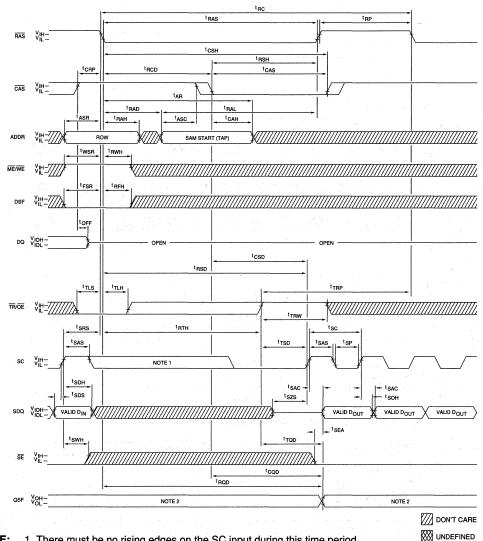
₩ undefined

NOTE: A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH and the DQ pins stay High-Z. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.



READ TRANSFER 3 (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode or SC idle)

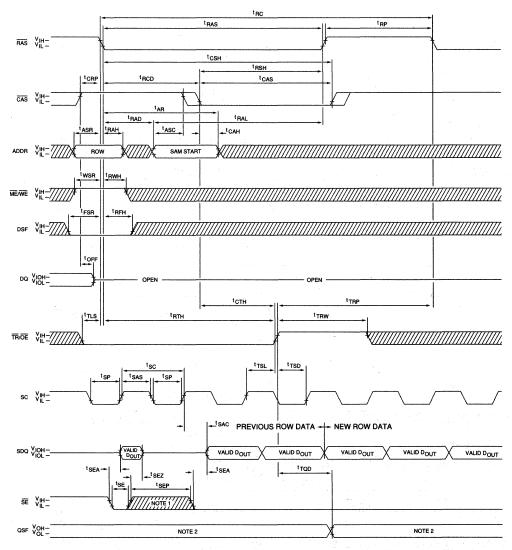


NOTE:

- 1. There must be no rising edges on the SC input during this time period.
- 2. QSF = 0 when the Lower SAM (bits 0-127) is being accessed. QSF = 1 when the Upper SAM (bits 128-255) is being accessed.
- 3. If TLH is timing for the TR/(OE) rising edge, the transfer is self-timed and the CSD and RSD times must be met. If ¹RTH is timing for the TR/(OE) rising edge, the transfer is done off of the TR/(OE) rising edge and ^tTSD must be met.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:

1. The SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

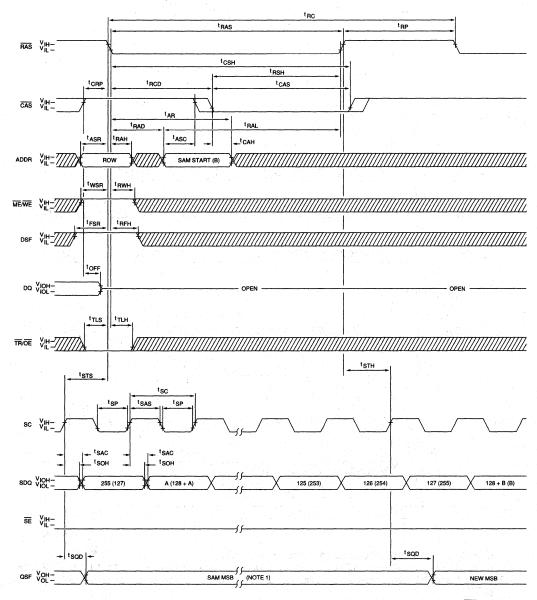
QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

DON'T CARE





SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)



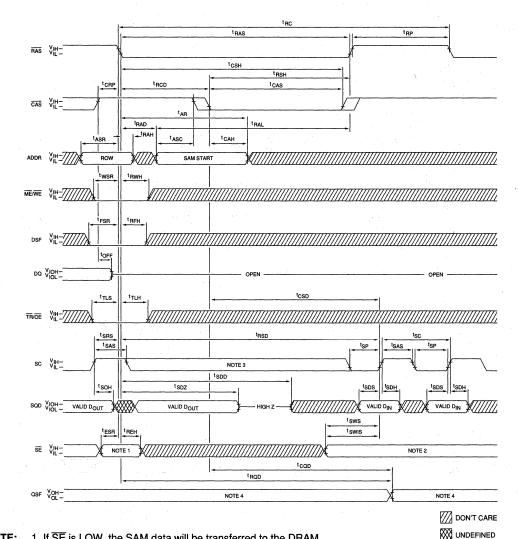
QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

DON'T CARE

₩ UNDEFINED

WRITE TRANSFER and PSEUDO WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



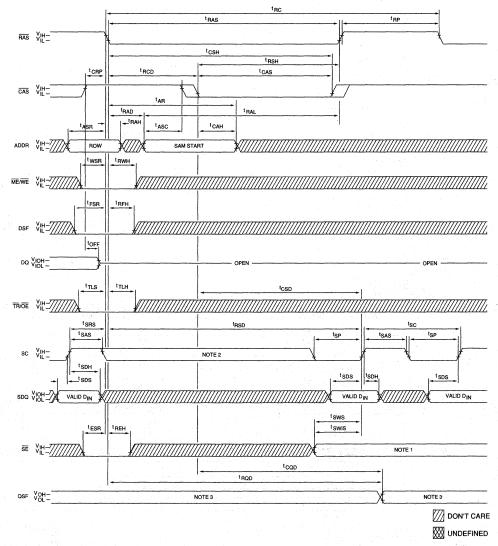
NOTE:

- 1. If SE is LOW, the SAM data will be transferred to the DRAM.
 - If SE is HIGH, the SAM data will not be transferred to the DRAM (SERIAL-INPUT-MODE ENABLE cycle).
- 2. SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 3. There must be no rising edges on the SC input during this time period.
- 4. QSF = 0 when the Lower SAM (bits 0-127) is being accessed. QSF = 1 when the Upper SAM (bits 128-255) is being accessed.



WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

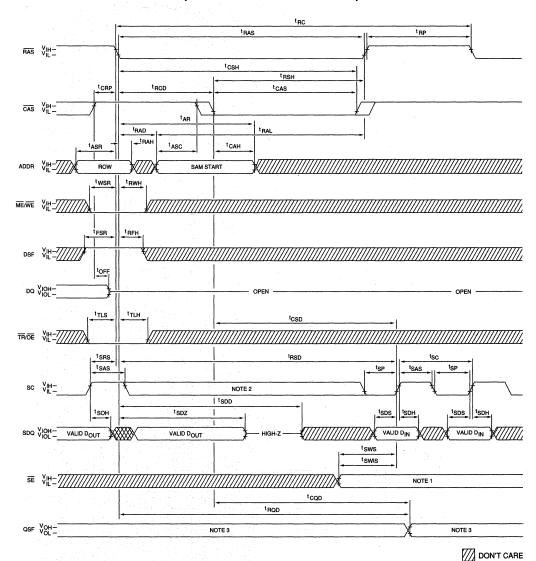
(When part was previously in the SERIAL INPUT mode)



VOTE:

- 1. SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 2. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

ALTERNATE WRITE TRANSFER (SAM-TO-DRAM TRANSFER)



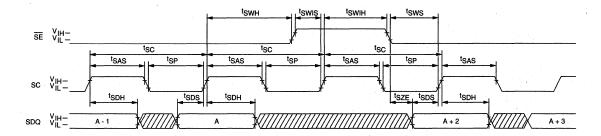
NOTE:

- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 2. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

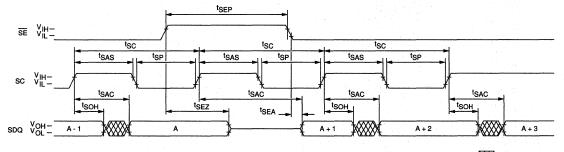
W UNDEFINED



SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

₩ UNDEFINED



VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- FAST PAGE MODE
- Dual port organization: 256K x 8 DRAM port
 512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times 70ns random, 22ns serial

SPECIAL FUNCTIONS

- NONPERSISTENT MASKED WRITE
- BLOCK WRITE
- SPLIT READ TRANSFER

OPTIONS

MARKING

• Timing [DRAM	, SAM (cycle/access)]
70ns, 25/22ns	- 7
80ns, 30/25ns	- 8 ·

Packages

Plastic SOJ (400 mil)			DJ
Plastic TSOP (400 mil)			TG
Plastic TSOP (400 mil):	revers	e pinout	RG

GENERAL DESCRIPTION

The MT42C8255 is a high speed, dual port CMOS dynamic random access memory or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 8-bit wide DRAM port or by a 512 \times 8 bit serial access memory (SAM) port. Data may be transferred from the DRAM to the SAM.

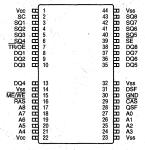
The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE and BLOCK WRITE. Eight 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data transfer

PIN ASSIGNMENT (Top View)

40-Pin SOJ (Q-6)

Vcc	þ	1		40	Ъ	Vss
SC	ď	2		39	þ	SQ8
SQ1	þ	3		38	þ	SQ7
SQ2	þ	4		37	þ	SQ6
SQ3	þ	5		36	þ	SQ5
SQ4	4	6		35	þ	SE
TR/OE	þ	7		34	þ	DQ8
DQ1	þ	8	-	33	þ	DQ7
DQ2	þ	9		32	þ	DQ6
DQ3	þ	10		31	þ	DQ5
DQ4	þ	11		30	þ	Vss
Vss	þ	12		29	Þ	DSF
ME/WE	þ	13		28	Þ	GND
RAS	þ	14		27	þ	CAS
. A8	q	15		26	þ	QSF
A7	þ	16		25	Þ	Α0
A6	q	17		24	þ	A1
A5	þ	18		23	þ	A2
A4	þ	19		22	þ	A3
Vcc	þ	20		21	þ	Vss

40/44-Pin TSOP (R-5)



40/44-Pin TSOP* (R-5)



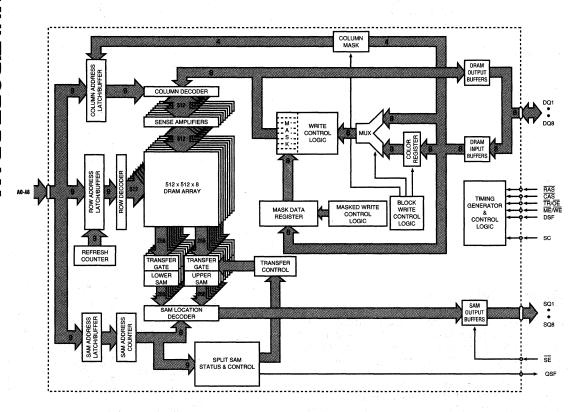
*Consult factory for availability.

are accomplished using three separate data paths: the 8-bit random access I/O port, the eight internal 512-bit wide paths between the DRAM and the SAM, and the 8-bit serial output port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8255 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN Numbers	TSOP(TG)PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter for the SAM registers.
7	7	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at \overline{RAS} (H \rightarrow L), or Output Enable: Enables the DRAM output buffers when taken LOW after \overline{RAS} goes LOW (\overline{CAS} must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM and READ TRANSFER (ME/WE = H) to the SAM.
35	39	SE	Input	Serial Port Enable: SE enables the serial output buffers and allows a serial READ operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when SE is inactive (HIGH).
29	31	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, MASKED WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	RAS	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits and strobe the ME/WE, TR/OE, DSF, SE, CAS and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycle.
27	29	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column- address bits and strobe the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and A0-A8 indicate the SAM start address (when CAS goes LOW). A8 = "don't care" for the start address during SPLIT READ TRANSFER.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SQ1-SQ8	Output	Serial Data Out: Output or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND	_	No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	Vcc	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8255 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note:

For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations.

DRAM OPERATION

DRAM REFRESH

Like any DRAM-based memory, the MT42C8255 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8255 supports CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH (CBR) cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8255 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES (RW)

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using

the A0-A8, \overline{RAS} and \overline{CAS} inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when \overline{RAS} transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when \overline{CAS} goes from HIGH-to-LOW.

Note:

RAS also acts as a "master" chip enable for the VRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.

For single port DRAMS, the \overline{OE} pin is a "don't care" when \overline{RAS} goes LOW. However, for the VRAM, when \overline{RAS} goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANS-FER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition for all DRAM operations (except \overline{CAS} -BEFORE- \overline{RAS}).

A DRAM READ operation is performed if $(\overline{\text{ME}})/\overline{\text{WE}}$ is HIGH when $\overline{\text{CAS}}$ goes LOW and remains HIGH until $\overline{\text{CAS}}$ goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{\text{TR}})/\overline{\text{OE}}$ input must transition from HIGH-to-LOW some time after $\overline{\text{RAS}}$ falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions; write mask enable and data write enable. ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If (ME)/WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.



MASKED WRITE (RWM)

The MASKED WRITE feature eliminates the need for a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. When $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF are LOW at the $\overline{\text{RAS}}$ HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8255 supports the nonpersistent mode of MASKED WRITE. In this mode, mask data must be entered with every RAS falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM

cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that \overline{CAS} is still HIGH. When \overline{CAS} goes LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every NONPERSISTENT MASKED WRITE.

FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The same mask is used during the entire FAST-PAGE-MODE \overline{RAS} cycle.

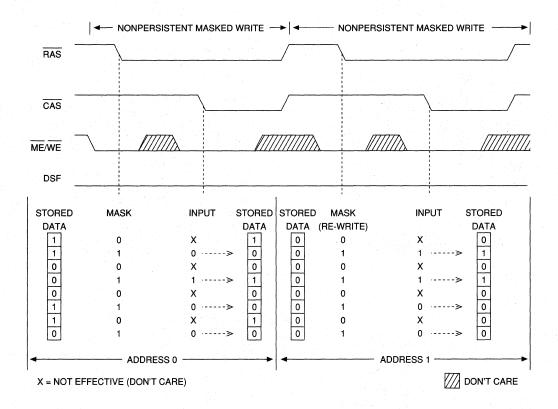


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

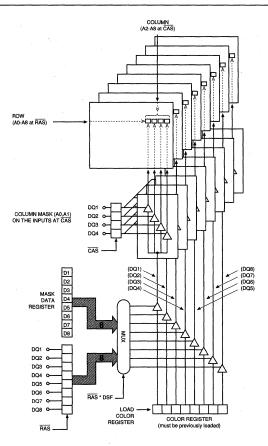


Figure 2
BLOCK WRITE EXAMPLE

BLOCK WRITE (BW)

If DSF is HIGH when $\overline{\text{CAS}}$ goes LOW, the MT42C8255 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 2). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER). Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

The row is addressed as in a normal DRAM WRITE cycle. However when $\overline{\text{CAS}}$ goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are "written" at the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

MASKED BLOCK WRITE (BWM)

The MASKED WRITE functions may be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of 4 column locations instead of just one column location.

The combination of $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF LOW when $\overline{\text{RAS}}$ goes LOW initiates a nonpersistent MASKED WRITE cycle. To perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when $\overline{\text{CAS}}$ goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the eight bit planes may be masked, along with any combination of the four column locations.

,	COLUMN ADDRESS CONTROLLED						
INPUTS	A0	A1					
DQ1	0	0					
DQ2	1	0					
DQ3	0	1					
DQ4	1	1					



LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when CAS goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGIS-TER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of RAS. The state of (ME)/WE when RAS goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER (RT)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when \overline{RAS} goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. CAS must fall for every RT in order to load a valid Tap address. An RT may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC, (REAL-TIME READ TRANSFER), $\overline{TR}/(\overline{OE})$ is taken HIGH after CAS goes LOW. The TRANSFER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANSFER), $\overline{TR}/(\overline{OE})$ may go HIGH before CAS goes LOW and the actual data TRANS-

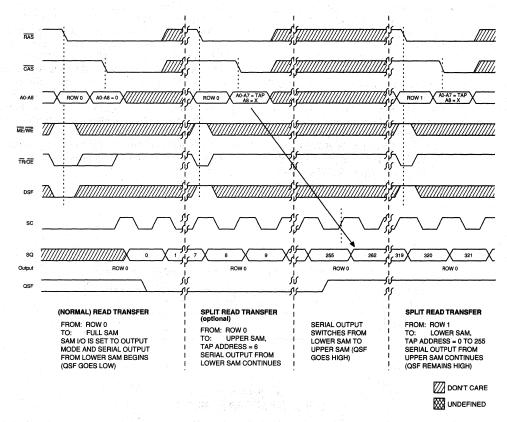


Figure 3 TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

FER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If SE is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. SE enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of SE.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRÂNSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer is not synchronized with the serial clock and may occur at any time while the other half is outputing data.

The $\overline{\text{TR}}/(\overline{\text{OE}})$ timing is also relaxed for SPLIT TRANSFER cycles. The rising edge of $\overline{\text{TR}}/(\overline{\text{OE}})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of $\overline{\text{CAS}}$ or the rising edge of SC. The transfer timing is generated internally for SPLIT TRANSFER cycles.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF). Then an SRT may be initiated by taking DSF HIGH when \overline{RAS} goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of \overline{CAS} . It is internally generated in such a manner that the SPLIT TRANSFER will automatically be to the SAM half not being accessed.

Figure 3 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is $\neq 0$. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7 = 1) the QSF output goes HIGH, and if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 3 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 4).

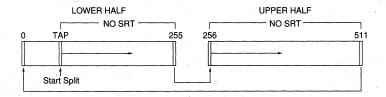


Figure 4
SPLIT SAM TRANSFER



SERIAL OUTPUT

The control inputs for serial output are SC and $\overline{\text{SE}}$. The rising edge of SC increments the serial address counter and provides access to the next SAM location. $\overline{\text{SE}}$ enables or disables the serial output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. \overline{SE} is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether \overline{SE} is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 4. Address count will wrap around

(after count 511) to Tap address 0 if in the "full" SAM modes.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100µs minimum, eight \overline{RAS} cycles must be executed to initialize the dynamic memory array. Micron recommends that $\overline{RAS} = \overline{TR}/\overline{OE} \ge V$ IH during power up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data.

The SAM portion of the MT42C8255 is completely static in operation and does not require refresh or initialization. The SAM port will power-up with the Output pins (SQs) in High- Z, regardless of the state of $\overline{\text{SE}}$. QSF initializes in the LOW state. The color register will contain random data after power-up.

TRUTH TABLE

		RAS FALLING EDGE			CAS FALL	A0-A81		DQ1-DQ8 ²		REGISTER	
CODE	FUNCTION	CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS,WE3	COLOR
	DRAM OPERATIONS										-
CBR	CAS-BEFORE-RAS REFRESH	0	X	16	16		х	х	_	X	X
ROR	RAS ONLY REFRESH	1	1	X	х	T - T	ROW	_	х	T -	X
RW	NORMAL DRAM READ OR WRITE	1	1	1	0 ;	0	ROW	COLUMN	х	VALID	х
RWM	MASKED WRITE TO DRAM (NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK	VALID DATA	X
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	х	COLUMN	USE
BWM	MASKED BLOCK WRITE TO DRAM (NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN	USE
	REGISTER OPERATIONS										
LCR	LOAD COLOR REGISTER	1	1	1	. 1	1	ROW ⁴	х	x	REG DATA	LOAD
	TRANSFER OPERATIONS										
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1,	0	1	. 0	X	ROW	TAP ⁵	X	X	X
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	Х	ROW	TAP ⁵	X	, X	Х

- 1. These columns show what must be present on the A0-A8 inputs when \overline{RAS} falls and when \overline{CAS} falls.
- 2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
- During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
- 4. The ROW that is addressed will be refreshed, but a ROW address is not required.
- 5. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half).
- 6. The MT42C8255 does not require a "1" on these pins, but to ensure compatibility with other 2 Meg VRAM function sets, it is recommended.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	1V to +7V
Operating Temperature, T _A (Ambient).	0°C to +70°C
Storage Temperature (Plastic)	55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	٧	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ VIN ≤ Vcc); all other pins not under test = 0V	lL .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (DQ, SQ disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Voн	2.4		٧	
Output Low Voltage (lout = 2.5mA)	Vol		0.4	٧	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C ₁₁		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SC, SE, DSF	C ₁₂		7	pF	2
Input/Output Capacitance: DQ, SQ	Ci/o		9	pF	2
Output Capacitance: QSF	Co		9	pF	2

CURRENT DRAIN, SAM IN STANDBY

		•
(000 × T	- 7000 N	F1/ 14/00/1
$0^{\circ}U \leq 1_{\star}$	_≤ 70°C: VCC	= 5V ±10%)
(A		

$(0^{-1}C \le 1_A \le 70^{-1}C, \ VCC = 5V \pm 10\%)$		M	AX		
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	lcc1	120	110	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; \overline{CAS} = Cycling: ${}^{t}PC = {}^{t}PC$ (MIN), other inputs \geq VIH or \leq VIL)	lcc2	110	100	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Viн after 8 RAS cycles (MIN); other inputs ≥ Viн or ≤ Vil.)	lcc3	10	10	mA	4
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vih)	lcc4	120	110	mA	3, 25
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	lcc5	120	110	mA	3, 5
SAM/DRAM DATA TRANSFER	lcce	130	120	mA	3

CURRENT DRAIN, SAM ACTIVE (*SC = MIN)

$0^{\circ}C \le I_A \le 70^{\circ}C$; $VCC = 5V \pm 10\%$)						
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES	
OPERATING CURRENT (RAS and \overline{CAS} = Cycling: ${}^{t}RC = {}^{t}RC$ (MIN))	lcc7	170	160	mA	3, 4 25	
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: ¹ PC = ¹ PC (MIN))	Iccs	160	150	mA	3, 4 26	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Viн after 8 RAS cycles (MIN); other inputs ≥ Viн or ≤Vil)	Icce	60	60	mA	3, 4	
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = Vih)	Icc10	170	160	mA	3, 4 25	
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	lcc11	170	160	mA	3, 4, 5	
SAM/DRAM DATA TRANSFER	lcc12	180	170	mA	3, 4	



DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES		
Random READ or WRITE cycle time	tRC tRC	130		150		ns	1		
READ-MODIFY-WRITE cycle time	tRWC	175		190		ns			
FAST-PAGE-MODE READ or WRITE	t _{PC}	45		50	1.00	ns			
cycle time					1000		4 11 1		
FAST-PAGE-MODE READ-MODIFY-WRITE	^t PRWC	90		95		ns	- 1, 1		
cycle time				4 gr. 1			14.4		
Access time from RAS	^t RAC		70	Service Services	80	ns	14		
Access time from CAS	tCAC		20		25	ns	15		
Access time from (TR)/OE	^t OE		20		20	ns			
Access time from column address	^t AA		35		40	ns	100		
Access time from CAS precharge	^t CPA		40		45	ns			
RAS pulse width	tRAS	70	20,000	80	20,000	ns	39.504		
RAS pulse width (FAST PAGE MODE)	^t RASP	70	100,000	80	100,000	ns	1000		
RAS hold time	^t RSH	20		25		ns			
RAS precharge time	^t RP	50		60		ns			
CAS pulse width	^t CAS	20	10,000	25	10,000	ns	1.00		
CAS hold time	t _{CSH}	70		80		ns	11.0		
CAS precharge time	^t CP	10		10		ns	16		
RAS to CAS delay time	tRCD	20	45	20	55	ns	17		
CAS to RAS precharge time	tCRP	10		10	11.11.11	ns			
Row address setup time	t _{ASR}	0		0		ns			
Row address hold time	^t RAH	. 10		10		ns	1971		
RAS to column	^t RAD	15	35	15	45	ns	18		
address delay time									
Column address setup time	†ASC	0		0		ns	14.		
Column address hold time	^t CAH	15		15		ns			
Column address hold time	^t AR	45		55		ns			
(referenced to RAS)									
Column address to	^t RAL	35		40		ns			
RAS lead time									
Read command setup time	t _{RCS}	0		0		ns			
Read command hold time	^t RCH	0		0		ns	19		
(referenced to CAS)									
Read command hold time	^t RRH	0		0		ns	19		
(referenced to RAS)									
CAS to output in Low-Z	^t CLZ	3		3		ns	19		
Output buffer turn-off delay from CAS	^t OFF	3	20	3	20	ns	20,23		
Output disable delay from (TR)/OE	tOD	3	10	3	10	ns	20,23		
Output disable hold time from start of WRITE	^t OEH	10		10		ns	27		
Output Enable to RAS delay	†ROH	0		0		ns			

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8				
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES	
Write command setup time	twcs	0		0		ns	21	
Write command hold time	tWCH	15		15		ns		
Write command hold time (referenced to RAS)	tWCR	45		55		ns		
Write command pulse width	^t WP	15		15		ns		
Write command to RAS lead time	t _{RWL}	20		20		ns		
Write command to CAS lead time	tCWL	15		20		ns		
Data-in setup time	t _{DS}	0		0		ns	22	
Data-in hold time	t _{DH}	15		15		ns	22	
Data-in hold time (referenced to RAS)	^t DHR	45		55		ns		
RAS to WE delay time	tRWD	90		100	1	ns	21	
Column address to WE delay time	tAWD	55		65	1 11	ns	21	
CAS to WE delay time	tCMD	40		45		ns	21	
Transition time (rise or fall)	t _T	3	35	3	35	ns	9, 10	
Refresh period (512 cycles)	tREF		8		8	ms	1	
RAS to CAS precharge time	tRPC	0		0		ns		
CAS setup time (CAS-BEFORE-RAS REFRESH)	^t CSR	10		10		ns	5	
CAS hold time (CAS-BEFORE-RAS REFRESH)	^t CHR	10		10		ns	5	
ME/WE to RAS setup time	†WSR	0		0		ns	†	
ME/WE to RAS hold time	tRWH	15		15		ns		
Mask data to RAS setup time	t _{MS}	0		0		ns		
Mask data to RAS hold time	^t MH	15		15		ns	1	



TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

CHARACTERISTICS -7		7	-8				
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
TR/(OE) LOW to RAS setup time	^t TLS	0		0		ns	1
TR/(OE) LOW to RAS hold time	^t TLH	15	10,000	15	10,000	ns	
TR/(OE) LOW to RAS hold time	^t RTH	65	10,000	70	10,000	ns	
(REAL-TIME READ-TRANSFER only)		`					1
TR/(OE) LOW to CAS hold time	^t CTH	25		25	1 2	ns	
(REAL-TIME READ-TRANSFER only)					1.11		
TR/(OE) HIGH to RAS precharge time	tTRP	50		60		ns	7.3
TR/(OE) precharge time	tTRW	20		25	e kanalan da	ns	
TR/(OE) HIGH to SC lead time	^t TSL	5		5		ns	
First SC edge to TR/(OE) HIGH	^t TSD	15		15		ns	
delay time							2.25
SC to RAS setup time	tSRS	25		30		ns	
TR/(OE) HIGH to RAS setup time	tYS	0		0		ns	
TR/(OE) HIGH to RAS hold time	tYH	15		15		ns	
DSF to RAS setup time	tFSR	0		0		ns	
DSF to RAS hold time	tRFH	15		15		ns	
SC to QSF delay time	tSQD		25		30	ns	
SPLIT TRANSFER setup time	tSTS	25		30		ns	
SPLIT TRANSFER hold time	tSTH	0		0		ns	
DSF (at CAS LOW) to RAS hold time	tFHR	50		55		ns	
DSF to CAS setup time	tFSC	0		0		ns	
DSF to CAS hold time	^t CFH	15		15		ns	
TR/OE to QSF delay time	^t TQD		25		25	ns	
RAS to QSF delay time	^t RQD		75		75	ns	
CAS to QSF delay time	tCQD		35		35	ns	
RAS to first SC delay	tRSD	80		80		ns	
CAS to first SC delay	tCSD	30	100	30	1:	ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7			-8	1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	tSC	25		30		ns	
Access time from SC	tSAC		22		25	ns	24, 28
SC precharge time (SC LOW time)	t _{SP}	8		10		ns	
SC pulse width (SC HIGH time)	tSAS	8		10		ns	
Access time from SE	tSEA		15		15	ns	24
SE precharge time	tSEP	10		10		ns	
SE pulse width	^t SE	10		10	l .	ns	
Serial data-out hold time after SC high	^t SOH	. 5		5	1 -	ns	24, 28
Serial output buffer turn-off delay from SE	^t SEZ	3	12	3	12	ns	20, 24

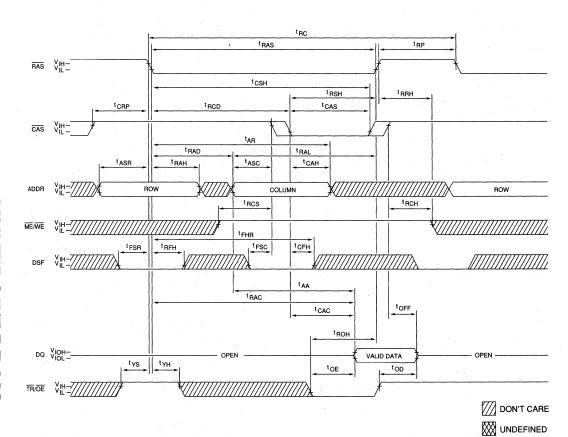


NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. Vcc = $5V \pm 10\%$, f = 1 MHz.
- Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition from 0 to 3V for AC testing.
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{\text{CAS}} = \text{ViH}$, DRAM data output (DQ1-DQ8) is High-Z.
- 12. If $\overline{\text{CAS}} = \text{VIL}$, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
- DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: VOH = 2.0V; VOL = 0.8V.
- 14. Assumes that [†]RCD < [†]RCD (MAX). If [†]RCD is greater than the maximum recommended value shown in this table, [†]RAC will increase by the amount that [†]RCD exceeds the value shown.
- 15. Assumes that ^tRCD ≥ ^tRCD (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCP.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

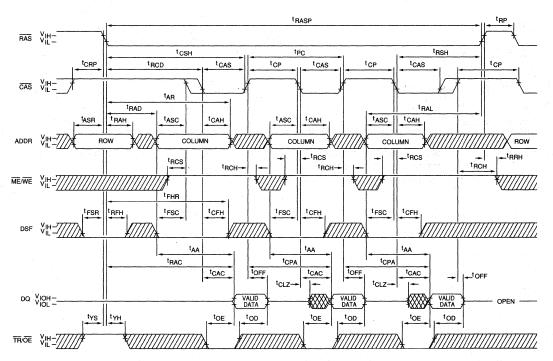
- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. OD, tOFF and tSEZ define the time when the output achieves open circuit (VoH -200mV, Vol. +200mV). This parameter is sampled and not 100% tested.
- tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \le$ tWCS (MIN), the cycle is a LATE-WRITE and $\overline{TR}/\overline{OE}$ must control the output buffers during the write to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate but the WRITE will be valid, if tOD and tOEH are met. See the LATE-WRITE AC Timing diagram.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and ME/WE leading edge in LATE-WRITE or READ-WRITE cycles.
- During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE or CAS, whichever goes HIGH first.
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. Address (A0-A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
- 26. Address (A0-A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 27. LATE-WRITE and READ-MODIFY-WRITE cycles must have 'OD and 'OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if CAS remains LOW and OE is taken LOW after 'OEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 28. ^tSAC is MAX at 70° C and 4.5V Vcc; ^tSOH is MIN at 0°C and 5.5V Vcc. These limits will not occur simultaneously at any given voltage or temperature. (^tSOH = ^tSAC output transition time); this is guaranteed by design.

DRAM READ CYCLE





DRAM FAST-PAGE-MODE READ CYCLE



DON'T CARE

₩ UNDEFINED

NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.

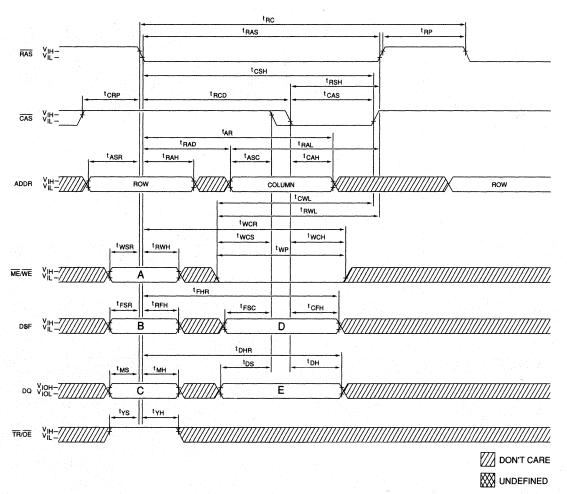
WRITE CYCLE FUNCTION TABLE 1

	LOGIC STATES								
		RAS Fal	ling Edge		CAS Falling Edge				
FUNCTION	A ME/WE	B DSF	C DQ (Input)	D DSF	E ² DQ (Input)				
Normal DRAM WRITE	1	0	Х	0	DRAM Data				
MASKED WRITE to DRAM	0	0	Write Mask	0	DRAM Data (Masked)				
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	Х	. 1	Column Mask				
MASKED BLOCK WRITE to DRAM	0	0	Write Mask	1	Column Mask				
Load Color Register	. 1	1	Х	1	Color Data				

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
- 2. CAS or ME/WE falling edge, whichever occurs later.

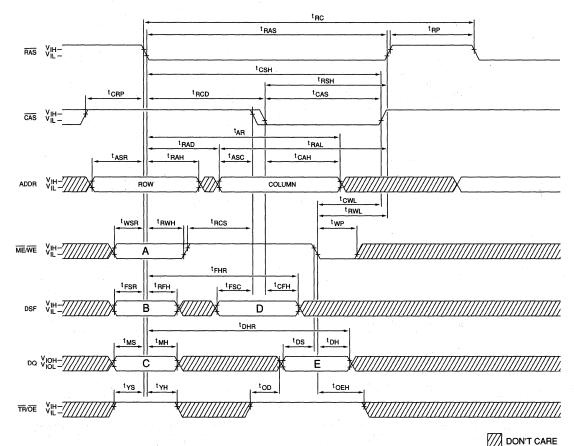


DRAM EARLY-WRITE CYCLE 1



NOTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE

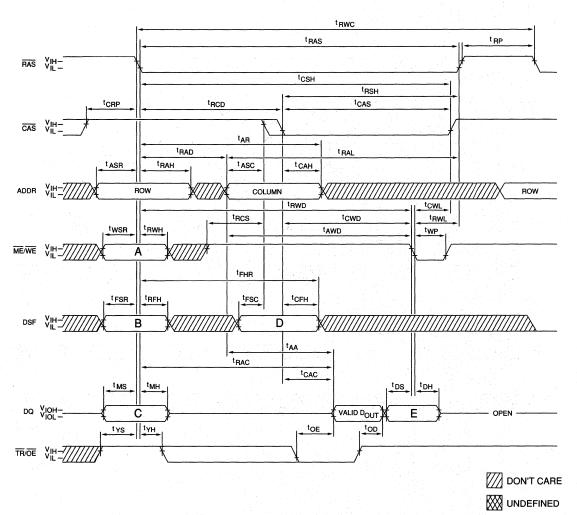


₩ UNDEFINED

NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

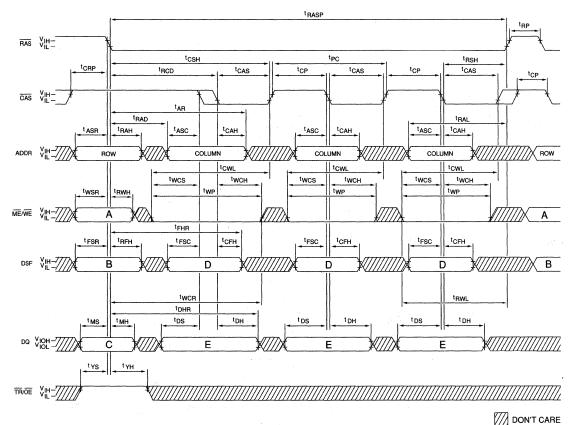


DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE



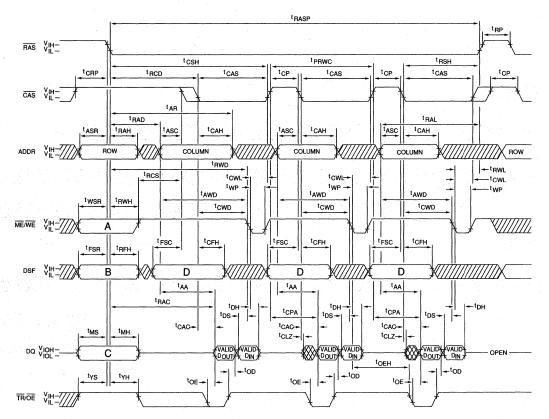
NOTE:

- READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
- 2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

₩ UNDEFINED



DRAM FAST-PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



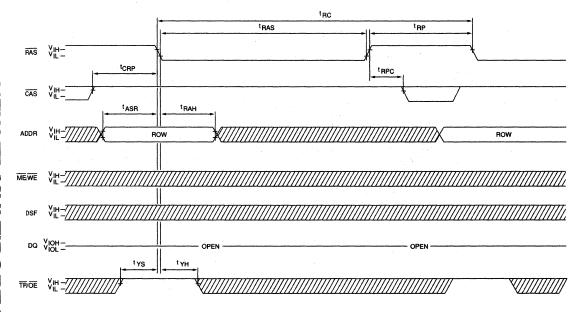
DON'T CARE

₩ undefined

NOTE:

- READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF state for the desired WRITE operation.
- 2. The logic states of "A", "B", "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

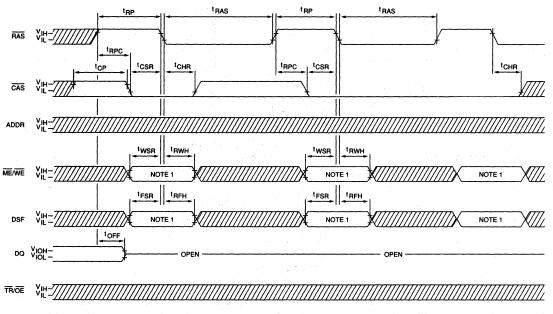
DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)



DON'T CARE

₩ undefined

CAS-BEFORE-RAS REFRESH CYCLE

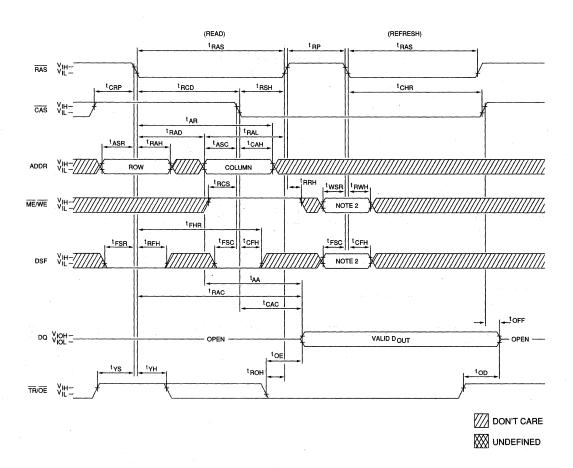


DON'T CARE

W UNDEFINED

OTE: 1. The MT42C8255 operates with ME/WE and DSF = "don't care," but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

DRAM HIDDEN-REFRESH CYCLE



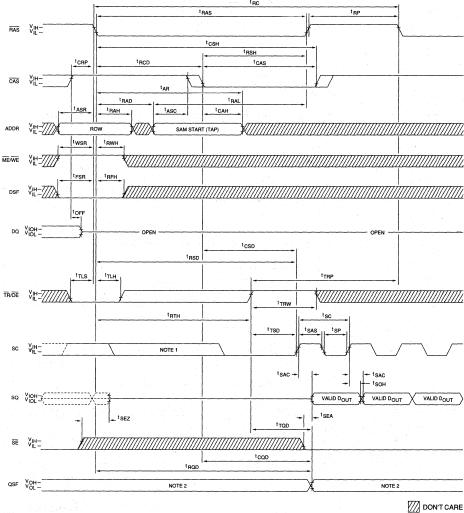
NOTE:

- 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case, ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.
- The MT42C8255 operates with ME/WE and DSF = "don't care", but to ensure compatibility with all 2 Meg VRAM feature sets, it is recommended that they be HIGH ("1").

NEW **M** MULTIPORT DRAN

READ TRANSFER 3 (DRAM-TO-SAM TRANSFER)

(When serial part was previously High-Z or SC idle)

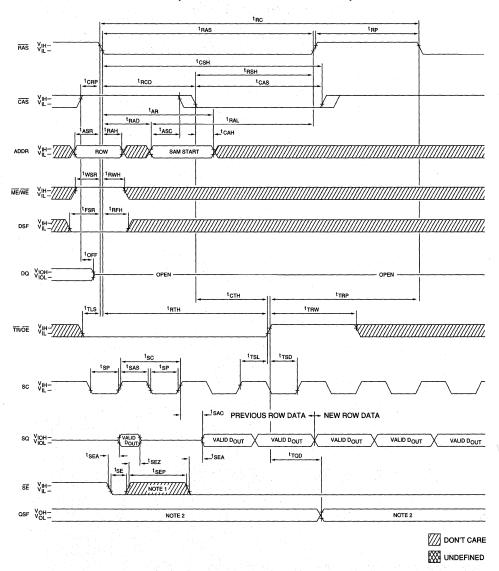


W UNDEFINED

IOTE:

- 1. There must be no rising edges on the SC input during this time period.
- 2. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.
- 3. If TLH is timing for the TR/(OE) rising edge, the transfer is self-timed and the CSD and RSD times must be met. If ^tRTH is timing for the TR/(OE) rising edge, the transfer is done off of the TR/(OE) rising edge and ^tTSD must be met.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

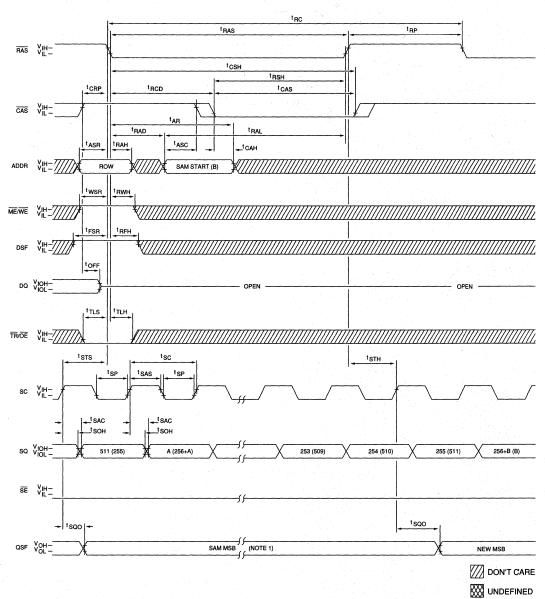


NOTE:

- 1. The SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.
- 2. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.

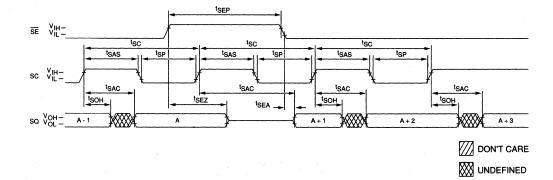


SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)



IOTE: 1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

SAM SERIAL OUTPUT



VRAM

256K x 8 DRAM WITH 512 x 8 SAM

FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL and CMOS compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 8ms
- FAST PAGE MODE access with Extended Data Out
- Dual port organization: 256K x 8 DRAM port 512 x 8 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 300mW active, typical
- Fast access times 70ns random, 15ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Mandatory Function set
- PERSISTENT MASKED WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- PROGRAMMABLE SPLIT SAM

OPTIONS

MARKING

• Timing [DRAM]	, SAN	1 (cycle	/access)]
70ns, 18/15ns		- 5 S		- 7
80ns, 25/20ns				- 8

Packages

Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic TSOP (400 mil) reverse pinout	RG

GENERAL DESCRIPTION

The MT42C8256 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 2,097,152 bits. These bits may be accessed by an 3-bit wide DRAM port or by a 512 \times 8 bit serial access nemory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

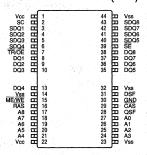
The DRAM portion of the VRAM is functionally identical of the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. light 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data

PIN ASSIGNMENT (Top View)

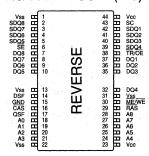
40-Pin SOJ (Q-6)

		_	 			
Vcc	þ	1		40	þ	Vss
SC	ď	2	 	39	þ	SDQ
SDQ1	þ	3		38	þ	SDQ
SDQ2	þ	4		37	þ	SDQ
SDQ3	þ	5		36	þ	SDQ
SDQ4	d	6		35	þ	SE
TR/OE	d	7		34	þ	DQ8
DQ1	d	8	. 4	33	þ	DQ7
DQ2	þ	9		32	þ	DQ6
DQ3	þ	10		31	þ	DQ5
DQ4	d	11		30	þ	Vss
Vss	þ	12		29	þ	DSF
ME/WE	þ	13		28	þ	GND
RAS	þ	14		27	þ	CAS
A8	þ	15		26		QSF
A7	þ	16		25	þ	AO-
A6	þ	17		24	þ	A1
A5	þ	18		23	þ	A2
A4	þ	19		22	þ	АЗ
Vcc	þ	20		21	þ	Vss

40/44-Pin TSOP (R-5)



40/44-Pin TSOP* (R-5)



*Consult factory for availability.

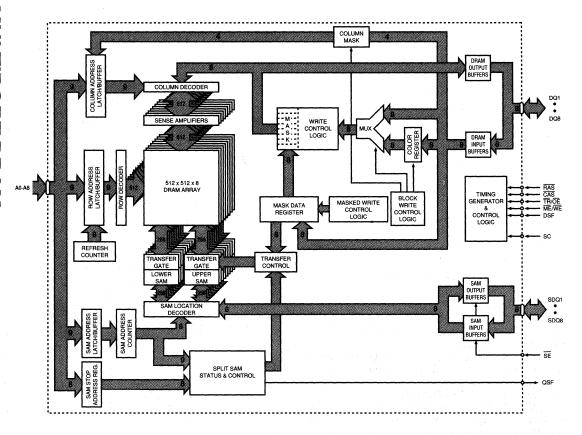
transfer are accomplished using three separate bidirectional data paths: the 8-bit random access I/O port, the eight internal 512 bit wide paths between the DRAM and the SAM, and the 8-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each port may be operated asynchronously and independently of the other except when data is being transferred internally. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of RAS addresses are executed at least every 8ms (regardless of sequence). Micron

recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C8256 are optimized for high performance graphics and communication designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT TRANSFERs, Extended Data Out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN Numbers	TSOP(TG) PIN Numbers	SYMBOL	TYPE	DESCRIPTION
2	2	SC	Input	Serial Clock: Clock input to the serial address counter and data latch for the SAM registers.
7	7	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at RAS (H → L), or Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a High-Z state.
13	15	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
35	39	SE	Input	Serial Port Enable: SE enables the serial I/O buffers and allows a serial READ or WRITE operation to occur, otherwise the output buffers are in a High-Z state. The SAM address count will be incremented by the rising edge of SC when SE is inactive (HIGH).
29	31 · ·	DSF	Input	Special Function Select: DSF is used to indicate which special functions (BLOCK WRITE, FLASH WRITE, SPLIT TRANSFER, etc.) are used for a particular access cycle (see Truth Table).
14	16	RAS	Input	Row Address Strobe: RAS is used to clock in the 9 row-address bits and strobe for ME/WE, TR/OE, DSF, SE, CAS and DQ inputs. It also acts as the master chip enable, and must fall for initiation of any DRAM or TRANSFER cycles.
27	29	CAS	Input	Column Address Strobe: CAS is used to clock in the 9 columnaddress bits and as a strobe for the DSF input (BLOCK WRITE only).
25, 24, 23, 22, 19, 18, 17, 16, 15	27, 26, 25, 24, 21, 20, 19, 18, 17	A0-A8	Input	Address Inputs: For the DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 8-bit word out of the 262,144 available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and A0-A8 indicate the SAM start address (when CAS goes LOW). A8 = "don't care" for the start address during SPLIT TRANSFERs.
8, 9, 10, 11, 31, 32, 33, 34	8, 9, 10, 13, 35, 36, 37, 38	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data input/output for DRAM access cycles: These pins also act as inputs for Mask and Color Register load cycles, DQ Mask and Column Mask for BLOCK WRITE.
3, 4, 5, 6, 36, 37, 38, 39	3, 4, 5, 6, 40, 41, 42, 43	SDQ1-SDQ8	Input/ Output	Serial Data I/O: Input, output, or High-Z.
26	28	QSF	Output	Split SAM Status: QSF indicates which half of the SAM is being accessed. LOW if address is 0-255, HIGH if address is 256-511.
28	30	GND		No Connect/GND: This pin must be tied to ground to allow for upward functional compatibility with future VRAM feature sets.
1, 20	1, 22	Vcc	Supply	Power Supply: +5V ±10%
12, 21, 30, 40	14, 23, 32, 44	Vss	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT42C8256 can be divided into three functional blocks (see Figure 1): the DRAM, the transfer circuitry, and the SAM. All of the operations described below are shown in the AC Timing Diagrams section of this data sheet and summarized in the Truth Table.

Note:

For dual-function pins, the function not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$ in references to transfer operations,

DRAM OPERATION

DRAM REFRESH

Like any DRAM based memory, the MT42C8256 VRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT42C8256 supports CAS-BEFORE-RAS, RAS ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH (CBR) cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data, and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period. CBR cycles are also used to reset MASKED WRITE and PROGRAMMABLE SPLIT SAM operating modes. There are three CBR cycles defined for the MT42C8256; CBR No Reset (CBRN), CBR Reset Stop Address (CBRS), and CBR Reset All Options (CBRR). To perform these functions, two additional pins are defined for CBR cycles, $\overline{\text{ME}}/\overline{\text{WE}}$ and DSF1. These operations are described in detail in the MASKED WRITE and SPLIT READ/ WRITE TRANSFER sections of the functional description.

The refresh address must be generated externally and applied to A0-A8 inputs for RAS-ONLY REFRESH cycles. The DQ pins remain in a High-Z state for both the RAS-ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH cycles are performed by toggling RAS (and keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row being accessed. The SAM portion of the MT42C8256 is fully static and does not require any refreshing.

DRAM ACCESS CYCLES (RW)

The DRAM portion of the VRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this part, several conditions that were undefined or in "don't care" states for the DRAM are specified for the VRAM. These conditions are highlighted in the following discussion. In addition, the VRAM has special functions that can be used when writing to the DRAM.

The 18 address bits that are used to select an 8-bit word from the 262,144 available are latched into the chip using the A0-A8, RAS and CAS inputs. First, the nine row-address bits are set up on the address inputs and clocked into the part when RAS transitions from HIGH-to-LOW. Next, the 9 column address bits are set up on the address inputs and clocked-in when CAS goes from HIGH-to-LOW.

Note:

 \overline{RAS} also acts as a "master" chip enable for the VRAM. If \overline{RAS} is inactive, HIGH, all other DRAM control pins $(\overline{CAS}, \overline{TR}/\overline{OE}, \overline{ME}/\overline{WE}, etc.)$ are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without \overline{RAS} falling.

For single port DRAMS, the OE pin is a "don't care" when \overline{RAS} goes LOW. However, for the VRAM, when \overline{RAS} goes LOW, $\overline{TR}/(\overline{OE})$ selects between DRAM access or TRANS-FER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition for all DRAM operations (except CAS-BEFORE-RAS).

A DRAM READ operation is performed if $(\overline{ME})/\overline{WE}$ is HIGH when CAS goes LOW and remains HIGH until CAS goes HIGH. The data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the VRAM, ME/WE performs two functions; write mask enable and data write enable. $\overline{\text{ME}}/(\overline{\text{WE}})$ is used, when RAS goes LOW, to select between a MASKED WRITE cycle and a normal WRITE cycle. If $\overline{\text{ME}}/(\overline{\text{WE}})$ is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any non-masked DRAM access cycle (READ or WRITE), $\overline{\text{ME}}/(\overline{\text{WE}})$ must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW before CAS goes LOW, a DRAM EARLY-WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells. If $(\overline{\text{ME}})$ WE goes LOW after CAS goes LOW, a DRAM LATE-WRITE operation is performed (refer to the AC timing diagrams).

The VRAM can perform all the normal DRAM cycles including READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ (with Extended Data Out), FAST-PAGE-MODE WRITE (Late or Early), and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

EXTENDED DATA OUTPUT

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of \overline{CAS} . If CAS goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT42C8256 offers an accelerated FAST PAGE MODE (FPM) cycle by eliminating output disable from CAS HIGH. This option is called Extended Data Out, and it allows CAS precharge time (tCP) to occur without the output data going invalid (see DRAM READ and DRAM FAST-PAGE-MODE READ waveforms).

Extended Data Out operates as any DRAM READ or FPM READ, except data will be held valid after \overline{CAS} goes HIGH, as long as RAS is LOW. If the DQ outputs are wire OR'd, (TR)/OE must be used to disable idle banks of VRAMs. During non-PAGE-MODE READ cycles, the outputs are disabled at tOFF time after RAS and CAS are HIGH. The ^tOFF time is referenced from the rising edge of RAS or CAS, whichever occurs later.

MASKED WRITE (RWM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing individual bits within the 8-bit word. The MT42C8256 supports two types of MASKED WRITE cycles, nonpersistent MASKED WRITE and persistent MASKED WRITE. When $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF are LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE is performed.

The MT42C8256 initializes in the nonpersistent mode. In this mode, mask data must be entered with every RAS falling edge. The data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register (see Figure 1). The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operation to proceed. Note that CAS is still HIGH. When CAS goes LOW, the bits present on the DO1-DO8 inputs will be either written to the DRAM (if the mask data bit is HIGH) or ignored (if the mask data bit is LOW). The DRAM contents that correspond to masked input bits will not be changed during the WRITE cycle. The mask data register is cleared at the end of every nonpersistent MASKED WRITE.

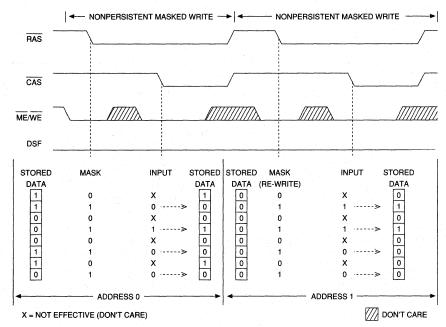


Figure 1 NONPERSISTENT MASKED WRITE EXAMPLE

The selection of persistent or nonpersistent MASKED WRITE is done by performing a LOAD MASK REGISTER (LMR) cycle (see LMR description). If an LMR is done, all ensuing MASKED WRITEs are persistent and the mask data will be provided by the Mask Data Register (see Figure 2). The mask data is applied in the same manner as in nonpersistent mode.

To reset the device back to the nonpersistent mode, a CAS-BEFORE-RAS, Reset All Options (CBRR) cycle must be performed. This cycle is defined as a CBR with DSF LOW when RAS falls, WE is "don't care." To preserve the persistent mode of MASKED WRITE, while using CAS-BEFORE-RAS REFRESH, a CBRN cycle is used. This cycle will perform a refresh of the internally addressed row of DRAM but will not reset the MASKED WRITE mode.

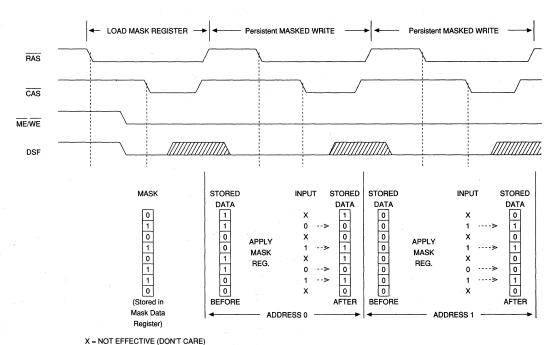
FAST PAGE MODE can be used with MASKED WRITE to write several column locations in an addressed row. The

same mask is used during the entire FAST-PAGE-MODE \overline{RAS} cycle.

BLOCK WRITE (BW)

If DSF is HIGH when $\overline{\text{CAS}}$ goes LOW, the MT42C8256 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register are directly written to four adjacent column locations (see Figure 3). The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However when \overline{CAS} goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" of four adjacent column locations that will be accessed. The DQ inputs (DQ1, 2, 3, and 4) are then used to determine what combination of the four column locations will be changed. The DQ inputs are



DON'T CARE

Figure 2 PERSISTENT MASKED WRITE EXAMPLE

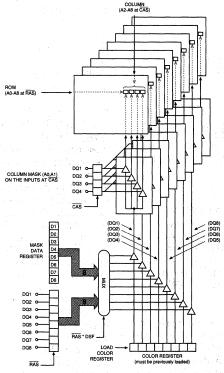


Figure 3 **BLOCK WRITE EXAMPLE**

"written" at the falling edge of CAS or WE, whichever occurs later (see the WRITE cycle waveforms). The table on this page illustrates how each of the DQ inputs is used to selectively enable or disable individual column locations within the block. The write enable controls are active HIGH; a logic "1" enables the WRITE function and a logic "0" disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DO location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane.

MASKED BLOCK WRITE (BWM)

The MASKED WRITE functions may also be used during BLOCK WRITE cycles. MASKED BLOCK WRITE operates exactly like the normal MASKED WRITE except the mask is now applied to the 8 bit-planes of four column locations instead of just one column location.

The combination of $\overline{ME}/(\overline{WE})$ LOW and DSF LOW when RAS goes LOW initiates a MASKED WRITE cycle. To

perform a MASKED BLOCK WRITE, the DSF pin must be HIGH when CAS goes LOW. By using both the column mask input and the MASKED WRITE function of BW, any combination of the eight bit planes may be masked, along with any combination of the four column locations.

The MASKED BLOCK WRITE will be nonpersistent (new mask) at device power-up. To enter persistent mode (old mask) a LOAD MASK REGISTER cycle is performed. All MASKED BLOCK WRITEs will be persistent after the LMR. To reset to nonpersistent mode, a CBRR (reset all) cycle must be performed.

INDUTO	COLUMN ADDRE	SS CONTROLLED
INPUTS	A0	A1
DQ1	0	0
DQ2	1	0
DQ3	0	1
DQ4	1	1

MASKED FLASH WRITE (FWM)

The MASKED FLASH WRITE cycle is similar to the MASKED BLOCK WRITE cycle in that it uses the color register to accelerate the writing of a select color to the DRAM memory array. Instead of writing to four adjacent column locations in one DRAM cycle (BLOCK WRITE), FWM writes the contents of the color register to all column locations on an addressed row in one cycle.

The FWM cycle is selected by taking $\overline{TR}/(\overline{OE})$ and DSF HIGH and $\overline{ME}/(\overline{WE})$ LOW at the falling edge of \overline{RAS} . DSF is "don't care" at the falling edge of \overline{CAS} . The DQ plane mask applies as it does for all masked write cycles; if the mask register has been loaded, the mask is persistent; if it has not, the mask is nonpersistent.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation loads the data present on the DQ pins into the 8-bit Mask Data Register at the falling edge of \overline{CAS} or $\overline{(ME)/WE}$. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{(ME)/WE}$, and DSF being HIGH when \overline{RAS} goes LOW indicates the cycle is a LOAD REGISTER cycle. DSF is used when \overline{CAS} goes LOW to select the register to be loaded and must be LOW for a LOAD MASK REGISTER cycle.

Note: LOAD MASK REGISTER cycles also enable the persistent MASKED WRITE mode. All ensuing MASKED WRITEs (including MASKED WRITE and MASKED SPLIT WRITE TRANSFER) will be masked with data from the mask register. A CBRR has to be done to reset back to nonpersistent mode.

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

During persistent operation, the mask data register contents are used for MASKED WRITE, MASKED BLOCK WRITE, MASKED FLASH WRITE, and MASKED WRITE and SPLIT WRITE TRANSFER cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF is HIGH when CAS goes LOW. The contents of the 8-bit color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE and FLASH WRITE cycles.

TRANSFER OPERATIONS

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of \overline{RAS} . The state of $(\overline{ME})/\overline{WE}$ when \overline{RAS} goes LOW indicates the direction of the TRANSFER (to or from the DRAM), and DSF is used to select between NORMAL TRANSFER and SPLIT TRANSFER cycles. Each of the TRANSFER cycles is described in this section.

READ TRANSFER (RT)

If $(\overline{ME})/\overline{WE}$ is HIGH and DSF is LOW when \overline{RAS} goes LOW, a READ TRANSFER cycle is selected. The row address bits indicate which eight 512-bit DRAM row planes are transferred to the eight SAM data register planes. The column address bits indicate the start address (or Tap address) of the serial output cycle from the SAM data registers. CAS must fall for every TRANSFER in order to load a valid Tap address. A read transfer may be accomplished in two ways. If the transfer is to be synchronized with the serial clock, SC (REAL-TIME READ TRANSFER), TR/(OE) is taken HIGH after CAS goes LOW. The TRANS-FER will be made when $\overline{TR}/(\overline{OE})$ goes HIGH. If the transfer does not have to be synchronized with SC (READ TRANS-FER), TR/(OE) may go HIGH before CAS goes LOW and the actual data TRANSFER will be timed internally (refer to the AC Timing Diagrams). During the TRANSFER, 4,096 bits of DRAM data are written into the SAM data registers and the Tap address is stored in an internal 9-bit register. The split SAM status pin (QSF) will be LOW if the Tap is in the lower half (addresses 0 through 255), and HIGH if it is in the upper half (256 through 511). If \overline{SE} is LOW, the first bits of the new row data will appear at the serial outputs with the first SC clock pulse. \overline{SE} enables the serial outputs and may be either HIGH or LOW during this operation. The SAM address pointer will increment with the SC LOW-to-HIGH transition, regardless of the state of SE. Performing a READ TRANSFER cycle sets the direction of the SAM I/O buffers to the output mode.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER (SRT) cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream. When using normal TRANSFER cycles to do midline reloads, a REAL-TIME READ TRANSFER must be done. The REAL-TIME READ TRANSFER has to occur between the last clock of "old" data and first clock of the "new" data of the SAM port.

When using the SPLIT TRÂNSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and is not synchronized with the serial clock.

The $\overline{TR}/(\overline{OE})$ timing is also relaxed for SPLITTRANSFER cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle and therefore is independent of the falling edge of \overline{CAS} or the rising edge of SC. The transfer timing is generated internally for SPLITTRANSFER cycles. A SPLIT READ TRANSFER does not change the direction of the SAM I/O port.

A "full" READ TRANSFER cycle must precede any sequence of SRT cycles to provide a reference to which half of the SAM the access will begin (the state of QSF), and to set SAM I/O direction. Then an SRT may be initiated by taking DSF HIGH when RAS goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. The column address, A0-A7, is used to input the SAM Tap address. Address pin A8 is a "don't care" when the Tap address is loaded at the HIGH-to-LOW transition of CAS. It is internally generated in such a manner that the SPLITTRANSFER will automatically be to the SAM half not being accessed.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is performed first, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is $\neq 0$. Serial access continues, and when the SAM address counter reaches 255 ("A8" = 0, A0-A7=1) the OSF output goes HIGH and, if an SRT was done for the upper half, the new Tap address is loaded for the next half ("A8" = 1, A0-A7 = Tap). Once the serial access has switched to the upper SAM (QSF has gone HIGH), new data may be transferred to the lower SAM. For example, the next step in Figure 4 would be to wait until QSF went LOW (indicating that row-1 data is shifting out of the lower SAM) and execute an SRT of the upper half of row 1 to the upper SAM. If the half boundary is reached before an SRT is done for the next half, the device will leave split mode and the access will start from address 256 if going to the upper half or at 0 if going to the lower half (see Figure 5).

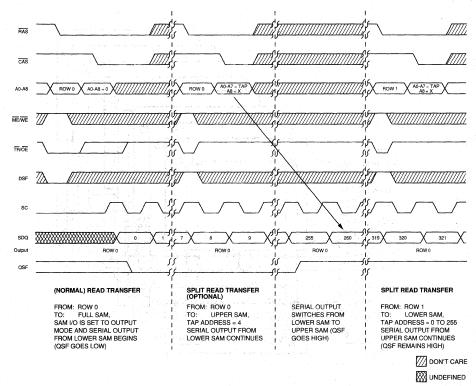


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE

The stop address of the SAM half (the point at which access will change to the next half) is programmable on the MT42C8256. This function is described in the PROGRAMMABLE SPLIT SAM section of the Functional Description.

MASKED WRITE TRANSFER (MWT)

The operation of the MASKED WRITE TRANSFER (MWT) is identical to that of the READ TRANSFER described previously except $(\overline{\text{ME}})/\overline{\text{WE}}$ is LOW and a DQ plane mask is applied when $\overline{\text{RAS}}$ goes LOW. The row address indicates the DRAM row to which the SAM data registers will be written. The column address (Tap) indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. A DQ mask must be applied to all MWTs as shown in Figure 6. This may be done using persistent or nonpersistent modes. When using persistent mode, the mask will be supplied by the mask register. When in nonpersistent mode, the DQ pins are used to input a bit plane mask at the falling

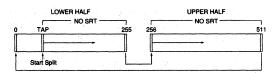


Figure 5
SPLIT SAM TRANSFER

edge of RAS. An MWT changes the direction of the SAM I/O buffers to the input mode. To change the SAM I/O buffers to input mode without SAM data being transferred to the DRAM, a mask of all 0's must be presented on the DQ pins when RAS falls. QSF is LOW if serial input is to the lower half of the SAM, and HIGH if it is to the upper.

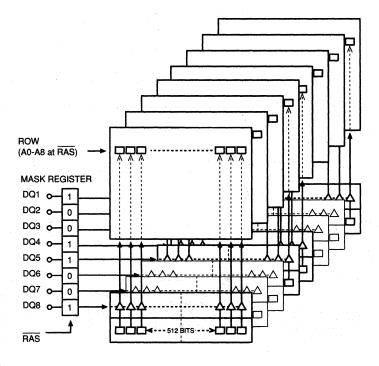


Figure 6
DQ MASKED WRITE TRANSFER

MASKED SPLIT WRITE TRANSFER (MSWT)

The MASKED SPLIT WRITE TRANSFER (MSWT) cycle allows serial input data to be transferred to the DRAM without interrupting the serial clock. Operation of the SWT cycle is very similar to the SPLIT READ TRANSFER cycle. It will transfer the idle half of the SAM to the DRAM and set the Tap address to where the new serial data will be loaded in that half. Selection of the MSWT cycle is the same as that of the MASKED WRITE TRANSFER with the exception of the state of DSF. When DSF is HIGH at the falling edge of RAS, an MSWT will occur. The initiation sequence for MSWT is shown in Figure 7. An MSWT will not change the direction of the SAM I/O buffers.

PROGRAMMABLE SPLIT SAM

Programmable Split SAM operation is an extension of the Split SAM mode. This mode optimizes SAM performance by allowing user-programmable stop points to be defined in the split SAM. The stop points define a SAM location at which the access will change from one half of the SAM to the other half (at the loaded Tap address). The locations of the stop points are programmable in power-of-two increments. The stop points and size of the resulting partitions are shown in Figure 8, along with an example.

The stop points are set by performing a CAS-BEFORE-RAS (Reset Stop Addrs) cycle (CBRS). A CBRS cycle is a CAS-BEFORE-RAS with ME/WE LOW and DSF HIGH at

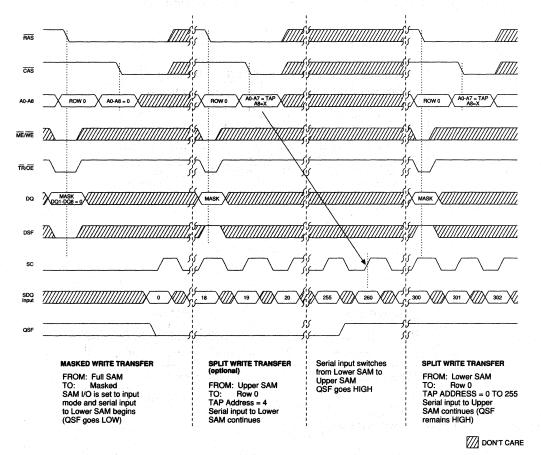


Figure 7
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

the RAS HIGH-to-LOW transition. This is a special CAS-BEFORE-RAS refresh cycle that, in addition to refreshing the DRAM, will sample the address pins (A4-A8) and set the stop point partition to the addressed value (See Figure 8). The programmable stop points will not become valid until a Split Transfer (READ or WRITE) is done, following the CBRS. Both halves of the SAM will be programmed simultaneously to the same partition lengths and stop points.

Access will progress from the Tap address to the end of the programmable partition into which the Tap fell. When the end of the "addressed" partition is reached, the access will jump to the tap address of the next half, provided that a SPLITTRANSFER (READ or WRITE) was done before the partition boundary was reached. If a SPLITTRANSFER (ST) is not done prior to the terminal count of the partition, the

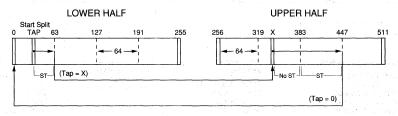
partition is not recognized and the address count will continue in the same half (this is shown Figure 8 at stop address 383). The count will continue in the same half until a SPLIT TRANSFER (READ or WRITE) occurs or the SAM half boundary is reached. In Figure 8, an ST occurs some time between addresses 383 and 447 and the boundary is recognized at 447. The programmable stop points may be reprogrammed at any time by performing another CBRS cycle, the new stop points will not be valid until an ST is performed.

Disabling the Programmable Split SAM requires a CBRR (Reset All Options). This is a CAS-BEFORE-RAS cycle with DSF LOW at the RAS HIGH-to-LOW transition. The CBRR (Reset) will take effect immediately; it does not require an ST to become active valid.

Number Stop	A	ddres	s @ T	AS LO	W	Number and Size
Points/Half	A8	A7	A6	A5	A4	of Partition(s)
1 (Default)	Х	1	1	1	1	1 x 256
2	Х	0	1	1	1.	2 x 128
4	Х	0	0	1	1	4 x 64
8	Х	0	0	0	1	8 x 32
16	Х	0	0	0	0	16 x 16

A0-A3 = "don't care"

EXAMPLE (4 stop points)



Programmed Partition (A4-A8) = 0001111111 MSB....LSB

Figure 8 PROGRAMMABLE SPLIT SAM OPERATION



SERIAL INPUT AND SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUTPUT are SC and \overline{SE} . The rising edge of SC increments the serial address counter and provides access to the next SAM location. \overline{SE} enables or disables the serial input/output buffers.

Serial output of the SAM contents will start at the serial start address that was loaded in the SAM address counter during a READ or SPLIT READ TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 8-bit port. $\overline{\rm SE}$ is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether $\overline{\rm SE}$ is HIGH or LOW. The address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. If an SRT was not performed before the half boundary is reached, the count will progress as illustrated in Figure 5. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the SAM address counter (loaded when the

serial input mode was enabled) will determine the serial address of the first 8-bit word written. \overline{SE} acts as a write enable for serial input data and must be LOW for valid serial input. If \overline{SE} = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the \overline{SE} input.

POWER-UP AND INITIALIZATION

After Vcc is at specified operating conditions, for 100 μ s minimum, eight RAS cycles must be executed to initialize the dynamic memory array. Micron recommends that RAS = (TR)/ $\overline{OE} \ge VIH$ during power-up to ensure that the DRAM I/O pins (DQs) are in a High-Z state. The DRAM array will contain random data, and the nonpersistent MASKED WRITE mode is enabled.

The SAM portion of the MT42C8256 is completely static in operation and does not require refresh or initialization. The SAM port will power-up in the serial input mode (MASKED WRITE TRANSFER) and the I/O pins (SDQs) will be High- Z, regardless of the state of $\overline{\text{SE}}$. QSF initializes in the LOW state. The mask and color register will contain random data after power-up.



TRUTH TABLE

		ì	RAS FALL	ING EDG	E	CAS FALL	A0-	A81	DQ1-	DQ8 ²	REGIS	TERS
CODE	FUNCTION	CAS	TR/OE	ME/WE	DSF	DSF	RAS	CAS	RAS	CAS ³	MASK	COLOR
	DRAM OPERATIONS	·										
CBRR	CAS-BEFORE-RAS REFRESH (RESET ALL OPTIONS)	0.	X	Х	0	_	Х	Х	_	X	Х	X
CBRS	CAS-BEFORE-RAS REFRESH (RESET STOP ADDRESS)	0	Х	0	1		STOP7	х	_	х	Х	X
CBRN	CAS-BEFORE-RAS REFRESH (NO RESET)	0	х	: 1	1	T -	Х	х	_	Х	Х	х
ROR	RAS ONLY REFRESH	1	1	· X	х	_	ROW	_	х		Х	х
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	0	ROW	COLUMN	×	VALID DATA	х	×
RWM	MASKED WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	0	ROW	COLUMN	WRITE MASK ⁴	VALID DATA	USE ⁴	х
BW	BLOCK WRITE TO DRAM	1	1	1	0	1	ROW	COLUMN (A2-A8)	х	COLUMN MASK	х	USE
BWM	MASKED BLOCK WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	0	1	ROW	COLUMN (A2-A8)	WRITE MASK ⁴	COLUMN MASK	USE ⁴	USE
FWM	MASKED FLASH WRITE TO DRAM (OLD OR NEW MASK)	1	1	0	1	Х	ROW	Х	WRITE MASK ⁴	Х	USE ⁴	USE
	REGISTER OPERATIONS											
LMR	LOAD MASK REGISTER	1	1	1	1	0	ROW ⁵	X	×	REG DATA	LOAD	х
LCR	LOAD COLOR REGISTER	1	1	1	1	1	ROW ⁵	X	×	REG DATA	X	LOAD
100	TRANSFER OPERATIONS									No. 1		
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	X	ROW	TAP ⁶	X	X	Х	Х
SRT	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	X	ROW	TAP ⁶	X	X	х	Х
MWT	MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	0	Х	ROW	TAP ⁶	WRITE MASK ⁴	X	USE ⁴	Х
MSWT	MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER) (NEW OR OLD MASK)	1	0	0	-1	×	ROW	TAP ⁶	WRITE MASK ⁴	Х	USE ⁴	X

NOTE:

- 1. These columns show what must be present on the A0-A8 inputs when \overline{RAS} falls and when \overline{CAS} falls.
- 2. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
- 3. During WRITE (including BLOCK WRITE) cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, on READ cycles, the output data is valid after the falling edge of CAS or TR/OE, whichever is later.
- After an LMR cycle, all masked WRITEs use the mask register (old mask). Data on the DQs at RAS falling edge will be ignored. A CBRR will reset to new mask state and mask data must be presented on the DQs at every RAS falling edge.
- 5. The ROW that is addressed will be refreshed, but a ROW address is not required.
- 6. This is the first SAM address location that the first SC cycle will access. For split SAM transfers, the Tap will be the first address location accessed of the "new" SAM half after the boundary of the current half is reached (255 for lower half, 511 for upper half or Programmable Stop Address boundary).
- 7. Defines the column addresses where access moves to the next half, see Programmable Split SAM functional description.



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss-1V to +7V Operating Temperature, T_A (Ambient) 0°C to +70°C Storage Temperature (Plastic)-55°C to +150°C Power Dissipation1W Short Circuit Output Current50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \le T_A \le 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	٧	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V \leq Vin \leq Vcc); all other pins not under test = 0V	lL .	-10	10	μА	
OUTPUT LEAKAGE CURRENT (DQ, SDQ disabled, 0V ≤ Vout ≤ Vcc)	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	
Output Low Voltage (Iout = -2.5mA)	Vol		0.4	V	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	Ci1		,5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SC, SE, DSF	Cı2		8	pF	2
Input/Output Capacitance: DQ, SDQ	Cı/o		9	pF	2
Output Capacitance: QSF	Co		9	pF	2



CURRENT DRAIN, SAM IN STANDBY

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 10\%)$

(O O = 1 A = 70 O, 100 = 01 = 1070)		M/	AX .	1	
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
OPERATING CURRENT (RAS and \overline{CAS} = Cycling: ${}^{t}RC = {}^{t}RC$ (MIN))	lcc1	110	100	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: ^t PC = ^t PC (MIN))	Icc2	85	75	mA	3, 4 26
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = Vih after 8 RAS cycles (MIN))	lcc3	10	10	mA	
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = ViH)	Icc4	110	100	mA	3, 25
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	Icc5	110	100	mA	3, 5
SAM/DRAM DATA TRANSFER	Icc6	115	105	mA	3
CURRENT DRAIN, SAM ACTIVE ([†] SC = MIN)					
$(0^{\circ}\text{C} \le \text{T}_{\text{A}} \le 70^{\circ}\text{C}; \text{Vcc} = 5\text{V} \pm 10\%)$		M	AX		
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES
OPERATING CURRENT (RAS and \overline{CAS} = Cycling: ${}^{t}RC = {}^{t}RC$ (MIN))	Icc7	160	145	mA	3, 4 25
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: ^t PC = ^t PC (MIN))	Icc8	135	120	mA	3, 4 26
				1	

			MAX		A Committee of the Comm	
PARAMETER/CONDITION	SYMBOL	-7	-8	UNITS	NOTES	
OPERATING CURRENT (RAS and CAS = Cycling: ^t RC = ^t RC (MIN))	Icc7	160	145	mA	3, 4 25	
OPERATING CURRENT: FAST PAGE MODE (RAS = VIL; CAS = Cycling: ^t PC = ^t PC (MIN))	Iccs	135	120	mA	3, 4 26	
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles (MIN))	Icc9	50	45	mA	3, 4	
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = VIH)	ICC10	160	145	mA	3, 4 25	
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	Icc11	160	145	mA	3, 4, 5	
SAM/DRAM DATA TRANSFER	ICC12	165	150	mA	3, 4	



DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-7		-8		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	130		150		ns	
READ-MODIFY-WRITE cycle time	^t RWC	175		195		ns	
FAST-PAGE-MODE READ or WRITE	t _{PC}	30		40		ns	
cycle time [Extended Data Out (READ)]							
FAST-PAGE-MODE READ-MODIFY-WRITE	^t PRWC	75		85		ns	
cycle time							
Access time from RAS	tRAC		70		80	ns	14
Access time from CAS	^t CAC		15		20	ns	15, 28
Access time from (TR)/OE	^t OE		15		15	ns	
Access time from column address	t _{AA}		25		35	ns	
Access time from CAS precharge	^t CPA		30		40	ns	350750
RAS pulse width	†RAS	70	20,000	80	20,000	ns	
RAS pulse width (FAST PAGE MODE)	^t RASP	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		ns	
RAS precharge time	tRP	50		60	1	ns	
CAS pulse width	†CAS	15	10,000	20	10,000	ns	
CAS hold time	^t CSH	65		75		ns	
CAS precharge time	[†] CP	10		10		ns	16
RAS to CAS delay time	tRCD	20	50	20	55	ns	17
CAS to RAS precharge time	^t CRP	5		5		ns	
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	^t BAH	10		10		ns	-
RAS to column	t _{RAD}	15	45	15	45	ns	18
address delay time							
Column address setup time	tASC	0		0		ns	
Column address hold time	^t CAH	10	† †	10		ns	
Column address hold time	tAR.	35	+	40	1	ns	
(referenced to RAS)	7					.,0	
Column address to	t _{RAL}	35	++	40		ns	
RAS lead time		-					
Read command setup time	tRCS	0		0		ns	
Read command hold time	^t RCH	0	+-+	. 0		ns	19
(referenced to CAS)							
Read command hold time	¹RRH	0		0		ns	19
(referenced to RAS)		Ŧ					
CAS to output in Low-Z	tCLZ	3	1	3		ns	
CAS HIGH to RAS HIGH lead time	tCRL	0	+-+	0		ns	
RAS HIGH to CAS HIGH lead time	tRCL	0	++	0		ns	
Output buffer turn-off delay from CAS or RAS	tOFF	3	20	3	20	ns	20, 23
Output disable delay from (TR)/OE	dO _t	3	10	3	10	ns	20, 23
Output disable delay from (ME)/WE	tWHZ	3	10	3	10	ns	20, 20
Output disable hold time from start of WRITE	†OEH	10	++	10		ns	27
Output Enable to RAS delay	tORD	0	+	0		ns	
Data output hold after CAS LOW	tCOH	5		5		ns	28

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			-7	-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	tWCS	0		0		ns	21
Write command hold time	¹WCH	15		15		ns	
Write command hold time	^t WCR	50		55		ns].
(referenced to RAS)							
Write command pulse width	tWP	15		15		ns	
Write command to RAS lead time	^t RWL	20		20		ns	
Write command to CAS lead time	^t CWL	15		20		ns	
Data-in setup time	^t DS	0		0		ns	22
Data-in hold time	t _{DH}	10		15		ns	22
Data-in hold time	t _{DHR}	50		-55		ns	
(referenced to RAS)			1	1			1
RAS to WE delay time	^t RWD	90		100		ns	21
Column address	t _{AWD}	45		55		ns	21
to WE delay time						1	
CAS to WE delay time	tCWD	35		40		ns	21
Transition time (rise or fall)	t _T	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF		8		8	ms	
RAS to CAS precharge time	^t RPC	0		0		ns	
CAS setup time	[†] CSR	10		10		ns	5
(CAS-BEFORE-RAS REFRESH)						} .	1
CAS hold time	^t CHR	15		15		ns	5
(CAS-BEFORE-RAS REFRESH)							
ME/WE to RAS setup time	^t WSR	0		0		ns	
ME/WE to RAS hold time	^t RWH	10		15		ns	
Mask data to RAS setup time	tMS	0		0		ns	
Mask data to RAS hold time	tMH	10		15		ns	1



TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS			7	-8		1.5	<u> </u>
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTE
TR/(OE) LOW to RAS setup time	^t TLS	0		0	y'' '	ns	1. 12
TR/(OE) LOW to RAS hold time	^t TLH	10	10,000	15	10,000	ns	
TR/(OE) LOW to RAS hold time (REAL-TIME READ-TRANSFER only)	^t RTH	55	10,000	65	10,000	ns	- 10 - 10
TR/(OE) LOW to CAS hold time (REAL-TIME READ-TRANSFER only)	^t CTH	20	7. (°.*	20	1.2	ns	2.7
TR/(OE) HIGH to RAS precharge time	tTRP	50		60		ns	
TR/(OE) precharge time	tTRW	25		25	†	ns	
TR/(OE) HIGH to SC lead time	tTSL	5		5	1	ns	
First SC edge to TR/(OE) HIGH delay time	^t TSD	15		15		ns	
Serial output buffer turn-off delay from RAS	^t SDZ	10	30	10	35	ns	
SC to RAS setup time	tSRS	20		25		ns	
Serial data input to SE delay time	tSZE	0		0,	1	ns	
Serial data input delay from RAS	tSDD	40		45	-	ns	
Serial data input to RAS delay time	tSZS	0		0	1	ns	
Serial-input-mode enable (SE) to RAS setup time	^t ESR	0		0	1 11 11 13	ns	
Serial-input-mode enable (SE) to RAS hold time	^t REH	10		15		ns	512.71
TR/(OE) HIGH to RAS setup time	tYS	0		0	1.5	ns	
TR/(OE) HIGH to RAS hold time	tYH	10		15		ns	
DSF to RAS setup time	tFSR	0		0		ns	
DSF to RAS hold time	^t RFH	10		15		ns	
SC to QSF delay time	tSQD		18		25	ns	
SPLIT TRANSFER setup time	tSTS	25		30	1	ns	
SPLIT TRANSFER hold time	tSTH	0		0		ns	
DSF (at CAS LOW) to RAS hold time	^t FHR	50		55		ns	
DSF to CAS setup time	†FSC	0		0	1	ns	
DSF to CAS hold time	^t CFH	15		15		ns	1.4
TR/OE to QSF delay time	†TQD	7.	20		25	ns	
RAS to QSF delay time	tRQD		55		65	ns	1 1,000
CAS to QSF delay time	tCQD		25		35	ns	100000
RAS to first SC delay	tRSD	70		80		ns	
CAS to first SC delay	tCSD	25		30	-	ns	

SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 10%)

AC CHARACTERISTICS		-7		-8		1 72	
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	tSC	18		25		ns	
Access time from SC	tSAC		15		20	ns	24, 28
SC precharge time (SC LOW time)	^t SP	5		10		ns	
SC pulse width (SC HIGH time)	tSAS	5		10		ns	
Access time from SE	tSEA		12		15	ns	24
SE precharge time	tSEP.	10		10		ns	
SE pulse width	tSE.	10		10		ns	
Serial data-out hold time after SC high	tSOH	5		5		ns	24, 28
Serial output buffer turn-off delay from SE	†SEZ	3	10	3	12	ns	20, 24
Serial data-in setup time	tSDS	3		3		ns	
Serial data-in hold time	tSDH	5		5		ns	
Serial input (Write) Enable setup time	tsws	0		0		ns	
Serial input (Write) Enable hold time	tSWH	10		10		ns	
Serial input (Write) disable setup time	tswis	0		0		ns	
Serial input (Write) disable hold time	tSWIH	10		10		ns	

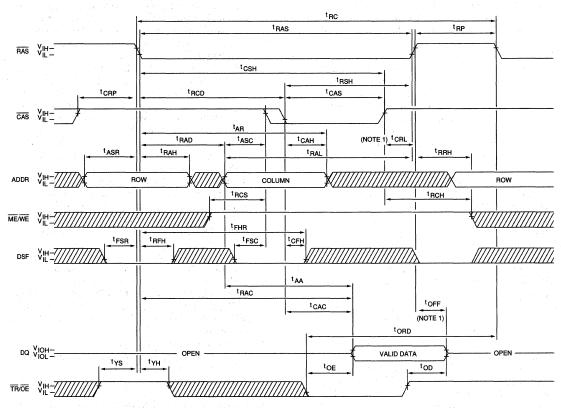


NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 10\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- AC characteristics assume ^tT = 5ns.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition from 0 to 3V for AC testing.
- In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
- 11. If $\overline{\text{CAS}} = \text{Vih}$, DRAM data output (DQ1-DQ8) is High-Z.
- 12. If CAS = VIL, DRAM data output (DQ1-DQ8) may contain data from the last valid READ cycle.
- 13. DRAM output timing measured with a load equivalent to 1 TTL gates and 50pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCP.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.

- 19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
- 20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (VoH -200mV, VoL +200mV). This parameter is sampled and not 100% tested.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \leq$ tWCS (MIN), the cycle is a LATE-WRITE and TR/OE must control the output buffers during the WRITE to avoid data contention. If ^tRWD ≥ ^tRWD (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate, but the WRITE will be valid if ^tOD and ^tOEH are met. See the LATE-WRITE AC Timing diagram.
- These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and ME/WE leading edge in LATE-WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE HIGH or when RAS and CAS go HIGH, whichever occurs first
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. Address (A0-A8) may be changed two times or less while $\overline{RAS} = V\pi$.
- 26. Address (A0-A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 27. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if CAS remains LOW and OE is taken LOW after ^tOEH is met. If CAS and RAS go HIGH prior to OE going back LOW, the DQs will remain open.
- 28. ^tSAC/^tCAC are MAX at 70° C and 4.5V Vcc; ^tSOH/
 ^tCOH are MIN at 0° C and 5.5V Vcc. These limits will
 not occur simultaneously at any given voltage or
 temperature. This is guaranteed by design (^tSOH/
 ^tCOH = ^tSAC/^tCAC output transition time).

DRAM READ CYCLE 1 (Outputs controlled by RAS)



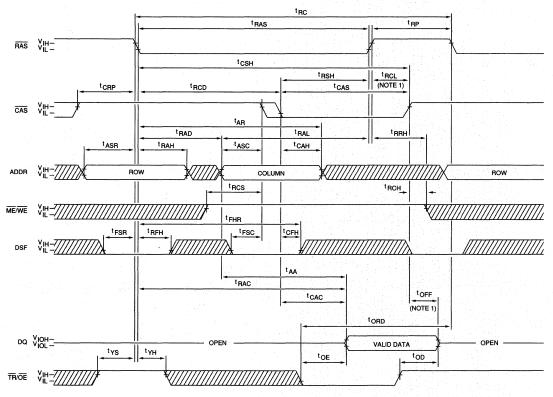
DON'T CARE

₩ UNDEFINED

NOTE: 1. [†]CRL is a reference parameter. If \overline{CAS} = HIGH [†]CRL before \overline{RAS} , [†]OFF is referenced from the rising edge of \overline{RAS} .



DRAM READ CYCLE 1 (Outputs controlled by CAS)



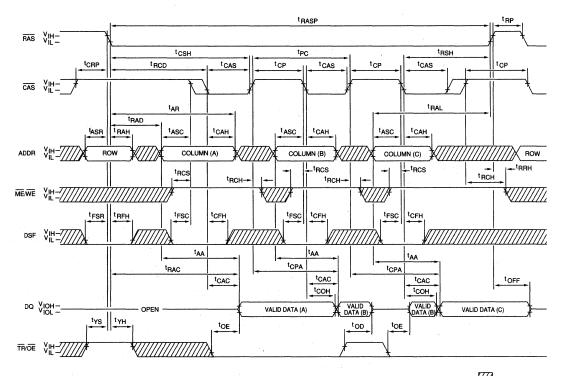
DON'T CARE

₩ undefined

NOTE: 1. ¹RCL is a reference parameter. If RAS = HIGH ¹RCL before CAS, ¹OFF is referenced from the rising edge of CAS.

DRAM FAST-PAGE-MODE READ CYCLE

(Extended Data Out)



DON'T CARE

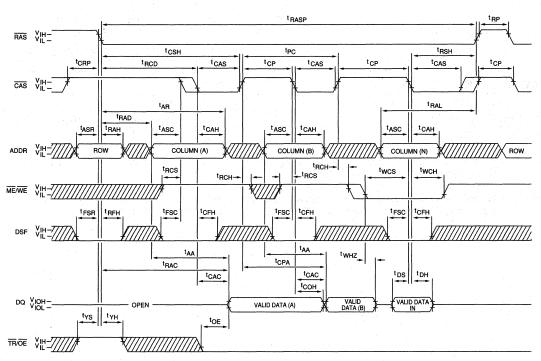
W UNDEFINED

NOTE: WRITE cycles or READ-MODIFY-WRITE cycles may be mixed with READ cycles while in FAST PAGE MODE.



DRAM FAST-PAGE-MODE READ/WRITE CYCLE

(Extended Data Out)



DON'T CARE

W UNDEFINED



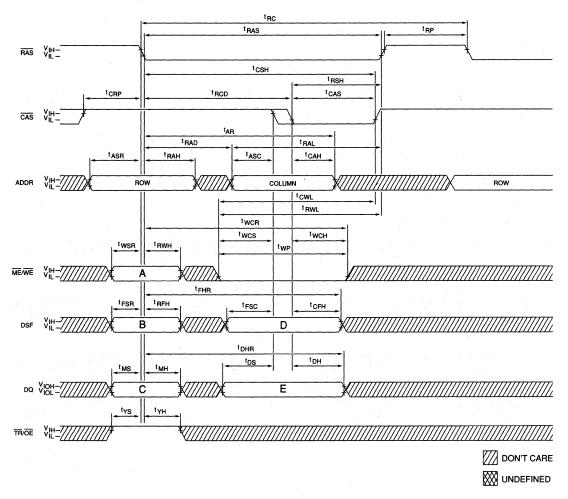
WRITE CYCLE FUNCTION TABLE 1

	LOGIC STATES						
		RAS Fal	ling Edge	CAS Falling Edge			
FUNCTION	A ME/WE	B DSF	C DQ (Input)	D DSF	E ² DQ (Input)		
Normal DRAM WRITE	1	0	X	0	DRAM Data		
MASKED WRITE to DRAM	0	0	Write Mask ³	0	DRAM Data (Masked)		
BLOCK WRITE to DRAM (No Bit-Plane Mask)	1	0	X	1	Column Mask		
MASKED BLOCK WRITE to DRAM	0	0	Write Mask ³	1	Column Mask		
MASKED FLASH WRITE to DRAM	0	1	Write Mask ³	Х	X		
Load Mask Data Register	1	1	X	0	Write Mask Data		
Load Color Register	1	1	X	1	Color Data		

NOTE:

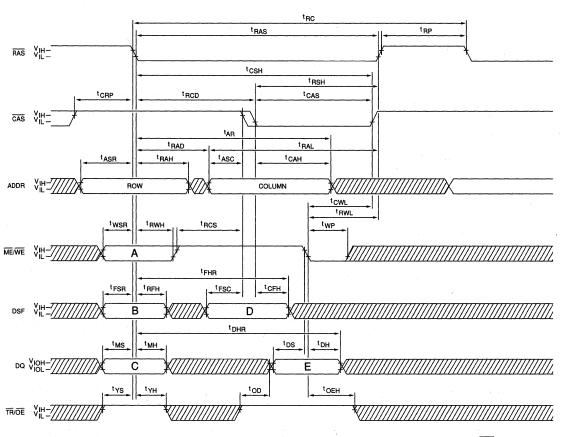
- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for the WRITE cycle timing diagrams on the following pages.
- 2. CAS or ME/WE falling edge, whichever occurs later.
- 3. Mask Data is loaded at RAS falling if nonpersistent mode is active. If persistent mode is active, mask data is supplied by the Mask Data Register and the DQs are "don't care" at the RAS falling edge.

DRAM EARLY-WRITE CYCLE 1



OTE: 1. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM LATE-WRITE CYCLE



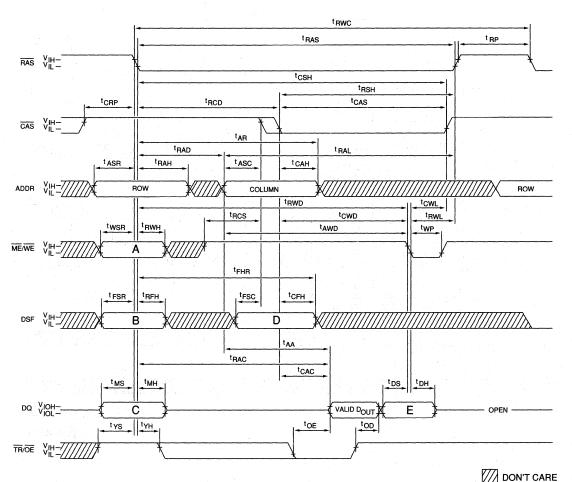
DON'T CARE

₩ UNDEFINED

NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.



DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)

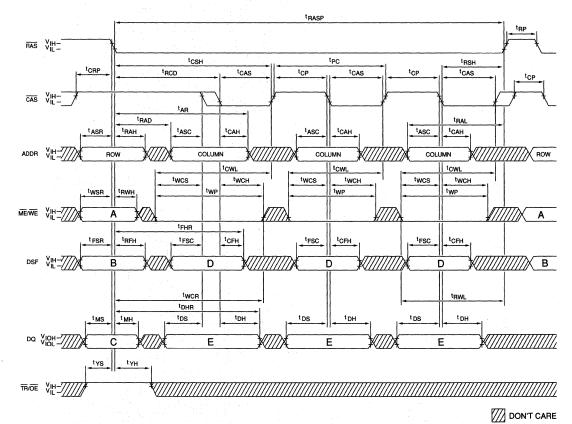


NOTE: The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

W UNDEFINED

NEW **M** MULTIPORT DRAM

DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE 1,2



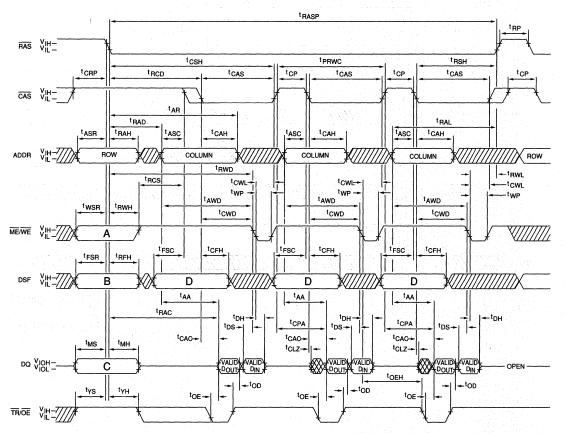
NOTE:

- READ cycles or READ-MODIFY-WRITE cycles can be mixed with WRITE cycles while in FAST PAGE MODE.
- 2. The logic states of "A", "B", "C", "D" and "E" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

W UNDEFINED



DRAM FAST-PAGE-MODE READ-WRITE CYCLE 1,2 (READ-MODIFY-WRITE OR LATE-WRITE CYCLES)



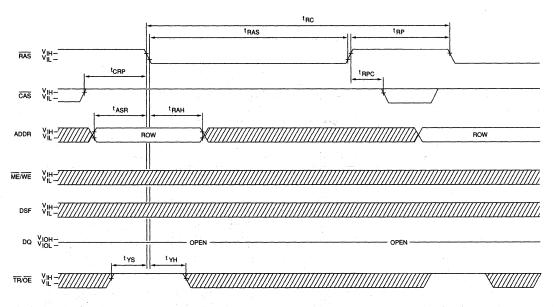
DON'T CARE

₩ UNDEFINED

NOTE:

- READ or WRITE cycles can be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use
 the Write Function Table to determine the proper DSF state for the desired WRITE operation.
- The logic states of "A", "B", "C" and "D" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)



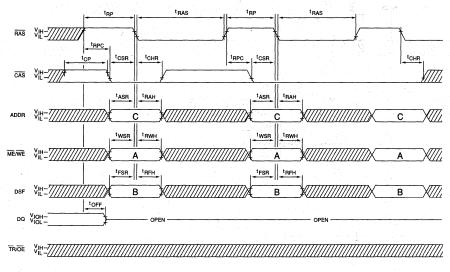
DON'T CARE

₩ undefined

CAS-BEFORE-RAS CYCLE FUNCTION TABLE

		LOGIC STATES RAS Falling Edge (CAS = LOW)			
FUNCTION	CODE	A ME/WE	B DSF	C A0-A8	
CAS-BEFORE-RAS REFRESH (Reset All Options)	CBRR	Х	0	Χ	
CAS-BEFORE-RAS REFRESH (Set/Reset Stop Address)	CBRS	0	1	STOP ADDRESS ¹	
CAS-BEFORE-RAS REFRESH (No Reset)	CBRN	1	1	Χ	

CAS-BEFORE-RAS REFRESH CYCLE²



DON'T CARE

₩ UNDEFINED

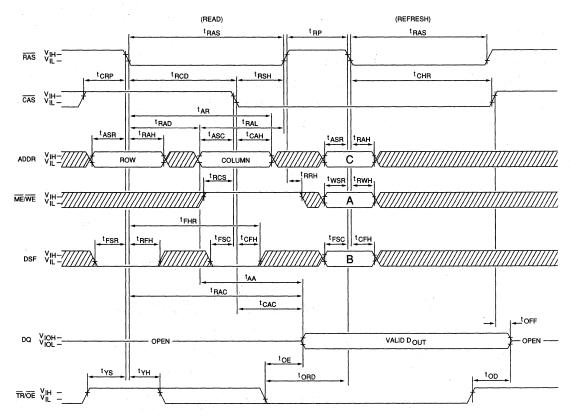
NOTE: 1. Programmable Stop Point column addresses:

Number Stop	A	ddres	s @ R	Number and Size		
Points/Half	A8	A7	A6	A5	A4	of Partition(s)
1 (Default)	Х	1	1	1	1	1 x 256
2	Х	0	1	1	1	2 x 128
4	Х	0	0	1	1	4 x 64
8	Х	0	0	0	1	8 x 32
16	X	0	0	0	0	16 x 16

A0-A3 = "don't care"

The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

DRAM HIDDEN-REFRESH CYCLE 1,2



DON'T CARE

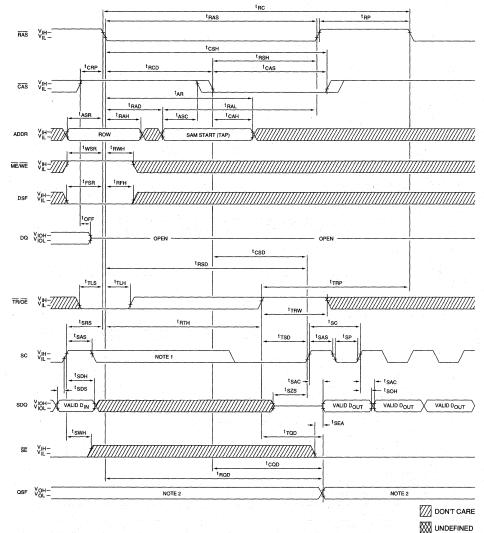
W UNDEFINED

NOTE:

- 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In this case ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.
- The logic states of "A", "B" and "C" determine the type of CBR operation performed. See the CBR Cycle Function Table for a detailed description.

READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode, or SC idle)

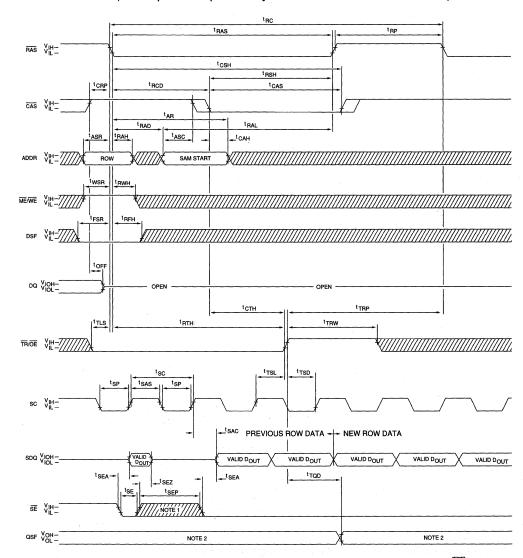


NOTE:

- 1. There must be no rising edges on the SC input during this time period.
- 2. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.
- 3. If tTLH is timing for the TR/(OE) rising edge, the transfer is self-timed and the tCSD and tRSD times must be met. If ^tRTH is timing for the TR/(OE) rising edge, the transfer is done off of the TR/(OE) rising edge and ^tTSD must be met.

REAL-TIME READ TRANSFER (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:

The SE pulse is shown to illustrate the SERIAL OUTPUT ENABLE and DISABLE timing. It is not required.

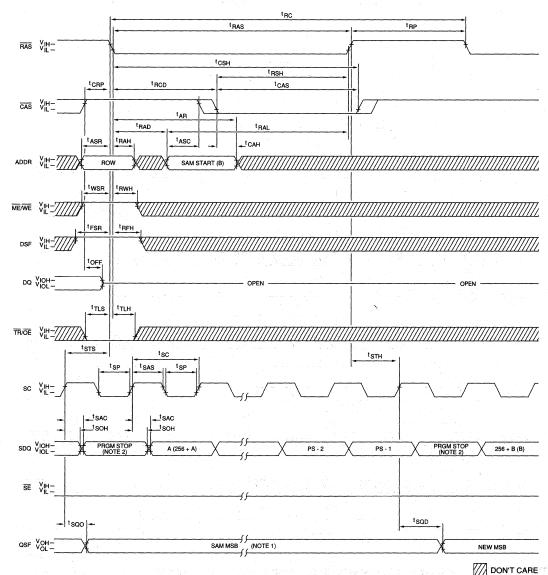
QSF = 0 when the Lower SAM (bits 0-255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256-511) is being accessed.

DON'T CARE





SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)



IOTE:

1. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

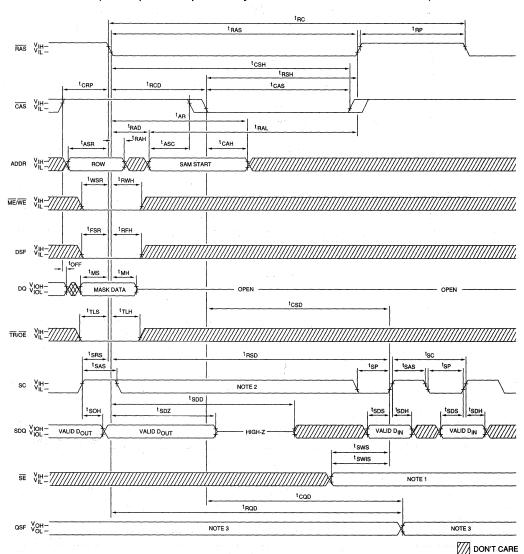
₩ UNDEFINED

Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functional description for detail.



MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)



NOTE:

1. SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.

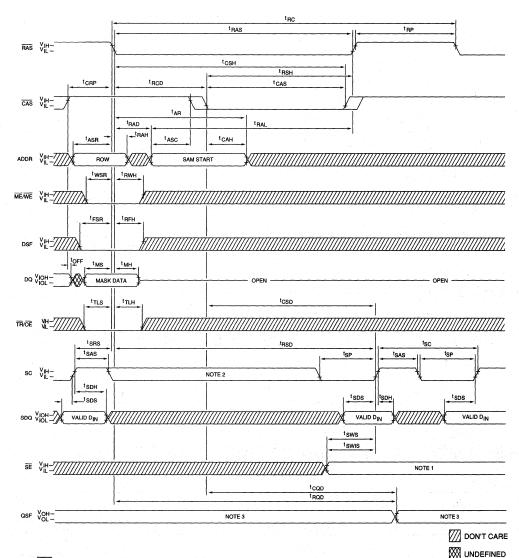
W UNDEFINED

- 2. There must be no rising edges on the SC input during this time period.
- 3. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.



MASKED WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

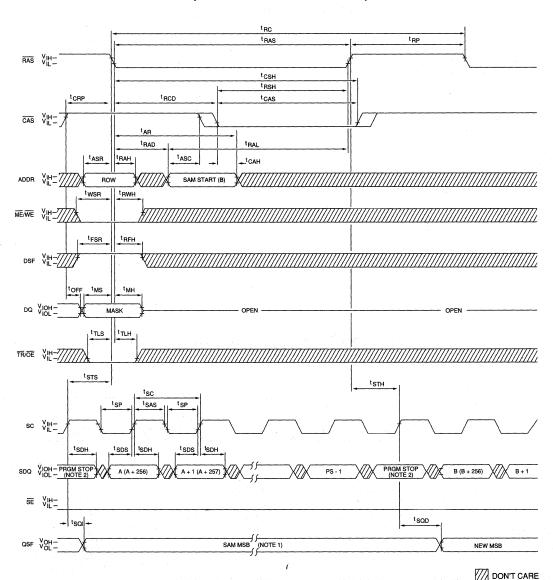
(When part was previously in the SERIAL INPUT mode)



IOTE:

- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 2. There must be no rising edges on the SC input during this time period.
- QSF = 0 when the Lower SAM (bits 0-255) is being accessed.
 QSF = 1 when the Upper SAM (bits 255-511) is being accessed.

MASKED SPLIT WRITE TRANSFER (SAM-TO-DRAM TRANSFER)

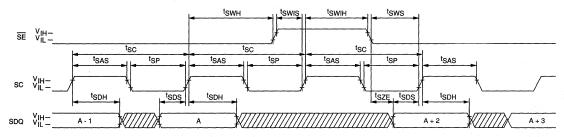


NOTE:

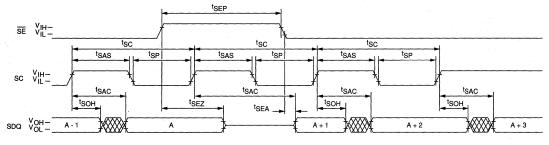
- 1. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
- 2. Programmable stop address or SAM half boundary (255 or 511). See the Programmable Split SAM functiona description for detail.

₩ undefined

SAM SERIAL INPUT



SAM SERIAL OUTPUT



DON'T CARE

₩ undefined

MULTIPORT DRAN

VRAM

256K x 16 DRAM **WITH 512 x 16 SAM**

FEATURES

- Industry standard pinout, timing, and functions
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Inputs and outputs are fully TTL compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh within 32ms
- FAST PAGE MODE access with Extended Data Out
- Upper and lower byte WE control
- Dual port organization: 256K x 16 DRAM port 512 x 16 SAM port
- No refresh required for serial access memory
- Low power: 10mW standby; 350mW active, typical
- Fast access times 60ns random, 15ns serial

SPECIAL FUNCTIONS

- JEDEC Standard Mandatory Function set plus
- PERSISTENT MASKED WRITE
- 4 or 8 COLUMN BLOCK WRITE (MASK)
- MASKED FLASH WRITE
- MASKED WRITE TRANSFER/SERIAL INPUT
- MASKED SPLIT WRITE TRANSFER
- PROGRAMMABLE SPLIT SAM

OPTIONS

MARKING

Timing [DRAM, SAM	I (c	ycle	e/a	access)]	
60ns, 18/15ns					-6
70ns, 25/20ns					-7
80ns, 30/25ns					-8

Packages

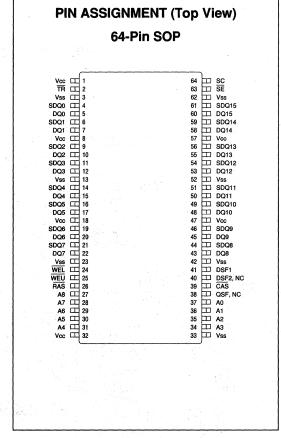
Plastic SOP (550 mil)

SG

GENERAL DESCRIPTION

The MT42C256K16A1 is a high speed, dual port CMOS dynamic random access memory, or video RAM (VRAM) containing 4,194,304 bits. These bits may be accessed by an 16-bit wide DRAM port or by a 512 x 16 bit serial access memory (SAM) port. Data may be transferred bidirectionally between the DRAM and the SAM.

The DRAM portion of the VRAM is functionally identical to the MT4C4256 (256K x 4-bit DRAM), with the addition of MASKED WRITE, BLOCK WRITE and FLASH WRITE. Sixteen 512-bit data registers make up the serial access memory portion of the VRAM. Data I/O and internal data



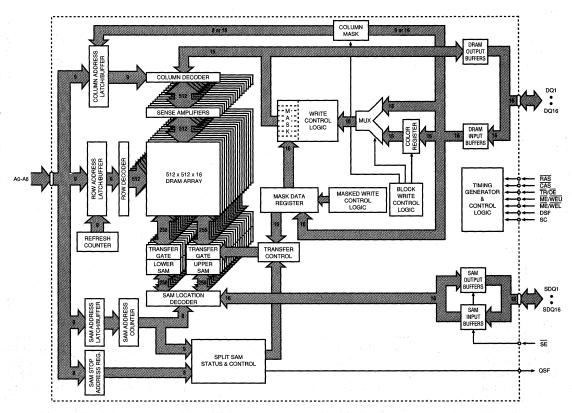
transfer are accomplished using three separate bidirectional data paths: the 16-bit random access I/O port, the 16 internal 512 bit wide paths between the DRAM and the SAM, and the 16-bit serial I/O port for the SAM. The rest of the circuitry consists of the control, timing, and address decoding logic.

Each of the ports may be operated asynchronously and independently of the other except when data is being transferred internally between them. As with all DRAMs, the VRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 32ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and the SAM counts as a refresh cycle. The SAM portion of the VRAM is fully static and does not require any refresh.

The operation and control of the MT42C256K16A1 are optimized for high performance graphics and communica-

tion designs. The dual port architecture is well suited to buffering the sequential data types used in raster graphics display, serial, parallel networking and data communications. Special features such as SPLIT READ TRANSFER, Extended Data Out and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



MULTIPORT DRAN

TRIPLE PORT **DRAM**

256K x 4 DRAM WITH DUAL 512 x 4 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAM
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- Low power: 15mW standby; 500mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAM and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ and WRITE TRANSFERS
- **BLOCK WRITE**
- BIT MASKED TRANSFERS

OPTIONS

MARKING

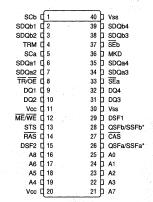
- Timing [DRAM, SAMs (cycle/access)] 80ns, 28ns/25ns 100ns, 30ns/27ns -10
- Packages Plastic SOI (400 mil) DI Plastic TSOP (400 mil) TG
- Functionality QSF output MT43C4257 (indicates SAM-half accessed) SSF input MT43C4258 (Split SAM special function, stop count)

GENERAL DESCRIPTION

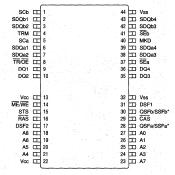
The MT43C4257/8 are high speed, triple port CMOS lynamic random access memories (TPDRAMs) containing ,048,576 bits. Data may be accessed by a 4 bit wide DRAM ort or by either of two independently-clocked 512 x 4-bit erial access memory (SAM) ports. Data may be transferred idirectionally between the DRAM and either SAM.

PIN ASSIGNMENT (Top View) 40-Pin SOJ

(Q-6)



40/44-Pin TSOP** (R-5)



*MT43C4257/MT43C4258 **Consult factory for TSOP availability.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4 DRAM). Eight 512-bit data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 4-bit random access I/O port, the pair of internal 2,048 bit wide paths between the DRAM and the SAMs, and the pair of 4-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing and address decoding logic.

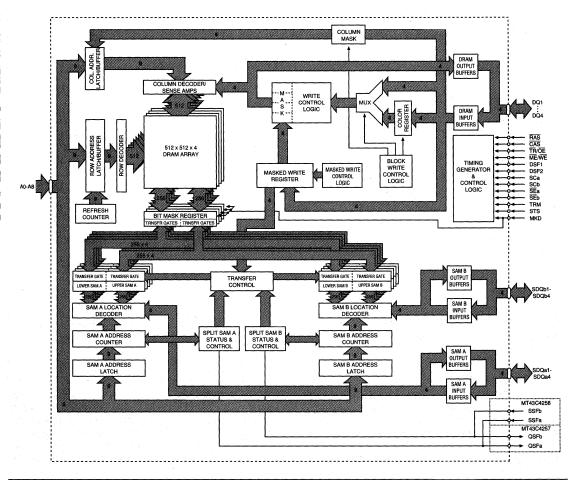
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512 x 4-bit Bit Mask Data register can be parallel loaded from the DRAM or either SAM, or serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all \overline{RAS} addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require refresh.

The operation and control of the MT43C4257/8 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in raster graphics display, serial/parallel networking and data communications. Special features such as SPLIT READ TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

SOJ PIN Numbers	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5	5	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
8	8	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of RAS, or
				Output Enable: Enables the DRAM output buffers when taken LOW after \overline{RAS} goes LOW (\overline{CAS} must also be LOW), otherwise the output buffers are in a high impedance state.
12	14	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or
				Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
33	37	SEa	Input	Serial Port Enable SAMa: SEa enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEa is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
37	41	SEb	Input	Serial Port Enable, SAMb: SEb enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEb is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
29	31	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
15	17	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
14	16	RAS	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits and as a strobe for control and data inputs.
27	29	CAS	Input	Column Address Strobe: CAS is used to clock-in the 9 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe control and data inputs.



PIN DESCRIPTIONS (continued)

SOJ PIN	TSOP PIN			
NUMBERS	NUMBERS	SYMBOL	TYPE	DESCRIPTION
25, 24, 23, 22, 19, 18, 17, 21, 16	27, 26, 25, 24, 21, 20, 19, 23, 18	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by \overline{RAS} and \overline{CAS} to select one 4-bit word out of the 256K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when \overline{RAS} goes LOW) and the SAM start address (when \overline{CAS} goes LOW).
13	15	STS	Input	SAM Transfer Select: The state of STS at RAS time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
36	40	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at RAS), then MKD is used as mask data input and is clocked by SCb into the mask data register.
4	4	TRM	Input	Transfer Mask Select: TRM is used to select between NORMAL TRANSFER cycles and BIT MASKED TRANSFER or BIT MASK REGISTER LOAD cycles.
9, 10, 31, 32	9, 10, 35, 36	DQ1-DQ4	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memory array; inputs for the MASK and COLOR REGISTER load cycles; address mask inputs for BLOCK WRITE cycles.
6, 7, 34, 35	6, 7, 38, 39	SDQa1-SDQa4	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 38, 39	2, 3, 42, 43	SDQb1-SDQb4	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
26	28	QSFa/SSFa	Output	Split SAM Status, SAMa (MT43C4257): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH).
			Input	Split SAM Special Function, SAMa (MT43C4258): SSFa = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
28	30	QSFb/SSFb	Output	Split SAM Status, SAMb (MT43C4257): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH).
			Input	Split SAM Special Function, SAMb (MT43C4258): SSFb = HIGH stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
11, 20	13, 22	Vcc	Supply	Power Supply: +5V ±5%
30, 40	32, 44	Vss	Supply	Ground



FUNCTIONAL DESCRIPTION

The MT43C4257/8 may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note:

For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/\overline{OE}$ in references to transfer operations.

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C4257/8 TPDRAM must be refreshed to retain data. All 512 row address combinations must be accessed within 8ms. The MT43C4257/8 support $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, $\overline{\text{RAS}}$ ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the rowaddresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 CAS-BEFORE-RAS cycles within

the 8ms time period.

For \overline{RAS} -ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the \overline{RAS} -ONLY and \overline{CAS} -BEFORE- \overline{RAS} cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling RAS (while keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS REFRESH cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C4257/8 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on his device, several conditions that were undefined or "don't

care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 18 address bits used to select a 4-bit word from the 262,144 available are latched into the chip using the A0-A8, \overline{RAS} , and \overline{CAS} inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when \overline{RAS} transitions from HIGH-to-LOW. Next, the 9 column-address bits are set up on the address inputs and clocked-in when \overline{CAS} goes from HIGH-to-LOW.

Note:

RAS also acts as a "master" chip enable for the TPDRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.

For single port DRAMS, the \overline{OE} pin is a "don't care" when \overline{RAS} goes LOW. For the TPDRAM, $\overline{TR}/(\overline{OE})$ is used when \overline{RAS} goes LOW to select between DRAM and TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition for all DRAM operations.

If (ME)/WE is HIGH when CAS goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ4 port. The (TR)/OE input must transition from HIGH-to-LOW some time after RAS falls to enable the DRAM output port.

For single port DRAMs, WE is a "don't care" when RAS goes LOW. For the TPDRAM, ME/(WE) is used, when RAS goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If ME/(WE) is LOW at the RAS HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), ME/(WE) must be HIGH at the RAS HIGH-to-LOW transition. If (ME)/WE is LOW when CAS goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ4 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

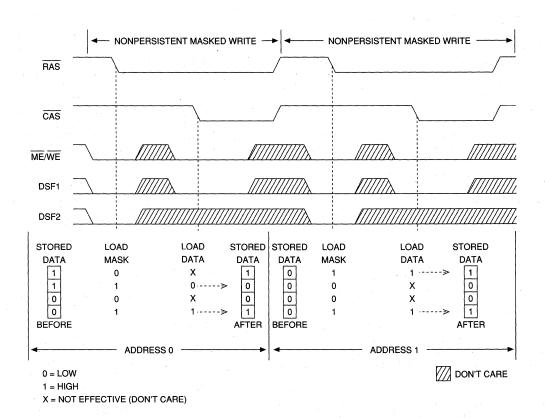


Figure 1
NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within a 4-bit word. The MT43C4257/8 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If $\overline{\text{ME}}/(\overline{\text{WE}})$, DSF1 and DSF2 are LOW at the $\overline{\text{RAS}}$ HIGH- to-LOW transition, the data (mask data) present on the DQ1-DQ4 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the four DQ1-DQ4 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This

convention is used for all masks on the MT43C4257/8. Note that $\overline{\text{CAS}}$ is still HIGH. When $\overline{\text{CAS}}$ or $\overline{\text{(ME)}}/\overline{\text{WE}}$ go LOW, the bits present on the DQ1-DQ4 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of $\overline{\text{RAS}}$. FAST PAGE MODE can be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one $\overline{\text{RAS}}$ cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 1.

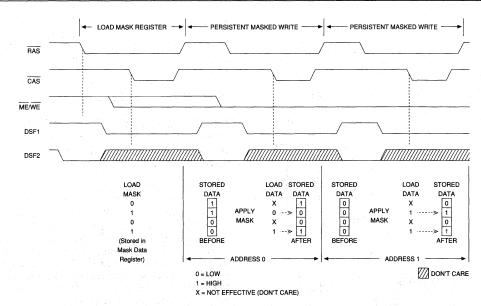


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{\text{RAS}}$ goes LOW. The mask data is loaded into the internal register when $\overline{\text{CAS}}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

PERSISTENT MASKED WRITE cycles may then be performed by taking ME/(WE) and DSF2 LOW and DSF1 HIGH when RAS goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when RAS falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycleoperations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at RAS time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

The MT43C4257/8 will perform a BLOCK WRITE cycle if DSF1 is HIGH when $\overline{\text{CAS}}$ goes LOW. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 16 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when \overline{CAS} goes LOW, only the A2-A8 inputs are used. A2-A8 specify the "block" (out of the 128 possible) of four adjacent column locations that will be accessed. When the later of $\overline{ME}/\overline{WE}$ and \overline{CAS} go LOW, the DQ inputs are latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

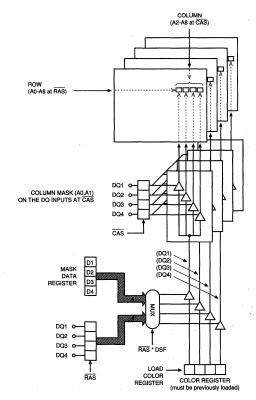


Figure 3
BLOCK WRITE EXAMPLE

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPERSISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{\text{ME}}/\overline{\text{WE}}$) LOW and DSF1 LOW when $\overline{\text{RAS}}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when $\overline{\text{CAS}}$ goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the four column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when $\overline{\text{CAS}}$ goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C4257/8 contains two 4-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when \overline{RAS} goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when \overline{RAS} goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when \overline{CAS} goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note:

For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSIS-TENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the four DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when CAS goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGISTER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.



TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note:

The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.

TRANSFER operations are initiated when $\overline{\text{TR}}/(\overline{\text{OE}})$ is LOW at the falling edge of $\overline{\text{RAS}}$. The state of STS when $\overline{\text{RAS}}$ goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{\text{ME}})/\overline{\text{WE}}$ when $\overline{\text{RAS}}$ goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping $\overline{\text{CAS}}$. In this case, the previously loaded Tap address will be used.

The MT43C4257/8 include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a transfer operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of RAS.

NORMAL TRANSFERS

The MT43C4257/8 support all of the popular transfer cycles available on the 1 Meg Video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{\text{ME}})/\overline{\text{WE}}$ is HIGH, and DSF1 and $\overline{\text{TR}}/(\overline{\text{OE}})$ are LOW when $\overline{\text{RAS}}$ goes LOW. When $\overline{\text{RAS}}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the four 512-bit DRAM rows that are to be transferred to the four SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM data registers. QSF indicates the SAM half being accessed; LOW

if the lower half, HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAM's I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while RAS and CAS are LOW. In order to synchronize the REAL-TIME READ TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of CAS. The transfer will be completed internally by the device. The first serial clock must meet the tRSD and tCSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 9-bit Tap address register is loaded into the address counter. If SE for the SAM selected (SEa for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. SE enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer can occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of \overline{RAS} and \overline{CAS} . The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (non-split) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT can be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when RAS goes LOW during the TRANSFER cycle. As in non-split transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that receives the transfer. When CAS falls, address pins A0-

A7 determine the Tap address for the SAM-half selected; A8 = "don't care." If CAS does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional and need only be done if the Tap for the upper half $\neq 0$. For the MT43C4257, serial access continues and when the SAM address counter reaches 255 ("A8" = 1, A0-A7 = 0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went

LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. \overline{CAS} is used to load the Tap address. If \overline{CAS} does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C4258. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (255; lower, 511; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–255) is being accessed. QSF = 1 when the Upper SAM (bits 256–511) is being accessed.

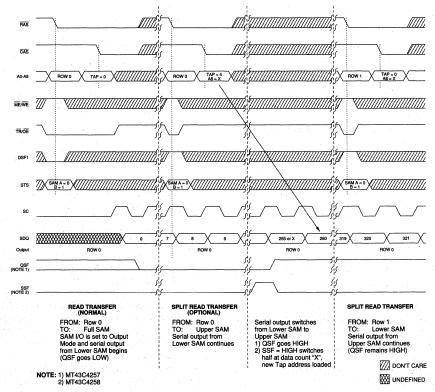


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE



WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except $(\overline{ME})/\overline{WE}$ and \overline{SE} must be LOW when \overline{RAS} goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STSpin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when \overline{RAS} goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the \$\overline{SE}\$ of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DO MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the four DQ planes (see Figure 5). The MWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of RAS.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The DQ MASKED SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANS-FER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately

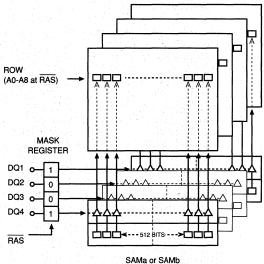


Figure 5
DQ MASKED WRITE TRANSFER

transferred to the first destination row. This half of the SAM may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all four of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, it is only needed if the Tap for the upper half is $\neq 0$.

Write mask data must be supplied to the DQ inputs during every MSWT cycle at RAS time. The mask data acts as an individual write enable for each of the four DRAM DQ planes. For example, DO1, at RAS time, during a MASKED WRITE enables or disables the transfer of the SAM SDQ1 register to the DO1 plane of the DRAM row selected (see the DQ MASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANS-FER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A7) for the other half is loaded when CAS falls (A8 is a "don't care"). If \overline{CAS} does not fall, the previously loaded Tap address, A0-A7, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

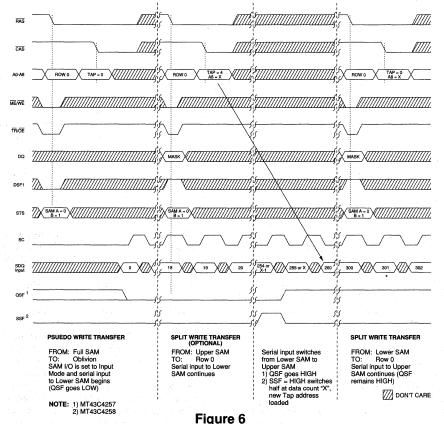
The QSFa and QSFb outputs (MT43C4257) indicate which half of SAMa or SAMb, respectively, is currently accepting data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

MICRON

When operating the MT43C4258 in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (255 or 511). If SSF is HIGH at SC before an MSWT is performed for the next half the access will jump to the old Tap address of the same half. Access will not proceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C4257.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUT-PUT are SCa,b, SEa,b and SSFa,b (MT43C4258). The rising edge of SC increments the serial address counter and provides access to the next SAM location. SE enables or disables the serial input/output buffers.



TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE

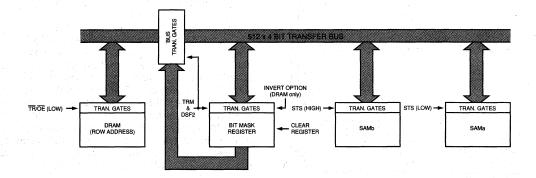


Figure 7 BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial tap address that was loaded in the SAMa, b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC input increments the address counter and presents the contents of the next SAM location to the 4-bit port. SE is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether SE is HIGH or LOW. For the MT43C4257, the address progresses through the SAM and will wrap around (after count 255 or 511) to the Tap address of the next half, for split modes. Address count will wrap around (after count 511) to Tap address 0 if in the "full" SAM modes.

For the 43C4258, the address count will wrap as it does for the MT43C4257 or it may be triggered, at will, to the next half by the SSF input (split SAM modes). If SSF is HIGH at a LOW-to-HIGH transition of SC, the Tap address of the next half will be loaded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address of the new half.

SC is also used to clock-in data when the device is in the serial input mode. As in the serial output operation, the contents of the serial address counter (loaded when the serial input mode was enabled) will determine the serial address of the first 4-bit word written. SE acts as a write enable for serial input data and must be LOW for valid serial input. If \overline{SE} = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address counter is incremented with every LOW-to-HIGH transition of SC, regardless of the logic level on the $\overline{\text{SE}}$ input. The operation of SSF (MT43C4258) is the same as described for serial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONs, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 512 x 4 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW, BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

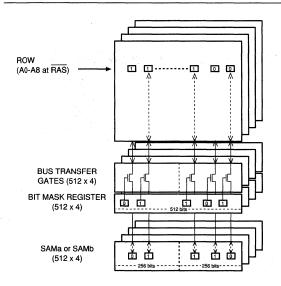


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH to select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when RAS falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when RAS falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at RAS time. If a DQ input is LOW at RAS time, none of the 256 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 256 SAM bits for that row half will be masked by the corresponding 256 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the BMR by using the BMR READ TRANSFER function. When RAS falls, TR/(OE) is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when \overline{RAS} falls selects whether the serial mask input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when \overline{RAS} falls to disable SMI or HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMR (SMI enabled) or is "don't care" (SMI disabled). The MKD input is tied to the 4 bit-planes, the data on the MKD pin is written to each bit plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at \overline{RAS} time the DRAM data will be inverted before being written to the BMR. All 2,048 bits involved in the transfer will be complemented. The functionality and logic levels for the other control inputs are identical to the BMR READ TRANSFER cycle. Note that



MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. ($\overline{\text{ME}}$)/ $\overline{\text{WE}}$ and DSF2 are LOW and TRM is HIGH when $\overline{\text{RAS}}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQbit-plane mask when $\overline{\text{RAS}}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{\text{RAS}}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at RAS time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. $(\overline{ME})/\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when RAS falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, he SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI node will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide iny particular ROW address at RAS time. However, whichever ROW address is present at RAS time will be used is the address for a RAS-ONLY REFRESH. Since a SAM is nvolved in the transfer, a new SAM starting address (or [ap] will be loaded at CAS time. This address will be loaded nto the serial address counter of the SAM selected by STS t RAS time.

Vote:

Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.

IMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of ne SAM registers. The $(\overline{ME})/\overline{WE}$ input is used to indicate

the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAM TRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when CAS falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at \overline{RAS} time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/(\overline{OE})$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are HIGH when \overline{RAS} falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANS-FERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at \overline{RAS} time the serial mask input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when \overline{RAS} falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all four of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at RAS time to enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the

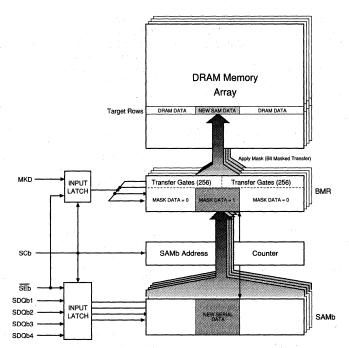


Figure 9 SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

BMR. For every address location to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all four planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear only half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa

TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms, the device must be initialized.

After Vcc is at specified operating conditions, for 100µs (minimum), eight RAS cycles must be executed to initialize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of (TR)/OE. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power-up in the serial input mode (WRITE TRANSFERS) and the SAM I/O pins (SDQs) are in a High-Z state, regardless of the state of SE ab. Also, SPLIT TRANSFER and SM modes are disabled. Both QSF (MT43C4257) outputs may be in the HIGH or LOW state. The SAMs, as well as the bit mask, color, and DRAM mask registers all contain random data after power-up.



TRUTH TABLE 1

				RA	S FAL	LING	EDGE				CAS FALL	AO	-A82	DQ1-	DQ4³	REGIS	STERS
CODE	FUNCTION	CAS	TR/ OE	ME/WE 10	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE 4	MASK	COLOR
	DRAM OPERATIONS						·	-					1.677	W	-		-
CBR	CAS-BEFORE-RAS REFRESH	0	х	111	X	X	Х	х	х	X	х	X	X	X	Х		T = "
ROR	RAS-ONLY REFRESH	1	1	х	х	Х	X	х	Х	х	_	ROW	T -	X	-	_	T =
RW	NORMAL DRAM READ OR WRITE	1	1	1	0	011	х	х	х	×	0	ROW	COLUMN	×	VALID DATA	_	-
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	011	X	Х	X	х	0	ROW	COLUMN	WRITE MASK	VALID DATA	LOAD & USE	-
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	011	х	Х	X	X	0	ROW	COLUMN	×	VALID DATA	USE	-
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	011	X	X	Х	х	1	ROW	COLUMN (A2-A8)	х	COLUMN MASK	-	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	011	х	Х	X	x	1	ROW	COLUMN (A2-A8)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	11	011	х	Х	х	Х	1	ROW	COLUMN (A2-A8)	х	COLUMN MASK	USE	USE
	REGISTER OPERATIONS																
LMR	LOAD MASK REGISTER	1	1	1	1	011	Х	х	Х	X	0	X ⁵	X	X.	WRITE MASK	LOAD	=
LCR	LOAD COLOR REGISTER	1	1	1	1	011	х	Х	Х	х	1	X ⁵	Х	X	COLOR DATA	-	LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	х	0	Х	0=SAMa 1=SAMb	х	ROW	TAP ⁶	X	х	-	[-
SRT ⁹	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1 1	1	0	х	0	Х	0=SAMa 1=SAMb	х	ROW	TAP ⁶	х	х	_	_
WT .	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0 :	х	0=SAMa 1=SAMb	х	ROW	TAP ⁶	Х	3., X	a 1 —	-
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	X	0=SAMa 1=SAMb	х	X ⁵	TAP ⁶	×	х	-	-
MSWT ⁹	SPLIT WRITE TRANSFER (SPLIT SAM- TO-DRAM TRANSFER WITH DQ MASK)	1	0	0	1	0	х	0	X	0=SAMa 1=SAMb	х	ROW	TAP ⁶	DQ MASK	х	1 -	-
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	1	Х	0	х	0=SAMa 1=SAMb	х	ROW	TAP ⁶	DQ MASK	х	_	-



TRUTH TABLE 1

				RA	S FAL	LING	EDGE			:	CAS FALL	A0-	A82	DQ1-	DQ4 ³	REGIS	TERS
CODE	FUNCTION	CAS	TR/ OE	ME/WE 10	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS	RAS	CAS,WE 4	MASK	COLOR
	BIT MASK REGISTER OPERATIONS	-			-												
BMR- RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	1	0	0	х	1 .	0/1 ⁷	0	х	ROW	х	X	X	_	_
BMR- IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	х	1	0/1 ⁷	1	x	ROW	х	х	X	_	_
BMR- WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	1	0	0	0	0	х	1	0/1 ⁷	0	Х	ROW	Х	DQ MASK	X	-	_
BMR- IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1 .	0	0	0	0	х	1	0/17	1	x	ROW	х	DQ MASK	х	- :	_
SAM- BMR	SAM→BMR TRANSFER	1	0	0	. 1	0	Х	1	0/17	0=SAMa 1=SAMb		X ⁵	TAP ⁶	x	Х	-	-
BMR- SAM	BMR→SAM TRANSFER	1	0	1	. 1	0	X	1	0/17	0=SAMa 1=SAMb		X ⁵	TAP ⁶	×	Х	- .	-
CLR- BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	×	0	0/17	×	х	X ⁵	X	×	X	-	-
	BIT MASKED TRANSFER OPERATIONS				1.5							-					
BMRT	BIT MASKED READ TRANSFER (BM DRAM→SAM TRANSFER)	1	0	1	0	1	×	1	х	0=SAMa 1=SAMb		ROW	TAP ⁶	х	Х	. –	_
BMSRT ⁹	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	. 1	X	1	×	0=SAMa 1=SAMb		ROW	TAP ⁶	×	х		-
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	×	1	X ⁸	0=SAMa 1=SAMb		ROW	TAP ⁶	×	х	-	-
BMSWT ⁹	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM→DRAM TRANSFER)	1	0	0	1	1	×	1	Χ ⁸	0=SAMa 1=SAMb		ROW	TAP ⁶	DQ MASK	х		

- 1. 0 = LOW (VIL), 1 = HIGH (VIH), X = "don't care," = "not applicable."
- 2. These columns show what must be present on the A0-A8 inputs when \overline{RAS} falls and when \overline{CAS} falls.
- 3. These columns show what must be present on the DQ1-DQ4 inputs when \overline{RAS} falls and when \overline{CAS} falls.
- With WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of CAS or TR/OE, whichever is
- 5. The ROW that is addressed will be refreshed, but no particular ROW address is required.
- 6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer. Column address A8 is a "don't care" for SPLIT TRANSFERs.
- 7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
- 8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
- SPLIT TRANSFERs 9.do not change SAM I/O direction.
- 10. SAM I/O direction is a function of the state of ME/WE at RAS time. If ME/WE is LOW, then the selected SAM is an input; if ME/WE is HIGH, then the SAM is an output (except for SPLIT TRANSFERs).
- 11. The MT43C4257/8 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.



ABSOLUTE MAXIMUM RATINGS*

 $\label{eq:Voltage} \begin{tabular}{lll} Voltage on Vcc Supply Relative to Vss & --1V to +7V \\ Operating Temperature, T_A (Ambient) & --0°C to +70°C \\ Storage Temperature (Plastic) & --55°C to +150°C \\ Power Dissipation & --55°C to +150°C \\ Power Dissipation & --50°C \\ Power Circuit Output Current & --50°C \\ \end{tabular}$

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_{\Delta} \leq 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	٧	1

DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le T_{\Delta} \le 70^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V \leq Vin \leq Vcc); all other pins not under test = 0V	IL.	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc).	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Journ 2 5mg CDCs) Fm A cil other outputs)	Vон	2.4		V	
Output High Voltage (Iout = -2.5mA, SDQs; -5mA all other outputs) Output Low Voltage (Iout = 2.5mA, SDQs; 5mA all other outputs)	Vol		0.4	ν	

CAPACITANCE

 $(T_A = 25^{\circ}C)$

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD	C _{l1}		5	pF	2
Input Capacitance: RAS, CAS, ME/WE, TR/OE, SCa,b, SEa,b, DSF1,2, STS SSFa,b	C ₁₂		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	Cı/o		9	pF	2
Output Capacitance: QSFa,b	Co		9	pF	2

TSOP THERMAL CONSIDERATIONS (preliminary)

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Thermal resistance - Junction to Ambient	øJA	85	°C/W	
Thermal resistance - Junction to Case	øJC	15	°C/W	
Maximum Case Temperature	TC	110	°C	

DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 5\%)$

(0 0 5 1 A 5 7 0 0, VCC = 5 V ±5 78)		M	AX		
PARAMETER/CONDITION	SYMBOL	-8	-10	UNITS	NOTES
OPERATING CURRENT (RAS and \overline{CAS} = Cycling; ${}^{t}RC = {}^{t}RC$ (MIN))	lcc ₁	100	90	mA	3, 4 25
OPERATING CURRENT: PAGE MODE (RAS = V _{IL} CAS = Cycling; ^t PC = ^t PC (MIN))	Icc2	95	85	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$, after 8 \overline{RAS} cycles (MIN))	Іссз	10	10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS = CAS = Vcc-0.2V, after 8 RAS cycles min). All other inputs ≥ Vcc -0.2V or ≤ Vss +0.2V	Icc4	2	2	mA	3 °
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = VIH)	lcc5	105	95	mA	3, 26
REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling)	Icc6	105	95	mA	3, 5 26
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	Icc7	100	90	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 5%) PARAMETER/CONDITION SYMBOL -8 -10 U

PARAMETER/CONDITION	SYMBOL	-8	-10	UNITS	NOTES
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; ^t SC = ^t SC (MIN); SEa/SEb = V _{IL})	Iccs	40	35	mA	. 1.
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^t SC = ^t SC (MIN); SEb = V _{IL})	Icc9	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = ViH or VIL; SEa/SEb = ViH)	Icc10	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = ViH or Vil.; SEb = ViH)	Icc11	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 5%)

ICC(TOTAL)	= DRAM CURRENT (Icc1-7) + SAMa CURRENT (Icc8 or Icc10) + SAMb CURRENT (Icc8 or Icc10) +
	SMI CURRENT (Icce or Icc11) [+ 10mA (If DRAM CURRENT = Icc3 or Icc4)]

Example 1:

Operating current (-8) with DRAM operating in Fast Page Mode, SAMa active, SAMb and SMI inactive:

ICC(TOTAL)	= DRAM CURRENT (Icc2) + SAMa CURRENT (Icc8) + SAMb CURRENT (Icc10) +	
	SMI CURRENT (Icc11) [+ 0]	
	= 95 + 40 + 0 + 0 = 135mA (MAX)	4,154

Example 2:

Operating current (-10) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

ICC(TOTAL)	= DRAM CURRENT (Icc4) + SAMa CURR	ENT (Iccs) + SAMb CURF	RENT (Iccs)	+	
	SMI CURRENT (Icce) [+ 10]				7 (1991)
	= 2 + 35 + 35 + 20 + 10 = 102mA (MAX)				



DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 5 %)

AC CHARACTERISTICS			-8		-10		
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC tRC	150		180		ns	1600
READ-MODIFY-WRITE cycle time	^t RWC	205		235		ns	3.30
FAST-PAGE-MODE READ or WRITE	^t PC	50		60		ns	yar e
cycle time					2.7		
FAST-PAGE-MODE READ-MODIFY-	^t PRWC	95		120		ns	
WRITE cycle time						La jaran a	
Access time from RAS	tRAC		80	1 8	100	ns	14, 17
Access time from CAS	^t CAC		20		25	ns	15
Access time from (TR)/OE	^t OE		20		25	ns	14.5
Access time from column address	^t AA		40		50	ns	
Access time from CAS precharge	^t CPA		45		55	ns	7 - 3 - 5
RAS pulse width	^t RAS	80	20,000	100	20,000	ns	194.15
RAS pulse width (FAST PAGE MODE)	^t RASP	80	100,000	100	100,000	ns	
RAS hold time	tRSH	20		25		ns	
RAS precharge time	t _{RP}	60		70		ns	
CAS pulse width	^t CAS	20	10,000	25	10,000	ns	
CAS hold time	^t CSH	80		100		ns	
CAS precharge time	[†] CP	10		10		ns	16
RAS to CAS delay time	tRCD	20	60	25	75	ns	17
CAS to RAS precharge time	tCRP	5		5		ns	3757
Row address setup time	tASR	0	7.2	0		ns	
Row address hold time	^t RAH	12		15		ns	
RAS to column	†RAD	17	40	20	50	ns	18
address delay time							W Bay
Column address setup time	tASC	0		0	1 - 5 - 5	ns	3.41.1
Column address hold time	^t CAH	15		20	1	ns	a Jahan
Column address hold time	t _{AR}	60		70		ns	
(referenced to RAS)							
Column address to	†RAL	40		50		ns	
RAS lead time							
Read command setup time	tRCS	0		0		ns	
Read command hold time	tRCH	0		0		ns	19
(referenced to CAS)			1				
Read command hold time	tRRH	0		0	1	ns	19
(referenced to RAS)							
CAS to output in Low-Z	CLZ	3	1	3		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	ns	20, 23
Output disable	tOD	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	tOEH	15		15	 -	ns	28
Output Enable to RAS delay	tORD	0		0	 	ns	



DRAM TIMING PARAMETERS (continued) ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-	8	-10		1	
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	twcs	0		0		ns	21
Write command hold time	^t WCH	15		20		ns	
Write command hold time (referenced to RAS)	^t WCR	60		75		ns	
Write command pulse width	tWP	15		15		ns	
Write command to RAS lead time	tRWL	20		25		ns	
Write command to CAS lead time	tCWL	20		25		ns	
Data-in setup time	^t DS	0		0		ns	22
Data-in hold time	tDH	15		20		ns	22
Data-in hold time (referenced to RAS)	^t DHR	55		70		ns	
RAS to WE delay time	tRWD	100		130		ns	21
Column address to WE delay time	tAWD	60		80		ns	21
CAS to WE delay time	tCWD	40		55		ns	21
Transition time (rise or fall)	ŀΤ	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF		8		8	ms	
RAS to CAS precharge time	^t RPC	0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	†CSR	10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	30		30		ns	5
ME/WE to RAS setup time	†WSR	0		0		ns	
ME/WE to RAS hold time	tRWH	15		15		ns	
Mask data to RAS setup time	tMS	0		0		ns	
Mask data to RAS hold time	tMH	15		15		ns	



TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS			-8	-10			100
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
TR/(OE) LOW to RAS setup time	^t TLS	0		0		ns	
TR/(OE) LOW to RAS hold time	[†] TLH	15	10,000	15	10,000	ns	10.00
TR/(OE) LOW to RAS hold time (REAL-TIME READ TRANSFER only)	^t RTH	70	10,000	80	10,000	ns	
TR/(OE) LOW to CAS hold time (REAL-TIME READ TRANSFER only)	^t CTH	20		25		ns	
TR/(OE) HIGH to SC lead time	^t TSL	5		5		ns	11.0
TR/(OE) HIGH to RAS precharge time	^t TRP	60		70	200	ns	100
TR/(OE) precharge time	tTRW	25		30		ns	
First SC edge to TR/(OE) HIGH delay time	[†] TSD	15		15	10.35	ns	1 224
RAS to first SC edge delay time	tRSD	80	1	95		ns	
CAS to first SC edge delay time	†CSD	25		30	1000	ns	3, 1, 13,
Serial output buffer turn-off delay from RAS	†SDZ	10	50	10	50	ns	1000
SC to RAS setup time	tSRS	30		30	: maias lasti	ns	
Serial data input to SE delay time	†SZE	0		0	167 7560	ns	
RAS to SD buffer turn on time	tSRO	10		15		ns	
Serial data input delay from RAS	tSDD	60		60		ns	Part Margaret
Serial data input to RAS delay time	tSZS	0		0		ns	12.55
Serial-Input-Mode enable (SE) to RAS setup time	tESR	0		0		ns	
Serial-Input-Mode enable (SE) to RAS hold time	tREH.	15		15		ns	
TR/(OE) HIGH to RAS setup time	tYS	0		0		ns	
TR/(OE) HIGH to RAS hold time	tYH	15		15		ns	10.00
DSF, TRM, STS, MKD to RAS setup time	tFSR	0		0	40 4 100	ns	
DSF, TRM, STS, MKD to RAS hold time	†RFH	15		15	1 2 2 3	ns	
DSF to RAS hold time	†FHR	60		65	tanat s	ns	100
DSF to CAS setup time	tFSC	0		0		ns	
DSF to CAS hold time	[†] CFH	15		20	1	ns	
SC to QSF delay time	tSQD		35		40	ns	29
RAS to QSF delay time	†RQD		65	-	85	ns	29
CAS to QSF delay time	tCQD		35		40	ns	29
TR/OE to QSF delay time	[†] TQD		25		30	ns	29
SPLIT TRANSFER setup time	tSTS	30	+	35		ns	29
SPLIT TRANSFER hold time	^t STH	0		0		ns	29



SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-8		-10		1	I
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	tsc	28	†	30		ns	
Access time from SC	†SAC		25		27	ns	24, 31
SC precharge time (SC LOW time)	tSP	10		10		ns	
SC pulse width (SC HIGH time)	^t SAS	10		10		ns	
Access time from SE	^t SEA		15		20	ns	24
SE precharge time	†SEP	10		15		ns	
SE pulse width	tSE.	10		15		ns	
Serial data out hold time after SC HIGH	tSOH	5		5		ns	24, 31
Serial output buffer turn off delay from SE	†SEZ	3	12	3	15	ns	20, 24
Serial data in setup time	tSDS	0		0		ns	24
Serial data in hold time	†SDH	10		10		ns	24
Serial mask data in setup time	†MDS	0		0		ns	
Serial mask data in hold time	^t MDH	10	T	10		ns	
SERIAL INPUT (Write) Enable setup time	tsws	0		0		ns	
SERIAL INPUT (Write) Enable hold time	tswH	15		15		ns	
SERIAL INPUT (Write) disable setup time	tswis	0		0	1 h	ns	
SERIAL INPUT (Write) disable hold time	tSWIH	15		15		ns	
SSF to SC setup time	tSFS	0		0		ns	30
SSF to SC hold time	^t SFH	15		20		ns	30
SSF LOW to SC HIGH delay	†SFD	5		5		ns	30

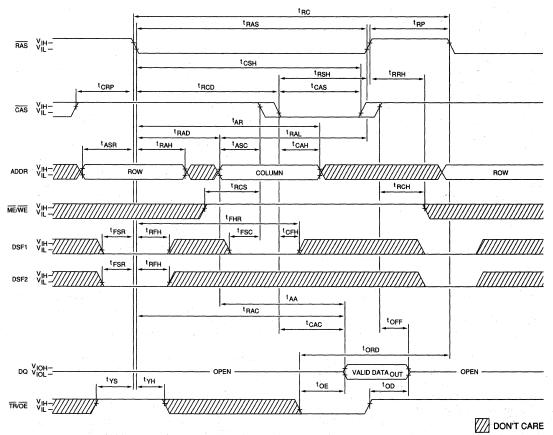


NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 5\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition between 0V and 3V for AC testing.
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If $\overline{\text{CAS}}$ = V_{IH}, DRAM data outputs (DQ1-DQ4) is High-Z.
- 12. If $\overline{\text{CAS}} = V_{IL}$, DRAM data outputs (DQ1-DQ4) may contain data from the last valid READ cycle.
- 13. DRAM output timing measured with a load equivalent to 2 TTL gates and 100pF. Output reference levels: VoH = 2.0V; VoL = 0.8V.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCP.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- 9. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

- 20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (VoH -200mV, Vol +200mV). This parameter is sampled and not 100% tested.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \leq$ tWCS (MIN), the cycle is a LATE-WRITE and TR/OE must control the output buffers during the WRITE to avoid data contention. If tRWD ≥ tRWD (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate but the WRITE will be valid, if tOD and tOEH are met. See the LATE-WRITE AC Timing diagram.
- These parameters are referenced to CAS leading edge in early WRITE cycles and ME/WE leading edge in late WRITE or READ-WRITE cycles.
- During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE or CAS, whichever goes HIGH first.
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. Addresses (A0-A8) change two times or less while $\overline{RAS} = V_{IL}$.
- 26. Addresses (A0-A8) change once or less while $\overline{RAS} = V_{IL}$.
- 27. Addresses (A0-A8) change once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met (\$\overline{OE}\$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if \$\overline{CAS}\$ remains LOW and \$\overline{OE}\$ is taken LOW after ^tOEH is met. If \$\overline{CAS}\$ goes HIGH prior to \$\overline{OE}\$ going back LOW, the DQs will remain open.
- 29. Applies to the MT43C4257 only.
- 30. Applies to the MT43C4258 only.
- 31. 'SAC is MAX at 70° C and 4.75V Vcc; 'SOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature. 'SOH = 'SAC output transition time, this is guaranteed by design.

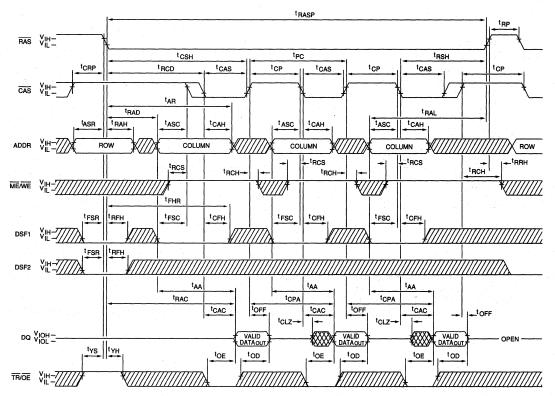
DRAM READ CYCLE



₩ undefined



DRAM FAST-PAGE-MODE READ CYCLE



DON'T CARE

W UNDEFINED

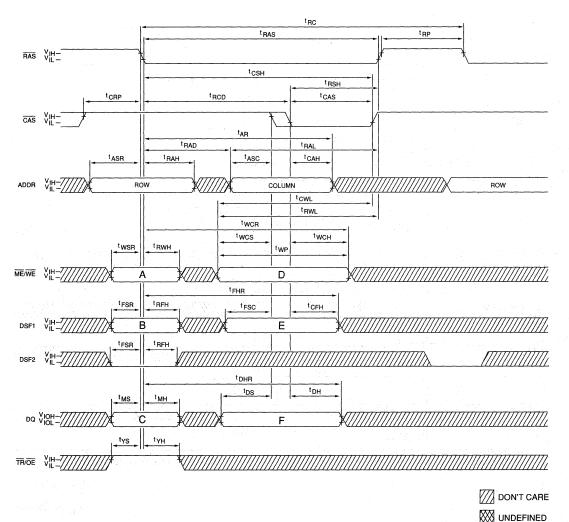
WRITE CYCLE FUNCTION TABLE 1

		LOGIC STATES ²								
			RAS Falling	g Edge	CAS Falling Edge					
CODE	FUNCTION	A ME/WE	B DSF1	C DQ (input)	D ME/WE	E DSF1	F DQ (Input)			
RW	Normal DRAM WRITE	1	0	X	0	0	DRAM			
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/1 ³	0	DRAM (Masked)			
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	Х	0/13	0	DRAM (Masked)			
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	Х	0/1 ³	1	Column Mask			
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1 ³	1	Column Mask			
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	Х	0/1 ³	1	Column Mask			
LMR	Load Mask Data Register	1	1	Х	0/1 ³	0	Write Mask			
LCR	Load Color Register	1	1	Х	0/1 ³	1	Color Mask			

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
- 2. TRM, MKD and STS are "don't care" for all WRITE cycles.
- 3. If ME/WE is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if ME/WE falls after CAS.

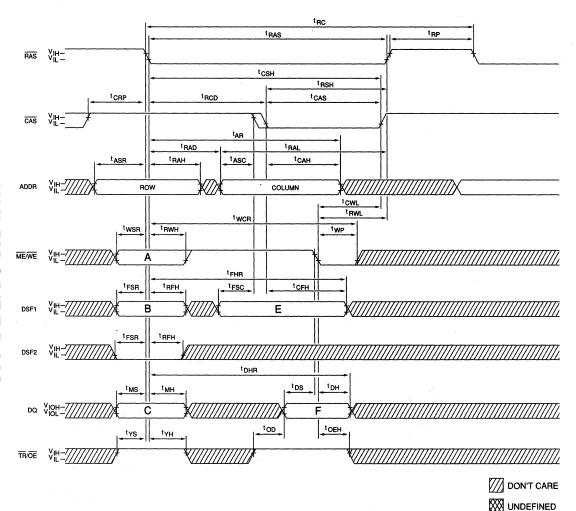


DRAM EARLY-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

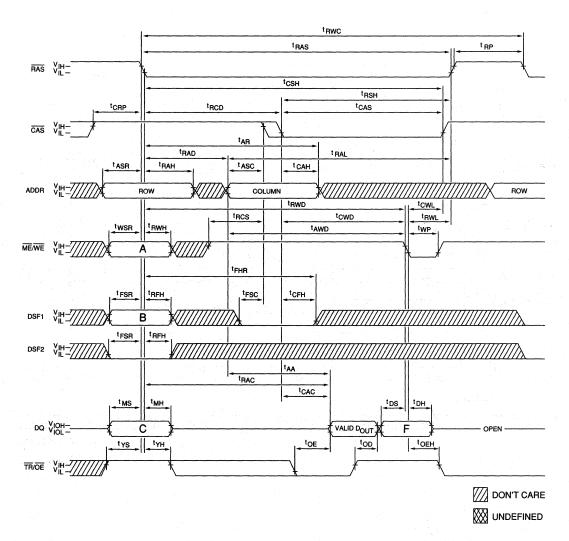
DRAM LATE-WRITE CYCLE 1



NOTE: 1. The logic states of "A", "B", "C", "E", and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

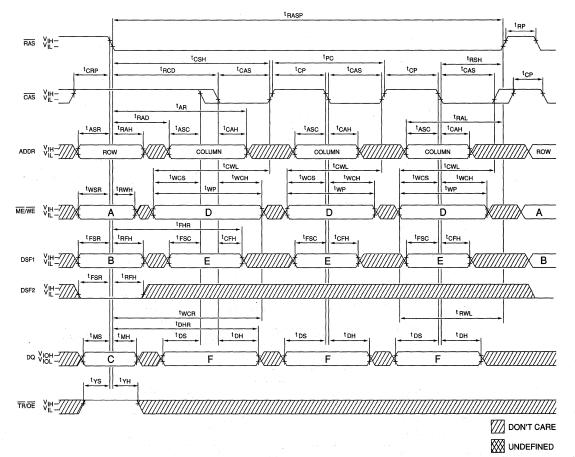


DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

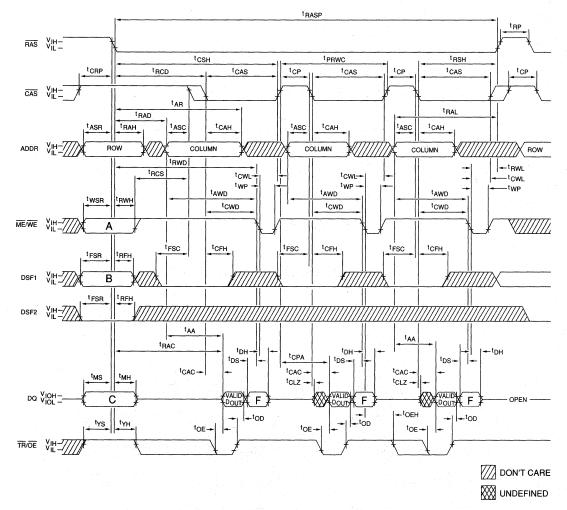
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE 1, 2



- READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST PAGE MODE.
- The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

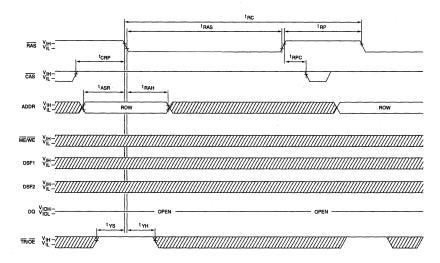
MULTIPORT DRAN

DRAM FAST-PAGE-MODE READ-WRITE CYCLE(READ-MODIFY-WRITE or LATE-WRITE CYCLES)

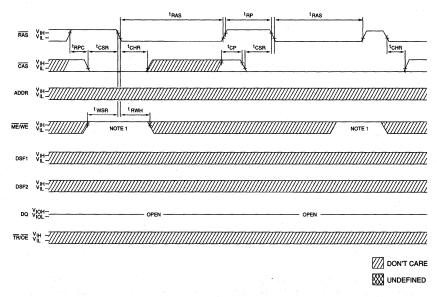


- READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use
 the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
- The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)

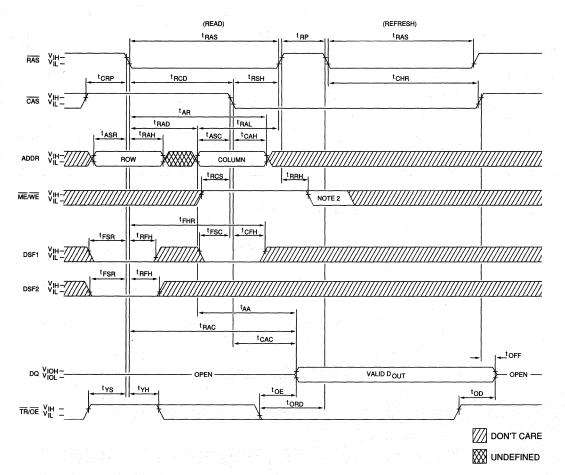


CAS-BEFORE-RAS REFRESH CYCLE



NOTE: 1. The MT43C4257/8 operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.

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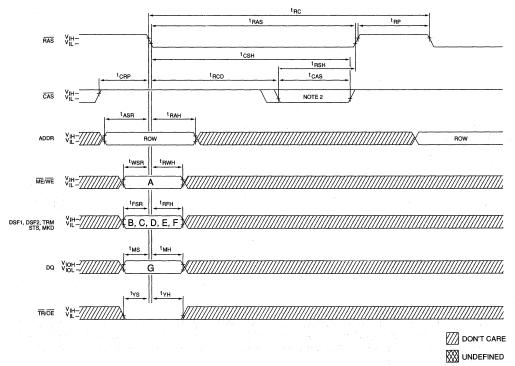
- A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH and the DQ pins stay High-Z. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.
- 2. The MT43C4257/8 operates with this state as "don't care," but to allow for future functional enhancements, it is recommended that they be driven as illustrated for system upgradability.



DRAM/BMR TRANSFER CYCLE FUNCTION TABLE 1

		LOGIC STATES RAS Falling Edge									
CODE	CODE FUNCTION	A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)			
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/11	Х			
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	. 1	0/11	Х			
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/11	Mask			
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	0	1	1	0/11	Mask			
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	Х	0/11	Х			

DRAM/BMR TRANSFERS



NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.



READ TRANSFER CYCLE FUNCTION TABLE 1

			LO:	GIC STATES					
		RAS Falling Edge							
CODE	FUNCTION	A DSF1	B DSF2	C TRM	D STS	E MKD			
RW	READ TRANSFER	0	0	0	0/12	Х			
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/12	Х			
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/12	Х			
BMSRT	BIT MASKED SPLIT READ TRANSFER	/- 1	1	1	0/12	Х			
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/12	0/13			

NOTE:

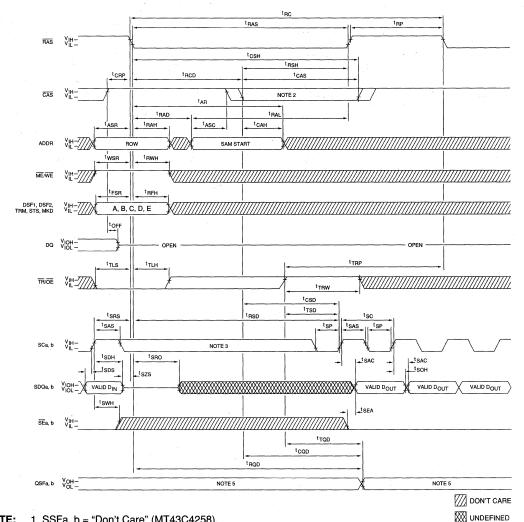
- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
- The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
- 3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

nd the Andreas **Aut** Salam Light and Andrea (1997). And Andreas (1997) And Andreas (1997) and Andreas (1997).



READ TRANSFER 1, 4 (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode)

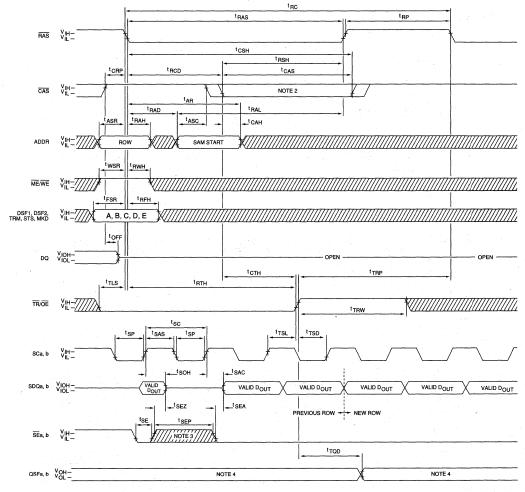


- 1. SSFa, b = "Don't Care" (MT43C4258).
- 2. CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.
- 3. There must be no rising edges on the SC input during this time period.
- 4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
- 5. QSF = 0 when the Lower SAM (bits 0-255) is being accessed. QSF = 1 when the Upper SAM (bits 256-511) is being accessed.



REAL-TIME READ TRANSFER 1, 5 (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL OUTPUT mode)

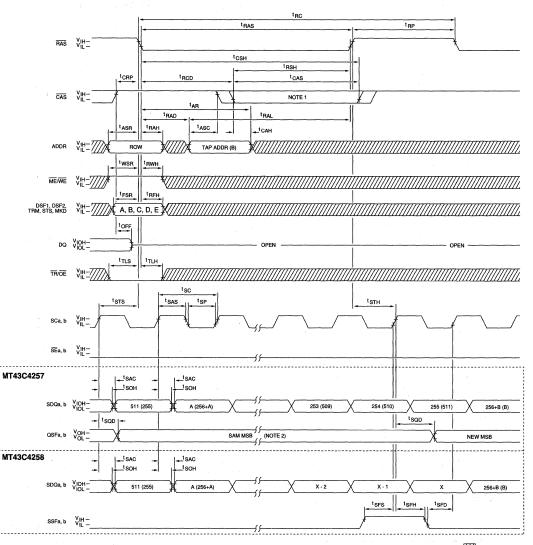


DON'T CARE

- 1. SSFa, b = "Don't Care" (MT43C4258).
- 2. CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed.
- 3. The SE pulse is shown to illustrate the serial output enable and disable timing. It is not required.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
- 5. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.



SPLIT READ TRANSFER ³ (SPLIT DRAM-TO-SAM TRANSFER)



DON'T CARE
UNDEFINED

- CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.
- QSF = 0 when the Lower SAM (bits 0–255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256–511) is being accessed.
- 3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.



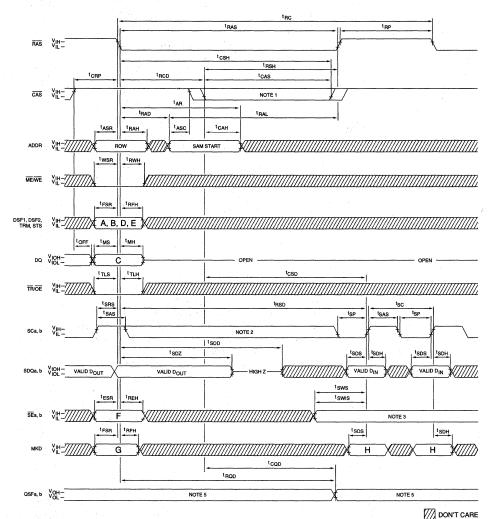
WRITE TRANSFER CYCLE FUNCTION TABLE 1

		LOGIC STATES									
			RAS Falling Edge								
CODE	FUNCTION	A DSF1	B DSF2	C DQ	D TRM	E STS	F SE	G MKD	H MKD		
WT	WRITE TRANSFER (SAM→DRAM)	0	0	Х	0	0/12	0	Х			
PWT	PSEUDO WRITE TRANSFER	0	0	Х	0	0/12	1	Х	-		
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/12	Х	Х	- - - -		
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/12	Х	Х	•		
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Х	A 1	0/12	Х	Х	0/14		
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/12	Х	х	0/14		
SAM-BMR	(SAM→BMR) TRANSFER	1	0	Х	1	0/12	Х	0/1 ³	-		

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G", and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
- The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
- 3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
- 4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.



WRITE TRANSFER 4 (When part was previously in the SERIAL OUTPUT mode)



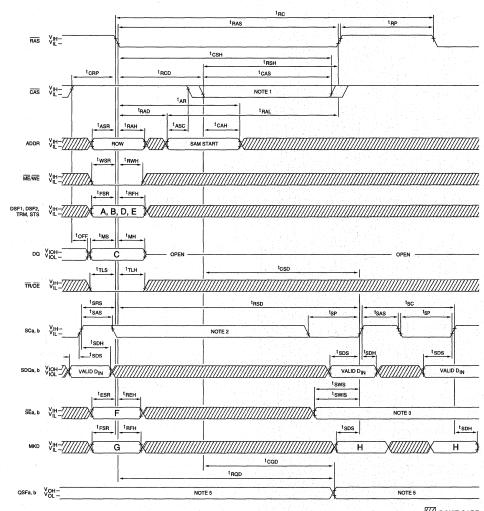
NOTE:

- CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.
- 2. There must be no rising edges on the SC input during this time period.
- 3. SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
- QSF = 0 when the Lower SAM (bits 0-255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256-511) is being accessed. SSFa,b = "don't care" (MT43C4258).

W UNDEFINED



WRITE TRANSFER 4 (When part was previously in the SERIAL INPUT mode)

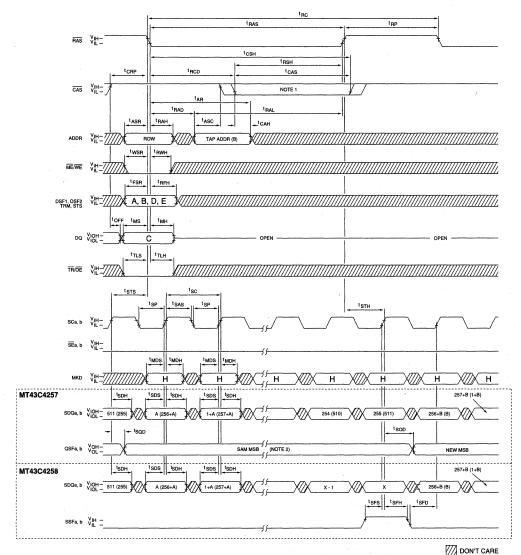


NOTE:

 CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused. DON'T CARE
UNDEFINED

- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 3. There must be no rising edges on the SC input during this time period.
- 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
- QSF = 0 when the Lower SAM (bits 0-255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256-511) is being accessed. SSFa,b = "don't care" (MT43C4258).

SPLIT WRITE TRANSFER 3 (SPLIT SAM-TO-DRAM TRANSFER)



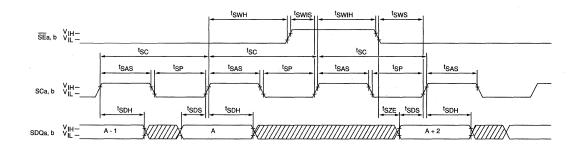
NOTE:

 CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused. UNDEFINED

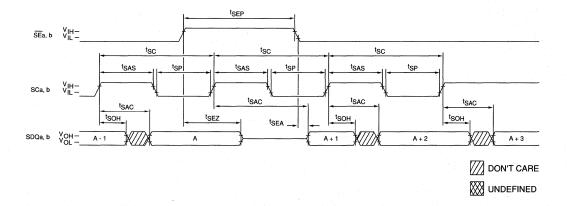
- QSF = 0 when the Lower SAM (bits 0-255) is being accessed.
 QSF = 1 when the Upper SAM (bits 256-511) is being accessed.
- The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.



SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



NOTE: SEa, SCa and SDQa are used when accessing SAMa and SEb; SCb and SDQb are used when access in SAMb.

TRIPLE PORT DRAM

128K x 8 DRAM WITH DUAL 256 x 8 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times 80ns random, 25ns serial
- Operation and control compatible with 1 Meg VRAMs
- High-performance, CMOS silicon-gate process
- Inputs and outputs are fully TTL compatible
- · Low power: 15mW standby; 550mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE access cycles
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 2,048-bit Bit Mask Register
- SERIAL MASK DATA INPUT mode

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- PERSISTENT MASKED WRITE
- SPLIT READ AND WRITE TRANSFERS
- BLOCK WRITE
- BIT MASKED TRANSFERS

OPTIONS

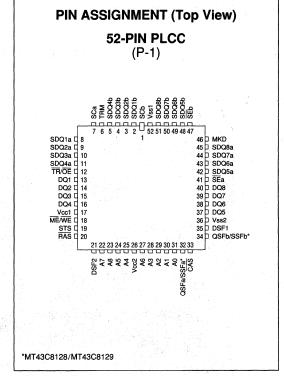
MARKING

- Timing [DRAM, SAMs (cycle/access)] 80ns, 28ns/25ns - 8 100ns, 30ns/27ns -10
- Packages
 Plastic LCC (750 mil)
 EJ
- Functionality
 QSF output
 (indicates SAM half accessed)
 SSF input
 (Split SAM special function, stop count)

GENERAL DESCRIPTION

The MT43C8128/9 are high speed, triple port CMOS dynamic random access memories (TPDRAM) containing 1,048,576 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 256 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally identical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit



data registers make up the serial access memory portions of the TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; the 8-bit random access I/O port, a pair of internal 2,048 bit wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

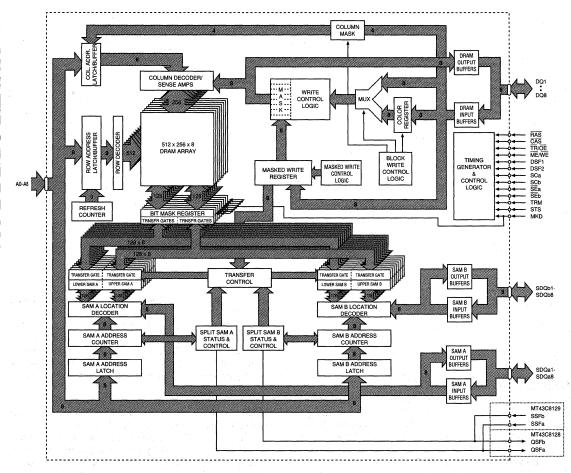
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 2,048 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 256 x 8-bit Bit Mask Data Register can be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C8128/9 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in rastor graphics display, video windowing, serial/parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERs and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

PLCC PIN Number	SYMBOL	TYPE	DESCRIPTION
. 7	SCa	Input	Serial Clock, SAMa: Clock input to the serial address counter for the SAMa registers and strobe for SAMa control and data inputs.
1	SCb	Input	Serial Clock, SAMb: Clock input to the serial address counter for the SAMb registers and strobe for SAMb control and data inputs.
12	TR/OE	Input	Transfer Enable: Enables an internal TRANSFER operation at the falling edge of RAS, or
			Output Enable: Enables the DRAM output buffers when taken LOW after RAS goes LOW (CAS must also be LOW), otherwise the output buffers are in a high impedance state.
18. 18. 18. 18. 18. 18. 18. 18. 18. 18.	ME/WE	Input	Mask Enable: If ME/WE is LOW at the falling edge of RAS, a MASKED WRITE cycle is performed, or
			Write Enable: ME/WE is also used to select a READ (ME/WE = H) or WRITE (ME/WE = L) cycle when accessing the DRAM. This includes a READ TRANSFER (ME/WE = H) or WRITE TRANSFER (ME/WE = L).
41	SEa	Input	Serial Port Enable SAMa: SEa enables Port A serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEa is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL INPUT MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
47	SEb	Input	Serial Port Enable, SAMb: SEb enables Port B serial I/O buffers and allows a serial READ or WRITE operation to occur; otherwise, the output buffers are in a High-Z state. SEb is also used during a TRANSFER operation to indicate whether a WRITE TRANSFER or a SERIAL-INPUT-MODE ENABLE (PSEUDO WRITE TRANSFER) cycle is performed.
35	DSF1	Input	Special Function (Control) 1: DSF1 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
21	DSF2	Input	Special Function (Control) 2: DSF2 is used to indicate which special functions are used on a particular access or transfer cycle. See the Functional Truth Table for a detailed description.
20	RAS	Input	Row Address Strobe: RAS is used to clock-in the 9 row-address bits and as a strobe for control and data inputs.
33	CAS	Input	Column Address Strobe: CAS is used to clock-in the 8 column-address bits, enable the DRAM output buffers (along with TR/OE), and strobe control and data inputs.

PIN DESCRIPTIONS (continued)

PLCC PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
31, 30, 29, 28, 25, 24, 27, 22, 23	A0-A8	Input	Address Inputs: For DRAM operation, these inputs are multiplexed and clocked by RAS and CAS to select one 8-bit word out of the 128K available. During TRANSFER operations, A0 to A8 indicate the DRAM row being accessed (when RAS goes LOW) and A0-A7 indicate the SAM start address (when CAS goes LOW). A7, A8 = "don't care" for the start address when doing SPLIT TRANSFER.
19	STS	Input	SAM Transfer Select: The state of STS at RAS time determines which SAM is involved in a transfer (SAMa = LOW, SAMb = HIGH).
46	MKD	Input	Mask Data Input: MKD is used during BIT MASK REGISTER LOAD cycles to enable or disable the serial mask input mode (SMI). If SMI is enabled (MKD = HIGH at RAS), then MKD is used as mask data input and is clocked by SCb into the mask data register.
6	TRM	Input	Transfer Mask Select: TRM is used to select between NORMA TRANSFER cycles and BIT MASKED TRANSFER or BIT MAS REGISTER LOAD cycles.
13, 14, 15, 16, 37, 38, 39, 40	DQ1-DQ8	Input/ Output	DRAM Data I/O: Data inputs and outputs for the DRAM memor array; inputs for the MASK and COLOR REGISTER load cycle: address mask inputs for BLOCK WRITE cycles.
8, 9, 10, 11, 42, 43, 44, 45	SDQa1-SDQa8	Input/ Output	Serial Data I/O, SAMa: Input, Output, or High-Z.
2, 3, 4, 5, 48, 49, 50, 51	SDQb1-SDQb8	Input/ Output	Serial Data I/O, SAMb: Input, Output, or High-Z.
32	QSFa/SSFa	Output	Split SAM Status, SAMa (MT43C8128): QSFa indicates which half of SAMa is being accessed (Lower = LOW, Upper = HIGH
		Input	Split SAM Special Function, SAMa (MT43C8129): SSFa = HIG stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFa is synchronized with SCa.
34	QSFb/SSFb	Output	Split SAM Status, SAMb (MT43C8128): QSFb indicates which half of SAMb is being accessed (Lower = LOW, Upper = HIGH
		Input	Split SAM Special Function, SAMb (MT43C8129): SSFb = HIG stops access to current half of SAM and will load the Tap address of the next half into the address pointer. SSFb is synchronized with SCb.
17, 26	Vcc	Supply	Power Supply: +5V ±5%
52, 36	Vss	Supply	Ground

MULTIPORT DRAM

FUNCTIONAL DESCRIPTION

The MT43C8128/9 may be divided into four functional blocks: the DRAM and its special functions, the bit mask register (BMR), the two serial access memories (SAMs), and the DRAM/SAM/BMR transfer circuitry. All the operations described below are also shown in the AC Timing Diagrams section of this data sheet and are summarized in the Functional Truth Table.

Note:

For dual function pins, the function that is not being discussed will be surrounded by parentheses. For example, when discussing transfer operations the $\overline{TR}/\overline{OE}$ pin will be shown as $\overline{TR}/(\overline{OE})$.

DRAM OPERATION

This section describes the operation of the random access port and the special functions associated with the DRAM.

DRAM REFRESH (ROR, CBR, and HR)

Like any DRAM-based memory, the MT43C8128/9 TPDRAM must be refreshed to retain data. All 512 row-address combinations must be accessed within 8ms. The MT43C8128/9 support CAS-BEFORE-RAS, RAS-ONLY and HIDDEN types of refresh cycles.

For the CAS-BEFORE-RAS REFRESH cycle, the row addresses are generated and stored in an internal address counter. The user need not supply any address data and simply must perform 512 CAS-BEFORE-RAS cycles within the 8ms time period.

For RAS-ONLY REFRESH cycles, the refresh address must be generated externally and applied to the A0-A8 inputs. The DQ pins remain in a High-Z state for both the RAS ONLY and CAS-BEFORE-RAS cycles.

HIDDEN REFRESH (HR) cycles are performed by toggling RAS (while keeping CAS LOW) after a READ or WRITE cycle. This performs CAS-BEFORE-RAS cycles but does not disturb the DQ lines.

Any DRAM READ, WRITE, or TRANSFER cycle also refreshes the DRAM row that is being accessed. The SAM and BMR portions of the MT43C8128/9 are fully static and do not require any refreshing.

DRAM READ AND WRITE CYCLES (RW)

The DRAM portion of the TPDRAM is nearly identical to standard 1256K x 4 DRAMs. However, because several of the DRAM control pins are used for additional functions on this device, several conditions that were undefined or "don't

care" states for the DRAM are specified for the TPDRAM. These conditions are highlighted in the following discussion. In addition, the TPDRAM has several special functions that may be used when writing to the DRAM.

The 17 address bits used to select an 8-bit word from the 131,072 available are latched into the chip using the A0-A8, \overline{RAS} , and \overline{CAS} inputs. First, the 9 row-address bits are set up on the address inputs and clocked into the part when \overline{RAS} transitions from HIGH-to-LOW. Next, the 8 column-address bits (A0-A7) are set up on the address inputs and clocked-in when \overline{CAS} goes from HIGH-to-LOW.

Note:

RAS also acts as a "master" chip enable for the TPDRAM. If RAS is inactive, HIGH, all other DRAM control pins (CAS, TR/OE, ME/WE, etc.) are a "don't care" and may change state without effect. No DRAM or TRANSFER cycles will be initiated without RAS falling.

For single port DRAMS, the \overline{OE} pin is a "don't care" when \overline{RAS} goes LOW. For the TPDRAM, $\overline{TR}/(\overline{OE})$ is used when \overline{RAS} goes LOW to select between DRAM and TRANSFER cycles. $\overline{TR}/(\overline{OE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition for all DRAM operations.

If $(\overline{ME})/\overline{WE}$ is HIGH when \overline{CAS} goes LOW, a DRAM READ operation is performed and the data from the memory cells selected will appear at the DQ1-DQ8 port. The $(\overline{TR})/\overline{OE}$ input must transition from HIGH-to-LOW some time after \overline{RAS} falls to enable the DRAM output port.

For single port DRAMs, \overline{WE} is a "don't care" when \overline{RAS} goes LOW. For the TPDRAM, $\overline{ME}/(\overline{WE})$ is used, when \overline{RAS} goes LOW, to select between a MASKED WRITE cycle or a normal WRITE cycle. If $\overline{ME}/(\overline{WE})$ is LOW at the \overline{RAS} HIGH-to-LOW transition, a MASKED WRITE operation is selected. For any TPDRAM non-masked access cycle (READ or WRITE), $\overline{ME}/(\overline{WE})$ must be HIGH at the \overline{RAS} HIGH-to-LOW transition. If $\overline{(\overline{ME})}/\overline{WE}$ is LOW when \overline{CAS} goes LOW, a DRAM WRITE operation is performed and the data present on the DQ1-DQ8 data port will be written into the selected memory cells.

The TPDRAM can perform all the normal DRAM cycles: READ, EARLY-WRITE, LATE-WRITE, READ-MODIFY-WRITE, FAST-PAGE-MODE READ, FAST-PAGE-MODE WRITE, and FAST-PAGE-MODE READ-MODIFY-WRITE. Refer to the AC timing parameters and diagrams in the data sheet for more details on these operations.

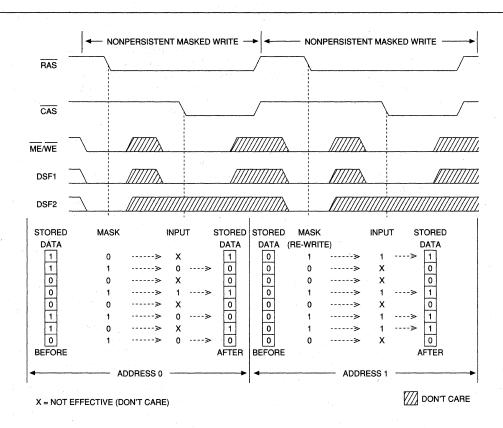


Figure 1 NONPERSISTENT MASKED WRITE EXAMPLE

NONPERSISTENT MASKED WRITE (RWNM)

The MASKED WRITE feature eliminates the need to do a READ-MODIFY-WRITE cycle when changing only certain bits within an 8-bit word. The MT43C8128/9 supports two types of MASKED WRITE cycles, NONPERSISTENT MASKED WRITE and PERSISTENT MASKED WRITE.

If ME/(WE), DSF1 and DSF2 are LOW at the RAS HIGHto-LOW transition, the data (mask data) present on the DQ1-DQ8 inputs will be written into the mask data register. The mask data acts as an individual write enable for each of the eight DQ1-DQ8 pins. If a LOW (logic 0) is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic 1) on a mask data register bit enables the input port and allows normal WRITE operations to proceed. This conven-

tion is used for all masks on the MT43C8128/9. Note that $\overline{\text{CAS}}$ is still HIGH. When $\overline{\text{CAS}}$ or $(\overline{\text{ME}})/\overline{\text{WE}}$ go LOW, the bits present on the DQ1-DQ8 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW). The DRAM contents that correspond to the masked bits will not be changed during the WRITE cycle. When using NONPERSISTENT MASKED WRITE, the data present on the DQ inputs is loaded into the mask data register at every falling edge of RAS. FAST PAGE MODE may be used in tandem with NONPERSISTENT MASKED WRITE to write several column locations using the same mask during one RAS cycle. An example of NONPERSISTENT MASKED WRITE cycle is shown in Figure 2.



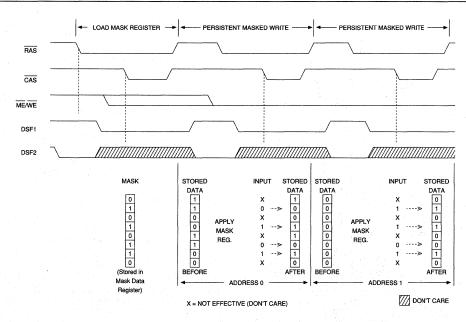


Figure 2
PERSISTENT MASKED WRITE EXAMPLE

PERSISTENT MASKED WRITE (RWOM)

The PERSISTENT MASKED WRITE feature eliminates the need to rewrite the mask data before each MASKED WRITE cycle if the same mask data is being used repeatedly. To initiate a PERSISTENT MASKED WRITE, a LOAD MASK REGISTER cycle is performed by taking $\overline{\text{ME}}/(\overline{\text{WE}})$ and DSF1 HIGH, and DSF2 LOW, when $\overline{\text{RAS}}$ goes LOW. The mask data is loaded into the internal register when $\overline{\text{CAS}}$ goes LOW, provided DSF1 is LOW (see the LOAD MASK REGISTER description).

PERSISTENT MASKED WRITE cycles may then be performed by taking ME/(WE) and DSF2 LOW and DSF1 HIGH when RAS goes LOW. The contents of the mask data register will then be used as the mask data for the DRAM inputs. Unlike the NONPERSISTENT MASKED WRITE cycle, the data present at the DQ inputs is not loaded into the mask register when RAS falls. Another PERSISTENT MASKED WRITE cycle may be performed without reloading the register. Figure 2 shows the LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycle operations. The LOAD MASK REGISTER and PERSISTENT MASKED WRITE cycles allow systems that cannot output data at RAS time to perform MASKED WRITE cycles. PERSISTENT MASKED WRITE can also operate in FAST PAGE MODE.

BLOCK WRITE (BW)

If DSF1 is HIGH when CAS goes LOW, the MT43C8128/9 will perform a BLOCK WRITE cycle instead of a normal WRITE cycle. In BLOCK WRITE cycles, the contents of the color register (instead of the DQ inputs) are directly written to four adjacent column locations (see Figure 3). A total of 32 bits will be written simultaneously, improving the normal DRAM fill rate by four times. The color register must be loaded prior to beginning BLOCK WRITE cycles (see LOAD COLOR REGISTER).

The row is addressed as in a normal DRAM WRITE cycle. However, when \overline{CAS} goes LOW, only the A2-A7 inputs are used. A2-A7 specify the "block" (out of the 64 possible) of four adjacent column locations that will be accessed. When the later of $\overline{ME}/\overline{WE}$ and \overline{CAS} go LOW, the DQ inputs latched and used to determine which of the four column locations will be written. DQ1 acts as a write enable for column location A0 = 0, A1 = 0; DQ2 controls column location A0 = 1, A1 = 0; DQ3 controls A0 = 0, A1 = 1; and DQ4 controls A0 = 1, A1 = 1. The write enable controls are active HIGH; a logic 1 enables and a logic 0 disables the WRITE function.

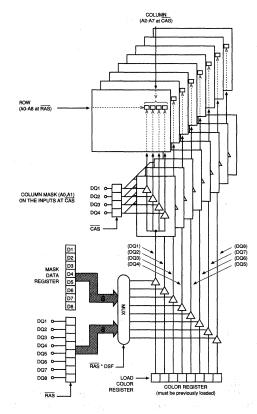


Figure 3 **BLOCK WRITE EXAMPLE**

The contents of the color register will then be written to the column locations enabled. Each DQ location of the color register is written to the four column locations (or any of the four that are enabled) in the corresponding DQ bit plane. The DQ mask is not used in this mode.

NONPERSISTENT MASKED BLOCK WRITE (BWNM)

The MASKED WRITE functions can also be used during BLOCK WRITE cycles. NONPERSISTENT MASKED BLOCK WRITE operates exactly like the normal NONPER-SISTENT MASKED WRITE except the mask is now applied to four column locations instead of just one column location.

Like NONPERSISTENT MASKED WRITE, the combination of $\overline{\text{ME}}/(\overline{\text{WE}})$ LOW and DSF1 LOW when $\overline{\text{RAS}}$ goes LOW, initiates a NONPERSISTENT MASK cycle. The DSF pin must be driven HIGH when CAS goes LOW to perform a NONPERSISTENT MASKED BLOCK WRITE. By using both the column mask input and the MASKED WRITE function, any combination of the four bit planes may be masked and any combination of the eight column locations may be masked.

PERSISTENT MASKED BLOCK WRITE (BWOM)

This cycle is also performed exactly like the normal PERSISTENT MASKED WRITE except that DSF1 is HIGH when CAS goes LOW to indicate the BLOCK WRITE function. Both the mask data register and the color register must be loaded with the appropriate data prior to starting a PERSISTENT MASKED BLOCK WRITE.

DRAM REGISTER OPERATIONS

The MT43C8128/9 contains two 8-bit registers that are used as data registers for special functions. This section describes how to load these registers.

LOAD MASK REGISTER (LMR)

The LOAD MASK REGISTER operation and timing are identical to a normal WRITE cycle except that DSF1 is HIGH when RAS goes LOW. As shown in the Truth Table, the combination of $\overline{TR}/(\overline{OE})$, $\overline{ME}/(\overline{WE})$, and DSF1 being HIGH when RAS goes LOW indicates the cycle is a REGISTER load cycle. DSF1 is used when CAS goes LOW to select the register to be loaded, and must be LOW for a LOAD MASK REGISTER cycle. The data present on the DQ lines will then be written to the mask data register.

Note:

For a normal DRAM WRITE cycle, the mask data register is disabled but not modified. The contents of mask data register will not be changed unless a NON-PERSISTENT MASKED WRITE cycle or a LOAD MASK REGISTER cycle is performed

The row address supplied will be refreshed, but it is not necessary to provide any particular row address. The column address inputs are ignored during a LOAD MASK REGISTER cycle.

The mask data register contents are used during PERSIS-TENT MASKED WRITE and PERSISTENT MASKED BLOCK WRITE cycles to selectively enable writes to the eight DQ planes.

LOAD COLOR REGISTER (LCR)

A LOAD COLOR REGISTER cycle is identical to the LOAD MASK REGISTER cycle except DSF1 is HIGH when CAS goes LOW. The contents of the color register are retained until changed by another LOAD COLOR REGIS-TER cycle (or the part loses power) and are used as data inputs during BLOCK WRITE cycles.



TRANSFER OPERATIONS

This section describes transfer operations between the DRAM and either SAM. The direction of the transfer is specified with respect to the DRAM portion of the device. A write is referenced to the DRAM array and a read is referenced from the array.

Note:

The three ports of the TPDRAM are independent and asynchronous to one another. Any or all of the ports may be accessed simultaneously at the maximum allowable frequencies. The only time the ports are synchronized is during transfers to or from the DRAM and SAM portions of the device. A transfer involving a SAM does not affect access from the other SAM port. Both SAMs may be accessed during a DRAM/BMR transfer operation or any other DRAM access cycle other than a SAM transfer.

TRANSFER operations are initiated when $\overline{TR}/(\overline{OE})$ is LOW at the falling edge of \overline{RAS} . The state of STS when \overline{RAS} goes LOW indicates which SAM the TRANSFER will address. The state of $(\overline{ME})/\overline{WE}$ when \overline{RAS} goes LOW indicates the direction of the TRANSFER. At the same time, DSF1 is used to select between normal TRANSFER cycles and SPLIT TRANSFER cycles and DSF2 is used to select between normal TRANSFER cycles and MASKED TRANSFER cycles. A TRANSFER cycle can be performed without dropping \overline{CAS} . In this case, the previously loaded Tap address will be used.

The MT43C8128/9 include a feature called BIT MASKED TRANSFER, which uses a third 2,048-bit data register to individually mask every bit involved in a TRANSFER operation. The BIT MASKED TRANSFER may be applied to either READ or WRITE TRANSFERs. The TRM pin is used to select between NORMAL and BIT MASKED TRANSFER (or BIT MASK REGISTER LOAD) cycles. The type of transfer operation is always selected on the falling edge of RAS.

NORMAL TRANSFERS

The MT43C8128/9 support all of the popular transfer cycles available on the 1 Meg video RAMs. Each of these is described in the following section.

READ TRANSFER (RT)

A READ TRANSFER cycle is selected if $(\overline{\text{ME}})/\overline{\text{WE}}$ is HIGH, and DSF1 and $\overline{\text{TR}}/(\overline{\text{OE}})$ are LOW when $\overline{\text{RAS}}$ goes LOW. When $\overline{\text{RAS}}$ goes LOW, the READ TRANSFER is to SAMa if STS = LOW, or to SAMb if STS = HIGH. The row address bits indicate the eight 256-bit DRAM rows that are to be transferred to the eight SAM data registers. The column address bits indicate the start address (or Tap point) of the next serial output cycle from the designated SAM

data registers. QSF indicates the SAM half being accessed: LOW if the lower half; HIGH if the upper half. Performing a READ TRANSFER cycle sets the direction of the selected SAMs I/O buffers to the output mode.

To complete a REAL-TIME READ-TRANSFER, $\overline{TR}/(\overline{OE})$ is taken HIGH while \overline{RAS} and \overline{CAS} are LOW. In order to synchronize the REAL-TIME READ-TRANSFER to the serial clock, the rising edge of $\overline{TR}/(\overline{OE})$ must occur between the rising edges of successive clocks on the SC input (refer to the AC timing diagrams). A "regular" READ TRANSFER is not sychronized with the SC pin of the addressed SAM. This type of RT is performed when $\overline{TR}/(\overline{OE})$ is taken HIGH "early," without regard to the falling edge of CAS. The transfer will be completed internally by the device. The first serial clock must meet the ^tRSD and ^tCSD delays (see READ TRANSFER AC timing diagram). The 2,048 bits of DRAM data are then written into the SAM data registers, and the selected SAM's Tap address that was stored in the internal, 8-bit Tap address register is loaded into the address counter. If SE for the SAM selected (SEa for SAMa) is LOW, the first bits of the new row data will appear at the serial outputs with the next SC clock pulse. SE enables the serial outputs, and may be either HIGH or LOW during this operation.

SPLIT READ TRANSFER (SRT)

The SPLIT READ TRANSFER cycle eliminates the critical transfer timing required to maintain a continuous serial output data stream (the "full" READ TRANSFER cycle has to occur immediately after the final bit of "old data," and before the first bit of "new data" is clocked out of the SAM port).

When using the SPLIT TRANSFER mode, the SAM is divided into an upper half and a lower half. While data is being serially read from one half of the SAM, new DRAM data may be transferred to the other half. The transfer may occur at any time while the other half is sending data, and need not be synchronized with the SC clock.

The $\overline{TR}/(\overline{OE})$ timing is relaxed for SRT cycles. The rising edge of $\overline{TR}/(\overline{OE})$ is not used to complete the TRANSFER cycle, and therefore is independent of the rising edges of \overline{RAS} and \overline{CAS} . The transfer timing is generated internally for SPLIT TRANSFER cycles.

SPLIT TRANSFERs do not change the SAM I/O direction. A normal (nonsplit) READ TRANSFER cycle must precede any sequence of SRT cycles to put the SAM I/O in the output mode and provide the initial SAM Tap address (which half). Then an SRT may be initiated by taking DSF1 HIGH and selecting the desired SAM (using STS) when RAS goes LOW during the TRANSFER cycle. As in nonsplit transfers, the row address is used to specify the DRAM row to be transferred. When an SRT cycle is initiated, the half of the SAM not actively being accessed will be the half that

receives the transfer. When \overline{CAS} falls, address pins A0-A6 determine the Tap address for the SAM-half selected; A7 = "don't care." If \overline{CAS} does not fall, the previously loaded Tap address will be reused and the TRANSFER will be to the idle half.

Figure 4 shows a typical SRT initiation sequence. The normal READ TRANSFER is first performed, followed by an SRT of the same row to the upper half of the SAM. The SRT to the upper half is optional, and need only be done if the Tap for the upper half is \neq 0. For the MT43C8128, serial access continues and when the SAM address counter reaches 127 ("A7" = 1, A0-A6 = 0), the QSF output for that SAM goes HIGH and the Tap address for the upper half is automatically loaded. Since the serial access has now switched to the upper half of the SAM, new data may be transferred to the lower half. This sequence of waiting for the state of QSF to change and then transferring new data to the SAM half that is not being accessed may now be repeated. For example, the next step in Figure 4 would be to wait until QSF went

LOW (indicating that row-1 data is shifting out the lower SAM) and then transferring the upper half of row 1 to the upper SAM. CAS is used to load the Tap address. If CAS does not fall, the last Tap address load for the addressed SAM will be reused.

The split SAM operation is slightly different for the MT43C8129. Instead of having a QSF, this device has a Split SAM Special Function (SSF) input. With this input the serial access may be switched at will from one half of the SAM to the other. In other words, the address count may be stopped on the current half and the Tap address of the next half may be loaded, without waiting for the maximum address count of the current half (127; lower, 255; upper). If no SSF pulse is applied, the Tap address of the next half will be automatically loaded when the maximum count of the current SAM-half is reached. QSF = 0 when the Lower SAM (bits 0–127) is being accessed. QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

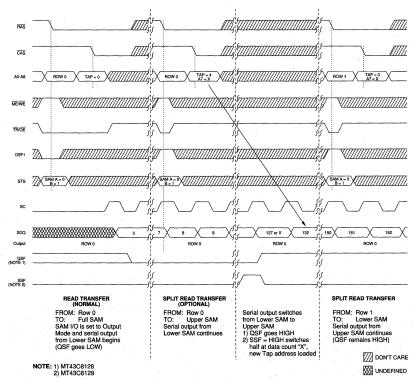


Figure 4
TYPICAL SPLIT-READ-TRANSFER INITIATION SEQUENCE



WRITE TRANSFER (WT)

The operation of the WRITE TRANSFER is identical to the READ TRANSFER described previously, except $(\overline{ME})/\overline{WE}$ and SE must be LOW when RAS goes LOW. The DSF2 input is used to select between the WT and DQ MASKED WRITE TRANSFER cycles, and must be LOW for the WT cycle. The STS pin is also taken LOW or HIGH to select SAMa or SAMb, respectively, when RAS goes LOW. The row address indicates the DRAM row to which the SAM data register will be written, and the Tap address indicates the starting address of the next SERIAL INPUT cycle for the SAM data registers. QSF indicates the SAM half being accessed; LOW if the lower half, HIGH if the upper half. Performing a WT sets the direction of the SAM I/O buffers to the input mode.

PSEUDO WRITE TRANSFER (PWT)

The PSEUDO WRITE TRANSFER cycle may be used to change the direction of a SAM port from output to input without disturbing the DRAM data in the selected row. A PSEUDO WRITE TRANSFER cycle is a WRITE TRANSFER cycle with the SE of the appropriate SAM held HIGH instead of LOW. The addressed row will be refreshed. A DQ MASKED WRITE TRANSFER (with all bits masked) is an alternate method for changing the direction of the SAM port without disturbing the addressed row data.

DQ MASKED WRITE TRANSFER (MWT)

The data being transferred from either SAM to the DRAM may be masked by performing a DQ MASKED WRITE TRANSFER cycle. The transfer of data may be selectively enabled for each of the eight DQ planes (see Figure 5). The DMWT cycle is identical to the WRITE TRANSFER cycle except DSF2 is HIGH and mask data must be on the DQ inputs at the falling edge of RAS.

The complete SAM register will be transferred to the selected row in each DQ plane if the mask data input is HIGH, and the SAM register will not be transferred if the mask data input for that DQ plane is LOW. DRAM data is not disturbed in masked DQ planes.

DQ MASKED SPLIT WRITE TRANSFER (MSWT)

The SPLIT WRITE TRANSFER feature makes it possible to input and transfer uninterrupted bit streams. Figure 6 shows a typical initiation sequence for SWT cycles.

Like the SRT, the DQ MASKED SPLIT WRITE TRANS-FER cycle does not change the state of the SAM I/O buffers. A normal, DQ MASKED or PSEUDO WRITE TRANSFER cycle is required to set the Tap address and set the SAM I/O direction to input mode.

After the WT, a MSWT is performed to enter the split SAM operating mode. This sets the Tap for the next half of the SAM. The addressed half of the SAM is immediately transferred to the first destination row. This half of the SAM

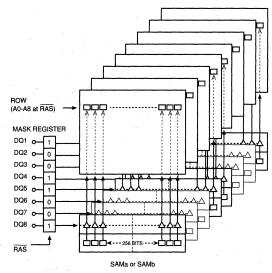


Figure 5 DQ MASKED WRITE TRANSFER

may not yet contain valid data. However, another MSWT to the same row will normally occur after this is loaded, so the initial invalid data will be overwritten. Another approach would be to initiate an MSWT addressed to any DRAM row, but mask (disable) all eight of the DQ planes. This method can be used to initiate the MSWT sequence without disturbing any DRAM data. The MSWT to the upper half is optional, and it is only needed if the Tap for the upper half

Write mask data must be supplied to the DQ inputs during every SWT cycle at RAS time. The mask data acts as an individual write enable for each of the eight DRAM DQ planes. For example, DQ1, at RAS time, during a DQ1 MASKED WRITE, enables or disables the transfer of the SAM SDQ1 register to the DQ1 plane of the DRAM row selected (see the DQMASKED WRITE TRANSFER description). As in all other MASKED WRITE operations, a HIGH enables the WRITE TRANSFER and a LOW disables the WRITE TRANSFER. As with SPLIT READ TRANSFER, the half of the SAM not receiving data will be the half transferred and the Tap address (A0-A6) for the other half is loaded when CAS falls (A7 is a "don't care"). If CAS does not fall, the previously loaded Tap address, A0-A6, will be reused. The TRANSFER will be to the idle half. When the serial clock crosses the half-SAM boundary, the new Tap address for that half is automatically loaded.

The QSFa and QSFb outputs (MT43C8128) indicate which half of SAMa or SAMb, respectively, is currently accepting

data. After QSF goes HIGH, indicating that serial input has now switched to the upper SAM, the contents of the lower half of the SAM may be transferred to any DRAM row. The cycle of checking for a change in QSF and then transferring the half of the SAM just filled may now be repeated. The next step on Figure 6 is to wait for QSF to go LOW and then SWT the contents of the upper half of the SAM to row 0. If the terminal count of the SAM half is reached before an SWT is performed for the next half, the access will be repeated from the same half and previously loaded Tap address (access will not move to the next half).

When operating the MT43C8129 in the MSWT mode, the address pointer may be changed to the new Tap address of the next half when the final desired input data is clocked-in. When the final data is input, the SSF input is taken HIGH at the corresponding rising edge of SC. The next SC rising

edge will input data into the Tap location of the next half of the SAM. If SSF is not applied, the Tap address will be automatically loaded when the maximum Tap address count is reached for the current half (127 or 255). If SSF is HIGH at SC before an MSWT is performed for the next half, the access will jump to the old Tap address of the same half. Access will not preceed to the next half. If terminal count is reached before an MSWT, the access will proceed as it does for the MT43C8128.

SERIAL INPUT and SERIAL OUTPUT

The control inputs for SERIAL INPUT and SERIAL OUT-PUT are SCa,b, \overline{SE} a,b and SSFa,b (MT43C8128). The rising edge of SC increments the serial address counter and provides access to the next SAM location. \overline{SE} enables or disables the serial input/output buffers.

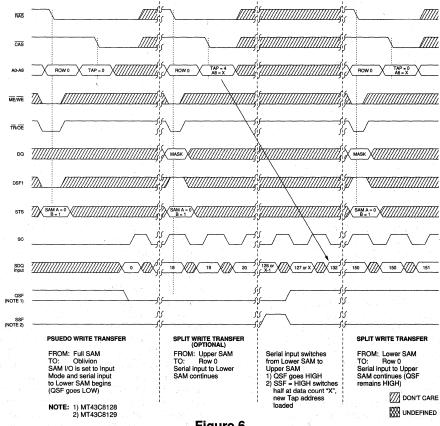


Figure 6
TYPICAL SPLIT-WRITE-TRANSFER INITIATION SEQUENCE



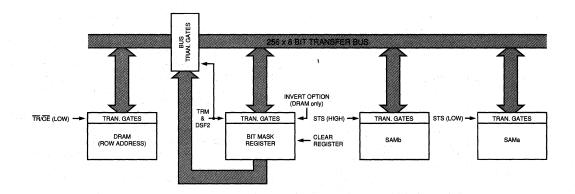


Figure 7
BIT MASKED TRANSFER BLOCK DIAGRAM

Serial output of the SAM contents will start at the serial ΓAP address that was loaded in the SAMa, b address counter during the DRAM-TO-SAM TRANSFER cycle. The SC nput increments the address counter and presents the contents of the next SAM location to the 8-bit port. SE is used as an output enable during the SAM output operation. The serial address is automatically incremented with every SC LOW-to-HIGH transition, regardless of whether \overline{SE} is HIGH or LOW. For the MT43C8128, the address progresses hrough the SAM and will wrap around (after count 127 or 255) to the Tap address of the next half, for split modes. Address count will wrap around (after count 255) to Tap ddress 0 if in the "full" SAM modes. For the MT43C8129, he address count will wrap as it does for the MT43C8128 or t may be triggered, at will, to the next half by the SSF input split SAM modes). If SSF is HIGH at a LOW-to-HIGH ransition of SC, the Tap address of the next half will be paded into the address pointer. The subsequent LOW-to-HIGH transition of SC will clock data from the Tap address f the new half.

SC is also used to clock-in data when the device is in the erial input mode. As in the serial output operation, the ontents of the serial address counter (loaded when the erial input mode was enabled) will determine the serial ddress of the first 8-bit word written. \overline{SE} acts as a WRITE NABLE for serial input data and must be LOW for valid erial input. If \overline{SE} = HIGH, the data inputs are disabled and the SAM contents will not be modified. The serial address outer is incremented with every LOW-to-HIGH transion of SC, regardless of the logic level on the \overline{SE} input. The peration of SSF (MT43C8129) is the same as described for trial output.

BIT MASKED TRANSFERS

This section describes transfers between the DRAM and either of the two SAMs using the BIT MASKED TRANSFER capability. Before performing these BIT MASKED TRANSFERs, the bit mask register must first be loaded with the mask data. See the next section, BIT MASK REGISTER OPERATIONs, for instructions on how to load the bit mask register (BMR).

The BMR is a 2,048-bit register that individually controls each of the 2,048 transfer gates on the internal 256×8 transfer bus (see Figure 7). These bus transfer gates reside between the DRAM array and the three data registers and are set to the "pass-thru" mode for nonmasked transfers. For BIT MASKED TRANSFERs, the data in the BMR is coupled to the control inputs of the bus transfer gates. A logic "1" in the BMR will select the pass-thru (unmasked) mode for the corresponding SAM data bit, while a logic "0" will select the masked mode for that bit.

BIT MASKED TRANSFERs may be incorporated when doing READ, WRITE, SPLIT READ and SPLIT WRITE TRANSFERs. The timing and control required for any particular BIT MASKED TRANSFER cycle is identical to the corresponding normal TRANSFER cycle, except that TRM and DSF2 are HIGH instead of LOW. BIT MASKED TRANSFERs between the DRAM and either of the two SAM registers are possible. Figure 8 illustrates the BIT MASKED TRANSFER functions.

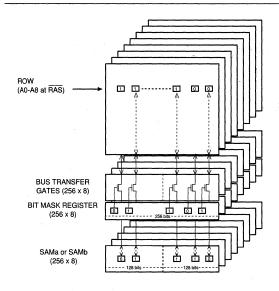


Figure 8
BIT MASK TRANSFER BLOCK DIAGRAM

BIT MASKED READ TRANSFER (BMRT)

BIT MASKED READ TRANSFER may be used to transfer any combination of the 2,048 bits contained in any DRAM row address to either of the two SAMs. The logic conditions and timing for the BMRT function are identical to the normal READ TRANSFER function except that TRM and DSF2 are HIGH select the BIT MASKED feature. If a bit in the BMR is a logic "1", the bus connection between the corresponding DRAM bit and the selected SAM bit is enabled and the data at the destination (one of the SAMs for BMRT) will be changed to the source data (the DRAM row for BMRT).

BIT MASKED SPLIT READ TRANSFER (BMSRT)

The BIT MASKED SPLIT READ TRANSFER operation is identical to the normal SPLIT READ TRANSFER except that the bit mask (stored in the bit mask register) is applied to the transfer data by taking TRM and DSF2 HIGH when \overline{RAS} falls. The remaining control timing is identical to the requirements for a normal SPLIT READ TRANSFER.

BIT MASKED WRITE TRANSFER (BMWT)

Like WRITE TRANSFER, the BIT MASKED WRITE TRANSFER function may be used to transfer data to any DRAM row address from either of the two SAM registers. In this case, the SAM data will be masked by the contents of the bit mask register before the data is written to the DRAM.

BIT MASKED SPLIT WRITE TRANSFER (BMSWT)

Like the other BIT MASKED TRANSFER cycles, the BMSWT is nearly identical to the SPLIT WRITE TRANSFER, except TRM and DSF2 are HIGH when \overline{RAS} falls. Two masks are applied during a BMSWT operation. Each of the individual bits are masked by the bit mask register and each of the DQ planes are masked by the DQ inputs at \overline{RAS} time. If a DQ input is LOW at \overline{RAS} time, none of the 128 SAM bits for that DQ plane will be transferred to the DRAM row-half selected. If a DQ input is HIGH, the 128 SAM bits for that row-half will be masked by the corresponding 128 mask register bits when written to the selected DRAM row-half. The remaining control timing is identical to the requirements for a normal SPLIT WRITE TRANSFER.

BIT MASK REGISTER OPERATIONS

This section describes how to transfer data to or from the Bit Mask Register (BMR) and how to clear the BMR's contents. Data may also be inverted when being transferred between the BMR and DRAM.

BMR READ TRANSFER (BMR-RT)

Any DRAM row may be transferred to the bit mask register by using the BMR READ TRANSFER function. When RAS falls, $\overline{TR}/(\overline{OE})$ is LOW to select a transfer cycle. TRM is HIGH to indicate that the BMR is involved in the TRANSFER cycle, and DSF2 is LOW to indicate that the data is to be transferred to the BMR (as opposed to using the contents of the BMR as bit mask data). The remainder of the timing and control required is identical to a normal READ TRANSFER cycle. No Tap address is loaded in this TRANSFER.

Note that the SAM transfer select (STS) pin is used to select whether non-inverted (STS = LOW) or inverted (STS = HIGH) data is transferred to the bit mask register. For all transfers to or from the bit mask register, the state of the MKD pin when \overline{RAS} falls selects whether the Serial Mask Input (SMI) feature is enabled (see the Functional Truth Table). SMI is a special serial input mode that allows mask information to be clocked into the BMR at the same address location as the data clocked into SAMb (see the SMI mode description). MKD is LOW when \overline{RAS} falls to disable SMI on HIGH to enable SMI. After the transfer is completed, the MKD pin then acts either as a mask data input to the BMF (SMI enabled) or is "don't care" (SMI disabled). The MKL input is tied to the 8 bit-planes, the data on the MKD pin is written to each bit-plane simultaneously.

BMR INVERTED READ TRANSFER (BMR-IRT)

If the STS pin is HIGH at \overline{RAS} time the DRAM data wil be inverted before being written to the BMR. All 2,048 bit involved in the transfer will be complemented. The functionality and logic levels for the other control inputs ar

MULTIPORT DRAM

identical to the BMR READ TRANSFER cycle. Note that MKD is still used to enable or disable the SMI mode. There is no added cycle time delay for either the BMR INVERTED READ or BMR INVERTED WRITE TRANSFER cycles.

BMR WRITE TRANSFER (BMR-WT)

The contents of the BMR may also be transferred to any DRAM row by using the BMR WRITE TRANSFER cycle. $(\overline{\text{ME}})/\overline{\text{WE}}$ and DSF2 are LOW and TRM is HIGH when $\overline{\text{RAS}}$ falls, to select a write transfer from the BMR. The DQ inputs are used to input a DQ bit-plane mask when $\overline{\text{RAS}}$ falls. This allows each of the four DQ planes to be write enabled or disabled during the BMR-WT. The MKD input is used to enable or disable the SMI mode. STS must be LOW at $\overline{\text{RAS}}$ time to transfer non-inverted BMR data to the DRAM row selected.

BMR INVERTED WRITE TRANSFER (BMR-IWT)

As with the BMR INVERTED READ TRANSFER, the 2,048 bits involved in the transfer may be inverted while being transferred. Taking STS HIGH at RAS time will cause the BMR data to be inverted before it is stored in the selected DRAM row. The other control and DQ (mask) inputs are the same as the BMR-WT.

SAM-TO-BMR TRANSFER (SAM-BMR)

The contents of either SAM may be transferred to the BMR in the same manner that a DRAM row is transferred. In this case, DSF1 is HIGH to indicate that the SAM is the source of the data instead of the DRAM. $(\overline{ME})/\overline{WE}$ is used to indicate the direction of the transfer and must be LOW, when RAS falls, for a SAM-TO-BMR TRANSFER. STS is no longer used to select between normal and inverted data, it now indicates which SAM is involved in the transfer. Since a SAM-TO-BMR TRANSFER "reads" data from the SAM, the SAM will be placed into input mode by this transfer cycle. The MKD input is still used to determine if the SMI mode will be enabled after the transfer is completed. Since no DRAM access is involved, it is not necessary to provide any particular ROW address at RAS time. However, whichever ROW address is present at RAS time will be used as the address for a RAS-ONLY REFRESH. Since a SAM is involved in the transfer, a new SAM starting address (or Γap) will be loaded at CAS time. This address will be loaded nto the serial address counter of the SAM selected by STS at RAS time.

Note:

Any SAM/BMR TRANSFER will take the SAM involved in the transfer out of the split SAM mode, if it was in that mode before the transfer.

BMR-TO-SAM TRANSFER (BMR-SAM)

The contents of the BMR may also be transferred to one of the SAM registers. The (ME)/WE input is used to indicate the direction of the transfer and must be HIGH for a BMR-TO-SAM TRANSFER. STS is LOW to select SAMa or HIGH to select SAMb as the destination for the BMR data. The remaining inputs and functionality are identical to the SAM-TO-BMR TRANSFER. Since a BMR-TO-SAMTRANSFER writes new data to the selected SAM register, the I/O for the SAM involved will be placed in the output mode and a new Tap address will be loaded when CAS falls.

CLEAR BIT MASK REGISTER (CLR-BMR)

The entire contents of the BMR can be cleared (set all bit LOW) within a single transfer cycle by performing a CLEAR BMR cycle. Unlike the other cycles that access the BMR, TRM is LOW at \overline{RAS} time for the CLEAR BIT MASK REGISTER function. $\overline{TR}/(\overline{OE})$ is LOW to indicate that the cycle is a transfer cycle (although there is really no data transfer involved). The CLR-BMR function is selected when $\overline{ME}/(\overline{WE})$, DSF1 and DSF2 are HIGH when RAS falls.

When the BMR is cleared, all data will be masked when a BIT MASKED TRANSFER cycle is performed.

The BMR INVERTED WRITE and BMR WRITE TRANS-FERS may be used with the CLR-BMR function to set or clear, respectively, any DRAM row. The CLR-BMR function is used to clear the BMR then the BMR TRANSFERS are performed to the addressed DRAM row.

The CLEAR BIT MASK REGISTER function is useful when using the SERIAL MASK INPUT mode. It is automatically performed (when in the SMI mode) when data is transferred from SAMb to the DRAM (see SERIAL MASK INPUT section).

SERIAL MASK INPUT (SMI)

Whenever the BMR is accessed, the MKD input is sensed and latched into the BMR control logic. If the MKD pin is LOW at \overline{RAS} time the Serial Mask Input (SMI) mode is disabled and the BMR may only be loaded via internal transfer cycles. If MKD is HIGH when \overline{RAS} falls, during a BMR access, then the BMR control logic enables the SMI mode and the BMR may be serially loaded via the MKD input.

When SMI is enabled, the MKD input is coupled to all eight of the bit mask register's DQ planes (see Figure 9). The SCb clock input and SAMb's address counter are used to input data to SAMb and the BMR. SEb will enable (LOW) or disable (HIGH) input data to SAMb and the BMR, the address count will increment regardless of the state of SEb.

The most common application of the SMI mode is to automatically load a transfer mask with the new data written to SAMb. To initialize the sequence, the BMR is cleared (CLR-BMR) with MKD = HIGH at \overline{RAS} time to

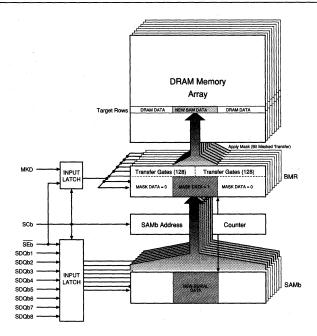


Figure 9
SERIAL-MASK-INPUT MODE BLOCK DIAGRAM

enable the SMI mode. Then SAMb is prepared to accept input data by performing PSEUDO WRITE TRANSFER. The SAM starting address loaded will also apply to the BMR. For every address location that to which data is written in SAMb, the corresponding address location in the BMR will be written to the value present on MKD (all eight planes of the BMR will be written). After the input of data to SAMb is complete, a BIT MASKED WRITE TRANSFER may be performed and only the unmasked data from SAMb will be transferred to the DRAM. The BMR will be cleared automatically after a BIT MASKED WRITE TRANSFER from SAMb, if the device is in the SMI mode. A BMSWT from SAMb will clear on half of the BMR. This allows a new mask to be loaded during the next fill of SAMb, without performing a CLR-BMR cycle. If data is to be masked during the BMWT, then MKD is held LOW when the corresponding SAMb data is written. If the data is to be written (unmasked) to the DRAM during the BMWT, then MKD is held HIGH when the corresponding SAMb location is written. The function of the MKD pin is dependent on the I/O direction of SAMb. MKD is an input only, if SMI is enabled and SAMb is in input mode. If SMI is enabled and SAMb is in output mode, the MKD input is a "don't care," and no new data may be written to the BMR via MKD. MKD is also "don't care" if the SMI mode is disabled. Note that the mask data loaded via SAMb may also be applied to a SAMa TRANSFER cycle, if the mask has not been cleared by a SAMb TRANSFER or a CLR-BMR cycle. The BMR will not be cleared after a TRANSFER involving SAMa.

POWER UP INITIALIZATION

When Vcc is initially supplied or when refresh is interrupted for more than 8ms the device must be initialized.

After Vcc is at specified operating conditions, for $100\mu s$ (minimum), eight \overline{RAS} cycles must be executed to initalize the dynamic memory array. When the device is initialized the DRAM I/O pins (DQs) are in a High-Z state, regardless of the state of $\overline{(TR)}/\overline{OE}$. The DRAM array will contain random data.

The SAM portion of the device is completely static and does not require an initialization cycle. Both SAM ports will power up in the serial input mode (WRITE TRANSFERs) and the SAM I/O pins (SDQ's) are in a High-Z state, regardless of the state of \$\overline{SE}\$ ab. Also, SPLITTRANSFER and SMI modes are disabled. Both QSF (MT43C8128) outputs may be in the High or LOW state. Both SAMs as well as bit mask, color, and DRAM mask registers all contain random data after power-up.



TRUTH TABLE 1

	et e e			RA	S FAL	LING	EDGE				CAS FALL	A0	-A82	DQ1-	DQ83	REGIS	STERS
CODE	FUNCTION	CAS	TR/OE	ME/WE 10	DSF1	DSF2	SEa,SEb	TRM	MKD	STS	DSF1	RAS	CAS, A8=X	RAS	CAS,WE4	MASK	COLOR
	DRAM OPERATIONS	۰	L				L		L	<u> </u>						L	
CBR	CAS-BEFORE-RAS REFRESH	0	Х	111	х	х	х	x	х	X	X	X	х	X	Х	-	T -
ROR	RAS-ONLY REFRESH	1	1	X	х	х	Х	x	х	×	_	ROW	_	Х	_	_	_
RW	NORMAL DRAM READ OR WRITE	1	1	. 1	0	011	X	Х	Х	Х	0	ROW	COLUMN	Х	VALID DATA	-	-
RWNM	NONPERSISTENT (LOAD AND USE) MASKED WRITE TO DRAM	1	1	0	0	011	х	х	X	x	0	ROW	COLUMN	WRITE	VALID DATA	LOAD & USE	-
RWOM	PERSISTENT (USE REGISTER) MASKED WRITE TO DRAM	1	1	0	1	011	Х	X	х	×	0	ROW	COLUMN	X	VALID DATA	USE	-
BW	BLOCK WRITE TO DRAM (NO DATA MASK)	1	1	1	0	011	x	Х	х	×	1	ROW	COLUMN (A2-A7)	Х	COLUMN MASK	-	USE
BWNM	NONPERSISTENT (LOAD & USE) MASKED BLOCK WRITE TO DRAM	1	1	0	0	011	х	х	X	х	1	ROW	COLUMN (A2-A7)	WRITE MASK	COLUMN MASK	LOAD & USE	USE
BWOM	PERSISTENT (USE MASK REGISTER) MASKED BLOCK WRITE TO DRAM	1	1	0	1	011	х	X	X	×	1	ROW	COLUMN (A2-A7)	X	COLUMN MASK	USE	USE
	REGISTER OPERATIONS													1.	N. 18		
LMR	LOAD MASK REGISTER	1	1	1	1	011	X	Х	х	×	0	X ⁵	х	Х	WRITE MASK	LOAD	_
LCR	LOAD COLOR REGISTER	1	1	1	.1	011	х	X	х	×	. 1	X ⁵	х	X	COLOR DATA		LOAD
	TRANSFER OPERATIONS																
RT	READ TRANSFER (DRAM-TO-SAM TRANSFER)	1	0	1	0	0	X	0	х	0=SAMa 1=SAMb		ROW	TAP ⁶	X	х	_	_
SRT ⁹	SPLIT READ TRANSFER (SPLIT DRAM-TO-SAM TRANSFER)	1	0	1	1	0	х	0	х	0=SAMa 1=SAMb		ROW	TAP ⁶	X	Х	_	-
WT	WRITE TRANSFER (SAM-TO-DRAM TRANSFER)	1	0	0	0	0	0	0	X	0=SAMa 1=SAMb		ROW	TAP ⁶	Х	Х	-	-
PWT	PSEUDO WRITE TRANSFER (SERIAL INPUT MODE ENABLE)	1	0	0	0	0	1	0	х	0=SAMa 1=SAMb		X ⁵	TAP ⁶	X	х	-	-
MSWT ⁹	SPLIT WRITE TRANSFER (SPLIT SAM- TO-DRAM TRANSFER DQ WITH MASK)	1:	0	0	1.1	0	х	0	X	0=SAMa 1=SAMb		ROW	TAP ⁶	DQ MASK	х	-	-
MWT	DQ MASKED WRITE TRANSFER	1	0	0	0	10	х	0	x	0=SAMa 1=SAMb		ROW	TAP ⁶	DQ MASK	х	_	-



TRUTH TABLE 1

				RA	Š FAL	LING E	DGE	- ;	9		CAS FALL	AO	-A8 ²	DQ1-	DQ8³	REGIS	TERS
CODE	FUNCTION	CAS	TR/OE	ME/WE 10	DSF1	DSF2	SEa, SEb	TRM	MKD	STS	DSF1	RAS	CAS, A8=X	RAS	CAS,WE ⁴	MASK	COLOR
	BIT MASK REGISTER OPERATIONS																
BMR- RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	-1	0	0	х	1	0/17	0	x	ROW	X	X	Х		
BMR- IRT	BMR READ TRANSFER (DRAM→INVERT→BMR TRANSFER)	1	0	1	0	0	х	1	0/17	1	x	ROW	X	х	x	_	<u> </u>
BMR- WT	BMR WRITE TRANSFER (BMRDRAM TRANSFER)	1	0	0	0	0	х	1	0/17	0	X	ROW	Х	DQ MASK	X	_	-
BMR- IWT	BMR WRITE TRANSFER (BMR→INVERT→DRAM TRANSFER)	1	0	0	0	0	×	1	0/17	1	Х	ROW	Х	DQ MASK	X	_	-
SAM- BMR	SAM→BMR TRANSFER	1	0	0	1	0	х	1	0/17	0=SAMa 1=SAMb		X ⁵	TAP ⁶	×	Х		
BMR- SAM	BMR→SAM TRANSFER	1	0	1	1	0	х	1	0/17	0=SAMa 1=SAMb		X ⁵	TAP ⁶	X	Х	-	-
CLR- BMR	CLEAR BIT MASK REGISTER (SETS BMR TO ALL "0's")	1	0	1	1	1	×	0	0/17	×	X	X ⁵	Х	Х	Х	-	-
	BIT MASKED TRANSFER OPERATIONS	3															
BMRT	BIT MASKED READ TRANSFER (BM DRAM-SAM TRANSFER)	1	0	1	0	1	X	1	Х	0=SAMa 1=SAMb		ROW	TAP ⁶	Х	Х	-	-
BMSRT ⁹	BIT MASKED SPLIT READ TRANSFER (BM SPLIT DRAM→SAM TRANSFER)	1	0	1	1	1	х	1	Х	0=SAMa 1=SAMb		ROW	TAP ⁶	х	х		
BMWT	BIT MASKED WRITE TRANSFER (BM SAM→DRAM TRANSFER)	1	0	0	0	1	х	1	X8	0=SAMa 1=SAMb		ROW	TAP ⁶	Х	х		_
BMSWT ⁹	BIT MASKED SPLIT WRITE TRANSFER (BM SPLIT SAM-DRAM TRANSFER)	1	0	0	1	1	X	1	X ₈	0=SAMa 1=SAMb		ROW	TAP ⁶	DQ MASK	×	_	_

- 1. $0 = LOW(V_{IL})$, $1 = HIGH(V_{IH})$, X = "don't care," = "not applicable."
- 2. These columns show what must be present on the A0-A8 inputs when RAS falls and A0-A7 when CAS falls.
- 3. These columns show what must be present on the DQ1-DQ8 inputs when RAS falls and when CAS falls.
- 4. With WRITE cycles, the input data is latched at the falling edge of CAS or ME/WE, whichever is later. Similarly, with READ cycles, the output data is enabled on the falling edge of CAS or TR/OE, whichever is later.
- 5. The row that is addressed will be refreshed, but no particular ROW address is required.
- 6. Tap Address; this is the SAM location that the first SC cycle will access. For SPLIT TRANSFERs, the half receiving the transfer is determined by the MSB of the internal address counter. The SAM half not currently being accessed will be the half receiving the transfer.
 Column address A7 is a "don't care" for SPLIT TRANSFERs.
- 7. The Serial Mask Input mode (SMI) is enabled ("1") or disabled ("0") when the BMR is accessed (see BMR OPERATIONS). If SMI is enabled (MKD = "1"), mask data is serially clocked into the BMR with SCb and the BMR is automatically cleared after a BIT MASKED WRITE or BIT MASKED SPLIT WRITE TRANSFER cycle from SAMb. For BIT MASKED READ TRANSFERs to any SAM and BIT MASKED WRITE TRANSFERs from SAMa, the BMR is not cleared automatically.
- 8. If the SMI mode is enabled, mask data is clocked into the BMR with SCb.
- 9. SPLIT TRANSFERs do not change SAM I/O direction.
- 10. SAM I/O direction is a function of the state of ME/WE at RAS time. If ME/WE is LOW, then the selected SAM is an input: if ME/WE is HIGH, then the SAM is an output (except for SPLIT TRANSFERS).
- 11. The MT43C8128/9 operates properly if this state is "X", but to allow for future functional enhancements it is recommended that they are driven as shown in the Truth Table.



ABSOLUTE MAXIMUM RATINGS*

 *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(0^{\circ}C \leq T_A \leq 70^{\circ}C)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.75	5.25	V	1
Input High (Logic 1) Voltage, All Inputs	ViH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	VIL	-1.0	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \le T_A \le 70^{\circ}C; Vcc = 5V \pm 5\%)$

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT Any input (0V ≤ Vin ≤ Vcc); all other pins not under test = 0V	1 . 1 . 1.	-10	10	μА	
OUTPUT LEAKAGE CURRENT (Dout is disabled, 0V ≤ Vout ≤ Vcc).	loz	-10	10	μА	
OUTPUT LEVELS Output High Voltage (Iout = -2.5mA)	Vон	2.4		٧	1
Output Low Voltage (IOUT = 2.5mA)	Vol		0.4	٧	

CAPACITANCE

 $T_A = 25^{\circ}C$

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, TRM, MKD	Cıı		5	pF	2
Input Capacitance: \overline{RAS} , \overline{CAS} , $\overline{ME/WE}$, $\overline{TR/OE}$, SCa,b , $\overline{SE}a,b$, DSF1,2, STS SSFa,b	Cı2		7	pF	2
Input/Output Capacitance: DQ, SDQa,b	Cı/o		9	pF	2
Output Capacitance: QSFa,b	Co	N 11 44	9	pF	2



DRAM CURRENT DRAIN; SAMa, SAMb and SERIAL MASK INPUT (SMI) INACTIVE

 $(0^{\circ}C \le T_{A} \le 70^{\circ}C; Vcc = 5V \pm 5\%)$

$(0.0 \le 1_A \le 70.0, \text{ VCC} = 5\text{ V} \pm 5\%)$		M.	AX		
PARAMETER/CONDITION	SYMBOL	-8	-10	UNITS	NOTES
OPERATING CURRENT (RAS and \overline{CAS} = Cycling; ${}^{t}RC = {}^{t}RC$ (MIN))	lcc1	105	95	mA	3, 4 25
OPERATING CURRENT: PAGE MODE (RAS = VIL CAS = Cycling; ¹PC = ¹PC (MIN))	Icc2	100	90	mA	3, 4 27
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS} = \overline{CAS} = V_{IH}$, after 8 \overline{RAS} cycles (MIN))	Іссз	10	10	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS = CAS = Vcc-0.2V, after 8 RAS cycles min). All other inputs ≥ Vcc -0.2V or ≤ Vss +0.2V	ICC4	2	2	mA	
REFRESH CURRENT: RAS-ONLY (RAS = Cycling; CAS = VIH)	lcc5	110	100	mA	3, 26
REFRESH CURRENT: \overline{CAS} -BEFORE- \overline{RAS} (\overline{RAS} and \overline{CAS} = Cycling)	Icc6	110	100	mA	3, 5 26
TRANSFER CURRENT: SAM/DRAM DATA TRANSFER	Icc7	105	95	mA	3

SERIAL PORT CURRENT DRAIN; SAMa, SAMb and/or SMI MODE

(Notes 3, 4) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 5%)

		141	nn .	1	
PARAMETER/CONDITION	SYMBOL	-8	-10	UNITS	NOTES
OPERATING CURRENT: SERIAL PORT (SAMa/SAMb) (SCa/SCb = Cycling; [†] SC = [†] SC (MIN); SEa/SEb = V _{IL})	Iccs	45	40	mA	
OPERATING CURRENT: SMI MODE (SAMb) (SCb = Cycling; ^t SC = ^t SC (MIN); SEb = V _{IL})	Icc9	20	20	mA	
STANDBY CURRENT: SERIAL PORT (SAMa/SAMb) Power supply standby current (SCa/SCb = ViH or VIL; SEa/SEb = VIH)	Icc10	0	0	mA	
STANDBY CURRENT: SMI MODE (SAMb) Power supply standby current (SCb = Vih or Vil.; SEb = Vih)	Icc11	0	0	mA	

TOTAL CURRENT DRAIN

(Notes 3, 4) (0°C \leq T_A \leq 70°C; Vcc = 5V \pm 5%)

ICC(TOTAL)	= DRAM CURRENT (Icc1-7) + SAMa CURRENT (Icc8 or Icc10) + SAMb CURRENT (Icc8 or Icc10) +
	SMI CURRENT (Icce or Icc11) [+ 10mA (If DRAM CURRENT = Icc3 or Icc4)]

Example 1:

Operating current (-8) with DRAM operating in Fast Page Mode, SAMa active, SAMb and SMI inactive:

ICC(TOTAL)	= DRAM CURRENT (Icc2) + SAMa C	CURRENT (Iccs) + SAMb CURRENT (Icc10) +	 	1.00
	SMI CURRENT (Icc11) [+ 0]			
	= 100 + 45 + 0 + 0 = 145mA (MAX)			

Example 2:

Operating current (-10) with DRAM operating in CMOS Standby, SAMa and SAMb active, SMI active:

ICC(TOTAL)	= DRAM CURRENT (Icc4) + SAMa CURRENT (Icc8)) + SAMb CURRENT (Iccs) +	
	SMI CURRENT (Icce) [+ 10]		
	= 2 + 40 + 40 + 20 + 10 = 112mA (MAX)		

MAX



DRAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C \leq T_A \leq +70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS			-8		-10	ļ	
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	150		180		ns	
READ-MODIFY-WRITE cycle time	tRWC	205		235	1 2 2	ns	
FAST-PAGE-MODE READ or WRITE	tPC	50		50		ns	
cycle time							
FAST-PAGE-MODE READ-MODIFY-	^t PRWC	95		120		ns	
WRITE cycle time		k i tot	9 1 2 2				
Access time from RAS	tRAC		80		100	ns	14, 17
Access time from CAS	tCAC		20		25	ns	15
Access time from (TR)/OE	‡ŌE		20		25	ns	
Access time from column address	^t AA		40		50	ns	
Access time from CAS precharge	^t CPA		45		55	ns	
RAS pulse width	tRAS	80	20,000	100	20,000	ns	
RAS pulse width (FAST PAGE MODE)	†RASP	80	100,000	100	100,000	ns	
RAS hold time	^t RSH	20		25		ns	
RAS precharge time	tRP	60		70		ns	
CAS pulse width	†CAS	20	10,000	25	10,000	ns	
CAS hold time	t _{CSH}	80		100		ns	
CAS precharge time	^t CP	10		10		ns	16
RAS to CAS delay time	tRCD	20	60	25	75	ns	17
CAS to RAS precharge time	^t CRP	5		5		ns	
Row address setup time	t _{ASR}	0		0		ns	
Row address hold time	^t RAH	12		15		ns	
RAS to column	^t RAD	17	40	20	50	ns	18
address delay time		A					
Column address setup time	†ASC	0		0		ns	
Column address hold time	†CAH	15		20		ns	
Column address hold time	†AR	60		70		ns	
(referenced to RAS)					1 1 1		
Column address to	†RAL	40		50		ns	
RAS lead time							
Read command setup time	tRCS	0		0		ns	
Read command hold time	^t RCH	0		0		ns	19
(referenced to CAS)							
Read command hold time	^t RRH	0		0	1 2 2 2	ns	19
(referenced to RAS)						34, 1	
CAS to output in Low-Z	^t CLZ	3		3		ns	
Output buffer turn-off delay	^t OFF	3	20	3	20	ns	20, 23
Output disable	t _{OD}	3	10	3	20	ns	20, 23
Output disable hold time from start of WRITE	†OEH	15		15	1	ns	28
Output Enable to RAS delay	tORD	0	1	0	-	ns	

DRAM TIMING PARAMETERS (continued)

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq +70$ °C; Vcc = 5V ± 5 %)

AC CHARACTERISTICS		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Write command setup time	twcs	0		0		ns	21
Write command hold time	tWCH	15		20		ns	
Write command hold time (referenced to RAS)	tWCR	60		75		ns	
Write command pulse width	tWP	15		15		ns	
Write command to RAS lead time	tRWL	20		25		ns	
Write command to CAS lead time	tCWL	20		25		ns	
Data-in setup time	t _{DS}	0		0		ns	22
Data-in hold time	^t DH	20		20		ns	22
Data-in hold time (referenced to RAS)	tDHR	60		70		ns	
RAS to WE delay time	tRWD	100		130	†	ns	21
Column address to WE delay time	tAWD .	60		80		ns	21
CAS to WE delay time	tCWD	40		60		ns	21
Transition time (rise or fall)	t _T	3	35	3	35	ns	9, 10
Refresh period (512 cycles)	tREF.		8		8	ms	
RAS to CAS precharge time	^t RPC	0		0		ns	
CAS setup time (CAS-BEFORE-RAS refresh)	tCSR	.10		10		ns	5
CAS hold time (CAS-BEFORE-RAS refresh)	tCHR	30		30		ns	5
ME/WE to RAS setup time	tWSR	0		0	1	ns	
ME/WE to RAS hold time	tRWH	15		15		ns	
Mask data to RAS setup time	tMS	0 .		0	1.0	ns	
Mask data to RAS hold time	tMH.	15		15		ns	1 1 2 2



TRANSFER AND MODE CONTROL TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-8		-10		100	1
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTE
TR/(OE) LOW to RAS setup time	tTLS	0		0		ns	136.47
TR/(OE) LOW to RAS hold time	tTLH	15	10,000	15	10,000	ns	1 2
TR/(OE) LOW to RAS hold time (REAL-TIME READ TRANSFER only)	^t RTH	70	10,000	80	10,000	ns	
TR/(OE) LOW to CAS hold time (REAL-TIME READ TRANSFER only)	^t CTH	20		25		ns	
TR/(OE) HIGH to SC lead time	^t TSL	5		5		ns	
TR/(OE) HIGH to RAS precharge time	tTRP	60		70		ns	
TR/(OE) precharge time	^t TRW	25		30		ns	W 1777
First SC edge to TR/(OE) HIGH delay time	tTSD	15		15	100000	ns	
RAS to first SC edge delay time	tRSD	80		95		ns	1.57
CAS to first SC edge delay time	tCSD	25		30		ns	
Serial output buffer turn-off delay from RAS	tSDZ	10	50	10	50	ns	J-61
SC to RAS setup time	tSRS	30		30		ns	
Serial data input to SE delay time	tSZE	0		0		ns	
RAS to SD buffer turn-on time	tSRO	10		15		ns	
Serial data input delay from RAS	tSDD	60		60		ns	
Serial data input to RAS delay time	tSZS	0		0		ns	
Serial Input Mode enable (SE) to RAS setup time	[†] ESR	0		0		ns	
Serial Input Mode enable (SE) to RAS hold time	†REH	15		15		ns	3,350
TR/(OE) HIGH to RAS setup time	tYS	0		0		ns	
TR/(OE) HIGH to RAS hold time	tYH	15		15		ns	
DSF, TRM, STS, MKD to RAS setup time	tFSR	0		0		ns	
DSF, TRM, STS, MKD to RAS hold time	^t RFH	15		15		ns	
DSF to RAS hold time	tFHR	60		65		ns	10.00
DSF to CAS setup time	tFSC	0		0		ns	
DSF to CAS hold time	^t CFH	15		20		ns	
SC to QSF delay time	tSQD		35		40	ns	29
RAS to QSF delay time	^t RQD		65		85	ns	29
CAS to QSF delay time	^t CQD		35		40	ns	29
TR/OE to QSF delay time	[†] TQD		25		30	ns	29
SPLIT TRANSFER setup time	tSTS	30		35		ns	29
SPLIT TRANSFER hold time	tSTH t	0		0		ns	29



SAM TIMING PARAMETERS

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 6, 7, 8, 9, 10) (0° C \leq T_A \leq + 70°C; Vcc = 5V \pm 5%)

AC CHARACTERISTICS		-8		-10		7	T
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Serial clock cycle time	tsc	28		30		ns	
Access time from SC	tSAC		25		27	ns	24, 31
SC precharge time (SC LOW time)	^t SP	10		10		ns	
SC pulse width (SC HIGH time)	^t SAS	10		10		ns	
Access time from SE	tSEA		15		20	ns	24
SE precharge time	^t SEP	10	1	15		ns	
SE pulse width	^t SE	10		15		ns	
Serial data out hold time after SC HIGH	^t SOH	5		5		ns	24, 31
Serial output buffer turn-off delay from SE	^t SEZ	3	12	3	15	ns	20, 24
Serial data in setup time	tSDS	0	1	0		ns	24
Serial data in hold time	tSDH	10		10		ns	24
Serial mask data in setup time	t _{MDS}	0		0	1.14	ns	
Serial mask data in hold time	tMDH	10		10		ns	
SERIAL INPUT (Write) Enable setup time	tsws	0		0		ns	
SERIAL INPUT (Write) Enable hold time	^t SWH	15		15		ns	
SERIAL INPUT (Write) disable setup time	tswis	0		0		ns	
SERIAL INPUT (Write) disable hold time	tSWIH	15		15		ns	
SSF to SC setup time	^t SFS	0		0		ns	30
SSF to SC hold time	^t SFH	15		20		ns	30
SSF LOW to SC HIGH delay	tSFD	5		5		ns	30

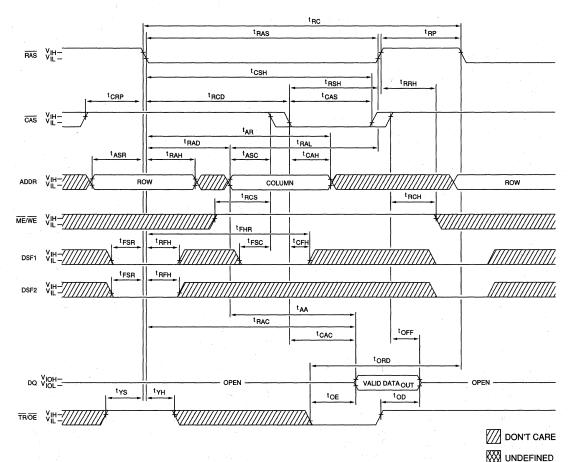


NOTES

- 1. All voltages referenced to Vss.
- 2. This parameter is sampled. $Vcc = 5V \pm 5\%$, f = 1 MHz.
- 3. Icc is dependent on cycle rates.
- Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
- 5. Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
- 7. An initial pause of 100µs is required after power-up followed by any 8 RAS cycles before proper device operation is assured. The 8 RAS cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
- 8. AC characteristics assume ${}^{t}T = 5ns$.
- VIH MIN and VIL MAX are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH). Input signals transition between 0V and 3V for AC testing.
- 10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIH (or between VIH and VIH) in a monotonic manner.
- 11. If CAS = VIH, DRAM data outputs (DQ1-DQ8) is High-Z.
- 12. If CAS = VIL, DRAM data outputs (DQ1-DQ8) may contain data from the last valid READ cycle.
- 13. DRAM output timing measured with a load equivalent to 1 TTL gate and 50pF. Output reference levels: VoH = 2.0V; VoL = 0.8V.
- 14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
- 15. Assumes that ${}^{t}RCD \ge {}^{t}RCD$ (MAX).
- 16. If CAS is LOW at the falling edge of RAS, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for ^tCP.
- 17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
- 18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
- Either ^tRCH or ^tRRH must be satisfied for a READ cycle.

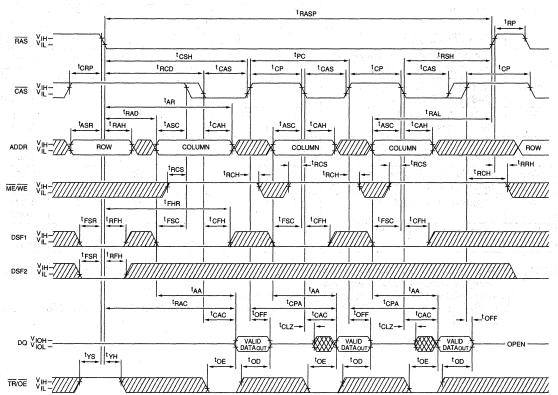
- 20. ^tOD, ^tOFF and ^tSEZ define the time when the output achieves open circuit (VoH -200mV, Vol. +200mV). This parameter is sampled and not 100% tested.
- 21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE-WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle, regardless of $\overline{TR}/\overline{OE}$. If ${}^{t}WCS \leq$ tWCS (MIN), the cycle is a LATE-WRITE and TR/OE must control the output buffers during the WRITE to avoid data contention. If tRWD ≥ tRWD (MIN), ${}^{t}AWD \ge {}^{t}AWD$ (MIN) and ${}^{t}CWD \ge {}^{t}CWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of the output buffers (at access time and until CAS goes back to VIH) is indeterminate but the WRITE will be valid, if tOD and tOEH are met. See the LATE-WRITE AC Timing diagram.
- These parameters are referenced to CAS leading edge in early WRITE cycles and ME/WE leading edge in late WRITE or READ-WRITE cycles.
- 23. During a READ cycle, if TR/OE is LOW then taken HIGH, DQ goes open. The DQs will go open with OE or CAS, whichever goes HIGH first.
- 24. SAM output timing is measured with a load equivalent to 1 TTL gate and 30pF. Output reference levels: Voh = 2.0V; Vol = 0.8V.
- 25. Addresses (A0-A8) change two times or less while $\overline{RAS} = V_{IL}$.
- 26. Addresses (A0-A8) change once or less while $\overline{RAS} = L$.
- 27. Addresses (A0-A8) change once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
- 28. LATE-WRITE and READ-MODIFY-WRITE cycles must have ^tOD and ^tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide previously read data if CAS remains LOW and OE is taken LOW after ^tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
- 29. Applies to the MT43C8128 only.
- 30. Applies to the MT43C8129 only.
- 31. 'SAC is MAX at 70° C and 4.75V Vcc; 'SOH is MIN at 0°C and 5.25V Vcc. These limits will not occur simultaneously at any given voltage or temperature 'SOH = 'SAC output transition time; this is guaranteed by design.

DRAM READ CYCLE





DRAM FAST PAGE MODE READ CYCLE



DON'T CARE

W UNDEFINED

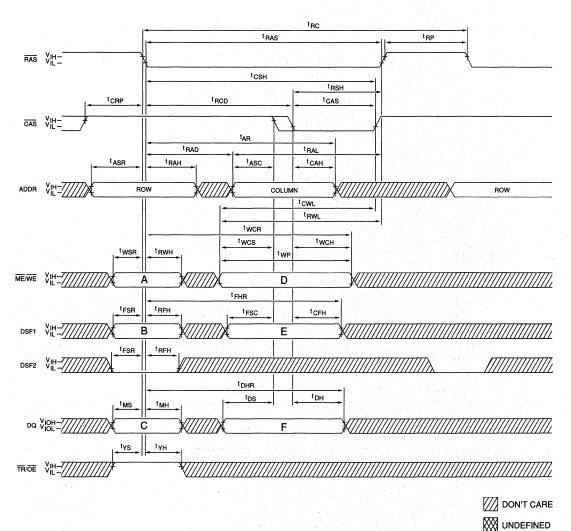
WRITE CYCLE FUNCTION TABLE 1

		LOGIC STATES ²							
1		1	RAS Falling	Edge	CAS Falling Edge				
CODE	FUNCTION	A ME/WE	B DSF1	C DQ (Input)	D ME/WE	E DSF1	F DQ (Input)		
RW	Normal DRAM WRITE	1	0	Х	0	0	DRAM		
RWNM	NONPERSISTENT (Load and Use) MASKED WRITE to DRAM	0	0	Write Mask	0/13	0	DRAM (Masked)		
RWOM	PERSISTENT (Use Register) MASKED WRITE to DRAM	0	1	X	0/1 ³	0	DRAM (Masked)		
BW	BLOCK WRITE to DRAM (No DQ Mask)	1	0	Х	0/1 ³	1	Column Mask		
BWNM	NONPERSISTENT (Load and Use) MASKED BLOCK WRITE to DRAM	0	0	Write Mask	0/1 ³	1	Column Mask		
BWOM	PERSISTENT (Use Register) MASKED BLOCK WRITE to DRAM	0	1	Х	0/1 ³	1	Column Mask		
LMR	Load Mask Data Register	1	1	Х	0/1 ³	0	Write Mask		
LCR	Load Color Register	1	1	Х	0/1 ³	1	Color Mask		

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E" and "F" for the WRITE cycle timing diagrams on the following pages.
- 2. TRM, MKD and STS are "don't care" for all WRITE cycles.
- 3. If ME/WE is LOW, an EARLY-WRITE is performed; if it is HIGH, a LATE-WRITE is performed if ME/WE falls after CAS.

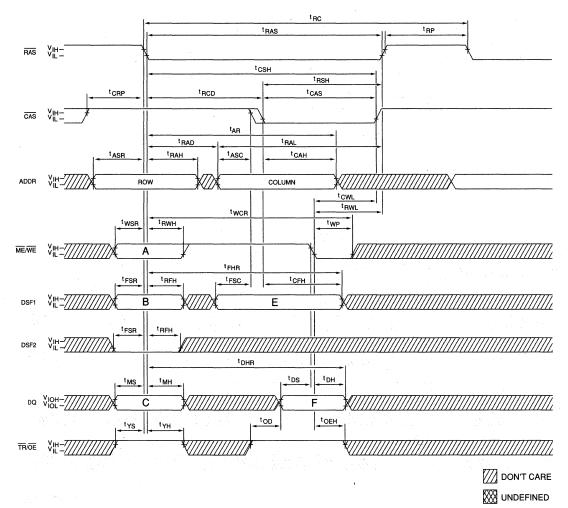


DRAM EARLY-WRITE CYCLE



NOTE: The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the WRITE Cycle Function Table for a detailed description.

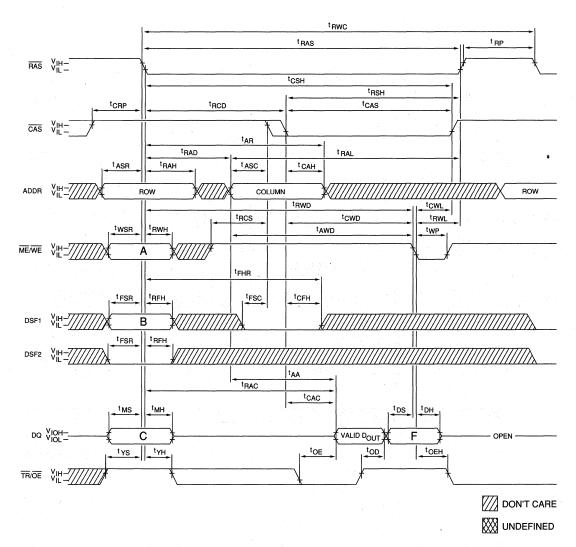
DRAM LATE-WRITE CYCLE 1



NOTE: 1. The logic states of "A", "B", "C", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

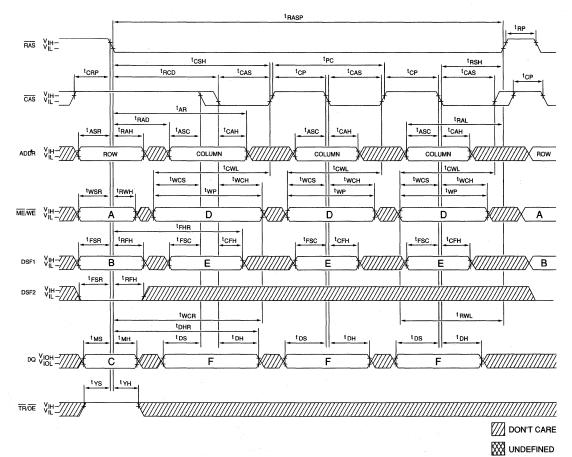


DRAM READ-WRITE CYCLE (READ-MODIFY-WRITE CYCLE)



NOTE: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.

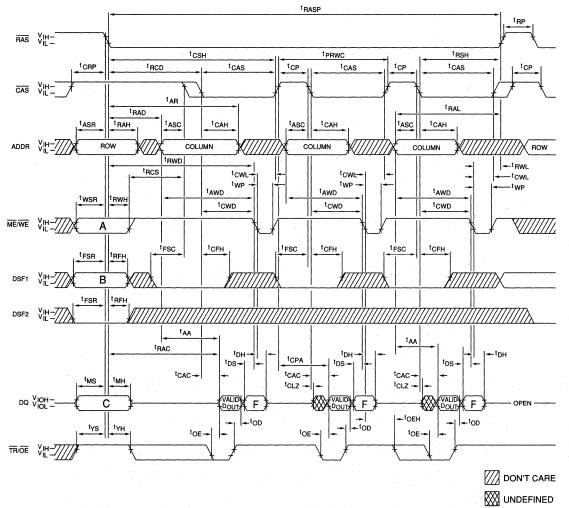
DRAM FAST-PAGE-MODE EARLY-WRITE CYCLE 1,2



- READ cycles or READ-MODIFY-WRITE cycles may be mixed with WRITE cycles while in FAST PAGE MODE.
- 2. The logic states of "A", "B", "C", "D", "E" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.



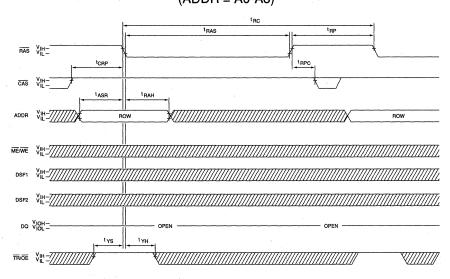
DRAM FAST-PAGE-MODE READ-WRITE CYCLE (READ-MODIFY-WRITE or LATE-WRITE CYCLES)



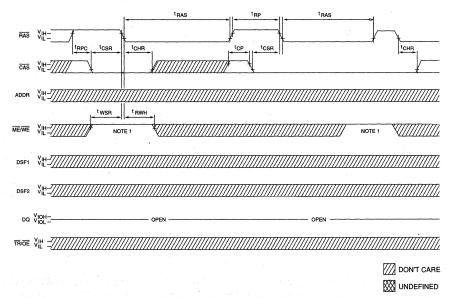
- READ or WRITE cycles may be mixed with READ-MODIFY-WRITE cycles while in FAST PAGE MODE. Use the Write Function Table to determine the proper DSF1 state for the desired WRITE operation.
- 2: The logic states of "A", "B", "C" and "F" determine the type of WRITE operation performed. See the Write Cycle Function Table for a detailed description.



DRAM RAS-ONLY REFRESH CYCLE (ADDR = A0-A8)

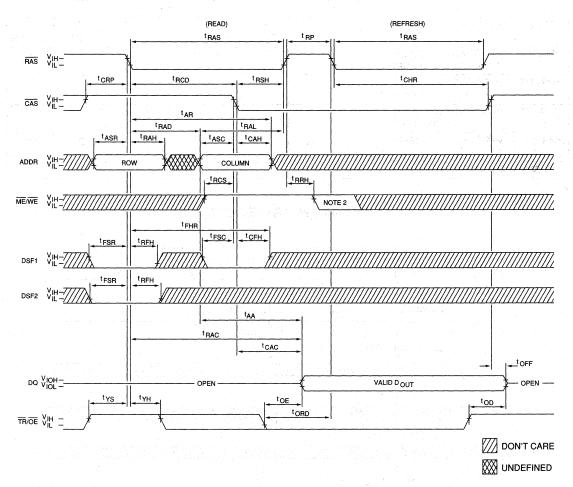


CAS-BEFORE-RAS REFRESH CYCLE



NOTE: 1. The MT43C8128/9 operates with this state as "don't care," but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

DRAM HIDDEN-REFRESH CYCLE



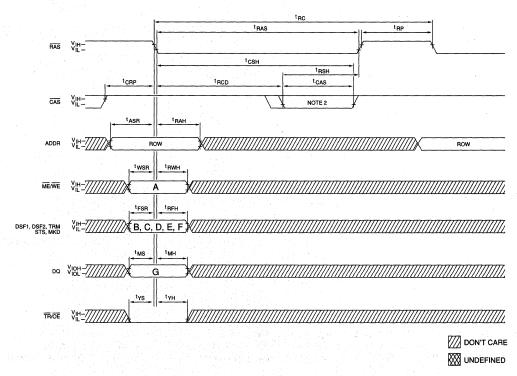
- 1. A HIDDEN REFRESH may also be performed after a WRITE or TRANSFER cycle. In the WRITE case, ME/WE = LOW (when CAS goes LOW) and TR/OE = HIGH and the DQ pins stay HIGH-Z. In the TRANSFER case, TR/OE = LOW (when RAS goes LOW) and the DQ pins stay High-Z during the refresh period, regardless of TR/OE.
- 2. The MT43C8128/9 operates with this state as "don't care," but to allow for future functional enhancements it is recommended that they be driven as illustrated for system upgradability.

DRAM/BMR TRANSFER CYCLE FUNCTION TABLE 1

MICHON

					LOGIC STA	TES			
		RAS Falling Edge							
CODE	FUNCTION	A ME/WE	B DSF1	C DSF2	D TRM	E STS	F MKD	G DQ(Input)	
BMR-RT	BMR READ TRANSFER (DRAM→BMR TRANSFER)	1	0	0	1	0	0/11	Х	
BMR-IRT	BMR READ TRANSFER (DRAM→invert→BMR TRANSFER)	1	0	0	1	1	0/11	Х	
BMR-WT	BMR WRITE TRANSFER (BMR→DRAM TRANSFER)	0	0	0	1	0	0/11	Mask	
BMR-IWT	BMR WRITE TRANSFER (BMR→invert→DRAM TRANSFER)	0	0	. 0	1	1	0/11	Mask	
CLR-BMR	CLEAR BMR (CLR-BMR)	1	1	1	0	Х	0/11	Х	

DRAM/BMR TRANSFERS



NOTE: 1. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

2. It is not necessary to drop CAS during a DRAM/BMR TRANSFER.



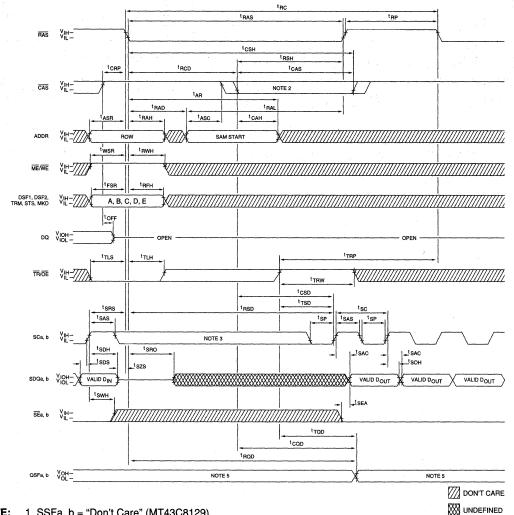
READ TRANSFER CYCLE FUNCTION TABLE 1

		LOGIC STATES RAS Falling Edge							
CODE	FUNCTION	A DSF1	B DSF2	C TRM	D STS	E MKD			
RW	READ TRANSFER	0	0	0	0/12	X			
SRT	SPLIT READ TRANSFER (DRAM→SAM)	1	0	0	0/12	Х			
BMRT	BIT MASKED READ TRANSFER	0	1	1	0/12	Х			
BMSRT	BIT MASKED SPLIT READ TRANSFER	1	1: -	1	0/12	Х			
BMR-SAM	BMR→SAM TRANSFER	1	0	1	0/12	0/1 ³			

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D" and "E" for READ TRANSFER cycle timing diagrams on the following pages.
- The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when STS = HIGH, the transfer is to SAMb.
- 3. Serial Mask Input mode is enabled if MKD = HIGH; disabled if MKD = LOW.

READ TRANSFER 1, 4 (DRAM-TO-SAM TRANSFER)

(When part was previously in the SERIAL INPUT mode)

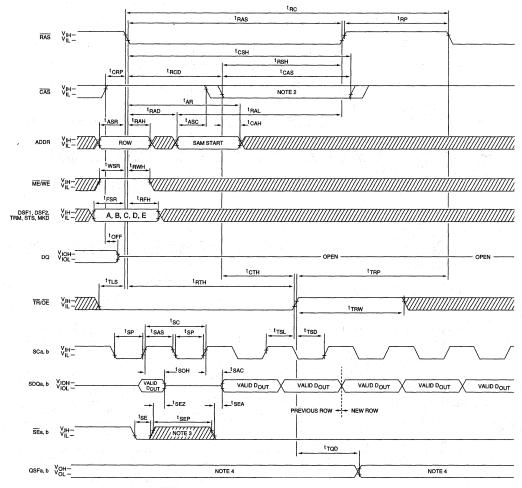


- 1. SSFa, b = "Don't Care" (MT43C8129)
- 2. CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.
- 3. There must be no rising edges on the SC input during this time period.
- 4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
- 5. QSF = 0 when the Lower SAM (bits 0-127) is being accessed. QSF = 1 when the Upper SAM (bits 128-255) is being accessed.



REAL-TIME READ TRANSFER 1, 4 (DRAM-TO-SAM TRANSFER)

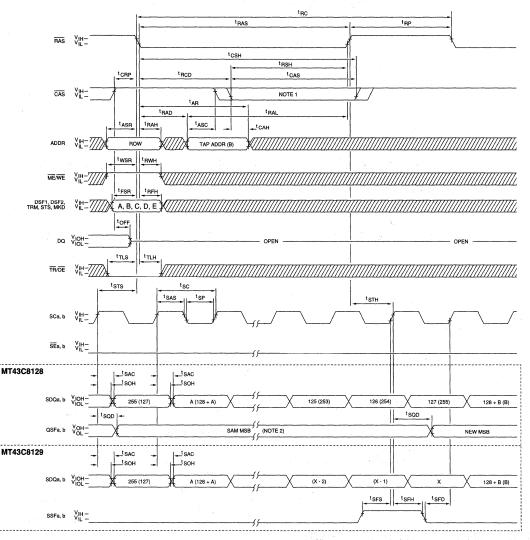
(When part was previously in the SERIAL OUTPUT mode)



DON'T CARE
UNDEFINED

- 1. SSFa, b = "Don't Care" (MT43C8129)
- CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed.
- 3. The SE pulse is shown to illustrate the serial output enable and disable timing. It is not required.
- 4. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.
- QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.

SPLIT READ TRANSFER³ (SPLIT DRAM-TO-SAM TRANSFER)



DON'T CARE

NOTE:

 CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused for the idle half.

W UNDEFINED

- QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed.
- 3. The logic states of "A", "B", "C", "D" and "E" determine the type of TRANSFER operation performed. See the Read Transfer Cycle Function Table.



WRITE TRANSFER CYCLE FUNCTION TABLE 1

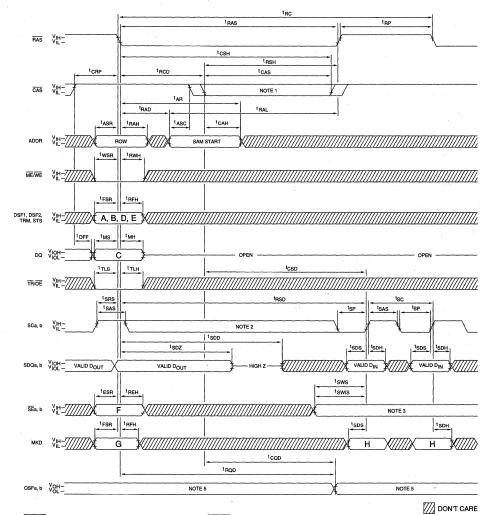
					LOGIC	STATES			
		RAS Falling Edge							SC
CODE	FUNCTION	A DSF1	B DSF2	C DQ	D TRM	E STS	F SE	G MKD	H MKD
WT	WRITE TRANSFER (SAM→DRAM)	0	0	Х	0	0/12	0	Х	-
PWT	PSEUDO WRITE TRANSFER	0	0	х	0	0/12	1	Х	-
MSWT	DQ MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	0	Mask	0	0/12	Х	X	- -
MWT	DQ MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Mask	0	0/12	Х	Х	-
BMWT	BIT MASKED WRITE TRANSFER (SAM→DRAM)	0	1	Х	1	0/12	Х	Х	0/14
BMSWT	BIT MASKED SPLIT WRITE TRANSFER (SAM→DRAM)	1	1	Mask	1	0/12	Х	Х	0/14
SAM-BMR	(SAM→BMR) TRANSFER	1	0	Х	1	0/12	Х	0/13	-

NOTE:

- 1. Refer to this function table to determine the logic states of "A", "B", "C", "D", "E", "F", "G" and "H" for WRITE TRANSFER cycle timing diagrams on the following pages.
- 2. The state of STS at the falling edge of RAS determines the SAM involved in the transfer. When STS = LOW, the transfer is to SAMa; when SAM = HIGH, the transfer is to SAMb.
- 3. Serial Mask Input (SMI) mode is enabled if MKD = HIGH and disabled if MKD = LOW.
- 4. When in the SMI mode (see BMR transfer waveforms) MKD is the SMI data input. MKD data is clocked into all bit planes of the bit mask register with SCb. A logic "1" on MKD will allow data to pass through all the mask; a logic "0" will mask the corresponding location of the SAM during a BIT MASKED TRANSFER. BIT MASKED TRANSFERs to or from SAMa must not take place while mask data is being serially input via SCb and MKD.



WRITE TRANSFER 4 (When part was previously in the SERIAL OUTPUT mode)



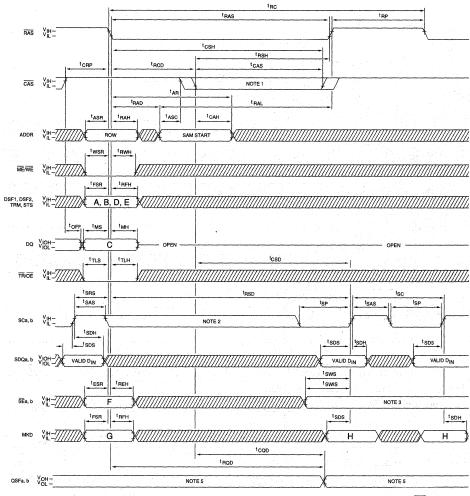
NOTE:

- CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.
- 2. There must be no rising edges on the SC input during this time period.
- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless
 of SE.
- 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
- QSF = 0 when the Lower SAM (bits 0-127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128-255) is being accessed. SSFa,b = "don't care" (MT43C8129).

₩ UNDEFINED



WRITE TRANSFER 4 (When part was previously in the SERIAL INPUT mode)



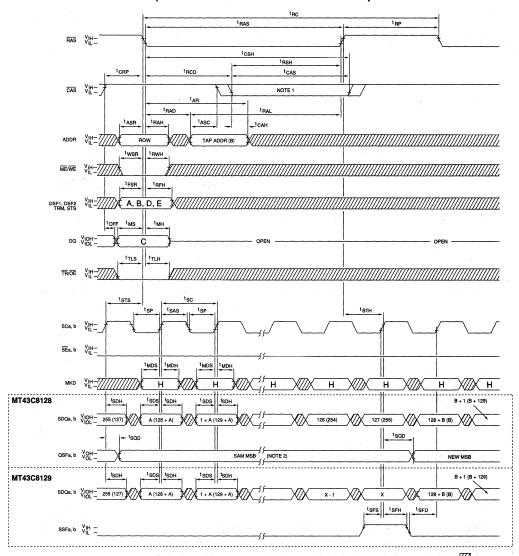
DON'T CARE
UNDEFINED

OTE:

 CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.

- SE must be LOW to input new serial data, but the serial address register is incremented by SC regardless of SE.
- 3. There must be no rising edges on the SC input during this time period.
- 4. The logic states of "A", "B", "C", "D", "E", "F", "G" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.
- QSF = 0 when the Lower SAM (bits 0–127) is being accessed.
 QSF = 1 when the Upper SAM (bits 128–255) is being accessed. SSFa,b = "don't care" (MT43C8129).

SPLIT WRITE TRANSFER 3 (SPLIT SAM-TO-DRAM TRANSFER)



NOTE:

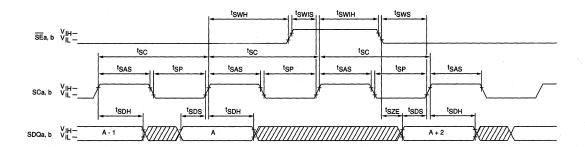
- 1. CAS is used to load the Tap address. If CAS does not fall, the last Tap address loaded for the addressed SAM will be reused.
- 2. QSF = 0 when the Lower SAM (bits 0-127) is being accessed. QSF = 1 when the Upper SAM (bits 128-255) is being accessed.
- 3. The logic states of "A", "B", "C", "D", "E" and "H" determine the type of TRANSFER operation performed. See the Write Transfer Cycle Function Table.

DON'T CARE

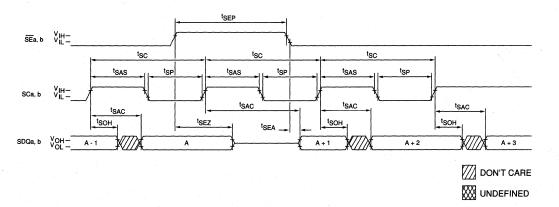
W UNDEFINED



SAMa or SAMb SERIAL INPUT



SAMa or SAMb SERIAL OUTPUT



OTE: SEa, SCa and SDQa are used when accessing SAMa and SEb; SCb and SDQb are used when access in SAMb.



TRIPLE PORT DRAM

256K x 8 DRAM WITH DUAL 512 x 8 SAMS

FEATURES

- Three asynchronous, independent, data access ports
- Fast access times 60ns random, 15ns serial
- Operation and control compatible with 2 Meg VRAMS
- High-performance, CMOS silicon-gate process
- Low power: 15mW standby; 450mW active, typical
- 512-cycle refresh within 8ms
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- FAST PAGE MODE with Extended Data Out (^tPC = 30ns)
- Two bidirectional serial access memories (SAMs)
- Fully static SAMs and Mask Register, no refresh required
- 4,096-bit Transfer Mask Register

SPECIAL FUNCTIONS

- MASKED WRITE (Write-Per-Bit)
- BLOCK WRITE
- SPLIT READ AND SPLIT WRITE TRANSFERS
- PROGRAMMABLE SPLIT SAMs
- BIT MASKED TRANSFERS
- SERIAL MASK DATA INPUT mode

OPTIONS

MARKING

 Timing [DRAM, SAMs (cycle/acces 	s)]
60ns, 20ns/15ns	- 6
70ns, 25ns/20ns	- 7
80ns, 28ns/25ns	- 8

Packages

Plastic SOP (550 mil)

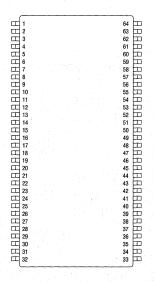
SG

GENERAL DESCRIPTION

The MT43C256K8A1 is a high speed, triple port CMOS dynamic random access memory (TPDRAM) containing 2,097,152 bits. Data may be accessed by an 8 bit wide DRAM port or by either of two independently-clocked 512 x 8-bit serial access memory (SAM) ports. Data may be transferred bidirectionally between the DRAM and the SAMs.

The DRAM portion of the TPDRAM is functionally idenical to the MT4C4256 (256K x 4) DRAM. Sixteen 256-bit lata registers make up the serial access memory portions of he TPDRAM. Data I/O and internal data transfer are accomplished using five separate bidirectional data paths; he 8-bit random access I/O port, a pair of internal 2,048 bit

PIN ASSIGNMENT (Top View) 64-Pin SOP*



*Pinouts to be determined

wide paths between the DRAM and the SAMs, and the pair of 8-bit serial I/O ports for the SAMs. The rest of the circuitry consists of the control, timing, and address decoding logic.

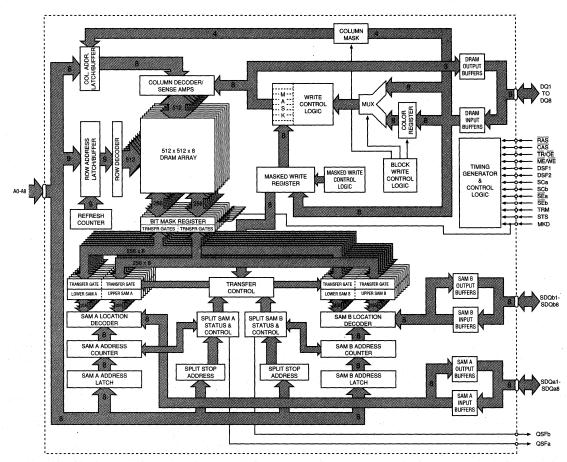
All three ports may be operated asynchronously and independently of the others except when data is being internally transferred between the DRAM and either SAM.

Each of the 4,096 bits involved in an internal transfer may be individually masked by performing a BIT MASKED TRANSFER operation. The 512×8 -bit, bit mask data register can be parallel loaded from the DRAM or either SAM, or it may be serial loaded through the MKD serial input.

As with all DRAMs, the TPDRAM must be refreshed to maintain data. The refresh cycles must be timed so that all 512 combinations of \overline{RAS} addresses are executed at least every 8ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity. An internal transfer between the DRAM and either SAM counts as a refresh cycle. The SAM portions of the TPDRAM are fully static and do not require any refresh.

The operation and control of the MT43C256K8A1 are optimized for high performance graphics and communication designs. The triple port architecture is well suited to buffering the sequential data types used in rastor graphics display, video windowing, serial and parallel networking and data communications. Special features, such as SPLIT TRANSFER, BIT MASKED TRANSFERS and BLOCK WRITE allow further enhancements to system performance.

FUNCTIONAL BLOCK DIAGRAM



MICHON TECHNOLOGY, INC.

DYNAMIC RAMS	
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9



APPLICATION/TECHNICAL NOTE SELECTION GUIDE

Technical Note	Title	Page				
TN-00-01	Moisture Absorption in Plastic Packages	6-1				
TN-00-02	Micron Tape and Reel Procedures	6-3				
TN-04-01	DRAM Power-Up and Refresh Constraints	6-9				
TN-04-02	MT4C1664 and MT4C1665 Compatibilities	6-11				
TN-04-03	MT4C1664: 256 Kilobyte Memory System with Four RAS Lines	6-13				
TN-04-04	MT4C1664: 256 Kilobyte Memory System with Four CAS Lines	6-15				
TN-04-06	DRAM OE Controlled/LATE-WRITE Cycles	6-17				
TN-04-08	DRAM Timing Parameters	6-19				
TN-04-09	LPDRAM BBU Current vs. RAS Active Time (1 Meg)	6-21				
TN-04-12	LPDRAM BBU Current vs. RAS Active Time (4 Meg)	6-23				
TN-04-14	Low Voltage (3V) DRAM Design Issues	6-25				
TN-43-01	MT43C4257/MT43C4258 Comparison	6-27				
TN-88-01	88-Pin IC DRAM Cards	6-29				
AN-04-01	Chips & Technologies' 82C456 VGA Controller Using MT4C1664					

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated circuit packages have a tendency to absorb moisture. During surface mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks, that might not be harmful initially, could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the noisture absorption characteristics of plastic packages. As he plastic takes on moisture, the weight of the device ncreases. Micron employs a standard procedure for veighing the device before and after it is exposed to noisture. We calculate the percentage of weight gain to letermine the relative efficiency of different packaging echniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn ailures with surface-mount packages by shipping all urface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight ain when subjected to a high humidity environment for ong time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

- 1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
- 2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
- 3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
- 4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K.: et. al.: 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et. al.: 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et. al.: 26th Annual Proceeding, Reliability Physics, 1988.

TAPE AND REEL PROCEDURES

GENERAL DESCRIPTION

Tape and reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape and reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape and reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm		DEVICES PER 13-INCH REEL
PLCC 18 Pin 52 Pin	24 32	12 16	1,000 500
SOJ (300 mil) 20/26 Pin 24 Pin 28 Pin	24 24 24	12 12 12	1,000 1,000 1,000
SOJ (400 mil) 28 Pin 32 Pin 40 Pin	32 44 44	16 16 16	500 500 500

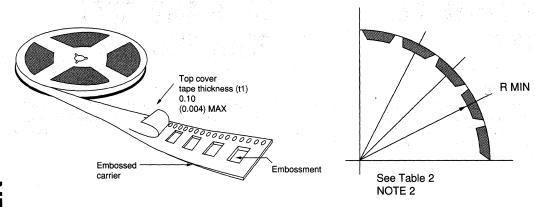
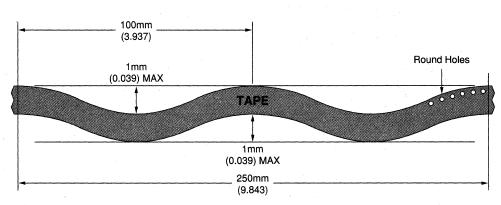


Figure 1 REEL

Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3 CAMBER (TOP VIEW)

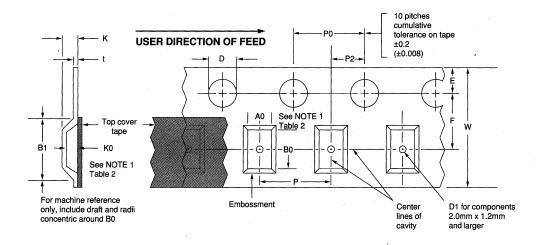


Figure 4 EMBOSSED CARRIER DIMENSIONS

(24mm Tape Only)

Table 2 24mm EMBOSSED TAPE DIMENSIONS 3

TAPE SIZE	D	E	P0	t (MAX)	AO, BO, KO
24mm	1.5 +0.10 (0.59) +0.004 -0.000	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	NOTE 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1	1.5	11.5 ±0.10	6.5	2 ±0.10	50	24 ±0.30
	(0.791)	(0.059)	(0.453 ±0.004)	(0.256)	(0.079 ±0.004)	(1.969)	(0.945 ±0.012)

			P			
TAPE SIZE	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			X	х	х	х

IOTE:

- 1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
- 2. Tape and components shall pass around radius "R" without damage.
- 3. All dimensions in millimeters (inches).

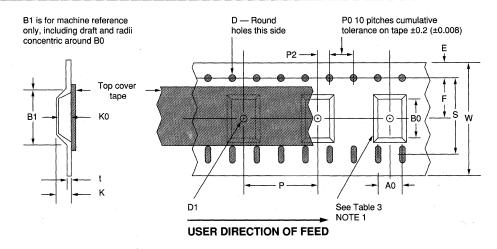


Figure 5
EMBOSSED CARRIER DIMENSIONS

(32 and 44mm Tape Only)

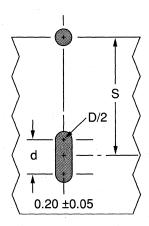


Figure 6
DETAIL ELONGATED HOLE



TN-00-02 TAPE AND REEL

Table 3 32 AND 44mm EMBOSSED TAPE 3

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 +0.10	2	1.75 ±0.10	10	4 ±0.10	0.500	NOTE 1
	(0.059) +0.004	(0.079)	(0.069 ±0.004)	(0.394)	(0.156 ±0.004)	(0.20)	

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23	14.2 ±0.10	2 ±0.10	28.4 ±0.10	32 ±0.30	50
	(0.906)	(0.559 ±0.004)	(0.079 ±0.004)	(1.118 ±0.004)	(1.26 ±0.012)	(1.973)
44mm	35	20.2 ±0.15	2 ±0.15	40.4 ±0.10	44.8 ±0.30	50
	(1.378)	(0.795 ±0.006)	(0.079 ±0.006)	(1.591 ±0.004)	(1.732 ±0.12)	(1.973)

					P			
TAPE SIZE	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	х	х	x			
44mm			x	×	х	х	х	x

NOTE:

- 1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
- 2. Tape and components shall pass around radius "R" without damage.
- 3. All dimensions in millimeters (inches).

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

DRAM POWER-UP AND REFRESH CONSTRAINTS

INTRODUCTION

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding and addressing these incompatibilities and providing for them will offer designers and system users greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the $\overline{\text{CAS-BEFORE-RAS}}$ (CBR) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{\text{WE}}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{\text{WE}}$ pin held at a voltage HIGH level.

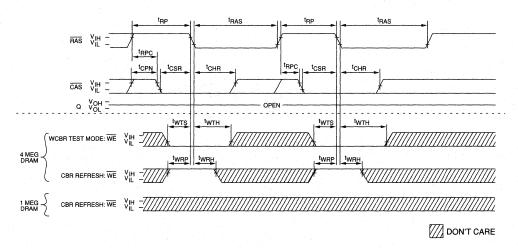
A CBR cycle with $\overline{\text{WE}}$ LOW will put the the 4 Meg into the JEDEC-specified test mode (WCBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIPs, pin 5 on SOJs and pin 8 on ZIPs). This HIGH signal is usually a "super voltage" (Vin \geq 7.5V), so normal TTL or CMOS HIGH levels will not cause the part to enter the test mode.

POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight \overline{RAS} cycles. The 4 Meg POWER-UP is more restrictive in that eight \overline{RAS} -ONLY REFRESH or CBR REFRESH (\overline{WE} held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a \overline{RAS} -ONLY or a CBR REFRESH cycle (\overline{WE} held HIGH).

SUMMARY

- For standard test mode, the 1 Meg requires a vaild HIGH on the test pin while the 4 Meg requires a CBR cycle with WE LOW.
- The 1 Meg CBR REFRESH allows the WE pin to be a "don't care" while the 4 Meg CBR requires WE to be HIGH.
- 3. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS-ONLY REFRESH or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

I APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664 AND MT4C1665 COMPATIBILITIES

INTRODUCTION

Micron provides the 64K x 16 DRAM in two versions: MT4C1664 and MT4C1665. The MT4C1664 has two $\overline{\text{WE}}$ pins which allow for BYTE-WRITE cycles. It does not support WRITE-PER-BIT. The MT4C1665 has one $\overline{\text{WE}}$ pin and offers nonpersistent, WRITE-PER-BIT (MASKED WRITE) cycles.

COMPATIBILITY

The MT4C1664 and MT4C1665 may be used interchangeably, provided precautions are taken. The memory system may not utilize the WRITE-PER-BYTE feature of the MT4C1664 or the WRITE-PER-BIT feature of the MT4C1665 in order to maintain interchangeability.

At the system level, a special timing constraint exists. $\overline{\text{WE}}$ must be held HIGH when $\overline{\text{RAS}}$ transitions from HIGH to LOW (preventing the MT4C1665 from performing WRITE-PER-BIT cycles). The two $\overline{\text{WE}}$ traces must be connected together (pins 12 and 13 on SOJ or pins 22 and 23 on ZIP) in order to ensure that all 16 bits will be written on the MT4C1664.

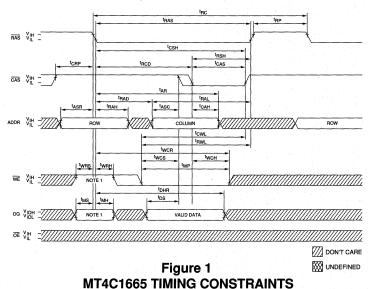
The MT4C1664 and MT4C1665 are now interchangeable.

The MT4C1664 will have twice the capacitive load on the write enable signal as the MT4C1665 due to its two $\overline{\text{WE}}$ pins. Its $\overline{\text{WE}}$ timing will be a "don't care" when $\overline{\text{RAS}}$ transitions from HIGH to LOW. The MT4C1665 will enter a WRITE-PER-BIT cycle if $\overline{\text{WE}}$ is LOW when $\overline{\text{RAS}}$ transitions from HIGH to LOW.

The MT4C1665 can provide the BYTE-WRITE capability of the MT4C1664 by allowing the mask register to be enabled by bytes. However, this may not be practical since it requires additional circuitry.

SUMMARY

An application that performs 16-bit word writes will allow either the MT4C1664 or MT4C1665 to be used. The MT4C1664 must have both $\overline{\text{WE}}$ pins connected, doubling capacitance on the write enable signal, but its timing is a "don't care" when $\overline{\text{RAS}}$ goes LOW. On the other hand, the MT4C1665 has only one $\overline{\text{WE}}$ for lower capacitance, but $\overline{\text{WE}}$ must always be held HIGH when $\overline{\text{RAS}}$ transitions from HIGH to LOW (refer to Note 1).



NOTE: 1. Applies to MT4C1665 only. The MT4C1664 specifies these as "don't cares" during this portion of operation.

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR RAS LINES

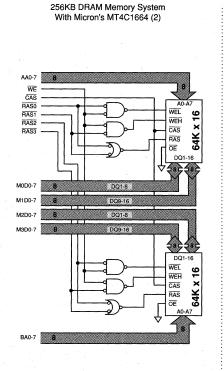
INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s replace eight $64K \times 4$ DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings, while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may be interfaced with a 256KB memory system using four RAS

controls and EARLY-WRITE cycles (\overline{OE} grounded). Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four \overline{RAS} controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles $(\overline{OE} \text{ controlled})$.



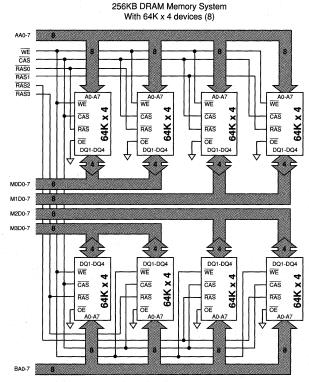


Figure 1
256KB EARLY-WRITE MEMORY

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT4C1664: 256 KILOBYTE MEMORY SYSTEM WITH FOUR CAS LINES

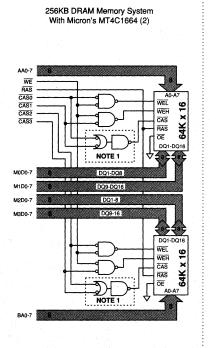
INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is a great solution for replacing 64K x 4 DRAMs in VGA systems. For a 256 kilobyte (KB) memory system, two MT4C1664s will replace eight 64K x 4 DRAMs, resulting in improved reliability and performance margins, decreased power consumption, reduced costs and board savings, while maintaining state-of-the-art technology.

This application note shows how the MT4C1664 may interface with a 256KB memory system using four $\overline{\text{CAS}}$ controls and EARLY-WRITE cycles ($\overline{\text{OE}}$ grounded).

Reference to the MT4C1664 data sheet will be helpful in understanding how the MT4C1664 functions. The schematic in Figure 1 shows 256KB memory systems using four CAS controls and EARLY-WRITE cycles and how memory is implemented with both the MT4C1664 and 64K x 4 DRAMs.

The same schematic for the MT4C1664 may also be used in systems using LATE-WRITE cycles $(\overline{OE}$ controlled), except Note 1 no longer applies and the two delay paths may be equal.



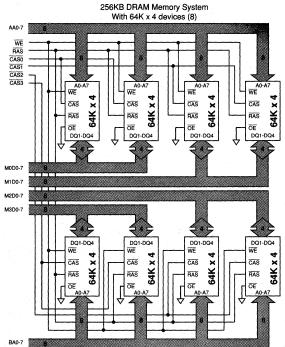


Figure 1
256KB EARLY-WRITE MEMORY

1. This delay path needs to be slightly longer than the two NAND gates to ensure the WE to CAS setup time is met. This will guarantee the DRAM will always be in EARLY-WRITE during WRITE cycles.

DRAM OF CONTROLLED **LATE-WRITE CYCLES**

INTRODUCTION

There are three cycles available to write to a DRAM: EARLY-WRITE cycles, READ-MODIFY-WRITE cycles and LATE-WRITE cycles. The industry standard definitions for DRAM WRITE cycles are fairly consistent for both the EARLY-WRITE and READ-MODIFY-WRITE cycles. An exception exists for the "LATE-WRITE" cycle.

COMMON DQ DRAM (x4, x8, etc.)

A LATE-WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin (OE) HIGH throughout the cycle. The timing parameters ^tRWD, ^tAWD and ^tCWD no longer apply since OE is HIGH.

This condition may be viewed as an EARLY-WRITE with tWCS "sliding" past the CAS time and violating the Ons setup time (WE going LOW prior to CAS going LOW). But, since the output buffers are not being used (\overline{OE} is HIGH), ^tWCS and ^tCWD are no longer required.

If WE transitions LOW after CAS transitions LOW, do not bring OE LOW (a noise spike may occur), as the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for such a WRITE cycle varies throughout

the industry. The use of "OE controlled WRITE," "Delayed WRITE" and "LATE-WRITE" all signify the same WRITE cycle described.

SPLIT D AND Q DRAM (x1)

A LATE-WRITE cycle is a READ-MODIFY-WRITE, except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected together). This is accomplished by ignoring the timing parameters tRWD, tAWD and tCWD.

This condition can be viewed as an EARLY-WRITE with tWCS "sliding" past the CAS time and violating the Ons setup time (WE going LOW prior to CAS going LOW). But, since the output buffers are "don't care," tWCS and tCWD are no longer required.

This cycle is not available on applications that have the D and Q connected together, as the output will contend with the input.

SUMMARY

A LATE-WRITE cycle is most useful on common DO DRAMs. Use caution to ensure the output enable pin is properly controlled.

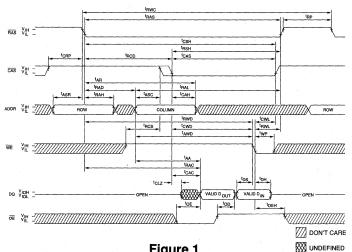


Figure 1 READ-MODIFY-WRITE (MULTIPLE DQ) TIMING



DRAM TIMING PARAMETERS

INTRODUCTION

A DRAM has many timing parameters, which are specified to help the memory designers define memory system timing. These parameters may be separated into several groups. This note separates these parameters as core parameters (COP) or calculated parameters (CAP).

The calculated parameters are tested by Micron prior to shipment. In cases where the summation of COP parameters is larger than the CAP parameter specification, the CAP parameter overrides the summation of COP

parameters. Additionally, if an incoming test is required, the testing of the COP parameter is typically sufficient since CAP parameters are simply combinations of COP parameters.

The CAP parameters are listed below, showing how they are calculated. This will aid the memory designer's understanding of the parameters affected when a COP parameter is altered. Additionally, during testing of the COP parameters, the CAP parameters are also tested by default.

^t RC	=	^t RAS + ^t RP + 2 ^t T
^t PC	=	^t CPA + ^t T or ^t CP + ^t CAS + 2 ^t T
^t AR	=	^t RCD (MAX) + ^t CAH
^t RSH	≈	[†] CAS
^t CSH	=	[†] CAS + [†] RCD (MAX)
^t CPA	=	^t AA + ^t T
^t AA	≈	^t RAS/2
^t DHR	=	^t RCD (MAX) + ^t DH
tWCH	=	tWP - tWCS - tT
tWCR	=	tRCD (MAX) + tWCH
tRAD (MIN)	=	^t RAH + ^t T
tRAD (MAX)	=	tRAC - tAA
tRCD (MIN)	=	${}^{t}RAD + {}^{t}ASC + {}^{t}T = {}^{t}RAH + {}^{t}ASC + 2{}^{t}T$
tRCD (MAX)	=	[†] RAS - [†] RSH
^t RWD (x1)	=	^t RAC
tRWD (x4)	=	^t RAC + ^t OD + 2 ^t T + ^t DS
^t CWD (x1)	=	†CAC
tCWD (x4)	=	tCAC + tOD + 2tT + tDS
tAWD (x1)	=	^t AA
tAWD (x4)	=	^t AA + ^t OD + 2 ^t T
tRWC (x1)	=	^t RWD + ^t RWL + ^t RP + 2 ^t T
tRWC (x4)	=	tRAC + tRWL + tRP + 4tT + tOD + tDS
tPRWC (x1)	=	^t CPA + ^t CWL + 2 ^t T + ^t DS
tPRWC (x4)	=	tCPA + tCWL + 4tT + tOD + tDS

LPDRAM BBU CURRENT VS. **RAS** ACTIVE TIME (1 MEG)

INTRODUCTION

One of the most significant features of the low power, extended refresh DRAM (LPDRAM) is its BATTERY BACKUP (BBU) cycle. BBU is essentially a CAS-BEFORE-RAS (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

RAS pulse width (tRAS) affects the BBU current and should be considered when designing a low power system. The longer RAS is held LOW, the more current an LPDRAM will consume while in the BBU mode. Therefore, keeping ^tRAS at a minimum will maximize power savings.

Figure 1 shows a typical curve of Micron's 1 Meg

LPDRAM (MT4C4256L and MT4C1024L) showing the relationship between its BBU standby current and the width of tRAS. The 25°C curve has a slope of 4.8µA increase for every additional 1µs RAS is held LOW. The 70°C curve has a slope of 4µA increase for every additional 1µs RAS is held LOW.

SUMMARY

The ^tRAS time should be kept as short as possible when the memory array is being designed. This will result in lower standby currents, especially with the BBU cycle.

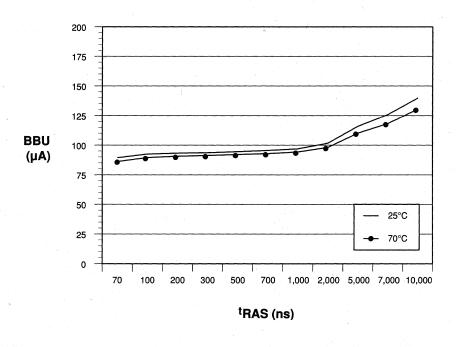


Figure 1 TYPICAL BBU CURRENT AS A FUNCTION OF TRAS

LPDRAM BBU CURRENT VS. RAS ACTIVE TIME (4 MEG)

INTRODUCTION

One of the most significant features of the low power extended refresh DRAM (LPDRAM) is its BATTERY BACKUP (BBU) cycle. BBU is essentially a CAS-BEFORE-RAS (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

RAS pulse width ('RAS) affects the BBU current and should be considered when designing a low power system. The longer RAS is held LOW, the more current an LPDRAM will consume while in the BBU mode. Therefore, keeping 'RAS at a minimum will maximize power savings.

Figure 1, a typical curve of Micron's second generation

4 Meg LPDRAM (MT4C4001L and MT4C1004L), shows the relationship between its BBU standby current and the width of tRAS . The 25°C curve has a slope of 79µA increase for each additional 1µs \overline{RAS} that is held LOW. The 70°C curve has a slope of 70µA increase for each additional 1µs that \overline{RAS} is held LOW.

SUMMARY

The ^tRAS time should be kept as short as possible when designing memory array timing. This will result in lower standby currents, especially for the BBU cycle.

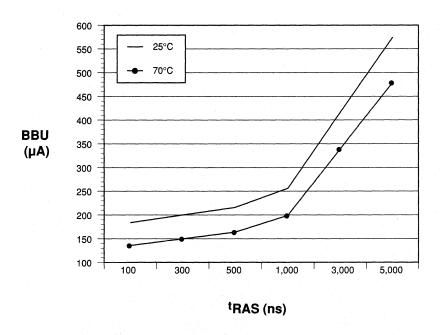


Figure 1

TYPICAL BBU CURRENT AS A FUNCTION OF ^tRAS



LOW-VOLTAGE (3V) DRAM DESIGN ISSUES

INTRODUCTION

Laptop and notebook personal computer markets demand low-voltage memories. This is in direct response to the consumer's demand for portable PCs with longer battery life. To help meet this demand, Micron introduced the industry's first 3.3V 1 Meg DRAM.

The introduction of low-voltage DRAMs, raised design concerns regarding the migration from 5V systems to 3.0, 3.3 and 3.3/5.0V systems. Several issues must be considered prior to selecting DRAM memory for low-voltage PC systems:

- Voltage limits
- Speed
- I/O levels
- Mixed/dual voltages
- Soft error rates (SERs)

VOLTAGE LIMITS

During the development phase of low-voltage DRAMs, manufacturers are expected to introduce offerings in four different voltage ranges:

- 3.3V ±5% (interim)
- 3.0V ±10%
- 3.3V ±10%
- 2.7V to 3.6V

The 3.3V ±5% version is the first available low-voltage DRAM. This is generally an enhanced version of existing 5V DRAMs specially processed for 3.3V operation. Micron is ible to offer 3.3V ±5% 1 Meg and 4 Meg DRAMs because Micron uses a leading-edge DRAM process. This type of ow-voltage DRAM works reliably in mixed/dual voltage ystems and offers early availability for 3.3V system levelopment.

The other versions are manufactured with a low-voltage-nly CMOS process and are commonly referred to as 3V-nly DRAMs. Micron's 3V-only DRAMs are being developed to operate over the 2.7V to 3.6V voltage range (fourth ersion). This will provide either 3.0V $\pm 10\%$ or 3.3V $\pm 10\%$ peration from the same DRAM. Devices manufactured with the low-voltage CMOS process are optimized for both igh-speed and low-power performance at low voltages.

The 3V-only process limits the allowed maximum Vcc stress to the DRAM at 4.6V. Any violation of this maximum specification can damage the DRAM. Careful review of this parameter is necessary prior to selecting a low-voltage DRAM.

The Micron device part number indicates one of the two process groups for low-voltage DRAMs. "C" designates 3.3V CMOS, while "LC" designates 3V-only low-voltage CMOS processing. For example, the 3.3V 1 Meg DRAM (256K x 4) is an MT4C4256 VL, which allows a 6V maximum Vcc stress. Although Micron has no plans to introduce a 3V-only 256K x 4 DRAM, the device would be a MT4LC4256 L if it were developed and introduced to the market. Additionally, Micron data sheets specify the maximum Vcc stress rating for a given DRAM.

SPEED

The most significant advantage of a 3V-only DRAM is that it will have similar speeds to that of a 5V DRAM operating at 5V, 60ns to 70ns. The interim 3.3V DRAMs will achieve only 100ns, but will achieve speeds in the range of 60 to 80ns when operating at 5V.

Micron's MT4C4256 VL timing parameters are tested for a $3.3V \pm 5\%$ operation. Although the device is not tested at 5V, characterization data shows the $3.3V \pm 1$ Meg DRAM will achieve 70ns or better when operating at 5V.

I/O LEVELS

The interim 3.3V DRAM has an I/O level issue. Since these devices are designed for 5V operation, the trip points will change when the DRAM is operating at 3.3V. In particular, VIL and VOH noise immunity guardbands are reduced and will be less forgiving than when they were at 5V. Since the variances are device specific, consulting the device's data sheet prior to design is recommended.

On the other hand, 3V-only DRAMs do not have I/O level issues. The device and process are designed for optimum drive levels and trip points at 3.3V. It is worth noting that the JEDEC 3.3V output specification states one TTL load rather than two TTL loads.



MIXED/DUAL VOLTAGES

Some of the first and second generation low-voltage systems may require the ability of both 3.3V and 5V operation. This would offer 3.3V operation for low power consumption while in the portable mode and faster speeds when plugged in to a power source such as at the desk or in the car. This application will be supported by the interim 3.3V DRAM, since it allows both 3.3V and 5V operation.

An important issue to consider in a mixed/dual voltage system is the switching of the Vcc power supply level. A DRAM will experienced what is referred to as a "Vbump" when the Vcc level changes. This occurs when the data is stored in the memory cell at a certain level and is read out (internally) at a different level due to a shift in the Vcc level. Switching the Vcc from 3.3V to 5.0V results in a severe "bump" and can corrupt the data stored in the DRAM memory cells.

The system designer has two alternatives when developing a system that will operate with mixed/dual voltages. The first is to require that all the contents of DRAM-based memory be saved (usually onto disk memory) prior to changing the power supply level, then restore the DRAM-based memory once the power-supply levels have been changed.

The second alternative is to increase the power supply in increments with the DRAM memory being completely refreshed at each interval. Ideally, the largest increment Vcc should be raised is no more than the difference between the maximum Vcc limit and the minimum Vcc limit. In the case of the 3.3V $\pm 5\%$ DRAM, Vcc should not increase by more than 300mV at a time. The Micron MT4C4256 VL, on the other hand, can accommodate up to a 1V step.

For example, starting at 3.3V, increase Vcc to 4.2V, then perform a complete set of refresh cycles. After the refresh is complete, raise the Vcc level to 5.0V and perform another complete set of refresh cycles. After the second refresh is complete, the DRAM memory will be ready for 5V operation.

If an application requires the DRAM's Vcc power to come from a different reference level than the input and/or output busses, the I/O pin reference levels must not exceed the Vcc reference levels by more than 1V, unless specified less by the data sheet. Exceeding this can cause the DRAM to either initiate the DRAM manufacturer's internal test mode or cause excessive leakage on the output pins.

SOFT ERROR RATES

A disadvantage with operating interim 3.3V DRAMs at 3.3V rather than at 5.0V is the increased susceptibility of the DRAM to soft errors. Preliminary SER data taken on the interim 3.3V 1 Meg DRAM shows diverging results. Real-time SER data shows no difference between 5V and 3.3V operation. Yet, accelerated SER data shows an increase in soft errors going from 5V to 3.3V operation. Additionally, SER will vary widely between vendors as the design and process employed determine the soft error susceptibility.

Until the SER divergence is well understood, Micron is recommending its interim 3.3V DRAMs be used for the PC-related memory market (low number of units per system). Micron discourages the use of its interim 3.3V DRAMs in memory-intensive systems that require hundreds of DRAMs. The 3V-only DRAM, on the other hand, should not experience an increase in SER and is an excellent choice for low-voltage memory in memory-intensive systems.

APPLICATION/TECHNICAL NOTE

TECHNICAL NOTE

MT43C4257/MT43C4258 COMPARISON

INTRODUCTION

Micron Technology, Inc., offers its Triple Port DRAM (TPDRAM) in two versions. The MT43C4257 supports the JEDEC split SAM status function (QSF) pin as defined for VRAMs. The MT43C4258 supports a variation of the QSF function called the split SAM special function (SSF) input function. Other than this difference, the function and performance of the two devices are identical.

MT43C4257 — OSF OUTPUT

The QSF output pin of the MT43C4257 is identical in function to the QSF pin of the MT42C4255 256K \times 4 VRAM. The QSF output pin indicates which half of the SAM is being accessed. When data is accessed from the lower half, the QSF is LIOW; when data is accessed from the upper half, QSF is HIGH (see Figure 1). When using the MT43C4257 or any standard VRAM in the split SAM mode, the transition between SAM halves occurs only when the SAM-half boundary is reached by the address pointer. This is address count 255 for the lower half and 511 for the upper half. When this boundary is reached, the new Tap address for the next

SAM-half is loaded ("X" for the lower, "Y" for the upper). The following SC will access data from the new half.

MT43C4258 — SSF INPUT

The MT43C4258 introduces functionality to the TPDRAM that is not available on standard VRAMs. The "QSF" pin as an input (SSF) offers a higher degree of design flexibility to the system engineer. The SSF applies only to split transfer cycles. It allows access to be switched from one half of the SAM to the other at will. If SSF is HIGH at the rising edge of the serial clock, the split SAM access will be switched to the other half of the SAM (see Figure 2).

By taking SSF HIGH for the rising edge of a serial clock (location "A" for the lower half, "B" for the upper), the access from the current half may be terminated. Data from this clock will appear on the outputs when in serial output mode or will be written if in serial input mode.

The next serial clock will access data at the new Tap address ("X" for the lower, "Y" for the upper) of the next half. The SSF input acts as a "stop address" input so the

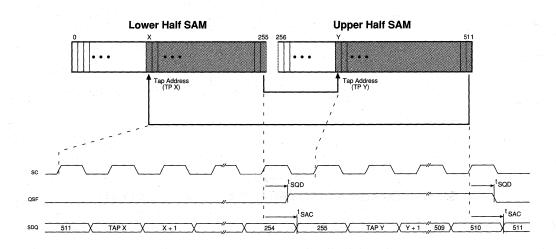


Figure 1
QSF OPERATION FOR THE MT43C4257 (SERIAL OUTPUT)

designer can "force" the access from one half to the next when desired. When operating in the split SAM mode, this option allows different sized "blocks" of data to be input or output from the SAM half regardless of the Tap address and stop point. This feature is useful when performing pans, zooms and scrolling in video-graphics systems and for handling distinct packet sizes in networking or controller applications.

SUMMARY

The only difference between the MT43C4257 and MT43C4258 is the variance in the functionality of the "QSF"

pin. The MT43C4258 SSF input pin allows more efficient handling, and therefore higher throughput, of input or output data in either SAM. This improves the performance of video-graphics and networking systems by providing high clock speed and no latency time between reaching the stop point of valid data in one half and the loading of the new Tap address for the next half.

The SSF functionality is also available on the x8 versions of the TPDRAM, the MT43C8128 (QSF) and MT43C8129 (SSF). Refer to the data sheets for detailed timing and functional descriptions.

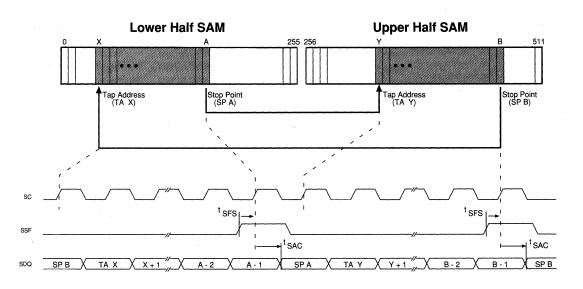


Figure 2
SSF OPERATION FOR THE MT43C4258 (SERIAL OUTPUT)

APPLICATION/TECHNICAL NOTI

TECHNICAL NOTE

88-PIN IC DRAM CARDS

INTRODUCTION

Just as SIMMs began a new period in memory placement and packaging in the 1980s, the 88-pin IC DRAM card promises to have an equal impact on the industry in the 1990s. The 88-pin IC DRAM card combines the architecture of a SIMM with an IC memory card form factor to create a high density, easy-to-use memory device. No longer do end-users have to disassemble their systems and risk ESD damage to add more SIMM modules or memory boards. Finally, a convenient, sensible, and rugged approach to memory packaging has arrived.

For engineers, Micron's 88-pin IC DRAM cards offer a significant improvement in the way system designers manage main and add-in memory. IC DRAM memory cards require less system interface logic, they pack more memory into a given area than SIMM modules and they are better able to withstand use and abuse than contemporary memory upgrade schemes. All this functionality is contained in a convenient, portable, and standardized package.

Standards for the 88-pin IC DRAM card have been jointly ratified by the three major standard-setting bodies: PCMCIA, JEDIA and JEDEC. As a companion to the 68-pin IC memory card, or by itself, the 88-pin IC DRAM card will enhance your product design or offerings.

IC DRAM cards provide a robust, rigid and durable enclosure for the printed circuit board and memory devices contained within. The card's physical dimensions are 2.126 ±0.004 inches wide by 3.37 ±0.004 inches long by 0.129

 ± 0.004 inches thick, which is about the same dimension as a credit card though three times its thickness.

Once assembled, the strength of the IC DRAM card surpasses that of SIMM modules. Moreover, since the card's components are not subjected to direct physical contact by the user, it can withstand casual, even abusive, handling much better than a SIMM module. When a SIMM module is installed, removed or transported, there is a risk of inflicting damage due to electrostatic discharge. The card is made with a conductive plastic that allows static charges to be safely dissipated to the ground pins via a High-Z path.

IC DRAM cards are designed to ease facilitation. Though the IC DRAM cards appear to function like 72-pin SIMM modules, significant differences favor the IC DRAM card. For example, the IC DRAM card provides its own buffering for its control lines, relieving the system board. Furthermore, buffering enhances system performance, both from noise reduction and reduced capacitive loading of the control lines.

The IC DRAM cards are preferable to SIMMs in small profile notebook and palmtop computers, because the cards offer a twofold improvement in board area usage. Proper choice of receptacle connector for the system board provides the ability for hot insertion or removal, which is impossible for a SIMM module. And the IC DRAM card's size and ruggedness make it ideal for mainframe or industrial applications.

Table 1 MEMORY ADDRESS RANGE

	MEMORY ADDRESS RANGE								
		Total Memory Size							
DRAM Address Space Per Bank	PD1	PD2	PD3	PD4	PD5 = 0	PD5 = 1			
no card installed	1	1	1	1	n/a	n/a			
256K	0	0	0	0	1MB	2MB			
512K	1	0	0	0	2MB	4MB			
1 Meg	0	1	0	0	4MB	8MB			
2 Meg	1	1	0	0	8MB	16MB			
4 Meg	0	0	1	0	16MB	32MB			
8 Meg	1	0	1	0	32MB	64MB			
16 Meg	0	1	1	0	64MB	128MB			

PRESENCE DETECT DEFINITIONS FOR THE 88-PIN IC CARD

It is necessary to clarify the presence detect definitions for the 88-pin IC DRAM cards. The eight presence detect pins are divided into four groups, consisting of memory size (4 bits), number of DRAM banks (1 bit), DRAM access timing (2 bits) and refresh control (1 bit). As shown in Table 1, presence detect bits are defined as 0 = ground, 1 = open.

Presence detect bits PD1, PD2, PD3 and PD4 relate to the byte size of the card or its memory address range. The PD5 presence detect indicates the number of memory banks present on the card. The card will be provided with either 1 or 2 banks (32-, 36- and 40-bit versions) or 2 or 4 banks (16- and 18-bit versions).

For 32-, 36- and 40-bit applications, PD5's definition relates to whether one or two banks are present. Each bank is defined by $2\ \overline{AAS}$ lines. In other words, both \overline{RAS} lines should be activated simultaneously for a 32-, 36- or 40-bit word access. When PD5 = 0, there is one bank present, activated by $\overline{RAS0}$ and $\overline{RAS2}$. When PD5 = 1, there are two banks present. Bank 1 is activated by $\overline{RAS0}$ and $\overline{RAS2}$ while bank 2 is activated by $\overline{RAS1}$ and $\overline{RAS3}$.

For 16- or 18-bit applications, PD5's definition relates to whether 2 or 4 banks are present. Each bank is defined by a single \overline{RAS} lines. When PD5 = 0, two banks are present, activated by $\overline{RAS0}$ and $\overline{RAS2}$. When PD5 = 1, two additional banks are present, activated by $\overline{RAS1}$ and $\overline{RAS3}$. A logical progression within the system's address space would be $\overline{RAS0}$, $\overline{RAS2}$, $\overline{RAS1}$ and $\overline{RAS3}$ in that order. For a 36-bit data bank interpreted as an 18-bit card, \overline{RAS} relates to the data bus as shown in Table 2.

The PD6 and PD7 presence detects indicate the access time of the card from \overline{RAS} true to data out. They are defined in Table 3.

The PD8 presence detect is related to the refresh type of the card, either auto-refresh when PD8 = 0, or a 125 μs per row refresh rate when PD8 = 1. Presently all DRAM cards will leave PD8 open, indicating that the system should provide refreshing, preferably a \overline{CAS} -BEFORE- \overline{RAS} -type of refresh. This allows an address-independent refresh, which allows interchangeability among different card types.

Table 2
RAS RELATION TO DATA BUS

RAS0	D0-D17	Bank 1
RAS1	D18-D36	Bank 2
RAS2	D0-D17	Bank 3
RAS3	D18-D36	Bank 4

Table 3 DATA OUT ACCESS TIME

ACCESS TIME	PD7	PD6
100ns (or 50ns for future cards)	0	0
80ns	0	1
70ns	1	0
60ns	1.	1



Table 4 32-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (32-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT8D88C25632-xx	1	16, 32	5V	60-100ns
MT8D88C25632-xxV	1	16, 32	3.3V	100ns
MT16D88C51232-xx	2	16, 32	5V	60-100ns
MT16D88C51232-xxV	2	16, 32	3.3V	100ns
MT8D88C132-xx	4	16, 32	5V	60-100ns
MT8D88C132-xxV	4	16, 32	3.3V	100ns
MT8D88C132-xxS	4	16, 32	3.0/3.3V	60-80ns
MT16D88C232-xx	8	16, 32	5V	60-100ns
MT16D88C232-xxV	8	16, 32	3.3V	100ns
MT16D88C232-xxS	8	16, 32	3.0/3.3V	60-80ns

PRODUCT OFFERING

IC DRAM cards are offered through Micron. The current product spectrum provides memory sizes from 1 MB to 8 MB in 16-, 18-, 32-, 36- and 40-bit word sizes, with both 5V and 3.3V (18- and 36-bit word sizes do not have 3.3V option).

IC DRAM CARD 32-BIT SERIES

The series MT8D88C25632 (1MB), MT16D88C51232 (2MB), MT8D88C132 (4MB) and MT16D88C232 (8MB) are organized to provide a 32-bit word. It is identical to the 36-bit series, except that no bits are provided for parity protec-

tion. The data pinout will differ from the 36-bit series as shown in Table 5.

Micron's product offering is shown in Table 4. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8 or -6 suffix to the part number where "xx" is shown. The cards use low power extended refresh DRAMs. Cards using a 3.3V supply have their speed grade appended with a "V" option. Cards that use self refresh DRAMs have their speed grade appended with an "S" option.

Table 5
32-BIT AND 36-BIT SERIES

	32-BIT SERIES	36-BIT SERIES
Byte 0	D0-D7	D0-D8
Byte 1	D9-D16	D9-D17
Byte 2	D18-D25	D18-D26
Byte 3	D27-D34	D27-D35

Table 6 36-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (36-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER Supply	SPEED (ns)	
MT12D88C25636-xx	1	16, 18, 32, 36	5V	60-100ns	
MT24D88C51236-xx	2	16, 18, 32, 36	5V	60-100ns	
MT12D88C136-xx	4	16, 18, 32, 36	5V	60-100ns	
MT24D88C236-xx	8	16, 18, 32, 36	5V	60-100ns	

IC DRAM CARD 36-BIT SERIES

The series MT12D88C25636 (1MB), MT24D88C51236 (2MB), MT12D88C136 (4MB) and MT24D88C236 (8MB) are organized to provide a 36-bit word with parity per byte. Each byte is specified by a $\overline{\text{CAS}}$ control line; therefore, the card can provide 9- or 18-bit words with appropriate design on the system board. The MT12D88C25636 provides 256K by 36 bits or 512K by 18 bits. Bank access (full word) is provided by the appropriate $\overline{\text{RAS}}$ lines. Refer to the appropriate datasheet for a block diagram of the internal architecture. Please note that this series does not support output enable and $\overline{\text{OE}}$ is internally tied. It is suggested for

compatibility reasons that the system board also provide a tie to ground for the \overline{OE} lines.

Micron's product offering is shown in Table 6. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8, -7 or -6 suffix to the part number where "xx" is marked. The cards use low power extended refresh DRAMs. If an 8- or 9-bit card is desired, it can be created through the use of $\overline{\text{CAS}}$ line controls to differentiate the data lines by tying the upper data lines to the lower data lines.



Table 7 **40-BIT PRODUCT OFFERINGS**

		the state of the s		production of the second
PRODUCT NUMBER (40-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT12D88C25640-xx	1	16, 18, 32, 36, 40	5V	60-100ns
MT12D88C25640-xxV	1	16, 18, 32, 36, 40	3.3V	100ns
MT24D88C51240-xx	2	16, 18, 32, 36, 40	5V	60-100ns
MT24D88C51240-xxV	2	16, 18, 32, 36, 40	3.3V	100ns
MT12D88C140-xx	4	16, 18, 32, 36, 40	5V	60-100ns
MT12D88C140-xxV	4	16, 18, 32, 36, 40	3.3V	100ns
MT12D88C140-xxS	4	16, 18, 32, 36, 40	3.0/3.3V	60-80ns
MT24D88C240-xx	8	16, 18, 32, 36, 40	5V	60-100ns
MT24D88C240-xxV	8	16, 18, 32, 36, 40	3.3V	100ns
MT24D88C240-xxS	8	16, 18, 32, 36, 40	3.0/3.3V	60-80ns

IC DRAM CARD 40-BIT SERIES

The series MT12D88C25640 (1MB), MT24D88C51240 (2MB), MT12D88C140 (4MB) and MT24D88C240 (8MB) provide a 40-bit word amenable to word-wise error correction coding. The series does support output enable control and, therefore, read-modify-write cycles for error detection and correction. If desired, the card may function as a universal solution for 8-, 9-, 16-, 18-, 32-, 36- or 40-bit solution. The RAS and CAS lines are configured the same way as the above cards. In a 40-bit mode, RASO is tied to RAS2 and RAS1 is tied to RAS3. Also, CAS lines are tied together. This allows the first bank to be selected by RASO

and RAS2 lines, and the second bank by RAS1 and RAS3 lines. This is external to the card.

Micron's product offering is shown in Table 7. The series is provided with speed grades from 100ns to 60ns. This is specified with a -10, -8 or -6 suffix to the part number. The cards use low power extended refresh DRAMs. Cards using a 3.3V supply have their speed grade appended with a "V" option. Cards that use self refresh DRAMs have their speed grade appended with an "S" option. Information on these and other IC card products is available from Micron.

SERVICES

Micron stands ready to help customers who wish to enter the IC DRAM card market with proprietary solutions. Our staff engineers are well versed in the design of boards for the entire PCMCIA/JEDEC/JEIDA arena. If one of our standard products does not meet your current needs, we are ready and able to design a custom solution for you.

For customers desiring a standard product under private label, Micron can supply current products labeled and marked in virtually any manner the customer wishes. Simply supply us with the desired artwork showing the desired markings and Micron will do the rest.

Often overlooked by companies considering entrance into the IC card market are the mechanical considerations. Micron has invested considerable time and effort into developing superior card frames, covers and components. Our custom design services break down the significant entry barriers to this burgeoning market and will get your product to market on-time and on-budget. Design services offered include

Design from concept
Schematic capture
Board layout
Enclosure design
Thermal and signal noise analysis
Custom marking
Comprehensive testing
Connector redesign
ASIC solutions
Packaging solutions

For those considering including IC DRAM cards in their system design as an add in product, turnkey solution or custom design, a design guideline, "Designing for IC Cards" (publication no. PPG03) is available through Micron. Applications engineering assistance is also available from 8 a.m. to 5 p.m. Mountain Time at (208) 368-3900.

The IC card arena is very fast-paced. Product development and introduction will quickly outdate current information. When contemplating a design in this arena, please call us for the latest product datasheets and design guidelines.

APPLICATION NOTE

CHIPS & TECHNOLOGIES' 82C456 CONTROLLER USING MT4C1664

INTRODUCTION

Micron's MT4C1664 64K x 16 DRAM is an ideal solution for replacing 64K x 4 DRAMs in VGA systems. For a 256KB memory system, two MT4C1664 components replace eight 64K x 4 DRAMs. This provides improved reliability and performance margins, decreased power consumption, reduced costs and board savings using state-of-the-art technology.

This application note shows how the MT4C1664 can be interfaced with the Chips and Technologies 82C456 VGA controller chip. It evaluates the pertinent timing parameters and determines the amount of margin available between the two components.

Micron's Technical Notes (TN-04-03 and TN-04-04) show that the MT4C1664 can interface with virtually any VGA controller available on the market. The timing analysis procedure used to evaluate the MT4C1664 and the 82C456 may also be applied to other VGA controllers to determine how they may best be used with the MT4C1664.

The schematics in Figure 1 show a 256KB memory, which interfaces with the 82C456. The memory is implemented with both MT4C1664 (64K x 16 DRAM) and 64K x 4 DRAMs.

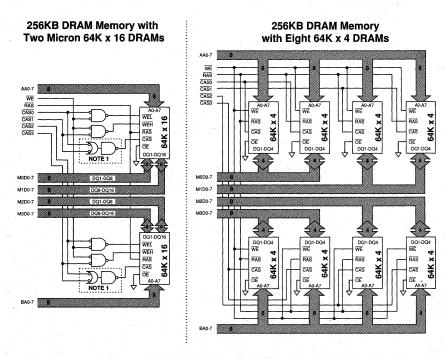


Figure 1 256KB EARLY-WRITE MEMORY

NOTE: 1. This delay path needs to be slightly longer (minimum of 0ns) than either NAND gate to ensure the WE to CAS setup time is met. This guarantees the DRAM will always be in EARLY-WRITE during WRITE cycles.

TIMING ANALYSIS

The timing margin available between the MT4C1664 and the 82C456 is determined using each device's guaranteed minimum timing specifications. The first step in determining the amount of timing margin is to construct the timing waveforms of the VGA controller (Figure 2). The control and data comes from the controller and goes to the DRAM memory except for data out (Q), which comes from the DRAM back to the controller.

The second step is to compare the specifications required by the DRAM to those of the VGA controller. The amount of margin available is the difference between the two. Remember that the minimum specification of the VGA controller is not the same as that of the DRAM. The VGA controller's minimum is that which the controller is guaranteed to provide to the DRAM. The DRAM's minimum is that which the DRAM requires in order to function properly. For example, the 82C456 specs its ^tCRP to be 25ns minimum (@ 40 MHz) while the MT4C1664 only requires a minimum of 5ns. Thus, this difference results in a margin of 20ns between what the 82C456 provides and what the MT4C1664 requires.

The additional logic required to use the MT4C1664 with the Chips and Technologies 82C456 VGA controller introduces a timing skew on the CAS, WE and Q signals. The

final portion of the analysis determines how much skew is tolerable. The second section of the timing waveform in Figure 2 shows the effects of the additional logic delays (timing skews) and the decrease in margin between the two devices.

The analysis shows that logic delays of 10ns and 15ns (10ns for the negated NAND path and 15ns for the negated OR connected to a NAND path) allows the MT4C1664 to meet all of the Chips and Technologies 82C456 VGA specifications.

Additional timing delay may be used in the added logic circuitry. The negated OR in series with the NAND path may have its delay increased by 5ns (from 15ns to 20ns). An additional delay of more than 5ns will violate the ${}^{t}CRP$ minimum of the MT4C1664. Except for ${}^{t}CRP$ and ${}^{t}RSH$, all the other parameters skewed by the added logic have more than sufficient timing margins.

Table 1 summarizes the memory timing specifications of a VGA system using the 82C456 VGA controller with the MT4C1664. Logic delays of 10ns and 15ns introduced by the additional logic are also evaluated. The amount of timing margin available in both cases (with and without the logic delays) is summarized.

Table 1 MINIMUM TIMING SPECIFICATION COMPARISON

		DATA SHEET SPECIFICATIONS		WI	TH LOGIC D	ELAY			
PARAMETER	SYM	82C456	MT4C1664	MARGIN	82C456	MT4C1664	MARGIN	UNITS	NOTES
RAS pulse width	tRAS	100	100	0	-		-	ns	1
CAS to RAS precharge time	tCRP	25	5	20	10	5	5	ns	
RAS hold time	tRSH	50	25	25	35	25	10	ns	
CAS pulse width	tCAS	100	25	75	-	-	-	ns	1
Write command hold time	tWCS	50	0	50	5	0	5	ns	
Write command setup time	tWCH	125	20	105	95	20	75	ns	
Column address setup time	tASC	25	0	25		10.00		ns	1
Column address hold time	^t CAH	75	15	60	-	-	-	ns	1
Data-in setup time	^t DS	50	0	50	65	0	65	ns	
Data-in hold time	^t DH	125	15	110	110	15	95	ns	
Access time from CAS	^t CAC	75	30	45	60	30	30	ns	
Access time from RAS	tRAC	125	100	25	-	-	-	ns	1

NOTE: 1. Additional logic does not skew timing between the 82C456 and the MT4C1664.



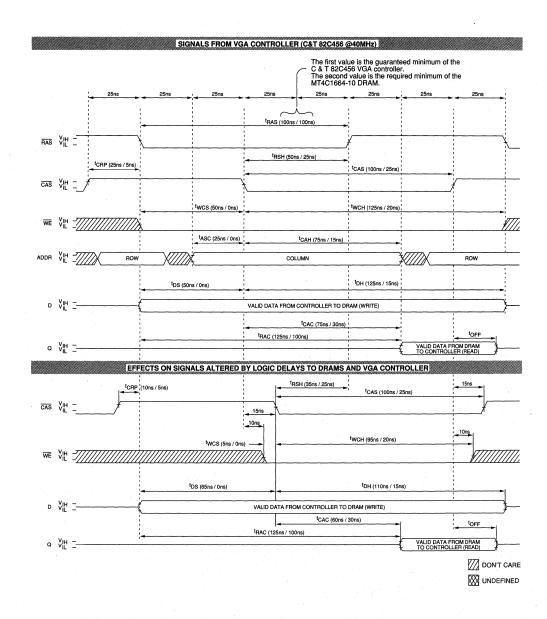


Figure 2 TIMING ANALYSIS OF MT4C1664 WITH C & T 82C456

MICHON TECHNOLOGY, INC.

DYNAMIC RAMS	
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9





OVERVIEW

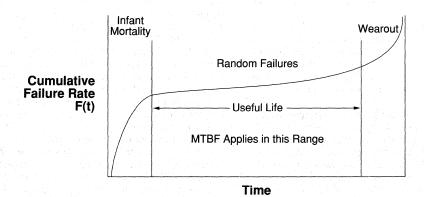
At Micron, we emphasize superior product quality through our unmatched reliability system. We define product reliability as a product's ability to perform its intended functions and operate under specified environmental conditions for a specified length of time. This section contains a brief overview of some of the issues that affect the reliability of IC devices, and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_n .

Figure 1 shows that the significant portion of this curve is the random failure segment. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX™ intelligent burn-in/test system, developed by Micron is described in the following section.



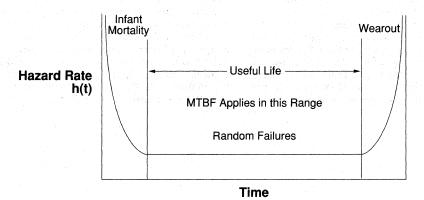


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX™ INTELLIGENT BURN-IN AND TEST SYSTEM

Throughout the semiconductor industry, burn-in has been a crucial factor to increase memory product reliability. Micron stresses our memory devices to simulate years of normal use. Then we document and analyze the results so that we can take any corrective action needed. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burnin cycle without removing them from the burn-in oven. We were so convinced of the importance of highly refined burn-in that we searched for a system to meet this need. Because we found no system that met our requirements, we introduced the concept of "intelligent" burn-in and, in 1986, developed the AMBYX™ intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of *individual* product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings the slightest variation in a product's failure rate to our attention.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then, we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the

burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons that Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test. All semiconductor manufacturers use this test to calculate random field failure rates. Second, we want to be sure we are not introducing new failure modes (failures unrelated to normal wearout) by testing them at extremely elevated conditions. In this way, Micron ensures that we've effectively screened our products for infant mortalities.

Control charts, such as the one shown in Figure 3, alert us to trends in the failure rates of some lots. When we detect an increase in a certain failure rate, we pinpoint the lots that need additional burn-in cycles to identify all variables that might influence the failure rates of those lots. Such variables could include fabrication and assembly equipment, manufacturing shifts and time frames when the lots were processed through specific steps.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.



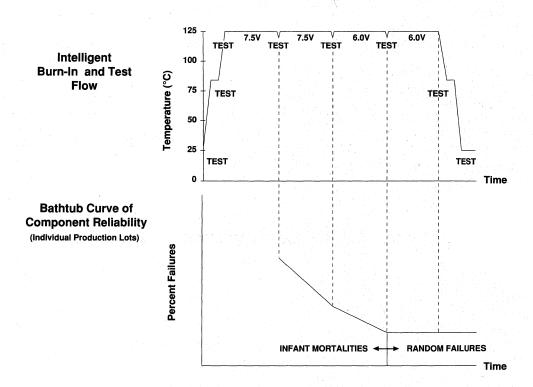


Figure 2
AMBYX™ BURN-IN/TEST FLOW AND TEST RESULTS

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of environmental stress tests.

As discussed in the previous pages, we test our devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under *normal use*. Figure 3 shows the conditions for these tests, known as "accelerated environmental stress" tests. The EPM program described in Figure 3 is for our 1 Meg SRAM.

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	100 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% R.H., 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% R.H., 15 PSI, No Bias)	288 Hours	25 Devices
LOW TEMPERATURE LIFE (-25°C, 7.0V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	5 Devices
TEMPERATURE CYCLE (-65°C TO +150°C, Air to Air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C TO +125°C, Liquid to Liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices

NOTE: Samples pulled from five different lots at finished goods.

Figure 3
SAMPLE ENVIRONMENTAL PROCESS MONITOR - 1 MEG SRAM

RELIABILITY

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). Using Micron's 4 Meg DRAM as an example, the failure rate is calculated as follows:

Failure Rate = $Pn \div [Device hours \times A.F. environment]$

A.F. is relative to the typical operating environment.

where: Pn = Poisson Statistic (at a given confidence level). In our example, Pn = 0.916 at at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 8.145×10^5 in an accelerated environment.

A.F. =acceleration factor between the stress environment and *typical* use conditions. For the 4 Meg DRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 89.2. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 4 Meg DRAM family is computed as follows:

Failure Rate = $0.916 \div (8.145 \times 10^5) (89.2) = 1.261 \times 10^{-8}$

where: total device hours at test conditions = 3.04×10^6 . Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 89.2 equals 89.2 (8.145×10^5) = 75×10^6 .

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10⁵:

Failure Rate = $(1.261 \times 10^{-8}) \times 10^{5} = 0.001261\%$ or 0.0013% per 1K device hours

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10°:

Failure Rate = $(1.261 \times 10^{-8}) \times 10^{9} = 12.61$ or 13 FITs

ACCELERATION FACTOR CALCULATION

Again, using the 4 Meg DRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$A.F._{t_1/t_2} = e \left[\frac{E_a}{kT_1} - \frac{E_a}{kT_2} \right]$$

where: $k = Boltzmann's constant , which is equal to <math display="inline">8.617 \times 10^{-5} \ eV/K$

T₁ and T₂ = typical operating and stress temperatures, respectively, in kelvins

E = activation energy in eV (For oxide defects, which is the most common failure mechanism for the 4 Meg DRAM, used in our example, the activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$A. \ F._{v_1/v_2} = e \left[\beta \left(\frac{v_1 \cdot v_2}{2} \right) \right]$$

where:

 ${\bf v}_1$ and ${\bf v}_2={\bf stress}$ voltage and typical operating voltage, respectively, in volts

 β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 4 Meg DRAM used in our example, β equals 4.92.)

Thus, the voltage acceleration factor for the 4 Meg DRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 11.70.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$A.F._{overall} = A.F._{temperature} \times A.F._{voltage}$$
$$= 7.62 \times 11.70$$
$$= 89.2$$

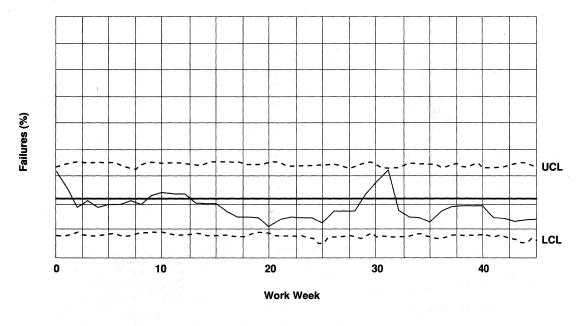


Figure 4 AMBYX™ FOURTH QUARTER FAILURES

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a one-percent sample from each production lot. These samples are subjected to visual and electrical testing in order to measure the acceptable quality level (AQL) of all outgoing product. Figure 4 shows a flowchart illustrating Micron's AQL test procedure.

Visual or mechanical testing consists of an unaided visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using

ATE (automatic test equipment) systems. Testing is conducted at room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the entire lot is retested at that point in the test flow. These are important steps to preserve the integrity of our test process.

Micron records the percent of devices found to be defective in the total number sampled weekly on a control chart. This chart, containing AQL data for the previous 52 weeks, is presented in weekly management meetings so that the quality assurance department can take appropriate action.

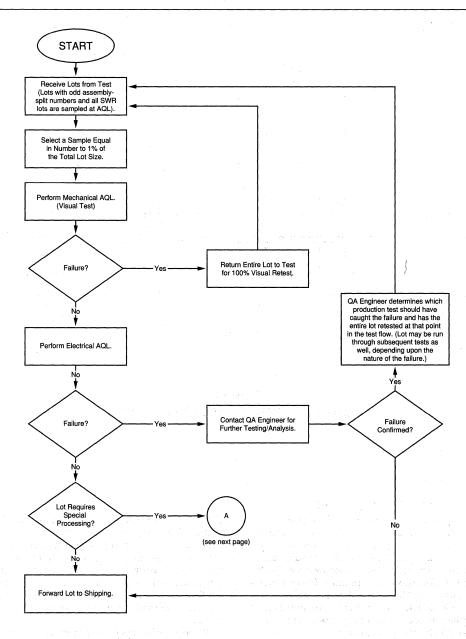


Figure 5
AQL TEST FLOW FOR ALL OUTGOING PRODUCTS



Example of Special Processing: Lot Mounted on Tape & Reel

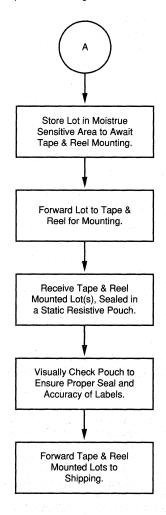


Figure 6
AQL TEST FLOW — SPECIAL PROCESSING

AUTOMATED DATA CAPTURE & ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 5 shows the various functional areas that provide the input to our VAX data bases.

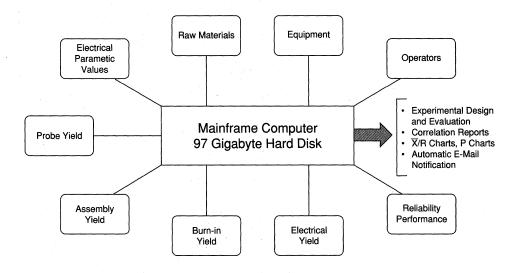


Figure 7
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting (\overline{X}) and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

ANALYTICAL TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make online projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the

impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.



CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors; such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

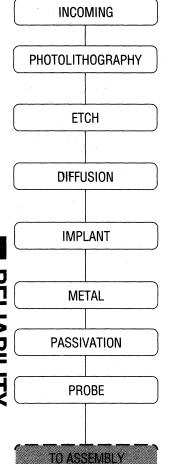
RS/1 DISCOVER/EXPLORE

This analysis software is used for experimental design, and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble shooting. It is also used to determine the relationships between process output and probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.



FABRICATION*



Incoming

Verification that the starting material is clean and uniform, and complies with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography

Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch

The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Thermal Processing

Wafers are placed in furnaces where they are exposed to various gases while being heated to temperatures over 1,000 degrees celsius.Layers similar to glass are grown on the wafer. These layers help form the building blocks for the circuitry constructed on each wafer.

Implant

Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping," and forms conductive regions on the wafer.

Metal

A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation

The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe

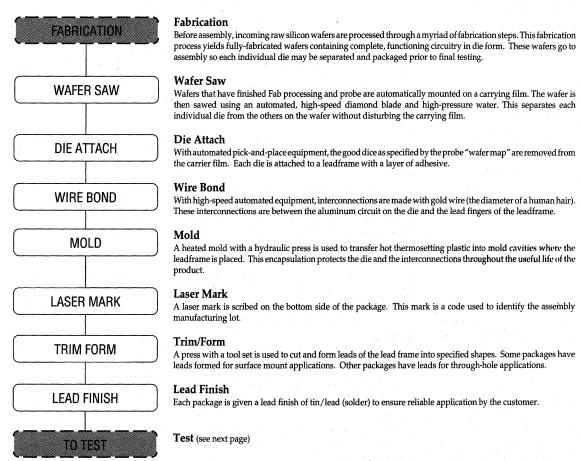
When the fabrication process is complete, each wafer consists of many "dice." Each die on the wafer is taken individually through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map" storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good dice are packaged.

Assembly (see next page)

^{*}This flow is general and is based on DRAM products.

RELIABILITY

ASSEMBLY*



^{*}This flow is general and is based on DRAM products.

ASSEMBLY HOT PREGRADE MARKING BURN-IN AMBIENT POST **HOT FINAL** SCANNER VISUAL INSPECTION QUARANTINE **PACKAGING** FINISHED GOODS

TEST*

Assembly

Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade

At temperatures ranging from 83°C to 125°C , parts are tested for speed grade and functionality. Parametric tests are performed to detect opens, shorts, input and output leakage, input and output high and low levels and standby current. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions, and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity. Specific tests and temperatures as applicable to specific products.

Marking

Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Burn-in

Micron uses its exclusive AMBYX™ intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 7.5V Vcc for the first two intervals and 125°C, 6V Vcc for the final two intervals. Functional testing is performed at 85°C and back to 25°C AMBYX™ tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 7.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Ambient Post

At a temperature of 25°C, parametric tests include input and output leakage as well as standby and operating currents. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Hot Final

At a temperature of 78°C to 100°C, parametric tests include input and output leakage as well as input and output high and low levels. Functional tests include low and high Vcc margin, vbump, speed sorting, dynamic and static refresh, and a full range of patterns and backgrounds. Patterns performed include row fast, column fast, single and multiple walking columns and diagonals, moving inversions and fast page or static column. Backgrounds used include solids, checkerboard, row stripes, column stripes and parity.

Scanner

Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection

All devices, now tested to be functional, are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired if possible. Data on the type of defects found is carefuly recorded and used for improving the manufacturing processes in both assembly and test.

Quarantine

All production lots are held at this stage until a quality assurance monitoring program confirms that electrical and environmental specifications are met.

Packaging

Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods

Devices are shipped through a system that maintains lot identity.

^{*}This flow is general and is based on DRAM products.

MICHON TECHNOLOGY, INC.

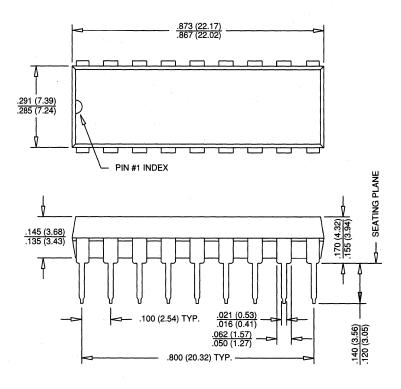
DYNAMIC RAMS	e I
WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9

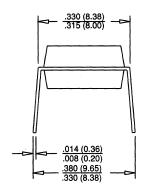


PACKAGE TYPE	PIN COU	NT	PAGE	PACKAGE TYPE	PIN COU	NT	PAGE
PLASTIC DIP	18		8-2	TSOP	20/26		8-16
	20		8-3		24/28		8-17
PLASTIC ZIP							
			-				
PLCC	52		8-8	MODULE SIP	30		8-22
PLASTIC SOJ	20/26		8-9	MODULE SIMM			
					12	•••••	0-34
				IC DRAM CARD.	88		8-41
		••••					
	42		8-15				

18-PIN PLASTIC DIP (300 mil)

N-1





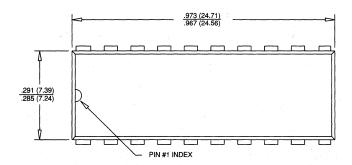
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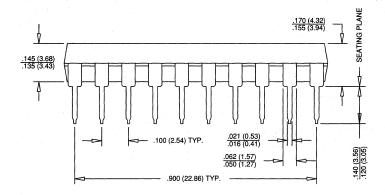
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- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

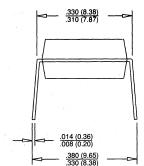
PACKAGE INFORMATION

20-PIN PLASTIC DIP (300 mil)

N-2





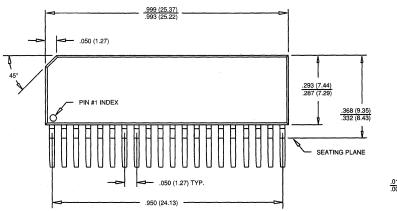


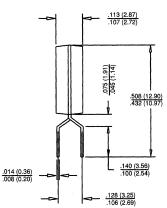
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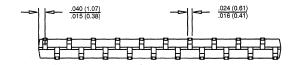
- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20-PIN PLASTIC ZIP (350 mil)

O-1





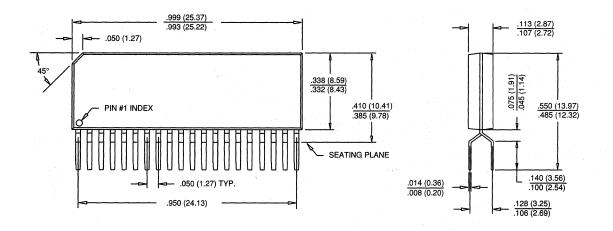


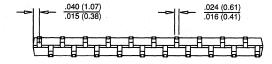
NOTE:

- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20-PIN PLASTIC ZIP (400 mil)

0-2



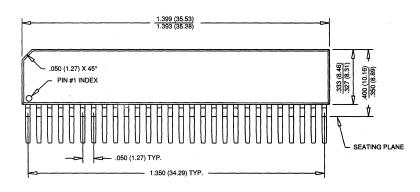


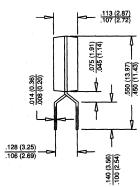
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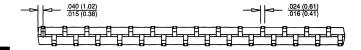
- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

28-PIN PLASTIC ZIP (375 mil)

O-3



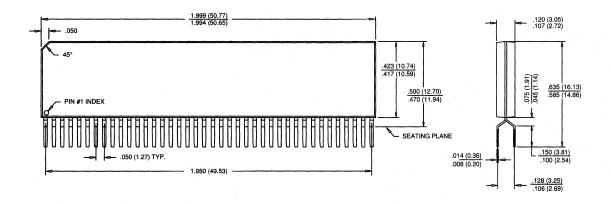


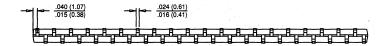


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

40-PIN PLASTIC ZIP (475 mil)

0-4



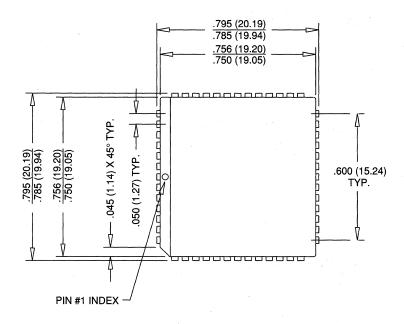


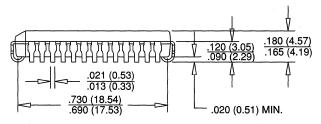
NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

52-PIN PLCC

P-1

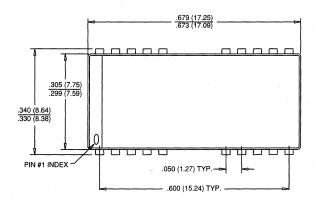


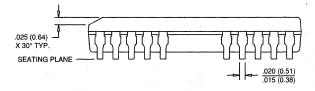


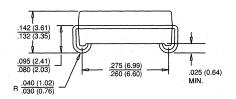
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- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

20/26-PIN PLASTIC SOJ (300 mil)

Q-1

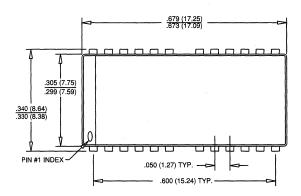


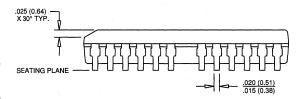


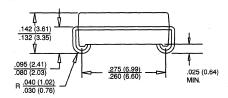


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

Q-2



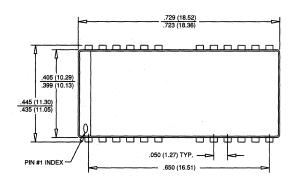


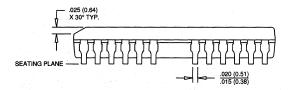


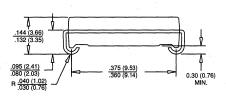
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- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.



Q-3

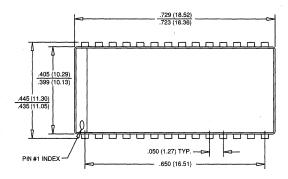


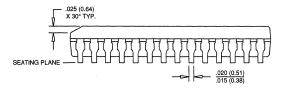


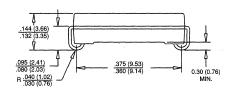


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

Q-4

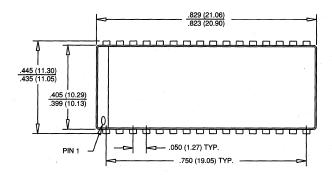


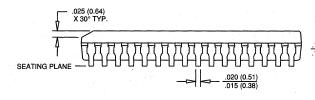


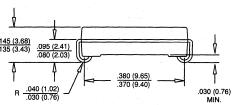


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

Q-5



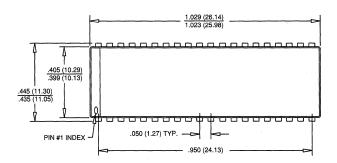


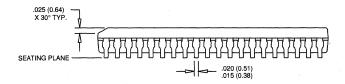


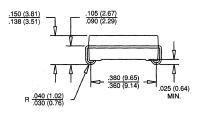
NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

Q-6

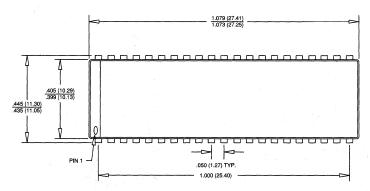


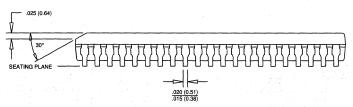


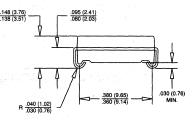


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

Q-7



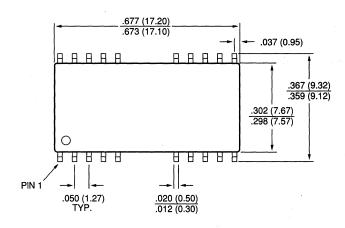


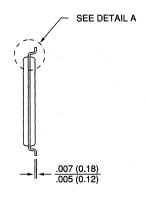


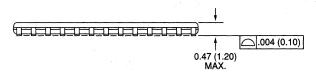
- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

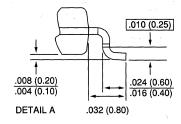
MICHON

20/26-PIN PLASTIC TSOP (300 mil) R-1







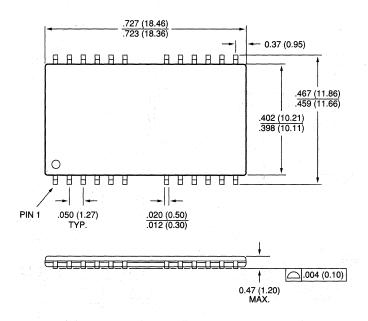


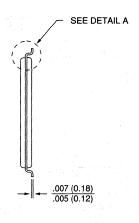
- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

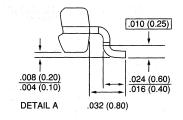


24/28-PIN PLASTIC TSOP (400 mil)

R-2

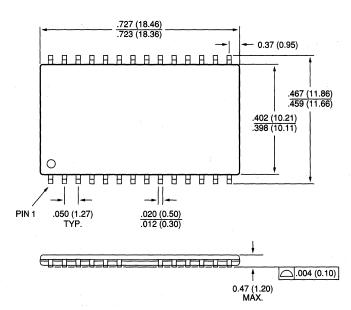


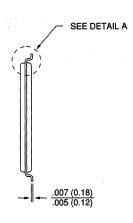


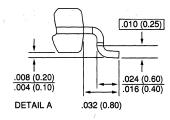


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

R-3



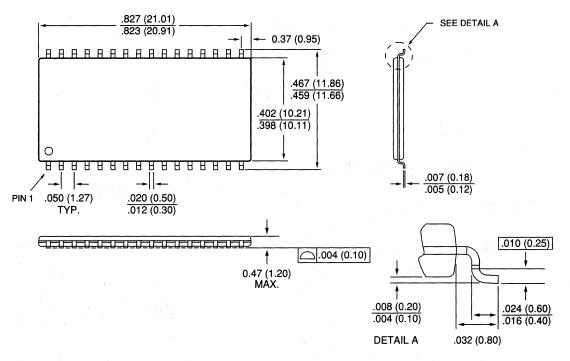




- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.



32-PIN PLASTIC TSOP (400 mil) R-4



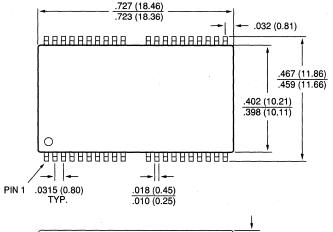
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

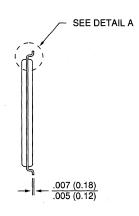
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.



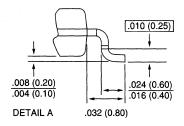
40/44-PIN PLASTIC TSOP (400 mil)

R-5







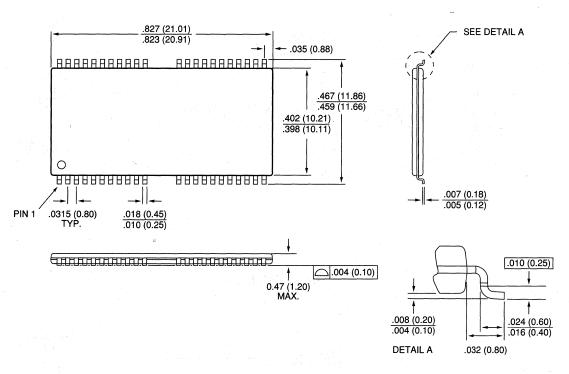


- 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
- 2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.



44/50-PIN PLASTIC TSOP (400 mil)

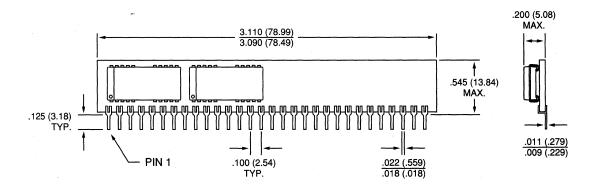
R-6



1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted. NOTE:

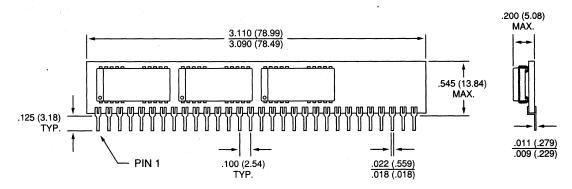
2. Package width and length do not include mold protrusion, allowable mold protrusion is .01" per side.

S-1



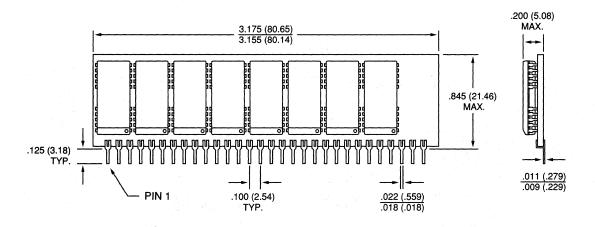
30-PIN MODULE SIP

S-2



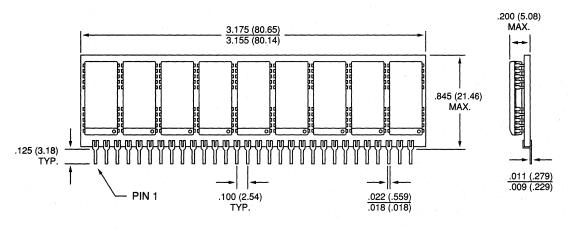
NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

S-3



30-PIN MODULE SIP

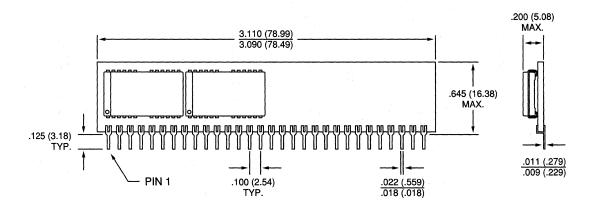
S-4



IOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.



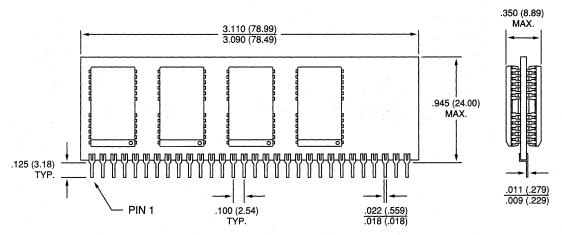
S-5



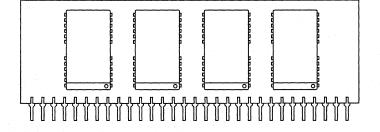
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

S-6

FRONT VIEW



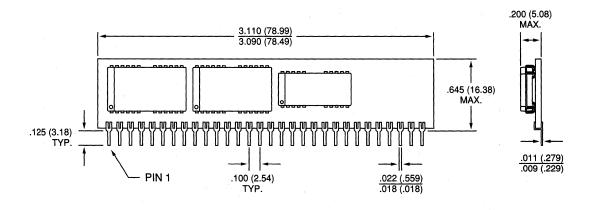
BACK VIEW



IOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



S-7

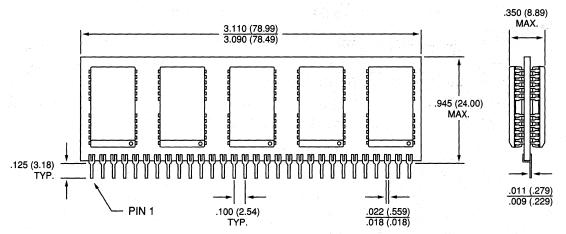


NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

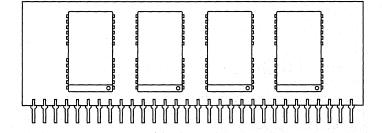
8-26

S-8

FRONT VIEW

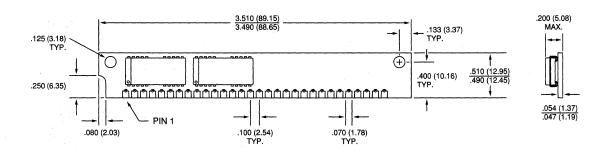


BACK VIEW



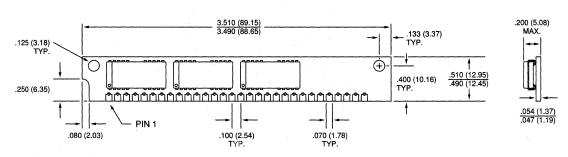
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

T-1



30-PIN MODULE SIMM

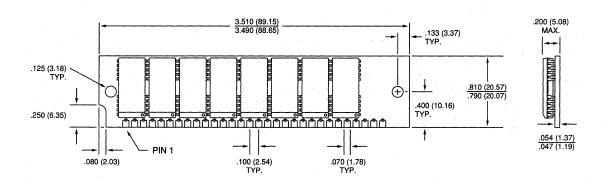
T-2



1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

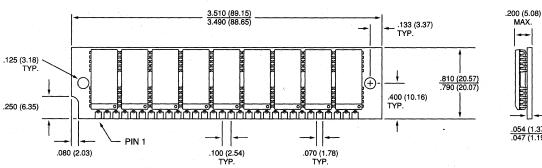
30-PIN MODULE SIMM

T-3



30-PIN MODULE SIMM

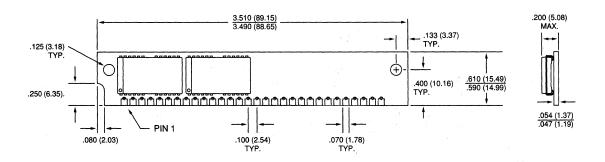
T-4



.054 (1.37) .047 (1.19)

1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted. IOTE:

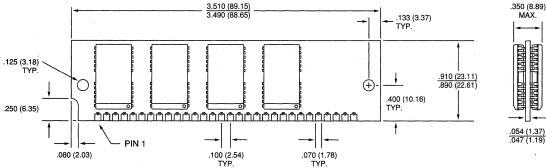
T-5

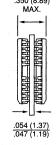


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

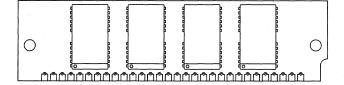
T-6

FRONT VIEW





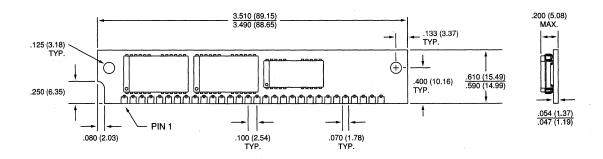
BACK VIEW



NOTE:

1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

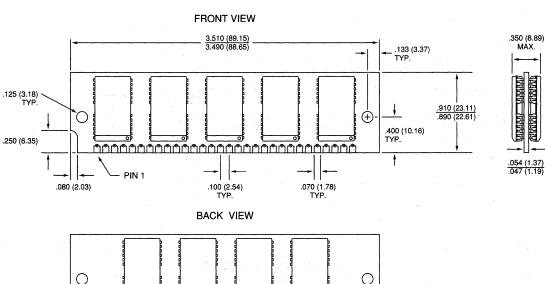
T-7



NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

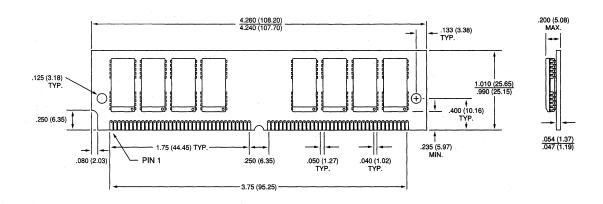
30-PIN MODULE SIMM

T-8



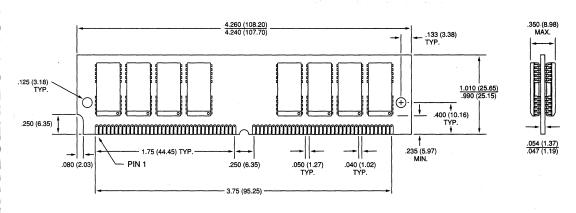
IOTE: 1. All dimensions in inches (millimeters) MAX/MIN or typical where noted.

T-9



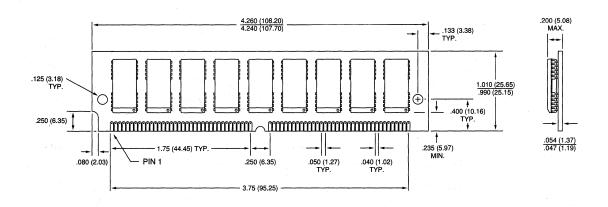
72-PIN MODULE SIMM

T-10



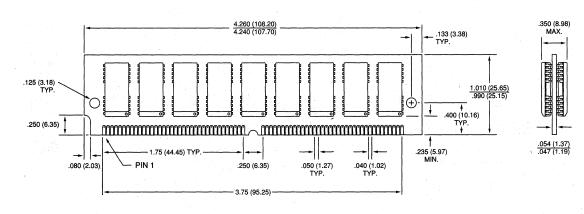
NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

T-11



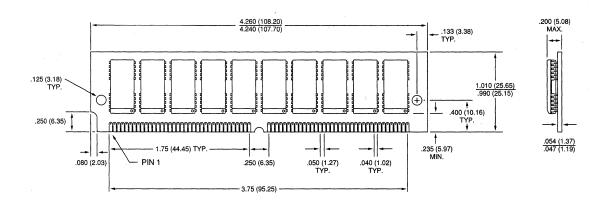
72-PIN MODULE SIMM

T-12



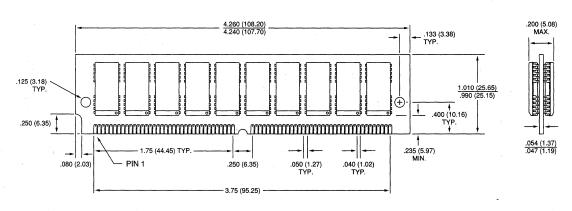
NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

T-13



72-PIN MODULE SIMM

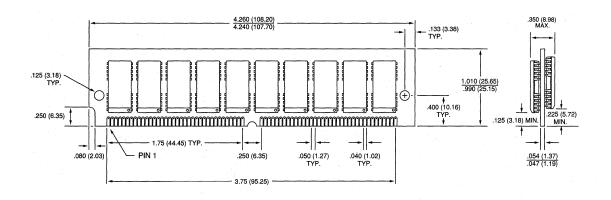
T-14



1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

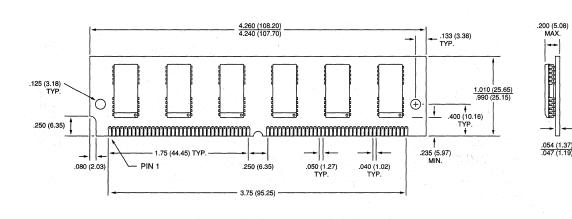
72-PIN MODULE SIMM

T-15



72-PIN MODULE SIMM

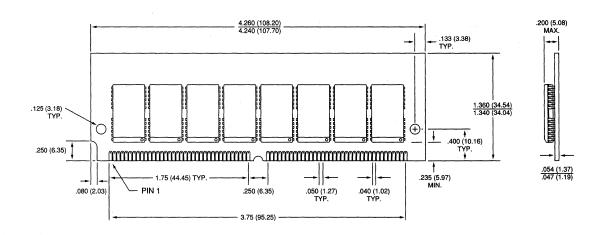
T-16



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

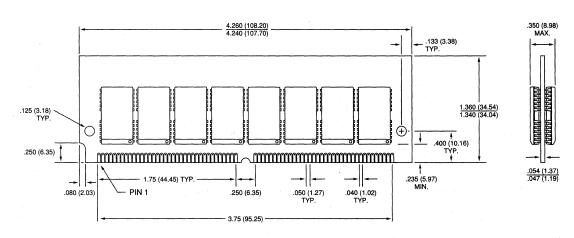
72-PIN MODULE SIMM

T-17



72-PIN MODULE SIMM

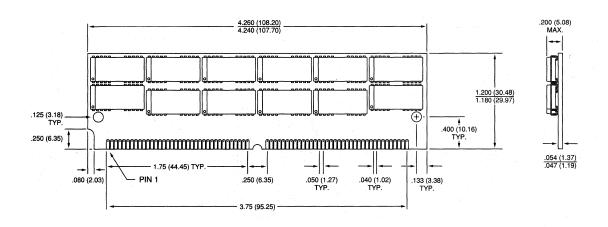
T-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

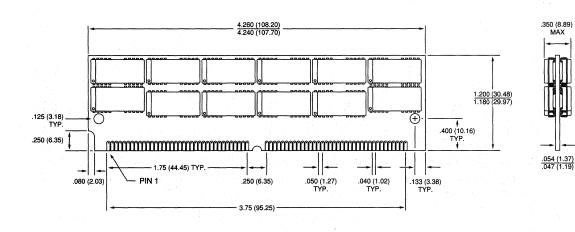
72-PIN MODULE SIMM

T-19



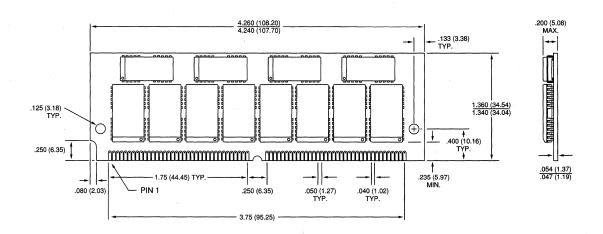
72-PIN MODULE SIMM

T-20



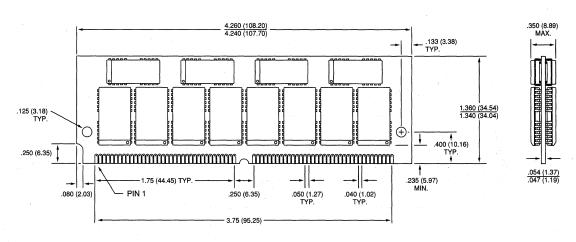
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

T-21



72-PIN MODULE SIMM

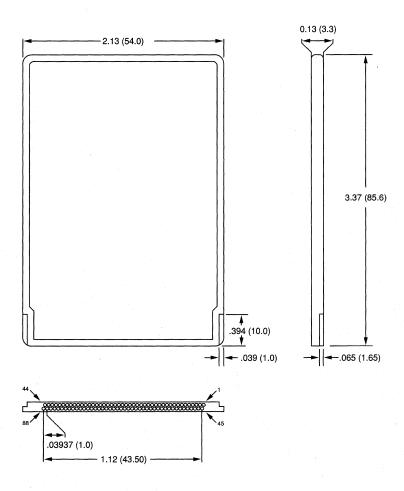
T-22



NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

88-PIN IC DRAM CARD

U-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.



SALES INFORMATION	9
PACKAGE INFORMATION	8
PRODUCT RELIABILITY	7
APPLICATION/TECHNICAL NOTES	6
MULTIPORT DRAMS	5
IC DRAM CARDS	4
DRAM MODULES	3
WIDE DRAMS	2
DYNAMIC RAMS	1



SALES INFORMATION

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Effective July 1, 1991, Micron Technology implemented new standard bar coding labels which will accompany all shipments. These labels conform to EIA Standard 556.

Samples and tape-and-reel boxes have their own individual bar code labels (see CSN-02). The bar code labels allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar coding label.

BAR CODE INFORMATION

The information provided on the label is: (S) — Serial: Individual box serial number

- (13Q) Special: Individual box number and total number of boxes in the shipment (example: 2 of 10)
 - (Q) Quantity: Total quantity of parts in the box
 - (K) Trans ID: Customer purchase order number
 - (P) Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address

Ship-From-Name: Micron name and address

Lot Date Code: Indicates date of oldest lot in the box

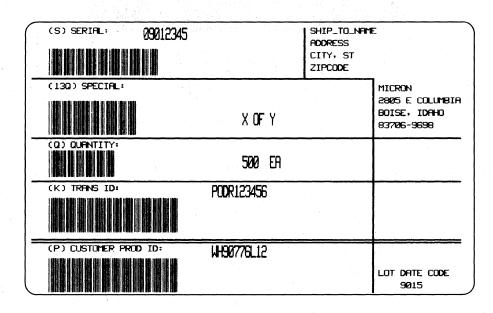


Figure 1
STANDARD BAR CODE LABEL

CUSTOMER SERVICE NOTE

TAPE-AND-REEL/SAMPLE BAR CODE LABELS

INTRODUCTION

Micron Technology provides a standard bar code label on each individual sample and tape-and-reel box. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multi-box shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*



09100084332 MT4C1024DJ-8 UD J1 1000 9117

> Figure 1 LABEL 1

*Indicates that more than one date code is contained on the reel.



CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCTS' SPC LABELS

INTRODUCTION

Effective November 15 1991, Micron Technology began providing a new SPC label on all surface-mount products. The label is attached to the static column bag for tubed products and to the front of the bag for tape-and-reel packaged products.

Figure 1 shows an example of the standard SPC label, while Figures 2 and 3 show the difference between the labels for tubed and tape-and-reel packaged products.

DATE INFORMATION

The SPC label includes the date on which the tube or reel was hermetically sealed in drypack. It also lists the ID number of the operator who sealed the product.



Figure 1
SURFACE-MOUNT PRODUCT SPC LABEL

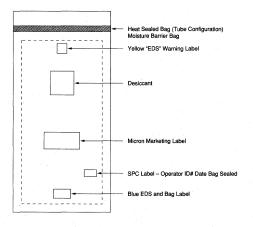


Figure 2
TUBED PRODUCT LABEL

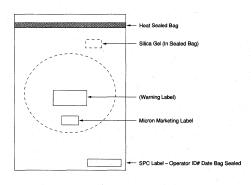
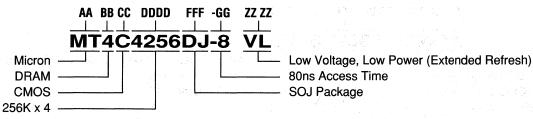


Figure 3
TAPE-AND-REEL PACKAGED
PRODUCT LABEL



EXPANDED COMPONENT NUMBERING SYSTEM

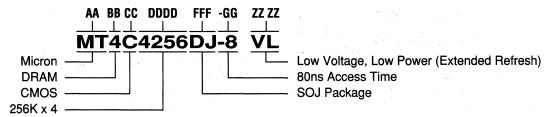


2001(X 4	
AA – PRODUCT LINE IDENTIFIER Component Product	MT
BB - PRODUCT FAMILY	
DRAM DPDRAM TPDRAM SRAM FIFO Cache Data SRAM Synchronous SRAM	
CC - PROCESS TECHNOLOGY	
CMOSLow Voltage CMOS	LC
DDDD – DEVICE NUMBER (Can be modified to indicate variations) DRAM DPDRAM TPDRAM SRAM CACHE Latched SRAM FIFO Synchronous SRAM	Width, Density Width, Density Width, Density Total Bits, Width Density, Width Total Bits, Width Width, Total Bits
E – DEVICE VERSIONS (Alphabetic characters only; located betwee required)	
JEDEC Test Mode (4 Meg DRAM) Errata on Base Part	
FFF - PACKAGE CODES	
PLASTIC DIP DIP (Wide Body) ZIP LCC	WZ

SOP/SOIC

FFF – PACKAGE CODES (continued)	
QFP	
TSOP (Type II)	
TSOP (Reversed)	RG
TSOP (Longer)	
S0J	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL
DIF * *	
DIÉ	XDC
Wafer	XWC
Military Die	
Military Wafer	
Ceramic	
DIP	_
DIP (Narrow Body)	
DIP (Wide Body)	
LCC	
LCC (Narrow Body)	
LCC (Wide Body)	
SOP/SOIC	
SOJ	
PGA	
FLAT PACK	F
GG - ACCESS TIME	
-55ns	or 50ns
-66ns	or 60ns
-77ns	or 70ns
-88ns	
-1010ns	
-1212ns	
-1515ns	
-17	
-20	
-25	
-35	
-45	
-50 (SRAM only)	
-53	53ns

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG - ACCESS TIME (continued) -5555ns -70 (SRAM only)70ns **ZZ ZZ - PROCESSING CODES** (Multiple processing codes are separated by a space and are listed in hierarchical order). A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: Low VoltageV DRAMS Low Power (Extended Refresh)L Low Voltage, Low Power (Extended Refresh)VL Low Power (Self Refresh) S Low Voltage, Low Power (Self Refresh)VS **SRAMS** Low Volt Data RetentionL Low Power P Low Power, Low Volt Data RetentionLP

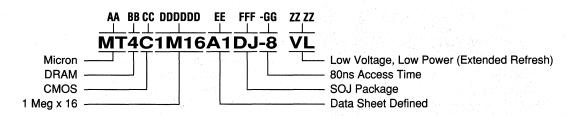
Low Voltage, Low PowerVP

ZZ ZZ – PROCESSING CODES (continued) Low Voltage, Low Volt Data Retention	\/I
Low Voltage, Low Volt Data Retention,	VL
Low Power	· · · \/B
EPI Wafer	V D
Commercial Testing	
0°C to +70°C	Rlank
-40°C to +85°C	TI
-40°C to +125°C	ΤΔ
-55°C to +125°C	XT
MII -CTD-992C Tecting	
-55°C to +125°C	8830
-55°C to +110°C (DRAMs)	
0°C to +70°C	M070
Special Processing	
	ES
Engineering Sample	MS
Sample Kit*	Sk
Tape and Reel*	
Bar Code*	

^{*} Used in device order codes; this code is not marked on device.

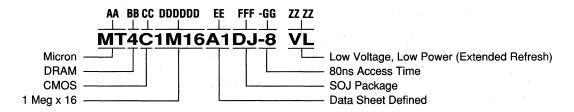
SALES INFORMATION

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER	FFF – PACKAGE CODES (continued) OFPLG
Component ProductMT	TSOP (Type II)TG
BB - PRODUCT FAMILY	TSOP (Reversed)
	TSOP (Longer)
DRAM4	SOJ DJ
DPDRAM	SOJ (Reversed)
TPDRAM43	SOJ (Longer) DL
Synchronous DRAM48	
SRAM5	
FIFO52	DieXDC
Latched SRAM56	WaferXWC
Synchronous SRAM58	Military DieXD
CC - PROCESS TECHNOLOGY	Military WaferXW
	CERAMIC
CMOS	DIP
Low Voltage CMOSLC	DIP (Narrow Body)CN
DDDDDD - DEVICE NUMBER	DIP (Wide Body)CW
그는 사람 하다 보고 사람들이 가게 하고 함께 느끼지 않는 모든 그는 그들의 사용이 없는 것이 없었다.	LCC (Narrow Body)ECN
Depth, Width	LCC :EC
Example:	LCC (Wide Body) ECW
1M16 = 1 Megabit deep by 16 bits wide = 16 Megabits of total memory	SOP/SOIC
No Letter Bits	SOJDCJ
K	PGA
	FLAT PACK F
MMegabits GGigabits	그리다일에 계시고 교육이에 그리면 이 작곡하는 모든데
	GG – ACCESS TIME
EE – DEVICE VERSIONS	-55ns or 50ns
(The first character is an alphabetic character only; the	-66ns or 60ns
second character is a numeric character only.)	-77ns or 70ns
Specified by individual data sheet	-88ns or 80ns
	-1010ns or 100ns
FFF – PACKAGE CODES	-1212ns or 120ns
Plastic	-1515ns or 150ns
DIPBlank	-1717ns
DIP (Wide Body)W	-2020ns
ZIPZ	-25
LCCEJ	-3535ns
SOP/SOICSG	-4545ns
	-50 (SRAM only)50ns

NEW COMPONENT NUMBERING SYSTEM (continued)



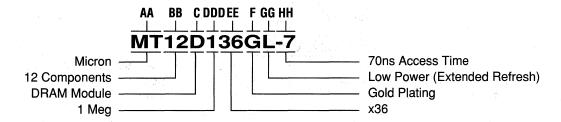
GG – ACCESS TIME (continued)
-5353ns
-5555ns
-70 (SRAM only)70ns
ZZ ZZ – PROCESSING CODES (Multiple processing codes are separated by a space and are listed in hierarchical order.)
Example: A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as: V L IT
Interim
Low VoltageV
DRAMs
Low Power (Extended Refresh)L
Low Voltage, Low Power (Extended Refresh)VL
Low Power (Self Refresh)
Low Voltage, Low Power (Self Refresh)VS
SRAMs
Low Volt Data RetentionL
Low PowerP
Low Power, Low Volt Data RetentionLP
Low Voltage, Low PowerVP

ZZ ZZ - PROCESSING CODES (continued) Low Voltage, Low Volt Data RetentionVL Low Voltage, Low Volt Data Retention, Low PowerVB EPI Wafer E Commercial Testing 0°C to +70°CBlank -40°C to +85°CIT -40°C to +125°CAT -55°C to +125°CXT MIL-STD-883C Testing -55°C to +125°C883C -55°C to +110°C (DRAMs)883C Special Processing Engineering SampleES Mechanical Sample MS Sample Kit*SK Tape and Reel*TR

Bar Code*

^{*} Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM

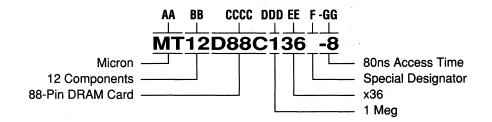


AA – PRODUCT LINE ID Micron Technology Co		
BB - NUMBER OF MEM	IORY COMPONE	NTS
C – RAM FAMILY SRAM DRAM		S
DDD – DEPTH		
EE – WIDTH		
F – PACKAGE CODE DIP Gold Plate ZIP SIP		G Z

Low Power	<u> </u>
and the second of the second o	
-10	10ns or 100ns
-15	15ns
-20	20ns
-25	25ns
	30ns
	35ns
-45	45ns
	60ns
	70ns
-8	80ns

SALES INFORMATION

IC DRAM CARD NUMBERING SYSTEM



Micron Technology Component Product	МТ
BB - NUMBER OF MEMORY COMPONENTS	3 , *
CCCC - DRAM CARD DESIGNATOR AND PI	N COUNT
88-Pin DRAM Card	D88C
60-Pin DRAM Card	D60C
DDD – DEPTH	

AA - PRODUCT LINE IDENTIFIER

EE - WIDTH

F - SPECIAL DESIGNATOR

SALES INFORMATION

ORDER INFORMATION*

Each Micron component family is manufactured and quality controlled in the USA at our modern Boise, Idaho, facility employing Micron's low-power, highperformance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX™ intelligent burn-in and test system.

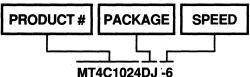
Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributors nearest you. Micron's quality assured policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

> Telephone: (208) 368-3900 FAX: (208) 368-4431 **Customer Comment Line:** (800) 932-4992 (USA) 01 (208) 368-3410 (Intl.)

ORDER EXAMPLES

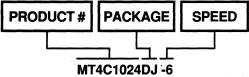
DRAM

1 Meg x 1, 60ns in Plastic SOJ



DRAM MODULE

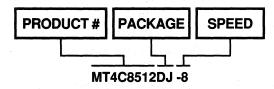
1 Meg x 8, 60ns in SIMM Module





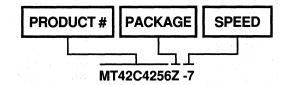
WIDE DRAM

512K x 8, 80ns in Plastic SOJ



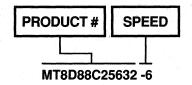
MULTIPORT

256K x 4, 70ns in Plastic ZIP



IC DRAM CARD

256K x 32, 60ns IC DRAM Card



*For more detailed information, refer to the Product Numbering charts on pages 9-4 through 9-9.



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WIDE DRAMS	2
DRAM MODULES	3
IC DRAM CARDS	4
MULTIPORT DRAMS	5
APPLICATION/TECHNICAL NOTES	6
PRODUCT RELIABILITY	7
PACKAGE INFORMATION	8
SALES INFORMATION	9

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3	DRAM MODULES
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7	PRODUCT RELIABILITY
8	PACKAGEINFORMATION
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