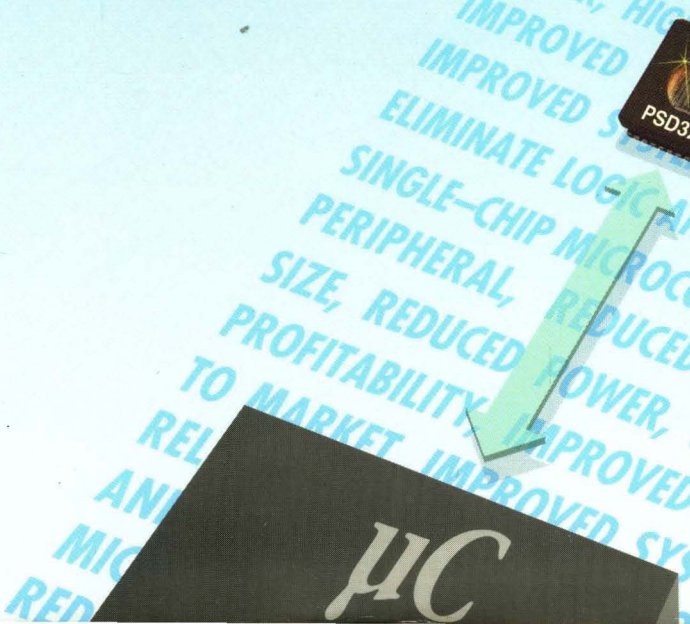
Programmable Peripherals Design and Applications Handbook



Programmable Peripherals Design and Applications Handbook

1992

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Printed in U. S. A.

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General Information

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363.

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Company Profile

Company Description

WSI is a market leading producer of high-performance programmable peripheral integrated circuits. The company was founded in 1983 to serve the needs of system designers who need to achieve higher system performance, reduce the size and power consumption of their systems, and shorten their product development cycles in order to achieve faster market entry.

WSI produces an innovative portfolio of Programmable Peripherals as well as a broad line of high-performance non-volatile programmable PROM and EPROM memory products, both based on its patented self-aligned split-gate CMOS EPROM technology. The new Programmable Peripherals enable rapid system design of high-performance application specific controllers and related products. These devices are the first to integrate high-performance EPROM, SRAM and user-configurable logic and deliver a performance and integration breakthrough to the programmable peripherals market.

WSI's Programmable Peripherals and non-volatile memory products enable electronic designers to reduce their system size, shorten product development cycles and bring new system products to market in less time. As a result, WSI has established itself as a leading supplier of high-performance programmable solutions to a broad customer base that includes some of the world's largest and most technologically advanced electronics companies.

Technology

WSI's patented self-aligned, split-gate EPROM technology enables higher performance and greater memory densities per chip area than the traditional stacked-gate method. By developing significantly higher read current, the WSI EPROM cell has enabled the development of several memory devices that are the fastest of their type on the market. This core NVM technology is further leveraged by WSI's architecture and design innovations such as staggered virtual ground and contactless memory arrays resulting in dramatic die area savings. This high density memory capability enables WSI to provide cost-effective market leading products such as the smallest 4-Mbit EPROM on the market. WSI's proprietary NVM technology (licensed to Sharp Corporation and National Semiconductor Corporation) has enabled WSI to be first in the industry with numerous product breakthroughs in speed, high density, process innovations and packaging.

Markets and Applications

WSI's Programmable Peripheral and high-performance non-volatile memory products are used by the world's leading suppliers of advanced electronic systems in telecommunications, data processing, military, automotive and industrial markets.

Applications for the Programmable Peripherals include cellular telephones, disk drive controllers, modems, bus controllers, engine management computers, telecom switchers, motor controllers and others. High performance memory applications include digital signal processing, engineering workstations, high-speed modems, video graphics controllers, radar and others. By virtue of their high speed and programming capability, WSI products are ideally suited for these applications where designers are pushing the limits of system performance in highly competitive markets.

Product Groups

Programmable Peripherals

WSI's family of Programmable Peripherals represents a new class of programmable products. They enable system designers to reduce the size of their products, achieve lower operating power, optimize system performance and shorten product development cycles. They are the first devices to integrate high-speed EPROM, SRAM and programmable logic on a single chip. The Programmable Peripherals include the PSD3XX family, the MAP168 and the PAC1000.

PSD3XX Family: Microcontroller Peripherals with Memory

Each member of the PSD3XX family is a single-chip, field-programmable circuit that integrates all the required peripheral memory and logic elements for an embedded-control design. Programmable logic, page logic, programmable I/O ports, busses, address mapping, port address/data tracking, 256K to 1 Mb EPROM, and 16K SRAM are all on board. Advanced features such as memory paging, microcontroller port reconstruction, track mode, configuration security bit, and cascading further enhance the utility and value of the PSD3XX family. PSD3XX family devices are ideal for applications requiring high-performance, low power and very small form factors such as fixed disk control, cellular telephones, modems, computer peripherals, and automotive and military applications.

MAP168 User-Configurable Peripheral with Memory

Similar to the PSD3XX family, the high speed MAP168 integrates high-performance EPROM, SRAM, a PAD and user-configurable logic. Ideal for high-speed applications requiring expanded memory, system integration and increased data security, the 45 ns MAP168 is used with high speed digital signal processors, microprocessors and microcontrollers.

PAC1000 Peripheral Controller

The high speed PAC1000 sets a new standard for Programmable Peripheral performance, integration and functionality. The PAC1000 replaces up to 50 complex devices in high-end embedded controllers and microprocessor-based systems. Combining a CPU, 1K x 64 EPROM and extensive user-configurable logic, the PAC1000 assists its host processor with high rates of data manipulation and control, freeing the processor for other system functions. The 16 MHz PAC1000 has been designed into numerous high-performance applications such as work-station direct memory access controllers, video imaging digital signal processors, and VME bus LAN controllers.

Programmable Peripheral Development Tools

WSI's Programmable Peripheral products are supported with complete easy-to-use system development tools from both Data I/O and WSI. The Data I/O Unisite programmer can be used for production programming. The WSI tools include program development, simulation, and programming software, the IBM-PC hosted MagicPro™ Memory and Peripheral Programmer, a dial-in applications bulletin board and WSI's team of factory service and field application engineers. The menu-driven software tools run on popular customer owned computers and enable designers to rapidly configure and program the WSI part and try it in a prototype system. Additional design iterations are quickly accomodated. The system development tools increase the efficiency of the design process resulting in faster market entry for WSI's customers' products.

High-Performance Memory Products

WSI offers a broad product line of high-performance CMOS PROMs and EPROMs featuring architectures ranging from 2K x 8 to 512K x 8, plus several x16 products, with speeds ranging from 25 to 150 ns. Commercial, industrial and military products including MIL-STD-883C/SMD are available. A wide variety of package selections include plastic and hermetic, through-hole and surface mount types.

CMOS PROMs

As WSI's fastest family of products, Re-Programmable Read Only Memories (RPROMs) provide high-speed bipolar PROM pinout with matching speed and low power operation. The product family includes architectures ranging from 2K x 8 to 32K x 8 with speeds ranging from 25 to 90 ns. Commercial, industrial and military MIL-STD-883C/SMD configurations are available in a variety of hermetic and plastic package types.

"F" Family EPROMs

The high-speed "F" series EPROM family offers speeds ranging from 35 to 70 ns and architectures from 8K x 8 to 32K x 8, plus several x16 products. "F" family EPROMs are ideal for use in high-end engineering and scientific workstations, data communications and similar high-performance applications.

"L" Family Military EPROMs

WSI's "L" family military EPROM memory products feature high-density and high speed in popular JEDEC pinouts. With speeds ranging from 120 to 300 ns and architectures from 64K x 8 to 512K x 8 including several x16 products, the "L" family offers significant speed and high density benefits for developers of military avionics, communications, and control systems. The "L" family delivers world class densities from WSI's conservative 1.2 micron lithography CMOS process technology.

Manufacturing

WSI's manufacturing strategy includes utilizing multiple world-class manufacturing partners for each facet of the production process.

WSI has licensed its CMOS EPROM and logic process technology to Sharp Corporation in Japan and National Semiconductor Corporation in the USA. The Sharp facility in Fukuyama, Japan employs the most advanced sub-micron VLSI integrated circuit manufacturing equipment available including ion implantation, reactive ion etch, and wafer stepper lithographic systems. The world-class high volume National Semiconductor operation delivers low cost production of 1.2 micron CMOS technology product on 6" wafers. This low defect density manufacturing resource is capable of producing sub-micron technology product in the near future.

High-volume, low cost integrated circuit packaging and testing is performed for WSI by ANAM Electronics in Seoul, Korea, Fine Products in Hsinchu,Taiwan, National Semiconductor in Santa Clara, CA and at WSI in Fremont, CA. ANAM is the largest independent manufacturer of I.C. packaging and produces excellent product quality. Test capability ranges from simple logic devices to complex VLSI product. ANAM routinely processes a wide variety of high volume packages and enables WSI to leverage its materiel needs through ANAM's combined high-volume, low cost procurement activity. Commercial, industrial, and military grade product processing is available from ANAM.

Additional quality assurance and reliability testing are performed at WSI in Fremont, CA.

WSI's manufacturing strategy ensures the supply of double-sourced high quality, high-volume product with low variable cost and fast delivery.

Sales Network

WSI's international sales network includes several regional sales managers who direct the resources of the company to major market opportunities. Experienced technical field application engineers located in each field office assist WSI's customers during their advanced product development and match customer needs with WSI's product solutions. Over sixty manufacturer's representatives and leading national and regional component distributors in the United States, Europe and Asia round out the WSI sales network.

United States

Direct sales and field application engineering offices in Boston, Chicago, Huntsville, Philadelphia, Dallas, Los Angeles and Fremont, CA; More than 25 manufacturer's representatives for major national accounts; national distributors include Arrow/Schweber, Time Electronics and Wyle Laboratories; and regional distributors.

International

Direct WSI Sales management offices in Paris, Munich and Hong Kong; sales representatives and distributors in Germany, England, France, Italy, Sweden, Finland, Denmark, Norway, Spain, Belgium, Luxembourg, the Netherlands, and Israel. Sales representatives and distributors for the Asia/Pacific Rim region in Japan, Korea, Taiwan, Hong Kong, Singapore and Australia.

Management and Previous Affiliations:

Michael Callahan
President, CEO and
Chairman of the Board
(Advanced Micro Devices, Monolithic Memories, Motorola)

Robert J. Barker
V. P. Finance, CFO and Secretary
(Monolithic Memories, Lockheed)

John Ekiss
V. P. Marketing
(Intel, Motorola)

Thomas Branch
V. P. Worldwide Sales
(Monolithic Memories, Fairchild)

George Kern
V. P. Operations
(Advanced Micro Devices, Monolithic Memories)

Boaz Eitan
V. P. New Product and Technology Development
(Intel)

Bob Buschini
Director of Human Resources
(General Electric, Raychem)

Financing

WSI is a privately held California corporation founded in August, 1983. The company has been financed by corporate investors, institutional investors, venture capital groups and private investors. Corporate investors are Sharp Corporation, National Semiconductor Corporation, Intergraph Corporation, and Kyocera Corporation. Venture capital investors include Accel Partners, Adler and Company, Bessemer Venture Partners, Genevest Consulting Group S. A., J. H. Whitney, Oak Investment Partners, Robertson Stephens and Co., Smith Barney Venture Corporation, and Warburg Pincus. The company has been audited annually since its inception by Ernst & Young (Arthur Young prior to 1989) and regularly reports financial information to Dunn & Bradstreet (Dunns number is 10-209-8167).

PROGRAMMABLE SYSTEM™ DEVICE FITS MULTIPLE MICROCONTROLLERS

IC HAS EPROM, RAM, AND LOGIC FOR 45 CONFIGURATIONS; INTERFACES 8- AND 16-BIT MICROCONTROLLERS.

MILT LEONARD

The embedded-controller market embraces a myriad of 8- and 16-bit microcontroller architectures that can satisfy just about any conceivable application requirement. However, each different controller requires its own unique combination of discrete devices to link the part to other system elements. Furthermore, changing application requirements usually call for restructuring I/O ports. Consequently, the application may eventually outgrow system memory and shared resources may demand multiple chip solutions. This means that in addition to comparing controllers on the merits of price and performance, prospective users must also consider the external circuitry that the controller needs to interface to the rest of the system.

A new chip from WaferScale Integration Inc., Fremont, Calif., simplifies system integration by combining RAM, EPROM, programmable decoding, and configurable I/O ports that expand 8- or 16-bit microcontrollers when they run out of on-chip resources. WaferScale's PSD301 is the first single-chip solution to offer a microcontroller with port expansion, latched address lines, a programmable address decoder (PAD), an expansion interface to shared resources, a 256-kbit EPROM, and a 16-kbit static RAM. In addition, the chip links directly to popular 8- and 16-bit microcontrollers without using glue logic.

The PSD301 architecture is a major enhancement of WaferScale's MAP168 mappable memory chip introduced last year *(see* ELECTRONIC DESIGN, *July 28, 1988, p. 91)*. In addition to the memory, decoding, and multiplexer functions of the 168, the 301 includes three software-configurable 8-bit I/O ports (A, B, and C), configuration registers, latched inputs, more chip-select lines, and more control on the strobe lines *(Fig. 1)*. Like the 168, a programmable security bit is given to protect against reverse engineering.

Most controllers can't be reprogrammed once they're configured. Moreover, their controller's I/O ports are designed to perform one of two mutually exclu-

USER-CONFIGURABLE MICROCONTROLLER INTERFACE

sive functions: convey control signals to peripheral devices or address and data signals to shared resources. Supplying both of these functions requires a multiple chip solution.

Microcontrollers also differ in boot-up locations and address mapping in memory. The 8051 and 8096 microcontrollers, for example, locate boot-up sequences in the lower half of their memory maps, while the 80186/88 and 68HCXXX use a high memory boot-up address. Another factor is the differences in control-signal polarities.

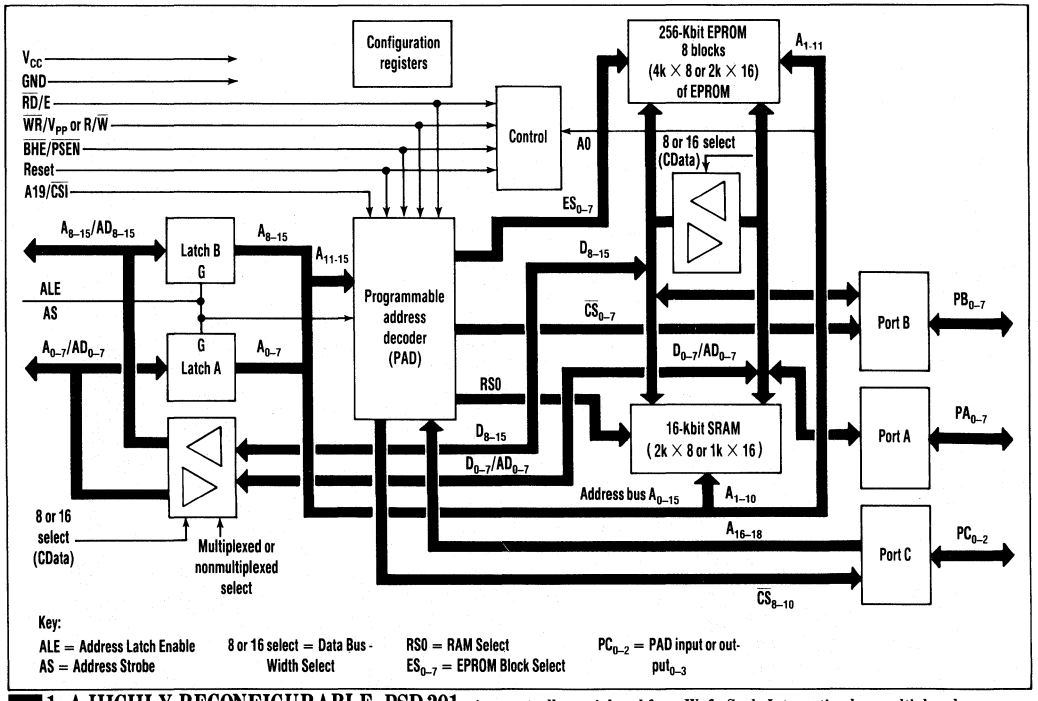
The **PSD301** is designed to adapt the characteristics of different microcontrollers to an embedded-control design. The PAD plays a major role in this function. It performs similarly to a small programmable array logic (PAL) device. The PAD has up to 13 inputs and 11 outputs in a NOR-gate array, and it can implement up to four sum-of-product expressions based on address inputs, control signals, and chip-select inputs. The PAD selects all of the chip's internal parts. and generates external chip selects with a 35-ns delay.

Address inputs from the host microcontroller are first fed to the 301's input latches, which stabilize the inputs when the device accesses memory in the multiplexed mode. The latches are made transparent in the nonmultiplexed mode. Five low-order address inputs and five programmable control lines are fixed functions; the Address-Latch-Enable and Reset lines have programmable polarity. The high-order address lines can be either address or general-purpose inputs for logic functions.

For more efficient use of memory space, internal and external PAD-Select signals can override EPROM memory with overlapping addresses. Therefore, if all of the EPROM isn't used for program storage, the unused space can be allocated to I/O ports, static RAM, or other PAD-select signals.

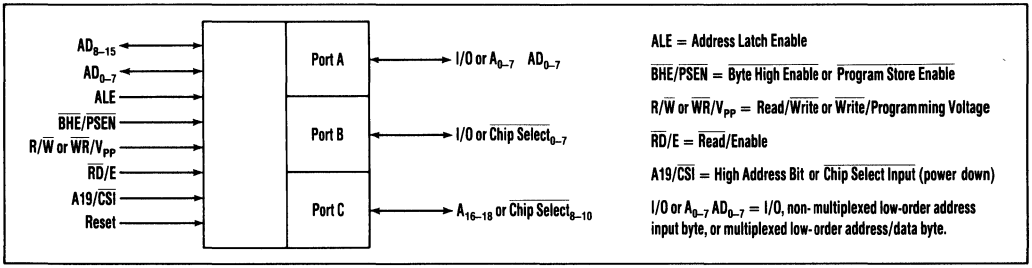
The EPROM is configurable as 32 kwords by 8 bits, or 16 kwords by 16 bits, and it's partitioned into eight equal mappable blocks with a resolution of 4 kbytes or 2 kwords. Access time, including PAD decoding time, is 120 ns. The configuration registers also consist of EPROM cells. The registers store the programmed configuration bits that make it possible for users to set the device, I/O, and control functions according to the required operating mode. The 16-kbit 120-ns static RAM is configurable as 2 kwords by 8 bits, or 1 kword by 16 bits. The memory blocks can be noncontiguously mapped over the addressable range of 1 Mbyte or 0.5 Mwords. Consequently, programmers can scramble the code to prevent direct copying.

I/O ports A and B in the 8- and 16-



1. A HIGHLY RECONFIGURABLE PSD 301 microcontroller peripheral from WaferScale Integration has multiplexed or nonmultiplexed data and address buses with selectable 8- or 16-bit bus widths. The programmable address decoder (PAD) helps supply up to 45 configuration options for supporting a range of 8- and 16-bit microcontrollers.

USER-CONFIGURABLE MICROCONTROLLER INTERFACE



2. I/O PORT CONFIGURATION FOR THE PSD301 IS PROGRAMMED by signals from the PAD, which are derived partly from programmed bits in the configuration registers. The three ports configured for multiplexed address and data with a 16-bit wide data bus are shown.

bit configurations are data ports in the nonmultiplexed mode, and both ports can be configured as either data or address ports in the multiplexed mode *(Fig. 2)*. Port C is independent of any configuration—it can supply multiple chip-select outputs or serve as address inputs.

The default configuration of port A in the nonmultiplexed address/data mode sets the port to deliver I/O lines. In this mode, each pin can be set as an input or output and can have a CMOS or open-drain output. Alternatively, each bit of port A can be configured as a low-order latched-address-bus bit to access external peripherals or memory that requires several low-order lines. Another option in this mode sets the entire port to track the low-order address/data multiplexed bus. This feature links the host microcontroller to shared resources without the use of external buffers and decoders.

In the nonmultiplexed mode, port A becomes the chip's low-order data-bus byte. When a read operation is executed from an internal 301 location, data is directed out on port A pins. When a write cycle is executed into an internal 301 location, data is driven into port A.

The operation of port B in the multiplexed address/data and 8-bit nonmultiplexed modes is the same as port A. However, as an alternative, each bit can be configured to supply a Chip-Select Output signal from the PAD. In the 16-bit nonmultiplexed mode, port B is the high-order data-bus byte of the chip. When a read operation is executed from an internal high-order data-bus byte location, the data appears on port B pins. When a write operation is executed into an internal high-order data-bus byte location, data and write operation signals are present at port B.

Each pin of port C in all modes can be configured as an input or output from the PAD. Although designated as high-order address bus pins, they can be used for any logic inputs to the PAD or for external chip-select outputs from the PAD.

With this degree of operational flexibility, the 301 can team up with all popular 8- and 16-bit microcontrollers from such companies as Advanced Micro Devices, Intel, Motorola, National Semiconductor, Texas Instruments, and Zilog. For example, the polarity of the 301's control signals can be programmed for direct connection of the read-write and output enable pins of the 68HCXX microcontroller family. The 16-bit configuration can boost the performance of 16-bit controllers, such as the 80186, 8096, 80196, 16000, and others, without adding external devices. And the 8051 microcontroller family can extend its memory space by using the separate address and program memory space of the 301. The 301 is cascadable for increased width or depth for multiplexed byte- or word-wide embedded-control designs.

In the standby mode, commercial versions of the 301 draw 150 μA and 1.5 mA for CMOS and TTL interfaces, respectively. Active current for CMOS interfaces with or without selected memory blocks, or with the EPROM blocks selected, is 55 mA. That level increases to 80 mA for TTL interfaces. Selecting the static RAM block increases active current to 105 mA and 130 mA for CMOS and TTL, respectively.

WaferScale Integration houses the device in a 44-pin surface-mounted package to meet the form-factor requirements of such products as 5.25-, 3.5-, and 2.5-in. disk drives, cellular phones, and modems. System development tools include an IBM-PC plug-in programmer board and remote socket adaptor. They also contain a software development package that runs on an IBM PC/XT/AT or compatible computer with a MS-DOS version 3.1 or higher, 640 kbytes of RAM, and a hard disk.□

PRICE AND AVAILABILITY

The commercial version of the PSD301, packaged in a 44-pin plastic leaded chip carrier, is priced at $15 each in quantities of 1000. Military parts are also available. Other package options are ceramic leaded chip carriers and pin grid array packages with windows. The PSD301 is being sampled now, with production quantities available in January, 1990.

WaferScale Integration Inc., 47280 Kato Rd., Fremont, CA 94538; (415) 656-5400.

WAFERSCALE INTEGRATION, INC.

PROGRAMMABLE PERIPHERALS

SINGLE-CHIP CMOS USER-CONFIGURABLE PERIPHERAL WITH MEMORY – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	Q	X
PSD301	Programmable Microcontroller Peripherals with Memory; x8/x16; 256Kb – 1Mb EPROM; 16K SRAM; PAD; System Features.	120		NOW	Q4 '91	•	•	•	
		150-200		NOW	NOW	•	•	•	•
			200		NOW		•		•
PSD311		120		NOW	Q4 '91	•	•	•	
		150-200		NOW	Q4 '91	•	•	•	•
			200		Q4 '91		•		•
PSD302		120		NOW	Q1 '92	•	•		
		150-200		NOW	Q1 '92	•	•		
PSD312		120		NOW	Q1 '92	•	•		
		150-200		NOW	Q1 '92	•	•		
PSD303		120		Q4 '91	Q1 '92				
		150-200		Q4 '91	Q1 '92				
PSD313		120		Q4 '91	Q1 '92				
		150-200		Q4 '91	Q1 '92				
MAP168	DSP Peripheral with Memory. Features: 128K Bits EPROM, 32K Bits SRAM Programmable Address Decoder (PAD) Configurable: x8 or x16.	45-55		NOW	NOW	•	•	•	•
			55		NOW	•		•	

HIGH-PERFORMANCE CMOS USER-CONFIGURABLE EMBEDDED CONTROLLER – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection Q	X
PAC1000	Programmable Peripheral Controller optimized for High-Performance Control Systems. Key Features Include: 16-Bit CPU, 16-Bit Address Port, 16-Bit Output Control, 8-Bit I/O Port and Configuration Registers.	12MHz		NOW	NOW	•	•
			12MHz	NOW	NOW		•
		16MHz		NOW	NOW	•	•

HIGH-PERFORMANCE CMOS USER-CONFIGURABLE MICROSEQUENCER/STATE MACHINE – COMMERCIAL & MILITARY

Part No.	Description	Speed (ns) Comm'l	Speed (ns) Military	Availability Samples	Availability Prodn	Package Selection J	L	S	T
SAM448	User-Programmable Microsequencer for Implementing High-Performance State Machines. Includes EPROM integrated with Branch Control Logic, Pipeline Register, Stack and Loop Counter and 768 Product Terms.	20-25MHz		NOW	NOW	*	•	*	•
			20MHz	NOW	NOW		•		•

*J and S packages not available in 30MHz

SOFTWARE DEVELOPMENT TOOLS †

Part No.	Includes	Availability
PSD - GOLD	Contains PSD301/MAP168 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6014(J/L) or WS6015(X) Adapter and 2 Sample Devices	NOW
PSD - SILVER	Contains PSD301/MAP168 Software and Users Manual	NOW
PAC1000 - GOLD	Contains PAC1000 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6010 (X) Adapter and 2 Sample Devices	NOW
PAC1000 - SILVER	Contains PAC1000 Software and Users Manual	NOW
SAM448 - GOLD	Contains SAM448 Software, Users Manual, WS6000 MagicPro (PC Based Programmer), WS6008(T) or 6009(C,J,L) Adapter and 2 Sample Devices	NOW
SAM448 - SILVER	Contains SAM448 Software and Users Manual	NOW
MEMORY - SILVER††	Contains WSI EPROM/RPROM Programming Software and Users Manual	NOW

† 1) All Development Systems include: 12 Month Software Update Service, access to WSI's 24 Hour Electronic Bulletin Board.
2) Package adaptor must be specified when ordering any "Gold" system.

†† 1) Memory-Silver is included in all development systems.

NON-VOLATILE MEMORY

CMOS PROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	P	S	T
WS57C191B	2K x 8	16K CMOS PROM	35-55	•	•		•		
WS57C291B	2K x 8	16K CMOS PROM	35-55					•	•
WS57C45	2K x 8	16K CMOS Reg. PROM	25-35					•	•
WS57C43B	4K x 8	32K CMOS PROM	35-70	•	•			•	•
WS57C49B	8K x 8	64K CMOS PROM	35-70	•	•			•	•
WS57C49C	8K x 8	64K CMOS PROM	35-70	•	•			•	•
WS57C51C	16K x 8	128K CMOS PROM	35-70	•	•	•			•
WS57C71C	32K x 8	256K CMOS PROM	45-70	•	•	•			•

CMOS PROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	F	H	K	T	Z
WS57C191B	2K x 8	16K CMOS PROM	45-55	•	•	•	•				•
WS57C291B	2K x 8	16K CMOS PROM	45-55	•					•	•	
WS57C45	2K x 8	16K CMOS Reg. PROM	35-45	•	•		•	•	•	•	
WS57C43B	4K x 8	32K CMOS PROM	45-70		•					•	
WS57C49B	8K x 8	64K CMOS PROM	45-70	•	•	•	•			•	
WS57C49C	8K x 8	64K CMOS PROM	45-70	•	•	•	•			•	
WS57C51C	16K x 8	128K CMOS PROM	45-70		•	•				•	
WS57C71C	32K x 8	256K CMOS PROM	55-70		•	•				•	

NON-VOLATILE MEMORY (Cont.)

HIGH-SPEED CMOS EPROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L	T
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	55-70	•	•		
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	55-70	•			
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	35-45	•	•	•	
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	45-70	•	•	•	•

HIGH-SPEED CMOS EPROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	T	L
WS57C64F	8K x 8	High-Speed 64K CMOS EPROM	70	•	•	•		
WS27C64F	8K x 8	Low-Power 64K CMOS EPROM	90	•	•	•		
WS57C128F	16K x 8	High-Speed 128K CMOS EPROM	70	•	•	•		
WS57C128FB	16K x 8	High-Speed 128K CMOS EPROM	45-55		•	•		
WS27C128F	16K x 8	Low-Power 128K CMOS EPROM	90	•	•	•		
WS57C256F	32K x 8	High-Speed 256K CMOS EPROM	55-70	•	•	•	•	
WS27C256F	32K x 8	Low-Power 256K CMOS EPROM	90	•	•	•		•

CMOS EPROMs – COMMERCIAL

Part No.	Architecture	Description	Speed (ns)	Package Selection D	J	L
WS27C010L	128K x 8	Low-Power 1 Meg CMOS EPROM	120-150	•	•	•
WS27C210L	64K x 16	Low-Power 1 Meg CMOS EPROM	100-200	•	•	•

CMOS EPROMs – MILITARY

Part No.	Architecture	Description	Speed (ns)	DESC SMD	Package Selection C	D	L	T
WS27C256L	32K x 8	Low-Power 256K CMOS EPROM	120-250	•	•	•		•
WS27C512L	64K x 8	Low-Power 512K CMOS EPROM	120-200	•	•	•		•
WS27C010L	128K x 8	Low-Power 1 Meg CMOS EPROM	150-200	•	•	•	•	
WS27C210L	64K x 16	Low-Power 1 Meg CMOS EPROM	150-200		•	•	•	

PRODUCT SELECTOR GUIDE

CMOS BIT SLICE AND LOGIC

Part No.	Description	Speed		Package Selection							
		Comm'l	Military	B	G	J	K	L	P	S	Y
WS5901	4-Bit CMOS Bit Slice Processor	32,43 MHz	32,43MHz						•		•
WS59016	16-Bit CMOS Bit Slice Processor	15 MHz	12.5MHz	•		•		•			
WS59032	32-Bit CMOS Bit Slice Processor	26.4,33 MHz	23.6,29 MHz		•						
WS5910	CMOS Microprogram Controller	20,30 MHz	20,30 MHz						•		•
WS59510	16K x 16 CMOS Multiplier-Accum.	30-50 ns			•	•			•		
WS59520	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59521	CMOS Pipeline Register	Tpd = 22ns	Tpd = 24ns				•			•	
WS59820	CMOS Bi-Directional Register	Tpd = 23ns	Tpd = 25ns		•	•					

WSI PACKAGE DESCRIPTIONS

Package Code	Description	Window	Surface Mount	Plastic/OTP
B/R	Ceramic Sidebrazed Dip	N/Y	N	–
C	Ceramic Leadess Chip Carrier (CLLCC)	Y	Y	–
C/Z	Ceramic Leadless Chip Carrier (CLLCC)	Y/N	Y	–
D/Y	0.600" Ceramic Dip	Y/N	N	–
F/H	Ceramic Flatpack	Y/N	Y	–
J	Plastic Leaded Chip Carrier (PLDCC)	N	Y	Y
L/N	Ceramic Leaded Chip Carrier (CLDCC)	Y/N	Y	–
P	Plastic Dip	N	N	Y
Q	Plastic Quad Flat Pack (PQFP)	N	Y	Y
S	0.300" Plastic Dip	N	N	Y
T/K	0.300" Ceramic Dip	Y/N	N	–
X/G	Ceramic Pin Grid Array (CPGA)	Y/N	N	–

47280 Kato Road
Fremont, California 94538-7333
Tel: 510-656-5400 Fax: 510-657-5916
800-TEAM-WSI (800-832-6974)
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Ordering Information
High-Performance CMOS Products

PSD3XX **–35** **D** **I** **B**

Basic Part Number

Manufacturing Process:

(Blank) = WSI Standard Manufacturing Flow

B = MIL-STD-883C Manufacturing Flow

Operating Temperature Range:

(Blank) = Commercial: 0° to +70°C
V_{CC}: +5V ± 5%

I = Industrial: –40° to +85°C
V_{CC}: +5V ± 10%

M = Military: –55° to +125°C
V_{CC}: +5V ± 10%

Package:

		Window
A	= PPGA Plastic Pin Grid Array	No
B	= 0.900″ Size Brazed Ceramic DIP	No
C	= CLLCC Ceramic Leadless Chip Carrier	Yes*
D	= 0.600″ CERDIP	Yes
F	= Ceramic Flatpack	Yes*
G	= CPGA Ceramic Pin Grid Array	No
H	= Ceramic Flatpack	No*
J	= Plastic Leaded Chip Carrier	No*
K	= 0.300″ Thin CERDIP	No
L	= CLDCC Ceramic Leaded Chip Carrier	Yes*
N	= CLDCC Ceramic Leaded Chip Carrier	No*
P	= 0.600″ Plastic DIP	No
Q	= Plastic Quad Flatpack	No*
R	= Ceramic Side Brazed	Yes
S	= 0.300″ Thin Plastic DIP	No
T	= 0.300″ Thin CERDIP	Yes
W	= Waffle Packed Dice	—
X	= Ceramic Pin Grid Array	Yes
Y	= 0.600″ CERDIP	No
Z	= CLLCC	No

Speed:

– 120 = 120 ns
– 150 = 150 ns
– 200 = 200 ns
Etc.

*Surface Mount

Section Index

Programmable Peripheral

PSD301

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A and PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Address Decoding up to 1 MB
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$ or R/$\overline{W}$/E
  - — BHE/pin for byte select in 16-bit mode
  - — PSEN/pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Configurable as 32K x 8 or as 16K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8 or 2K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD301 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD301 on an IBM PC
- ❑ Pin Compatible with the PSD3XX Family

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/8098, 80186/88, 80196/98
- ❑ **TI:** TMS320C14
- ❑ **Signetics:** SC80C451, SC80552
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000, HPC63400

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD301 is a member of the rapidly growing family of PSD devices. The PSD301 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 8096, 16000, etc.) and the PSD301 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD301 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD301 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K bits of high speed EPROM, 16K bits of high speed SRAM, input latches, and output ports. The PSD301 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD301 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.

WSI's PSD301 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 256K bit EPROM, and 16K bit SRAM on a single chip. The PSD301 does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD301's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD301 in a 16-bit configuration. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD301 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD301 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (as 4K x 8 or as 2K x 16) and SRAM (as 2K x 8 or as 1K x 16) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

Figure 1. PSD301 Architecture

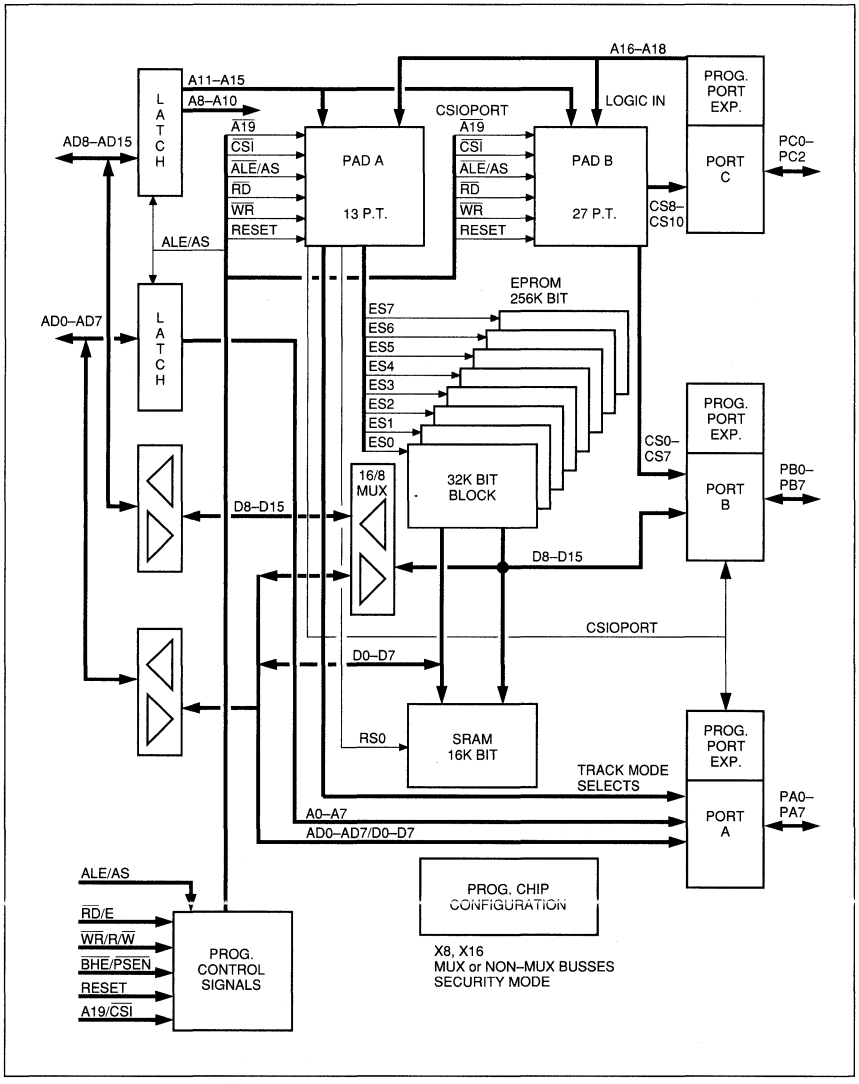
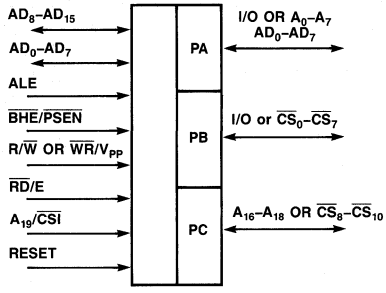
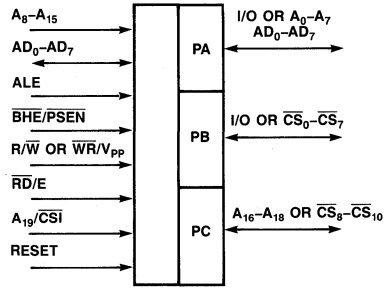


Figure 2. PSD301 Port Configurations

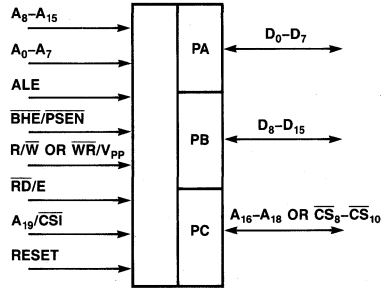
Figure 2 shows the PSD301's I/O port configurations.



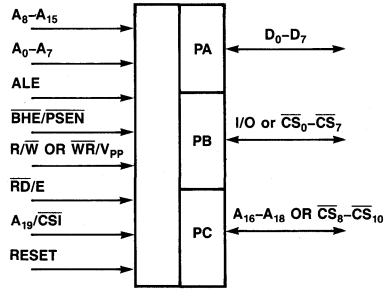
PSD301 configured for multiplexed 16-bit address/data bus



PSD301 configured for multiplexed 8-bit address/data bus.



PSD301 configured for non-multiplexed 16-bit address/data bus.



PSD301 configured for non-multiplexed 8-bit address/data bus.

Legend:

AD_0–AD_7 = addresses A_0–A_7 multiplexed with data lines D_0–D_7.
AD_8–AD_{15} = addresses A_8–A_{15} multiplexed with data lines D_8–D_{15}.

Table 1. PSD301 Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated when $\overline{RD}$ is low (CRRWR = 0), or when E and R/$\overline{W}$ are high (CRRWR = 1). If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, a high-order byte is read from, or written into the PSD301, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{WR}/V_{PP}$ or R/$\overline{W}/V_{PP}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1). When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10 and 11 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD301 configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose PAD input signal.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 3. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD301 Pin Descriptions (Cont.)

Name	Type	Description
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRDAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD; $\overline{CS4}$–$\overline{CS7}$ then are each a function of up to two product terms. When the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the most significant byte of the data bus (D8–D15). See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD input or output. When configured as an input (CPCF = 0), the bits can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PAD (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input byte.
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input byte.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD301's four operating modes allow it to interface directly to 8- and 16-bit microcontrollers and microprocessors with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus

Multiplexed 8-Bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-Bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-Bit Data Bus

This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Non-Multiplexed 16-Bit Address/Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Table 2. PSD301 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-Bit Data Bus		
Port A	I/O and/or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus lines
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–CS7
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order address bus byte	High-order address bus byte
16-Bit Data Bus		
Port A	I/O and/or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O and/or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Programmable Address Decoder (PAD)

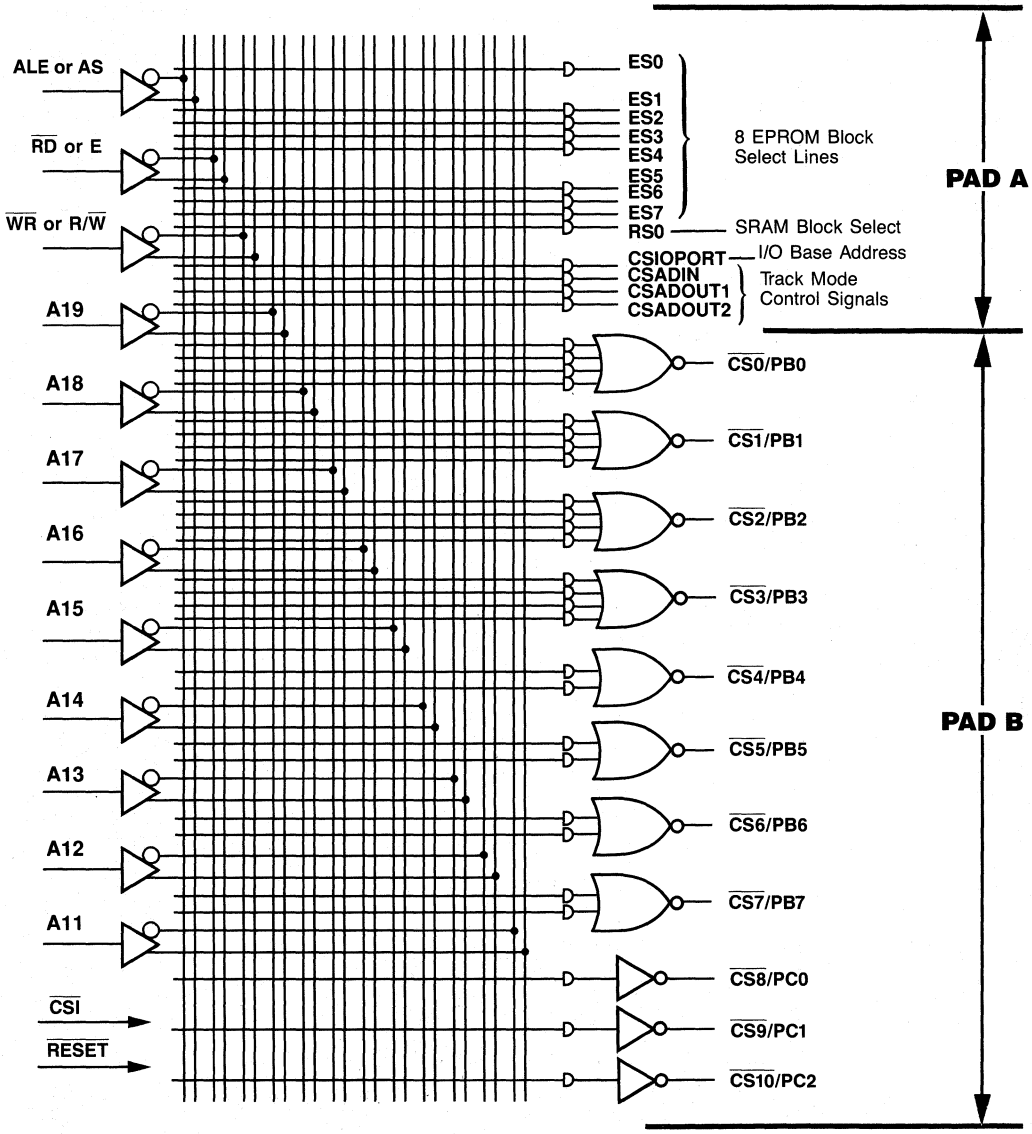
The PSD301 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use UV CMOS EPROM technology and can be programmed and erased by the user.

Table 3. PSD301 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Figure 3. PSD301 PAD Description



Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD301 MAPLE software to set the bits.

Table 4. PSD301 Non-Volatile Configuration Bits

Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits.
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/W status.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.[8]
CSECURITY	Set the security on or off.
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CATD	Configure pins A16–A19 as PAD logic inputs or high-order address inputs.

NOTE: 8. For functional and value descriptions, refer to table 5.

Table 5. PSD301 Configuration Bits (46 total bits)

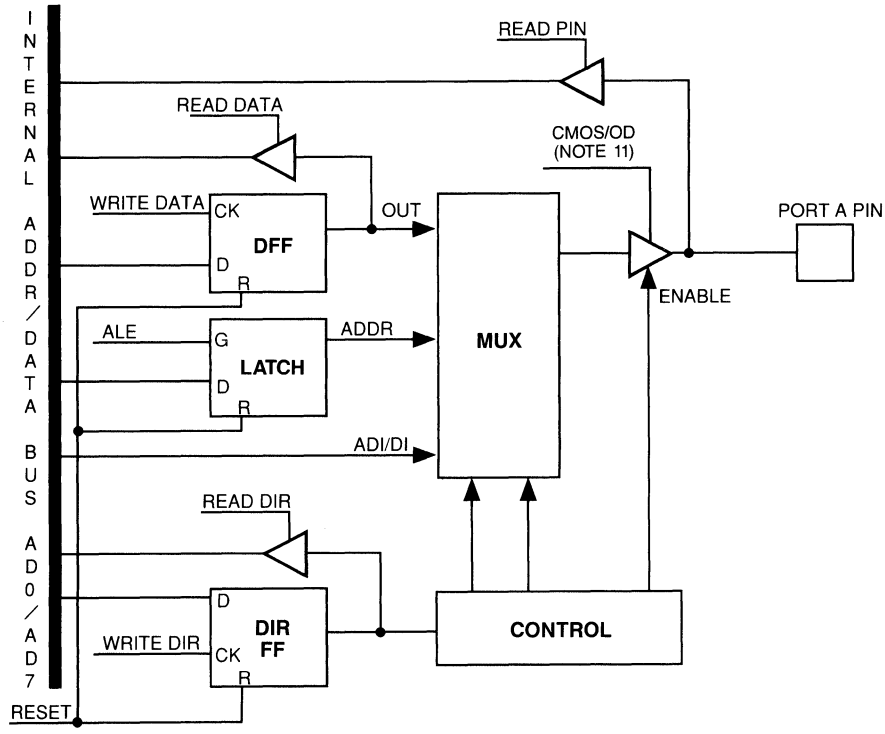
Configuration Bits	No. of Bits	Description
CDATA	1	8-bit or 16-bit data bus width CDATA = 0, 8-bit data bus CDATA = 1, 16 bit data bus
CADDRDAT	1	Address/data multiplexed or non-multiplexed (separate buses) CADDRDAT = 0, non-multiplexed address/data bus CADDRDAT = 1, multiplexed address/data bus
CRRWR	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down mode CA19/$\overline{CSI}$ = 1, A19 input to PAD
CALE	1	Active high or active low CALE = 0, active high CALE = 1, active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or separate memory space for EPROM and SRAM $\overline{COMB}$/SEP = 0, combined $\overline{COMB}$/SEP = 1, separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = Ai ($0 \leqslant i \leqslant 7$)
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CPBF	8	Port B I/Os or $\overline{CS0}$–$\overline{CS7}$ CPBF = 0, Port B Pin = $\overline{CSi}$ ($0 \leqslant i \leqslant 7$) CPBF = 1, Port B Pin = I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C Pin = Ai ($16 \leqslant i \leqslant 18$) CPCF = 1, Port C Pin = $\overline{CSi}$ ($8 \leqslant i \leqslant 10$)
CPACOD	8	Port A CMOS or open-drain outputs CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBCOD	8	Port B CMOS or open-drain outputs CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CADDHLT	1	A16–A19 latched or latch transparent CADDHLT = 0, address latch transparent CADDHLT = 1, address latched (ALE dependent)
CATD	1	A16–A19 used as address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CSECURITY	1	Security on or off CSECURITY = 0, no security CSECURITY = 1, secured part (cannot be copied)

NOTES: 9. WSI's MAPLE software will guide the user to the proper configuration choice.
10. In an unprogrammed or erased part, all configuration bits are 0.

Port Functions

The PSD301 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 11. CMOS/OD determines whether the output is open drain or CMOS.

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register.

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD301 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

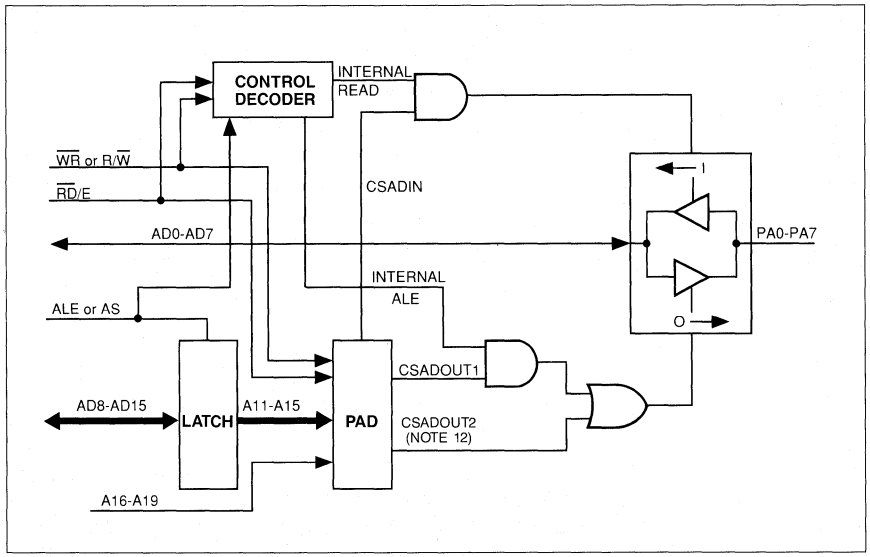
Port Functions (Cont.)

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figures 22 and 23). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD301 location, data is presented on Port A pins. When writing to an internal PSD301 location, data present on Port A pins is written to that location.

Figure 5. Port A Track Mode



NOTE: 12. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register.

Port Functions (Cont.)

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from the PAD. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms. Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode

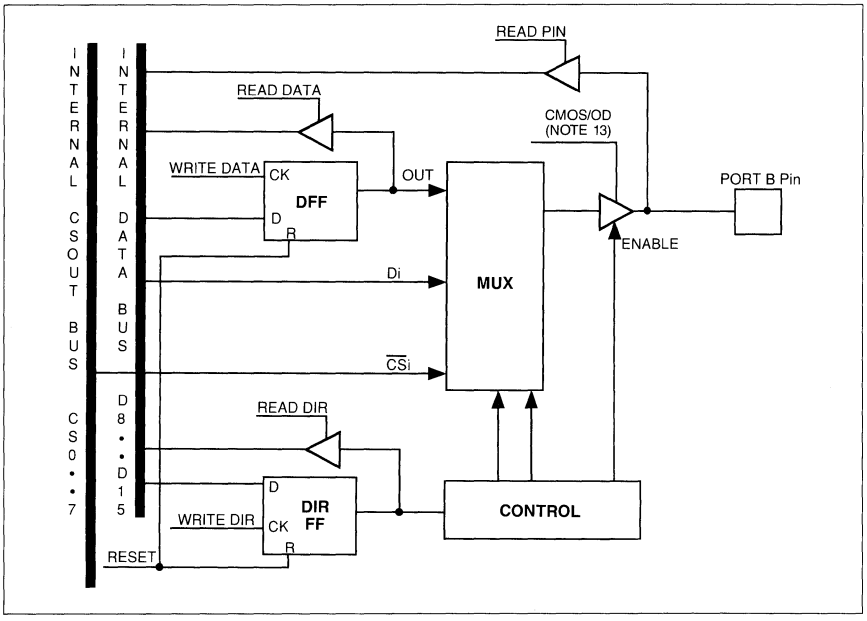
In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal PSD301 high-order data bus byte location, the data is presented on Port B pins. When writing to an internal PSD301 high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

2

Figure 6. Port B Pin Structure



NOTE: 13. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+2 (accessible during read operation only)
Direction Register of Port A	+4
Data Register of Port A	+6
Pin Register of Port B	+3 (accessible during read operation only)
Direction Register of Port B	+5
Data Register of Port B	+7

Table 7. I/O Port Addresses in a 16-bit Data Bus Mode

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+2 (accessible during read operation only)
Direction Register of Ports B and A	+4
Data Register of Ports B and A	+6

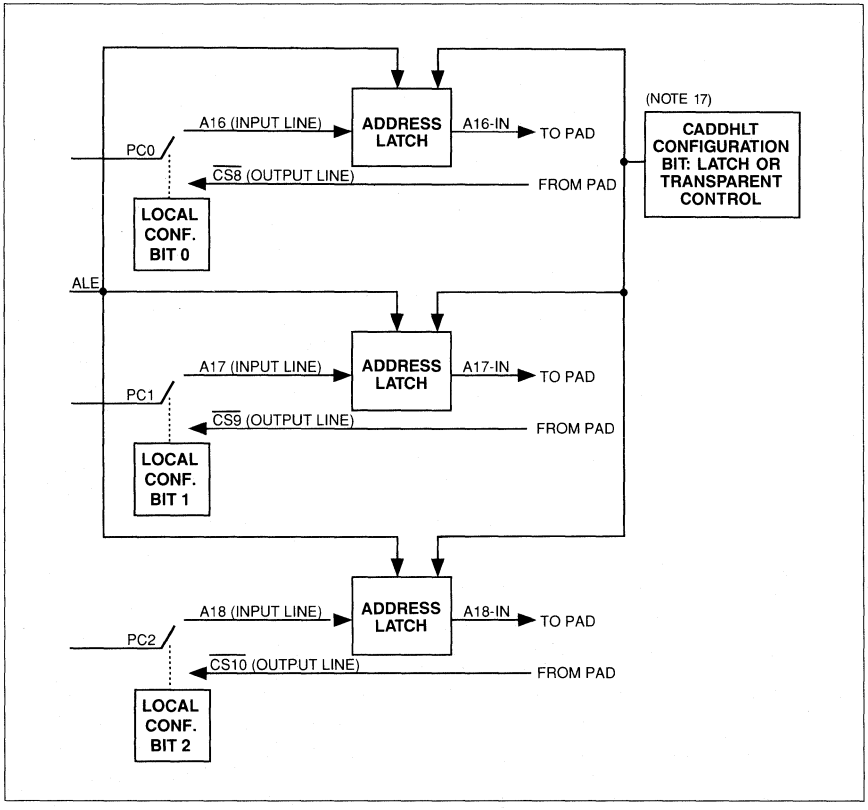
NOTES: 14. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
15. When accessing words, the high-order byte is connected to Port B, and the low-order byte is connected to Port A.
16. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input or output from the PAD. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other logic inputs to the PAD. For example, A8–A10 can also be connected to those pins, reducing the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. Port C address latches can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

Figure 7. Port C Structure



NOTE: 17. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

A16-A19 As Inputs

If one or more of the pins PC0, PC1, PC2 and CSI/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD301 at all times (CADDHLT = 0, transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

EPROM

The PSD301 has 256K bits of EPROM. Depending on the configuration of the data bus, the EPROM can be organized as 32K x 8 (8-bit data bus) or as 16K x 16 (16-bit data bus). The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 4K x 8 (8-bit data bus) or as 2K x 16 (16-bit data bus).

2

SRAM

The PSD301 has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Control Signals

The PSD301 control signals are WR/V_{PP} or R/W, RD/E, ALE, BHE/PSEN, Reset, and A19/CSI. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

WR/V_{PP} or R/W

In operational mode, this signal can be configured as WR or R/W. As WR, all write operations to the PSD301 are activated by an active low signal on this pin. As R/W, the pin works with the E strobe of the RD/E pin. When R/W is high, an active high signal on the RD/E pin performs a read operation. When R/W is low, an active high signal on the RD/E pin performs a write operation.

RD/E

In operational mode, this signal can be configured as RD or E. As RD, all read operations to the PSD301 are activated by an active low signal on this pin. As E, the pin works with the R/W strobe of the WR/V_{PP} or R/W pin. When R/W is high, an active high signal on the RD/E pin performs a read operation. When R/W is low, an active high signal on the RD/E pin performs a write operation.

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, and Port C address latches to be transparent. The falling edge of ALE latches the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE latches the appropriate information into the latches. ALE is active only in the multiplexed modes.

BHE/PSEN

This pin's function depends on the PSD301 data bus width. If it is 8, the pin is PSEN; if it is 16, the pin is BHE. In 8-bit mode, the PSEN function lets the user work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the PSEN pin causes the EPROM to be read. The SRAM and I/O ports read operation are done by RD low (CRRWR = 0), or by E and R/W high (CRRWR = 1).

Control Signals (Cont.)

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD301's $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1). See Figures 8 and 9.

Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA = 0, CADDRDAT = 0	8-bit data, non-multiplexed	Transparent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE dependent
AD0/A0–AD7/A7	CADDRDAT = 0	Non-multiplexed modes	Transparent
	CADDRDAT = 1	Multiplexed modes	ALE dependent
$\overline{BHE}$/$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, $\overline{BHE}$ is active	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, $\overline{BHE}$ is active	ALE dependent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE dependent

Figure 8. Combined Address Space

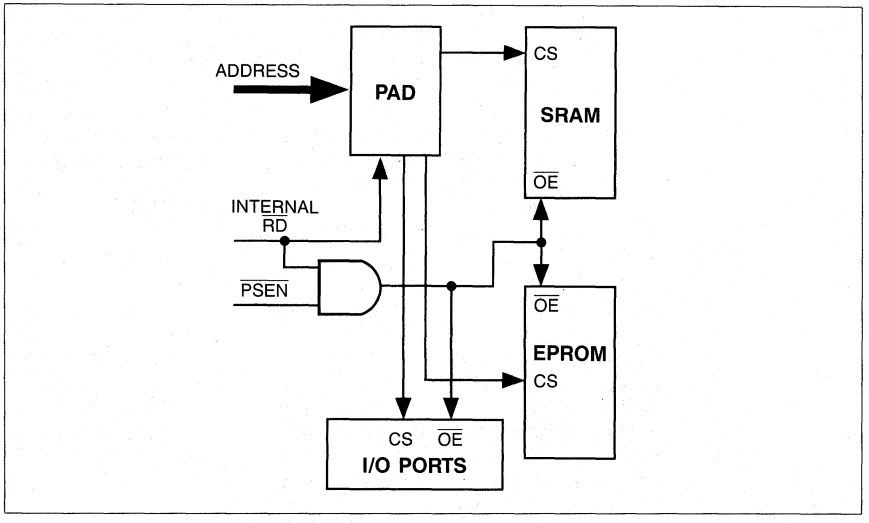
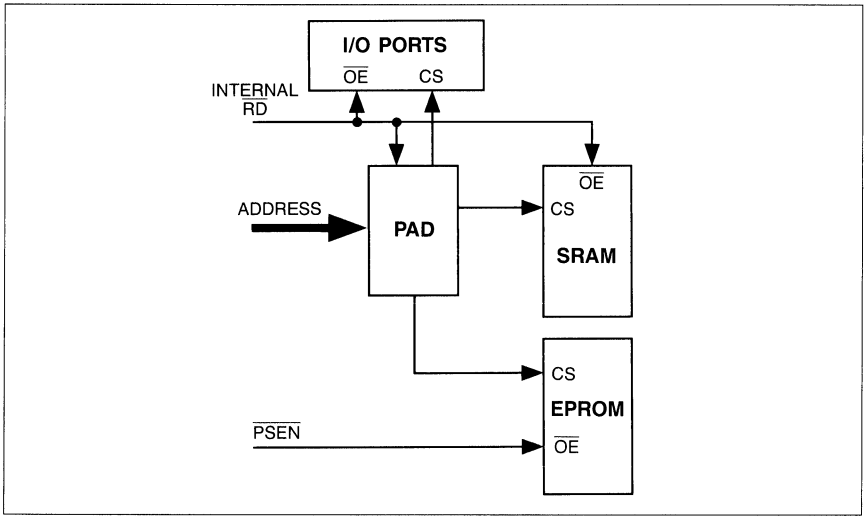


Figure 9. 8031-Type Separate Code and Data Address Spaces



In BHE mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

BHE	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address (AD8–AD15)
1	0	Lower Byte From/To Even Address (AD0–AD7)
1	1	None

RESET

This is an asynchronous input pin that clears and initializes the PSD301. Reset polarity is programmable (active low or active high). Whenever the PSD301 reset input is driven active for at least 100 ns, the chip is reset. The PSD301 must be reset before it can be used. Tables 10 and 11 indicate the state of the part during and after reset.

Table 10. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7 (Port A)	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O CS7–CS0 CMOS outputs CS7–CS0 open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 CS8–CS10 CMOS outputs	Input High

Table 11. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1^{18}
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0^{18}
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 18. All PAD outputs are in a non-active state.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD301 states during the power-down mode, see Tables 12 and 13.

Table 12. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A	n/a	All unchanged
Direction register A	n/a	
Data register B	n/a	
Direction register B	n/a	

In A19 mode, the pin is an additional input to the PAD. It can be used as a high-order address line or as a general-purpose logic input. A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Security Mode

Security Mode in the PSD301 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD301 contents cannot be copied on a programmer.

System Applications

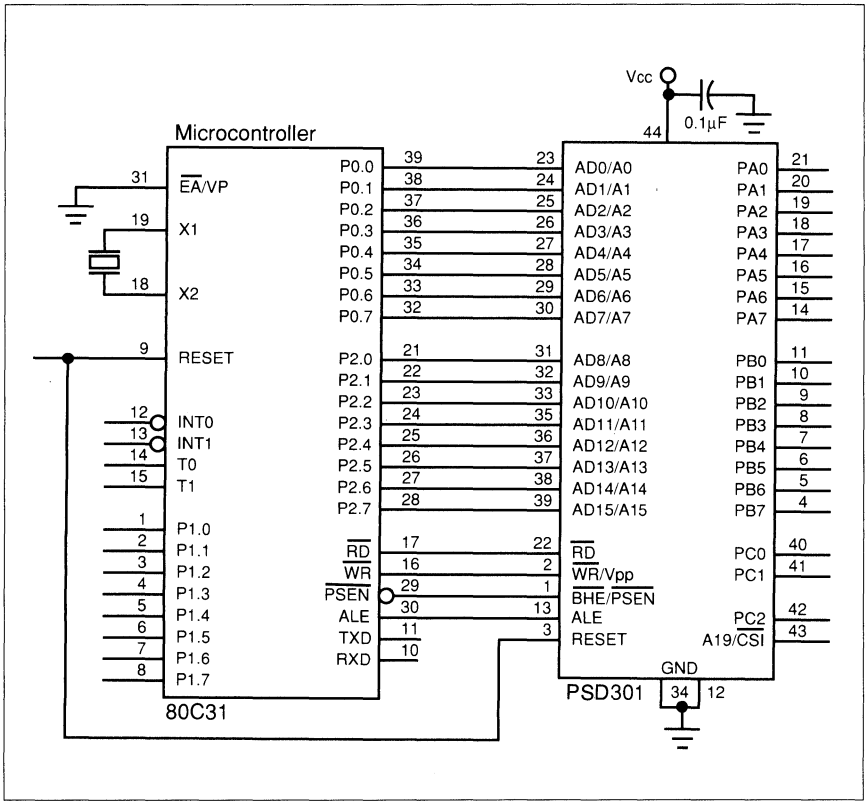
In Figure 10, the PSD301 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

The configuration bits for Figure 10 are:

CRESET	1
CALE	0
CDATA	0
CADDRDAT	1
COMB/SEP	0 or 1 (both valid)
CRRWR	0

All other configuration bits may vary according to the application requirements.

Figure 10. PSD301 Interface with Intel's 80C31



System Applications (Cont.)

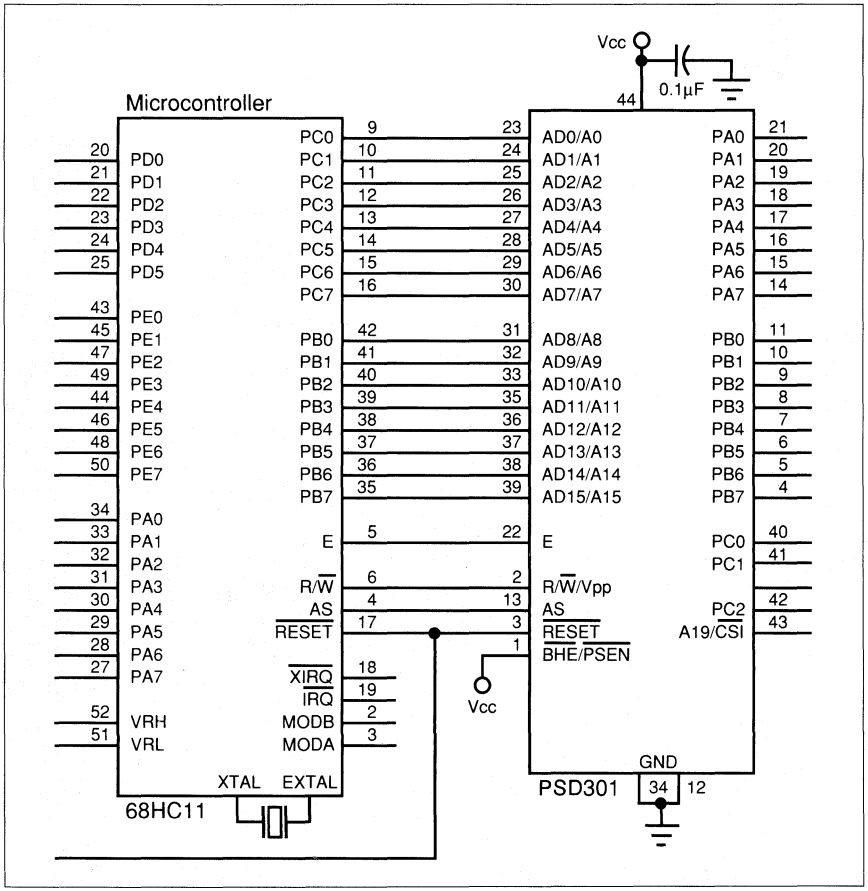
In Figure 11, the PSD301 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

The configuration bits for Figure 11 are:

CRESET	0
CALE	0
CDATA	0
CADDRDAT	1
COMB/SEP	0
CRRWR	1

All other configuration bits may vary according to the application requirements.

Figure 11. PSD301 Interface with Motorola's 68HC11



In Figure 12, the PSD301 is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD301 is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part

System Applications (Cont.)

in the PAD equations implementation.

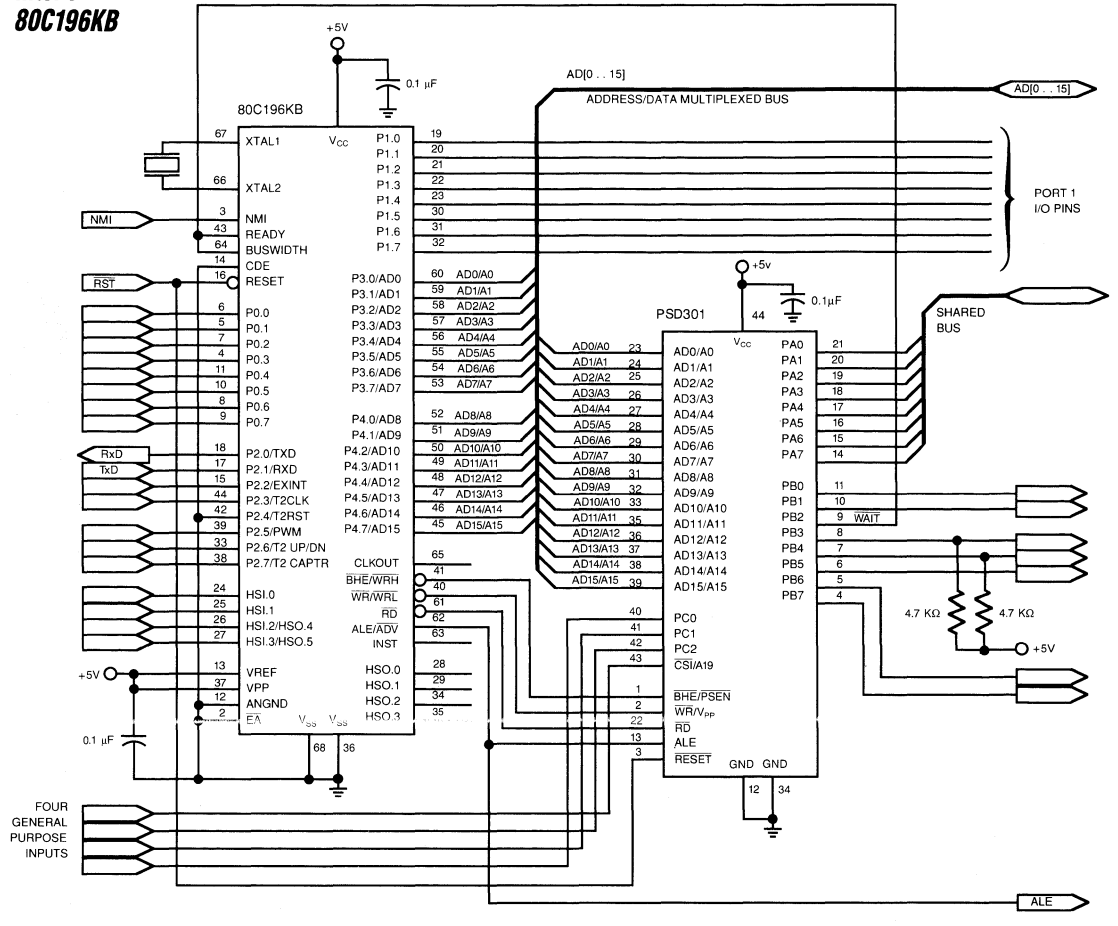
Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

The configuration bits for Figure 12 are:

CRESET	0
CALE	0
CDATA	1
CADDRDAT	1
CPAF1	Don't care
CPAF2	1
CA19/$\overline{CSI}$	1
$\overline{CRRWR}$	0
$\overline{COMB}$/SEP	0
CADDHLT	0
CSECURITY	Don't care
CPCF2, CPCF1, CPCF0	0, 0, 0
CPACOD7–CPACOD0	00H
CPBF7–CPBF0	00H
CPBCOD7–CPBCOD0	18H

2

Figure 12. PSD301 Interface with Intel's 80C196KB



Absolute Maximum Ratings[19]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CERDIP	– 65	+ 150	°C
		PLASTIC	– 65	+ 125	
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 19. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0°C to + 70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40°C to + 85°C	+ 5 V		± 10%	± 10%
Military	–55°C to + 125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2		V_{CC}	V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 20 and 22)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 21 and 22)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 20 and 23)	Comm'l (Note 24)		16	35	mA
		Comm'l (Note 25)		28	50	
		Ind/Mil (Note 24)		16	45	
		Ind/Mil (Note 25)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 20 and 23)	Comm'l Note 24		47	80	mA
		Comm'l Note 25		59	95	
		Ind/Mil (Note 24)		47	100	
		Ind/Mil (Note 25)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 21 and 23)	Comm'l (Note 24)		36	65	mA
		Comm'l (Note 25)		58	80	
		Ind/Mil (Note 24)		36	80	
		Ind/Mil (Note 25)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 21 and 23)	Comm'l (Note 24)		67	105	mA
		Comm'l (Note 25)		79	120	
		Ind/Mil (Note 24)		67	130	
		Ind/Mil (Note 25)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 20. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
21. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
22. $\overline{CSI}$/A19 is high in a power-down configuration mode.
23. AC power component is 3.5 mA/MHz (power = AC + DC).
24. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
25. Forty-one (41) PAD product terms active.

AC Characteristics

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	5		10		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	140		170		220		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		150		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		35		40		45	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, or $\overline{PSEN}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	20		30		40		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

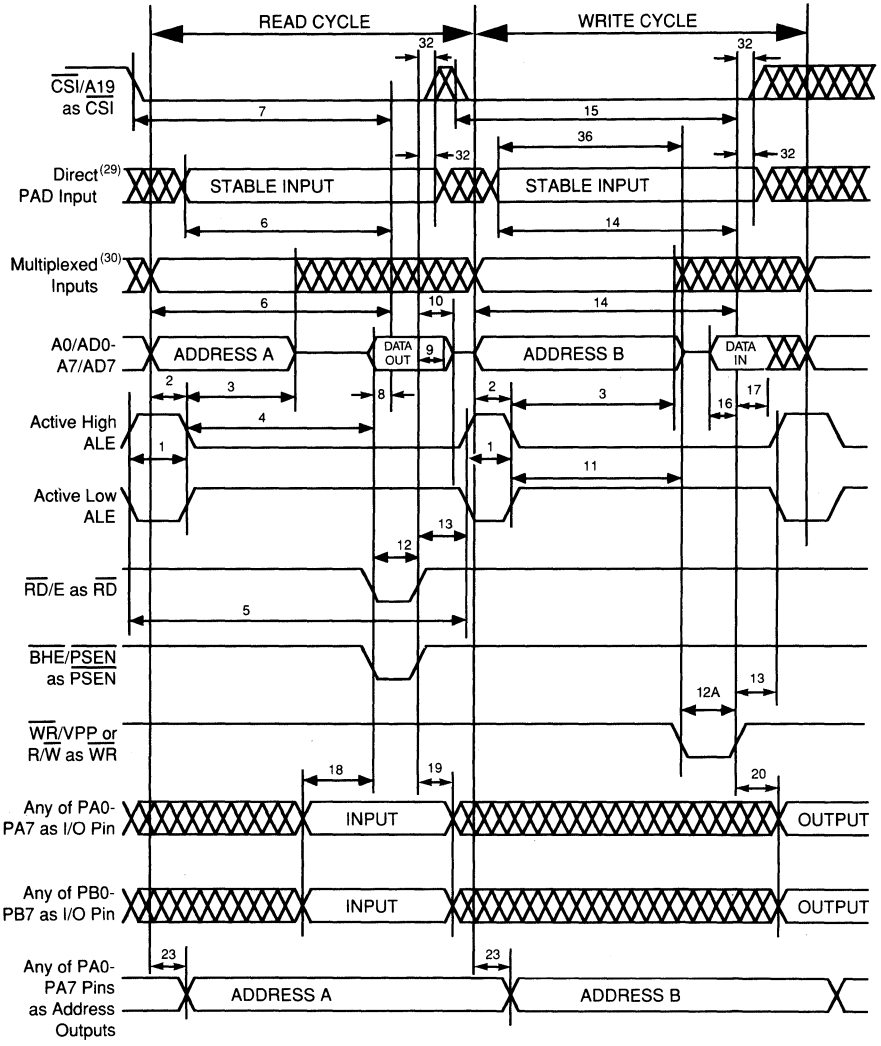
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		210		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi [26] or Control to $\overline{CSOi}$ [27] Valid	6	35	6	35	5	45	
T22	ADi [26] or Control to $\overline{CSOi}$ [27] Invalid	5	35	4	35	4	45	
T23	Track Mode Address Propagation Delay: • CSADOUT1 Already True or:		22		22		28	
	• CSADOUT1 Becomes True During ALE or AS		33		40		50	
T24	Track Mode Address Hold Time	15		15		27		
T25	Track Mode Read Propagation Delay		29		29		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		20		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ [27] Active	9	45	9	45	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ [27] Inactive	9	45	9	45	8	60	
T32	Direct PAD Input [28] Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E High	20		30		40		
T34	E Low to R/$\overline{W}$ Inactive	20		30		40		
T35	AS Inactive to E High	15		20		25		

NOTES: 26. ADi = any address line.

27. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).

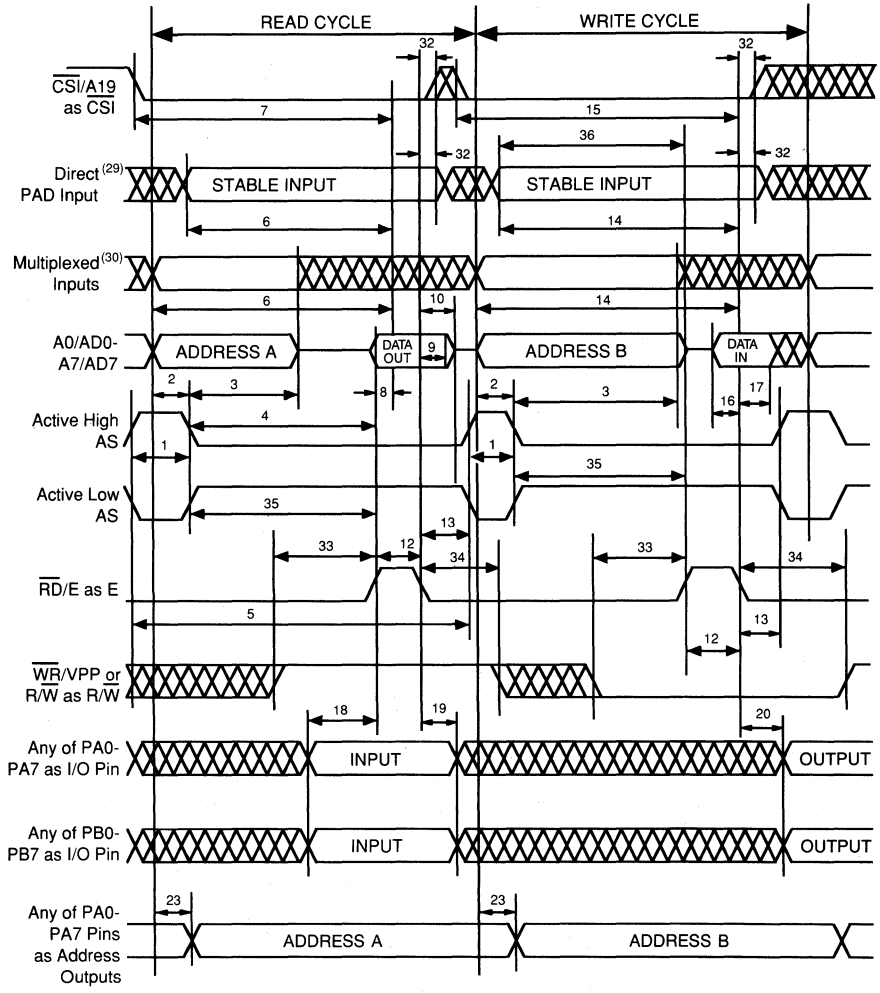
28. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).

Figure 13. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



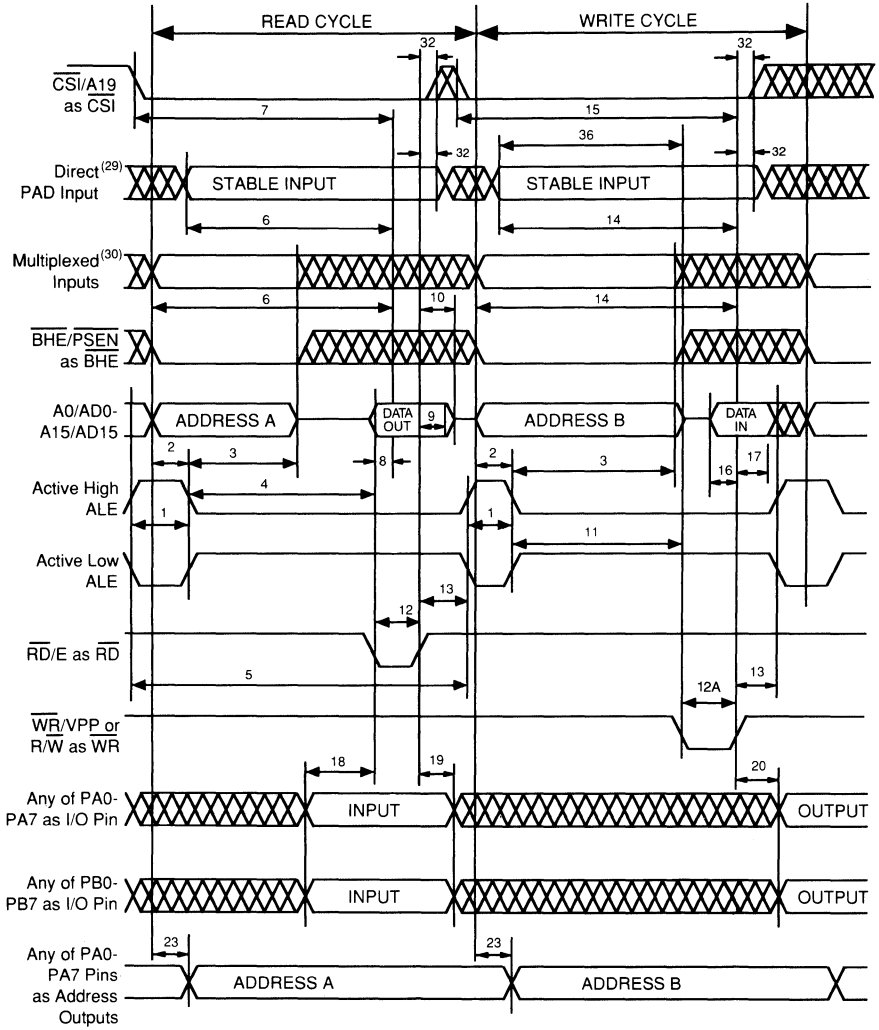
See referenced notes on page 2-36.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



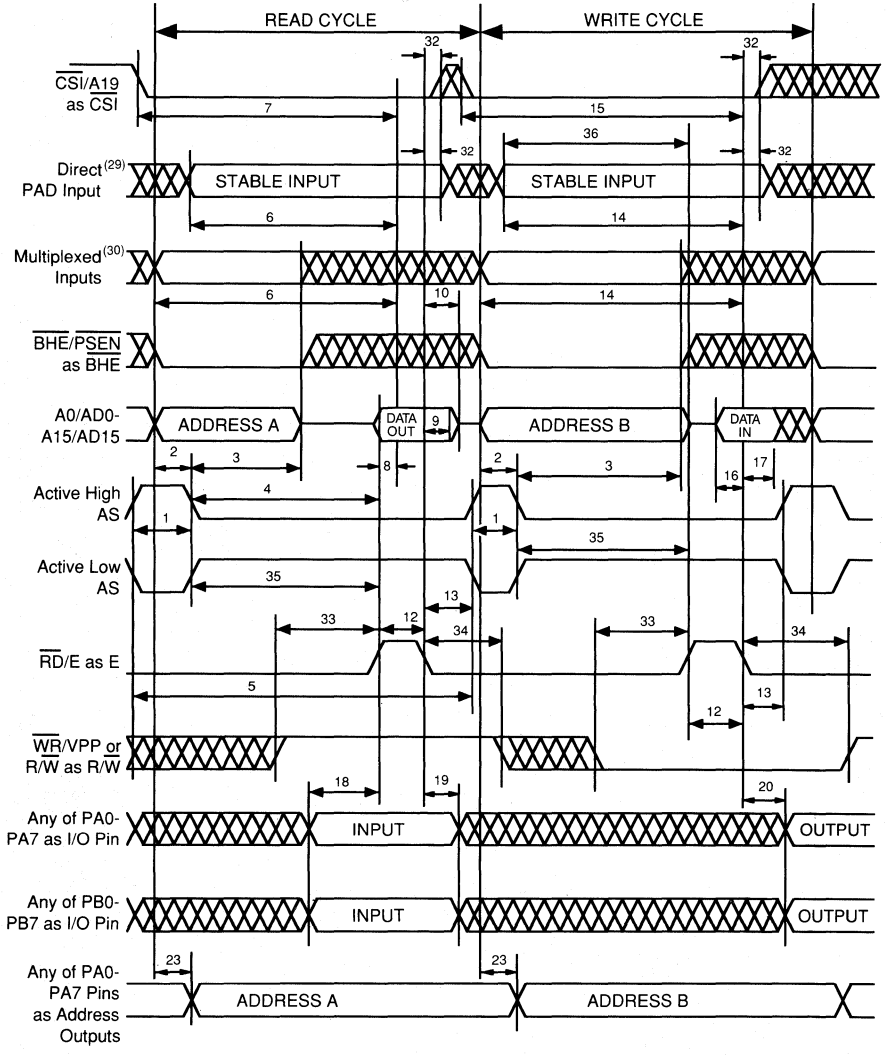
See referenced notes on page 2-36.

Figure 15. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



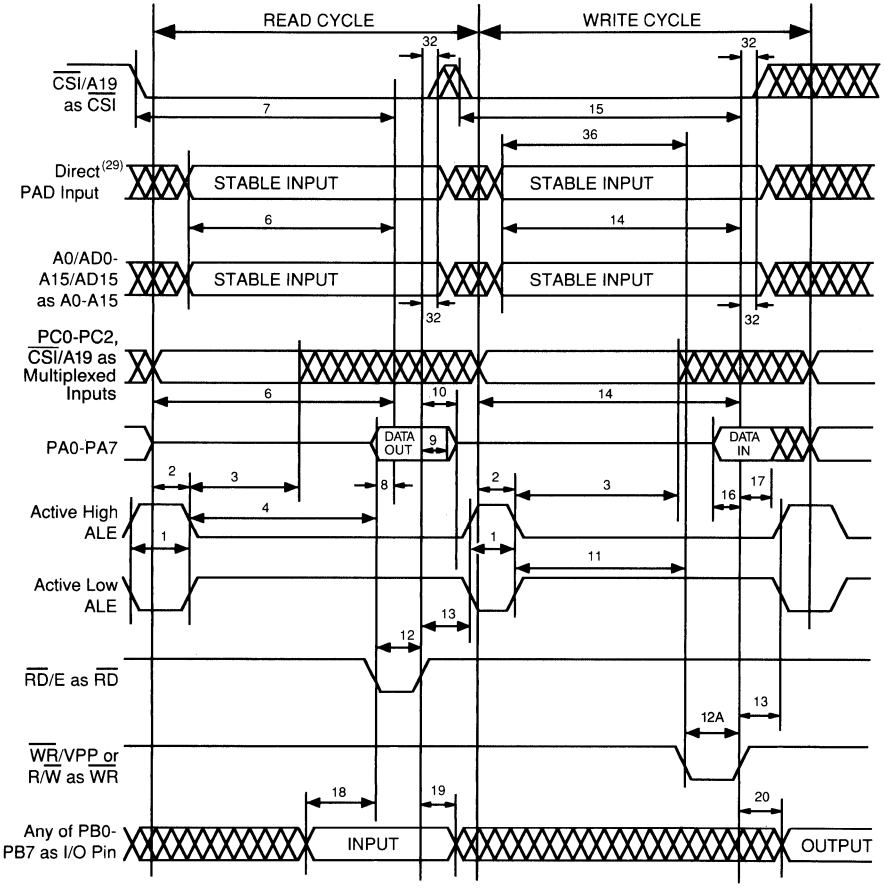
See referenced notes on page 2-36.

Figure 16. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



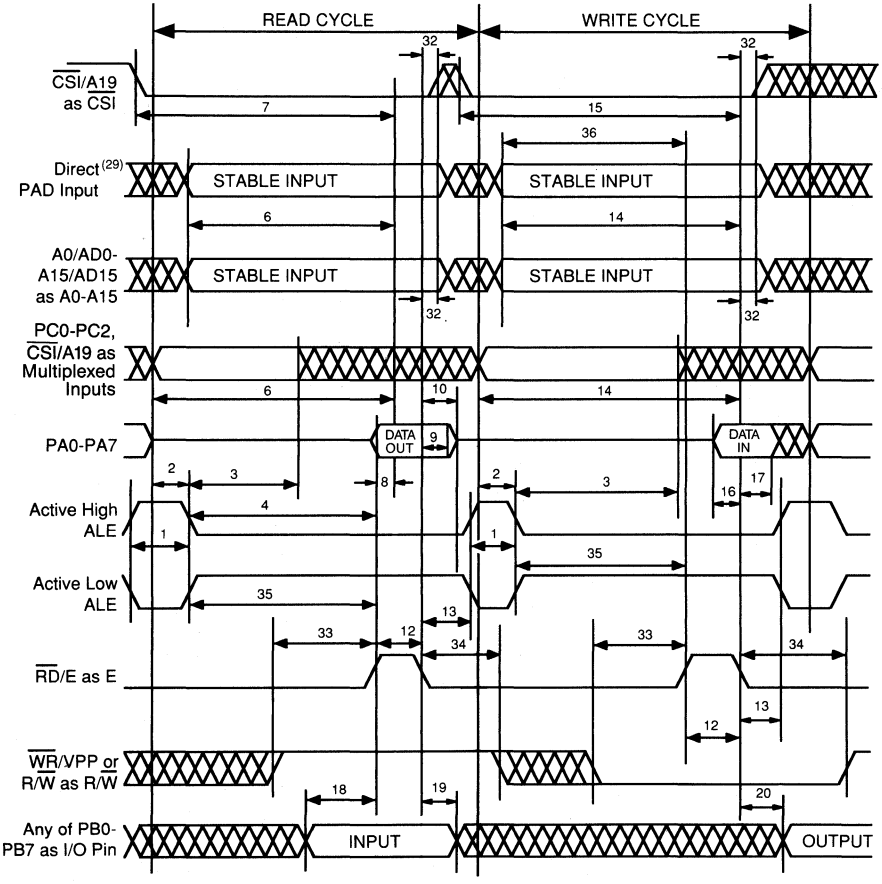
See referenced notes on page 2-36.

Figure 17. Timing of 8-Bit Data, Non-Multiplexed Address/Data Bus, CRRWR = 0



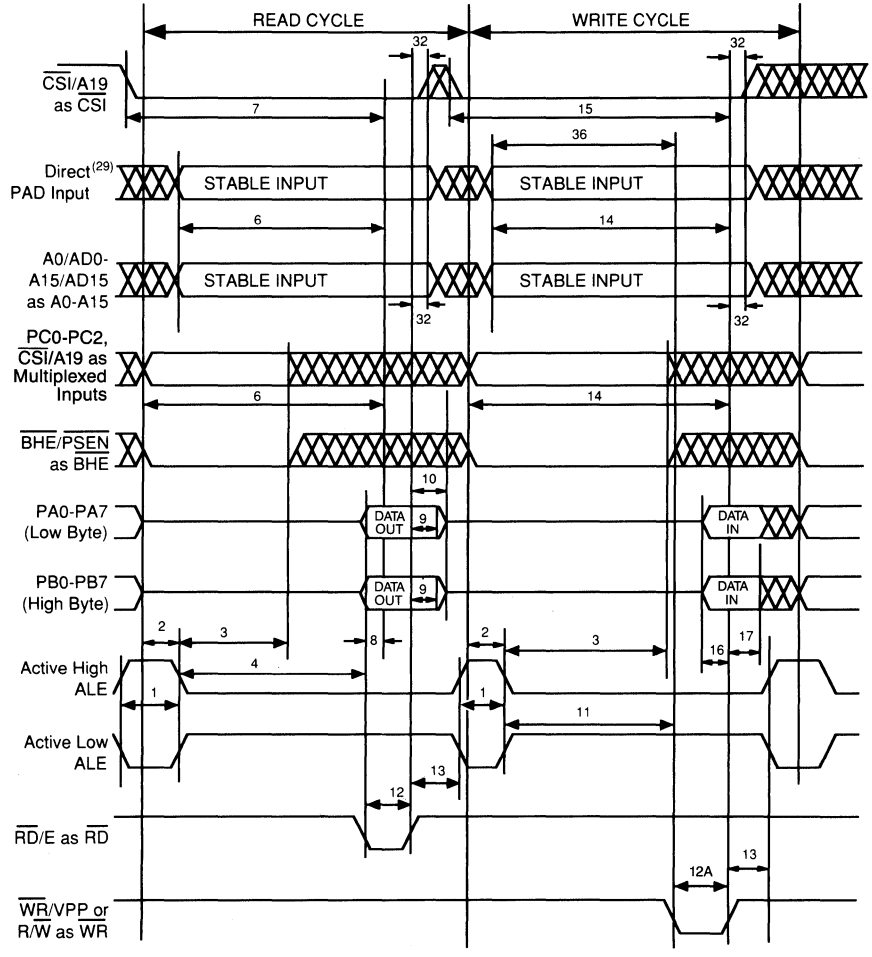
See referenced notes on page 2-36.

Figure 18. Timing of 8-Bit Data, Non-Multiplexed Address/Data Bus, CRRWR = 1



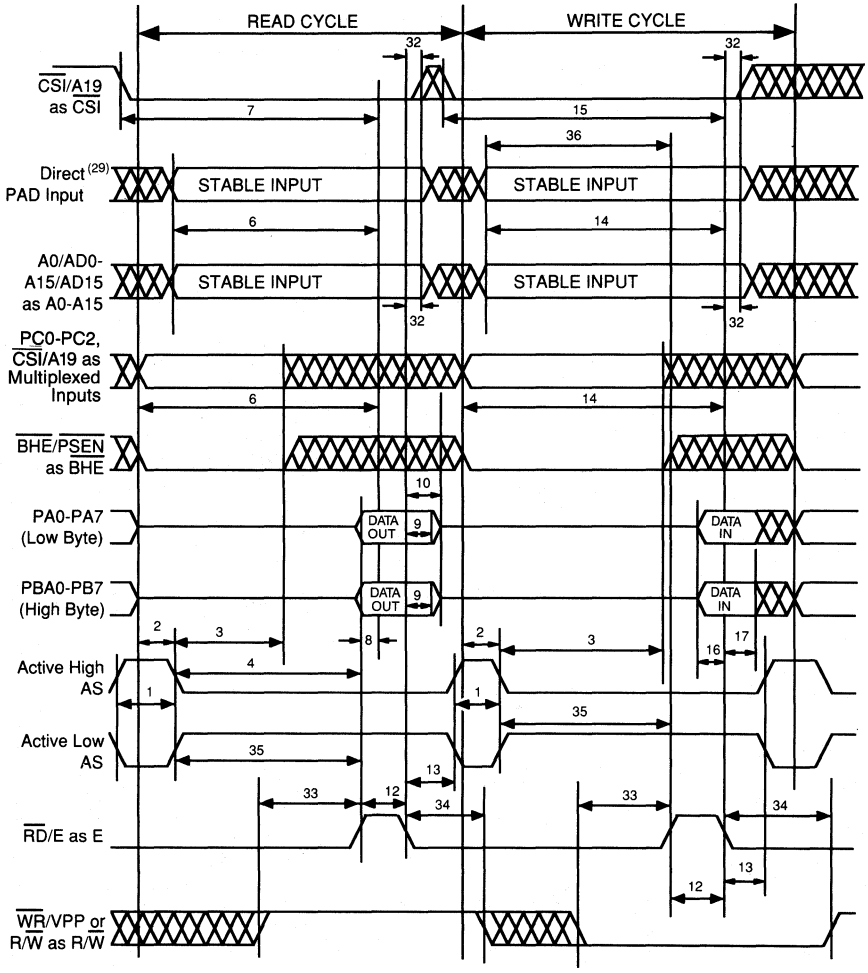
See referenced notes on page 2-36.

Figure 19. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-36.

Figure 20. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-36.

Figure 21. Chip-Select Output Timing

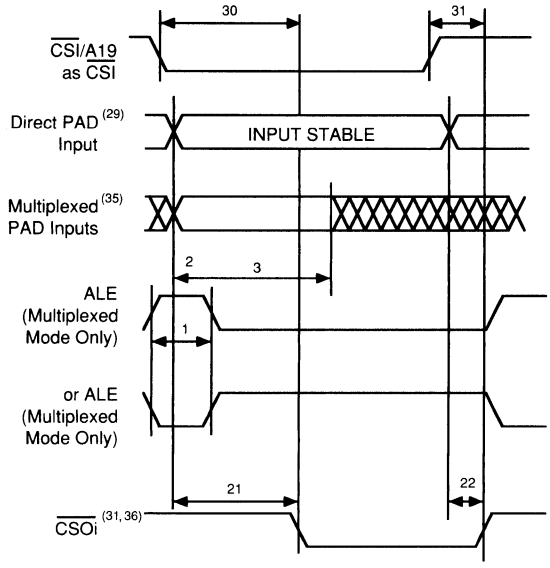
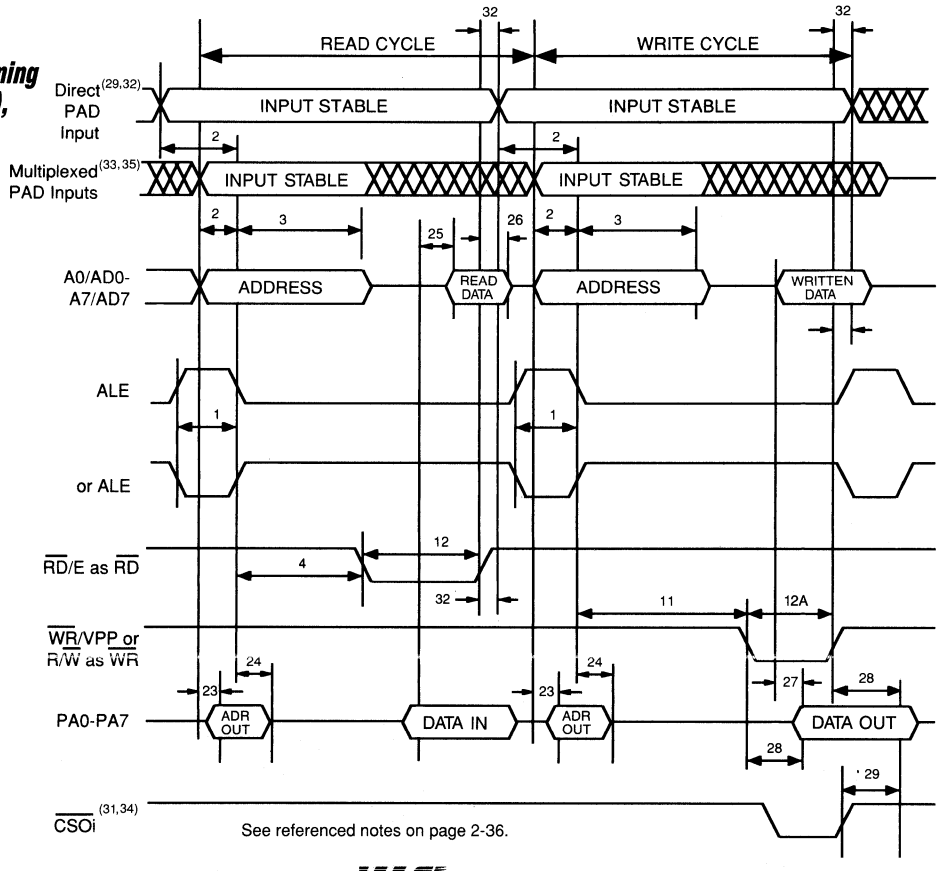
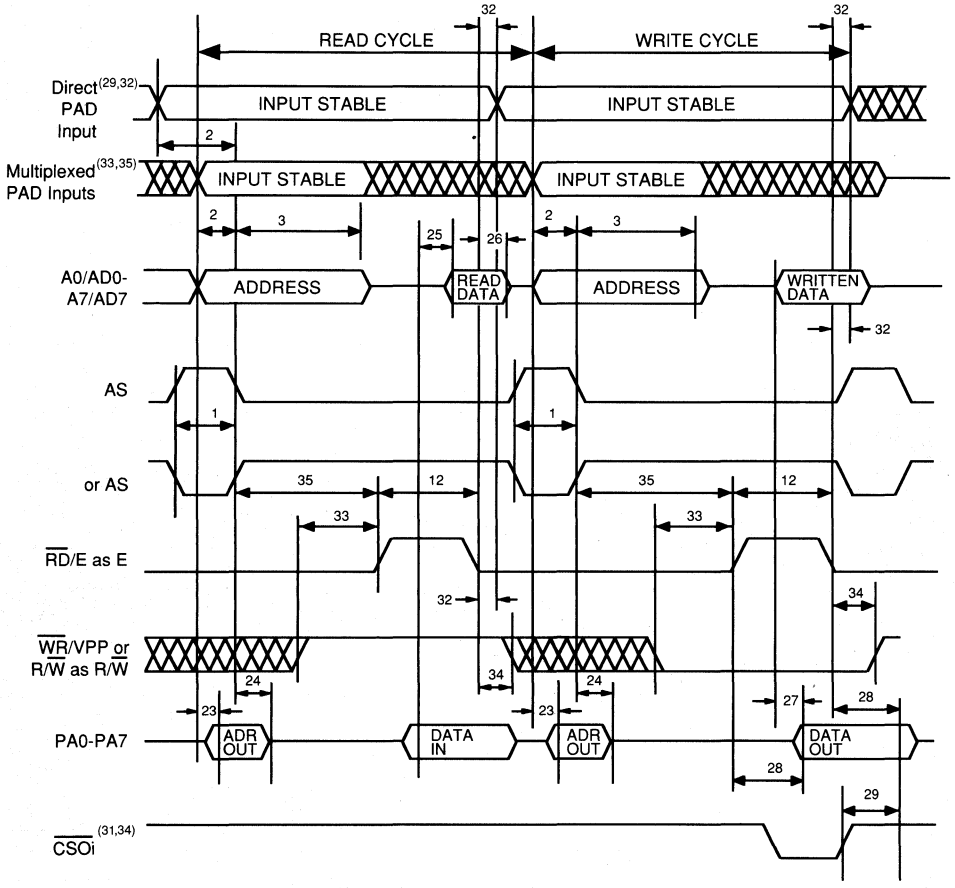


Figure 22. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-36.

Figure 23. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

29. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE and A11/AD11–A15/AD15 in non-multiplexed modes.
30. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
31. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
32. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
33. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
34. The write operation signals are included in the CSOi expression.
35. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.

36 CSOi product terms can include any of the PAD input signals shown in Figure 3, except for reset and CSI.

Table 14. Pin Capacitance[37]

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Conditions	Typical[38]	Max	Units
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	V_{PP} = 0 V	18	25	pF

NOTES: 37. This parameter is only sampled and is not 100% tested.
38. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 24. AC Testing Input/Output Waveform

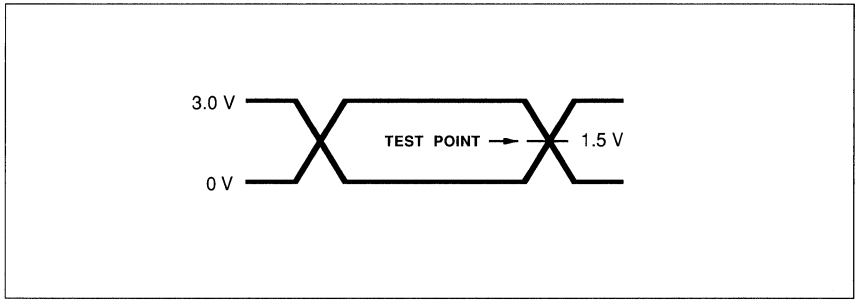
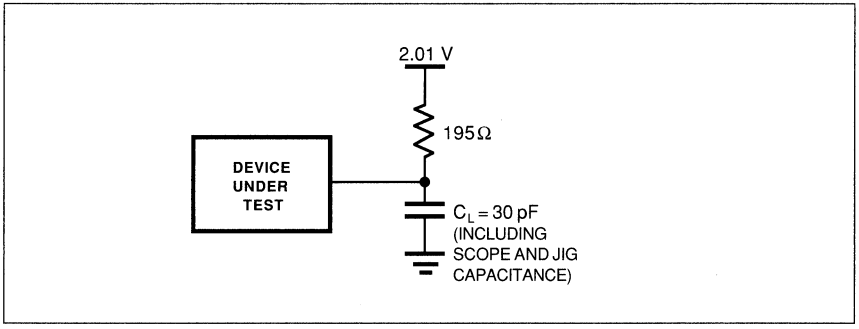


Figure 25. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to an ultra-violet light source. A dosage of 15 W-second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD301 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD301 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

PSD301 Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}/E$	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
AD8/A8	31	F_7	30
AD9/A9	32	F_8	31
AD10/A10	33	E_7	32
GND	34	E_8	33
AD11/A11	35	D_8	34
AD12/A12	36	D_7	35
AD13/A13	37	C_8	36
AD14/A14	38	C_7	37
AD15/A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

Package Information

Figure 26. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

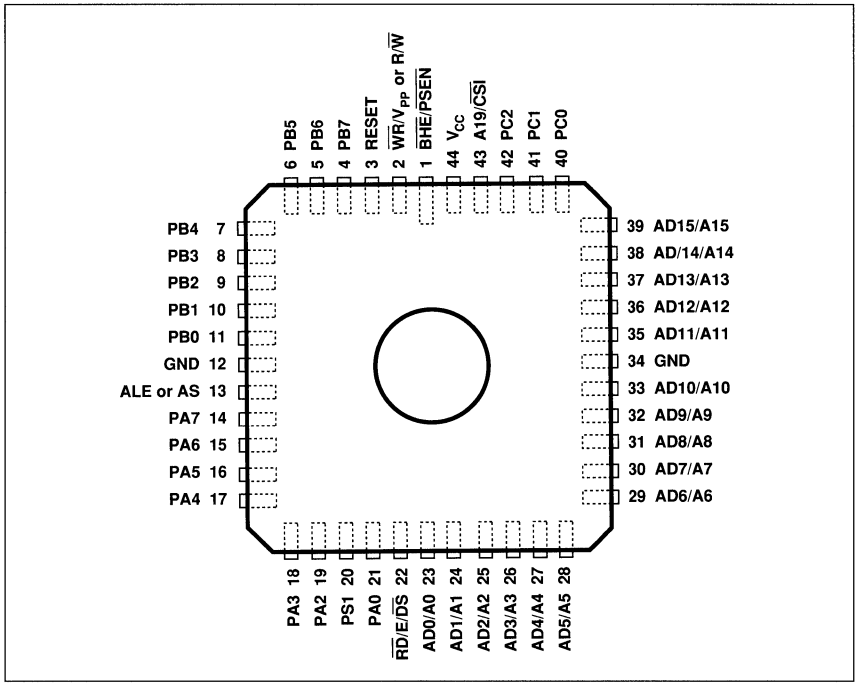


Figure 27. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

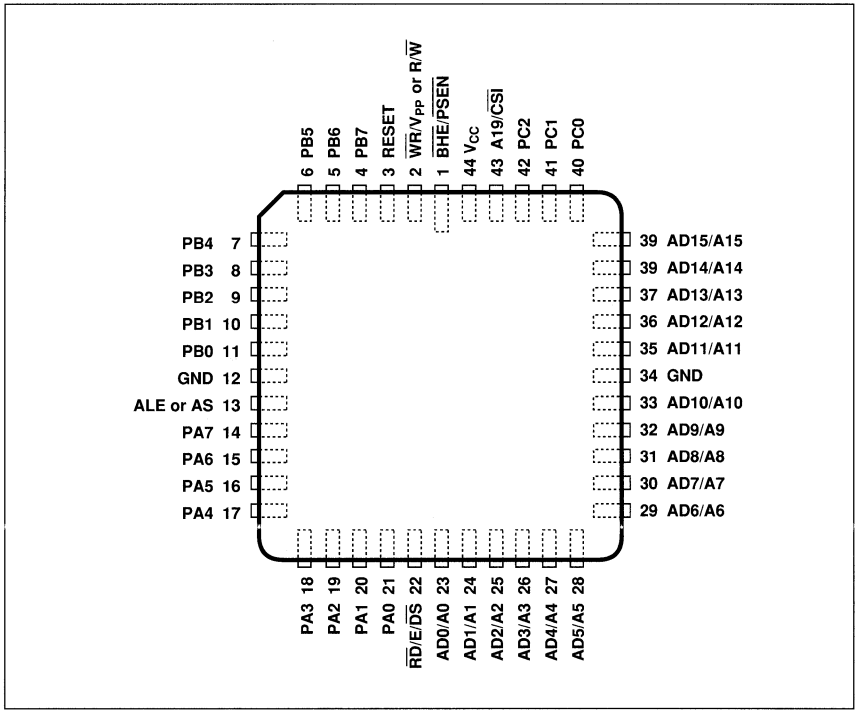


Figure 28. Drawing Q2 — 52-Pin PQFP (Package Type Q)

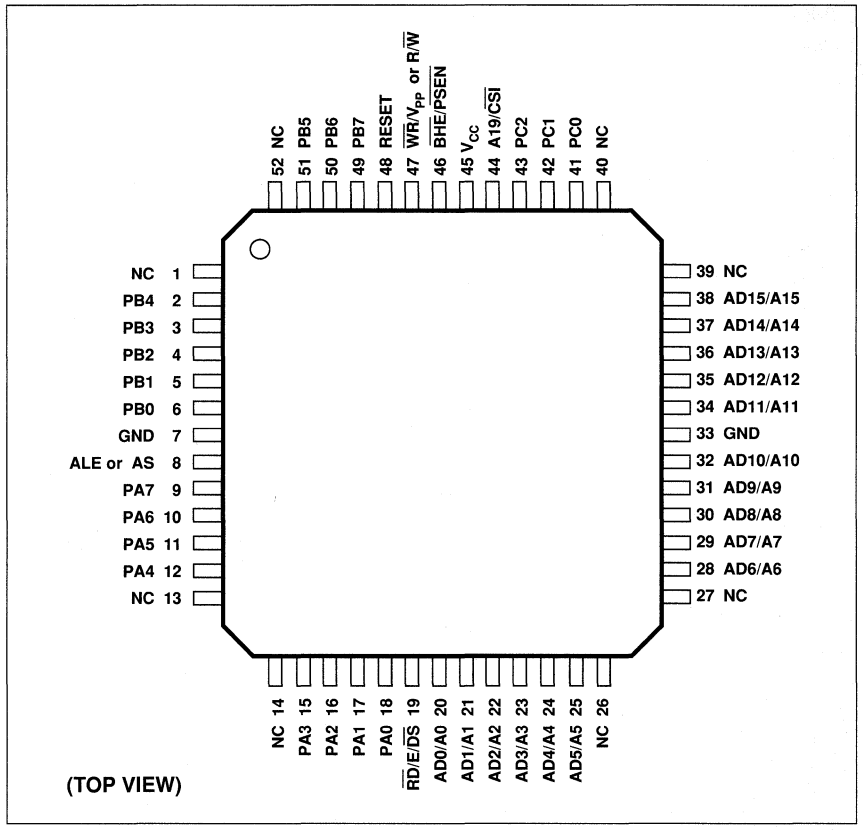
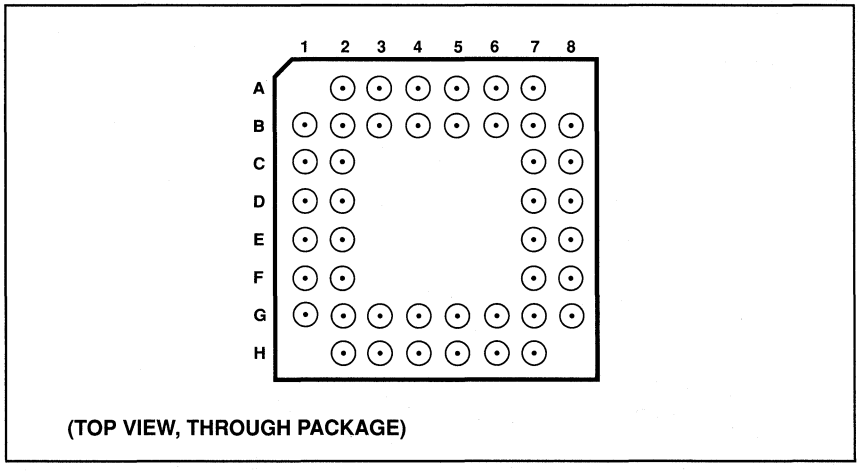


Figure 29: Drawing X2 — 44-Pin CPGA (Package Type X)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD301-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD301-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD301-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD301-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD301-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD301-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD301-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD301-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD301-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD301-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD301-20JI	200	44-pin PLDCC	J2	Industrial	Standard
PSD301-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD301-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD301-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD301-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD301-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD301-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD301-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD301-20XM	200	44-pin CPGA	X2	Military	Standard
PSD301-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

System Development Tools

The PSD301 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD301 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD301 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6015 44-pin CPGA Package Adaptor
- ❑ WS6020 52-pin PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD301 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD301 Location Editor Software
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC Packages)

The configuration of the PSD301 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD301 device, which then can be used. The development cycle is depicted in Figure 30.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour electronic bulletin board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD301 device and System Development Tools. Workshop participants learn how to program high-performance, user-configurable mappable memory subsystems. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD

- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD301 Product Samples

PSD-SILVER

- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000

- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6015

- ❑ 44-pin CPGA Package Adaptor; Used with WS6000 MagicPro Programmer

WS6020

- ❑ 52-pin PQFP Package Adaptor; Used with the WS6000 MagicPro Programmer

WS6021

- ❑ 44-Pin Package Adaptor for CLDCC and PLDCC Packages; Used with the WS6000 MagicPro Programmer

WSI Support

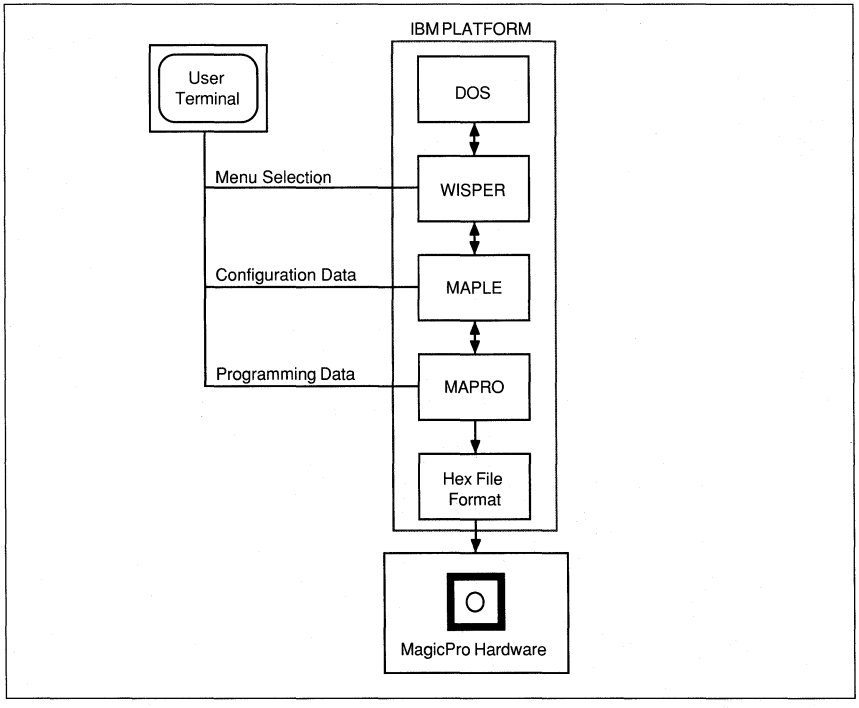
Support services include:

- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training

- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 30. PSD301 Development Cycle



Programmable Peripheral

PSD311

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E
  - — PSEN/ pin for 8051 users
- ❑ 256 Kbits of UV EPROM
  - — Organized as 32K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 4K x 8
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Organized as 2K x 8
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD311 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD311 on an IBM PC

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8098, 80188, 80198
- ❑ **Signetics:** SC80C451
- ❑ **Zilog:** Z8, Z80, Z180

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD311 is the latest member in the rapidly growing WSI family of PSD devices. The PSD311 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumption are essential. When combined in a system, virtually any microcontroller (68HC11, 8051 etc.) and the PSD311 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD311 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD311 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 256K bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD311 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD311 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.

WSI's PSD311 (shown in Figure 1) can efficiently interface with, and enhance, any microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 256K bit EPROM, and 16K bit SRAM on a single chip. The PSD311 does not require any glue logic for interfacing to any 8-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD311's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/W and E. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD311 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD311 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (4K x 8 each) and SRAM (2K x 8) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

Figure 1. PSD311 Architecture

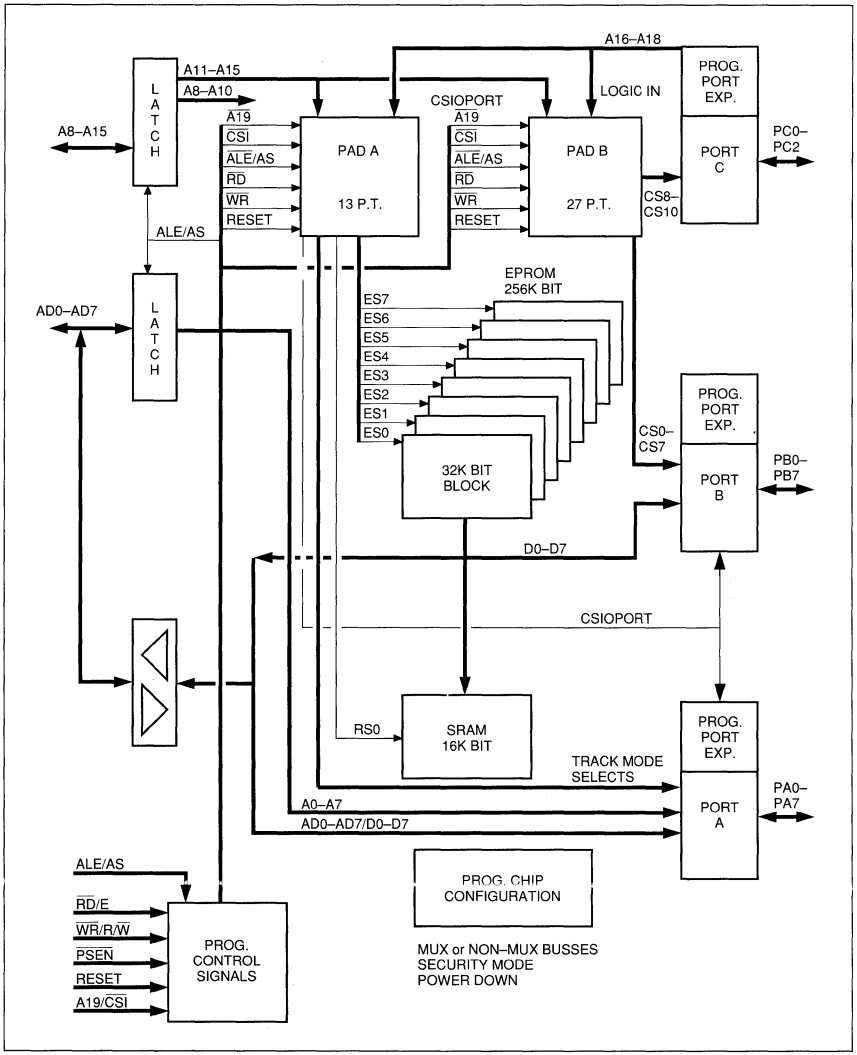


Table 1. PSD311 Pin Descriptions

Name	Type	Description
$\overline{PSEN}$	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, $\overline{PSEN}$ should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$/V_{PP}	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1). When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E	I	When configured as $\overline{RD}$ (CRRWR = 0), this pin provides an active low $\overline{RD}$ strobe. When configured as E (CRRWR = 1), this pin becomes an active high pulse, which, together with R/$\overline{W}$ defines the cycle type. Then, if R/$\overline{W}$ = 1 and E = 1, a read operation is executed. If R/$\overline{W}$ = 0 and E = 1, a write operation is executed.
$\overline{CSI}$/A19		This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 10 and 11 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 8 and 9 for the chip state after reset.
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD7/A7–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD311 configuration. See Table 7. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD311 Pin Descriptions (Cont.)

Name	Type	Description
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 = 1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRDAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD input or output. When configured as an input (CPCF = 0), the bits can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PAD (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
A8 A9 A10 A11 A12 A13 A14 A15	I/O	These pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD311's two operating modes allow it to interface directly to 8-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are described below.

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bidirectional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E, $\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address bus (A8–A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to a microcontroller with an 8-bit non-multiplexed bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (A8–A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

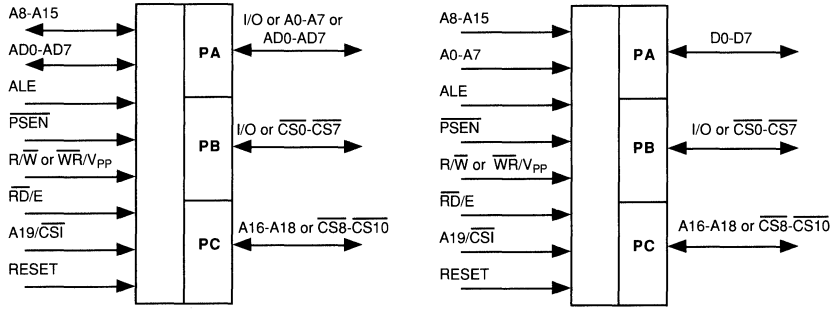
Programmable Address Decoder (PAD)

The PSD311 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 2. PSD311 Port Configurations

Figure 2 shows the PSDS311's I/O port configurations.



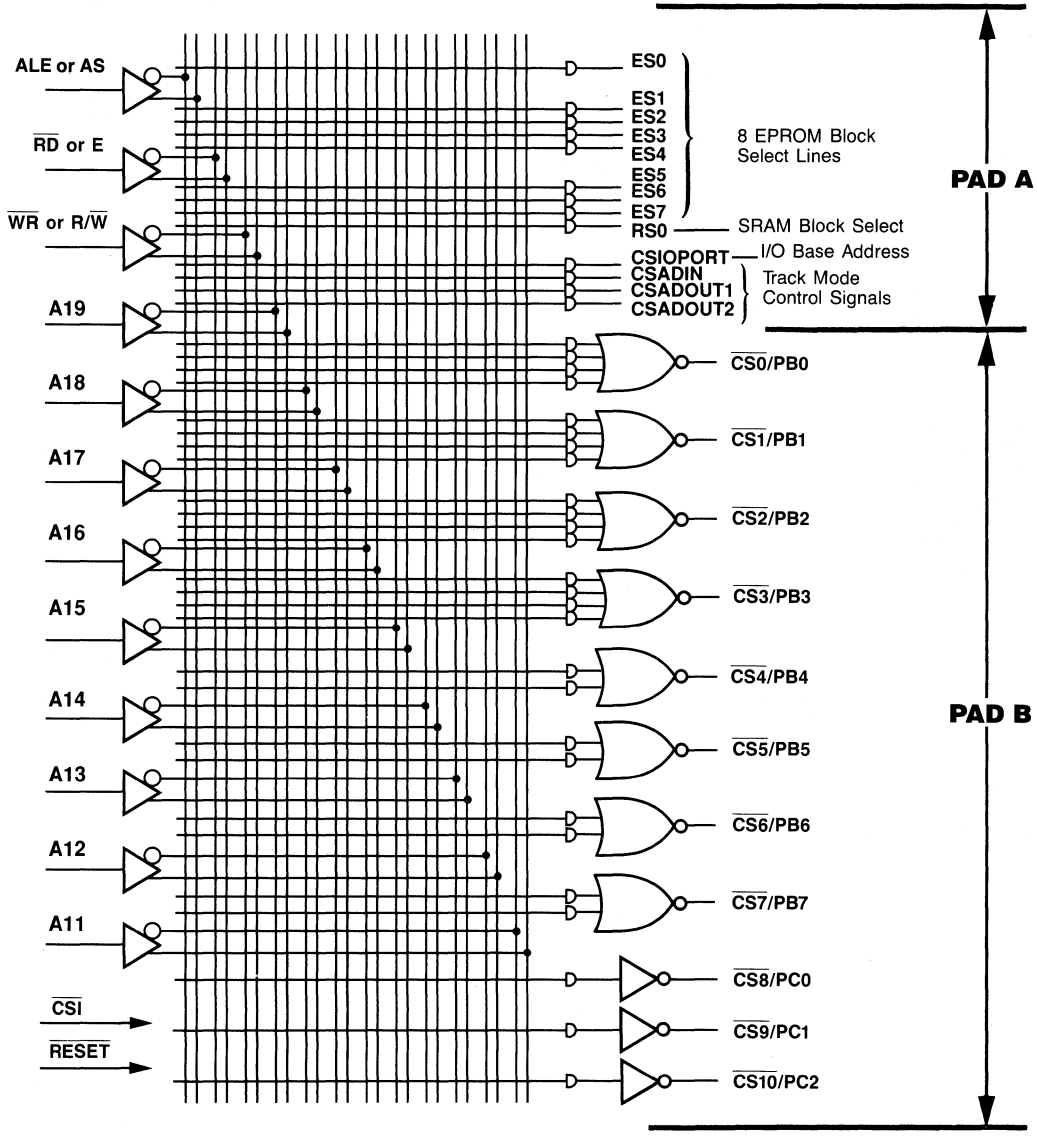
1. PSD311 configured for multiplexed 8-bit address/data bus.
2. PSD311configured for non-multiplexed address/data, 8-bit bus.

Legend: AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD311 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

Figure 3. PSD311 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 10 and 11.
3. RESET deselects all PAD output signals. See Tables 8 and 9.
4. Maximum PAD latency is 35 ns.
5. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A10 or $\overline{CS8}$ can be routed to the external pins of Port C.

Table 3. PSD311 PAD A and B I/O Functions

Function	
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 10 and 11). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 8 and 9.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Table 6.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD311 MAPLE software to set the bits.

Table 4. PSD311 Non-Volatile Configuration Bits

Use This Bit	To
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CRRWR	Set the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins to $\overline{RD}$ and $\overline{WR}$ pulse, or to E strobe and R/$\overline{W}$ status.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option. (Note 6)
CSECURITY	Set the security on or off.
CRESET	Set the RESET polarity.
$\overline{COMB}$/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CATD	Configure Pins A16–A19 as PAD logic inputs or higher-order address inputs

NOTE: 6. For functional and value descriptions, refer to Table 5.

Table 5. PSD311 Configuration Bits[7,8] (45 total bits)

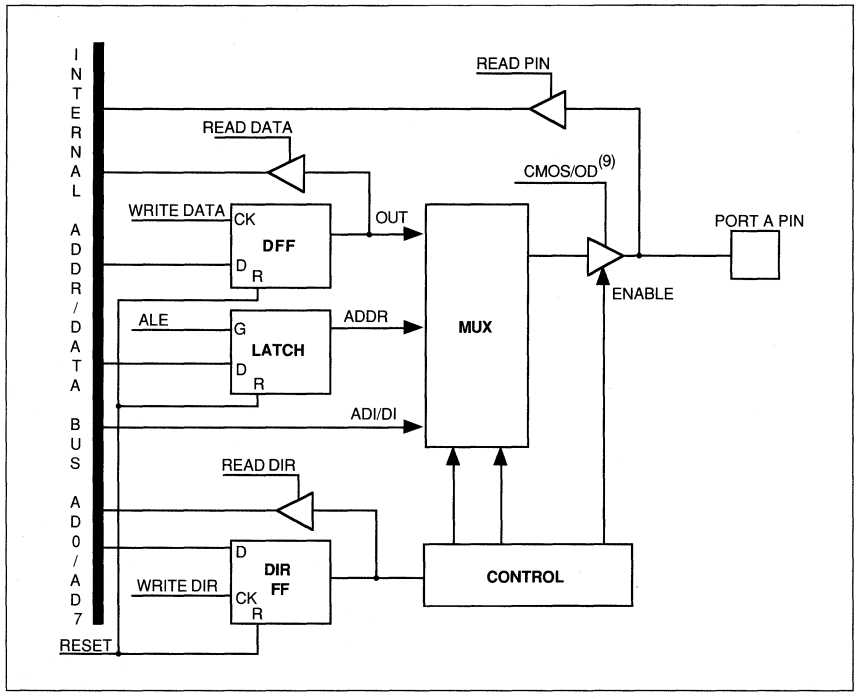
Configuration Bits	No. of Bits	Function
CADDRDAT	1	Address/data multiplexed or non-multiplexed (separate buses) CADDRDAT = 0, non-multiplexed address/data bus CADDRDAT = 1, multiplexed address/data bus
CRRWR	1	CRRWR = 0, $\overline{RD}$ and $\overline{WR}$ active low strobes CRRWR = 1, R/$\overline{W}$ status and E active high pulse
CA19/CSI	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down mode CA19/$\overline{CSI}$ = 1, A19 input to PAD
CALE	1	Active high or active low CALE = 0, active high CALE = 1, active low
CRESET	1	Active high or active low CRESET = 0, active low reset signal CRESET = 1, active high reset signal
$\overline{COMB}$/SEP	1	Combined or separate memory space for EPROM and SRAM $\overline{COMB}$/SEP = 0, combined $\overline{COMB}$/SEP = 1, separate
CPAF1	8	Port A I/Os or A0–A7 CPAF1 = 0, Port A pin = I/O CPAF1 = 1, Port A pin = Ai ($0 \leq i \geq 7$)
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CPBF	8	Port B I/Os or $\overline{CS0}$–$\overline{CS7}$ CPBF = 0, Port B Pin = $\overline{CSi}$ ($0 \leq i \leq 7$) CPBF = 1, Port B Pin = I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C Pin = Ai ($16 \leq i \leq 18$) CPCF = 1, Port C Pin = $\overline{CSi}$ ($8 \leq i \leq 10$)
CPACOD	8	Port A CMOS or open-drain outputs CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBCOD	8	Port B CMOS or open-drain outputs CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CADDHLT	1	A16–A19 latched or latch transparent CADDHLT = 0, address latch transparent CADDHLT = 1, address latched (ALE dependent)
CATD	1	A16–A19 used as address or logic inputs CATD = 0, logic inputs CATD = 1, address inputs
CSECURITY	1	Security on or off CSECURITY = 0, no security CSECURITY = 1, secured part (cannot be copied)

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

Port Functions

The PSD311 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Port Functions (Cont.)

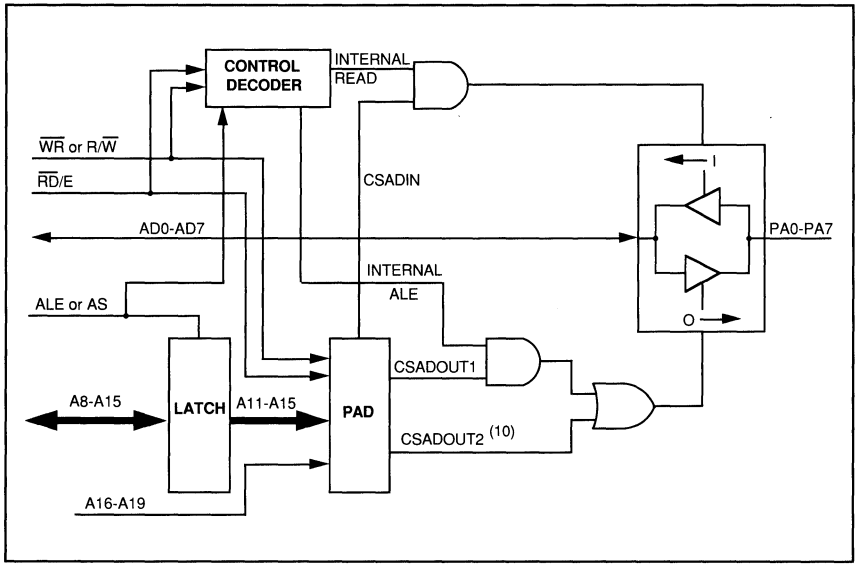
Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register.

Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD311 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Figure 5. Port A Track Mode



NOTE: 10. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Port Functions (Cont.)

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figure 17). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD311 location, data is presented on Port A pins. When writing to an internal PSD311 location, data present on Port A pins is written to that location.

Port B

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Accessing the I/O Port Registers

Table 6 shows the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes

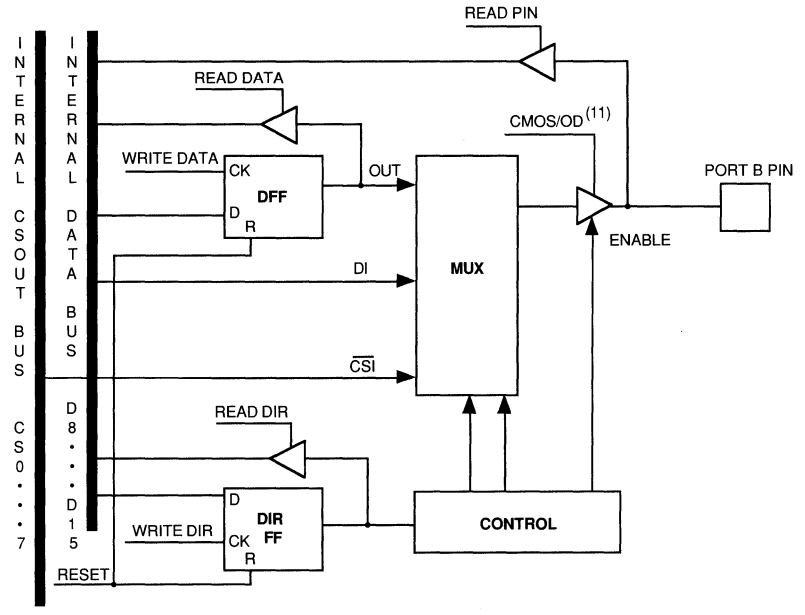
In non-multiplexed modes, A0–A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. See Table 7.

A16–A19 As Inputs

If one or more of the pins PC0, PC1, PC2 and $\overline{CSI}$/A19 are configured as inputs, the configuration bits CADDHLT and CATD define their functionality inside the part. CADDHLT determines if these inputs are to be latched by the trailing edge of the ALE or AS signal (CADDHLT = 1), or enabled into the PSD311 at all times (CADDHLT = 0), transparent mode). CATD determines whether these lines are high-order address lines, that take part in the derivation of memory and I/O select signals inside the chip (CATD = 1), or logic input lines that have no impact on memory or I/O selections (CATD = 0). Logic input lines typically participate in the Boolean expressions implemented in the PAD.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.

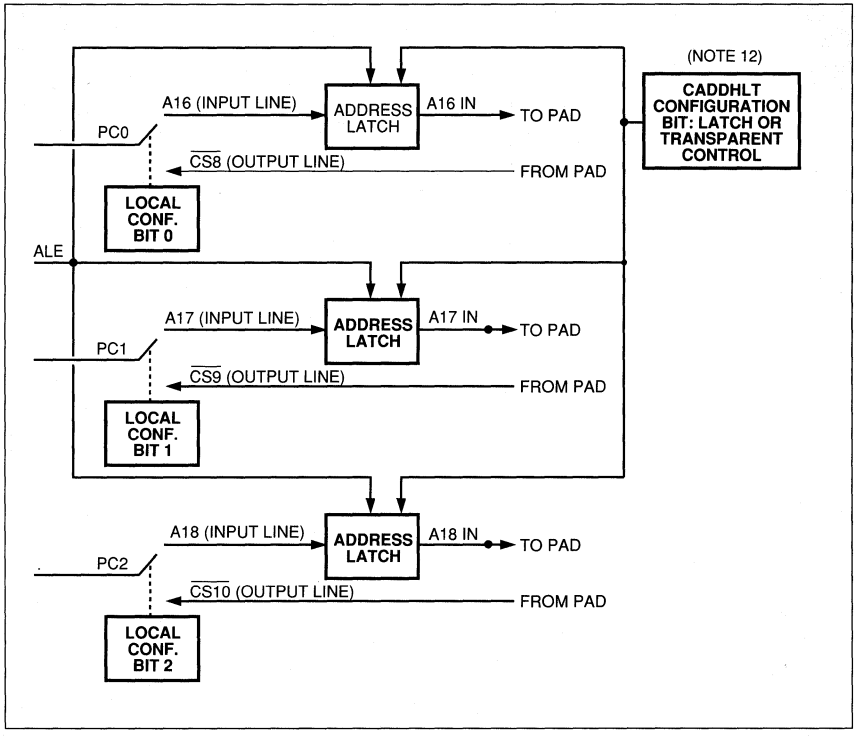


NOTE: 11. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Figure 7. Port C Structure



NOTE: 12. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 7. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD0/A0-AD7/A7	CADDRDAT = 0	non-multiplexed mode	Transparent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

EPROM

The PSD311 has 256K bits of EPROM and is organized as 32K x 8. The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 4K x 8.

SRAM

The PSD311 has 16K bits of SRAM and is organized as 2K x 8. The SRAM is selected by the RS0 output of the PAD.

Control Signals

The PSD311 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E, ALE, $\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD311 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

$\overline{RD}$/E

In operational mode, this signal can be configured as $\overline{RD}$, or E. As $\overline{RD}$, all read operations to the PSD311 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ strobe of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E pin performs a write operation.

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{PSEN}$

The $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if $\overline{COMB}$/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1).

Control Signals (Cont.)

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD311's $\overline{PSEN}$ pin must be connected to the $\overline{PSEN}$ pin of the microcontroller.

If $\overline{COMB}$/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the $\overline{PSEN}$ pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by $\overline{RD}$ low (CRRWR = 0), or by E and R/$\overline{W}$ high (CRRWR = 1). See Figures 8 and 9.

Figure 8. Combined Address Space

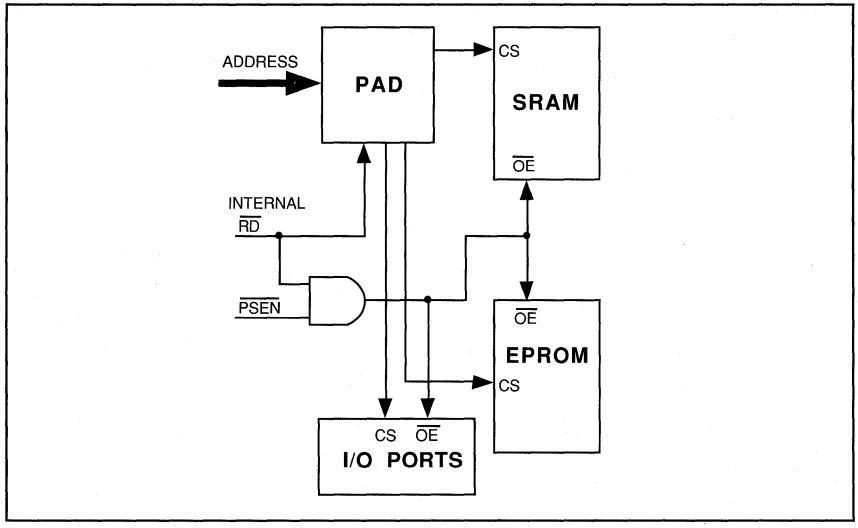
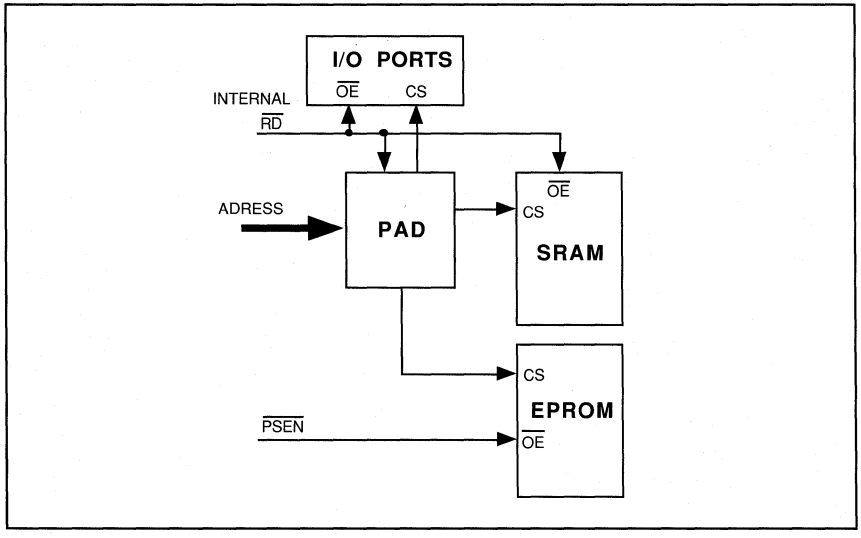


Figure 9. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD311. Reset polarity is programmable (active low or active high). Whenever the PSD311 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 8 and 9 indicate the state of the part during and after reset.

A19/CSI

When configured as CSI, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD311 states during the power-down mode, see Tables 10 and 11, and Figure 10.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADDHLT = 1) or as a general-purpose logic input (CADDHLT = 0). A19 can be configured as ALE dependent or as transparent input (see Table 7). In this mode, the chip is always enabled.

Table 8. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 9. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 13)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 13. All PAD outputs are in a non-active state.

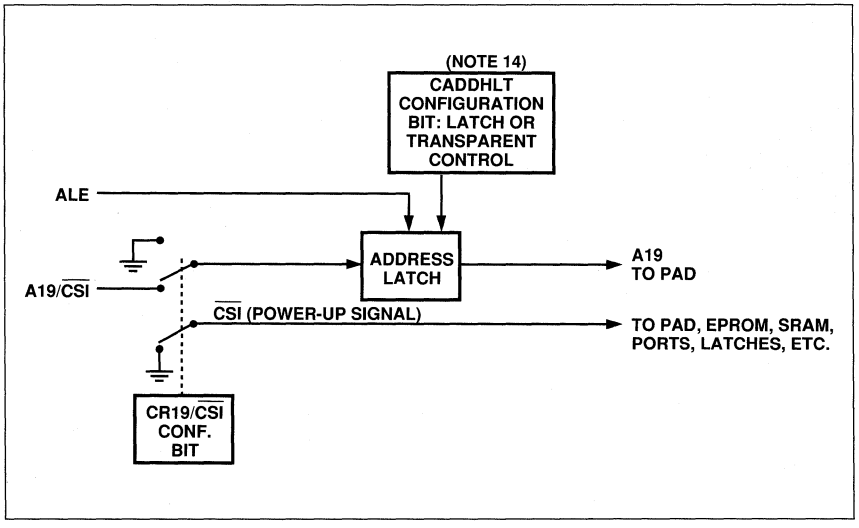
Table 10. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 11. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 10. A19/$\overline{CSI}$ Cell Structure

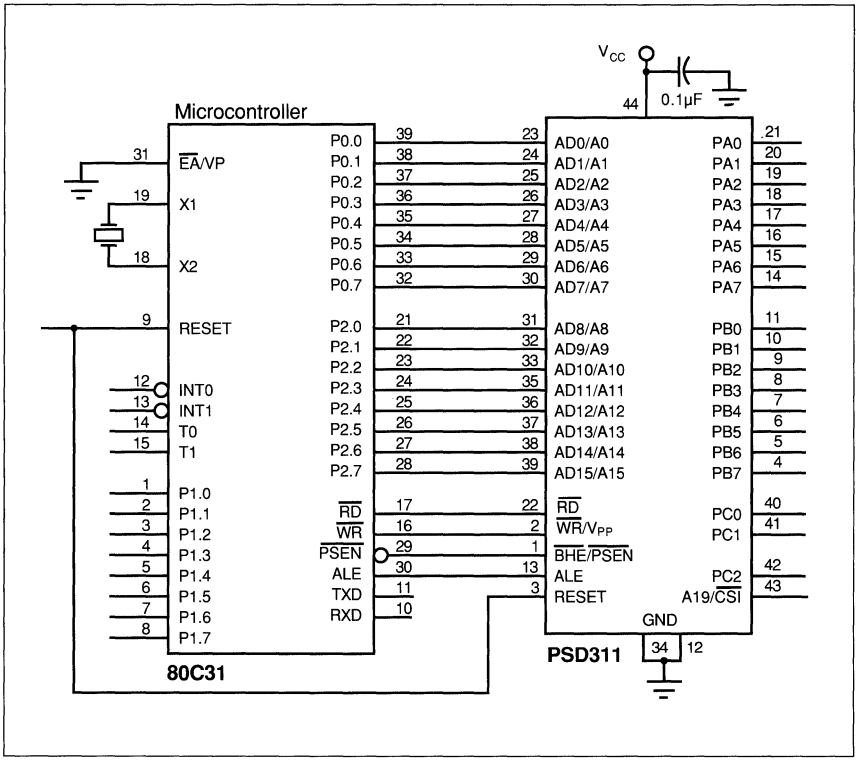


NOTE: 14. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

System Applications

In Figure 11, the PSD311 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 11. PSD311 Interface With Intel's 80C31



The configuration bits for Figure 11 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

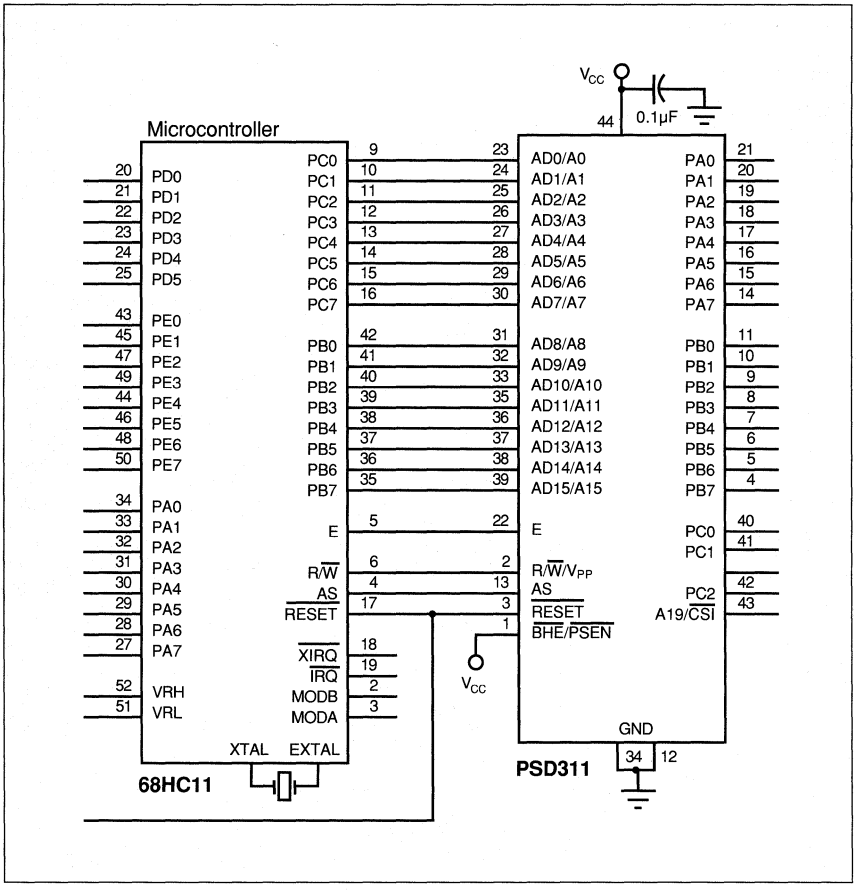
Security Mode

Security Mode in the PSD311 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD311 contents cannot be copied on a programmer.

System Applications

In Figure 12, the PSD311 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/W signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 12. PSD311 Interface With Motorola's 68HC11



The configuration bits for Figure 12 are:

CRESET	0
CALE	0
CDATA	0
CADDRDAT	1
COMB/SEP	0
CRRWR	1
CEDS	0

All other configuration bits may vary according to the application requirements.

Absolute Maximum Ratings[15]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 15. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40°C to +80°C	+ 5 V		± 10%	± 10%
Military	–55°C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 16 and 18)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 17 and 18)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 16 and 19)	Comm'l (Note 20)		16	35	mA
		Comm'l (Note 21)		28	50	
		Ind/Mil (Notes 20)		16	45	
		Ind/Mil (Notes 21)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 16 and 19)	Comm'l (Note 20)		47	80	mA
		Comm'l (Note 21)		59	95	
		Ind/Mil (Note 20)		47	100	
		Ind/Mil (Note 21)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 17 and 19)	Comm'l (Note 20)		36	65	mA
		Comm'l (Note 21)		58	80	
		Ind/Mil (Note 20)		36	80	
		Ind/Mil (Note 21)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 17 and 19)	Comm'l (Note 20)		67	105	mA
		Comm'l (Note 21)		79	120	
		Ind/Mil (Note 20)		67	130	
		Ind/Mil (Note 21)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 16. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
17. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
18. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
19. AC power component is 3.0 mA/MHz (power = AC + DC).
20. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
21. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

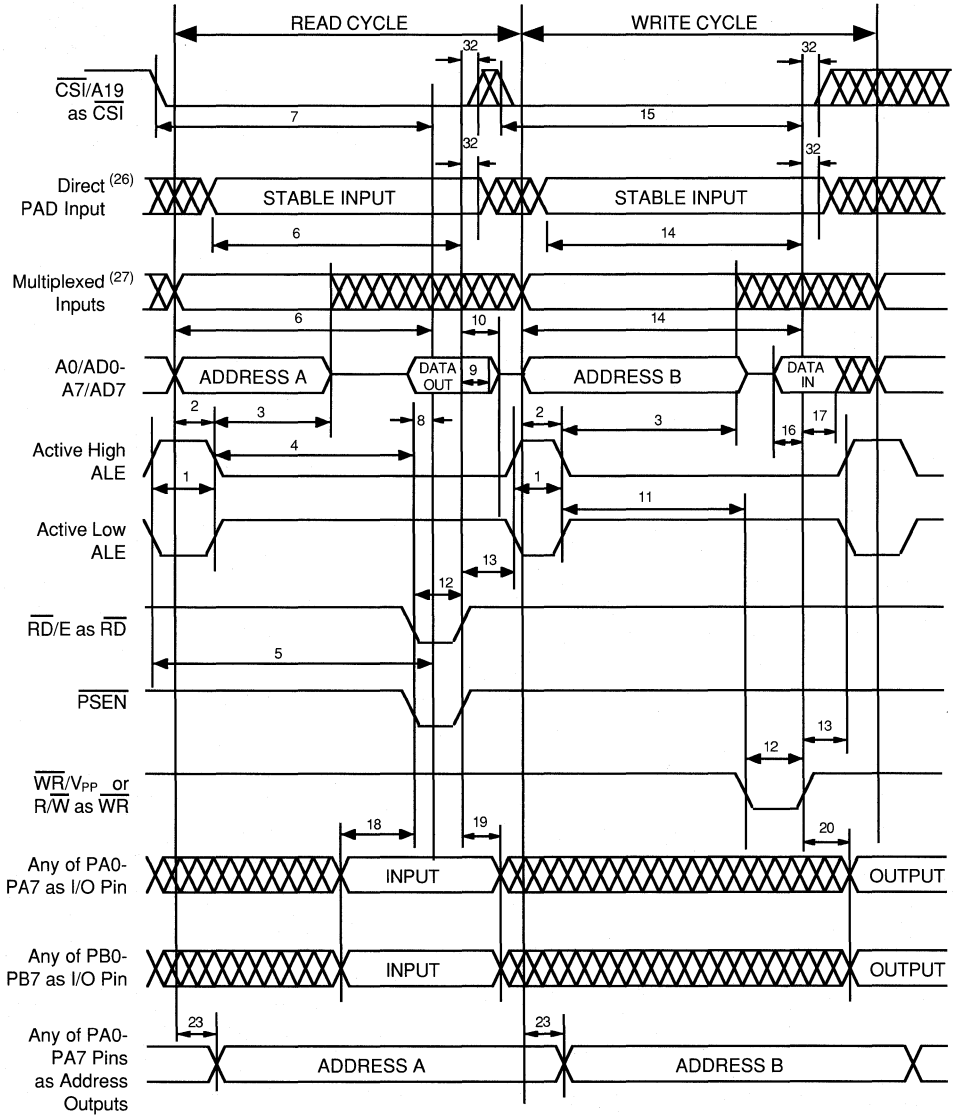
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	5		10		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	140		170		220		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		150		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		35		40		45	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	20		30		40		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		210		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	35	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	35	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		22		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		40		50	
T24	Track Mode Address Holding Time	15		15		27		
T25	Track Mode Read Propagation Delay		29		29		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		20		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	45	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	45	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E High	15		20		25		

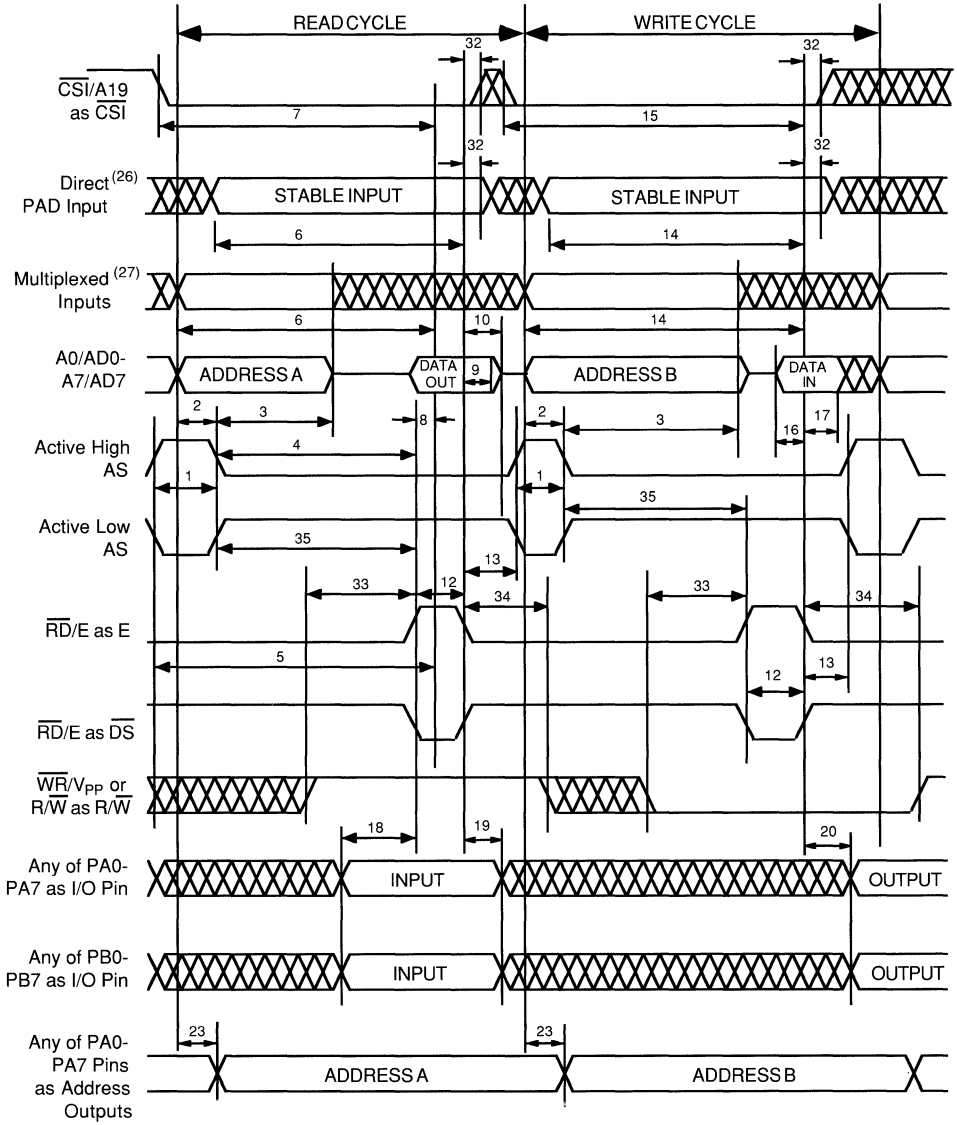
NOTES: 22. ADi = any address line.
23. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
24. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, $\overline{RD}$/E, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
25. Control signals $\overline{RD}$/E or $\overline{WR}$ or R/$\overline{W}$.

Figure 13. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



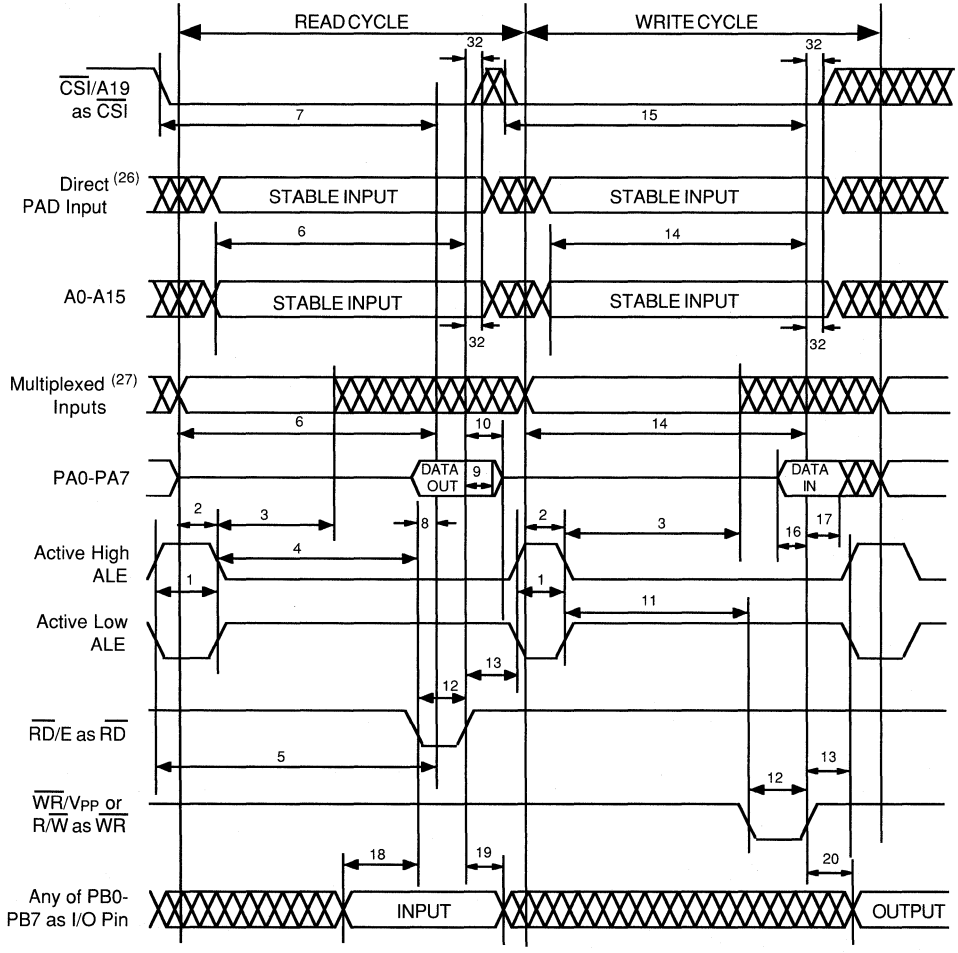
See referenced notes on page 2-75.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



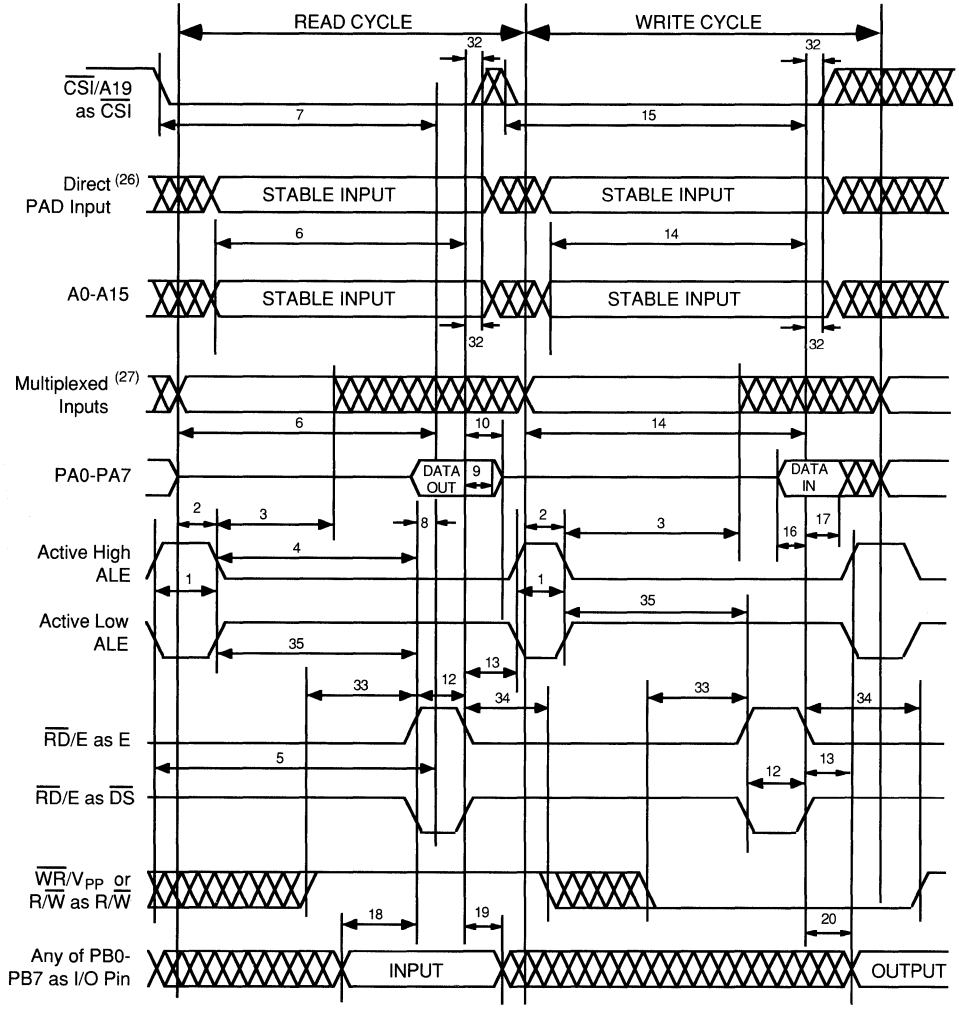
See referenced notes on page 2-75.

Figure 15. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-75.

Figure 16 Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-75.

Figure 17. Chip-Select Output Timing

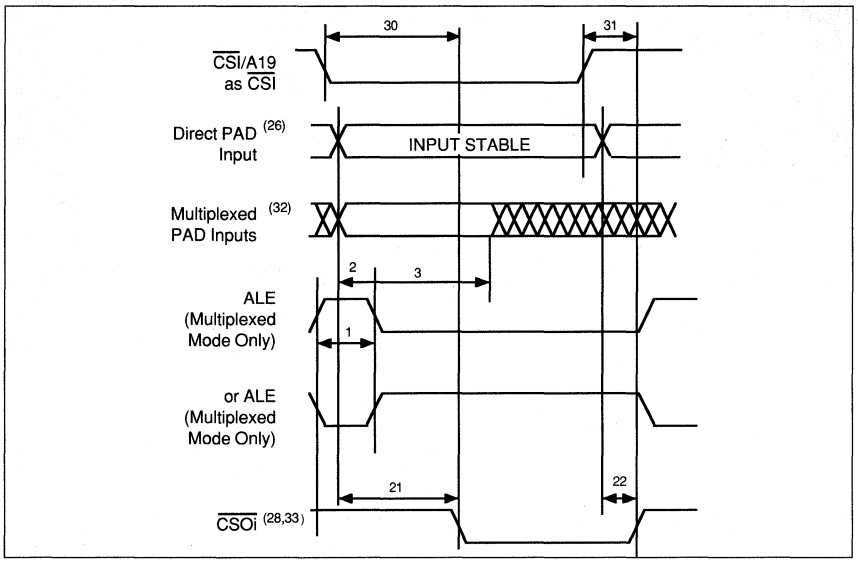
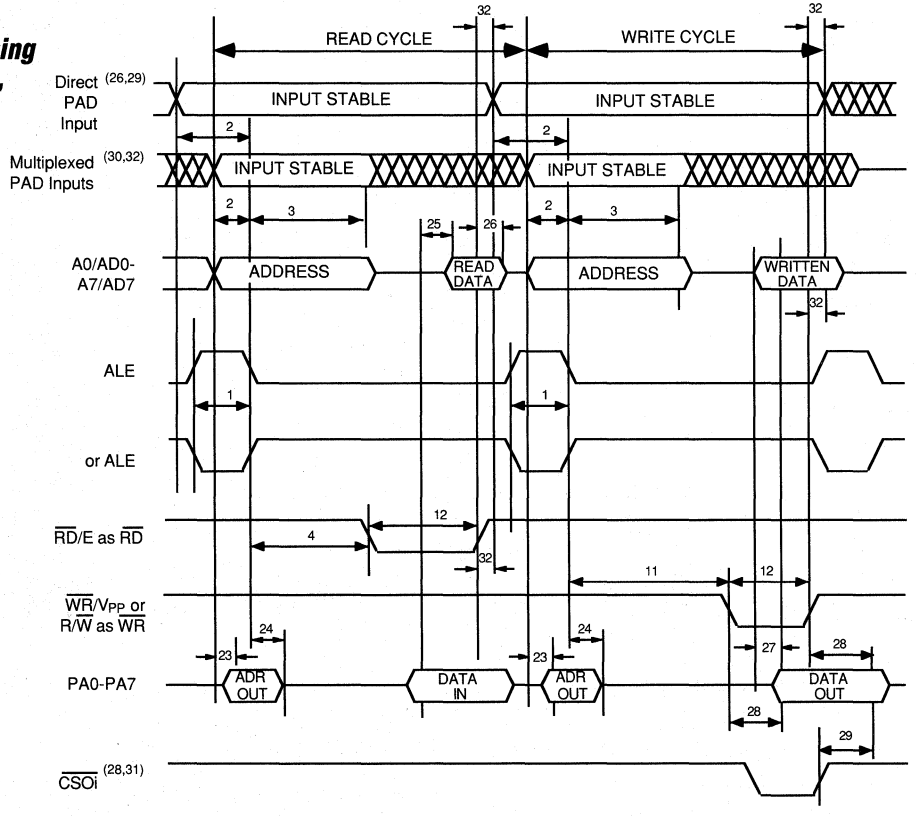
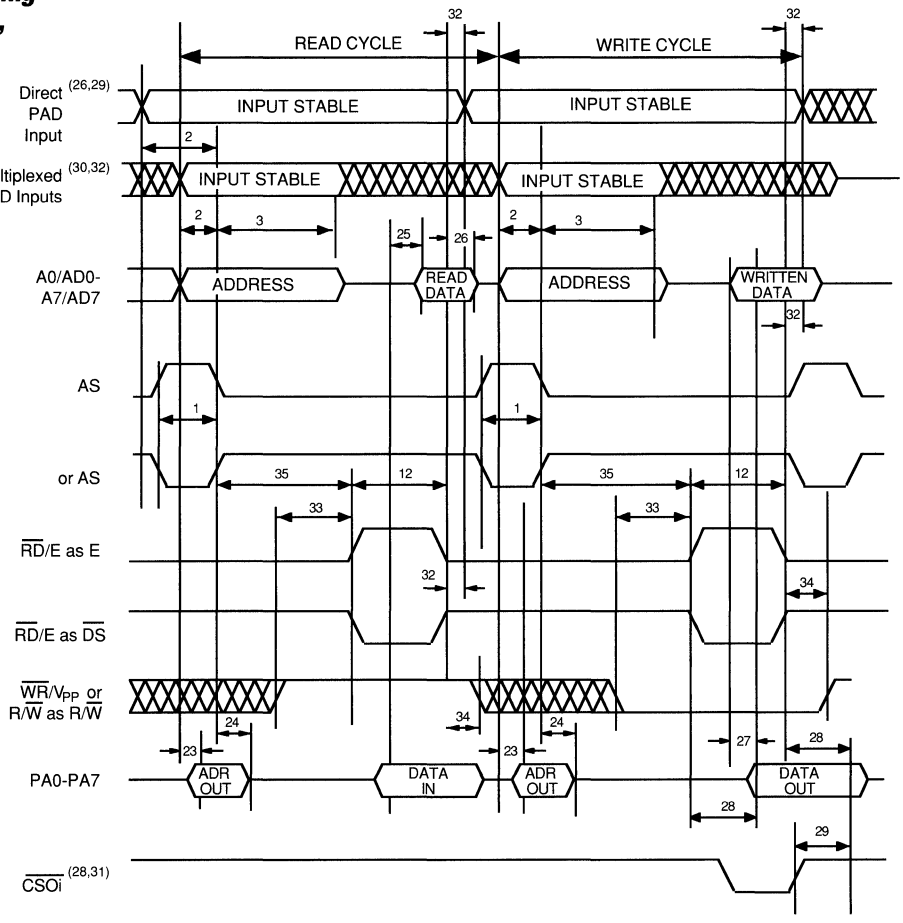


Figure 18. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-75.

Figure 19. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

26. Direct PAD input = any of the following direct PAD input lines: CSI/A19 as transparent A19, RD/E, WR or R/W, transparent PC0–PC2, ALE in non-multiplexed modes.
27. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A7/AD7, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
28. CSOi = any of the chip-select output signals coming through Port B (CS0–CS7) or through Port C (CS8–CS10).
29. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
30. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
31. The write operation signals are included in the CSOi expression.
32. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11–A15, CSI/A19 as ALE dependent A19, ALE dependent PC0–PC2.
33. CSOi product terms can include any of the PAD input signals shown in Figure 3, except for reset and CSI.

Table 12 Pin Capacitance[34]

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Conditions	Typical[35]	Max	Units
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	V_{PP} = 0 V	18	25	pF

NOTES: 34. This parameter is only sampled and is not 100% tested.
35. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 20. AC Testing Input/Output Waveform

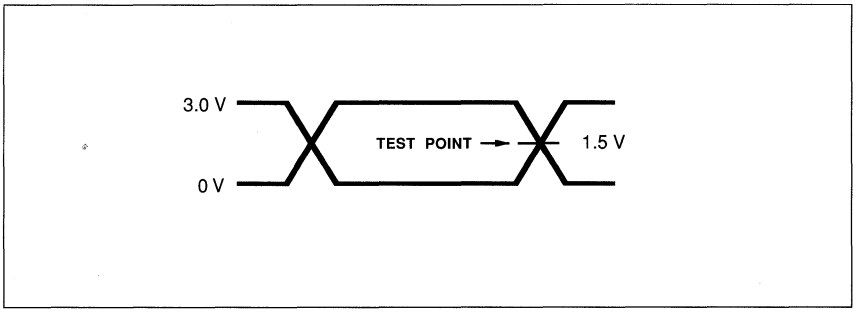
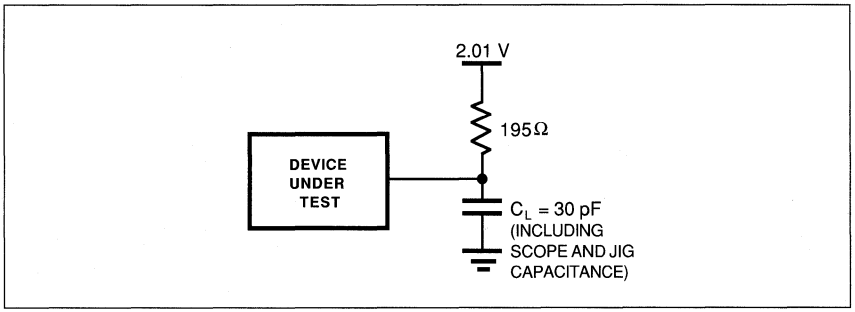


Figure 21. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD311 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD311 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}$/E	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
A8	31	F_7	30
A9	32	F_8	31
A10	33	E_7	32
GND	34	E_8	33
A11	35	D_8	34
A12	36	D_7	35
A13	37	C_8	36
A14	38	C_7	37
A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 22 Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

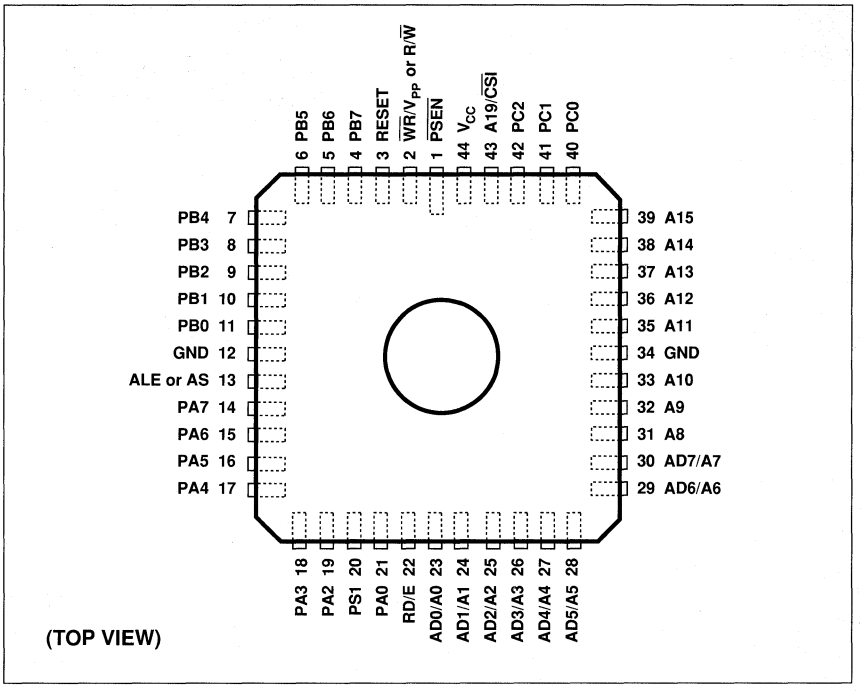


Figure 23. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

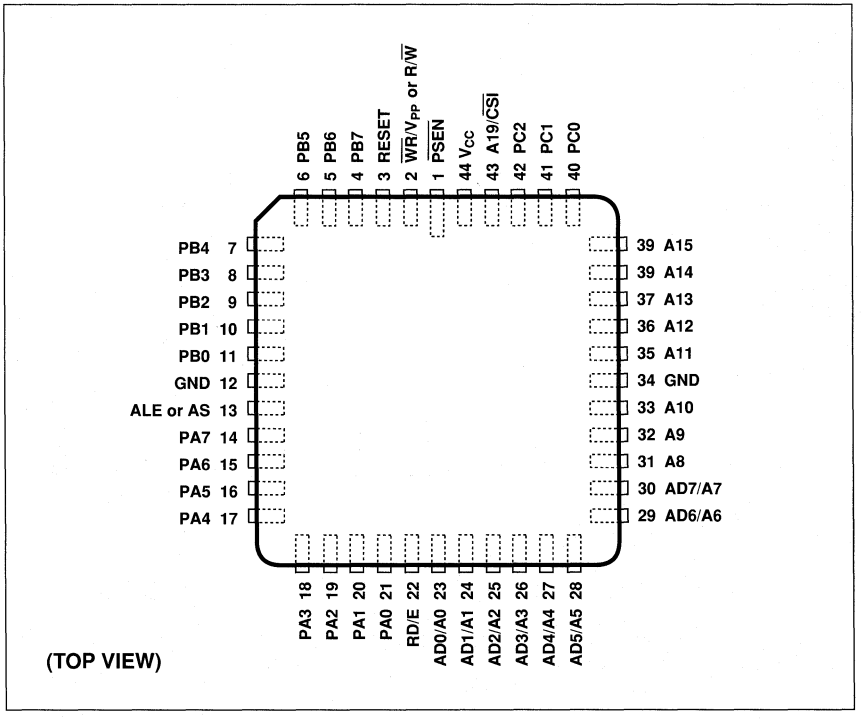


Figure 24. Drawing Q2 — 52-Pin PQFP (Package Type Q)

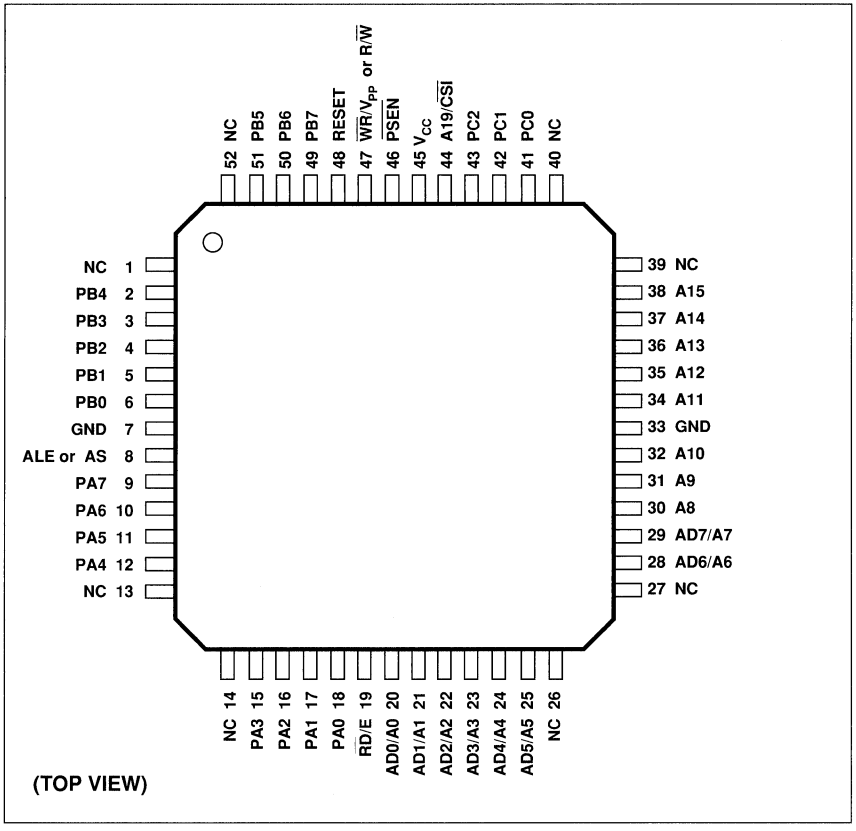
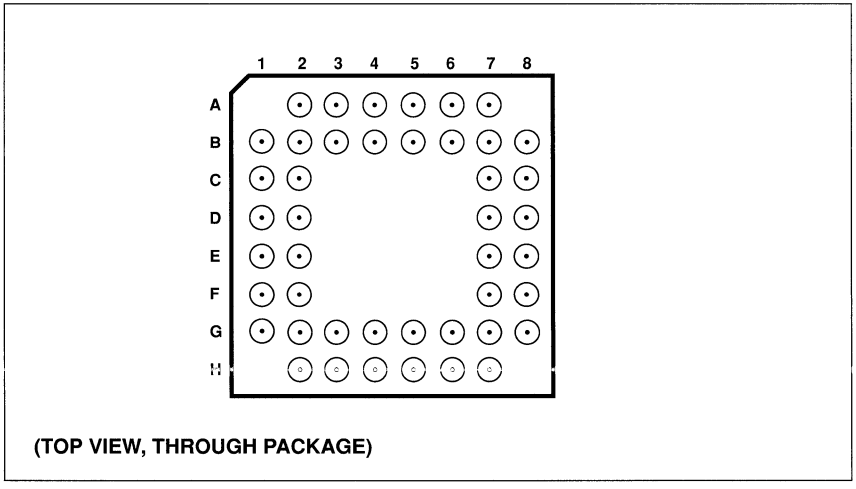


Figure 25. Drawing X2 — 44-Pin CPGA (Package Type X)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD311-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD311-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD311-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD311-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD311-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD311-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD311-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD311-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD311-15LM	150	44-pin CLDCC	L4	Military	Standard
PSD311-15LMB	150	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD311-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD311-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD311-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD311-15XM	150	44-pin CPGA	X2	Military	Standard
PSD311-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD311-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD311-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD311-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD311-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD311-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD311-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD311-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD311-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD311-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD311-20XM	200	44-pin CPGA	X2	Military	Standard
PSD311-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

PSD311
System Development Tools

System Development Tools

The PSD311 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD311 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD311 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6020 52-pin PSD311 PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD311 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD311 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD311 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD311 device, which then can be used in the target system. The development cycle is depicted in Figure 26.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD311 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD311 Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6020
- ❑ 52-pin PQFP Package Adaptor. Used with the WS6000 MagicPro Programmer

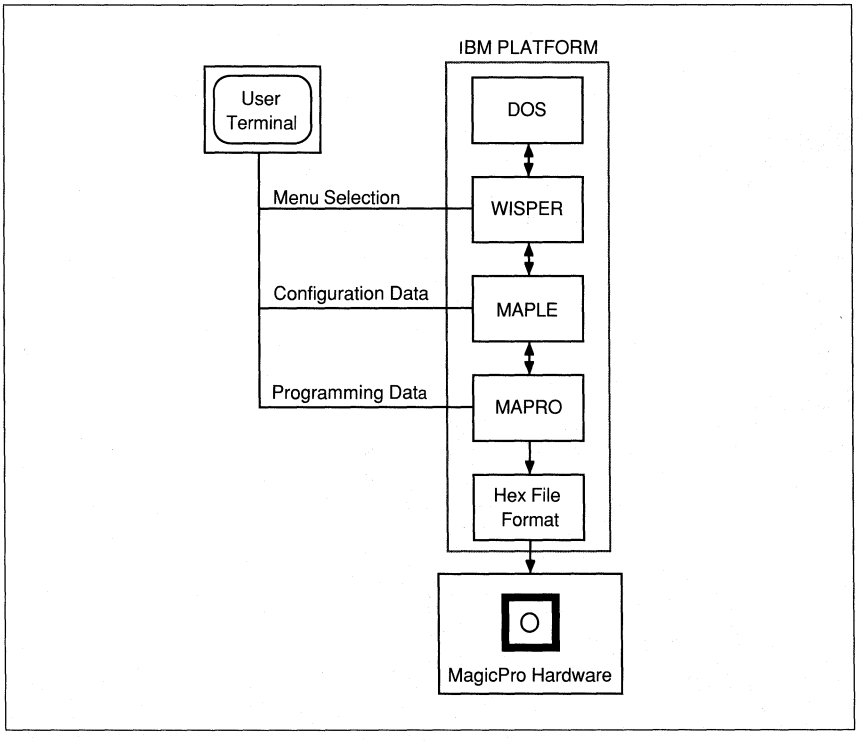
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 26. PSD311 Development Cycle



Programmable Peripheral

PSD302

Programmable Microcontroller Peripheral with Memory

Preliminary

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — BHE/ pin for byte select in 16-bit mode
  - — PSEN/ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Configurable as 64K x 8 or as 32K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8 or 4K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD302 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD302 on an IBM PC
- ❑ Downward Pin and Functionally Compatible with the PSD301

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/8098, 80186/88, 80196/98
- ❑ **Signetics:** SC80C451, SC80C552
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD302 is the latest member in the rapidly growing family of PSD devices. The PSD302 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 8096, 16000, etc.) and the PSD302 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD302 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD302 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 512K bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD302 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD302 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanding address space of microcontrollers

WSI's PSD302 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 512K bit EPROM, and 16K bit SRAM on a single chip. The PSD302 does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD302's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD302 in a 16-bit configuration. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD302 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD302 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (as 8K x 8 or as 4K x 16) and SRAM (as 2K x 8 or as 1K x 16) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

The page register extends the accessible address space of certain microcontrollers from 64K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line processors by a factor of 16.

Figure 1. PSD302 Architecture

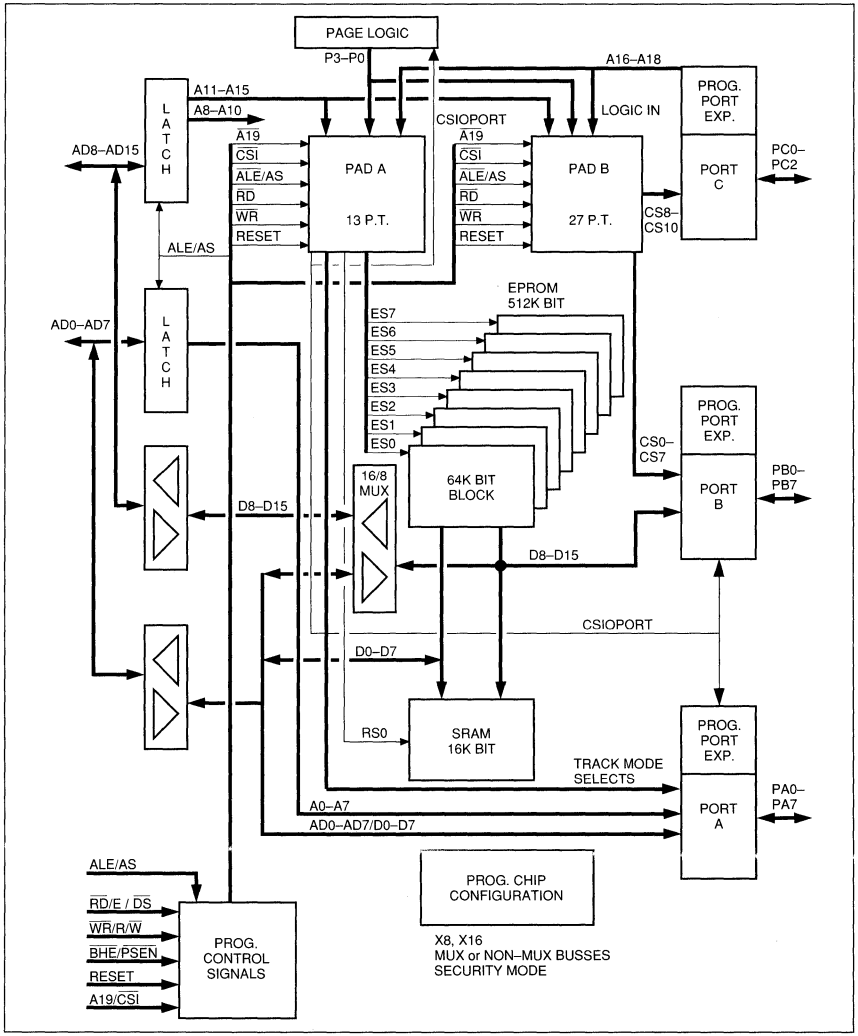


Table 1. PSD302 Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/E/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD302, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0: R/$\overline{W}$ = X, E = 0, NOP; R/$\overline{W}$ = 0, E = 1, write; R/$\overline{W}$ = 1, E = 1, read CEDS = 1: R/$\overline{W}$ = X, $\overline{DS}$ = 0, NOP; R/$\overline{W}$ = 0, $\overline{DS}$ = 1, write; R/$\overline{W}$ = 1, $\overline{DS}$ = 0, read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/E/\overline{DS}$	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10 and 11 for the chip state after reset.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD302 Pin Descriptions (Cont.)

Name	Type	Description
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD302 configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. When the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.

Table 1. PSD302 Pin Descriptions (Cont.)

Name	Type	Description
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD302's four operating modes allow it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- Multiplexed 8-bit address/data bus
- Multiplexed 16-bit address/data bus
- Non-multiplexed address/data, 8-bit data bus
- Non-multiplexed 16-bit address/data bus

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

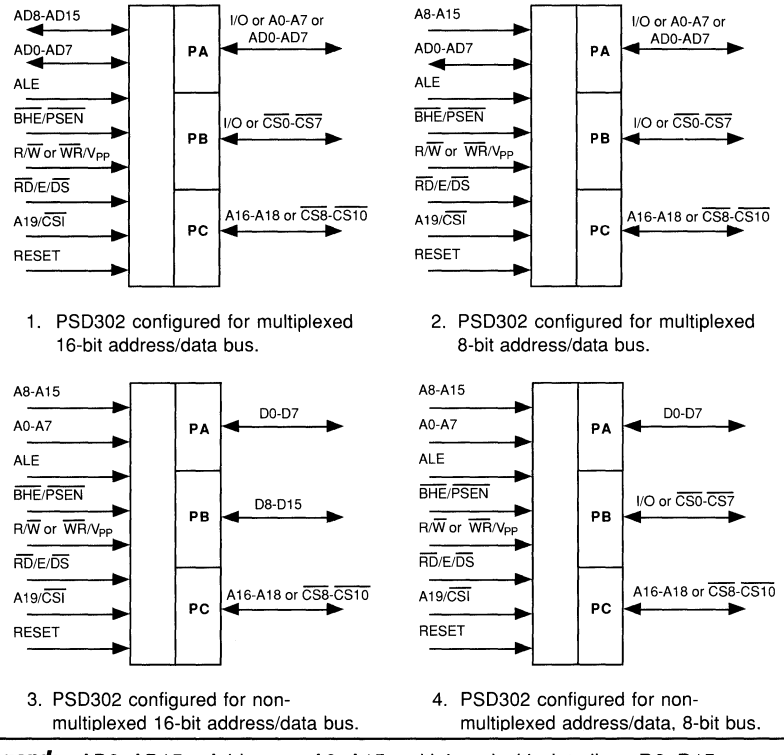
Non-Multiplexed Address/Data, 16-bit Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Figure 2. PSD302 Port Configurations

Figure 2 shows the PSDS302's I/O port configurations.



1. PSD302 configured for multiplexed 16-bit address/data bus.
2. PSD302 configured for multiplexed 8-bit address/data bus.
3. PSD302 configured for non-multiplexed 16-bit address/data bus.
4. PSD302 configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD302 Bus and Port Configuration Options

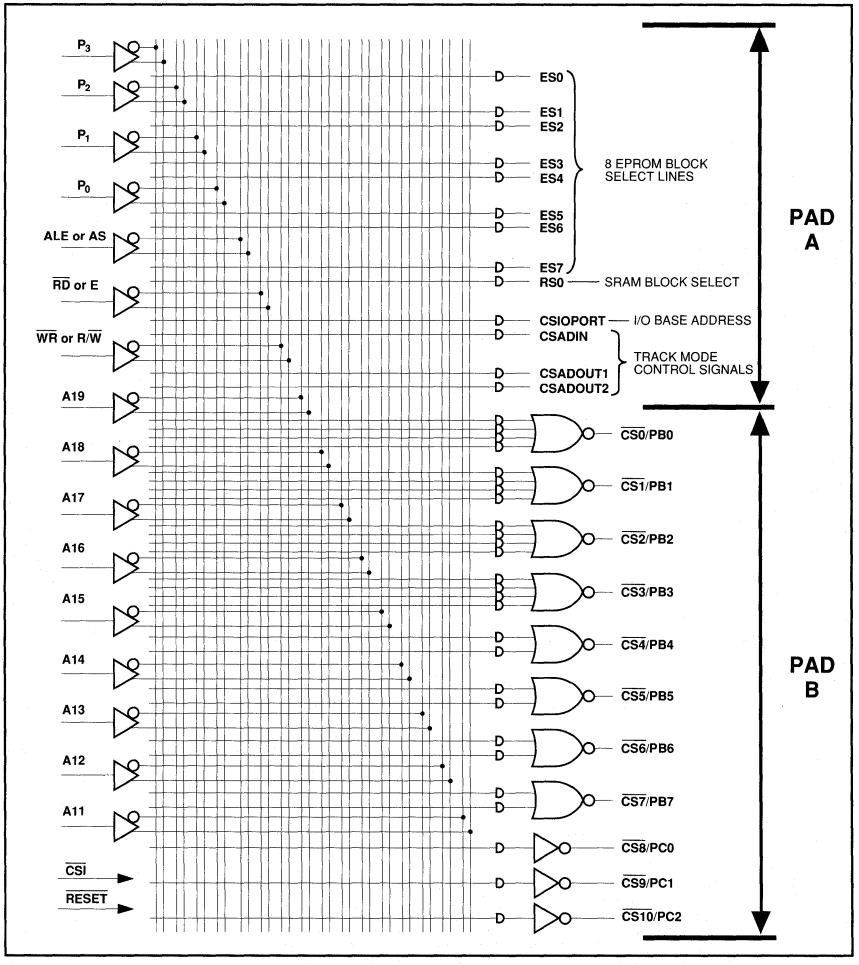
	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Programmable Address Decoder (PAD)

The PSD302 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PSD302 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.

3. RESET deselects all PAD output signals. See Tables 10 and 11.

4. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Table 3. PSD302 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD302 MAPLE software to set the bits.

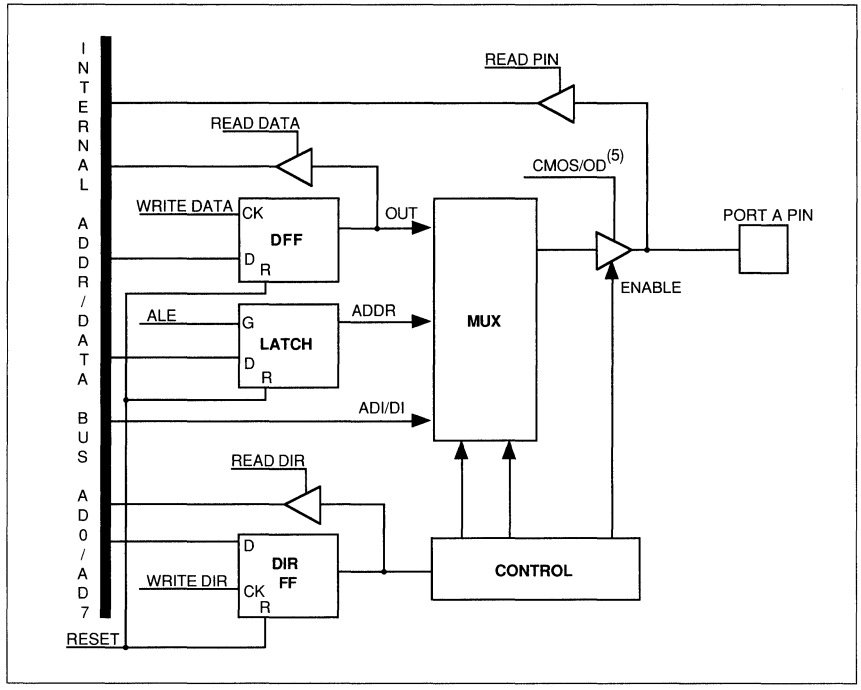
Table 4. PSD302 Non-Volatile Configuration Bits

Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits.
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
COMB/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16–A19 individually as logic or address inputs.
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched.
CRRWR	Configure the polarity and control methods of read and write cycles.

Port Functions

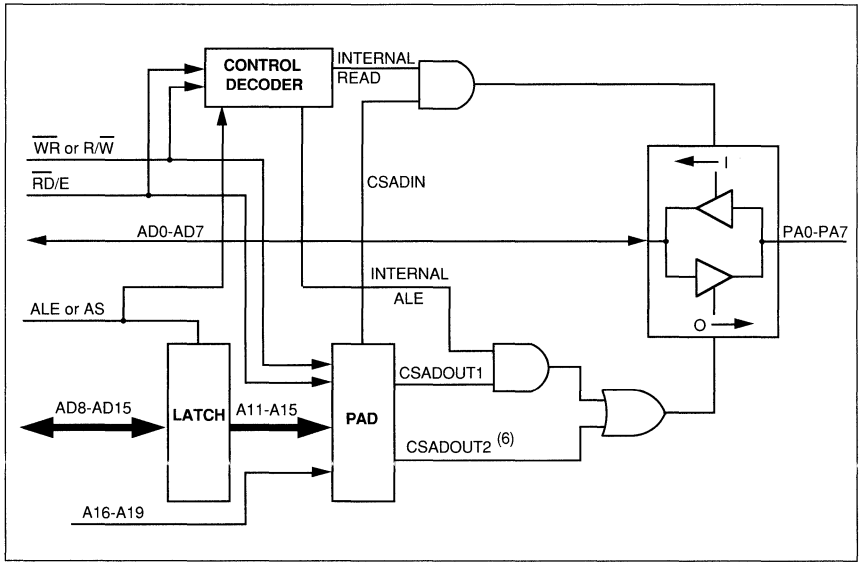
The PSD302 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 5. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 6. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD302 Configuration Bits[7,8]

Configuration Bits	No. of Bits	Function
CDATA	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active HIGH or Active LOW CRESET = 0, Active low RESET CRESET = 1, Active high RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CPAF1	8	Port A I/O or A0–A7 CPAF1 = 0, Port A pin is I/O CPAF1 = 1, Port A pin is Ai ($0 \le i \le 7$)
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CSI}$ ($0 \le i \le 7$) CPBF = 1, Port B pin is I/O

Table 5. PSD302 Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is Ai (16 ≤ i ≤ 18) CPCF = 1, Port C pin is $\overline{CSi}$ (8 ≤ i ≤ 10)
CADLOG	4	A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSi}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSi}$ is Ai (16 ≤ i ≤ 19)
Total Bits	**51**	

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

2

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD302 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figures 22 and 23). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E/$\overline{DS}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD302 location, data is presented on Port A pins. When writing to an internal PSD302 location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal PSD302 high-order data bus byte location, the data is presented on Port B pins. When writing to an internal PSD302 high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

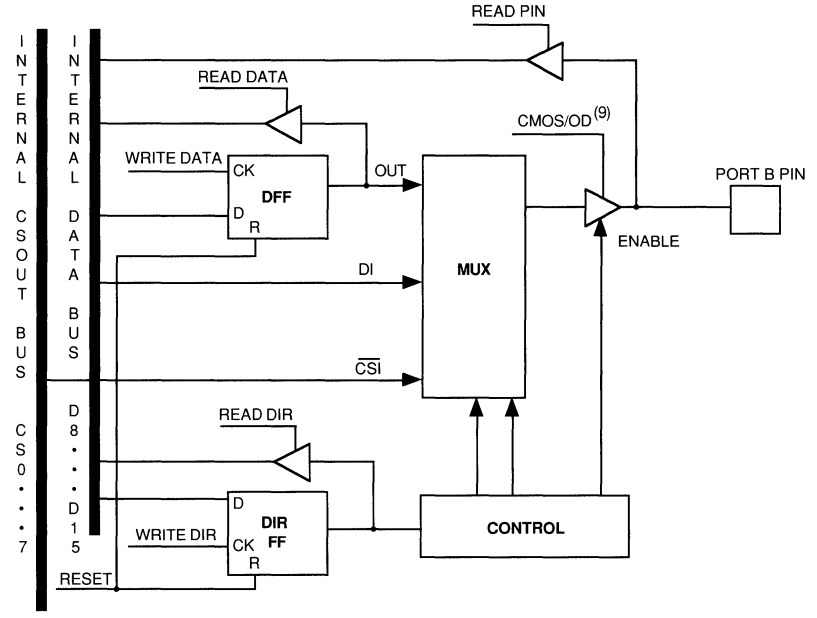
Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.



NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Table 7. I/O Port Addresses in an 16-bit Data Bus Mode[10,11]

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 10. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
11. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

EPROM

The PSD302 has 512K bits of EPROM. Depending on the configuration of the data bus, the EPROM can be organized as 64K x 8 (8-bit data bus) or as 32K x 16 (16-bit data bus). The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 8K x 8 (8-bit data bus) or as 4K x 16 (16-bit data bus).

SRAM

The PSD302 has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Page Register

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Control Signals

The PSD302 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

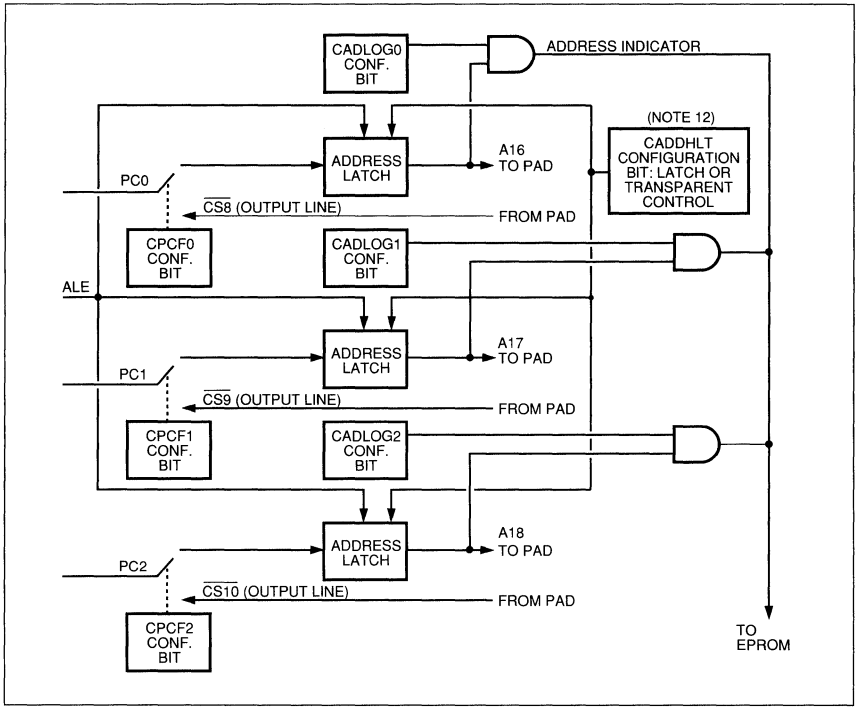
In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD302 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations to the PSD302 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

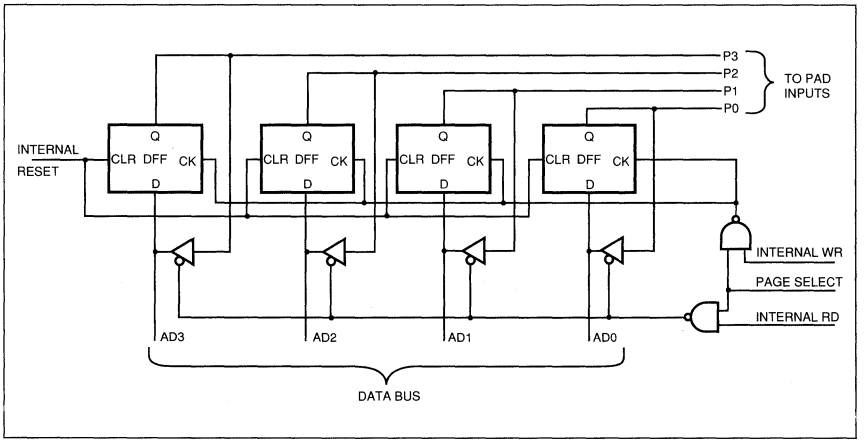
As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

Figure 7. Port C Structure



NOTE: 12. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Figure 8. Page Register



Control Signals (Cont.)

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}$/$\overline{PSEN}$

This pin's function depends on the PSD302 data bus width. If it is 8, the pin is $\overline{PSEN}$; if it is 16, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Figure 9. Combined Address Space

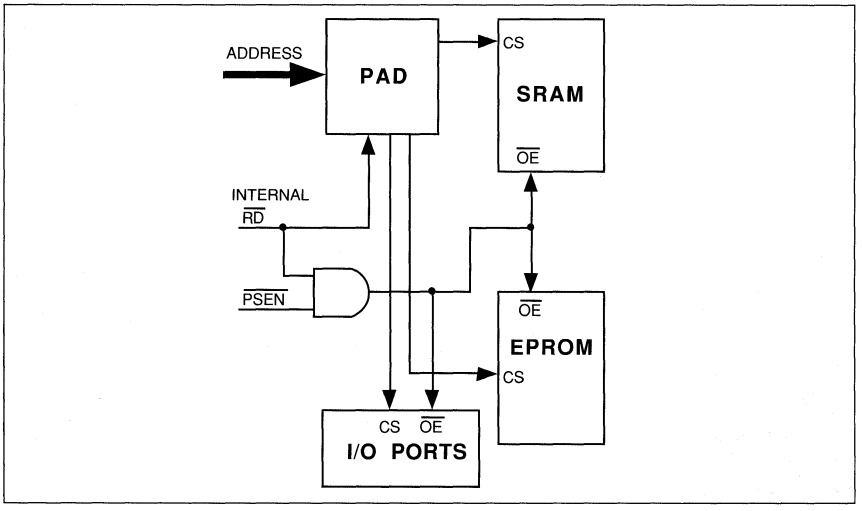
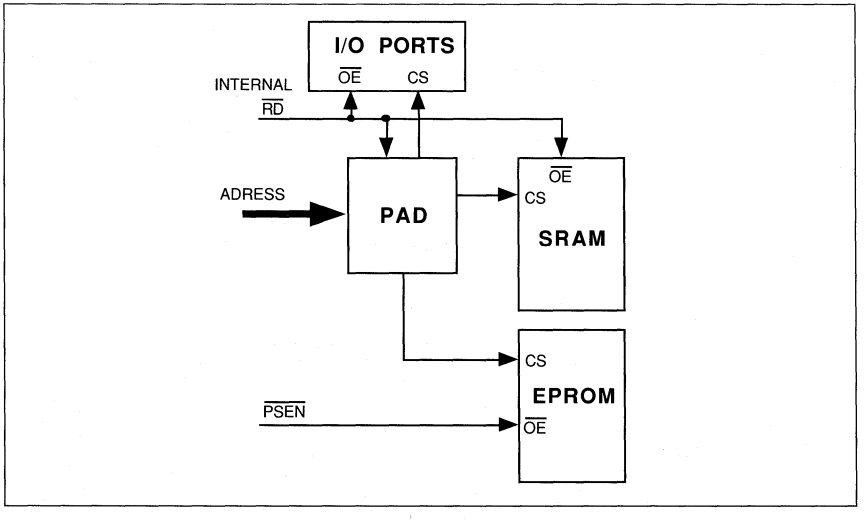


Figure 10. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

BHE/PSEN

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD302's PSEN pin must be connected to the PSEN pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the PSEN pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by RD low (CRRWR = 0), or by E high and R/W high (CRRWR = 1, CEDS = 0) or by DS low and R/W high (CRRWR, CEDS = 1). See Figures 9 and 10.

In BHE mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
BHE/PSEN	CDATA = 0	8-bit data, PSEN is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, BHE is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, BHE is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD302. Reset polarity is programmable (active low or active high). Whenever the PSD302 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 10 and 11 indicate the state of the part during and after reset.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD302 states during the power-down mode, see Tables 12 and 13, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Table 10. Signal States During and After Reset

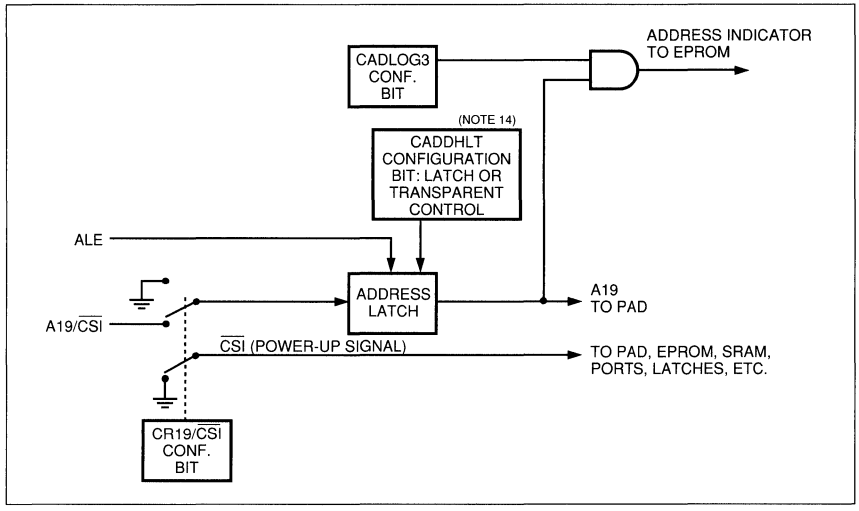
Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 13)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 13. All PAD outputs are in a non-active state.

Figure 11. A19/CSI Cell Structure



NOTES: 14. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

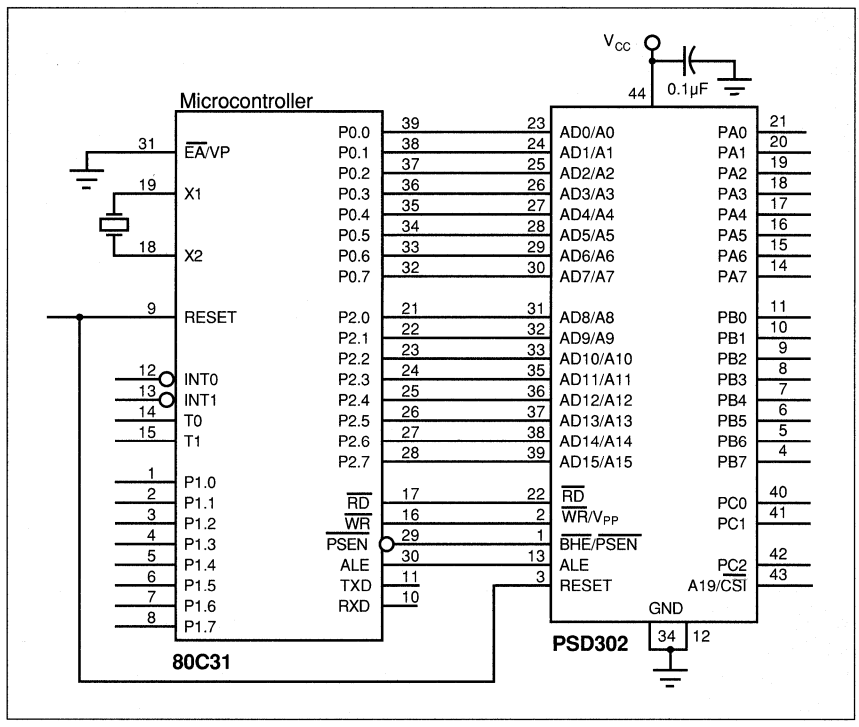
Table 12. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 12. PSD302 Interface With Intel's 80C31



The configuration bits for Figure 12 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Security Mode

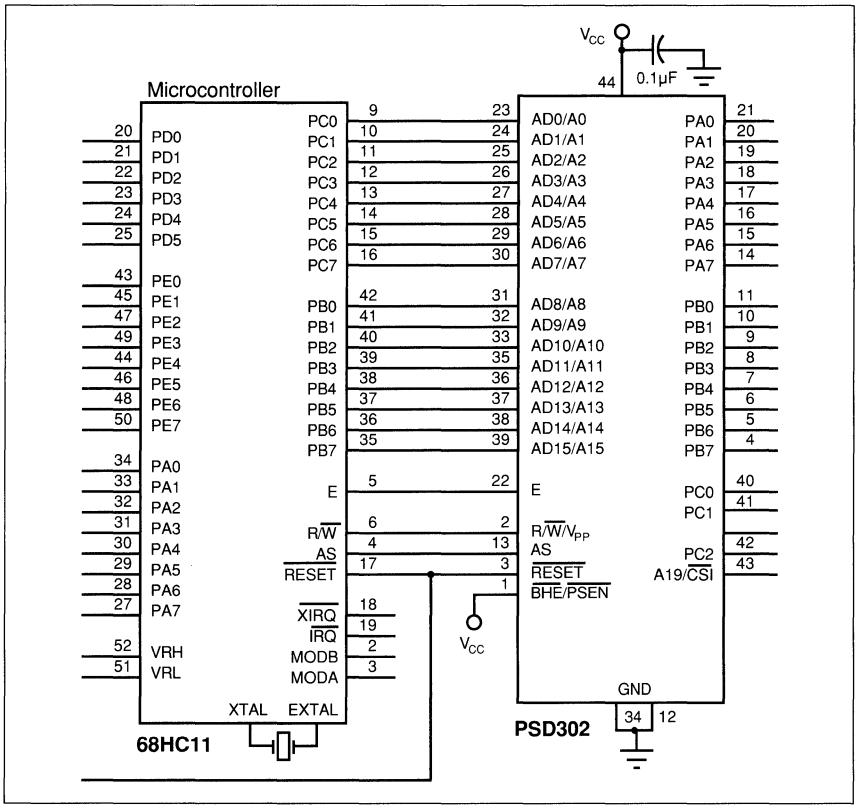
Security Mode in the PSD302 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD302 contents cannot be copied on a programmer.

System Applications

In Figure 12, the PSD302 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD302 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 13. PSD302 Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

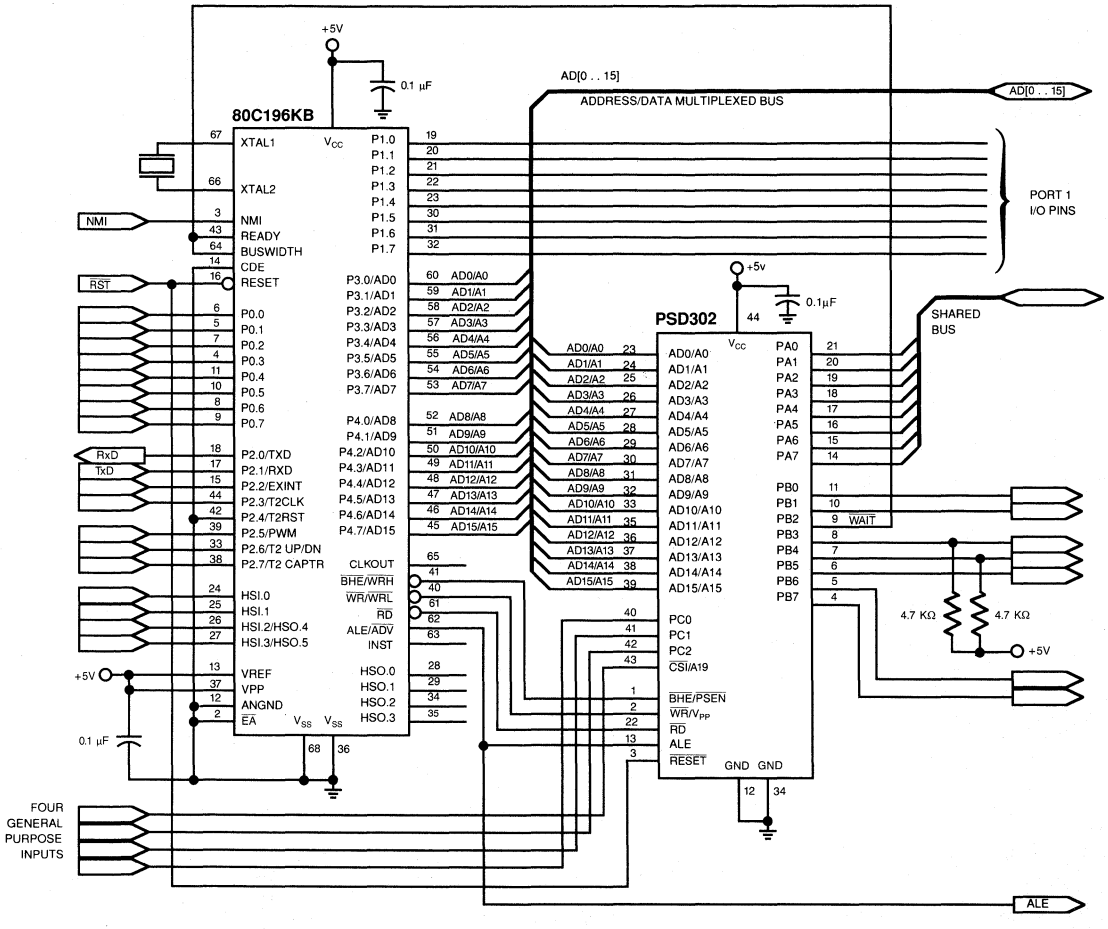
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 14, the PSD302 is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD302 is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 14. PSD302 Interface With Intel's 80C196KB.



The configuration bits for Figure 14 are:

CRESET	0	CSECURITY	Don't care
CALE	0	CPCF2, CPCF1, CPCF0	0, 0, 0
CDATA	1	CPACOD7–CPACOD0	00H
CADDRDAT	1	CPBF7–CPBF0	00H
CPAF1	Don't care	CPBCOD7–CPBCOD0	18H
CPAF2	1	CEDS	0
CA19/$\overline{CSI}$	1	CADLOG3—CADLOG0	0H
CRRWR	0		
COMB/SEP	0		
CADDHLT	0		

Absolute Maximum Ratings[15]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 15. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 16 and 18)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 17 and 18)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 16 and 19)	Comm'l (Note 20)		16	35	mA
		Comm'l (Note 21)		28	50	
		Ind/Mil (Note 20)		16	45	
		Ind/Mil (Note 21)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 16 and 19)	Comm'l (Note 20)		47	80	mA
		Comm'l (Note 21)		59	95	
		Ind/Mil (Note 20)		47	100	
		Ind/Mil (Note 21)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 17 and 19)	Comm'l (Note 20)		36	65	mA
		Comm'l (Note 21)		58	80	
		Ind/Mil (Note 20)		36	80	
		Ind/Mil (Note 21)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 17 and 19)	Comm'l (Note 20)		67	105	mA
		Comm'l (Note 21)		79	120	
		Ind/Mil (Note 20)		67	130	
		Ind/Mil (Note 21)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 16. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
17. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
18. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
19. AC power component is 3.0 mA/MHz (power = AC + DC).
20. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
21. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

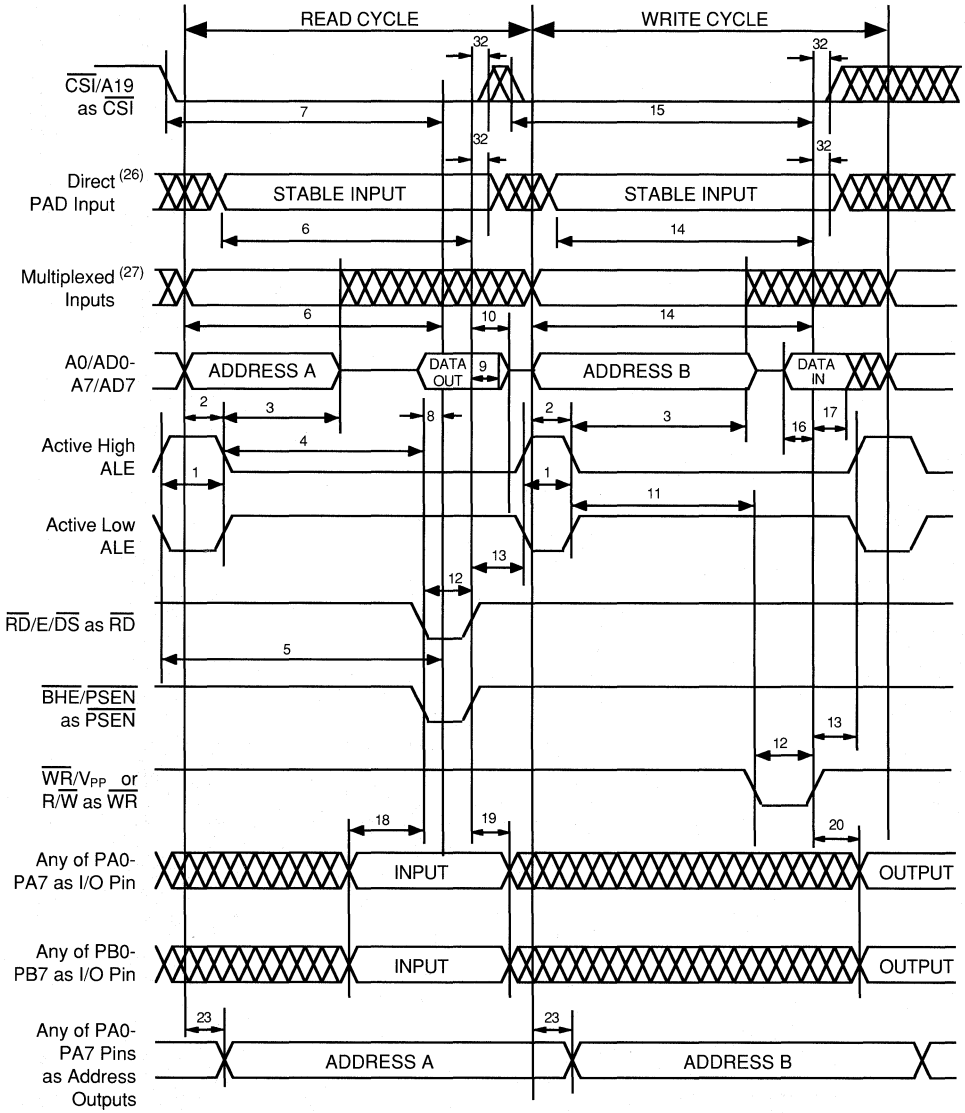
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	9		12		15		
T3	Address Hold Time	9		12		15		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	130		140		170		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		130		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		32		35		40	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ pulse width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		200		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	40	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	40	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		28		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		50		50	
T24	Track Mode Address Holding Time	15		27		27		
T25	Track Mode Read Propagation Delay		29		35		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		30		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	55	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	55	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E high	15		20		25		

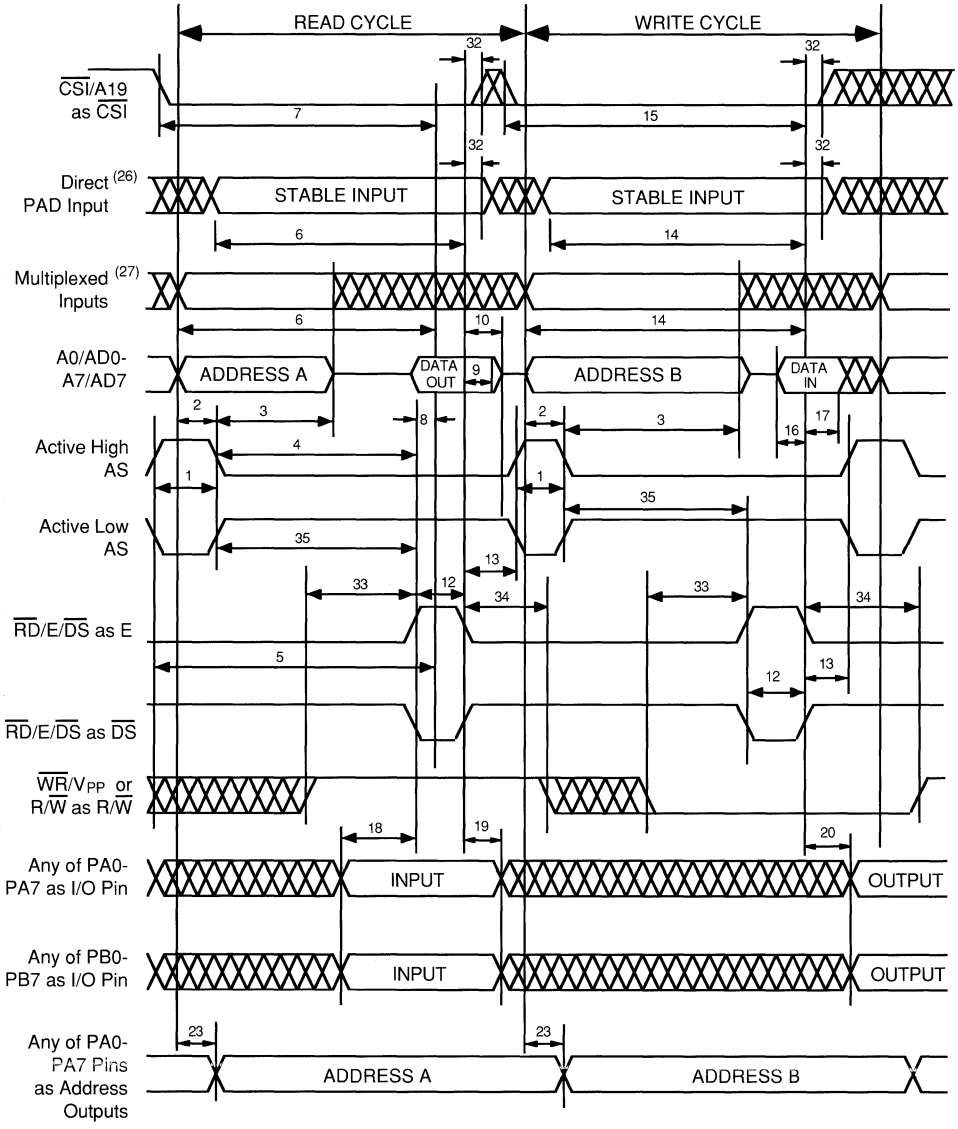
NOTES: 22. ADi = any address line.
23. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
24. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
25. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 15. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



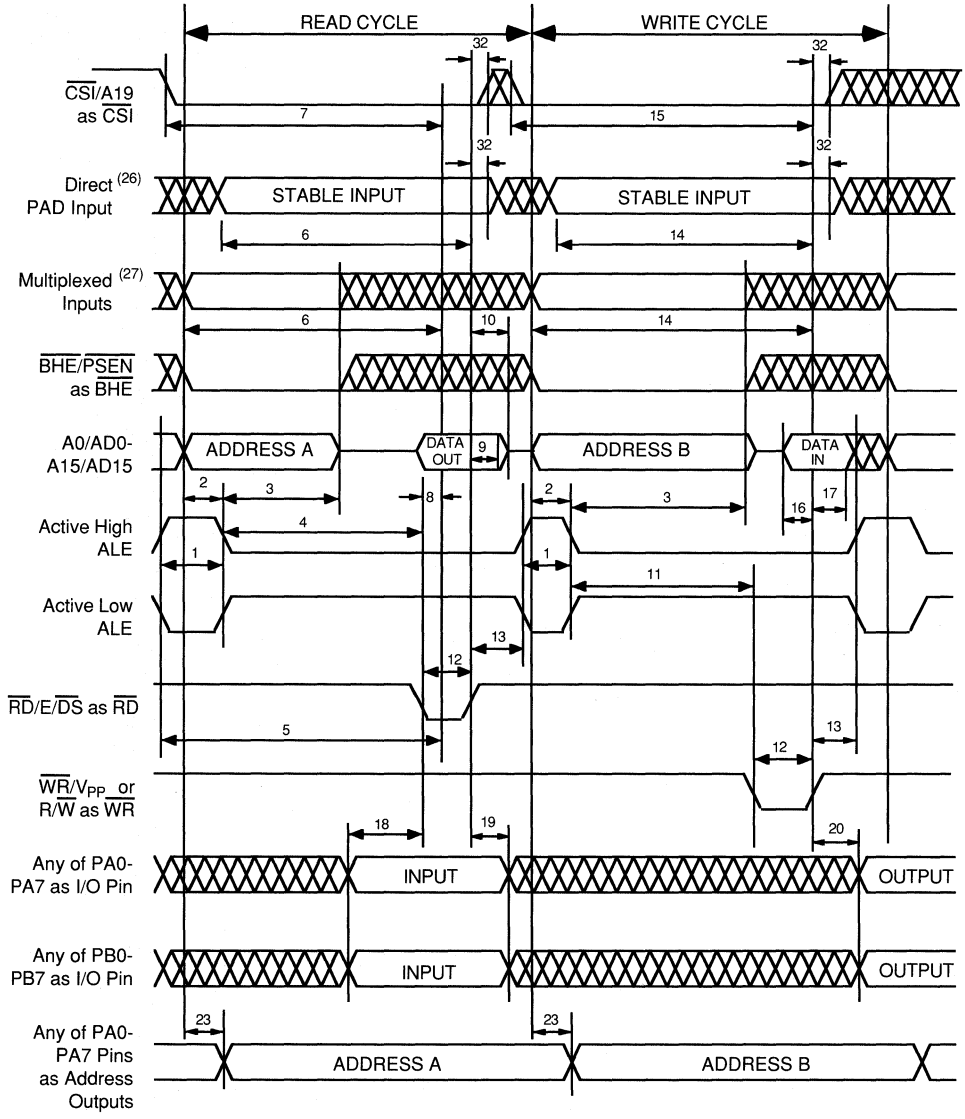
See referenced notes on page 2-119.

Figure 16. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



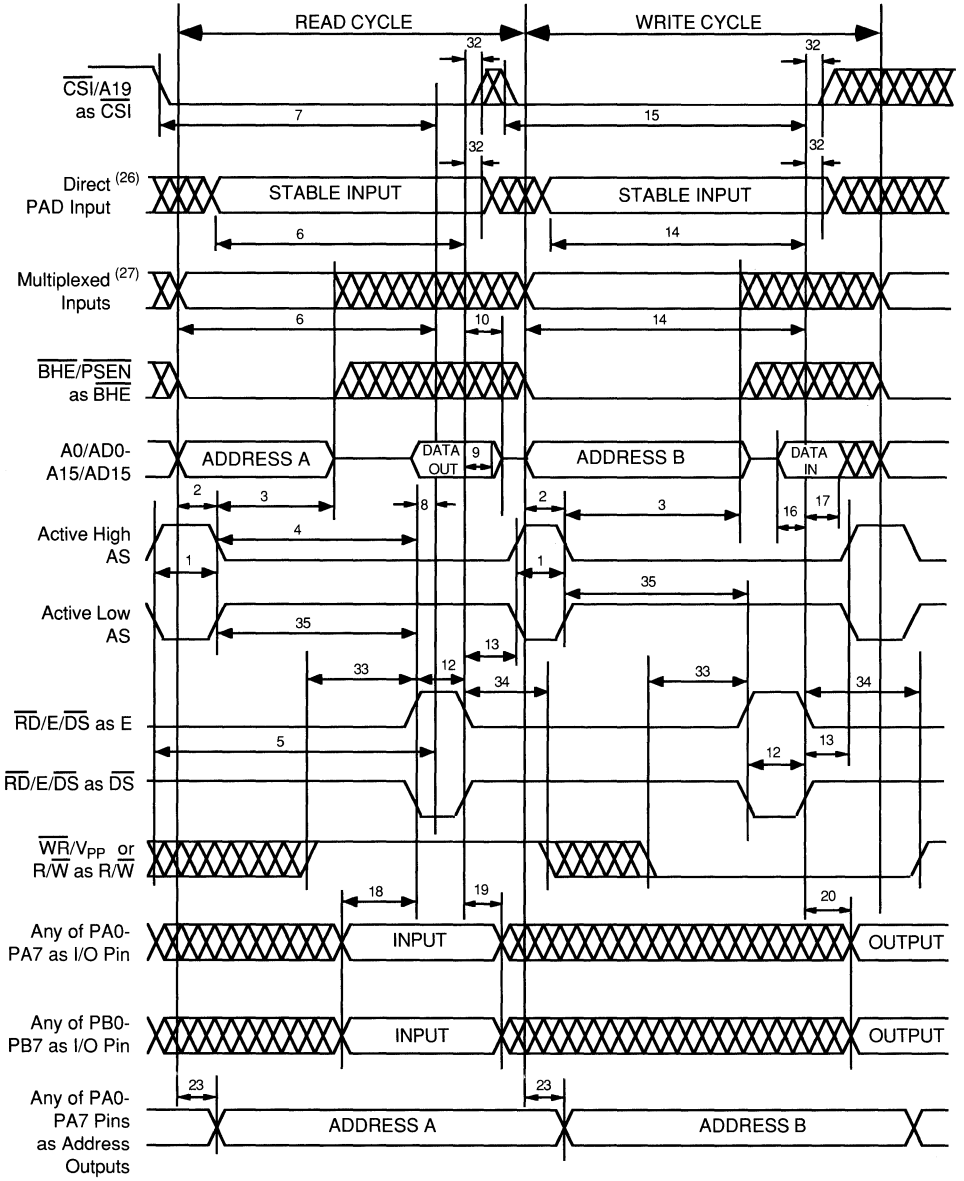
See referenced notes on page 2-119.

Figure 17. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



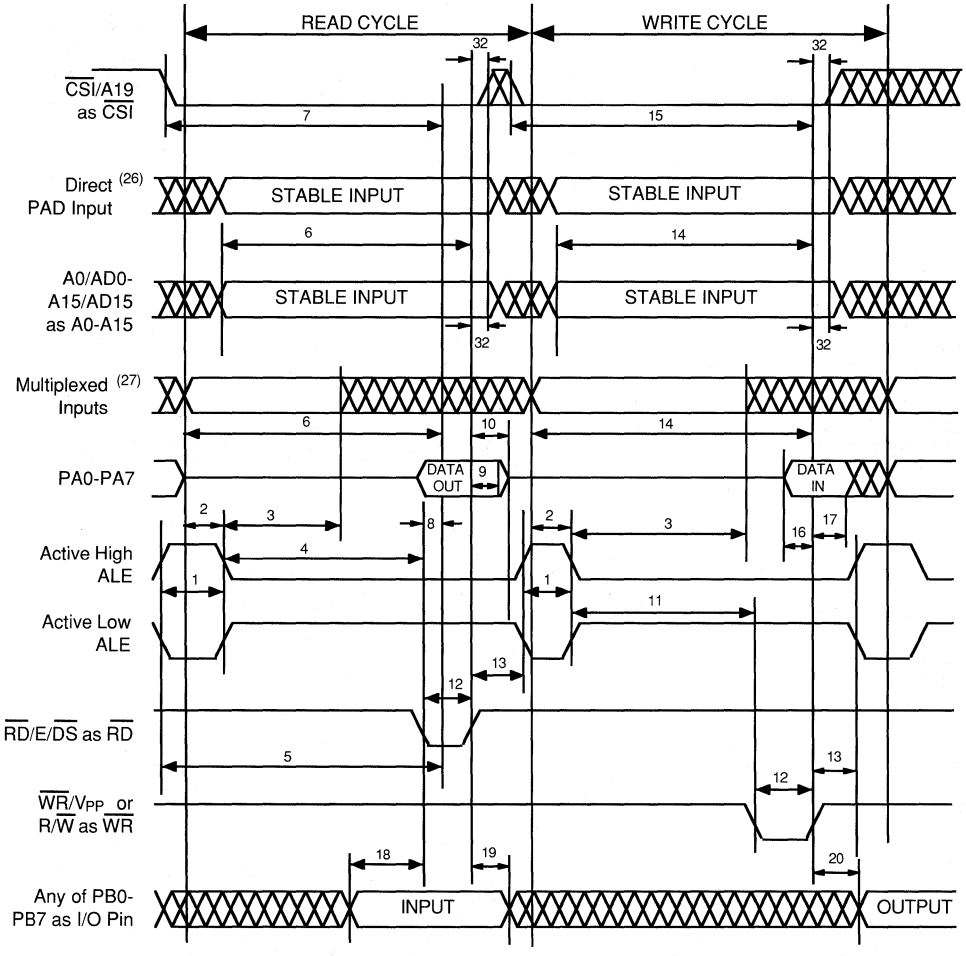
See referenced notes on page 2-119.

Figure 18. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



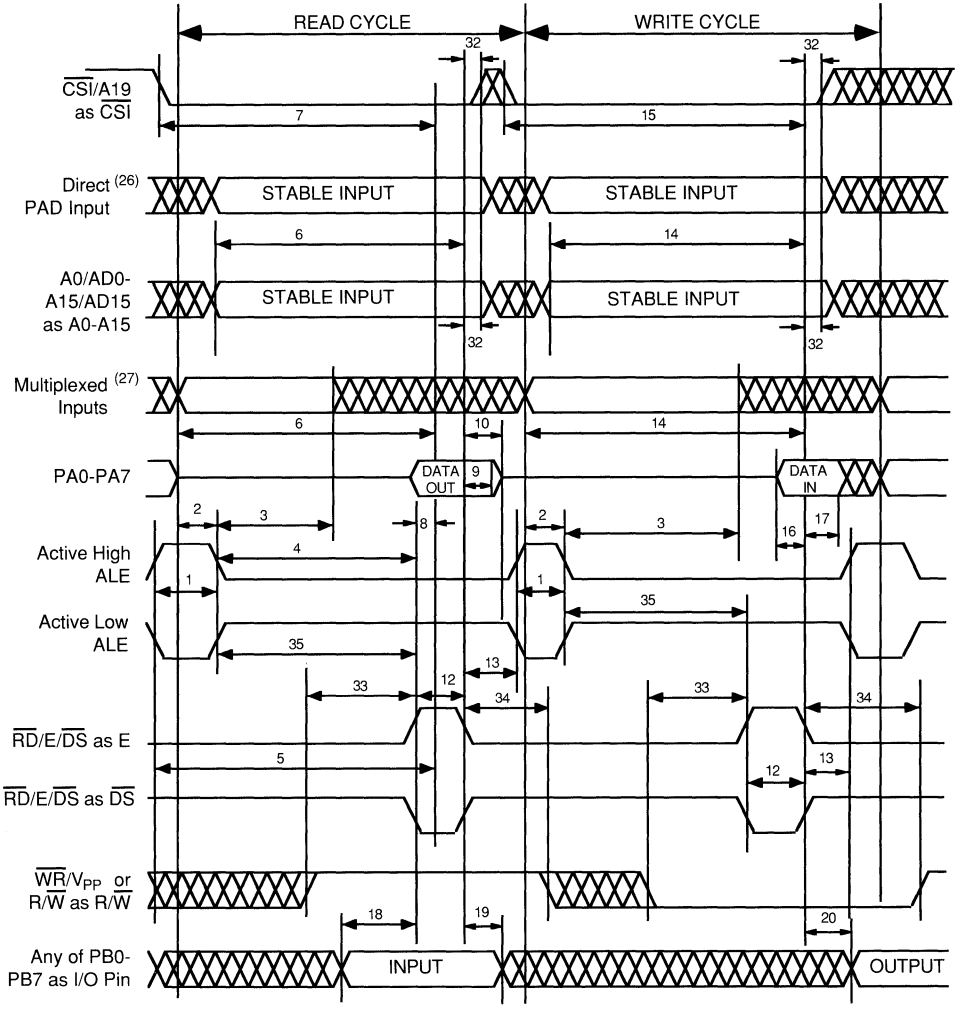
See referenced notes on page 2-119.

Figure 19. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



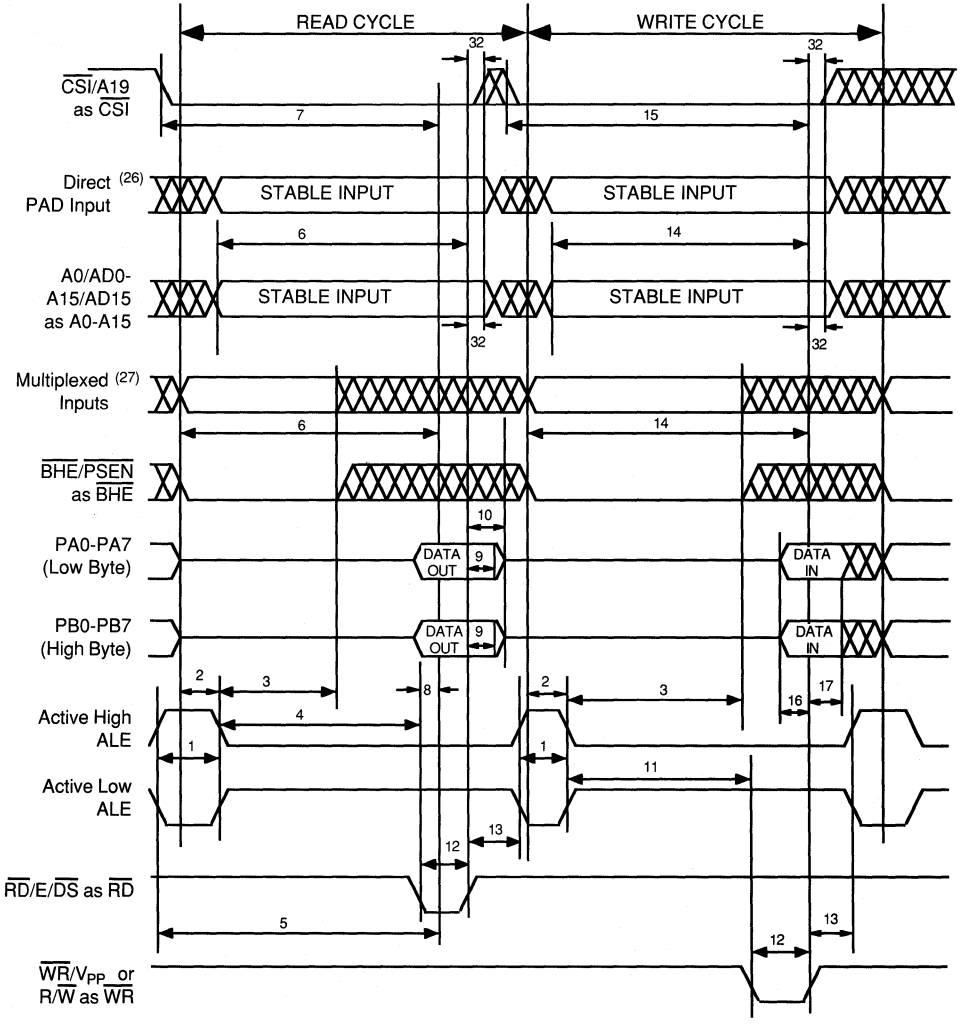
See referenced notes on page 2-119.

Figure 20. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



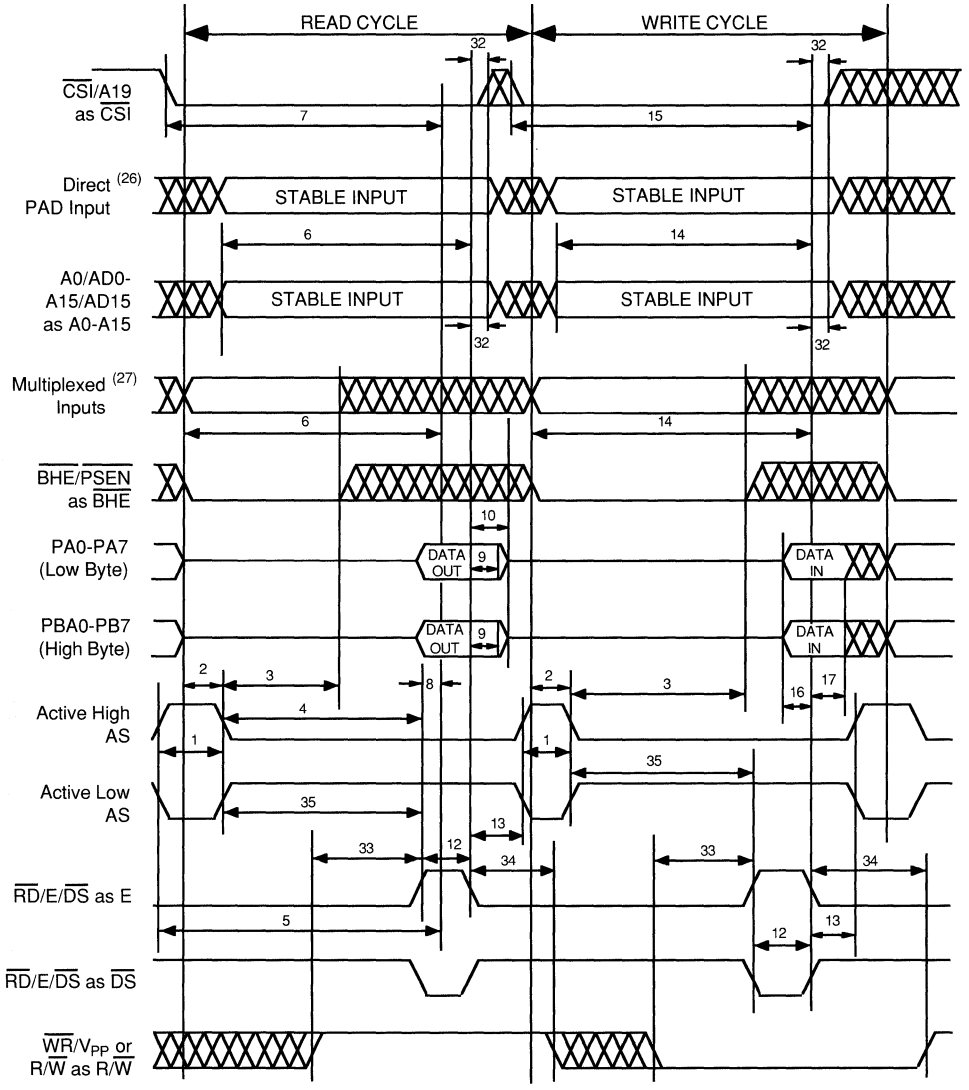
See referenced notes on page 2-119.

Figure 21. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-119.

Figure 22. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-119.

Figure 23. Chip-Select Output Timing

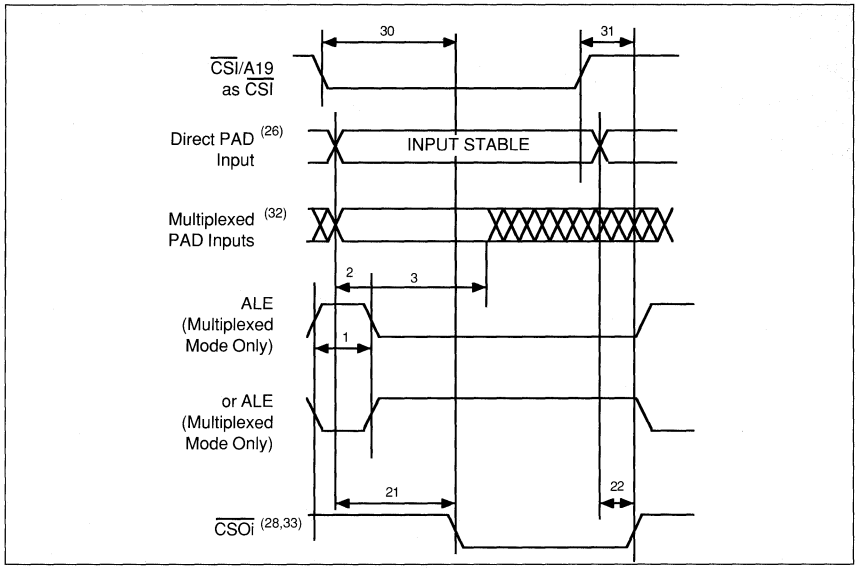
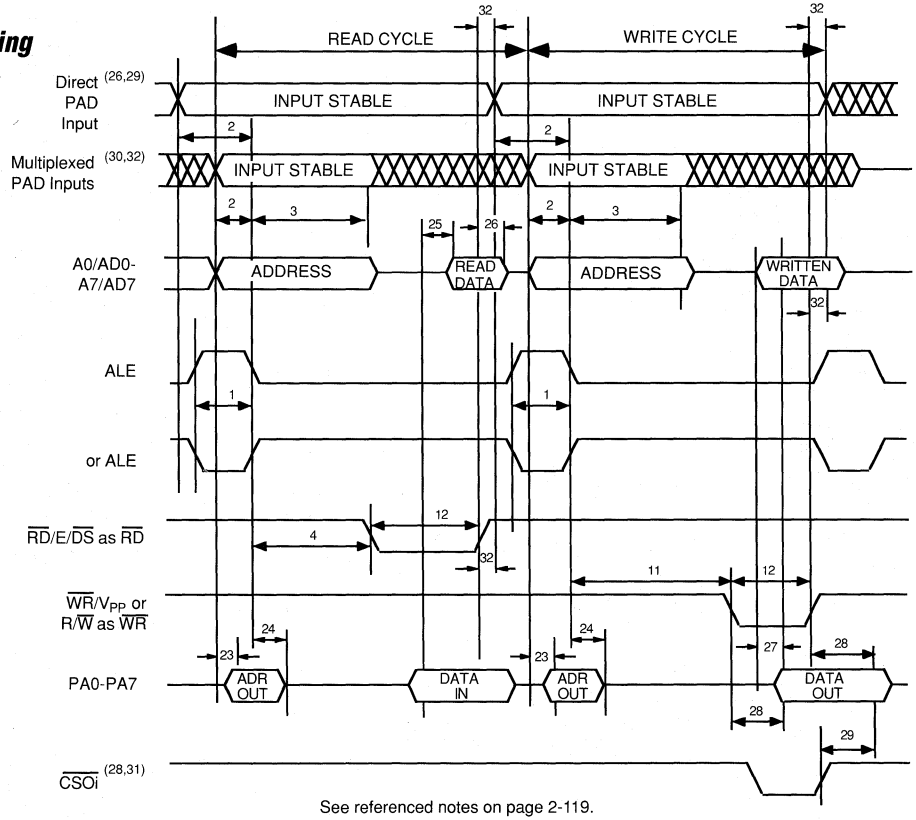
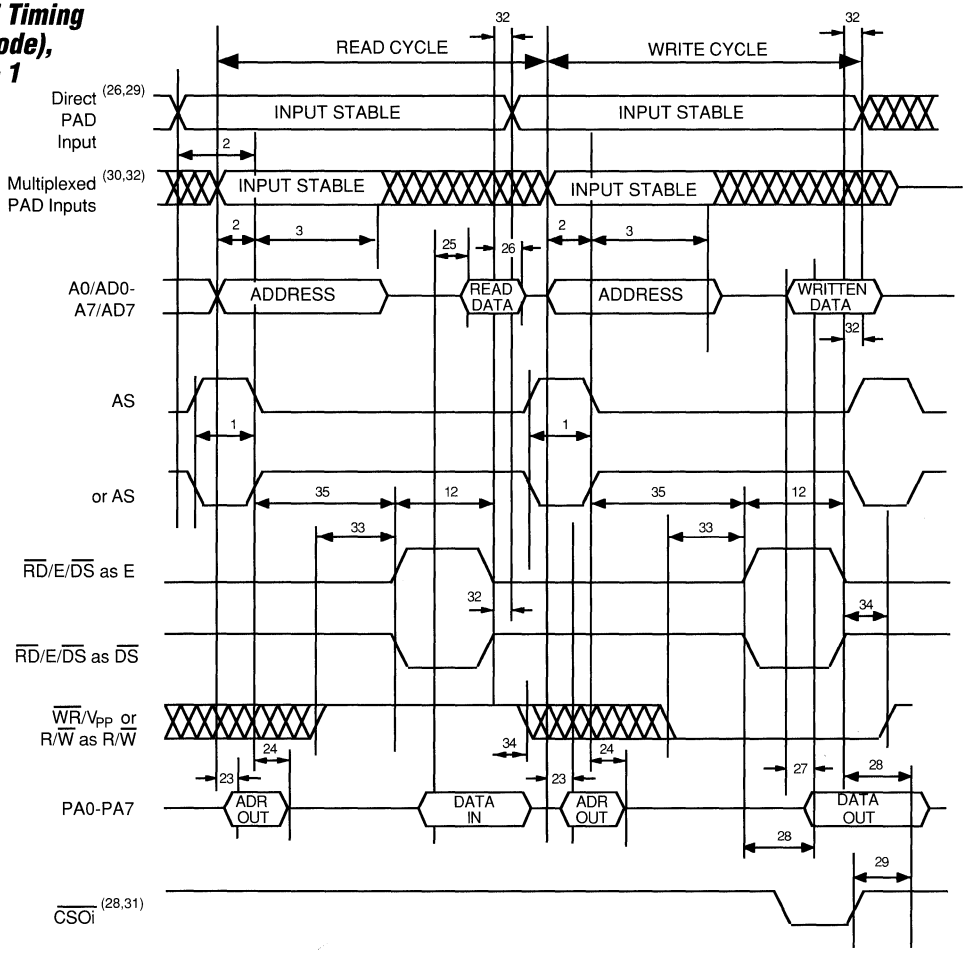


Figure 24. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-119.

Figure 25. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

26. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
27. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
28. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
29. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
30. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
31. The write operation signals are included in the $\overline{CSOi}$ expression.
32. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
33. $\overline{CSOi}$ product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 14. Pin Capacitance[34]

$T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Conditions	Typical[35]	Max	Unit
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 34. This parameter is only sampled and is not 100% tested.
35. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Figure 26. AC Testing Input/Output Waveform

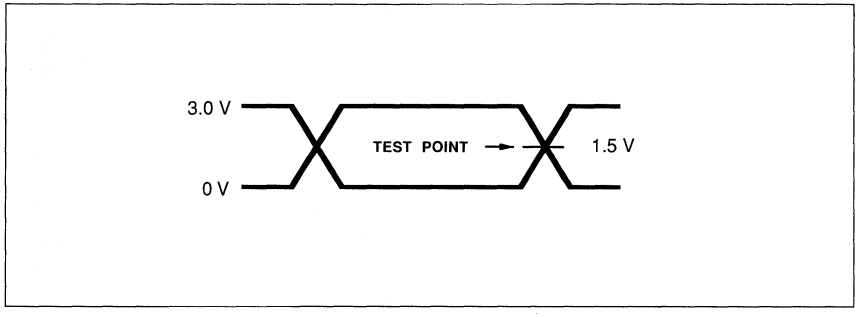
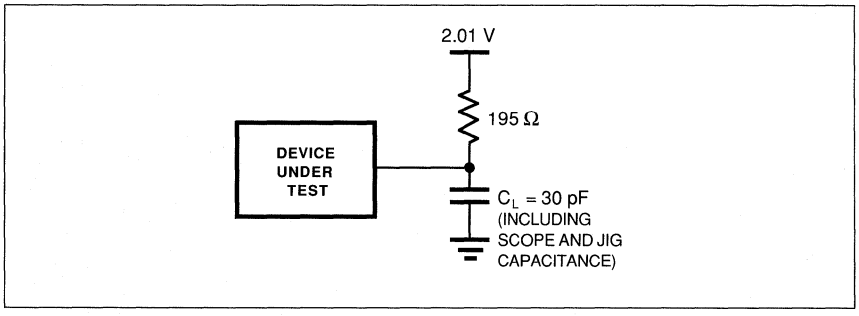


Figure 27. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 μW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD302 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD302 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{BHE}/\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}/E/\overline{DS}$	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
AD8/A8	31	F_7	30
AD9/A9	32	F_8	31
AD10/A10	33	E_7	32
GND	34	E_8	33
AD11/A11	35	D_8	34
AD12/A12	36	D_7	35
AD13/A13	37	C_8	36
AD14/A14	38	C_7	37
AD15/A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

NOTE: 36. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 28. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

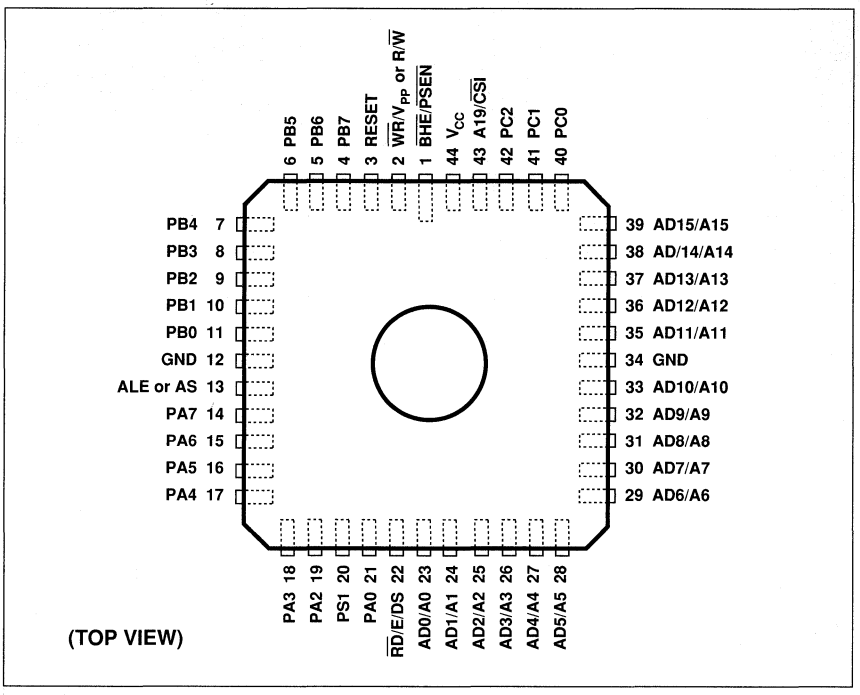


Figure 29. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

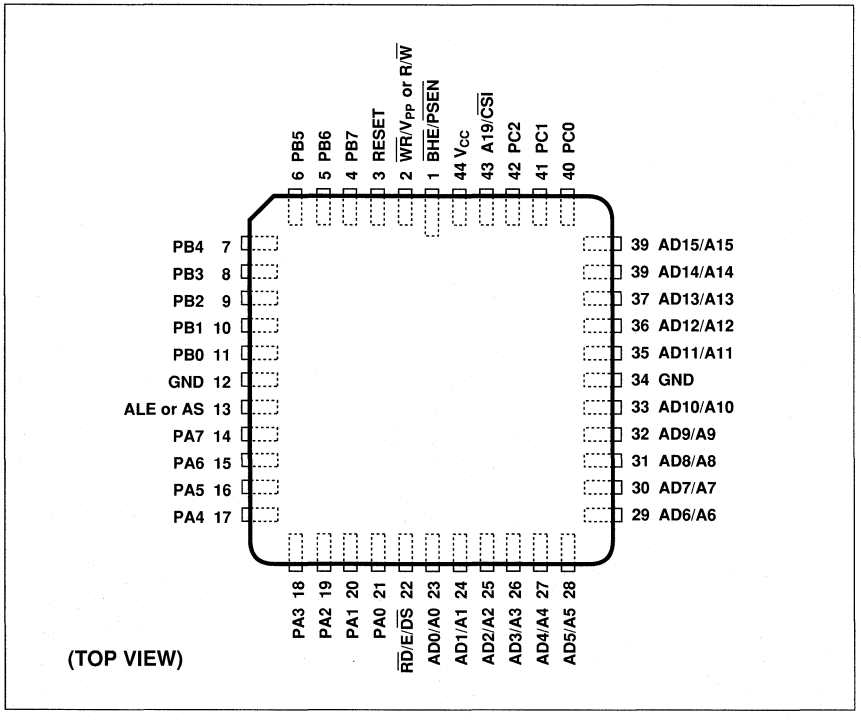


Figure 30. Drawing Q2 — 52-Pin PQFP (Package Type Q)

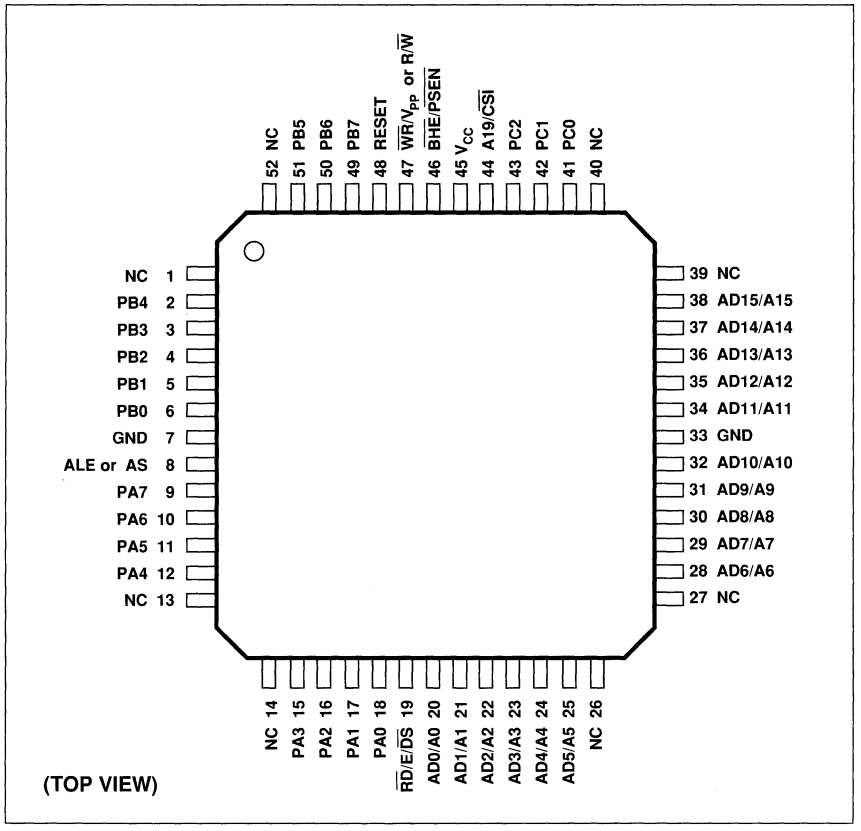
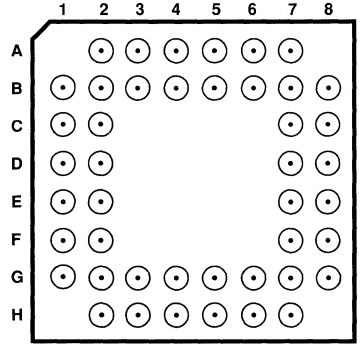


Figure 31: Drawing X2 — 44-Pin CPGA (Package Type X)



(TOP VIEW, THROUGH PACKAGE)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD302-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD302-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD302-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD302-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD302-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD302-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD302-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD302-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD302-15LM	150	44-pin CLDCC	L4	Military	Standard
PSD302-15LMB	150	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD302-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD302-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD302-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD302-15XM	150	44-pin CPGA	X2	Military	Standard
PSD302-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD302-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD302-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD302-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD302-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD302-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD302-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD302-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD302-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD302-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD302-20XM	200	44-pin CPGA	X2	Military	Standard
PSD302-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

PSD302
System Development Tools

System Development Tools

The PSD302 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD302 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD302 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6020 52-pin PSD302 PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD302 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD302 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD302 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD302 device, which then can be used in the target system. The development cycle is depicted in Figure 32.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD302 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD302 Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6020
- ❑ 52-pin PQFP Package Adaptor. Used with the WS6000 MagicPro Programmer

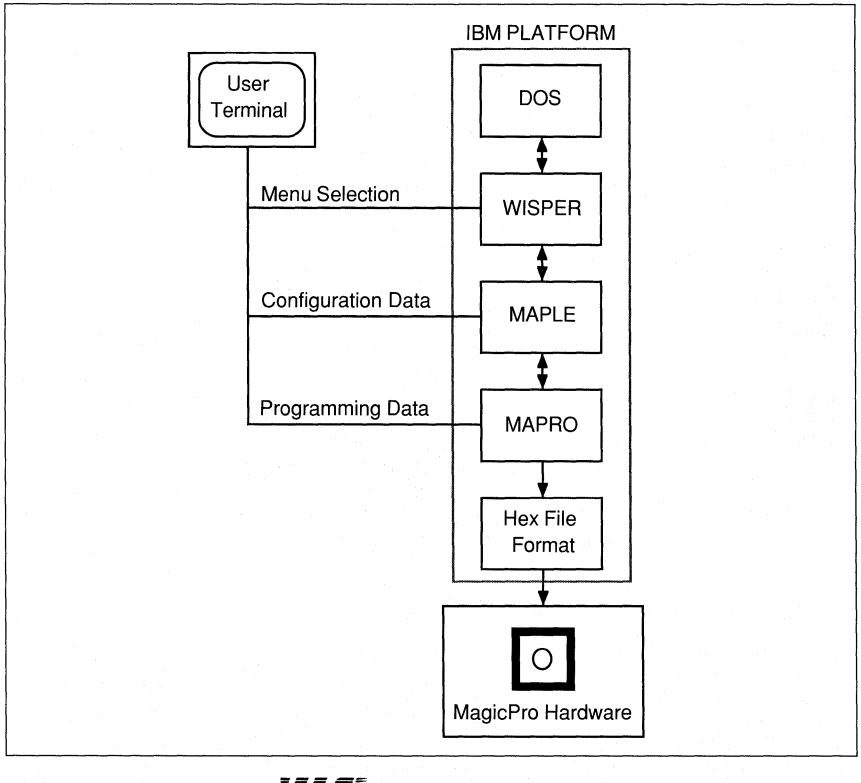
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA

Figure 32. PSD302 Development Cycle



Programmable Peripheral

PSD312

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — PSEN/ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 512 Kbits of UV EPROM
  - — Organized as 64K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 8K x 8
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Organized as 2K x 8
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD312 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 52 Pin PQFP
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD312 on an IBM PC
- ❑ Downward Pin and Functionally Compatible with the PSD301 in 8-bit Mode

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family**: 8031/8051, 8096/98, 80186/88, 80196/98
- ❑ **Signetics:** SC80C451
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD312 is the latest member in the rapidly growing WSI family of PSD devices. The PSD312 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumption are essential. When combined in a system, virtually any microcontroller (68HC11, 8051 etc.) and the PSD312 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD312 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD312 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 512K bits of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD312 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD312 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanding address space of microcontrollers

WSI's PSD312 (shown in Figure 1) can efficiently interface with, and enhance, any microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 512K bit EPROM, and 16K bit SRAM on a single chip. The PSD312 does not require any glue logic for interfacing to any 8-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD312's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD312 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD312 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (8K x 8 each) and SRAM (2K x 8) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

The page register extends the accessible address space of certain microcontrollers from 64K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line processors by a factor of 16.

Figure 1. PSD312 Architecture

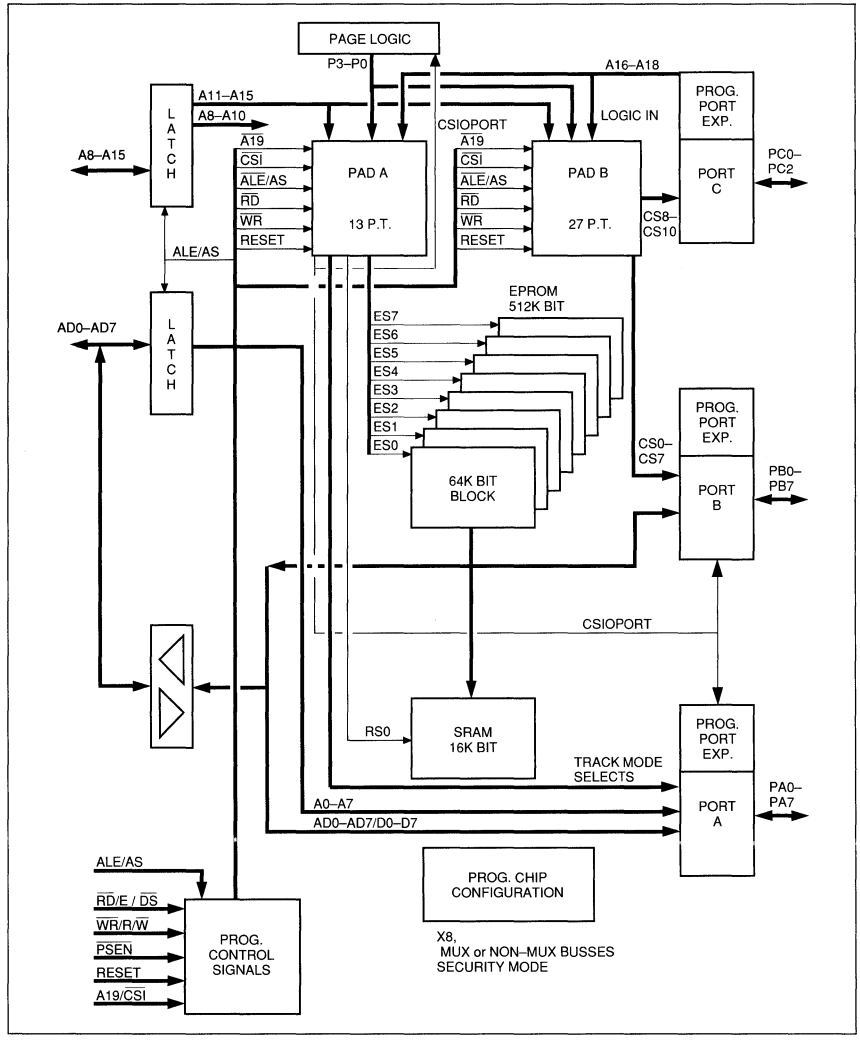


Table 1. PSD312 Pin Descriptions

Name	Type	Description
$\overline{PSEN}$	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E/$\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 1 | NOP 0 | 0 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E/$\overline{DS}$	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 10 and 11 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 8 and 9 for the chip state after reset.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD312 Pin Descriptions (Cont.)

Name	Type	Description
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD312 configuration. See Table 7. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.

Table 1. PSD312 Pin Descriptions (Cont.)

Name	Type	Description
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
A8 A9 A10 A11 A12 A13 A14 A15	I/O	These pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD312's two operating modes allow it to interface directly to 8-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are described below.

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bidirectional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address bus (A8–A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to a microcontroller with an 8-bit non-multiplexed bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (A8–A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

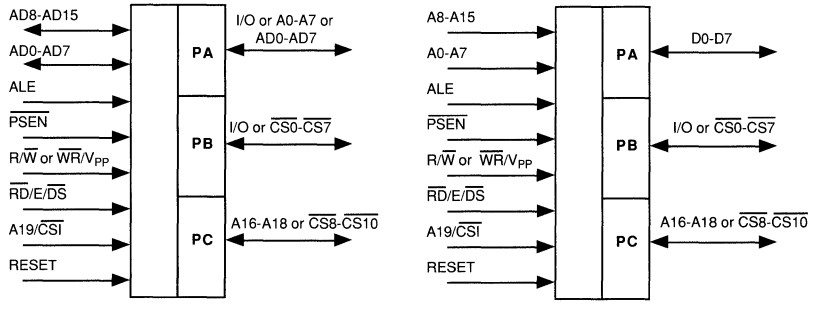
Programmable Address Decoder (PAD)

The PSD312 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 2. PSD312 Port Configurations

Figure 2 shows the PSDS312's I/O port configurations.



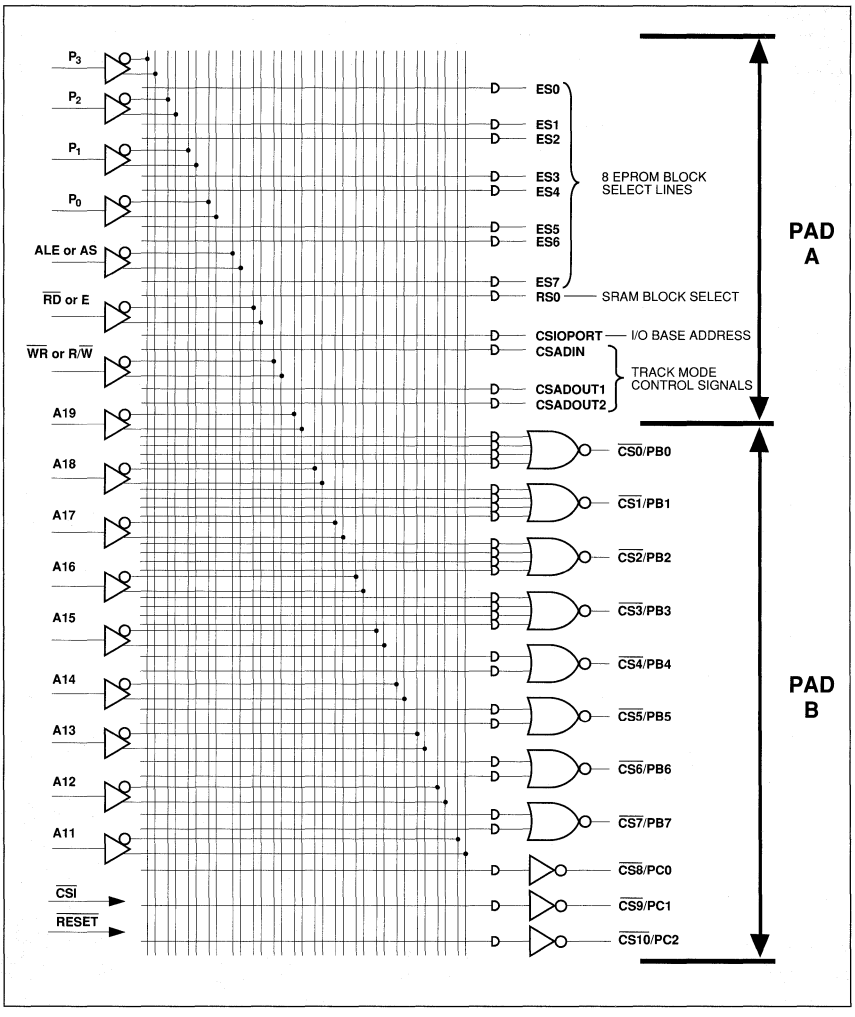
1. PSD312 configured for multiplexed 16-bit address/data bus.
2. PSD312 configured for non-multiplexed address/data, 8-bit bus.

Legend: AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD312 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or CS0–CS7	I/O and/or CS0–CS7
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8—A15	High-order address bus byte	High-order address bus byte

Figure 3. PSD312 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 10 and 11.
3. RESET deselects all PAD output signals. See Tables 8 and 9.
4. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Table 3. PSD312 PAD A and B I/O Functions

Function	
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 10 and 11). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 8 and 9.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Table 6.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD312 MAPLE software to set the bits.

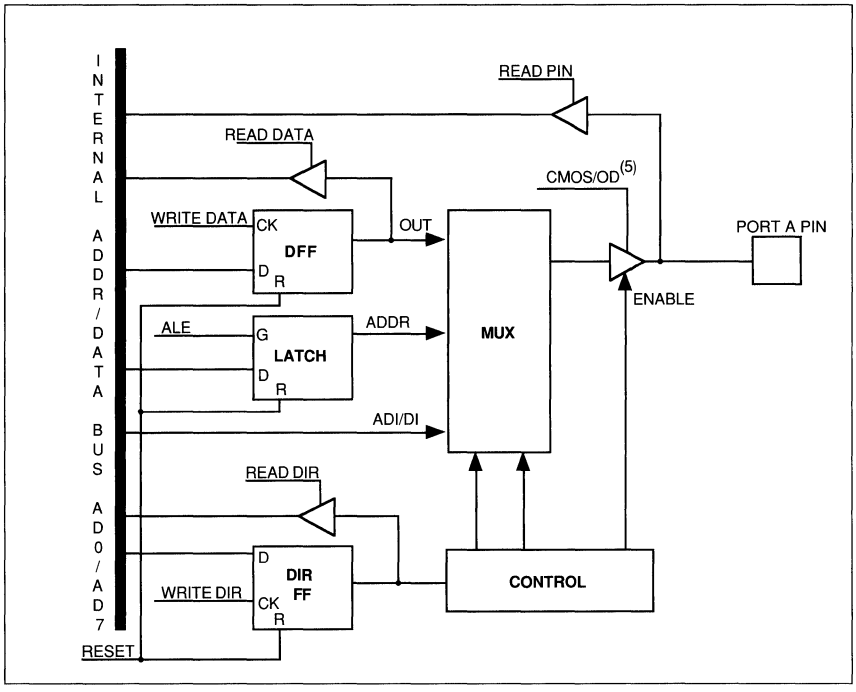
Table 4. PSD312 Non-Volatile Configuration Bits

Use This Bit	To
CADDRDAT	Set the address/data bus to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
COMB/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16–A19 individually as logic or address inputs.
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched.
CRRWR	Configure the polarity and control methods of read and write cycles.

Port Functions

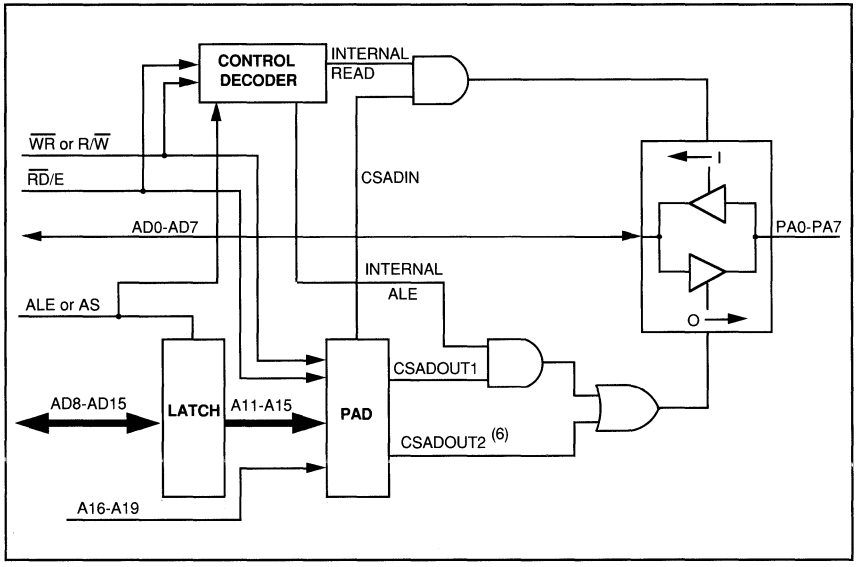
The PSD312 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 5. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 6. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD312 Configuration Bits[7,8]

Configuration Bits	No. of Bits	Function
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active HIGH or Active LOW CRESET = 0, Active low RESET CRESET = 1, Active high RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CPAF1	8	Port A I/O or A0–A7 CPAF1 = 0, Port A pin is I/O CPAF1 = 1, Port A pin is Ai ($0 \le i \le 7$)
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CSI}$ ($0 \le i \le 7$) CPBF = 1, Port B pin is I/O

Table 5. PSD312 Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is Ai ($16 \le i \le 18$) CPCF = 1, Port C pin is $\overline{CSI}$ ($8 \le i \le 10$)
CADLOG	4	A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is Ai ($16 \le i \le 19$)
Total Bits	**50**	

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

2

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD312 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figure 18). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E/$\overline{DS}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD312 location, data is presented on Port A pins. When writing to an internal PSD312 location, data present on Port A pins is written to that location.

Port B

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Accessing the I/O Port Registers

Table 6 shows the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

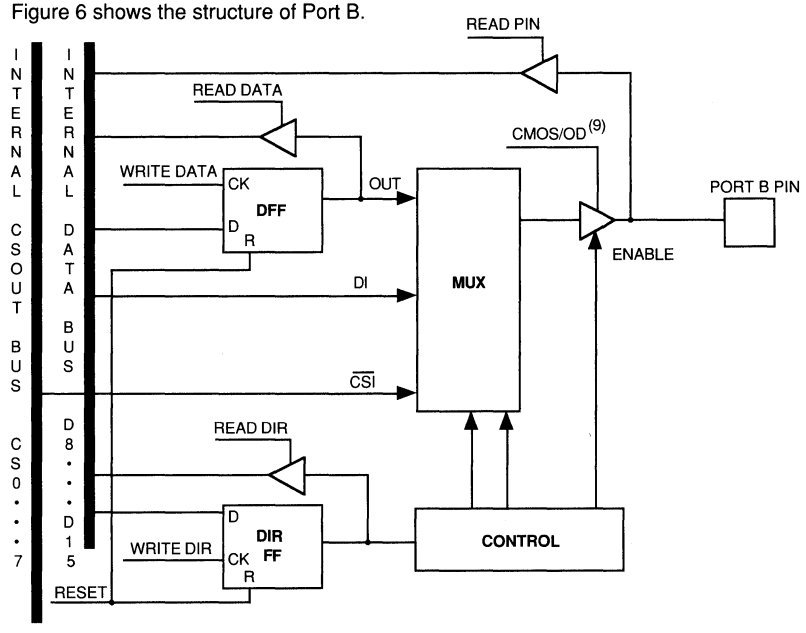
Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. See Table 7.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.

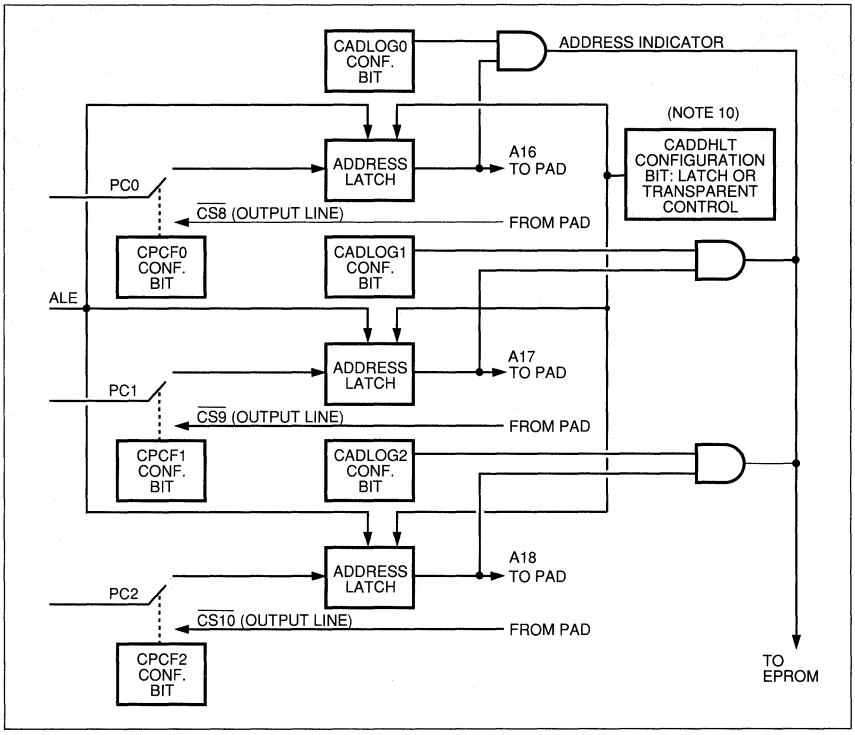


NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Figure 7. Port C Structure



NOTE: 10. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 7. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

EPROM

The PSD312 has 512K bits of EPROM and is organized as 64K x 8. The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 8K x 8.

SRAM

The PSD312 has 16K bits of SRAM and is organized as 2K x 8. The SRAM is selected by the RS0 output of the PAD.

Page Register

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Control Signals

The PSD312 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD312 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations to the PSD312 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin works with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{PSEN}$

The $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Control Signals (Cont.)

PSEN

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD312's PSEN pin must be connected to the PSEN pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the PSEN pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by RD low (CRRWR = 0), or by E high and R/W high (CRRWR = 1, CEDS = 0) or by DS low and R/W high (CRRWR, CEDS = 1). See Figures 9 and 10.

Figure 8. Page Register

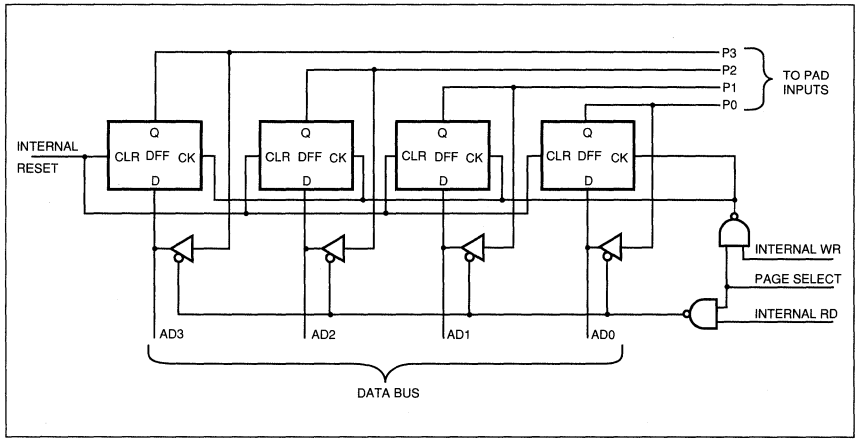


Table 8. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O CS7–CS0 CMOS outputs CS7–CS0 open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 CS8–CS10 CMOS outputs	Input High

Figure 9. Combined Address Space

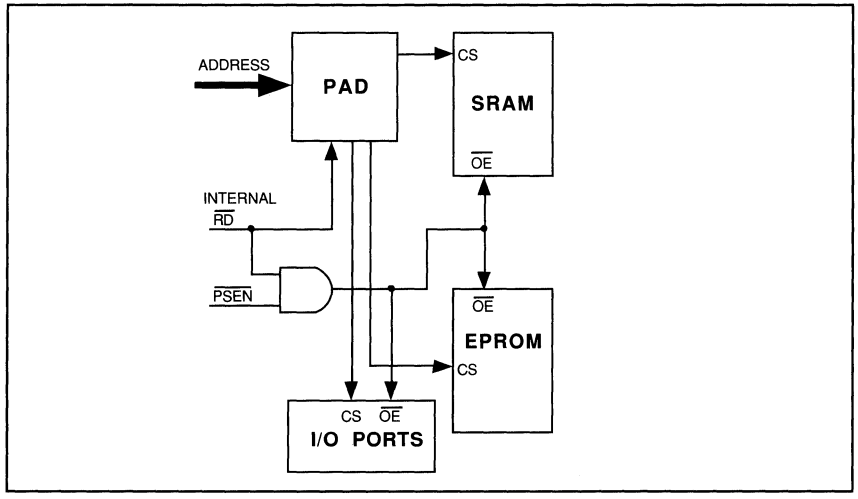
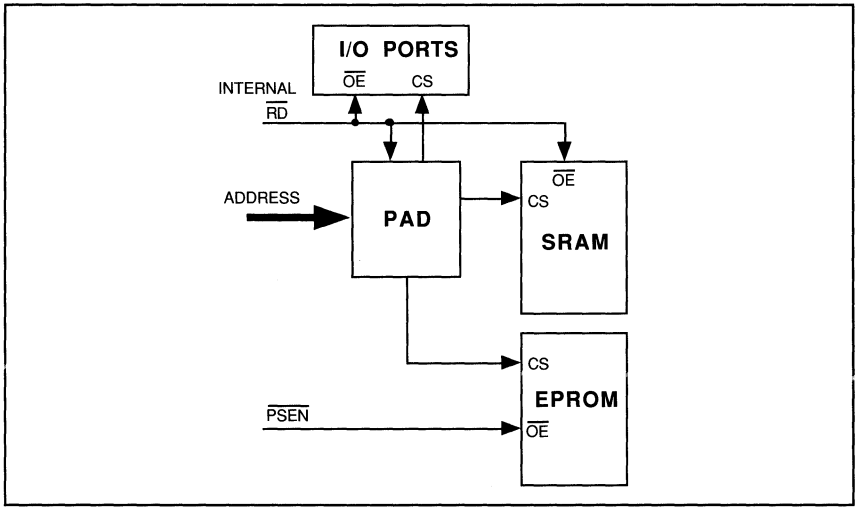


Table 9. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 11)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 11)
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 11. All PAD outputs are in a non-active state.

Figure 10. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD312. Reset polarity is programmable (active low or active high). Whenever the PSD312 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 8 and 9 indicate the state of the part during and after reset.

A19/$\overline{CSI}$

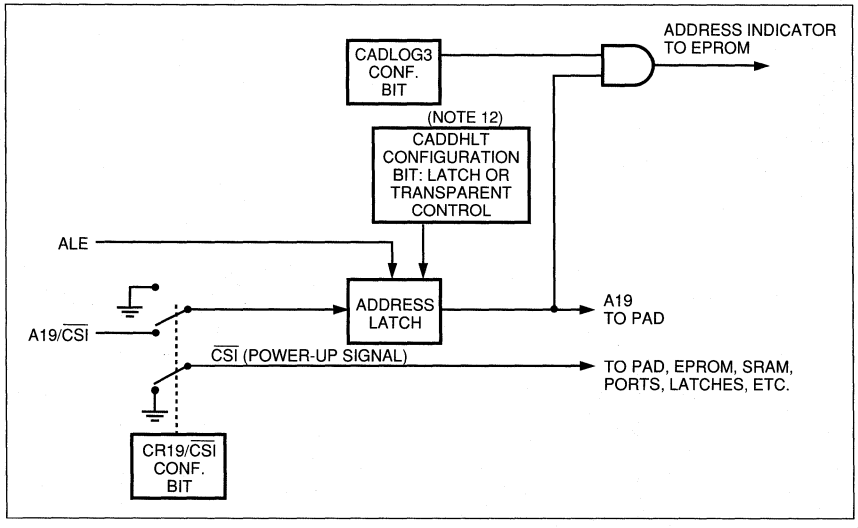
When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD312 states during the power-down mode, see Tables 10 and 11, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 7). In this mode, the chip is always enabled.

Table 10. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Figure 11. A19/$\overline{CSI}$ Cell Structure



NOTE: 12. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 11. Internal States During Power-Down

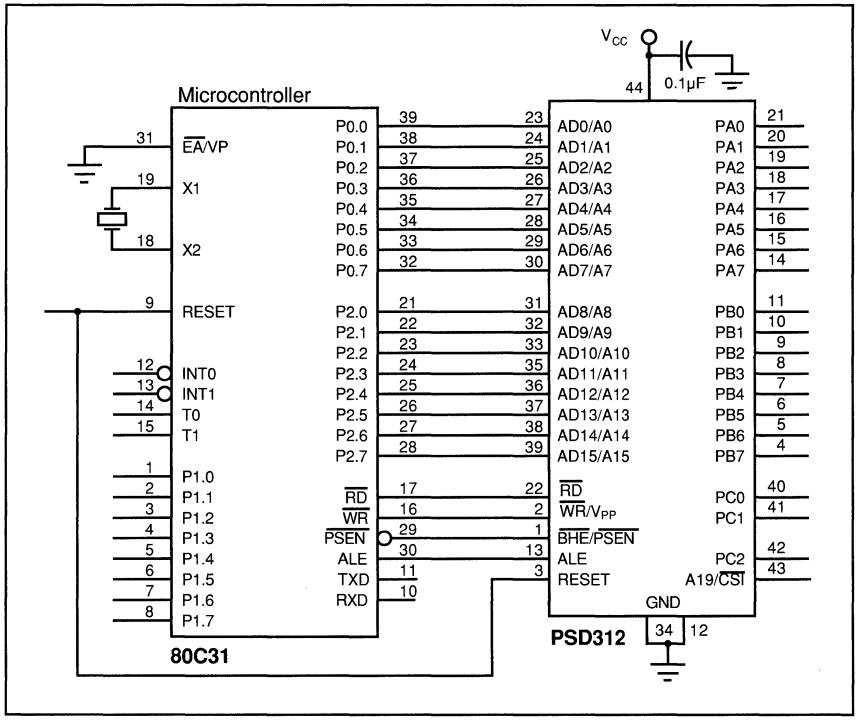
Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Security Mode

Security Mode in the PSD312 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD312 contents cannot be copied on a programmer.

2

Figure 12. PSD312 Interface With Intel's 80C31



The configuration bits for Figure 12 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

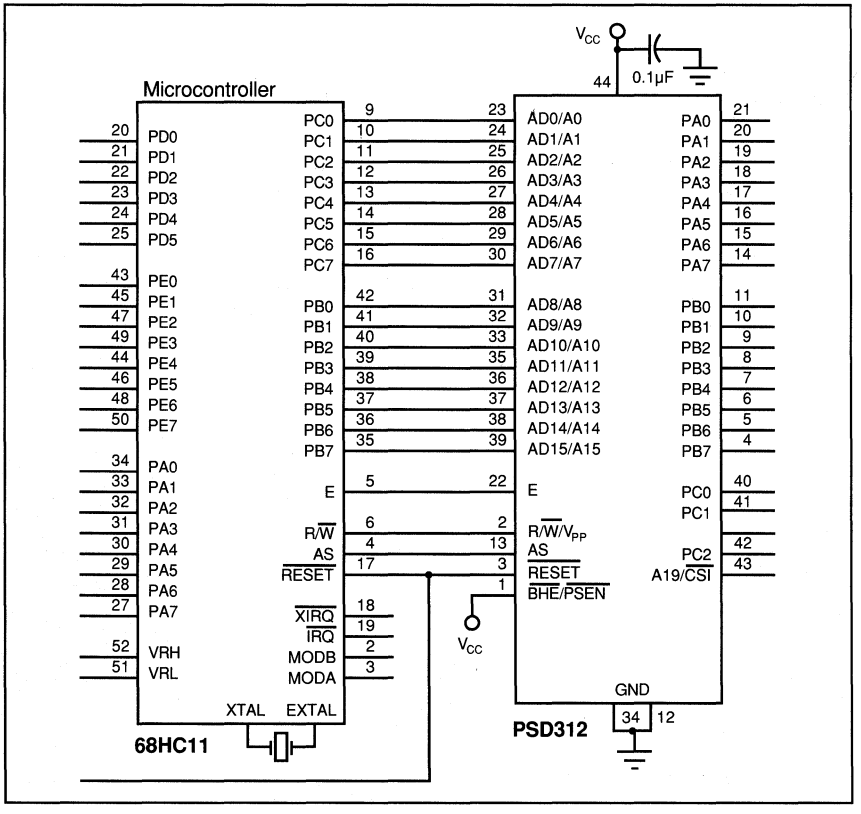
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 12, the PSD312 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD312 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 13. PSD312 Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Absolute Maximum Ratings[13]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 13. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 14 and 16)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 15 and 16)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 14 and 17)	Comm'l (Note 18)		16	35	mA
		Comm'l (Note 19)		28	50	
		Ind/Mil (Note 18)		16	45	
		Ind/Mil (Note 19)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 14 and 17)	Comm'l (Note 18)		47	80	mA
		Comm'l (Note 19)		59	95	
		Ind/Mil (Note 18)		47	100	
		Ind/Mil (Note 19)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 15 and 17)	Comm'l (Note 18)		36	65	mA
		Comm'l (Note 19)		58	80	
		Ind/Mil (Note 18)		36	80	
		Ind/Mil (Note 19)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 15 and 17)	Comm'l (Note 18)		67	105	mA
		Comm'l (Note19)		79	120	
		Ind/Mil (Note 18)		67	130	
		Ind/Mil (Note 19)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 14. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
15. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
16. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
17. AC power component is 3.0 mA/MHz (power = AC + DC).
18. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
19. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

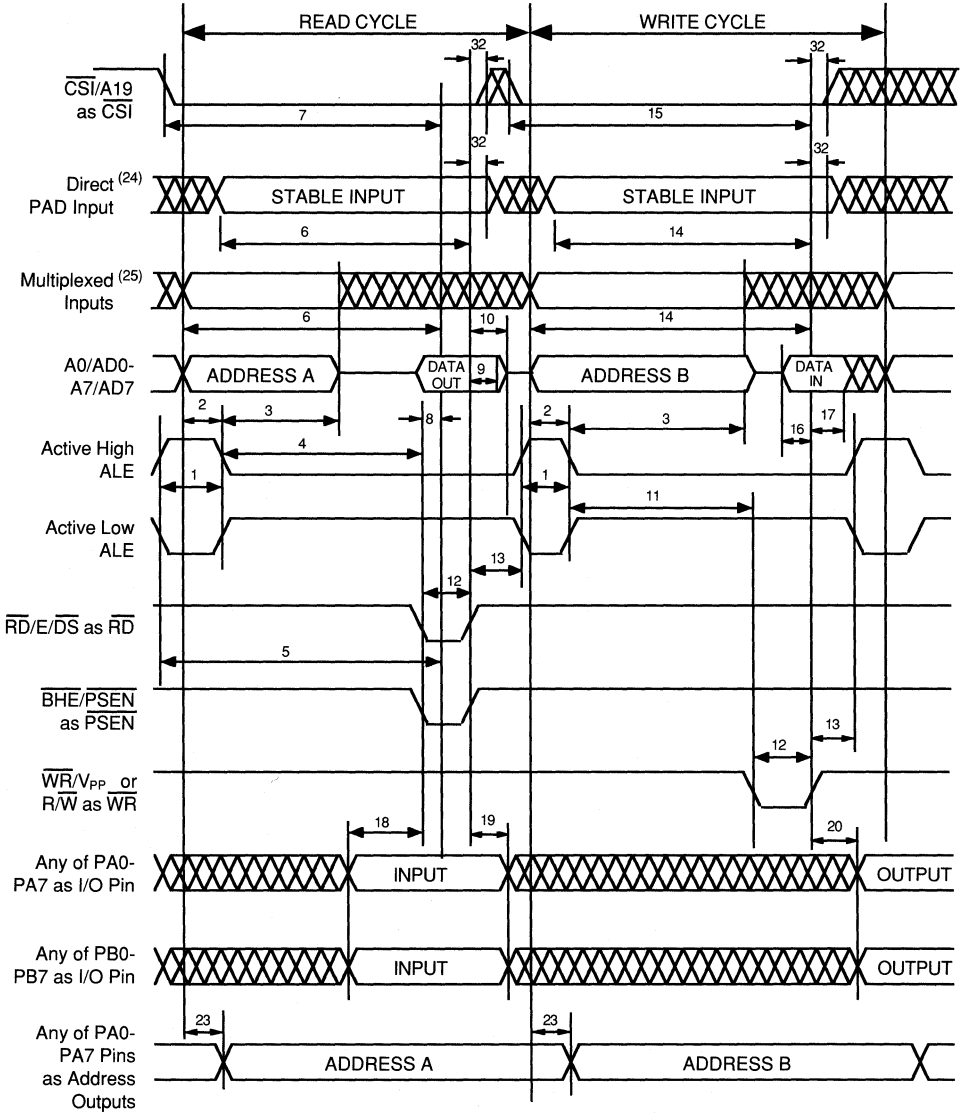
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	9		12		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	130		140		170		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		130		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		32		35		40	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		200		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	40	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	40	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		28		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		50		50	
T24	Track Mode Address Holding Time	15		27		27		
T25	Track Mode Read Propagation Delay		29		35		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		30		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	55	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	55	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E High	15		20		25		

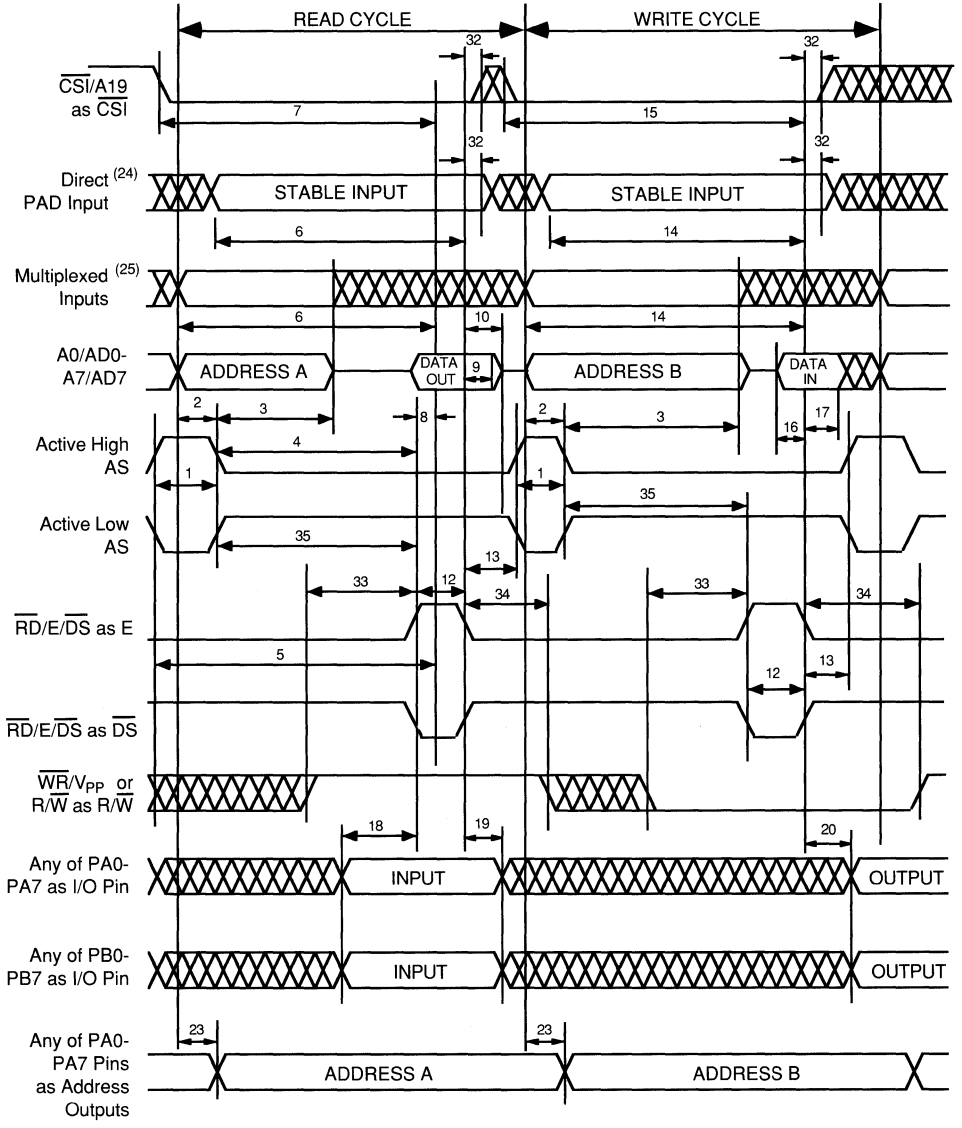
NOTES: 20. ADi = any address line.
21. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
22. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
23. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



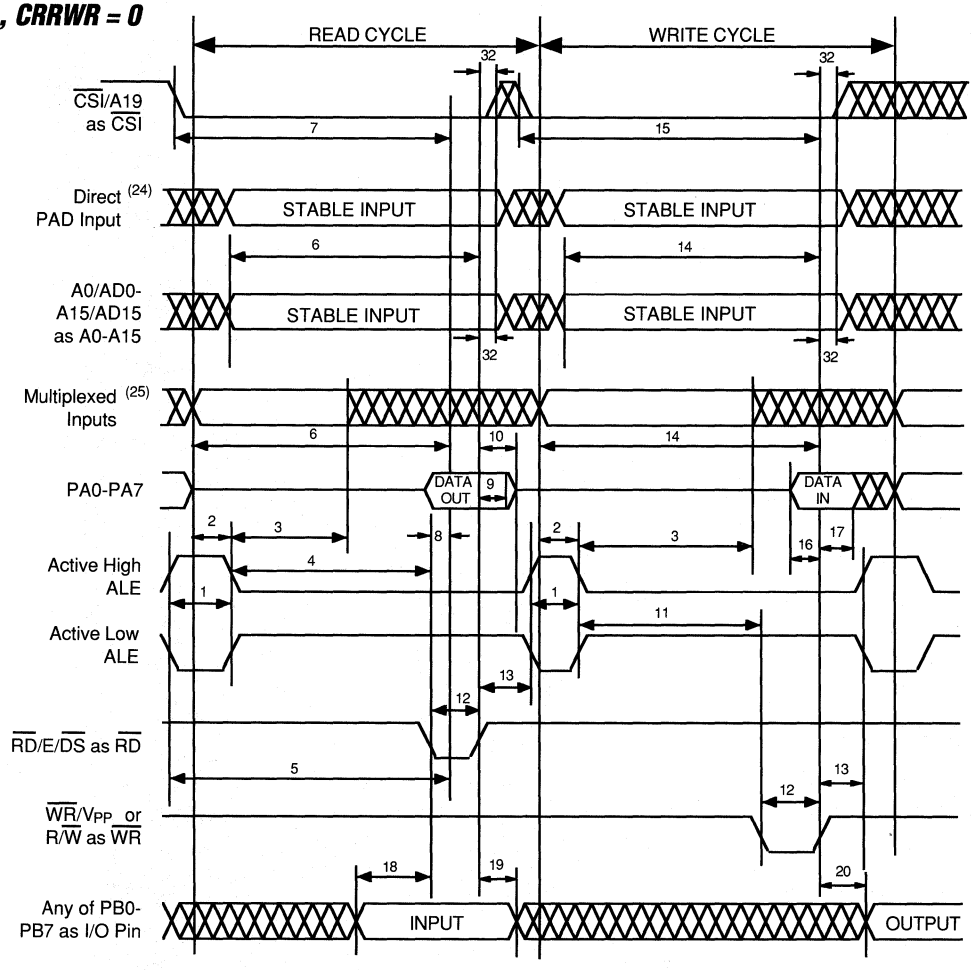
See referenced notes on page 2-157.

Figure 15. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



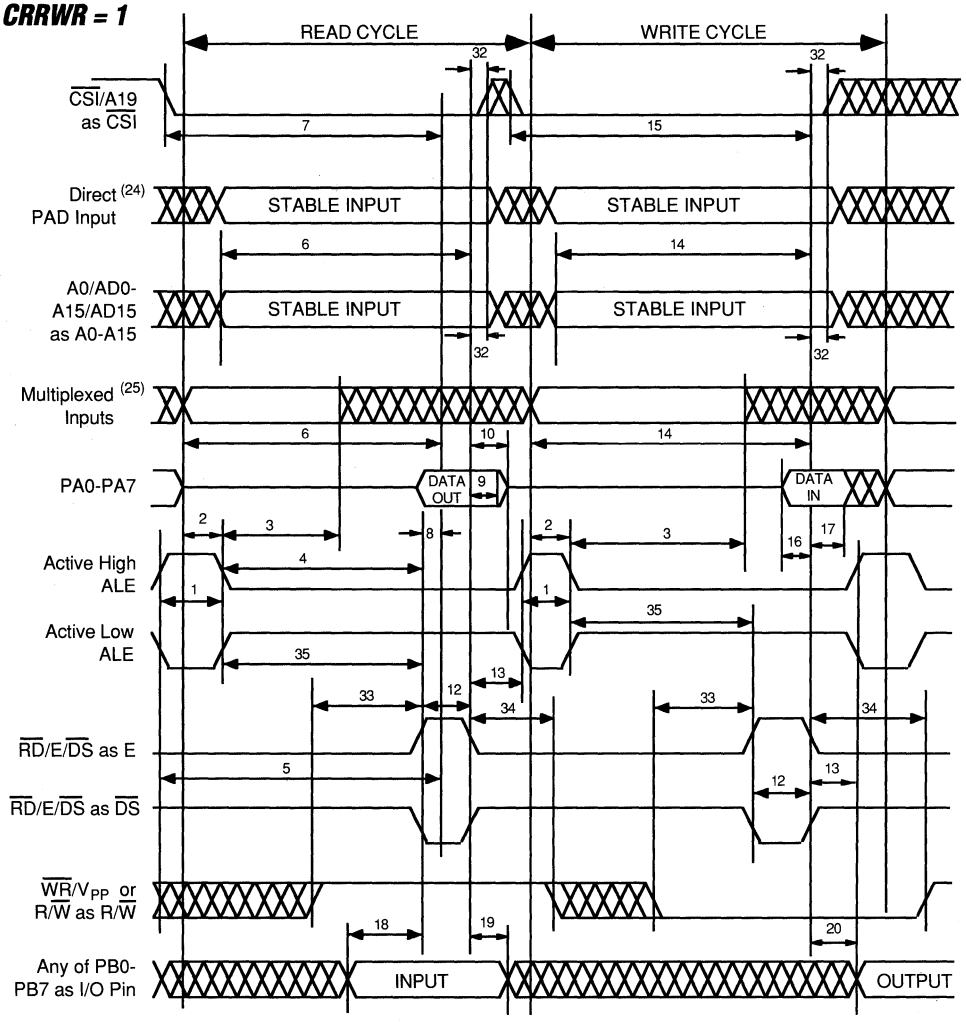
See referenced notes on page 2-157.

Figure 16. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-157.

Figure 17. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-157.

Figure 18. Chip-Select Output Timing

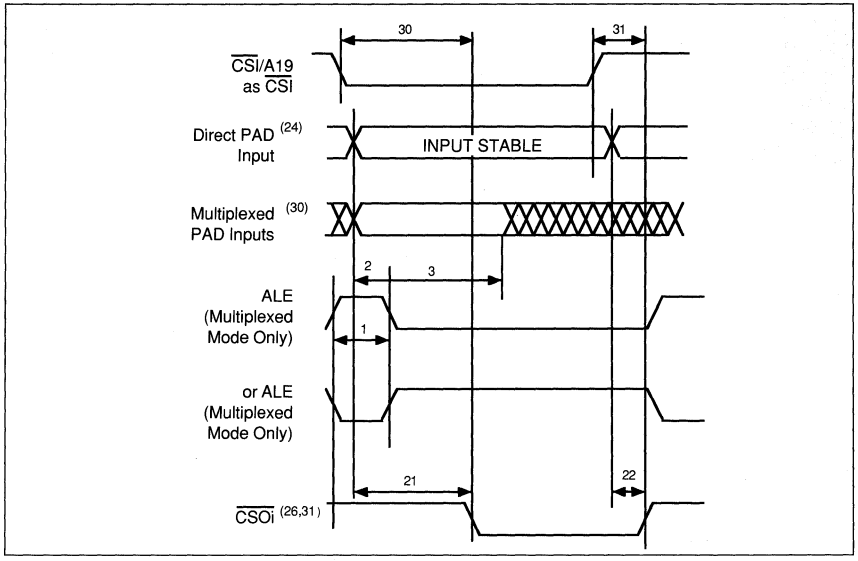
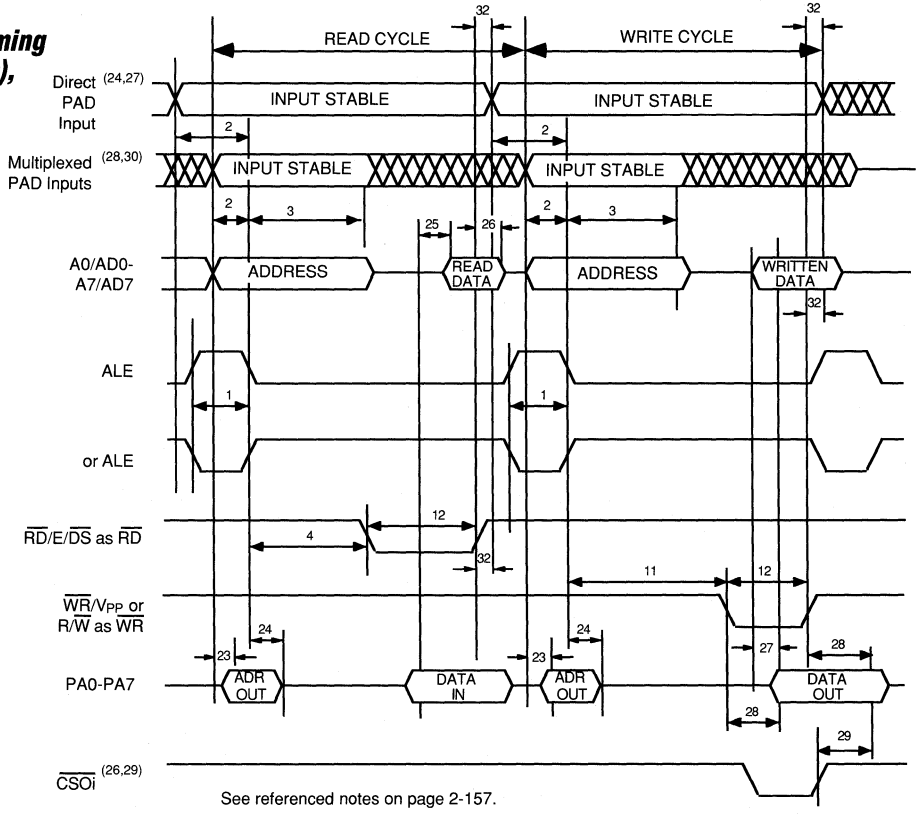
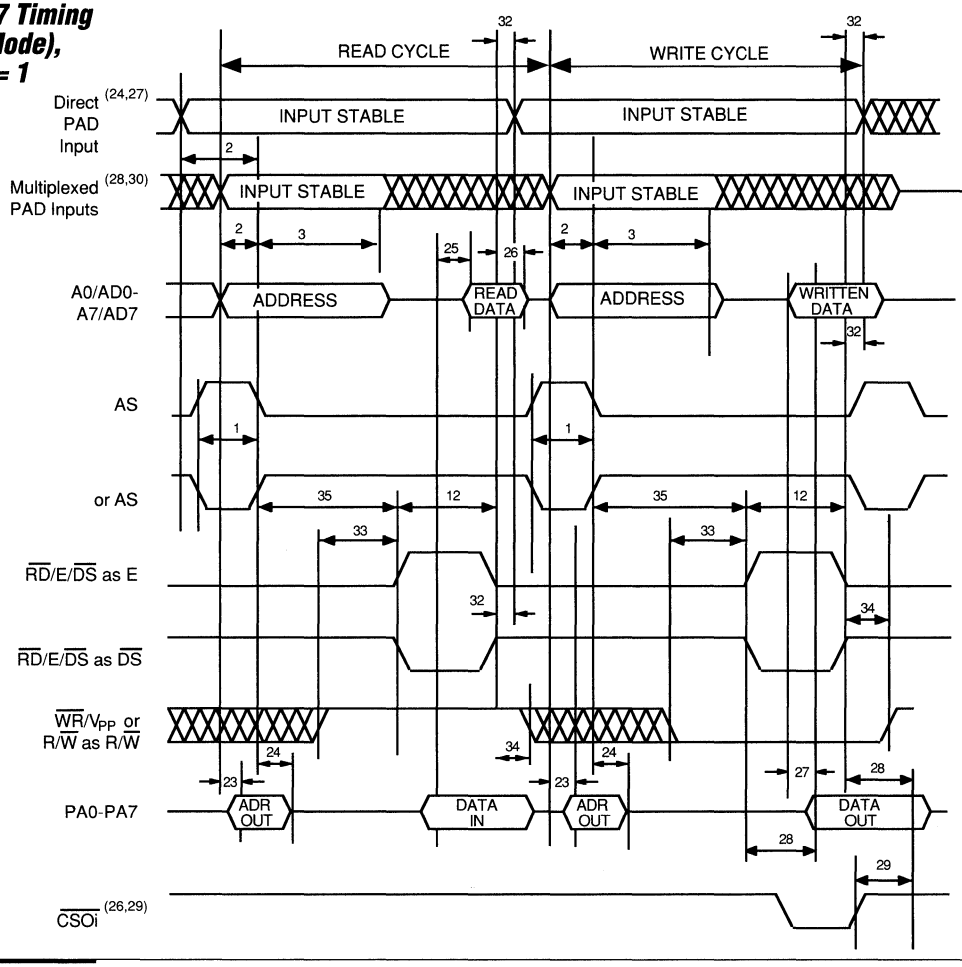


Figure 19. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-157.

Figure 20. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

24. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
25. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A7/AD7, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
26. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
27. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
28. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
29. The write operation signals are included in the $\overline{CSOi}$ expression.
30. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11–A15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
31. CSOi product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 12 Pin Capacitance[32]

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Conditions	Typical[33]	Max	Units
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	V_{PP} = 0 V	18	25	pF

NOTES: 32. This parameter is only sampled and is not 100% tested.
33. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 21. AC Testing Input/Output Waveform

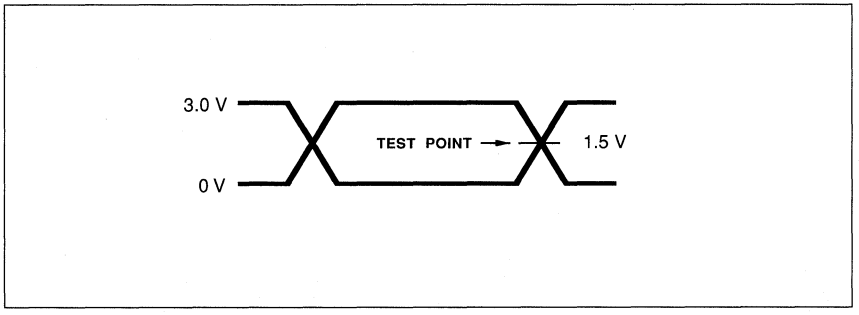
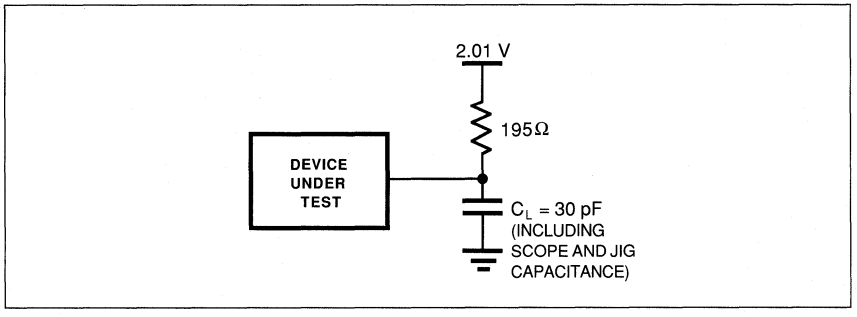


Figure 22. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD312 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD312 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package	52-Pin PQFP Package
$\overline{PSEN}$	1	A_5	46
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	A_4	47
RESET	3	B_4	48
PB7	4	A_3	49
PB6	5	B_3	50
PB5	6	A_2	51
PB4	7	B_2	2
PB3	8	B_1	3
PB2	9	C_2	4
PB1	10	C_1	5
PB0	11	D_2	6
GND	12	D_1	7
ALE or AS	13	E_1	8
PA7	14	E_2	9
PA6	15	F_1	10
PA5	16	F_2	11
PA4	17	G_1	12
PA3	18	G_2	15
PA2	19	H_2	16
PA1	20	G_3	17
PA0	21	H_3	18
$\overline{RD}$/E/$\overline{DS}$	22	G_4	19
AD0/A0	23	H_4	20
AD1/A1	24	H_5	21
AD2/A2	25	G_5	22
AD3/A3	26	H_6	23
AD4/A4	27	G_6	24
AD5/A5	28	H_7	25
AD6/A6	29	G_7	28
AD7/A7	30	G_8	29
A8	31	F_7	30
A9	32	F_8	31
A10	33	E_7	32
GND	34	E_8	33
A11	35	D_8	34
A12	36	D_7	35
A13	37	C_8	36
A14	38	C_7	37
A15	39	B_8	38
PC0	40	B_7	41
PC1	41	A_7	42
PC2	42	B_6	43
A19/$\overline{CSI}$	43	A_6	44
V_{CC}	44	B_5	45

NOTE: 34. Pins 1, 13, 14, 26, 27, 39, 40, and 52 are No Connect.

Package Information

Figure 23 Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

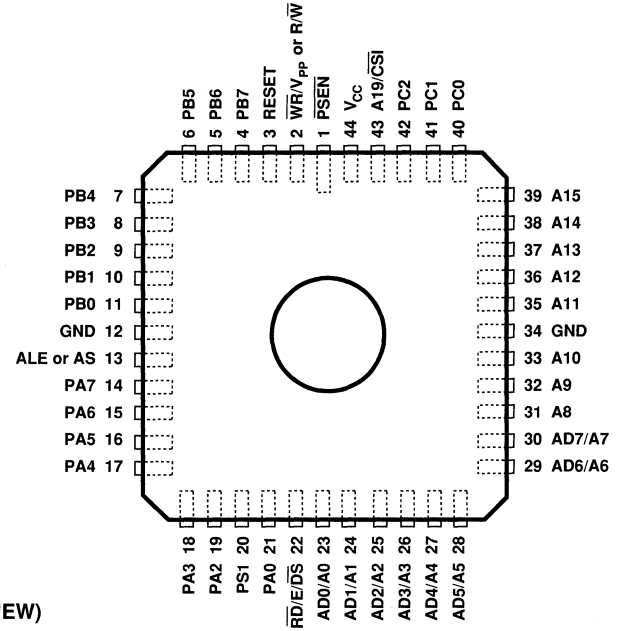


Figure 24. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

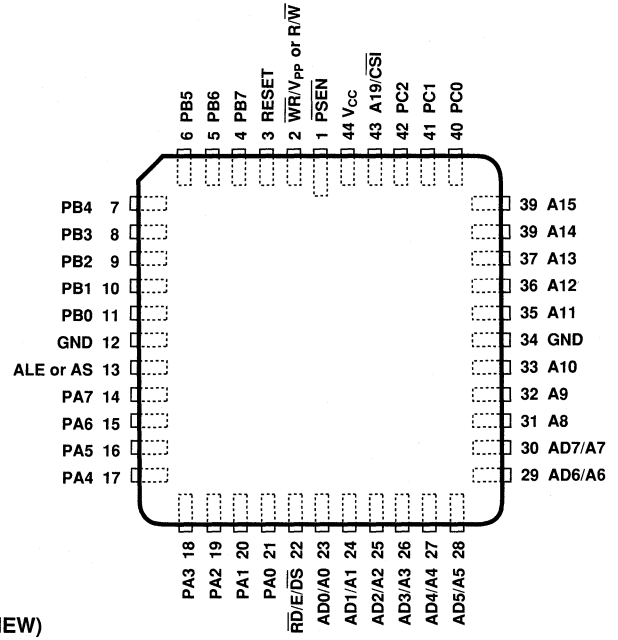


Figure 25. Drawing Q2 — 52-Pin PQFP (Package Type Q)

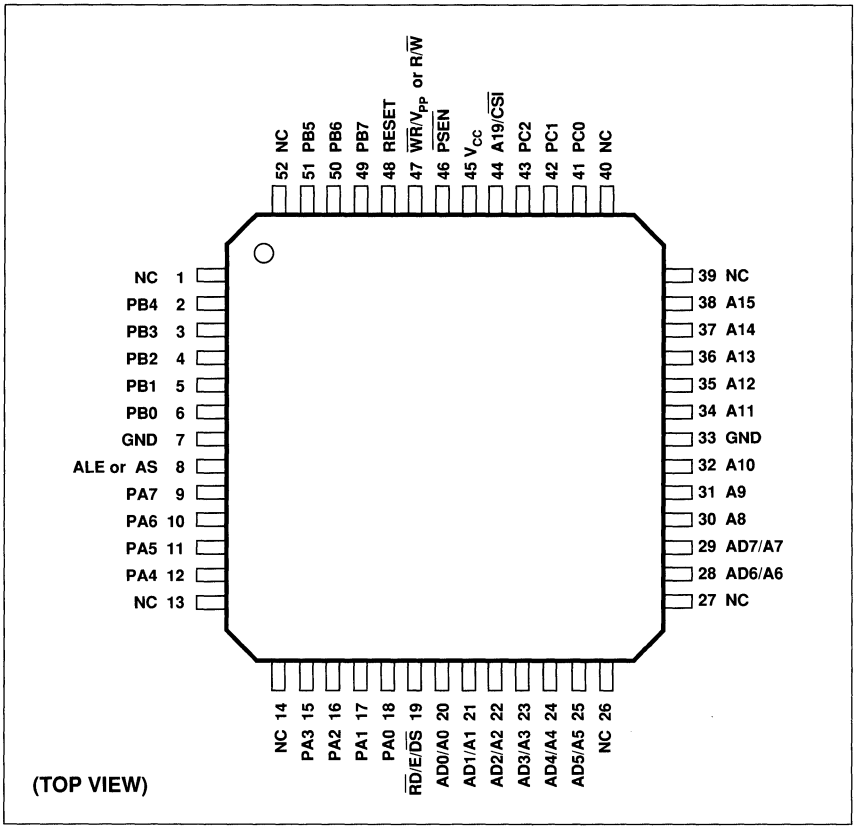
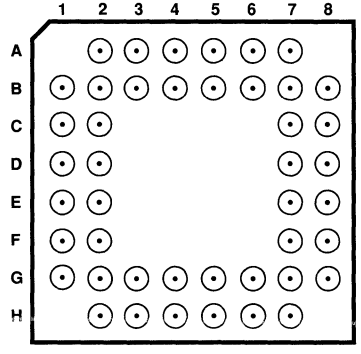


Figure 26. Drawing X2 — 44-Pin CPGA (Package Type X)



Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD312-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD312-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD312-12Q	120	52-pin PQFP	Q2	Commercial	Standard
PSD312-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD312-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD312-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD312-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD312-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD312-15LM	150	44-pin CLDCC	L4	Military	Standard
PSD312-15LMB	150	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD312-15Q	150	52-pin PQFP	Q2	Commercial	Standard
PSD312-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD312-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD312-15XM	150	44-pin CPGA	X2	Military	Standard
PSD312-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD312-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD312-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD312-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD312-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD312-20LM	200	44-pin CLDCC	L4	Military	Standard
PSD312-20LMB	200	44-pin CLDCC	L4	Military	MIL-STD-883C
PSD312-20Q	200	52-pin PQFP	Q2	Commercial	Standard
PSD312-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD312-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD312-20XM	200	44-pin CPGA	X2	Military	Standard
PSD312-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

System Development Tools

The PSD312 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD312 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD312 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6020 52-pin PSD312 PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD312 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD312 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD312 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD312 device, which then can be used in the target system. The development cycle is depicted in Figure 27.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD312 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

WS6020
- ❑ 52-pin PQFP Package Adaptor. Used with the WS6000 MagicPro Programmer

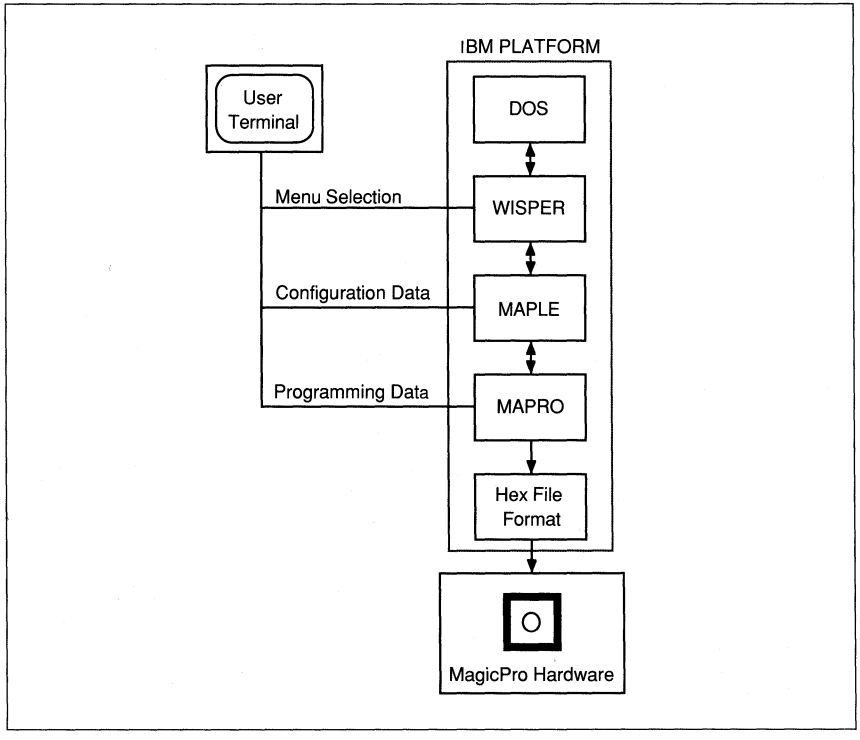
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 27. PSD312 Development Cycle



Programmable Peripheral

PSD303

Programmable Microcontroller Peripheral with Memory

Preliminary

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — Selectable 8 or 16 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, R/$\overline{W}$/E, or R/$\overline{W}$/$\overline{DS}$
  - — BHE/ pin for byte select in 16-bit mode
  - — PSEN/ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1M bit of UV EPROM
  - — Configurable as 128K x 8 or as 64K x 16
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8 or 8K x 16
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Configurable as 2K x 8 or as 1K x 16
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD303 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD303 on an IBM PC
- ❑ Downward Pin and Functionally Compatible with the PSD301 and PSD302

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/8098, 80186/88, 80196/98
- ❑ **Signetics:** SC80C451, SC80C552
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD303 is the latest member in the rapidly growing family of PSD devices. The PSD303 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumptions are essential. When combined in an 8- or 16-bit system, virtually any microcontroller (68HC11, 8051, 8096, 16000, etc.) and the PSD303 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD303 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD303 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 1M bit of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD303 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD303 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanding address space of microcontrollers

WSI's PSD303 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 1M bit EPROM, and 16K bit SRAM on a single chip. The PSD303 does not require any glue logic for interfacing to any 8- or 16-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD303's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD303 in a 16-bit configuration. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD303 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD303 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (as 16K x 8 or as 8K x 16) and SRAM (as 2K x 8 or as 1K x 16) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

The page register extends the accessible address space of certain microcontrollers from 64K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line processors by a factor of 16.

Figure 1. PSD303 Architecture

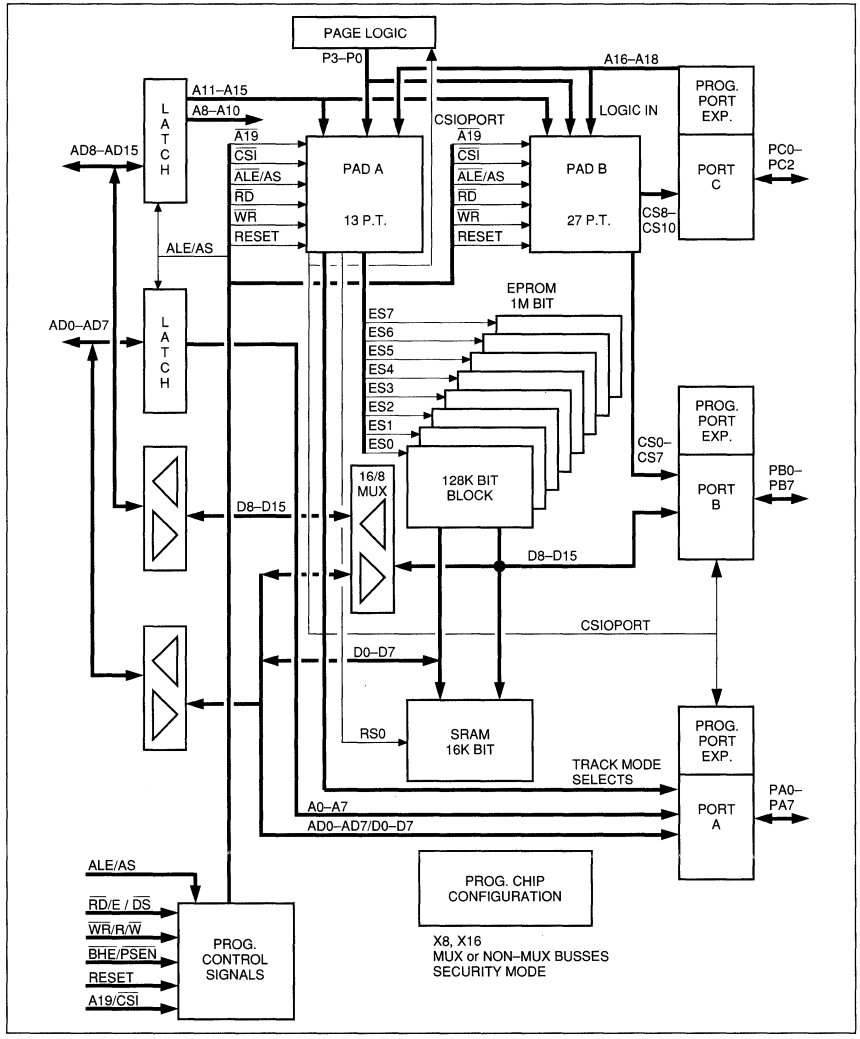


Table 1. PSD303 Pin Descriptions

Name	Type	Description
$\overline{BHE}/\overline{PSEN}$	I	When the data bus width is 8 bits (CDATA = 0), this pin is $\overline{PSEN}$. In this mode, $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ and $\overline{RD}/\overline{E}/\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM. When the data bus width is configured as 16 (CDATA = 1), this pin is $\overline{BHE}$. When $\overline{BHE}$ is low, data bus bits D8–D15 are read from, or written into, the PSD303, depending on the operation being read or write, respectively. In programming mode, this pin is pulsed between V_{PP} and 0.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 0 | NOP 0 | 1 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}/\overline{E}/\overline{DS}$	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 12 and 13 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 10 and 11 for the chip state after reset.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD303 Pin Descriptions (Cont.)

Name	Type	Description
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD303 configuration. See Table 8. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. When the chip is in non-multiplexed mode (CADDRAT = 0) and the data bus width is 16 (CDATA = 1), the port becomes the data bus (D8–D15). See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/PSEN pins. In non-multiplexed mode, these pins are the low-order address input.

Table 1. PSD303 Pin Descriptions (Cont.)

Name	Type	Description
AD8/A8 AD9/A9 AD10/A10 AD11/A11 AD12/A12 AD13/A13 AD14/A14 AD15/A15	I/O	In 16-bit multiplexed mode, these pins are the multiplexed high-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{BHE}$/$\overline{PSEN}$ pins. In all other modes, these pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD303's four operating modes allow it to interface directly to 8- and 16-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are:

- ❑ Multiplexed 8-bit address/data bus
- ❑ Multiplexed 16-bit address/data bus
- ❑ Non-multiplexed address/data, 8-bit data bus
- ❑ Non-multiplexed 16-bit address/data bus

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Multiplexed 16-bit Address/Data Bus

This mode is used to interface to microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bi-directional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address/data bus (AD8/A8–AD15/A15) is bi-directional and permits latching of the high-order address when the ALE signal is active on the same pins. The high-order data bus is read from or written to the device, depending on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{BHE}$/$\overline{PSEN}$, and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to non-multiplexed 8-bit microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

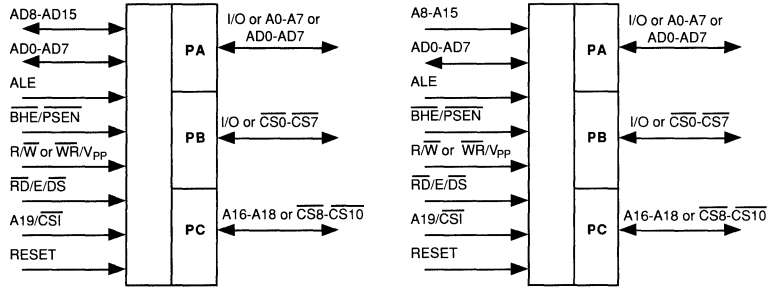
Non-Multiplexed Address/Data, 16-bit Data Bus

This mode is used to interface to non-multiplexed 16-bit microcontrollers with a 16-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (AD8/A8–AD15/A15) is the high-order address bus byte. Port A is the low-order data bus. Port B is the high-order data bus.

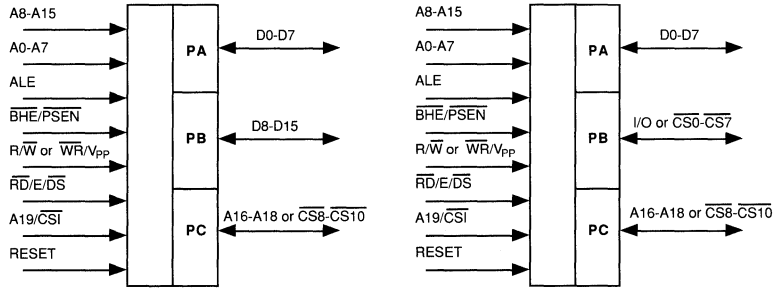
Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

Figure 2. PSD303 Port Configurations

Figure 2 shows the PSDS303's I/O port configurations.



1. PSD303 configured for multiplexed 16-bit address/data bus.
2. PSD303 configured for multiplexed 8-bit address/data bus.



3. PSD303 configured for non-multiplexed 16-bit address/data bus.
4. PSD303 configured for non-multiplexed address/data, 8-bit bus.

Legend: AD8–AD15 = Addresses A8–A15 multiplexed with data lines D8–D15.
AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD303 Bus and Port Configuration Options

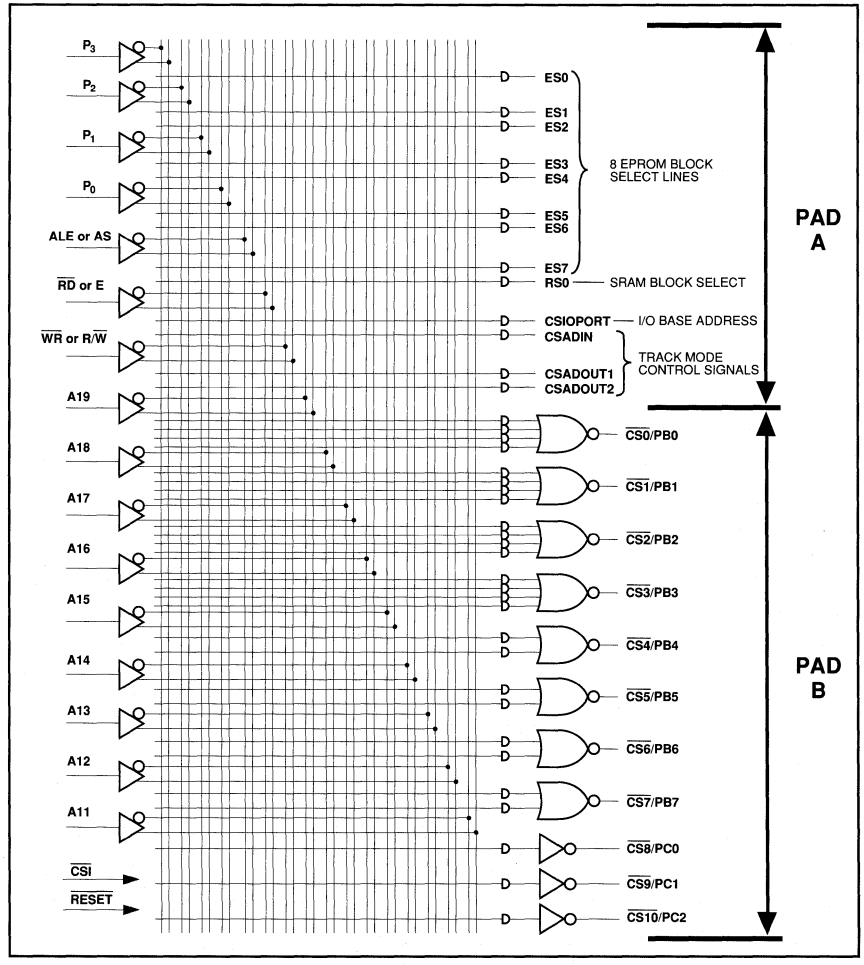
	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address data byte	High-order address bus byte
16-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	Low-order data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	High-order data bus byte
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
AD8/A8–AD15/A15	High-order multiplexed address/data byte	High-order address bus byte

Programmable Address Decoder (PAD)

The PSD303 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 3. PSD303 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 12 and 13.

3. RESET deselects all PAD output signals. See Tables 10 and 11.

4. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Table 3. PSD303 PAD A and B I/O Functions

Function	
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 12 and 13). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 10 and 11.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Tables 6 and 7.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD303 MAPLE software to set the bits.

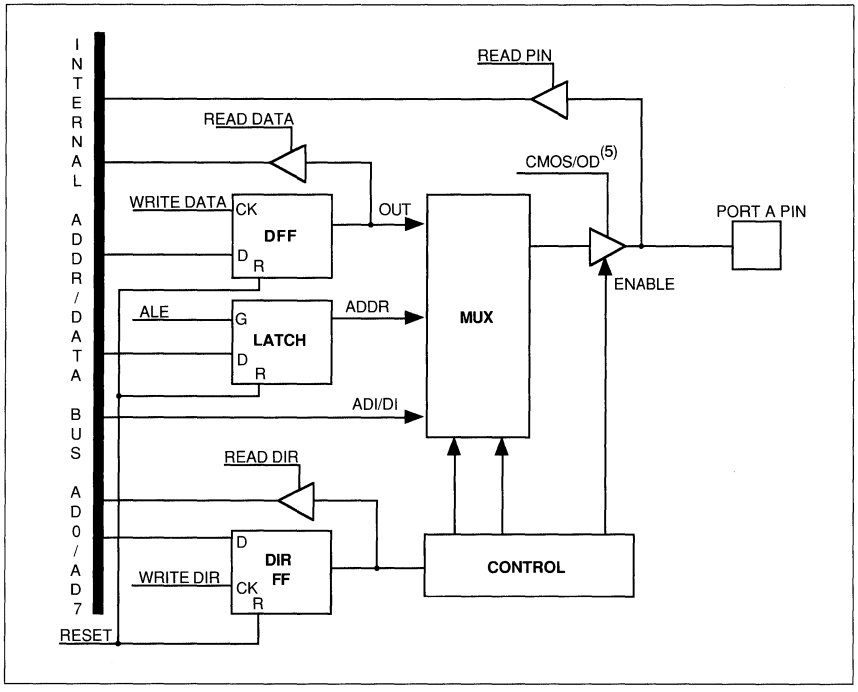
Table 4. PSD303 Non-Volatile Configuration Bits

Use This Bit	To
CDATA	Set the data bus width to 8 or 16 bits.
CADDRDAT	Set the address/data buses to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
COMB/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address out.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16–A19 individually as logic or address inputs.
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched.
CRRWR	Configure the polarity and control methods of read and write cycles.

Port Functions

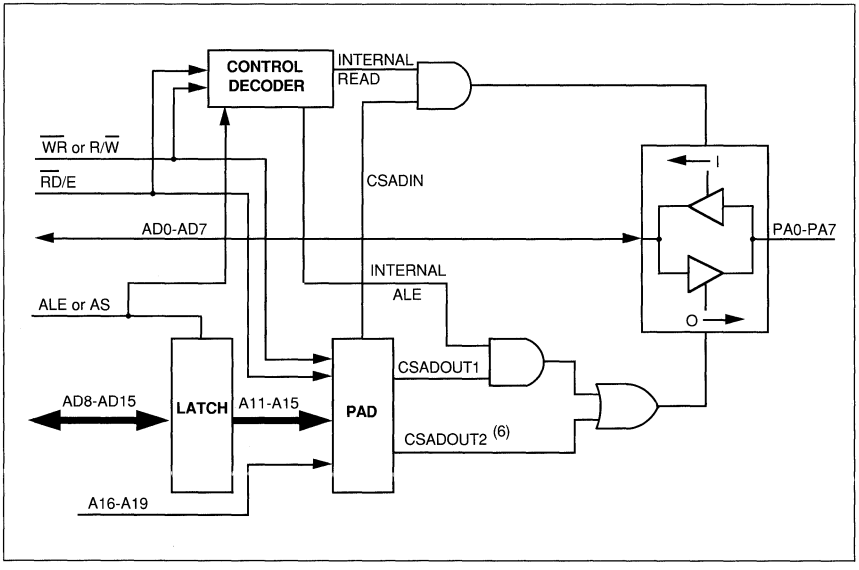
The PSD303 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 5. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 6. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD303 Configuration Bits[7,8]

Configuration Bits	No. of Bits	Function
CDATA	1	8-bit or 16-bit Data Bus Width CDATA = 0 eight bits CDATA = 1 sixteen bits
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active HIGH or Active LOW CRESET = 0, Active low RESET CRESET = 1, Active high RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CPAF1	8	Port A I/O or A0–A7 CPAF1 = 0, Port A pin is I/O CPAF1 = 1, Port A pin is Ai ($0 \le i \le 7$)
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CSI}$ ($0 \le i \le 7$) CPBF = 1, Port B pin is I/O

Table 5. PSD303 Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is $\overline{Ai}$ ($16 \leq i \leq 18$) CPCF = 1, Port C pin is $\overline{CSI}$ ($8 \leq i \leq 10$)
CADLOG	4	A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is Ai ($16 \leq i \leq 19$)
Total Bits	**51**	

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

2

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD303 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figures 22 and 23). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E/$\overline{DS}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD303 location, data is presented on Port A pins. When writing to an internal PSD303 location, data present on Port A pins is written to that location.

Port B in Multiplexed Address/Data and in 8-Bit Non-Multiplexed Modes

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Tables 6 and 7.

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Port B in 16-Bit Non-Multiplexed Address/Data Mode

In this mode, Port B becomes the high-order data bus byte of the chip. When reading an internal PSD303 high-order data bus byte location, the data is presented on Port B pins. When writing to an internal PSD303 high-order data bus byte location, data present on Port B is written to that location. See Table 9.

Accessing the I/O Port Registers

Tables 6 and 7 show the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

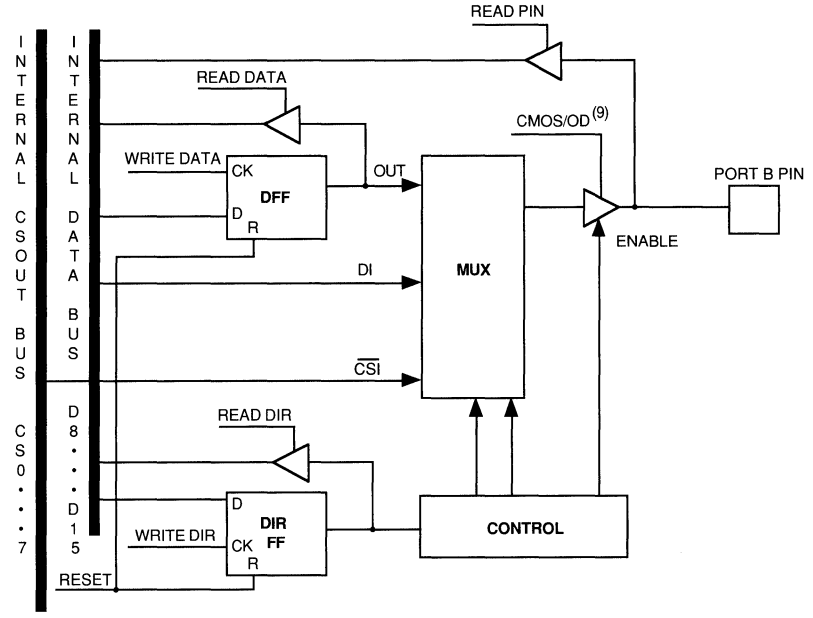
Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.



NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Table 7. I/O Port Addresses in an 16-bit Data Bus Mode[10,11]

Register Name	Word Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Ports B and A	+ 2 (accessible during read operation only)
Direction Register of Ports B and A	+ 4
Data Register of Ports B and A	+ 6

NOTES: 10. When the data bus width is 16, Port B registers can only be accessed if the $\overline{BHE}$ signal is low.
11. I/O Ports A and B are still byte-addressable, as shown in Table 6. For I/O Port B register access, $\overline{BHE}$ must be low.

Port Functions (Cont.)

ALE/AS and AD0/A0–AD15/A15 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. (See Table 8.)

EPROM

The PSD303 has 1M bit of EPROM. Depending on the configuration of the data bus, the EPROM can be organized as 128K x 8 (8-bit data bus) or as 64K x 16 (16-bit data bus). The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 16K x 8 (8-bit data bus) or as 8K x 16 (16-bit data bus).

SRAM

The PSD303 has 16K bits of SRAM. Depending on the configuration of the data bus, the SRAM organization can be 2K x 8 (8-bit data bus) or 1K x 16 (16-bit data bus). The SRAM is selected by the RS0 output of the PAD.

Page Register

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Control Signals

The PSD303 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{BHE}$/$\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

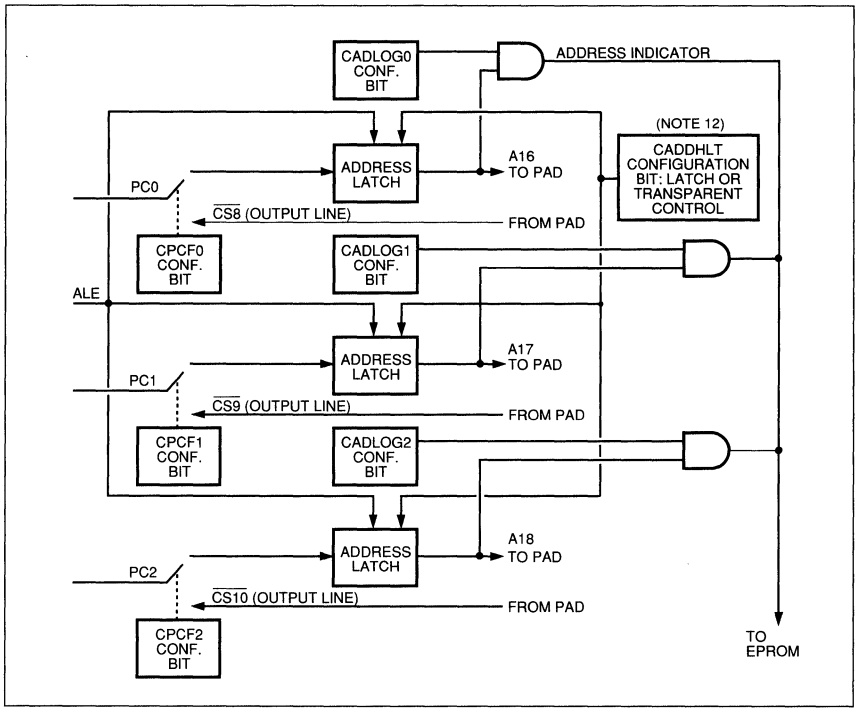
In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD303 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations to the PSD303 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

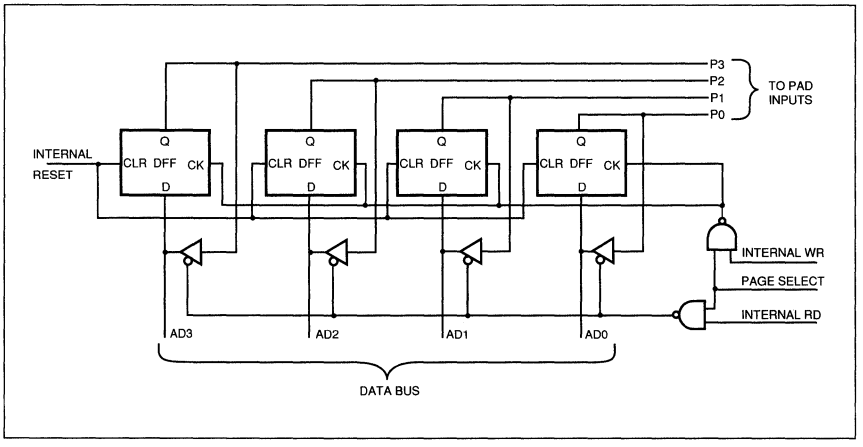
As $\overline{DS}$, the pin functions with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

Figure 7. Port C Structure



NOTE: 12. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Figure 8. Page Register



Control Signals (Cont.)

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{BHE}/\overline{PSEN}$

This pin's function depends on the PSD303 data bus width. If it is 8, the pin is $\overline{PSEN}$; if it is 16, the pin is $\overline{BHE}$. In 8-bit mode, the $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Figure 9. Combined Address Space

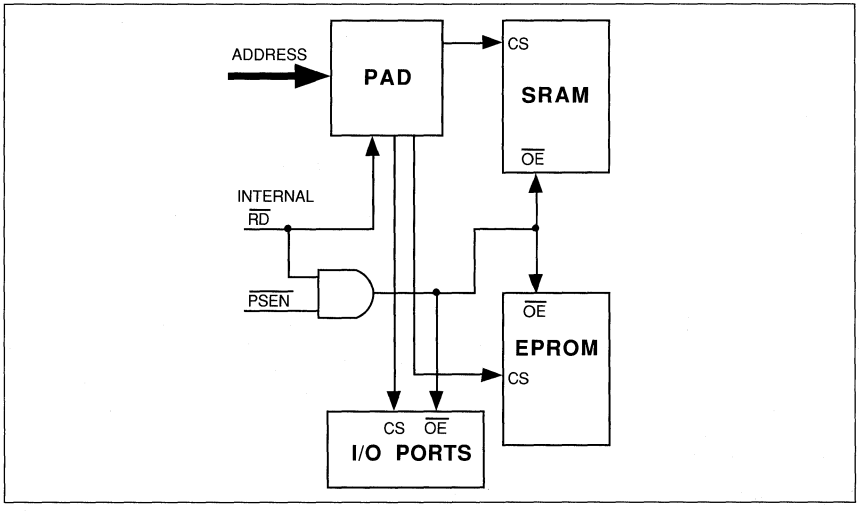
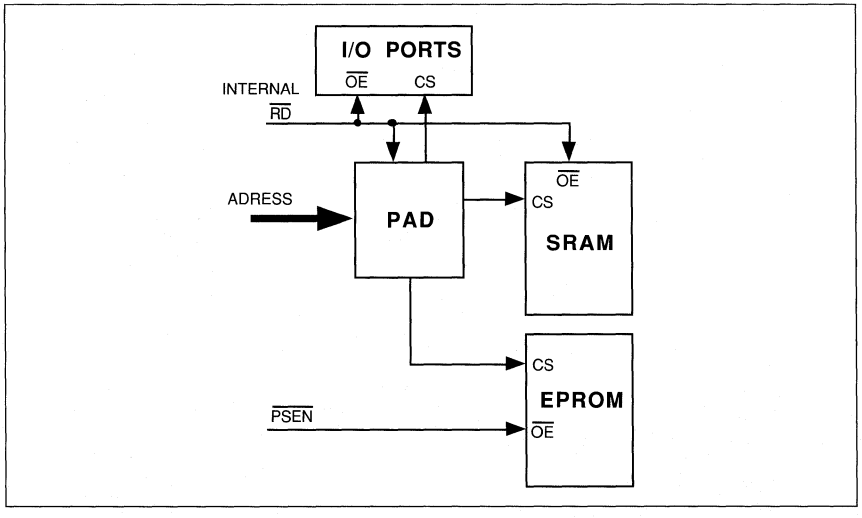


Figure 10. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

BHE/PSEN

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD303's PSEN pin must be connected to the PSEN pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the PSEN pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by RD low (CRRWR = 0), or by E high and R/W high (CRRWR = 1, CEDS = 0) or by DS low and R/W high (CRRWR, CEDS = 1). See Figures 9 and 10.

In BHE mode, this pin enables accessing of the upper-half byte of the data bus. A low on this pin enables a write or read operation to be performed on the upper half of the data bus (see Table 9).

Table 8. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD8/A8–AD15/A15	CDATA , CADDRDAT, CLOT = 0	8-bit data, non-multiplexed	Transparent
	CDATA, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 1, CADDRDAT, CLOT = 0	16-bit data, non-multiplexed	Transparent
	CDATA = 1, CADDRDAT = 0, CLOT = 1		ALE Dependent
	CDATA = 0, CADDRDAT = 1	8-bit data, multiplexed	Transparent
	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed	ALE Dependent
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
BHE/PSEN	CDATA = 0	8-bit data, PSEN is active	Transparent
	CDATA = 1, CADDRDAT = 0	16-bit data, non-multiplexed mode, BHE is active	Transparent
A19 and PC2–PC0	CDATA = 1, CADDRDAT = 1	16-bit data, multiplexed mode, BHE is active	ALE Dependent
	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD303. Reset polarity is programmable (active low or active high). Whenever the PSD303 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 10 and 11 indicate the state of the part during and after reset.

A19/$\overline{CSI}$

When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD303 states during the power-down mode, see Tables 12 and 13, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 8). In this mode, the chip is always enabled.

Table 9. High/Low Byte Selection Truth Table (in 16-Bit Configuration Only)

$\overline{BHE}$	A_0	Operation
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

Table 10. Signal States During and After Reset

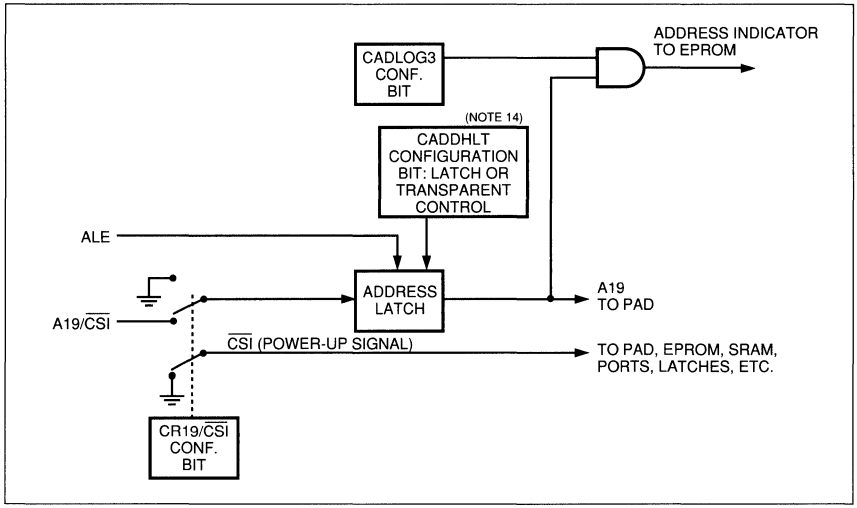
Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O $\overline{CS7}$–$\overline{CS0}$ CMOS outputs $\overline{CS7}$–$\overline{CS0}$ open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input High

Table 11. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 13)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 13)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	0 0 0 0

NOTE: 13. All PAD outputs are in a non-active state.

Figure 11. A19/CSI Cell Structure



NOTES: 14. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

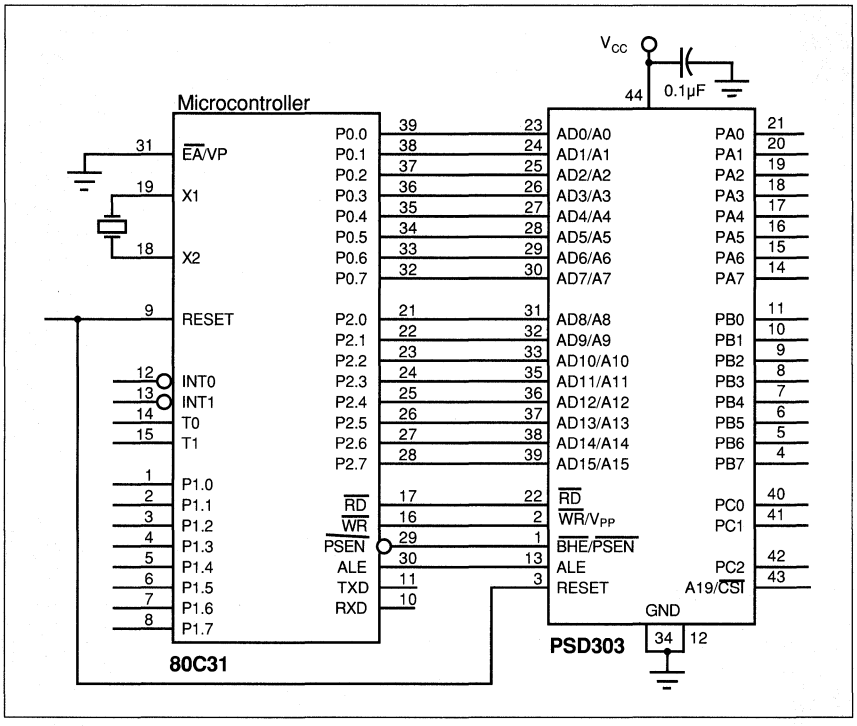
Table 12. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD15/A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Table 13. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Figure 12. PSD303 Interface With Intel's 80C31



The configuration bits for Figure 12 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Security Mode

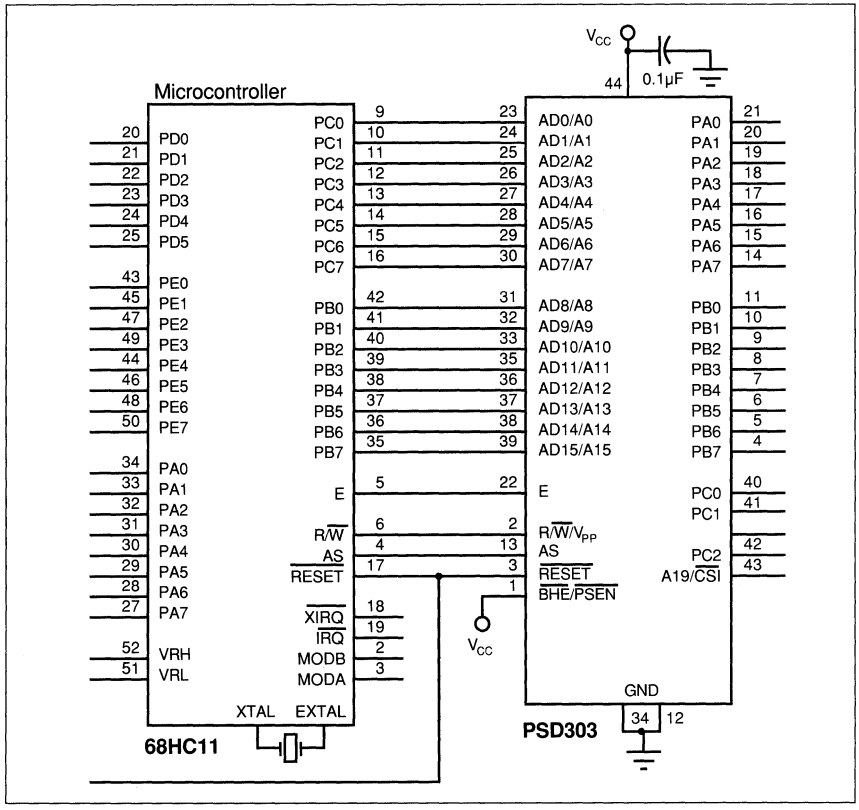
Security Mode in the PSD303 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD303 contents cannot be copied on a programmer.

System Applications

In Figure 12, the PSD303 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD303 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 13. PSD303 Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

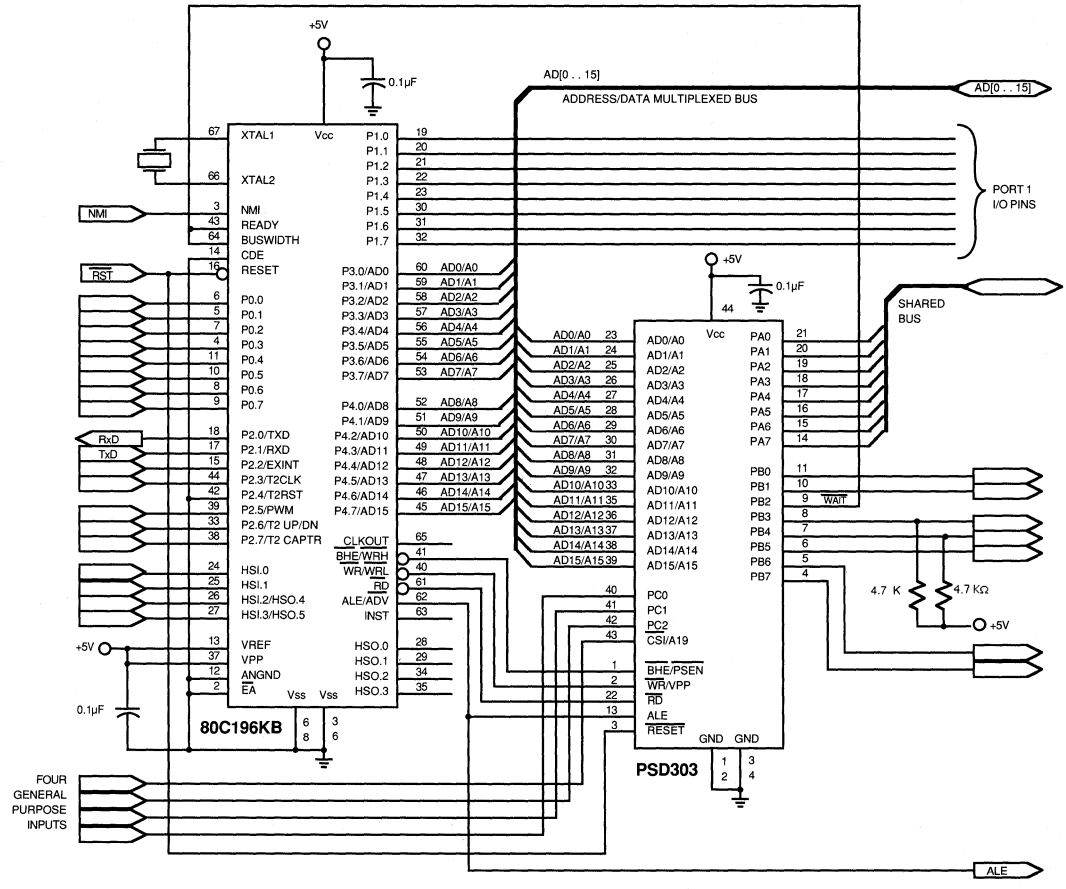
All other configuration bits may vary according to the application requirements.

System Applications (Cont.)

In Figure 14, the PSD303 is configured to work directly with Intel's 80C196KB microcontroller, which is a 16-bit address/16-bit data bus processor. Address and data lines multiplexed. In the example shown, all configuration bits are set. The PSD303 is configured to use PC0, PC1, PC2, and $\overline{CSI}$/A19 as A16, A17, A18, and A19 inputs, respectively. These signals are independent of the ALE pulse (latch-transparent). They are used as four general-purpose logic inputs that take part in the PAD equations implementation.

Port A is configured to work in the special track mode, in which (for certain conditions) PA0–PA7 tracks lines AD0/A0–AD7/A7. Port B is configured to generate $\overline{CS0}$–$\overline{CS7}$. In this example, PB2 serves as a $\overline{WAIT}$ signal that slows down the 80C196KB during the access of external peripherals. These 8-bit wide peripherals are connected to the shared bus of Port A. The $\overline{WAIT}$ signal also drives the buswidth input of the microcontroller, so that every external peripheral cycle becomes an 8-bit data bus cycle. PB3 and PB4 are open-drain output signals; thus, they are pulled up externally.

Figure 14. PSD303 Interface With Intel's 80C196KB.



The configuration bits for Figure 14 are:

CRESET	0	CSECURITY	Don't care
CALE	0	CPCF2, CPCF1, CPCF0	0, 0, 0
CDATA	1	CPACOD7–CPACOD0	00H
CADDRDAT	1	CPBF7–CPBF0	00H
CPAF1	Don't care	CPBCOD7–CPBCOD0	18H
CPAF2	1	CEDS	0
CA19/$\overline{CSI}$	1	CADLOG3—CADLOG0	0H
CRRWR	0		
COMB/SEP	0		
CADDHLT	0		

Absolute Maximum Ratings[15]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 15. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 16 and 18)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 17 and 18)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 16 and 19)	Comm'l (Note 20)		16	35	mA
		Comm'l (Note 21)		28	50	
		Ind/Mil (Note 20)		16	45	
		Ind/Mil (Note 21)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 16 and 19)	Comm'l (Note 20)		47	80	mA
		Comm'l (Note 21)		59	95	
		Ind/Mil (Note 20)		47	100	
		Ind/Mil (Note 21)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 17 and 19)	Comm'l (Note 20)		36	65	mA
		Comm'l (Note 21)		58	80	
		Ind/Mil (Note 20)		36	80	
		Ind/Mil (Note 21)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 17 and 19)	Comm'l (Note 20)		67	105	mA
		Comm'l (Note 21)		79	120	
		Ind/Mil (Note 20)		67	130	
		Ind/Mil (Note 21)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 16. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
17. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
18. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
19. AC power component is 3.0 mA/MHz (power = AC + DC).
20. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum
21. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

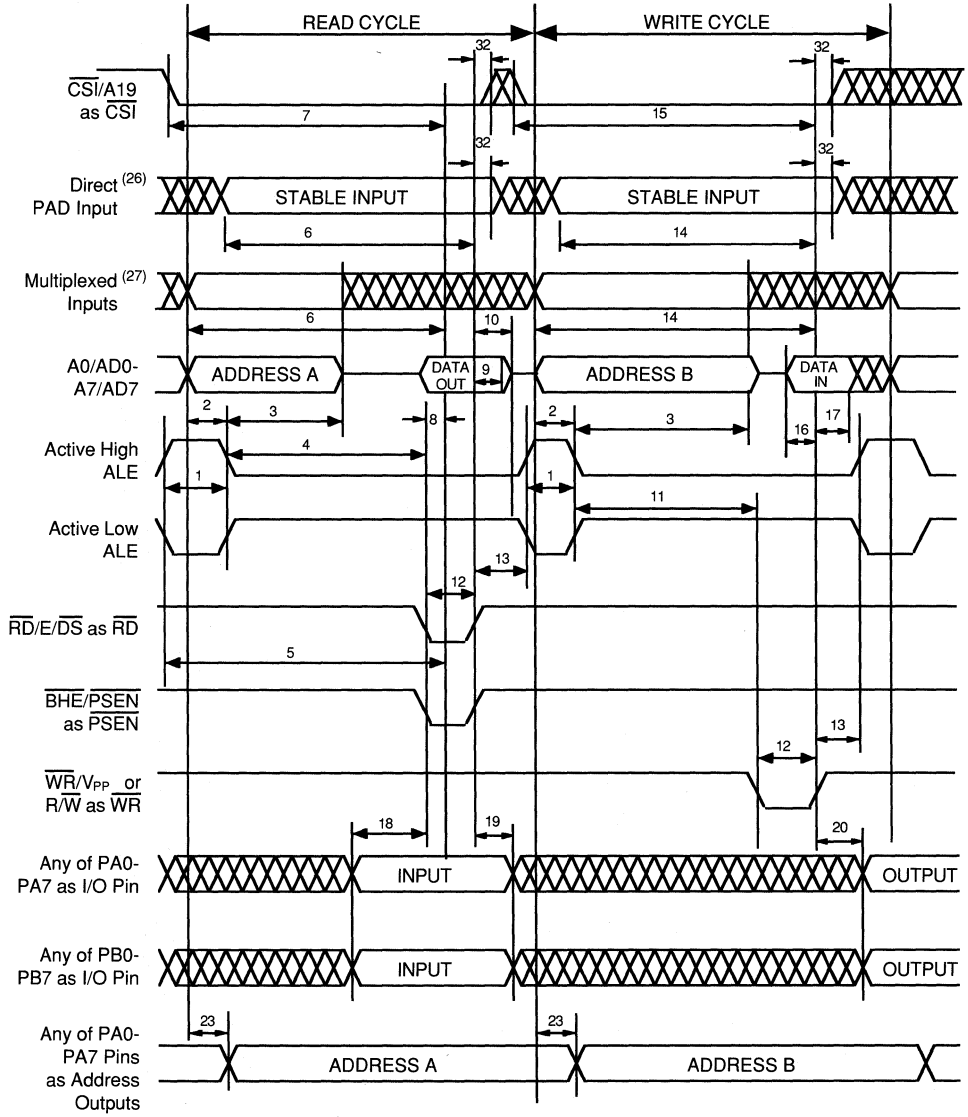
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	9		12		15		
T3	Address Hold Time	9		12		15		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	130		140		170		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		130		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		32		35		40	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ pulse width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		200		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	40	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	40	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		28		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		50		50	
T24	Track Mode Address Holding Time	15		27		27		
T25	Track Mode Read Propagation Delay		29		35		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		30		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	55	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	55	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E high	15		20		25		

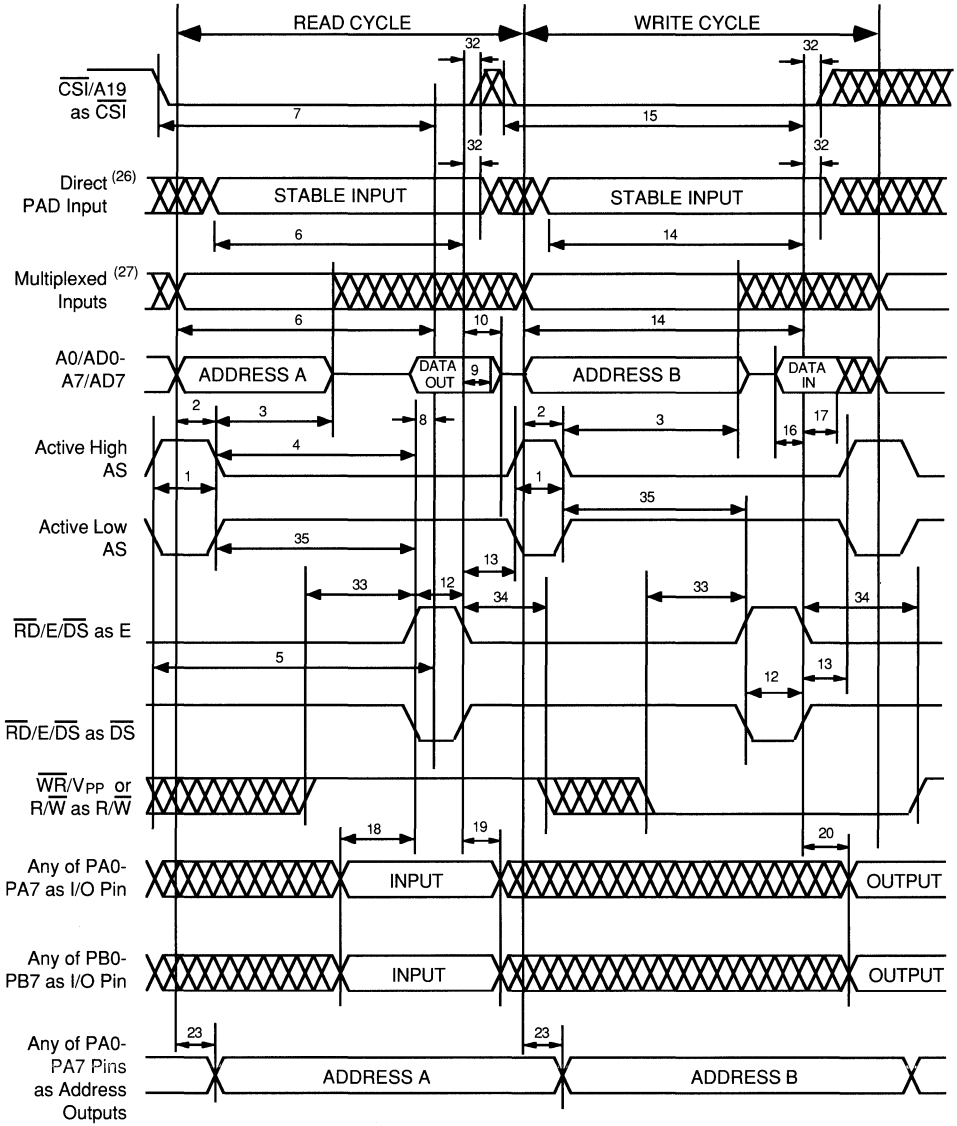
NOTES: 22. ADi = any address line.
23. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
24. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
25. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 15. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



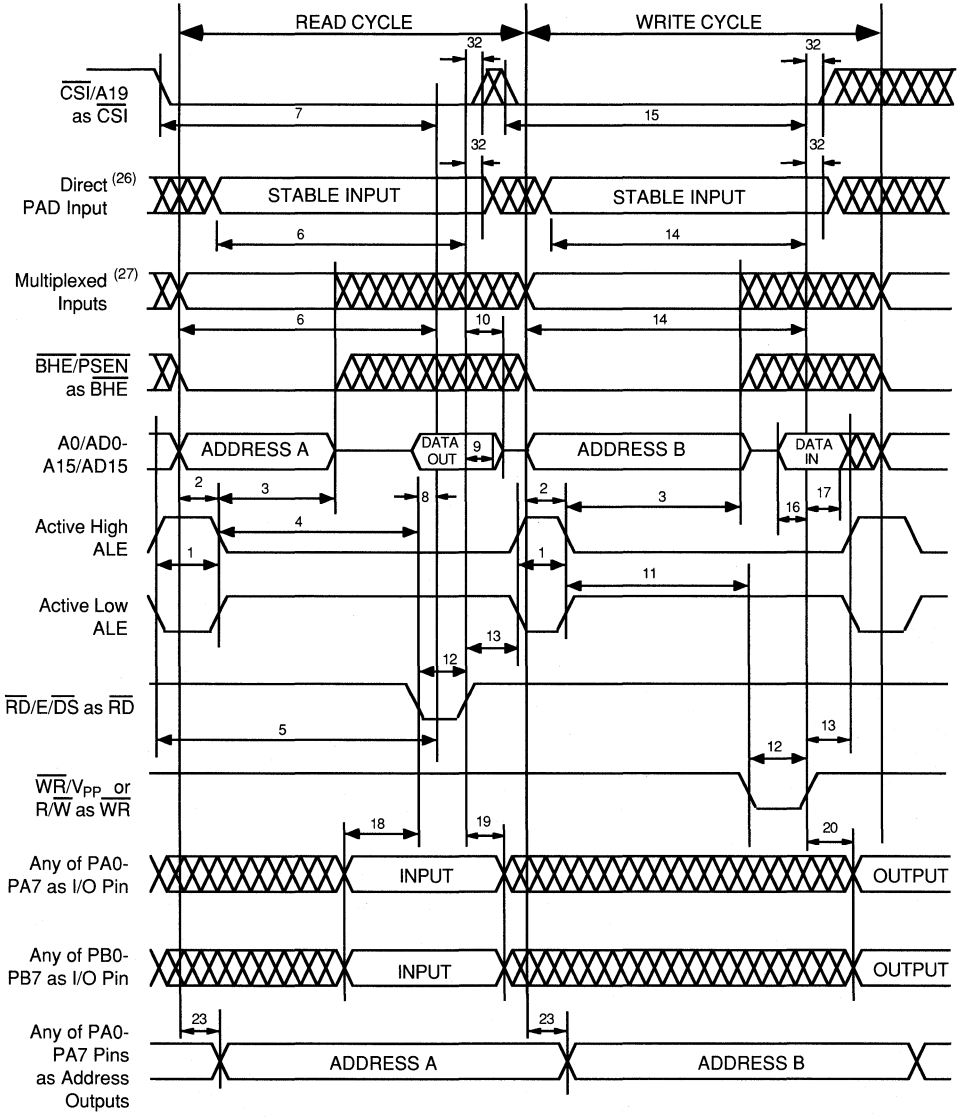
See referenced notes on page 2-201.

Figure 16. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



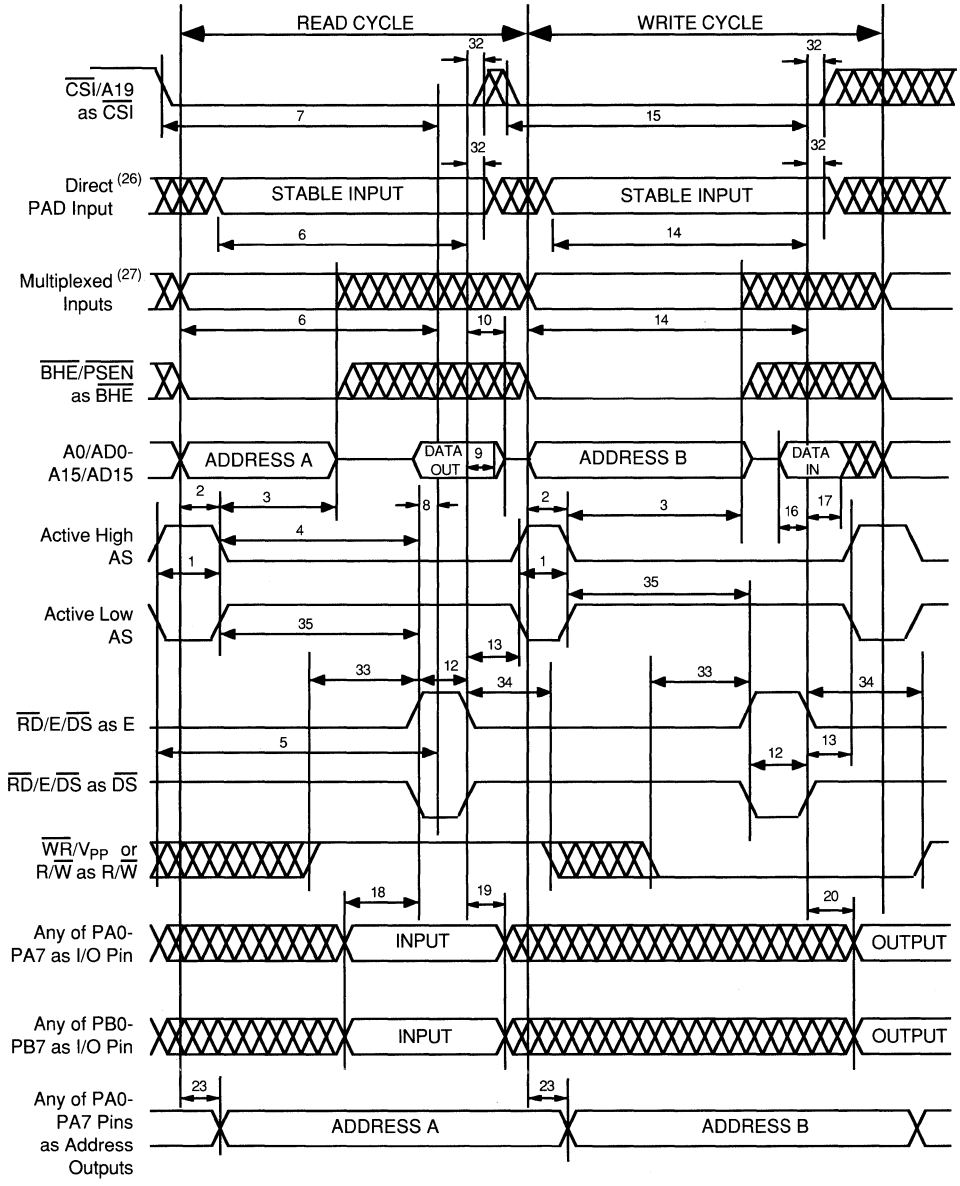
See referenced notes on page 2-201.

Figure 17. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 0



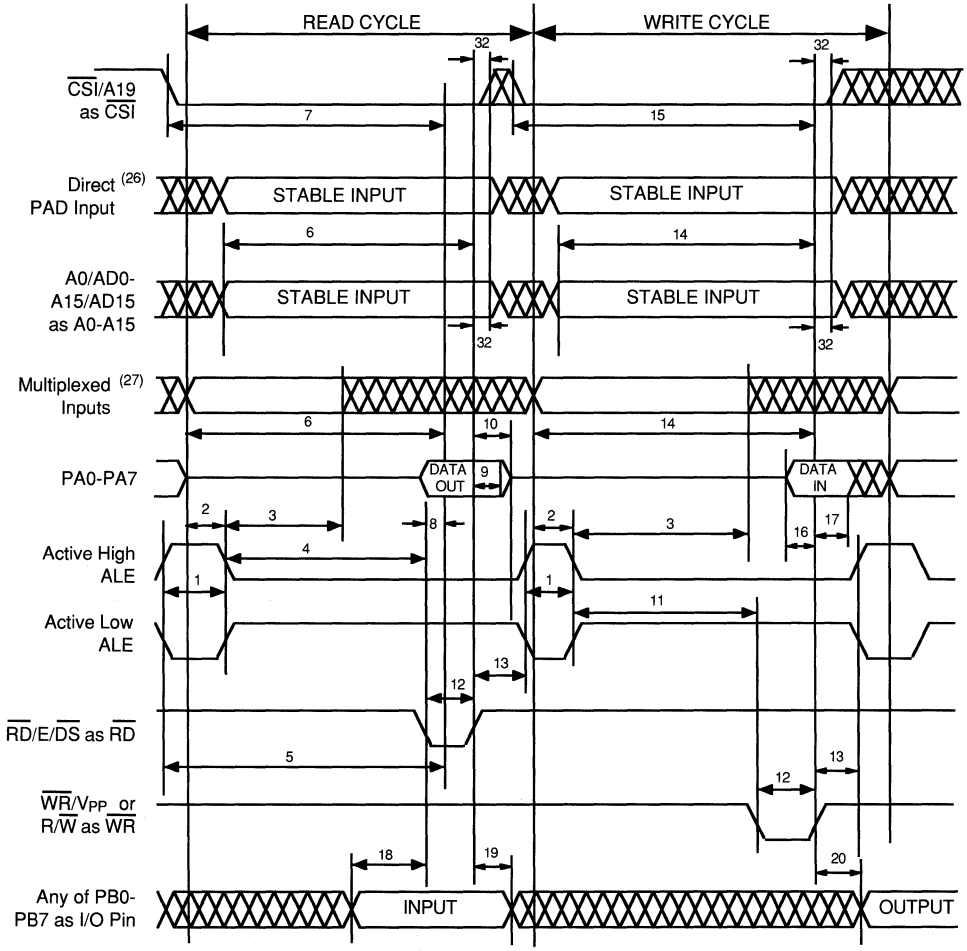
See referenced notes on page 2-201.

Figure 18. Timing of 16-Bit Multiplexed Address/Data Bus, CRRWR = 1



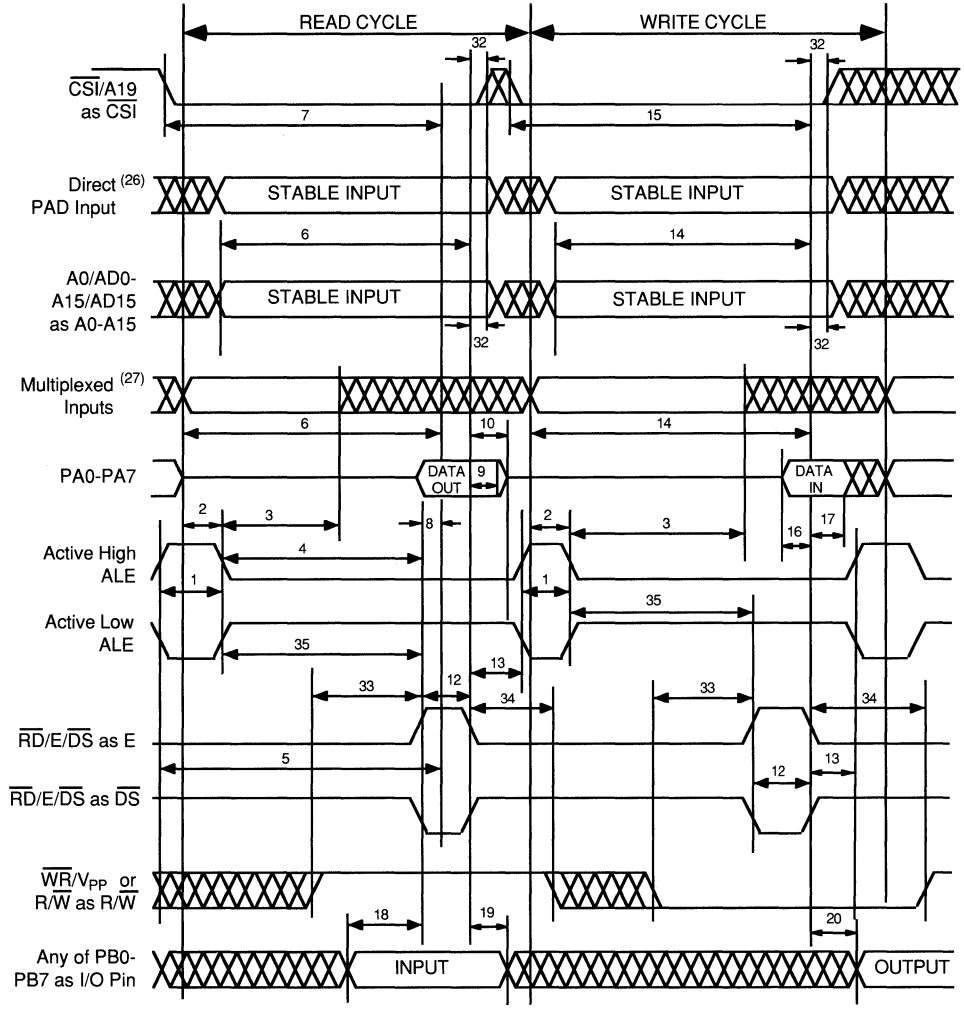
See referenced notes on page 2-201.

Figure 19. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



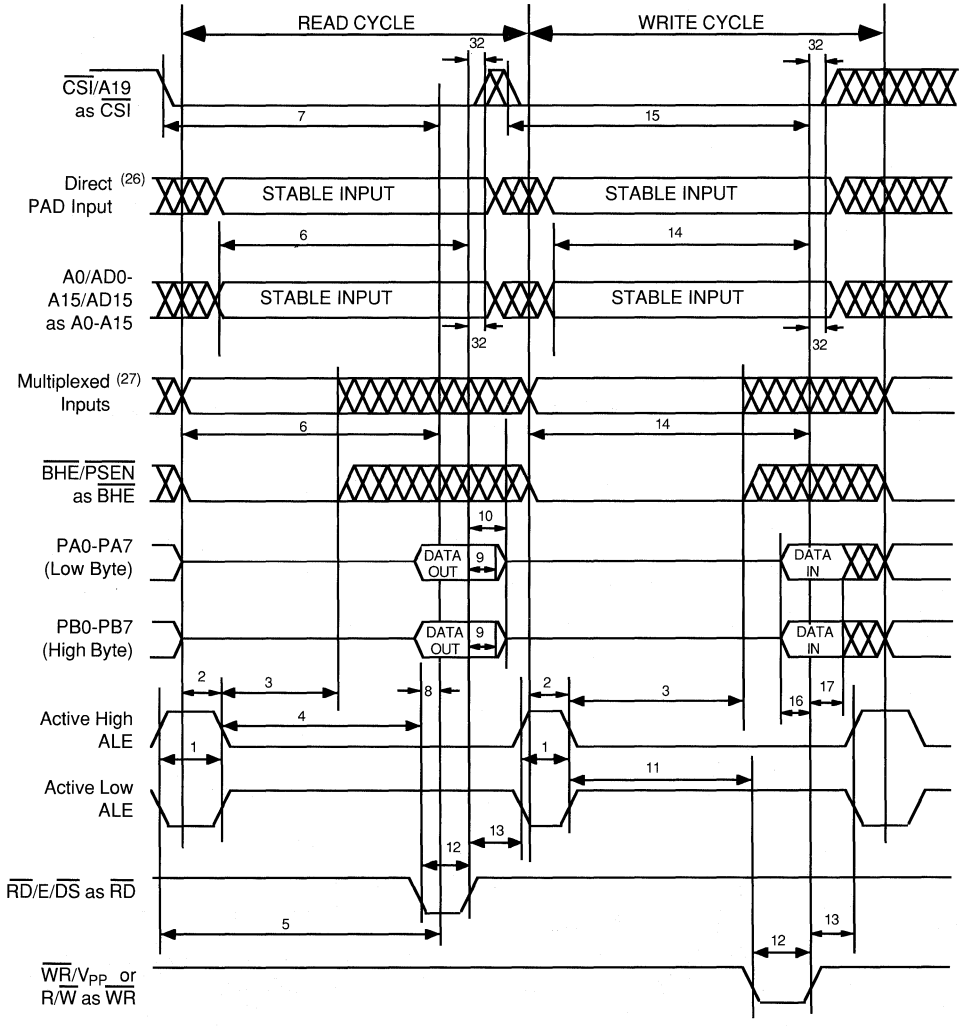
See referenced notes on page 2-201.

Figure 20. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



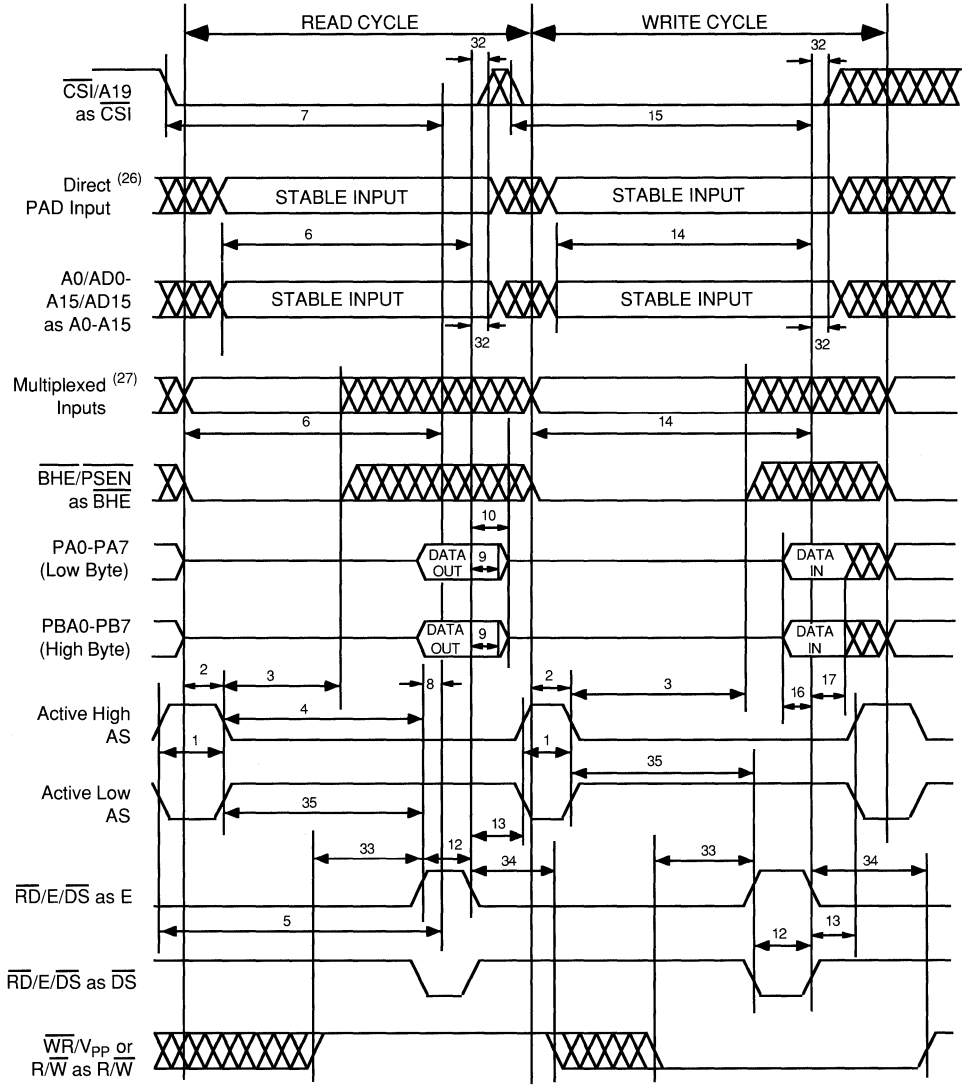
See referenced notes on page 2-201.

Figure 21. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-201.

Figure 22. Timing of 16-Bit Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-201.

Figure 23. Chip-Select Output Timing

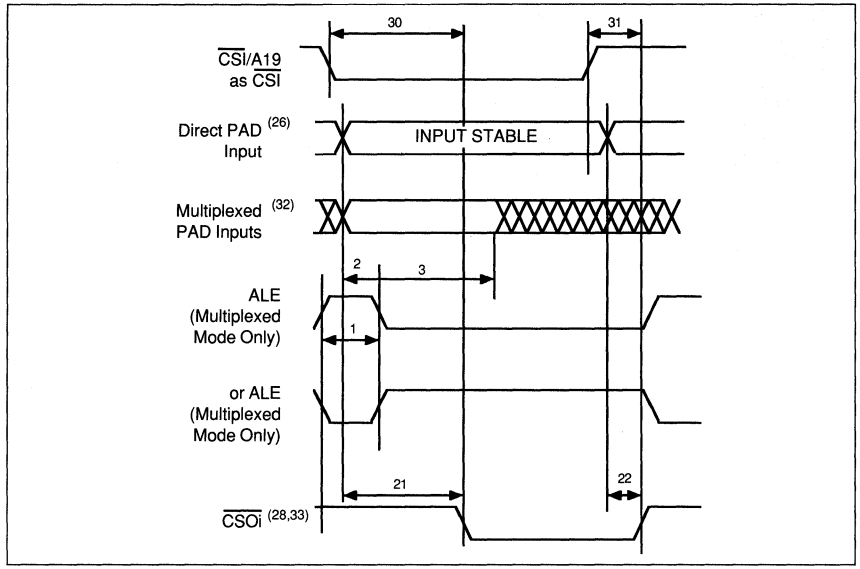
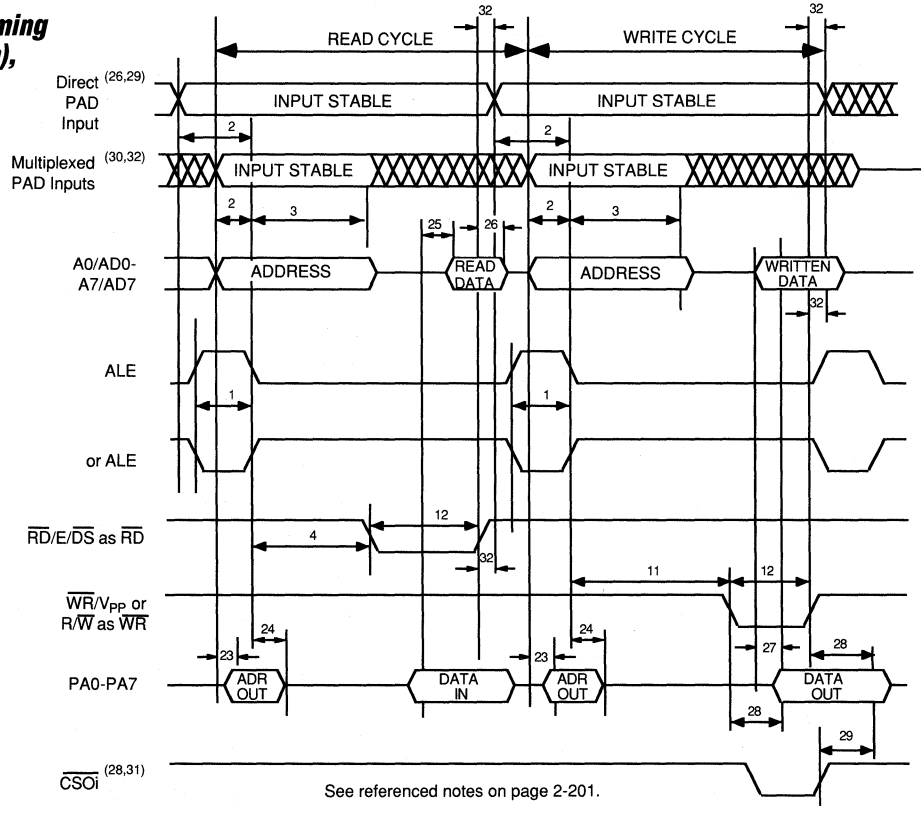
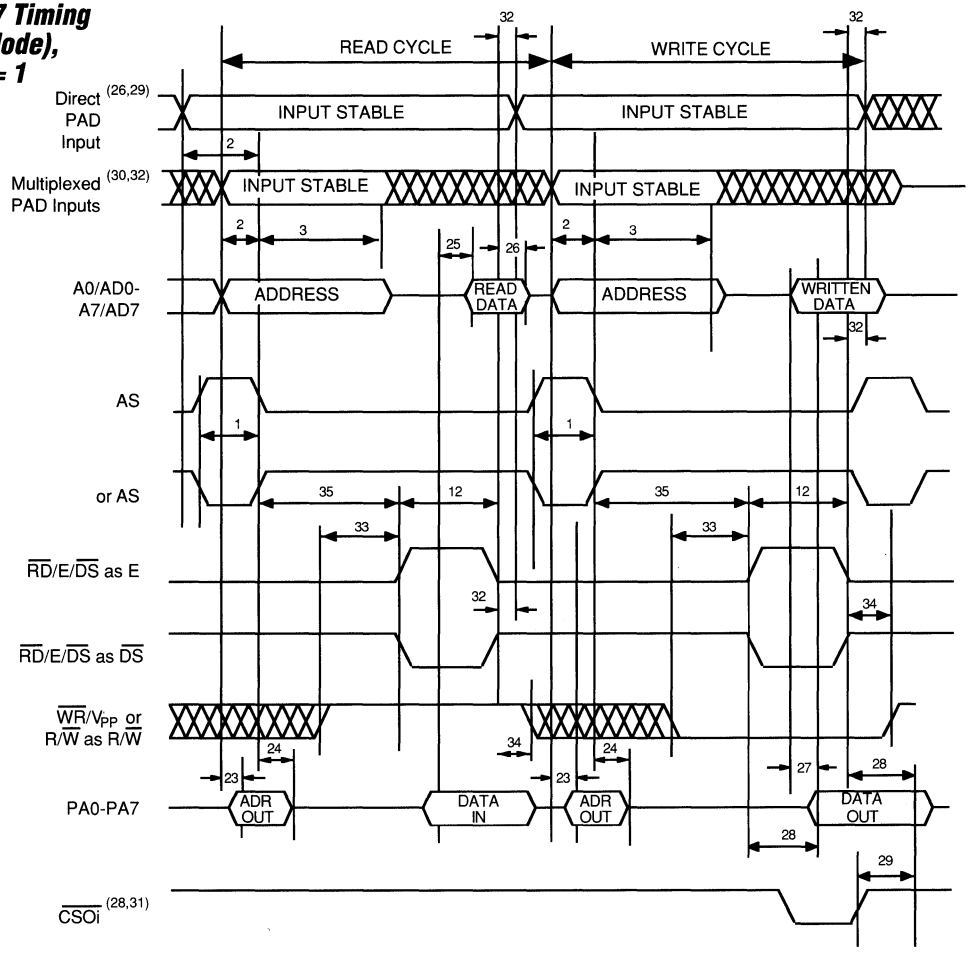


Figure 24. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-201.

Figure 25. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

26. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
27. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
28. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
29. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
30. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
31. The write operation signals are included in the $\overline{CSOi}$ expression.
32. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11/AD11–A15/AD15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
33. $\overline{CSOi}$ product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 14. Pin Capacitance[34]

T_A = 25 °C, f = 1 MHz

Symbol	Parameter	Conditions	Typical[35]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	V_{PP} = 0 V	18	25	pF

NOTES: 34. This parameter is only sampled and is not 100% tested.
35. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 26. AC Testing Input/Output Waveform

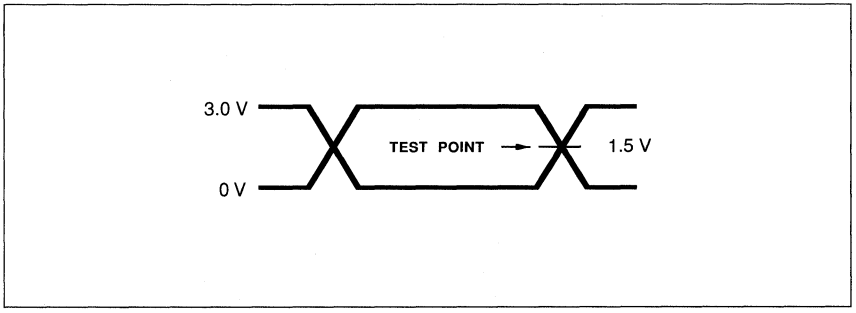
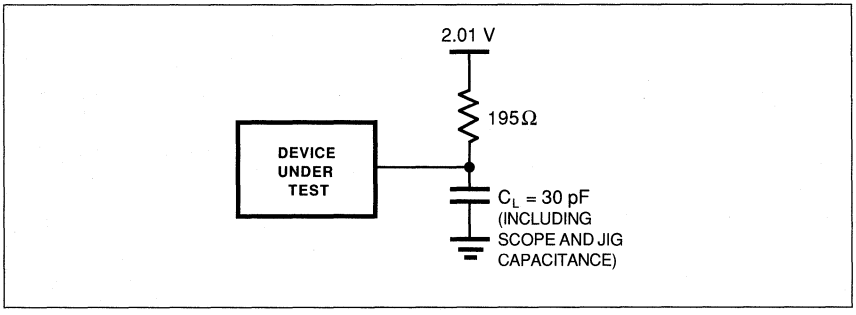


Figure 27. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD303 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD303 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package
$\overline{BHE}/\overline{PSEN}$	1	A_5
$\overline{WR}/V_{PP}$ or $R/\overline{W}$	2	A_4
RESET	3	B_4
PB7	4	A_3
PB6	5	B_3
PB5	6	A_2
PB4	7	B_2
PB3	8	B_1
PB2	9	C_2
PB1	10	C_1
PB0	11	D_2
GND	12	D_1
ALE or AS	13	E_1
PA7	14	E_2
PA6	15	F_1
PA5	16	F_2
PA4	17	G_1
PA3	18	G_2
PA2	19	H_2
PA1	20	G_3
PA0	21	H_3
$\overline{RD}/E/\overline{DS}$	22	G_4
AD0/A0	23	H_4
AD1/A1	24	H_5
AD2/A2	25	G_5
AD3/A3	26	H_6
AD4/A4	27	G_6
AD5/A5	28	H_7
AD6/A6	29	G_7
AD7/A7	30	G_8
AD8/A8	31	F_7
AD9/A9	32	F_8
AD10/A10	33	E_7
GND	34	E_8
AD11/A11	35	D_8
AD12/A12	36	D_7
AD13/A13	37	C_8
AD14/A14	38	C_7
AD15/A15	39	B_8
PC0	40	B_7
PC1	41	A_7
PC2	42	B_6
A19/$\overline{CSI}$	43	A_6
V_{CC}	44	B_5

Package Information

Figure 28. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L

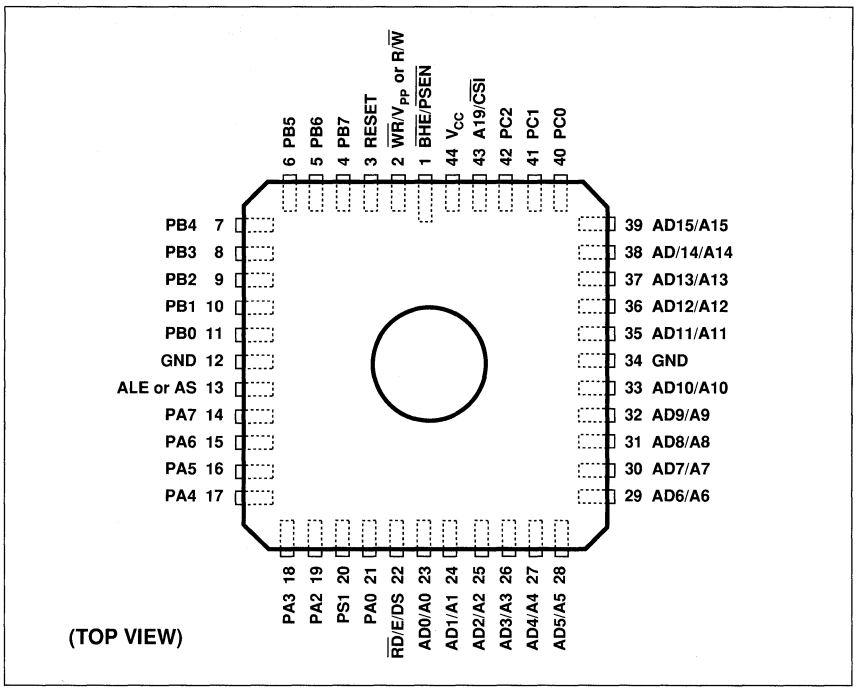


Figure 29. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

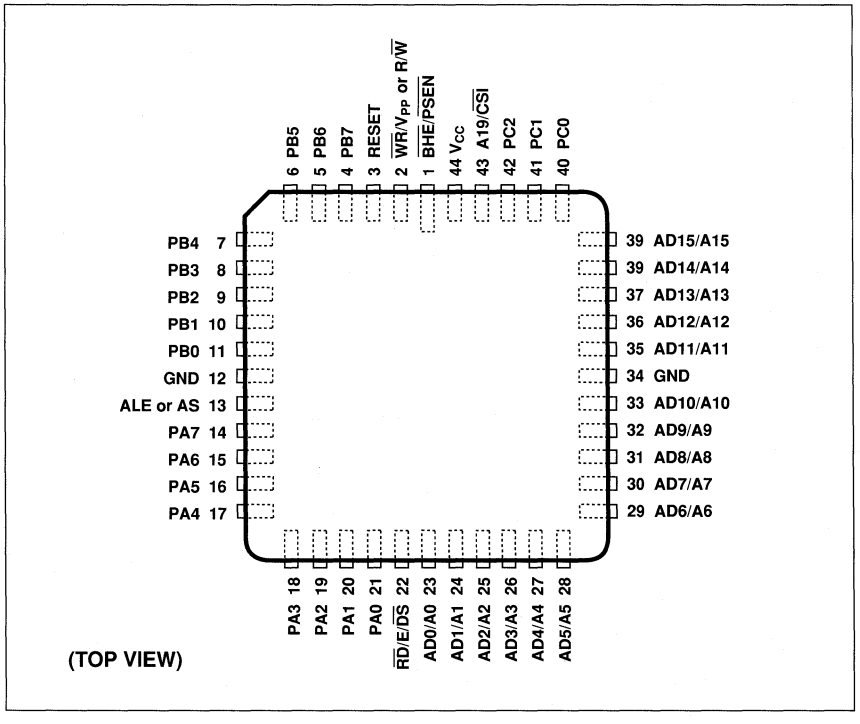
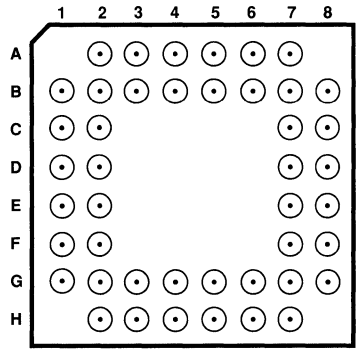


Figure 30: Drawing X2 — 44-Pin CPGA (Package Type X)



(TOP VIEW, THROUGH PACKAGE)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD303-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD303-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD303-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD303-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD303-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD303-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD303-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD303-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD303-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD303-15XM	150	44-pin CPGA	X2	Military	Standard
PSD303-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD303-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD303-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD303-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD303-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD303-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD303-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD303-20XM	200	44-pin CPGA	X2	Military	Standard
PSD303-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

System Development Tools

The PSD303 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD303 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD303 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD303 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD303 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD303 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD303 device, which then can be used in the target system. The development cycle is depicted in Figure 31.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD303 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two PSD303 Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

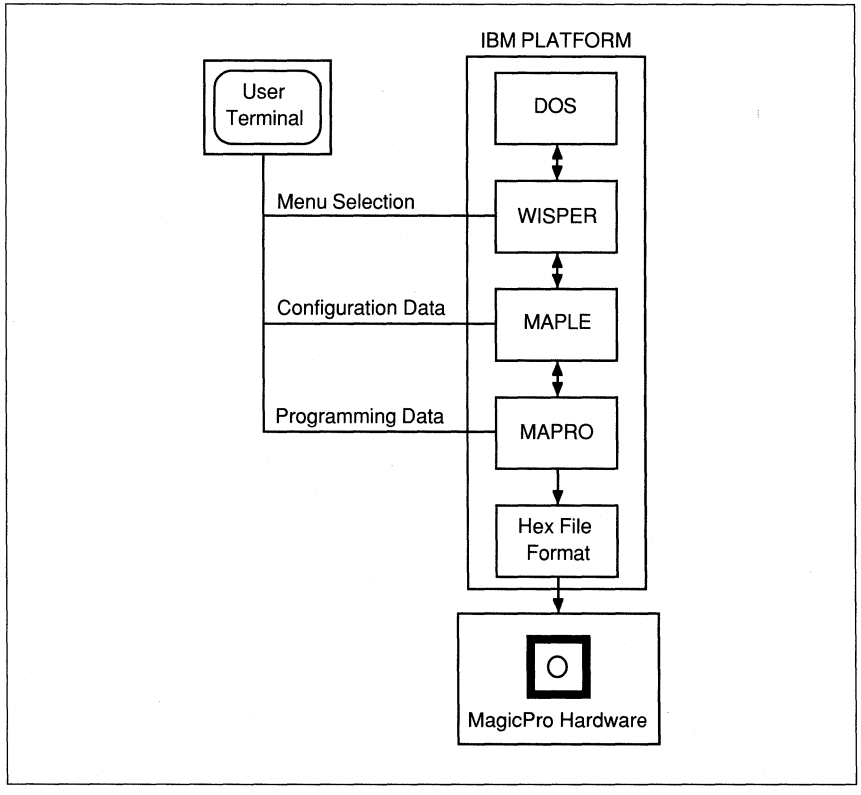
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA

Figure 31. PSD303 Development Cycle



Programmable Peripheral

PSD313

Programmable Microcontroller Peripheral with Memory

Key Features

- ❑ Single Chip Programmable Peripheral for Microcontroller-based Applications
- ❑ 19 Individually Configurable I/O pins that can be used as
  - — Microcontroller I/O port expansion
  - — Programmable Address Decoder (PAD) I/O
  - — Latched address output
  - — Open drain or CMOS
- ❑ Two Programmable Arrays (PAD A & PAD B)
  - — Total of 40 Product Terms and up to 16 Inputs and 24 Outputs
  - — Direct Address Decoding up to 1 Meg address space and up to 16 Meg with paging
  - — Logic replacement
- ❑ "No Glue" Microcontroller Chip-Set
  - — Built-in address latches for multiplexed address/data bus
  - — Non-multiplexed address/data bus mode
  - — 8 bit data bus width
  - — ALE and Reset polarity programmable
  - — Selectable modes for read and write control bus as $\overline{RD}/\overline{WR}$, $R/\overline{W}/E$, or $R/\overline{W}/\overline{DS}$
  - — PSEN/ pin for 8051 users
- ❑ Built-In Page Logic
  - — To Expand the Address Space of Microcontrollers with Limited Address Space Capabilities
  - — Up to 16 pages
- ❑ 1 Mbit of UV EPROM
  - — Organized as 128K x 8
  - — Divides into 8 equal mappable blocks for optimized mapping
  - — Block resolution is 16K x 8
  - — 120 ns EPROM access time, including input latches and PAD address decoding.
- ❑ 16 Kbit Static RAM
  - — Organized as 2K x 8
  - — 120 ns SRAM access time, including input latches and PAD address decoding
- ❑ Address/Data Track Mode
  - — Enables easy Interface to Shared Resources (Mail Box SRAM) with other Microcontrollers or a Host Processor
- ❑ Built-In Security
  - — Locks the PSD313 Configuration and PAD Decoding
- ❑ Available in a Variety of Packaging
  - — 44 Pin PLDCC and CLDCC
  - — 44 Pin CPGA
- ❑ Simple Menu-Driven Software: Configure the PSD313 on an IBM PC
- ❑ Downward Pin and Functionally Compatible with the PSD311 and PSD313

Partial Listing of Microcontrollers Supported

- ❑ **Motorola family:** M6805, M68HC11, M68HC16, M68000/10/20, M60008, M683XX
- ❑ **Intel family:** 8031/8051, 8096/98, 80186/88, 80196/98
- ❑ **Signetics:** SC80C451
- ❑ **Zilog:** Z8, Z80, Z180
- ❑ **National:** HPC16000

Applications

- ❑ Computers (Workstations and PCs)
  - — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- ❑ Telecommunications
  - — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- ❑ Industrial
  - — Robotics, Power Line Access, Power Line Motor
- ❑ Medical Instrumentation
  - — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- ❑ Military
  - — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Introduction

The PSD313 is the latest member in the rapidly growing WSI family of PSD devices. The PSD313 is ideal for microcontroller-based applications, where fast time-to-market, small form factor, and low power consumption are essential. When combined in a system, virtually any microcontroller (68HC11, 8051 etc.) and the PSD313 work together to create a very powerful chip-set solution. This implementation provides all the required control and peripheral elements of a microcontroller-based system peripheral with no external discrete "glue" logic required.

The solution comes complete with simple system software development tools for integrating the PSD313 with the microcontroller. Hosted on the IBM PC platforms or compatibles, the easy to use software enables the designer complete freedom in designing the system.

Product Description

The PSD313 integrates high performance user-configurable blocks of EPROM, SRAM, and programmable logic technology to provide a single chip microcontroller interface. The major functional blocks include two programmable logic arrays, PAD A and PAD B, 1 Mbit of EPROM, 16K bits of SRAM, input latches, and output ports. The PSD313 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD313 offers a unique single-chip solution for microcontrollers that need:

- ❑ I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- ❑ More EPROM and SRAM than the microcontroller's internal memory.
- ❑ Chip-select, control, or latched address lines that are otherwise implemented discretely.
- ❑ An interface to shared external resources.
- ❑ Expanding address space of microcontrollers

WSI's PSD313 (shown in Figure 1) can efficiently interface with, and enhance, any microcontroller system. This is the first solution that provides microcontrollers with port expansion, latched addresses, page logic, two programmable logic arrays PAD A and PAD B, an interface to shared resources, 1 Mbit EPROM, and 16K bit SRAM on a single chip. The PSD313 does not require any glue logic for interfacing to any 8-bit microcontroller.

The 8051 microcontroller family can take full advantage of the PSD313's separate program and data address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E, or the R/$\overline{W}$ and $\overline{DS}$ signals. Address and data buses can be configured to be separate or multiplexed, whichever is required by the host processor.

Product Discription (Cont.)

The flexibility of the PSD313 I/O ports permits interfacing to shared resources. The arbitration can be controlled internally by PAD A outputs. The user can assign the following functions to these ports: standard I/O pins, chip-select outputs from the PAD A and PAD B, or latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD313 on-chip programmable address decoder (PAD A) enables the user to map the I/O ports, eight segments of EPROM (16K x 8 each) and SRAM (2K x 8) anywhere in the address space of the microcontroller. PAD B can implement up to 4 sum-of-product expressions based on address inputs and control signals.

The page register extends the accessible address space of certain microcontrollers from 64K to 1 M. There are 16 pages that can serve as base address inputs to the PAD, thereby enlarging the address space of 16 address line processors by a factor of 16.

Figure 1. PSD313 Architecture

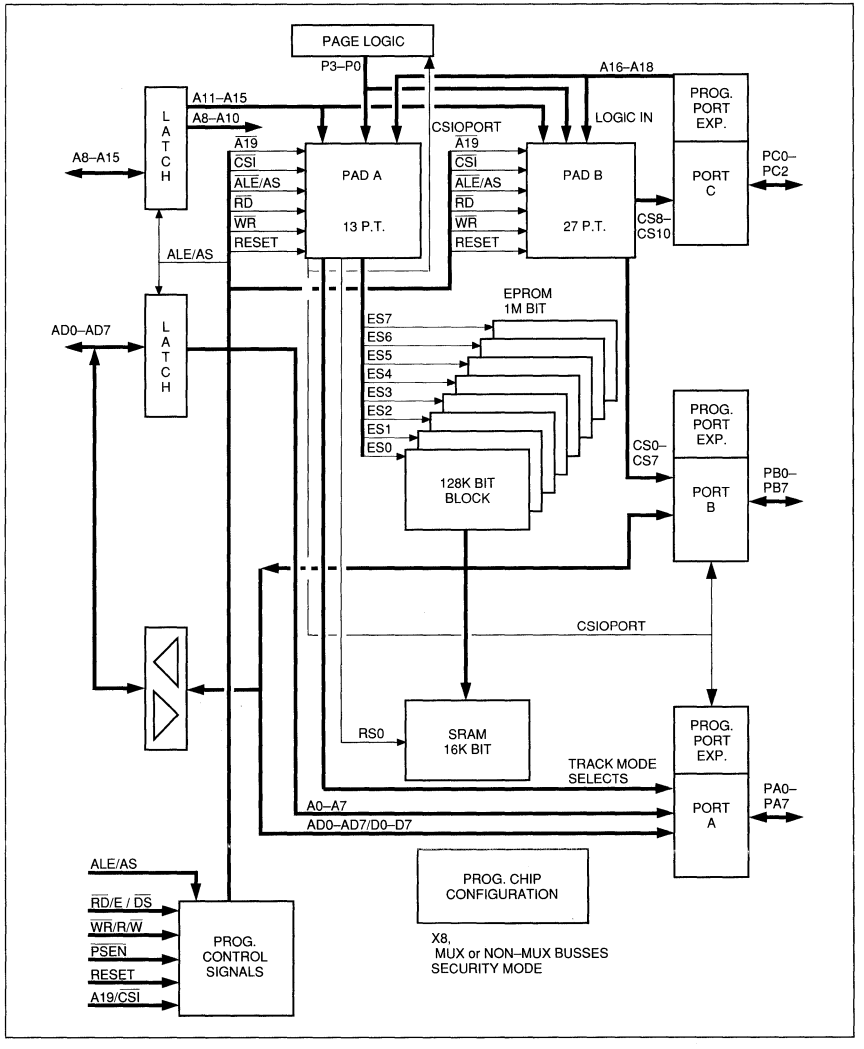


Table 1. PSD313 Pin Descriptions

Name	Type	Description
$\overline{PSEN}$	I	The $\overline{PSEN}$ is the active low EPROM read pulse. The SRAM and I/O ports read signal is generated according to the description of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$, and $\overline{RD}$/E/$\overline{DS}$ pins. If the host processor is a member of the 8031 family, $\overline{PSEN}$ must be connected to the corresponding host pin. In other 8-bit host processors that do not have a special EPROM-only read strobe, PSEN should be tied to V_{CC}. In this case, $\overline{RD}$ or E and R/$\overline{W}$ provide the read strobe for the SRAM, I/O ports, and EPROM.
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	I	In the operating mode, this pin's function is $\overline{WR}$ (CRRWR = 0) or R/$\overline{W}$ (CRRWR = 1) when configured as R/$\overline{W}$. The following tables summarize the read and write operations (CRRWR = 1): CEDS = 0 R/$\overline{W}$ | E | X | 0 | NOP 0 | 1 | write 1 | 1 | read CEDS = 1 R/$\overline{W}$ | $\overline{DS}$ | X | 1 | NOP 0 | 0 | write 1 | 0 | read When configured as $\overline{WR}$, a write operation is executed during an active low pulse. When configured as R/$\overline{W}$, with R/$\overline{W}$ = 1 and E = 1, a read operation is executed; if R/$\overline{W}$ = 0 and E = 1, a write operation is executed. In programming mode, this pin must be tied to V_{PP} voltage.
$\overline{RD}$/E/$\overline{DS}$	I	The pin function depends on the CRRWR and CEDS configuration bits. If CRRWR = 0, $\overline{RD}$ is an active low read pulse. When CRRWR = 1, this pin and the R/$\overline{W}$ pin define the following cycle type: If CEDS = 0, E is an active high strobe. If CEDS = 1, $\overline{DS}$ is an active low strobe.
$\overline{CSI}$/A19	I	This pin has two configurations. When it is $\overline{CSI}$ (CA19/$\overline{CSI}$ = 0) and the pin is asserted high, the device is deselected and powered down. (See Tables 10 and 11 for the chip state during power-down mode.) If the pin is asserted low, the chip is in normal operational mode. When it is configured as A19, (CA19/$\overline{CSI}$ = 1), this pin can be used as an additional input to the PAD. CADLOG3 = 1 defines the pin as an address; CADLOG3 = 0 defines it as a logic input. If it is an address, A19 can be latched with ALE (CADDHLT = 1) or be a transparent logic input (CADDHLT = 0). In this mode, there is no power-down capability.
RESET	I	This user-programmable pin can be configured to reset on high level (CRESET = 1) or on low level (CRESET = 0). It should remain active for at least 100 ns. See Tables 8 and 9 for the chip state after reset.

Legend: The I/O column abbreviations are: I = input; I/O = input/output; P = power.

NOTE: 1. All the configuration bits mentioned in Table 1 appear in parentheses and are explained in the Configuration Register section.

Table 1. PSD313 Pin Descriptions (Cont.)

Name	Type	Description
ALE or AS	I	In the multiplexed modes, the ALE pin functions as an Address Latch Enable or as an Address strobe and can be configured as an active high or active low signal. The ALE or AS trailing edge latches lines AD15/A15–AD0/A0, A16–A19, and $\overline{BHE}$, depending on the PSD313 configuration. See Table 7. In the non-multiplexed modes, it can be used as a general-purpose logic input to the PAD.
PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0	I/O	PA7–PA0 is an 8-bit port that can be configured to track AD7/A7–AD0/A0 from the input (CPAF2 = 1). Otherwise (CPAF2 = 0), each bit can be configured separately as an I/O or lower-order latched address line. When configured as an I/O (CPAF1 = 0), the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data bit (which resides in the data register) comes out. When it is configured as a low-order address line (CPAF1 =1), A7–A0 can be made the corresponding output through this port (e.g., PA6 can be configured to be the A6 address line). Each port bit can be a CMOS output (CPACOD = 0) or an open drain output (CPACOD = 1). When the chip is in non-multiplexed mode (CADDRAT = 0), the port becomes the data bus lines (D0–D7). See Figure 4.
PB7 PB6 PB5 PB4 PB3 PB2 PB0	I/O	PB7–PB0 is an 8-bit port for which each bit can be configured as an I/O (CPBF = 1) or chip-select output (CPBF = 0). Each port bit can be a CMOS output (CPBCOD = 0) or an open drain output (CPBCOD = 1). When configured as an I/O, the direction of the pin is defined by its direction bit, which resides in the direction register. If a pin is an I/O output, its data (which resides in the data register) comes out. When configured as a chip-select output, $\overline{CS0}$–$\overline{CS3}$ are a function of up to four product terms of the inputs to the PAD B; $\overline{CS4}$,–$\overline{CS7}$ then are each a function of up to two product terms. See Figure 6.
PC0 PC1 PC2	I/O	This is a 3-bit port for which each bit is configurable as a PAD A and B input or output. When configured as an input (CPCF = 0), a bit individually becomes an address (CADLOG = 1) or a logic input (CADLOG = 0). The addresses can be latched with ALE (CADDHLT = 1) or be transparent inputs to the PADs (CADDHLT = 0). When a pin is configured as an output (CPCF = 1), it is a function of one product term of all PAD inputs. See Figure 7.

Table 1. PSD313 Pin Descriptions (Cont.)

Name	Type	Description
AD0/A0 AD1/A1 AD2/A2 AD3/A3 AD4/A4 AD5/A5 AD6/A6 AD7/A7	I/O	In multiplexed mode, these pins are the multiplexed low-order address/data byte. After ALE latches the addresses, these pins input or output data, depending on the settings of the $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and $\overline{PSEN}$ pins. In non-multiplexed mode, these pins are the low-order address input.
A8 A9 A10 A11 A12 A13 A14 A15	I/O	These pins are the high-order address input.
GND	P	V_{SS} (ground) pin.
V_{CC}	P	Supply voltage input.

Operating Modes

The PSD313's two operating modes allow it to interface directly to 8-bit microcontrollers with multiplexed and non-multiplexed address/data buses. These operating modes are described below.

Multiplexed 8-bit Address/Data Bus

This mode is used to interface to microcontrollers with an 8-bit data bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is bidirectional and permits the latching of the address when the ALE signal is active. On the same pins, the data is read from or written to the device; this depends on the state of the $\overline{RD}$/E/$\overline{DS}$, $\overline{PSEN}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins. The high-order address bus (A8–A15) contains the high-order address bus byte. Ports A and B can be configured as in Table 2.

Non-Multiplexed Address/Data, 8-bit Data Bus

This mode is used to interface to a microcontroller with an 8-bit non-multiplexed bus and a 16-bit or larger address bus. The low-order address/data bus (AD0/A0–AD7/A7) is the low-order address input bus. The high-order address/data bus (A8–A15) is the high-order address bus byte. Port A is the low-order data bus. Port B can be configured as shown in Table 2.

Table 2 summarizes the effect of the different operating modes on ports A, B, and the address/data pins. The configuration of Port C is independent of the four operating modes.

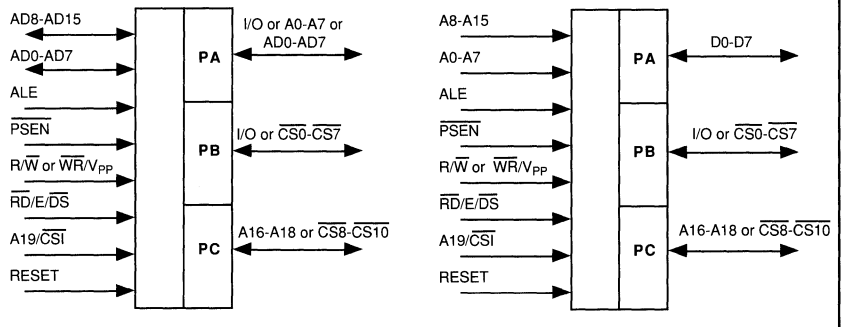
Programmable Address Decoder (PAD)

The PSD313 consists of two programmable arrays referred to as PAD A and PAD B (Figure 3). PAD A is used to generate chip select signals derived from the input address to the internal EPROM blocks, SRAM, I/O ports, and Track Mode signals. All its I/O functions are listed in Table 3 and shown in Figure 3. PAD B outputs to Ports B and C for off-chip usage.

PAD B can also be used to extend the decoding to select external devices or as a random logic replacement. The input bus to both PAD A and PAD B is the same. Using WSI's MAPLE software, each programmable bit in the PAD's array can have one of three logic states of 0, 1, and don't care (X). In a user's logic design, both PADs can share the same inputs using the X for input signals that are not supposed to affect other functions. The PADs use reprogrammable CMOS EPROM technology and can be programmed and erased by the user.

Figure 2. PSD313 Port Configurations

Figure 2 shows the PSDS313's I/O port configurations.



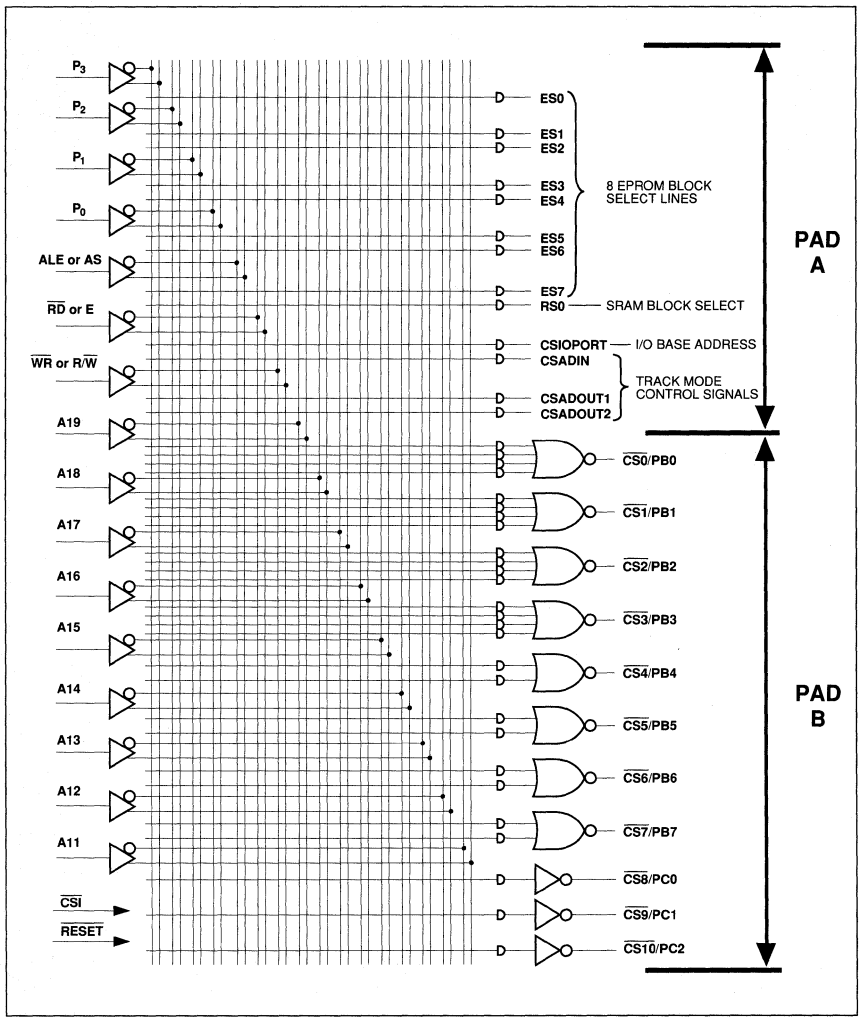
1. PSD313 configured for multiplexed 16-bit address/data bus.
2. PSD313 configured for non-multiplexed address/data, 8-bit bus.

Legend: AD0–AD7 = Addresses A0–A7 multiplexed with data lines D0–D7.

Table 2. PSD313 Bus and Port Configuration Options

	Multiplexed Address/Data	Non-Multiplexed Address/Data
8-bit Data Bus		
Port A	I/O or low-order address lines or Low-order multiplexed address/data byte	D0–D7 data bus byte
Port B	I/O or $\overline{CS0}$–$\overline{CS7}$	I/O and/or $\overline{CS0}$–$\overline{CS7}$
AD0/A0–AD7/A7	Low-order multiplexed address/data byte	Low-order address bus byte
A8–A15	High-order address bus byte	High-order address bus byte

Figure 3. PSD313 PAD Description



NOTES: 2. $\overline{CSI}$ is a power-down signal. When high, the PAD is in stand-by mode and all its outputs become non-active. See Tables 10 and 11.
3. RESET deselects all PAD output signals. See Tables 8 and 9.
4. A18, A17, and A16 are internally multiplexed with $\overline{CS10}$, $\overline{CS9}$, and $\overline{CS8}$, respectively. Either A18 or $\overline{CS10}$, A17 or $\overline{CS9}$, and A16 or $\overline{CS8}$ can be routed to the external pins of Port C. Port C can be configured as either input or output.

Table 3. PSD313 PAD A and B I/O Functions

	Function
PAD A and PAD B Inputs	
$\overline{CSI}$ or A19	In $\overline{CSI}$ mode (when high), PAD deselects all of its outputs and enters a power-down mode (see Tables 10 and 11). In A19 mode, it is another input to the PAD.
A16–A18	These are general purpose inputs from Port C. See Figure 3, Note 4.
A11–A15	These are address inputs.
P0–P3	These are page number inputs.
$\overline{RD}$ or E	This is the read pulse or enable strobe input.
$\overline{WR}$ or R/$\overline{W}$	This is the write pulse or R/$\overline{W}$ select signal.
ALE	This is the ALE input to the chip.
RESET	This deselects all outputs from the PAD; it can not be used in product term equations. See Tables 8 and 9.
PAD A Outputs	
ES0–ES7	These are internal chip-selects to the 8 EPROM banks. Each bank can be located on any boundary that is a function of one product term of the PAD address inputs.
RS0	This is an internal chip-select to the SRAM. Its base address location is a function of one term of the PAD address inputs.
CSIOPORT	This internal chip-select selects the I/O ports. It can be placed on any boundary that is a function of one product term of the PAD inputs. See Table 6.
CSADIN	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the input direction of Port A. CSADIN is gated externally to the PAD by the internal read signal. When CSADIN and a read operation are active, data presented on Port A flows out of AD0/A0–AD7/A7. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT1	This internal chip-select, when Port A is configured as a low-order address/data bus in track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT1 is gated externally to the PAD by the ALE signal. When CSADOUT1 and the ALE signal are active, the address presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
CSADOUT2	This internal chip-select, when Port A is configured as a low-order address/data bus in the track mode (CPAF2 = 1), controls the output direction of Port A. CSADOUT2 must include the write-cycle control signals as part of its product term. When CSADOUT2 is active, the data presented on AD0/A0–AD7/A7 flows out of Port A. This chip-select can be placed on any boundary that is a function of one product term of the PAD inputs. See Figure 5.
PAD B Outputs	
$\overline{CS0}$–$\overline{CS3}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to four product terms of the PAD inputs.
$\overline{CS4}$–$\overline{CS7}$	These chip-select outputs can be routed through Port B. Each of them is a function of up to two product terms of the PAD inputs.
$\overline{CS8}$–$\overline{CS10}$	These chip-select outputs can be routed through Port C. See Figure 3, Note 4. Each of them is a function of one product term of the PAD inputs.

Configuration Bits

The configuration bits shown in Table 4 are non-volatile cells that let the user set the device, I/O, and control functions to the proper operational mode. Table 5 lists all configuration bits. The configuration bits are programmed and verified during the programming phase. In operational mode, they are not accessible. To simplify implementing a specific mode, use the WSI's PSD313 MAPLE software to set the bits.

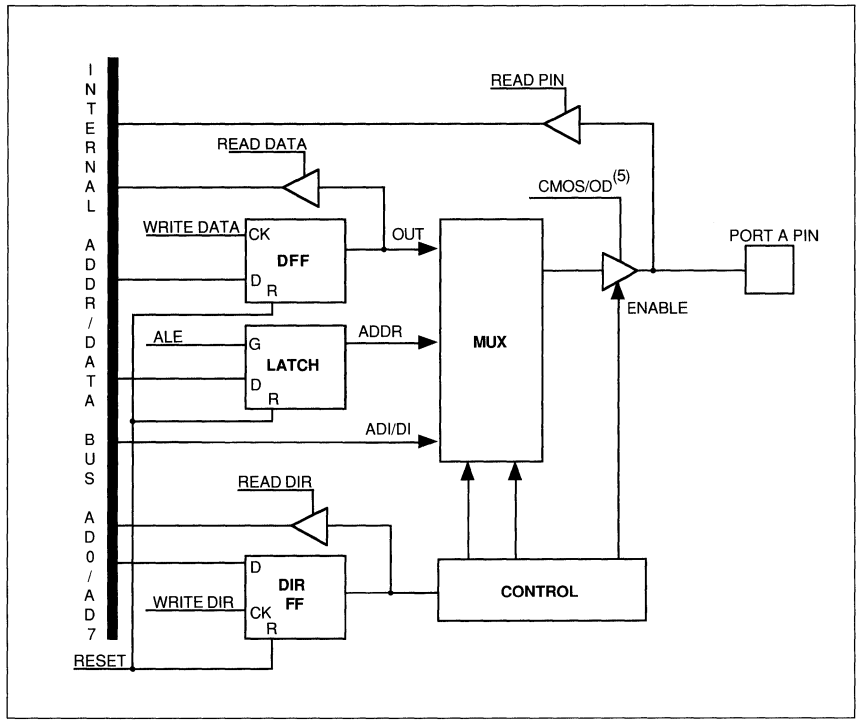
Table 4. PSD313 Non-Volatile Configuration Bits

Use This Bit	To
CADDRDAT	Set the address/data bus to multiplexed or non-multiplexed mode.
CEDS	Determine the polarity and functionality of read and write.
CA19/$\overline{CSI}$	Set A19/$\overline{CSI}$ to $\overline{CSI}$ (power-down) or A19 input.
CALE	Set the ALE polarity.
CPAF2	Set Port A either to track the low-order byte of the address/data multiplexed bus or to select the I/O or address option.
CSECURITY	Set the security on or off (a secured part can not be duplicated).
CRESET	Set the RESET polarity.
COMB/SEP	Set $\overline{PSEN}$ and $\overline{RD}$ for combined or separate address spaces (see Figures 8 and 9).
CPAF1 (8 Bits)	Configure each pin of Port A in multiplexed mode to be an I/O or address output.
CPACOD (8 Bits)	Configure each pin of Port A as an open drain or active CMOS pull-up output.
CPBF (8 Bits)	Configure each pin of Port B as an I/O or a chip-select output.
CPBCOD (8 Bits)	Configure each pin of Port B as an open drain or active CMOS pull-up output.
CPCF (3 Bits)	Configure each pin of Port C as an address input or a chip-select output.
CADDHLT	Configure pins A16–A19 to go through a latch or to have their latch transparent.
CADLOG (4 Bits)	Configure A16–A19 individually as logic or address inputs.
CLOT	Determine in non-multiplexed mode if address inputs are transparent or latched.
CRRWR	Configure the polarity and control methods of read and write cycles.

Port Functions

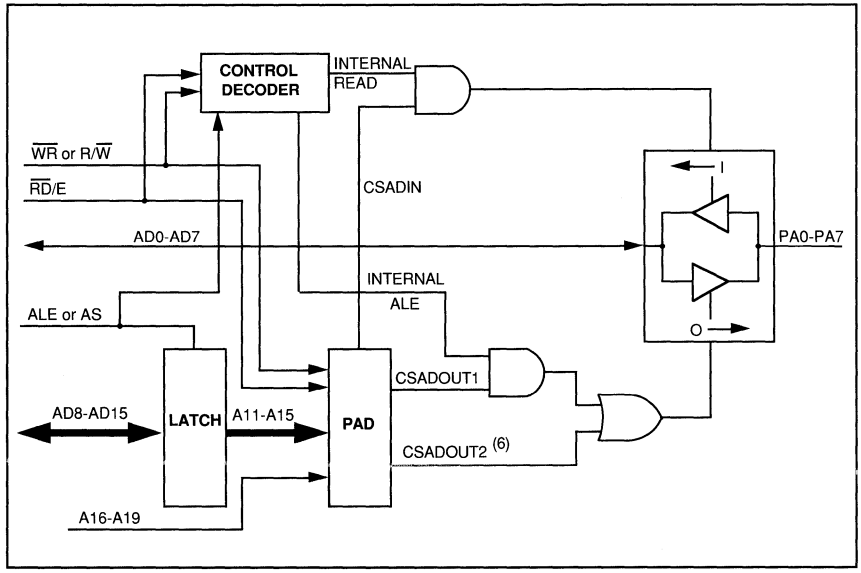
The PSD313 has three I/O ports (Ports A, B, and C) that are configurable at the bit level. This permits great flexibility and a high degree of customization for specific applications. The following is a description of each port. Figure 4 shows the pin structure of Port A.

Figure 4. Port A Pin Structure



NOTE: 5. CMOS/OD determines whether the output is open drain or CMOS.

Figure 5. Port A Track Mode



NOTE: 6. The expression for CSADOUT2 must include the following write operation cycle signals:
For CRRWR = 0, CSADOUT2 must include $\overline{WR}$ = 0.
For CRRWR = 1, CSADOUT2 must include E = 1 and R/$\overline{W}$ = 0.

Table 5. PSD313 Configuration Bits[7,8]

Configuration Bits	No. of Bits	Function
CADDRDAT	1	ADDRESS/DATA Multiplexed (separate buses) CADDRDAT = 0, non-multiplexed CADDRDAT = 1, multiplexed
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$ CA19/$\overline{CSI}$ = 0, enable power-down CA19/$\overline{CSI}$ = 1, enable A19 input to PAD
CALE	1	Active HIGH or Active LOW CALE = 0, Active high CALE = 1, Active low
CRESET	1	Active HIGH or Active LOW CRESET = 0, Active low RESET CRESET = 1, Active high RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM 0 = Combined, 1 = Separate
CPAF2	1	Port A AD0–AD7 (address/data multiplexed bus) CPAF2 = 0, address or I/O on Port A (according to CPAF1) CPAF2 = 1, address/data multiplexed on Port A (track mode)
CADDHLT	1	A16–A19 Transparent or Latched CADDHLT = 0, Address latch transparent CADDHLT = 1, Address latched (ALE dependent)
CSECURITY	1	SECURITY On/Off CSECURITY = 0, off CSECURITY = 1, on
CLOT	1	A0–A15 Address Inputs are transparent or ALE-dependent in non-multiplexed modes CLOT = 0, transparent CLOT = 1, ALE-dependent
CRRWR CEDS	2	Determine the polarity and control methods of read and write cycles. CEDS CRRWR 0 0 $\overline{RD}$ and $\overline{WR}$ active low pulses 0 1 R/$\overline{W}$ status and high E pulse 1 1 R/$\overline{W}$ status and low $\overline{DS}$ pulse
CPAF1	8	Port A I/O or A0–A7 CPAF1 = 0, Port A pin is I/O CPAF1 = 1, Port A pin is Ai ($0 \le i \le 7$)
CPACOD	8	Port A CMOS or Open Drain Output CPACOD = 0, CMOS output CPACOD = 1, open-drain output
CPBF	8	Port B is I/O or $\overline{CS0}$– $\overline{CS7}$ CPBF = 0, Port B pin is $\overline{CSI}$ ($0 \le i \le 7$) CPBF = 1, Port B pin is I/O

Table 5. PSD313 Configuration Bits (Cont.)

Configuration Bits	No. of Bits	Function
CPBCOD	8	Port B CMOS or Open Drain CPBCOD = 0, CMOS output CPBCOD = 1, open-drain output
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$ CPCF = 0, Port C pin is Ai ($16 \le i \le 18$) CPCF = 1, Port C pin is $\overline{CSI}$ ($8 \le i \le 10$)
CADLOG	4	A16–A19 Address or Logic Input CADLOG = 0, Port C pin or A19/$\overline{CSI}$ is logic input CADLOG = 1, Port C pin or A19/$\overline{CSI}$ is Ai ($16 \le i \le 19$)
Total Bits	**50**	

NOTES: 7. WSI's MAPLE software will guide the user to the proper configuration choice.
8. In an unprogrammed or erased part, all configuration bits are 0.

2

Port Functions (Cont.)

Port A in Multiplexed Address/Data Mode

The default configuration of Port A is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 4). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 4). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port A pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6.

Alternatively, each bit of Port A can be configured as a low-order latched address bus bit. The address is provided by the port address latch, which latches the address on the trailing edge of ALE. PA0–PA7 can become A0–A7, respectively. This feature of the PSD313 lets the user generate low-order address bits to access external peripherals or memory that require several low-order address lines.

Another mode of Port A (CPAF2 = 1) sets the entire port to track the inputs AD0/A0–AD7/A7, depending on specific address ranges defined by the PAD's CSADIN, CSADOUT1, and CSADOUT2 signals. This feature lets the user interface the microcontroller to shared external resources without requiring external buffers and decoders. In this mode, the port is effectively a bi-directional buffer. The direction is controlled by using the input signals ALE, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$/V_{PP} or R/$\overline{W}$, and the internal PAD outputs CSADOUT1, CSADOUT2 and CSADIN (see Figure 5). When CSADOUT1 and ALE are true, the address on the input AD0/A7–AD7/A7 pins flows out through Port A. (Carefully check the generation of CSADOUT1, and ensure that it is stable during the ALE pulse; see Figure 18). When CSADOUT2 is active, a write operation is performed (see note to Figure 5). The data on the input AD0/A7–AD7/A7 pins flows out through Port A. When CSADIN and a read operation is performed (depending on the mode of the $\overline{RD}$/E/$\overline{DS}$ and $\overline{WR}$/V_{PP} or R/$\overline{W}$ pins), the data on Port A flows out through the AD0/A7–AD7/A7 pins. In this operational mode, Port A is tri-stated when none of the above-mentioned three conditions exist.

Port Functions (Cont.)

Port A in Non-Multiplexed Address/Data Mode

In this mode, Port A becomes the low order data bus byte of the chip. When reading an internal PSD313 location, data is presented on Port A pins. When writing to an internal PSD313 location, data present on Port A pins is written to that location.

Port B

The default configuration of Port B is I/O. In this mode, every pin can be set as an input or output by writing into the respective pin's direction flip flop (DIR FF, in Figure 6). As an output, the pin level can be controlled by writing into the respective pin's data flip flop (DFF, in Figure 6). When DIR FF = 1, the pin is configured as an output. When DIR FF = 0, the pin is configured as an input. The controller can read the DIR FF bits by accessing the READ DIR register; it can read the DFF bits by accessing the READ DATA register. Port B pin levels can be read by accessing the READ PIN register. Individual pins can be configured as CMOS or open drain outputs. Open drain pins require external pull-up resistors. For addressing information, refer to Table 6

Alternatively, each bit of Port B can be configured to provide a chip-select output signal from PAD B. PB0–PB7 can provide $\overline{CS0}$–$\overline{CS7}$, respectively. Each of the signals $\overline{CS0}$–$\overline{CS3}$ is comprised of four product terms.Thus, up to four ANDed expressions can be ORed while deriving any of these signals. Each of the signals $\overline{CS4}$–$\overline{CS7}$ is comprised of two product terms. Thus, up to two ANDed expressions can be ORed while deriving any of these signals.

Accessing the I/O Port Registers

Table 6 shows the offset values with the respect to the base address defined by the CSIOPORT. They let the user access the corresponding registers.

Port C in All Modes

Each pin of Port C (shown in Figure 7) can be configured as an input to PAD A and PAD B or output from PAD B. As inputs, the pins are named A16–A18. Although the pins are given names of the high-order address bus, they can be used for any other address lines or logic inputs to PAD A and PAD B. For example, A8–A10 can also be connected to those pins, improving the boundaries of $\overline{CS0}$–$\overline{CS7}$ resolution to 256 bytes. As inputs, they can be individually configured to be logic or address inputs. A logic input uses the PAD only for Boolean equations that are implemented in any or all of the $\overline{CS0}$–$\overline{CS10}$ PAD B outputs. Port C addresses can be programmed to latch the inputs by the trailing edge ALE or to be transparent.

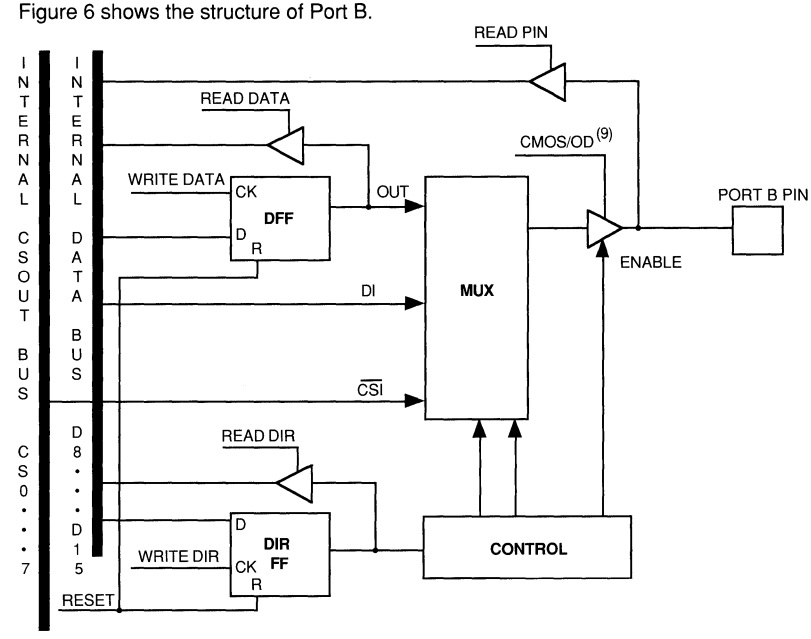
Alternatively, PC0–PC2 can become $\overline{CS8}$–$\overline{CS10}$ outputs, respectively, providing the user with more external chip-select PAD outputs. Each of the signals $\overline{CS8}$–$\overline{CS10}$ is comprised of one product term.

ALE/AS and AD0/A0–AD7/A7 in Non-Multiplexed Modes

In non-multiplexed modes, AD0/A0–AD15/A15 are address inputs only and can become transparent (CLOT = 0) or ALE dependent (CLOT = 1). In transparent mode, the ALE/AS pin can be used as an additional logic input to the PADs. The non-multiplexed ALE dependent mode is useful in applications for which the host processor has a multiplex address/data bus and AD0/A0–AD7/A7 are not multiplexed with A0–A7 but rather are multiplexed with other address lines. In these applications, Port A serves as a data bus and each of its pins can be directly connected to the corresponding host's multiplexed pin, where that data bit is expected. See Table 7.

Figure 6. Port B Pin Structure

Figure 6 shows the structure of Port B.

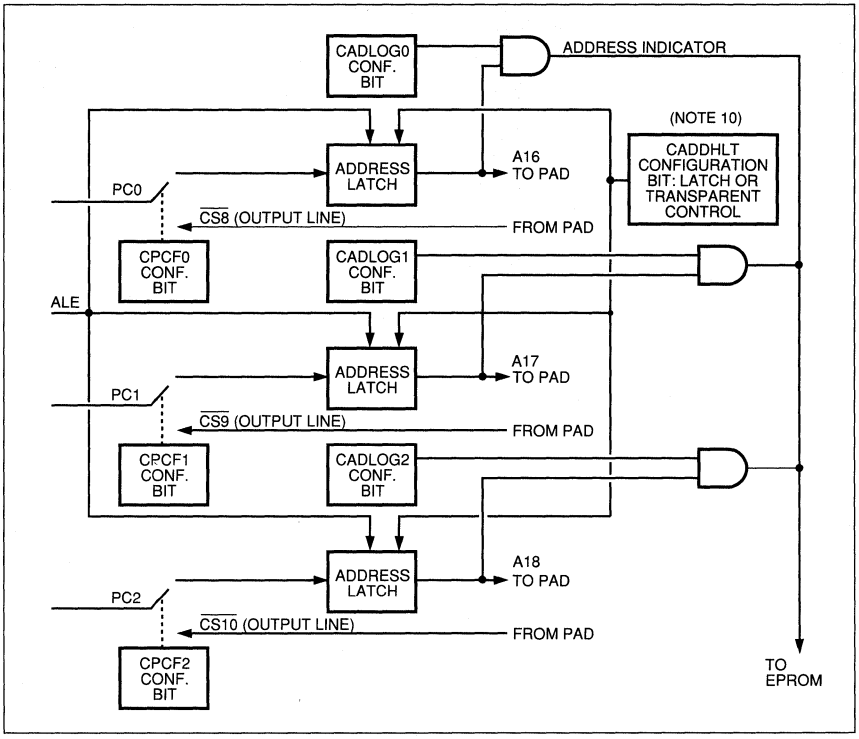


NOTE: 9. CMOS/OD determines whether the output is open drain or CMOS.

Table 6. I/O Port Addresses in an 8-bit Data Bus Mode

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Figure 7. Port C Structure



NOTE: 10. The CADDHLT configuration bit determines if A18–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

Table 7. Signal Latch Status in All Operating Modes

Signal Name	Configuration Bits	Configuration Mode	Signal Latch Status
AD0/A0-AD7/A7	CADDRDAT = 0, CLOT = 0	non-multiplexed modes	Transparent
	CADDRDAT = 0, CLOT = 1		ALE Dependent
	CADDRDAT = 1	multiplexed modes	ALE Dependent
$\overline{PSEN}$	CDATA = 0	8-bit data, $\overline{PSEN}$ is active	Transparent
A19 and PC2–PC0	CADDHLT = 0	A16–A19 can become logic inputs	Transparent
	CADDHLT = 1	A16–A19 can become multiplexed address lines	ALE Dependent

EPROM

The PSD313 has 1M bit of EPROM and is organized as 128K x 8. The EPROM has 8 banks of memory. Each bank can be placed in any address location by programming the PAD. Bank0–Bank7 can be selected by PAD outputs ES0–ES7, respectively. The EPROM banks are organized as 16K x 8.

SRAM

The PSD313 has 16K bits of SRAM and is organized as 2K x 8. The SRAM is selected by the RS0 output of the PAD.

Page Register

The page register consists of four flip-flops, which can be read from, or written to, through the I/O address space (CSIOPORT). The page register is connected to the D3–D0 lines. The Page Register address is CSIOPORT + 18H. The page register outputs are P3–P0, which are fed into the PAD. This enables the host microcontroller to enlarge its address space by a factor of 16 (there can be a maximum of 16 pages). See Figure 8.

Control Signals

The PSD313 control signals are $\overline{WR}/V_{PP}$ or R/$\overline{W}$, $\overline{RD}$/E/$\overline{DS}$, ALE, $\overline{PSEN}$, Reset, and A19/$\overline{CSI}$. Each of these signals can be configured to meet the output control signal requirements of various microcontrollers.

$\overline{WR}/V_{PP}$ or R/$\overline{W}$

In operational mode, this signal can be configured as $\overline{WR}$ or R/$\overline{W}$. As $\overline{WR}$, all write operations to the PSD313 are activated by an active low signal on this pin. As R/$\overline{W}$, the pin works with the E strobe of the $\overline{RD}$/E/$\overline{DS}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

$\overline{RD}$/E/$\overline{DS}$

In operational mode, this signal can be configured as $\overline{RD}$, E, or $\overline{DS}$. As $\overline{RD}$, all read operations to the PSD313 are activated by an active low signal on this pin. As E, the pin works with the R/$\overline{W}$ signal of the $\overline{WR}/V_{PP}$ or R/$\overline{W}$ pin. When R/$\overline{W}$ is high, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a read operation. When R/$\overline{W}$ is low, an active high signal on the $\overline{RD}$/E/$\overline{DS}$ pin performs a write operation.

As $\overline{DS}$, the pin works with the R/$\overline{W}$ signal as an active low data strobe signal. As $\overline{DS}$, the R/$\overline{W}$ defines the mode of operation (Read or Write).

ALE or AS

ALE polarity is programmable. When programmed to be active high, a high on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The falling edge of ALE locks the information into the latches. When ALE is programmed to be active low, a low on the pin causes the input address latches, Port A address latches, Port C, and A19 address latches to be transparent. The rising edge of ALE locks the appropriate information into the latches.

$\overline{PSEN}$

The $\overline{PSEN}$ function enables the user to work with two address spaces: program memory and data memory (if COMB/SEP = 1). In this mode, an active low signal on the $\overline{PSEN}$ pin causes the EPROM to be read if selected. The SRAM and I/O ports read operation are done by $\overline{RD}$ low (CRRWR = 0), or by E high and R/$\overline{W}$ high (CRRWR = 1, CEDS = 0) or by $\overline{DS}$ low and R/$\overline{W}$ high (CRRWR, CEDS = 1).

Control Signals (Cont.)

PSEN

Whenever a member of the 8031 family (or any other similar microcontroller) is used, the PSD313's PSEN pin must be connected to the PSEN pin of the microcontroller.

If COMB/SEP = 0, the address spaces of the program and the data are combined. In this configuration (except for the 8031-type case mentioned above), the PSEN pin must be tied high to V_{CC}, and the EPROM, SRAM, and I/O ports are read by RD low (CRRWR = 0), or by E high and R/W high (CRRWR = 1, CEDS = 0) or by DS low and R/W high (CRRWR, CEDS = 1). See Figures 9 and 10.

Figure 8. Page Register

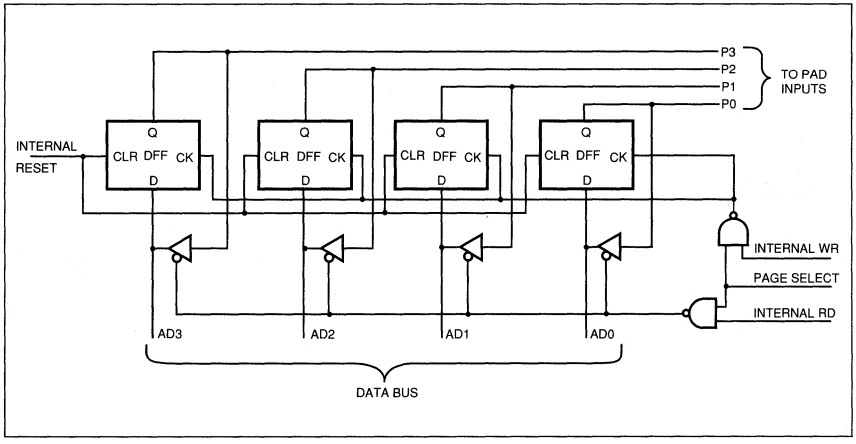


Table 8. Signal States During and After Reset

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7) (Port A	I/O Tracking AD0/A0–AD7 Address outputs A0–A7	Input Input Low
PB0–PB7 (Port B)	I/O CS7–CS0 CMOS outputs CS7–CS0 open drain outputs	Input High Tri-stated
PC0–PC2 (Port C)	Address inputs A16–A18 CS8–CS10 CMOS outputs	Input High

Figure 9. Combined Address Space

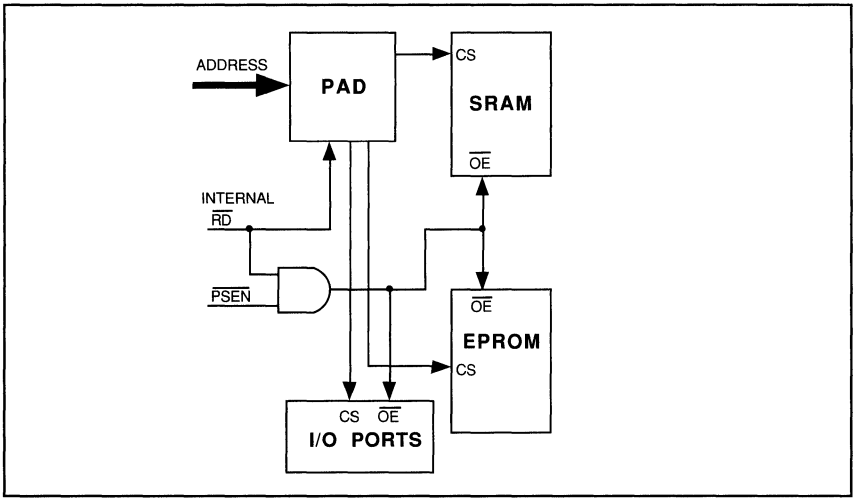
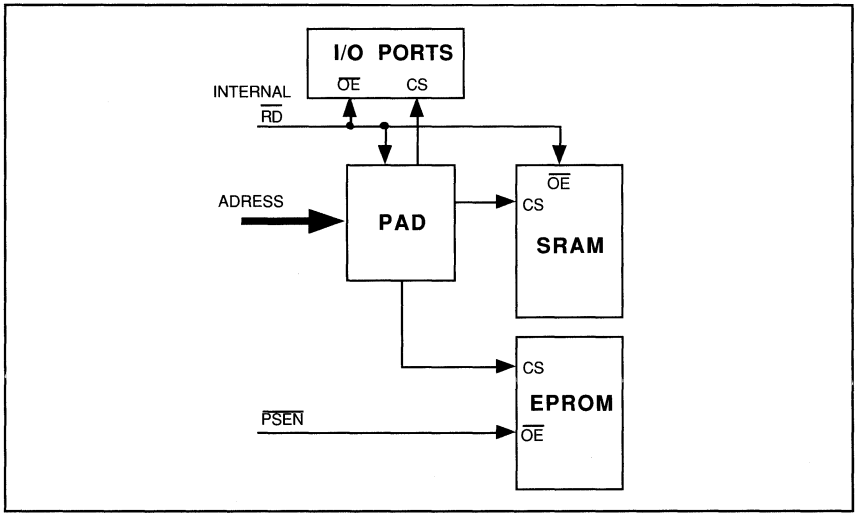


Table 9. Internal States During and After Reset

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All = 1 (Note 11)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All = 0 (Note 11)
Data register A	n/a	0
Direction register A	n/a	0
Data register B	n/a	0
Direction register B	n/a	0

NOTE: 11. All PAD outputs are in a non-active state.

Figure 10. 8031-Type Separate Code and Data Address Spaces



Control Signals (Cont.)

RESET

This is an asynchronous input pin that clears and initializes the PSD313. Reset polarity is programmable (active low or active high). Whenever the PSD313 reset input is driven active for at least 100 ns, the chip is reset. During boot-up (V_{CC} applied), the device is automatically reset internally (internal automatic reset is over by the time V_{CC} operating range has been achieved during boot-up). Tables 8 and 9 indicate the state of the part during and after reset.

A19/$\overline{CSI}$

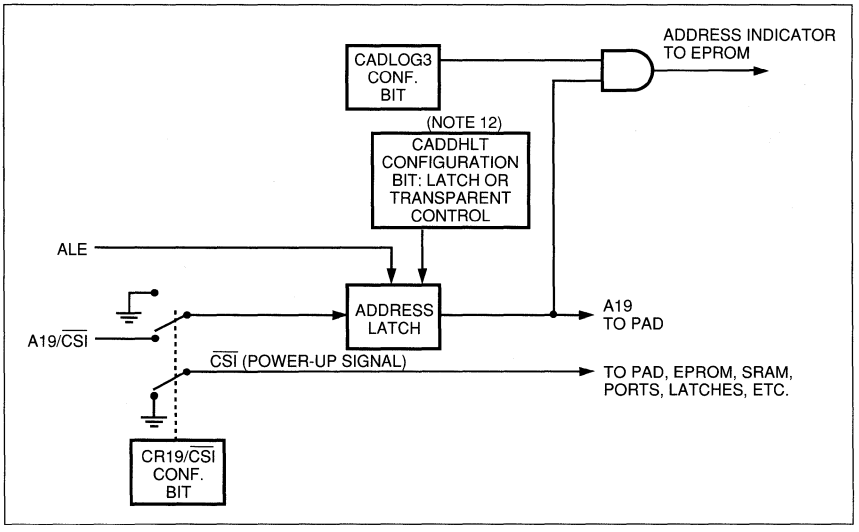
When configured as $\overline{CSI}$, a high on this pin deselects, and powers down, the chip. A low on this pin puts the chip in normal operational mode. For PSD313 states during the power-down mode, see Tables 10 and 11, and Figure 11.

In A19 mode, the pin is an additional input to the PAD. It can be used as an address line (CADLOG3 = 1) or as a general-purpose logic input (CADLOG3 = 0). A19 can be configured as ALE dependent or as transparent input (see Table 7). In this mode, the chip is always enabled.

Table 10. Signal States During Power-Down Mode

Signal	Configuration Mode	Condition
AD0/A0–AD7/A7	All	Input
A8–A15	All	Input
PA0–PA7	I/O Tracking AD0/A0–AD7/A7 Address outputs A0–A7	Unchanged Input All 1's
PB0–PB7	I/O $\overline{CS0}$–$\overline{CS7}$ CMOS outputs $\overline{CS0}$–$\overline{CS7}$ open drain outputs	Unchanged All 1's Tri-stated
PC0–PC2	Address inputs A18–A16 $\overline{CS8}$–$\overline{CS10}$ CMOS outputs	Input All 1's

Figure 11. A19/$\overline{CSI}$ Cell Structure



NOTE: 12. The CADDHLT configuration bit determines if A19–A16 are transparent via the latch, or if they must be latched by the trailing edge of the ALE strobe.

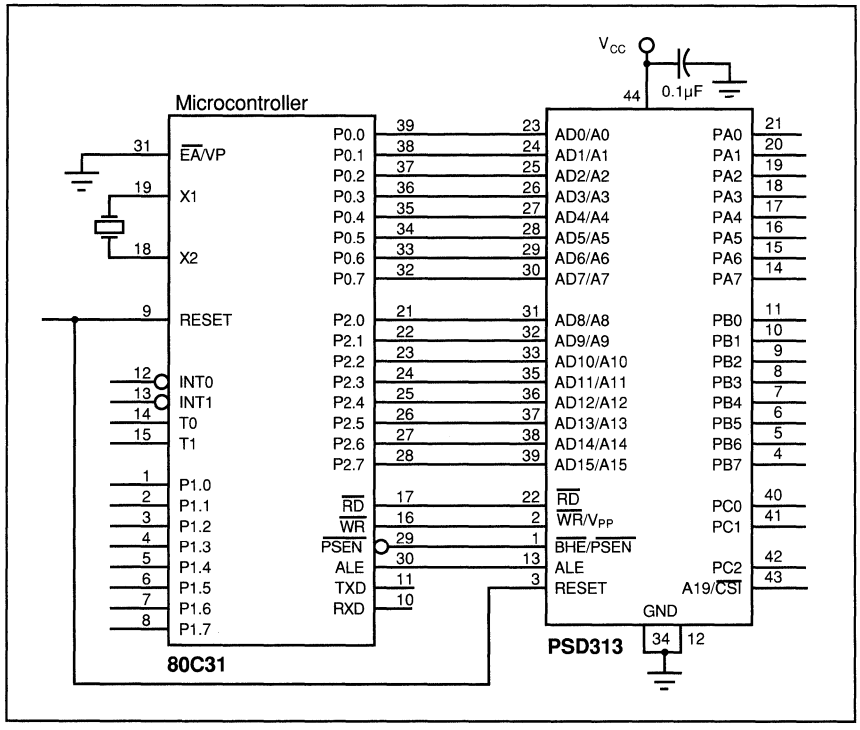
Table 11. Internal States During Power-Down

Component	Signals	Contents
PAD	$\overline{CS0}$–$\overline{CS10}$	All 1's (deselected)
	CSADIN, CSADOUT1, CSADOUT2, CSIOPORT, RS0, ES0–ES7	All 0's (deselected)
Data register A Direction register A Data register B Direction register B	n/a n/a n/a n/a	All unchanged

Security Mode

Security Mode in the PSD313 locks the contents of the PAD A , PAD B and all the configuration bits. The EPROM, SRAM, and I/O contents can be accessed only through the PAD. The Security Mode can be set by the MAPLE or Programming software. In window packages, the mode is erasable through UV full part erasure. In the security mode, the PSD313 contents cannot be copied on a programmer.

Figure 12. PSD313 Interface With Intel's 80C31



The configuration bits for Figure 12 are:

CRESET	1	COMB/SEP	0 or 1 (both valid)
CALE	0	CRRWR	0
CDATA	0	CEDS	0
CADDRDAT	1		

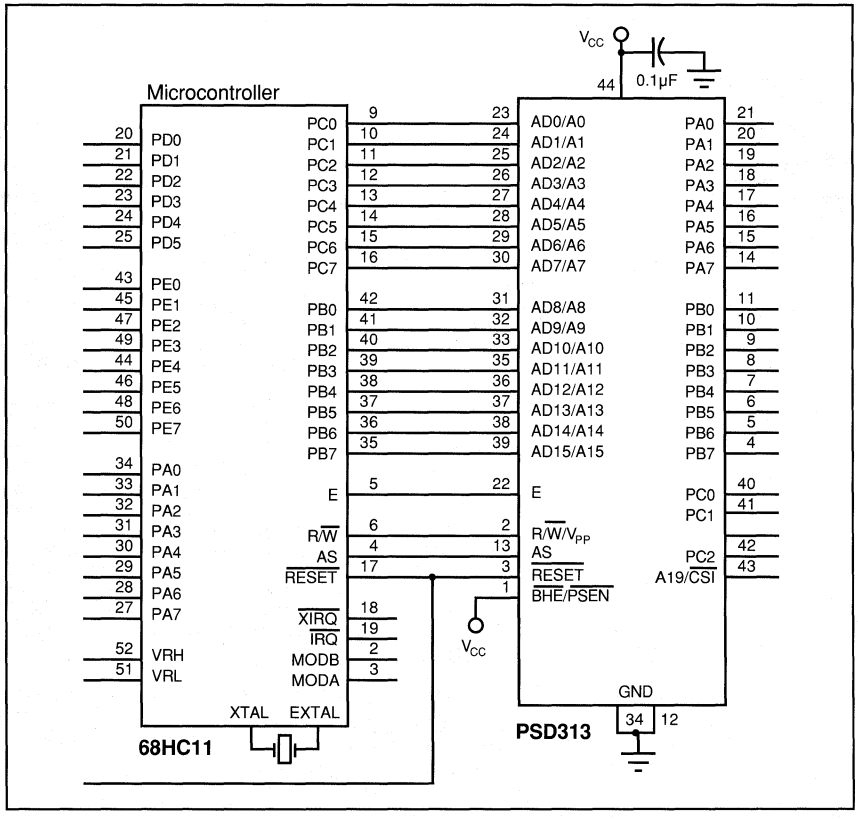
All other configuration bits may vary according to the application requirements.

System Applications

In Figure 12, the PSD313 is configured to interface with Intel's 80C31, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 80C31 uses signals $\overline{RD}$ to read from data memory and $\overline{PSEN}$ to read from code memory. It uses $\overline{WR}$ to write into the data memory. It also uses active high reset and ALE signals. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

In Figure 13, the PSD313 is configured to interface with Motorola's 68HC11, which is a 16-bit address/8-bit data bus microcontroller. Its data bus is multiplexed with the low-order address byte. The 68HC11 uses E and R/$\overline{W}$ signals to derive the read and write strobes. It uses the term AS (address strobe) for the address latch pulse. RESET is an active low signal. The rest of the configuration bits as well as the unconnected signals (not shown) are application specific and, thus, user dependent.

Figure 13. PSD313 Interface With Motorola's 68HC11



The configuration bits for Figure 13 are:

CRESET	0	COMB/SEP	0
CALE	0	CRRWR	1
CDATA	0	CEDS	0
CADDRDAT	1		

All other configuration bits may vary according to the application requirements.

Absolute Maximum Ratings[13]

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 150	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection			>2000	V

NOTE: 13. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at theses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance		
			-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 5%	± 10%	± 10%
Industrial	–40° C to +80°C	+ 5 V		± 10%	± 10%
Military	–55° C to +125°C	+ 5 V		± 10%	± 10%

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	-12 Version	4.75	5	5.25	V
V_{CC}	Supply Voltage	-15/-20 Versions	4.5	5	5.5	V
V_{IH}	High-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level Input Voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	V

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 µA V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA V_{CC} = 4.5 V		0.15	0.45	
V_{OH}	Output High Voltage	I_{OH} = –20 µA V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA V_{CC} = 4.5 V	2.4	3.9		
I_{SB1}	V_{CC} Standby Current (CMOS) (Notes 14 and 16)	Comm'l		50	100	µA
		Ind/Mil		75	150	
I_{SB2}	V_{CC} Standby Current (TTL) (Notes 15 and 16)	Comm'l		1.5	3	mA
		Ind/Mil		2	3.2	
I_{CC1}	Active Current (CMOS) (SRAM Not Selected) (Notes 14 and 17)	Comm'l (Note 18)		16	35	mA
		Comm'l (Note 19)		28	50	
		Ind/Mil (Note 18)		16	45	
		Ind/Mil (Note 19)		28	60	

DC Characteristics (Cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC2}	Active Current (CMOS) (SRAM Block Selected) (Notes 14 and 17)	Comm'l (Note 18)		47	80	mA
		Comm'l (Note 19)		59	95	
		Ind/Mil (Note 18)		47	100	
		Ind/Mil (Note 19)		59	115	
I_{CC3}	Active Current (TTL) (SRAM Not Selected) (Notes 15 and 17)	Comm'l (Note 18)		36	65	mA
		Comm'l (Note 19)		58	80	
		Ind/Mil (Note 18)		36	80	
		Ind/Mil (Note 19)		58	95	
I_{CC4}	Active Current (TTL) (SRAM Block Selected) (Notes 15 and 17)	Comm'l (Note 18)		67	105	mA
		Comm'l (Note19)		79	120	
		Ind/Mil (Note 18)		67	130	
		Ind/Mil (Note 19)		79	145	
I_{LI}	Input Leakage Current	V_{IN} = 5.5 V or GND	–1	± 0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or GND	–10	± 5	10	

NOTE: 14. CMOS inputs: GND ± 0.3 V or V_{CC} ± 0.3V.
15. TTL inputs: $V_{IL} \leq 0.8$ V, $V_{IH} \geq 2.0$ V.
16. $\overline{CSI}$/A19 is high and the part is in a power-down configuration mode.
17. AC power component is 3.0 mA/MHz (power = AC + DC).
18. Ten (10) PAD product terms active. (Add 380 µA per product term, typical, or 480 µA per product term maximum.)
19. Forty-one (41) PAD product terms active.

AC Characteristics (See Timing Diagrams)

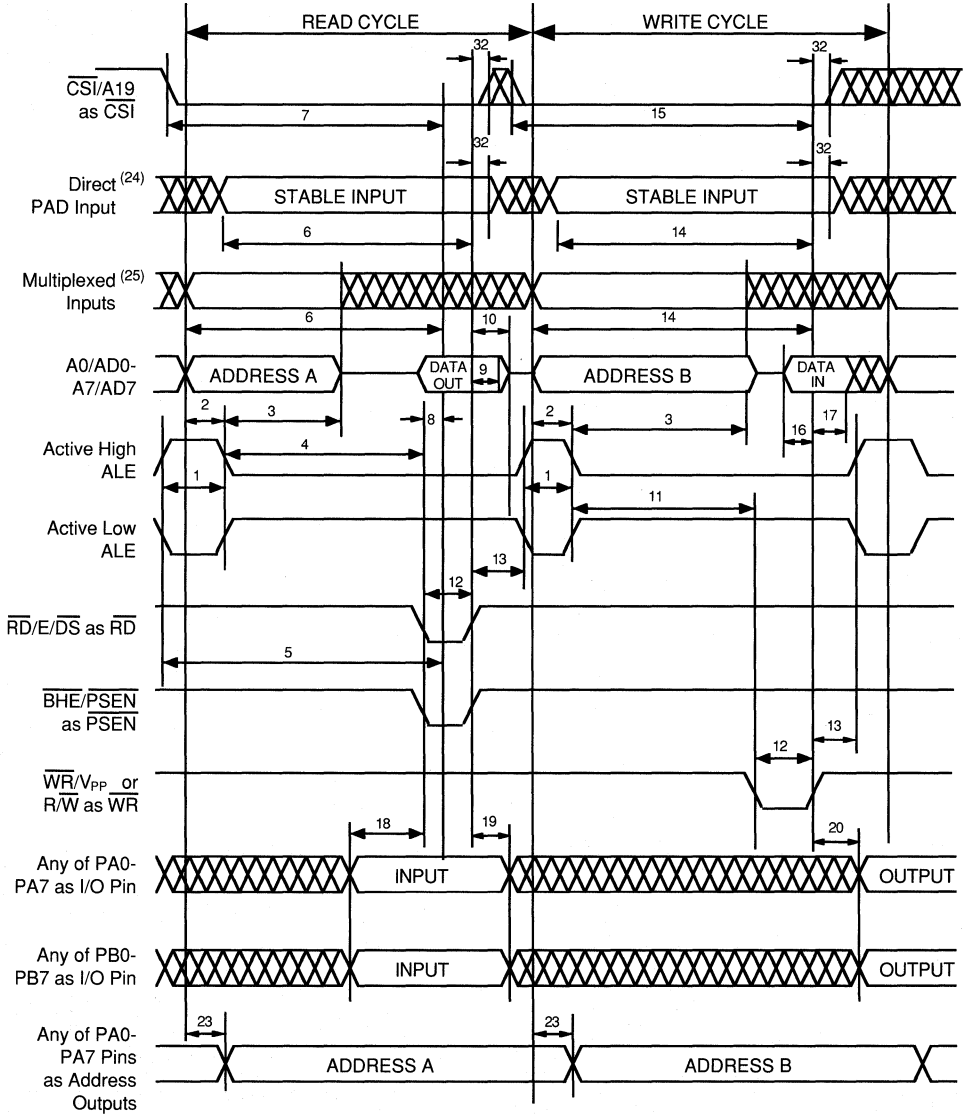
Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T1	ALE or AS Pulse Width	30		40		50		ns
T2	Address Set-up Time	9		12		15		
T3	Address Hold Time	13		15		25		
T4	ALE or AS Trailing Edge to Leading Edge of Read	12		15		20		
T5	ALE Valid to Data Valid	130		140		170		
T6	Address Valid to Data Valid		120		150		200	
T7	$\overline{CSI}$ Active to Data Valid		130		160		200	
T8	Leading Edge of Read to Data Valid		38		55		60	
T9	Read Data Hold Time	0		0		0		
T10	Trailing Edge of Read to Data High-Z		32		35		40	
T11	Trailing Edge of ALE or AS to Leading Edge of Write	12		15		20		
T12	$\overline{RD}$, E, $\overline{PSEN}$, $\overline{DS}$ Pulse Width	45		60		75		
T12A	$\overline{WR}$ Pulse Width	25		35		45		
T13	Trailing Edge of Write or Read to Leading Edge of ALE or AS	0		0		0		
T14	Address Valid to Trailing Edge of Write	120		150		200		

AC Characteristics (Cont.)

Symbol	Parameter	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
T15	$\overline{CSI}$ Active to Trailing Edge of Write	130		160		200		ns
T16	Write Data Set-up Time	20		30		40		
T17	Write Data Hold Time	5		10		15		
T18	Port Input Set-up Time	30		35		45		
T19	Port Input Hold Time	0		0		0		
T20	Trailing Edge of Write to Port Output Valid	40		50		60		
T21	ADi or Control to $\overline{CSOi}$ Valid	6	35	6	40	5	45	
T22	ADi or Control to $\overline{CSOi}$ Invalid	5	35	4	40	4	45	
T23	Track Mode Address Propagation Delay: CSADOUT1 Already True		22		28		28	
T23A	Track Mode Address Propagation Delay: CSADOUT1 Becomes True During ALE or AS		33		50		50	
T24	Track Mode Address Holding Time	15		27		27		
T25	Track Mode Read Propagation Delay		29		35		35	
T26	Track Mode Read Hold Time	11	29	10	29	10	35	
T27	Track Mode Write Cycle Data Propagation Delay		20		30		30	
T28	Track Mode Write Cycle Write to Data Propagation Delay	8	30	7	40	7	55	
T29	Hold Time of Port A Valid During Write $\overline{CSOi}$ Trailing Edge	2		4		4		
T30	$\overline{CSI}$ Active to $\overline{CSOi}$ Active	9	45	9	55	8	60	
T31	$\overline{CSI}$ Inactive to $\overline{CSOi}$ Inactive	9	45	9	55	8	60	
T32	Direct PAD Input as Hold Time	10		12		15		
T33	R/$\overline{W}$ Active to E or $\overline{DS}$ Start	20		30		40		
T34	E or $\overline{DS}$ End to R/$\overline{W}$	20		30		40		
T35	AS Inactive to E High	15		20		25		

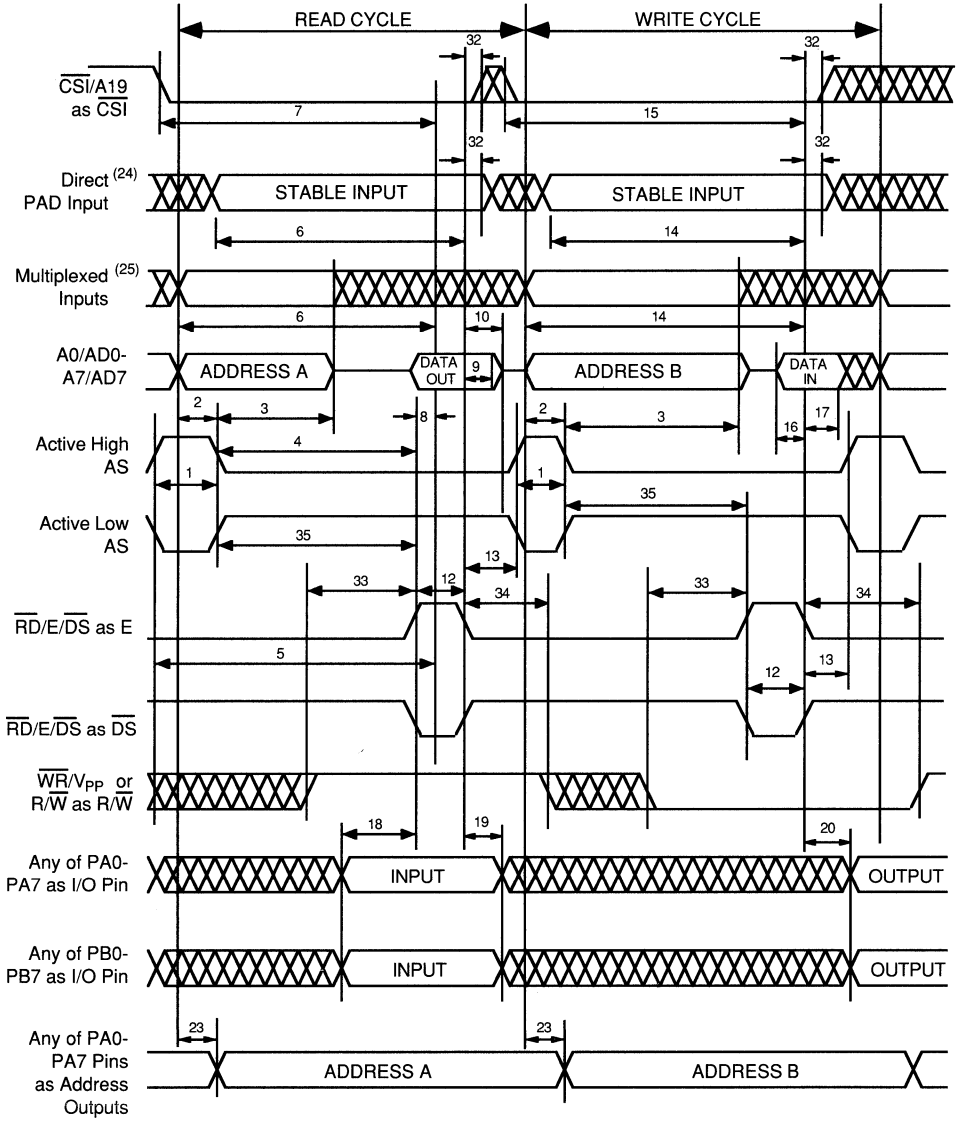
NOTES: 20. ADi = any address line.
21. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
22. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE (or AS).
23. Control signals $\overline{RD}$/E/$\overline{DS}$ or $\overline{WR}$ or R/$\overline{W}$.

Figure 14. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 0



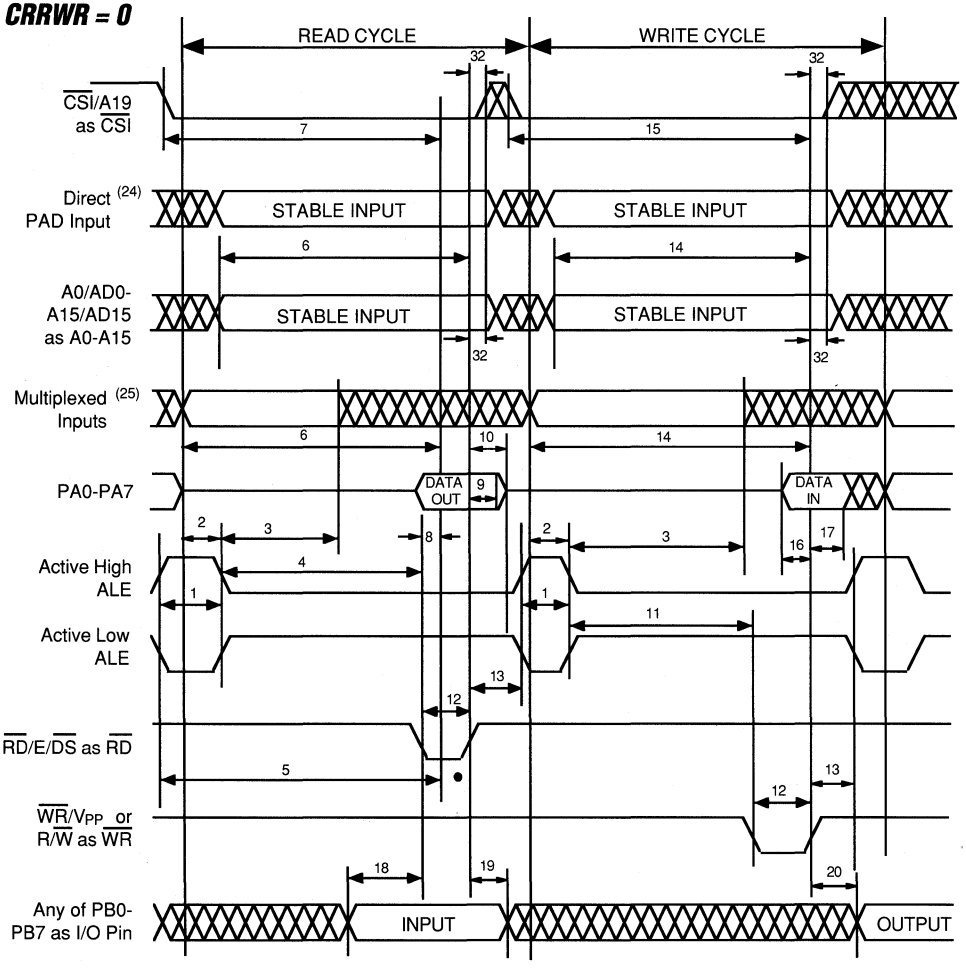
See referenced notes on page 2-239.

Figure 15. Timing of 8-Bit Multiplexed Address/Data Bus, CRRWR = 1



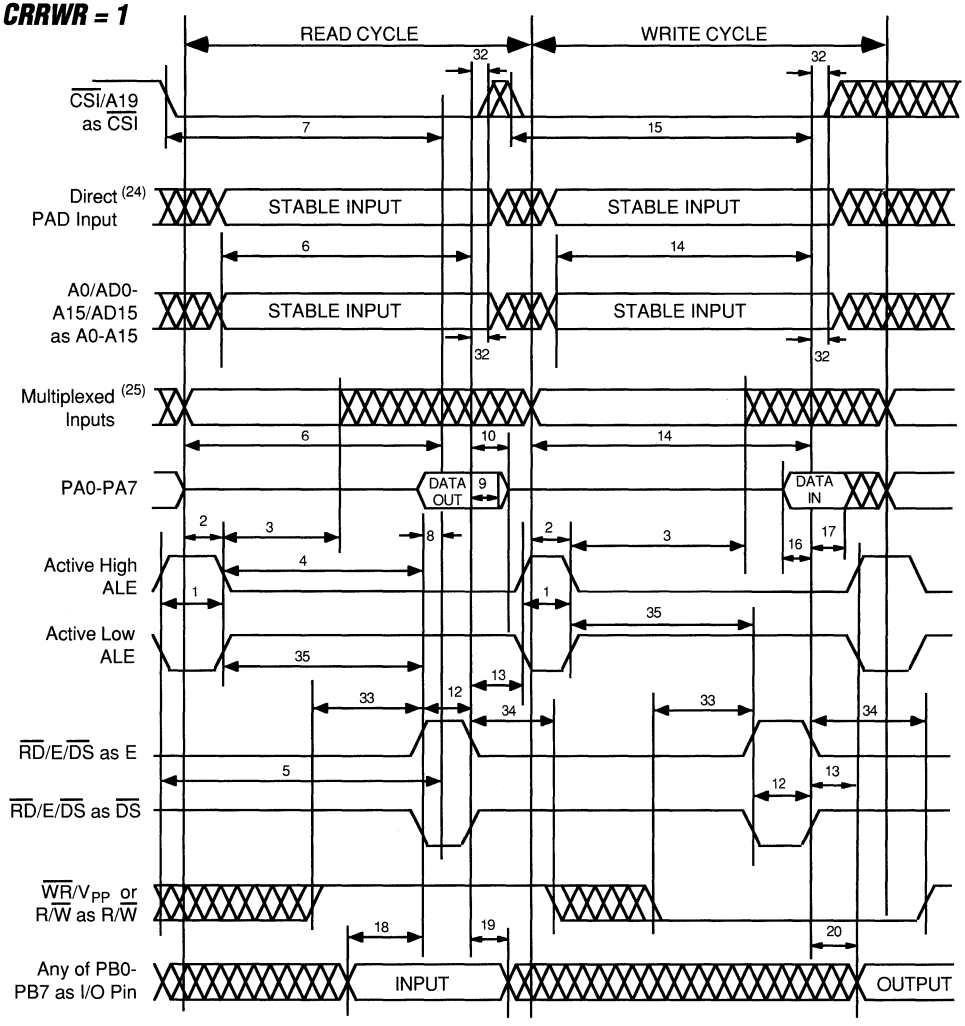
See referenced notes on page 2-239.

Figure 16. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 0



See referenced notes on page 2-239.

Figure 17. Timing of 8-Bit Data Non-Multiplexed Address/Data Bus, CRRWR = 1



See referenced notes on page 2-239.

Figure 18. Chip-Select Output Timing

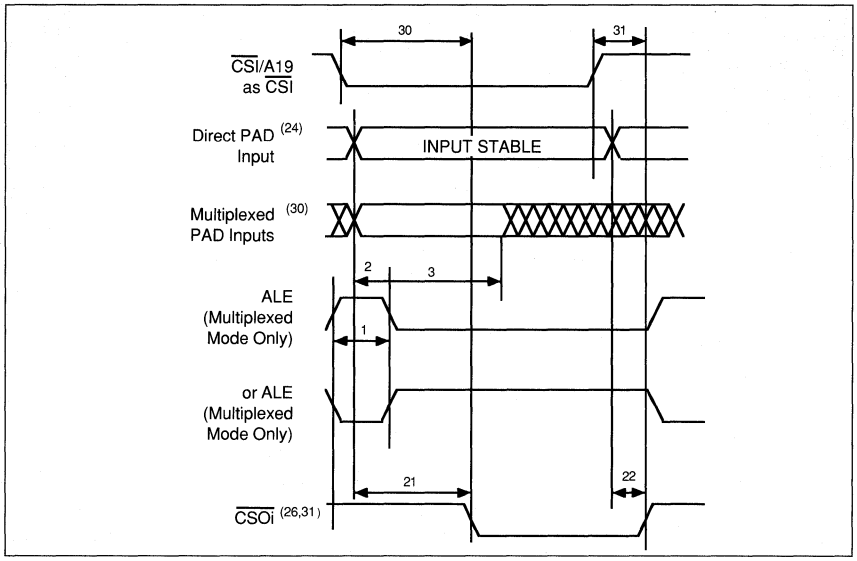
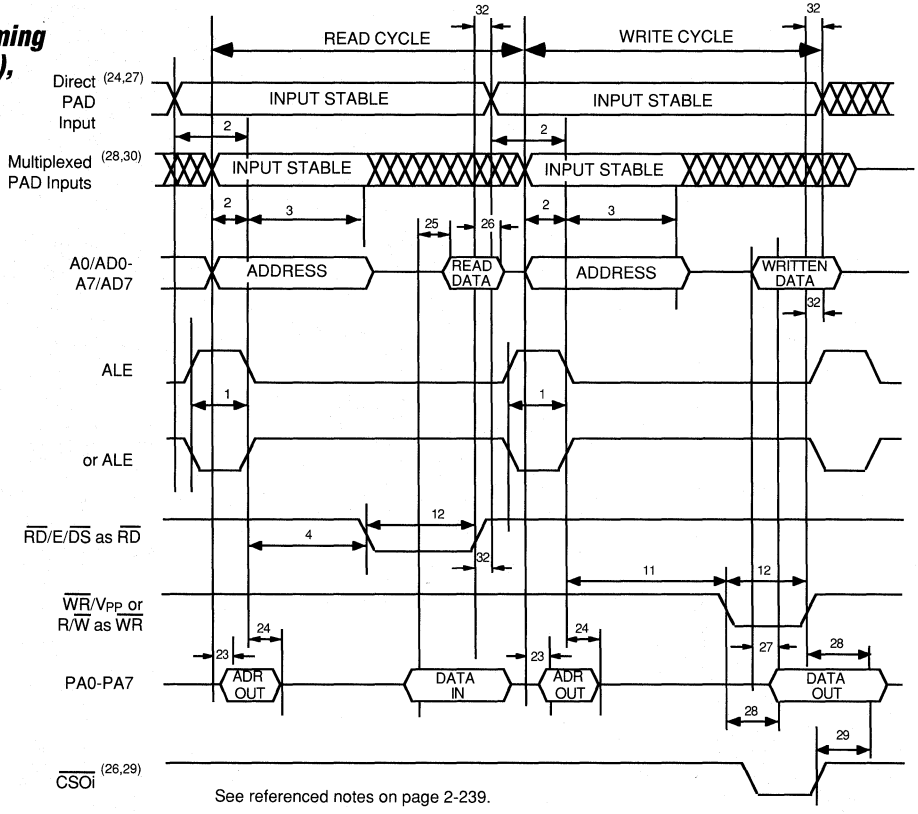
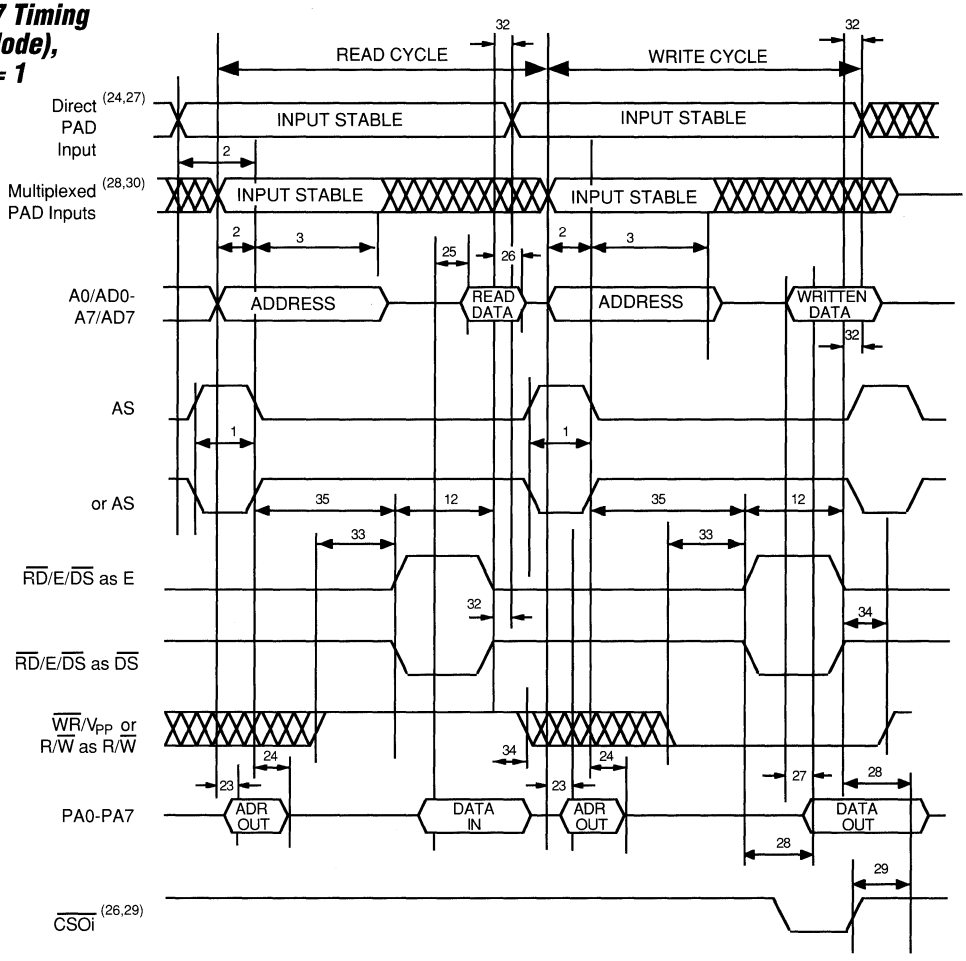


Figure 19. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 0



See referenced notes on page 2-239.

Figure 20. Port A as AD0–AD7 Timing (Track Mode), CRRWR = 1



Notes for Timing Diagrams

24. Direct PAD input = any of the following direct PAD input lines: $\overline{CSI}$/A19 as transparent A19, $\overline{RD}$/E/$\overline{DS}$, $\overline{WR}$ or R/$\overline{W}$, transparent PC0–PC2, ALE in non-multiplexed modes.
25. Multiplexed inputs: any of the following inputs that are latched by the ALE (or AS): A0/AD0–A7/AD7, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
26. $\overline{CSOi}$ = any of the chip-select output signals coming through Port B ($\overline{CS0}$–$\overline{CS7}$) or through Port C ($\overline{CS8}$–$\overline{CS10}$).
27. CSADOUT1, which internally enables the address transfer to Port A, should be derived only from direct PAD input signals, otherwise the address propagation delay is slowed down.
28. CSADIN and CSADOUT2, which internally enable the data-in or data-out transfers, respectively, can be derived from any combination of direct PAD inputs and multiplexed PAD inputs.
29. The write operation signals are included in the $\overline{CSOi}$ expression.
30. Multiplexed PAD inputs: any of the following PAD inputs that are latched by the ALE (or AS) in the multiplexed modes: A11–A15, $\overline{CSI}$/A19 as ALE dependent A19, ALE dependent PC0–PC2.
31. CSOi product terms can include any of the PAD input signals shown in Figure 3, except for reset and $\overline{CSI}$.

Table 12. Pin Capacitance[32]

$T_A = 25\,°C$, $f = 1$ MHz

Symbol	Parameter	Conditions	Typical[33]	Max	Units
C_{IN}	Capacitance (for input pins only)	$V_{IN} = 0$ V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	$V_{OUT} = 0$ V	8	12	pF
C_{VPP}	Capacitance (for $\overline{WR}/V_{PP}$ or $R/\overline{W}/V_{PP}$)	$V_{PP} = 0$ V	18	25	pF

NOTES: 32. This parameter is only sampled and is not 100% tested.
33. Typical values are for $T_A = 25°C$ and nominal supply voltages.

Figure 21. AC Testing Input/Output Waveform

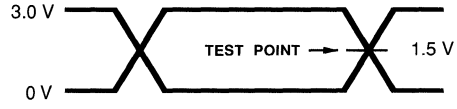
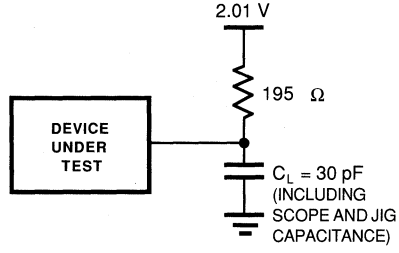


Figure 22. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the device to ultra-violet light source. A dosage of 15 W second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 15 to 20 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD313 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD313 device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Pin Assignments

Name	44-Pin PLDCC/ CLDCC Package	44-Pin CPGA Package
$\overline{PSEN}$	1	A_5
$\overline{WR}/V_{PP}$ or R/$\overline{W}$	2	A_4
RESET	3	B_4
PB7	4	A_3
PB6	5	B_3
PB5	6	A_2
PB4	7	B_2
PB3	8	B_1
PB2	9	C_2
PB1	10	C_1
PB0	11	D_2
GND	12	D_1
ALE or AS	13	E_1
PA7	14	E_2
PA6	15	F_1
PA5	16	F_2
PA4	17	G_1
PA3	18	G_2
PA2	19	H_2
PA1	20	G_3
PA0	21	H_3
$\overline{RD}$/E/$\overline{DS}$	22	G_4
AD0/A0	23	H_4
AD1/A1	24	H_5
AD2/A2	25	G_5
AD3/A3	26	H_6
AD4/A4	27	G_6
AD5/A5	28	H_7
AD6/A6	29	G_7
AD7/A7	30	G_8
A8	31	F_7
A9	32	F_8
A10	33	E_7
GND	34	E_8
A11	35	D_8
A12	36	D_7
A13	37	C_8
A14	38	C_7
A15	39	B_8
PC0	40	B_7
PC1	41	A_7
PC2	42	B_6
A19/$\overline{CSI}$	43	A_6
V_{CC}	44	B_5

Package Information

Figure 23. Drawing L4 — 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

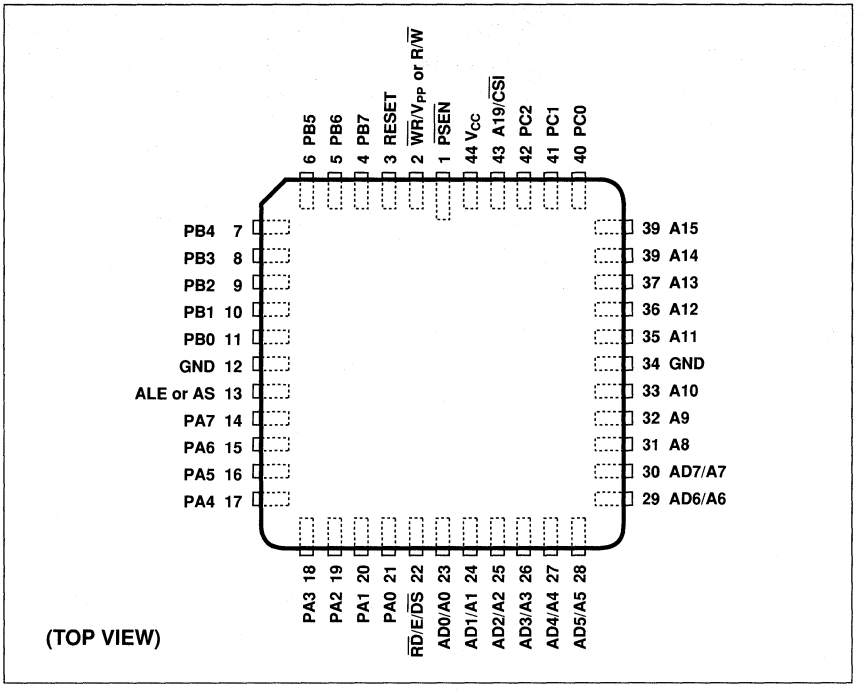


Figure 24. Drawing J2 — 44-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

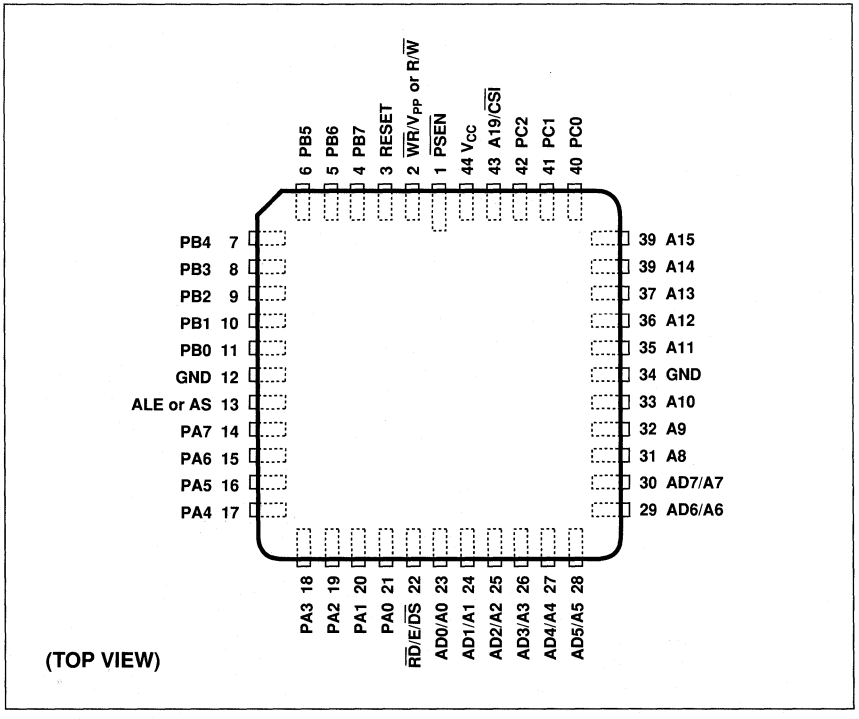
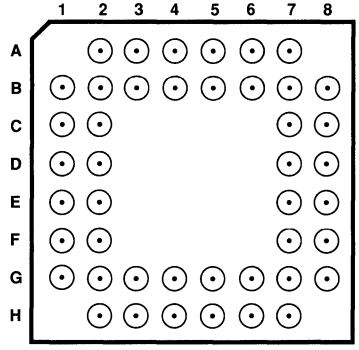


Figure 25. Drawing X2 — 44-Pin CPGA (Package Type X)



(TOP VIEW, THROUGH PACKAGE)

Ordering Information

Part Number	Spd. (ns)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
PSD313-12J	120	44-pin PLDCC	J2	Commercial	Standard
PSD313-12L	120	44-pin CLDCC	L4	Commercial	Standard
PSD313-12X	120	44-pin CPGA	X2	Commercial	Standard
PSD313-15J	150	44-pin PLDCC	J2	Commercial	Standard
PSD313-15JI	150	44-pin PLDCC	J2	Industrial	Standard
PSD313-15L	150	44-pin CLDCC	L4	Commercial	Standard
PSD313-15LI	150	44-pin CLDCC	L4	Industrial	Standard
PSD313-15X	150	44-pin CPGA	X2	Commercial	Standard
PSD313-15XI	150	44-pin CPGA	X2	Industrial	Standard
PSD313-15XM	150	44-pin CPGA	X2	Military	Standard
PSD313-15XMB	150	44-pin CPGA	X2	Military	MIL-STD-883C
PSD313-20J	200	44-pin PLDCC	J2	Commercial	Standard
PSD313-20JI	200	44-pin PLDCC	J2	Industrail	Standard
PSD313-20L	200	44-pin CLDCC	L4	Commercial	Standard
PSD313-20LI	200	44-pin CLDCC	L4	Industrial	Standard
PSD313-20X	200	44-pin CPGA	X2	Commercial	Standard
PSD313-20XI	200	44-pin CPGA	X2	Industrial	Standard
PSD313-20XM	200	44-pin CPGA	X2	Military	Standard
PSD313-20XMB	200	44-pin CPGA	X2	Military	MIL-STD-883C

PSD313
System Development Tools

System Development Tools

The PSD313 features a complete set of System Development Tools. These tools provide an integrated, easy-to-use software and hardware environment to support PSD313 device development. To run these tools requires an IBM-XT, -AT, or compatible computer, MS-DOS 3.1 or higher, 640K byte RAM, and a hard disk.

Hardware

The PSD313 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6020 52-pin PSD313 PQFP Package Adaptor
- ❑ WS6021 44-pin LCC Package Adaptor (for CLDCC and PLDCC packages)
- ❑ WS6022 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of an IBM-PC plug-in programmer board and a remote socket adaptor.

Software

The PSD313 System Development Software consists of:

- ❑ WISPER, WSI's Software Environment
- ❑ MAPLE, the PSD313 Location Editor Software
- ❑ MAPPRO, the Device Programming Software

The configuration of the PSD313 device is entered using MAPLE software. MAPPRO software uses the MagicPro programmer and the socket adaptor to configure the PSD313 device, which then can be used in the target system. The development cycle is depicted in Figure 26.

Support

WSI provides a complete set of quality support services to registered System Development Tools owners, including:

- ❑ 12-month software updates
- ❑ Design assistance from WSI field application engineers and application group experts
- ❑ 24-hour Electronic Bulletin Board for design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PSD313 device and System Development Tools. Workshop participants learn how to program high-performance, programmable peripherals. Workshops are held at the WSI facility in Fremont, California.

Ordering Information – System Development Tools

PSD-GOLD
- ❑ WISPER Software
- ❑ MAPLE Software
- ❑ User's Manual
- ❑ WSI Support
- ❑ WS6000 MagicPro™ Programmer
- ❑ One Package Adaptor and Two Product Samples

PSD-SILVER
- ❑ WISPER Software
- ❑ MAPLE software
- ❑ User's Manual
- ❑ WSI Support

WS6000
- ❑ MagicPro Programmer
- ❑ IBM-PC© Plug-in Adaptor Card
- ❑ Remote Socket Adaptor

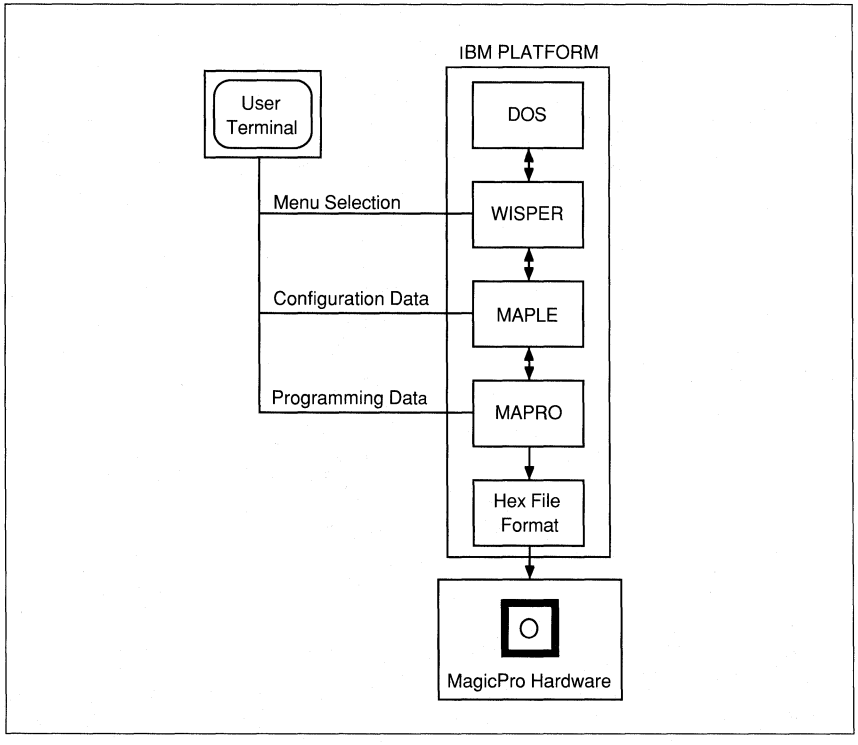
WS6021
- ❑ 44-Pin LCC Package Adaptor for CLDCC and PLDCC Packages. Used with the WS6000 MagicPro Programmer.

WS6022
- ❑ 44-Pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.

WSI Support
Support services include:
- ❑ 12-month Software Update Service
- ❑ Hotline to WSI Application Experts
- ❑ 24-hour access to WSI Electronic Bulletin Board

WSI Training
- ❑ Workshops at WSI, Fremont, CA
- ❑ For details and scheduling, call PSD Marketing (510) 656-5400.

Figure 26. PSD313 Development Cycle



Programmable Peripheral

Application Note 011

PSD3XX Device Description

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Programmable Peripheral
Application Note 011
PSD3XX Device Description

Chapter 1

Introduction

The PSD3XX family of products include flexible I/O ports, PLD, Page Register, 256K to 1M EPROM, 16K bit SRAM and "Glueless" Logic Interface to the micro controller. The PSD3XX is ideal for microcontroller based applications where fast time-to-market, small form factor and low power consumption are essential. These applications include disk controllers, cellular phones, modems, fax machines, medical instrumentation, industrial control, automotive engine control and many others.

Traditionally, central processing units (CPUs) require the support of non-volatile memory for program storage, random access memory (RAM) for data storage, and some input/output (I/O) capability to communicate with external devices. The addition of general logic circuitry is necessary to 'glue' the parts of the system together. Figure 1 shows a block diagram of such a system, configured with a CPU (or microprocessor). The typical microprocessor also has integrated into it on-board timers, a small amount of RAM and ROM, as well as a limited I/O capability.

The microprocessor (and often the microcontroller) requires additional external support EPROM and RAM memory, additional ports, memory mapping logic, and sometimes latches to separate address and data from a multiplexed address/data bus. Until very recently, designers had to create a discrete solution from a number of chips, or generate a full custom solution. Now, the PSD3XX integrates the different system support blocks into a single-chip solution. This relieves the designer from the constraint of thinking that memory mapping, ports, and address latch requirements should be developed from separate elements.

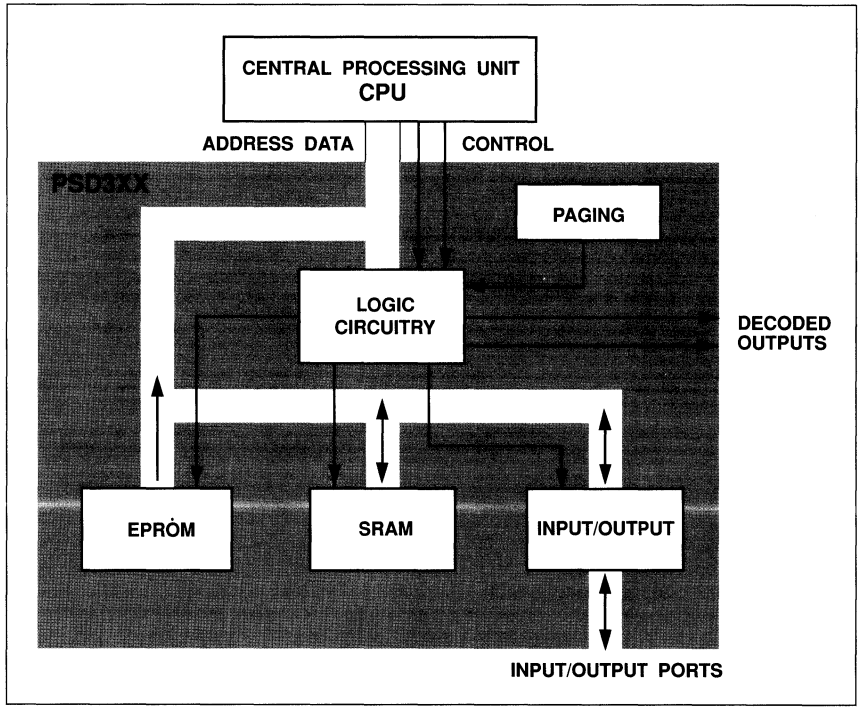


Figure 1. PSD3XX supports CPU as a Complete peripheral, memory, and logic subsystem

Introduction (Cont.)

This high integration of functionality into a single chip enables designers to reduce the overall chip count of the system. The result is increased system reliability, simpler PCB layout, and lower inventory and assembly costs. By integrating ports, latches, a Programmable Address Decoder (PAD), EPROM, and static RAM, the PSD3XX can bring the system solution down to only two chips: a microcontroller and a PSD3XX. The alternative solution would be discrete elements of RAM, EPROM, I/O mapped ports, and latches all mapped into the address scheme by a programmable logic device (PLD). This could escalate the chip count to 8–12 packages, depending on size and complexity.

For larger systems, multiple PSD3XX 's can be configured. Due to its versatility and flexibility, two or more PSDs can be cascaded either horizontally (increasing bus width) or vertically (increasing sub-system depth). This proportionally increases the complement of memory, I/O ports, and chip-selects without the need for additional external glue logic.

An additional feature of the PSD3XX is its ability to support a wide range of microcontrollers or microprocessors because it has been designed with a wide range of configurable options. The designer can program any one of a number of different options to create specific compatibility with a host processor. Furthermore, this can be done without the need for external glue logic.

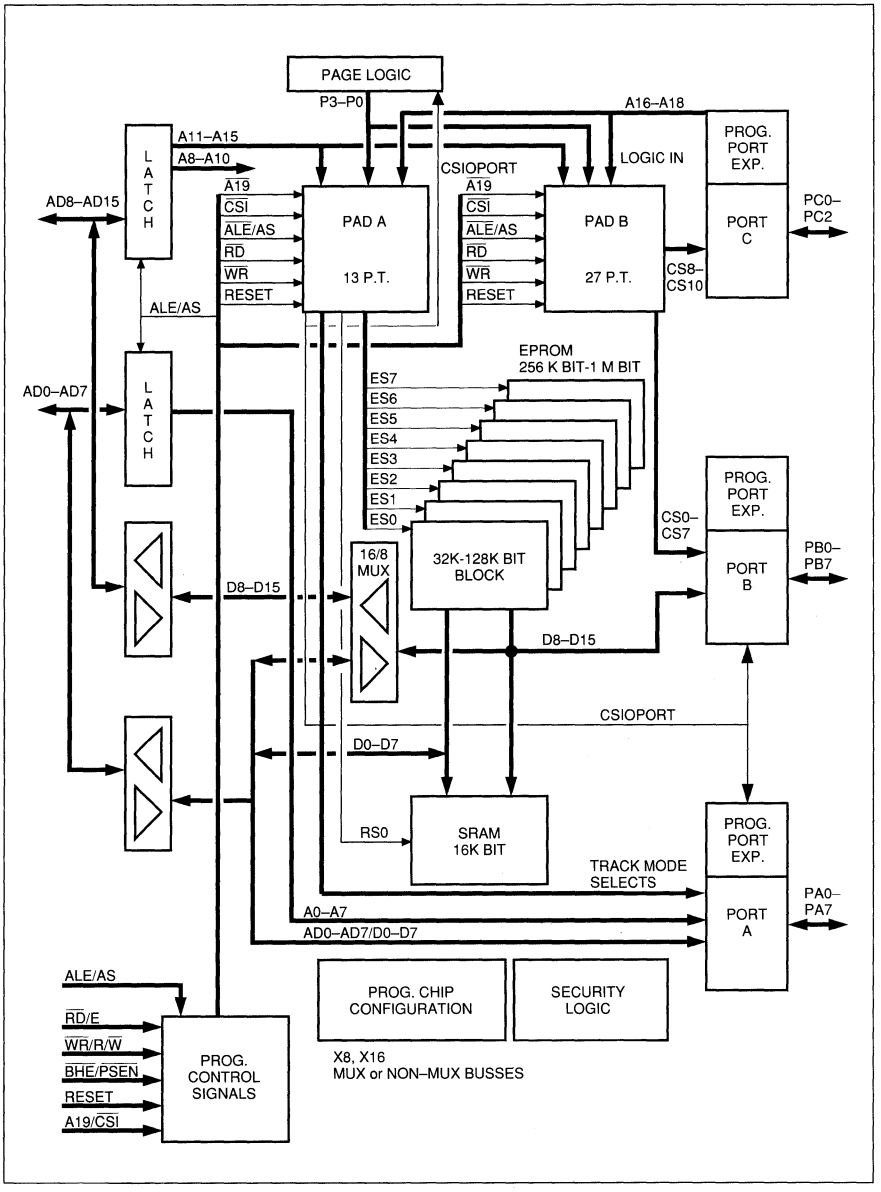
WSI Software Support for the PSD Family

The PSD family from WSI can be easily configured from a low-cost software support package called MAPLE. Designed to run in an IBM/PC environment, MAPLE makes design and configuration of the PSD3XX a simple task. Memory mapping of EPROM and RAM blocks replaces PLD-like equations with user-friendly, high-level command entries.

PSD3XX Architecture and Pin Nomenclature

The PSD3XX is available in a variety of 44-pin packages (see the PSD3XX Data Sheet). Figure 2 is a functional block diagram of the PSD3XX that shows the pin functions, internal architecture, and bus structure.

Figure 2. PSD3XX Architecture.



PSD3XX Architecture and Pin Nomenclature (Cont.)

Inputs AD0–AD15 enter the PSD through latches. These can be programmed to latch the address/data inputs, removing the need for such devices as the 74HCT373 or 573. Alternatively, in the transparent mode they simply buffer address inputs. The Address Latch Enable (ALE) signal is available to register a valid address input on the AD0–AD15 lines; its active polarity is programmable. Another name for this input is Address Strobe (AS). It provides the same function and the same timing as the ALE, but this pin name is more appropriate to Motorola-type systems. When either ALE or AS is valid, the latches are transparent; when inactive, the address/data inputs on AD0–AD15 remain latched.

The PSD3XX also contains a Programmable Address Decoder (PAD). Figure 2 shows that address inputs A11–A15 (and, possibly, inputs A16–A19) go directly to the PAD. Other inputs to the PAD include $\overline{RD}$(E), $\overline{WR}$ (R/$\overline{W}$), and ALE(AS). Programming of the PAD enables the designer to internally select the EPROM banks via internal chip-select lines ES0–ES7. An additional chip-select for the internal SRAM is available through RS0. Port C conveys either $\overline{CS8}$–$\overline{CS10}$ to external devices or receives A16–A18 inputs, directing them to the PAD. Also, A19 can be programmed to go directly into the PAD. Note that these lines are not necessarily dedicated to address inputs; they can be used as general purpose logic inputs. Thus, the PAD can be programmed to perform general combinational logic without adding any 'glue logic' to the overall system design. Address inputs A16–A19 can be used as general inputs to the PAD for implementing logic equations, and not for address decoding. If they are not used, A16–A19 are "don't care" conditions in memory map allocation. (See Figure 7 for a more detailed diagram of the PAD.)

The internal port options (Ports A and B) are both 8 bit-wide and can be programmed to act as traditional I/O ports. Port C is a 3-bit port designed to output logic functions from the PAD, receive address inputs A16–A18, or a combination of both. Ports A and B, however, are more complex because a number of different options can be selected with regard to system configuration. Figures 3, 4, 5, and 6 show the variety of configurations that are available to these ports.

Performance Characteristics

Two key timing parameters associated with the device are the EPROM/SRAM access times and the propagation delay through the PAD. The worst-case delay from valid address input to valid data output is 120 ns whether the address input is multiplexed or not. The cycle time of the system is virtually 120 ns with a small margin for address switching. This gives a system clock rate of about 8.3 MHz. Considering the power-down option, it takes 100 ns for active power input enabled through the $\overline{CSI}$ to valid data output. If the chip-select output option is chosen for either Port B or Port C, the propagation delay for address and control input through the PAD to valid chip-select output is 35 ns.

PSD3XX System Configuration for Port and I/O Options

In this section, the EPROM and SRAM are treated as separate entities and the four options available for configuring the PSD301 in a processor system are detailed. Figure 3 shows an 8-bit data configuration for systems that multiplex 8-bits of data (D0–D7) with the corresponding address inputs (A0–A7). Lines A8–A15 are dedicated to higher-order address inputs. Ports A and B are then available for data I/O and Port C is available for additional inputs, A16–A18 or chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Port A also has the option of passing any one or all of the internally latched lower-order addresses (A0–A7) to the output. Another mode supported by Port A is called "track mode." In this mode, the PSD301 can be programmed to pass the I/Os AD0–AD7 through the device enabling a shared memory or peripheral resource to be accessed. Port B has an additional mode to the general port mode. The PSD301's on-chip PAD can be programmed to generate chip-select signals which can be routed to Port B's output for external chip selection as $\overline{CS0}$–$\overline{CS7}$. Port C can be programmed for inputs A16–A18 or as additional chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Although labeled as address inputs, A16–A18 can be used for general Boolean inputs to the PAD array.

Figure 3. 8-bit multiplexed address/data mode

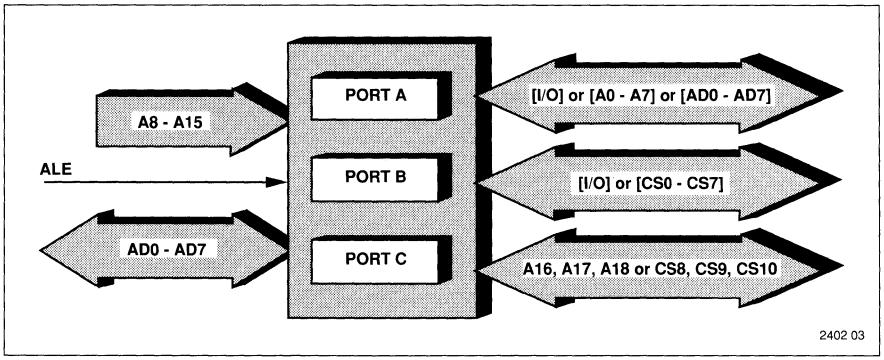
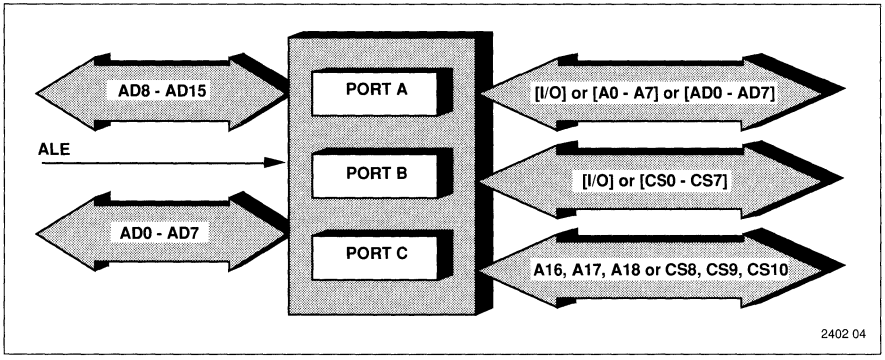


Figure 4 extends the option offered in Figure 3 to a 16-bit multiplexed bus. AD8–AD15 convey address and data I/O. The port options remain the same as for Figure 3; thus, these two configurations are suitable for multiplexed address/data systems of 8 or 16 bits.

Figure 4. 16-bit multiplexed address/data mode.



Figures 5 and 6 show options for a non-multiplexed host processor or controller. Figure 5 is suited to byte-wide systems and Figure 6 to 16-bit word-wide configurations. In Figure 5, Port A is used for data D0–D7 but Port B is still available for general I/O operations or chip-select outputs. This configuration is suitable for processors such as the M68008.

Figure 5. Non-multiplexed Mode 8-bit Data Bus

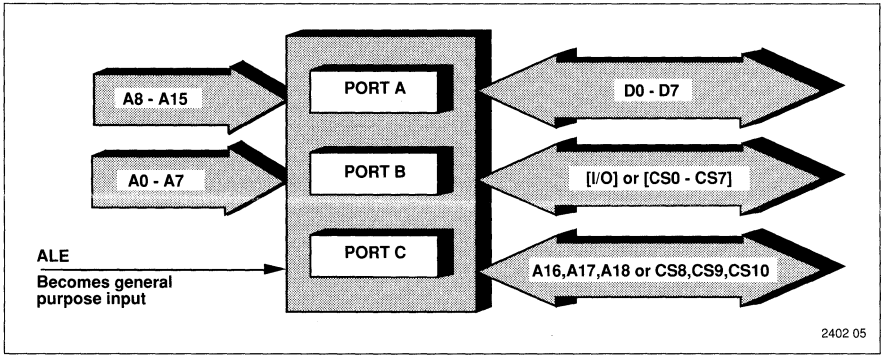
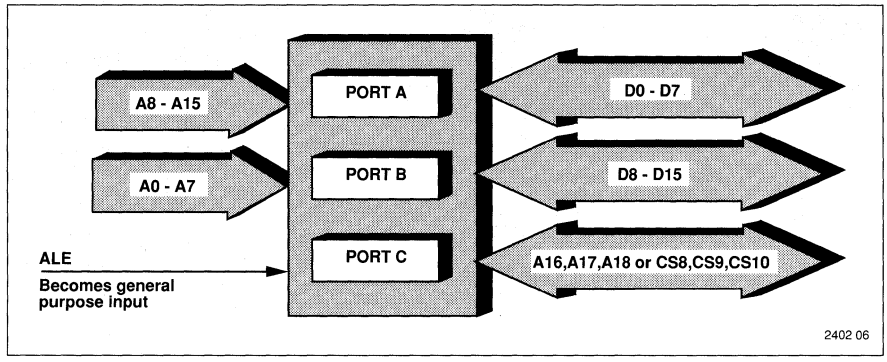


Figure 6. Non-multiplexed Mode 16-bit Data Bus



The function of Port C is the same in all of the four modes of operation. For 16-bit data transfers, an additional 8 bits of data is required. Figure 6 shows Port B as the data bus for the higher-order data byte D8–D15.

With D0–D7, this configuration is suitable for 16-bit microprocessors such as the M68000. Port C is available for address inputs or chip-select outputs.

Address Inputs

The processor interface has 16 address inputs: AD0–AD15. The device can be programmed to accept either address inputs or multiplexed address/data inputs. The address lines can be latched into the one or two octal latches for multiplexed byte or word-wide buses respectively. The device is initially programmed with a word configuration setting the PSD3XX to a specific mode; for example, one configuration bit selects whether the address input is multiplexed with data or is a non-multiplexed dedicated address. In the non-multiplexed scheme, the input latches are held as transparent. When the address inputs are valid on the chip as A0–A15, they can be subdivided into two buses: as lower-order addresses (A1–A11), and as higher-order addresses (A12–A15). A1–A11 go directly to the EPROM and inputs A1–A10 go to the SRAM (see Figure 2). The EPROM blocks are selected through the PAD via outputs ES0–ES7 as shown in Figure 2; and the SRAM is selected by the RS0 output.

The address input lines A11–A15, along with possible additional address inputs A16–A19, go into the PAD array. These address inputs are available for mapping the blocks of memory into the map scheme of the system. One option is to program the additional address inputs as valid higher-order address inputs for memory addressing ranges above 64K bytes or 32K words. If A16–A18 are not required, these PAD inputs can be ignored. Only microprocessors and microcontrollers with a large addressing range use these higher-order address lines. A second option is to disregard these address inputs to the chip in favor of additional chip-select outputs. A third option is available if the designer does not need additional chip-select outputs or high-order address inputs. The inputs A16–A18 can be used as general-purpose logic inputs. Examples of this are illustrated in some of the following applications.

An interface with the Z80B microprocessor uses inputs A16, A17, and A18 for signals $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$, respectively. In the M68008 application, two of these pins are programmed as $\overline{DTACK}$ and $\overline{BERR}$ from the PSD301 to the M68008. A wired-OR function can be implemented on the $\overline{DTACK}$ or $\overline{BERR}$ input if the user takes advantage of Port B's open-drain feature. If two PSD3XX devices are used together, the $\overline{DTACK}$ and $\overline{BERR}$ lines can be wired together and the external pull-up resistors can be used to tie these lines HIGH. It is also possible to use the internal PAD of one PSD3XX to gate these lines together and produce composite $\overline{DTACK}$ and $\overline{BERR}$ inputs to the M68008.

Internally, the memory blocks are arranged word-wide with a byte-wide isolation buffer separating the lower and upper bytes. This buffer is controlled from the configuration section of the PSD3XX. When the PSD3XX is configured to operate in word-wide mode, this buffer isolates the two buses into D0–D7 and D8–D15. In word-wide mode, the control of the data flow through this buffer is determined by BHE, A0, and the device's current configuration mode. Accessing byte-wide data can be thought of as accessing bytes on even and odd word boundaries or as two separate

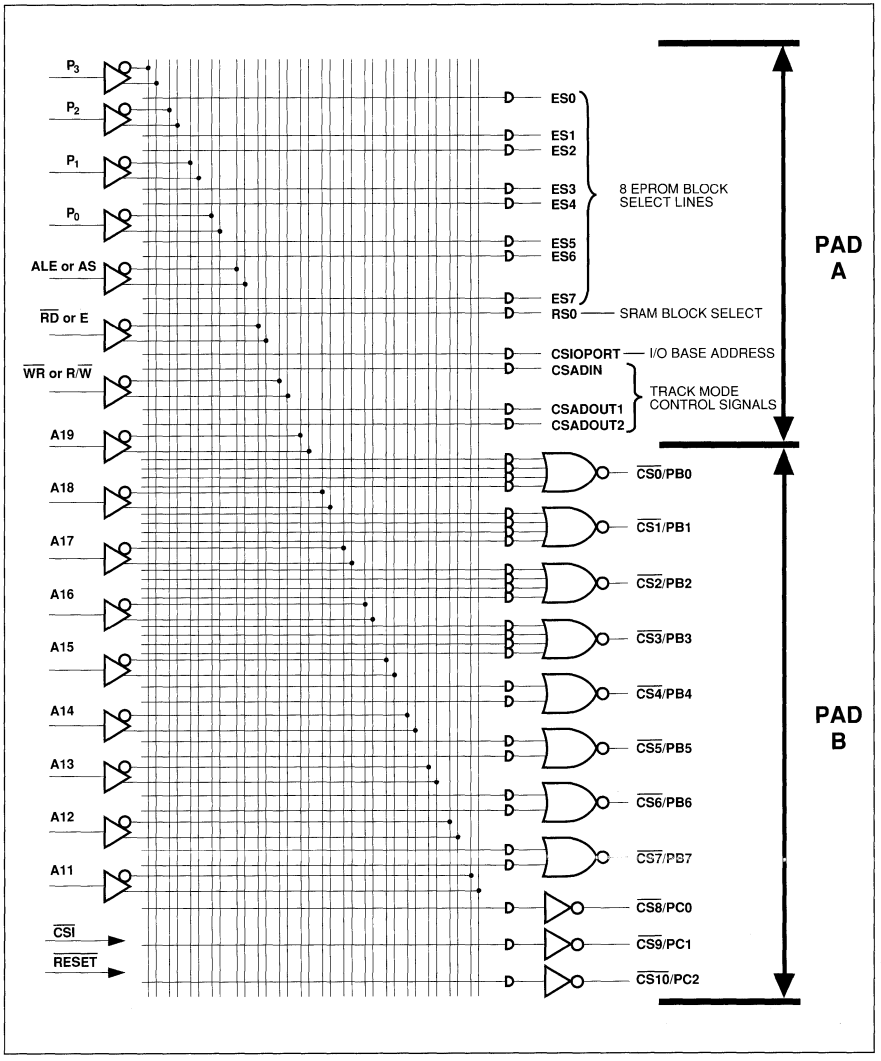
Address Inputs (Cont.)

banks of byte-wide data. The total complement of EPROM is shown as eight banks. The chip-select outputs ES0-ES7 come from the PAD. These are programmable address and control decode signals from the PAD inputs. Figure 7 provides a detailed schematic diagram of the PAD in terms of a traditional PLD.

PSD3XX Programmable Array Decoder (PAD)

The PAD is an EPROM-based reprogrammable logic fuse array with sum-of-product outputs. For Intel-type configurations, inputs to the PAD are A11–A19, ALE, $\overline{RD}$, and $\overline{WR}$. For Motorola type configurations, they are R/$\overline{W}$, AS, and E. The $\overline{CSI}$ and RESET inputs are used to deselect the PAD for power-down configurations and initialization, respectively. Internal to the PSD301 are the ES0–ES7 EPROM select lines. There is one product term dedicated to each EPROM block, and a single product term (RSO) for the SRAM selection. Address and control for each EPROM bank can programmed to a resolution of a 4K word boundary and positioned anywhere in the mapping scheme of the designer's system. Similarly, the SRAM can be positioned on 2K word boundaries.

Figure 7. PSD3XX Programmable Array Decoder



PSD3XX Programmable Array Decoder (PAD) (Cont.)

Other internal product term outputs from the PAD are the CSIOPORT, CSADIN, CSADOUT1, and CSADOUT2 lines. A single product term generates the CSIOPORT signal; this provides a base address for Ports A and B. The registers relevant to these ports are addressed as a base offset (see Table 1). The CSADIN signal is used to control the input buffer in the track mode. It can be enabled to read data in a programmed address space from Port A through the PSD3XX. CSADOUT1–2 are used to control the multiplexed address and write data through the PSD3XX to the Port A pads. The address range is programmed into the PAD qualifying the address space, but CSADOUT1 is qualified by the ALE signal outside of the PAD. This automatically lets the design distinguish between address and write data. To qualify valid write data, the PSD3XX automatically includes the CSADOUT2 product term with the $\overline{WR}$ or R/$\overline{W}$ signal.

Table 1. Port Base Address Offset

Register Name	Offset From The CSIOPORT Base Address
Pin Register of Port A	+2 (Accessible only during Read)
Pin Register of Port B	+3 (Accessible only during Read)
Direction Register Port A	+4
Direction Register Port B	+5
Data Register Port A	+6
Data Register Port B	+7 (Byte Wide)
Pin Register of Ports A and B	+2 (Accessible only during Read)
Direction Register of Ports A and B	+4
Data Register of Ports A and B	+6 (Word Wide)

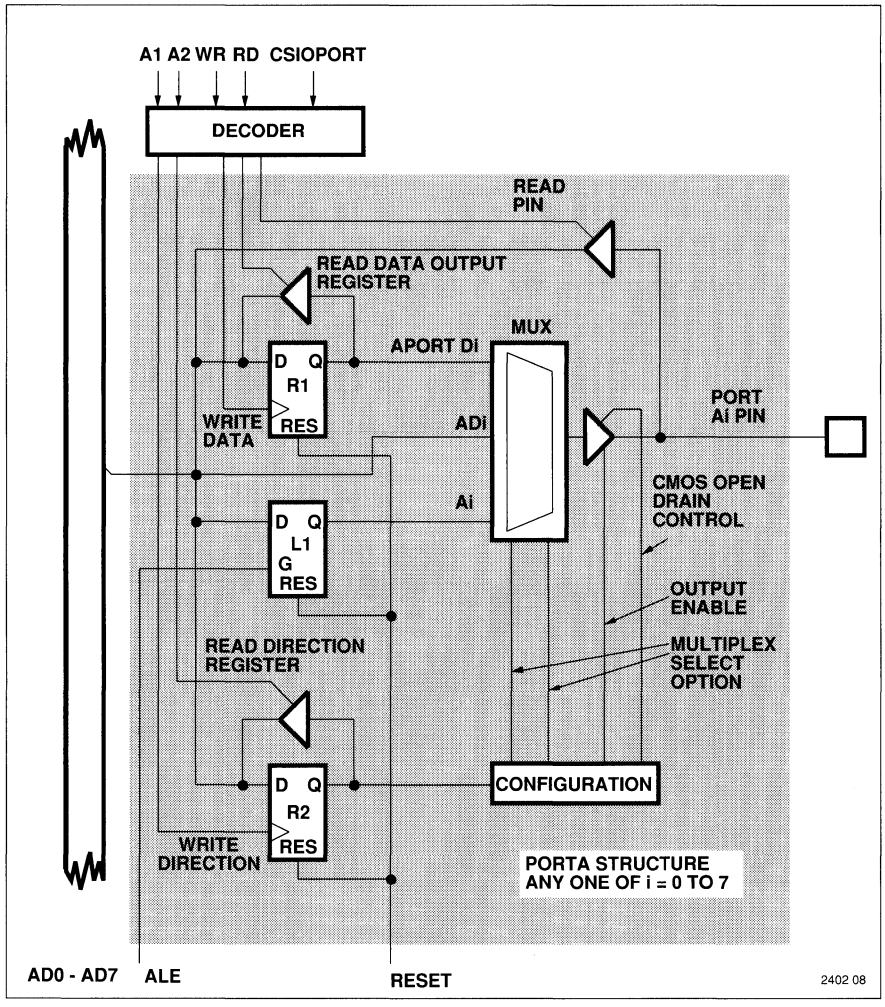
The PAD structure enables additional chip-selects to be routed to the Port B output pins. The four chip-select outputs ($\overline{CS0}$–$\overline{CS3}$) are supported by four product terms per output. $\overline{CS4}$–$\overline{CS7}$ have two product terms per output. The ability to use more than one product term from a chip-select enables the mapping of additional devices to be distributed through the address space, rather than selecting memory as a block. Sacrificing Port B terminals for chip-selects could occur in systems requiring a larger EPROM, RAM, or I/O space. Additional PSD3XX devices can be designed into a system by using the chip-select outputs from Port C or B of one master PSD3XX. This is required for addressing a space greater than 1M. Finally, the outputs of the sum-of-product terms are inverted to be consistent with active LOW chip-select inputs for additional external RAM, EPROM, peripherals, or busses. Port C has the capability of providing three additional external chip-selects, each supporting one product term per output.

Microcontroller/ Microprocessor Control Inputs

The control inputs are also programmable: $\overline{WR}$ or R/$\overline{W}$ and $\overline{RD}$ or E are used for read/write control of the internal EPROM, RAM, and I/O capability. Other control inputs are a programmable option for Bus High Enable or Program Store Enable ($\overline{BHE}$/$\overline{PSEN}$) and Address Latch Enable or Address Strobe (ALE/AS). These pins are selected to suit the bus protocol of the host processor or, where not applicable, they can be ignored. The $\overline{CSI}$/A19 input is available either for a power-down chip-select enable or as a higher-order address input without the power-down feature. The final control input is the RESET input; this also is a programmable option. Its active polarity can be chosen to be compatible with the host system. The function of the RESET input is to clear and initialize the PSD301 at start-up. All I/Os are set up as inputs and all outputs are either in a non-active or three-state condition.

Consequently, the PSD3XX is prevented from actively driving outputs during start-up. This feature was incorporated to prevent potential bus conflicts. In Figure 2, the $\overline{CSI}$ and RESET inputs are shown also as PAD inputs. $\overline{CSI}$ is a hardwire option into the PAD that powers down the internal circuitry and is used in power-sensitive applications. Neither signal is available as a programmable option.

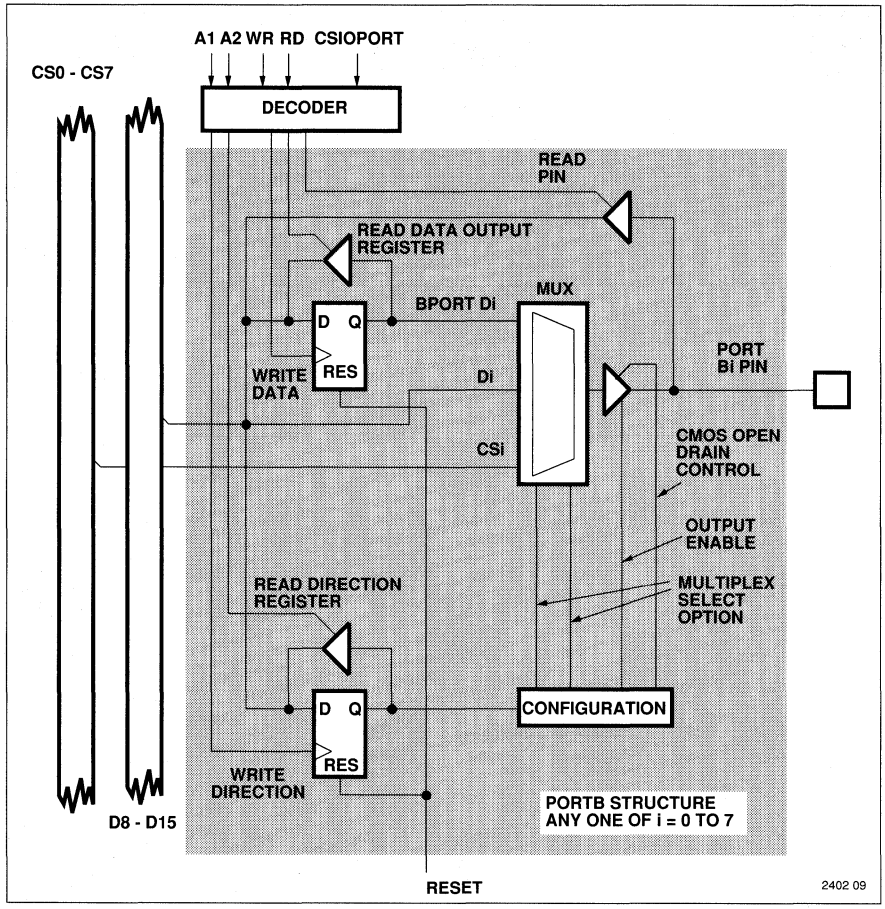
Figure 8. PSD3XX Port A Structure



Input and Output Ports

The port section comprises Port A (8 bits), Port B (8 bits), and Port C (3 bits). These support the many different I/O operations. For port expansion, Ports A and B can be configured as general I/O ports, each to convey eight bits of digital data to and from an external device. Figure 8 shows a single cell of Port A; Figure 9 shows a single cell of Port B.

Figure 9. PSD3XX Port B Structure



Writing data to a port is similar to writing data to a RAM location. If a port is programmed as an output, data is loaded into the output register as if it were a RAM location. Although the ports are not bit addressable, individual bits can be selected as either input or output. Thus, PA0–5 can be set as data outputs while PA6 and PA7 can be configured as inputs. Any mix of I/Os is possible giving the ports additional flexibility.

The direction of data flow through the port is determined by the data direction register. This register is dynamically programmable so that the I/O direction through Ports A and B can be altered during the microcontroller program execution. The data direction register initializes with logic zeros after an active RESET and causes each port bit to be set as an input. This state of initialization guarantees that the ports are prevented from driving the output lines at start-up. If the user requires all the Port A or Port B bits to be

Input and Output Ports (Cont.)

inputs, the data direction register can be left in this default state. To enable it as an output, logic ones can be written into the data direction location.

Due to the internal design, it is possible to program Port A or Port B bit lines as inputs and still write data to the port locations. This is because both ports have on-chip latches and can hold data. These registers are hidden or buried; i.e., they exist in the port and their condition can be read back at any time. However, these outputs do not drive the output pins because the port has been enabled as an input.

To access the port as a memory mapped location, the initial selection is made through the PAD's CSIOPORT. This provides a base address from which the locations shown in Table 1 give access to the various ports or their options. The configuration support software automatically ensures that there is no conflict between an SRAM location and I/O port in the case of memory mapped peripherals. It is also possible for the PSD3XX to distinguish between I/O and memory mapped locations. The user can input memory and I/O control signals to the PAD through the A16–A18 inputs and program an active CSIOPORT output by decoding these signals. This can be achieved with Intel- and Zilog-type processors which have separate memory and I/O controls. Signal input through pins A16–A18 is made possible through Port C. This 3-bit port is responsible for either PAD chip-select outputs or address/logic inputs. CSIOPORT points to a base address at which Ports A and B reside. Table 1 provides the offset from the base address and the associated port function. Figure 2 shows that Port A is driven by a multiplexed address/data bus of AD0–AD7 and the selection of address/data is made from the configuration memory and internal control functions.

The other options available to the user are selecting 1) the shared resource or track mode where AD0–AD7 is routed directly through to the Port A output, or 2) the latched address A0–A7. In track mode, AD0–AD7 inputs to the PSD3XX are used to access local or private memory and peripherals and the outputs AD0–AD7 through Port A are used to access a public resource.

PSD3XX General System Configuration

The PSD3XX family devices consists of two byte-wide configurable I/O ports (Ports A and B), 256K to 1M bits of EPROM, 16K bits of RAM, and the PAD. Additional I/O capability to and from the PAD is through a 3-bit I/O (Port C). There are also on-chip latches to support processors and controllers that multiplex address and data on the same bus. The EPROM memory section of the device is programmable just like a standard EPROM device. However, unlike the single-chip EPROM, the PSD3XX must also be configured to function into one of its many possible modes of operation. This is done by programming a non-volatile EPROM memory location with 45 configuration bits. These bits select the mode of operation and are programmed into the EPROM along with the hexadecimal microprocessor/microcontroller assembly language object code. When using MAPLE software, the assignment of logic conditions to the configuration bits locations is transparent to the user; the resultant word is merged with the EPROM code and the data map for the PAD.

Table 2 shows the the configuration locations and their functional assignment. For example, one of the configuration bits enables the device architecture to be compatible for either byte- or word-wide data buses. This is the configuration data or CDATA bit. The 256 Kbits of EPROM can be configured as a 32K byte-wide bus for applications with an 8031 microcontroller or as a 16K word-wide bus for applications with an M68000 microprocessor. These configuration bits are discussed in detail as each feature is covered in this application note.

Table 2. Non-volatile Configuration Bits

Configuration Bits	Number of Bits	Function
CDATA	1	CDATA . 0 = eight bits, 1 = sixteen bits
CADDRAT	1	ADDRESS/DATA Multiplexed. 0 = Non-multiplexed, 1 = Multiplexed
CRRWR	1	CRRWR. 0 = $\overline{RD}$ and $\overline{WR}$, 1 = R/$\overline{W}$ and E
CA19/$\overline{CSI}$	1	A19 or $\overline{CSI}$. 0 = Enable power-down, 1 = Enable A19
CALE	1	ALE Polarity. 0 = Active HIGH,1 = Active LOW
CRESET	1	CRESET. 0 = Active LOW RESET, 1 = Active HIGH RESET
$\overline{COMB}$/SEP	1	Combined or Separate Address Space for SRAM and EPROM. 0 = Combined, 1 = Separate
CPAF2	1	Port A Track Mode or Port Mode. 0 = Port or Address, 1 = AD0–AD7 Track Mode
CPAF1	8	Port A I/O or A0–A7. 0 = Port A pin is I/O, 1 = Port A pin is Address
CPBF	8	Port B I/O or CS. 0 = Port B pins are CSi (i = 0–7), 1 = Port B pins are I/O
CPCF	3	Port C A16–A18 or $\overline{CS8}$–$\overline{CS10}$. 0 = Port C pins are Address, 1 = Port C pins are Chip-select
CPACOD	8	Port A CMOS or Open Drain. 0 = CMOS drivers, 1 = Open Drain
CPBCOD	8	Port B CMOS or Open Drain. 0 = CMOS Drivers, 1 = Open Drain
CADDHLT	1	A16–A18 Transparent or Latched. 1 = Address latched, 0 = Address transparent
CSECURITY	1	CSECURITY On/Off. 0 = Off, 1 = On

In addition to bus width, the polarity and mode of the bus control signals are programmable. There are two types of read/write control: one is consistent with either a Motorola and Texas Instruments control bus standard; the other is consistent with the Intel/National Semiconductor/Zilog control bus standard. The configure read and write bit (CRRWR), distinguishes between one of two conventions: either an Intel (8031) or Motorola (M68HC11) convention can be selected by programming this single bit in the configuration memory. The Intel device requires the PSD3XX to be programmed with an active LOW $\overline{RD}$ and $\overline{WR}$ controls (CRRWR = 0). For applications with the Motorola microprocessor, select the R/$\overline{W}$ and E option (CRRWR = 1). In addition to a choice of two READ/WRITE controls, the user can select either a multiplexed Address/Data Bus or separate address and data lines.

Figure 3 shows the configuration that is best suited for the 8031 microcontroller; Figure 4 shows the configuration for an 80196 microcontroller with a 16-bit multiplexed addressed/data bus. For the non-multiplexed modes: Figure 5 applies to M6809 microprocessors, while Figure 6 shows the mode applicable to the M68000. Selection of multiplexed or non-multiplexed buses is a programmable option that can be invoked through the configure address/data multiplex (CADDRAT) bit. With the 8031 controller, address outputs A0–A7 are multiplexed with the data D0–D7 input/output lines to create a composite AD0–AD7 bus.

The PSD3XX's input latches can be programmed to catch a valid address when the microcontroller's ALE signal transitions from active HIGH to inactive LOW. The polarity of the ALE signal is also a programmable feature in the CALE field of the configuration table. Address latching can be programmed to occur on either an active HIGH or an active LOW ALE signal. With Intel devices, the address is valid when ALE is HIGH. Once latched, data or code can be read from, or written to, the PSD3XX. The CALE active HIGH or LOW ALE configuration bit only applies to addresses A0–A15. A separate configuration bit, (CADDHLT), exists for the control of the higher-order address inputs

PSD3XX General System Configuration (Cont.)

(A16–A19). If necessary, these addresses can also be latched by the host system.

The highest address input is A19 but this signal can be omitted in favor of a power-down chip-select input ($\overline{CSI}$). A19/$\overline{CSI}$ is selected by the CA19/$\overline{CSI}$ configuration bit. When the $\overline{CSI}$ input is selected and the pin is driven HIGH, the device can be powered-down consuming only standby power. When configured with other CMOS devices, the standby power is in the 80–250 µA range. Many CMOS microcontrollers do not need a large memory address space; thus, address inputs A16–A19 would be unnecessary. The CA19/$\overline{CSI}$ input can be programmed with a logic LOW to enable a power-down option for power sensitive applications.

The address/data multiplexed scheme also supports the 16-bit processors. In this case, AD0–AD15 convey a 16-bit address qualified by ALE (or AS for the Motorola convention) and 16-bits of data I/O. This feature is shown in Figure 4. A microcontroller that would use this scheme is the 80C196. The M68HC11, like the 8031, uses the 8-bit multiplexed scheme but with the Motorola convention for bus control.

Another control pin used for 80C31 applications used to distinguish between program and data memory is the $\overline{PSEN}$ output. The $\overline{COMB}$/SEP configuration bit should be programmed HIGH if data and memory are separate and LOW to configure a combined memory space in the PSD3XX. This is a useful feature for systems that require program memory and data memory to be in separate blocks.

For systems that use separate data and address buses, the address latches can be set into a transparent mode by clearing the CADDRDAT bit location. Thus, the PSD3XX is suitable for multiplexed or non-multiplexed bus structures employing 8- or 16-bit bus widths.

The RESET input to the PSD3XX enables the device to be initialized at start-up. RESET can be either active HIGH or active LOW depending on the processor type. The CRESET configuration bit selects the polarity of the RESET input: LOW for active LOW and HIGH for active HIGH RESET. Normally, memory systems do not require a RESET input; however, the PSD3XX contains data direction registers for the ports that must be initialized at start-up. Note that all port I/O buffers are automatically programmed as inputs during start-up.

PSD3XX Configuration for Port Reconstruction

A key feature of the PSD3XX is the concept of port reconstruction. When using microcontrollers with additional off-chip memory, port I/O address lines are sacrificed for address, data, and memory control lines. With a multiplexed address/data scheme, two 8-bit controller ports could be lost to address and data. Furthermore, in some control applications, many port I/O bits are required to send actuating signals to solenoids, instrument displays, etc., and receive data through sensors and switch panels. In many control environments, a large amount of I/O capability is required; also, additional external memory is needed for microcontroller instructions to perform data manipulation. Without the PSD3XX, the supplement of extra ports as discrete latches addressed through logic decoders can add a number of chips to the final design. By using the PSD3XX, additional EPROM, RAM, and ports are all provided on one chip. Port reconstruction lets the designer reclaim the two ports sacrificed for the microcontroller's address and data.

Port configuration is achieved through the configuration register bits. CPAF1 configuration of Port A contains eight bits; programming a logic LOW assigns the selected bit with I/O capability as if it were a conventional port. If programmed HIGH, the internally latched address inputs A0–A7 are routed to Port A lines PA0–PA7. This feature enables other on-card peripherals to use A0–A7 as latched addresses. Without this feature, external peripherals to the PSD3XX would require an external octal latch to catch the multiplexed address when it becomes valid at the microcontroller's output. Configuration of Port A as general I/O or address/data is on a bit-wise basis; thus, the choice of port or address/data assignment can be mixed. For example, configuration code 11100000B programmed into location CPAF1 passes addresses A0–A2 to outputs PA0–PA2 and enables PA3–PA7 as conventional port lines.

Configuration bit CPAF2 is a 1-bit location. When programmed LOW, it selects the port/address option, as described above. If CPAF2 is programmed HIGH, port bits PA0–PA7 are set into track mode. Activity on the PA0–PA7 outputs follow logic transitions on inputs AD0–AD7. The multiplexed ad-

PSD3XX Configuration for Port Reconstruction (Cont.)

dress/ data input is tracked through PA0–PA7. Track mode enables the host microcontroller to access a shared memory and peripheral resource through the PSD3XX while maintaining the ability to access its own (private) memory/peripheral resource directly from the microcontroller's address/data outputs. In this mode, the address/data AD0–AD7 passes through the PSD3XX logically unaltered. In summary, PA0–PA7 can be programmed as port I/O or latched address outputs A0–A7 (each bit being programmed on an individual basis), or as AD0–AD7 outputs (track mode).

Port B bits PB0–PB7 can be programmed either as regular port I/Os, or as chip-select outputs $\overline{CS0}$–$\overline{CS7}$ encoded from the PAD outputs. Figure 7 shows the PAD structure as a conventional PLD. Eight bits are programmed into CPBF. Logic LOW indicates that a port pin is a chip-select output derived from the PAD. Programming a logic HIGH sets the appropriate pin as an I/O function. The bit pattern 11111000B programmed into the CPBF location sets up PB0–PB4 as I/O ports and PB5–PB7 as chip-selects. The typical applications, where Port B is programmed as bi-directional, would be with microcontroller chips that need additional port bits. This would be in applications where port reconstruction is needed to drive many indicators, solenoids, read switches, sensors, etc. In large microprocessor-based systems, the chip-select option would probably be chosen; in this case, the PAD outputs select other PSD devices, DRAM memory chips, and peripherals such as timers, UARTs, etc.

The three bits comprising Port C can be programmed by the CPCF configuration bits. This group of three bits define whether Port C is used for inputs (typically A16–A18) or whether the pins are used as chip-select outputs from the PAD. Although labeled as A16–A18, the nomenclature of these pins does not constrain the designer to using these inputs as dedicated higher-order address inputs. In fact, they can be general-purpose inputs to the PAD for processors that do not have an address capability above 64K locations. When the PSD3XX is used with the Z80B microprocessor, the Port C inputs have been programmed as $\overline{MREQ}$, $\overline{IORQ}$, and $\overline{M1}$. In the case of an interface to the M6809B, two inputs of Port C have been converted to chip-select outputs for other memory devices and one output has been used to feedback a READY input to the M6809B. Port C can be used as a general I/O from the PAD in the form of address, control, and chip-select bits. A logic LOW programs a port bit as an input; a HIGH programs it as an output.

Chapter 2

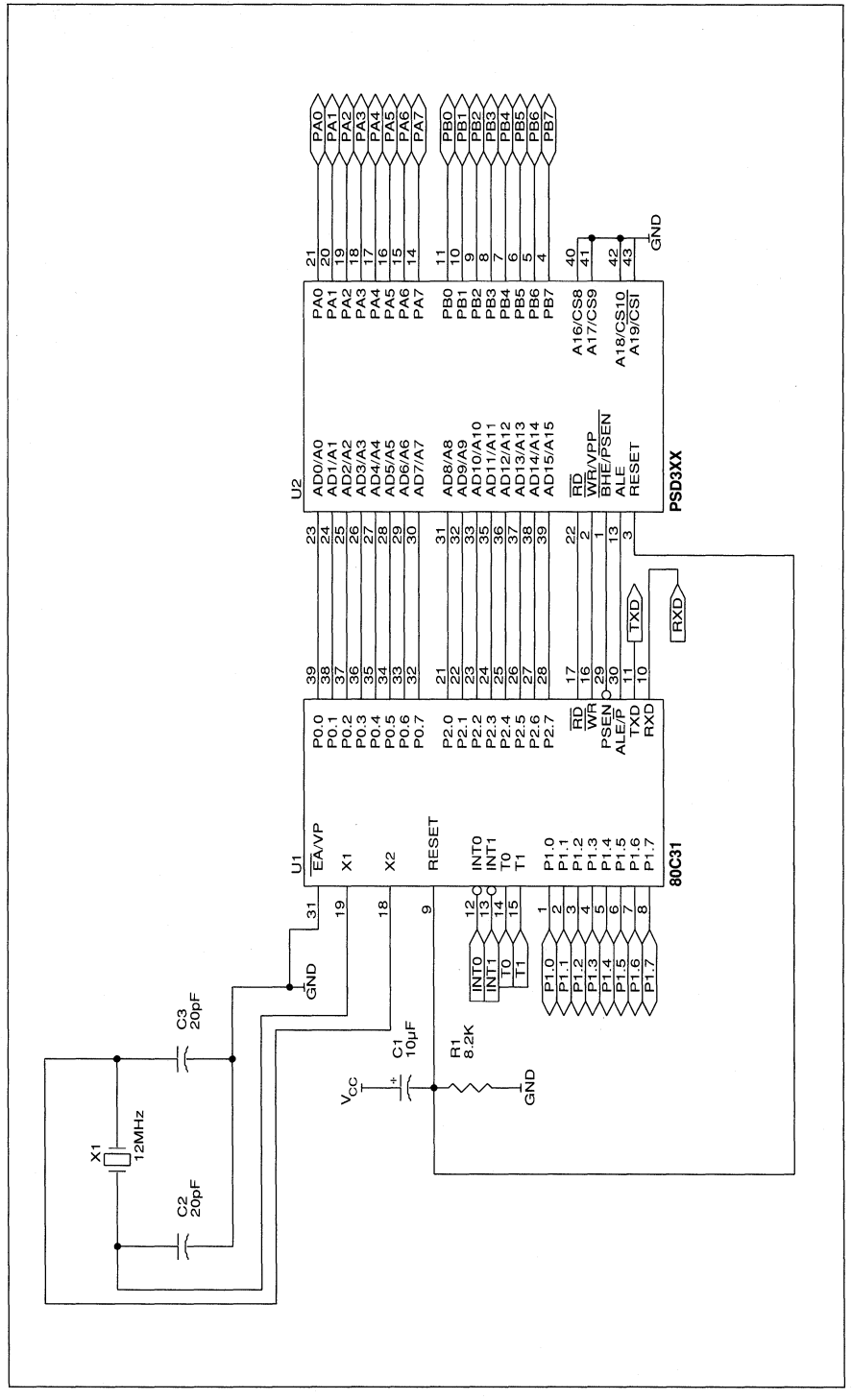
8-Bit Microcontroller to PSD3XX Interface

Figure 10 illustrates the minimum configuration of one controller and one PSD3XX. The application illustrates port reconstruction through the device's Port A and Port B I/O, reconstituting port 2 and port 0 of the microcontroller. Table 3 gives the configuration information that would be programmed in the configuration section of the PSD. Table 3 shows that both port I/Os have been programmed with CMOS load and drive characteristics. A feature of the 8051/8031 family is the $\overline{PSEN}$ signal, which determines whether the memory selection is active for executable code or data. This family of controllers has separate memory locations for code and data. To maintain full compatibility, the PSD3XX is also capable of being programmed to respond to the $\overline{PSEN}$ signal. When A16–A18 are programmed as inputs but not driven, they should be tied active HIGH or LOW. Unused inputs to the PSD3XX must not be permitted to float. Tying can be avoided on unused A16–A18 lines if these are programmed as 'dummy' $\overline{CS8}$–$\overline{CS10}$ outputs. A19/$\overline{CSI}$ cannot be programmed as an output; thus, it must be tied if not used.

Table 3. Small Controller System with One 80C31 and One PSD3XX

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set $\overline{CSI}$ input power-down mode
CALE	0	Active HIGH ALE
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	1	Code and data memory separate
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A (0–7)
CPBF	FFH	Input/Output Port B
CPCF	000B	Port C programmed for inputs
CPACOD	00H	Configure CMOS outputs Port A
CPBCOD	00H	Configure CMOS outputs Port B
CADDHLT	0	Transparent inputs A16–A19
CSECURITY	0	No security

Figure 10. 80C31/PSD3XX Applications



Two PSD3XX Byte-Wide Interfaces to the Intel 80C31

Figure 11 illustrates an extension to the previous design in that two PSD3XX devices have been used, doubling the memory and port resources of the system solution. In this application, the power-down capability has been used so that one PSD3XX can be active while the other device is in power-down mode. The mean power consumption is reduced, so this configuration can be considered for power-sensitive applications.

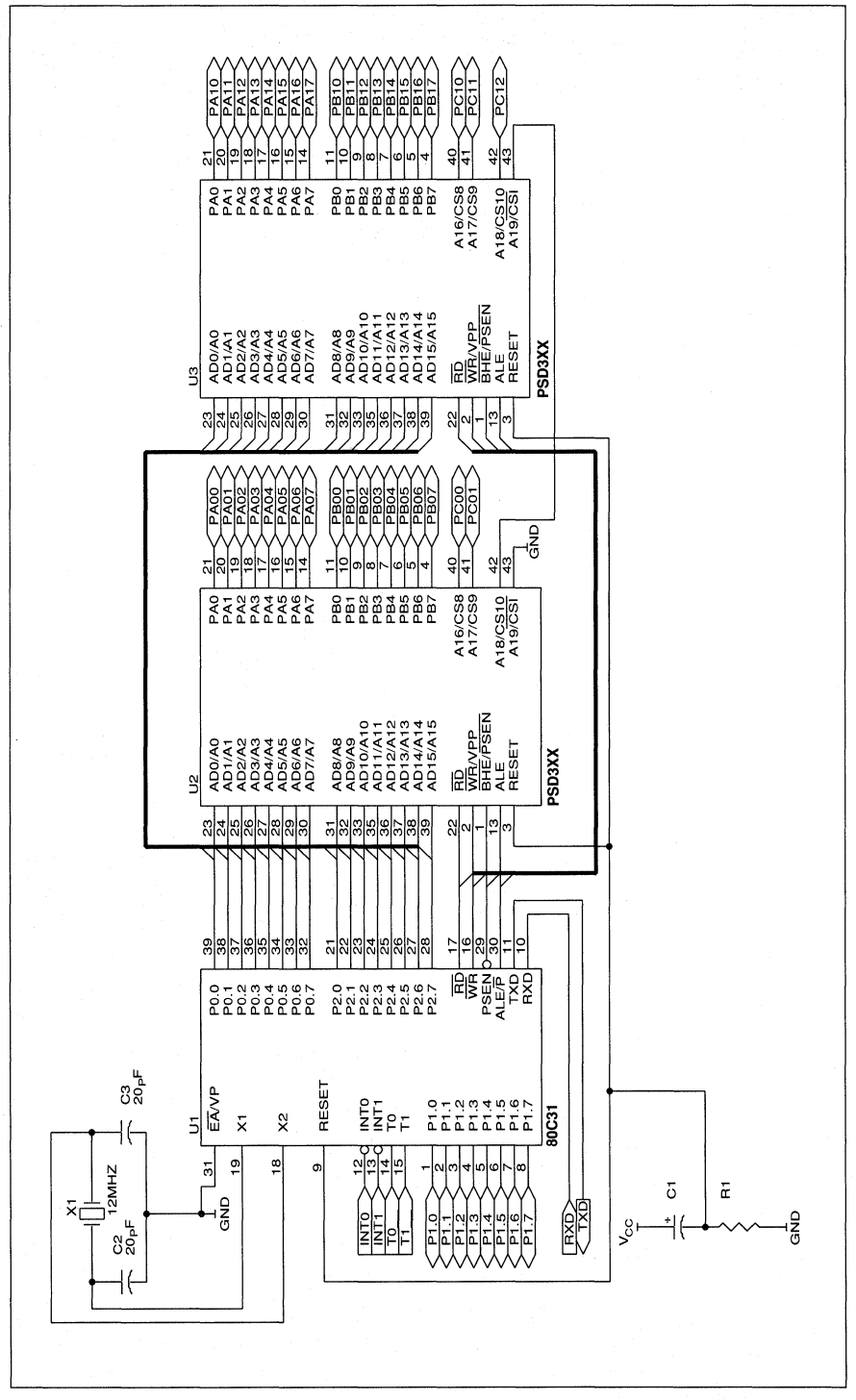
The configuration Table 4 indicates that Port C has been configured as outputs. Provided one PSD3XX is powered up for the whole address range, its PAD can decode an address range to select and deselect the second PSD3XX device through the $\overline{CS10}$ output. In Figure 11, the PAD output A18/$\overline{CS10}$ on PSD3XX U2 can be used to power-down the second PSD3XX through the A19/$\overline{CSI}$ input.

Table 4. 80C31 Interface to Two PSD3XX Devices with Power Economy Feature

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set $\overline{CSI}$ input power-down mode
CALE	0	Active HIGH ALE
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	1	Code and data memory separate
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A (0–7)
CPBF	FFH	Input/Output Port B
CPCF	111B	Outputs $\overline{CS8}$–$\overline{CS10}$
CPACOD	00H	Configure CMOS outputs Port A
CPBCOD	00H	Configure CMOS outputs Port B
CADDHLT	X	"Don't care" for latched A16–A19
CSECURITY	0	No security

It is not recommended that the two PSD3XX devices select each other because the PAD section of a PSD device is powered down with the rest of the device. At least one PAD decoder must be kept active to select and deselect others. Port C outputs $\overline{CS16}$–$\overline{CS18}$ can power-down as many as three other PSD3XX devices.

Figure 11. 80C31/2/PSD3XX Applications



PSD3XX M68HC11 Byte-Wide Interface

Figure 12 illustrates the configuration of an M68HC11 microcontroller which also uses the 8-bits wide multiplexed address/data bus. The application is similar to that given in Figures 6 and 7 except that the R/$\overline{W}$ and E control lines have been invoked to establish compatibility with the Motorola device. The address strobe output from the M68HC11 is HIGH so the AS(ALE) input is set HIGH. The SRAM and EPROM section are programmed as combined and both Ports A and B are enabled as I/Os with CMOS drives. Port C is programmed with chip-select outputs $\overline{CS8}$–$\overline{CS10}$. Other PSD3XX devices can be mapped into the addressing scheme or the lines can be programmed to transition as strobes in defined mapping areas. The latch enable bit for the higher-order address lines A16–A19 is not used establishing a don't care condition. The CADDHLT condition must be selected if any one of A16–A19 lines is selected as input to the PSD.

In this design, the security bit is programmed. This bit prevents the reading of the PAD configuration by an unauthorized user. Furthermore, if the security bit has been programmed, standard programming machines can not read the internal code of a PSD3XX . However, data can always be read from the EPROM, RAM, and ports. This provides normal use of the device. If the address map in the PAD cannot be interpreted, the actual location of data within the address and I/O space is difficult to determine. Besides programming the CSECURITY bit, added security can be applied by scrambling the sequence of address and data inputs. A short PASCAL or 'C' program can be written to reorganize the original Intel MCS code to be aligned with the scrambled pins. Table 5 indicates the configuration for the M68HC11/ PSD3XX interface.

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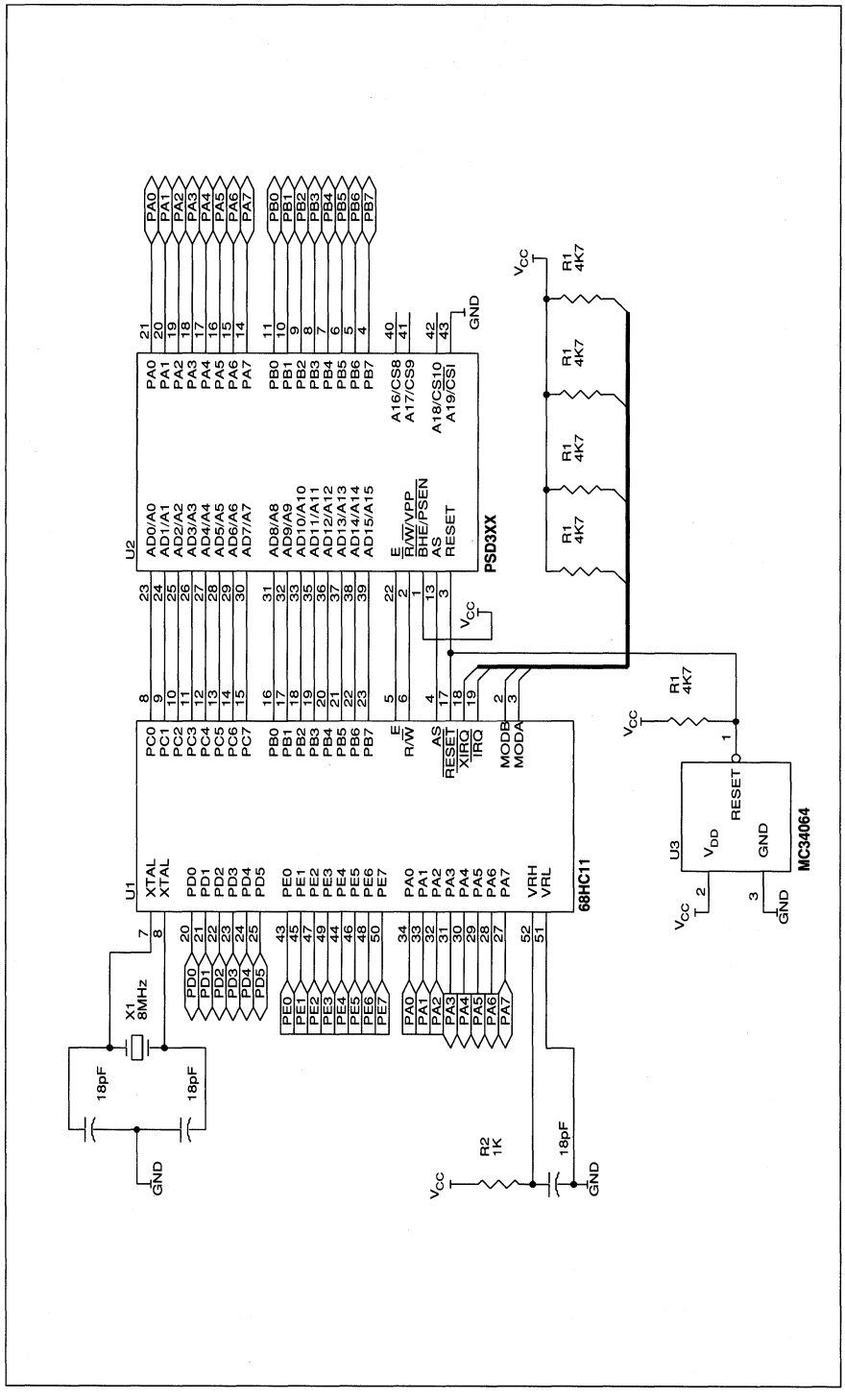
Table 5. M68HC11 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Enable $\overline{CSI}$ input
CALE	0	Active HIGH AS (ALE)
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Input/Output Port A
CPAF1	00H	Input/Output Port A
CPBF	FFH	Input/Output Port B
CPCF	111B	Output $\overline{CS8}$–$\overline{CS10}$
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	X	"Don't care" A16–A19 not used
CSECURITY	1	Security on

Figure 12. 68HC11/PSD3XX Applications



8-BIT Non-Multiplexed PSD3XX Interface to M68008

Figure 13 illustrates an application in which the address and data are not multiplexed. The M68008 has an 8-bit data bus and 20-bit address bus. The PSD3XX can be programmed to support the microprocessor by providing data I/O through Port A. The address lines from the microprocessor go to inputs A0–A19. Port B outputs are used for external chip-selects to other MAP devices or other memory resources. The configuration has been set for compatibility with Motorola control signals. There are six chip-select outputs ($\overline{CS0}$–$\overline{CS5}$) and an address decode for $\overline{DTACK}$ and $\overline{BERR}$. The PAD decodes an address range which is fed back to the microprocessor through these inputs. Using the open-drain configuration has been implemented in Port B bits 6 and 7. The two pull-up resistors enable external memory and peripherals to access the $\overline{DTACK}$ and $\overline{BERR}$ inputs as a wired-OR function.

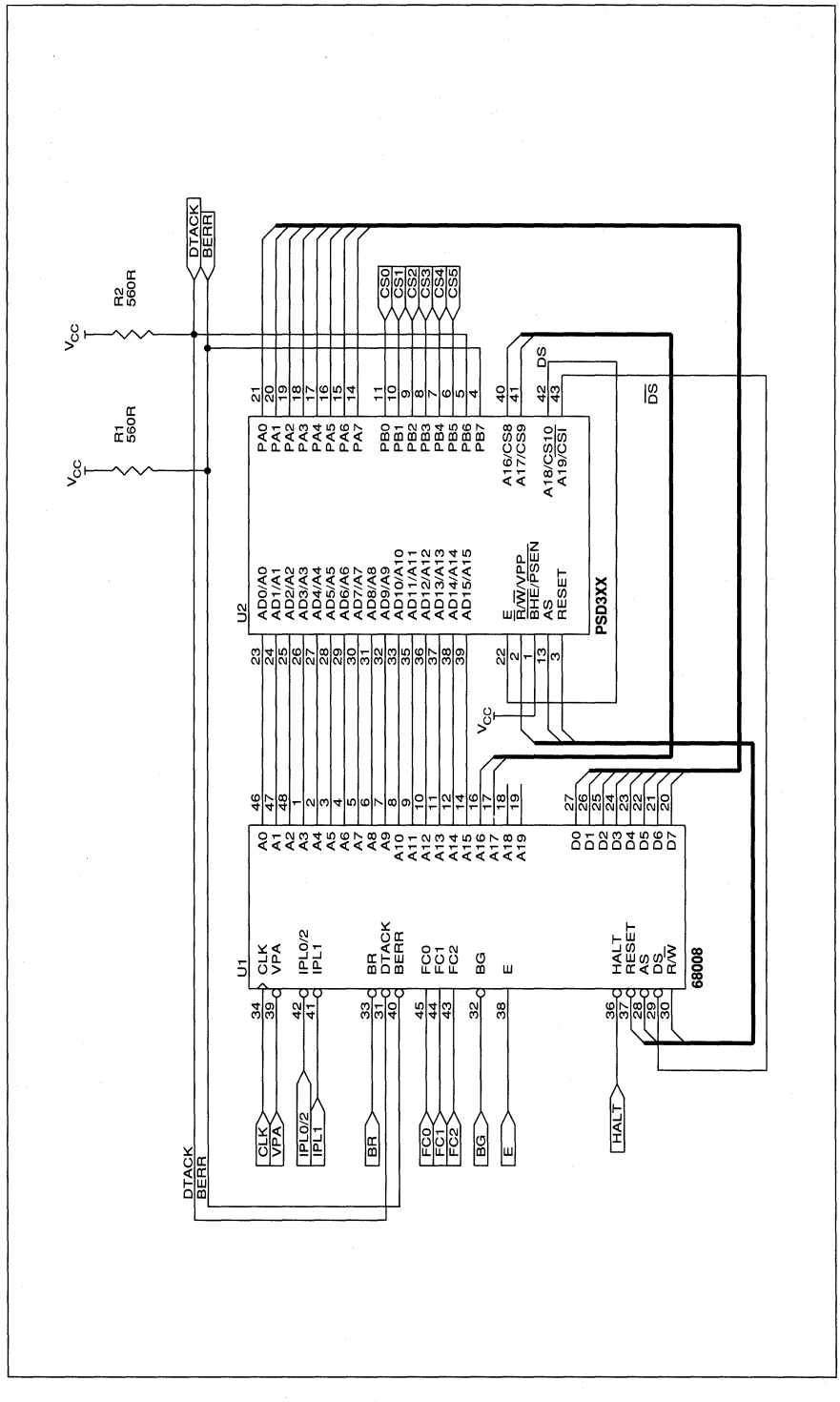
If other PSD3XX devices are mapped into the M68008 system, no additional glue logic is needed to avoid possible bus contention on these lines. In this application, ALE(AS) can be used as a general-purpose logic input to the PAD because the function of ALE becomes redundant in a non-multiplexed address/data bus. Also shown in Figure 13 is a method of inverting the active LOW $\overline{DS}$ (Data Strobe) M68008 output. The A19 input is enabled to the PSD internal PAD and inverted at the output of $\overline{CS10}$ to drive the PSD3XX E input. The E input must be active HIGH but $\overline{DS}$ is active LOW and qualifies a valid data transfer. Thus, the PAD must perform a signal inversion. The E signal output from the M68008 is used to interface to Motorola 8-bit peripherals. However, with Motorola microcontroller families such as the M68HC11, the E signal output can drive the E input to the PSD3XX. Table 6 gives the configuration information associated with the design given in Figure 13.

Table 6. M68008 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	1	Enable A19 input[1]
CALE	X	"Don't care" non-multiplexed mode
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	00H	Port B used for chip-selects
CPCF	001B	Configure A16 and A17 In, $\overline{CS10}$ Out[2]
CPACOD	00H	CMOS drivers
CPBCOD	3FH	CMOS drivers, PB6, PB7 open drain
CADDHLT	0	Address latch transparent A16–A19
CSECURITY	1	Security on

1. The $\overline{DS}$ output from the M68008 drives the A19 input to the PSD3XX.
2. The internal PAD of the PSD3XX inverts the $\overline{DS}$ input to drive its own E input from the $\overline{CS10}$ PAD output. A16 and A17 are programmed as PSD inputs.

Figure 13. M68008/PSD3XX Applications



16-Bit Non-Multiplexed Address/Data PSD3XX Interface to M68000

An extension to the design is shown in Figure 14, with the configuration information shown in Table 7. The M68000 interface to the PSD3XX has a 16-bit data bus. Both Ports A and B are used to convey data. The generation of an E input to the PSD3XX has been extended from the signal inversion shown in Figure 13. The M68000 has two data strobe signals ($\overline{LDS}$ and $\overline{UDS}$), to qualify the lower and upper bytes of a 16-bit word. The $\overline{LDS}$ and $\overline{UDS}$ lines drive the A18 and A19 inputs and are gated to provide the correct logic condition into the M68000.

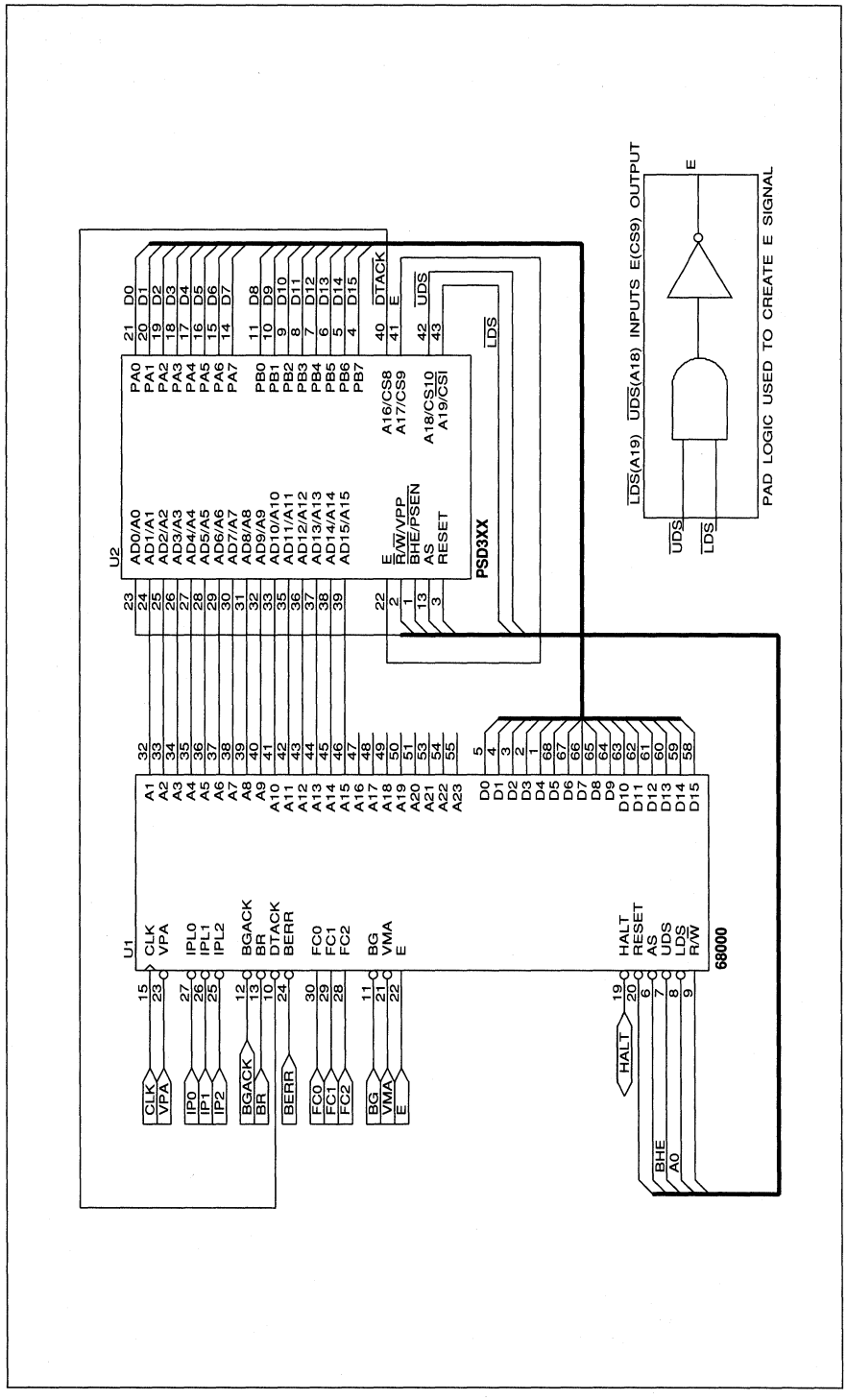
Table 7. M68000 Microprocessor to one PSD3XX Interface

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E control inputs
CA19/$\overline{CSI}$	1	Enable A19 input
CALE	X	ALE polarity set at "don't care"
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A
CPAF1	XX	"Don't care" Port A
CPBF	X	"Don't care" Port B
CPCF	110B	Enable A16 and A17 Out, A18 In[1]
CPACOD	00H	Configure CMOS buffers Port A
CPBCOD	00H	Configure CMOS buffers Port B
CADDHLT	0	Transparent A16–A19
CSECURITY	0	Security off

1. Outputs $\overline{UDS}$ and $\overline{LDS}$ drive the A18 and A19 inputs of the PAD and are gated internally to give a valid E input signal to the M68000 from the $\overline{CS9}$ output. DTACK comes from the $\overline{CS8}$ output.

This application takes advantage of the AS input which is redundant as a latch control input in a non-multiplexed system; however, it can be used as general-purpose logic input to the PAD. $\overline{CS9}$ and $\overline{CS8}$ are used as output signals to the M68000's DTACK and BERR inputs.

Figure 14. M68000/PSD3XX Applications



M68000/ 2X PSD3XX Applications

With the circuit design given in Figure 15, two PSD3XX devices are used in a byte-wide mode. One PSD stores the upper data byte and one the lower data byte of a 16-bit word. By using the devices in this way, two 6-bit wide ports can be created in Port B of each device. PB6 and PB7 are programmed as open-drain outputs and wired-OR giving composite DTACK and BERR feedback signals to the M68000. The generation of the E signal for both PSD devices is achieved in the same way it was in the M68008. The $\overline{LDS}$ and $\overline{UDS}$ inputs (to U2 and U3 respectively) are inverted by the PAD and drive the relevant E inputs. Table 8 gives the configuration information relevant to both PSD devices.

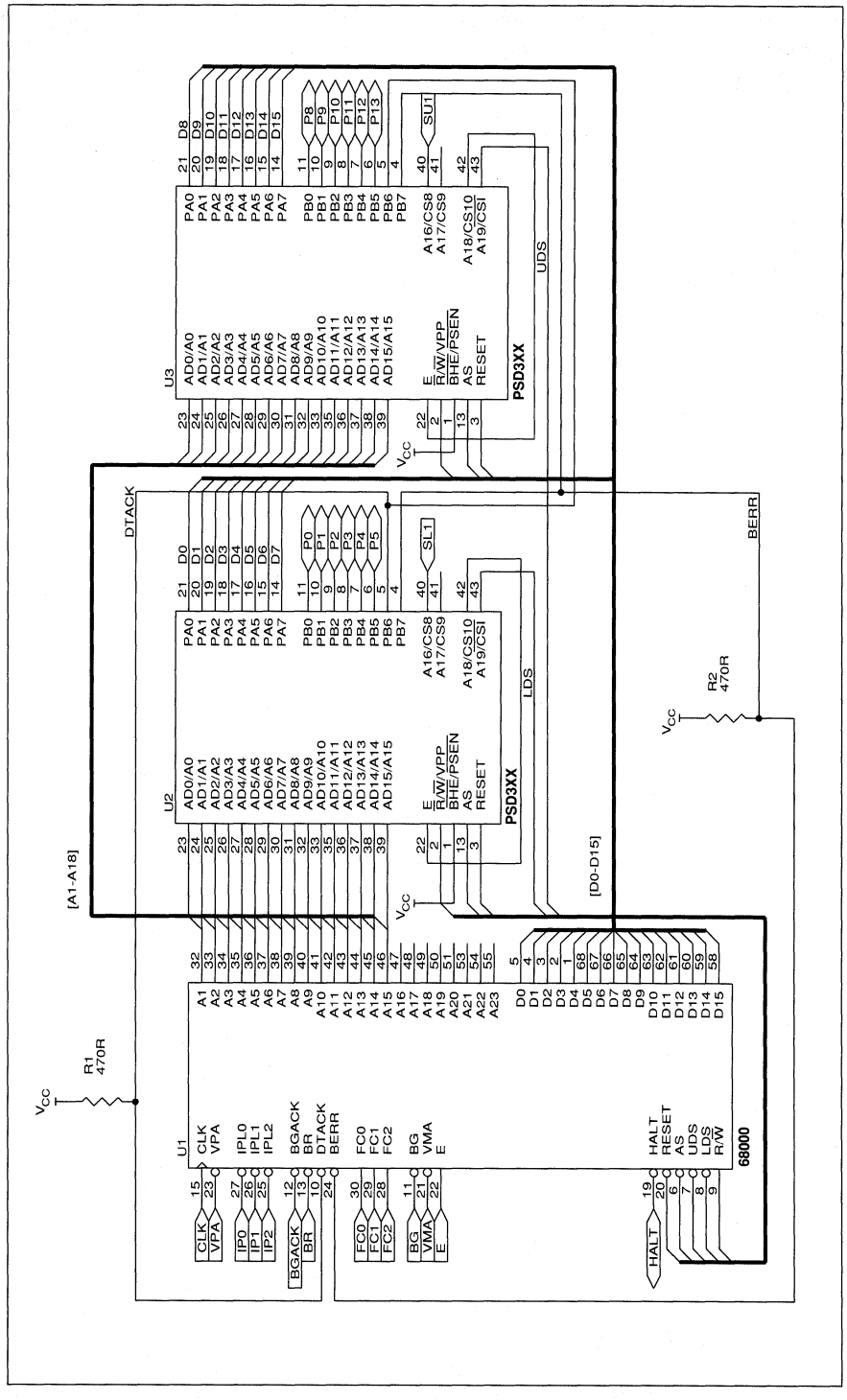
Table 8. M68000 Microprocessor to Two PSD3XX Devices in Parallel

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E control inputs
CA19/$\overline{CSI}$	1	Enable A19 input[1]
CALE	X	"Don't care" not used
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	Port B used for I/O
CPCF	111B	Configure $\overline{CS8}$–$\overline{CS10}$[2]
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Transparent A19
CSECURITY	0	No security

1. A19 input to the PSD3XX's is used to receive $\overline{UDS}$ and $\overline{LDS}$ from the M68000 microprocessor. These signals are inverted by the PAD of each PSD3XX and fed back to the E input of each divice.

2. $\overline{CS10}$ of each PSD3XX drives the inverted $\overline{UDS}$ and $\overline{LDS}$ back to E input. Port C is programmed to output $\overline{CS8}$ and $\overline{CS9}$. Additional byte-wide peripherals can be configured to the system and selected by these signals.

Figure 15. M68000/ 2X PSD3XX Applications



16- Bit Address/ Data PSD3XX Interface to Intel 80186

Figure 16 and Table 9 give the configuration of the PSD3XX in an Intel 80186 system. This device has a 16-bit multiplexed address/data bus. Ports A and B are used for data I/O functions, so this design can take advantage of the port expansion capability. To distinguish between memory and I/O functions, it is necessary to decode the S2 output from the 80186. This output line goes directly to the PAD through Port C bit zero. When LOW, this signal qualifies a memory access; when HIGH, it indicates that an I/O operation is in progress. Programming the PAD can use this input to differentiate between I/O and memory access.

Two additional signals from the 80186 are $\overline{UCS}$ and $\overline{LCS}$ (upper chip-select and lower chip-select, respectively). The signals have been included in the system to help minimize the requirement for additional glue logic. Both can be used in the PAD decoder to position sections of EPROM and RAM. The $\overline{UCS}$ is designed to decode addresses FFFFFH to a programmable limit. The 80186 begins executing from memory location FFFF0H after a system reset; thus, this signal should be used to select EPROM that contain a system initialization sequence. The $\overline{LCS}$ has been designed to program from 00000H up to a programmable limit. In this example, the RESET line from the 80186 is active HIGH and drives the RESET input of the PSD301 which is programmed to respond to a HIGH level.

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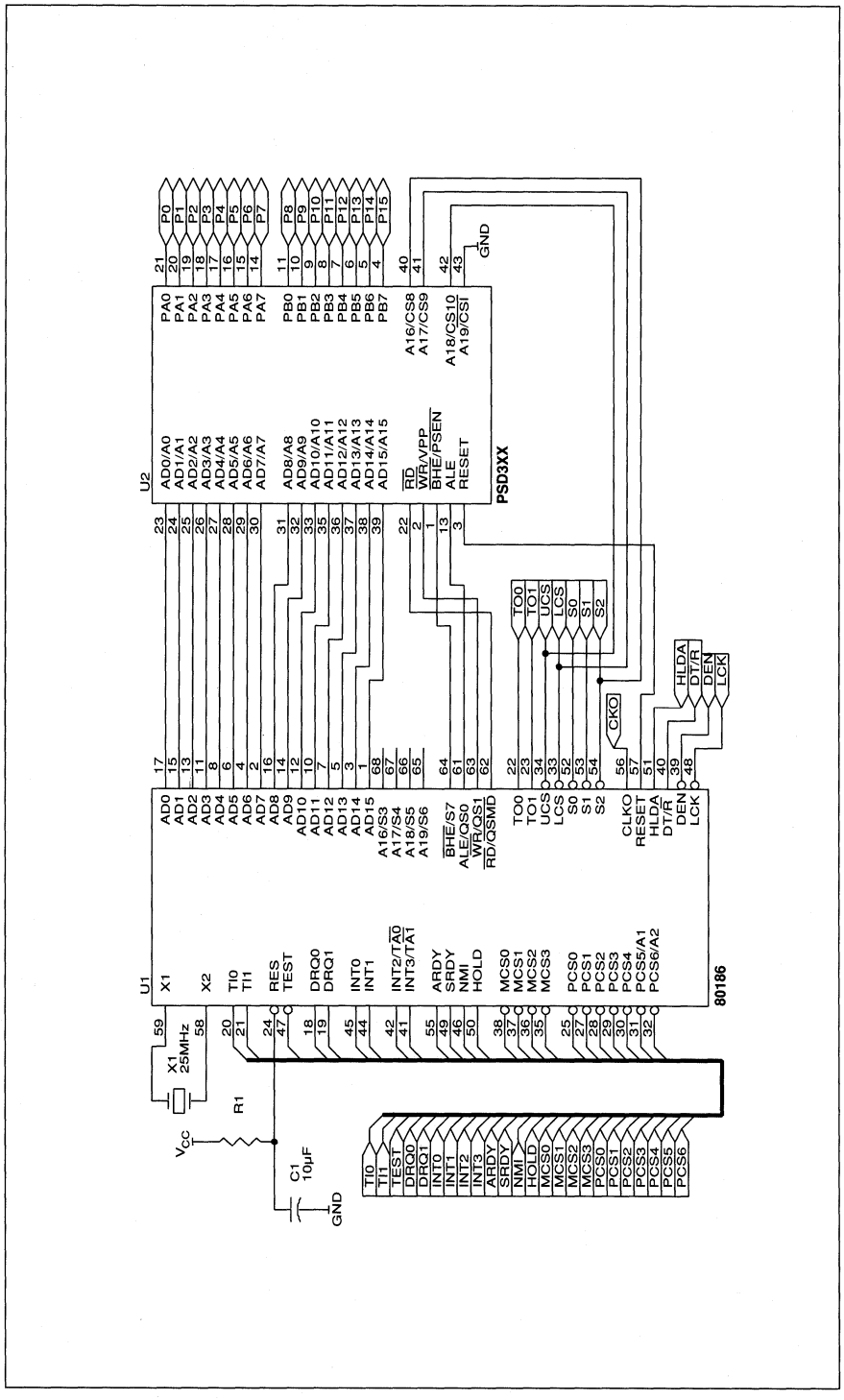
Table 9. Intel 80186 to PSD3XX Configuration for CMOS Ports

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	1	$\overline{CSI}$ input to PAD
CALE	X	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	I/O Port A
CPAF1	XXH	I/O Port A
CPBF	FFH	I/O Port B
CPCF	000B	Input A16–A18
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Latched A16–A19
CSECURITY	0	No security

Figure 16. Intel 80186/ PSD3XX Applications



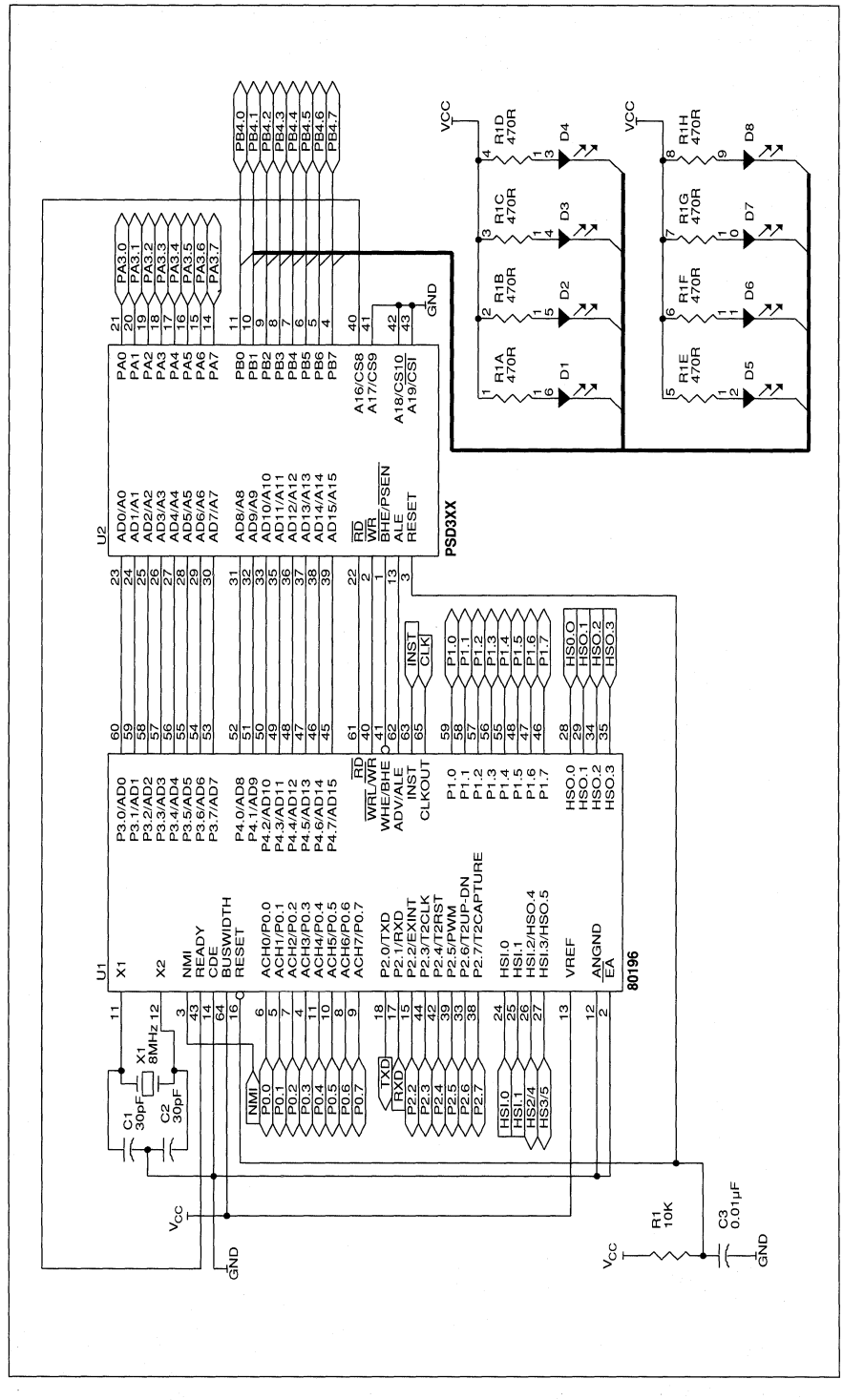
16-Bit Address/ Data PSD3XX to Intel 80196 Interface

In Figure 17, the PSD3XX is connected to an Intel 80196 microcontroller. In many microcontroller applications it is necessary to illuminate indicators (such as LEDs). Here, the PSD3XX is used to drive LED indicator displays. High-efficiency LEDs can be illuminated through the open drain outputs of Port B. The configuration information in Table 10 indicates that Port B has open drain drivers to sink LED illumination current.

Table 10. Intel 80196 to PSD3XX Configuration for LED Drivers

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	X	"Don't care" A19/$\overline{CSI}$
CALE	0	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	I/O Port A
CPAF1	00H	I/O Port A
CPBF	FFH	I/O Port B
CPCF	000B	Output A16–A18
CPACOD	00H	CMOS drivers
CPBCOD	FFH	Open drain drivers
CADDHLT	X	"Don't care" (not used)
CSECURITY	0	No security

Figure 17. Intel 80196/ PSD3XX Application Open Drain Drivers



Interfacing the PSD3XX to 8-Bit Microprocessors Z80 and M6809 Applications

Figures 18 and 19 illustrate the PSD3XX used with 8-bit microprocessors, such as the Z80B and M6809B. Tables 11 and 12 reflect the configuration of each design, respectively. The mode of operation is 8-bit data bus with a non-multiplexed address/data input. In the case of the Z80B, $\overline{CS8}$–$\overline{CS10}$ inputs are tied to $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$ respectively. Since the PAD can be programmed to distinguish between memory and I/O operations, the Z80B system has access to an 8-bit data port Port B. With the M6809B system, $\overline{CS8}$ is used to respond to the MRDY input of the microprocessor and $\overline{CS9}$ and $\overline{CS10}$ are available for external chip-select.

Table 11. Z80B to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	$\overline{CSI}$ input
CALE	X	"Don't care" (not used)
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	I/O Port B
CPCF	000B	Configure A16–A18 as inputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	A16–A18 transparent[1]
CSECURITY	0	No security

1. A16–A18 inputs are used as $\overline{M1}$, $\overline{MREQ}$, and $\overline{IORQ}$ inputs to the PAD from the Z80B output. Use the ALIAS command in the support software.

Table 12. M6809 to PSD3XX Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Enable $\overline{CSI}$ input
CALE	X	"Don't care" non-multiplexed mode
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	FFH	Port B used for I/O
CPCF	111B	$\overline{CS8}$–$\overline{CS10}$ outputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	"Don't care"
CSECURITY	0	No security

Figure 18
Z80B/PSD3XX
Applications

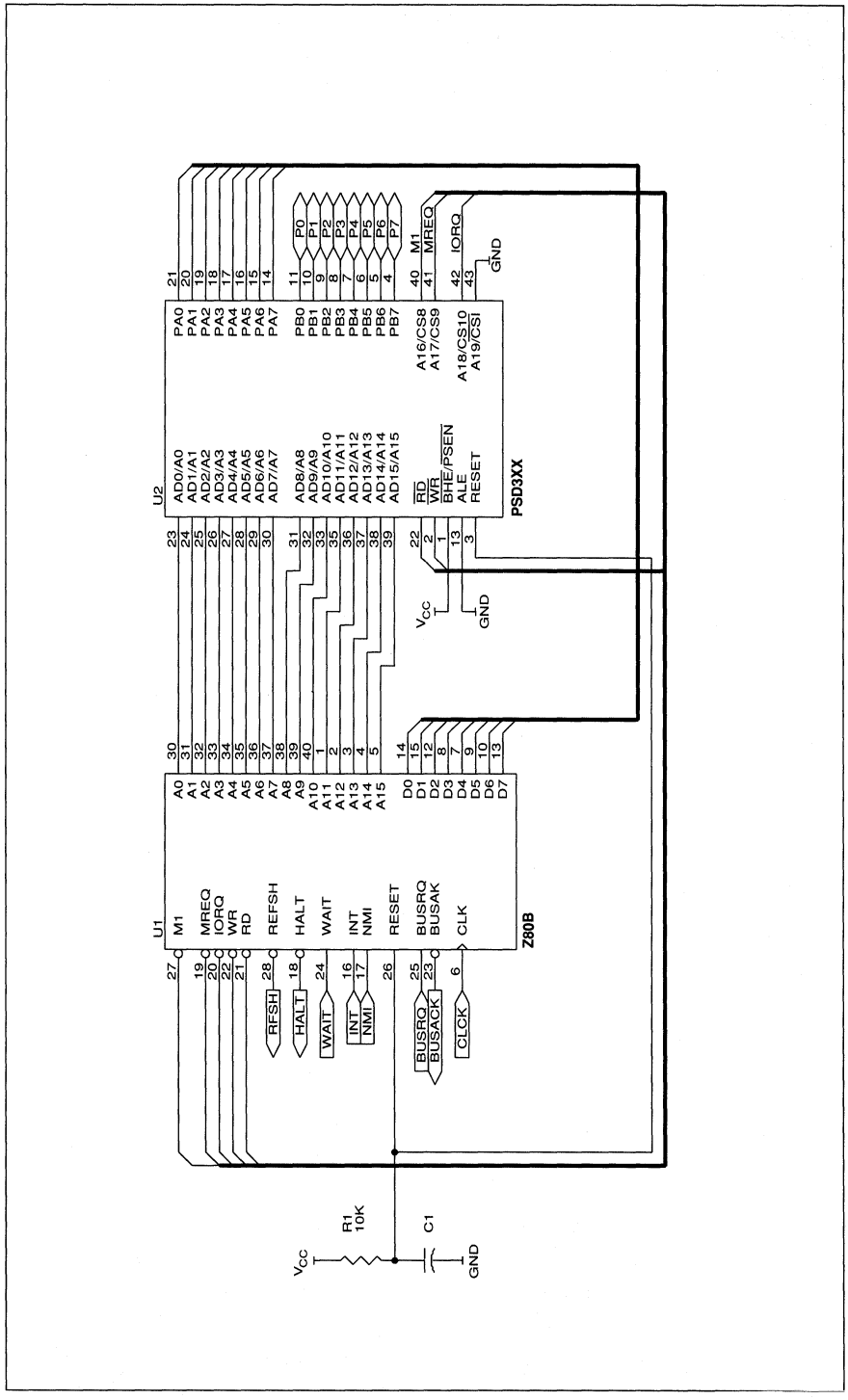
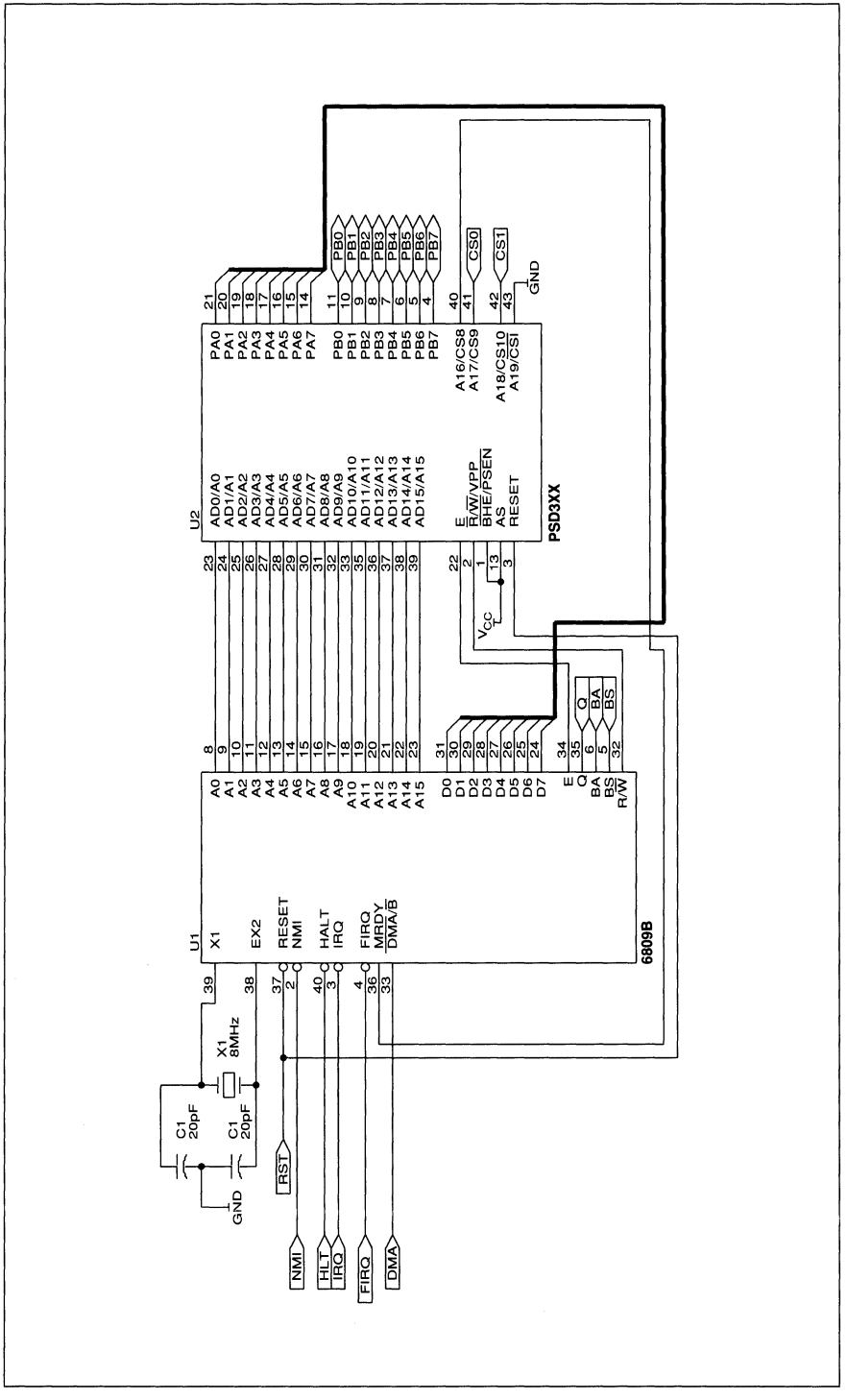


Figure 19
6809/PSD3XX
Applications



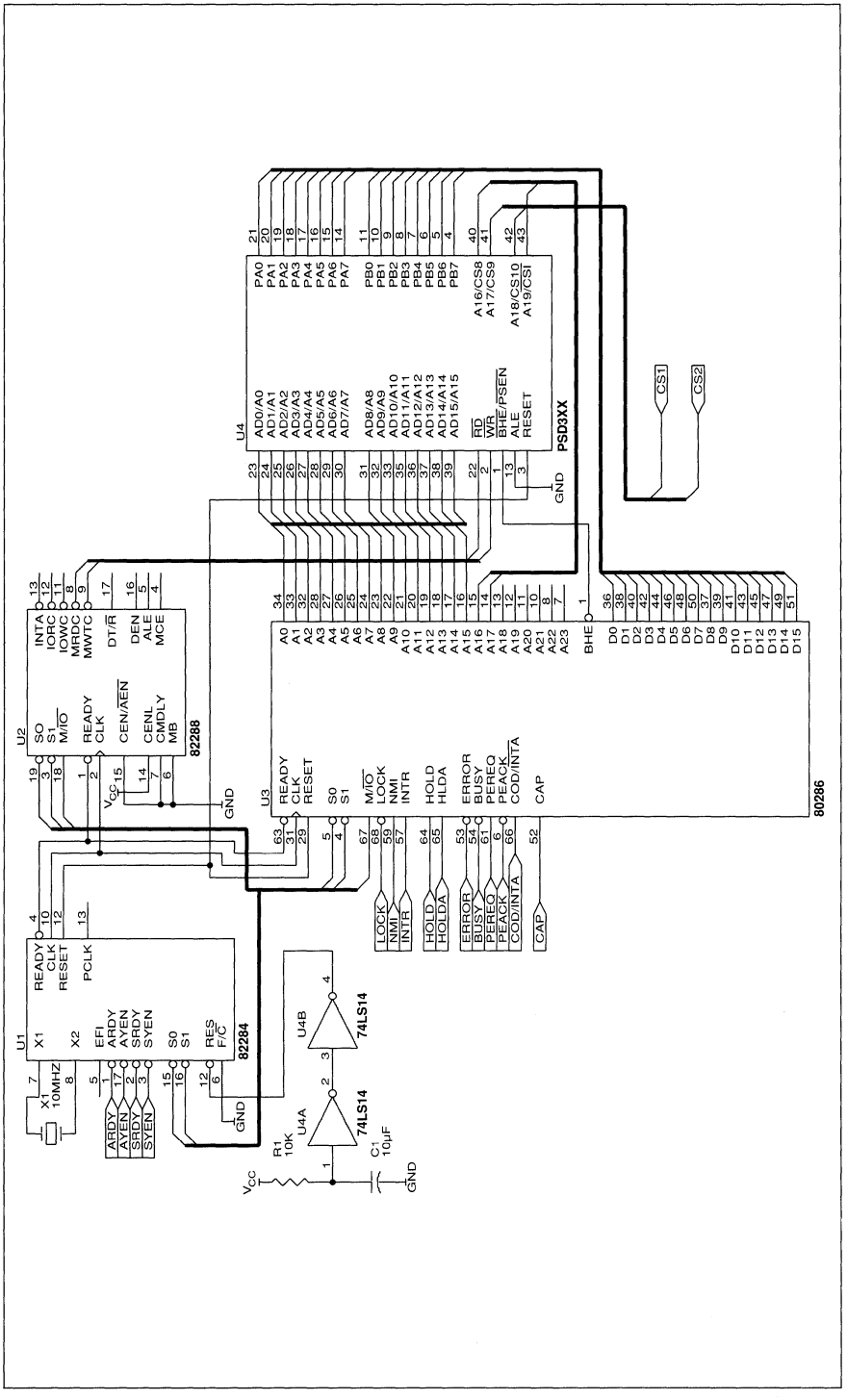
PSD3XX Interface to the Intel 80286

Figure 20 provides a schematic of the PSD3XX interface to an 80286. The device is configured for a 16-bit data bus in the non-multiplexed mode. Ports A and B are converted automatically for use as a bi-directional data path into the PSD3XX. (This was also the case for the M68000 microprocessor). To eliminate (or lessen) glue logic, $\overline{CS1}$ and $\overline{CS2}$ are generated from the internal PAD. This is programmed as an address decoder. Table 13 provides configuration information relevant to this system design.

Table 13. Intel 80286 to PSD3XX Interface

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	0	Non-multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ control inputs
CA19/$\overline{CSI}$	1	Enable A19 input
CALE	X	"Don't care" non-multiplexed mode
CRESET	1	Active HIGH RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	X	"Don't care" Port A used for data
CPAF1	XXH	"Don't care" Port A used for data
CPBF	XXH	"Don't care" Port B used for data
CPCF	011B	A16 input; $\overline{CS9}$ and $\overline{CS10}$ outputs
CPACOD	00H	CMOS drivers
CPBCOD	00H	CMOS drivers
CADDHLT	0	Transparent A16–A19 input
CSECURITY	0	No security

Figure 20 Intel 80286/ PSD3XX Applications



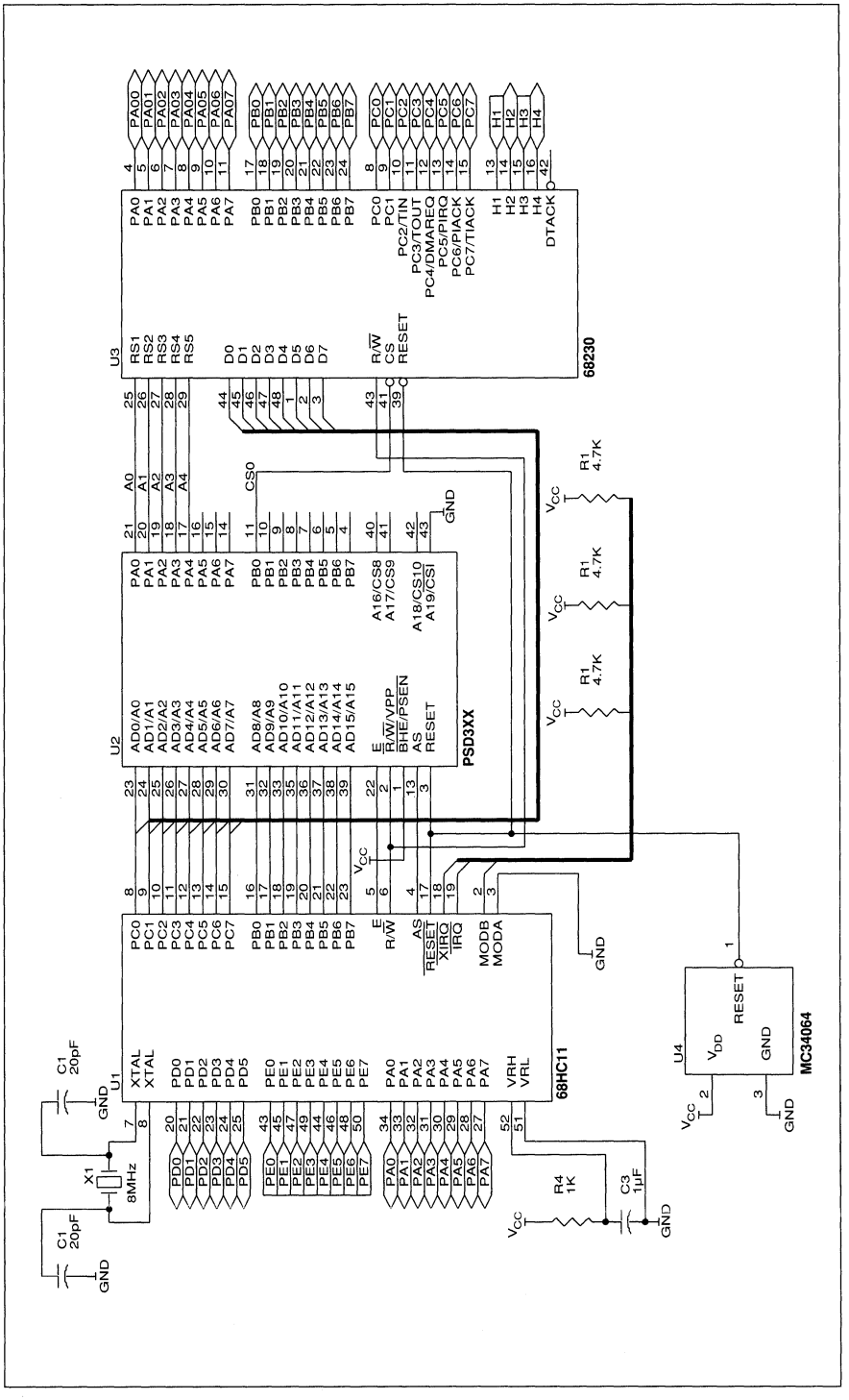
External Peripherals to the PSD3XX/M68HC11 Configuration

The configuration in Figure 21 illustrates how the user can feed address outputs from the internal latch to Port A. Addresses A0–A7, derived from a multiplexed address/data bus, can go directly to an additional peripheral without the need for an additional octal latch such as the 74HC373 or 74HC573. Port A can be used for address outputs A0–A7 while PB0–PB7 can be used as chip-selects. Lines A0–A4 of the PSD3XX drive the RS1–RS5 register select inputs of the M68230. For the M68HC11, the eight bits of address and data come from its PC port PC0–PC7 (AD0–AD7) and are latched by the AS input. Configured in this mode, the PSD3XX can address and map additional peripheral chips. Port A of the PSD3XX conveys the internally latched address outputs A0–A7 to the output and can be used to address registers in the peripheral chips while Port B outputs can place individual peripherals at peripheral or memory-mapped boundaries. Thus, a number of additional chips can be selected through Port B. This effectively can increase the port density of the system design. The general I/O capability can then be extended to extra ports, timers, UARTs, serial communications channels, keyboard interface devices, CRT controllers, etc. without the need for additional glue logic. Table 14 highlights the configuration information programmed into the PSD3XX when configuring the M68HC11 to a M68230 peripheral.

Table 14. M68HC11/PSD3XX to External Peripheral M68230 Interface

Configuration	Bits	Function
CDATA	0	8-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH AS
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Port A = address A0–A7
CPAF1	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	X	"Don't care"
CSECURITY	0	No security

Figure 21
M68HC11/PSD3XX to M68230 Applications



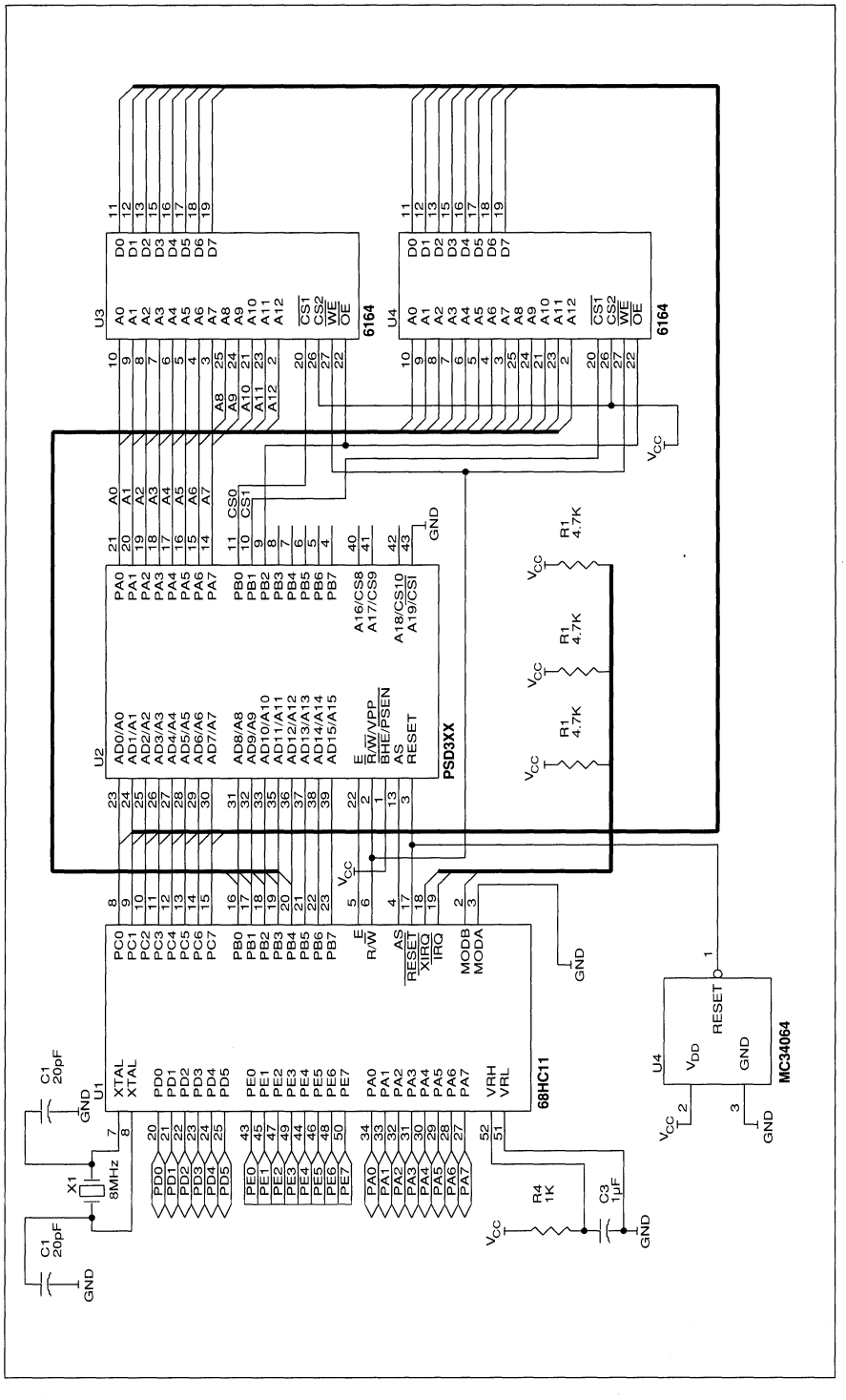
Additional External SRAM

Figure 22 illustrates how additional SRAMs can be configured into a system. This PSD3XX configuration is not limited to external peripheral expansion; it can also be used to add additional memory without the need for external glue logic. With an 8-bit address/data multiplexed scheme, the higher-order addresses (A8–A15) are non-multiplexed. These address lines are fed directly to the external SRAM from the microcontroller and do not need to go through the PSD3XX These lines can drive the RAM chip directly. Thus the M68HC11 system, which is highly memory-intensive and requires more RAM than the microcontroller and PSD3XX can supply, can take advantage of the configuration shown in Figure 23 which is detailed in Table 15.

Table 15. M68HC11/PSD3XX Configured to Address Additional SRAM

Configuration	Bits	Function
CDATA	1	8-bit data bus
CADDRDAT	0	Multiplexed address/data
CRRWR	1	Set R/$\overline{W}$ and E mode
CA19/$\overline{CSI}$	1	Set power-down mode
CALE	0	Active HIGH AS
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Combined memory mode
CPAF2	0	Port A = address A0–A7
CPAF1	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	X	Latched A16–A19 "don't care"
CSECURITY	0	No security

Figure 22. M68HC11/PSD3XX to 16K SRAM Applications



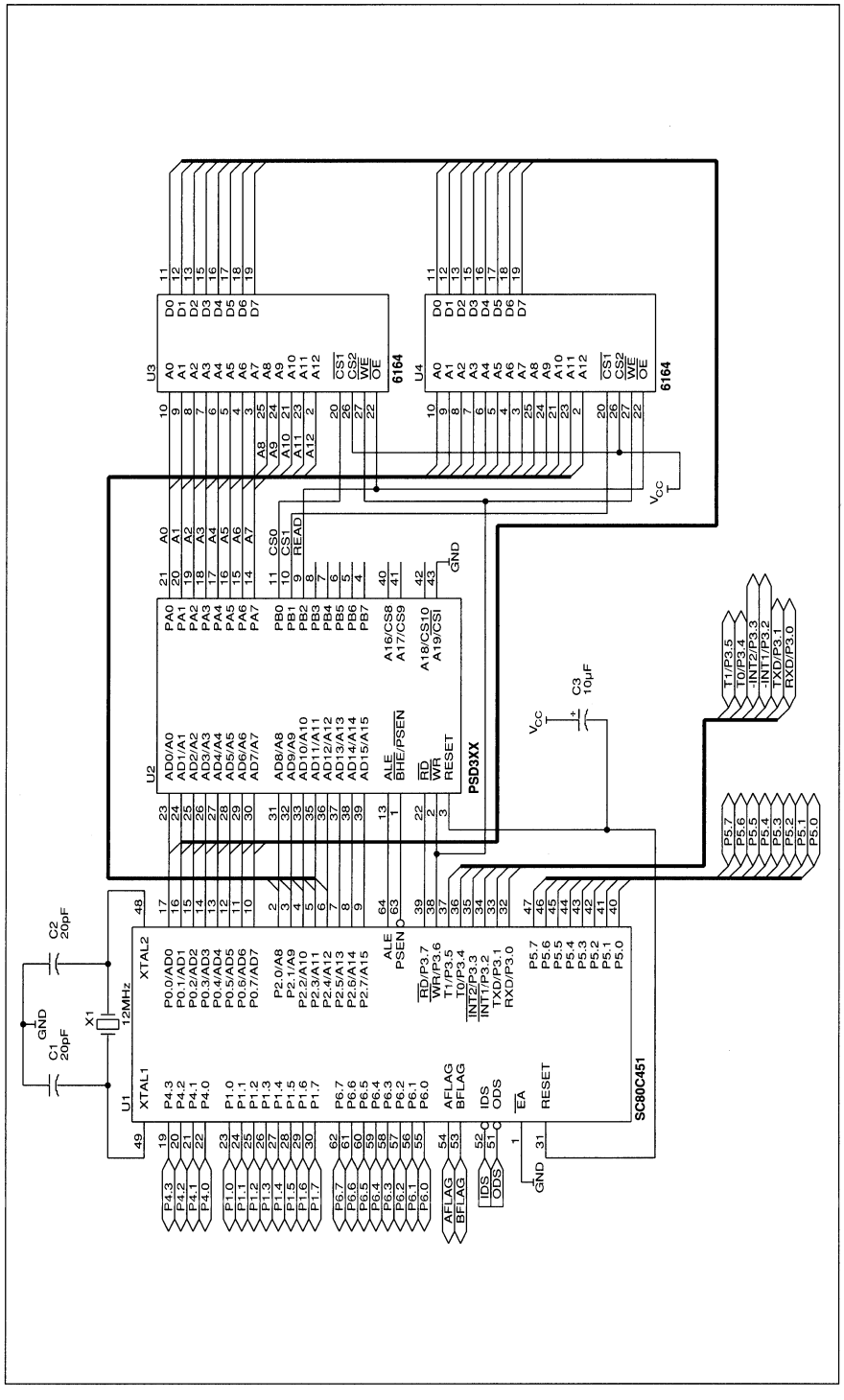
Additional External SRAM (Cont.)

Figure 23 illustrates, and Table 16 details, a similar system using the Signetics SC80C451. This microcontroller has many ports and some SRAM but requires off-chip EPROM to store programmed instructions. This device is similar to the 8051/31 family which uses the active LOW $\overline{PSEN}$ signal to differentiate between executable code and data. Since it is a multiplexed 8-bit machine, it can use the on-chip latches. In highly RAM-intensive applications, an additional two 8K x 8 SRAM chips can be included and selected through Port B. If additional SRAM chips are not needed, Ports A and B can recreate Ports 0 and 2 which are lost in addressing external memory.

Table 16. SC80C451/ PSD3XX Configured to Address Additional SRAM

Configuration	Bits	Function
CDATA	1	8-bit data bus
CADDRDAT	0	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	1	Separate data/program memory
$CPAF_2$	0	Port A = address A0–A7
$CPAF_1$	FFH	Port A set for address
CPBF	00H	Port B set for chip-select
CPCF	111B	Port C set for chip-select
CPACOD	00H	CMOS buffers
CPBCOD	00H	CMOS buffers
CADDHLT	0	"Don't care" (not used)
CSECURITY	0	No security

Figure 23. SC80C451/ PSD3XX to 16K SRAM Applications



PSD3XX Used in Track Mode

Figure 24 illustrates a design that utilizes the track mode of operation that has been discussed but not illustrated in an application. Here, Port A passes or tracks through the multiplexed address and data of the 80196. Address and data outputs AD0–AD7 from the 80196 appear on the PSD3XX Port A pins. In this mode, the SRAM, shown in Figure 24 as U4, can be accessed either by the 80196 (used in byte mode) or by a second processor in the host system. The SRAM in the design can be used as a common resource. An example would be a system in which the host uses the memory to pass parameters to the local 80196. Table 17 gives the configuration data for an 80196/PSD301 interface to SRAM using Track Mode.

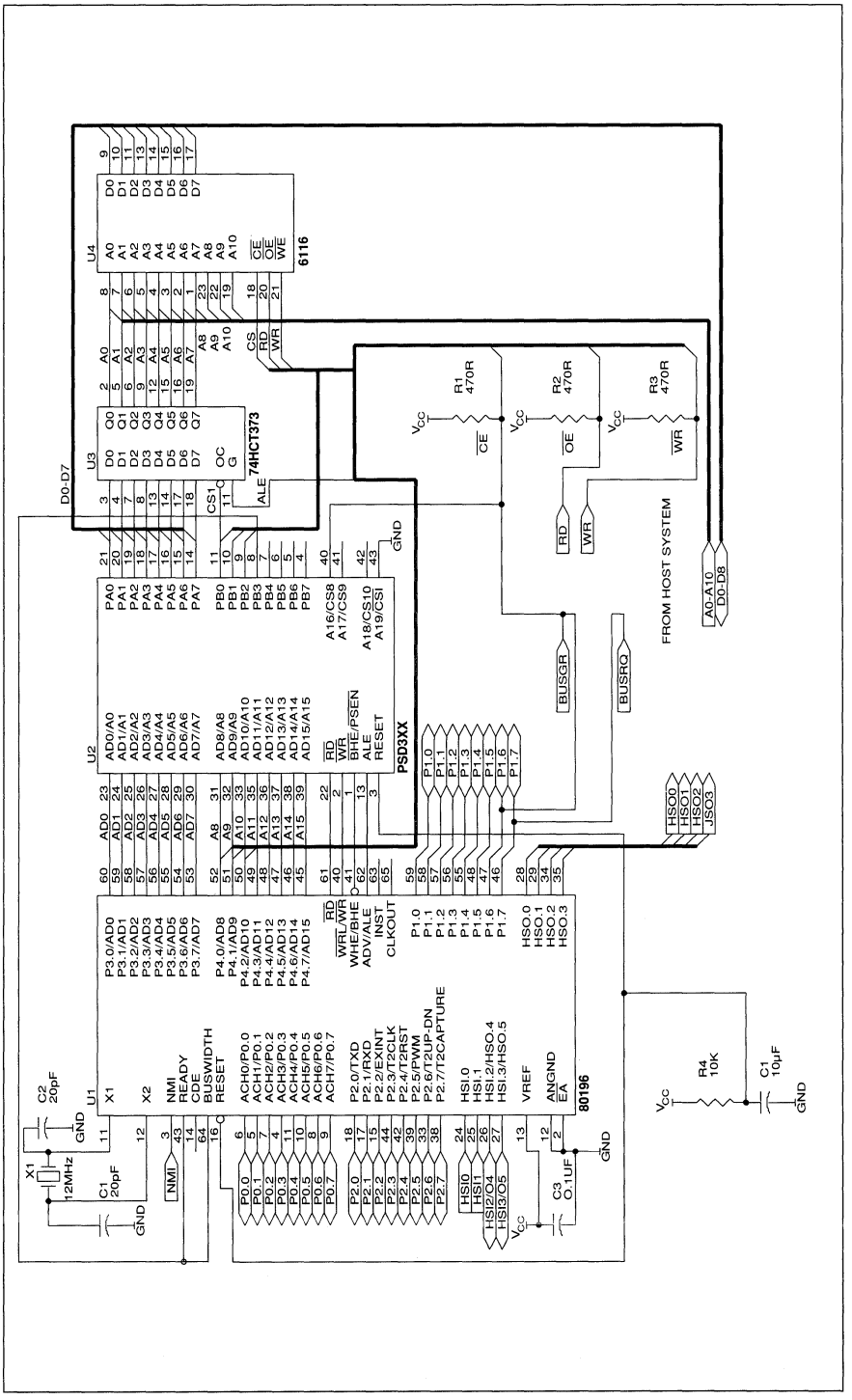
A Direct Memory Access can transfer data to the common memory via a BUSRQ/BUSGR handshake. Note that the PAD in the PSD3XX controls the three-state condition of the octal latch U3 74HCT373 enabling the host system to control SRAM addresses A0–A7. Port A of the PSD3XX is also put into a three-state condition during host-to-SRAM activity. In the design given in Figure 24, Port B outputs PB0, PB1, and PB2 are used to control the SRAM inputs $\overline{CE}$, $\overline{OE}$, and $\overline{WR}$ respectively. Also, A8, A9, and A10 are fed through the PAD as identity functions to the open drain drivers of PB3, PB4, and PB5 respectively. There is no track-through feature for these address lines; however, if they are fed through the PAD, they can drive the external memory resource as if they were tracked through.

The M80196 can operate in either byte- or word-wide mode controlled by its BUSWIDTH input. In this application, the PB6 output drives the BUSWIDTH line to switch between the byte-wide bus of the external SRAM and the word-wide interface of the PSD3XX. All Port B outputs, with the exception of PB6, are configured as open-drain. Provided the host system also has open drain/ collector drivers, both systems can access the SRAM without bus conflict. The only additional circuitry required would be the pull-up resistors.

Table 17. Intel 80196 to PSD3XX Used to Access External SRAM in Track Mode

Configuration	Bits	Function
CDATA	1	16-bit data bus
CADDRDAT	1	Multiplexed address/data
CRRWR	0	Set $\overline{RD}$ and $\overline{WR}$ mode
CA19/$\overline{CSI}$	0	Set power-down mode
CALE	0	Active HIGH ALE
CRESET	0	Active LOW RESET
$\overline{COMB}$/SEP	0	Separate data/program memory
CPAF2	1	Address/data (Track Mode)
CPAF1	XXH	"Don't care" in Track Mode
CPBF	00H	Port B set for chip-select outputs
CPCF	111B	Port C set for logic outputs
CPACOD	00H	CMOS buffers
CPBCOD	FFH	Open drain buffers
CADDHLT	X	Latched A16–A19 "don't care"
CSECURITY	0	No security

Figure 24. Intel 80196/ PSD3XX Track Mode to External SRAM

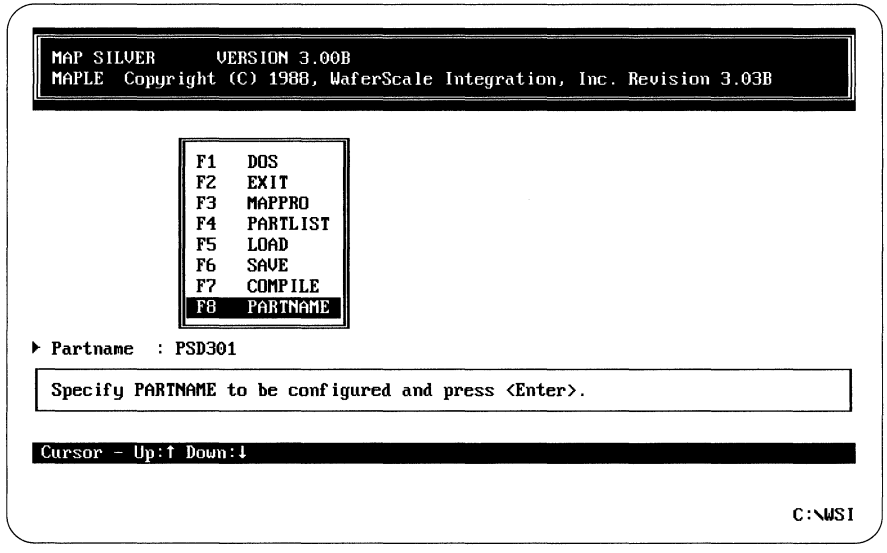


Chapter 3

The support software for both PSD3XX family and MAP168 memory-mapped peripheral devices is designed to run on IBM PC XT/AT or 100% compatible systems. It is menu-driven and very user-friendly. In many cases it has the capability of preventing the user from creating invalid configurations. For example, in a non-multiplexed system with a 16-bit data bus, Ports A and B are used for data I/O. The software recognizes this and prevents the user from inadvertently programming Ports A and B as regular ports.

When running in the IBM PC environment, the PSD development software creates the menu shown in Figure 25. Initially, the designer selects the part type with the user key F8 or moves the screen cursor to PARTNAME. In the example shown, the selection for the part type is PSD301.

Figure 25. MAPLE Main Menu



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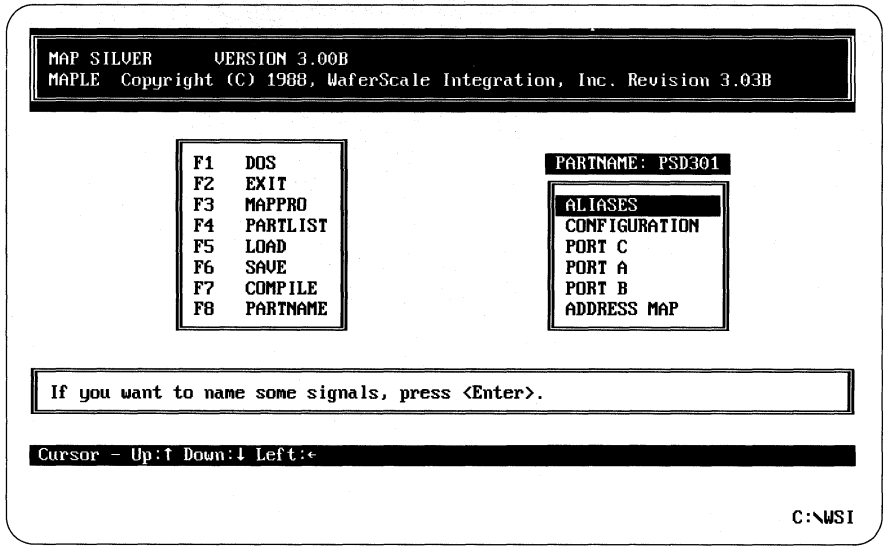
The menu listed to the left of Figure 25 links the function keys and their association. F1 suspends the MAPLE software to DOS for file editing or updating. F2 exits the program and returns the user to the DOS environment. F3 selects the programmer option so the user can program the compiled object file into the PSD301 device provided a programmer is connected to the system. The LOAD selection (F5), loads an existing program into the MAPLE environment for editing and compiling. F6 saves that program under a user-defined name. F7 compiles the user-generated file into an object file that can be transferred to the programmer. F8 provides part type selection, either PSD301 or MAP168.

Figure 26 illustrates a second menu to the right of the main menu. The list shows ALIASES, CONFIGURATION, PORT C, PORT A, PORT B, and ADDRESS MAP. The designer selects each choice, starting from ALIASES, and moves down through the list configuring each option.

Figure 26. MAPLE Menu with PARTNAME Submenu



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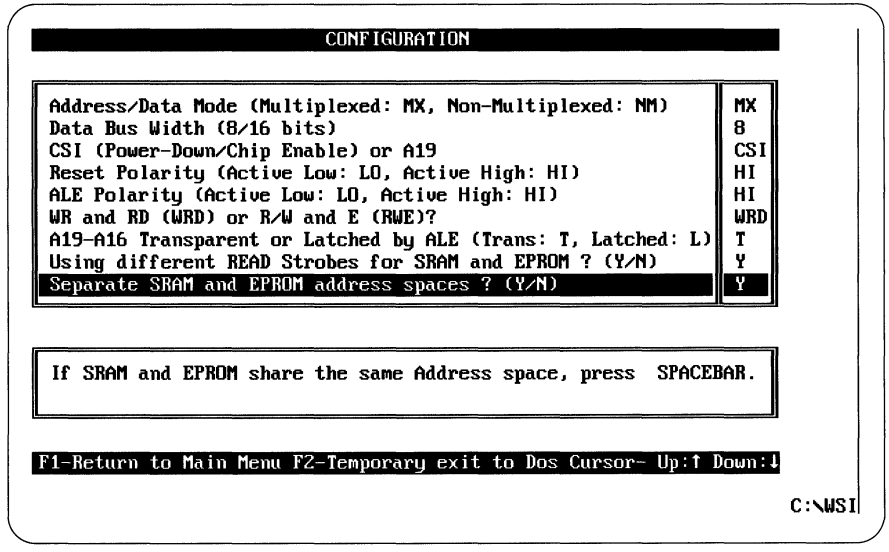
ALIASES Menu

The ALIASES selection lets the user individually define the port pins with user-relevant names. The circuit diagram shown in Figure 13 uses an M68008 processor, with BERR and DTACK signals coming from the PAD, as well as the remaining CS0, CS5 chip-select outputs.

Figure 27. CONFIGURATION Menu

Figure 27 gives the CONFIGURATION menu. In this case, the PSD301 has been configured for the system shown in Figure 10: interfacing to an 80C31; the 8-bit data/address bus is multiplexed. The chip-select input is chosen over the A19 input. The RESET and ALE polarity is set as active HIGH with $\overline{RD}$ and $\overline{WR}$ control inputs enabled. The inputs A16–A19 are transparent and separate strobes are enabled for SRAM and EPROM. This feature activates the $\overline{PSEN}$ input. In this configuration it is possible for the SRAM and EPROM to share the same address space. After the device is configured, Ports A, B, and C can be set up. If the main menu is invoked by selecting F1 (Figure 28), Port C can be selected as shown in Figure 26. Here, the individual selection of $\overline{CS}$/Ai configures the three pins as outputs.



2402 27

Figure 28. Port C Configuration Menu

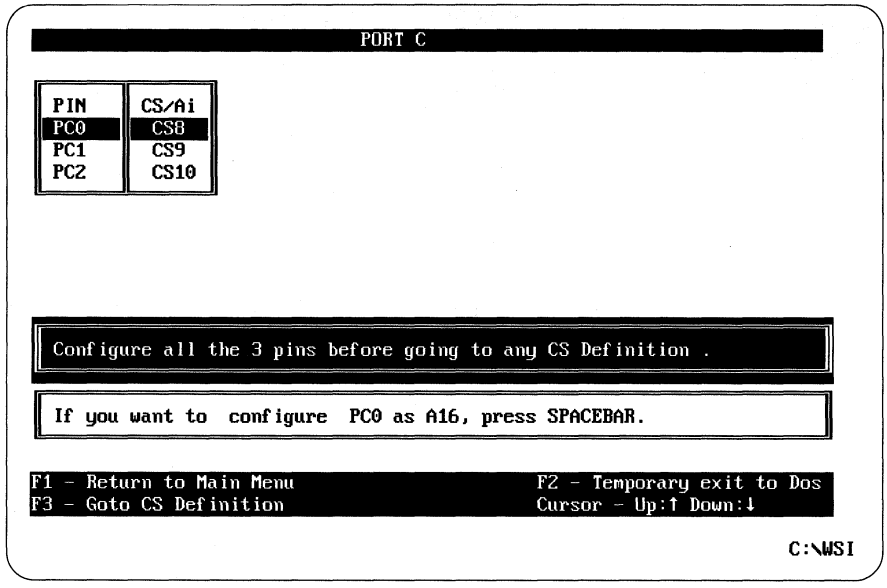


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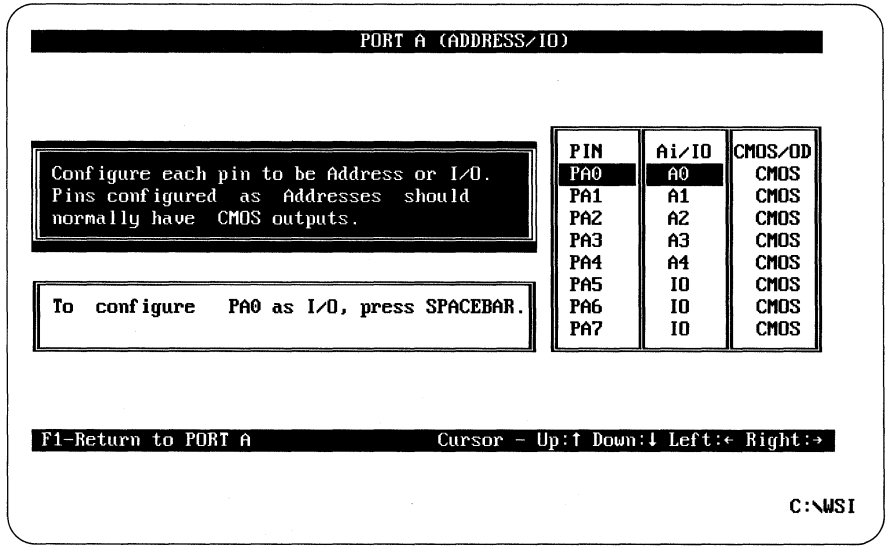
Figure 29. Port A Configuration Menu, Part 1.

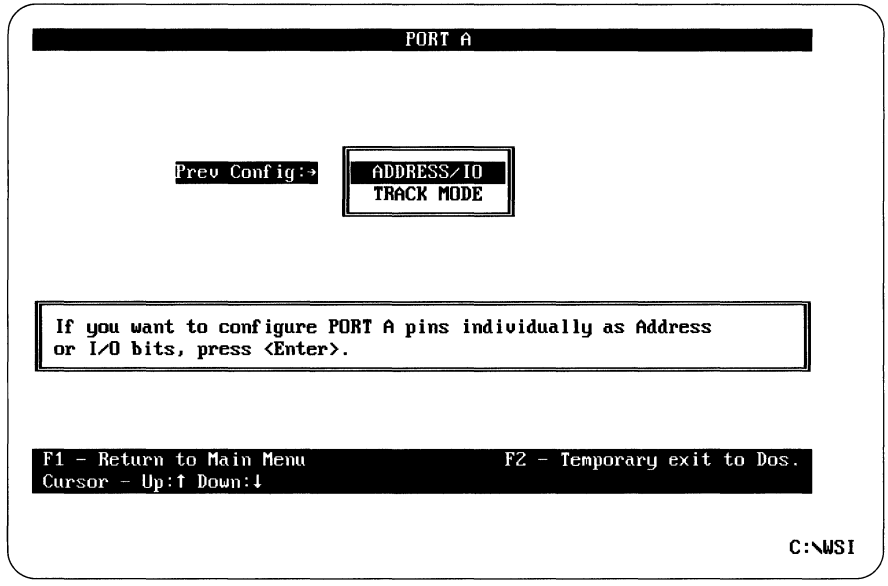
Figure 29 shows the configuration of Port A. This could be applied to the example shown in Figure 21 which shows the PSD301 interfacing to an M68230. Port A passes the PSD301's internally latched address lines A0–A4 directly to the M68230. PA5–PA7 are configured as port outputs and can be used as general I/Os.



2402 29

Figure 30. Port A Configuration Menu, Part 2.

Port A can be programmed to be either address I/O or track mode, as illustrated in Figure 30. Track mode is selected if the designer wants to program the device as shown in Figure 24.



2402 30

Figure 31. Port B Configuration Menu

Figure 31 gives the configuration of Port B. This is similar to the configuration pattern for the M68008 shown in Figure 13. Here, $\overline{CS6}$ and $\overline{CS7}$ have been programmed as open-drain outputs connected to the microprocessor's $\overline{DTACK}$ and $\overline{BERR}$, respectively.

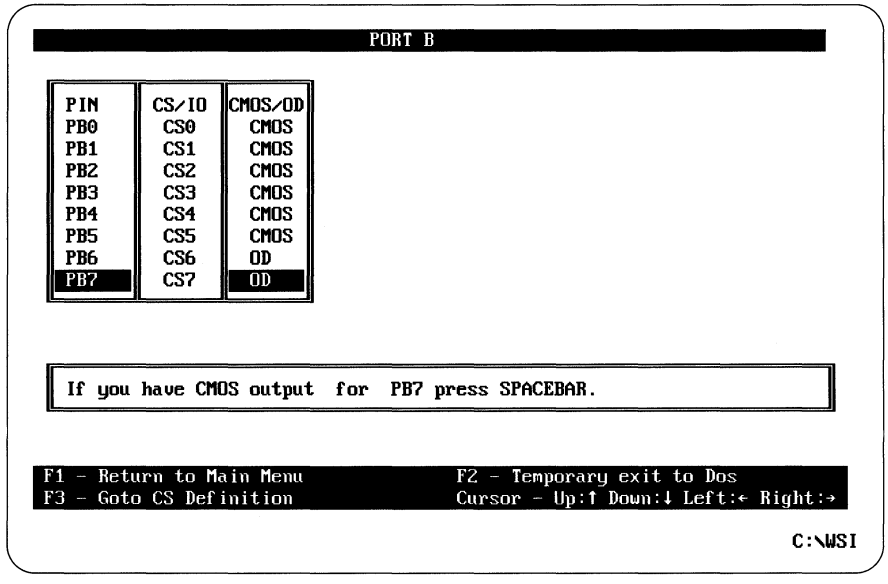


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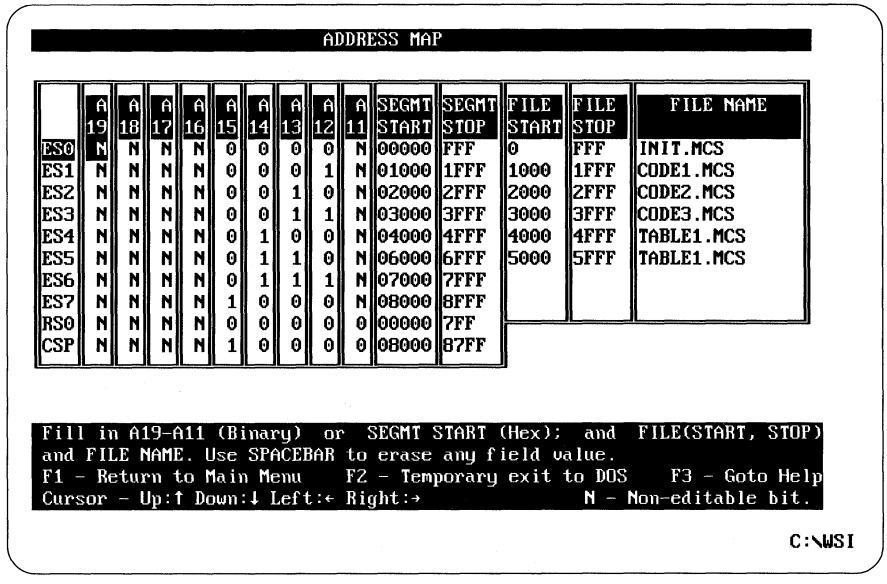
Figure 32. ADDRESS MAP Menu

Figure 32 shows the ADDRESS MAP menu. The designer can enter a binary code for the address range of the various select lines; ES0–ES7, RS0, and CSP, being the EPROM, SRAM, and PERIPHERAL assignments, respectively. A space for individual hexadecimal files is reserved under the FILENAME section. The Intel MCS files are listed as they would be compiled and programmed into the device.



	A19	A18	A17	A16	A15	A14	A13	A12	A11	SEGMT START	SEGMT STOP	FILE START	FILE STOP	FILE NAME
ES0	N	N	N	N	0	0	0	0	N	00000	FFF	0	FFF	INIT.MCS
ES1	N	N	N	N	0	0	0	1	N	01000	1FFF	1000	1FFF	CODE1.MCS
ES2	N	N	N	N	0	0	1	0	N	02000	2FFF	2000	2FFF	CODE2.MCS
ES3	N	N	N	N	0	0	1	1	N	03000	3FFF	3000	3FFF	CODE3.MCS
ES4	N	N	N	N	0	1	0	0	N	04000	4FFF	4000	4FFF	TABLE1.MCS
ES5	N	N	N	N	0	1	1	0	N	06000	6FFF	5000	5FFF	TABLE1.MCS
ES6	N	N	N	N	0	1	1	1	N	07000	7FFF			
ES7	N	N	N	N	1	0	0	0	N	08000	8FFF			
RS0	N	N	N	N	0	0	0	0	0	00000	7FF			
CSP	N	N	N	N	1	0	0	0	0	08000	87FF			

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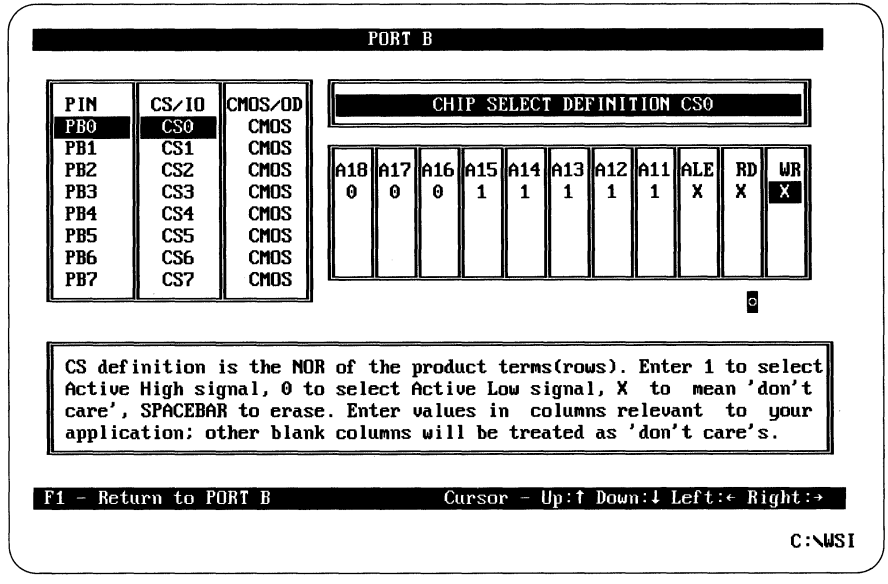
After configuration has been established, the user can return to the main menu and select the COMPILE option. The configuration is compiled and converted to a JEDEC array program map.

When successfully finished, the designer can select the MAPPRO option (see Figure 25), and when a WSI MAGICPRO™ programmer is available in the PC system, finalize the design by programming a PSD301.

The Address Map for Port B can be configured as shown in Figure 33. Per Figure 31, depress function key F3 to invoke the chip select definition. The entries can be made for logic HIGH, LOW, or "don't care" conditions.

Figure 33. Port B Configuration Menu with Address Map



2402 31

Summary

The PSD3XX microcontroller peripheral with memory, supported with low-cost software and programming capability form WSI, greatly simplifies the overall design of microcontroller based systems. The key advantage is the extensive condensing of glue logic, latches, ports, and discrete memory elements into a single-device, enhancing the reliability of the final product. Applications for the device extend to practically any area that uses microcontrollers or microprocessors, from modems and vending machines to disc controllers and high-end processor systems.

Programmable Peripheral

Application Note 013

The PSD301 Streamlines a Microcontroller-based Smart Transmitter Design

By Seyamak Keyghobad – Bailey Controls, and Karen Spesard – WSI

Abstract

A smart transmitter design is described which takes advantage of the integration capabilities and flexibility of WSI's PSD301 microcontroller peripheral. The following discussion illustrates how the PSD301, in effect, was responsible for eliminating an extra 2.5 inch diameter board in a system where real estate is at a premium by reducing the number of components from 12 down to 5.

Introduction

Designers of systems using microcontrollers and microprocessors often face the problem of how to integrate peripheral logic and memory functions into their designs without using many discrete chips and large areas of board space. For example, when external EPROM and SRAMs are configured into systems with ROMless microcontrollers, general I/O ports are typically sacrificed for address, data input/output, and control functions. When these I/O ports are depleted, the total chip count of the system is increased by requiring the use of additional external ports and steering logic. Designers, who have limited board space, such as found in the disk drive, modem, cellular phone, industrial/process control, and automotive industries, find this a critical problem.

The PSD301 programmable peripheral device from WSI solves this problem by integrating all SRAM, EPROM, programmable decoding and configurable I/O port functions needed in 8 or 16-bit microcontroller designs into a single-chip user-configurable solution. This is illustrated in the following industrial control application where the PSD301 eliminates seven chips and saves the designer from needing another board in the system.

The Design Application

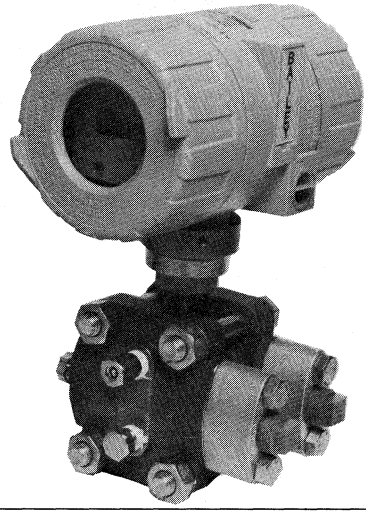
The smart transmitter, shown in Figure 1, was developed by Bailey Controls, a manufacturer of process control instruments, to support a popular field bus protocol. One of its functions in this sensor application is to measure pressure, differential pressure, and flow rates through pipes in industrial environments such as chemical plants, oil refineries, or utility plants. A host system monitors the transmitter via a process control network.

The completed transmitter design consists of three main boards. The first board includes the power supply and communications hardware to provide power to the rest of the system and feedback to the process control network. It consists of communications transformers and line drivers/receivers.

The second board is the digital microcontroller board and contains the 68HC11 microcontroller as well as the PSD301 programmable peripheral, a PLD, UART, and LCD display. Its function is to communicate and receive the inputs from the third board, process the data, and display the appropriate results to the LCD.

The third board or input board is mostly analog. It receives inputs from string gauge sensors which use a bridge circuit for measuring pressure using a diaphragm. The input board then converts the signals so the microcontroller can read them.

Figure 1. "Smart" Transmitter from Bailey Controls



▲ Pressure/Flow

Design Considerations

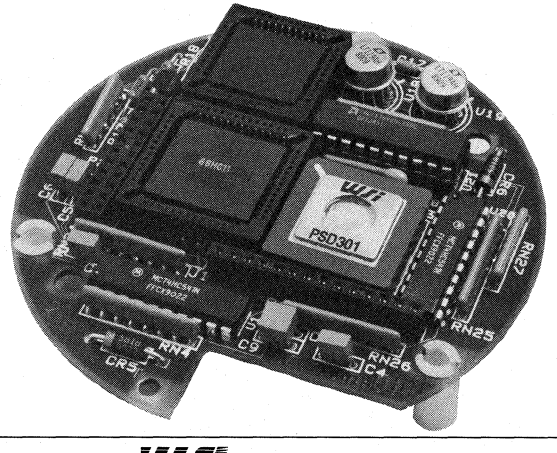
The smart transmitter system is rather small. Its case is only 2.5 inches in diameter and thus requires boards that fit this small form factor as shown in Figure 2. Not surprisingly, the major design consideration during development was board space. This was especially true for the microcontroller/digital board where real estate is at a very high premium.

One of the problems was that there were already requirements for the 68HC11 microcontroller, a 256K EPROM, 16K SRAM, a PLD, TTL logic, a UART, and an LCD display on the digital board. This meant extending the number of boards used beyond one unless a way could be found to integrate some of these elements.

Other important considerations, or goals actually, for the design were to reduce power consumption to less than 2.4W, improve reliability, lower design costs, and shorten the time-to-market.

To meet these objectives, Bailey Controls looked to WSI's user-configurable peripheral, the PSD301, for its integration capabilities, its flexibility, and its low power of less than 35 mA active and 90 µA typical powerdown.

Figure 2. The Bailey Smart Transmitter Board Using the WSI PSD301.

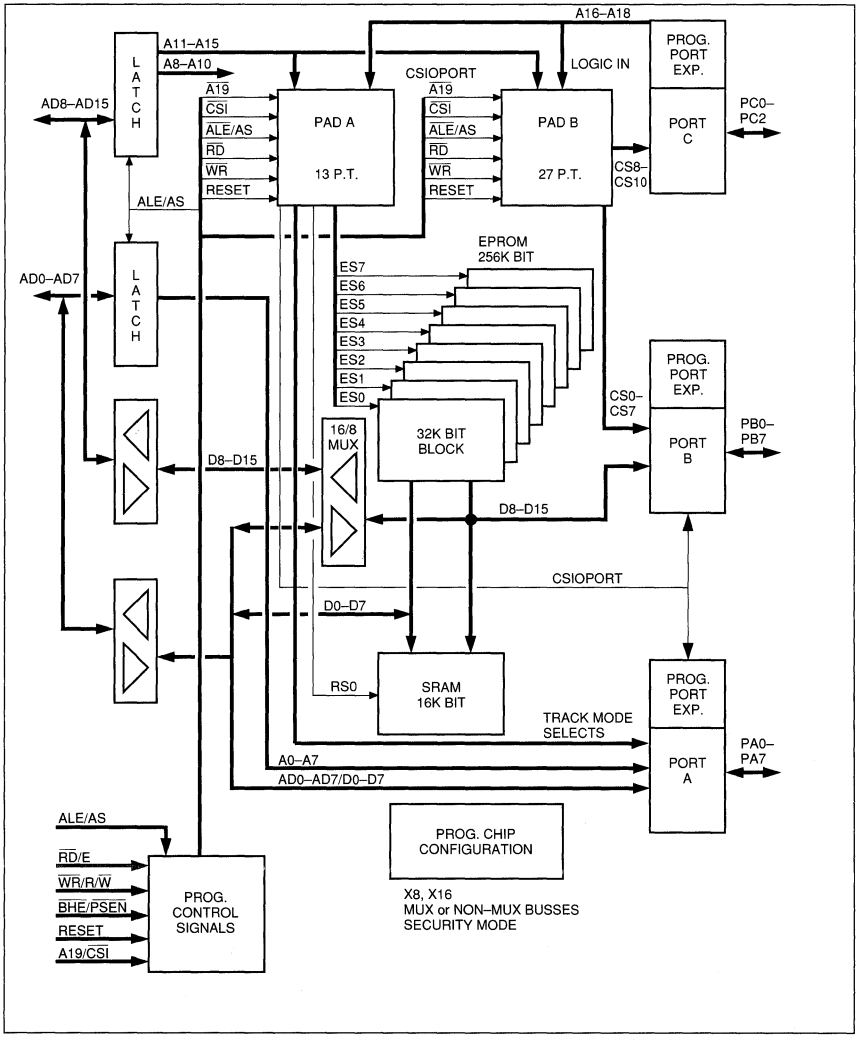


PSD301 Architecture

The PSD301 is a field programmable device that has the ability to interface to virtually any 8- or 16-bit microcontroller without the need for external glue logic. This is possible because the PSD301 combines the elements necessary for a complete microcontroller peripheral solution, such as user-configurable logic, I/O ports, EPROM and SRAM, all into one device. The functional block diagram of the PSD301 in Figure 3 shows its main sections: the internal latches and control signals, the programmable address decoder (PAD), the memory, and the I/O ports.

The control signals and internal latches in the PSD301 were designed so interfacing to any microcontroller would be easy and require no glue logic. For instance, the PSD301 can interface directly to all multiplexed (and non-multiplexed) 8- and 16-bit microcontroller address/data buses because it has two on-chip 8-bit address latches. This means no external latches are required to interface to multiplexed buses. It also has programmable polarity on the control inputs ALE/AS and RESET, so they can be configured to be active high or active low.

Figure 3. PSD301 Architecture



PSD301 Architecture (Cont.)

The other control signals, $\overline{RD}$/E, and $\overline{WR}$/R/$\overline{W}$, are also programmable as /RD and /WR or E and R/$\overline{W}$, enabling direct interface to all Motorola- and Intel-type controllers.

The programmable array decoder (PAD) is an EPROM-based reprogrammable logic "fuse" array with 11 dedicated inputs, up to 4 general-purpose inputs, and up to 24 outputs. The PAD is used to configure the 8 EPROM blocks on 2K word boundaries and the SRAM on a 1K word boundary anywhere within a 1 Meg address space. It is also used to generate a base address for mapping ports A and B, as well as to provide mapping for the track mode. The PAD, like a traditional PLD, can generate up to eight sum-of-product outputs to extend address decoding to external peripherals or to implement logic replacement on a board.

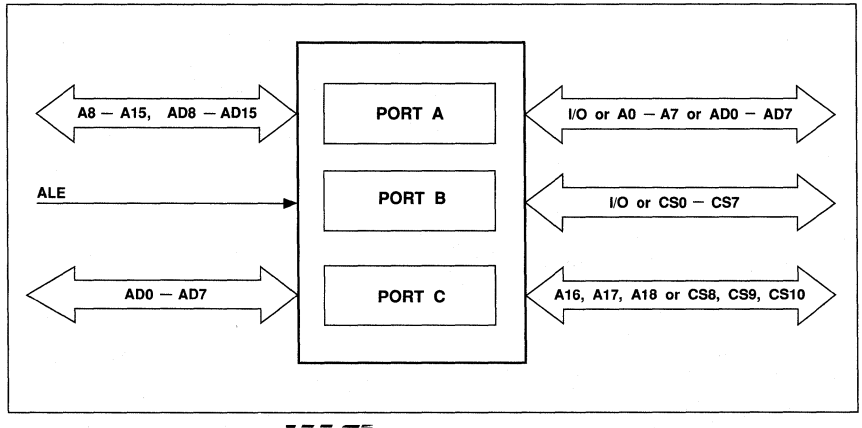
Memory in the PSD301 is provided by EPROM for program and table storage and SRAM for scratch pad storage and development and diagnostic testing. The EPROM density is 256K bits and the SRAM density is 16K bits. Both can be operated in either word-wide or byte-wide fashion, which translates to a 32K x 8 or 16K x 16 EPROM configuration and a 2K x 8 or 1K x 16 SRAM configuration. As described above, the EPROM is divided into 8 blocks (of 4K x 8 or 2K x 16), with each block typically on a 2K boundary locatable within a 1 Meg address space.

There are 3 ports on the PSD301 that are highly flexible and programmable: Ports A, B and C, illustrated in Figure 4. Port A is an 8-bit port that can be configured in a variety of ways. For example, if the PSD301 is in the multiplexed mode, port A can be configured pin-by-pin to be an I/O or a lower order latched address. Alternatively, port A can be configured in the track mode to transfer 8 bits of address and data inputs through port A. This enables the micro-controller to share external resources, such as additional SRAM, with other controllers. In either case, each port A output can be configured to be CMOS or open drain. If the PSD301 is in the non-multiplexed mode, port A becomes the lower order data for the chip.

Port B is another flexible 8-bit port. In the multiplexed mode or 8-bit non-multiplexed mode, each pin on port B can be customized to function as an I/O or a chip-select output. The chip-select signals are determined by the PAD programming and are used for general logic replacement or to extend the address decoding to external peripherals. Each pin in this mode can also be programmed to have a CMOS or an open drain output. In the 16-bit non-multiplexed mode, port B becomes the higher order data for the chip.

Port C is the third port which is available on the PSD301. It is a 3-bit port that can be programmed on a pin-by-pin basis to be chip-select outputs and/or general-purpose logic inputs or addresses to the PAD. Some uses for port C might be to extend the address range to 1 Meg, or to create finer address decoding resolution down to 256. Or, one might use port C to help create a simple state machine.

Figure 4. PSD301 Multiplexed Address/Data Configuration



Simple Interfaces to the PSD301.

One of the overwhelming advantages of the PSD301 is its ability to interface to virtually any microcontroller without any glue logic, while providing additional I/O ports and memory. This is accomplished by configuring or programming the part to function in an operational mode geared for a specific application.

For instance, there are 45 configuration bits on the PSD301 that have to be programmed in addition to the EPROM prior to usage. These configuration bits are determined during development by the designer using the WSI MAPLE software package. After the configuration bits are determined, the EPROM code and configuration data can be merged during compilation and the part subsequently programmed.

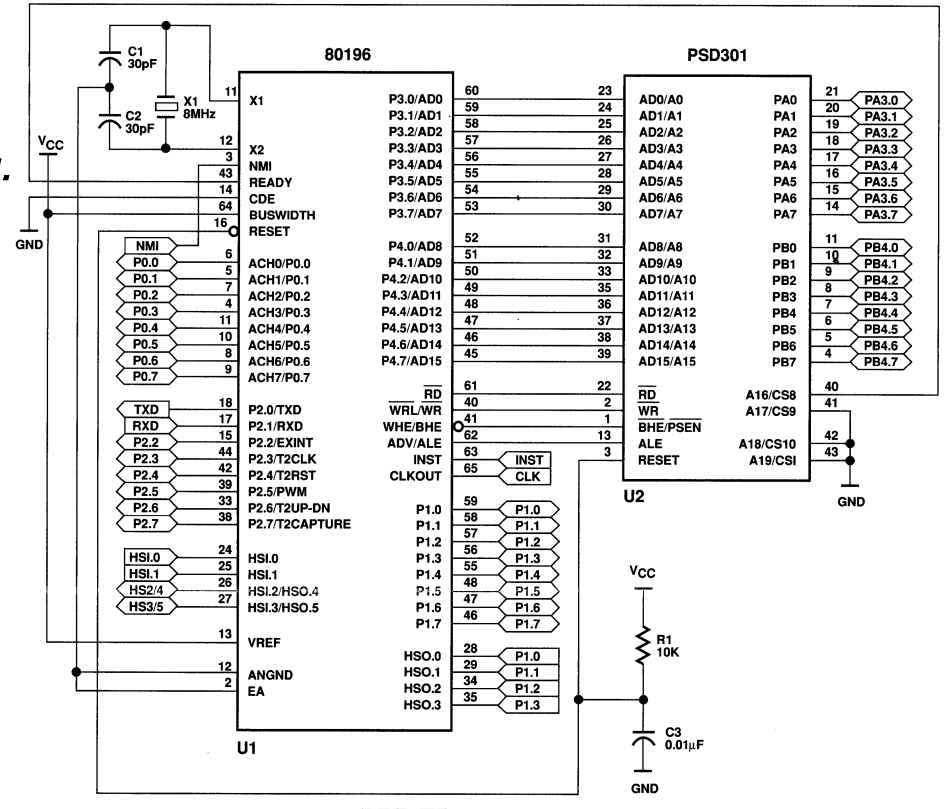
Interfacing the PSD301 to different microcontrollers is accommodated by the configuration bits discussed above. To illustrate how this works, two examples are provided.

The first example is with the 80C196 microcontroller. This 16-bit microcontroller from Intel interfaces directly to the PSD301, providing it with additional off-chip program store EPROM and data store SRAM, as well as the flexibility that comes with three additional I/O ports. As illustrated in Figure 5, the 80C196's 16-bit multiplexed address/data bus and control signals ($\overline{RD}$,$\overline{WR}$, BHE, ALE, RESET) connect directly to the PSD301. This is achieved with the PSD301 in the following configuration:

- ❑ 16-bit data bus
- ❑ Multiplexed address/data
- ❑ $\overline{RD}$ and $\overline{WR}$ mode set
- ❑ Active HIGH ALE
- ❑ Active LOW RESET
- ❑ A16–A18 configured as output
- ❑ Combined memory mode

2

Figure 5. General Schematic Diagram of the 80C196 and PSD301.



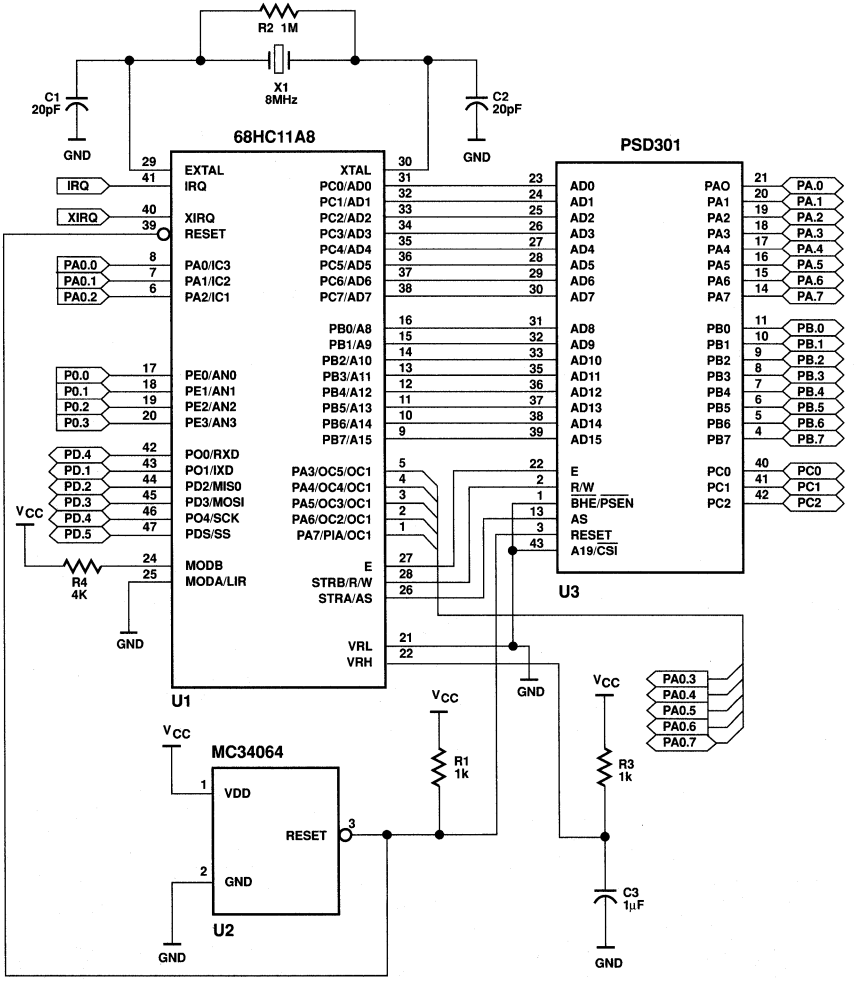
Simple Interfaces to the PSD301 (Cont.)

The other configuration options that are available, but not listed above, are application dependent and can be changed to meet the requirements of the design. For instance, on pin 43 (A19/$\overline{CSI}$), the power-down option $\overline{CSI}$ could be selected if power consumption savings is important. If it isn't and another logic input to the PAD would be helpful, A19 could be selected. And, if open-drain drivers are important on one of the ports to drive a display, for example, they also could be selected instead of CMOS drivers.

All other microcontrollers have simple interfaces to the PSD301 as well. This includes all the variations of microcontrollers in the 8-bit 68HC11 family from Motorola. For simplicity's sake, the PSD301 interface to 68HC11 versions with multiplexed address/data buses will be discussed, although the non-multiplexed versions will interface to the PSD301 in a similar manner, except in this case port A will become dedicated for 8-bit data.

Figure 6 illustrates the interconnections between the PSD301 and the 68HC11 microcontroller with multiplexed address/data buses. Again, all the address/data connections are direct, as well as the control signals (E, R/$\overline{W}$, AS, and /RESET). Because $\overline{BHE}$/$\overline{PSEN}$ is not used, this PSD301 input signal is tied HIGH.

Figure 6. General Schematic Diagram of the 68HC11and PSD301.



Simple Interfaces to the PSD301 (Cont.)

The PSD301 must be programmed using WSI's MAPLE software package in the following modes to achieve this configuration:

- ❑ 8-bit data bus
- ❑ Multiplexed address/data
- ❑ R/W and E mode set
- ❑ Active HIGH AS (ALE)
- ❑ Active LOW RESET
- ❑ Combined memory mode

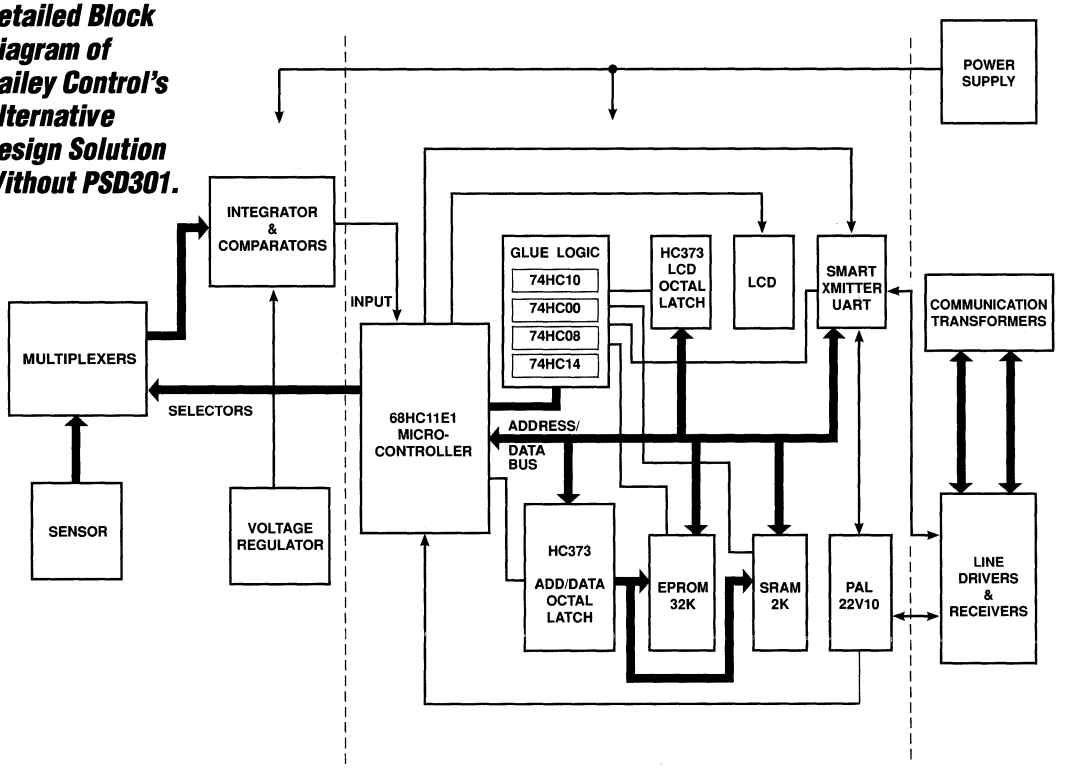
Again, other parameters on the PSD301 can be set to fit additional design requirements. These include the security bit, the port I/Os, and the PAD inputs and outputs.

The "Smart" Transmitter Design.

The microcomputer-based smart transmitter design, by Bailey Controls, requires program store 256K bits EPROM for storing algorithms and data store 16K bits SRAM for storing A/D, communication and LCD routines. It also requires two octal latches, a PLD, and a variety of glue logic to interface to its 68HC11 microcontroller, UART, and LCD display. This is illustrated in Figure 7. Of course, with board space on the digital board being limited, another board would have been needed to accommodate these components, unless they in some way could be integrated.

2

Figure 7. Detailed Block Diagram of Bailey Control's Alternative Design Solution Without PSD301.



The "Smart" Transmitter Design (Cont.)

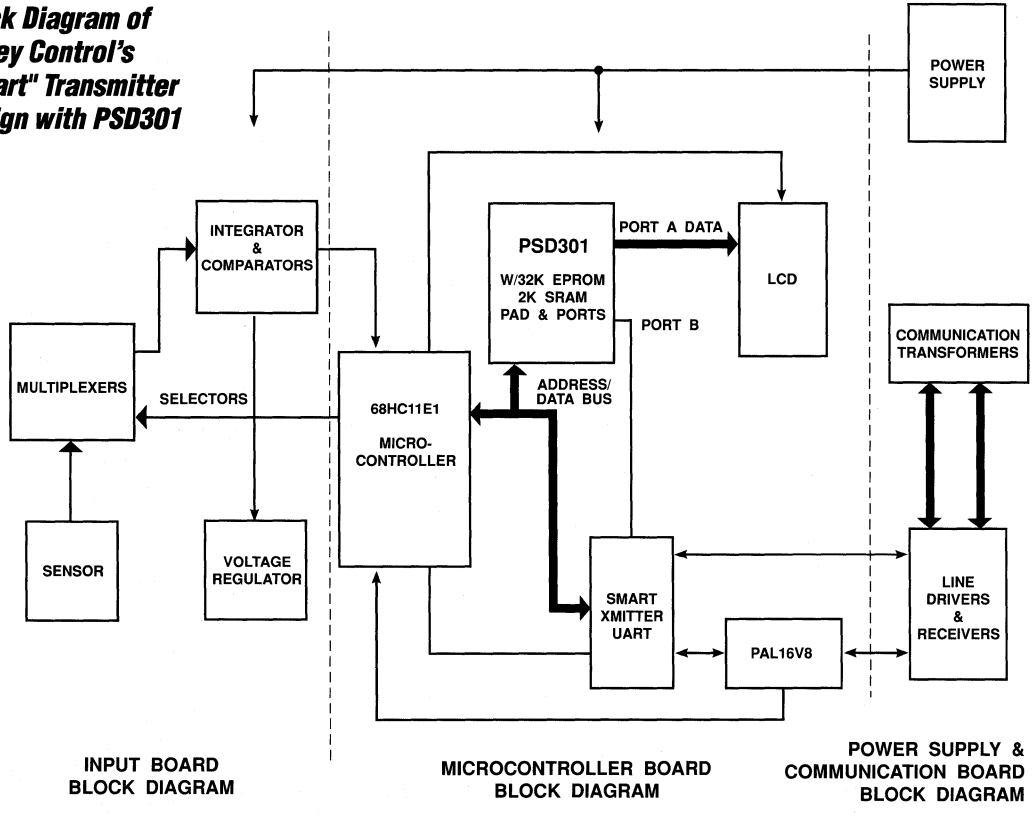
This is where the PSD301 provides exceptional value. As discussed, the PSD301 already integrates EPROM,[1] SRAM,[2] a PLD, and other glue logic all on one chip. It interfaces to the 68HC11 directly and actually integrates 8 chips from the alternative design into one, eliminating the need to add another board. The resultant architecture is illustrated in Figure 8.

Note that in the alternative design shown in Figure 7, ports typically lost when connecting the microcontroller to external memory had to be recreated externally with latches and buffers when memory was connected to the microcontroller. With the PSD301, these ports are recreated internally, eliminating the latches and buffers.

For example, to interface the PSD301 to the 24-character LCD display, each pin of port A is configured as an I/O and mapped to the byte-wide LCD data inputs. Then to write to or read from the LCD display, port A is accessed like a memory-mapped peripheral via an address offset from the base CSIOPORT defined in the PAD. Since port A is qualified by and handled through the PAD, there is no need for an external octal latch.

Other TTL logic is not required to interface to the 68HC11's control signals, memory, or peripherals either. It is all integrated in the PSD301. Thus, a smaller PLD than originally thought required in the design was used — a 16V8 instead of a 22V10 — because the PAD was able to reduce the amount of logic by creating chip selects for the UART and other logic functions.

Figure 8. Block Diagram of Bailey Control's "Smart" Transmitter Design with PSD301



PSD301 Bonuses

Besides considerably reducing board space in this smart transmitter design by reducing parts count, several other benefits of the PSD301 were also seen. These include reliability improvement, power consumption savings, inventory savings, faster time-to-market, and cost savings.

Reliability was improved because there are seven less chips required for implementation that could fail in the design. Also, by reducing chip count, 112 pins and about 100 traces were eliminated and the number of layers on the board were reduced from 8 to 4, making failures due to open or shorted pins and traces less likely to occur.

Power consumption was reduced because much faster discrete EPROM and SRAM devices with access times of ~75 ns would have been required in conjunction with glue logic for selecting different devices instead of using the PSD301, saving at least 20 mA I_{CC}. (The access time for the PSD301 memories include decoding and input address latch delays). If the power-down feature on the PSD301 were also used, power savings could be increased further. For example, in a system which is accessing the PSD301 only a quarter of the time, the power consumption could be reduced by 75% to 8 mA typical.

As an added benefit, the PSD301 helped reduce inventory significantly by obsoleting multiple chips. And, if last minute changes in the design were required, the PSD301 would be able to accomodate them without additional hardware modifications. So, purchasing line item management is made simpler and easier.

With the reprogrammable PSD301, development time was kept to a minimum by easily accommodating design iterations in both hardware and software. Changes in I/O, address mapping, bus interface, and code were simple to make. Also, debugging was made easier with the PSD301's on-chip SRAM for down-loading test programs. This all helped to shorten the design development cycle, reduce development costs, and speed up market introduction of the smart transmitter.

By using the PSD301, cost savings were realized by reducing system cost with fewer boards (or reduced board space), improving reliability, and reducing inventory levels. Savings were also attributable to lower manufacturing costs because there were fewer parts to program and place. And by getting to market faster, profits were improved significantly.

Summary

The PSD301 peripheral solved a fundamental problem often seen in that instead of getting "locked into" an inflexible multiple chip memory sub-system solution, the PSD301 was able to provide much higher integration and flexibility all at the same time. Clearly, using the PSD301 was the better choice for the smart transmitter design.

Notes

1. If more EPROM was needed, the PSD302/312 w/512K bits EPROM and the PSD303/313 w/1024K bits EPROM are available in the same pinout and packages (please call your local WSI sales representative for availability). Or, multiple PSD301s can be cascaded together with the added benefit of increased functionality and I/O's.

2. If more SRAM is needed, it can be added externally without requiring any additional glue logic. See WSI Application Note 011. Note that many engineers have 8K x 8 SRAM in their systems now – not because they need it, but because 2K x 8 SRAMs are not as readily available.

Appendix 1. PSD301 Configuration

WSi PSD301 Configuration Save File for Smart Transmitter Design

ALIASES

```
CS0 = ASICCS
```

```
********************************************************************************
                    GLOBAL CONFIGURATION

Address/Data Mode:                                      MX
Data Bus Size:                                          8
CSI/A19:                                                CSI
Reset Polarity:                                         LO
ALE Polarity:                                           HI
WRD/RWE:                                                RWE
A16-A19 Transparent or Latched by ALE:                  T
Using different READ strobes for SRAM and EPROM:        N

********************************************************************************
             PORT A CONFIGURATION (Address/IO)

 Bit No.      Ai/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          IO          CMOS

********************************************************************************
             PORT B CONFIGURATION

 Bit No.      CS/IO.      CMOS/OD.
    0          CS0          CMOS
    1          CS1          CMOS
    2          CS2          CMOS
    3          CS3          CMOS
    4          CS4          CMOS
    5          CS5          CMOS
    6          CS6          CMOS
    7          CS7          CMOS

         CHIP SELECT EQUATIONS

/ASICCS = /A15 * A14 * /A13 * /A12 *  E

/CS1 = /A15 * A14 * /A13 * A12 *  E

/CS2 = /A15 * A14 * A13 * /A12 *  E

/CS3 = /A15 * A14 * A13 * A12 *  E

/CS4 = /A15 * /A14 * /A13 * /A12 * /A11 *  E
   + /A15 * /A14 * /A13 * /A12 * /A11 * / R/W

/CS5 = /A15 * /A14 * /A13 * /A12 * A11 *  E
   + /A15 * /A14 * /A13 * /A12 * A11 * / R/W

/CS6 = /A15 * /A14 * /A13 * A12 * /A11 *  E
   + /A15 * /A14 * /A13 * A12 * /A11 * / R/W

/CS7 = /A15 * /A14 * /A13 * A12 * A11 *  E
   + /A15 * /A14 * /A13 * A12 * A11 * / R/W
```

Appendix 1. PSD301 Configuration. (Cont.)

```
*******************************************************************************
              PORT C CONFIGURATION

 Bit No.      CS/Ai.
    0          CS8
    1          CS9
    2          CS10


         CHIP SELECT EQUATIONS

/CS8 = /A15 * /A14 * A13 * /A12 * /A11 *  R/W

/CS9 = /A15 * /A14 * A13 * /A12 * A11 *  R/W

/CS10 = /A15 * /A14 * A13 * A12 * /A11 *  R/W

*******************************************************************************
              ADDRESS  MAP

      A  A  A  A  A  A  A  A  A SEGMT  SEGMT   EPROM   EPROM   File Name
     19 18 17 16 15 14 13 12 11 STRT   STOP    START    STOP
ES0   N  N  N  N  1  0  0  0  N  8000    8FFF    8000    8fff    BCN2.0
ES1   N  N  N  N  1  0  0  1  N  9000    9FFF    9000    9fff    BCN2.0
ES2   N  N  N  N  1  0  1  0  N  A000    AFFF    a000    afff    BCN2.0
ES3   N  N  N  N  1  0  1  1  N  B000    BFFF    b000    bfff    BCN2.0
ES4   N  N  N  N  1  1  0  0  N  C000    CFFF    c000    cfff    BCN2.0
ES5   N  N  N  N  1  1  0  1  N  D000    DFFF    d000    dfff    BCN2.0
ES6   N  N  N  N  1  1  1  0  N  E000    EFFF    e000    efff    BCN2.0
ES7   N  N  N  N  1  1  1  1  N  F000    FFFF    f000    ffff    BCN2.0
RS0   N  N  N  N  0  1  1  0  0  6000    67FF
CSP   N  N  N  N  0  0  1  1  0  3000    37FF


*******************************  END  ****************************************
CDATA        = 0                          CPAF1 [0] = 0
CADDRDAT     = 1                          CPAF1 [1] = 0
CRRWR        = 1                          CPAF1 [2] = 0
CA19/(/CSI)  = 0                          CPAF1 [3] = 0
CALE         = 0                          CPAF1 [4] = 0
CRESET       = 0                          CPAF1 [5] = 0
COMB/SEP     = 0                          CPAF1 [6] = 0
CADDHLT      = 0                          CPAF1 [7] = 0

CPAF2        = 0

CPACOD [0] = 0                            CPBCOD [0] = 0
CPACOD [1] = 0                            CPBCOD [1] = 0
CPACOD [2] = 0                            CPBCOD [2] = 0
CPACOD [3] = 0                            CPBCOD [3] = 0
CPACOD [4] = 0                            CPBCOD [4] = 0
CPACOD [5] = 0                            CPBCOD [5] = 0
CPACOD [6] = 0                            CPBCOD [6] = 0
CPACOD [7] = 0                            CPBCOD [7] = 0

CPBF [0] = 0                              CPCF [0] = 1
CPBF [1] = 0                              CPCF [1] = 1
CPBF [2] = 0                              CPCF [2] = 1
CPBF [3] = 0
CPBF [4] = 0
CPBF [5] = 0
CPBF [6] = 0
CPBF [7] = 0
```

Programmable Peripheral Application Note 014

Using the PSD3XX PAD for System Logic Replacement

By Jeff Miller

Introduction

In 1990, WSI introduced the Programmable System Device (PSD): the first device in the world integrating UVEPROM, SRAM and programmable logic on a single chip of silicon. The highly-successful PSD301 was the first device in the PSD family and is currently used in applications ranging from fluid analyzers to high performance computers. The PSD device, by combining most of the peripheral functionality required by a typical microcontroller unit into one package, has enabled designers to greatly reduce part count, power and board space which has translated into significant cost savings.

Even if the PSD3XX family were simply a collection of EPROM and SRAM with an on-chip decoder, it would be capable of adding significant value to the system into which it were designed. However, the PSD3XX family is much more than just a combination of memory devices. The on-chip PLD may be used for many useful purposes in addition to providing the address decode capability. The purpose of this note is to demonstrate, in detail, the full capability of the PAD section of the PSD3XX family. A basic, though not extensive, knowledge of the PSD 3XX family and the Maple programming software is assumed by this note. Please consult Application Note 011 and/or the appropriate PSD3XX family data sheet for this general knowledge.

PAD Architecture

The Programmable Array Decoder (PAD) contained in the PSD3XX family is a standard PLD array designed to provide all of the internal memory and I/O device chip selects as well as an external logic replacement capability. It has 14 inputs, 24 outputs and 40 product terms with which to perform these functions. See Figure 1 for an illustration of the PAD.

The PAD's 14 inputs are as follows:

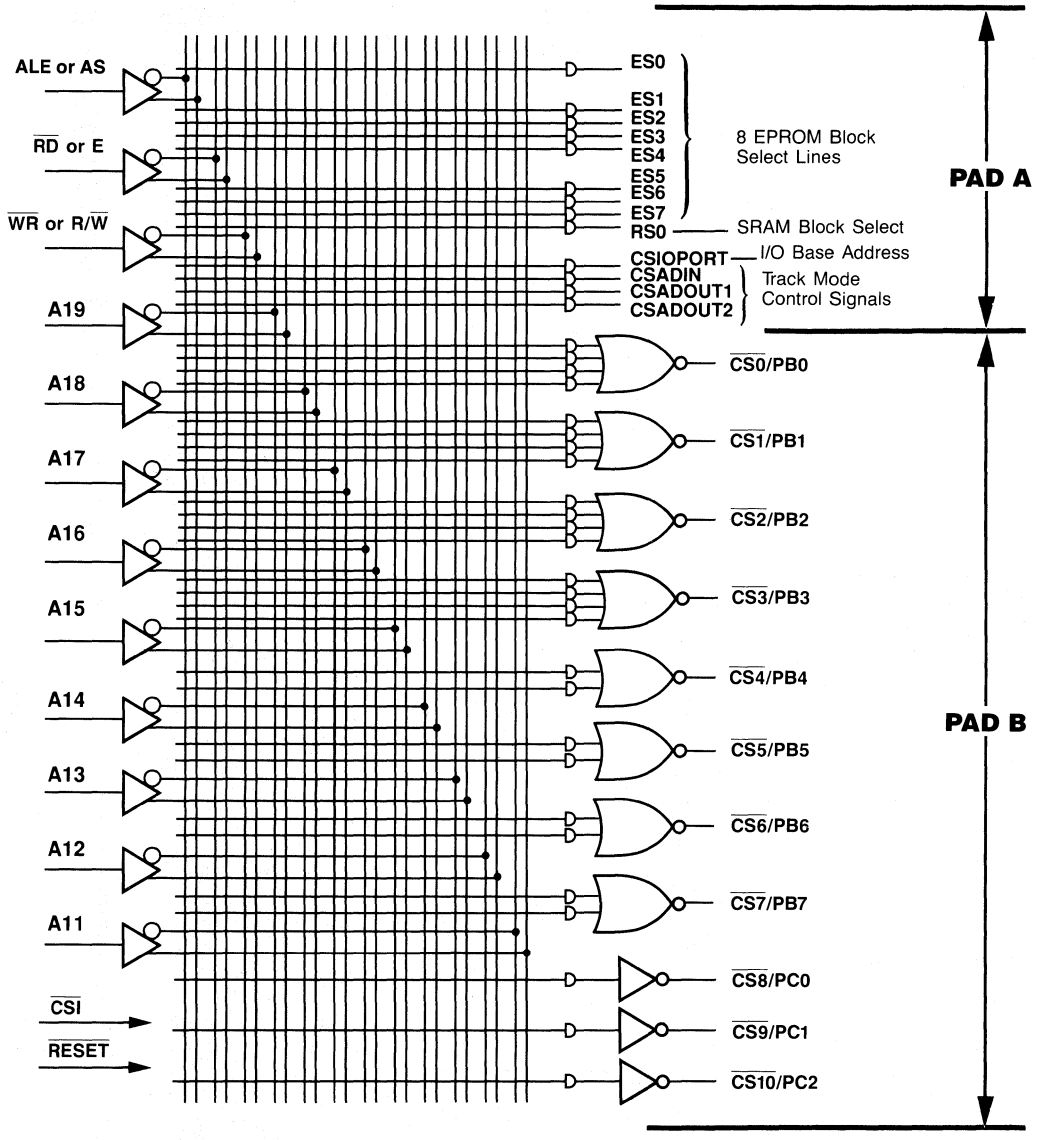
- A11 – A19
- ALE or AS
- $\overline{RD}$ or E
- $\overline{WR}$ or R/$\overline{W}$

The A11 – A19 pins are labeled as address inputs, however, they do not have to be. A11 - A15 are generally sourced by the microcontroller or microprocessor that is connected to the PSD device. If the controller generates more than 16 bits of address, the A16 – A19 inputs may be used to connect the high order address bits for a full 1 MByte of address space. If the controller does not require this much address space, A16 – A19 may be used for other purposes, like general I/O or logic inputs.

A19 is multiplexed with the $\overline{CSI}$ signal, which is used to place the PSD device in a low power mode when the system requires it. When configured as $\overline{CSI}$, the A19 pin may not be used for any other purpose except the power down mode. In this mode, the $\overline{CSI}$ signal is used by the PAD only to disable it, causing it to expend less power. When configured as A19, this signal may be used as a general purpose input to the PAD from the external system. This capability will be described in more detail later in this note. A16 – A18, when not necessary for address expansion, may also be used as general purpose inputs to the PAD. Thus, a total of four of the 14 PAD inputs may be general purpose, allowing the replacement of external logic by the PSD device. These inputs may be combined with the other PAD inputs to form complex equations involving addresses, strobes and external signals.

When attempting to visualize the full capability of the PAD outputs, it is most clear when it is broken into two sections, labeled in Figure 1 as PAD A and PAD B. PAD A is responsible for providing all of the internal chip selects for the EPROM, SRAM and I/O ports and the track mode control signals, and PAD B is responsible for the external logic replacement function.

Figure 1. PAD Architecture



PAD A

Thirteen of the 24 PAD outputs and thirteen of the 40 product terms are dedicated to PAD A. PAD A should be considered the internal address decoder, used to select the various on-chip memories and I/O devices according to the memory map programmed by the user. Each output has a single product term, allowing a particular resource to be allocated a single contiguous range of addresses which will be used to access it. All of the PAD inputs are available for generation of the PAD A outputs, allowing the designer to select internal resources using any combination of address, strobe and external signals.

PAD A (Cont.)

The PAD A outputs are as follows:

- ES0 – ES7
- RS0
- CSIOPORT
- CSADIN
- CSADOUT1
- CSADOUT2

ES0 – ES7 are used to select the internal EPROM resources. Using the PSD301 as an example, there are eight select lines with which to access 32 KBytes of EPROM. Thus, each select line can enable a block of 4 KBytes of EPROM configured as 4K x 8 or 2K x 16. Each block must be contiguous, but the blocks may be placed anywhere within the address space of the microcontroller.

RS0 is used to select the SRAM resource. This single signal accesses a single 2 KByte block of SRAM which may be configured as 2K x 8 or 1K x 16. Again, this block must be contiguous but may be placed anywhere in the address map.

CSIOPORT is the signal which defines the base address of the on-chip I/O ports and control registers. The I/O ports and control registers occupy a 2K block of addresses which, like the memories, must be contiguous but may be located anywhere in the address space of the microcontroller. Once configured in the address map, CSIOPORT defines the base address of these ports and registers. An offset is added to the base address to individually access the registers. Table 1 below lists the offset values for these registers.

CSADIN, CSADOUT1 and CSADOUT2 are used to control the Track Mode operation. The Track Mode is an available option for Port A to allow it to "track" the Address/Data bus inputs to the PSD device from the microcontroller. This provides the capability to connect the PSD device, and therefore the microcontroller, to one or more shared resources. These resources may be memory or other devices which must be accessed by more than one microprocessor or microcontroller.

CSADIN is generated when the microcontroller is attempting to read data from Port A in the track mode. It is generated from one product term involving the address inputs and the $\overline{RD}$ strobe (Intel mode) or R/$\overline{W}$ and E (Motorola mode). This allows the user to configure the address range in which the data is to be read from Port A. CSADOUT1 is generated when the microprocessor is accessing a "tracked" address. It is generated from a single product term involving the address inputs and ALE. When the address generated by the microcontroller is within the block specified by the user for track mode, and the ALE is active, CSADOUT1 becomes active, transferring the address and outputting it from Port A. CSADOUT2 is generated when the microcontroller is performing a write operation to a tracked address. It also has one product term involving the address inputs and $\overline{WR}$ (Intel mode) or R/$\overline{W}$ and E (Motorola mode). When the microcontroller performs a write to the appropriate address, CSADOUT2 is generated, transferring the data and outputting it from Port A. For further details on the operation of the Track Mode, please consult Application Note 017.

Table 1. I/O Port Offset Addresses

Register Name	Byte Size Access of the I/O Port Registers Offset from the CSIOPORT
Pin Register of Port A	+ 2 (accessible during read operation only)
Direction Register of Port A	+ 4
Data Register of Port A	+ 6
Pin Register of Port B	+ 3 (accessible during read operation only)
Direction Register of Port B	+ 5
Data Register of Port B	+ 7

Example: Address Mapping With PAD A

In this example, we will choose a sample address map which is similar to those used in typical microcontroller applications. This example assumes the use of a PSD301 device with 256 Kbits of EPROM and 16 Kbits of SRAM. Figure 2 below illustrates our sample address map.

In this example, we have located the boot code and interrupt service routines beginning at address 0000 in EPROM block 0. The SRAM is located in the 2K block beginning at address 0x1000 and can be used for the stack and/or other scratchpad data. The I/O ports occupy the 2K block beginning at address 0x1800. Addresses in this range will access ports A and B and their control registers. The area from 0x2000 to 0x8FFF is unused in this example, though it could be used for external resources as will be shown later. Finally, the main program resides in the 28K block of EPROM located from address 0x9000 to 0xFFFF and is selected by ES1 – ES7.

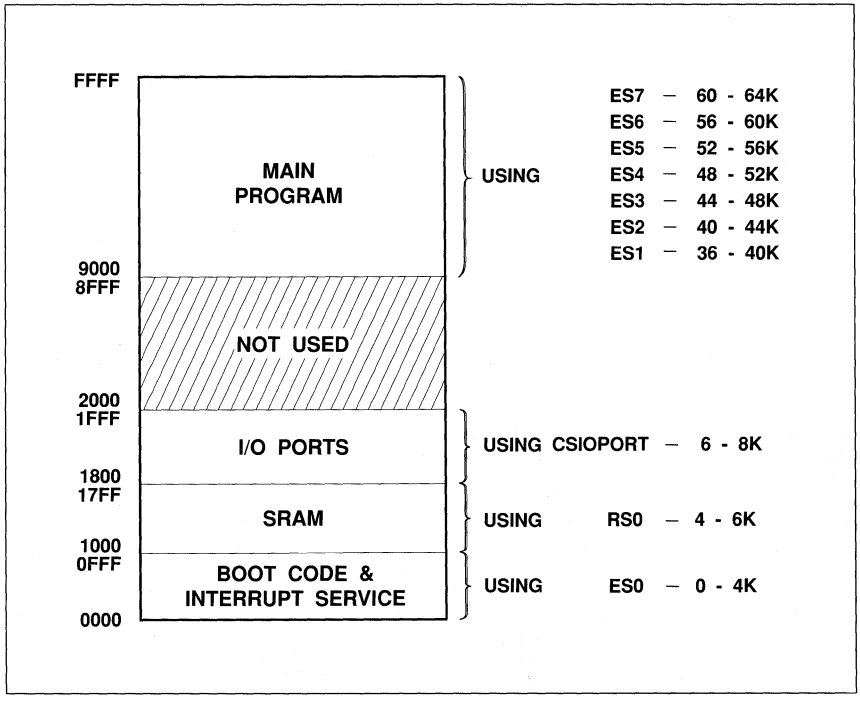
Configuring this memory map would normally require designing a decoder to generate the appropriate chip selects for each given address range. For example, assuming that a microcontroller with a 16-bit address bus is used, the chip select for EPROM bank 0 (ES0) would be generated with the following equation:

$$ES0 = /A12 \cdot /A13 \cdot /A14 \cdot /A15$$

Equations like this one would be formulated for each of the chip selects, and the entire function would probably be placed in some kind of programmable device. When the PSD device is used, PAD A replaces this programmable device. Programming PAD A to perform this function is a simple task using WSI's Maple software.

Entering the ADDRESS MAP menu in the Maple software running on a PC compatible computer, the user will see a screen similar to the one shown in Figure 3.

Figure 2. Example Memory Map



Example: Address Mapping With Pad A (Cont.)

Upon displaying this screen, the Maple software is ready for the user to enter the memory map data. This is performed quite simply by moving the cursor to the appropriate point with the arrow keys, and then entering the appropriate data. The address mapping may be entered in either of two ways. First, the user may select each address bit individually for each chip select and enter a 0 or 1 as appropriate for the equation desired. In our example, for ES0 we would enter a 0 in the columns for A12, A13, A14 and A15. The other bits are don't cares. In the other method of programming the pad, the user simply moves the cursor to the SEGMT START column and enters the desired starting address for the block. Again, using our sample memory map, the user would move to the SEGMT START column for ES0 and enter 0000. Maple then automatically programs the 0's and 1's into the address bits correctly to program a 4K block of EPROM beginning at address 0x0000. Note that all EPROM blocks must begin on 4K boundaries. Figure 3 shows the resulting address map table for our example.

The address inputs which were unused in this example (A16, A17, A18 and A19) could have been used as general purpose inputs to the PAD for specialized control of the on-chip memory and I/O resources. When this is done, the designer has complete flexibility as to the configuration of the PSD device resources and may easily absorb many system functions into the PSD device. More detail about the use of A16 – A19 will be provided later in this note.

PAD B

Eleven of the PAD outputs and 27 of the product terms are dedicated to PAD B. Where PAD A was used to control the on-chip PSD device resources, PAD B controls any off-chip resources required by the system. As with PAD A, all inputs to the PAD are available to PAD B, allowing the system designer to formulate outputs involving any combination of address, strobes and external signals. Unlike PAD A, several of the outputs of PAD B have up to four product terms each.

The outputs of PAD B are as follows:

- CS0 – 7 (Port B)
- CS8 – 10 (Port C)

The outputs from PAD B are brought to the outside world through Port B and Port C. These outputs are called chip selects, though they may be used for any function whatsoever. The port pins are configured as selected by the user when the device is programmed with the Maple output file. There are many configuration options for each port pin.

Figure 3. Maple Address Map Entry

ADDRESS MAP

	A 19	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	SEGMT START	SEGMT STOP	FILE START	FILE STOP	FILE NAME
ES0	X	X	X	X	0	0	0	0	N	0000	0FFF			
ES1	X	X	X	X	0	0	0	1	N	9000	9FFF			
ES2	X	X	X	X	1	0	1	0	N	A000	AFFF			
ES3	X	X	X	X	1	0	1	1	N	B000	BFFF			
ES4	X	X	X	X	1	1	0	0	N	C000	CFFF			
ES5	X	X	X	X	1	1	0	1	N	D000	DFFF			
ES6	X	X	X	X	1	1	1	0	N	E000	EFFF			
ES7	X	X	X	X	1	1	1	1	N	F000	FFFF			
RS0	X	X	X	X	0	0	0	1	0	1000	17FF			
CSP	X	X	X	X	0	0	0	1	1	1800	1FFF			

ALIASES:
Fill in A19 – A11 (Binary) or SEGMT START (Hex): and FILE (START, STOP) and FILE NAME, Use SPACEBAR to erase any field value.
F1 – Return to Main Menu F2 – Temporary Exit to DOS F3 – Go to Help
Cursor – UP: ↑ Down: ↓ Left Col: ← Right Col: → Right – F4 Left – F5

PAD B (Cont.)

If you require more information about port configuration, please consult application note 011. If the port outputs are configured as chip selects (outputs from the PAD), they may not be used for any other purpose. For example, the three Port C signals may be configured as chip selects (outputs) or addresses (inputs) but cannot be both. Fortunately, the flexibility of the PSD device and the Maple software allows the designer to configure each Port B and C pin individually, so that the number of outputs and inputs may be optimized for a particular design requirement. See Table 2 below for an example of this flexibility.

This sample port configuration demonstrates all of the possible uses of a particular port pin. Though only Ports B and C may be inputs or outputs to/from the PAD, Port A is included in the table for completeness. In this example, five of the port pins are configured as PAD outputs (CS) and two are configured as PAD inputs (A). The remaining port pins in this example are configured as either I/O or address outputs. Several of the CS outputs have been configured as open drain. This allows them to be connected together in a wired OR configuration to increase the number of product terms even further if desired.

Table 2. Sample Port Configuration

Pin	Configuration	CMOS/OD
PA0	Address Out	CMOS
PA1	Address Out	CMOS
PA2	Address Out	CMOS
PA3	Address Out	CMOS
PA4	I/O	CMOS
PA5	I/O	OD
PA6	I/O	OD
PA7	I/O	CMOS
PB0	$\overline{CS0}$	CMOS
PB1	$\overline{CS1}$	CMOS
PB2	$\overline{CS2}$	OD
PB3	$\overline{CS3}$	OD
PB4	I/O	CMOS
PB5	I/O	CMOS
PB6	I/O	CMOS
PB7	I/O	CMOS
PC0	A16	—
PC1	A17	—
PC2	$\overline{CS10}$	OD

Example: Generating a Logic Equation With PAD B

Assume that it is necessary to generate the following equation given the port configuration in Table 2 above. This equation is a simple OR of three product terms.

CS0 = A15 • A14 • /A13 • /A17 • RD
+ /A15 • A14 • A12 • WR + A16

Figure 4 illustrates the Maple programming sequence to generate this equation.

To program this equation, the PORT B menu is entered from the Maple software. CS0 is selected by moving the cursor to it using the arrow keys. With CS0 selected, the user then presses the F3 key to bring up the CHIP SELECT DEFINITION table for CS0. The table contains four rows for data entry, each one corresponding to one of the available product terms for CS0. Implementing this equation required using three of the four available product terms. The fourth is left blank and will not be used to generate the output.

To enter the equation into the table, simply move the cursor around into the appropriate position and enter a 1 if the corresponding signal should be high for the equation to be true, 0 if it should be low, and X or SPACE if the signal is a don't care. The first term of the equation requires a low on A17, a high on A15, a high on A14, a low on A13 and a high on RD for the term to become active. Thus, 1's are placed in the A15, A14 and RD positions,

Example: Generating a Logic Equation With PAD B (Cont.)

and 0's are placed in the A17 and A13 positions. The remaining terms in the equation are entered in the same way. Note that A17 and A16 in this example need not be address bits, but may instead be used to bring external signals into the PAD.

Four product terms are available on each of the CS0 – CS3 outputs, two terms are available on the CS4 – CS7 outputs and one term is available on CS8 – CS10. When planning the use of the PAD outputs, it is important to consider this so that the most efficient use of the product terms can be achieved.

Figure 4. Programming PAD Outputs

PORT B

PIN	CS/I/O	CMOS/OD
PB0	CS0	CMOS
PB1	CS1	CMOS
PB2	CS2	CMOS
PB3	CS3	CMOS
PB4	CS4	CMOS
PB5	CS5	CMOS
PB6	CS6	CMOS
PB7	CS7	CMOS

CHIP SELECT DEFINITION CS0

A19	A18	A17	A16	A15	A14	A13	A12	A11	ALE	RD	WR
X	X	0	X	1	1	0	X	X	X	1	X
X	X	X	X	0	1	X	1	X	X	X	1
X	X	X	1	X	X	X	X	X	X	X	X

ALIASES:

CS definition is the NOR of the product terms (rows). Enter 1 to select Active High signal, 0 to select Active Low signal, X to mean "don't care", SPACEBAR to erase. Enter values in columns relevant to your application; other blank columns will be treated as "don't cares".

F1 – Return to PORT B Cursor – Up: ↑ Down: ↓ Left: ← Right: →

Application Examples

The following section will illustrate the use of the PAD for system logic replacement in some common microcontroller applications.

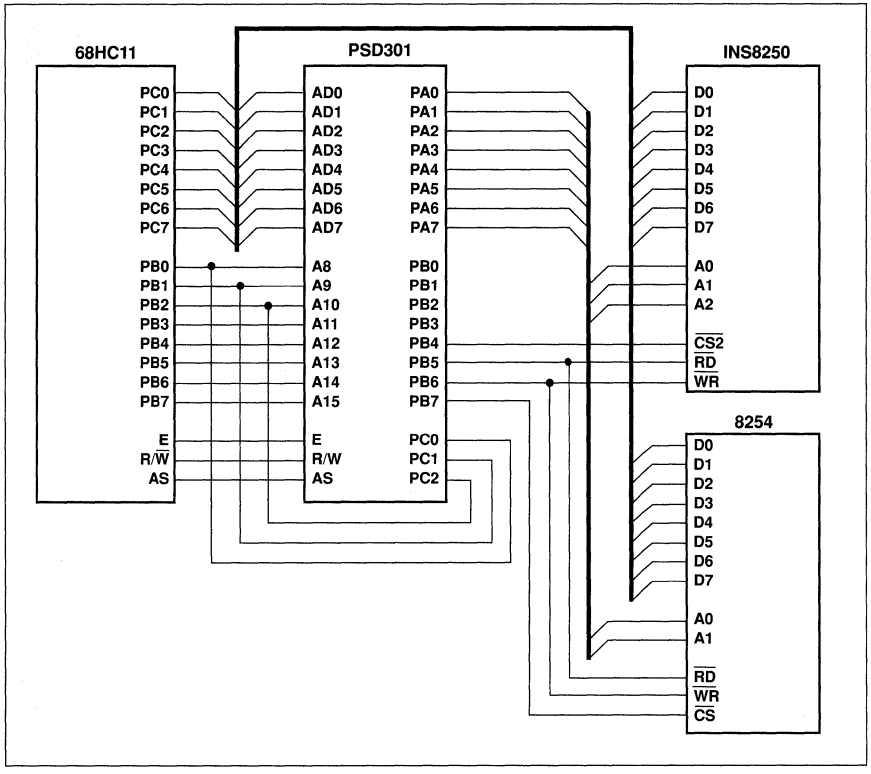
Basic Chip Select Generation

One of the simplest uses of PAD B is the generation of chip selects for off-chip resources such as I/O devices or memories. Figure 5 below depicts the connection between a 68HC11 microcontroller, the PSD301 and two common peripheral devices: the 8250 UART and the 8254 counter/timer.

The 68HC11 is an 8-bit microcontroller with a 16-bit address bus. The lower 8 bits of address are multiplexed with the data bus while the upper 8 bits are transmitted on their own bus. An address strobe (AS) is provided to latch the address off of the multiplexed bus. A R/$\overline{W}$ signal indicates whether the current bus transaction is a read or a write (R/$\overline{W}$ = 1 = read, R/$\overline{W}$ = 0 = write). The E signal is the clock used to strobe the data in or out of the microcontroller. The PSD301 can be configured to exactly match this signal definition and then connected as shown in the diagram. Not all of the 68HC11 or PSD301 signals are shown, only those relevant to this example of PAD capability.

The 8250 is a UART device commonly used in microcontroller systems to provide a serial data communication port. It has a simple bus interface, yet does not directly connect with the 68HC11 bus architecture. It requires an 8-bit bus to transfer data to and from the microcontroller and a separate 3-bit address bus used to access its internal registers. It also requires a chip select and separate read and write strobes ($\overline{RD}$ and $\overline{WR}$). The chip select is generated by decoding the address from the microcontroller. The $\overline{RD}$ and $\overline{WR}$ signals may be generated from the R/$\overline{W}$ and E signals

Figure 5. A Typical Microcontroller System



Application Examples (Cont.)

according to the following equations:

$$/RD = /(R/\overline{W} \bullet E)$$

$$/WR = /(/R/\overline{W} \bullet E)$$

These equations may be easily generated using PAD B and sent out through two of the chip select outputs. We have chosen CS5 and CS6, which come out on PB5 and PB6, for this example.

In order to provide the address lines to the 8250, we have configured Port A to output the latched address. This eliminates the need for any external latches to demultiplex the address/data bus from the microcontroller. Though all eight of the Port A pins have been configured as address outputs in this example, it is possible to configure only those address bits required for the application, A0 – A2 in this example, and configure the remaining Port A pins as general I/O.

The 8254 is a programmable interval timer which, like the 8250, is a peripheral used in many microcontroller applications. Its bus connection is very similar to the 8250, allowing it to use the same read and write strobes ($\overline{RD}$ and $\overline{WR}$) and address lines. It also requires a chip select which is decoded from the microcontroller address.

The chip selects for both of the peripheral devices may be easily decoded from the address inputs to PAD B. Normally, the addresses which are inputs to the PAD (A11 – A19) would give decoding resolution down to 2K. This means that each of the two peripheral devices that require chip selects would be allocated an address range of at least 2K. Since these devices do not require this much space and the 68HC11 has only a 16-bit address bus, it is possible to use the high order address inputs of the PSD device to improve the decoding resolution. To achieve this goal, we have configured Port C as address inputs A16 – A18, but have connected them to A8 – A10 from the microcontroller. This means that the PAD will now have

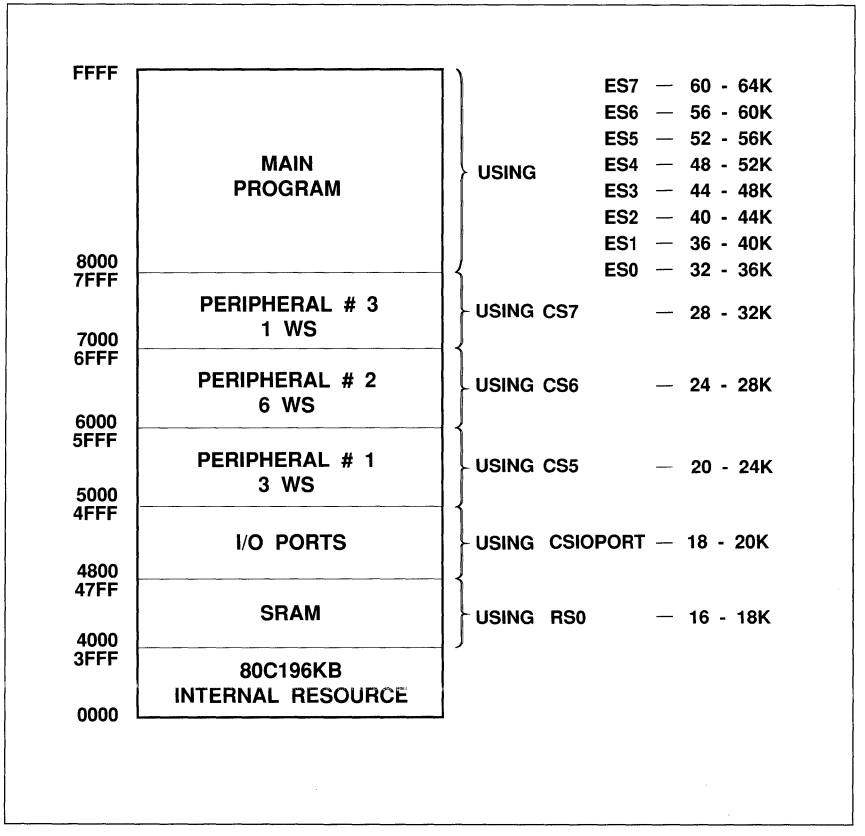
Application Examples (Cont.)

access to A8 – A15 for decoding, thus providing a resolution of 256 instead of 2K. This could actually be further reduced to a resolution of 128 if we were to configure the A19/CSI input to be A19, and then connect it to A7 from the microcontroller. In this example, we have not done this so that CSI is still available to place the PSD301 into low power mode if required.

We now have to define the addresses of each of the peripherals so that the chip select equations may be defined. We will start from the memory map provided earlier in Figure 2. This map allocated all of the internal resources of the PSD device. The external peripherals may be easily added to the unused area between addresses 0x2000 and 0x8FFF. Figure 6 depicts the new map with the external devices added. Notice that the internal resources can keep their original address mapping even though the additional address inputs (A8 – A10) have been added. This is because these inputs may be don't cares in the decoding for the internal resources even when they are being used for the external resources.

Now, to wrap up this simple design, we must enter the configuration and mapping information into Maple. The configuration of the PSD device must be consistent with the operation of the 68HC11 microcontroller. The address/data mode must be multiplexed, the data bus must be 8 bits wide, CSI/A19 may be configured either way, the reset polarity should be active low, the ALE polarity is active high, the read and write lines must be R/$\overline{W}$ and E, A19 – A16 should be latched so that these bits become available just like the rest of the address bus, and the read strobes for the

Figure 6. Memory Map With Peripherals



Application Examples (Cont.)

SRAM and EPROM will be the same. This configuration should be entered from the configuration menu of the Maple software.

The address map programming for this example will remain the same as the one used earlier in Figure 3. The only items remaining are the programming of the ports and the generation of the equations for the chip selects and read/write strobes. First we must configure Port A to provide the latched address to the peripherals. This is accomplished by entering the PORT A menu in the Maple software. Maple will then ask you if you would like Port A configured for address I/IO or the Track Mode. For this example, we will use the address/I/O configuration. Next, Port A must be configured pin for pin as an address output. This is easily performed by using the cursor keys to select the appropriate pin and pressing the SPACE BAR to change the configuration. It is also possible to configure each pin as an open drain or CMOS output, but for address outputs, it is better to make them CMOS.

Now, PORT C must be configured to provide the three additional address inputs. This is performed by entering the PORT C menu in Maple and selecting the appropriate pin with the cursor. Each pin should be configured as an address bit (Ai). Maple will call the pins A16 – A18 even though we will be using them as A8 – A10.

Lastly, we must configure the Port B outputs to become the chip selects and read/write strobes. First, the PORT B menu must be entered. Now, we must configure each pin as an I/O or CS output. PB0 – PB3 may be configured as general purpose I/O pins. PB4 – PB7 must be configured as chip selects. Once configured as chip selects, the equations for each output may be entered by following the Maple instructions. The procedure is the same as the one used in the earlier chip select example. Our equations, including the ones developed earlier for the read and write strobes, are defined for each output as follows:

$PB5 = /CS5 = /RD = /(R/W \bullet \overline{E})$

$PB6 = /CS6 = /WR = /(/R/W \bullet \overline{E})$

$PB4 = /CS4 = /8250CS = /(A15 \bullet /A14 \bullet A13 \bullet /A12 \bullet /A11 \bullet /A18 \bullet /A17 \bullet /A16)$

$PB7 = /CS7 = /8254CS = /(A15 \bullet /A14 \bullet A13 \bullet /A12 \bullet /A11 \bullet /A18 \bullet /A17 \bullet A16)$

This completes the design integrating these four components with no additional logic whatsoever. There is also additional space in the PAD for more functions if necessary, so we have not yet reached the limit of the integration possibilities with the PSD301.

Wait State Generation

Often, when using some of the newer high-performance microcontrollers with slower external peripherals, it is not possible to complete a read or write cycle to the peripheral in the time allowed by the microcontroller's minimum bus cycle. In this case, one or more wait states must be added to slow the controller down to the speed of the peripheral. One way of doing this is to fix a number of wait states for all bus cycles to allow the slowest device enough time for its access. Some controllers even provide the capability to do this internally through the programming of a register. This works, of course, but can severely impact the performance of the system. There is no need to penalize the performance of the entire system, which can include zero wait state memory devices and other peripherals, simply because one or more of the external devices requires some number of wait states. It is possible, with minimal logic, to create a completely programmable automatic wait state generator using the PSD301 which will allow the fast resources to operate at zero wait states and still provide from one to eight wait states for the slower resources.

For this example, we will use an Intel 80C196KB microcontroller running at 12 MHz. This controller has the capability to operate in a 16-bit data mode, providing the opportunity to further increase performance if the system can also operate in this mode. The PSD301 does have the capability of operating in the 16-bit mode, making it a good match for the 80C196. We will assume that the 80C196 must be interfaced to several slow 8-bit peripherals requiring from one to eight wait states. With

Wait State Generation (Cont.)

the PSD301, we can provide the correct number of wait states for each peripheral with the added capability of dynamically sizing the bus to the appropriate width for the current access.

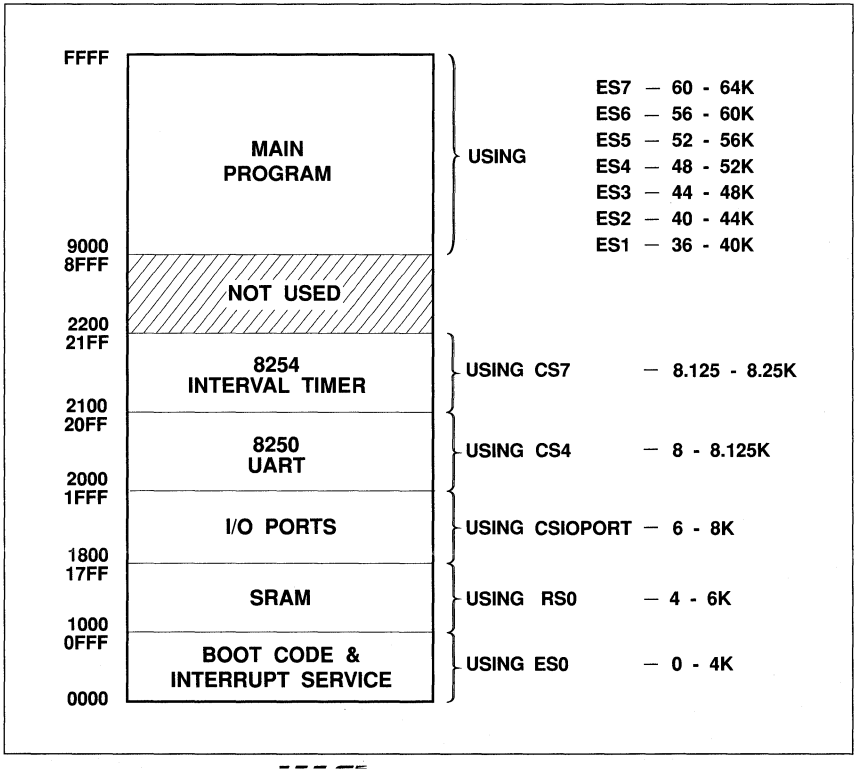
The memory map we will use for this design is depicted in Figure 7. The internal resources of some 80C196 derivatives occupy most of the address space from 0x0000 to 0x3FFF, though some have less resources. Therefore, we have constructed the memory map to place the PSD device resources above address 0x4000. The PSD301 SRAM and I/O devices occupy from address 0x4000 to 0x4FFF. This leaves the area from 0x5000 to 0x7FFF for external peripherals while leaving 0x8000 to 0xFFFF for the EPROM banks. We assume that we must connect three external peripherals to the PSD device using this address space, one requiring one wait state, one requiring three and one requiring six. This memory map is entered into the part similarly to the previous examples.

To achieve the variable number of wait states, the ideal solution is to decode the address to determine the number of wait states required for a particular address range, and then to use a counter to count the appropriate number. By using the PAD to initialize an external counter, a variable wait state counter can be created in this manner. This wait state generator requires only one external device, a 74FCT191 counter. The circuit used to implement this function is illustrated in Figure 8. The 80C196KB is directly connected to the PSD device which in turn provides the three chip select signals for the external peripherals ($\overline{PER1CS}$, $\overline{PER2CS}$ and $\overline{PER3CS}$) as well as the wait state generator function and the dynamic bus sizing. Ports B and C are fully utilized to provide the logic inputs and outputs required to implement these functions, while Port A is still available for general I/O or address use.

This circuit uses PAD B to decode the addresses driven by the microcontroller

2

Figure 7. Memory Map



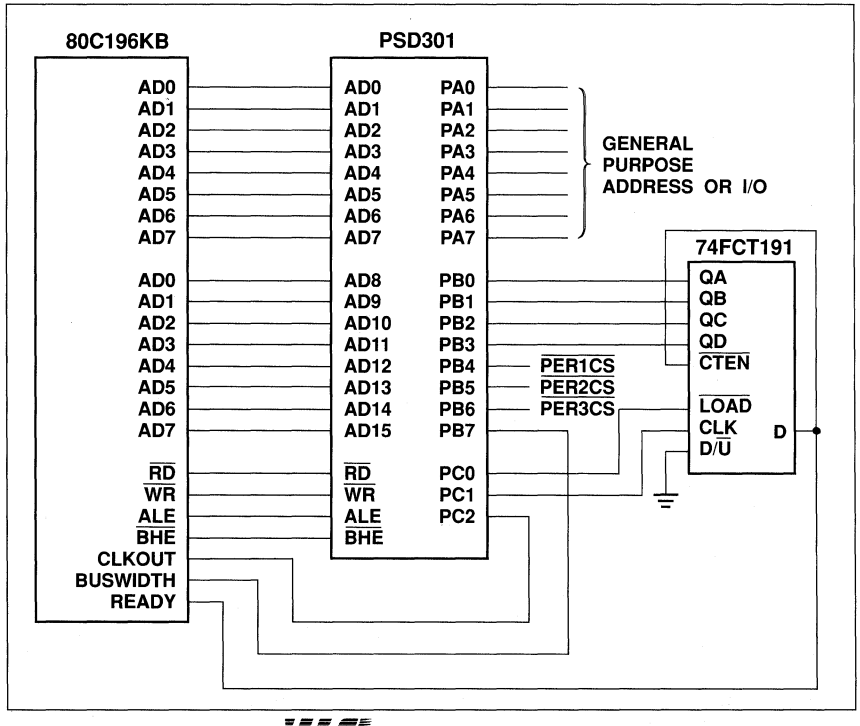
Wait State Generation (Cont.)

and provide four outputs, based on these addresses, which are used to initialize the 74FCT191 counter with its initial value. The counter is initialized using ALE to latch these four PAD outputs. The load signal for the counter is active low, however, while ALE is active high, so ALE is inverted using PAD B and sent out through Port C. Though the 80C196KB can be configured to provide an active-low address strobe, $\overline{ADV}$, the timing of the signal is inappropriate for use as the $\overline{LOAD}$ input to the counter. Once the counter is initialized, it counts up from the initial value until the most significant bit increments from 0 to 1. The output of the most significant counter bit is routed to the READY input of the microcontroller. Thus, the controller will be held in wait states until the most significant counter bit is incremented. This output is also routed to the $\overline{CTEN}$ signal of the counter so that counting will cease once the READY signal has been issued to the controller. The clock for the counter is an inverted version of the CLKOUT signal from the controller. This clock must be inverted since the 80C196KB uses the falling edge of the clock to sample the READY input. PAD B again provides the inversion function by routing CLKOUT into one of the Port C pins, inverting it and routing it back out through another Port C pin.

The counter provides from zero to eight wait states depending on the initialized value. For zero wait states, the most significant counter bit is initialized to a "1", which provides the READY signal to the controller immediately and disables the counter from incrementing. If one wait state is desired, the counter is loaded with the value 7 (0111 binary) so that after it increments once, the most significant bit switches to a "1" and provides the READY to the controller. When two wait states are required, a 6 (0110 binary) is loaded into the counter, and so on for the rest of the wait state values.

To properly size the bus to the appropriate width, PAD B is again used to decode the addresses of the 8-bit devices. When the address of an 8-bit device is encountered, the BUSWIDTH signal is driven to configure the 80C196KB address to eight

Figure 8. Wait State Generation Circuit



Wait State Generation (Cont.)

bits. For all other addresses, the width is set for 16 bits. The BUSWIDTH signal is output from one of the Port B pins.

The PSD device must now be configured to provide the functions required by the example circuit. The configuration of the PSD must first be programmed to function with the 80C196KB. This is easily performed by the Maple software as in the previous example. The address/data mode should be multiplexed, the data bus width should be 16 bits, CSI/A19 may be configured as required for the application, the reset polarity should be active low, the ALE polarity should be active high, separate $\overline{RD}$ and $\overline{WR}$ strobes should be used and A19 – A16 should be transparent, not latched, since they are used as logic inputs to the PAD.

Next, we must program the functionality of Port C. For this example, PC0 and PC1 are used as outputs from the PAD to provide the $\overline{LOAD}$ and CLK signals for the '191 counter. This is performed by entering the PORT C menu in Maple and configuring PC0 and PC1 as CS8 and CS9, respectively. PC2 is used to input the CLKOUT signal from the microcontroller to the PAD so that it may be inverted. Therefore, it must be configured as address input A18. Now, the equations used to generate the PC0 and PC1 outputs must be entered into the PAD. PC0 is the $\overline{LOAD}$ signal which is just the ALE input inverted. PC1 is an inverted version of A18, which contains the CLKOUT signal. These equations are listed below:

PC0 = /LOAD = /ALE

PC1 = /CLKOUT = /A18

The equations are programmed by entering the CHIP SELECT DEFINITION menu for each of the two chip selects, as in the previous example, and entering the appropriate 1's, 0's and DON'T CARES. In the case of PC0, there are don't cares in all of the PAD inputs except ALE, where there is a 0. Similarly, for PC1, the A18 input is a 0 while the rest of the PAD inputs are don't cares.

Port A is usually configured next, and in this example it is free to be configured in any mode necessary for the application. It may become either I/O or address outputs, or may be set in the Track Mode as described earlier.

We are now ready to configure Port B. This example requires that all of the Port B pins be used as chip selects (logic outputs) from PAD B. PB0 – PB3 are used to initialize the counter with the correct number of wait states for each device. These outputs are defined according to the address ranges for each of the peripherals and the number of wait states required for each. Table 3 summarizes the outputs required for each peripheral so that we may define the correct equations for the outputs.

Table 3. Wait State Summary

Peripheral No.	Address Range	No. Wait States	PB0–PB3
1	0x5000-5FFF	3	1010
2	0x6000-6FFF	6	0100
3	0x7000-7FFF	1	1110

Wait State Generation (Cont.)

This table can be easily used to form the necessary equations for PB0 – PB3. PB3 can be considered the enable for the wait state generator which is active low only in the address ranges of the three peripherals. It must remain high for all other address ranges. The other three outputs simply encode the proper number of wait states. The resulting equations are listed below:

PB0 = /QA = /(A15 • A14 • A13 • /A12)

PB1 = /QB = /(A15 • A14 • /A13 • A12)

PB2 = /QC = /(A15 • A14 • A13 • /A12)

PB3 = /QD = /(A15 • A14 • /A13 • A12 + /A15 • A14 • A13 • /A12 + /A15 • A14 • A13 • A12)

PB4 – PB6 are used as chip selects for each of the three peripherals and are simply decoded from the address inputs by PAD B corresponding to the address ranges listed in Table 2. These equations are listed below:

PB4 = /PER1CS = /(A15 • A14 • /A13 • A12)

PB5 = /PER2CS = /(A15 • A14 • A13 • /A12)

PB6 = /PER3CS = /(A15 • A14 • A13 • A12)

Finally, PB7 is used to perform the bus sizing function. It should be sized to eight bits whenever any of the external peripherals is accessed. It should be sized to 16 bits for all other accesses. The 80C196KB requires a high on the BUSWIDTH input for 16-bit operation and a low for 8-bit operation. This is accomplished by the equation below:

PB7 = BUSWIDTH = /(A15 • A14 • A13 + /A15 • A14 • /A13 • A12)

This completes the equations for Port B. These equations are entered in the Maple software by selecting the Port B chip select definition screens as described in the previous example and entering 1's and 0's in the appropriate locations. Remember that don't cares (X's or blanks) must be entered in all inputs which are not used by a particular equation.

Finally, we must enter the memory map into Maple Address Map screen. This is performed as in the previous example by entering 1's, 0's or don't cares in the appropriate places.

Conclusion

The PSD device may be used in a variety of applications requiring the simplicity, space savings and performance possible by the integration of memory and programmable elements. But a significant portion of the value of the PSD device, is its ability to absorb much of the logic functionality which normally surrounds a microcontroller application. The programmability of the device allows the designer to make changes to both the software and the design itself as required. This is not possible with masked ROM or ASIC-based designs. The PSD device can truly turn a microcontroller into a complete two-chip solution.

Programmable Peripheral
Application Note 016
Power Considerations In The PSD3XX

By Jeff Miller

Introduction

The PSD3XX is a configurable microcontroller peripheral integrating programmable logic, EPROM and SRAM technologies into a single piece of silicon. It has been used extensively in microcontroller applications around the world by virtue of its high level of integration, configurability and ease of use. This integration makes possible the design of very compact microcontroller systems, enabling the user to squeeze a great deal of functionality into a very small space. Thus, the PSD3XX has found its way into many small hand-held and/or battery operated applications such as cellular phones, medical instrumentation and laptop or notebook computers which usually require, in addition to small space, a very low power consumption.

The PSD3XX family is based on a patented high-performance CMOS technology and, like other CMOS devices, requires very low power consumption even when no particular effort is made to minimize the PSD3XX power. But, when some special care is taken during the programming and configuration of the device, power can be reduced even further, making the PSD3XX even more valuable in these power-sensitive applications. This application note will describe the methods which can be used to reduce the PSD3XX power consumption in both active and stand-by modes. It makes sense to use some of these techniques even when low power is not a primary design requirement since they are easy to implement and require no additional expense. We believe that proper implementation of the material in this note will make the PSD3XX an invaluable member of any low-power microcontroller system.

Power Use In The PSD3XX

The PSD3XX contains several modules internally, each of which can be considered a power consumer when in operation. These modules include the PAD, (Programmable Address Decoder)EPROM and SRAM blocks. The key to reducing the power used by the PSD3XX is to reduce the power used by each of these modules individually.

Under normal operation, several of the functional modules may be operating, while others may be standing by. A module in stand by uses much less power than one that is active. For example, whenever the SRAM is not being actively used, it is disabled and therefore consumes less power. This is also true of the PAD. A PAD term which is active expends more power than one which is inactive. This would also be true of the EPROM. However, in some PSD3XX models, the EPROM is always active, in which case it will always draw power. This is done in order to provide the best access time possible for the EPROM. The Low Power family of PSD3XXs does not keep the EPROM enabled at all times, and thus the designer can save power by minimizing the time during which the EPROM is accessed. Use of this feature does impact the speed of the PSD3XX EPROM, which results in the loss of the 120 ns speed grade. There are other methods of reducing EPROM power even when the EPROM is enabled. These will be discussed in detail later in this note. When the time that each PSD3XX function is kept in standby mode is maximized, the power expense is minimized.

There is a way to place the entire PSD3XX into the standby mode at once, thereby reducing power usage to the bare minimum. This can be done through the use of the CSI (Chip Select Input) pin. When the PSD3XX is deselected by the CSI pin, the entire part enters the standby mode using only about 50 μA of current. While in this mode, the PSD3XX is incapable of performing any functions, including PAD logic equations, but this is an excellent method of reducing system power in designs which have low active duty cycles.

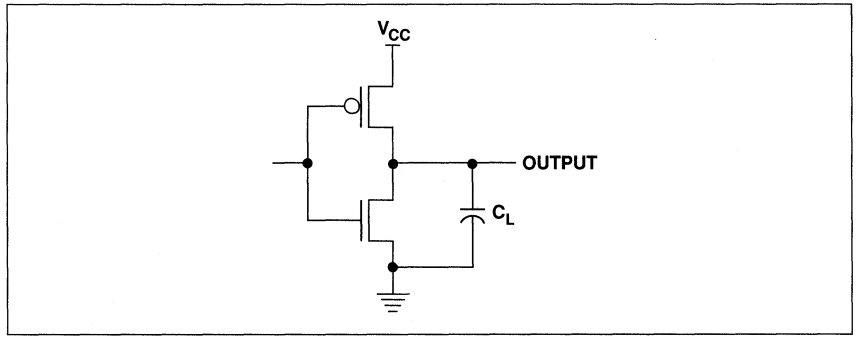
CMOS Power Characteristics

As a CMOS part, the PSD3XX behaves in the same way as other CMOS devices in terms of power dissipation. The PSD3XX consumes the most power when the temperature is low, the voltage is high and the frequency is high. Low temperature in CMOS devices, unlike in bipolar devices, causes the transistors to speed up, thus consuming more power. Therefore, if the system will never operate in low temperature environments, power dissipation will be lower. Another result of this characteristic is that CMOS parts do not generally experience thermal runaway. As temperature increases, the power expended by the CMOS device decreases, thus the part tends to effectively cool itself off.

Another characteristic of CMOS devices is the effect of voltage variations. CMOS behaves similarly to TTL devices with respect to voltage. When input voltage rises, the current drawn by a CMOS device also rises. As input voltage falls, input current also falls. Thus, the CMOS device will draw the least current at its lowest allowable supply voltage. This voltage is 4.5V in the PSD3XX. Taking the voltage below this level will generally slow the device down to below its specified speed as well as jeopardize its data retention capability. Between 4.5 and 5.5V, the PSD3XX varies by about 0.85mA per 0.1V variation. Thus, the PSD3XX will draw approximately 0.85 mA less current at 4.9V than at 5.0V V_{CC}.

Lastly, frequency of operation plays an important role in the power dissipation of a CMOS device. A CMOS gate expends the greatest power while it is switching between the logic 0 and logic 1 states, or vice versa. This can be easily understood when looking at the circuit diagram for a typical CMOS output shown in Figure 1.

Figure 1. Typical CMOS Output Circuit



The circuit above represents a typical CMOS inverter output. Normally, either the top transistor is off (output = logic 0) or the bottom transistor is off (output = logic 1). MOS transistors have very low leakage currents which means that under these normal conditions, very little current will be passing from V_{CC} to ground. However, when the input to the inverter is switching, both transistors will not switch from their present conditions to their new conditions at precisely the same instant. Therefore, both transistors will be on for a very brief instant during the transition. During this time there is a low impedance path from V_{CC} to ground and some current is drawn by the circuit. In addition, the output will have some load capacitance (C_L) which must be charged during switching, even if the load itself draws little or no static current. Thus, during the switching process the power expended by a CMOS device is at its highest.

The switching current drawn by the device is dependent on the number of times the outputs are forced to switch logic states in a unit of time. Therefore, the frequency of operation of the part directly influences its dynamic power consumption. The lower the operational frequency, the lower the dynamic power expended by the device. In the PSD3XX, frequency of operation is determined by the rate at which the addresses are changing, usually indicated by the frequency of the ALE or AS signal. Generally, the PSD3XX draws about 3 mA of additional current for each 1 MHz added to the frequency of operation.

Power Management Techniques In The PSD3XX

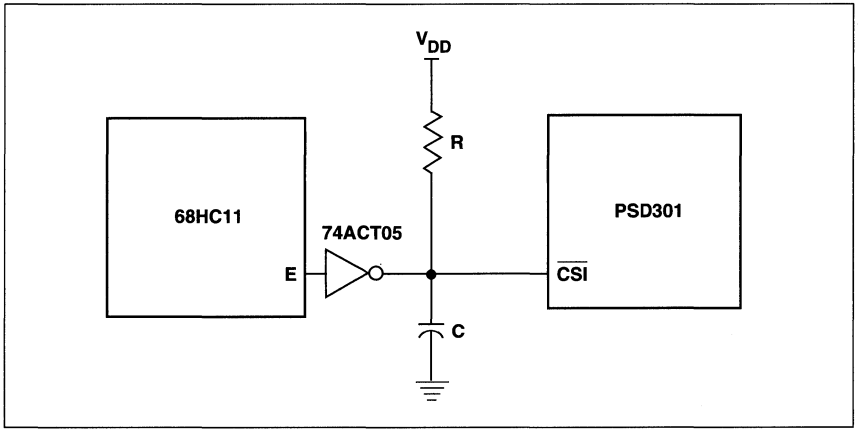
The above mentioned features and characteristics can be used to the designer's advantage when designing compact microcontroller systems which have a tight power budget. In the sections that follow, several methods for reducing the PSD3XX power will be presented.

Power Down Mode

Many system designs do not require the microcontroller, and therefore the PSD3XX, to operate continuously. Systems, like cellular telephones and notebook computers, spend a large amount of time inactive – waiting for something to happen like a press of a button or keyboard. During this time, many designers place the microcontroller into a low power idle or sleep mode. In the sleep mode, the controller expends significantly lower power. The microcontroller is usually awakened by some event – a key on a keypad being pressed, for instance, which may result in an interrupt. There is no need for the PSD3XX to be active during the time that the microcontroller is not active. Therefore, the PSD3XX should be placed in the power down mode (CSI inactive) to reduce the PSD3XX current down to its standby value.

The PSD3XX must also be awakened when the microcontroller is awakened so that it may provide an instruction to the controller when it requires one. If the microcontroller itself has a chip select output, like the Motorola 683XX series controllers, it may be used to awaken the PSD3XX as necessary. However, if it does not, there will be a problem. If the microcontroller itself is used to power down the PSD3XX, through an I/O port pin for example, there will be no way to power up the PSD3XX again since the PSD3XX itself contains the instruction that the microcontroller must use to activate the CSI signal to awaken the PSD3XX. The way to correct this situation is to design a circuit which detects when the microcontroller is coming out of its power down mode before it must fetch the first instruction. Such a circuit is depicted in Figure 2

Figure 2. Simple Power Down Circuit



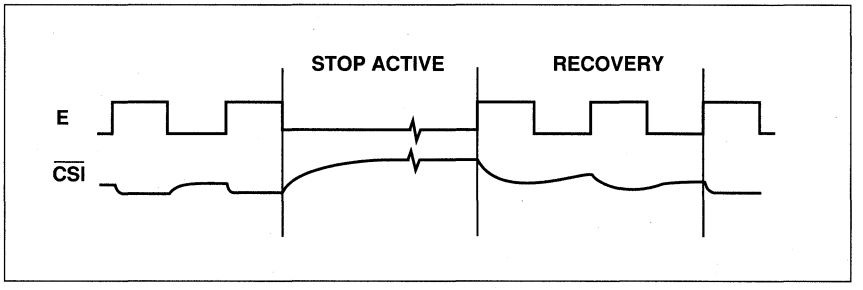
In this circuit diagram, a Motorola 68HC11 microcontroller is connected to a PSD3XX in a low power system. The circuit functions quite simply. The E signal from the HC11 is normally a free running clock at 1/4 the frequency of the input clock. When the HC11 is placed into the sleep mode by the software (by executing the STOP instruction), the E signal stops oscillating and remains low until an interrupt or internal timer event occurs. After the interrupt has been received by the controller, the E signal resumes toggling, but there will be a minimum of two E clock cycles prior to the first AS. This characteristic can be used to place the PSD3XX into its low power standby mode whenever the STOP has been executed in the HC11 and to awaken it before it must supply an instruction to the HC11.

Power Management Techniques In The PSD3XX (Cont.)

The ACT05 device shown in the diagram is simply an open collector inverter. When the E signal is oscillating, the output of the inverter will be toggling between ground and high impedance. When the output is at ground, the capacitor will rapidly discharge from its present state into the ACT05. When the output is high impedance, the capacitor will slowly charge up to V_{CC} through the resistor. Thus, under normal operation the $\overline{CSI}$ input of the PSD3XX will be at or near 0 V, provided the RC time constant is large enough to prevent the capacitor from charging up beyond a logic zero level of 0.6 V.

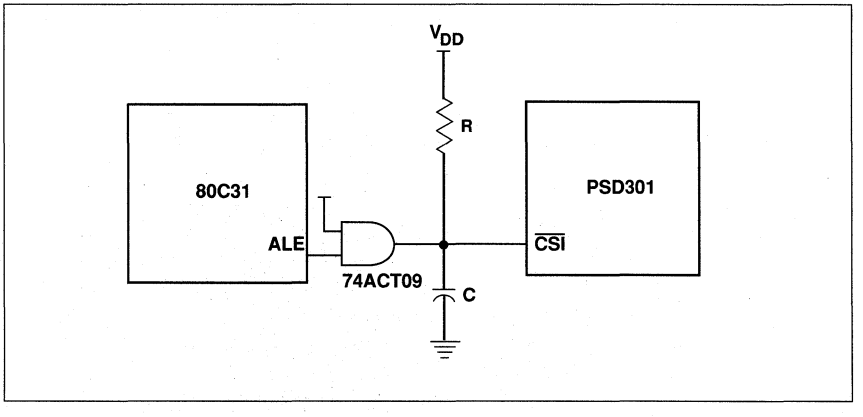
When the HC11 enters the sleep mode the E signal remains low. This enables the capacitor to slowly charge up to a logic one level which then places the PSD3XX into the standby mode in which it will consume only about 50µA of current. After the controller exits the sleep mode, the E signal will resume oscillating which rapidly discharges the capacitor. This, in turn, activates the $\overline{CSI}$ input to the PSD3XX, bringing it out of the power down mode. Since the E signal will oscillate for at least two full cycles before the first AS strobe begins a new bus cycle, the PSD3XX will have ample time to recover from the power down mode before having to supply an instruction to the HC11 for processing. In operation, the circuit results in a timing diagram similar to the one in Figure 3.

Figure 3. 68HC11 Stop Timing



A similar circuit can be used for Intel 8031 type controllers. Controllers conforming to the Intel 8031 family generally have two low power modes: IDLE and POWER DOWN. The IDLE mode causes the controller to cease instruction execution, but its internal clocks continue to run. This saves significant power while leaving the internal timers and other functions operational. When in the IDLE mode, both the ALE signal and the $\overline{PSEN}$ signal are held high. A circuit similar to the one illustrated for the 68HC11 may be used to detect the end of oscillation on the ALE signal. This circuit is shown in Figure 4.

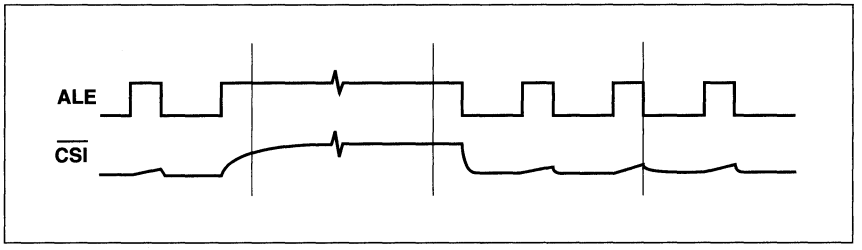
Figure 4. 8031 Idle Circuit



Power Management Techniques In The PSD3XX (Cont.)

The circuit operates on the same principle as the one used earlier for the Motorola processor. The ALE signal normally oscillates high for 2 clocks out of every 6 or 12 clocks, depending on whether instruction or data accesses are being performed. The software places the 8031 into the Idle mode by setting bit 0 in the PCON register. Once set, the ALE and $\overline{PSEN}$ signals remain high until an interrupt or hardware reset occur. During this time, the $\overline{CSI}$ signal will float high with the RC circuit, as in the earlier example. The ACT09 is simply an AND gate with an open collector output. It performs the same function as the inverter in the previous example without inverting the signal. When an interrupt or reset is received, the ALE signal begins to toggle again, but at least two "dummy" unused ALE cycles will occur before the first meaningful instruction is fetched, giving the PSD3XX time to recover from the power down mode. The timing for the above circuit is shown in Figure 5.

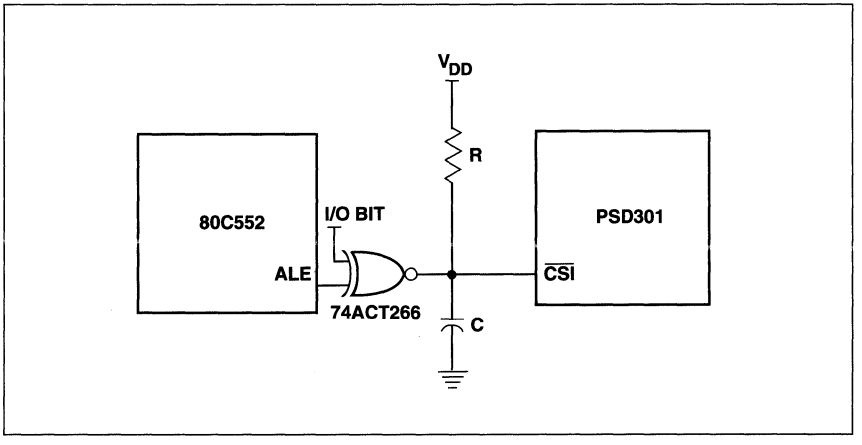
Figure 5. 8031 Idle Timing



If the system requires truly the lowest power available, the 8031 POWER DOWN mode may be used. This disables all internal operations of the 8031 as well as the external ones. Thus, any on-chip peripherals like timers and serial communication links will be disabled. This places the controller into its lowest power mode possible. Software may place the 8031 into the POWER DOWN mode by setting bit 1 in the PCON register. When execution of the instruction is complete, the ALE signal will be driven low and will remain in this state until a hardware reset or an interrupt is received. Thus, a circuit similar to the one above may be used to detect the static condition of the ALE signal, but an inverting gate must be used instead of the ACT09 (such as the ACT05 used in the Motorola example earlier).

If both the POWER DOWN and IDLE modes must be used, the gate may be replaced with an ACT266 exclusive NOR with an open collector output. This circuit is shown in Figure 6.

Figure 6. 8031 Power Down or Idle Circuit



Power Management Techniques In The PSD3XX (Cont.)

The I/O bit can be provided by either the PSD3XX or the controller itself. If the controller is used to provide the I/O bit, it must hold the correct value on the output even when in the idle or sleep mode, as the PSD3XX does. When the I/O bit is low, the POWER DOWN mode is enabled (a low on ALE and a LOW on the I/O bit will result in a high on $\overline{CSI}$). When the I/O bit is high, the IDLE mode is enabled (a high on ALE and a high on the I/O bit will result in a high on $\overline{CSI}$).

For all of the above circuits to operate correctly, the value of the RC network must be carefully calculated to insure proper operation in the normal mode. This means that under normal operation, $\overline{CSI}$ must never climb above 0.4 V, which will guarantee that it is always recognized by the PSD3XX as a low.

For example, the 68HC11 circuit shown in Figure 2 used the E signal from the controller to disable the PSD3XX. The E signal oscillates at 1/4 the frequency of the HC11's input clock. If an 8 MHz HC11 is used, the E signal will oscillate at 2 MHz. This results in an E signal clock period of 500 ns. During this 500 ns the E signal will be low for 250 ns. Thus, the RC network must be chosen to prevent the $\overline{CSI}$ signal from climbing above 0.4 V for at least 250 ns. The equation below governs the voltage across the capacitor (V_C), and thus the voltage present on the $\overline{CSI}$ pin:

$$V_C = V_{CC}(1 - e^{-t/RC})$$

where V_C is the voltage across the capacitor (which is the same as the $\overline{CSI}$ pin), V_{CC} is the supply voltage, and t is the time in seconds after the output of the open collector gate switches from a low to an open circuit. Solving for RC we get:

$$RC = -t/\ln(1-V_C/V_{CC})$$

In order to determine the minimum values for R and C, we must solve this equation for the point of time which is of interest. We must have V_C no greater than 0.4V at time t = 250 ns. Thus, with V_{CC} = 5 V, the equation may be rewritten as follows:

$$RC = -250 \times 10^{-9}/\ln(1 - 0.4/5.0) = 3.0 \times 10^{-6}$$

An acceptable RC network for this case might be a resistor of 100KΩ and a capacitor of 30pF. These values will provide no margin for the circuit so some additional resistance or capacitance may be desired. Of course, larger values may be used without harming the circuit, they will just cause the low power mode to be entered more slowly. The case of leaving the low power mode is less critical, since the capacitor will discharge more quickly through the gate than it will charge up through the resistor. In the interest of minimizing power use by the circuit itself, it is best to use a larger resistor value and a smaller capacitor value, since this will cause less current to be sunk by the gate which drives the circuit.

Using this equation, it is possible to determine the RC value required for any controller and/or frequency. It is only necessary to determine the length of time that the RC will be required to hold the $\overline{CSI}$ signal below 0.4 V and plug that value into the above equation.

If a more deterministic method is desired for placing the PSD3XX in the power down mode, a fully digital circuit may be implemented which uses very few additional components. This circuit is shown in Figure 7 for the 68HC11 controller.

This circuit performs the same function as the RC circuit described earlier, but does it digitally. The 74ACT164 is a shift register which is used in this example to detect when eight HC11 input clocks occur while the E signal remains low. In normal operation, no more than two clocks should occur without E transitioning from low to high, thus providing a clear to the ACT164. If the HC11 is stopped, the E signal will remain high until an interrupt is received, but the input clock continues to run freely. Thus, the shift register will shift in "one's" until the E signal goes high again. When the ACT164 has shifted eight times, the $\overline{CSI}$ signal will go high, placing the PSD3XX into the power down mode. The timing diagram corresponding to this circuit is shown in Figure 8.

Figure 7. Digital Sleep Circuit For 68HC11

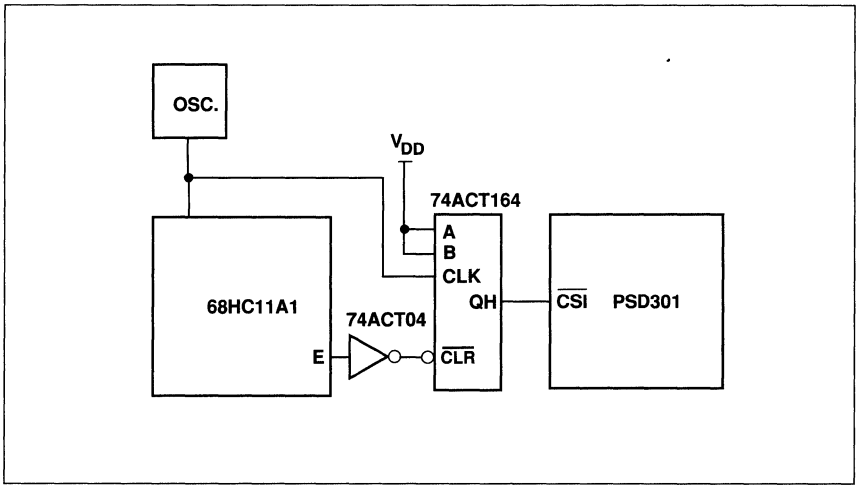
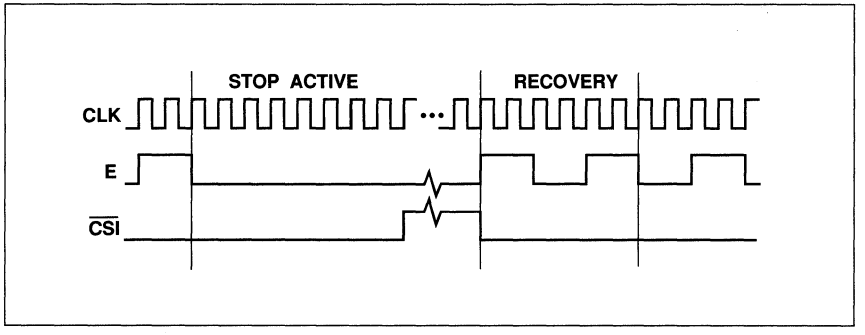


Figure 8. 68HC11 Stop Mode Timing



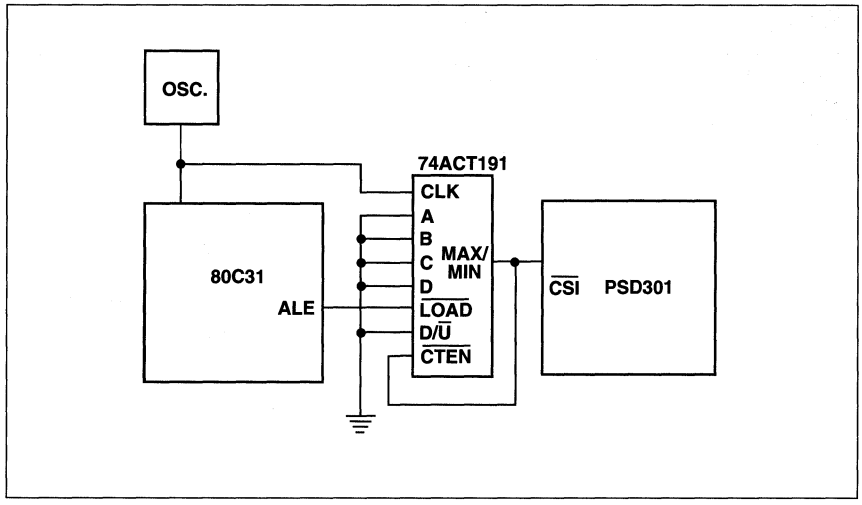
Power Management Techniques In The PSD3XX (Cont.)

A similar circuit may be used for the 8031 family of controllers, and is depicted in Figure 9.

This circuit, like the others, detects when ALE stops toggling. Since up to 10 clocks may normally occur without an ALE pulse, a counter which can count to at least 11 is required in order to function properly. Thus, an 8-bit shift register like the one used with the HC11 will not work. In this case, a 74ACT191 is used to count 16 clocks prior to raising its MAX/MIN output high. A low on the ALE signal will load zero's into the counter and clear the MAX/MIN output. The MAX/MIN output is also used as the counter enable to prevent the counter from counting further after attaining the count of 16. The circuit shown will function with the IDLE mode of the 8031. If the POWER DOWN mode is used, an inverter must be inserted in the ALE signal path.

Other controllers, not listed here, may also have power down modes which may function with these circuits. Any controller which has some sort of external indication when the power down mode has been entered may usually be used to place the PSD3XX in its low power mode also.

Figure 9. Digital Sleep Circuit for 8031 Family



Power Management Techniques In The PSD3XX (Cont.)

PAD Programming Techniques

The preceding section has described methods of using the power down capability of the PSD3XX with several microcontrollers. There are also techniques which may be utilized during programming of the device to further reduce power. These techniques can significantly reduce the power expended by the PSD3XX when it is in full operation.

The programmable logic section of the PSD3XX, called the PAD, provides much of its great flexibility and configurability. It is used to control the internal resources of the PSD3XX and can also be used to control external resources as well. The power use of the PAD varies greatly depending on how its product terms are programmed and used.

The PAD is illustrated in Figure 10. It is divided into two sections, called PAD A and PAD B. PAD A is responsible for generating the control and selection for the internal resources of the PSD3XX and utilizes 13 product terms to perform these functions. PAD B provides any external chip selection and logic replacement that is necessary for the system and has 27 product terms for this purpose. A single product term is functionally illustrated in Figure 11.

Each of the PAD inputs and its complement is available to each of the 40 product terms of the PAD. Each of these inputs is connected to an n-channel transistor which is used to connect the entire line to ground when the input is in the appropriate state. A high on the input to the gate causes the transistor to turn on. When the device is programmed, each of these transistors may be left in place or may be functionally removed (programmed out) from the circuit. If all of the transistors are programmed out, the line is left connected only to the pull-up resistor which makes it always high. Thus, the output of the inverter is always low. If an equation such as:

$$/CSx = In\#1 \bullet /In\#2$$

is programmed into the PAD, the output $\overline{CSx}$ must be high except when In#1 is high and In#2 is low. Thus, all of the transistors are programmed out except the ones connected to In#1 and In#2. This means that unless In#1 is high and In#2 is low, there will always be at least one of the two remaining transistors turned on, which in turn results in the $\overline{CSx}$ output being high. When the appropriate input condition is met, the remaining two transistors will turn off, which allows the output to become low.

Figure 10. PAD Illustration

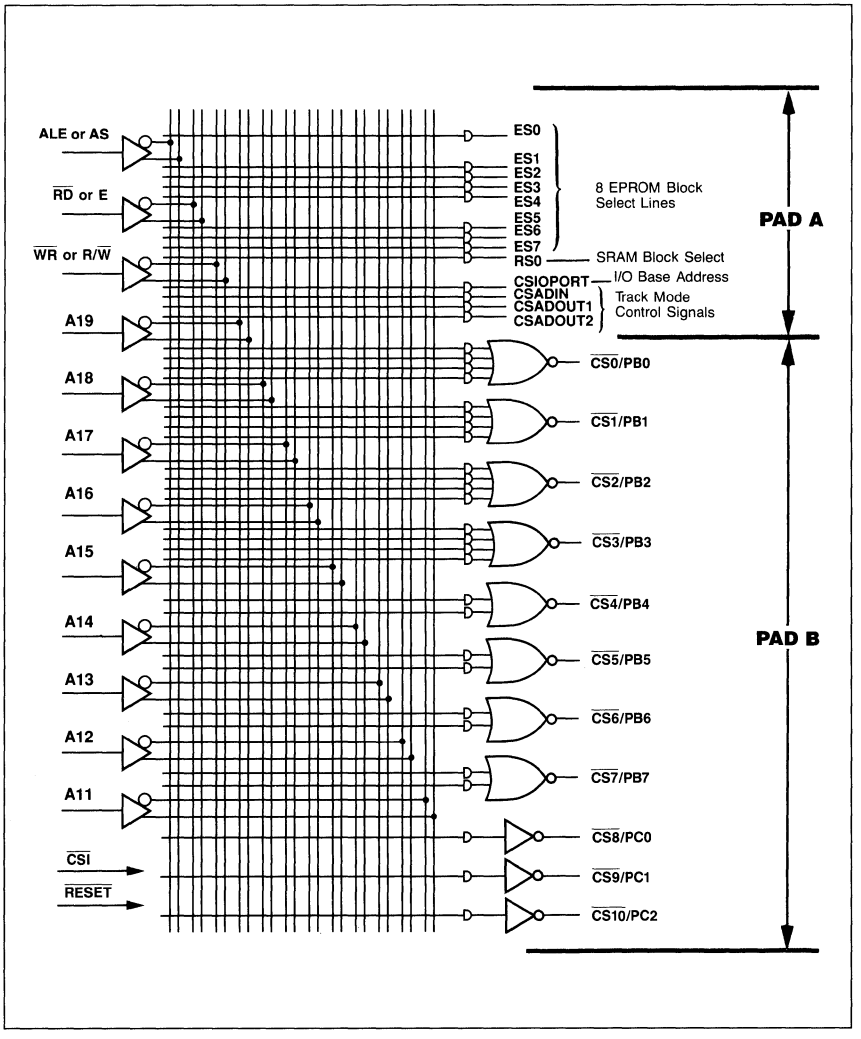
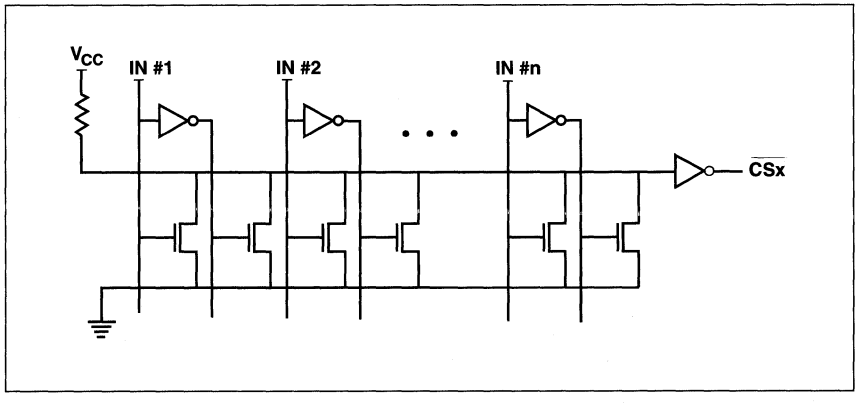


Figure 11. Product Term Functionality



Power Management Techniques In The PSD3XX (Cont.)

As can be seen in the figure, the product term expends very little power when all of the transistors are either programmed out or turned off. The only power used in this case is the result of the leakage current through the various off transistors, which is very low in CMOS technology. When one or more of the transistors is turned on, there will be current drawn through the pull-up resistor to ground. Therefore, the power used by a product term varies greatly according to the way it is programmed.

Experimental data has shown that a product term with all of the transistors programmed out draws approximately 380µA less current at room temperature and 5.0 V V_{CC} than a product term which has some active transistors. WSI's MAPLE software packages take advantage of this fact to reduce power as much as possible.

When the user intends to use some or all of the Port B pins as I/O signals, then they are not connected to the PAD in any way. Thus, the MAPLE software is free to program the unused PAD B product terms in any way. In MAPLE versions 4.03B and subsequent, the software automatically programs out all transistors in each unused product term, which can eliminate up to 24 product terms for Port B. This results in a power reduction of up to 9.1 mA.

If one or more of the Port C pins is programmed as an address or logic input, MAPLE is free again to program out all of the transistors in each unused PAD B product term dedicated to Port C. This can eliminate up to 3 additional product terms resulting in a power reduction of over 1 mA.

Finally, there are three product terms from PAD A which are dedicated to controlling the Port A Track Mode operation. If the Track Mode is not used in the application, these product terms may also be eliminated by MAPLE for a power reduction of over 1 mA.

The remaining ten product terms are the 8 EPROM select lines, the SRAM select line and the I/O port select line. These terms may not be eliminated by MAPLE without disrupting the operation of the device. But in a system which uses Port A and Port B as I/O or address outputs, and Port C as address or logic inputs, the total system power saving is 10.2 mA typical.

The same methods may also be used in non-multiplexed microcontroller applications. In this case, Port A and Port B may be used as microcontroller data input pins, depending on whether the controller is 8- or 16-bit. As in the earlier cases, if the ports are used as data input pins, they are not connected to the PAD which allows MAPLE to program out the appropriate product terms.

Again, MAPLE 4.03B or a subsequent revision must be used to obtain this capability. If your software is an older revision, contact your local WSI regional sales office for a free update.

EPROM Programming Techniques

Like the PAD, the EPROM in the PSD3XX uses varying amounts of power depending on how it is programmed. When programmed to a one, an EPROM bit draws more current than when programmed to a zero. Thus, for minimum power usage it is best to have the majority of the EPROM programmed to zeros.

Unfortunately, the contents of the EPROM are fixed by the program and data requirements of the system and thus cannot be easily optimized for power. However, the user can program all unused sections of the EPROM to zeros. This will not substantially cut the power used by the PSD3XX under normal operation when EPROM accesses are being performed, but it will reduce the power consumption during periods when there is not a valid address on the bus because these invalid addresses will often point to unused EPROM locations. When an EPROM location is currently addressed, it is expending power even if the $\overline{RD}$ or $\overline{PSEN}$ signals are not actually enabling an output. Therefore, it is best that unused EPROM locations be filled with zeros so that power is minimized during these periods of invalid addresses. It should be noted that all power figures used in this application note as well as those specified in the PSD3XX data sheet are based on an average of 50% "ones" and 50% "zeros" contained in the EPROM. An EPROM location programmed to "ones" will draw approximately 1.5 mA of additional current over an EPROM location programmed to "zeros".

Power Management Techniques In The PSD3XX (Cont.)

An even better way to help minimize power usage is to control the addresses which appear on the bus when there is no valid address being driven by the microcontroller. The least power expense will be when this unused address points to an area which has no PSD3XX resource mapped into it. This will result in no internal resource block receiving a chip select and thus the least amount of current will be drawn. The next best approach is to have the unused address point to an EPROM area containing zeros. The next lowest power would be to have the unused address point to an EPROM area containing something other than zeros. Finally, the highest power will occur when the unused address points to an SRAM location.

Since there is not much that can be done about the address that is appearing at the output of the microcontroller, the best that can be done is to know what address the controller will have active on its bus at various non-operational times and insure, if possible, that the PSD3XX's address map maps that address into a desired range of memory (preferably no memory at all). This will truly minimize the power expended by the PSD3XX during these times.

Summing It All Up

After taking all of these factors into account, what kind of power use can you expect from the PSD3XX in your own system? As a guideline, we will calculate the typical power required of a PSD3XX installed in a hypothetical system. The requirements of this system are listed in Table 1.

Using this information, we can calculate the approximate typical power requirements of the PSD3XX. Before we can begin, we must know what the base power of the PSD3XX is under the voltage and temperature conditions specified. The base power of the PSD3XX is the power used by the PSD3XX when only the product terms which control the EPROM, SRAM and I/O ports are not programmed out (10 active product terms). The base power also assumes that no internal resources (EPROM, SRAM and I/O ports) are being currently accessed. The current drawn by the PSD3XX under these conditions has been determined experimentally to be 16 mA. To this current, we must add additional current for the other active product terms, SRAM access and EPROM access.

Table 1. Hypothetical System Requirements

Characteristic	Specification
PSD3XX Operational Frequency	2 MHz
Port A	Address Output
Port B	4 Chip Select, 4 I/O
Port C	Logic inputs
$\overline{CSI}$	Configured for Auto. Power Down
V_{CC}	5.0 V
Temperature	25°C
Standby duty cycle	60%
EPROM duty cycle	30%
SRAM duty cycle	10%

Summing It All Up (Cont.)

The system is requiring only four of the 11 available chip select outputs. Therefore, most of the PAD B product terms may be programmed out. To determine how many product terms we will be using, we must look at the equations for the four chip selects. Assume that the following equations are to be used:

/CS#1 = /(A15 • A14 • RD + A13 • A12 • WR)

/CS#2 = /(/A18 + /A17)

/CS#3 = /(A16 • A18 + A17 • ALE)

/CS#4 = A17

In order to configure the system for the lowest power usage, we must be sure that we place these chip selects on the output pins which will require the minimum number of product terms to remain active. Since the maximum number of product terms required to generate the above equations is only two, there is no need to place these chip selects on Port B pin 0,1,2 or 3 since these pins each have four product terms. The lower power configuration would place these chip selects on Port B pin 4,5,6 and 7, where only two product terms will be drawing power for each chip select. One of the above chip selects, #4, actually requires only one product term, meaning that it could be placed on one of the Port C pins which have only one product term. However, all of Port C is used in this case as logic inputs (A16, A17 and A18) and therefore cannot be used as chip selects. Since the rest of the Port pins are not used as PAD outputs, the MAPLE software will automatically program them out.

If we do configure the chip selects to output on PB[0:3], we must add 8 product terms to the 10 used in calculating the base power number. Using the current per product term of 380µA provided earlier, eight additional product terms result in an additional 3.0 mA of current.

Experimental data has shown that accessing the SRAM results in an additional current expense of 31 mA above the base current. Also, accessing the EPROM draws an additional 0.5 mA over the base current. The standby current has been measured at 50 µA. Finally, we must consider the additional current used by the frequency of operation. This is 3 mA per 1 MHz for a total of 6 mA, since the PSD3XX will be operating at 2 MHz. This provides us with all of the data that we need to calculate the total power usage of the PSD3XX in this system.

Table 2 can be used to calculate the EPROM access current, the SRAM access current and the standby current.

Table 2. Summary of PSD3XX Current Usage In Hypothetical System

PSD3XX Block	Current Used
Base Configuration	16 mA
PAD (as configured)	3.0 mA
EPROM	0.5 mA
SRAM	31 mA
Frequency Component	6 mA
Standby Current	50 µA

Now, summarizing further, the total EPROM access current is:

Base Current + PAD Current + EPROM Current + Frequency Component
= 16 mA + 3.0 mA + 0.5 mA + 6 mA
= **25.5 mA**

The total SRAM access current is:

Base Current + PAD Current + SRAM Current + Frequency Component
= 16 mA + 3.0 mA + 31 mA + 6 mA
= **56.0 mA**

Summing It All Up (Cont.)

Now we must account for the duty cycle of the system to determine the total average power for the PSD3XX. In order to apply the duty cycle, we simply multiply each power component by its duty cycle and add them all together. The equation to perform this is given below:

Total Current = $0.6(i_{SBY}) + 0.3(i_{EPROM}) + 0.1(i_{SRAM})$

where i_{SBY} is the standby current, i_{EPROM} is the active EPROM current and i_{SRAM} is the active SRAM current. Plugging in the numbers we developed earlier, the equation becomes:

Total Current = 0.6 (50 μA) + 0.3 (25.5 mA) + 0.1(56.0 mA) = **13.3 mA**

The average current drawn by the PSD3XX under the specified conditions of configuration, frequency and environment is therefore 13.3 mA. The peak typical current used by the PSD3XX is 54 mA while the SRAM is being accessed. The minimum current is 50 μA, drawn by the PSD3XX while it is in the Power Down mode. This compares very favorably with the typical current usage of a fully discrete solution.

Typical vs. Maximum Current

The typical and maximum current numbers are both specified by most integrated circuit manufacturers. Many designers are unsure of what these parameters are and how they relate to the power which will actually be dissipated by the system. This is compounded by the configurability of the PSD3XX.

The maximum power numbers published in most product specifications are usually chosen as the number which will never be exceeded by the device under any circumstances, including variations in processing, V_{CC} and temperature. To truly be a maximum number, all three of these parameters must be at their worst cases simultaneously, which is quite unlikely. Therefore, power use will more likely follow the typical values when the system is actually running.

In the PSD3XX data sheet published by WSI, two current values are published for typical conditions and another two are published for worst case conditions. These two sets of numbers are used to specify current use in two different PSD3XX configurations. The lower numbers represent the current drawn by the PSD3XX while configured with 10 active product terms. To arrive at the maximum value for this configuration, we assume that the programming of the device has not changed, but we take the temperature, voltage and processing to their worst case conditions. These numbers are generated again for the configuration of the PSD3XX which has all 40 product terms active. To determine the typical current drawn by the PSD3XX in your system, it is best to use the techniques presented in this application note. All of the typical current values used in this note are the result of careful experimentation, and should parallel very closely the values measured in your own system. To extrapolate the worst case current for your configuration from your calculated typical value, you must add about 50% to account for voltage, temperature and process variation.

When calculating the worst case current for your entire system it is usually best to use the typical current numbers for all of the components installed and then apply some margin to allow for worst case conditions. This is much more accurate than using the worst case parameters for each component since it is *extremely* unlikely that *all* of the components used are simultaneously at their worst case process parameters, though they may all be at worst case voltage and temperature. Usually 20% margin above the typical numbers will sufficiently cover the worst case for the entire system.

Table 3 summarizes the typical current numbers for the PSD3XX which can be used when calculating the current used in your own system.

Table 3. Summary of PSD3XX Typical Current Usage

Base Current (10 product terms, SRAM and EPROM Unselected)	16 mA
Additional Current per Product Term	0.38 mA
Additional Current for SRAM Access	31 mA
Additional Current for EPROM Access	0.5 mA
Additional Current for Frequency Effects	3 mA/MHz
Additional Current for Voltage > 5V	0.85 mA/0.1V
Standby Current	50 µA

Conclusion

The PSD3XX is a very important device in the design of compact, low-power systems. It provides a cost effective minimum part count solution for a typical microcontroller system. It also provides a very low power solution for those designs which are handheld and/or battery operated. As the PSD3XX family grows and evolves, more innovations will be presented in terms of integration and power usage. The new low power PSD3XX family will be introduced soon, providing the designer with an even lower power solution. Until then, use of the techniques described in this note will provide a minimum power solution for your microcontroller system.

Programmable Peripheral
Application Note 018
Security of Design in the PSD3XX

By Oudi Moran

Introduction

The PSD3XX is a family of field programmable and UV erasable microcontroller peripherals that have the ability to interface to virtually any microcontroller without the need for external glue logic.

Any PSD3XX family member is a complete microcontroller peripheral solution with Memory (EPROM, SRAM), Logic, I/O Ports and a Security bit on chip.

In today's competitive business environment, where the cost of the product and its quick introduction to market are the most important factors for success, some companies tend to copy a competitor's design. By doing so, they can save development time which can reduce their engineering cost and eventually reduce the product's price and its introduction time to the market.

This is true mainly for the consumer and commodity product markets where microcontrollers are widely used. The PSD3XX, as the primary microcontroller peripheral, contains all the important code and architectural data that a potential competitor may want to copy.

Since the PSD3XX is a field programmable device, its contents may be read by an I.C. programmer, decompiled and copied by a competitor.

Obviously, it is an undesirable situation for the EPROM, PAD and configuration data of the PSD3XX to fall into the hands of a competitor. To prevent this, the PSD3XX device implements a security "fuse" or programmable bit feature to protect its contents from unauthorized access and use by a competitor.

Uploading the programmed data from EPROM, PAD, ACR and NVM port configuration sections of a secured PSD3XX device is disabled by the security bit (if turned ON). The RAM of the programmer (after trying to upload a secured PSD3XX device) will contain invalid random data.

A secured PSD3XX device will function properly in the system – the microcontroller will be able to access the EPROM, SRAM, PAD and the I/O ports but any attempt to read or verify the contents of a secured PSD3XX by external hardware will fail.

Use of the Security Bit

PSD3XX devices contain non-volatile configuration bits to enable the user to set and configure the device to the proper operational mode. The configuration bits will configure the device to interface successfully with the microcontroller and also configure the PSD3XX I/O Ports. The configuration bits are programmed during the programming phase and cannot be accessed in operational mode.

During programming the configuration bits are programmed as two separate sections:

1) The ACR section of the PSD3XX device contains global configuration bits for proper microcontroller interface. The security bit resides as an individual configuration bit in the ACR section of the device.
2) The NVM section of the PSD3XX device contains port configuration bits for proper set up of Ports A, B and C.

PSD3XX devices use the security bit to prevent unauthorized access to the configuration data inside. Since the security bit is part of the ACR global configuration bits section, it can be programmed in the same manner as all other configuration bits.

All ACR and NVM configuration bits of the PSD3XX are non-volatile, so their contents will not be erased or corrupted during the power down mode of the device (when the PSD3XX is deselected with $\overline{CSI}$/A19 = High) or during power down when V_{CC} is removed.

Use of the Security Bit (Cont.)

The security configuration bit is user programmable and UV erasable as well, so a secured part can be erased completely and be reprogrammed (only if the device is in a windowed package).

Setting the security bit will lock all the contents of the PAD, ACR global configuration bits, and NVM port configuration bits. By setting the security bit the device cannot be entered into Initialization and Override mode (resets the device and enters it to a known default configuration before activating the individual read mode for each section). Any attempt afterwards to enter the device to DIRECT mode for uploading or programming will fail. Setting the security bit prevents a programmer from directly accessing the various sections of the device.

Even though the EPROM, SRAM and I/O port contents are not directly disabled by setting the security bit, it is impossible to read them by using external equipment (except by the microcontroller in the system where the PSD3XX designed in). This is because the external equipment will lack information about the address mapping of the eight EPROM blocks, SRAM and I/O ports in the memory map of the microcontroller and the unknown status of the global and I/O port configuration bits.

Even if an unauthorized user figures out the configuration of the part by knowing what microcontroller is interfaced (ALE polarity, what type of read and write signals, etc.) and gets data out of the PSD3XX (after applying address and control signals to the device), the user will have no idea where it came from: EPROM, SRAM, I/O Port Register, Page Register, etc. This effectively renders the data useless.

Setting the Security Bit

The security configuration bit is called CSECURITY.

If CSECURITY = 0, it means security is off (security bit is not set and its value will be '1' in the object file).

If CSECURITY = 1, it means security is on (security bit is set and its value will be '0' in the object file).

Setting the security bit and activating the security mode can be done in two different ways:

1) By turning security ON in the configuration menu of Maple development software.

2) By setting the security in the programming software (done after the device is fully programmed and verified).

Using Maple development software to turn security ON gives the security bit the value '0', and will integrate it in one of the ACR addresses of the object file created after compilation. (See Security Bit File Location section of this document).

If Setting of the security bit is done in the programming software (Third party programming software or WSI Mappro programming software), the user should program and verify the device using a Maple generated object file (with security option OFF) and then set the security ON by using a separate programming software command.

Some third party programmer manufacturer's software will load the Maple generated object file but mask the security bit before programming the device. In that case the user will have to set the security bit (if necessary) by using a separate command in the programming software menu.

Security Bit File Location

The object file created by compilation with Maple software is an Intel Intelec format, compatible file.

The programming algorithm defines the address scrambling that translates the file addresses to device addresses (the address that the device "sees" on its address pins during programming). By looking at a screen dump or a hard copy of the object file the user can determine the status of the security bit.

The security bit of the PSD301/311 resides in data bit #1 of file address 81D3h. This address contains three configuration bits that reside in data bits 0 – 2, so this address in the file can have any value between 0 and 7.

If this address has a value X1X (where X can be either 0 or 1), the security bit is off ('1' value means an unprogrammed bit) and CSECURITY = 0 (displayed by Mappro WSI programmer interface software as SECA = 0).

If this address has a value X0X, the security bit is on and CSECURITY = 1 (displayed by Mappro WSI programmer interface software as SECA = 1).

The security bit of PSD302/312 resides in data bit #1 of file address 10253h. This address contains three configuration bits that reside in data bits 0 – 3 (bit 3 is reserved for future usage). This address can have any value between 0 and F. If this address has a value XX1X (where X can be either 0 or 1), the security bit is OFF ('1' value means an unprogrammed bit) and CSECURITY = 0 (displayed by Mappro WSI programmer interface software as SECA = 0). If this address has a value XX0X, the security bit is ON and CSECURITY = 1 (displayed by Mappro WSI programmer interface software as SECA = 1).

If users do not want to look for the security bit status in the object file, they can call MAPPRO programming software from the main menu of MAPLE, Load the RAM with the object file and Display the ACR configuration bits status on the screen.

The value of SECA will indicate the status of the security bit (SECA = 0 means security is OFF, SECA = 1 means security is ON).

Summary

The PSD3XX family of programmable microcontroller peripheral devices provides security of design not readily available in conventional PLDs and EPROMs.

Though not entirely fool-proof, the security bit feature helps make it more cost effective for competitors to design their own hardware instead of trying to copy systems that already exist.

Programmable Peripheral Application Note 019

The PSD311 Simplifies an Eight Wire Cable Tester Design and Increases Flexibility in the Process

— By Timothy E. Dunavin, Antec – Anixter Mfg. and Karen S. Spesard, WSI

Abstract

With the ever increasing complexity of wiring networks and cables to match a wide variety of computer and telecommunication systems, a means of testing them becomes a necessity. The wire tester design described below is a simple yet effective design which uses the Motorola 68HC11 and WSI PSD311 pair to create a system that insures 8-wire cables are wired properly, and at the same time offers a substantial increase in design flexibility over alternative hardware solutions.

Introduction

More and more microcontroller and microprocessor designers are trying to design integrated core-based systems with the intention of being able to easily configure their systems to fit a wide variety of product applications. The problem is that when these applications require new or changing features such as expanding I/Os or address maps, they may find their designs are not flexible enough to accommodate the new requirements, forcing a lengthy and expensive redesign anyway.

A solution to this problem is to design in user-configurable programmable peripheral products which are flexible enough to accommodate future design revisions without the need for board relayout. The PSD3XX family from WSI, Inc., fits this profile exactly in that the products can be tailored to a specific application and then can be re-configured for other applications using the same core design. Also, the PSD3XX product family can enhance microcontroller-based systems in other ways. For instance, it can improve system integration resulting in lower system costs, and it can significantly shorten time to market resulting in increased revenues and profits.

In the cable tester system in which the PSD311 was used with the 68HC11, the PSD311 integrates address decoding, latches, 32K x 8 EPROM, and 2K x 8 SRAM all into a one-chip user-configurable microcontroller peripheral. It also replaces the two ports lost by the 68HC11 to extend program and data memory outside the MCU with two additional configurable 8-bit I/O ports, and adds a third 3-bit port, while easily enabling still further port expansion .

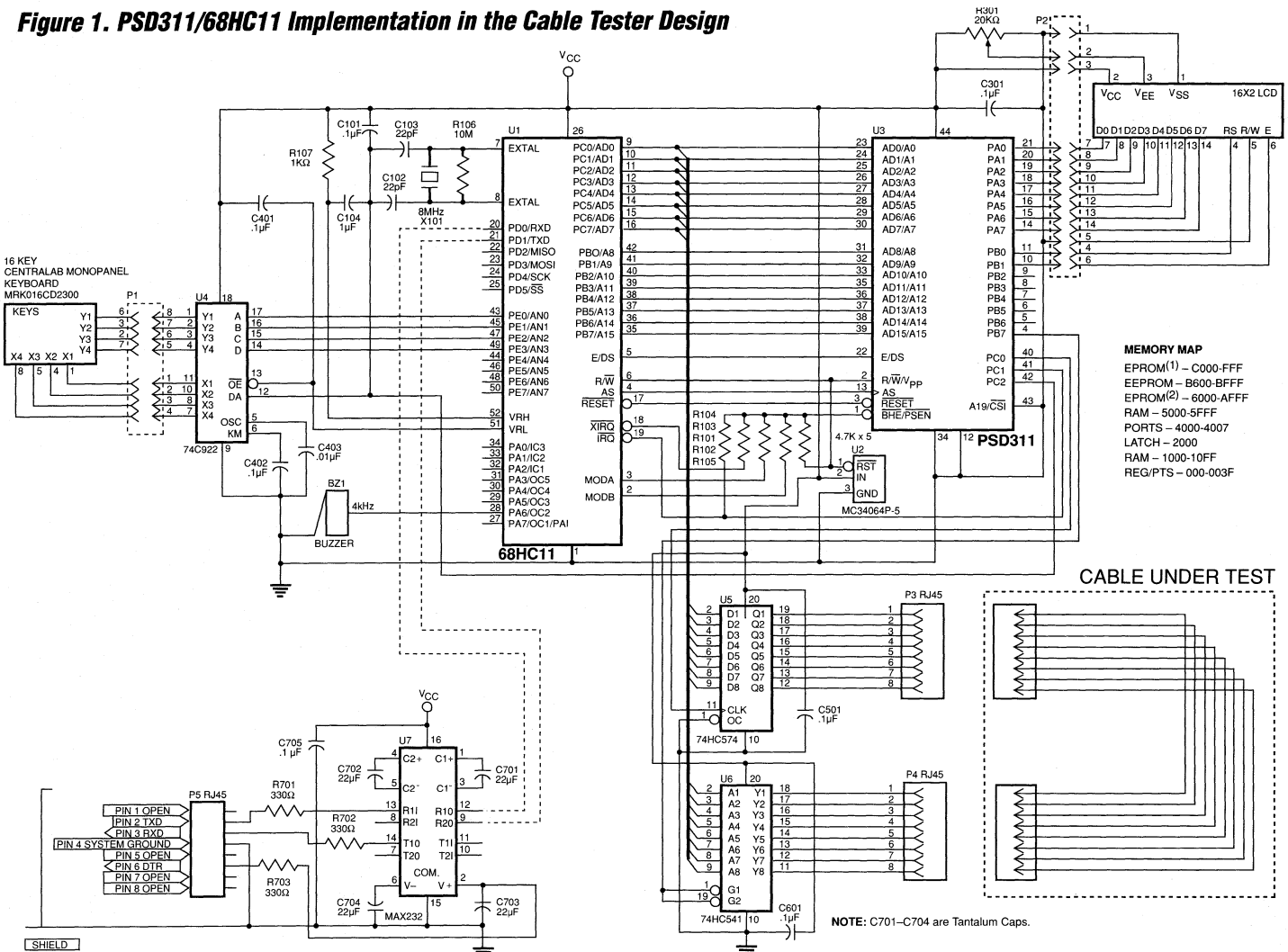
The Cable Tester System Design

The cable tester described below operates by sending a known bit pattern through the cable under test and checking the bit pattern at the other end. The hardware configuration utilized to achieve this function is shown in Figure 1.

Note that there are very few components overall in the design. The core contains just the 68HC11 microcontroller from Motorola, the PSD311 Programmable Peripheral with Memory from WSI and a few other key components including a keypad, LCD display, and an optional RS232 communications device.

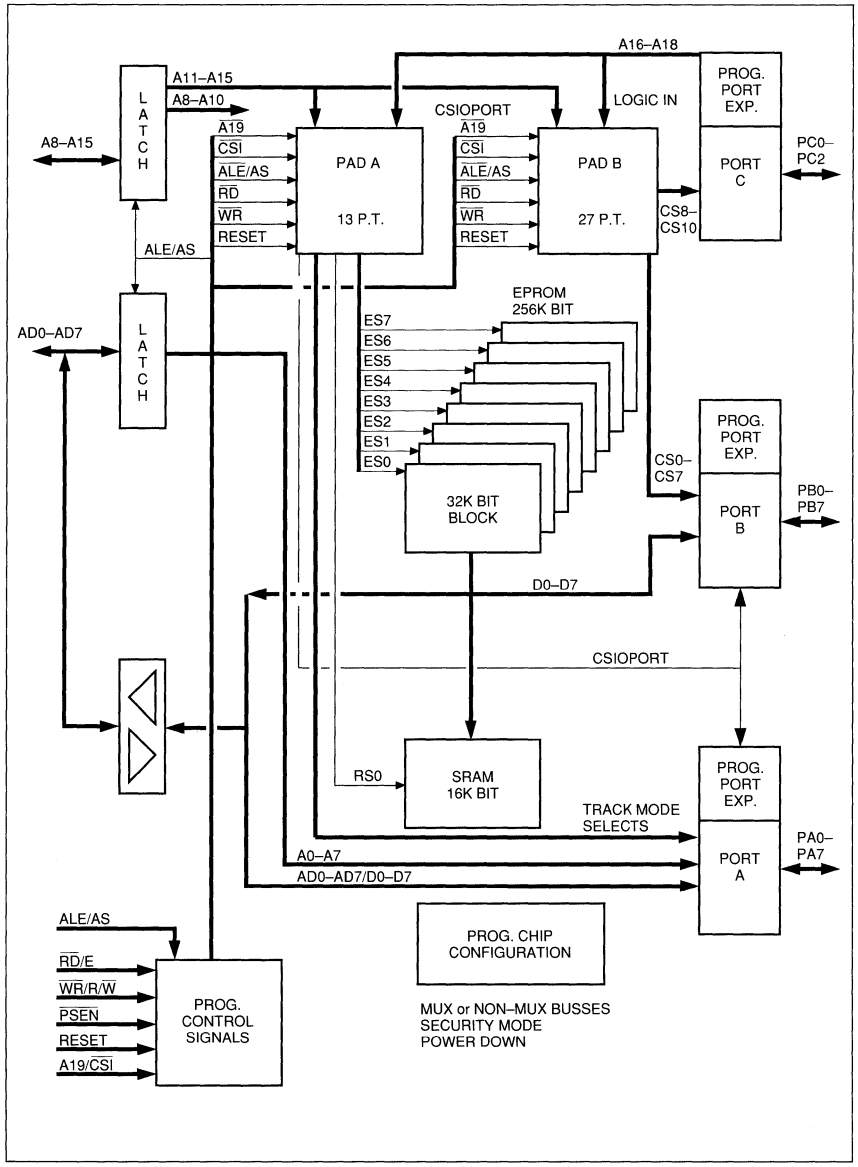
Also note that the interconnections between the 68HC11 and PSD311 are direct and require no "glue logic". That means that no external latches are needed to demultiplex the multiplexed address and data bus from the 68HC11. And, no other external logic is needed to generate the address mapping for the on-board EPROM and SRAM and to select external peripherals, or create the control signal interface. The PSD311 already incorporates these features internally, thereby simplifying the design considerably. In fact, the PSD311's architecture, as shown in Figure 2, specifically includes 32K x 8 mappable EPROM for program

Figure 1. PSD311/68HC11 Implementation in the Cable Tester Design



NOTE: C701–C704 are Tantalum Caps.

Figure 2. PSD311 Architecture



The Cable Tester System Design (Cont.)

storage, 2K x 8 mappable SRAM for data storage (or 16K x 16 EPROM and 1K x 16 SRAM, if using the similar PSD301 configured to interface to x16 micros) three highly configurable I/O ports, a programmable address decoder, and chip select logic.

In this design, the reconstructed port space of the PSD311 is used to add a keypad and an LCD display to the system, as well as additional output control and input lines with an 8-bit latch and an 8-bit buffer/line driver. Besides these components, the completed cable tester design also includes an undervoltage sensing circuit for generating a reset signal and an encoder for interfacing to the keypad.

Interfacing To The PSD311

Not only does the PSD311 interface to the 68HC11 simply and directly because of its internal latches and programmable control signals – as it does with any 8-bit microcontroller – it also facilitates easy interfacing to other components. (The PSD301 interfaces to any 8-or 16-bit microcontroller.) This is possible because of its three I/O ports and the Programmable Address Decoder (PAD) which offer unsurpassed flexibility. The PAD block diagram is shown in Figure 3.

For instance, the no "glue-logic" interface of the keypad in the system is accomplished by using a 74C922 encoder in conjunction with the PAD section of the PSD311. The PAD is useful because the Data Available (DA) line of the 74C922 is a logic "1" when a key is pressed, and the signal must be inverted before it reaches the /IRQ input of the 68HC11. Connecting the encoder's DA line to the PSD311's PC2 pin and configuring it to be a general-purpose logic input enables the signal to be inverted inside the PAD. The inverted signal is then "outputed" on PC1 which is configured as a chip select and routed to /IRQ. (See Port C Configuration and Chip Select Equation in Appendix A.) This simple internal manipulation inside the PSD311 helps reduce the number of components in the system. By connecting the 74C922 outputs directly to PE0-PE3 on the 68HC11, reading of the data is straightforward.

The display used in the system is a 16 character by 2 line dot matrix LCD module. The interface to the LCD display is handled by mapping the data bus directly to Port A of the PSD311, which is configured pin-by-pin to be general-purpose I/O. The control logic for the LCD is handled through two pins on Port B: PB0 and PB1, which are also configured to be general-purpose I/O. (See Ports A and B Configuration in Appendix A.) With the display used as a "WOM" (Write Only Memory), its R/$\overline{W}$ line is tied to ground to free an I/O pin of the PSD311 for other purposes. To free up Port A completely on the PSD311, an alternative approach would have been to connect the LCD directly to the 68HC11.

To expand the I/O capabilities of the system further, two port pins from the PSD311 are used with a 74HC574 and a 74HC541 to create 8 additional inputs and 8 additional latched outputs, both at the same address. (This is shown in Figure 1.) The PSD311's chip select outputs from ports B and C are derived from the addresses, DS strobe, and R/$\overline{W}$ signal available as inputs into the PAD. These chip selects will enable data to be latched to the outputs or enable input data onto the extended address/data bus from the outside world, imitating the capability of a PIA.

The chip select equation for the output latch, 74HC574, is decoded from the upper address byte, the DS/E signal, and the active low R/$\overline{W}$ signal as follows:

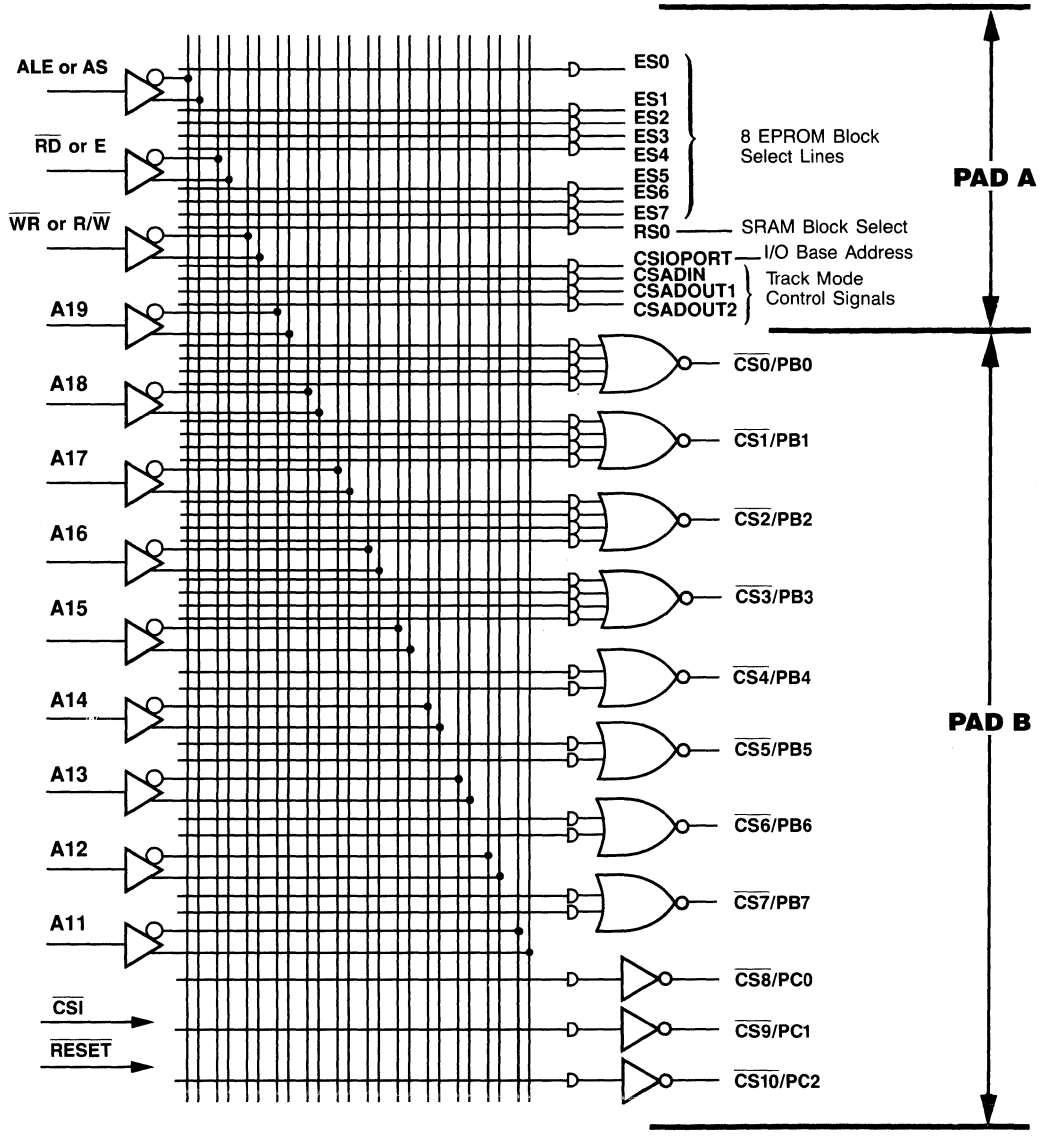
/CS8 = /A15 • /A14 • A13 • /A12 • DS • /R/$\overline{W}$.

The resulting latched address is $2000H with DS = 1 and R/$\overline{W}$ = 0. The chip select equation for the input driver, 74HC541, is the same, because the address is the same ($2000H), except that R/$\overline{W}$ is active high. So, this equation becomes:

/CS9 = /A15 • /A14 • A13 • /A12 • DS • R/$\overline{W}$.

The PSD311 simplifies the interface to the program and data memory, external peripherals, and I/O ports in the system by integrating the address decoder internally. This is illustrated with the direct interconnection between the microcontroller and other peripherals and the PSD311, without the need for a PLD or other logic.

Figure 3. Programmable Address Decoder Block Diagram



Interfacing To The PSD311 (Cont.)

The PAD enables the 8 blocks of 4K bytes EPROM (256K bits) to be located anywhere within the available address space – in this case, the address space of the 68HC11 is 64K bytes. So, the EPROM memory is split into two segments of 16K bytes EPROM each, separated by the 512 bytes of the internal E2PROM on the 68HC11. This means that the first 4 EPROM blocks are mapped contiguously, as well as the last 4 EPROM blocks. Here,the program memory (6000H-9FFFH: EPROM2, and C000H-FFFFH: EPROM1) is allocated to the upper portion of address space.

The data or SRAM memory, on the other hand, is allocated to the lower portion of address space and is partitioned into two segments: one segment containing the SRAM internal to the 68HC11 (256 bytes) and the other containing the SRAM internal to the PSD311 (2K bytes). The SRAM in the PSD311 is mapped via the address decoder to location 5000H-5FFFH, respectively.

Data direction and data registers of the PSD311's two ports are paired and accessed via an offset from a configurable I/O port mapped base address, such as 4000H in this cable tester design. This enables 16-bit data instructions to access the two I/O ports together, which in turn reduces both the Load and Store times during program execution.

Benefits of the PSD311 Usage in System

Board layout of the cable tester design was greatly simplified with the PSD311. In fact, when pin 1 of the PSD311 is oriented 180 degrees from pin 1 of the 68HC11 in the PLCC package, port B of the 68HC11 is directly across from the AD8-AD15 pins of the PSD311. This positioning enables close layout of the two parts, greatly reducing costs due to less board space.

Additional space is saved by using the latch and buffer for general-purpose I/O instead of the larger and more expensive PIA. And other I/O port lines are not sacrificed by using the multiplexed address/data bus instead of the Serial Peripheral Interface of the 68HC11.

In fact, board space is estimated to have been reduced by more than 50% over the alternative cumbersome design because of the PSD311 positioning on the PC board, its port expansion capabilities, and of course, the number of parts it replaces: including a 256K EPROM, a 16K SRAM, a latch, a decoder, and other miscellaneous CMOS logic.

A benefit of parts reduction is lower CMOS power consumption that results from an integrated single-chip CMOS peripheral/memory solution. By analyzing the power that would have been consumed with the alternative design and comparing that against the PSD311 solution, it was found that power was reduced by at least 30%. This translates into requiring a smaller power supply and a further reduction in cost.

The flexibility of the PSD311 in the cable tester design is also an advantage when design changes need to be made quickly. Since the I/O ports, PAD, control signals, and EPROM are all programmable, the part just needs to be reprogrammed when the configuration or program memory for the entire system needs modifying.

For instance, the current system has ten I/O, eleven input, and eleven output lines remaining. This can change if other variables need to be stored or other peripherals need to be accessed. To avoid relaying out another board to accommodate these changes, the PSD311 may be able to be reconfigured to easily handle them. Also, if more features and/or capabilities in EPROM are required, the PSD312 and PSD313 with 512Kbits (64K x 8) and 1Mbits (128K x 8) EPROM, respectively, are available in the same package and pinout.

The PSD311 also provides additional SRAM beyond the limited amount that may be on the microcontroller being used. This provides obvious benefits including more scratchpad RAM for such uses as storing cable "signatures" and system tests that can be downloaded for diagnostic purposes.

Benefits of the PSD311 Usage in System (Cont.)

But other benefits not readily seen are also important. For product designs that have a short life cycle and are "pushed" to go to market quickly, the additional SRAM gives the designer the option of writing the code in a high-level language such as "C", without the worry of running out of variable storage space. The capability of writing software in "C" could speed up the software development cycle, thereby reducing time-to-market!

Configuring and Programming the PSD311

All of the control logic, address mapping, and port configurations for the PSD311 are handled during device configuration as part of WSI's easy-to-use, menu-driven PSD MAPLE software program, which is included in the PSD-SILVER or PSD-GOLD software development package. See Appendix A for the PSD311 configuration used in this application.

After the configuration for the PSD311 has been determined and "Save"d, the hex file that is needed for programming the PSD311 is created. That is done during "Compile". "Compile" reads the code written for the microcontroller (in Intel hex format) and concatenates or merges it with the PSD311 configuration data to produce the desired output file for downloading to a programmer for programming.

That is all there is to programming the PSD311 which is now supported on industry-standard programmers like the Data I/O, BP Microsystems, Bytek, and Logical Devices programmers as well as the low-cost WSI MagicPro programmer.

2

The 68HC11/ PSD311 System Software

The software for the 68HC11 was written with a word processor and assembled using a cross assembler. A portion of the cable tester design code which is programmed into the PSD311 is listed in Appendix B. Here the register and RAM memory locations are set up within the first 64 clock cycles from reset of the 68HC11 and located at 0000H to enable easy Direct Addressing and Bit manipulations of often used registers.

Initialization of the Option Register, Timer prescaler, Stack and Serial Communications Interface complete the basic set up for the 68HC11 operation. Other initialization operations include: Ports A and B of the PSD311 which are set up as outputs for display control and data transfer operations, and the LCD display which is set up to display the first screen. Final initialization is achieved by setting several internal registers and clearing any pending interrupts. Now, the IRQ mask bit can be cleared and the main program loop entered.

Included in the code is a demonstration of some useful routines which will illustrate how to easily work with the Latch and Buffer expansion from the 68HC11/ PSD311. Remember that these extended addresses off the 68HC11 can be accessed in several ways. The example code shown uses the Bit Set and Bit Clear instructions in the indexed addressing mode. With these Bit Set and Bit Clear instructions, which are read-modify-write instructions, an additional register should be set up in the internal RAM, not on the latched (write-only) address, so the instructions will function properly. Data can then be manipulated and stored as a complete byte to the latch enabling data to be read and the current value in the latch to be checked. (Bit manipulation on the latched addresses using the indexed addressing mode will result in a correct bit change. However, the rest of the byte will be unusable as data on the bus will be scrambled at the rising edge of the chip select signal.) The latch and buffer expansion keeps software algorithms simple.

The 68HC11/ PSD311 System Software (Cont.)

Regarding the software for the keypad, no debounce software is necessary because the 74C922 has a built in debounce circuit. Actually, direct access from Port E to the keypad data and the AND instruction allows easy compare and execution of the correct routine.

The remaining subroutines in the program are straightforward and basic to most microcontrollers and microprocessors. Those used by the 68HC11 are found in previously published handbooks and articles which can be obtained through your local Motorola sales office.

Putting the System to Work

The 68HC11/PSD311 cable tester design could be expanded very easily with software to learn many different wiring configurations and to check several cables against a good one. Its usefulness can also be increased by making it battery operated for field use because of the low current draw of the tester.

The cable tester, as designed, will display the test results and step through the program to show the pin by pin connections of the cable. Results are then stored and later fed into a computer through the RS232 communications port of the tester.

Summary

Requirements for microcontroller-based designs are continually changing and to be able to adapt to these changes means being flexible. Of course, flexibility in hardware is sometimes hard to achieve, while flexibility in software is mostly a given. One of the goals of the PSD3XX family of products is to bridge the gap in flexibility between hardware and software.

By that, it is meant that hardware will not be a gating item when developing a new design that needs to be introduced to market quickly. And the PSD311, as illustrated in this cable tester design, addresses that issue perfectly by providing a user-configurable peripheral solution for hardware designers. So, if an application is modified and the I/O configuration changes, or design fixes are required, the P.C. board does not have to be re-engineered. The PSD3XX can just be reprogrammed to reflect the new changes.

The flexibility provided by the PSD311 solution in this design is crucial in that it enabled development to be completed quickly and successfully using a "core" approach which can handle many different cable applications, including applications for telephone interconnections, printers, and local area networks.

Appendix A. PSD311 Part Configuration Listed in .SV1 File

```
                              ALIASES
A16/CS8   = CS8
A17/CS9   = IRQ
A18/CS10 = DA
A19/CSI   = CSI
************************************************************************
                    GLOBAL CONFIGURATION

Address/Data Mode:                                    MX
Data Bus Size:                                        8
CSI/A19:                                              CSI
Reset Polarity:                                       LO
ALE Polarity:                                         HI
WRD/RWE:                                              RWE
A16-A19 Transparent or Latched by ALE:                T
Using different READ strobes for SRAM and EPROM:      N
************************************************************************
             PORT A CONFIGURATION (Address/IO)

 Bit No.      Ai/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          IO          CMOS
************************************************************************
                  PORT B CONFIGURATION

 Bit No.      CS/IO.      CMOS/OD.
    0          IO          CMOS
    1          IO          CMOS
    2          IO          CMOS
    3          IO          CMOS
    4          IO          CMOS
    5          IO          CMOS
    6          IO          CMOS
    7          CS7         CMOS

                CHIP SELECT EQUATIONS

/CS7 = /A15 * /A14 * A13 * /A12 *  E  *  R/W
   +
************************************************************************
                  PORT C CONFIGURATION

 Bit No.      CS/Ai.
    0          CS8
    1          CS9
    2          A18

                CHIP SELECT EQUATIONS

/CS8 = /A15 * /A14 * A13 * /A12 *  E  * / R/W
/IRQ = DA
************************************************************************
                    ADDRESS  MAP

      A  A  A  A  A  A  A  A  A  SEGMT   SEGMT  EPROM    EPROM   File Name
     19 18 17 16 15 14 13 12 11  STRT    STOP   START    STOP
ES0   N  X  N  N  0  1  1  0  N  6000    6FFF   6000     6fff    BASE301.OBJ
ES1   N  X  N  N  0  1  1  1  N  7000    7FFF
```

Appendix A. PSD311 Part Configuration Listed in .SV1 File (Cont.)

```
ES2   N  X  N  N  1  0  0  0  N  8000    8FFF

ES3   N  X  N  N  1  0  0  1  N  9000    9FFF

ES4   N  X  N  N  1  1  0  0  N  C000    CFFF   c000     cfff    BASE301.OBJ
ES5   N  X  N  N  1  1  0  1  N  D000    DFFF   d000     dfff    BASE301.OBJ
ES6   N  X  N  N  1  1  1  0  N  E000    EFFF   e000     efff    BASE301.OBJ
ES7   N  X  N  N  1  1  1  1  N  F000    FFFF   f000     ffff    BASE301.OBJ
RS0   N  X  N  N  0  1  0  1  0  5000    57FF

CSP   N  X  N  N  0  1  0  0  0  4000    47FF
****************************** END ***********************************
CDATA         = 0
CADDRDAT      = 1
CRRWR         = 1
CA19/(/CSI)   = 0
CALE          = 0
CRESET        = 0
COMB/SEP      = 0
CADDHLT       = 0

CPAF2         = 0

CPAF1 [0] = 0
CPAF1 [1] = 0
CPAF1 [2] = 0
CPAF1 [3] = 0
CPAF1 [4] = 0
CPAF1 [5] = 0
CPAF1 [6] = 0
CPAF1 [7] = 0

CPACOD [0] = 0
CPACOD [1] = 0
CPACOD [2] = 0
CPACOD [3] = 0
CPACOD [4] = 0
CPACOD [5] = 0
CPACOD [6] = 0
CPACOD [7] = 0

CPBF [0] = 1
CPBF [1] = 1
CPBF [2] = 1
CPBF [3] = 1
CPBF [4] = 1
CPBF [5] = 1
CPBF [6] = 1
CPBF [7] = 0

CPBCOD [0] = 0
CPBCOD [1] = 0
CPBCOD [2] = 0
CPBCOD [3] = 0
CPBCOD [4] = 0
CPBCOD [5] = 0
CPBCOD [6] = 0
CPBCOD [7] = 0

CPCF [0] = 1
CPCF [1] = 1
CPCF [2] = 0
```

Appendix B. Core System Software for Cable Tester Design


```
0000                    CPU     "6811.TBL"
0000                    HOF     "INT8"
                ;
                ;*********************************************************
                ;*      THE 68HC11 IN CONJUNCTION WITH THE PSD301          *
                ;*      ARE USED IN DEVELOPEMENT OF SOFTWARE FOR           *
                ;*      DISPLAY, KEYBOARD FUNCTION, AND OTHER APPL.        *
                ;*      MEMORY MAP:EPROM(1)   C000-FFFF (PROGRAM)          *
                ;*                 EEPROM     B600-BFFF (68HC11)           *
                ;*                 EPROM(2)   6000-9FFF (DATA)             *
                ;*                 RAM        5000-5FFF (PSD301)           *
                ;*                 I/O        4000-4007 (PSD301)           *
                ;*                 LAT        2000      (LATCH & BUFFER)   *
                ;*                 RAM        1000-10FF (68HC11)           *
                ;*                 I/O & REG  0000-003F (68HC11)           *
                ;*                                                         *
                ;*                    BY TIM DUNAVIN                       *
                ;*                      ANTEC                              *
                ;*                 ANIXTER MANUFACTURING                   *
                ;*********************************************************
                ;
6000                    ORG     06000H      ;DATA MEMORY
                ;
                ;***********************
                ;*    LOOKUP TABLES    *
                ;***********************
                ;
6000 3638484331DATTAB:  DFB     "68HC11/PSD311 UP",00H
                ;
6011 54494D4F54CREDITS: DFB     "TIMOTHY E. DUNAVIN"
6023 414E544543         DFB     "ANTEC - ANIXTER MFG."
6037 524F434B20         DFB     "ROCK FALLS, ILL. 61071"
                ;
                ;*********************************************************
                ;
C000                    ORG     0C000H      ;PROGRAM MEMORY
                ;
103D =          INIT:   EQU     103DH       ;RAM AND I/O MAPPING REGISTER
4000 =          PORTBC: EQU     04000H      ;I/O BASE ADDRESS OF THE 301
2000 =          LAT:    EQU     02000H      ;LATCH AND BUFFER
0000 =          KEY1:   EQU     00H         ;KEYPAD 1
0001 =          KEY2:   EQU     01H         ;KEYPAD 2
0002 =          KEY3:   EQU     02H         ;KEYPAD 3
0003 =          KEYA:   EQU     03H         ;KEYPAD A
0004 =          KEY4:   EQU     04H         ;KEYPAD 4
0005 =          KEY5:   EQU     05H         ;KEYPAD 5
0006 =          KEY6:   EQU     06H         ;KEYPAD 6
0007 =          KEYB:   EQU     07H         ;KEYPAD B
0008 =          KEY7:   EQU     08H         ;KEYPAD 7
0009 =          KEY8:   EQU     09H         ;KEYPAD 8
000A =          KEY9:   EQU     0AH         ;KEYPAD 9
000B =          KEYC:   EQU     0BH         ;KEYPAD C
000C =          KEYZ:   EQU     0CH         ;KEYPAD *
000D =          KEY0:   EQU     0DH         ;KEYPAD 0
000E =          KEYY:   EQU     0EH         ;KEYPAD #
000F =          KEYD:   EQU     0FH         ;KEYPAD D
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                ;***********************************************
                ;*       INITIALIZATION ROUTINE                *
                ;***********************************************
                ;
                ;NOTE: OPTION and TMSK2 must be programed in first 64 E
                ;      cycles out of RESET
                ;
C000 0F         START:   SEI                 ;SET IRQ MASK
C001 8610                LDAA    #010H      ;SET RAM AT 1000 AND
C003 B7103D              STAA    INIT       ;SET REGISTERS AT 0000
                ;***********************************************
                ;
                ;******* 64 BYTES OF REGISTER AREA *******
0000 =          PORTA:   EQU     0000H      ;PORT A DATA REGISTER
                ;                           ;0001 IS RESERVED
0002 =          PIOC:    EQU     0002H      ;PARALLEL I/O CONTROL REGISTER
0003 =          PORTC:   EQU     0003H      ;PORT C DATA REGISTER (AD0 - AD7)
0004 =          PORTB:   EQU     0004H      ;PORT B DATA REGISTER (A8 - A15)
0005 =          PORTCL:  EQU     0005H      ;PORT C LATCHED DATA REGISTER
                                            ;0006 IS RESERVED
0007 =          DDRC:    EQU     0007H      ;DATA DIRECTION REG FOR PORT C
0008 =          PORTD:   EQU     0008H      ;PORT D DATA REGISTER (RxD, TxD, AND I/O)
0009 =          DDRD:    EQU     0009H      ;DATA DIRECTION REG FOR PORT D
000A =          PORTE:   EQU     000AH      ;PORT E DATA REGISTER
000B =          CFORC:   EQU     000BH      ;TIMER COMPARE FORCE REGISTER
000C =          OC1M:    EQU     000CH      ;OUTPUT COMPARE 1 MASK REGISTER
000D =          OC1D:    EQU     000DH      ;OUTPUT COMPARE 1 DATA REGISTER
000E =          TCNT:    EQU     000EH      ;TIMER COUNTER REGISTER (16 BIT)
                                            ;000F LSB TCNT
0010 =          TIC1:    EQU     0010H      ;TIMER INPUT CAPTURE REGISTER 1 (16 BIT)
                                            ;0011 LSB TIC1
0012 =          TIC2:    EQU     0012H      ;TIMER INPUT CAPTURE REGISTER 2 (16 BIT)
                                            ;0013 LSB TIC2
0014 =          TIC3:    EQU     0014H      ;TIMER INPUT CAPTURE REGISTER 3 (16 BIT)
                                            ;0015 LSB TIC3
0016 =          TOC1:    EQU     0016H      ;TIMER OUTPUT COMPARE REG 1 (16 BIT)
                                            ;0017 LSB TOC1
0018 =          TOC2:    EQU     0018H      ;TIMER OUTPUT COMPARE REG 2 (16 BIT)
                                            ;0019 LSB TOC2
001A =          TOC3:    EQU     001AH      ;TIMER OUTPUT COMPARE REG 3 (16 BIT)
                                            ;001B LSB TOC3
001C =          TOC4:    EQU     001CH      ;TIMER OUTPUT COMPARE REG 4 (16 BIT)
                                            ;001D LSB TOC4
001E =          TOC5:    EQU     001EH      ;TIMER OUTPUT COMPARE REG 5 / INPUT CAPTURE
                                            ;REGISTER 4 (16 BIT) -  001F LSB TOC5/TIC4
0020 =          TCTL1:   EQU     0020H      ;TIMER CONTROL REGISTER 1
0021 =          TCTL2:   EQU     0021H      ;TIMER CONTROL REGISTER 2
0022 =          TMSK1:   EQU     0022H      ;MAIN TIMER INT MASK REGISTER 1
0023 =          TFLG1:   EQU     0023H      ;MAIN TIMER INT. FLAG REG 1
0024 =          TMSK2:   EQU     0024H      ;MAIN TIMER INT MASK REGISTER 2
0025 =          TFLG2:   EQU     0025H      ;MAIN TIMER INT. FLAG REG 2
0026 =          PACTL:   EQU     0026H      ;PULSE ACCUMULATOR CONTROL REG
0027 =          PACNT:   EQU     0027H      ;PULSE ACCUMULATOR COUNT REG
0028 =          SPCR:    EQU     0028H      ;SPI CONTROL REGISTER
0029 =          SPSR:    EQU     0029H      ;SPI STATUS REGISTER
002A =          SPDR:    EQU     002AH      ;SPI DATA REGISTER
002B =          BAUD:    EQU     002BH      ;SCI BAUD RATE CONTROL REGISTER
002C =          SCCR1:   EQU     002CH      ;SCI CONTROL REGISTER 1
002D =          SCCR2:   EQU     002DH      ;SCI CONTROL REGISTER 2
002E =          SCSR:    EQU     002EH      ;SCI STATUS REGISTER
002F =          SCDR:    EQU     002FH      ;SCI DATA REGISTER
0030 =          ADCTL:   EQU     0030H      ;A/D CONTROL/STATUS REGISTER
0031 =          ADR1:    EQU     0031H      ;A/D RESULT REGISTER 1
0032 =          ADR2:    EQU     0032H      ;A/D RESULT REGISTER 2
0033 =          ADR3:    EQU     0033H      ;A/D RESULT REGISTER 3
0034 =          ADR4:    EQU     0034H      ;A/D RESULT REGISTER 4
                                            ;0035 - 0038 RESERVED
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
0039 =          OPTION:  EQU     0039H       ;SYSTEM CONFIGURATION OPTIONS
003A =          COPRST:  EQU     003AH       ;ARM/RESET COP TIMER CIRCUITRY
003B =          PPROG:   EQU     003BH       ;EEPROM PROGRAMMING REGISTER
003C =          HPRIO:   EQU     003CH       ;HIGHEST PRIORITY INTERRUPT
                ;INIT:   EQU     003DH       ;RAM AND I/O MAPPING REGISTER (NEW ADD.)
003E =          TEST1:   EQU     003EH       ;FACTORY TEST REGISTER
003F =          CONFIG:  EQU     003FH       ;CONFIGURATION CONTROL REGISTER
                ;
                ;******* 256 BYTES OF INTERNAL RAM *******
1000 =          FLAGS:   EQU     1000H       ;FLAG REGISTER
1001 =          LA1:     EQU     1001H       ;LATCH DATA REGISTER
1002 =          STOR:    EQU     1002H       ;BASIC RAM STORAGE AREA
10FF =          STACK:   EQU     10FFH       ;STACK AREA
                ;
                ;******* 2K X 8 EXTERNAL RAM ********
5000 =          MASSTOR: EQU     05000H      ;MASS STORAGE RAM IN PSD301
                ;
                ;******* EEROM AREA, 512 BYTES *******
B600 =          EROM:    EQU     0B600H      ;DATA RETENTION AREA
                ;
                ;***********************************************
C006 01                  NOP                 ;SLIGHT DELAY TO ALLOW REGISTER SET UP
C007 86E3                LDAA    #0E3H       ;SET UP OPTION REG. - ADPU =1, CSEL = 1,
                                              IRQE = 1
C009 9739                STAA    OPTION      ;(ENABLE EEPROM CHARGE PUMP, IRQ EDGE
                                              SENSITIVE)
C00B 8602                LDAA    #002H       ;SET TIMER PRESCALER TO 8
C00D 9724                STAA    TMSK2       ;AND DISABLE TIMER INTERRUPTS
C00F 7F0028              CLR     SPCR        ;DISABLE ALL SPI INT.
C012 8E10FF              LDS     #STACK      ;SET UP STACK
C015 8680                LDAA    #080H
C017 9726                STAA    PACTL       ;PA7 OUTPUT
                ;******* INITIALIZE THE SCI TO 9600 BAUD AT 8MHZ (DISABLED)
C019 86FC       ONSCI:   LDAA    #0FCH       ;INIT. PORT D DDR (02H)
C01B 9709                STAA    DDRD        ;PD0, PD1 - INPUT, PD2-PD5 - OUTPUT
C01D 8600                LDAA    #000H       ;SET UP PORT D
C01F 9708                STAA    PORTD
C021 7F002C              CLR     SCCR1       ;SET UP SER. COM. CON. REG. 1
C024 7F002D              CLR     SCCR2
C027 962E                LDAA    SCSR        ;TO CLEAR TDRE AND TC OF SCSR
C029 4F                  CLRA                ;READ STATUS REG., LOAD TRANS. DATA REG.
C02A 972F                STAA    SCDR
                ;******* INITIALIZE THE 301 FOR DISPLAY INTERFACE
C02C CEFFFF     ONPIA:   LDX     #0FFFFH     ;SET UP PORTS B & C AS OUTPUTS
C02F FF4004              STX     PORTBC+4
                ;******* DISPLAY SET UP (NEW REV. 15 MAY 91) *******
C032 CE2710     DISINIT: LDX     #02710H     ;100mS DELAY (POWER UP DELAY FOR DISPLAY)
C035 BDC0E1              JSR     TDELAY      ;TIME DELAY
C038 8630                LDAA    #030H       ;SET UP DISPLAY
C03A BDC0F4              JSR     SENDI       ;SEND INSTRUCTION (30 1ST TIME)
C03D CE0300              LDX     #00300H     ;6.1mS DELAY
C040 BDC0E1              JSR     TDELAY      ;TIME DELAY
C043 BDC0F4              JSR     SENDI       ;SEND INSTRUCTION (30 2ND TIME)
C046 BDC0DE              JSR     TD40        ;TIME DELAY
C049 BDC0F4              JSR     SENDI       ;SEND INSTRUCTION (30 3RD TIME)
C04C BDC0DE              JSR     TD40        ;TIME DELAY
C04F 8638                LDAA    #038H       ;FUNCTION SET (8 BIT-SINGLE LINE)
C051 BDC0F4              JSR     SENDI       ;SEND INSTRUCTION
C054 CE0280              LDX     #00280H     ;5mS DELAY
C057 BDC0E1              JSR     TDELAY      ;TIME DELAY
C05A 860C                LDAA    #00CH       ;DISPLAY ON - NO CURSOR
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
C05C BDC0F4            JSR     SENDI        ;SEND INSTRUCTION
C05F CE0280            LDX     #00280H      ;5mS DELAY
C062 BDC0E1            JSR     TDELAY       ;TIME DELAY
C065 8606              LDAA    #006H        ;ENTRY MODE SET
C067 BDC0F4            JSR     SENDI        ;SEND INSTRUCTION
C06A CE0280            LDX     #00280H      ;5mS DELAY
C06D BDC0E1            JSR     TDELAY       ;TIME DELAY
C070 BDC0EC            JSR     HOME         ;DISPLAY CURSOR HOME!
C073 CE0190            LDX     #00190H      ;4.0mS DELAY
C076 BDC0E1            JSR     TDELAY       ;TIME DELAY
C079 18CE6000          LDY     #DATTAB      ;TOP OF DATA TABLE
C07D BDC0CC            JSR     PDOD         ;SEND MESSAGE TO DISPLAY
                ;******* FINAL INIT. *******
C080 9629       FINIT: LDAA    SPSR         ;CLEAR ANY SPI INT.
C082 962A              LDAA    SPDR
C084 86FF              LDAA    #0FFH        ;CLEAR ANY TIMER INT.
C086 9723              STAA    TFLG1
C088 9725              STAA    TFLG2
C08A 962E              LDAA    SCSR         ;CLEAR ANY SCI INT.
C08C 962F              LDAA    SCDR
                ;
                ;EXAMPLES OF WORKING WITH LATCH AND BUFFER
C08E 7F2000            CLR     LAT          ;CLEAR LATCH
C091 CE1001            LDX     #LA1         ;SET INDEX
C094 1C0200            BSET    2,X,00H      ;SET BIT 2 OF LA1
C097 A600              LDAA    0,X          ;GET LATCH REGISTER
C099 B72000            STAA    LAT          ;STORE DATA TO LATCH
C09C B62000            LDAA    LAT          ;GET DATA FROM BUFFER
                ;
C09F BDC0B0            JSR     BEEP         ;SOUND OFF!
                ;
C0A2 0E                CLI                  ;CLEAR IRQ MASK
                ;
                ;*************************
                ;*       MAIN LOOP       *
                ;*************************
                ;
C0A3 01         LOOP:  NOP
C0A4 7EC0A3            JMP     LOOP         ;RETURN
                ;
                ;***********************************
                ;*       SUBROUTINES               *
                ;***********************************
                ;
                ;******* WATCHDOG SERVICE ROUTINE ******
C0A7 8655       DOG:   LDAA    #055H        ;RESET WATCHDOG TIMER
C0A9 973A              STAA    COPRST
C0AB 86AA              LDAA    #0AAH
C0AD 973A              STAA    COPRST
C0AF 39                RTS                  ;RETURN FROM SUB.
                ;
                ;******* HOOTER OSC. ROUTINE ********
C0B0 18CE01FF   BEEP:  LDY     #001FFH      ;SET COUNT
C0B4 8640       BEEP1: LDAA    #040H        ;BEEPER ON
C0B6 9700              STAA    PORTA
C0B8 CE0014            LDX     #00014H
C0BB BDC0E1            JSR     TDELAY       ;DELAY
C0BE 4F                CLRA                 ;BEEPER OFF
C0BF 9700              STAA    PORTA
C0C1 CE0014            LDX     #00014H
C0C4 BDC0E1            JSR     TDELAY       ;DELAY
C0C7 1809              DEY                  ;COUNT -1
C0C9 26E9              BNE     BEEP1        ;IF NOT DONE, KEEP GOING
C0CB 39                RTS                  ;RETURN FROM SUB.
                ;
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                ;******* PUT DATA ON DISPLAY ********
C0CC 18A600     PDOD:   LDAA    0,Y             ;GET BYTE
C0CF 2707               BEQ     PDOD1           ;IF END, GOTO NEXT1
C0D1 BDC100             JSR     SENDD
C0D4 1808               INY                     ;NEXT BYTE
C0D6 20F4               BRA     PDOD            ;RETURN TO NEXT
C0D8 39         PDOD1:  RTS                     ;RETURN FROM SUB.
                ;
                ;******* TIME DELAY ROUTINE *********
C0D9 CE0002     TD20:   LDX     #00002H         ;20uS DELAY
C0DC 2003               BRA     TDELAY
C0DE CE000F     TD40:   LDX     #0000FH         ;150uS DELAY
C0E1 09         TDELAY: DEX                     ;DECRAMENT COUNT
C0E2 8C0000             CPX     #00000H         ;COUNT = 0?
C0E5 26FA               BNE     TDELAY          ;IF NOT DONE, GOTO TDELAY
C0E7 39                 RTS                     ;RETURN FRO SUB.
                ;
                ;******* CLEAR SCREEN, CURSOR HOME, AND SEND INSTRUCTION *******
C0E8 8601       CSCREEN: LDAA   #001H           ;CLEAR DISPLAY
C0EA 2008               BRA     SENDI           ;SEND INSTRUCTION
C0EC 8602       HOME:   LDAA    #002H           ;CURSOR HOME
C0EE 2004               BRA     SENDI           ;SEND INSTRUCTION
C0F0 86C0       LINE2:  LDAA    #0C0H           ;SET CURSOR TO LINE 2
C0F2 2000               BRA     SENDI           ;SEND INSTRUCTION
C0F4 CE4000     SENDI:  LDX     #PORTBC         ;SET UP DATA TRANSFER
C0F7 A706               STAA    6,X             ;STORE AT PIA PORT A
C0F9 1C0702             BSET    7,X,02H         ;DISPLAY E HIGH
C0FC 1D0702             BCLR    7,X,02H         ;DISPLAY E LOW
C0FF 39                 RTS                     ;RETURN FROM SUB.
                ;
                ;******* SEND DATA TO DISPLAY ********
C100 CE4000     SENDD:  LDX     #PORTBC         ;SET UP DATA TRANSFER
C103 A706               STAA    6,X             ;SEND DATA
C105 1C0701             BSET    7,X,01H         ;DISPLAY RS HIGH
C108 1C0702             BSET    7,X,02H         ;DISPLAY E HIGH
C10B 1D0702             BCLR    7,X,02H         ;DISPLAY E LOW
C10E 1D0701             BCLR    7,X,01H         ;DISPLAY RS LOW
C111 BDC0DE             JSR     TD40            ;150uS TIME DELAY
C114 39                 RTS                     ;RETURN FROM SUB.
                ;
                ;*************************************************
                ;*      ROUTINE TO CHANGE BYTE IN EEROM          *
                ;*      PRELOADED X = ADDRESS IN EEROM (B600 - B7FF) *
                ;*      DATA TO BE STORED, IS IN "STOR"          *
                ;*      (THIS IS A MOTOROLA ROUTINE)             *
                ;*************************************************
C115 A600       CHGBYT: LDAA    0,X             ;GET DATA AT ADDRESS TO BE CHANGED
C117 81FF               CMPA    #0FFH           ;CHECK IF ERASED
C119 2717               BEQ     CHGBYT1         ;JUMP IF BYTE ERASED
C11B 8616               LDAA    #016H           ;SET BYTE, ERASE, AND EELAT
C11D 973B               STAA    PPROG
C11F 86FF               LDAA    #0FFH
C121 A700               STAA    0,X
C123 8617               LDAA    #017H           ;SET EEPRG
C125 973B               STAA    PPROG
C127 3C                 PSHX                    ;SAVE X
C128 CE0300             LDX     #00300H
C12B BDC0E1             JSR     TDELAY          ;20mS TIME DELAY
C12E 38                 PULX                    ;RESTORE X
C12F 4F                 CLRA                    ;CLEAR BYTE, ERASE, EELAT, AND EEPRG
C130 973B               STAA    PPROG           ;END OF BYTE ERASE
C132 8602       CHGBYT1: LDAA   #002H           ;SET EELAT - DO BYTE PROGRAM
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
C134 973B              STAA    PPROG
C136 B61002            LDAA    STOR          ;GET DATA TO BE STORED
C139 A700              STAA    0,X           ;STORE IN NEW LOCATION IN EEROM
C13B 7C003B            INC     PPROG
C13E 3C                PSHX                  ;SAVE X
C13F CE0300            LDX     #00300H
C142 BDC0E1            JSR     TDELAY        ;20mS DELAY
C145 38                PULX                  ;RESTORE X
C146 7A003B            DEC     PPROG         ;CLEAR EEPRG
C149 7F003B            CLR     PPROG         ;CLEAR EELAT, END OF BYTE PROGRAM
C14C 39                RTS                   ;RETURN FROM SUB.
                ;
                ;*****************************************************
                ;*       ROUTINE TO SET UP A/D CONVERTER             *
                ;*       ACC A = VALUE TO INITIATE CONVERSION        *
                ;*       BEFORE ENTRY TO THIS ROUTINE                *
                ;*****************************************************
C14D 9730       CONV:   STAA    ADCTL         ;SET UP A/D CONVERTER
C14F 133080FC   CONV1:  BRCLR   ADCTL,80H,CONV1 ;WAIT HERE TILL CONVERSION COMPLETE
C153 39                 RTS                   ;RETURN FROM SUB.
                ;
                ;*****************************
                ;*    INTERRUPT ROUTINES     *
                ;*****************************
                ;
                ;*****************************************************
                ;*       SERIAL COMMUNICATIONS INTERFACE - IRQ       *
                ;*****************************************************
                ;
C154 3B         SCOM:   RTI                   ;RETURN FROM INT.
                ;
                ;*******************************
                ;*  SERIAL TRANSFER COMPLETE   *
                ;*******************************
                ;
C155 3B         TRANC:  RTI                   ;RETURN FROM INT.
                ;
                ;*********************************
                ;*  PULSE ACCUMLATOR INPUT EDGE  *
                ;*********************************
                ;
C156 3B         PULSEE: RTI                   ;RETURN FROM INT.
                ;
                ;*********************************
                ;*  PULSE ACCUMULATOR OVERFLOW   *
                ;*********************************
                ;
C157 3B         PULSEO: RTI                   ;RETURN FROM INT.
                ;
                ;********************
                ;*  TIMER OVERFLOW  *
                ;********************
                ;
C158 3B         TIMEO:  RTI                   ;RETURN FROM INT.
                ;
                ;*****************************
                ;*  TIMER OUTPUT COMPARE 5   *
                ;*****************************
                ;
C159 3B         COMP5:  RTI                   ;RETURN FROM INT.
                ;
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;****************************
                        ;*  TIMER OUTPUT COMPARE 4 *
                        ;****************************
                        ;
C15A 3B                 COMP4:   RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER OUTPUT COMPARE 3  *
                        ;****************************
                        ;
C15B 3B                 COMP3:   RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER OUTPUT COMPARE 2  *
                        ;****************************
                        ;
C15C 3B                 COMP2:   RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER OUTPUT COMPARE 1  *
                        ;****************************
                        ;
C15D 3B                 COMP1:   RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER INPUT COMPARE 3  *
                        ;****************************
                        ;
C15E 3B                 ICOMP3:  RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER INPUT COMPARE 2  *
                        ;****************************
                        ;
C15F 3B                 ICOMP2:  RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  TIMER INPUT COMPARE 1  *
                        ;****************************
                        ;
C160 3B                 ICOMP1:  RTI                ;RETURN FROM INT.
                        ;
                        ;****************************
                        ;*  REAL TIME INT. ROUTINE  *
                        ;****************************
                        ;
C161 3B                 REALT:   RTI                ;RETURN FROM INT.
                        ;
                        ;**********************
                        ;*  IRQ INT. ROUTINE  *
                        ;**********************
                        ;
C162 960A               DOIT:    LDAA    PORTE      ;GET KEYBOARD DATA
C164 840F                        ANDA    #00FH      ;FILTER DATA
                        ;
C166 8100                        CMPA    #KEY1      ;1 KEY?
C168 2601                        BNE     DOIT10     ;IF NOT GOTO DOIT10
C16A 3B                          RTI                ;RETURN FROM INT.
                        ;
C16B 8101               DOIT10:  CMPA    #KEY2      ;2 KEY?
C16D 2601                        BNE     DOIT20     ;IF NOT GOTO DOIT20
C16F 3B                          RTI                ;RETURN FROM INT.
```

Appendix B. Core System Software for Cable Tester Design (Cont.)

```
                        ;
C170 8102       DOIT20:  CMPA    #KEY3        ;3 KEY?
C172 2601                BNE     DOIT30       ;IF NOT, GOTO DOIT30
C174 3B                  RTI                  ;RETURN FROM INT.
                        ;
C175 8103       DOIT30:  CMPA    #KEYA        ;A KEY?
C177 2601                BNE     DOIT40       ;IF NOT GOTO DOIT40
C179 3B                  RTI                  ;RETURN FROM INT.
                        ;
C17A 8104       DOIT40:  CMPA    #KEY4        ;4 KEY?
C17C 2601                BNE     DOIT50       ;IF NOT GOTO DOIT50
C17E 3B                  RTI                  ;RETURN FROM INT.
                        ;
C17F 8105       DOIT50:  CMPA    #KEY5        ;5 KEY?
C181 2601                BNE     DOIT60       ;IF NOT GOTO DOIT60
C183 3B                  RTI                  ;RETURN FROM INT.
                        ;
C184 8106       DOIT60:  CMPA    #KEY6        ;6 KEY?
C186 2601                BNE     DOIT70       ;IF NOT GOTO DOIT70
C188 3B                  RTI                  ;RETURN FROM INT.
                        ;
C189 8107       DOIT70:  CMPA    #KEYB        ;B KEY?
C18B 2601                BNE     DOIT80       ;IF NOT GOTO DOIT80
C18D 3B                  RTI                  ;RETURN FROM INT.
                        ;
C18E 8108       DOIT80:  CMPA    #KEY7        ;7 KEY?
C190 2601                BNE     DOIT90       ;IF NOT GOTO DOIT90
C192 3B                  RTI                  ;RETURN FROM INT.
                        ;
C193 8109       DOIT90:  CMPA    #KEY8        ;8 KEY?
C195 2601                BNE     DOIT100      ;IF NOT GOTO DOIT100
C197 3B                  RTI                  ;RETURN FROM INT.
                        ;
C198 810A       DOIT100: CMPA    #KEY9        ;9 KEY?
C19A 2601                BNE     DOIT110      ;IF NOT GOTO DOIT110
C19C 3B                  RTI                  ;RETURN FROM INT.
                        ;
C19D 810B       DOIT110: CMPA    #KEYC        ;C KEY?
C19F 2601                BNE     DOIT120      ;IF NOT GOTO DOIT120
C1A1 3B                  RTI                  ;RETURN FROM INT.
                        ;
C1A2 810C       DOIT120: CMPA    #KEYZ        ;* KEY?
C1A4 2601                BNE     DOIT130      ;IF NOT GOTO DOIT130
C1A6 3B                  RTI                  ;RETURN FROM INT.
                        ;
C1A7 810D       DOIT130: CMPA    #KEY0        ;0 KEY?
C1A9 2601                BNE     DOIT140      ;IF NOT GOTO DOIT140
C1AB 3B                  RTI                  ;RETURN FROM INT.
                        ;
C1AC 810E       DOIT140: CMPA    #KEYY        ;# KEY?
C1AE 2601                BNE     DOIT150      ;IF NOT GOTO DOIT150
C1B0 3B                  RTI                  ;RETURN FROM INT.
                        ;
C1B1 810F       DOIT150: CMPA    #KEYD        ;D KEY?
C1B3 2600                BNE     DOIT160      ;IF NOT GOTO DOIT160
C1B5 3B         DOIT160: RTI                  ;RETURN FROM INT.
                        ;
                        ;*******************************
                        ;*  XIRQ SERVICE ROUTINE       *
                        ;*******************************
```

Appendix B. Core System Software for Cable Tester Design (Cont.)


```
C1B6 3B         NOMASK:  RTI                ;RETURN FROM INT.
                ;
                ;*******************************
                ;*  SWI SERVICE ROUTINE        *
                ;*******************************
C1B7 3B         INTER:   RTI                ;RETURN FROM INT.
                ;
                ;***********************************
                ;*  RESET AND INTERRUPT VECTORS    *
                ;***********************************
                ;
FFC0                     ORG    0FFC0H
                ;
FFC0            RES:     DFS    11*2        ;NOT USED
FFD6 C154       SERCOM:  DWM    SCOM        ;SERIAL COMM. INT.
FFD8 C155       SPISTC:  DWM    TRANC       ;SERIAL TRANSFER COMPLETE
FFDA C156       PAIE:    DWM    PULSEE      ;PULSE ACCUMLATOR INPUT EDGE
FFDC C157       PAOV:    DWM    PULSEO      ;PULSE ACCUMULATOR OVERFLOW
FFDE C158       TOV:     DWM    TIMEO       ;TIMER OVERFLOW
FFE0 C159       TOCP5:   DWM    COMP5       ;TIMER OUTPUT COMPARE 5
FFE2 C15A       TOCP4:   DWM    COMP4       ;TIMER OUTPUT COMPARE 4
FFE4 C15B       TOCP3:   DWM    COMP3       ;TIMER OUTPUT COMPARE 3
FFE6 C15C       TOCP2:   DWM    COMP2       ;TIMER OUTPUT COMPARE 2
FFE8 C15D       TOCP1:   DWM    COMP1       ;TIMER OUTPUT COMPARE 1
FFEA C15E       TICP3:   DWM    ICOMP3      ;TIMER INPUT COMPARE 3
FFEC C15F       TICP2:   DWM    ICOMP2      ;TIMER INPUT COMPARE 2
FFEE C160       TICP1:   DWM    ICOMP1      ;TIMER INPUT COMPARE 1
FFF0 C161       RTIME:   DWM    REALT       ;REAL-TIME INT.
FFF2 C162       IRQ:     DWM    DOIT        ;TIMER/VIA INT.
FFF4 C1B6       XIRQ:    DWM    NOMASK      ;NON-MASKABLE INT.
FFF6 C1B7       SWI:     DWM    INTER       ;SOFTWARE INT.
FFF8 C000       IOT:     DWM    START       ;ILLEGAL OPCODE TRAP (START OVER)
FFFA C000       COPS:    DWM    START       ;COP FAILURE (RESET)
FFFC C000       COPS1:   DWM    START       ;COP CLOCK MONITOR FAIL (RESET)
FFFE C000       RESET:   DWM    START       ;RESET
                ;
                ;************************************************
0000                     END                ;THE END!!!!!
```

Section Index

Programmable Peripheral

MAP168 Introduction

User-Configurable Peripheral with Memory

Overview

The MAP168 is a high-performance, user-configurable DSP peripheral with memory. It is used in DSP applications including modems, motor control and medical instrumentation. The MAP168 is ideal for DSP based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any DSP chip (TMS320 series, etc.) and the MAP168 work together to create a very powerful 2-piece chip-set. This implementation provides the core of the required control and peripheral elements of a DSP system.

The MAP168 contains three elements normally associated with discrete solutions to system memory requirements. It incorporates EPROM and SRAM plus a Programmable Address Decoder (PAD), all on the same die. The MAP168 is ideal for the systems designer who wishes to reduce the board space of his final design. By using the MAP168 in a system, five or six EPROM, SRAM and decode logic chips may be reduced into a single 44-pin PLDCC, CLDCC or PGA package.

Architecture

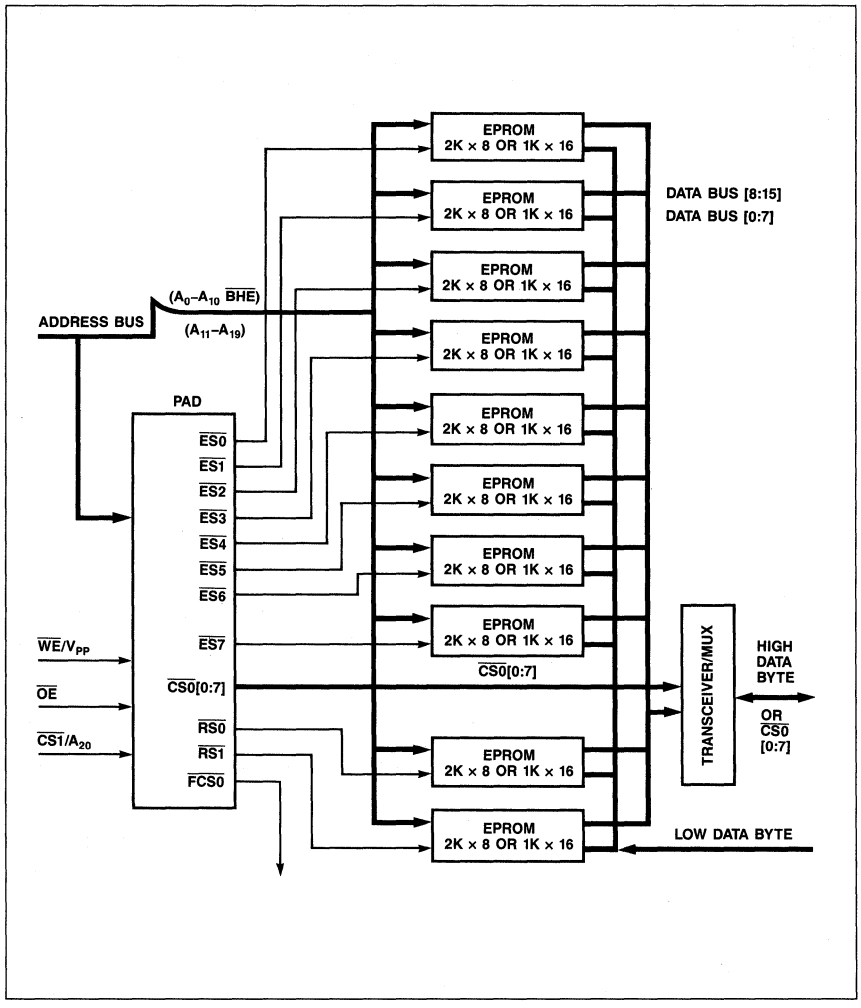
The MAP168 incorporates the flexibility of using discrete memory addressing and decoding. With the support of WSI's user friendly PSD software called MAPLE, designers may configure their MAP168 subsystem for 8- or 16-bit data paths. If the host system uses an 8051 microcontroller, the MAP168 can be programmed with an eight bit data path. A sixteen bit data path can be programmed for microcontrollers like Intel's 80196. The depth of the memory organization will be modified accordingly to accept the different dat path widths. The low cost MAPLE software package will handle the data path width adjustment automatically. The user can select either 16K bytes of EPROM and 4K bytes of SRAM or 8K words of EPROM and 2K words of SRAM. The flexibility of the MAP168 enables two devices to be cascaded in width. It is possible to double the memory size of a sixteen bit system by using two MAP168 products in parallel but programmed in a byte-wide configuration. For example, with two MAP168 devices, 16K words of EPROM and 4K words of SRAM may be organized as upper and lower data bytes of a 16 bit word. Alternately, two MAP168 chips may expand the system memory vertically as two word organized memory devices. A block diagram of the MAP168 is shown in Figure 1.

An important feature of the MAP168 is its ability to incorporate the memory address decoding on-chip. One MAP168 memory peripheral can reside with other MAP168 devices in the same memory addressing scheme, with the on-chip decoder allocating the memory blocks to different non-conflicting segments of the entire memory area. The decoding function is achieved by an on-chip feature called a Programmable Address Decoder (PAD), which is similar to a single fuse array programmable logic device supporting one product term (AND gate) per output in the MAP168.

In the MAP168, eighteen standard chip select outputs from the PAD are available with one fast chip select output generally used to select other external high speed memory devices. The chip select lines may be subdivided into ($\overline{ES0}$–$\overline{ES7}$, active low internal EPROM chip selects, and two internal RAM chip selects $\overline{RS0}$ and $\overline{RS1}$. In byte-wide applications, eight chip select outputs drive external pins $\overline{CS0}$–$\overline{CS7}$. These can be used as external chip selects for other MAP168 devices or system memory. These outputs are not available for word-wide MAP168 configurations because the $\overline{CS0}$–$\overline{CS7}$ output pins carry the higher order data byte. Only $\overline{FCS0}$ is available for external chip selection.

Figure 1 shows the organization of the EPROM and SRAM in relation to the PAD, for the MAP168 device.

Figure 1. MAP168 Memory Architecture



Important Features:

- 45 ns EPROM/SRAM Access Time.
- Byte or Word Operation, Mappable into 1M Word or 2M Byte Address Space.
- 22 ns Chip-Select 8 Outputs, 17 ns Fast Chip Select Output.
- 128K EPROM Bits, 32K SRAM Bits, On-Chip Programmable Decoder, Security Bit.

Software Support

The object code generated for the support microprocessor/microcontroller is generated by an assembler. This code, when generated as an Intel MCS file, may be easily programmed into the EPROM section of the MAP168 device because the MAPLE software has been designed to accept this standard format.

The programmable address decoder is used to define the mapping of the various EPROM and SRAM memory blocks. This mapping is achieved by the designer in the MAPLE environment. The software provides a safeguard that prevents the designer from inadvertently overlapping the address selection. After selecting the memory block assignments, the MAP168 device may be programmed by the WSI MagicPro™ memory and PSD programmer.

Programmable Peripheral
MAP168
DSP Peripheral with Memory

Features

- First-generation Programmable System Device (PSD)
  - User-Configurable Peripheral with Memory
  - 16Kx8 EPROM
  - 4Kx8 SRAM
  - Programmable address decoder
- Byte or Word Memory Configurations
  - 16Kx8 or 8Kx16 EPROM
  - 4Kx8 or 2Kx16 SRAM
  - 2Mbyte or 1 Mword address range
- High-Speed Operation
  - 45-nsec memory access
  - 17-nsec fast chip select output
- External Chip Select Outputs
  - 8 external chip selects
  - 1 fast chip-select output
- Programmable Security
  - Protects memory map
  - Protects program code
- Programming Support Tools
  - PSD integrated software environment
  - PC-XT/AT/PS2 platform support
  - MAPLE location entry Software
  - MAPPRO device programming Software
  - MagicPro device programmer (PC-XT, AT)
- Military and Commercial Specifications
  - 44-pin Ceramic Leaded Chip Carrier package
  - 44-pin Plastic Leaded Chip Carrier package
  - 44-pad Ceramic Leadless Chip Carrier package
  - 44-pin Ceramic Pin Grid Array package

3

General Description

In 1988 WSI introduced a new concept in programmable VLSI, Programmable System Devices (PSD). The PSD family consists of user-configurable system-level building blocks on-a-chip, enabling quick implementation of application-specific controllers and peripherals. The first generation PSD series includes the MAP168 User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The MAP168 is the first of WSI's Programmable System Devices (PSD) product line. The device integrates high performance, user-configurable blocks of EPROM, SRAM, and logic in a single circuit. The major functional blocks include a Programmable Address Decoder (PAD), 16K bytes of high speed EPROM, and 4K bytes of high speed SRAM. A block diagram is given in Figure 1.

The MAP168 device is a complete memory subsystem that can be mapped anywhere in a 2M-byte address space of a microprocessor or microcontroller system. The EPROM and SRAM memory blocks can be user-configured in either byte-wide or word-wide organizations. The MAP168 device significantly reduces the board space and power necessary to implement memory subsystems, increases system performance, and provides for secure data or program storage.

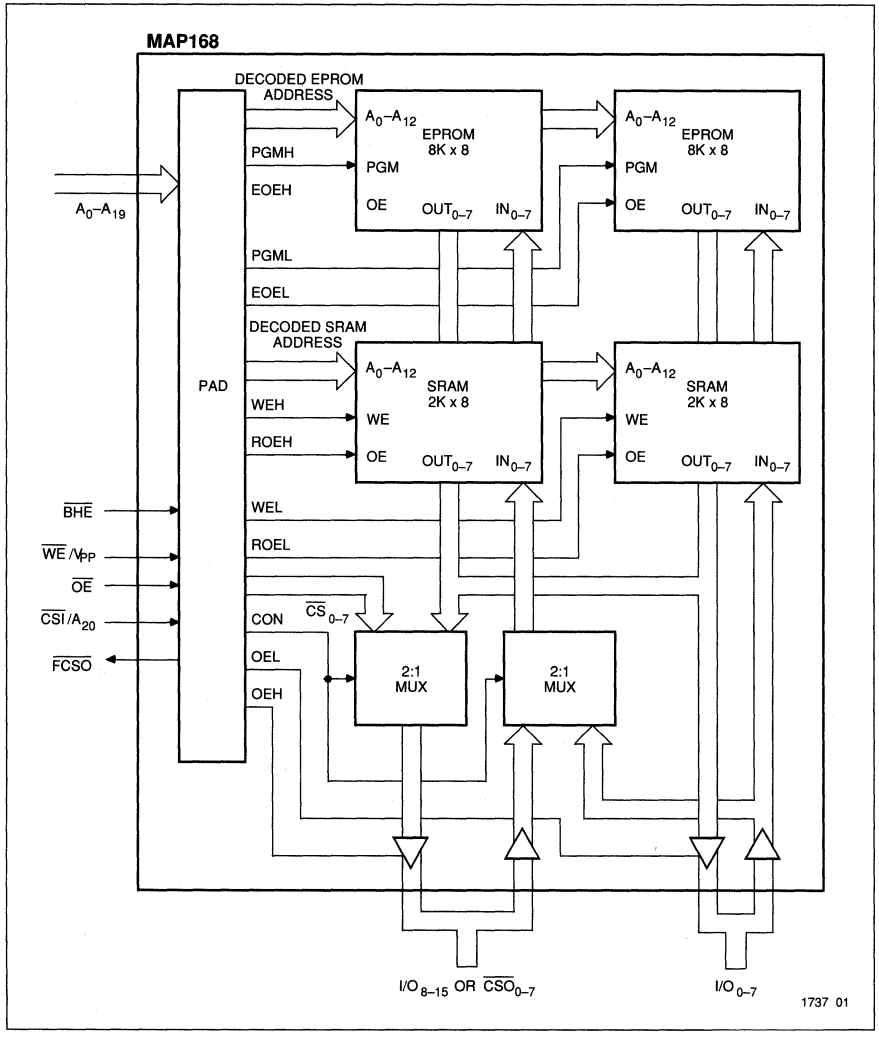
The device's high level of integration and flexibility make it ideal for high-speed microprocessors, microcontrollers, and Digital Signal Processors like the TMS320XX family. The EPROM can be configured either as 16Kx8 or 8Kx16. The SRAM can be configured either as 4Kx8 or 2Kx16. Individual memory blocks of 2Kx8 or 1Kx16 can be selectively mapped anywhere in the address space. Since the Chip Select Input ($\overline{CSI}$) can be programmed as A20, the highest-order address bit, the device's address range can extend from 1M byte with $\overline{CSI}$ to 2M byte without $\overline{CSI}$.

For 16-bit microprocessors capable of byte operations, the MAP168 device provides a Byte High Enable input for accessing bytes on any address boundary.

Pinout is compatible with the JEDEC WS27C257 256K high-speed EPROM. This pinout provides for memory expansion with future WSI EPROM and PSD products.

The device's PAD and EPROM memory are

Figure 1.
Block Diagram



General Description (Con't)

programmed using the same WSI MagicPro programmer used to program other WSI devices. Two software packages, MAPLE Location Entry and MAPPRO Device Programming Software are available in the menu-driven WISPER software environment on an IBM® PC XT/AT or 100% compatible platform.

For additional information on the MAP168 device, refer to *Application Note No. 002, Introduction to the MAP168 User-Configurable Peripheral with Memory*. For additional information on development and programming software for the MAP168 device, refer to the *MAP168 User-Configurable Peripheral with Memory Software User's Manual.*

Functional Description

The user-configurable architecture of the MAP168 consists of an EPROM memory block, an SRAM memory block, and a fast Programmable Address Decoder (PAD) that can be configured to select 2K-byte memory blocks anywhere in a 2M-byte address range. The device can be programmed to operate with memory configured either in a byte or word organization (bytes can be addressed in word mode). A programmable security bit prevents access to the PAD address-decode configuration table.

Table 1. Pin Description

Signal	I/O	Description
A_{0-19}	I	*Address Lines.* For access to EPROM or SRAM.
$\overline{FCSO}$	O	*Fast Chip-Select Output (active low).* Used by the Programmable Address Decoder (PAD).
$\overline{BHE}$	I	*Byte High Enable (active low).* Selects the high-order byte when writing to SRAM.
$\overline{WE}/V_{pp}$	I	*Write Enable (active low) or Programming Voltage.* In normal mode, this pin causes data on the I/O pins to be written into SRAM. In programming mode, the pin supplies the programming voltage, V_{pp}.
$\overline{OE}$	I	*Output Enable (active low).* Enable the I/O pins to drive the external bus.
$\overline{CSI}/A_{20}$	I	*Chip Select Input (active low) or High-Order Address.* This pin can be programmed as the bus-access chip select or as an additional high-order address bit (A_{20}).
I/O_{0-7}	I/O	*Low-Order Byte of EPROM or SRAM.*
$I/O_{8-15,}$ $\overline{CSO}_{0-7}$	I/O	*High-Order Byte or Chip-Select Outputs.* In word mode, these pins serve as the high-order byte ($I/O_{8-15,}$) of EPROM or SRAM. In byte mode, the bits serve as Chip-Select Out signals ($\overline{CSO}_{0-7}$) for the Programmable Address Decoder (PAD).

Programmable Address Decoder

The MAP168 device has a minimum of 20 address inputs A_0–A_{19} allowing the EPROM and SRAM memory blocks to reside anywhere in a 1M-byte address space. If the $\overline{CSI}/A_{20}$ input is user-configured as an address line, the maximum addressable space increases to 2M bytes, as shown in the Configurations table.

The 16K bytes of EPROM and 4K bytes of SRAM, can be configured into eight independent 2K-byte blocks and two 2K-byte blocks respectively, as shown in the Memory Architecture figure. The PAD is a user-configurable address decoder that compares input addresses to the 2K-byte address range selected for each of the eight EPROM blocks and two SRAM blocks. When the input address A_0–A_{20} is detected to be within one of the EPROM or SRAM address ranges, the PAD enables an internal chip select (ES_0–ES_7 or RS_0–RS_1) to the selected block. If no block is selected, both the EPROM and SRAM memories remain in a power-down mode and the outputs are disabled allowing other devices to drive the data bus. The SRAM retains its data in the power-down mode. The 2K-byte address ranges for any of the eight EPROM or two SRAM blocks may not overlap.

The PAD can also be user-configured to generate up to eight external chip selects, $\overline{CS_0}$–$\overline{CS_7}$. These outputs can be used to decode the input address lines A_0–A_{20} and to select other devices in the system. The outputs $\overline{CS_0}$–$\overline{CS_7}$ are available on the eight higher-order I/O_8–I/O_{15} lines but only when the MAP168 device is configured in the byte mode; the lines are not available as chip-select outputs when the device is configured in the word mode.

The $\overline{CSI}/A_{20}$ input is user-configurable as the most-significant address line or as an active-low chip enable. Its function is programmed as part of the PAD programming cycle.

The PAD also provides $\overline{FSCO}$, a single, fast chip-select output configurable by the user for any address. It can overlap with any of the internal EPROM, SRAM or external $\overline{CSO}$ addresses.

Memory Subsystem

EPROM Memory

The memory configuration of the MAP168 device includes 128K bits of WSI's patented high-speed, split-gate, UV-erasable EPROM. The EPROM is configured in byte mode as 16Kx8 and in word mode as 8Kx16. The memory is organized as eight 2Kx8 or 1Kx16 blocks, as shown in the Block Diagram figure. Each block has a separate and independent address range that cannot overlap. Each block is individually selected by one of the ES_0–ES_7 internal chip selects generated by the PAD when an input address is detected within its designated address range, as shown in the Memory Architecture figure. If not selected, each block of EPROM remains in a power-down mode.

For programming, the EPROM memory requires the $\overline{WE}/V_{PP}$ input to maintain the programming voltage V_{PP}.

SRAM Memory

The device also includes 32K bits of high-speed SRAM. The SRAM is configured in byte mode as 4Kx8 and in word mode as 2Kx16. The memory is organized as two 2Kx8 or one 2Kx16 block(s), each with a separate and independent address range that cannot overlap. Each SRAM block is individually selected by one of the RS_0–RS_1, shown in the Memory Architecture figure, when an input address is detected by the PAD within its designated address range. When not selected, each of the SRAM memory blocks remains in a power down mode but does retain all data stored.

Data can be written into the SRAM only when the $\overline{WE}/V_{PP}$ input is active low.

Memory Subsystem EPROM Memory (Con't)

Byte/Word Mode

The PAD can be programmed to configure the MAP168 device for either a byte or word memory architecture. This allows the device to be used conveniently with either 8-bit or 16-bit microcontrollers, microprocessors or digital signal processor (DSP) systems. See the Configurations table.

In byte mode, the EPROM is organized as 16Kx8 and the SRAM as 4Kx8. The outputs of both are tied to the eight low-order input/output lines I/O_0–I/O_7 and enabled onto the output bus when the $\overline{OE}$ input is low.

Only when configured in byte mode are the eight external chip selects provided by the PAD available on the eight high-order input/output lines I/O_8–I/O_{15} and enabled onto the output bus when the $\overline{OE}$ input is low.

In word mode, the EPROM is organized as 8Kx16 and the SRAM as 2Kx16. The outputs of both are tied to the 16 input/output lines I/O_0–I/O_{15} and enabled onto the bus when $\overline{OE}$ is low.

In word mode, the $\overline{BHE}$ input along with address input A0 allows the eight bits of any 16-bit word on an even or odd boundary to be selected as shown in the High-Low Byte Selection table. This is a useful feature for 16-bit processors that are not restricted to reading or writing memory only on even-word address boundaries.

Mode Selection

The device's operational mode is controlled by three inputs, $\overline{CSI}$, $\overline{OE}$, and $\overline{WE}/V_{PP}$. There are ten separate modes of operation, all of which are shown the Mode Selection table.

Table 2. Configurations

	x8 Configuration		x16 Configuration	
	$\overline{CSI}$	A_{20}	$\overline{CSI}$	A_{20}
Address Space words	1M bytes	2M bytes	512K words	1M
Block Size words	2K bytes	2K bytes	1K words	1K
Addressable Blocks	512	1024	512	1024
EPROM Blocks	8	8	8	8
SRAM Blocks	2	2	2	2
Chip-Select Outputs	9	9	1	1
EPROM Configuration	16Kx8	16Kx8	8Kx16	8Kx16
SRAM Configuration	4Kx8	4Kx8	2Kx16	2Kx16
I/O Pins	8	8	16	16
Low-power Standby	yes	no	yes	no
Protected Mode	yes	yes	yes	yes
Byte Operations	yes	yes	yes	yes

Table 3. Mode Selection

Mode/Pin	$\overline{CSI}$	$\overline{OE}$	$\overline{WE}/V_{pp}$	Address	x16 (I/O_{0-15}) x8 (I/O_{0-7})	x16 ($\overline{FCSO}$) x8 $\overline{FCSO}$, $\overline{CSO}_{0-7}$
Read EPROM/SRAM	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Selected	D_{OUT}	CS_{OUT}
Read External	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Not Selected	High Z	CS_{OUT}
Output Disable	X	V_{IH}	X	X	High Z	CS_{OUT}
Stand-By	V_{IH}	X	X	X	High Z	CS_{OUT}
Write SRAM	V_{IL}	X	V_{IL}	SRAM Selected	D_{IN}	CS_{OUT}
Write External	V_{IL}	X	V_{IL}	No SRAM Selected	X	CS_{OUT}
Program EPROM	V_{IL}	V_{IH}	V_{PP}	EPROM Program Address	D_{IN}	D_{IN}
Program Verify EPROM	V_{IL}	V_{IL}	V_{IH}	EPROM Program Address	D_{OUT}	CS_{OUT}
Program PAD	V_{IL}	V_{IH}	V_{PP}	PAD Program Address	D_{IN}	D_{IN}
Program Verify PAD	V_{IL}	V_{IL}	V_{IH}	PAD Program Address	D_{OUT}	CS_{OUT}

Table 4. High/Low Byte Selection

x16 Configuration Only

$\overline{BHE}$ (Pin 1)	A_0	Write Operation	Read Operation
0	0	Whole word	Whole word
0	1	Upper byte from/to odd address	Upper byte = Data Out Lower byte = 'FF'
1	0	Lower byte from/to even address	Whole word
1	1	None	Upper byte = Data Out Lower byte = 'FF'

$\overline{WR}$ and $\overline{BHE}$ are used for SRAM functions

Table 5. Product Selection Guide

Parameter	MAP168-45	MAP168-55	Units
Address Access Time (max)	45	55	ns
Chip-Select Access Time (max)	45	55	ns
Output Enable Time (max)	21	23	ns
Chip-Select Output Time	25	27	ns
Fast Chip-Select Output Time (max)	20	22	ns

Table 6. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Units
Output Low Voltage	V_{OL}	I_{OL}=8 mA		0.5	V
Output High Voltage	V_{OH}	I_{OH}=–2 mA	2.4		V
CMOS Standby Current	I_{SB1}	notes 1, 3			
—Commercial				25	mA
—Military				35	mA
TTL Standby Current	I_{SB2}	notes 2, 3			
—Commercial				35	mA
—Military				45	mA
CMOS Active Current No Blocks Selected	I_{CC} 1A	notes 1, 4			
—Commercial				25	mA
—Military				35	mA
CMOS Active Current EPROM Block Selected	I_{CC} 1B	notes 1, 4			
—Commercial				40	mA
—Military				50	mA
CMOS Active Current SRAM Block Selected	I_{CC} 1C	notes 1, 4			
—Commercial				80	mA
—Military				90	mA
TTL Active Current No Blocks Selected	I_{CC} 2A	notes 2, 4			
—Commercial				35	mA
—Military				45	mA
TTL Active Current EPROM Block Selected	I_{CC} 2B	notes 2, 4			
—Commercial				45	mA
—Military				55	mA
TTL Active Current SRAM Block Selected	I_{CC} 2C	notes 2, 4			
—Commercial				90	mA
—Military				100	mA
Input Load Current	I_{LI}	V_{IN}=5.5V or GND	–10	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=5.5V or GND	–10	10	µA

Notes:
1. CMOS inputs: GND ± 0.3V or VCC ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1.5 mA/MHz for AC power component.
4. Add 3.5 mA/MHz for AC power component.

Table 7. AC Characteristics

Parameter	Symbol	MAP168-45 Min	MAP168-45 Max	MAP168-55 Min	MAP168-55 Max	Units
Read Cycle Time	t_{RC}	45		55		ns
Address to Output Delay	t_{ACC}		45		55	ns
$\overline{CSI}$ to Output Delay	t_{CE}		45		55	ns
$\overline{OE}$ to Output Delay	t_{OE}		21		23	ns
Output Disable to Output Float	t_{OEF}		18		20	ns
Chip Disable to Output Float	t_{CSF}		18		20	ns
Address to Output Hold	t_{OH}	10		10		ns
Address to $\overline{CSO}_{0-7}$ True	t_{CSO}		25		27	ns
Address to $\overline{FCSO}$ True	t_{FCSO}		20		22	ns
SRAM Write Cycle Time	t_{WC}	45		55		ns
Chip Enable to Write End	t_{CSW}	45		55		ns
Address Setup Time	t_{AS}	0		0		ns
Address Hold Time	t_{AH}	0		0		ns
Address Valid to Write End	t_{AW}	45		55		ns
SRAM Write Enable Pulse Width	t_{PWE}	30		35		ns
Data Setup Time	t_{DS}	20		30		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Data Float	t_{WEF}		21		23	ns
Write Disable to Data Low Z	t_{WELZ}	3		3		ns
$\overline{BHE}$ Setup Time	t_{BHES}	0		0		ns
$\overline{BHE}$ Hold Time	t_{BHEH}	10		10		ns

Table 8. Data Retention Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Units
Minimum V_{CC} for Data Retention	V_{DR}	V_{CC}=2.0V,	2.0		V
Current in Data Retention Mode	I_{CCDR}	$\overline{CSI} \geq V_{CC}$–0.2V,		1	mA
Chip Deselect to Data Retention	t_{CSDR}	$V_{IN} \geq V_{CC}$–0.2V	0		ns
Recovery Time from Data Retention	t_{RDR}	or $V_{IN} \leq 0.2V$	t_{RC}		ns

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Voltage to any pin with respect to GND	−0.6V to +7V
V_{PP} with respect to GND	−0.6 V to +14.0V
ESD Protection	>2000V

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 9. Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

Figure 3. Read Cycle Timing Diagram

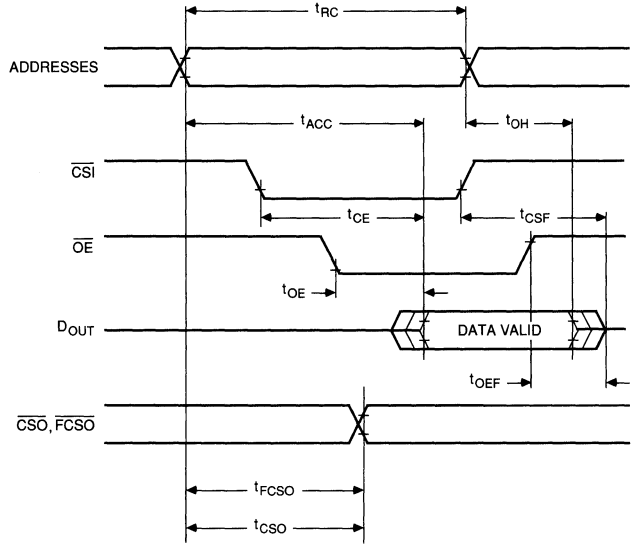
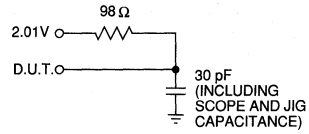


Figure 4. Test Load



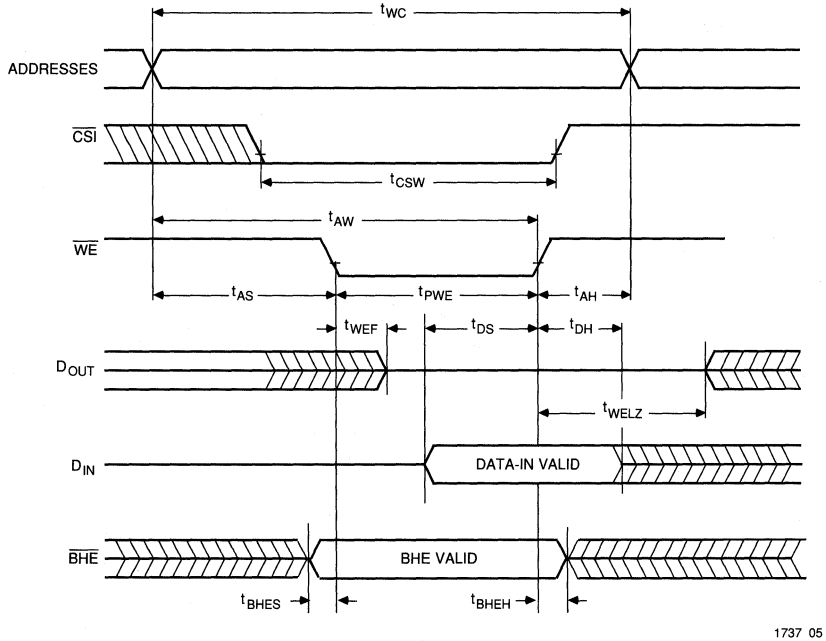
High-impedance test systems

1737 04

Table 10. Timing Levels

Level	Voltage
Input	0 and 3V
Reference	1.5V

Figure 5. Write Cycle Timing Diagram



1737 05

Figure 6. Memory Architecture

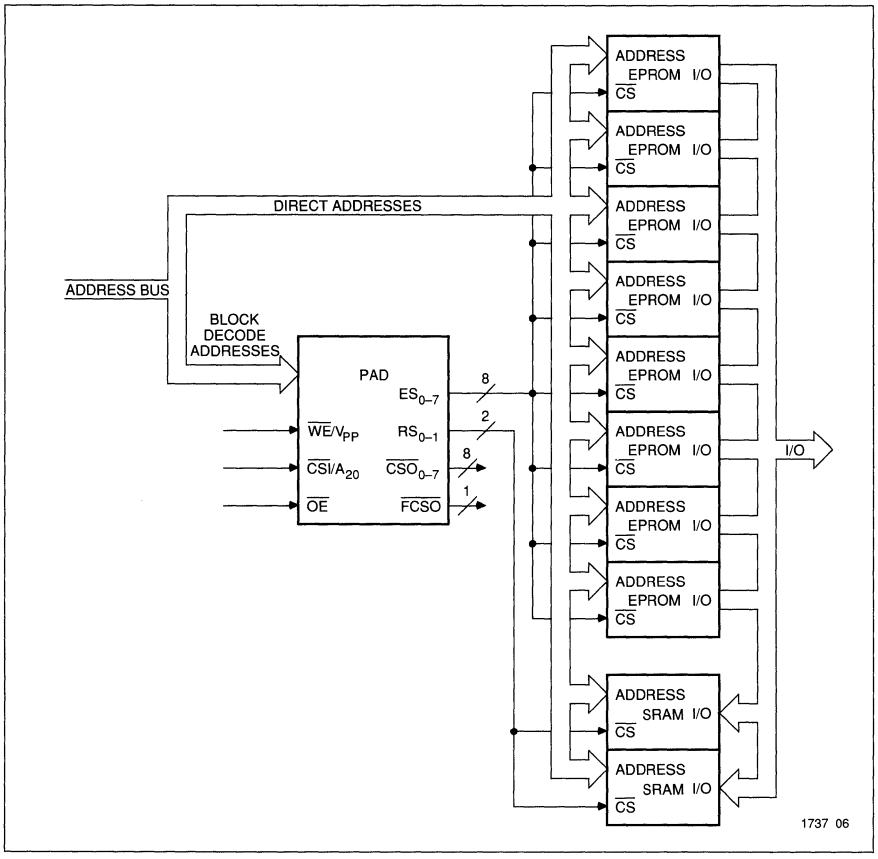


Table 11. MAP168 Pin Assignments

44-pin CLDCC Package
44-pin PLDCC Package
44-pad CLLCC Package

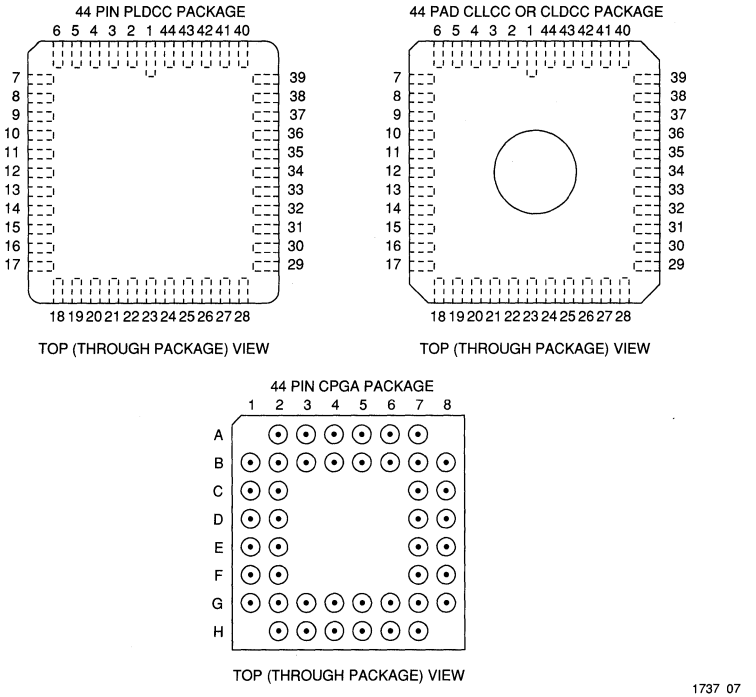
Pin No.	x8	x16
1	GND	$\overline{BHE}$
2	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
3	$\overline{CSI}/A_{20}$	$\overline{CSI}/A_{20}$
4	$\overline{CSO}_7$	I/O_{15}
5	$\overline{CSO}_6$	I/O_{14}
6	$\overline{CSO}_5$	I/O_{13}
7	$\overline{CSO}_4$	I/O_{12}
8	$\overline{CSO}_3$	I/O_{11}
9	$\overline{CSO}_2$	I/O_{10}
10	$\overline{CSO}_1$	I/O_9
11	$\overline{CSO}_0$	I/O_8
12	GND	GND
13	$\overline{FCSO}$	$\overline{FCSO}$
14	I/O_7	I/O_7
15	I/O_6	I/O_6
16	I/O_5	I/O_5
17	I/O_4	I/O_4
18	I/O_3	I/O_3
19	I/O_2	I/O_2
20	I/O_1	I/O_1
21	I/O_0	I/O_0
22	$\overline{OE}$	$\overline{OE}$
23	A_0	A_0
24	A_1	A_1
25	A_2	A_2
26	A_3	A_3
27	A_4	A_4
28	A_5	A_5
29	A_6	A_6
30	A_7	A_7
31	A_8	A_8
32	A_9	A_9
33	A_{10}	A_{10}
34	GND	GND
35	A_{11}	A_{11}
36	A_{12}	A_{12}
37	A_{13}	A_{13}
38	A_{14}	A_{14}
39	A_{15}	A_{15}
40	A_{16}	A_{16}
41	A_{17}	A_{17}
42	A_{18}	A_{18}
43	A_{19}	A_{19}
44	V_{CC}	V_{CC}

$\overline{WE}$ and $\overline{BHE}$ are for SRAM functions.

Table 12. MAP168 Pin Assignments

44-pin CPGA Package		
Pin No.	**x8**	**x16**
A_5	GND	$\overline{BHE}$
A_4	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
B_4	$\overline{CSI}/A_{20}$	$\overline{CSI}/A_{20}$
A_3	$\overline{CSO}_7$	I/O_{15}
B_3	$\overline{CSO}_6$	I/O_{14}
A_2	$\overline{CSO}_5$	I/O_{13}
B_2	$\overline{CSO}_4$	I/O_{12}
B_1	$\overline{CSO}_3$	I/O_{11}
C_2	$\overline{CSO}_2$	I/O_{10}
C_1	$\overline{CSO}_1$	I/O_9
D_2	$\overline{CSO}_0$	I/O_8
D_1	GND	GND
E_1	$\overline{FCSO}$	$\overline{FCSO}$
E_2	I/O_7	I/O_7
F_1	I/O_6	I/O_6
F_2	I/O_5	I/O_5
G_1	I/O_4	I/O_4
G_2	I/O_3	I/O_3
H_2	I/O_2	I/O_2
G_3	I/O_1	I/O_1
H_3	I/O_0	I/O_0
G_4	$\overline{OE}$	$\overline{OE}$
H_4	A_0	A_0
H_5	A_1	A_1
G_5	A_2	A_2
H_6	A_3	A_3
G_6	A_4	A_4
H_7	A_5	A_5
G_7	A_6	A_6
G_8	A_7	A_7
F_7	A_8	A_8
F_8	A_9	A_9
E_7	A_{10}	A_{10}
E_8	GND	GND
D_8	A_{11}	A_{11}
D_7	A_{12}	A_{12}
C_8	A_{13}	A_{13}
C_7	A_{14}	A_{14}
B_8	A_{15}	A_{15}
B_7	A_{16}	A_{16}
A_7	A_{17}	A_{17}
B_6	A_{18}	A_{18}
A_6	A_{19}	A_{19}
B_5	V_{CC}	V_{CC}

Figure 7. Pin Assignments Programming



Upon delivery from WSI or after each erasure (see Erasure section), the MAP168 device has all bits in the PAD and EPROM in the "one" or high state. Zeros are loaded through the procedure of programming.

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Erasure

To clear all locations of their programmed contents, expose the device to an ultra-violet light source. A dosage of 15W-second/cm^2 is required. This dosage can be obtained with exposure to a wavelength of 2537Å and intensity of 12000μW/cm^2 for 15 to 20 minutes. The device should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

The MAP168 device and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the device; for maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque label or substance.

System Development Tools

MAP168 System Development Tools are a complete set of PC-based development tools. Installed on an IBM PC or compatible computer, these tools provide an integrated, easy-to-use software and hardware environment to support MAP168 device development. The tools run on an IBM-XT, AT, or compatible computer running MS-DOS version 3.1 or later. The system must be equipped with 640K bytes of RAM and a hard disk.

System Development Tools (Con't)

Hardware

The MAP168 System Programming Hardware consists of:

- ❑ WS6000 MagicPro Memory and PSD Programmer
- ❑ WS6014 44-pin LCC Package Adaptor (for 44-pin CLLCC, CLDCC, and PLDCC packages)
- ❑ WS6015 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of the IBM-PC plug-in Programmer Board and the Remote Socket Adaptor Unit.

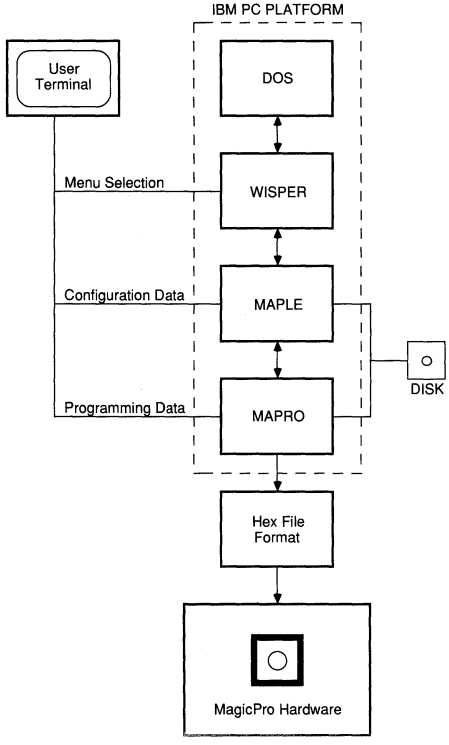
Software

The MAP168 System Development Software consists of the following:

- ❑ WISPER Software—PSD Software Environment
- ❑ MAPLE Software—MAP168 Location Editor
- ❑ MAPPRO Software—Device Programming Software

The configuration of the MAP168 device is entered using MAPLE software. MAPRO software configures MAP168 devices by using the MagicPro programmer and the socket adaptor. The programmed MAP168 is then ready to be used. The development cycle is depicted in Figure 8.

Figure 8. MAP168 Development Cycle



System Development Tools (Con't)

Support

WSI provides a complete set of quality support services to registered System Development Tools owners. These support services include the following:

- 12-month Software Updates.
- Hotline to WSI Application Experts—For direct design assistance.
- 24-Hour Electronic Bulletin Board—For design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the MAP168 device and System Development Tools. Workshop participants learn how to program their own high-performance, user-configurable mappable memory subsystems. Workshops are held at the WSI facility in Fremont, California.

Ordering Information

MAP168 Part Number	Speed (ns)	Package Type	Package Drawing	Operating Temperature	Manufacturing Procedure
MAP168-45J	45	44-pin PLDCC	J2	Commercial	Standard
MAP168-45L	45	44-pin CLDCC	L4	Commercial	Standard
MAP168-45X	45	44-pin CPGA	X2	Commercial	Standard
MAP168-55C	55	44-pad CLLCC	C3	Commercial	Standard
MAP168-55CI	55	44-pad CLLCC	C3	Industrial	Standard
MAP168-55CM	55	44-pad CLLCC	C3	Military	Standard
MAP168-55CMB	55	44-pad CLLCC	C3	Military	MIL-STD-883C
MAP168-55J	55	44-pin PLDCC	J2	Commercial	Standard
MAP168-55L	55	44-Pin CLDCC	L4	Commercial	Standard
MAP168-55LM	55	44-Pin CLDCC	L4	Military	Standard
MAP168-55LMB	55	44-pin CLDCC	L4	Military	MIL-STD-883C
MAP168-55X	55	44-pin CPGA	X2	Commercial	Standard
MAP168-55XI	55	44-pin CPGA	X2	Industrial	Standard
MAP168-55XM	55	44-pin CPGA	X2	Military	Standard
MAP168-55XMB	55	44-pin CPGA	X2	Military	MIL-STD-883C

Ordering Information

System Development Tools

Part Number	Contents
MAP168-GOLD	WISPER Software MAPLE Software User's Manual WSI-SUPPORT WS6000 MagicPro Programmer
MAP168-SILVER	WISPER Software MAPLE Software User's Manual WSI-SUPPORT
WS6000	MagicPro Programmer IBM PC plug-in Adaptor Card Remote Socket Adaptor
WS6014	44-pin LCC Package Adaptor for 44-pin CLLCC, CLDCC, and PLDCC Packages. Used with the WS6000 MagicPro Programmer.
WS6015	44-pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.
WSI-SUPPORT	Support Services including: ❑ 12-month Software Update Service ❑ Hotline to WSI Application Experts ❑ 24-hour access to WSI Electronic Bulletin Board
WSI-TRAINING	Workshops at WSI, Fremont, CA. For details and scheduling, call PSD Marketing, (415) 656-5400.

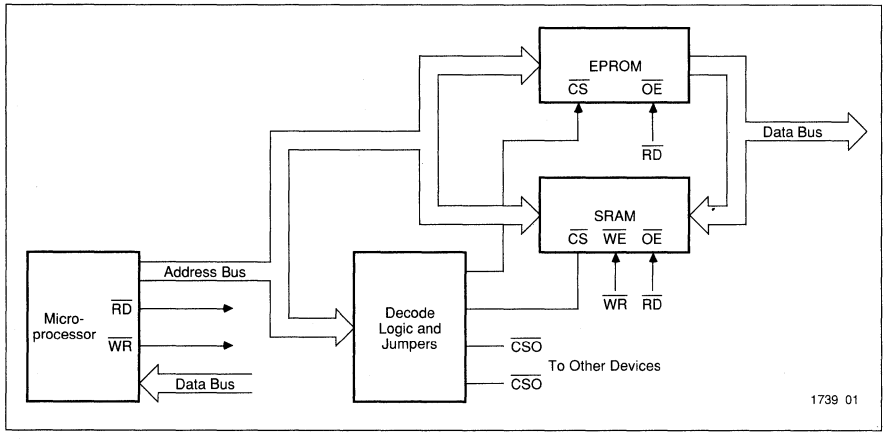
Programmable Peripheral Application Note 002

Introduction to the MAP168 User-Configurable Peripheral with Memory

Memory Structure

Memory configurations in microprocessor and microcontroller systems have similar structure, irrespective of the application. (see Figure 1.) They share basic components, such as an EPROM (for program storage), and an SRAM (for data storage). In addition, a decoder circuit is required to select blocks of memory from the address inputs applied by the processor. A common implementation of address decoding originally used MSI building blocks, such as 74xx138 devices. Memory-configuration changes and expansions in a fixed-logic solution required jumpers on the printed circuit board. More recently, decoders based on PAL® devices have provided a more compact and flexible solution. PAL devices allow configuration changes to be implemented by insertion of a programmed device and avoid jumper changes.

Figure 1. Memory Subsystem Using Standard Devices



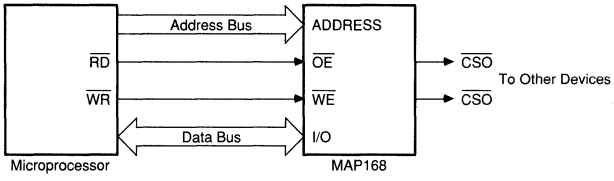
Both solutions involve compromises that affect system performance, board space, power and cost. Since the decoder is in the memory access path, the total memory access time is the sum of the decoder delay and the access time of the memory itself. For example, a 40ns total access time can be achieved with a 12ns decoder and a 25ns memory. This allows 3ns for on-board interconnect delay. Memory products in the 25ns range are expensive and therefore such a performance entails additional cost. To be able to integrate the programmable address decoder with system memory, EPROM and static RAM would offer a more flexible approach. The resulting device would provide board-space economy, higher performance and less overall power consumption without the cost of a multichip solution.

Memory Structure (Cont.)

The WSI MAP168 user-configurable peripheral with memory has been developed to significantly enhance system performance by integrating high density EPROM for program store, high density SRAM for data store and high performance logic in the form of a Programmable Address Decoder (PAD) on one chip. (See Figure 2.) The MAP168 integrates 128K bits of EPROM and 32K bits of SRAM. It is ideally suited for a number of common design applications:

- ❑ High-speed Digital Signal Processor applications (modems, analog data filtering or analysis)
- ❑ Expanding memory systems for microprocessors and microcontrollers
- ❑ Space- and power-sensitive applications (plug-in cards, avionics, portable systems)

Figure 2. Using the MAP168



Features of the MAP168

The MAP168 offers significant design advantages through integration, performance and user-configurability. It integrates both volatile and non-volatile memory on the same chip, along with a flexible decoding system. The memory is structured as a series of blocks to achieve a highly configurable circuit for general purpose applications. The device operates in one of several modes, one of which is for normal operation and the rest are for device configuration. At the heart of all MAP168 device's is a Programmable Address Decoder (PAD), which is programmed during the PAD programming mode through the circuit's address and I/O pins. The PAD offers the following features:

- ❑ Flexible EPROM/SRAM location within the address space
- ❑ Memory array power-down when not being accessed
- ❑ Security protection of memory configuration data to inhibit copying
- ❑ Integrated external device mapping through Chip Select Outputs

Memory Architecture And Technology

The memory in the MAP168 consists of non-volatile EPROM and volatile SRAM. (See Figure 3.) The EPROM is subdivided into 8 blocks and the SRAM into 2 blocks. The blocks may be configured in either a 2Kx8 or a 1Kx16 format, allowing optimal interaction with both 8- and 16-bit systems. These memory blocks can be considered as separate memories with dedicated internal chip selects. The PAD selects the appropriate block, decoded from the incoming address provided at the device inputs. This architecture enables the product to be configured and compatible with virtually any system address map. Complicated address maps of microcontroller systems can be fully realized by programming blocks of EPROM and SRAM in the memory-mapping scheme of the system.

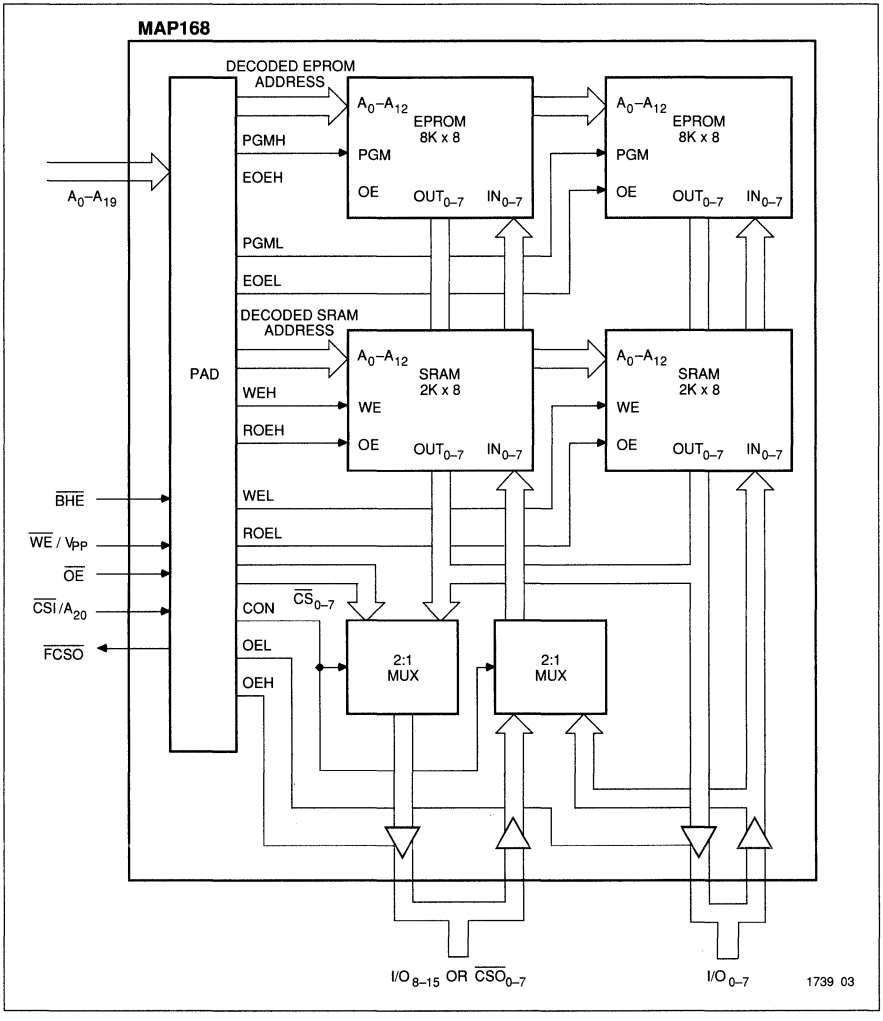
Features of the MAP168 (Cont.)

In addition to having fine control of memory allocation, software updates which require changes in the address map boundaries can be easily accomplished by simply reprogramming the PAD at the same time as the EPROM code. This means only one part need be sent to the end-product customer to accommodate field software changes. This becomes a user-transparent method that requires no change of PC board jumpers.

The EPROM is based on WSI's patented split-gate EPROM technology for high density and very high speed. It is also used in the reconfigurable PAD section, permitting both fast decode and reconfiguration of the same device. The MAP168 contains a 128K-bit UV erasable EPROM which can be organized as 16Kx8 (byte-wide) or as 8Kx16 (word-wide).

The SRAM is based on the industry standard full CMOS 6-transistor cell. The advantages of this cell are high speed, very low stand-by power, high noise immunity and good data retention when disturbed by alpha particles. In the MAP168 device, the SRAM contains 32K bits which can be configured as 4Kx8 in the byte mode or 2Kx16 in the word-wide mode.

Figure 3. Internal Architecture



Features of the MAP168 (Cont.)

PAD Logic Implementation

The PAD uses the same non-volatile EPROM cells as the EPROM array. (See Figure 4.) It can be erased and configured at the same time as the EPROM. After UV erase or with new parts, the EPROM cells in the MAP168 device normally connect between the address inputs and the select outputs. The EPROM cells are disconnected by selective programming.

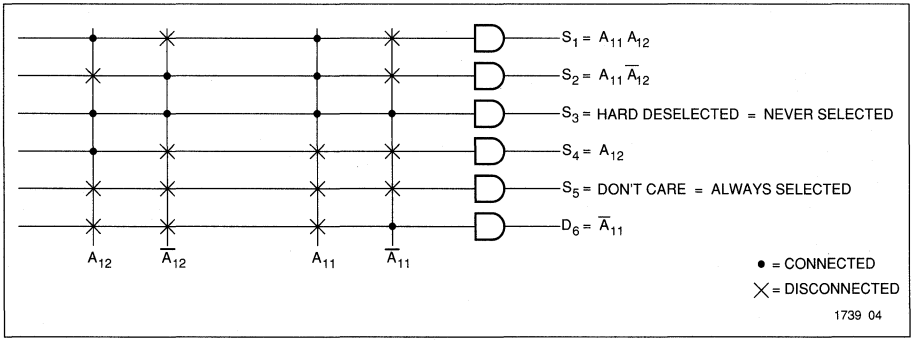
The PAD performs as an address comparator. When the address configuration previously programmed into the PAD is detected, the internal chip-select signal to the memory block selected by that address is enabled. If no block is selected by the address, neither the EPROM nor the SRAM arrays are enabled and other devices may drive the data bus. Independent of internal block selection, external chip-select decoding (known as $\overline{CSO}$s) are programmable in the same block resolution as the internal memory.

Actual implementation of the PAD is similar to that of a PAL device. (See Figure 5.) In the erased state, all the block decode addresses are connected to the AND plane. There is only one output per AND gate and there is no OR plane. Each AND gate output either selects a block of internal memory or a number of blocks of external memory for the external $\overline{CSO}$s. Only addresses A_{11}–A_{20} are used as block decode address. Lower-order address lines are used only for addressing within the internal memory arrays.

EPROM select outputs ES_0–ES_7 (ES outputs) select 1 of the 8 available EPROM blocks. SRAM select outputs RS_0–RS_1 (RS outputs) select one of the 2 available SRAM blocks. Because only one EPROM or SRAM block can be active at a particular time, only one line from either ES_0–ES_7 or RS_0–RS_1 is allowed to be active at one time. The $\overline{CSO}$s are independent of the ES and RS outputs and therefore any one address can be programmed to select one or more of the $\overline{CSO}$s, even simultaneous to the selection of one of the ES or RS outputs. This is particularly useful for I/O control or address decode for wait state generation.

Programming the decoder is similar to programming a PAL device that has only one product term (AND gate) per output. To enable an output S_1 as shown in Figure 4, fuse locations A_{11} and A_{12} are left intact while $\overline{A}_{11}$ and $\overline{A}_{12}$ are programmed. Conversely, if A_{11} and A_{12} are programmed while their complements are left intact, then the select S function is active when $\overline{A}_{11} = \overline{A}_{12} = 0$. If all fuse locations are programmed on a product term, the inputs are pulled HIGH and no select output can take place. If all fuse locations are left intact, the S output is permanently LOW, always selected.

Figure 4. PAD Programming Examples

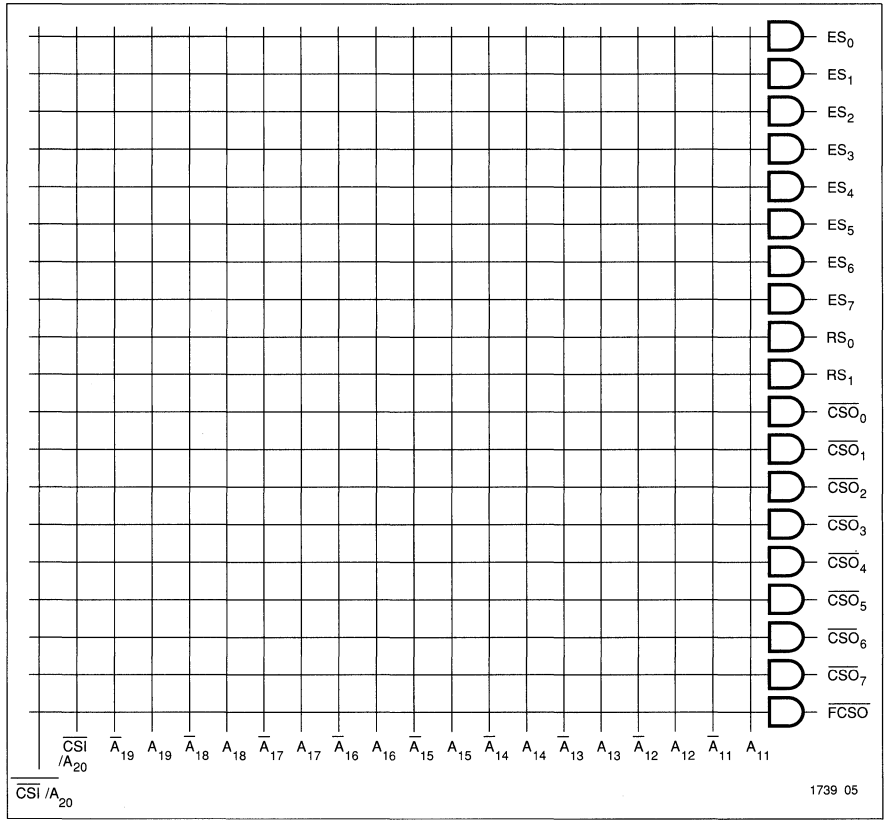


Features of the MAP168 (Cont.)

Device Array Power-Down

Power dissipation on the chip is minimized through logic in the PAD. It selectively powers up the EPROM or SRAM arrays only when they are being accessed. If the EPROM is selected through the decoder, it will draw power while the SRAM stays powered down and vice versa. When neither the EPROM or the SRAM is selected, both are powered down. Note that data integrity in a "powered down" SRAM is maintained. A Chip Select Input ($\overline{CSI}$) to the device is provided for a very low-power quiescent mode. With $\overline{CSI}$=1, the EPROM and SRAM are powered down but the PAD is powered up, independent of the incoming address signals. The $\overline{CSI}$ input pin can be connected to a system power-down signal. If such a signal is unavailable, addressing a location in memory that does not select either the EPROM or the SRAM also reduces power drain. In this case, only the PAD is powered up and draws a small fraction of the active power.

Figure 5. PAD Array Architecture



Features of the MAP168 (Cont.)

The $\overline{CSI}/A_{20}$ input is actually a dual function pin. It can be an address (MSB) input, or it can be programmed to be a chip select input as well. As a chip select input, it will enable the EPROM and SRAM memory when active (LOW). If the address option A_{20} is chosen the chip is always enabled.

Address Map Security

Upon entering the PAD programming mode, the contents of the PAD are fully accessible through the I/O pins. After programming is completed, it is possible to render the PADs programmed configuration invisible by programming the security (SEC) bit. This disables external access to the PAD and ensures that the PAD configuration can not be copied. To further aid in securing data in the MAP168, it is suggested that memory blocks that are addressed in a linear block placement be programmed in the PAD as chip selects from product terms that are randomly placed.

Chip Select Outputs

The MAP168 device can be user-configured for 8-bit or 16-bit systems. In the former case, eight unused data lines ($\overline{CSO}_{0-7}$) are available as chip select outputs, driven by the address decoder section of the PAD. This provides the ability to integrate external devices into the address map with no hardware overhead. Unlike the internal memory blocks, a $\overline{CSO}$ can be active for more than one address combination or block. Also, groups of blocks may overlap both each other and the internal memory. By deselecting both the true and the complement it is possible to make an address line "don't care".

An external memory can therefore be selected with only one $\overline{CSO}$. It is possible to enable another external 128K byte memory by programming a single $\overline{CSO}$ to be active for that entire address range.

A $\overline{CSO}$ can be programmed to function as a configuration bit which is always deselected (e.g., $\overline{CSO}_0$=1) or always selected (e.g., $\overline{CSO}_0$=0) by programming the addresses with "hard deselect" or with the "don't care" patterns, respectively. This is similar in function to a PC-board wire jumper. If unused $\overline{CSO}$s are programmed with all addresses "don't care", then switching is eliminated and power consumption reduced for those lines.

Since the PAD is always powered up when the device is selected ($\overline{CSI}$=0), $\overline{CSO}$s are always active and their state is a direct function of the PAD configuration and current address line inputs.

Systems Applications

The MAP168 device is designed to reduce memory access time and board area utilization in high performance digital signal processor, microcontroller and microprocessor systems. These systems typically have the following requirements:

- 16-bit data path
- 64K to 1 Meg address space
- Fast memory access time (100ns to 40ns)
- Decoding for I/O and memory
- Printed circuit board area limitations
- Multiple types of memory, including EPROMs and SRAMs for program and data store.

The DSP System Architecture shown in Figure 6 illustrates a typical system based upon a 40MHz TMS320C25 digital signal processor. Such a system allows only 40ns for memory access time. The access time must be broken down into decoding time and memory-access time. The fastest decoders available today require approximately 10ns to complete their decode function. Due to this decoding time, memory access time for both the EPROM and SRAM must be 30ns or less. The MAP168 performs decoding on-chip with no speed penalty. As a result, the performance of a 45ns MAP168 device in the above example is equivalent to a 10ns decoder and a 35ns EPROM and SRAM memory. In addition, the package equivalent of two fast EPROMs, two fast SRAMs and at least one decoder are combined into one MAP168 chip resulting in at least a 5-to-1 component count reduction.

Systems Applications (Cont.)

High-Speed, Word-Oriented Application

The MAP168 device is especially suited for high-speed word-only microprocessors. The TMS320C20/25 DSP family is an example of such a microprocessor. Interfacing the MAP168 device to a TMS320C25 operating at 40MHz with no wait states is illustrated in Figure 7. The TMS320C25 has two pins for selecting Program Memory (PS) and Data Memory (DS). These functions are connected to the higher order address of the MAP168 device. PS is connected to A_{18} and DS is connected to A_{17}. Usually PS will select the EPROM and DS will select the SRAM. The PAD permits partitioning of the MAP168 memory to accommodate virtually any system address map. Figure 8 shows two possibilities.

Figure 6. DSP System Architecture

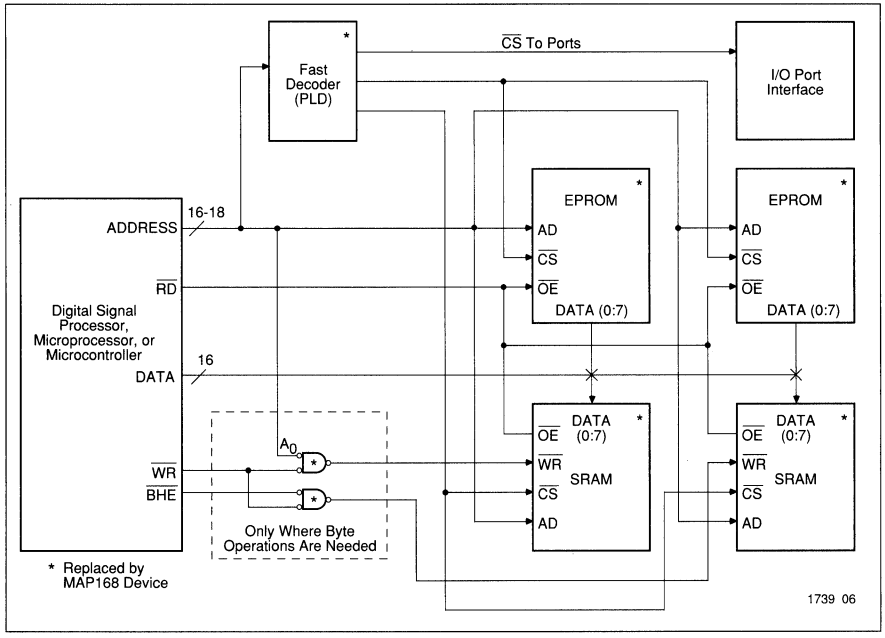
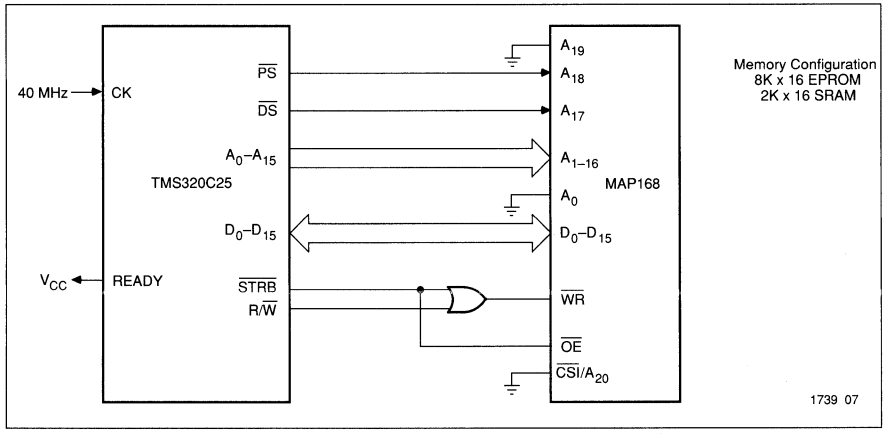


Figure 7. TMS320C25 Interfacing
x16 Configuration



Systems Applications (Cont.)

When in a word-wide (x16) configuration, the total memory available on the MAP168 device is 8Kx16 of EPROM and 2Kx16 of SRAM. The implementation shown in Figure 7 replaces at least five circuits:

- One high-speed decoder (10ns)
- Two 8Kx8 EPROMs (30ns)
- Two 2Kx8 SRAMs (30ns)

If the system was previously implemented using a boot EPROM, the MAP168 device replaces ten circuits:

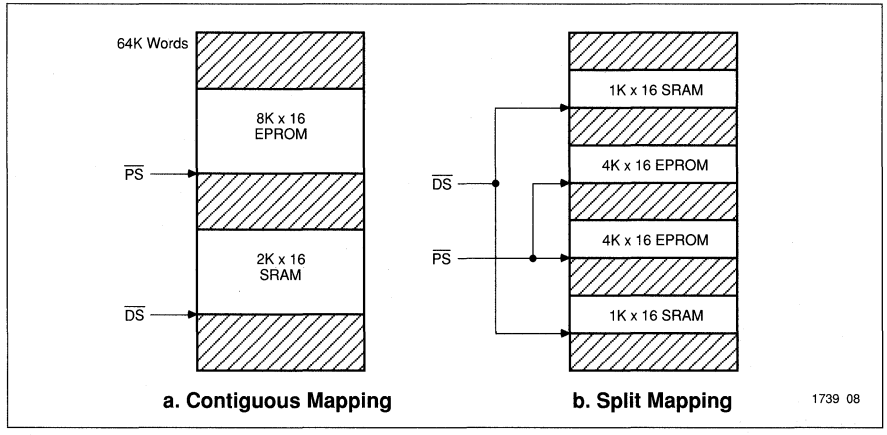
- One high-speed decoder (10ns)
- Two 8Kx8 EPROMs (30ns)
- Two 2Kx8 SRAMs (30ns)
- Two 8Kx8 slow EPROMs
- Three ICs for Wait-State generation

For expanded memory requirements in a word-wide (x16) configuration, two MAP168 devices can be interfaced directly with a TMS320C25, as shown in Figure 9. The two MAP168 devices provide the total system memory. Key features of this system are:

- 40ns access time
- 16Kx16 EPROM
- 4Kx16 EPROM
- 16 general purpose programmable chip selects

The general-purpose programmable chip select outputs can be mapped to any location in the address space via the PAD. These chip selects can be used to access I/O ports, select additional memory or control other system functions.

Figure 8. Memory Mapping with MAP



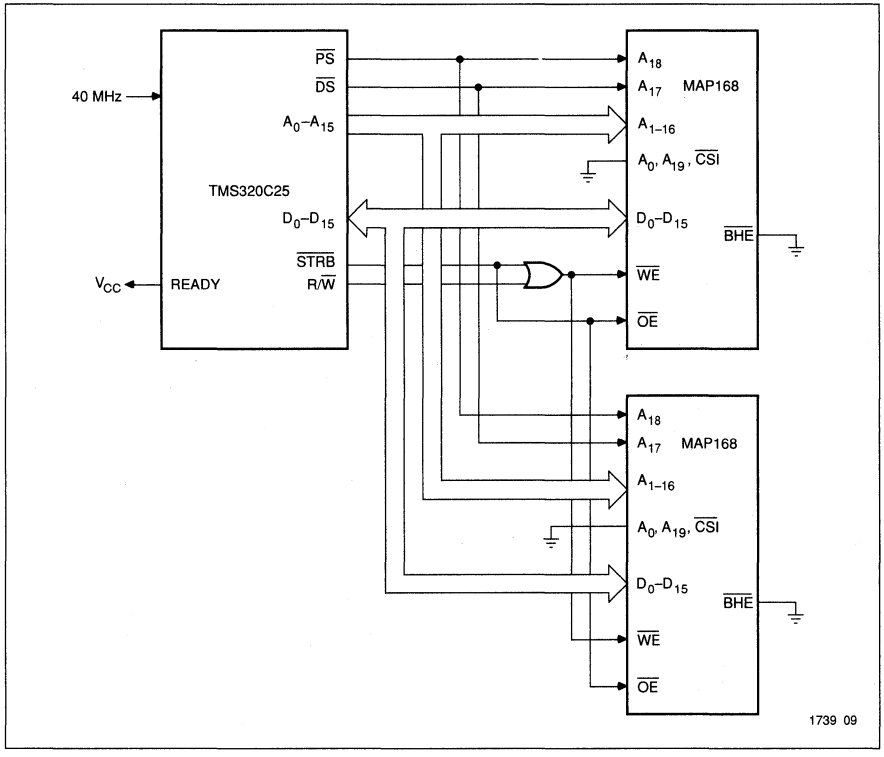
Microcontroller Application

The MAP168 device has two basic configurations. They are a word-wide (x16) configuration with byte operation capability and a byte-wide (x8) configuration with 8 chip select outputs.

The 128K address space (during byte operations in the word-wide mode) makes the MAP168 device especially suited for microcontroller applications. Figure 10 illustrates a simple interconnection of the MAP168 device to a microcontroller. The HPC16040 operating without wait states requires a memory access time of 65ns or better. This makes the MAP168 device a good fit, since it offers an access time of 45ns, leaving a 20ns margin.

The MAP168 device can be configured in a byte-wide (x8) mode and can also be doubled-up with a second device.

Figure 9. DSP with Expanded Memory



Microcontroller Application (Cont.)

Embedded Controller Application

An embedded controller is an intelligent section of logic, usually based around a processor, dedicated to a particular task and is not accessible for software alteration by the user. Such applications are generally complex and are becoming more common in system design. Typically, embedded controllers are high performance systems designed under severe space/power constraints. On the other hand, they have a limited ability to be upgraded and limited program memory. This makes them ideal candidates for the MAP168 implementation. The MAP168 has the following key features which are useful in such an application:

- 1M address space decoding
- 45ns access time
- Byte operations in word-wide mode (BHE)
- One output chip select when in the word-wide mode ($\overline{FCSO}$)
- Nine output chip selects when in the byte-wide mode
- Programmable Address Decoder (PAD)

A popular processor for embedded applications, due largely to its extensive software library and development support, wide availability of compatible peripherals and low cost from volume production is the 80186 from Intel. Figure 11 shows how a MAP168 device can be interfaced to an 80186.

The UCS (Upper Chip Select) is connected to $\overline{CSI}/A_{20}$ on the MAP168 device. The PAD is programmed to locate a 1Kx16 EPROM slot in the upper memory address space for a reset subroutine. The rest of the memory can be located as required by the user. Figure 12 shows one possibility.

MAP168 Development Support

WSI provides the development environment needed to program the MAP168. A menu-driven software package known as MAPLE is available under the WISPER top-level software. It operates on the popular IBM-PC® as a platform and includes extensive documentation on installation and operation. It generates configuration files for use by the programming tools. These programming tools include the MagicPro™ programmer hardware and the MAPPRO software. They enable the user to program the PAD and the EPROM. For additional information, consult your nearest WSI sales representative.

Figure 10. Microcontroller Interfacing

x16 Configuration

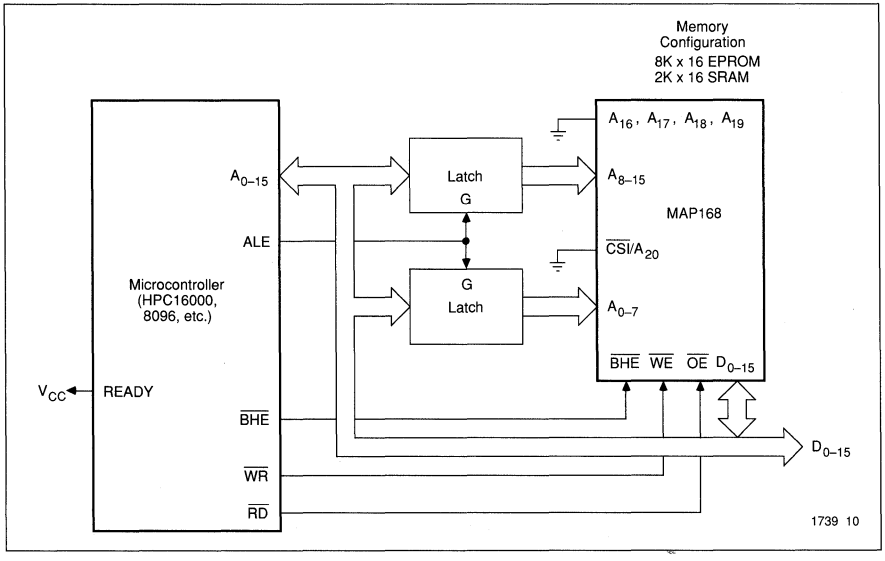


Figure 11. Interfacing To An 80186
x16 Configuration

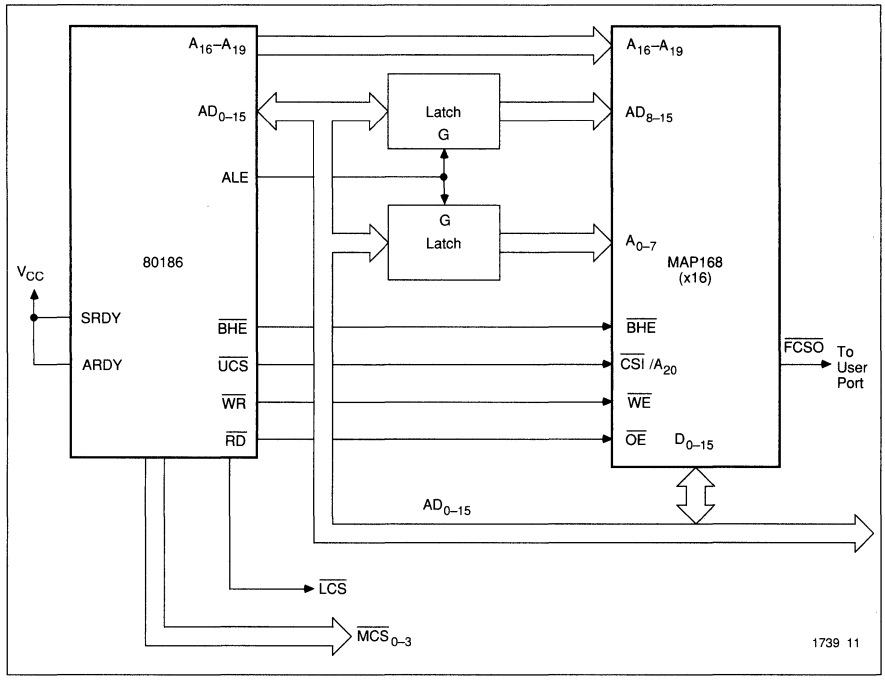
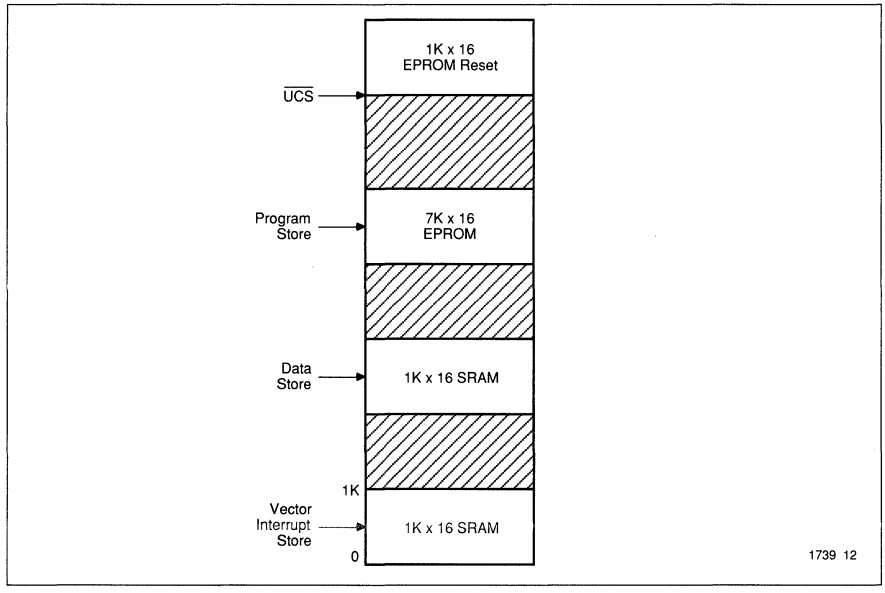


Figure 12. Optional Memory Mapping For An 80186



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Section Index

Development Systems

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363.

Programmable Peripheral
Electronic Bulletin Board

Bulletin Board

WSI provides a 24-hour electronic bulletin board system that provides the user with the latest information on software updates, enhancements, and applications relating to WSI products. In addition, users developing applications software for WSI products can send portions of their code to WSI for application's consultation if desired.

The following hardware is required to use the WSI bulletin board:

- ❑ Computer Terminal
- ❑ 300, 1200, 2400 Baud Modem
- ❑ 8 Data Bits
- ❑ No Parity
- ❑ 1 Stop Bit

Access Line

To access the bulletin board, dial

(510) 498-1002

and wait for the modem tone. When your modem establishes a connection, enter <return> <return> to signal the bulletin board software. The board should respond:

WSI Customer Engineering Support
Electronic Bulletin Board Service

followed by some other messages, after which you will be asked for your name, and a password. Upon initial use, follow the on-screen prompts for establishing your password.

Now that you have entered the bulletin board service, you will be given a choice of "MAIN" commands:

Main Commands

M)sg-Section
Choose this option to leave messages.

F)ile-Section
Choose this option to download or upload data files and/or utility programs

B)ulletins
Choose this option to see the latest important news such as software versions and programming tips for WSI Memory and PSD products.

S)tatistics
This option describes the current bulletin board statistics

C)hange
Choose this option to change operational settings that the bulletin board maintains for your user name.

P)age-Operator
Choose this to page the operator for assistance. It is not likely that the operator will be available during West Coast U.S. non-business hours.

L)ist-Callers
Choose this option to see who else is using the board at this moment.

A)ns-Questionnaire
Choose this option to answer a user profile questionnaire.

V)ersion
Describes the board software version.

G)oodbye
Choose this to leave the bulletin board.

See the individual software manuals for more detailed explanation and usage of the bulletin board.

Programmable Peripherals
PSD-Gold/PSD-Silver Development System
PSD3XX/MAP168

Description

PSD-Gold/PSD-Silver is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support PSD3XX family and MAP168 program development and device programming.

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

MAPLE

MAPLE is the Locator Editor. It has the following features:

- ❑ Simple Menu Driven Commands for selecting different configurations of the PSD3XX/MAP168
  - – Byte wide or word wide operation.
  - – Address or Chip Select Input (CSI) Mode.
  - – PAD security option.
- ❑ Generating the PAD programming data that maps the EPROM, SRAM and Chip Selects Outputs to the user's address space.
- ❑ Combining all the different files to be programmed into the EPROM segments.

MAPPRO

MAPPRO is the interface software that enables the user to program a PSD3XX or MAP168 device on the WS6000 MagicPro™ programmer. The MAPPRO enables the user to load the program into the programmer and to execute the following operations.

- ❑ Help
- ❑ Upload RAM from MAP
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display MAP data
- ❑ Blank test MAP
- ❑ Verify MAP
- ❑ Program MAP
- ❑ Configuration
- ❑ Quit

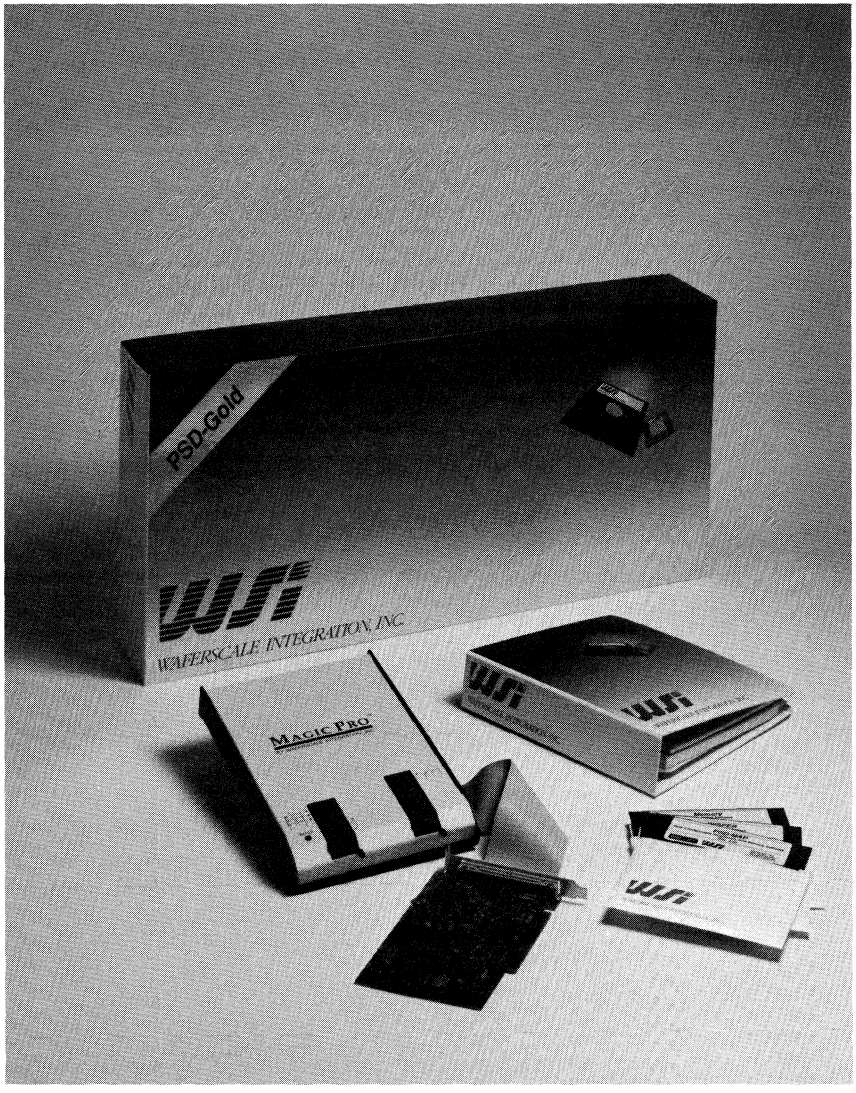
WS6000 MagicPro™ Programmer

The WS6000 MagicPro Programmer is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, MAP168, PSD3XX family and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support WSI's 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

WS6014 Socket Adaptor

The WS6014 is a socket adaptor that mounts on the MagicPro RSA and adapts the MAP168 in 44-in CLDCC, PLDCC or CLLCC packages to the programmer.

PSD-Gold



Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to MAP168 device programmer (MagicPro™)
- ❑ Software user's manual
- ❑ WSI-Support agreement
- ❑ WS6000 MagicPro Programmer
- ❑ A Socket Adaptor and Two Product Samples

PSD-Silver

Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to MAP168 device programmer (MagicPro™)
- ❑ Software user's manual
- ❑ WSI-SUPPORT agreement.

WS6015 Socket Adaptor

The WS6015 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX or MAP168 in a 44-pin PGA package to the programmer.

WS6020 Socket Adaptor

The WS6020 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX in a 52-pin PQFP package to the programmer.

WS6021 Socket Adaptor

The WS6021 is a socket adaptor that mounts on the MagicPro RSA and adapts the PSD3XX in a 44 pin CLDCC or PLDCC package to the programmer.

WSI-Support

WSI provides on-going support for users of PSD-Gold/Silver. For the first year, software and programmer updates are included at no charge. After that, the user may purchase the WSI-Support agreement to continue to receive the latest software releases.

Ordering Information

Product	Description
PSD-Silver	Contains PSD3XX and MAP168 Software (MAPLE-MAP and MAPPRO), Software User's Manual, WSI-Support.
PSD-Gold	Contains PSD-Silver, WS6000 MagicPro Programmer, a Socket Adaptor and Two Product Samples, WSI-Support.
WSI-Support	12-Month Software Update Service, Access to WSI's 24-Hour Electronic Bulletin Board, and Hotline to WSI System Application Experts.

WS6000

MagicPro™ Memory and Programmable Peripheral Programmer

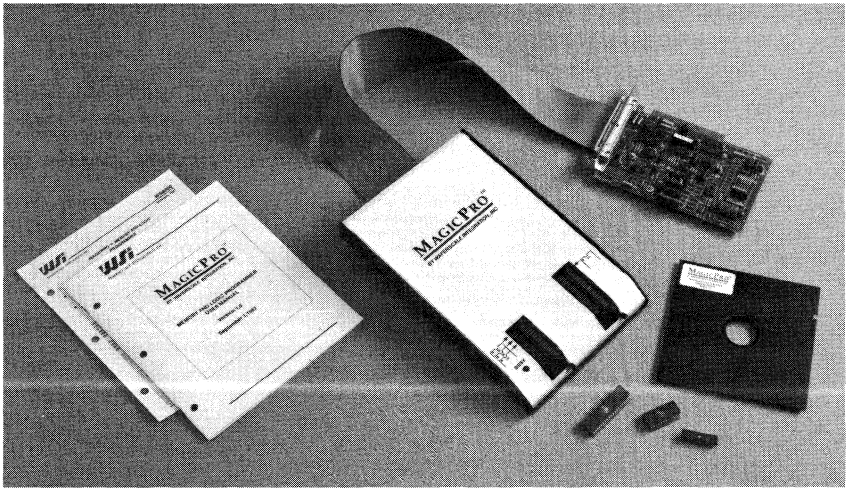
Key Features

- ❑ Programs All WSI CMOS Memory and and Programmable Peripheral Products and All Future Programmable Products
- ❑ Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages without Adaptors
- ❑ Programs LCC, PGA and QFP Packaged Product by Using Adaptors
- ❑ Easy-to-Use Menu-Driven Software
- ❑ Compatible with IBM PC/XT/AT Family of Computers (and True Plug-Compatible

General Description

MagicPro is an engineering development tool designed to program existing WSI EPROMs, RPROMs, Programmable Peripherals, and future WSI programmable products. It is used within the IBM-PC® and compatible computers. The MagicPro is meant to bridge the gap betweeen the introduction of a new WSI programmable product and the availability of programming support from programmer manufacturers (e.g., Data I/O, etc.). The MagicPro programmer and accompanying software enable quick programming of newly released WSI programmable products, thus accelerating the system design process.

The MagicPro plug-in board is integrated easily into the IBM-PC. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC, PGA and QFP packages are supported using adaptors.



General Description (Cont.)

Many features of the MagicPro Programmer show its capabilities in supporting WSI's future products. Some of these are:

- ❑ 24 to 40 pin JEDEC Dip Pinouts
- ❑ 1 Meg Address Space (20 address lines)
- ❑ 16 Data I/O Lines

The MagicPro menu driven software makes using different features of the MagicPro an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading. Please call 800-TEAM-WSI for information regarding programming WSI products not listed herein. The MagicPro reads Intel Hex format for use with assemblers and compilers.

MagicPro Commands

- ❑ Help
- ❑ Upload RAM from Device
- ❑ Load RAM from Disk
- ❑ Write RAM to Disk
- ❑ Display RAM Data
- ❑ Edit RAM
- ❑ Move/Copy RAM
- ❑ Fill RAM
- ❑ Blank Test Device
- ❑ Verify Device
- ❑ Program Device
- ❑ Select Device
- ❑ Configuration
- ❑ Quit MagicPro

Technical Information

- ❑ ***Size:***
  IBM-PC Short Length Card
- ❑ ***Port Address Location:***
  100H to 1FFH – default 140H (if a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)
- ❑ ***System Memory Requirements:***
  256K Bytes of RAM
- ❑ ***Power:***
  + 5 Volts, 0.03 Amp; +12 Volts, 0.04 Amp
- ❑ ***Remote Socket Adaptor (RSA):***
  The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC, PGA and QFP packages.

Ordering Information

The WS6000 MagicPro Systems Contains:

- ❑ MagicPro IBM-PC Plug-in Programmer Board
- ❑ MagicPro Remote Socket Adaptor and Cable
- ❑ MagicPro Operating System Floppy Disk and Operating Manual

The WS6000 MagicPro Adaptors Include:

- ❑ WS6001 28-Pin CLLCC Package Adaptor for Memory.
- ❑ WS6008 28-Pin 0.3" Wide Dip Adaptor for SAM448
- ❑ WS6009 28-Pin PLDCC/CLDCC/ CLLCC Package Adaptor for SAM448
- ❑ WS6010 88-Pin PGA Package Adaptor for PAC1000
- ❑ WS6012 32-Pin CLDCC Package Adaptor for Memory
- ❑ WS6013 100-Pin QFP Package Adaptor for PAC1000
- ❑ WS6014 44-Pin CLDCC/PLDCC Package Adaptor for MAP168
- ❑ WS6015 44-Pin PGA Package Adaptor for MAP168 and PSD3XX
- ❑ WS6016 44-Pin CLDCC/PLDCC Package Adaptor for Memory
- ❑ WS6020 52-Pin PQFP Package Adaptor for PSD3XX
- ❑ WS6021 44-Pin CLDCC/PLDCC Package Adaptor for PSD3XX

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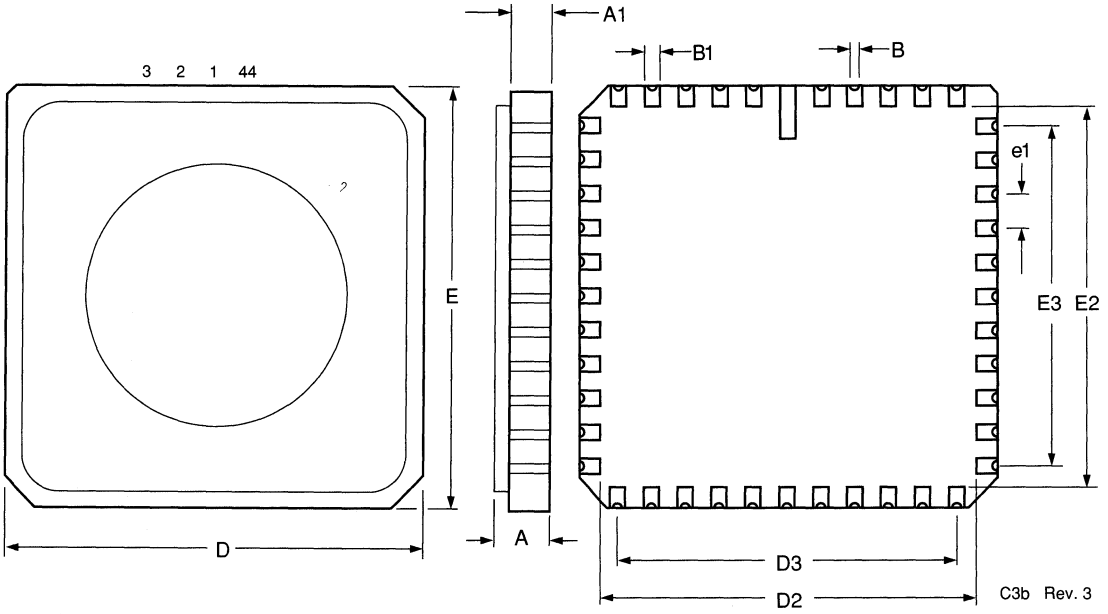
MagicPro™ is a trademark of WaferScale Integration, Inc.
IBM-PC® is a registered trademark of IBM Corporation.

Section Index

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, Call 800-562-6363.

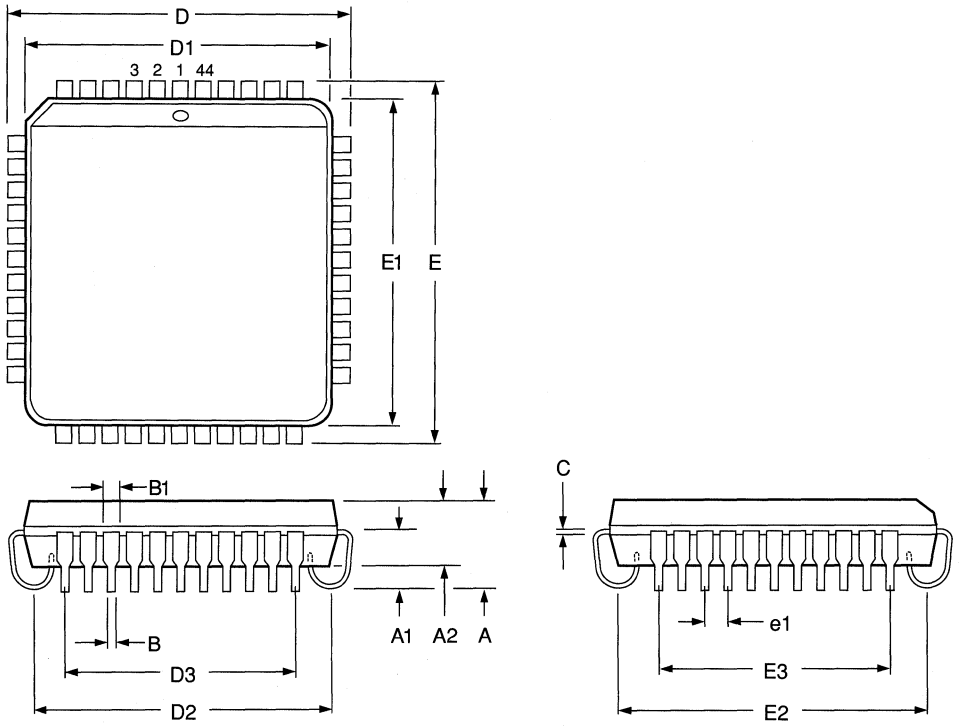
Drawing C3 44 Pad Ceramic Leadless Chip Carrier (CLLCC)
(Package Type C)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.41	3.30		0.095	0.130	
A1	1.47	2.03		0.058	0.080	
B	0.46		Typical Dia.	0.018		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	16.26	16.81		0.640	0.662	
D2	13.97		Typical	0.550		Typical
D3	12.70		Reference	0.500		Reference
E	16.36	16.81		0.640	0.662	
E2	13.97		Typical	0.550		Typical
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

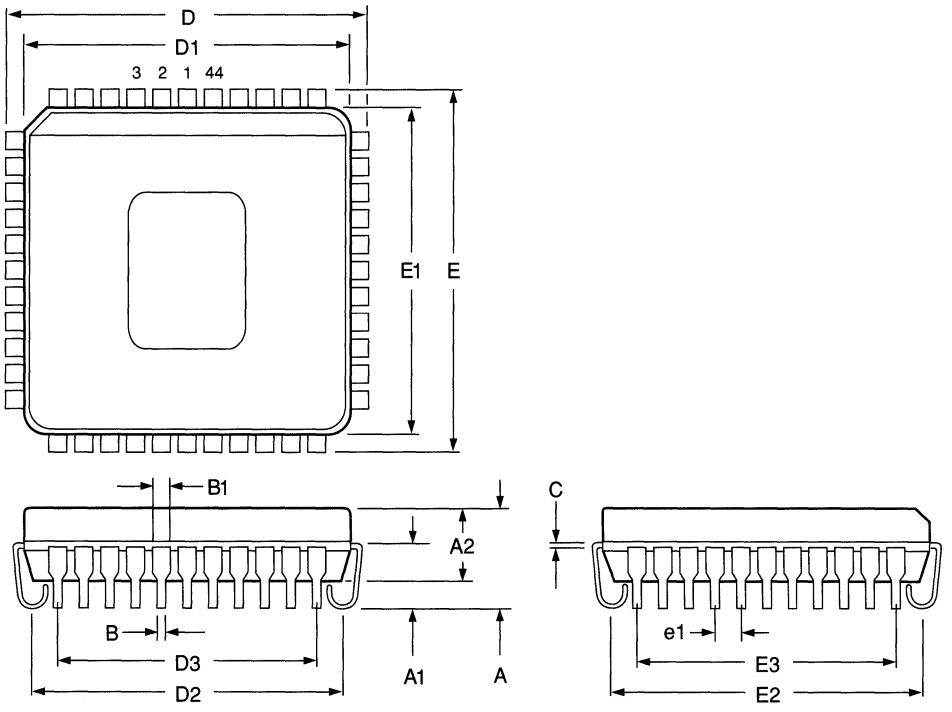
C3, C3b

Drawing J2 44 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.76	3.96		0.148	0.156	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	17.40	17.65		0.685	0.695	
D1	16.51	16.61		0.650	0.654	
D2	14.99	16.00		0.590	0.630	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.51	16.61		0.650	0.654	
E2	14.99	16.00		0.590	0.630	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

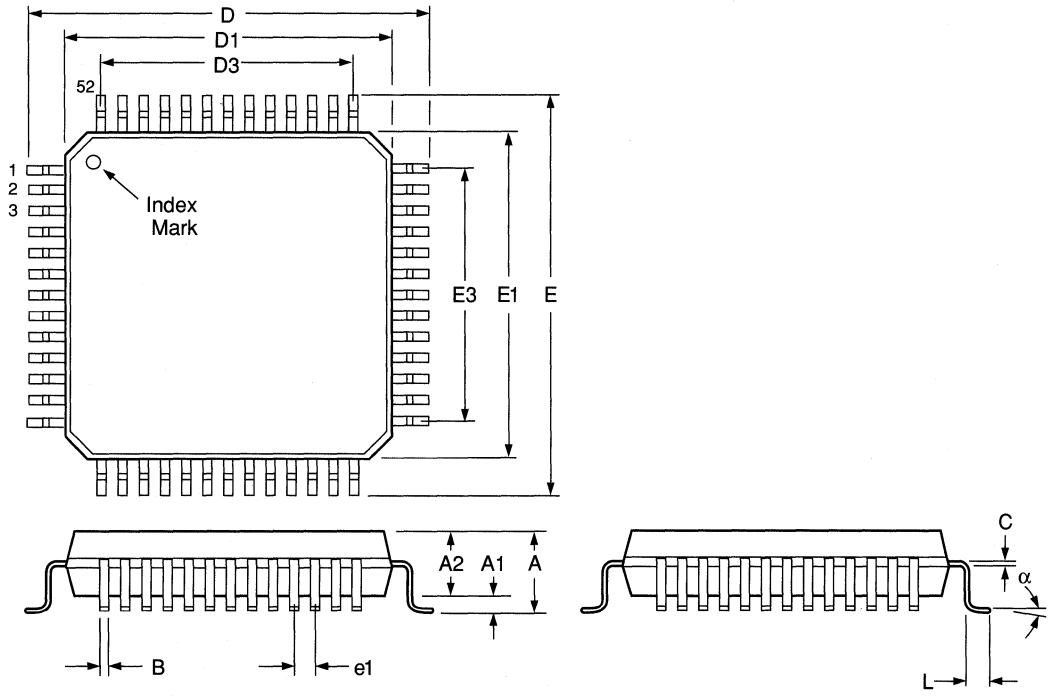
Drawing L4 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.095	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	17.40	17.65		0.685	0.695	
D1	16.31	16.66		0.642	0.656	
D2	14.99	16.00		0.590	0.630	
D3	12.70		Reference	0.500		Reference
E	17.40	17.65		0.685	0.695	
E1	16.31	16.66		0.642	0.656	
E2	14.99	16.00		0.590	0.630	
E3	12.70		Reference	0.500		Reference
e1	1.27		Reference	0.050		Reference
N	44			44		

5

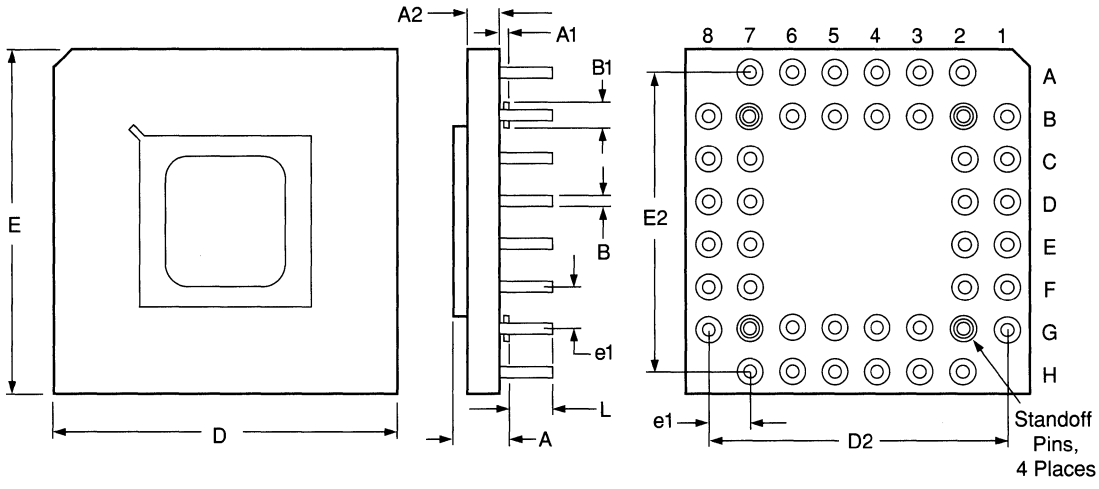
Drawing Q2 52 Pin Plastic Quad Flatpack (PQFP)



Rev. 6

Family: Plastic Quad Flatpack						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.55	3.05		0.100	0.120	
A1	0.00	0.25		0.000	0.010	
A2	2.55	2.80		0.100	0.110	
B	0.35	0.50		0.014	0.020	
C	0.13	0.23		0.005	0.009	
D	17.65	18.15		0.695	0.715	
D1	13.95	14.05		0.549	0.553	
D3	12.00		Reference	0.472		Reference
E	17.65	18.15		0.695	0.715	
E1	13.95	14.05		0.549	0.553	
E3	12.00		Reference	0.472		Reference
e1	1.00		Reference	0.0394		Reference
L	0.65	0.95		0.026	0.037	
N	52			52		

Drawing X2 44 Pin Ceramic PGA



Rev. 6

Family: Ceramic Pin Grid Array Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.81	4.83		0.150	0.190	
A1	1.27		Typical	0.050		Typical
A2	1.78	2.29		0.070	0.090	
B	0.41	0.51	Diameter	0.016	0.020	Diameter
B1	1.19		Typical Dia.	0.047		Typical Dia.
D	21.21	21.97		0.835	0.865	
D2	17.78		Reference	0.700		Reference
E	21.21	21.97		0.835	0.865	
E2	17.78		Reference	0.700		Reference
e1	2.54		Reference	0.100		Reference
L	3.30		Typical	0.130		Typical
N	44			44		

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A) Life support devices or systems are devices or systems which 1) are intended for surgical implant into the body, or 2) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury or death to the user,

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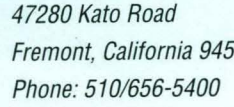
Rev. 1.4

Notes:



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Printed in U.S.A. 2/92