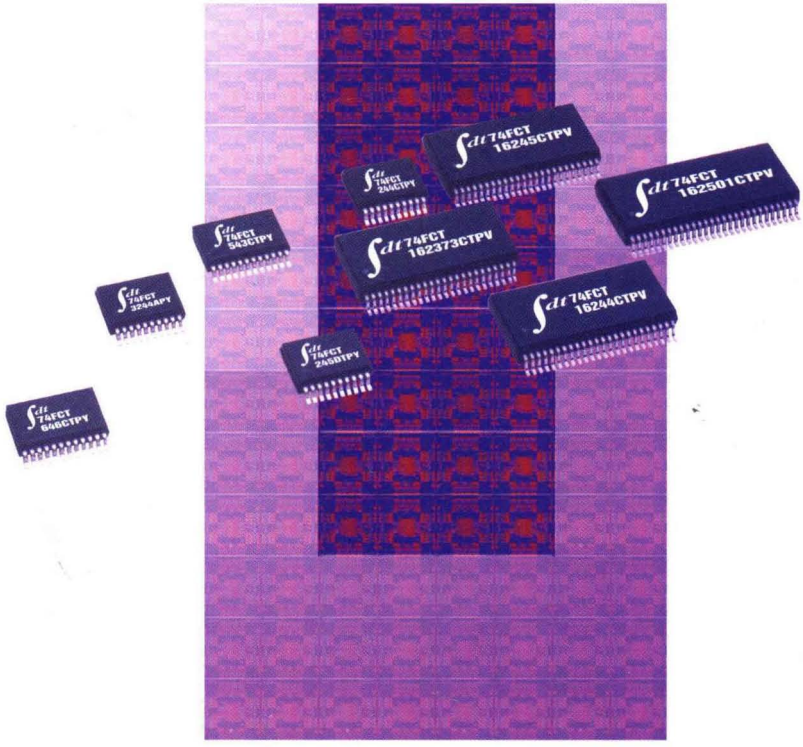
1993
IDT High-Speed CMOS Logic Design Guide

Includes Double-Density and
3.3V Application Notes



Integrated Device Technology, Inc.

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High Speed CMOS
Logic Design Guide

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

INTRODUCTION

This collection of application notes and conference papers is presented to provide information which has been proven useful to the designers who use or plan to use high-speed TTL-compatible, CMOS logic in high-performance systems. These notes cover a broad range of topics; some discuss aspects of **high-speed design** with new application notes specifically related to the new Double-Density family. Also included are application notes on **error detection and correction**.

Double-Density Family Defined

The demand for higher integration and high speed continues to push the need for high-performance, high-density logic families. IDT has recently introduced a new series of extra-quiet, high-performance, 16-, 18-, and 20-bit logic functions. This exciting new family offers users significant board area savings, power savings, higher speeds, excellent guaranteed low noise characteristics, and guaranteed low output skew. The Double-Density family is the premiere octal upgrade and is considered the high-speed, low-power replacement for all existing CMOS and BiCMOS wide bus width products.

High Speed Design

With the push for higher clock rates to increase system performance in a predominantly TTL world, the hardware designer is now required to deal with problems and issues which were largely academic only a few years ago. The introduction of high-speed, high-drive CMOS logic, combined with the increased packing density of multi-layer boards has resulted in the awareness and the need to deal with problems such as ground bounce, transmission line effects, and dynamic power dissipation.

Error Detection and Correction

Today's high-performance systems are becoming increasingly DRAM intensive. IDT has developed a range of high-performance EDC devices that eliminate the performance penalties once associated with these circuits while assuring the designer continuous, error-free operation necessary in high-reliability systems.

ABOUT THE PRODUCT SELECTOR GUIDE

Pages 2–5 contain the 1993 IDT Logic Product Selector Guide. The data book page numbers are preceded by the alpha character "G". This signifies the IDT 1992/1993 High-Performance Logic data book. Following the character will be the section number and the page number, consecutively. "CALL" might appear in the page number area as well. This means the data sheet was not included in the data book. A copy of the data sheet may be obtained by contacting IDT's Literature Department at (800) 345-7015 [(408) 492-8674], or from your local sales representative.

Shaded areas indicate new products introduced since the last publication of the product selector guide.

Boldface type indicates an improved IDT product feature.

The availability column shows the date when limited production quantities will be available.

The symbol "■" after the data book page number indicates further updated information has become available since the publication of the 1992/1993 High-Performance Logic data book. This information should be available from your local IDT sales office.

High-Speed CMOS Logic Products — Bus Interface Devices

- FCT and FCT-T CMOS families are the fastest in the industry with maximum propagation delays as low as 3.6 ns.
- The FCT-T family offers the lowest-power solution. No other logic family uses less dynamic power, standby power, or static high or low power.
- The clock driver family provides guaranteed low-skew clock distribution in a variety of configurations.
- The new Double-Density bus interface family offers users significant board area savings, power savings, higher speeds, guaranteed low noise, and a choice of output drive characteristics. Three configurations are available:
  1. Standard 64mA high drive device for bus and backplane interface.
  2. 24mA balanced output drive with on-chip resistors for internal bus and point to point driving.
  3. 3.3V bus interface logic for systems with 3.3V regulated supplies.
- The EDC (Error Detection and Correction) devices can detect multiple errors as fast as 10ns and correct as fast as 14ns.
- IDT features a series of read-write buffers with 8&18 bit bidirectional registers and 16-bit pipeline registers.
- The DSP Building Blocks are composed of 16-bit ALUs, Multipliers, and Multiplier-Accumulators with speeds as fast as 20ns.
- Parity generation and checking circuits designed to minimize part count and maximize parity checking time.

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page	
FCT/FCT-T FAMILY							
IDT29FCT52A/B/C IDT29FCT52AT/BT/CT/DT	Non-inverting Octal Registered Transceiver	7.3	**4.5**	1.0	NOW	G 6.26 G 6.1	
IDT29FCT53A/B/C IDT29FCT53AT/BT/CT	Inverting Octal Registered Transceiver	7.3	6.3	1.0	NOW	G 6.26 G 6.1	
IDT29FCT520A/B/C IDT29FCT520AT/BT/CT/DT	Multi-level Pipeline Register	7.0	**5.2**	1.0	NOW	G 6.27 G 6.2	
IDT29FCT521AT/BT/CT/DT	Octal Multi-level Pipeline Register (level 1 replaced)	7.0	**5.2**	1.0	NOW	G 6.2	
IDT54/74FCT138/A/C IDT54/74FCT138T/AT/CT	1-of-8 Decoder	6.0	5.1	1.0	NOW	G 6.29 G 6.3	
IDT54/74FCT139/A/C IDT54/74FCT139T/AT/CT	Dual 1-of-4 Decoder	6.2	5.0	1.0	NOW	G 6.30 G 6.4	
IDT54/75FCT151T/AT/CT	8-Input Multiplexer	6.2	5.6	1.0	NOW	G 6.5	
IDT54/74FCT157T/AT/CT/DT	Quad 2-input Multiplexer	5.0	**3.9**	1.0	NOW	CALL	■
IDT54/74FCT161/A IDT54/74FCT161T/AT/CT	Synchronous Binary Counter w/Synchronous Reset	6.3	5.8	1.0	NOW	G 6.31 G 6.7	
IDT54/74FCT163/A IDT54/74FCT163T/AT/CT	Synchronous Binary Counter w/Asynchronous Master Reset	6.3	5.8	1.0	NOW	G 6.31 G 6.7	
IDT54/74FCT182/A	Carry Lookahead Generator	10.7	7.0	1.0	NOW	G 6.32	
IDT54/74FCT191/A	Up/Down Binary Counter	10.5	7.8	1.0	NOW	G 6.33	
IDT54/74FCT193/A	Up/Down Binary Counter	6.9	6.5	1.0	NOW	G 6.34	
IDT54/74FCT240/A/C IDT54/74FCT240T/AT/CT/DT	Inverting Octal Buffer Line Driver	4.7	**3.6**	1.0	NOW	G 6.35 G 6.10	
IDT54/74FCT241/A/C IDT54/74FCT241T/AT/CT/DT	Inverting Octal Buffer Line Driver	4.6	**3.6**	1.0	NOW	G 6.35 G 6.10	
IDT54/74FCT244/A/C IDT54/74FCT244T/AT/CT/DT	Inverting Octal Buffer Line Driver	4.6	**3.6**	1.0	NOW	G 6.35 G 6.10	
IDT54/74FCT3244/A	3.3V Inverting Octal Buffer Line Driver	—	**4.8**	1.0	NOW	G 7.7	
IDT54/74FCT245/A/C IDT54/74FCT245T/AT/CT/DT	Inverting Octal Buffer Transceiver	4.5	**3.8**	1.0	NOW	G 6.36 G 6.11	
IDT54/74FCT3245/A	3.3V Inverting Octal Buffer Transceiver	—	**4.6**	1.0	NOW	G 7.8	
IDT54/74FCT257T/AT/CT/DT	Quad 2-input Multiplexer w/OE	5.0	**3.9**	1.0	NOW	CALL	■
IDT54/74FCT273/A/C IDT54/74FCT273T/AT/CT/DT	Octal D Flip-Flop with Reset	6.5	5.8	1.0	NOW	G 6.37	
IDT54/74FCT299/A/C IDT54/74FCT299/AT/CT	Octal Universal Shift Register w/Common Parallel I/O Pins	7.5	6.5	1.0	NOW	G 6.38 G 6.13	
IDT54/74FCT373/A/C IDT54/74FCT373T/AT/CT/DT	Octal Transparent Latch	5.1	**3.8**	1.0	NOW	G 6.39 G 6.14	

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page
IDT54/74FCT374/A/C IDT54/74FCT374T/AT/CT/DT	Octal D Register	6.2	**4.2**	1.0	NOW	G 6.40 CALL ■
IDT54/74FCT377/A/C IDT54/74FCT377T/AT/CT/DT	Octal D Flip-Flop w/Clock Enable	5.5	**4.4**	1.0	NOW	G 6.41 G 6.16
IDT54/74FCT399/A IDT54/74FCT399T/AT/CT	Quad Dual-Port Register	6.6	6.1	7.0	NOW	G 6.42 G 6.17
IDT54/75FCT521/A/B/C IDT54/74FCT521T/AT/BT/CT	8-Bit Identity Comparator	5.1	4.5	1.0	NOW	G 6.43 G 6.18
IDT54/74FCT533/A/C IDT54/74FCT533T/AT	Inverting Octal Transparent Latch w/3-State	5.1	4.7	1.0	NOW	G 6.39 G 6.14
IDT54/74FCT534/A/C IDT54/74FCT534T/AT/CT	Inverting Octal D Register w/3State	6.2	5.2	1.0	NOW	G 6.40 G 6.15
IDT54/74FCT540/A/C IDT54/74FCT540T/AT/CT	Inverting Octal Buffer/Line Driver	4.7	4.3	1.0	NOW	G 6.35 G 6.10
IDT54/74FCT541/A/C IDT54/74FCT541T/AT/CT	Non-Inverting Octal Buffer/Line Driver	4.7	4.3	1.0	NOW	G 6.35 G 6.10
IDT54/74FCT543/A/C IDT54/74FCT543T/AT/CT/DT	Non-Inverting Octal Latched Transceiver	6.1	**4.4**	1.0	NOW	G 6.44 G 6.19
IDT54/74FCT573/A/C IDT54/74FCT573T/AT/CT/DT	Octal Transparent Latch	5.1	**3.8**	1.0	NOW	G 6.39 G 6.19
IDT54/74FCT574/A/C IDT54/75FCT574T/AT/CT/DT	Octal D Register w/ 3-State	6.2	**4.2**	1.0	NOW	G 6.40 G 6.15
IDT54/74FCT620T/AT/CT	Inverting Octal Bus Transceiver w/3-State	5.1	4.5	1.0	NOW	G 6.21
IDT54/74FCT621T/AT	Non-Inverting Octal Bus Transceiver w/Open Drain	12.5	12.0	1.0	NOW	G 6.22
IDT54/74FCT623T/AT/CT	Non-Inverting Octal Bus Transceiver w/3-State	5.4	4.8	1.0	NOW	G 6.21
IDT54/74FCT640/A/C IDT54/74FCT640T/AT/CT	Inverting Octal Transceiver	4.7	4.4	1.0	NOW	G 6.36 G 6.11
IDT54/74FCT645/A/C IDT54/74FCT645T/AT/CT/DT	Non-Inverting Bidirectional Transceiver	4.5	**3.8**	1.0	NOW	G 6.36 G 6.11
IDT54/74FCT646/A/C IDT54/74FCT646T/AT/CT/DT	Octal Transceiver/Register	6.0	4.4	1.0	NOW	G 6.45 G 6.20
IDT54/74FCT648T/AT/CT	Octal Transceiver/Register	6.0	5.4	1.0	NOW	G 6.20
IDT54/74FCT651T/AT/CT	Inverting Octal Registered Transceiver	6.0	5.4	1.0	NOW	G 6.20
IDT54/74FCT652T/AT/CT/DT	Non-Inverting Octal Registered Transceiver	6.0	**4.4**	1.0	NOW	G 6.20
IDT54/74FCT821A/B/C IDT54/74FCT821AT/BT/CT	10-Bit Non-Inverting Register	7.0	6.0	1.0	NOW	G 6.46 CALL ■
IDT54/74FCT823A/B/C IDT54/74FCT823AT/BT/CT/DT	9-Bit Non-inverting Register	7.0	**5.0**	1.0	NOW	G 6.46 G 6.23
IDT54/74FCT825A/B/C IDT54/74FCT825AT/BT/CT	8-Bit Inverting Register	7.0	6.0	1.0	NOW	G 6.46 G 6.23
IDT54/74FCT827A/B/C IDT54/74FCT827AT/BT/CT/DT	10-Bit Non-Inverting Buffer	5.0	**3.8**	1.0	NOW	G 6.47 G 6.24
IDT54/74FCT828AT/BT/CT/DT	10-Bit Inverting Register	5.0	**3.8**	1.0	NOW	G 6.24
IDT54/74FCT833A/B	8-Bit Transceiver w/Parity	10.0	7.0	1.0	NOW	G 6.48
IDT54/74FCT841A/B/C IDT54/74FCT841AT/BT/CT/DT	10-Bit Non-Inverting Latch	6.3	**4.2**	1.0	NOW	G 6.49 G 6.25
IDT54/74FCT843A/B/C IDT54/74FCT843AT/BT/CT	9-Bit Non-Inverting Latch	6.3	5.5	1.0	NOW	G 6.49 G 6.25

High-Speed CMOS Logic Products

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page	
IDT54/74FCT845A/B/C IDT54/74FCT845AT/BT/CT	8-Bit Non-Inverting Latch	6.3	5.5	1.0	NOW	G 6.49 G 6.25	
IDT54/74FCT861A/B/C	10-Bit Non-Inverting Transceiver	6.5	6.0	1.0	NOW	G 6.50	
IDT54/74FCT863A/B/C	9-Bit Non-Inverting Transceiver	6.5	6.0	1.0	NOW	G 6.50	
CLOCK DRIVER FAMILY							
IDT49FCT805/A	Clock Driver w/Guaranteed Skew	6.8	5.8	1.0	NOW	G 6.28	
IDT49FCT805BT/CT		—	4.5	1.0	MAR'93	CALL	■
IDT49FCT806/A	Inverting Clock Driver w/Guaranteed Skew	6.8	5.8	1.0	NOW	G 6.28	
IDT49FCT806BT/CT		—	4.5	1.0	MAR'93	CALL	■
IDT49FCT807AT	1:10 Clock Driver w/Guaranteed Skew	—	3.5	1.0	MAR'93	CALL	■
IDT49FCT810AT	Inverting/Non-InvertingClock Driver w/Guaranteed Skew	—	4.5	1.0	JUNE'93	CALL	■
IDT54/74FCT88915	Low Skew PLL-Based Clock Driver	N/A	N/A	1.0	Q2'93	CALL	■
5V DOUBLE-DENSITY FAMILY							
IDT54/74FCT16240T/AT/CT IDT54/74FCT162240T/AT/CT	16-Bit Buffer/Line Driver	4.7	4.3	0.006	NOW	G 5.1 G 5.1	
IDT54/74FCT16244T/AT/CT IDT54/74FCT162244T/AT/CT	16-Bit Buffer/Line Driver	4.6	4.1	0.006	NOW	G 5.2 G 5.2	
IDT54/74FCT16245T/AT/CT IDT54/74FCT162245T/AT/CT	16-Bit Bidirectional Transceivers	4.5	4.1	0.006	NOW	G 5.3 G 5.3	
IDT74FCT16357T/AT	12-Bit Tri-Port Bus Exchanger	—	6.0	0.006	MAR'93	CALL	■
IDT54/74FCT16373T/AT/CT IDT54/74FCT162373T/AT/CT	16-Bit Transparent Latches	5.1	4.2	0.006	NOW	G 5.4 G 5.4	
IDT54/74FCT16374T/AT/CT IDT54/74FCT162374T/AT/CT	16-Bit Register (3-State)	6.2	5.2	0.006	NOW	G 5.5 G 5.5	
IDT54/74FCT16646T/AT/CT IDT54/74FCT162646T/AT/CT	16-Bit Bus Transceiver/Registers (3-State)	6.0	5.4	0.006	NOW	G 5.9 G 5.9	
IDT54/74FCT16500AT/CT IDT54/74FCT162500AT/CT	18-Bit Registered Bus Transceiver (3-State)	5.1	4.6	0.006	NOW	G 5.6 G 5.6	
IDT54/74FCT16501AT/CT IDT54/74FCT162501AT/CT	18-bit Registered Bus Transceiver (3-State)	5.1	4.6	0.006	NOW	G 5.7 G 5.7	
IDT54/74FCT162511AT/CT	18-Bit Registered Transceiver w/ Parity	—	4.6	0.006	NOW	CALL	■
IDT54/74FCT16543T/AT/CT/DT IDT54/74FCT162543T/AT/CT/DT	16-Bit Latched Transceiver	6.1	**4.4**	0.006	NOW	G 5.8 G 5.8	
IDT54/74FCT16952T/AT/CT/DT IDT54/74FCT162952T/AT/CT/DT	16-Bit Registered Transceivers	7.3	**4.5**	0.006	NOW	G 5.11	
IDT54/74FCT16651T/AT/CT	16-Bit Transceiver/Registers	6.0	5.4	0.006	NOW	CALL	■
IDT54/74FCT16652T/AT/CT IDT54/74FCT162652T/AT/CT	16-Bit Transceiver/Registers	6.0	5.4	0.006	NOW	G 5.10	
IDT74FCT162701T	18-Bit R/W Buffer	—	5.3	0.006	NOW	CALL	■
IDT54/74FCT16823AT/BT/CT IDT54/74FCT162823AT/BT/CT	18-Bit Bus Interface Registers	7.0	6.0	0.006	NOW	G 5.12	
IDT54/74FCT16827AT/BT/CT IDT54/74FCT162827AT/BT/CT	20-Bit Buffers	5.0	4.4	0.006	NOW	G 5.13	
IDT54/74FCT16841AT/BT/CT IDT54/74FCT162841AT/BT/CT	20-Bit Latches	6.3	5.5	0.006	NOW	G 5.14	
3.3V DOUBLE-DENSITY FAMILY							
IDT54/74FCT163244/A	3.3V CMOS 16-Bit Buffer/Line Driver	—	**4.8**	0.006	NOW	G 7.1	
IDT54/74FCT163245/A	3.3V CMOS 16-Bit Bidirectional Tranceivers	—	4.6	0.006	NOW	G 7.2	

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Data Book Page
IDT54/74FCT164245T	CMOS 16-Bit Bidirectional 3.3V to 5V Translator	—	6.3	0.006	NOW	G 7.9
IDT54/74FCT163373/A	3.3V CMOS 16-Bit Bidirectional Latches	—	5.2	0.006	NOW	G 7.3
IDT54/74FCT163374/A	3.3V CMOS 16-Bit Register	—	**5.2**	0.006	NOW	G 7.4
IDT54/74FCT163646/A	3.3V CMOS 16-bit Bus Transceiver/ Registers	—	**6.3**	0.006	NOW	G 7.6
IDT54/74FCT163501/A	3.3V 18-Bit Registered Bus Transceiver	—	**5.1**	0.006	NOW	G 7.5
ERROR DETECTION AND CORRECTION		**Detect Time**				
IDT39C60 IDT39C60-1 IDT39C60A IDT39C60B	16-bit Cascadable EDC Replaces Am2960, -1, A; N2960, MC74F2960, -1, A	36 28 24 22	32 25 20 18	300	NOW NOW NOW NOW	G 8.10
IDT49C460 IDT49C460A IDT49C460B IDT49C460C IDT49C460D	32-bit Cascadable EDC Replaces Am29C660. Functional equivalent to DP8402; AS/ALS632	44 33 28 21 16	40 30 25 16 12	350	NOW NOW NOW NOW NOW	G 8.11 G 8.11 G 8.11 G 8.11 G 8.11
IDT49C465/A	32-bit Flow-thruEDC™ two separate bidirectional 32-bit buses; expandable to 64-bit, 144-pin PGA.	15	20	400	NOW	G 8.12
IDT49C466	64-bit Flow-thruEDC—two separate bidirectional 64-bit buses; 208-pin PGA	**25**	20	500	NOW	G 8.13
READ-WRITE BUFFERS						
73200	16-bit 8-level-deep pipeline Register; replaces four Am29520s	12	10	150	NOW	G 8.7
73201	16-bit 7-level-deep pipeline Register with pass-through mode	12	10	150	NOW	G 8.7
73210/A/B	8-bit bidirectional registers with parity; two registers from B to A	7.5	6.0	50	NOW	G 8.8
73211/A/B	8-bit bidirectional registers with parity; one register from B to A	7.5	6.0	50	NOW	G 8.8
73720/A	16-bit tri-port Bus Exchanger	—	6.0		NOW	G 8.9
DSP BUILDING BLOCKS						
IDT7381	16-bit cascadable ALU (replaces Logic Devices' L4C381)	**20**	**16**	150	NOW	G 8.6
IDT7383	16-bit cascadable ALU (32 instructions)	**20**	**16**	150	NOW	G 8.6
IDT7210L	16 x 16-bit with 35-bit output, replaces TDC1010J	**20**	**16**	225	NOW	G 8.4
IDT7216L	16 x 16-bit, replaces Am29516	**20**	**16**	200	NOW	G 8.5
IDT7217L	16 x 16-bit with single-clock architecture, replaces Am29516	**20**	**16**	200	NOW	G 8.5
MICROSLICE™ PRODUCTS		**(Com'l.)**				
IDT49C402 IDT49C402A IDT49C402B	16-Bit zμP Slice, quad 2901 with 8 additional destination functions and 64 x 16 register file capacity—superset of Am29C101, CY7C9101, WS159016	A,B addr to Y = 47ns A,B addr to Y = 37ns A,B addr to Y = 28ns		350	NOW NOW NOW	G 8.2
IDT39C10B IDT39C10C	12-bit Sequencer with 33-deep stack —replaces AM2910/A, CY7C910	D to Y = 20ns D to Y = 12ns		150	NOW NOW	G 8.2
IDT49C410 IDT49C410A	16-bit Sequencer with 33-deep stack address up to 64K microcode	D to Y = 20ns D to Y = 12ns		150	NOW NOW	G 8.3

Integrated Device Technology, Inc.

DOUBLE-DENSITY™ LOGIC CHARACTERISTICS AND APPLICATIONS

APPLICATION NOTE AN-117

By Anupama Hegde and Stanley Hronik

INTRODUCTION

The increasing demand for integration in computer systems has lead to the evolution of logic components with wider buses and highly integrated functionality. Shorter delays and fewer components are welcome features when board space and performance are at a premium. With such increased integration and increased clock speeds, power dissipation and simultaneous switching noise become important issues. In the light of such developments, IDT has introduced a new 16-bit wide logic family - **Double-Density** - to address the system designer's need for increased performance, reduced noise and low power dissipation. The family not only doubles the number of bits in a single package but also offers users other features such as a small package size, extremely low power dissipation, low leakage, reduced ground bounce and a very friendly user interface. The Double-Density logic family is an extension of IDT's Fast CMOS TTL-compatible (FCT-T) line of logic products. These devices are built using IDT's submicron CMOS 5E technology.

The Double-Density logic family consists of three subfamilies, each of which seeks to address specific design needs. The first is the **High-Drive FCT16xxxT** family, designed for backplane and other applications that require a high static and dynamic output drive capability. The second is the **Balanced-Drive FCT162xxxT** family. This family features a balanced output drive and has excellent noise characteristics, which is a central issue to most high-speed applications. The last is the **Low Voltage (3.3V), FCT163xxx family** which is aimed at low-power, high-performance design applications. For a detailed discussion of the FCT163xxx family, please refer to Logic Application Note, AN-103 ("3.3V Logic"). All three Double-Density sub-families offer lower power solutions than their industry counter parts.

This application note discusses IDT's Double-Density High-Drive and Balanced-Drive families which are designed to give the best cost/performance ratio in a variety of applications. It provides useful information needed to evaluate and/or design in these devices. The focus is on the families' features and benefits, product characteristics and design guidelines. The application note is divided into several sections, each dealing with a specific characteristic or feature of the family. Design information and actual data on the Double-Density FCT16xxxT and FCT162xxxT families are provided in the form of graphs and tables making them easier to interpret and access. In cases where the characteristics are common to both the FCT16xxxT and FCT162xxxT families, only one graph is given for both families.

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DOUBLE-DENSITY LOGIC FAMILIES

Description

IDT's Double-Density product line is comprised of 16, 18 and 20-bit fast CMOS interface parts available in 48 and 56 pin dual-in-line surface mount packages. Three broad families are available to serve different market segments.

FCT16xxxT High-Drive Family

The key features of the FCT16xxxT family are high static and dynamic drive. This family includes drivers which a suitable for driving low-impedance busses, back planes or heavily terminated lines while retaining excellent noise immunity. Certain standards such as the VME bus electrical specification require a high static output drive for which FCT16xxxT devices are a good choice. Low-impedance and high-capacitance driving ability are the hallmarks of the High-Drive family.

FCT162xxxT Balanced-Drive Family

The FCT162xxxT family offers controlled edge rates and Balanced-Drive resulting in reduced undershoot and overshoot. Balanced-Drive components significantly reduce board level noise and solve many of the transmission line problems that develop with high-speed logic.

The Balanced-Drive output structure has been designed to match the impedance of a typical transmission line for effective line driving. This is accomplished through a symmetric pull-up and pull-down current drive capability during transitions, and through integrated source-termination. The source termination emulates external series termination without severely limiting the drive capability of the device. The Balanced-Drive characteristics provide transmission line matching for signals undergoing both HIGH and LOW transitions. In addition, controlled output transitions reduce EMI and RFI effects. The main features of the Balanced-Drive family are reduced ground bounce, fewer line reflections and smaller over/undershoot making it very effective for point-to-point line driving. For further details on the Balanced-Drive implementation refer to Appendix A.

FCT163xxx Low-Voltage(3.3V) Family

IDT's LOW Vcc family is intended for use with a regulated 3.3V power supply and has been developed to maintain system speed at lower voltages. A benefit of using the reduced power supply is the significant reduction in the overall system power consumption. These devices will interface with the future and existing 3.3V devices. The family is designed to be TTL compatible and meets the JEDEC standard 8-1A for low-voltage interfacing. Another benefit of the low-voltage family is the decreased switching noise due to a reduction in overall output voltage swing. These devices are ideal for use in laptop and notebook computer designs. Space applications will also benefit from the lower noise and power levels from using a lower Vcc. IDT's low-voltage 163xxx family uses the same process technology as the other 5V Double-Density families, meaning that at 3.3V supply, the 163xxx family provides an excellent reliability margin due to minimal part stress.

DOUBLE-DENSITY FAMILY FEATURES

IDT's **Double-Density** FCT16xxxT and FCT162xxxT device families are an extension of the IDT FCT-T(**F**ast **C**mos **T**TL-compatible - **T**TL level output swings) family. Many of the features discussed in this application note are common to all three Double-Density families, but since this document deals exclusively with the FCT16xxxT High-Drive and the FCT162xxxT Balanced-Drive devices, all further references to IDT Double-Density are used in connection with these last two families.

Functions

Double-Density devices, as the name indicates, are comprised of two byte-wide functions on a single die, in a single package. These components offer 16, 18 or 20-bit bus widths with control signals for each group of 8, 9 or 10 bits (for standard functions) that correspond to their octal counterparts. This allows designers to use these new devices without changing their system architecture. Most of the popular octal functions are available in the Double-Density family.

In addition to the dual byte-wide functions, there are several new functions available in Double-Density which broaden the product line offerings beyond the octal capabilities. These products take advantage of the larger pin counts of the packages by offering increased functionality while providing single control pins for both bytes.

Speed Grades

The Double-Density components are specified at the same speed as the industry standard FCT/FCT-T family. This means that existing designs can be upgraded to reduce space and improve performance with very little effort.

Operating Range

IDT Double-Density family components have been characterized and specified over the extended commercial temperature range (industrial range) of –40 °C to +85°C and the power supply(Vcc) range of ±10% to be consistent with the trend to offer system designers a wider operating range and greater operating margin.

DC ELECTRICAL CHARACTERISTICS

INPUT CHARACTERISTICS

The input structure of the FCT16xxxT and FCT162xxxT Double-Density families is shown in Figure 1. The equivalent circuit for the input stage includes the ESD protection circuit, input clamp diode, TTL-CMOS translator and the hysteresis circuit.

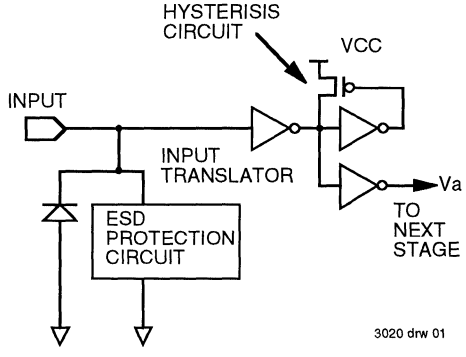

Figure 1. Input Circuit for Double-Density FCT16xxxT and FCT162xxxT

All of the inputs for the Double-Density family are designed with 100mV of hysteresis in the input stage as shown in Figure 2. Due to the hysteresis, the effective LOW-to-HIGH and HIGH-to-LOW switching thresholds are separated. This feature improves both static and dynamic noise margins. It is also useful in providing immunity against overriding noise associated with slowly ramping inputs.

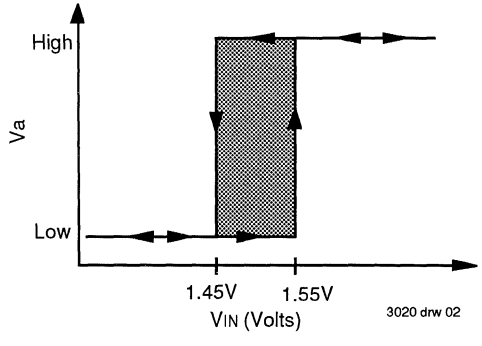

Figure 2. Double-Density Transfer Characteristic showing hysteresis

The typical input V-I characteristics for the High-Drive and Balanced-Drive Double-Density devices are shown in Figure 3. In the normal input operating voltage range of 0 to 5V, practically zero current is drawn by the input stage. The input stage offers very high-impedance and; therefore, low leakage currents (<+/–5µA). When the input voltage is one diode turn-on voltage below ground, the input clamp diode turns on as shown by the increase in current around –0.6V. The diode clamps negative voltage spikes at the input.

Balanced-Drive and High-Drive devices have no clamp diode to Vcc at the input. Consequently, voltages much higher than Vcc can be tolerated with input breakdown occurring at approximately 14V as shown in Figure 3. These characteristics apply to pure inputs only, whereas I/O(input/output) pins will follow the characteristics shown in Figure 8.

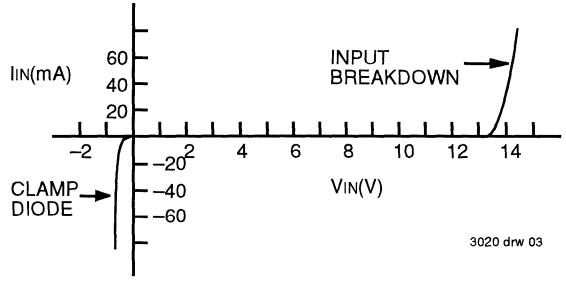

Figure 3. Double-Density Input Characteristics

Although breakdown occurs at approximately 14V, the absolute maximum steady state input voltage rating for reliable device operation is limited to a lower level. FCT16xxxT can tolerate a steady state voltage of 7V at inputs and I/O pins while FCT162xxxT can tolerate 7V at inputs and Vcc + 0.5V at I/O pins. Beyond this, long term reliability of the device may be affected.

The absolute maximum voltage specification of GND –0.5V for all pins on both the FCT16xxxT and FCT162xxxT, and Vcc +0.5V for I/O and output pins on the Balanced-Drive part refers to a steady-state condition. The specification does not imply that the device cannot withstand transient overshoots/undershoots greater than the rated values. Under transient conditions, the device is expected to withstand an overshoot of 7V or an undershoot of –3V for 20ns regardless of clamp diodes. While the part will not sustain damage from these overshoots/undershoots, it is possible that false switching may occur if there are device inputs sitting at a marginal voltage level or if other marginal conditions exist.

In addition to the above, Double-Density devices have the advantage of extremely-low input capacitance where typical values range from 3 to 5pF. This makes it possible for a high-impedance source elsewhere on the board to drive many Double-Density inputs.

OUTPUT CHARACTERISTICS

The output stage of FCT16xxxT and FCT162xxxT devices has a "totem pole" configuration with N-channel pulldown and N-channel pullup transistors. The N-channel pull-up in the output stage reduces the output swing to TTL levels by limiting the output voltage in a logic HIGH state to around 3.5V (TTL logic high level). A simplified output circuit for the High-Drive family is shown in Figure 4a and a circuit for the Balanced-Drive family is shown in Figure 4b.

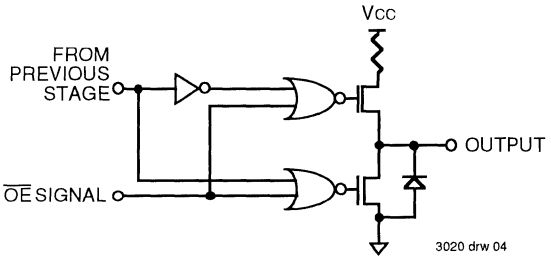

Figure 4a. Output Circuit for FCT16xxxT

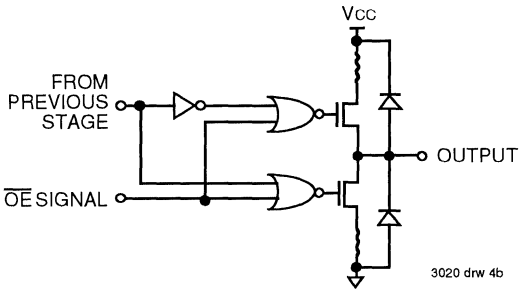

Figure4b. Output Circuit Schematic for FCT162xxxT

The FCT16xxxT and FCT162xxxT families both have resistors in the drain of the device pull up structure giving the two families similar pull-up capabilities. The clamp diode to Vcc in the pull up of the FCT162xxxT does not affect the output characteristics of the device if the output voltage remains between Vcc and ground. The typical logic high output impedance characteristics are shown in Figure 5 for both FCT16xxxT and FCT162xxxT devices. In the logic HIGH state, the output impedance, as obtained from the linear portion of the V-I characteristic, is 28Ω.

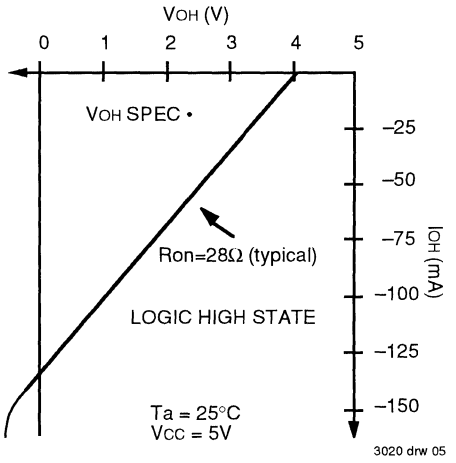

Figure 5. Logic High Output Characteristics

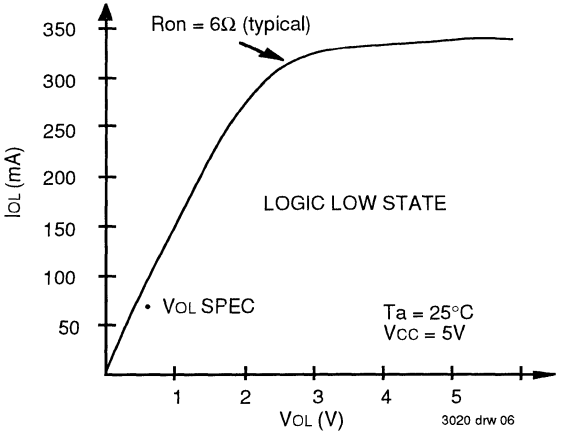

Figure 6. FCT16xxxT Logic LOW Output Characteristics

The typical output characteristics are different for the two families for the logic LOW state. This is because of a different pull down structure for the Balanced-Drive (FCT162xxxT) family which includes a resistor in the source of the pull down transistor. Because of this, the Balanced-Drive part has a higher output impedance when pulling down than the High-Drive part.

The typical V-I curve for the High-Drive logic low state is shown in Figure 6. From the chart it can be seen that the output impedance for the logic LOW state is about 6Ω which is sufficiently LOW to allow the part to drive low-impedance loads such as backplanes operating at high speeds.

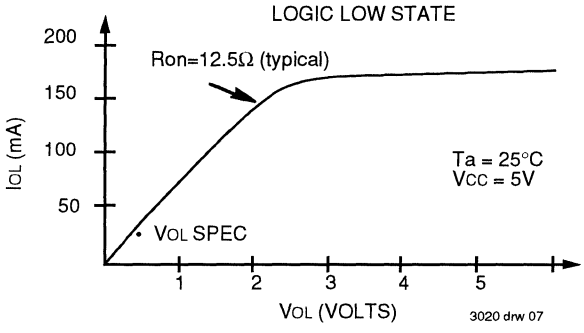

Figure 7. FCT162xxxT Logic LOW Output Characteristics

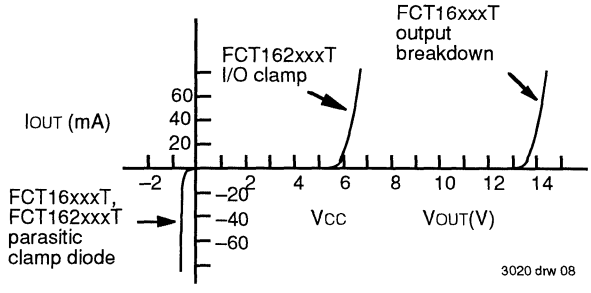

Figure 8. Output High-Z Characteristics for FCT16xxxT and FCT162xxxT

The V-I curve for the Balanced-Drive part is shown in Figure 7 and shows an output impedance of about 12.5Ω. This gives the Balanced-Drive family enhanced output edge rate control which improves the signal characteristics during transitions and improves the overshoot and undershoot characteristics of the device. Due to differences in the output structure of the Balanced-Drive from that of the High-Drive part, the Balanced-Drive will exhibiit about 0.5ns less propagation delay for the HIGH-to-LOW transition than the High-Drive part for loads of less than 200pf. A discussion of this can be seen in Appendix A.

As the graphs show, the actual device static drive current under typical conditions is larger than that indicated by the datasheet specifications. The typical dynamic drive current during switching will be much larger than the data sheet static specification and can also be seen from the charts. For example, a device driving a capacitive load, upon switching, will easily drive over 100mA dynamic current until the load acquires the new state. The dynamic switching current for the FCT162xxxT family is specified in the data book at 115mA (typical for both directions), but the FCT16xxxT switching current will be much higher for the transition to a logic LOW.

The output V-I characteristics (pure outputs and I/O) for FCT16xxxT and FCT162xxxT in the high-impedance state are shown in Figure 8. Under normal operating voltages, in the high-Z state, the pull-up and pull-down transistors are off and the output current is small (50μA), as revealed by an almost flat line, close to zero on the current axis of the V-I graph. For output voltages one diode voltage drop below ground, the parasitic diode of the N-channel pull-down transistor turns on, clamping the voltage at around 0.6V. For output voltages above Vcc, since the FCT16xxxT devices have no parasitic diode to Vcc, breakdown occurs at approximately 14V which gives the **Power-Off Disable** feature. FCT162xxxT devices have a parasitic diode to Vcc at their outputs and hence voltages above Vcc+0.5V are clamped. The user must maintain static output voltages within the maximum ratings stated in the datasheets in order to maintain reliable operation.

The Power-Off Disable feature is useful in interface applications where one side of the interface may intentionally or inadvertently become unpowered. Some of the applications where this is possible include Hot Insertion where a board is installed into an active, powered system or where a cable may accidently become disconnected or attached to a live system. The power off disable feature of the FCT16xxxT family ensures that the device outputs will remain in the high-impedance state when Vcc=0V and that there is no path through which voltage applied to an output can raise the supply rail of the powered down device.

Applications which may require the Power-Off Disable feature include power conserving systems, fault tolerant systems, telecommunications, networking systems and backplanes. These applications may use Power-Off Disable to power off unused portions of the system to conserve power, allow the replacement of faulty boards in an active system, or switch portions of a network in and out without disrupting network communications. Refer to AN-102 [6] for a detailed discussion on the Power-Off Disable feature.

Any signal pin of an FCT16xxxT device may be at any voltage within the ABSOLUTE MAXIMUM VOLTAGE rating for the input while the device is powered off. During the power-off state, the device supply voltage is at 0V and the device outputs remain in high-impedance, hence there is no contention when plugging such a device into an active bus. Devices having this feature specify an "IOFF" current in the datasheet. This is a measure of the leakage current at the outputs when Vcc=0V.

During power ramping, control ($\overline{OE}$) signals must be suitably conditioned to ensure that the outputs remain in the high-Z state. For negative assertion output enable pins, the output enable should be tied to a logic HIGH (>Vcc/2). When the outputs of these devices are so conditioned, all 3-state outputs will offer high-impedance independent of the power supply (within ABSOLUTE MAXIMUM Vcc limits). At Vcc levels of less than 1.5V, the device outputs will not turn on, regardless of the state of the output enable.

The FCT162xxxT family does not have the Power-Off Disable feature. The presence of a diode to Vcc at the outputs of these devices creates a DC path to the supply pin during power-off conditions precluding use of these devices in power-off situations.

POWER DISSIPATION

Power calculations are done to determine power supply sizing, cooling/heat sink requirements and criteria for device selection. Power calculations can also determine maximum reliable operating frequency.

Power dissipation calculations for High-Drive and Balanced-Drive parts are discussed below.

Power dissipation in an unloaded device is
$P_{D(unloaded)} = V_{CC} \times I_C$
where I_C= Total power supply current

The total power supply current, I_C, in CMOS circuits has 3 power supply current components:

(1) I_{CC} - Static or quiescent power supply current, specified at V_{IN} = GND or V_{CC}.

(2) ΔI_{CC} - Power supply current through input translator for TTL level logic high inputs, specified at V_{IN} = 3.4V.

(3) I_{CCD} - Dynamic power supply current due to switching of internal circuitry and outputs.

The total power supply current is the sum of these three components for unloaded conditions. So,

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} \times N_D \times f$
where N_T = Number of TTL level inputs
D_H = Duty cycle of TTL level input
N_D = Number of switching bits
f = Switching Frequency

Static Power Supply Current (I_{CC})

This component is typically very small for CMOS devices. It represents current from V_{CC} to ground through leakage paths. Double-Density components have a typical quiescent power supply current of 50 µA.

Static Power Supply Current Due to TTL Level Inputs (ΔI_{CC} or I_{CCQT})

ΔI_{CC} or I_{CCQT} is the current component associated with TTL level inputs and is specified in mA per input at 3.4V (TTL level). Figure 9 shows ΔI_{CC} as a function of VIN at room temperature and at V_{CC} = 5.5V. The input translator of a CMOS device input (Figure 1) plays a significant role in these characteristics. If V_{TN} and V_{TP} are the threshold voltages of the n and p channel transistors of a CMOS stage respectively, then for $V_{IN} < V_{TN}$ or $V_{IN} > V_{CC} - V_{TP}$, only one of the transistors of the input translator is on and the other is off. Hence, the current drawn from the supply is very small. For $V_{TN} < V_{IN} < V_{CC} - V_{TP}$, both the pull-up and pull-down transistors are partially on and current is drawn from the supply. The ΔI_{CC} is maximum at the switching threshold (nominally 1.5V for FCT/FCT-T at V_{CC}=5V) and progressively tapers off for input voltages greater or less than this.

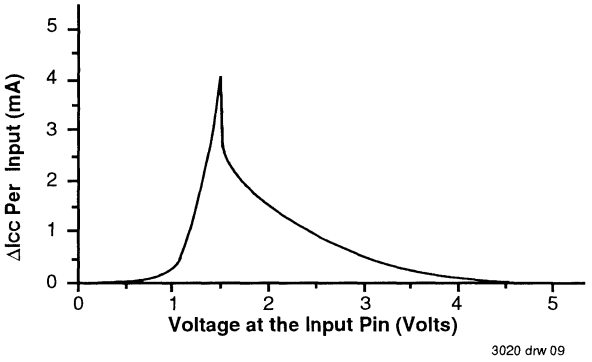

Figure 9. ΔI_{CC} vs Vin Characteristics

Note that the graph shows this component for a single bit. To find the total ΔI_{CC} one must multiply the datasheet value by the number of inputs at 3.4V and the switching duty cycle,as indicated in the equation for I_C.

Dynamic Power Supply Current (I_{CCD})

The last component is I_{CCD} or the dynamic switching current. This component of current represents the charging and discharging of the internal gate capacitance, and the charging and discharging of the device output drivers with no load. I_{CCD}, which is specified in terms of mA/MHz/bit, is dependent upon the switching frequency and the number of bits switching. Some manufacturers specify C_{PD} or dynamic power dissipation capacitance which can be used to calculate I_{CCD} as follows:

$$C_{PD} = I_{CCD} \text{ (in } \mu A/MHz/bit \text{)} / V_{CC}$$

The output drivers of a device are responsible for a large portion of the dynamic power dissipation. If a device is being switched with the output drivers disabled (3-state), I_{CCD} will be significantly reduced. The typical value of I_{CCD} for the Double-Density devices in the unloaded condition is 60µA/MHz/bit. To find the total dynamic power supply current , I_{CCD} value must be multiplied by the number of bits switching.

Dynamic power dissipation may change considerably with loading. Switching of the load in addition to the device capacitance (C_{PD}) adds a factor to the total power supply current as shown in the equation below :

I_{CCD} (loaded) = I_{CCD} (unloaded) + fC_LV_{OH}
where C_L = Load Capacitance

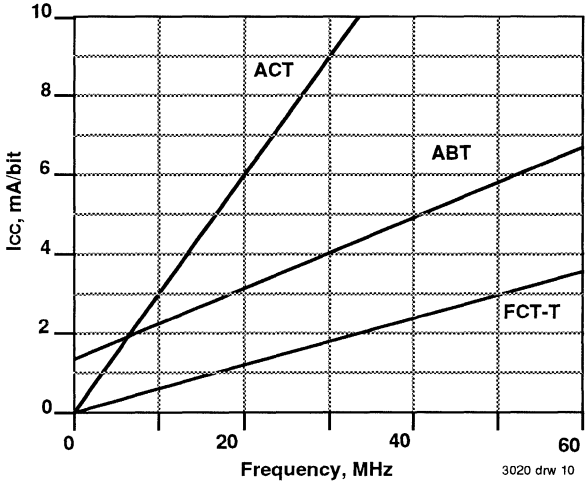

Figure 10. ICC vs Frequency (no output loading)

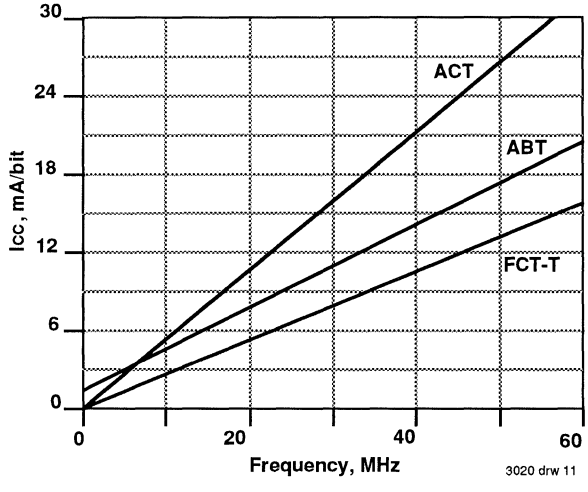

Figure 11. ICC vs Frequency (with 50pF output loading)

Figure 10 shows the total power supply as a function of frequency for various 16-bit logic families. Figure 11 shows a similar graph for the loaded case. The total supply current in these graphs includes the static and dynamic power supply components but not ΔI_{CC} as the inputs are at CMOS levels. inputs. Because of their internal structure, bipolar technologies have a larger static or quiescent power component than CMOS. CMOS has almost zero power dissipation under static conditions due to the fact that one transistor of the CMOS pair is off in a valid logic state leading to a high-impedance path between Vcc and ground.

It is seen that power dissipation characteristics of both FCT16xxxT and FCT162xxxT families are similar. Total power dissipation, under typical operating conditions, however, is an important Figure of merit. A common argument against CMOS families in the past has been that although they have a very low-static power, at higher frequencies they consume more total power than corresponding Bipolar/BiCMOS parts, due to a larger dynamic power supply component. This may have been true for older technologies. The Double-Density family, however, has dynamic power dissipation characteristics that are much superior to older CMOS technologies and existing advanced BiCMOS logic families.

As an example of a power comparison between ABT and FCT-T with no load (Figure 10), an FCT-T part will consume the same current level at 34MHz as ABT at 8MHz. It should also be noted that when the devices are not switching, ABT consumes a significant static current level while FCT will approach zero in current consumption.

STATIC AND DYNAMIC DRIVE

Drive is one of the key features that differentiates the FCT16xxxT and FCT162xxxT Double-Density families. High-Drive devices are specified at 64/–32mA static drive while the Balanced-Drive devices are specified at 24/–24mA static. The static drive is the current that the device is continuously capable of sourcing or sinking in a stable logic state. It is typically specified at the minimum V_{OH} or the maximum V_{OL}.

Dynamic drive is the transient output current that the device can sink or source during a HIGH-to-LOW or a LOW-to-HIGH transition. Dynamic drive is not always specified in datasheets, but it can be determined from the device V-I graphs. Static drive indicates the ability of the device to maintain static noise margins in the presence of a DC load. It is the current at which V_{OH} and V_{OL} are specified. Dynamic drive, on the other hand, indicates the ability of the device to charge and discharge capacitive loads while meeting the AC performance limits and incident wave switching requirements.

Unless there is a DC load on the line or a low-impedance line (e.g. a loaded backplane) is being driven, a large static drive is typically not required to drive CMOS devices to valid logic levels. Due to their large input impedance and low-input current requirements, CMOS devices do not require a driver with a large static drive capability except in the case of low-resistive termination. Dynamic drive, however, plays a more important role since it determines the speed derating with capacitive loading.

FCT162xxxT devices have a modest static drive compared to FCT16xxxT devices; but, as indicated by datasheet specifications, they have ample dynamic drive (typically > 100 mA at 1.5V). Due to the particular implementation of the source termination, unlike some other series terminated parts, the FCT162xxxT devices do not suffer from lack of drive due to the additional impedance.

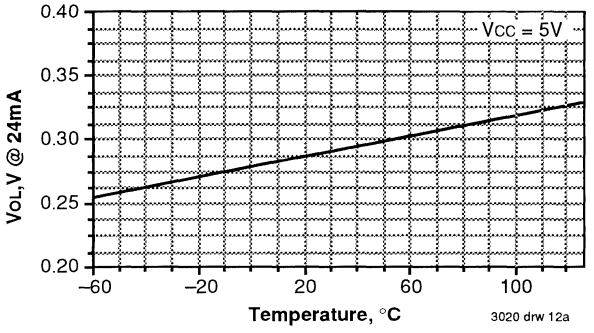

Figure 12a. VOL vs Temperature at VCC = 5V

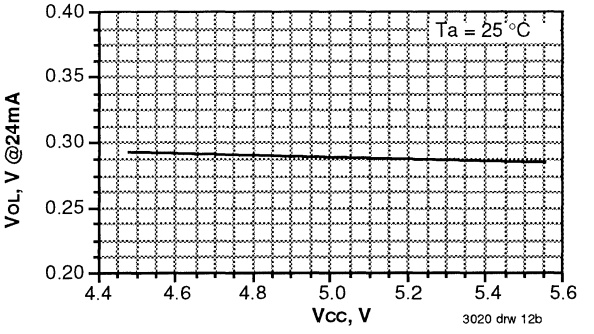

Figure 12b. VOL vs VCC at 25°C

Because of the excellent noise characteristics of Balanced-Drive devices, it is in the best interest of the designer, to use Balanced-Drive parts unless high static drive is essential. Figures 12a and 12b show the variation of VOL with temperature and VCC at a drive current of 24mA static drive. Figures 13a and 13b show similiar characteristics for VOH at –24mA static drive. Refer to appendix B for standard datasheet specifications.

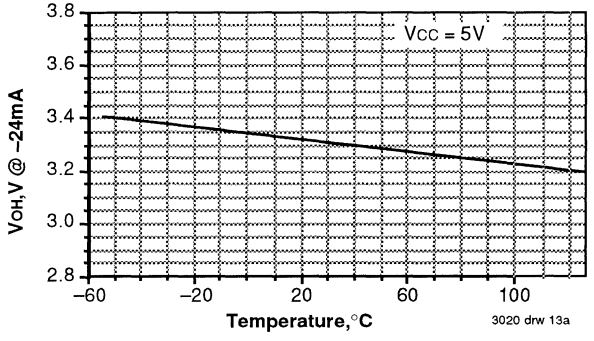

Figure 13a. VOH vs Temperature at VCC = 5V

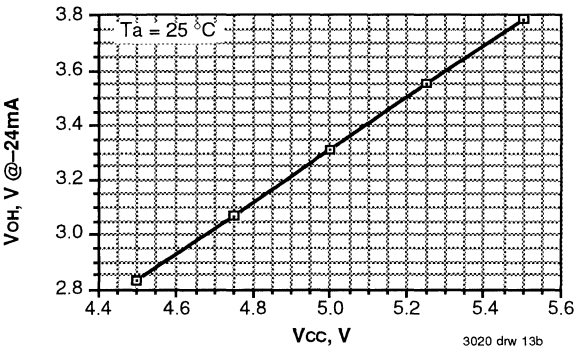

Figure 13b. VOH vs VCC at 25°C

AC PERFORMANCE

AC TEST CONDITIONS

Double-Density is offered in the same speed grades as the octal FCT and FCT-T devices. With different speed grades available, the designer can choose cost/performance trade-offs for the overall system implementation. The following chart shows the commercial speed grades for four of the most popular Double-Density functions.

Function	Standard Speed(1)	Aspeed(1)	C Speed(1)
244	6.5	4.8	4.1
245	7.0	4.6	4.1
373	8.0	5.2	4.2
374	10.0	6.5	5.2

3020 tbl 01

NOTE:
1. All speeds in ns.

AC limits of the Double-Density family are specified over extended commercial, industrial and military temperature ranges. VCC tolerance is ±10 % for both commercial and military devices. The limits are based on the worst case operating conditions with VCC = 4.5V and TA = 85°C for commercial grade limits and TA = 125°C for military grade limits. All AC parameters are measured using the industry standard load shown in Figure 14. AC tests are done with a single bit switching and timings may need to be derated for the worst case of 16/18/20-bits switching simultaneously.

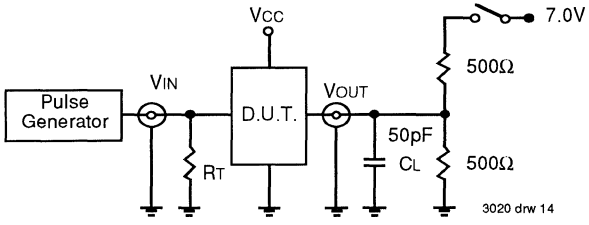

Figure 14. Standard Logic Test Load

The 50pF capacitance in the standard load allows for stray and parasitic capacitances due to the ATE test fixture. In most measurements the switch is in the open position. The 500Ω resistors offer a nominal DC load and help establish "artificial" logic levels for testing enable and disable time parameters.

In many cases, the test load may not be a true representation of a customer's load. When the loading is lighter, the limits may be used as a worst case, but when the loading is heavier they may need to be derated. Also the system under consideration may normally operate in a narrower temperature and/or Vcc range. In such circumstances, it is useful to have the option to derate for the different variables that affect the AC characteristics. In order to serve this purpose a variety of derating graphs are provided in the following sections.

PROPAGATION DELAY

DELAY AS A FUNTION OF TEMPERATURE

Figures 15 and 16 show the normalized graphs of propagation delay as a function of temperature for FCT16xxxT and FCT162xxxT. The FCT16244T and FCT162244T are used as a basis for these graphs.

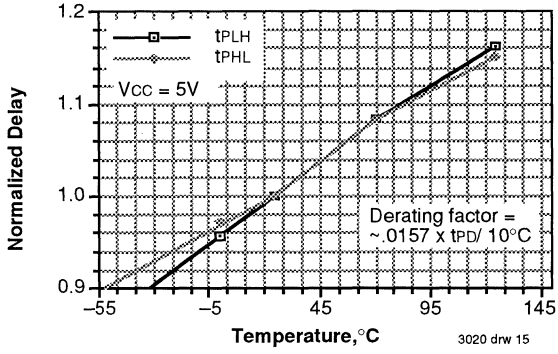

Figure 15. FCT16xxxT Delay vs Temperature

Propagation delay is related to the current available for charging and discharging the internal and external capacitances. The current itself depends on a number of process parameters, which vary with temperature. As a result, propagation delay has a temperature gradient as shown.

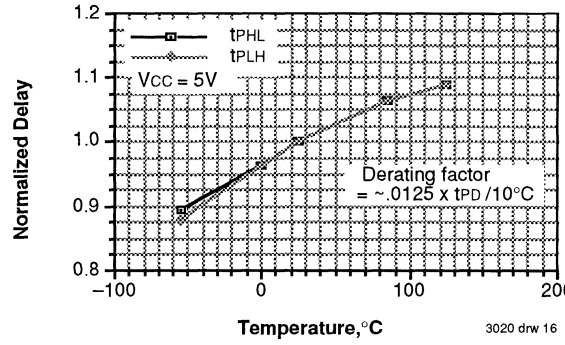

Figure 16. FCT162xxxT Delay vs Temperature

Note: Due to the similarity in output structure, the graphs are representative of the characteristics of all devices belonging to the same family.

Derating factors are useful in accounting for the effect of a variable on a specific parameter. For example given a temperature derating factor of 0.0157tPD/10°C for FCT16xxxT, the FCT16245CT (delay spec = 4.1ns) when operating at 25°C can be assumed to have a delay of:

$$t_{PD} = [4.1 - 0.015 \times 4.1\ (85\text{-}25)/10] = 3.73\text{ns max}$$

Delay as a Function of Supply Voltage

Figures 17 and 18 show the normalized graphs of propagation delay as a function of supply voltage. Again the data is based on the FCT16244T and FCT162244T, but is representative of all devices within each of these families. With an increase in Vcc the current available for charging and discharging goes up and hence the propagation delays go down. For reduced Vcc, the current goes down and there is an increase in the propagation delay.

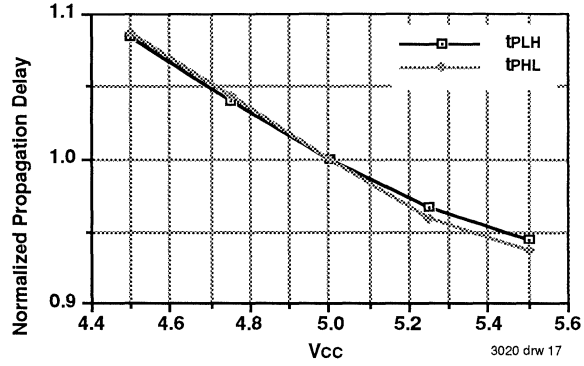

Figure 17. FCT16xxxT Delay vs VCC

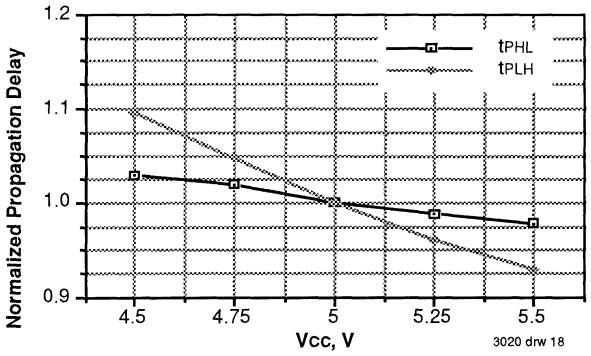

Figure 18. FCT162xxxT Delay vs Vcc

Delay as a Function of Number of Outputs Switching

The AC characteristics are tested and specified for single bit switching. In reality, multiple bits can switch simultaneously generating internal noise which causes the observed propagation delays to change. Figure 19 shows the change in propagation delay as a function of number of outputs switching. The data for this graph is based on the FCT16245T and FCT162245T.

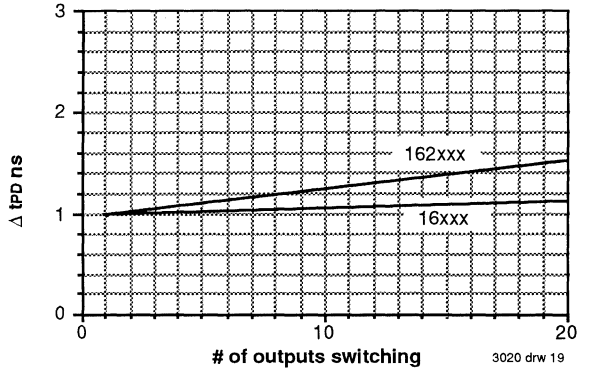

Figure 19. FCT16xxxT and FCT162xxxT Delay vs # of Outputs Switching

Delay as a Function of Load

The AC characteristics are tested and specified for a standard load of 50pF. One needs to derate AC parameters for loading conditions greater than the standard load.

Figures 20 through 22 show the change in propagation delay as a function of external load. These characteristics are essentially linear and can be extrapolated. Large load capacitances require more time to charge and discharge casuing longer propagation delays, where as smaller loads will charge and discharge more quickly. Designers can derate at about 3ns/100pF worst case or 1.5ns/100pF typically. Loads above 400pf may draw significant current levels when switching at high frequencies and the designer must be careful not to exceed the maximum power dissipation specifications.

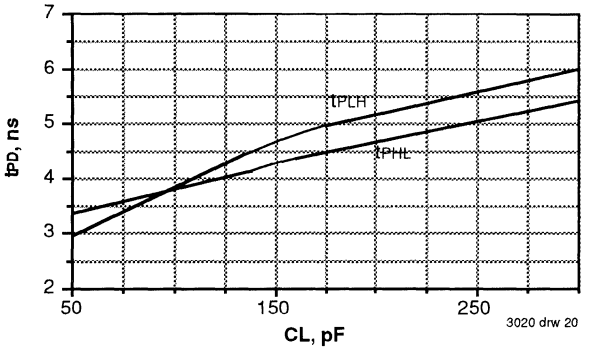

Figure 20. FCT16xxxT Delay vs Load

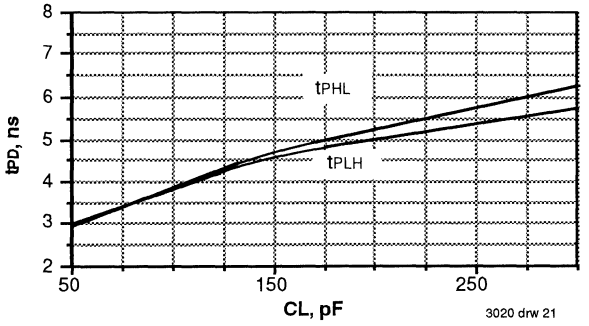

Figure 21. FCT162xxxT Delay vs Load

Figures 20 and 21 are based on data for the FCT16245T and FCT162245T.

RISE AND FALL TIMES

With shrinking geometries and improvements in processing technology, devices are becoming faster and edge rates are increasing. Given today's technology, edge rates of 1V/ns to 2V/ns are common and for such fast edges one needs to consider transmission line effects on PCB traces. Application Note AN-49 [3] describes the characteristics of PCB traces in detail.

If the transition time of the signal is shorter than the round trip propagation delay of the transmission line, the line may need termination to maintain quiet operation. For short traces the signal reaches the receiving end quickly and reflections are absorbed by and add to the transitioning signal. For longer traces, the signal makes a complete transition at the source before the signal can reach the receiving end and be reflected. The reflection from the signal then is considered noise and may distort the waveform of the signal.

These signal transition times are affected by the output loading conditions as shown by the variation of Trise and Tfall as a function of loading in Figures 22 and 23. For standard loading with high-speed logic such as IDT's FCT-T, any line longer than 8 inches is a potential transmission line and may need termination to maintain quiet operation. The FCT162xxxT family has intermal termination which will reduce many of these problems.

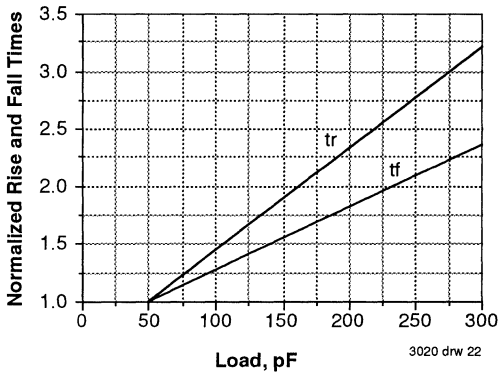

Figure 22. FCT16xxxT Trise and Tfall vs Load

The edge rate of a device into a given standard load is important to users because it is a measure of the inherent speed of the device as opposed to external factors such as load or system clock frequency. The rise and fall times of the device are defined as the time interval between the 10 and 90 percent (of the steady state value) voltage levels. Typical edge rates per this definition looking into a standard 50pF, 500Ω load, for the FCT16xxxT and FCT162xxxT families are:

Trise = 2.8ns
Tfall = 1.7ns (FCT16xxxT)
Tfall = 2.5ns (FCT162xxxT)

As the capacitive loading to the device output is increased. the output edge rates will slow down as shown in Figure 22, for the FCT16xxxT family, and Figure 23, for the FCT162xxxT family.

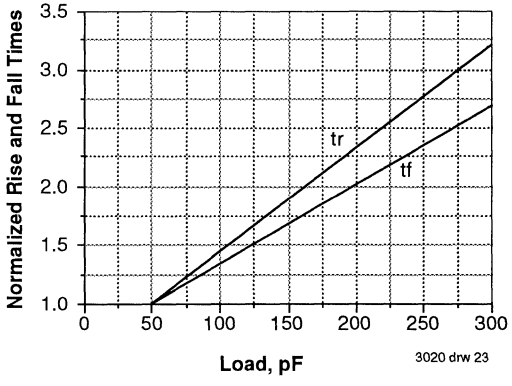

Figure 23. FCT162xxxT Trise and Tfall vs Load

ENABLE AND DISABLE TIMES

Like propagation delay and rise and fall times, enable and disable times also vary with temperature and Vcc. Figures 24, 25, 26 and 27 show the variation of enable time with temperature and Vcc and are based on data taken on the FCT16245T and FCT162245T. Variation of disable time is more a function of the load than the device itself. Therefore derating of disable time is independent of the device but depends on the temperature and Vcc coefficients of the load.

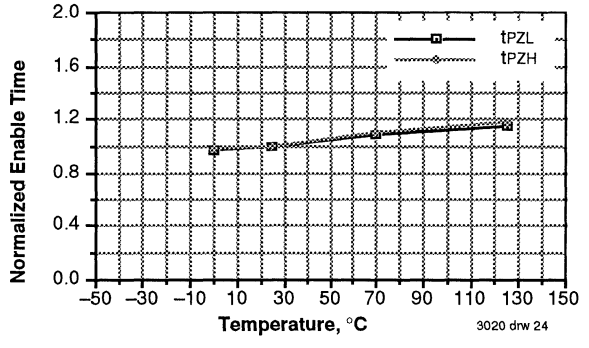

Figure 24. Enable Time vs temperature for FCT16xxxT

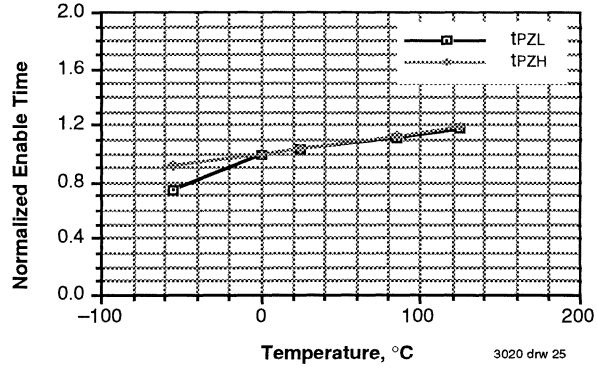

Figure 25. Enable Time vs Temperature for FCT162xxxT

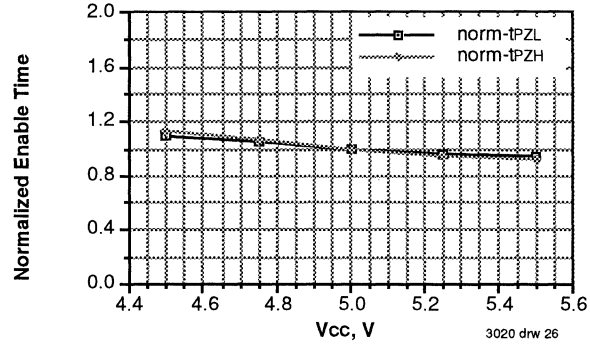

Figure 26. Enable Time vs Vcc for FCT16xxxT

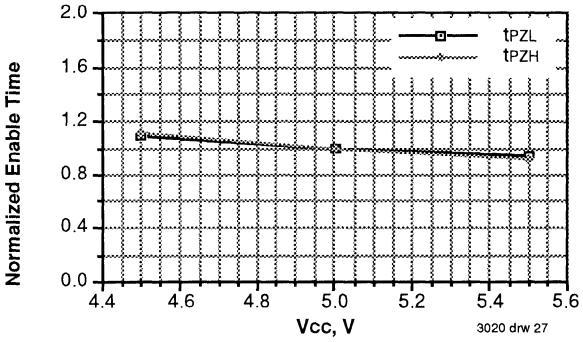

Figure 27. Enable Time vs VCC for FCT162xxxT

SKEW

Skew reflects the worst case propagation delay difference between the different outputs. Skew results from design (routing/placement), process and packaging specific to the device. For the user, as the clock frequency goes up, timing margins become tighter. Signal skew makes the timing margin even tighter. Reduction in the spread of the output propagation delays results in reduced skew and improved timing margins.

There is a tendency among designers to compute the difference between the maximum and minimum specifications and use this Figure as the worst case skew; however, this is not a realistic measure of skew because the maximum (worst case) and minimum (best case) delays occur under mutually exclusive conditions of temperature, power supply voltage and process. In order to provide the user with the required information, Double-Density devices have an output skew specification of 0.5ns maximum between outputs on the same device. For further discussion on types of skew, the reader is referred to Application Note AN-82[8].

SIMULTANEOUS SWITCHING NOISE

In a digital circuit when multiple outputs switch, the current through the ground or Vcc lead changes rapidly. As this current flows through the ground (or Vcc) return path, it develops a voltage across the parasitic inductance of the bond wire and package pin. This phenomenon is called simultaneous switching noise. The noise is seen as ground bounce or Vcc bounce and can cause problems such as data loss and false triggering in a system. For a detailed discussion of ground bounce the reader is directed to Application Note AN-47 [4]. Ground and Vcc bounce cannot be entirely eliminated, but they can be minimized by controlling edge rates, reducing output swing and providing multiple power, ground and Vcc pins. Double-Density has 8 ground pins and 4 Vcc pins. This is a marked improvement over the ground distribution in the octal devices and manifests itself in the noise characteristics of the device. Ground bounce depends on many factors with device speed being one of the important influences. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. Due to this correlation between speed and ground bounce, high-speed logic families arouse increased concern over noise due to the simultaneous switching of outputs .

The standard method of measuring ground bounce involves keeping one output in a logic LOW state and switching all other outputs at a given frequency (1MHz typical). The quiet output will reflect the bounce on the internal device ground. Similarly Vcc bounce can be observed by keeping one output in the logic HIGH state. The naming convention for ground bounce characterization is as follows :

VOLP = Peak positive ground bounce on a LOW output
VOLV = Peak negative ground bounce on a LOW output
VOHP = Peak positive Vcc bounce on a HIGH output
VOHV = Peak negative Vcc bounce on a HIGH output

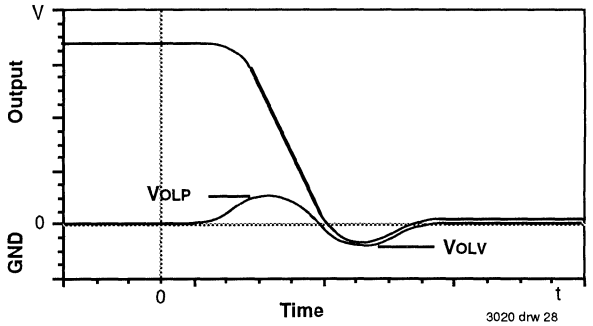

Figure 28. Ground Bounce for HIGH-to-LOW Transitions

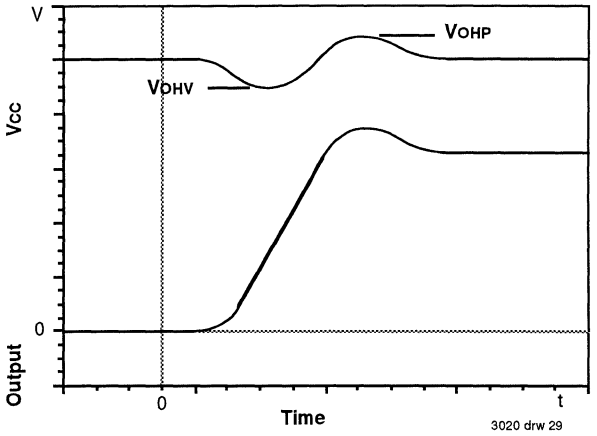

Figure 29. Vcc Bounce for LOW-to-HIGH Transitions

The "ground bounce" phenomenon is primarily dependent on the output edge rate, number of outputs switching and package lead inductance. Other factors that can affect ground bounce are the output swing and drive. Most current technology consists of TTL-compatible logic where the output drivers can be made to pull the outputs from rail-to-rail with a P-channel pullup transistor ("CMOS level outputs") or they may

drive the output to approximately 3V with an n-channel pullup ("TTL-level outputs"). The equations below illustrate why the ground bounce is higher with CMOS level output swings.

$$i = C_L \frac{dV_O}{dt} \quad ...(i)$$

where,

V_O = Output voltage
C_L = load capacitance
V_g = voltage induced on ground pin
L_g = inductance at the ground pin

$$V_g = L_g \frac{di}{dt} \quad ...(iia)$$

using (i) in (iia), we get -

$$V_g = L_g C_L \frac{d^2V_O}{dt^2} \quad ...(iib)$$

Because of the lower voltage swing, TTL level outputs give better noise immunity than CMOS, rail swing, output levels.

The other factor affecting ground bounce is output drive. The higher the output current, the greater the switching noise. This is evident from the equation (iia) above.

FCT16xxxT/162xxxT devices are available in SSOP and Cerpack packages. These packages have multiple ground and Vcc pins, giving multiple parallel paths and low inductance to the high-speed switching currents. The surface mount package avoids the inductance of through hole mounting and is the package configuration for high-speed logic. The combination of these package characteristics results in a significant reduction in the magnitude of simultaneous switching noise. Package dimensions and pin inductance values are shown in Appendix C.

Ground Bounce vs Number of Outputs Switching

Every logic family has a characteristic edge rate (for a given load condition) and every package has a fixed lead inductance. Hence given a specific family, package, and loading, a distinct correlation can be observed between the number of outputs switching and the amount of undershoot/overshoot due to ground bounce. Figure 30 illustrates this relationship for the Double-Density devices in an SSOP package.

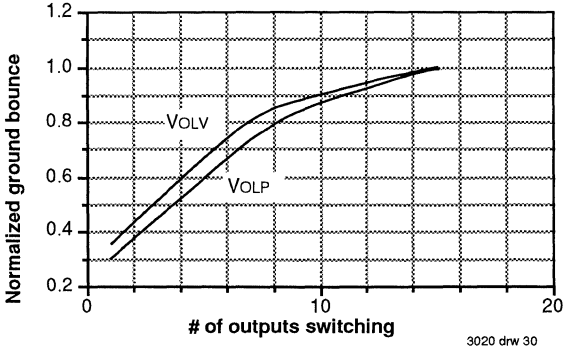

Figure 30. Double-Density ground bounce vs number of outputs switching (16-bit function)

Ground Bounce vs Load

Simultaneous switching noise is affected by the output loading. As the value of the load capacitance increases, the charge stored in the capacitance is increased. The larger charge implies a slower rate of discharge through the package parasitics and hence lower ground bounce as shown in Figures 31 and 32. Another way to look at it is, the load slows down the signal transition increasing the transition time and reducing ground bounce.

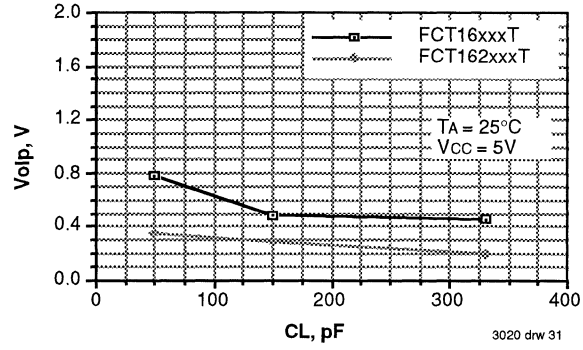

Figure 31. VOLP vs Load

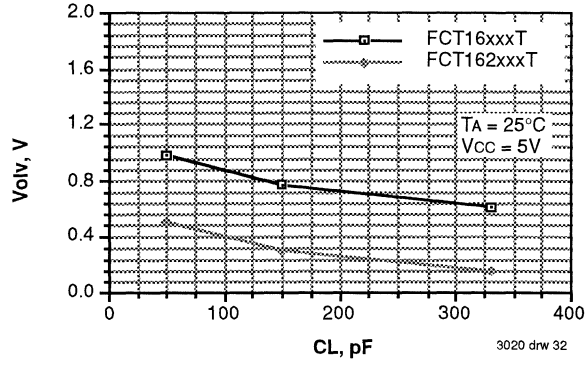

Figure 32. VOLV vs load

MISCELLANEOUS ISSUES

ESD

There are two standard methods to characterize ESD, the machine model and the human body model. Double-Density devices meet MIL-STD-883 (Method 3015) Class 2 ESD level requirements. This means that they can withstand voltage levels greater than 2KV (4KV typical) under the human body model test methodology. With the machine model test methodology, Double-Density ESD tolerance is greater than 200V. Storage of devices in protective foam and the use of a ground strap during handling are standard precautions.

DECOUPLING

Good decoupling techniques are required to achieve optimum noise and performance levels from Double-Density components. The multiple ground and Vcc pins on the SSOP and Cerpack packages reduce the effect of the lead inductance of the devices, but do not provide a single point for the capacitor. The best style and location of the decoupling capacitor is the use of a surface mount chip capacitor placed directly over the component, on the reverse side of the board. An alternative location for boards with components on one side only is to place the capacitor at either end of the component. The capacitor should have a LOW series inductance and resistance in order to maximize the effect of the capacitance. The function of the capacitor is to provide a low-impedance path to high-frequency components, while also satisfying the load's initial high-current requirements.

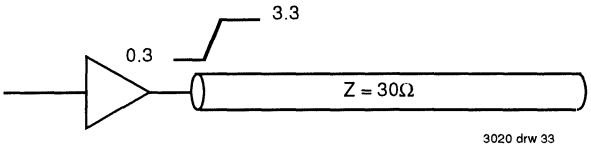

Figure 33. Buffer Driving a Loaded Trace

As an example of a decoupling situation, Figure 33 shows a driver driving a 30Ω transmission line as could be encountered when driving a heavily loaded backplane. When the output of the buffer switches LOW-to-HIGH, about 100mA (dynamic) drive is required [(3.3 - 0.3)/30 = 100]. For 16 bits switching simultaneously 1.6A dynamic drive is required. For a Vcc drop of 0.1V and a 3ns rise time on the signal, the value of the decoupling capacitor can be decided as shown below.

i = C(dV/dt) approximating this with deltas
1.6 = C(0.1/3x10**-9)
Hence, C = 0.048μF

With this calculation, the value of the capacitor can then be selected from the standard capacitor values. A capacitor equal to the value in the equation or larger should be selected to achieve the noise value decided upon. The value of 0.1μF is a good choice. The application note AN-116, Decoupling Double-Density Components, contains a complete discussion on capacitor selection and placement.

MAXIMUM INPUT RISE AND FALL TIMES

When an input rises or falls slowly, the noise overriding the input can cause the device to oscillate for some time before the output becomes steady. Such oscillations are not desirable because they cause the effective propagation delay to go up by a large amount, and affect system reliability. There is a restriction on the maximum input rise and fall time for reliable circuit operation. For FCT16xxxT, the slowest recommended rise and fall times on the device inputs are 50ns. The hysteresis circuit in the input stage (see Figure 2) helps in reducing the effect of noise on slowly changing inputs.

UNUSED INPUTS

The unused inputs of logic devices should not be left floating because these high-impedance inputs act like antennae and pick up noise. To prevent the noise on such inputs from switching the device and consuming extra power, all unused inputs must be connected to Vcc or ground, preferably via a current limiting series resistor to limit unwanted current surges.

SUMMARY

IDT has introduced the Double-Density logic family to meet the demands of high-performance systems. These high-integration components save board space while maintaining the compatibility with the older octal devices in terms of speed and functionality. Three different varieties are offered to meet to the users' diverse application needs. The standard High-Drive family is ideal for bus/backplane applications. The Balanced-Drive family has user friendly outputs for low noise, reliable systems. The 3.3V family is ideal for power-sensitive applications such as laptops and notebooks. The various characteristics, graphs, and information provided herein are intended to aid the designer in achieving desired cost/performance goals.

REFERENCES

[1] "Series Termination"(AN-50), High-Speed CMOS Logic Design Guide, IDT, Inc., November 1991.

[2] "Power Dissipation in Clock Drivers"(AN-51), High-Speed CMOS Logic Design Guide, IDT, Inc., November 1991.

[3] "Characteristics of PCB Traces"(AN-49), High-Speed CMOS Logic Design Guide, IDT, Inc., November 1991.

[4] "Simultaneous Switching Noise"(AN-47), High-Speed CMOS Logic Design Guide, IDT, Inc., November 1991.

[5] "3.3V Logic"(AN-103), IDT 3.3V Logic Product Information, IDT, Inc., February 1992.

[6] "Power off Disable in IDT Double-Density Devices"(AN-102), IDT, Inc., 1992-93.

[7] "Decoupling Double-Density Components"(AN-116), IDT, Inc.,1992.

[8] "Clock Distribution Simplified With IDT Guaranteed Skew Clock Drivers"(AN-82), Logic Databook, IDT, Inc., 1990-91.

APPENDIX A
BALANCED-DRIVE CAPABILITY

The output structure of the Balanced-Drive part (Figure 6) has been specifically designed to give similar transition times with matching absolute edge rates in both the high going and low going directions. This means the IDT Balanced-Drive Family has a matched dynamic drive capability for driving transmission lines, but still has sufficiently low static output impedance to maintain state during steady state conditions. As shown in Figure A1, during transitions the Balanced-Drive output structure will current limit at about 115mA typical forboth low-to-high and high-to-low transitions, limiting surge current into the transmission line, but still providing sufficient drive current to drive all except the most demanding loads. Limiting the pull down drive capability of the device during transitions also reduces problems with undershoot, ground bounce and general noise generation. In almost all applications, the Balanced-Drive part will generate less noise than BiCMOS components and the associated ringing that BiCMOS generates.

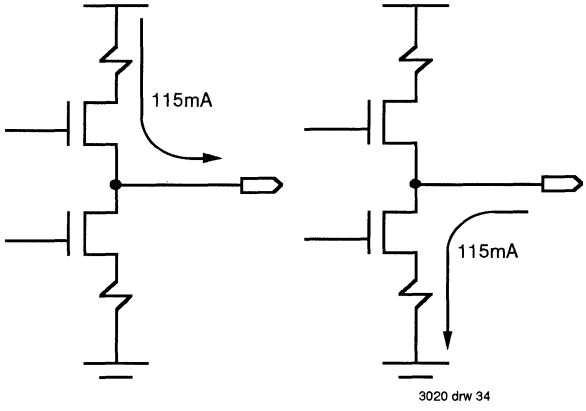

Figure A1, Dynamic Balanced-Drive Output

During steady state DC conditions, IDT specifies the static drive capability of the devices at 24mA worst case in both directions as shown in Figure A2. Balanced-Drive components will give better line matching than equivalent drivers with lower output impedance eliminating the need for external resistors in most cases.

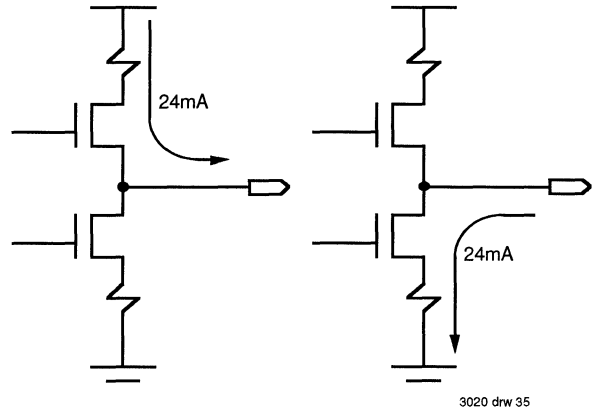

Figure A2, Static Balanced-Drive Output

Adding External Resistors to Balanced-Drive

With the Balanced-Drive components, the effective series termination impedance of 28Ω is slightly lower than the characteristic impedance of most transmission lines. Backplanes may sometimes approach levels as low as 30Ω, but most lines will have a higher impedance. Despite this difference, the current surge driven into the transmission line will be limited by the output impedance and controlled edge rate.

If it is desirable to further enhance the quiet operation and to achieve a close match between the source impedance and the line impedance, the user may add external resistors to the output of his Balanced-Drive parts. Because of the integrated resistor in the drain of the pull up FET, and the output structure of the Balanced-Drive part, the addition of an external series resistor will not cause significant attenuation of the output signal in the pull-up structure of the device as happens with standard TTL output components. This means that when series resistors are added to a Balanced-Drive part, the LOW-to-HIGH edge rate will retain similar characteristics to the HIGH-to-LOW edge rate. With similar edge rates, the performance and noise levels will be superior to situations where an external resistor has been added to a standard TTL output part.

Driving Capacitive Loads

Standard parts which have a low pull-down impedance and a high pull-up impedance have problems with RC time delays when driving capacitive loads. This is due to the inability to match the line impedance for both directions. Usually the addition of a large enough resistor to perform line matching in the pull down direction will cause significant degradation of the pull up capability of the part. IDT's Balanced-Drive parts have overcome this problem by providing equal line driving capability in both directions and will drive capacitive loads equally well in both directions with or without external resistors. This means that adding a series resistor will not degrade the speed of the part significantly because the effective line matching resistor will have a lower resistance value than one that would be used with a standard part.

IDT's Balanced-Drive and High-Drive components have very similar response times for capacitive loads of less than 300pf. Because of its quicker response, the Balanced-Drive part will switch faster than a High-Drive part for loads of less than 200pf. As the load increases above 200pf the High-Drive part will respond more quickly for a high-to-low because of its lower output impedance. Despite these minor differences the differences in the effects of capacitance on propagation delay between the High-Drive and Balanced-Drive parts should be less than 0.5ns for any load of less than 300pf. The capacitive derating curves are shown in Figure A3.

When the capacitive load is larger than 400pf at high switching speeds, the load will begin looking like a direct short upon switching and may begin to overdrive the output of both the Balanced-Drive and High-Drive part. The power dissipation equation is $P = fCV^2$ and should be used to calculate the power consumption for each pin to assure that the total power dissipation in the device does not exceed the maximum rated limits. To avoid exceeding the limit for heavy capacitive loads, a 100Ω series resistor can be used to limit the current to acceptable levels.

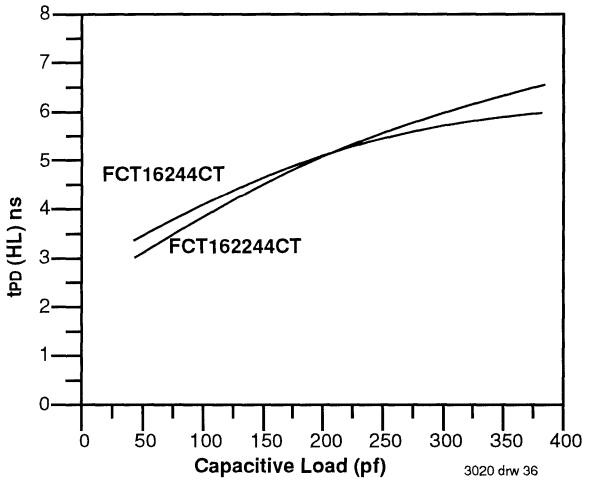

Figure A3, Capacitive Derating for Double Density Balanced-Drive and High-Drive

SUMMARY

Utilizing the Balanced-Drive family in high speed bus driving applications will solve most of the problems with noise and line termination experienced with traditional high-speed, low-output impedance line drivers. The Balanced-Drive logic family provides the benefits of series termination on signal lines while avoiding many of the drawbacks of adding external series termination resistors. The Balanced-Drive family of devices from IDT will generate lower levels of noise than other components in the same speed grade, solve many of the termination line problems encountered by the designer, reduce power consumption and give superior performance to other high speed logic. Balanced-Drive is the logic family of choice for most applications.

APPENDIX B
STANDARD DEVICE SPECIFICATIONS

This section includes specifications and ratings for IDT's High-Drive and Balanced-Drive families. The standard tables for DC Electrical characteristics, output drive, capacitance and absolute maximum ratings are common to all Double-Density device types and are the same as in any characteristics are similiar if not identical for all devices.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6.0	pF
CI/O	I/O Capacitance	VOUT = 0V	5.5	8.0	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8.0	pF

NOTE: 3020 tbl 02
1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Resect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Resect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	–40 to +85	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 3020 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔICC	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max. VIN = 3.4V[3]		—	0.5	1.5	mA
ICCD	Dynamic Power Supply Current[4]	Vcc = Max. Outputs Open xOE = xDIR = GND One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	—	60	100	µA/ MHz
IC	Total Power Supply Current[6]	Vcc = Max. Outputs Open fi = 10MHz	VIN = VCC VIN = GND	—	0.7	2.5	mA
		50% Duty Cycle xOE = xDIR = GND One Bit Toggling	VIN = 3.4V VIN = GND	—	0.9	3.3	
		Vcc = Max. Outputs Open fi = 2.5MHz	VIN = VCC VIN = GND	—	2.5	5.5[5]	
		50% Duty Cycle xOE = xDIR = GND Sixteen Bit Toggling	VIN = 3.4V VIN = GND	—	6.5	17.5[5]	

3020 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (VIN = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CPNCP/2} + f_iN_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   DH = Duty Cycle for TTL Inputs HIGH
   NT = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   NCP = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—V	
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IIH	Input HIGH Current (Input Pins)	VCC = Max.	VI = VCC	—	—	±5	µA
	Input HIGH Current (I/O Pins)			—	—	±15	
IIL	Input LOW Current (Input Pins)		VI = GND	—	—	±5	
	Input LOW Current (I/O Pins)			—	—	±15	
IOZH	High-Impedance Output Current	VCC = Max.	VO = 2.7V	—	—	±10	µA
IOZL	(3-State Output Pins)		VO = 0.5V	—	—	±10	
VIK	Clamp Diode Voltage	VCC + Min., IIN = –18mA		—	–0.7	–1.2	V
IOS	Short Circuit Current	VCC = Max., VO = GND[3]		–80	–140	–200	mA
IO	Output Drive Current	VCC = Max., VO = 2.5V[3]		–50	—	–180	mA
VH	Input Hysteresis	—		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = Max., VIN = GND or VCC		—	0.05	1.5	mA

3020 tbl 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16XXXT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
VOH	Output HIGH Voltage	VCC = Min.	IOH = –3mA	2.5	3.5	—	V
		VIN = VIH or VIL	IOH = –12mA MIL.	2.4	3.5	—	V
			IOH = –15mA COM'L.				
			IOH = –24mA MIL.	2.09	3.0	—	V
VOL	Output LOW Voltage	VCC = Min.	IOH = –32mA COM'L[4]				
		VIN = VIH or VIL	IOL = 48mA MIL.	—	0.2	0.55	V
			IOL = 64mA COM'L.				
IOFF	Input/Output Power-Off Leakage	VCC = 0V, VIN or VO ≤4.5V		—	—	±100	µA

3020 tbl 06

OUTPUT DRIVE CHARACERISTICS FOR FCT162XXXT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
IODL	Output LOW Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V(3)		60	115	150	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH or VIL, VOUT = 1.5V(3)		–60	–115	–150	mA
VOH	Output HIGH Voltage	VCC = Min.	IOH = –16mA MIL.	2.4	3.3	—	V
		VIN = VIH or VIL	IOH = –24mA COM'L				
VOL	Output LOW Voltage	VCC = Min.	IOL = 16mA MIL.	—	0.3	0.55	V
		VIN = VIH or VIL	IOL = 24mA COM'L				

3020 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

APPENDIX C

PACKAGE INFORMATION

Double-Density devices are offered in the space saving 48- and 56-pin SSOP (shrink small outline package) for commercial and the 48- and 56-pin CERPACK for military. Figure C1 shows the dimension details for the two SSOP packages, and figure C2 shows the dimensions of the two CERPACK packages.

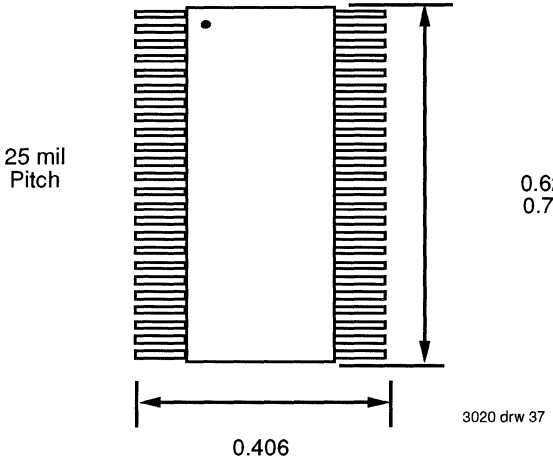

Figure C1. The Physical Dimensions of SSOP

Both SSOP packages have the same width and pin-to-pin separation but different body lengths. Due to the fine pitch (25 mil), significant area savings are achieved over multiple octal packages. Table C1 shows the key dimensions and characteristics of the SSOP packages.

AREA COMPARISON FOR SSOP PACKAGES

	48 SSOP	56 SSOP
Body Width	300 mil	300mil
Body Length	625 mil	725 mil
Body Height	2.74mm	2.74mm
Body Weight	0.6grams	—
θJC	17	17
θJA	70	70
Pin Inductance	1.5nH (ground) 2.9nH (I/O)	1.8nH (ground) 3.1nH (I/O)

3020 drw 08

AREA COMPARISON FOR CERPAK PACKAGES

	48 CERPAK	56 CERPAK
Body Width	390 mil	390mil
Body Length	626 mil	727 mil
Body Height	86 mil	86 mil
Body Weight	.6g	.6g
θJC	5	5
θJA	70	75
Pin Inductance	1.5nH (ground) 3.1nH (I/O)	1.8nH (ground) 3.1nH (I/O)

3020 drw 09

The thermal characteristics are used for estimating the junction temperature for given loading and frequency conditions. The devices should be operated below the maximum junction temperature for reliable operation over an extended period of time. For the FCT16xxxT family the maximum junction temperature allowed is about 150°C.

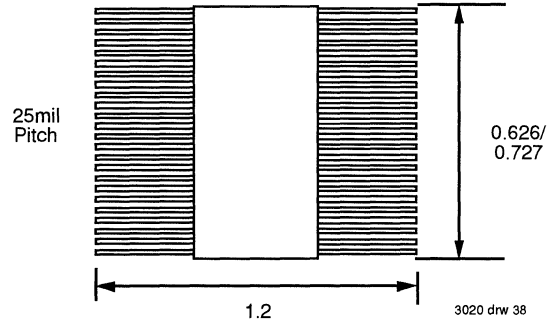

Figure C2, The Physical Dimensions of CERPACK

Integrated Device Technology, Inc.

POWER-OFF DISABLE IN IDT'S FCT16xxxT DOUBLE-DENSITY™ DEVICES

APPLICATION NOTE AN-102

By Stanley Hronik

INTRODUCTION

Power-off Disable is a feature of IDT's FCT16xxxT family which allows a user to shut down portions of his system, or to remove and install boards or peripherals during full power conditions, in a properly designed system. In order to have the ability to remove and install during live power conditions, the devices must be able to withstand the maximum rated voltages on their inputs and outputs when Vcc is between 5 volts and zero. The devices must not source or sink current that would affect the remaining fully functional system, or drive an active data bus in the power off state. The purpose of the Power-off Disable feature is to maintain data integrity, to eliminate bus contention, and to avoid component damage during power off while tied to or while being inserted into or removed from an active system.

This application note describes the Power-off Disable feature built into IDT's FCT16xxxT High-drive Double-Density family of products and portions of the eight bit FCT6xxT family, both of which are designed for standard 5V supply operation. Design techniques and applications for partially powered systems are discussed and the circuit configurations used in the FCT16xxxT Double-Density family of components to achieve the Power-off Disable feature are described.

APPLICATIONS OF POWER OFF DISABLE

There are many applications for the Power-off Disable feature in systems that either intentionally or accidentally become partially powered. A few of them are:

a) Fault Tolerant/Fault Resilient Systems
Fault-tolerant/fault-resilient systems often employ multiple redundancy. Critical system elements and functions are duplicated with the provision to transfer operation from one module or board to its "identical twin" if a fault is detected. The faulty board can then be removed from the rack for repair while the system is in operation, and replaced by a substitute board to maintain redundancy. The active data bus on the backplane must not be affected during the "live" insertion of the board.

b) Power Conserving Systems
Certain parts of a system may be powered off or operated at a lower Vcc to conserve power in redundant, backup or unused circuits. The maximum amount of power is conserved when the Vcc rail of the powered down section is at GND potential. Under these conditions, all signal pins of the powered down circuits must offer high impedance in order to prevent loading of the surrounding circuits.

c) Attaching Peripherals
It is a fairly common practice for people who are using computers and peripherals to connect the peripheral to the computer without powering off the system. Also, frequently a cable will become inadvertently disconnected during system installation, or if an activity adjacent to a system causes a disruption of the setup. Under these conditions the components interfacing the disconnection point should sustain no damage from the powered disconnection and subsequent powered reconnection.

COMPONENT SELECTION

All IDT logic components will support Power-off Disable on their inputs. The IDT logic components that will support Power-off Disable on their outputs, and I/O ports include all of the FCT16xxxT High Drive family, the FCT164245T 3.3 volt translator, and FCT620T, FCT621T, FCT622T, FCT623T, FCT646T, FCT648T, FCT651T, and FCT652T from the eight-bit family.

Component families which will not support Power-off Disable on their outputs have a parasitic clamp diode from the device output or I/O to Vcc. Some of these families are the FCT162xxxT Balanced Drive parts, the FCT 3.3 volt devices (except the translator), the FCT CMOS output devices, and the FCT-T octals which have not specifically been mentioned as having Power-off Disable.

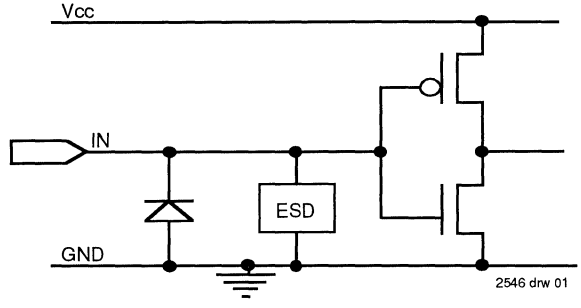

Figure 1. FCT16xxxT Input Stage

SYSTEM DESIGN CONSIDERATIONS

Input Considerations

Figure 1 shows the equivalent schematic of the input stage of an IDT FCT16xxxT Double-Density device. A signal on the input that is between 0 volts and the Absolute Maximum Rating Voltage will see the gate to the MOS-FET transistors, the cathode of the clamp diode to ground, and the ESD protection circuit. There is no clamp diode from the input pin to Vcc and therefore the input will maintain a high impedance when the voltage on the input rises above the Vcc level. With

Vcc at any voltage level between 0 and the maximum rated voltage, the input voltage could be as high as the device's Absolute Maximum Rating without damaging the device or causing significant current drain into or out of the input.

Output Considerations

Figure 2 shows the equivalent circuit schematic of an output buffer with 3-state control as used in the FCT16xxxT family. The output stage contains a totem-pole structure which consists of N-Channel pull up/down transistors. These transistors have a clamp diode from their drains to GND, but have no clamp to Vcc and therefore no low impedance path to Vcc through a forward biased diode.

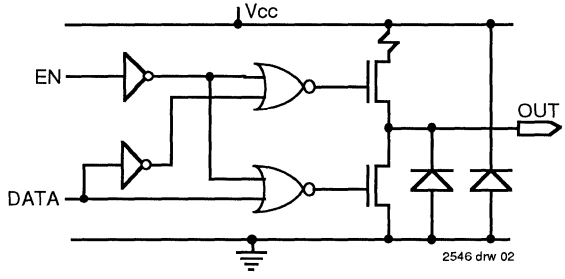

Figure 2. FCT16xxxT Output Buffer

Combination Input/Output Port Considerations

The I/O ports on IDT's FCT16xxxT High Drive and other families that support Power-off Disable contain combinations of the input and output structures shown in figures 1 and 2. These parts will handle powered installation/removal and other Power-off Disable functions with no problems.

I/O ports on families that do not support Power-off Disable on the device outputs have a diode from the I/O port to Vcc causing the same restrictions as the device outputs for those families.

Using Power-off Disable

In the system design, the designer must disable the outputs on all drivers which interface the point at which connection is being made, through control of the output enable pins, to assure that the bus interface components are not driving the bus despite their low power condition. On devices that require a logic high on the output enable pin (EN) to disable the output, maintaining the output enable pins near Vcc will assure that the output is disabled despite the voltage on Vcc approaching zero. As the Vcc level drops, the voltage required for a logic high will drop proportionately and the high impedance is maintained for power supply voltages from 0V to Vccmax (maximum operating Supply Voltage). If properly done, the power down condition will be transparent to active boards on the system bus despite other active components in the system driving the bus to logic high conditions.

Situations to Be Avoided

The connection of Vcc only without GND should be avoided. Under this condition the devices will "look for" a ground connection on their inputs or outputs through the clamp diode and ESD protection circuit as the pins are connected. With all of the components on the powered down board using a common ground, the entire current draw of the board may pass into the component ground pin on a single device and out the grounded input or output of that component. If the driving component on the other side of the connection is a bus driver or similar device, currents high enough to cause device damage to the connected components may occur.

Tying device inputs directly to Vcc and GND on a backplane or cable without series resistors may also produce a damaging current flow. This situation usually arises with board configuration pins on a backplane (e.g. for card slot identification, parity sense, pipeline register depth, etc.) All configuration pins should be current limited with series resistors if they are to tie directly to device inputs. This same situation is experienced if unused inputs are tied to Vcc or GND across a cable without series resistors.

If the above situations are avoided while attaching Vcc first, there is still the probability that bus contention or bus interference will occur which will cause system disruption during the board installation or removal. Designers should make provisions to assure that during installation into, and removal of components from powered systems, the GND connection is made first.

Some methods of guaranteeing that the GND pins will make first contact are as follows. The ground pins on the card edge connector can be made longer than the other pins so they make contact first. The ground pins can be placed towards both ends of the connector with Vcc near the center so that when the board goes in at a slight angle, the ground will make contact first. A ground wire can be connected between the board ground and the connection point ground prior to, and during insertion, to assure ground contact before Vcc. In the case of an electrically isolated connector, the connector shroud can be grounded.

CONCLUSION

The need for Power-off Disable is becoming prevalent in many of the high reliability and power conserving systems currently being designed. To utilized Power-off Disable, certain design criteria must be followed. The first item is to assure that the ground pin is connected across the interface before the Vcc pin, the ground pin remains connected while Vcc is connected, and that Vcc is disconnected before the ground pin. The second item is to condition the output enables of the powered down component so that the device outputs will remain disabled. The third item is to assure that there are no inputs hardwired to GND or Vcc across the interface without series resistors. The IDT parts which support Power-off disable will function in partially powered situations and will

Integrated Device Technology, Inc.

3.3 VOLT LOGIC

APPLICATION NOTE AN-103

By Stanley Hronik and Suren Kodical

INTRODUCTION

The demand for an increase in performance and portability of digital systems has created a need for integrated circuits of ever increasing performance and density with reduced power consumption. To meet this need, the semiconductor industry is moving rapidly towards a lower supply voltage standard based on 3.3Vs nominal supply. This new standard allows the retention of TTL threshold levels while providing improved reliability, noise levels and a significant reduction in power consumption. The lower power consumption internal to the circuitry will allow component densities to reach new levels of integration utilizing fine line technologies. Eventually it is expected that the sophistication level of 3.3V circuitry will dwarf 5V technologies.

Currently in the marketplace there are processors, memories and ASICs available which are either designed for or characterized for 3.3V operation. To support and accelerate the transition to the new 3.3V environment, Integrated Device Technology has developed families of 3.3V logic and bus interface circuits which will enable the designer to develop complete 3.3V systems. The 3.3V components now available are approaching the speeds of their 5V counterparts and in the near future will exceed those capabilities. These speed breakthroughs will be obtained by the further miniaturization of components as the lowering of breakdown levels allows the reduction in critical dimensions, path sizes, and device capacitances which will increase the device speed. Additional benefits include an increase in reliability due to lower power consumption and a reduction in noise generation due to lower voltage swings.

Systems that will find use for 3.3V logic include battery operated portable systems such as notebook/laptop computers, hand-held electronic field instruments and portable communications gear. Space and military systems that require low power with high reliability should find the 3.3V operation an attractive alternative. Thermally sensitive systems such as any electronic system that operates in harsh environments or has extremely high density will benefit from 3.3V logic. Eventually the uses of 3.3V logic will exceed those of the 5V systems.

3.3V LOGIC FAMILY FROM IDT

IDT is responding to the need for products that operate from a 3.3 ± 0.3 volt supply by introducing new logic families which have been named FCT3xxx and FCT163xxx. These families contain 8-bit and 16-bit bus interface functions, key "glue" logic elements and special interface components which solve interfacing problems in mixed 3.3V/5V supply systems. The IDT parts have all of the benefits inherent in 3.3V logic as well as, excellent drive capability and performance characteristics. These families are offered in a plastic Shrunk Small Outline Package (SSOP) for commercial applications and a CERPAK package for military applications. These packages offer significant space savings.

This Application Note on IDT's 3.3V families will discuss the following topics:

- Input and Output structures
- Performance characteristics
- Power, noise and reliability issues
- System considerations
- Solutions for "mixed supply" operation

KEY FEATURES OF THE 3.3V LOGIC FAMILY

The FCT3xxx and FCT163xxx families of circuits are optimized for high performance 3.3V systems. Important features of these families include:

- True TTL compatibility with a minimum of 400 mV noise margin.
- Rail-to-rail output swing provides additional noise immunity.
- **Quiescent power supply current of 80 μA maximum.**
- Typical Ground Bounce is under 0.3 V for the FCT163xxx family and under 1.0V for the FCT3xxx family.
- **Input and Output leakages guaranteed to be under 500 nanoamps.**
- Propagation delays match those of 5 V FCT logic for like functions.
- All inputs (except I/O) can be driven from either 3.3V or 5V components.
- Extended Commercial temperature range of -40°C to +85°C.
- ESD >2000 V per MIL-STD-883, Method 3015.

The low leakage and quescent currents offer a distinct advantage in power-critical systems through longer battery life and improved reliability. True TTL compatibility offers the system designer the freedom to mix 3.3V components and 5V components on the same board in most situations without sacrificing noise margin. By offering the same speed grades as the 5V logic for the same function, reduced power consumption is achieved without performance compromise.

3.3V LOGIC FAMILY CHARACTERISTICS

DC Specifications

Appendix A shows the complete set of DC specifications for the FCT3xxx and FCT163xxx families. These DC specifications meet or exceed the proposed JEDEC standard for 3.3V ± 0.3V TTL-compatible circuits.

Input Characteristics

The input to the FCT3xxx and FCT163xxx families consists of an ESD protection circuit, a clamp diode to GND, and the gates of two MOSFET transistors as is shown in Figure 1.

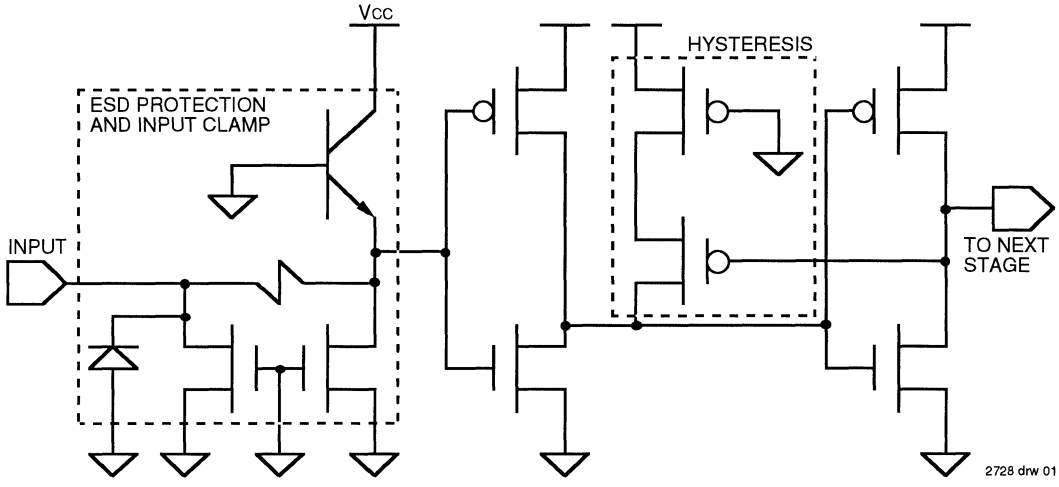

Figure 1. Input Stage of FCT 3.3V Components

The Input protection circuit provides excellent immunity (>2000 volts) to the effects of electrostatic discharge (ESD). It also provides an effective clamp for input voltage undershoots by forward-biasing the p-n junction during input voltage excursions below device ground. Note that there is no similar clamp to VCC. Therefore the input can withstand a maximum voltage rating of 7 volts, thus allowing the inputs to be driven by either 3.3V circuits or 5V circuits without exceeding maximum ratings. Typical input V-I characteristic is shown in Figure 2.

The input translator consists of two CMOS inverters with a feedback circuit which provides *Hysteresis* in the input transfer characteristic by means of a change in the ratio of P-channel to N-channel transistor areas in the input translator. Typical transfer characteristic with 150 mV of hysteresis is shown in Figure 3. Hysteresis increases static noise immunity in both logic states and also offers immunity to noise superimposed on slow edge-rate input signals if the amplitude of the superimposed noise is less than the hysteresis margin.

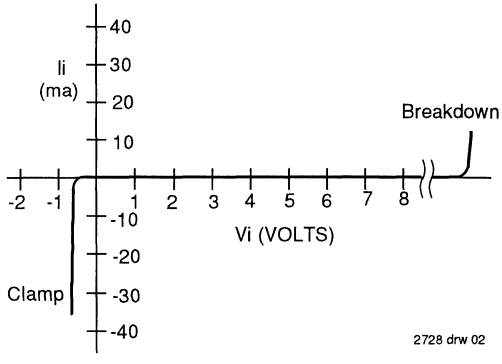

Figure 2. Typical Input V-I Characteristics

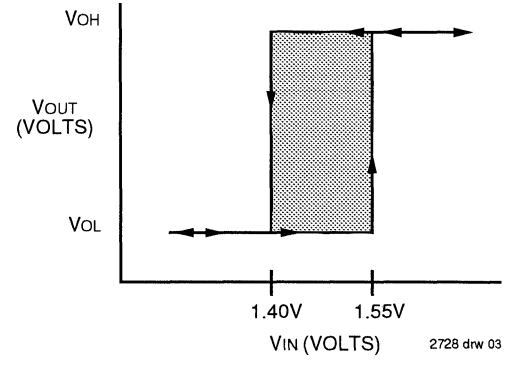

Figure 3. Typical Input Hysteresis Characteristics

Output Characteristics

The outputs on the FCT163xxx and FCT3xxx parts switch rail to rail in order to provide a good noise margin and full 3.3V CMOS output capability at low current levels and TTL-compatible guaranteed output levels at high drive currents. In order to achieve the CMOS output levels there is a P channel 'source' between the device output and Vcc acting as a pullup on the output. Inherent in this transistor is a parasitic clamp diode between the output and Vcc which will drain excess current if the voltage on the output rises a diode drop level above the Vcc rail. Similarly, there is a parasitic diode to GND associated with the N channel 'sink' transistor. Because of the presence of the clamp diode to Vcc there is no ability to shut off the power on a component that has an output directly tied to an active data bus. In other words, the FCT 3.3V components have no power-down disable capability on device outputs. Also, the 3.3V output cannot be readily connected to a 5V output on a bus because of the possibility of drawing large amounts of current through the parasitic diode under certain conditions. When connecting a 3.3V output to a 5V bus or output, the user needs to utilize the techniques for overcoming this problem as described later in this document or use the 5V to 3.3V interface components which IDT has developed to solve this problem.

The output structure of a typical FCT 3.3V logic circuit is shown in Figure 4. Along with this the typical Output V-I characteristic for a high-impedance (Hi-Z) state @ Vcc = 3.3Vs is shown in Figure 5.

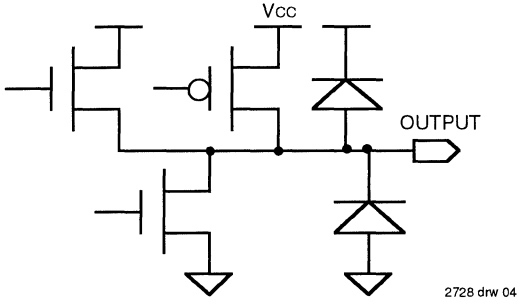

Figure 4. Output Structure of the FCT 3.3V Logic Families

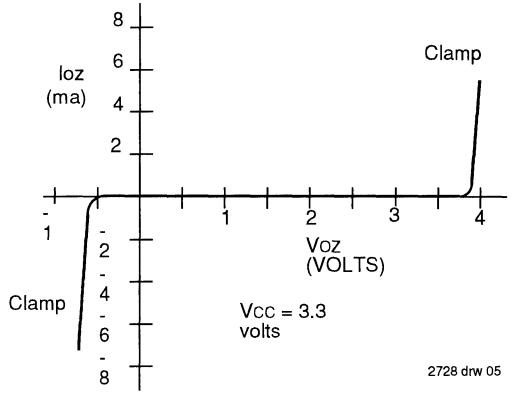

Figure 5. Typical Three-State Output V-I Characteristics

Figure 6 shows the output drive characteristics of the FCT 3.3V families for a logic LOW state. The low output impedance allows incident wave switching when driving transmission lines of >45Ω (typ.) characteristic impedance. The output also offers excellent dynamic current capability to drive large capacitive loads without significant speed degradation. The typical propagation delay derating is 1ns per 50pF of output load.

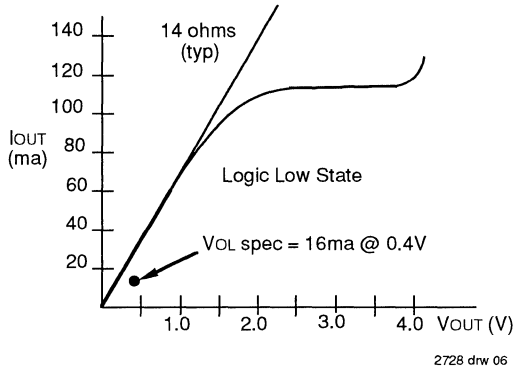

Figure 6. Typical Output Low Characteristics

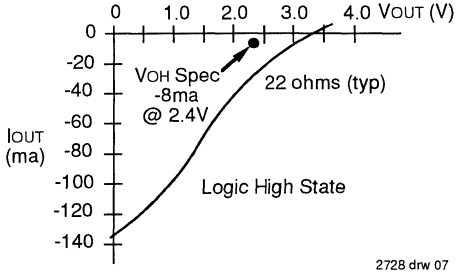

Figure 7. Typical Output High Characteristics

Figure 7 shows the output drive characteristics for a logic HIGH state. The V-I characteristic is somewhat linear due to the parallel combination of the P channel 'source' transistor and the N channel transistor shown in Figure 4. Again, the low output impedance in the logic HIGH state allows incident wave switching when driving transmission lines of >35Ω (typ) characteristic impedance. The output 'pull-up' circuit also offers excellent dynamic current drive to charge large capacitive loads without significant speed degradation. Typical propagation delay derating is 1ns per 50pF for the low to high transition.

POWER SPECIFICATIONS

There are three components of power supply current in CMOS circuits. The total power supply current is given by:

$$I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$$

The first one is the Quiescent Power Supply current (Icc). This is a static current through the power pins of the device when all inputs are held at either supply rails. This current is typically in the nanoampere range.

The second component of supply current is the sum of the static component through the input stages (ΔIcc) when the input voltage is between Vcc and GND. Under this condition both N channel and P channel transistors of the input translator shown in Figure 1 can conduct current. The magnitude of this current is dependent on the voltage on the input pin. Typical input translator current ΔIcc as a function of input voltage is shown in Figure 8.

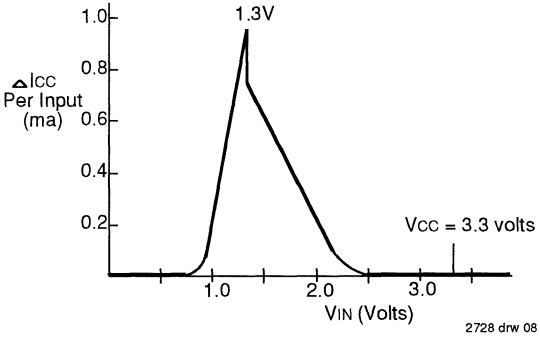

Figure 8. Typical ΔIcc characteristics

The ΔIcc component is specified in the data sheets for the FCT3xxx and FCT163xxx families at V_{IN} = 2.4V and at V_{IN} = V_{CC} - 0.6V. The first test condition where V_{IN} = 2.4V is useful when a worst-case power supply mismatch is expected between two circuits interfacing with each other. When the circuits are operating from substantially the same supply voltage, the condition of V_{IN} = V_{CC} - 0.6V is more realistic. A detailed explanation of the use of the power supply components is provided in the data sheets for the 3.3V logic products.

The ΔIcc component can be significant when a 5V circuit is driven from a 3.3V circuit, particularly if the 3.3V supply is at its minimum of 3.0 volts and the 5V supply is at 5.5Vs. Under these conditions, both the P channel and the N channel transistors of the input translator are operating in the saturation region.

The third component of power supply current is the Dynamic Power Supply Current or I_{CCD}. This component represents the power consumed by the device in charging and discharging the internal node capacitances of the circuit through the transistors. Since each internal node switches between the supply rails, the power consumption is given by the formula:

$$P = VI_{CCD} = fCV^2$$

where f = equivalent frequency of the voltage transitions, C is the net capacitance of the circuit (sum of the switching node capacitances) and V is the supply voltage. Notice the squared term in the equation. This equation shows the benefits of a lower operating voltage since a drop from 5Vs (nom) to 3.3Vs (nom) represents a 56% reduction in the dynamic power dissipation.

The equation for dynamic power dissipation can be rewritten as follows:

$$I_{CCD} = fCV$$

I_{CCD} is expressed in mA or μA per MHz of switching frequency which will be constant for a set voltage and capacitance. In bus interface circuits with several identical paths, it is customary to specify I_{CCD} per bit. Over a wide frequency range, I_{CCD} is a linear function of frequency. Figure 9 shows I_{CCD} for the FCT163245 16-bit transceiver in comparison with other popular 5V 16-bit transceivers.

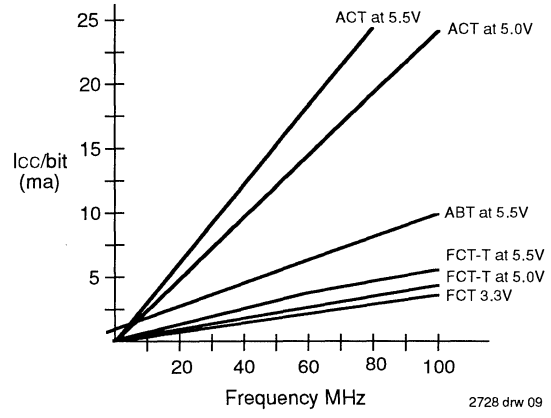

Figure 9. I_{CCD} vs Frequency for the 16245

A comparison of dynamic power supply current per MHz per bit for various 16-bit transceivers is shown in Table 1. Note that this current represents the power consumption in the device with the outputs unloaded.

Device	I_{CCD}/MHz/Bit	Vcc
ACT16245	240μA	5.5V
ABT16245	90μA	5.5V
FCT16245T	48μA	5.0V
FCT163245	27μA	3.3V

2728 tbl 01

Table 1. Dynamic Power Supply Current Comparison

Power Consumption Due To Device Output Loading

From the preceding discussion on power supply current components, one can see that the dynamic current will become dominant at higher frequencies. When the outputs of a circuit drive capacitive loads, the dynamic power supply current component due to the load capacitance increases the device power dissipation. This component is given by the equation:

$P_L = fC_LV^2$

Since the voltage swing on the output pin is the same as that on the internal nodes, the total power dissipation of the device with loaded outputs is:

$P_{TOTAL} = f(C_{PD} + C_L)V^2$

where C_{PD} represents an equivalent total capacitance for internal device nodes, CPD can be obtained from the following equation: $C_{PD} = I_{CCD} / V$ (µA/MHz).

RELIABILITY

The 3.3V family will inherently dissipate less power and run at cooler temperatures than corresponding 5V parts. The reduced supply voltage level means that internal dielectrics are not stressed at the levels they would be in higher voltage applications and therefore device breakdowns will be less prevalent than in higher voltage families. The IDT 3.3V components retain the 7V breakdown voltage on device inputs, equivalent to that of 5V parts, giving a wide margin of protection against potentially damaging input voltage levels. The devices also have ESD protection on the inputs and outputs helping to avoid handling problems.

In addition to the device reliability, system reliability is improved by using 3.3V components which generate less system noise, reduce device power dissipation and possibly reduce system size and cooling requirements.

NOISE CONSIDERATIONS

Accompanying the increase in system speed and bus widths, there is a concern about the increase in system noise. Several types of device-generated noise are associated with high speed integrated circuits. The most commonly recognized noise component is the Simultaneous Switching noise, often referred to as *Ground Bounce*. This transient noise is a result of voltage developed across the parasitic inductance associated with the ground return path of the circuit during simultaneous HIGH-to-LOW switching of several outputs. At its worst, ground bounce can cause false switching and data integrity problems in storage elements such as latches and registers. Since the ground lead inductance plays a major role in the amount of ground bounce generated, Octal bus interface circuits with a single ground generate more noise than 16-bit bus interface circuits with 8 ground return paths. The 3.3V logic families from IDT feature edge-rate control to contain ground bounce to 1.0V typical in the octal interface components and to 0.3V typical in the 16-bit interface components. These noise levels are considerably lower than those in 5V circuits of the same performance characteristics. IDT's Application note AN-47 offers a detailed discussion on this subject.

The second component of noise is that associated with output edge rates. For fast edge rates a PCB trace behaves like a transmission line. Signal overshoots and undershoots are generated when driving such traces without termination which matches the characteristic impedance of the traces. Under the worst-case scenario, these transients can degrade system reliability. The FCT3xxx and FCT163xxx families are designed to minimize these noise components. For a more complete treatment on this subject, the reader is referred to IDT Application note AN-49 'Characteristics of PCB Traces.'

Lastly, by avoiding abrupt voltage changes during the output voltage transitions, transmission of EMI and RFI noise is minimized. This helps with the board layout by reducing the need for special considerations in component placement, decoupling, line termination, and shielding and leads to quicker, easier designs that meet FCC guidelines.

Noise Immunity

To improve immunity to system noise, the FCT3xxx and FCT163xxx families of components have been optimized for an input trip point at 1.4V typical, at the center of the guaranteed input voltage range. Addition of the hysteresis feature further increases immunity to noise on signal lines. Since the outputs are designed to swing rail to rail, any 3.3V component interfacing with the 3.3V logic from IDT will experience the benefit of an additional noise margin.

PERFORMANCE

The device performance for the FCT3xxx and FCT163xxx families is the same as for the 5V FCT16xxxT family and FCTxxxT families. These speeds can be seen in the IDT Logic Data Book. Propagation delay limits of key parameters for commonly used functions in the FCT 3.3V families are compared with industry-accepted 74AC series devices operating at 3.3Vs. See Table 2.

Function	Path	74FCT163xxxA	74ACxxx
245	Input to Output	5.2ns	12.4ns
373	Input to Output	5.2ns	15.0ns
374	Clock to Output	6.5ns	18.0ns

2728 tbl 02

Table 2. Speed Comparison of FCT 3.3V with AC at 3.3Vs

INTERFACING 3.3V COMPONENTS TO 5V FAMILIES

During the transition from 5V to 3.3V, there will be a need to interface between 3.3V parts and 5V parts in a system or between a 3.3V system and a 5V peripheral. When operating 3.3V parts and 5V parts in the same system, the designer needs to be aware of the compatibility issues between the families and provide protection against component damage in some cases where excess current or voltage may develop. The 3.3V family was designed to be TTL-compatible with 3.3V or 5V components, but there are many situations inherent in the interface that will cause problems if the interface is not properly constructed.

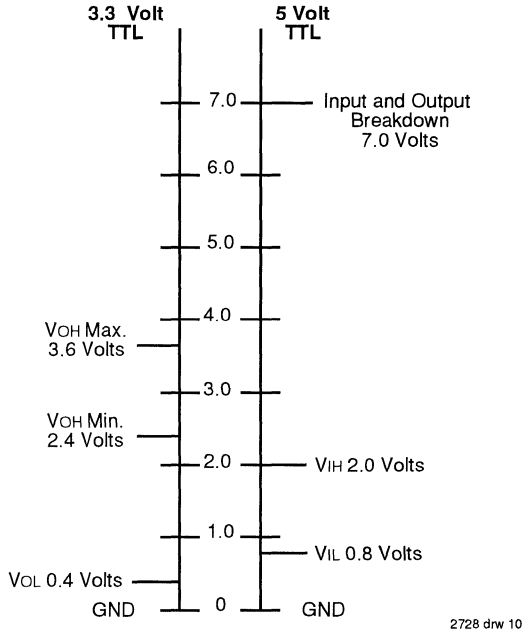

Figure 10. 3.3 Volt Device Driving a 5 Volt System

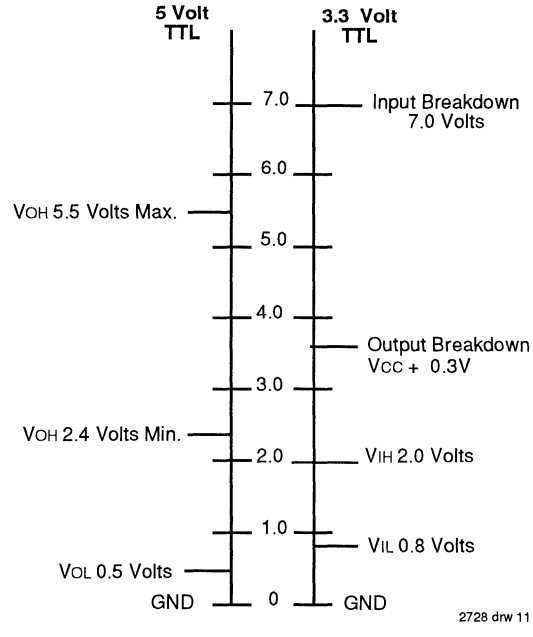

Figure 11. 5 Volt Device Driving a 3.3 Volt Device

3.3V Logic Driving a 5V System

As described earlier in this application note, the FCT 3.3V logic components have CMOS outputs which offer rail to rail output swing and guarantee TTL compatible output logic levels at high drive currents. Because of this, there is no problem with 3.3V logic driving standard 5V TTL logic. The logic input thresholds on the 5V TTL parts are V_{IL} = 0.8V, VIH = 2.0V. The 3.3V logic is guaranteed to drive a LOW to less than 0.4V and to drive a HIGH to greater than 2.4V at rated output load currents. This provides very good driving voltages for the 5V inputs with noise immunity making 3.3V outputs fully compatible with 5V TTL inputs.

Despite the logic compatibility of the 3.3V outputs with the 5V inputs, the designer needs to be aware of the slight increase in power consumption that may occur when interfacing 3.3V parts to 5V parts as discussed in the section on power consumption.

True 5V CMOS devices that utilize CMOS thresholds (not TTL) require higher input voltages to reach the guaranteed minimum logic high. *(The 3.3V logic is not guaranteed to reach the output voltage levels necessary to drive CMOS level inputs on true CMOS devices operating at a 5V supply level.)*

5V Logic Driving a 3.3V System

As stated earlier, 5V logic will drive 3.3V inputs (not I/O ports or three-state outputs) directly and will meet all voltage levels and input requirements of the 3.3V logic without component damage on either side while retaining full functionality. The 5V TTL component may output up to 5.5Vs worst case which will not exceed the 7V absolute maximum input voltage rating on the 3.3V parts.

Problems may develop from the output clamp diode when 5V TTL outputs are connected to 3.3V outputs or I/O ports on a bus. The logic HIGH on 3.3V device outputs and I/O ports is limited to Vcc + 0.5V. Driving a 3.3V I/O port directly from a 5V part may exceed this absolute maximum rating and damage the 3.3V device.

Other mixed supply situations include interfacing a 3.3V module or sub-system with a 5V system and interfacing a 3.3V system such as a laptop/notebook computer with an external 5V peripheral such as a printer. The 3.3V parts have no power down disable on the device outputs and therefore they cannot be unpowered and receiving voltage on their outputs without sustaining damage. It is likely in a dual power supply system that one supply will become active or shut down prior to the other. To avoid damage to the 3.3V part, the current from the 5V outputs to the 3.3V outputs must be limited.

Members of the 5V FCT16xxxT and FCT6xxT family do have power-down disable capability and therefore will sustain no damage in the partially powered situation regardless of whether only the 5V supply is active or only the 3.3V supply is active.

To avoid excessive current flow from an active 5V output into a 3.3V output, the user may place a resistor between each 5V output and the corresponding 3.3V output or I/O. When the 3.3V I/O is in a high-impedance state, a current will flow from the 5V part to the 3.3V part through the resistor and clamp diode causing a voltage drop between the devices and preventing damage. When calculating the value of the resistor, the designer should consider the worst case situation of the 5V

supply at the maximum operating rated voltage and the 3.3V supply at the minimum operating voltage. If the 3.3V system may power down when the 5V system is active the calculation should consider the 3.3V supply at zero. See Figure 12.

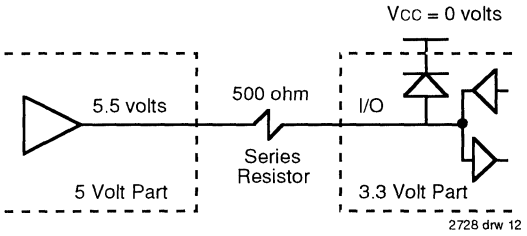

Figure 12. A 5V Part Driving a 3.3V I/O Port

Placing a series resistor between 5V and 3.3V parts will cause some speed degradation due to the RC time constant that will develop between the series resistor and the input capacitance of the 3.3V part and other parts that may be similarly attached.

The designer must be aware of the following situation when connecting 5V parts to 3.3V parts with a series resistor. If the 3.3V power supply is off and the 5V power supply is active, current may flow from the 5V output into the 3.3V output and through the clamp diode to the 3.3V power supply plane. When this happens, the voltage on the 3.3V power plane will rise if there is no low impedance path from the power plane to ground. Under certain conditions, it may rise sufficiently to cause unstable operation of the 3.3V parts or failure of the power on reset when the 3.3V supply is activated. This condition may be avoided by shorting the 3.3V power plane to ground when the power is off. This could be done through the use of a pull down transistor in the power on reset circuit. Another solution is to use the 3.3V to 5V interface components developed by IDT which avoid this and other problems.

If the user can guarantee power sequencing and tracking between the 3.3V and 5V power supplies, the value of the current-limiting resistor between the 3.3V inputs and 5V outputs can be significantly reduced.

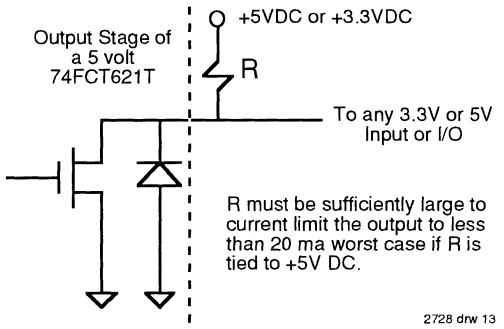

Figure 13. Using Open Drain Components as a 3.3V Interface

Using Open-Drain Components as an Interface

Another means of interfacing 5V outputs to 3.3V I/O ports is to use the FCT621T and FCT622T 5V open drain components as interface devices. If the pull-up resistor from the open-drain output is returned to the 3.3V supply as shown in Figure 13, the voltage on the bus will never exceed the 3.3V supply voltage and will assure safe operation. If the series resistor is tied from the device output to the 5V power supply instead of the 3.3V power supply, the output current would be limited by the resistor and also provide safe operation.

5V TO 3.3V INTERFACE COMPONENTS

To combat the problems associated with mixed supply operation, any of IDT's 3.3V unidirectional parts can be used as translators when connected as described earlier. This would include the FCT163244, FCT163373, FCT163374 and others.

When connecting 3.3V outputs to a 5V bus, it is necessary to use special interface components which will handle the higher voltages on the device outputs. One of the devices that IDT has developed for this purpose is the FCT164245T which will directly tie a bidirectional 3.3V bus to a bidirectional 5V bus. This part is also useful in situations where there is no power sequencing or where one of the power supplies may remain off while the other is active.

DEVICE CONFIGURATION AND NOMENCLATURE

All 3.3V parts are pin compatible with the industry standard for their 5V counterparts. This includes the FCT163xxx parts that are configured as 16 bit wide *DOUBLE-DENSITY* parts for wide bus widths and the FCT3xxx octal and glue parts.

The *DOUBLE-DENSITY* device types within the family retain the familiar naming conventions of the eight bit families (e.g. 245, 373, 374 etc.) but are arranged with two octal functions with independent control per package giving the devices dual eight bit capability or full sixteen bit operation. An example of the naming convention would be an FCT163245 which is a sixteen bit 3.3V device, with an FCT245T type function.

The pins on the *DOUBLE-DENSITY* devices are configured so that all power and ground pins are in identical locations for all functions. In addition data inputs have a *flow-thru* architecture for ease of board layout.

CONCLUSION

Using the FCT3xxx and FCT163xxx families of logic parts in 3.3V, high speed designs will help the designer overcome problems with noise and power consumption, and improve reliability. With the high density and lower power consumption, the user may be able to reduce his overall system size and cost without sacrificing performance. Prior to the availability of a complete 3.3V family, there are techniques for interfacing the 3.3V parts with 5V systems including special translator functions for mixed supply environment. The FCT3xxx and FCT163xxx families of devices are ideal for transmission line driving, point-to-point driving, bus interface and memory interface applications.

APPENDIX A

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC} +0.5	
V_{IL}	Input Low Level	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±0.5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±0.5	
I_{IL}	Input LOW Current		V_I = GND	—	—	±0.5	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = VCC	—	—	±0.5	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±0.5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V		—	–60	—	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V		—	90	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC} –0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA Mil. I_{OH} = –8mA Com'l.	2.4	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND		—	135	—	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.02	80	µA

2728 tbl 03

Integrated Device Technology, Inc.

DECOUPLING DOUBLE-DENSITY™ COMPONENTS

APPLICATION NOTE AN-116

By Stanley Hronik

INTRODUCTION

Double-Density is IDT's FCT-T family of 16, 18, and 20 bit bus interface components. The family is functionally compatible with the Wide Bus product line, but offers users power savings, higher speeds, and excellent guaranteed low noise operation with a choice of output drive characteristics. The components are available in a 64ma drive version for use in backplane driving where line termination exists, a balanced drive 24ma version with internal series line termination for quiet operation, and a 3.3V version for use in applications requiring the lower supply voltage.

Although IDT's Double-Density family is more forgiving than the older eight bit families, the decoupling must be properly executed to achieve optimum results. The three versions of the Double-Density components (64ma, 24ma, and 3.3V) have similar switching speeds and therefore have similar decoupling needs despite having different device parameters and output specifications. Because of this, the techniques for decoupling which are addressed herein apply uniformly across all versions of the Double-Density family.

When setting goals for decoupling a circuit, a designer should focus his attention on reducing the radiated emissions to meet the FCC limitations for the geographical area in which his circuit will be used. When this has been accomplished, the low noise levels needed to prevent cross talk and false switching will probably have been achieved. If the circuit contains low-level analog signals, additional decoupling will probably be necessary.

SELECTING THE CAPACITOR PACKAGE

The effectiveness of decoupling capacitors is often degraded by the series resistance and inductance inherent in the capacitor. The use of chip capacitors reduces the inductance due to the capacitor leads and through hole placement, making chip capacitors the optimum choice where that package style can be used. If the use of chip capacitors is not possible, the package should allow the capacitor to fit close to the board with very short lead lengths. With through hole capacitors the excess lead should be trimmed as close to the board surface as possible.

PC BOARD POWER AND GROUND PLANE

IDT's Double-Density devices are packaged in a 48- or 56-pin SSOP with multiple power and ground pins as shown in Figure 1. Unlike older logic families with corner Vcc and ground pins, Double-Density packages have eight ground pins and 4 Vcc pins which are equally spaced on both sides of the package. By providing multiple, short, parallel paths for current, the lead inductance is lowered, reducing the effects of simultaneous switching noise. This also reduces the effects of inductance in the board metalization by decentralizing the current path.

When laying out a circuit board for use with Double-Density, the designer should use full ground and power planes with all ground and power pins on all devices connected to the proper plane. No power or ground pins on any Double-Density device should be left floating. The board should have a large capacitor near the power entry point on the board to stabilize any power surges from the power distribution system. If the board has an effective power distribution system, decoupling Double-Density should be easier than decoupling corner Vcc and ground packages.

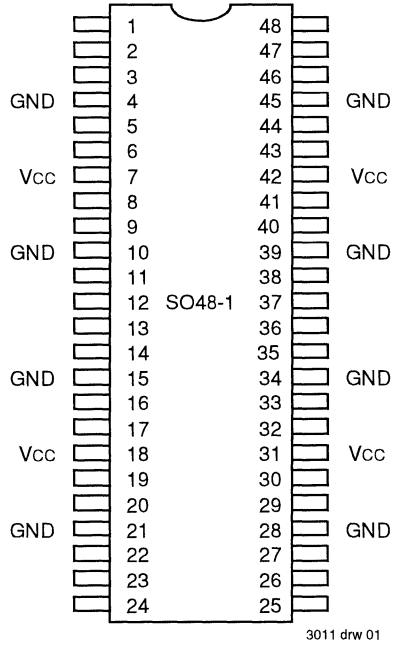

Figure 1. A 48-pin Double Density package

Capacitors have a circle of influence around them meaning that pins and components that are in the immediate proximity of the capacitor will be effectively decoupled while those components that are further away will be less affected. This characteristic is modeled in Figure 2.

While the number of capacitors per component will vary depending upon the decoupling needs of the circuit and the cost sensitivity of the design, it is suggested that the designer use at least one ceramic capacitor per IC on the board. In cost sensitive applications it may be possible to reduce the overall number of capacitors to less than one per component. In noise

sensitive circuits (e.g. A/D applications) more than one capacitor type per component may be necessary. Tantalum capacitors work well in high frequency analog situations which already include a ceramic capacitor.

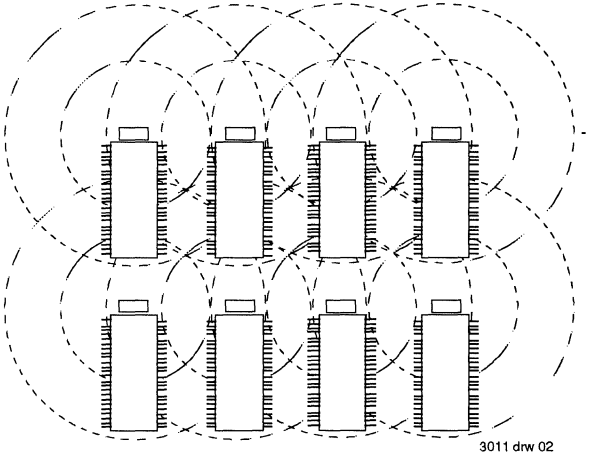

Figure 2. All capacitors have a "circle of influence" around them

CAPACITOR PLACEMENT RELATIVE TO THE COMPONENT

The decoupling capacitor should be placed as close as possible to the component being decoupled. It is not necessary to provide a separate capacitor for each Vcc on the device, but the decoupling capacitor should be solidly connected to both planes providing a short conductive path to all power and ground pins on the device. Relative to the component, the optimum placement would be on the reverse side of the board, centered over the device as shown in Figure 3.

The power and ground pins on the SSOP package that are adjacent to the device outputs will generate more switching noise than pins near the device inputs or enable pins. Since these pins are usually near the center of the package, placing the decoupling capacitor on the reverse side of the board centered over the component will provide the shortest path from the capacitor to the pins giving optimum decoupling.

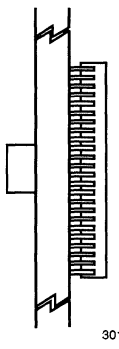

Figure 3. Capacitor placementfor a board with components on both sides

If the board has components on only one side, the capacitor can be placed at either end of the device (considering the direction to the power source) with a solid connection to the power and ground planes as shown in Figure 4. This will give

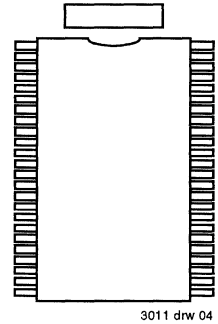

Figure 4. Capacitor macement for boards with one component side

the board designer direct access to the sides of the package to run traces and avoid placement interference.

If more than one capacitor is used, the capacitors can be placed at either end of the package or if that causes placement conflicts the capacitors can be located at adjacent corners of the package as shown in Figure 5.

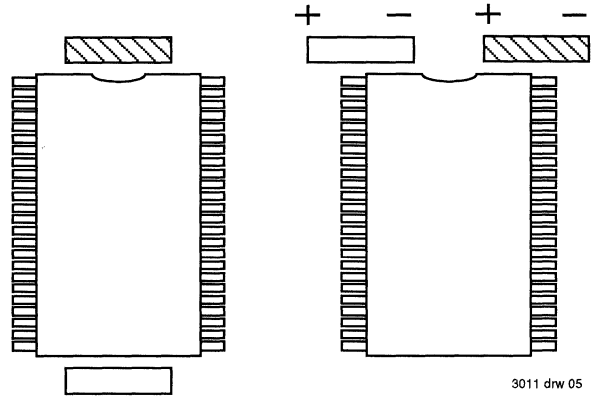

Figure 5. Placement of dual capacitors on the component side for special applications

POSITION RELATIVE TO POWER ENTRY

The decoupling capacitor should be placed between the power entry point on the board and the component that is being decoupled as is shown in Figure 6. Since the ultimate source of all charge is the power entry point, placing the capacitor between the component and the entry point positions the capacitor to receive and stabilize the voltage prior to the component. If the capacitor and component are reversed, the charge will flow directly from the entry point to the component and not pass the capacitor. This will make it easier for noise in the power system to reach the component, and for noise generated by the component to propagate into the

power system. When the capacitor is not in the path of the charge flow, the capacitor can only react to noise after it has passed into the component or power system rather than prevent it.

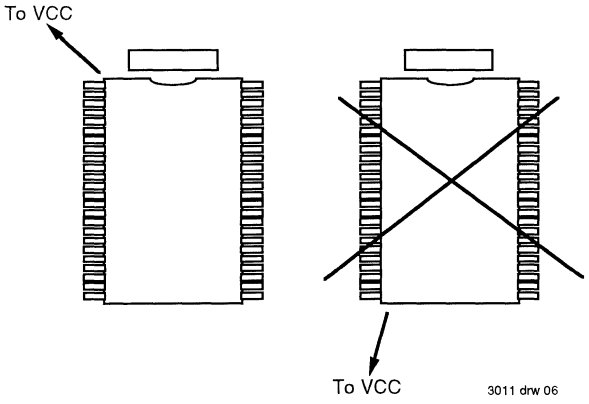

Figure 6. The decoupling capacitor works best if placed between the power source and the pin being decoupled

FREQUENCY CONSIDERATIONS

IDT's Double-Density components have very high internal switching speeds, but the lead inductance, packaging, and board placement will absorb most of the high frequency components above 120MHz before the noise can enter the power distribution system or radiate. The frequencies most likely to cause problems by reaching the power distribution system are in the 60-80MHz range (40-120MHz on a broader scale) and therefore the decoupling effort should be focused on this range.

Capacitors can be modeled as a capacitor in series with an inductor and a resistor as shown in Figure 7. With typical ceramic capacitors at low noise frequencies (<10MHz), the model can be considered as a single capacitive element with no inductance or resistance. As the noise frequency increases to levels above 50MHz the influence of the inductance and resistance increases to the point that the inductance becomes the dominating component of the capacitor's impedance. If noise issues are critical, the designer may be required to use two capacitors to cover both the high and low frequency components of the spectrum.

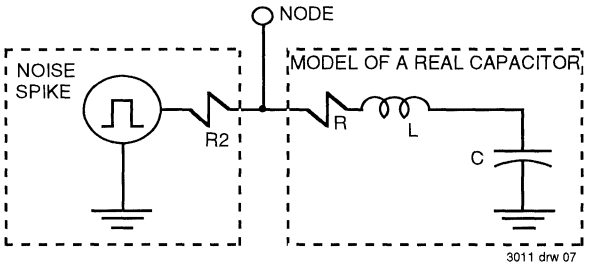

Figure 7. Model of the influence of a noise source and a decoupling capacitor on a node

Capacitors that are operating near their characteristic frequency will resonate at that frequency and provide good noise filtration with no inductive kick. Using this characteristic, designers frequently use a 0.01uf or a 0.001uf capacitor to filter out high frequency noise. The characteristic frequency of the capacitor can be obtained by contacting the capacitor manufacturer. Typically ceramic capacitors have a characteristic frequency in the 20-40MHz range. Tantalum capacitors typically work best at frequencies above 80MHz and have decreasing effectiveness at lower frequencies.

While picking capacitors at the resonant frequency of the circuit will prove beneficial to noise suppression, the selection of smaller valued capacitors will not. The value of the capacitor should always be at the resonant frequency or have a larger capacitance value. If small valued capacitors are used, it will be necessary to have good low frequency decoupling through additional larger valued capacitors located near the component.

USING CAPACITORS WITH DIFFERING INTERNAL STRUCTURES

When using capacitors of different values and different types on the same board in close proximity to one another, it is possible for the two capacitors to begin interacting with one another. With different frequency responses, the two capacitors will respond with different timings to voltage spikes with

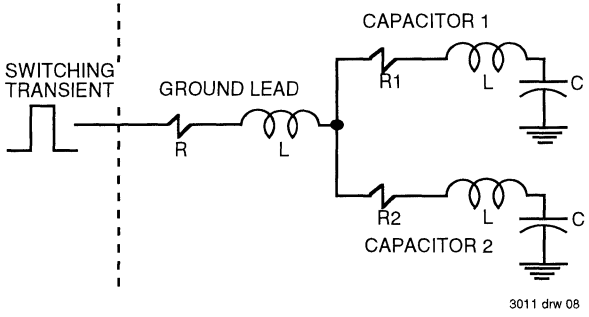

Figure 8. If using two capacitors with different characteristics, oscillations may develop between them

the result being an instantaneous difference in the internal voltages between the two capacitors. The two capacitors can then begin oscillating by passing charge between themselves through their characteristic series inductors as modeled in Figure 8. The end result will be a reduction in the effective decoupling that takes place and the possible addition of a noise source on the board.

Additionally, two capacitors with highly different dielectric constants in close proximity on the same board may affect each other because the high dielectric constant part will dampen the high frequency resonance of the low dielectric constant capacitor and the end result will be reduced noise suppression.

To effectively handle the problem of capacitors with differing internal structures, be sure the two types are not placed in close proximity to one another as shown in Figure 9. This can be done by placing the different capacitors at opposite ends

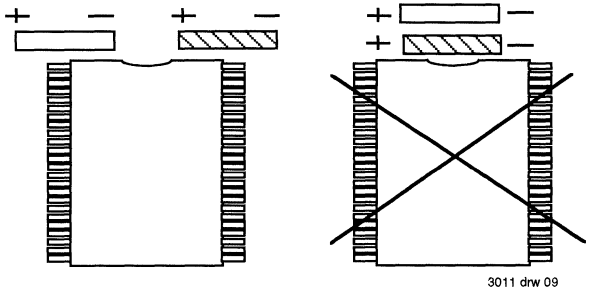

Figure 9. Exercise care when positioning two capacitors with differing frequency response in close proximity to one another

of the device or equally spaced on the back side of the board. If these choices are not feasible, the capacitors can be spaced in opposing corners of the device. The key to placement is to avoid having the Vcc pins of two capacitors adjacent or having the Gnd pins of two capacitors adjacent.

CONCLUSIONS

To properly decouple IDT's Double-Density parts do the following:

1) Select a capacitor that will meet the needs of the component. A 0.1uf ceramic is a good starting point. A 0.01uf ceramic may be better in situations which have good low frequency decoupling elsewhere on the board but are experiencing high frequency noise.

2) For best results use at least one capacitor per IC. More may be necessary in noisy situations, fewer may be possible with careful component and capacitor placement.

3) Place the capacitor as close to the component as possible. On the reverse side of the board is best. At either end of the component is also good.

4) Make sure that there is a good connection between all ground pins on the component and the capacitor. This should be in the form of a solid ground plane under the device. The same is true for the Vcc pins.

5) Place the capacitor between the component and the power entry point on the board if possible.

6) In critical situations two or more capacitors of different values may be used. In this case select a larger capacitor to provide low frequency stability and a smaller capacitor to give a series resonance to higher frequencies. Examples may be a 0.1uf or a 1uf ceramic along with a 0.001uf or a 0.01uf.

7) If caps of different internal structures are used, they should not be placed in close proximity to one another. Capacitors of different types that are close to one another may resonate between themselves and negate any positive effect of using two capacitors.

Integrated Device Technology, Inc.

MAXIMUM FREQUENCY CONSIDERATIONS FOR THE IDT49FCT805/6

APPLICATION NOTE AN-118

By Anupama Hegde

INTRODUCTION

An important factor in determining maximum operating frequency of a device is total power dissipated in the device. In CMOS circuits, the total power dissipation is dominated by the frequency-dependant dynamic component, since the static component is typically very small. The maximum permissible power dissipation is determined by the thermal characteristics of the package and the environment, which, in turn, sets the upper limit for the operating frequency. Although this is true for all CMOS circuits, the implications are particularly important in the case of clock drivers, where multiple outputs are continuously switching at the system clock rate and are driving significant capacitive loads.

Factors that influence the maximum operating frequency of a device based on power dissipation include :

- Maximum allowable junction temperature for reliable operation
- Junction-to-ambient thermal resistance of the device
- Ambient temperature
- Inherent device power dissipation characteristics
- Number of TTL level inputs
- Number of outputs switching
- Output loading

The following equations demonstrate how these factors determine operating frequency limits.

MAXIMUM FREQUENCY CALCULATIONS

In order to determine the maximum operating frequency, one must first calculate the maximum allowable power dissipation based on thermal limitations and maximum allowable junction temperature for the device. Starting with the thermal equation;

$$\theta_{JA} = (T_J - T_A)/P_D$$

the maximum allowable power dissipation for a device is given by:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad \text{..... (i)}$$

where,

θ_{JA} = Junction to Ambient thermal resistance of the device

T_J = Junction Temperature

T_{JMAX} = Maximum allowable T_J (T_{JMAX} = 150°C for IDT logic devices)

T_A = Ambient Temperature

P_D = Total Power Dissipation

P_{DMAX} = Maximum allowable Power Dissipation based on T_{JMAX}

Power dissipation in an unloaded CMOS device can be calculated using the following equation:

$$P_D \text{ (unloaded)} = \underbrace{(I_{CCQ} + \Delta I_{CC} N_T D_T}_{\text{static power}} + \underbrace{N_D f I_{CCD})}_{\text{dynamic power}} V_{CC}$$

..... (iia)

where,

f = output frequency

I_{CCQ} = static or quiescent current

N_T = Number of TTL level inputs

ΔI_{CC} = static current due to TTL level inputs

D_T = Duty cycle of TTL level inputs

I_{CCD} = dynamic power supply current per MHz per bit

N_D = Number of output bits switching at frequency f

Some manufacturers express the dynamic power dissipation component in terms of another parameter — C_{PD}, rather than I_{CCD}, as shown above.

$C_{PD} = I_{CCD}/V_{CC}$ = equivalent device power dissipation capacitance

Equation (ii) may be expressed in terms of C_{PD} as follows:

$$P_D \text{ (unloaded)} = (I_{CCQ} + \Delta I_{CC} N_T D_T + N_D f C_{PD} V_{CC}) V_{CC}$$

..... (iib)

Device loading can dramatically alter the dynamic power dissipation. Additional power is dissipated due to switching of the load. Consequently, equations (iia) and (iib), change as follows with the addition of a load:

$$P_D \text{ (loaded)} = P_D \text{ (unloaded)} + \mathbf{N_D f C_L V_{OH}^2}$$

$$= \underbrace{(I_{CCQ} + \Delta I_{CC} N_T D_T}_{\text{static power}} + \underbrace{N_D f I_{CCD})}_{\text{dynamic power}} V_{CC} + N_D f C_L V_{OH}^2$$

..... (iiia)

$$= (I_{CCQ} + \Delta I_{CC} N_T D_T + N_D f C_{PD} V_{CC}) V_{CC} + N_D f C_L V_{OH}^2$$

..... (iiib)

where,

C_L = Load Capacitance

V_{OH} = Logic High Output Voltage level (which is the voltage across the load)

Since CMOS devices have a negligible static power dissipation component, and V_{OH} equals V_{CC} for CMOS output swing FCT devices, equation (iiib) is sometimes approximated as;

$$P_D \text{ (loaded)} = P_D \text{ (unloaded)} \times [1 + C_L/C_{PD}] \quad \text{..... (iiic)}$$

From eqn(iiia),

$$P_{DMAX} = (I_{CCQ} + \Delta I_{CC} N_T D_T + N D f_{MAX} I_{CCD}) V_{CC} + N D f_{MAX} C_L V_{OH}^2 \quad \text{..... (iv)}$$

Substituting the P_{DMAX} value obtained from eqn(i) in equation (iv) gives:

$$(T_{JMAX} - T_A)/\theta_{JA} = (I_{CCQ} + \Delta I_{CC} N_T D_T + N D f_{MAX} I_{CCD}) V_{CC} + N D f_{MAX} C_L V_{OH}^2$$

For a given set of operating conditions, the only variable in this equation is the frequency. So, transposing all other factors to the righthand side gives the operating frequency limit.

$$\mathbf{f_{MAX} = \{(T_{JMAX} - T_A)/\theta_{JA} - (I_{CCQ} + \Delta I_{CC} N_T D_T) V_{CC}\} / \{N D I_{CCD} V_{CC} + N D C_L V_{OH}^2\}} \quad \text{..... (v)}$$

The application of these equations is illustrated in the following example for the IDT49FCT805/6 clock drivers.

Example (for the 49FCT805/6)

49FCT805/6 specifications:
- I_{CCQ} = 1.5mA
- ΔI_{CC} = 2.5mA
- I_{CCD} = 0.2mA/MHz/output

Assumed conditions:
- T_A = 25°C
- V_{CC} = 5V
- 11 bits switching
- C_L = 40pF (on each output)
- No airflow/cooling }
- Package = 20-pin SOIC } ==> (θ_{JA} = 90°C /Watt)
- f = operating frequency in MHz
- TTL level inputs (for CMOS level input signals ΔI_{CC} = 0)

This gives:

$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} = (150 - 25) / 90$ ...using equation (i)

$= 1.38W$

Power dissipation of the device, at frequency f, with no load is:

$P_D \text{ (unloaded)} = (1.5+2.5x\ 2 \times 0.5+0.2 \times f \times 11)mA \times V_{CC}\ V$ ...using equation (ii)

$= (4 + 2.2f)\ mA \times V_{CC}\ V$

$= 5(4 + 2.2f) \times 10^{-3}\ W$

With the assumed 40pF loading on each output:

$P_D \text{ (loaded)} = P_D \text{ (unloaded)} + [11f \times 40 \times 5^2 \times 10^{-6}]W$ ...using equation (iii-a)

$= P_D \text{ (unloaded)} + [11f \times 10^{-3}]\ W$

Using eqn (iv) gives:

$1.38W = P_D \text{ (unloaded)} + 11f_{MAX} \times 10^{-3}$

$1.38W = 5(4 + 2.2f_{MAX}) \times 10^{-3} + 11f_{MAX} \times 10^{-3}$

$1.38W = 5(4 + 4.4f_{MAX}) \times 10^{-3}$

$\Rightarrow f_{MAX} = 62.2MHz$

This is the figure obtained assuming TTL level inputs. With CMOS level inputs, since $\Delta I_{CC} = 0$, f_{MAX} goes up to 62.7MHz.

Similar calculations can be done to obtain the operating frequency limits for various other cases. The table below gives f_{MAX} values for these different cases.

T_A	# of Bits	Load	Package	Airflow(1)	θ_{JA}(2)	f_{MAX}
25°C	11	40pF	20-pin SOIC	0 LFM	90°C/W	62.2MHz
70°C	6	40pF	20-pin SOIC	0LFM	90°C/W	72.5MHz
25°C	11	40pF	20-pin SSOP	0LFM	107°C/W	52.2MHz
70°C	6	40pF	20-pin SSOP	0LFM	107°C/W	60.6MHz
25°C	11	40pF	20-pin SSOP	250LFM	82°C/W	68.4MHz
70°C	11	40pF	20-pin SOIC	250LFM	82°C/W	43.4MHz

NOTES:
1. LFM = Linear Feet per Minute.
2. Graphs for θ_{JA} are given in Section 4.1 of 1992 High-Performance Logic data book.

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SUMMARY

This application note discusses frequency limits based on thermal considerations. The theory discussed here is applicable to all CMOS devices, but the issue is particularly relevant to clock driver operation. This is due to the large number of simultaneously switching outputs and higher average power dissipation in clock drivers, as compared to other logic devices such as simple data/address buffers. Other considerations such as timing margins may fix an even lower maximum operating frequency than one calculated on the basis of thermal limits, in which case, power considerations do not limit the operating frequency.

Integrated Device Technology, Inc.

SIMULTANEOUS SWITCHING NOISE

APPLICATION NOTE AN–47

By Suren Kodical

INTRODUCTION

The need for increasing levels of throughput and improved performance in today's systems has placed certain demands on the logic and interface devices used in these systems. Two of the key requirements are high speed and high dynamic drive. Often the traditional glue logic and interface parts are in the critical timing paths and play a key role in determining system performance. Better speed (shorter propagation delays) lead to improved timing margins and offer opportunities for performance upgrading. The techniques used for improving the speed also result in faster edge rates at the outputs of these devices. As edge rates get faster, printed circuit board traces and back plane wiring appear transmissive at shorter distances. More and more interconnections between circuits now have to be treated as transmission lines. This scenario leads to a requirement for higher dynamic drive at the outputs of most high–speed circuits in order to drive low impedance transmission lines and to sustain high levels of DC current if the traces or backplane wiring are terminated at the far end.

This simultaneous requirement for high speed and high drive has certain important implications. First, the high speed in most CMOS integrated circuits is achieved by improved device processing and topology. Internal nodes slew faster and transistors reach their saturation current more rapidly, resulting in a higher rate of change of current (di/dt) in all switching transistors. Since most outputs of glue logic and interface devices are designed to handle high levels of dynamic current, the rate of build–up of current is particularly severe in the output transistors. When several outputs switch simultaneously, the total build–up of current in the common ground or Vcc lead inductance can be substantial (of the order of 200mA/ns to 300mA/ns) and can develop a large transient potential difference between the device power trace (ground or V_{CC} trace) and the external power plane. The term "lead" used here refers to the combination of bonding wire and package pin. A specific area of interest is the simultaneous switching of several "sink" transistors during the logic HIGH to LOW transition and the resultant transient potential difference between the chip ground and the external ground plane. This phenomenon is the simultaneous switching noise on the device (chip) ground plane and is commonly referred to as "GROUND BOUNCE".

Second, the high dynamic drive currents will cause very fast voltage edges at the switching outputs of the device subjected to predominantly capacitive loads. For example, a load capacitance of 50pF (equivalent of 6 to 7 typical CMOS inputs) will be discharged at a rate of 2V/ns during the high–to–low output transition if the dynamic drive current of the output sink transistor is 100mA. Such rapid edge rates will make relatively short PCB traces look like transmission lines. For example, a 2V/ns edge rate will make a typical trace of 6 inches or more look transmissive. These fast edges will contribute to system noise due to ringing, overshoots and undershoots on the signals, EMI and RFI due to sharp output voltage transitions and cross–talk between two adjacent signal lines on a PCB surface.

In this application note we will discuss the phenomenon of GROUND BOUNCE, its contributing factors and some design and application guidelines for minimizing the effects of ground bounce.

THE "GROUND BOUNCE" PHENOMENON

Figure 1 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load.

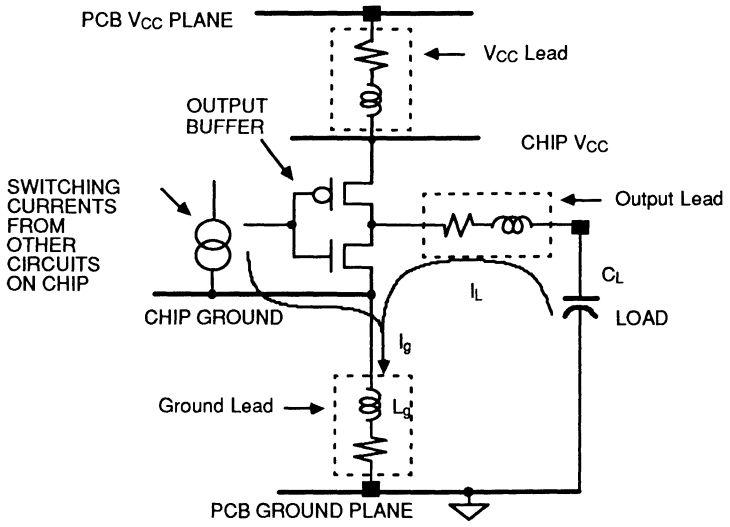


Figure 1. Output Buffer with External Parasitics

The parasitic components which influence ground bounce are; (a) inductance and resistance of the ground bond wire and pin, (b) inductance and resistance of the output bond wire and pin, and (c) load impedance. For first order analysis, the parasitics associated with the V_{CC} terminal can be ignored. Also the external ground plane is assumed to be ideal.

During the output high to low transition, the sum of output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance (Lg) and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both positive and negative ground bounce are a function Lgdi/dt and of the number of outputs switching simultaneously. The ground bounce phenomenon can be clearly observed at an unswitched "LOW" output of a device by switching several other outputs simultaneously from logic HIGH to LOW. Figure 2 shows a typical output voltage transition and the corresponding ground bounce as observed at the unswitched LOW output.

The positive ground bounce is primarily the result of the rate of change of current (dig/dt) through the ground lead inductance. This rate is determined by the rate at which the gate to source voltage (Vgs) of the sink transistor changes. During the early part of the output fall time, the ground voltage rises while the output voltage (at the drain of the transistor) falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor Ron (the "on" resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L–C–R circuit formed by the ground and output lead inductance, load capacitance and the total resistance in the loop which includes Ron. The oscillation frequency is determined by the net values of L and C while the damping is determined by L and the total resistance in the loop.

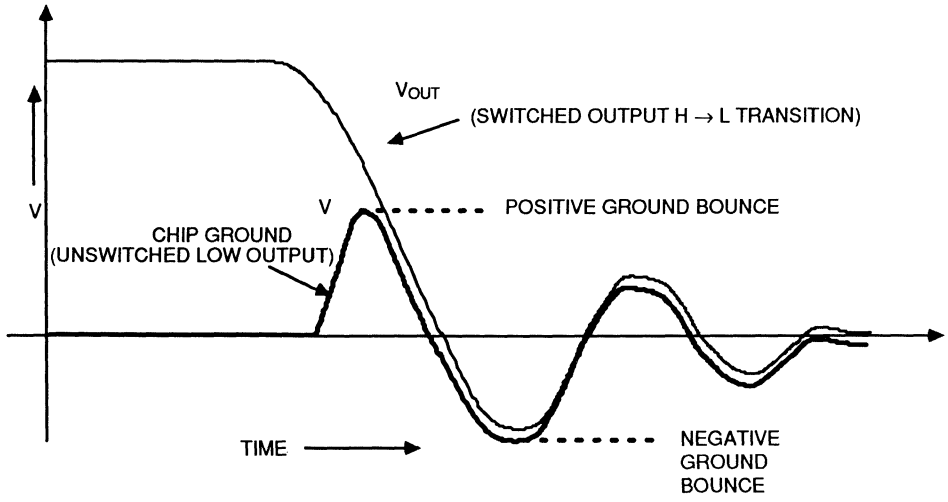


Figure 2. Ground Bounce Waveform

Ground bounce is also generated during the output LOW to HIGH transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

GROUND BOUNCE MEASUREMENT

There is no industry standard *per se* for measuring ground bounce. However, the method most commonly used by IC vendors and customers alike is based on observing the disturbance of the logic LOW level of an unswitched output of a multiple output device while switching all other (or several other) outputs from HIGH to LOW state. Figure 3 shows the schematic for measuring ground bounce on a device such as the FCT244 octal buffer. One output is in the LOW state while 7 outputs are switched simultaneously. The load on each output consists of a 50pF capacitor to ground in parallel with a 500Ω resistor to ground. Two outputs are connected to the oscilloscope; one for observing the HIGH to LOW transition of a "switched" output and the other for observing the ground bounce on the "quiet" output. At these outputs, the 500Ω load is split into a 450Ω resistor in series with the 50Ω input impedance of the scope probe. Alternatively, a 500Ω load resistor can be returned to ground and a high impedance probe connected to the device output pins.

With careful layout, proper bypassing to filter out high frequency noise and with a good oscilloscope and probes (bandwidth of at least 400 MHz), it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched "LOW" output whose sink transistor operates in the linear region and provides a "Kelvin connection" to the chip ground.

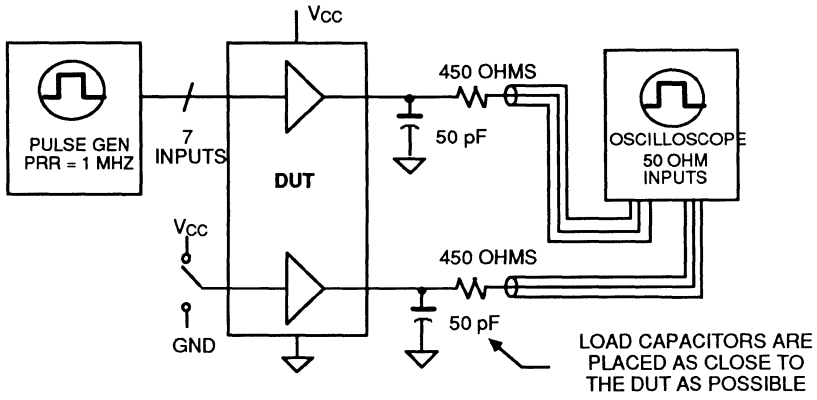


Figure 3. Ground Bounce Test Circuit

A scheme similar to the one shown in Figure 3 can be adapted for any multiple–output circuit. It can also be modified (by changing the load on the switched outputs) to observe and measure ground bounce during HIGH Z to LOW transitions in devices with 3–state control.

THE RELATIONSHIP BETWEEN GROUND BOUNCE AND SPEED

In CMOS circuits, the effective channel length (Leff) is the primary determinant of speed. However, for a given topology, this parameter also determines the saturation current (dynamic drive current) in the output sink transistor. A shorter Leff results in a faster device, but at the same time gives a larger di/dt in the sink transistor. Therefore, there is a direct correlation between ground bounce (caused by di/dt) and speed. This relationship is shown in Figure 4 where the positive ground bounce is plotted as a function of t_{PHL} for an FCT244 device in PDIP, SOIC and LCC. The ground bounce is measured at room temperature and V_{CC} = 5V using the test method shown in Figure 3.

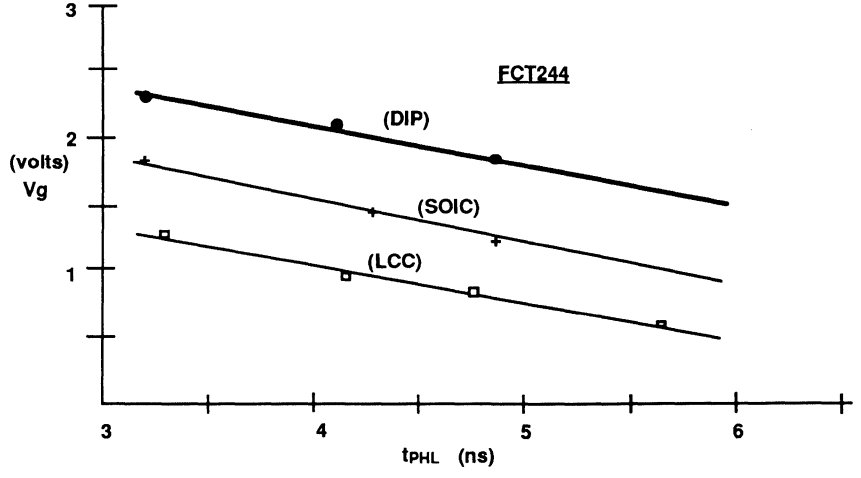


Figure 4.

Figure 4 illustrates two important points. First, because faster devices show a higher amplitude of ground bounce, one must exercise caution when comparing different logic families or different vendors for ground bounce. The samples to be compared should be in the same type of package and their propagation delays should be in close proximity. Second, package parasitics (ground lead inductance in particular) have a significant impact on the magnitude of ground bounce. In a standard DIP package, the corner pin ground lead inductance (pin #10 in a 20 pin package) is around 12 nH. In an SOIC this inductance is only about 7 nH and shrinks to around 4 nH in an LCC. The difference in ground bounce amplitude for different packages is clear from the above graph.

EFFECT OF NUMBER OF OUTPUTS SWITCHING

Ground bounce increases as more outputs switch HIGH to LOW simultaneously. Actual measurements indicate that the relationship is not linear. The reason is as follows. When the chip ground voltage rises due to the Ldi/dt effect, it modulates the gate–to–source voltage (Vgs) of the sink transistor and limits the peak current in the transistor. As more outputs switch simultaneously, the peak current in each transistor actually decreases, although the total current in the ground lead increases. This "diminishing returns" effect results in a non–linear relationship between ground bounce and the number of outputs switching simultaneously.

Figure 5 shows the ground bounce for an FCT244 octal buffer in a PDIP package measured on pin #18 under nominal operating conditions.

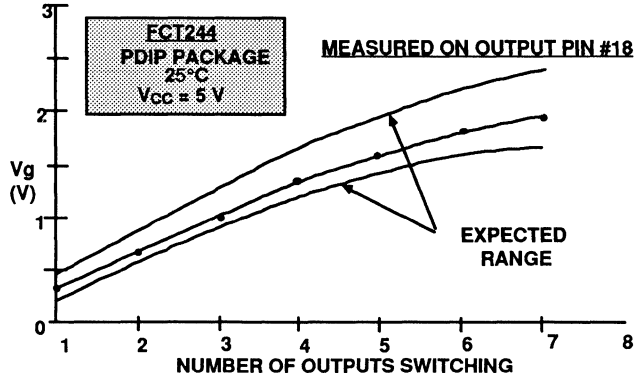


Figure 5. Simultaneous Switching Effect on Ground Bounce

EFFECT ON DEVICE PERFORMANCE

Ground bounce causes a variety of effects in the application environment as described below:

1. The most commonly observed effect is the noise on a "quiet" logic LOW output level in a device when several other outputs switch from high to low simultaneously. If the amplitude of the positive ground bounce exceeds the input threshold of the device driven by it, then all noise margin disappears and the driven device may recognize the noise as a legitimate input transition. A work–around for this problem is to allow some settling time before the signals at the output of the device are treated as valid. This solution generally applies to combinatorial paths only. A large positive transition on certain control signals such as CLOCK, LATCH ENABLE, RESET, etc. can cause loss of data. Such a problem can only be solved by taking steps to reduce the magnitude of the positive ground bounce below the recognition level (threshold) of the device.

2. Changes in the chip ground voltage disturb the thresholds, or trip points, of internal gates. This can cause non–monotonic output transitions that look similar to the effect of short unterminated transmission lines. Often this is not a serious issue.

3. The phenomenon described in (2) also causes a skew or a separation between edges of several outputs switching simultaneously. This skew is a function of the number of outputs switching. Figure 6 shows the effect of simultaneous switching on output skew for an FCT244 device used as a clock driver. The actual measurements were made under worst case commercial temperature and V_{CC} conditions for speed.

In critical clock driving applications, the absolute magnitude of output skew can be reduced by using devices in SOIC or LCC packages. Switching fewer outputs per device will further reduce the skew. However, this approach has to be weighed against the device to device skew if more packages have to be used as a result.

4. The most serious effect of ground bounce is associated with the loss of dynamic noise margin which results in the loss of stored data in latches and registers. This loss of noise margin is often caused by the negative ground bounce which follows the high to low transition of several simultaneously switching outputs (see Figure 2). Simply stated, the undershoots on the chip ground lower the input threshold, or trip point, of the device. This has the same effect as an input making a LOW to HIGH transition relative to the chip ground. If the undershoot is large enough to bring the input threshold near the logic LOW level of any of the inputs held LOW (with reference to the external ground plane), all dynamic noise immunity in the input stage of the device is destroyed. The apparent LOW to HIGH transition of clock (or latch enable) and any logic "LOW" data inputs of registers (or latches) will have the effect of losing stored "LOW" data which is now replaced by "HIGH" data.

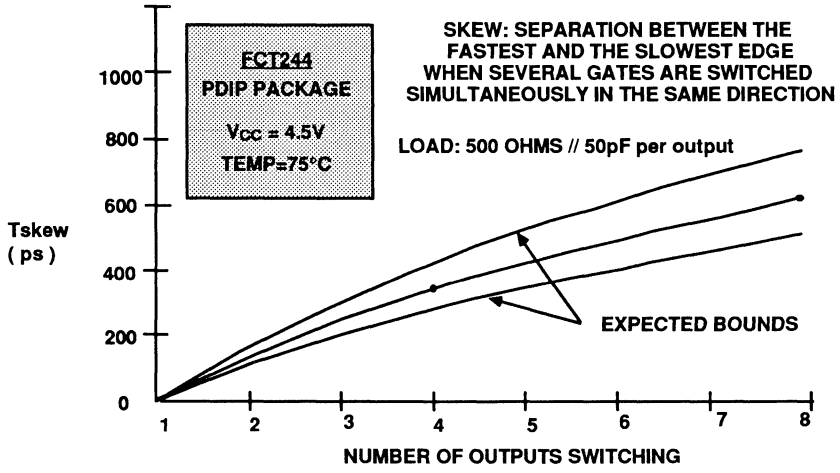


Figure 6. Effect of Simultaneous Switching on Output Skew

SOLUTIONS TO THE GROUND BOUNCE PROBLEM

Ground bounce is a pervasive phenomenon. It can be minimized or circumvented, but rarely eliminated since the parasitic inductance cannot be totally removed from the package. The solutions to the ground bounce problem take essentially two forms; (a) minimizing the effects of ground bounce and (b) minimizing the magnitude of ground bounce.

To minimize the effects of ground bounce, the design should be made "ground bounce tolerant". This can only be done at the expense of system throughput, since additional time must be allowed for the ground bounce to settle. As a result, the benefit of using high speed logic is partially negated.

The techniques for minimizing the magnitude of ground bounce take many forms. They are generally aimed at reducing either the parasitic inductance, or the amount of di/dt or both. These techniques are discussed in some detail below.

Using Smaller Packages

Since ground bounce is the voltage induced in the ground lead inductance by the rapid rate of change of current through it, there is a direct correlation between the amount of inductance and the magnitude of ground bounce. Ground lead inductance can be reduced by using packages with smaller internal cavities and lead dimensions. For example, for corner V_{CC} and GND configuration, the typical ground lead inductance for a 20 or 24 pin Plastic DIP package is of the order of 12 nH to 15 nH. This inductance drops to about 7 nH in an SOIC package and to about 4 nH in an LCC package. Figure 7 shows the effect of package lead inductance on the positive ground bounce for an FCT244 device.

Another method of reducing ground lead inductance is to arrange the pad layout such that the power pins (particularly the GND pins) are at the center of the package for the shortest lengths. Although this is an acceptable solution, it raises standardization and compatibility issues on industry–standard functions. This choice does exist for new functions and as an addition to existing standard functions.

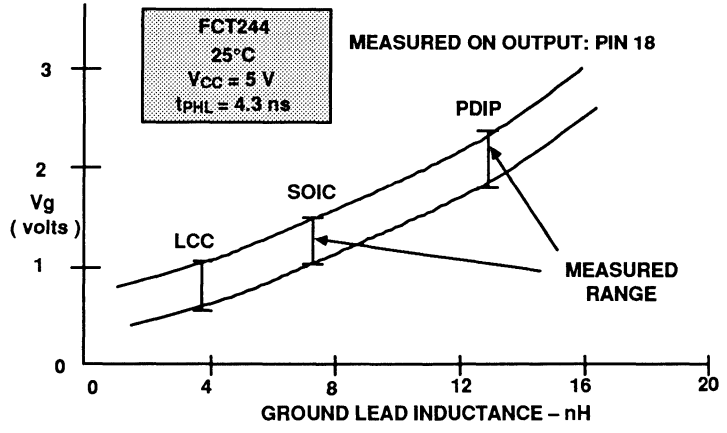


Figure 7. Effect of Package Lead Inductance

Series Damping

di/dt can be reduced either by limiting the magnitude of the peak current (Imax) *through the ground lead* or by slowing down the build-up of the total ground lead current during the output transition. The value of Imax depends on the size of the output sink transistor as well as on the load. Since this is a dynamic phenomenon, the peak current depends more on the amount of energy stored in the load capacitance.

One effective method of limiting the magnitude of Imax is to use a series damping resistor at the output. During the output transition, this resistor comes in series with the "on" resistance of the output buffer and limits the peak current, and hence the di/dt. Figure 8 shows the effect of series damping resistance on ground bounce for an FCT244 device.

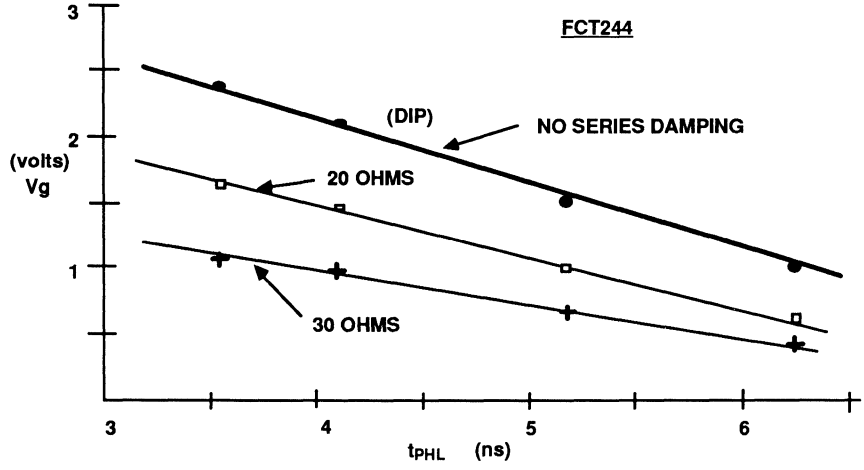


Figure 8. Effect of Series Damping on Positive Ground Bounce

As seen from the figure above, the series damping resistor causes a significant reduction in ground bounce. However, it is important to understand the implications of using series damping. Since the total output impedance is significantly higher, the transmitted signal is attenuated at the driving end; the attenuation being determined by the source impedance ($R_O + R_S$) and the loaded transmission line impedance (Z_L). R_O is the "on" impedance of the output circuit. This attenuation limits the amplitude of the first incident wave. Therefore, the series damping technique must be used with caution and is not recommended if first incident wave switching is desired. This subject is covered more thoroughly in the Application Note entitled "*SERIES TERMINATION*". The series damping resistor, if properly chosen, does have the advantage of limiting overshoots and undershoots on the transmitted signal without increasing system power dissipation.

The series damping resistor also decreases the magnitude of negative ground bounce and the undershoot on HIGH to LOW transitions. Therefore, series damping is effective in driving CMOS memories, particularly DRAMs where undershoots on input signals are undesirable.

Reduced Output Swing

Another technique for reducing ground bounce relies on limiting the energy stored in the load on the device output(s). If the voltage swing at the output is limited, less energy stored in the load. For example, if the output swing is limited to 3.3 volts nominal (similar to most bipolar or BiCMOS totem–pole outputs) instead of rail–to–rail, the energy stored in the output load can be decreased by a factor of 2.5:1 for a given load capacitance. This results in a smaller positive as well as negative ground bounce.

There is a beneficial side effect of this method. Since the high to low transition starts from a lower voltage level, the fall time component (the time taken for the output to switch from the logic HIGH level to the 1.5V measurement level) of t_{PHL} is smaller than that for a rail–to–rail transition. This translates into an improvement in t_{PHL}. However, since speed improvement is not the primary objective, some or all of this speed improvement can be sacrificed in order to further reduce the simultaneous switching noise. This can be achieved by means of a circuit configuration which provides a smaller initial di/dt during the logic HIGH to LOW transition. The resulting degradation in the output fall time cancels the speed improvement. In practice, about 40 improvement in ground bounce (relative to rail to rail swing output) can be obtained for the same speed. The FCT–T family of products introduced by IDT has been designed using this approach. Figure 9 shows the ground bounce characteristics for IDT74FCT244T/AT devices in PDIP and SOIC packages in comparison with the IDT74FCT244/A.

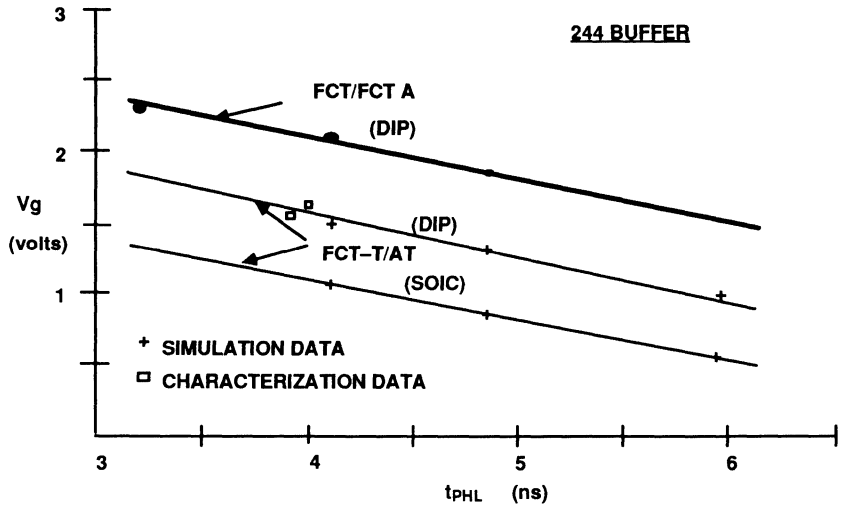


Figure 9. Improved Ground Bounce in FCT–T Family

SUMMARY

The requirement for high speed and high drive results in the phenomenon of ground bounce or simultaneous switching noise in high speed logic and interface circuits. The effects of ground bounce range from a noise spike on a quiet output to data loss in registers and latches. The magnitude of ground bounce can be reduced by using smaller packages with lower ground lead inductance, by switching fewer outputs of a device simultaneously, or by using a series damping resistor in the rail–to–rail swing FCT logic. The new FCT–T logic family is designed to offer much smaller ground bounce at the same speed by reducing the output voltage swing and by controlling the di/dt in the ground lead during the output transitions.

Integrated Device Technology, Inc.

USING HIGH–SPEED LOGIC

APPLICATION NOTE AN–48

By Suren Kodical

This application note gives some general guidelines and recommendations for using high speed logic such as FCT, FCT A and FCT B family of products.

POWER DISTRIBUTION

1. Use Ground and V_{CC} planes on multi–layer boards.
2. On two–layer boards with no V_{CC} and Ground plane, use a "grid" type ground distribution system to equalize ground potential at different points on the P C board.
3. Use Power Distribution Elements – PDEs (conductor–dielectric–conductor) to reduce characteristic impedance. Use separate PDEs for devices that switch large amounts of sink and source currents.
4. Do not use jumper wires for ground connections.
5. Provide a separate "noisy" ground distribution for high current drivers, particularly those driving backplanes.
6. Place high current driving circuits near their loads. For example, place backplane drivers at the edge of the board.
7. Make adequate provision for supplying transient energy to handle PC trace impedance and load capacitance. This is done by connecting individual bypass capacitors across the power pins of high current switching circuits.
8. Use low–inductance, ceramic disk capacitors (4700 pF to 0.1 uF) for high frequency filtering. These can be used in parallel with normal bypass capacitors.

SIGNAL TRACES

1. Treat the PC board traces as transmission lines. A conservative rule of thumb is to consider a trace as a transmission line if the unloaded signal transition time at the driving end equals the round–trip propagation delay for the trace in question. Typically, the transmission line delay is 0.15 ns per inch, or 0.3 ns for one inch round–trip. That means, for a transition time of 2 ns, a trace longer than 7 inches should be considered as a transmission line.
2. To minimize cross–talk between signal traces, avoid running sensitive signal lines close to traces connected to high current drivers.
3. Any signal lines that cross each other should be placed at right angles to further reduce cross–talk.

DEVICE SELECTION

1. Select devices which offer the largest amount of "real" noise margin. Ground noise due to simultaneous switching of multiple outputs causes a loss of dynamic noise immunity in the logic low state. Therefore, it is important to improve "low level" noise immunity. This can be achieved by:

a. Using CMOS outputs to drive inputs of "storage" devices such as latches and registers. This will offer better noise margin when compared to driving with devices with bipolar outputs which have a higher logic low level due to the offset voltage of the Schottky–clamped NPN sink transistor.

b. Reducing DC loading, i.e. reduce the fanput, on the outputs of devices that drive the data and control inputs of latches and registers.

c. Using devices with "hysterisis" on the inputs. This will further improve dynamic as well as static noise margin.

d. Use of series damping resistors (25 to 35 ohms) at the output of latches and registers will reduce the undershoot on the device intenal ground due to simultaneous switching of multiple outputs of the device. This undershoot normally follows the overshoot (also referred to as the ground bounce).

Series damping will overdamp the series L–C–R circuit formed by the parasitic ground path inductance, load capacitance and the low impedance of the sink transistor.

2. Several measures can be taken to reduce the power supply noise — both ground bounce and V_{CC} bounce:

a. Contention should be avoided on devices connected to a bus. Although bus contention is not detrimental to the device in a normal application, it causes very large positive and negative di/dt in the ground and V_{CC} paths. Such contention has the same effect as charging a very large load capacitance.

b. Series termination (i.e. series damping resistors) will also reduce the magnitude of the ground bounce by limiting the maximum transient current and thereby decreasing the total energy transferred to the parasitic inductances.

c. Use of local high frequency filtering will minimize the propagation of noise on ground and V_{CC} traces.

3. Avoid running control lines through a device that drives data/address buses.
4. Since the magnitude of ground and V_{CC} noise is a direct function of parasitic inductance, if all other conditions are unchanged, much benefit is gained by using packages with lower bond–wire and lead inductance. Thus, surface mount packages (SO, LCC, PLCC, etc.) will offer lower levels of ground and V_{CC} noise than standard DIP packages
5. Output drive "overkill" should be avoided. In non–critical paths, use of low–drive circuits will generally reduce the overall supply noise.
6. In very high speed circuits, minimize the loading per device to reduce total load capacitance.

SUMMARY

A combination of high speed (particularly fast edge rates) and high drive contribute to increased noise in power supply path as well as in signal paths. Much care is needed to minimize such noise so that maximum performance benefit is derived from the FCT family of high speed logic products.

Integrated Device Technology, Inc.

CHARACTERISTICS OF PCB TRACES

APPLICATION NOTE AN–49

By Suren Kodical

Printed circuit board traces carrying high speed digital signals can behave like transmission lines for fast edge rates of the driving signal. The transmission line effects can cause signal distortion, overshoots, undershoots and crosstalk between adjacent lines. It is therefore important to understand this behavior for trouble–free board design. In this application note we discuss the transmissive effects of PCB traces, the relevant electrical parameters and a simple technique for measuring unloaded or loaded characteristic impedance.

PCB TRACE AS A TRANSMISSION LINE

A PCB trace is normally regarded as a very low impedance medium which carries electrical signals from one point to another. This is true for most signals with relatively slow edge rates (long rise and fall times). However, when a trace is subjected to fast edge rates, its behavior changes completely. It behaves like a transmission line with a certain characteristic impedance Z. This impedance now presents a load to the driving circuit. In addition, the transmissive trace introduces a finite signal delay from source (driving end) to destination (receiving end). The equivalent circuit for a transmission line, represented by distributed L+R and C is shown in Figure 1.

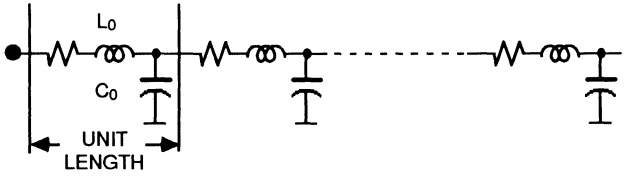


Figure 1. Transmission Line — Equivalent Circuit

In this schematic,

L_0 = Inductance of the trace per unit length, and

C_0 = Capacitance per unit length.

For the purpose of this discussion the series resistance can be ignored, thus treating the PCB trace as a "lossless" transmission line. The subscript "0" implies that the inductance and capacitance pertain to the "unloaded" condition, i.e. the inductance is the "self inductance" of the trace and the capacitance is that offered by the dielectric separating the trace in question from the adjacent conducting media.

Two important parameters can be derived from L_0 and C_0. The first one is Z_0, the characteristic impedance of the trace. The second parameter is T_0, the propagation delay per unit length of the trace. It should be noted that the parameter Z_0 is independent of the length of the trace.

$$Z_0 = (L_0/C_0)^{1/2}$$, normally defined in ohms.....(1)

$$T_0 = (L_0C_0)^{1/2}$$ per unit length, normally defined in nanoseconds.....(2)

Example

A typical *MICROSTRIP* PCB trace (a dielectric separating the trace from the ground plane on one side and free air on the other 3 sides of a rectangular trace cross–section) which is 10 mils wide and 1.5 mil thick separated from the ground plane by 15 mil glass–filled epoxy has a typical $C_0 = 2$ pF/inch and $L_0 = 10$ nH/inch. Using the above equations, we get $Z_0 = 70\ \Omega$ and $T_0 = 0.15$ ns/inch. The table in Figure 2 gives various transmission line geometries and their parameters.

TYPE	GEOMETRY	Z_0 ohms	T_0 ns / inch
CO–AX		50 – 125	0.13
WIRE OVER GROUND	GND	70 – 170	0.14
MICROSTRIP LINES	GND DIELECTRIC	30 – 150	0.15
STRIP LINE	GND	15 – 100	0.19
PC BOARD TRACES	DIELECTRIC	50 – 200	0.16

Figure 2. Transmission Line Geometries

EFFECT OF LOADING

The concept of an unloaded transmission line applies to point–to–point connections which consist of a driver and a receiver at the two ends of a trace, with no connections to the trace in–between. Most often, a PCB trace is tapped at several points and connected to inputs of several ICs. Clock, R/W, Chip Select lines and Data and Address buses are examples of this. These IC inputs represent a quasi–distributed load to the driving circuit. Whereas bipolar TTL inputs present a DC leakage path to V_{CC} in addition to the input capacitance, most CMOS inputs offer a capacitive load (ignoring the effects of input lead inductance).

As a result, the transmission line parameters are modified under the loaded condition, because the additional distributed load capacitance must be taken into account in addition to the unloaded distributed capacitance C_0.

To simplify the discussion, let us assume that the distributed load capacitance is represented by C_L per unit length, as shown in Figure 3.

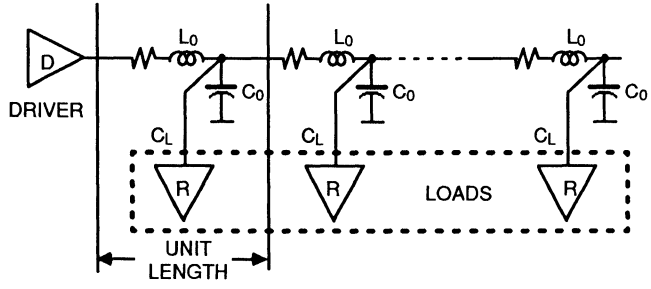


Figure 3. Loaded Transmission Line

Taking the effect of C_L into account, the loaded trace impedance Z_L and the loaded transmission delay T_L per unit length are given by:

$$Z_L = Z_0 [C_0/ (C_0 + C_L)]^{1/2} \text{ ohms} \quad (3)$$

$$\text{and } T_L = T_0 [(C_0 + C_L)/ C_0]^{1/2} \text{ per unit length} \quad (4)$$

Example

Consider a clock driver driving a bank of registers in DIP package, mounted 0.5 inches apart. Assuming a typical input capacitance of the clock pin of 5 pF, the PCB trace is loaded with 5 pF capacitance every 1/2 inch. This is equivalent to a distributed C_L of 10 pF per inch.. Using the example for the PCB trace given earlier, the loaded parameters can be calculated using equations (3) and (4):

$$Z_L = 70 [2 / (2+10)]^{1/2} = 70[1/6]^{1/2} = 70/2.45 = 29\ \Omega \text{ and}$$

$$T_L = 0.15 \times 2.45 = 0.37 \text{ ns/inch.}$$

This example illustrates the need for a significantly higher drive as the trace impedance drops from 70 Ω to 29 Ω. It also shows the impact of such loading on clock skew caused by the increase in transmission delay.

WHEN IS THE PCB TRACE TRANSMISSIVE?

As a general statement, a PCB trace looks like a transmission line for fast edge rates of the transmitted signal. To quantify this, a commonly used **rule of thumb** is:

TREAT A PC BOARD TRACE AS A TRANSMISSION LINE IF $T \leq 2L \times T_L$.

In this equation, T = output transition time (rise or fall time)
T_L = loaded transmission delay per unit length.
$T_L = T_0$ for the point–to–point case
L = Length of the PCB trace

Example

Consider the loaded transmission line in the example cited above. If the clock driver has an output transition time of 5 ns, the length at which the PCB trace should be treated as transmissive is given by:

$$L = T / 2T_L = 5 / (2 \times 0.37) = 6.8 \text{ inches.}$$

It is clear that, with slower edge rates a driver can drive longer traces without transmission line effects. The table in Figure 4 shows the limiting signal line length for different logic families based on typical edge rates for each of the families and typical unloaded signal traces.

LOGIC FAMILY	SIGNAL LINE LENGTH* (INCHES)
LS	25
S , AS	11
F, ACT	8
AS, ECL	6
FCT, FCT A	5

*Length above which the signal trace looks like a transmission line.

Figure 4. Signal Line Length vs Logic Family

This table shows that, as we go to faster logic devices, it becomes more critical to understand the transmission–line effects. Note that the signal lengths given in the table are not guarantees for any logic family. The actual limiting signal length is a function of trace and board characteristics, trace loading and the edge rates of individual devices in any logic family.

MEASUREMENT OF PCB TRACE PARAMETERS

Since both Z_L and T_L depend on board layout and loading, a simple practical method of determining these two parameters is useful. Described below is one such method which is particularly applicable to traces with well–distributed loading.

Equipment required:

1. Pulse generator with known source impedance (typ. 50 Ω) and capable of rise and fall times faster than 2.5 ns.
2. Oscilloscope: >350 MHz bandwidth.
3. High impedance scope probes.

Method

a. If the source impedance of the pulse generator is unknown, it can be easily obtained by observing the unloaded output waveform of the pulse generator, and then loading the pulse generator output with a resistance that will halve the amplitude of the original signal. The value of this load resistance is the source impedance (Rs) of the pulse generator.

b. Connect the pulse generator and the oscilloscope to one end of the PCB trace. Use a minimum of 9 inches of PCB trace. Insert the devices that will form the distributed load on the PCB trace. See Figure 5.

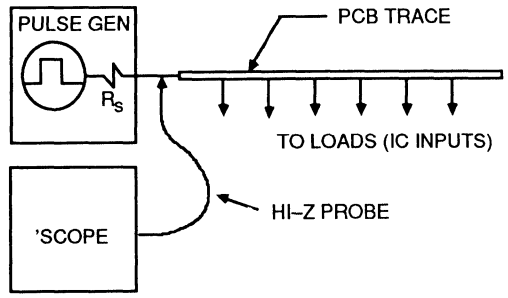


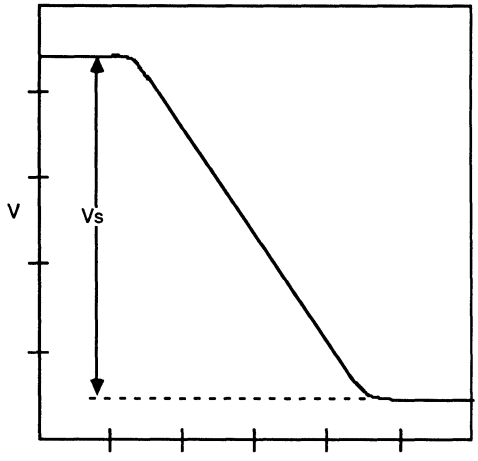
Figure 5. Test Set–Up for Measuring PCB Trace Parameters

c. Set up the pulse generator to obtain a 5V amplitude square wave of 1 MHz frequency. Adjust the rise and fall times to get 30 ns (10% to 90%). These slow edges ensure that the PCB trace behaves like a lumped load and not like a transmission line. Overshoots and undershoots on the waveform are avoided. Record the amplitude (V_s) observed on the oscilloscope *under these conditions* as shown in Figure 6A.

d. Now change the setting on the pulse generator to get the fastest rise and fall time. Observe the high to low transition on the oscilloscope. Note that there is a step in the output transition as shown in Figure 6B. Record the amplitude of the first segment of the output transition (V_t) and time interval between the start of the first transition and the start of the second transition ($2L \times T_L$).

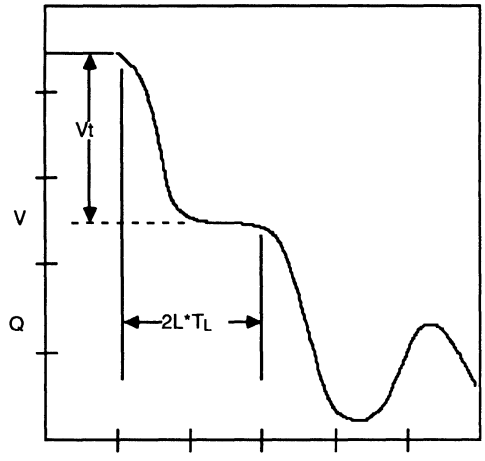
e. Determine the characteristic impedance of the loaded PCB trace (Z_L) by the formula:

$$Z_L = R_S \times [\, V_t / (V_s - V_t) \,]$$



Measuring Vs with Slow Edge Rate

Figure 6A.



Measuring Vt and T_L with Fast Edge Rate

Figure 6B.

The line propagation delay to the end of the trace is given by T_L.

Example

In a test performed on a 9 inch trace, we get $R_s = 45\ \Omega$, $V_t = 2.8$ V and $2L \times T_L = 6$ ns. Then,

$$ZL = 45 \times [\ 2.8 / (5 - 2.8)\ ]$$
$$= 57\ \Omega.$$
$$TL = 6 / (2 \times 9)$$
$$= 0.33 \text{ ns per inch}$$

THE IMPORTANCE OF PCB TRACE CHARACTERISTICS

The relative values of source impedance (R_s) of the driving circuit and the loaded characteristic impedance of the transmission line (Z_L) determine the effectiveness of driving transmission lines. As Rs increases for a given ZL, the amplitude of the transmitted component of the waveform (V_t) decreases. If the transmitted wave does not cross the threshold of a receiving device, the receiving device may not respond to the signal at the driving end (see Figure 6B) until the reflected wave reinforces the signal after a turn–around delay along the PCB trace. This implies that if a driver is driving a PCB trace from one end, the receiver nearer to the driver will respond *after* the receiver at the far end of the PCB trace. Such skew may be unacceptable in certain conditions.

The relative values of trace impedance and the load impedance at the far end also determine the amount of reflection and hence the overshoots and undershoots on the waveform. By understanding the implications of transmissive traces, a designer can choose the right termination and drive capability of the driving circuit to derive the maximum benefit.

SUMMARY

This application note describes the effect of fast edge–rates on the behavior of PCB traces. A simplified method for measuring the trace parameters in a given application environment is shown. The procedure discussed here can be extended to fully loaded backplanes.

Integrated Device Technology, Inc.

SERIES TERMINATION

APPLICATION NOTE AN–50

By Suren Kodical

Series termination is one of several forms of terminating transmissive lines. In this bulletin we discuss the pros and cons of series termination and the effect of termination impedance on simultaneous switching noise (a.k.a. Ground Bounce).

WHY TERMINATE?

With the constant push for higher speeds, particularly in the area of standard logic and bus interface products, system designers have to deal with devices with fast edge rates. At the same time, high packing density of multi–layer boards results in PC board traces with low loaded impedance and long transmission delays. This combination of fast edge rates and low transmission line impedance requires the system designer to pay careful attention to PCB design in order to maximize the benefits of today's high–speed logic. As more and more devices on the boards go to CMOS technology, typical nets consist of outputs with fast edges looking into transmission lines with some distributed capacitance along the line or lumped capacitance of CMOS IC inputs at the end of the line or a combination of both. In the absence of some form of termination, overshoots and undershoots on the signal can impose bandwidth limitation on the system, or subsystem due to settling time requirements or, even worse, can cause false triggering and data loss.

Termination of transmission lines is the time–honored method of improving signal quality. There are several forms of termination:

a. **Parallel or shunt termination:** a single resistor terminated to either V_{CC} or GND at the end of the PCB trace. For back–planes, termination is provided at each end.

b. **Series termination:** a single resistor is connected between the output node of the driver and the PCB trace or any other transmission line being driven.

c. **Thevenin termination:** two resistors form a potential divider at the far end of the transmission line. The junction of the two resistors goes to the transmission line and the two ends typically go to GND and V_{CC}. This type of termination is commonly used on back–planes at both ends.

d. **RC termination:** an R–C series combination is connected between the transmission line and GND at the far end.

Each of the termination schemes listed above has certain advantages and disadvantages. A detailed discussion of the relative merits of these schemes will be part of a separate application note. In this issue, we will focus on **SERIES TERMINATION**.

SERIES TERMINATION

Figure 1 shows a typical case of a series terminated driver connected to a load via a PCB trace.

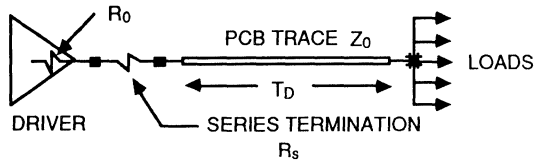


Figure 1.

The effective output impedance of the driver is now the sum of device source impedance ($\mathbf{R_0}$) and the series terminating resistance ($\mathbf{R_s}$). This modified output impedance of the driver comes in series with the characteristic impedance ($\mathbf{Z_0}$) of the PCB trace and forms a potential divider for the incident signal. Therefore, the signal that propagates down the trace is a fraction of the "open–circuit" signal at the driving end. The magnitude of the transmitted wave is given by the following equation:

$$V_t = V_s [Z_0 / (R_0 + R_s + Z_0)] \quad \text{.....(1)}$$

This equation shows that, as the total source impedance approaches the characteristic impedance of the line, approximately half of the incident wave will be transmitted to the other end of the trace. Since the load impedance is much larger than Z_0 due to the high input impedance of the CMOS devices, most of the transmitted wave is reflected. As a result, overshoots and undershoots on the signal are minimized at the receiving end. If $R_0 + R_s$ is much smaller than Z_0, a larger portion of the incident wave is transmitted down the trace. Since most of it is reflected, such a condition will cause overshoots and undershoots at the receiving end. Figure 2 shows the effect of series termination under prefect matching (total source impedance equals trace impedance).

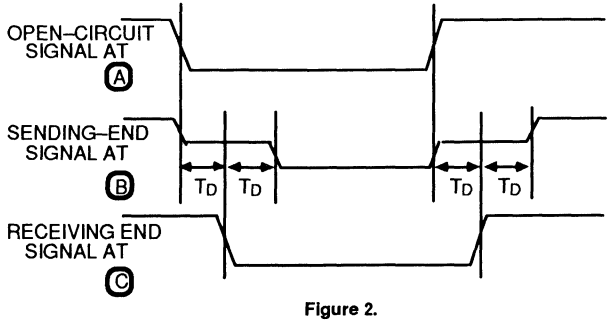


Figure 2.

The example shown highlights some important points:

1. For the best signal quality, the series terminating resistor should be chosen such that the total source impedance ($R_O + R_S$) is close to the characteristic impedance of the PCB trace. It is not essential that the two quantities match exactly. It is, however, important to ensure that the total source impedance is not greater than the trace impedance. Otherwise, multiple reflections may be needed to obtain the entire signal transition at the receiving end.
2. The waveforms in Figure 2 clearly show the effect of series termination on the waveform at both the sending end A and receiving end B. For a perfectly matched condition, the signal will attain the final value at the sending end after a round–trip delay ($2T_D$), although it will attain the final value after one transmission delay (T_D) at the receiving end. If loads (several IC inputs) are distributed along the PCB trace and are driven by the driver at one end, this condition results in signal skew which may be unacceptable. Therefore, series termination may not be the most suitable form of termination for distributed loads. Of course, the ratio of source to trace impedance can be adjusted to ensure that the threshold of the receiver is crossed on the **first incidence of the transmitted wave**, but this is normally at the expense of some undershoot and overshoot during signal transitions.
3. There is no limit to the number of lumped loads (as shown in Figure 1) that can be used, provided that the total DC loading does not reduce the static noise margin because of a voltage drop across the series terminating resistor. This implies that series termination is well–suited to drive inputs of CMOS devices because of their very low input current requirements. The primary limitation to the number of CMOS loads is the additional delay due to the total input capacitance being driven.
4. When series termination is used with lumped loads, the distance between the indvidual loads should be kept to a minimum. If the loads being driven are spread apart, a preferred method of driving them from one source is to make several groups of loads and drive each group from the driving source via individual transmission lines with their own series termination resistors. The driver should of course be capable of handling this additional transmission line loading.
5. It is clear that the series termination does not add any power dissipation to the system. It is, therefore, the preferred form of termination if power dissipation is a key consideration.
6. Series termination adds flexibility to the design in that the termination values can be tailored to suit a variety of trace characteristics and timing requirements.

SERIES TERMINATION WITH FCT DRIVERS

Like most TTL–compatible drivers designed to meet the standard DC specifications, the FCT output buffers offer different output impedance in the logic LOW and HIGH states. Typically, the output impedance is 6 ohms in the LOW state and 25 ohms in the HIGH state. Since the internal thresholds of all TTL–compatible devices (independent of technology) are with reference to GND and the noise immunity is normally worse in the logic LOW state, it is important to consider the logic LOW state and the high–to–low transitions when evaluating the effect of terminations.

First, let us consider the requirements for first incident wave switching. The aim is to cause enough voltage swing on the first part of the transmitted wave to cross the threshold of a receiving device close to the driver. For a typical V_{OH} of 4.8V with CMOS P–channel pull–up transistors and specified V_{IL} = 0.8 V for the receiver, the required amplitude of the incident signal is $V_t = V_{OH} - V_{IL} = 4.8 - 0.8 = 4$ V. The open circuit swing is $V_S = 4.8$ V.

Reworking equation #1, we get:

$$Z_O = (R_O + R_S)\ [\ (V_{OH} - V_{IL}) / V_{IL}]$$

Therefore,

$$R_S = Z_O\ [\ V_{IL} / (V_{OH} - V_{IL})\ ] - R_O \quad \text{.....(2)}$$

Using the values for V_S and V_t and for a device source impedance of 6 ohms, the maximum value of series termination resistance which will assure incident wave switching is given by

$$R_S = Z_O\ [\ 0.8 /\ (4.8 - 0.)\ ] - 6$$
$$= (0.2Z_O - 6) \text{ ohms}$$

For example, if the PCB trace impedance is 70 ohms, the maximum value of series termination resistance is **8 ohms** to assure incident wave switching. A similar consideration for the low to high transition yields the expression:

$$R_S = Z_O\ [\ (V_{OH} - V_{IH}) / V_{IH}\ ] - R_O \quad \text{.....(3)}$$

For a V_{OH} = 4.8 V, V_{IH} = 2.0 V and a source impedance of 25 ohms in the logic high state, the maximum value of series termination resistance to assure incident wave switching is,

$$R_S = (1.4Z_O - 25) \text{ ohms}$$

Again, if the PCB trace impedance is 70 ohms, the maximum value of Rs is **73 ohms**. This indicates that the high to low transition is the worst case.

The above example shows that a requirement for incident wave switching will impose severe restrictions on the series termination resistance due to the high to low switching case. Since the termination value is much less than the trace impedance, a certain amount of overshoots and undershoots are to be expected on the output waveform at the far end of the PCB trace. In effect, the incident wave switching requirement is in conflict with signal integrity for FCT logic devices with rail to rail output switching *when using series termination.* If signal integrity is the primary consideration, then the series termination has to be chosen to match the trace impedance. However, signal skew has to be tolerated when driving a transmission line with distributed loading. Alternatively, series termination should be limited to driving lumped loads at the far end of the transmission line (PCB trace).

In high–speed switching circuits, series termination offers another advantage. When driving predominantly capacitive loads, the series resistor serves to limit the peak current in the output pull–down transistor and therefore the resultant di/dt in the parasitic lead and bond wire inductance. This has the beneficial effect of limiting the amount of ground bounce (induced by the L.di/dt effect) as a result of simultaneous switching of high drive outputs.

SUMMARY

Series termination is an effective method for minimizing overshoots and undershoots on signals with fast edges and for reducing the amount of ground bounce caused by simultaneous switching. An understanding of the device output characteristics, particularly the output impedance values, is required to properly determine the value of series termination in order to assure incident wave switching.

Integrated Device Technology, Inc.

POWER DISSIPATION IN CLOCK DRIVERS

APPLICATION NOTE AN-51

By Suren Kodical

Power dissipation in switching circuits is discussed in this bulletin, particularly with reference to CMOS clock driver circuits. The IDT54/74FCT244 octal buffer is used as an example to compare the power supply current in CMOS, bipolar and bipolar–based BiCMOS technologies over a wide range of operating frequencies.

POWER DISSIPATION COMPONENTS

There are two components of power dissipation in integrated circuits. One is the steady–state component. This is the dissipation when all inputs are held at some fixed voltage level. The other component is frequency dependent and is generally referred to as the dynamic component.

In CMOS and CMOS–based BiCMOS circuits, the steady–state component is further divided into two sub–components; the quiescent power supply current (I_{CC}) primarily due to device leakage and the quescent power supply current when inputs are at TTL high level (ΔI_{CC}). This latter component applies to circuits with TTL compatible inputs. In bipolar and bipolar–based BiCMOS circuits, no such distinction is made and it is customary to specify power supply current for a given logic state on the output(s).

The dynamic component of power dissipation (I_{CCD}) is dominant in CMOS circuits because most of the power is dissipated in moving charge in the parasitic capacitors of CMOS gates. Therefore, the simplified model of a CMOS circuit consisting of several gates looks like one large capacitor which is charged and discharged between power supply rails. For this reason, a parameter called C_{PD} (power dissipation capacitance) is often specified as a measure of this equivalent capacitance and is used by the designers to estimate the dynamic power supply component. In the bipolar technology, the dynamic component is generally very small in comparison with the steady–state component because internal voltage swings are small.

Since power supply parameters are traditionally specified under "unloaded" condition, a comparison of power dissipation for a given device type (FCT244 with F244, for example) based on data sheet numbers alone can be misleading. For a true "apples–to–apples" comparison, the effect of capacitive load on the device should be taken into consideration. This is particularly true in the case of clock drivers which drive heavy capacitive loads and operate at high frequency. Under these conditions, the dynamic power dissipation component due to output loading could be significant in both bipolar and CMOS circuits. This is illustrated in the following section by using the '244 Octal Buffer as an example.

'244 Example

Consider the '244 as a clock driver with 30 pF load on each of the 8 outputs, operating at room temperature and V_{CC} = max. Power dissipation of IDT's FCT244 is compared with F244 (FAST™) and TI's BCT244. Data sheet numbers are used where applicable.

FCT244

First, we need to determine the C_{PD} for the device. Since $C_{PD} = I_{CCD}/V$ in pF if I_{CCD} is expressed in μA/MHz, we can determine C_{PD} using the max. limit specified for I_{CCD} in the data sheet. Therefore,

$$C_{PD} = 250 / 5.5 = 45 \text{ pF}$$

When the device is loaded with 30 pF capacitance per output, the dynamic dissipation component increases due to load. The loaded value is given by,

$$I_{CCD} \text{ (loaded)} = \{ (C_{PD} + C_L) / C_{PD} \} I_{CCD}$$
$$= \{ (45 + 30) / 45 \} 250 \text{ μA / MHz / bit}$$
$$= 0.42 \text{ mA / MHz / bit.}$$

When all eight outputs are switching simultaneously, the total I_{CCD} (loaded) is 3.3 mA/MHz.

If quiescent power dissipation is ignored, the above equation can be used to determine the total power dissipation at any frequency when the input levels are CMOS compatible. For the case where the inputs are driven from a bipolar TTL device, the ΔI_{CC} component needs to be added in order to obtain the total power dissipation. Assuming a 50 duty cycle, for ΔI_{CC} (max.) of 2 mA, this static I_{CC} component is 8 mA. Figure 1 shows the power dissipation versus frequency for both conditions.

F244

The specified power dissipation is I_{CCL} = 90 mA and I_{CCH} = 60 mA. For a 50 duty cycle, the steady–state dissipation is 75 mA. In addition, the dynamic dissipation component appears due to the external load capacitance and the output pin capacitance of the device. For C_L = 30 pF and C_{OUT} = 10 pF (assumed), the dynamic component can be derived:

$$I_{CCD} \text{ (loaded)} = 40 \text{ pF x (4.3 V – 0.3 V) in μA/MHz.}$$
$$= 160 \text{ μA / MHz / bit}$$

where the 4.3 V – 0.3 V represents the voltage swing (for V_{CC} = 5.5V) on the total load capacitance. For 8 outputs switching simultaneously, I_{CCD} is 1.28 mA/ MHz. The total dissipation as a function of frequency is also shown in Figure 1.

BCT244

The BCT family from TI is developed with a bipolar–based BiCMOS process. Therefore, the power dissipation characteristics are similar to F244. The steady–state dissipation is 57.5 mA for a 50 duty cycle. The dynamic component of the dissipation is 1.28 mA/MHz. The total power dissipation versus frequency is again shown in Figure 1.

The graph in Figure 1 shows that over a wide range of frequencies the power dissipation of FCT family of circuits is much less than that of BCT and F families, even under heavy capacitive loading.

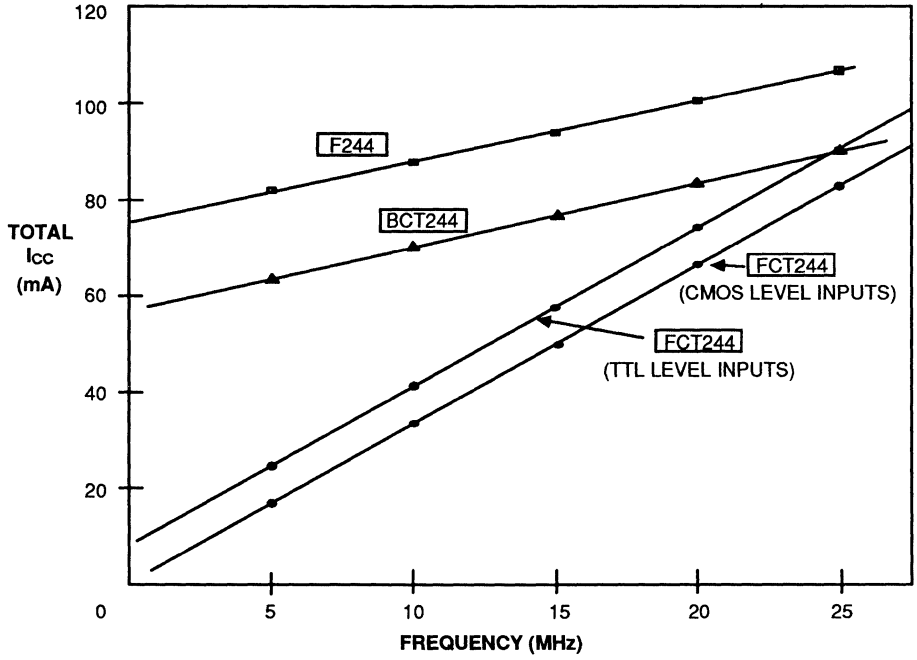


Figure 1. Total Icc vs Frequency

SUMMARY

A simple method for calculating "real" power dissipation in an operating environment is shown by using '244 as an example. This method can be extended to any other product and can be used to determine realistic power consumption if the loading and effective operating frequency can be estimated for each device.

Integrated Device Technology, Inc.

FCT OUTPUT STRUCTURES AND CHARACTERISTICS

APPLICATION NOTE AN–52

By Suren Kodical

INTRODUCTION

The FCT family of products has gone through an evolution in terms of die size, process technology (critical dimensions) and circuit implementation. Originally, the family of products was derived from the Z–step gate arrays ("4004" gate array for small gate count and "8000" array for large gate count). Later, a "shrunk" version of the smaller array was developed to obtain performance improvement. This array is called the Y–step. Recently, some of the high volume runners have been "customized", i.e. redesigned to minimize the die size and get some performance improvement with a more efficient topology. These customized versions are called the W–step devices. The current FCT portfolio consists of a mix of Z, Y and W step devices. This bulletin describes the output structures used in different steppings and the corresponding output characteristics for the logic HIGH and LOW states.

"4004" Z– STEP OUTPUT BUFFER

The schematic for the buffer used in the "4004" Z step devices is shown in Figure 1. This output consists of an N–channel "sink" transistor which turns on in the logic low state at the output and maintains a logic low voltage close to GROUND for normal loading.

The pull–up or "source" circuit consists of a combination of a P–channel transistor, an N–channel transistor and an NPN bipolar transistor with a series current limiting resistor. This circuit configuration is designed to give a resistive characteristic during the LOW to HIGH transition at the output.

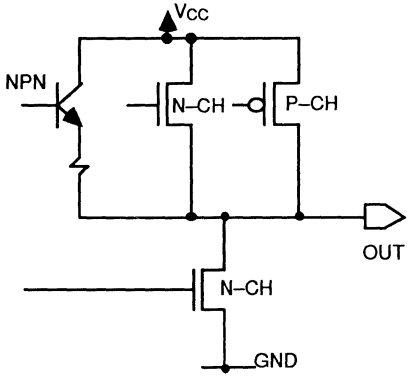


Figure 1. Step Output Structure

The output V–I characteristics for the Z step output structure in the logic HIGH and LOW states are shown in Figures 2A and 2B, respectively.

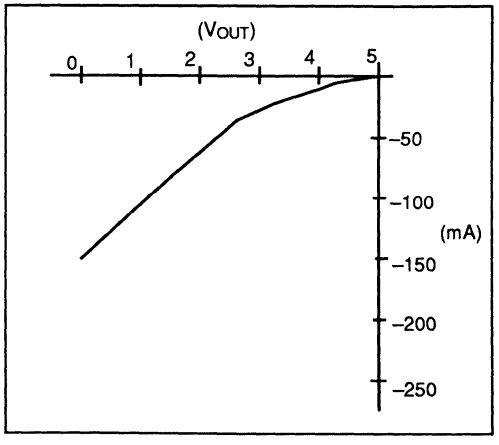


Figure 2A. "4004" Z Step Logic "High" Characteristics

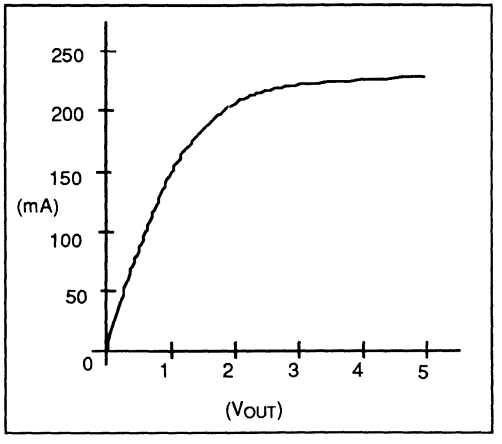


Figure 2B. "4004" Z Step Logic "Low" Characteristics

The output characteristic in the logic HIGH state is dominated by the current limiting resistor in series with the NPN pull–up transistor. As the output reaches the V_{CC} rail, the output characteristic is primarily influenced by the P–channel transistor. In the logic LOW state, the output characteristic is that of a large N–channel pull–down transistor. Note that the characteristics shown in Figure 2 represent typical process parameters at 25°C.

Y–STEP OUTPUT BUFFER

The circuit schematic for the Y step output buffer is shown in Figure 3.

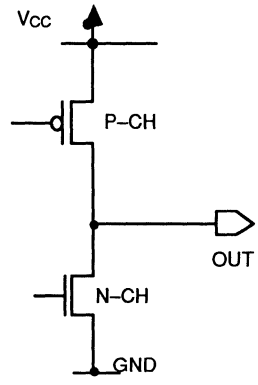


Figure 3. Y–Step Output Structure

This output structure is designed to get shorter propagation delays. The output characteristic in both HIGH and LOW states is non–linear as shown in Figures 4A and 4B, below.

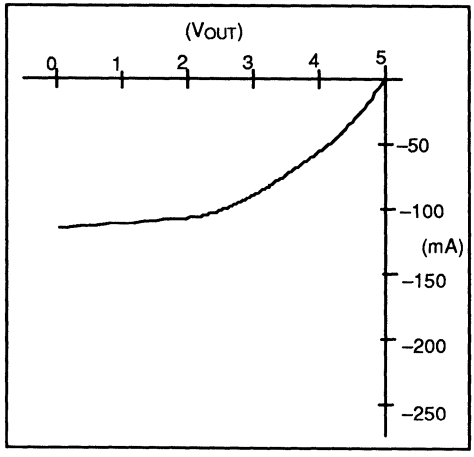


Figure 4A. Y Step Logic "High" Characteristics

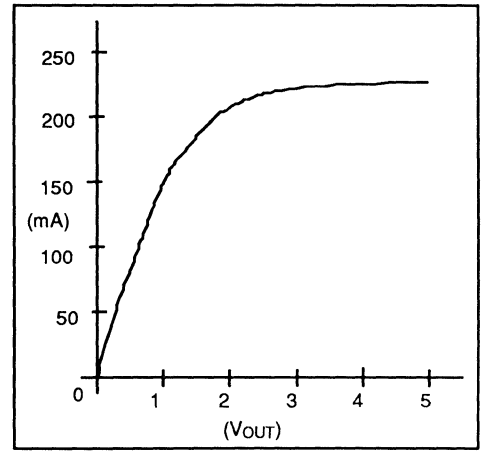


Figure 4B. Y Step Logic "Low" Characteristics

W STEP & "8000" Z STEP OUTPUT BUFFER

The schematic of the output buffer used in the "8000" Z step gate array as well as the W step devices is shown in Figure 5. The structure consists of a parallel combination of P–channel and N–channel transistors in the pull–up circuit and a large N–channel transistor in the pull–down circuit.

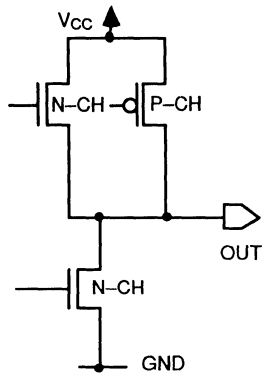


Figure 5. W Step and "8000" Z Step Output Structure

The pull–up structure yields an almost resistive characteristic in the logic HIGH state. The characteristic in the logic LOW state is again non–linear due to the N–channel transistor.

These output characteristics are shown in Figures 6A and 6B.

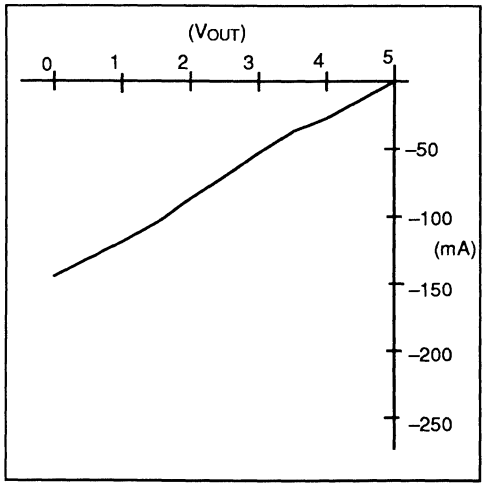


Figure 6A. W & "8000" Z Step Logic "High" Characteristics

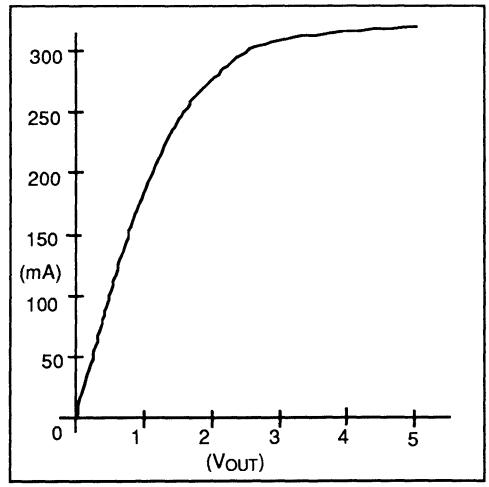


Figure 6B. W & "8000" Z Step Logic "Low" Characteristics

SUMMARY

The output V–I characteristics are determined by the circuit implementation and transistor geometries. Output buffer schemes and the corresponding typical characteristics for FCT devices manufactured in the Z, Y and W stepping are shown in this bulletin.

The characteristics are intended to aid the designer in developing nominal circuit simulation models so that the effect of driving different types of lumped and transmissive loads can be evaluated. In order to develop suitable models, the customer should first determine the stepping for the subject device. This information can be obtained by contacting IDT's LOGIC Marketing group.

Integrated Device Technology, Inc.

POWER–DOWN OPERATION

APPLICATION NOTE AN–53

By Suren Kodical

INTRODUCTION

In a **POWER–DOWN** mode, a device operates with a supply voltage that is lower than the normal operating range of 5V ± 5 for commercial grade and 5V ± 10 for military grade. *This should not be confused with the "low–power dissipation standby mode" of CMOS static RAMs where part of internal circuitry is shut off to reduce standby power.* The power–down mode is used to either conserve power in a part of a system or to provide a battery back–up in fault–tolerant systems. The devices operating in the power down mode are expected to co–exist with other devices which are connected to normal power supply rails in the same system. This bulletin discusses the use of our FCT devices in the power–down mode.

DESIGN FEATURES

All FCT and AHCT devices currently manufactured by IDT support rail–to–rail output voltage swing. This is a benefit in the power–down operation because the logic high noise immunity is not compromised. In addition, these circuits have the following design features:

- The inputs (except for I/O ports) do not have a clamp diode to V_{CC} but do have a clamp diode to ground to prevent excessive undershoot on the inputs.
- The outputs have P–channel pull–up transistors to raise output high level close to V_{CC}.

The P–channel devices have a junction diode as an integral part of the geometry. To prevent this junction from floating, the cathode of this diode is tied to V_{CC}, the most positive potential. Similarly, the N–channel transistors used in the output circuit have an integral junction diode whose anode is tied to GND, the most negative potential. Figure 1 shows the diodes associated with inputs and outputs.

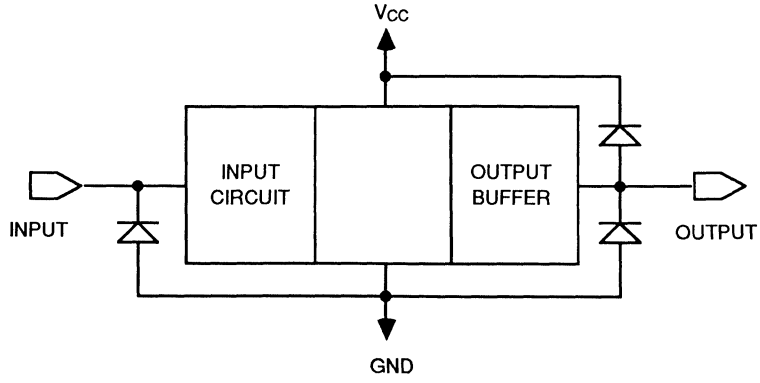


Figure 1. FCT Logic with Parasitic Diodes

POWER–DOWN OPERATION

Consider the case where an FCT or AHCT device operating in the power–down mode (say at a V_{CC} of 3 volts) is driven from another device operating from a higher V_{CC}. Because of the absence of a diode clamp to V_{CC}, there is no current flow from the driving device into the low voltage power supply through the input pin. The FCT and AHCT inputs thus permit power down operation on the input side.

An FCT or AHCT device in the power–down mode can easily drive TTL–compatible inputs or I/O ports, because the TTL–compatible inputs normally demand negligible input current in the logic high state.

LIMITATIONS

The presence of a diode from the output pin to V_{CC} as shown in Figure 1, however, imposes certain limitations in the power–down operation when the output of a device which is powered down is in the high–impedance state and the bus to which this device is tied is driven by another device operating from a higher V_{CC} (see Figure 2).

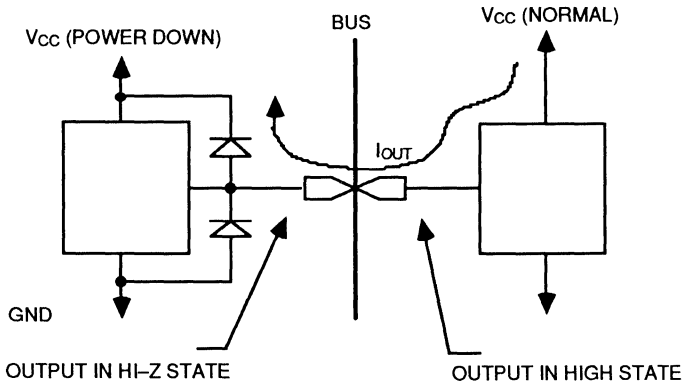


Figure 2.

In this case, the output diode to V_{CC} provides a low impedance path to the lower V_{CC} if the interfacing device output is in the HIGH state and the logic HIGH voltage is in excess of the power–down supply rail by more than a forward diode drop. In such an event, the logic high voltage will be clamped. This is normally not a serious issue if the driving devices have bipolar outputs or N–channel CMOS outputs with reduced voltage swings. However, if the driving device pulls up to V_{CC} and offers a low source impedance, the current into the output of the FCT or AHCT device in the power–down mode can exceed the absolute maximum rating. This situation can be avoided if a current limiting resistor (25 ohms or more) is used in series with the outputs of the device in power–down mode.

A similar restriction applies to I/O ports of devices such as the FCT245 and FCT646 when operating from a lower V_{CC}. The I/O port consists of an input node physically connected to an output which can be put in high–Z state when the port is to be used as an input. The presence of P–channel pull–up transistor in the output circuit adds a parasitic diode to V_{CC} at the I/O port. Therefore, this diode will offer a low impedance path to the lower V_{CC} if the driving device pulls up to the higher (nominal 5V) V_{CC}.

SUMMARY

The design of the FCT and AHCT input structures facilitates use of these devices in a dual–rail system or in a power–down mode to conserve system power or to provide a battery back–up. Although the design of the output structures imposes a limitation in certain power–down situations, it can be overcome easily.

Integrated Device Technology, Inc.

FCT–T LOGIC FAMILY

APPLICATION NOTE AN–54

By Suren Kodical

INTRODUCTION

Present day systems and board level products have two important characteristics; higher clock rates to obtain improved throughput and higher packing density to reduce space and cost. System designers are demanding higher speed and user friendliness from IC vendors to cope with the tight timing requirements and with the switching noise induced by high–speed TTL circuits. As discussed in the Application Note entitled "***SIMULTANEOUS SWITCHING NOISE***", high speed and simultaneous switching noise (particularly Ground Bounce) go hand in hand. For a given speed, less board–level noise translates into reduced design time, lower rework cost and better quality of outgoing product. Since most standard "glue" logic elements such as buffers, transceivers, latches and registers are used for their high drive capability and speed, they can also become the primary source of noise. Therefore, vendors of such high–speed circuits are faced with the challenge of providing "*friendly but fast*" glue logic to the performance–driven user.

IDT has met this challenge with the FCT–T family of standard logic which is designed to give the best speed/noise trade–off to the system designer. This new logic family features reduced output voltage swing and a high current output stage designed to minimize simultaneous switching noise. In this application note, we discuss this TTL–compatible family in terms of its features and benefits, product characteristics, performance curves and certain special features.

WHAT IS FCT–T LOGIC?

The FCT–T family is form, fit and function compatible with the industry standard FCT family of high–speed, high–drive logic from IDT. The FCT–T family offers the same speed grades (standard, A, B and C) as the FCT family while generating much lower level of noise (particularly ground bounce). It is, therefore, backward–compatible with the FCT family of products in all applications where rail–to–rail switching at the output is not essential. Typical FCT–T output logic levels are 0.1V in the logic LOW state and 3.3V in the logic HIGH state.

The FCT–T family also includes several products with *power off/up/down disable* feature. These are intended for backplane driving, especially in applications which require "hot insertion" capability for the boards without interrupting system operation.

FCT–T FEATURES AND BENEFITS

The key features of FCT–T family are described below:

TTL Level Outputs — The output pull–up circuit has been modified to offer a quiescent output HIGH level of about 3.3V, similar to most bipolar and BiCMOS output stages. This feature makes FCT–T truly compatible with existing bipolar and BiCMOS functions and thus offers an attractive low–power alternative without any performance penalty.

Ground Bounce Control — The output pull–down circuit has been modified to control the rate of build–up of current in the "sink" transistors so that the Lgdi/dt effect is minimized (Lg is the total inductance in the ground return path) and ground bounce is reduced for a given speed. This feature also slows the output edge rates and minimizes transmission–line effects on PC boards.

Input Hysteresis — Input buffers (TTL–to–CMOS translators) have been designed to offer 200mV (typical) hysteresis in order to improve both high and low level noise immunity. This feature decreases propensity for data loss or oscillations in high noise environment and offers immunity to noise superimposed on slow input signal transitions.

Variety Of Speed Grades — The FCT–T family offers the following speed grades:

FCTxxxT — corresponds to FCTxxx
FCTxxxAT — corresponds to FCTxxxA
FCTxxxBT — corresponds to FCTxxxB
FCTxxxCT — corresponds to FCTxxxC

The system designer can choose the speed grade necessary for optimum performance. It is important to note, however, that there is a strong correlation between the amount of simultateous switching noise and speed. Therefore, designers using higher speed devices should pay careful attention to board layout, termination, decoupling and package selection in order to get the maximum benefit.

Compatibility — The FCT–T logic family is compatible with all other TTL compatible logic families (AS, ALS, FAST, BCT, etc.). The reduced output swing makes the FCT–T outputs look very much like standard bipolar outputs. The static noise margin when driving from an FCT–T device is the same as that with any bipolar output device in the logic HIGH state. In the logic LOW state, the typical static noise margin is greater with the FCT–T family than with any bipolar logic family because of the absence of a voltage offset usually seen in bipolar Schottky outputs in the logic LOW state. Input thresholds are set to be within the 0.8V and 2.0V range.

Power–Off Disable — Certain members of the FCT–T family are designed to offer the power off/up/down disable feature. These devices with 3–state control maintain high–impedance state at their outputs during power supply ramping and power down (i.e., V_{CC} = 0V) if the Output Enable pin is conditioned to *disable* the outputs. This feature is attractive, and often essential, for backplane drivers in applications which require *hot insertion.* These applications include on–line transaction systems, factory floor automation, critical medical life support systems, etc. This feature is currently offered in double density devices with high drive capability, since these devices offer board space savings in backplane environment.

JEDEC Standard 18 Compliance — FCT–T specifications meet or exceed the requirements of JEDEC Standard No. 18 entitled **"Standard for Description of 54/74FCTXXXX, Fast CMOS TTL Compatible Logic"**.

FCT–T CHARACTERISTICS

In this section, we discuss various characteristics of the FCT–T family. This information is offered to the system designer to understand the operation of a device, boundary conditions and interface requirements in terms of transmission line driving.

DC CHARACTERISTICS TABLE

Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%
Military: T_A = –55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IL}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IH}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max. V_I = 0.5V	Except I/O Pins	—	—	–5	µA
			I/O Pins	—	—	–15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max.; V_I = V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min.; I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.; V_O = GND[3]		–60	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL.	2.4	3.3	—	V
			I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	V
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Line Drivers	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} Standard, 3–State and 800 Series	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.; V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

Figure 1.

The table in Figure 1 is similar to that for the FCT family of products. Significant differences are summarized below. Then individual parameters are discussed in detail with the aid of circuit schematics and V–I characteristics.

Differences between FCT–T and FCT

1. V_{OH} limit of 2.4 volts is guaranteed at –6mA military and –8mA commercial for the FCT–T family. The corresponding currents are –12mA and –15mA, respectively, for FCT.

2. Maximum limit of –225mA has been added to the I_{OS} (Short Circuit Current) specification to maintain compatibility with other TTL–output families.

3. Since the output voltage swing is reduced, low drive (300µA) specifications for logic HIGH and LOW levels have been omitted. Similarly, all specifications at V_{CC} = 3.3V have been omitted, as these CMOS level output specifications are not applicable.

4. Hysteresis specification has been added to indicate the amount of nominal hysteresis built into the design.

5. Static I_{CC} specification has been added to maintain compatibility with other TTL data sheets.

INPUT CIRCUIT AND CHARACTERISTICS

The input circuit for the FCT–T family is shown in Figure 2.

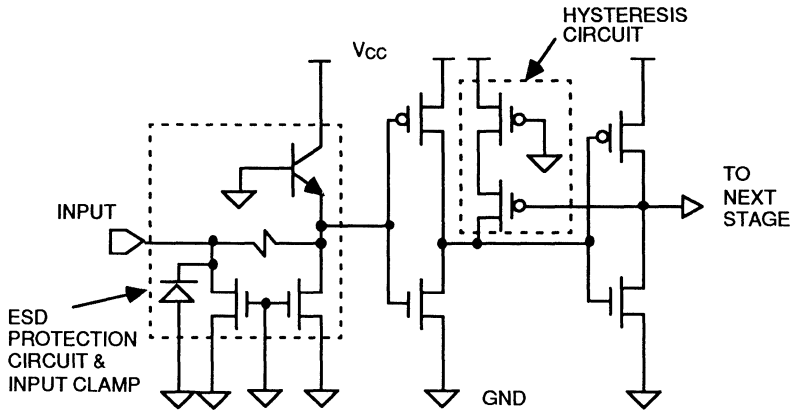


Figure 2. FCT–T Input Stage

The input stage is, in effect, a TTL to CMOS translator. It consists of (a) Input clamp diode to limit input voltage undershoots to approximately one diode below ground, (b) ESD protection circuit, (c) Input buffer designed for TTL threshold with a typical 200mV hysteresis and (d) Inverter which interfaces with the following stage.

Hysteresis is achieved by means of a change in the ratio of P–channel to N–channel transistor areas in the input translator. Typical V–I characteristics of the input stage is shown in Figure 3A and the typical transfer characteristic is shown in Figure 3B.

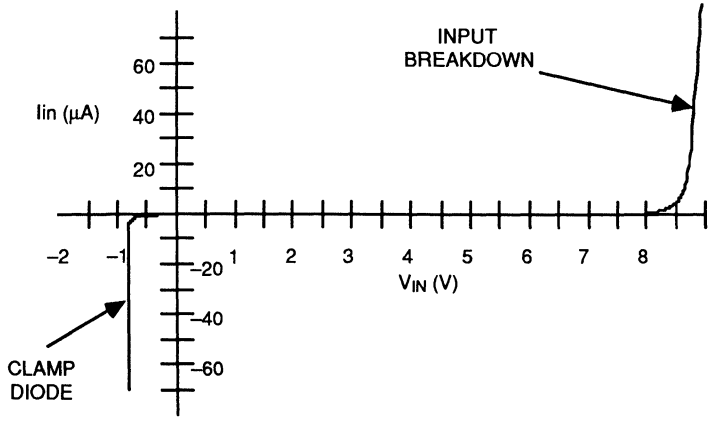


Figure 3A. FCT–T Input V–I Characteristics

The input current in the operating input voltage range is extremely low, in the order of nanoamps because of the very high input impedance of the CMOS gate. At voltages greater than one diode drop below device ground, the input offers low impedance because of the forward–biased input clamp diode. Input breakdown voltage is well outside the normal operating limit of V_{CC} (max).

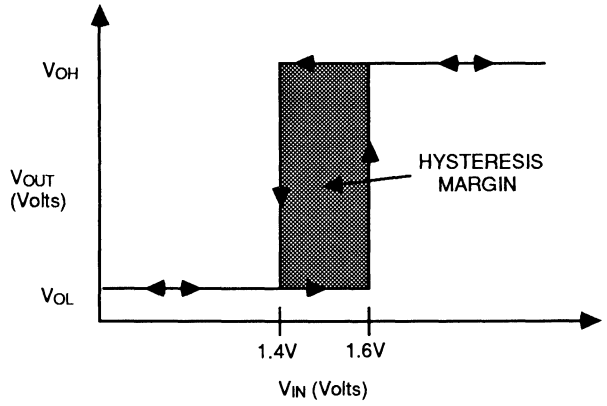


Figure 3B. Input Stage Transfer Characteristics

An important feature of the FCT–T logic family is that all inputs have hysteresis in the input stage transfer characteristic. Hysteresis increases static noise immunity in both logic states and also offers immunity to noise superimposed on slow edge–rate input signals, if the amplitude of the superimposed noise is less than the hysteresis margin.

OUTPUT CIRCUIT AND CHARACTERISTICS

The FCT–T output circuit is designed for a nominal voltage swing of about 3.3V. (In comparison, the FCT family output swing is from rail to rail.) The reduced output swing has certain benefits:

Benefits of reduced output swing

1. The output characteristics of FCT–T logic more closely match those of the industry–accepted Bipolar and BiCMOS logic families (AS, ALS, FAST, BCT, etc.).
2. Nominal threshold of any TTL inputs tied to an FCT–T output is almost in the middle of the output swing. Therefore duty–cycle distortion of signal propagating through a chain of devices is minimized.
3. For the same High–to–Low edge rate, reduced output swing would result in improved t_{PHL} because of smaller output voltage excursion relative to a device with full rail–to–rail output swing. Alternatively, a given t_{PHL} spec can be met with a slower High–to–Low edge rate. In the FCT–T family, we have taken advantage of this latter feature and improved the output circuit to reduce ground bounce as well as the level of radiated noise (EMI and RFI) caused by sharp output transitions and fast edges.
4. Less energy is stored in the output load capacitance when compared with a rail–to–rail swing device. This results in less ground bounce for the same speed when compared with a rail–to–rail switching device.

Output Circuit Schematic

The equivalent circuit of a typical FCT–T output stage is shown in Figure 4.

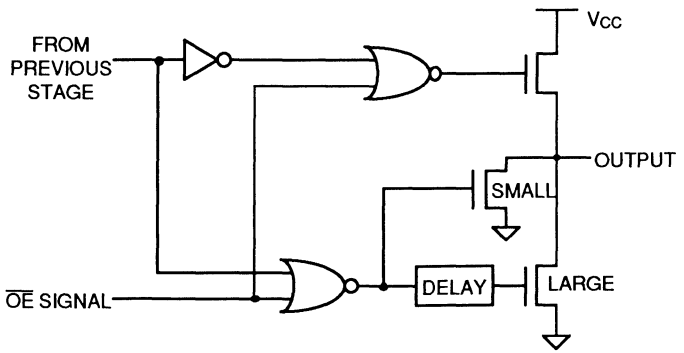


Figure 4. FCT–T Output Stage Schematic

The schematic shown here differs from a traditional CMOS output stage (P–channel pull up and N–channel pull–down) in the following ways:

- An N–channel pull–up transistor is used to obtain a voltage offset in the logic High state, so that the quiescent V_{OH} level is approximately 3.3 volts.
- The pull–down circuit consists of two stages. During the High–to–Low transition, a small N–channel transistor turns on first, followed by a large N–channel transistor after some delay. This arrangement results in a smaller di/dt in the ground return path during the output transition and adequate DC drive in the logic Low state. There are minor variations in the actual implementation of the output stage from mask–set to mask–set. The schematic shown is intended to give the general concept.

DC Output Characteristics (Logic LOW and HIGH States)

Typical DC output characteristics for the logic LOW and HIGH states are shown in Figures 5A and 5B, respectively. These curves are obtained at 25°C and V_{CC} = 5 volts.

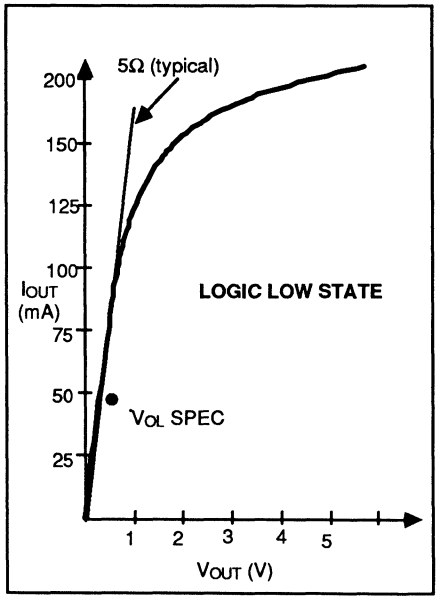


Figure 5A. Output Low Characteristics

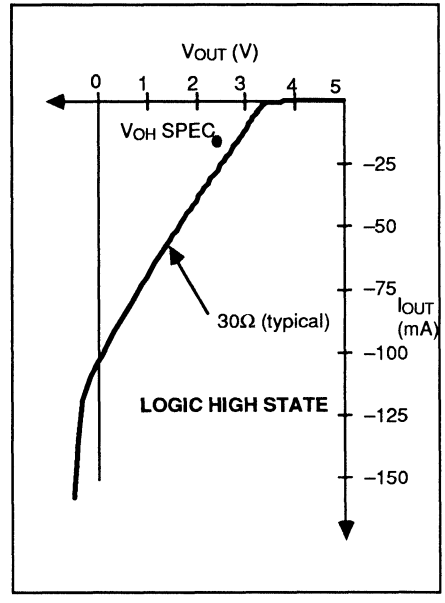


Figure 5B. Output High Characteristics

The output characteristic in the logic LOW state shows high static drive capability and low output impedance in the linear region. Typical output impedance in the LOW state is 5Ω.

The output characteristic in the logic HIGH state has a slope of 30Ω typical. This relatively high output impedance and the reduced voltage swing make the LOW–to–HIGH transition the worst case for incident wave switching. The characteristics are presented here to assist the system designer in determining proper termination based on the application at hand.

DC Output Characteristics (High Z State)

The output characteristics in the High Impedance state are shown in Figure 6 on the following page. The breakdown region for output voltage above V_{CC} depends on the actual circuit implementation.

In the High Impedance state, both pull–up and pull–down sections of the output stage are disabled. Therefore, the output ports exhibit very high impedance in the normal operating range. For output voltages below GND, parasitic junction diodes associated with the N–channel output transistors come into effect and offer very low output impedance to GND as shown by the diode characteristic in Figure 6. For output voltages above V_{CC}, one of two different characteristics can be observed:

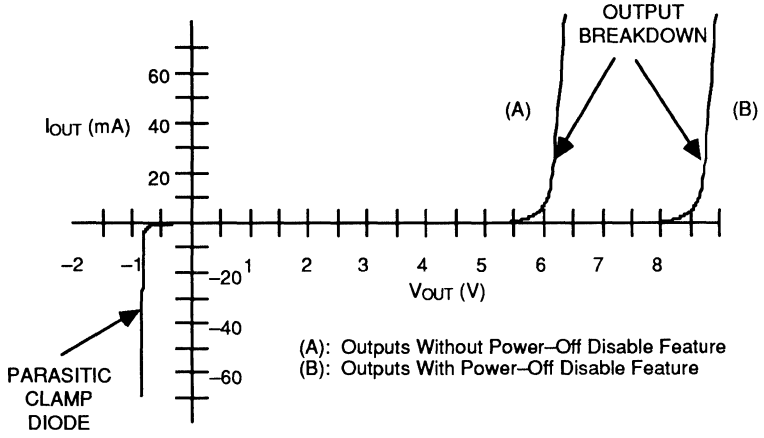


Figure 6. Output High–Z Characteristics

Curve (A): The devices with P–channel transistors in the output stage exhibit low impedance at output voltage greater than a diode above V_{CC}. These devices do not have the *"power–off disable"* feature.

Curve (B): The devices with the "power–off disable" feature show high output impedance at output voltages higher than V_{CC}. The output stage in these devices has been designed to avoid any parasitic junction diode to V_{CC}.

The "power–off disable" feature is discussed in detail later in this bulletin.

POWER SUPPLY CHARACTERISTICS

Components of Power Supply Current

There are three power supply current components in TTL compatible CMOS circuits:

(1) I_{CC} — The quiescent power supply current through the supply pin when all inputs are either at GND or at applied V_{CC}. This current normally represents internal leakages as well as pacakage–related leakages.

(2) ΔI_{CC} — The quiescent power supply current when inputs are held at "TTL levels", and

(3) I_{CCD} — Dynamic current caused by an Input Transition Pair (HLH or LHL). This current is a function of frequency associated with the signal transitions.

The total current $I_C = I_{CC} + \Delta I_{CC} + I_{CCD}$.

The last two components of power supply current are discussed in detail below.

ΔI_{CC} Characteristics

The input stage of a CMOS device draws current from the power supply pin for an input voltage range bounded by V_{tn} and $(V_{CC}–V_{tp})$ where V_{tn} and V_{tp} are the thresholds of N–channel and P–channel devices, respectively. Within this voltage range, both P and N channel transistors in the input translator stage are on (see Figure 2 for reference). Figure 7 shows the relationship between ΔI_{CC} and input voltage (V_{IN}) for a typical FCT–T input stage.

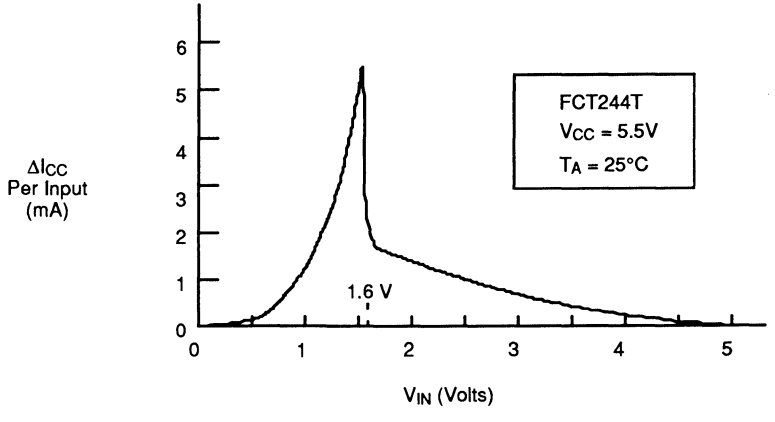


Figure 7. ΔI_{CC} Characteristics

As the input voltage is raised above V_{tn}, the ΔI_{CC} component increases, reaching a peak at the input threshold for the low–to–high transition. The sharp drop in current at threshold indicates the presence of hysteresis which effectively modifies the P–channel to N–channel ratio. As the input voltage is raised further, the ΔI_{CC} component falls because the P–channel transistor is being progressively turned off. Note that the characteristic is plotted "per input". The total current drawn from an IC depends on the number of inputs and the voltage applied to each input. The ΔI_{CC} parameter is specified for an input voltage of 3.4 volts at V_{CC} = max. in the data sheet.

Dynamic Power Supply Current – I_{CCD}

CMOS gates use power from the power supply source to charge and discharge parasitic capacitances when changing logic levels. This power is related to the frequency at which the logic level transitions occur. It is given by the formula:

$$\text{Power} = V \times i = fC_pV^2$$

where
f = frequency of logic level transitions,
C_p = parasitic capacitance associated with the gate,
V = voltage change on the capacitor, and
i = average switching current through the power supply path.

The average power supply current is given by $i = fC_pV$. Since this current is a function of frequency, it can be represented in the form of current per MHz and its value is given by C_pV with appropriate units. This is the *dynamic power supply current* for the gate. In a CMOS integrated circuit the total dynamic current is the sum of all such currents and is represented by I_{CCD}.

I_{CCD} is measured with the switching output(s) open, so that there is no influence of capacitance external to the package. Capacitive loading on the switching outputs will increase the measured value of I_{CCD} by an amount equal to the load–dependent fC_LV. Also, input transitions should be from GND to V_{CC} to eliminate any ΔI_{CC} component in the measurement. For devices with multiple identical paths (FCT244T Octal Buffer, for example), I_{CCD} is specified for one bit switching. Figure 8 shows a graph for dynamic power supply current for FCT244T buffer. This graph shows the linear relationship between I_{CCD} and frequency. I_{CCD} characteristic for an FCT244 with rail–to–rail output swing is also shown for comparison. The difference in the current at any frequency is due to the reduced output voltage swing.

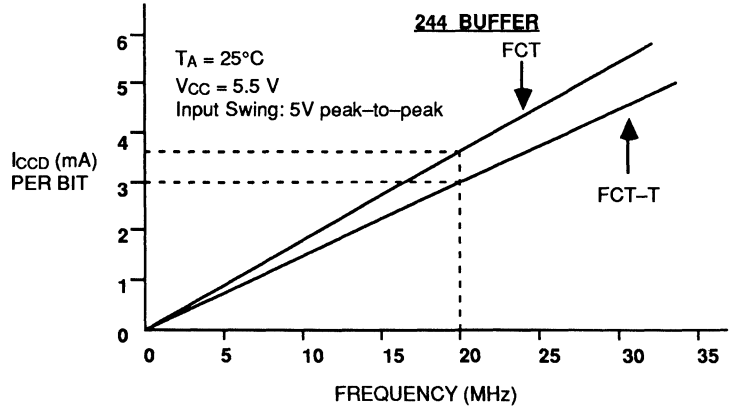


Figure 8. Dynamic Power Supply Current

NOTE: The units for I_{CCD} have the dimensions of current x time. Therefore, this parameter should be treated as "charge". In fact, the JEDEC Standard 18 for FCT logic uses the symbol Q_{CCD} for this parameter. In this application note, the author has chosen the symbol I_{CCD} since the measurement is in terms of current and is also consistent with the data sheets.

Figure 9, below, shows the Power Supply Characteristics table for FCT244T as an example.

SYMBOL	PARAMETER	TEST CONDITIONS		TYP.	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = V_{CC} or GND f = 0		0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V		0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	0.15	0.25	mA/ MHz

Figure 9. FCT244T Power Supply Characteristics

Total Power Supply Current – Example

From the information provided in the table above, the total power supply current can be calculated for a given operating condition. For example, let us assume that the FCT244T is used as a clock buffer, distributing the clock with a fan–out of 8 (one input, 8 outputs) at 25 MHz with 50 duty cycle. This clock distribution is accomplished by tying all inputs together. Output Enable pins are at GND. Inputs are driven from a TTL compatible device.

Typical power supply current I_C (*outputs unloaded*) is calculated as follows:

I_{CC} = 0.2mA
ΔI_{CC} = 0.5(duty ratio) x 8(switching inputs) x 0.5mA = 2mA
I_{CCD} = 25(frequency) x 8(switching outputs) x 0.15mA = 30mA

Therefore,
I_C = 0.2 + 2 + 30 = 32.2mA (typical).

Note that the above example shows the dissipation due to the device alone. In reality, the capacitive loading on the outputs will contribute additional power dissipation and must be taken into consideration for determining power supply requirements. This topic is discussed in depth in the Application Note entitled "*POWER DISSIPATION IN CLOCK DRIVERS*".

Similar calculations can be performed for any device once the operating conditions are known. In more complex devices, as well as in interface devices used in data and address paths, it is necessary to estimate the "average" frequency of operation to determine the total device dissipation under realistic operating conditions.

AC PERFORMANCE

Except for the reduced output voltage swing, the AC characteristics of the FCT–T family are the same as those of the FCT family in terms of operating conditions and limits. Given below in Figure 10 are the performance figures for four FCT–T logic parts for different speed grades. The performance is compared with the popular FAST family of bipolar parts.

FCT–T Speed Grades

DEVICE	74FCT–CT CMOS	74FCT–AT CMOS	74FCT–T CMOS	74F BIPOLAR	PARAMETER
244 Buffer	4.1ns	4.8ns	6.5ns	6.5ns	D to Y
245 XCVR	4.1ns	4.6ns	7.0ns	7.0ns	A to B, B to A
373 Latch	4.7ns	5.2ns	8.0ns	8.0ns	Dn to Qn
374 Register	5.2ns	6.5ns	10.0ns	10.0ns	CLK to Qn

Figure 10. FCT–T AC Performance Comparison

The variety of speed grades offer the system designer a choice in optimizing overall system performance. In many cases, the use of higher speed logic allows the designer a choice of using lower speed memory devices to reduce the overall cost of the system.

AC Performance Over Temperature Range

The AC performance of FCT–T family of products over the operating temperature range is similar to that of the FCT family. A normalized graph of t_{PLH} and t_{PHL} for the FCT244T device is presented in Figure 11 as an example.

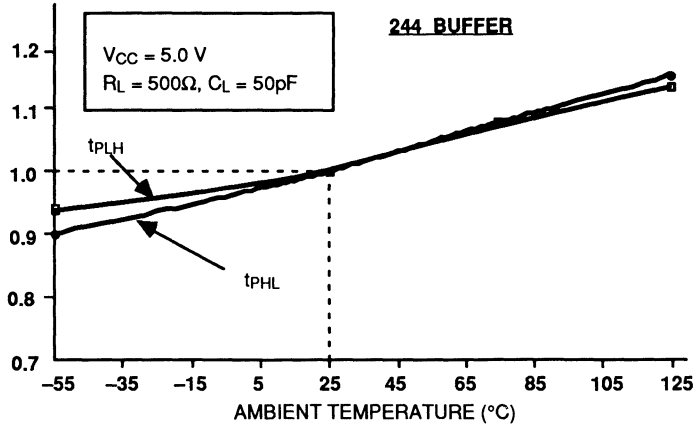


Figure 11. Normalized Switching Characteristics

Simultaneous Switching Noise

One of the primary benefits of FCT–T family of products is the improvement in performance with respect to simultaneous switching noise, or ground bounce, when compared with any CMOS family with rail–to–rail output swing. The combination of a modified TTL output stage and reduced output voltage swing results in a significant reduction in the magnitude of both the positive and the negative components of ground bounce. The relationship between ground bounce and t_{PHL} for the FCT244T is shown in Figure 12. The graph shows the improvement achieved when compared with the FCT family over the same speed range. All measurements are at V_{CC} = 5 volts and 25°C ambient temperature.

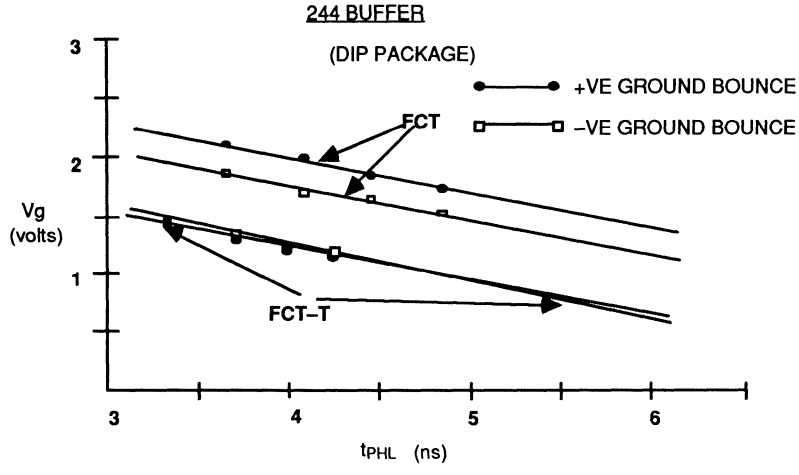


Figure 12. Ground Bounce vs. Speed

The reader is referred to the Application Note entitled "*SIMULTANEOUS SWITCHING NOISE*" for an in–depth discussion on the cause and effects of ground bounce and applications guidelines.

POWER–OFF DISABLE FEATURE

Power–off Disable is a condition where the output of a device maintains high impedance state **during power supply ramping** if the output enable control pins are conditioned to place the appropriate outputs in the high–Z state. This is a desirable feature in backplane applications where it is often necessary to perform "hot" insertion and disinsertion of printed circuit cards for on–line maintenance. It is essential that this activity does not violate data integrity on the backplane. Another application where this feature is useful is in systems with multiple redundancy where one or more redundant cards may be powered off while still plugged into the system. Under these conditions the backplane drivers on these cards should offer very low loading on the backplane.

Most drivers designed for backplane application do not offer this feature. For example, CMOS drivers which use a P–channel output transistor in the pull–up circuit have a parasitic diode to the V_{CC} rail at each such output. Therefore the output node offers a low impedance to the V_{CC} pin when the output voltage exceeds applied V_{CC} by a junction diode drop. This feature precludes use of such devices in applications which require power–off or power up/down disable capability.

Certain members of the FCT–T family (such as the 646/648T, 651/652T Bidirectional Register/Transceivers, FCT52/53T bidirectional registers, 620/621/622/623T backplane transceivers) offer the power off/up/down disable capability. When the outputs of these devices are conditioned to be in the High Impedance state, all 3–state outputs will offer high impedance independent of power supply voltage (excluding negative V_{CC} with respect to GND). The Power Off Disable capability is shown in the DC Characteristics table in the form of a leakage current of 100μA max. at V_{CC} = 0 volts and V_{OUT} = 4.5 volts.

SUMMARY

The FCT–T family of logic products is introduced in an effort to alleviate some of the simultaneous switching noise problems while maintaining compatibility with the industry–standard FCT family as well as with other TTL–compatible logic families. A variety of speed grades and packaging alternatives are offered to help design an optimum system in terms of speed, cost, performance and board space.

Integrated Device Technology, Inc.

CLOCK DISTRIBUTION SIMPLIFIED WITH IDT GUARANTEED SKEW CLOCK DRIVERS

APPLICATION NOTE AN-82

By Michel Conrad

INTRODUCTION

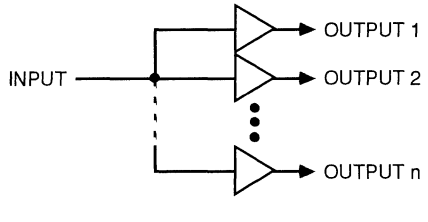
In today's world of RISC or CISC microprocessor based systems there is an endless quest for cost effective solutions which offer the best system performance. Faster processors, increased integration and innovations in architecture have resulted in high performance systems which can be packed into smaller and smaller boxes. With processor clock frequencies migrating towards 33, 40 and 50Mhz, clock signals are becoming more and more critical. As the clock period gets shorter, the uncertainty or skew in the clock distribution system becomes more of a problem. Since clocks are used to drive the processors and to synchronize the transfer of data between system components the clock distribution system is an essential part of the system design. A clock distribution system design that does not take skew into consideration may result in a system with degraded performance and reliability.

Designing a clock distribution system which minimizes skew is not a trivial problem. To address this problem IDT has developed the IDT49FCT805 and IDT49FCT806 guaranteed skew clock drivers. These high-speed clock drivers have been designed to minimize skew, thus simplifying the problem of designing a reliable, minimum skew clock distribution system. This application note discusses the issues surrounding clock skew, clock drivers, and clock distribution. It will show how the IDT49FCT805 and IDT49FCT806 can be used to simplify the design of minimum skew clock distribution systems.

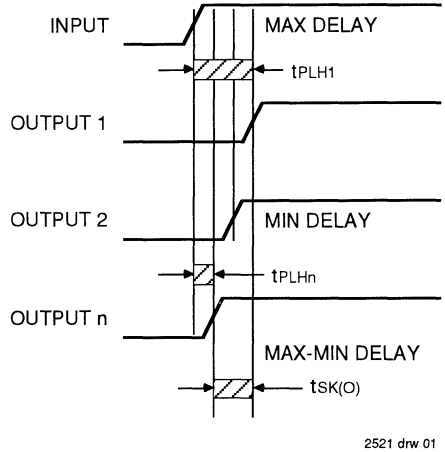
WHAT IS CLOCK SKEW ?

The term clock skew is used to describe the timing differences between signals in a clock distribution system. The non-ideal characteristics of system components and their connecting circuitry result in uncertainties as to when clock signals trigger their loads. Figure 1 shows a generalized, multiple output clock driver and its associated timing for the low-to-high transition. A common signal drives each input resulting in "n" copies of that signal on the clock driver outputs. The clock skew is the difference in propagation delay between the driver's slowest output and its fastest output. Since output "n" has the minimum propagation delay and output "1" has the maximum propagation delay, the clock skew is the difference or $t_{PLH1} - t_{PLHn}$.

In a typical system clock skew has two distinct sources. The first source of skew is the clock driver device itself. The clock driver is a piece of interface logic used to drive clock signal lines. With any given technology the clock driver is an inherent source of skew. In an ideal clock driver all the internal circuit elements of the device are perfectly matched so that propagation delays through equivalent paths are identical. In a practical clock driver there are many variables which can effect the propagation delay through equivalent paths and therefore contribute to skew. The layout and electrical characteristics of the circuit elements, the location of those elements relative to ground and Vcc, as well as the parasitics of the



Output Skew, $t_{SK(O)}$ =
$t_{P(max)} - t_{P(min)} = t_{PLH1} - t_{PLHn}$
(same package, same transition)



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Output Skew is the difference in propagation delay between the fastest and the slowest outputs of a single chip for the same input and output transition.

Figure 1. Output Skew $t_{SK(O)}$ Schematic and Timing Diagram

package can all have an effect on propagation delay. Many of these variables are dependant on manufacturing process parameters, which adds many more variables that can effect the skew characteristics of the device.

The second source of clock skew is the clock distribution system. How the clock driver device is incorporated into the clock distribution system is critical. The issues include the layout of signal lines, device loading, power supply connections and power supply decoupling. Operating conditions such as the power supply voltage and the ambient temperature also play a significant role. Because of the fast edge rates found in today's high speed logic, most PCB traces should be treated as transmission lines. If the design does not address the transmission line effects caused by the fast edge rates, the design may never work as intended.

THE CLOCK SKEW PROBLEM

Clock skew problems arise when the timing requirements of a system component are violated. Many of the common clocking bottlenecks can be categorized into two types of clock skew problems. The first is the synchronization problem caused by skew between multiple copies of a system clock. The second problem is that of meeting the duty cycle requirements of system components which require a controlled duty cycle.

A simple pipeline register can be used to illustrate the synchronization problem (Figure 2). The pipeline is composed of two registers and some clock circuitry. The clock circuit begins with a Master Clock which is buffered into two clock signals, CLK1 and CLK2. CLK1 drives Register X and CLK2 drives Register Y. The registers are configured to pass sequential data on each clock cycle so that the current output of Register Y is the previous cycle's output of Register X. The circuit's timing is shown in Figure 3.

In Figure 3-a the data sample "N" is the input to Register X and data "N-1" is the input to Register Y. For correct operation the input to each register must satisfy the setup and hold time requirements with respect to its clock. Since the output of Register X is the input to Register Y, the hold time tHy should not be greater than $t_{PDx(min)}$. In Figure 3-a CLK1 and CLK2 switch at the same time so that the output of Register X satisfies the setup and hold time requirements of the input to Register Y.

In Figure 3-b CLK2 is delayed relative to CLK1 resulting in a t_{SKEW} between the two clocks. Now, for correct operation the hold time t_{Hy} should not be greater than $t_{PDx(min)}$-t_{SKEW}. As shown, the skew in CLK2 causes a violation of either the hold time requirement of data "N-1" or the setup time requirement of data "N" as input to Register Y. For correct operation data "N-1" must be clocked into Register Y and in Figure 3-b it is unclear whether data "N" or "N-1" is clocked into Register Y. If the timing margin $t_{PDx(min)}$-t_{Hy} is about 2.5ns then a clock skew of 2.5ns or greater is a threat to the reliability of the system

Many microprocessor systems require that the clock have a controlled duty cycle. Guaranteeing a fixed duty-cycle at fast clock rates is difficult because propagation delays for opposite transitions in standard interface logic used for clock distribution are seldom identical. Also, timing differences between transitions do not scale with frequency. If a driver has 3.0ns of pulse skew (see definitions below) the tolerance of a 25ns cycle time (40Mhz) is ±12%. If the clock is pushed to 50Mhz, the tolerance grows to ±15%. A rule-of-thumb is that no more than 10% of the clock cycle be used for clock distribution. It is clear that if standard components are used the rule is easily violated at higher clock frequencies.

CLOCK SKEW DEFINITIONS

With the objective of minimizing skew inherent to the clock driver device, IDT has designed the IDT49FCT805 and IDT49FCT806 clock drivers. These clock drivers are designed to meet very tight skew specifications. The critical parameters are output skew, pulse skew, and package or part-to-part skew.

Output skew $t_{SK(O)}$ is the difference in propagation delay between any two outputs of the same device going through the same transition. This is the type of skew illustrated in Figure 1. If the propagation delay of the slowest output (t_{PLH1})

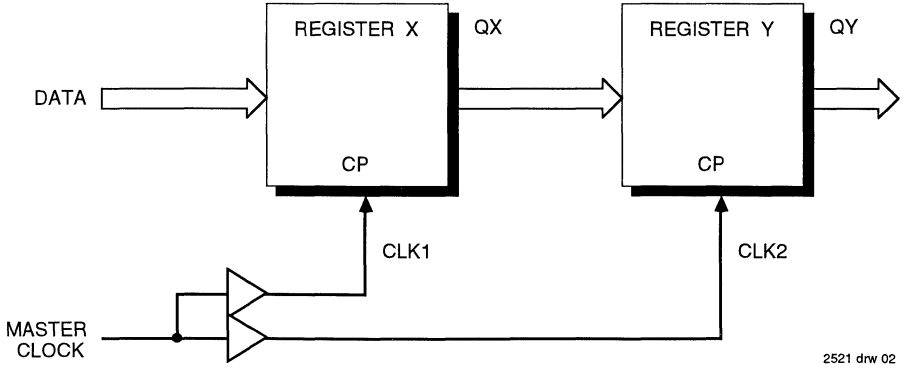


Figure 2. Schematic for a Two Register Pipeline

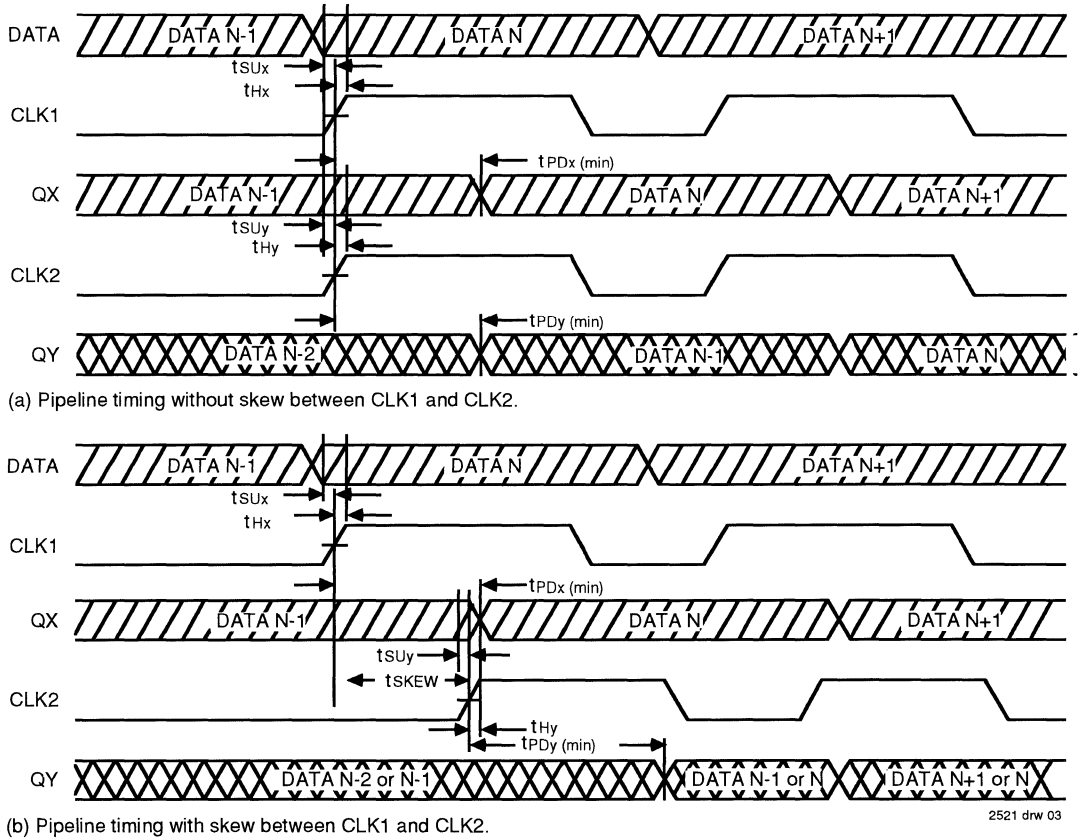


Figure 3. Timing Diagrams for Pipeline Register Example

is 5.0ns and the fastest output (t_{PLHn}) is 3.0ns then the output skew is 2.0ns. The $t_{SK(O)}$ parameter applies to all the outputs of a single clock driver chip. It is measured separately for the high-to-low and low-to-high transitions. Figure 4 shows the measured output skew of several IDT49FCT805As for low-to-high and high-to-low transitions. Under typical conditions (V_{CC}=5.0V, TEMP=25°C) the maximum skew is less than 450 picoseconds for both the low-to-high and high-to-low conditions. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 700 picoseconds over the commercial operating range.

Pulse skew $t_{SK(P)}$ is the difference in propagation delay for low-to-high and high-to-low transitions and is measured on a single output pin. In Figure 5, if t_{PLH1} is 5.5ns and t_{PHL1} is 4.0

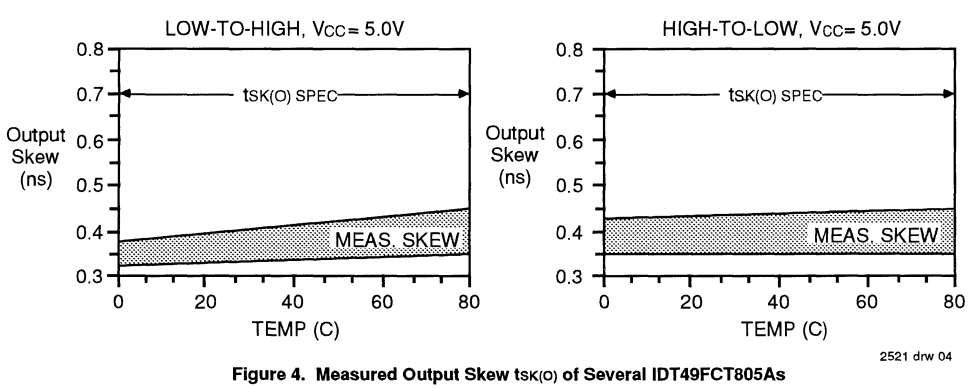


Figure 4. Measured Output Skew $t_{SK(O)}$ of Several IDT49FCT805As

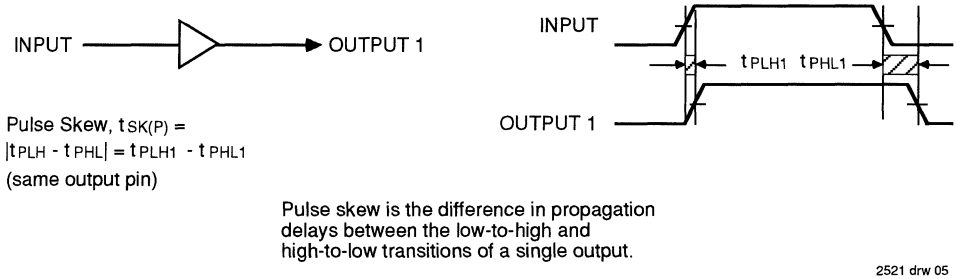


Figure 5: Pulse Skew $t_{SK(P)}$ Schematic and Timing Diagram.

ns, $t_{SK(P)}$ will be the the difference, or 1.5ns. Pulse skew is also a measure of the duty cycle distortion that the clock driver will contribute to an incoming clock signal. This is an important parameter for applications that use both edges of the clock and where a controlled duty cycle is required. Figure 6 shows the pulse skew measured on several IDT49FCT805As. Under typical conditions the measured pulse skew was less than 825 picoseconds. In the data sheet this value is guaranteed to be less than 1.0 nanosecond over the commercial operating range. For a 40Mhz clock with a period of 25ns, the IDT49FCT805/806 guarantees a maximum of 4% duty cycle distortion.

Part-to-part or package skew $t_{SK(T)}$ is similar to output skew. The difference is that it applies to outputs of two or more devices. The timing diagram in Figure 7 illustrates the case

49FCT805A PULSE SKEW VERSUS TEMPERATURE

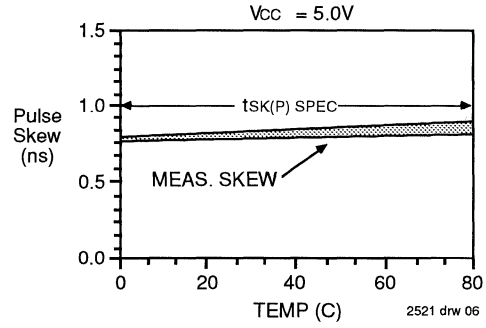


Figure 6. Measured Pulse Skew $t_{SK(P)}$ on Several IDT49FCT805As

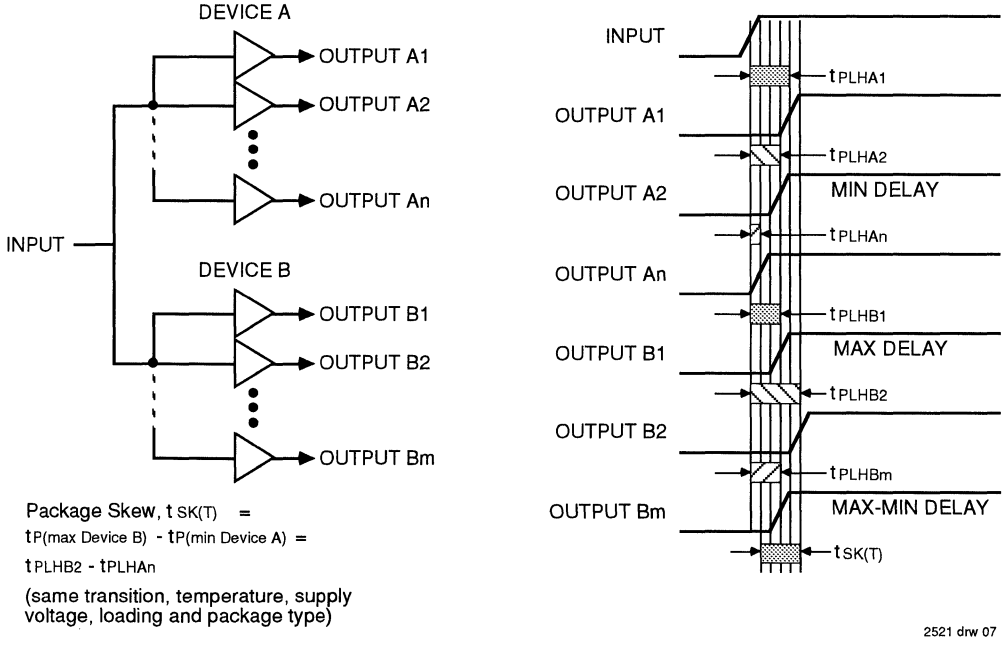


Figure 7. Package Skew $t_{SK(T)}$ Schematic and Timing Diagram

where two generalized clock drivers are driven by a common input. The result is "n" outputs from device A and "m" outputs from device B making the same transition. The package skew is the difference in propagation delay between the slowest output of one device and the fastest output of the other device for the same transition. In this case the output An is the fastest output and the output B2 is the slowest If t_{PLHAn} is 4.0ns and t_{PLHB2} is 6.0ns the package skew is 2.0ns. Certain conditions must be satisfied for the package skew specification to apply. The devices must have the same Vcc, ambient temperature and be assembled in the same package type. Also each device must have equivalent loading and be of the same speed grade.

Part-to-part skew is difficult to specify because it implies that the characteristics every part ever sold will operate within a window of operation. The window of operation ensures that parts that run too fast or too slow do not get sold. Figure 8 shows the measured values of package skew on several IDT49FCT805As under typical conditions. The maximum measured package skew from this sample is 525 picoseconds. In the IDT49FCT805/806 data sheet this value is guaranteed to be less than 1.5 nanoseconds over the commercial operating range.

49FCT805A PACKAGE (PART-TO-PART) SKEW VERSUS TEMPERATURE

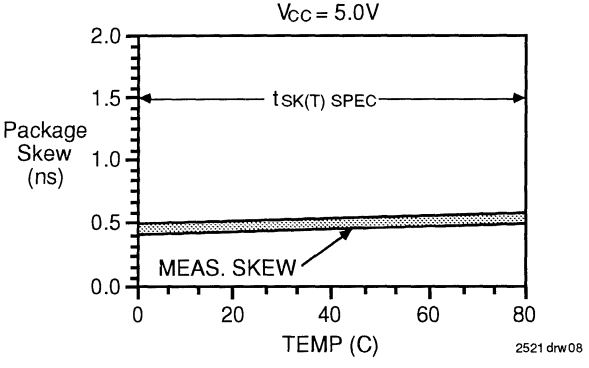


Figure 8. Measured Package Skew $t_{SK(T)}$ for Several IDT49FCT805As

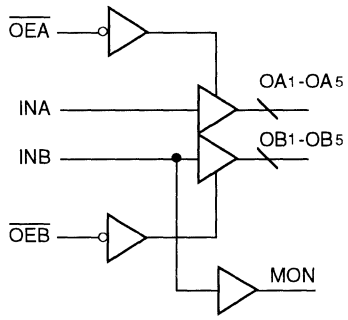
THE IDT49FCT805 & IDT49FCT806 CLOCK DRIVERS

The IDT49FCT805 and 49FCT806 are high-speed guaranteed skew clock driver chips specifically designed to meet the clocking requirements of today's high-performance systems. The logic diagram and pin configuration of the IDT49FCT805 are given in Figure 9. The IDT49FCT806 is the inverting option of IDT49FCT805.

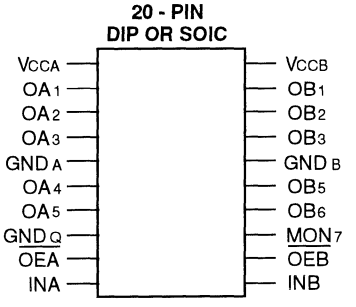
Skew in the IDT49FCT805/806 is minimized throughout the design process. Careful circuit design and layout in silicon have resulted in a pin configuration that is specifically designed for very low output and pulse skew. Independent power and ground pins reduce the amount of ground bounce and dynamic threshold shift caused by multiple outputs switching. The 1:5 input to output ratio reduces the amount of capacitive loading on the previous stage which simplifies termination and reduces component count when compared to conventional solutions. The devices are optimized for both PDIP and SOIC packages.

The IDT49FCT805/806 clock drivers consist of two independent banks of drivers. Each bank drives five output buffers from a single standard TTL compatible CMOS input. The input has 200mV of hysteresis for increased immunity to system noise. Independent active low output enable pins ($\overline{OEA}$ and $\overline{OEB}$) control each of the banks, allowing for independent control of the outputs. This feature may be used in applications where clock bussing or a power savings mode is required. The input IN_B drives the B bank as well as an output called MON (Monitor). The MON output is not controlled by $\overline{OEB}$ and therefore runs continuously. The MON signal can be used for priming phase locked loops or driving diagnostic hardware.

Each IDT49FCT805/806 has 3 ground pins and 2 VCC pins. The ground pins, GND_A and GND_B, are located in the middle of the package to minimize inductance in the ground return path. The two grounds are returns for the A and B bank output buffer and pre-driver currents. The third ground pin, GND_Q (Quiet Ground), provides a ground return for the remaining circuitry. The ground pin arrangement reduces ground bounce on the outputs and noise on the thresholds of the internal logic. Since GND_A and GND_B are completely



LOGIC DIAGRAM



PIN CONFIGURATION

2521 drw 09

Figure 9. Logic Diagram and Pinout of the IDT49FCT805

isolated from each other on the die, switching effects on one bank will have minimal effects on the other bank. The independent Vcc pins, VccA and VccB, supply power to the two banks.

Each output of the IDT49FCT805/806 clock driver features a high current drive output buffer. These outputs can be used to drive both TTL and CMOS loads. With a typical Vol of 0.3 volts the buffer can sink 64mA. For a typical Voh of 3.8 volts the output buffer can source 24mA. These output buffers are optimized around the 1.5 volts switching threshold which is the standard for TTL compatible logic. These output buffers can easily meet the edge rate requirements of today's microprocessors and peripheral components. Typical edge rates for the IDT49FCT805A are 1.0 volt/nanosecond for risetime and 2.0 volt/nanosecond for falltime

WORKING WITH THE DATA SHEET

In the past, designers have used the minimum and maximum limits of a clock driver's propagation delay specifications to determine skew in their designs. With the IDT74FCT244A (t_{PHL} min=1.5ns and t_{PHL} max=4.8 ns) the difference between the two limits results in a 3.3ns window. With the IDT49FCT805/806, subtracting the minimum from the maximum limit is no longer necessary because the skew is specified in the data sheet. However, because the IDT49FCT805/806 data sheet still specifies a 1.5ns minimum for propagation delay there may be some confusion as to whether or not the skew specifications are real. In the following discussion it will be shown that meeting the skew specifications is not a problem for IDT49FCT805.

The Switching Characteristics (Table 1) for the FCT805A/806A show the maximum propagation delay ($t_{PLH/HL}$) to be 5.8 ns and the minimum propagation delay to be 1.5ns. If the skew is calculated by subtracting the minimum delay from the maximum delay the result is a number much larger than the $t_{SK(O)}$ spec of 700ps. How can IDT guarantee a 700ps output skew number and still have such a wide range of minimum and maximum propagation delay values?

The range of values between the minimum and maximum propagation delay reflects the wide range of conditions under which the part must operate and the range of manufacturing process parameters. Consider a part that under typical conditions has a median propagation delay of 5.0ns. According to the $t_{SK(O)}$ specification of 700ps, each output of that driver will switch within a 5.0±0.35 ns window. If the median propagation delay drops to 4.0ns, due to variations in Vcc or temperature, the specification guarantees that each output will then switch within a 4.0±0.35ns window. In the unlikely event that the operating conditions cause the median delay to drop to 1.85ns, then all outputs will switch within a 1.85±0.35ns window. It is important to recognize that all the devices are assumed to be operating under the same conditions. If one part is running fast because of cold temperature and high Vcc, all the other parts will be running fast as well. The following data is provided to show that the IDT49FCT805A does indeed meet its skew specifications over the commercial operating range.

Figure 10 shows the range of output skew measurements for low-to-high and high-to-low transitions with Vccs of 4.75 and 5.25 volts. For both low-to-high and high-to-low transitions,

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions [1]	IDT49FCT805/806 Com'l. Min.[2]	IDT49FCT805/806 Com'l. Max.	IDT49FCT805A/806A Com'l. Min.[2]	IDT49FCT805A/806A Com'l. Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay INA to OAn, INB to OBn	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.8	ns
t_{PZL} t_{PZH}	Output Enable Time OEA to OAn, OEB to OBn		1.5	8.0	1.5	8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time OEA to OAn, OEB to OBn		1.5	7.0	1.5	7.0	ns
$t_{SK(O)}$[3]	Skew between two outputs of same package (same transition)		—	0.7	—	0.7	ns
$t_{SK(P)}$[3]	Skew between opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	1.0	ns
$t_{SK(T)}$[3]	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5	—	1.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays
3. Skew guaranteed across temperature range but measured at maximum temparature only. Skew parameters apply to propagation delays only.

Table 1. IDT49FCT805/806 Switching Characteristics

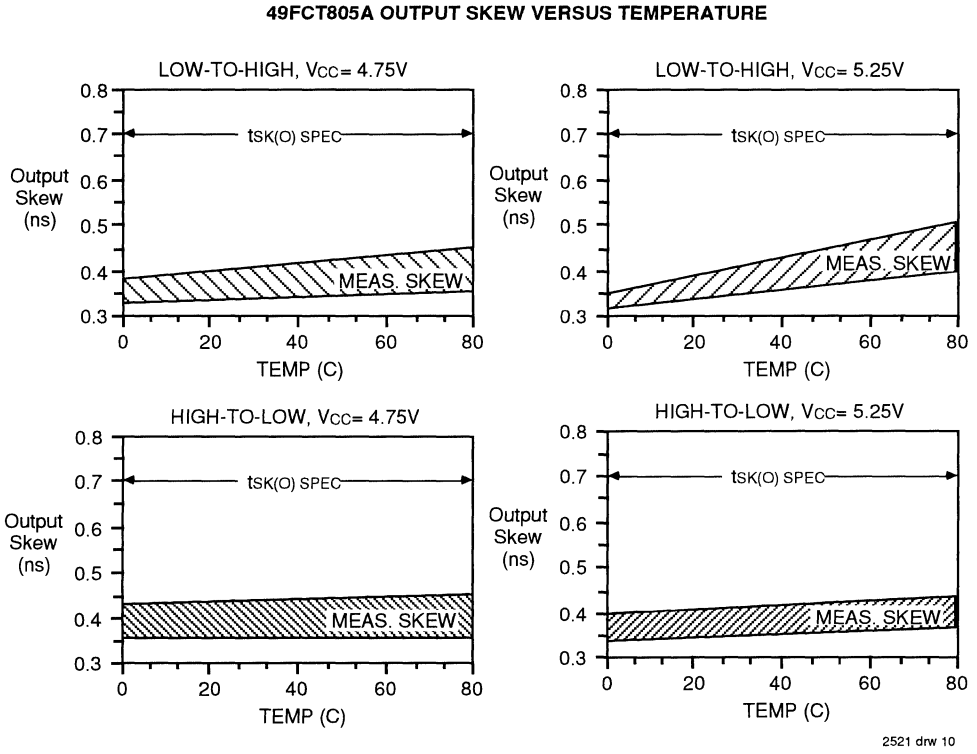


Figure 10. Measured Output Skew $t_{SK(O)}$ for Several IDT49FCT805As over the Operating Range

the graphs show that output skew is maximum at hot temperature (70°C). In each case the skew is well below the data sheet specification of 700ps.

Figure 11 shows the range of pulse skew measurements with Vccs of 4.75 and 5.25 volts. The measured pulse skew peaks at hot temperature and is slightly greater for a Vcc of 4.75V. The measured performance is safely within the data sheet specification of 1.0ns.

Figure 12 shows the range of package skew measurements for low-to-high and high-to-low transitions with Vccs of 4.75 and 5.25 volts. For both low-to-high and high-to-low transitions the skew peaks at hot temperature with minimal differences between low and high Vcc. Again the measured performance easily meets the data sheet specification of 1.5ns.

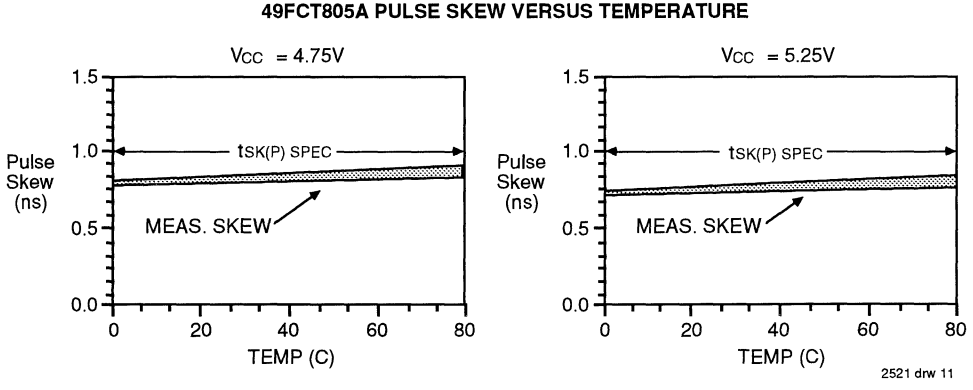


Figure 11. Measured Pulse Skew $t_{SK(P)}$ for Several IDT49FCT805As over the Operating Range

CLOCK DISTRIBUTION SIMPLIFIED

To show how easy it is to design with the IDT49FCT805, consider a hypothetical clock distribution system. The system has a 50Mhz clock source and must drive 75 loads. Each load is a CMOS input connected by 70Ω micro-strip trace at a density of 1 load every 0.5 inches. Assume that all the inputs are positive edge triggered and the objective is to minimize skew.

One approach would be to drive all 75 inputs with a single clock driver output (Figure 13). There are many problems with this approach. The first problem is the large amount capacitance associated with 75 CMOS inputs. Assuming 10pF maximum of capacitance per CMOS input, the total capacitive load is 750pF. A standard clock driver such as the IDT74FCT244A has Δt_{PLH} of 2ns/100pF for loads above 50pF. If the IDT74FCT244A is used the capacitance alone adds up to 14ns of additional propagation delay. If 75 loads are distributed along a single trace, the trace length is 38 inches (75 X 0.5 inputs/inch). If the PCB trace has an intrinsic delay of 0.15ns/inch (1), the delay from point B to point C is 5.7ns (38" X 0.15 ns/inch). Using a loaded trace delay of 0.37ns/inch (1), the skew between the ends of the trace approaches 15ns (38" X 0.37ns/inch). Given a 20ns cycle time (40 MHz), 14ns of clock skew implies that 70% of the clock cycle is given to clock distribution.

A second approach is the clock tree shown in Figure 14. By adding a level of buffers between the clock source and the 75 loads, the capacitive loading on the buffer outputs is reduced from 750pF to 50pF and the amount of PCB trace associated with each driver is reduced to 2.5". If IDT74FCT244As are used at least three packages (8 drivers per package) will be required. Since the 244's do not specify skew the designer might assume that each device output will switch within a 3.3ns window (t_{PHLmax}-t_{PHLmin}= 4.8ns -1.5ns). If the output transitions at points B, C, and D occur within a 3.3ns window, then the outputs of the second level (point E) may occur within a 6.6ns window. Assuming a 20ns cycle time (50Mhz) the designer has lost 33% of the cycle time to clock distribution without even considering transmission line effects.

A third approach is to use IDT49FCT805As as shown in Figure 15. Since each group of six buffers in Figure 14 can be replaced by 1/2 of an IDT49FCT805, only two devices are

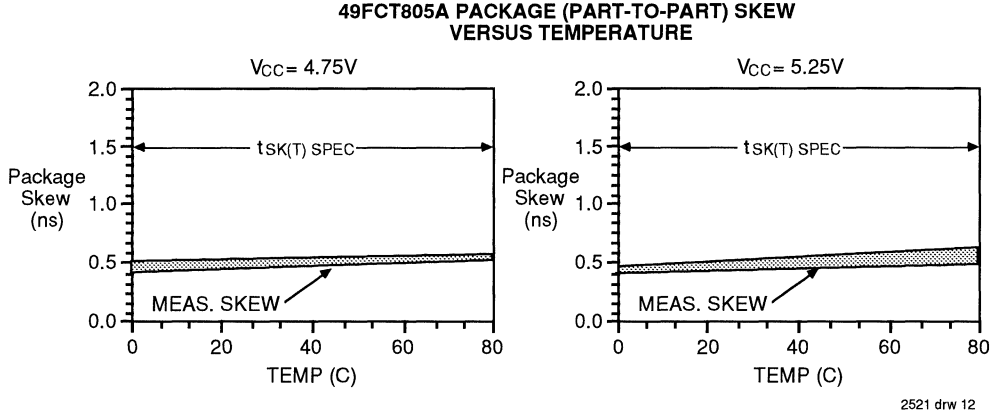


Figure 12. Measured Output Skew $t_{SK(T)}$ for Several IDT49FCT805As over the Operating Range

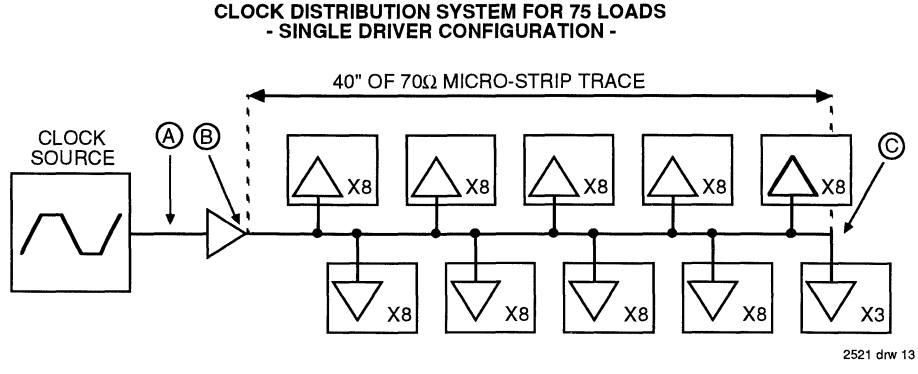


Figure 13. Single Driver Clock Distribution System

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

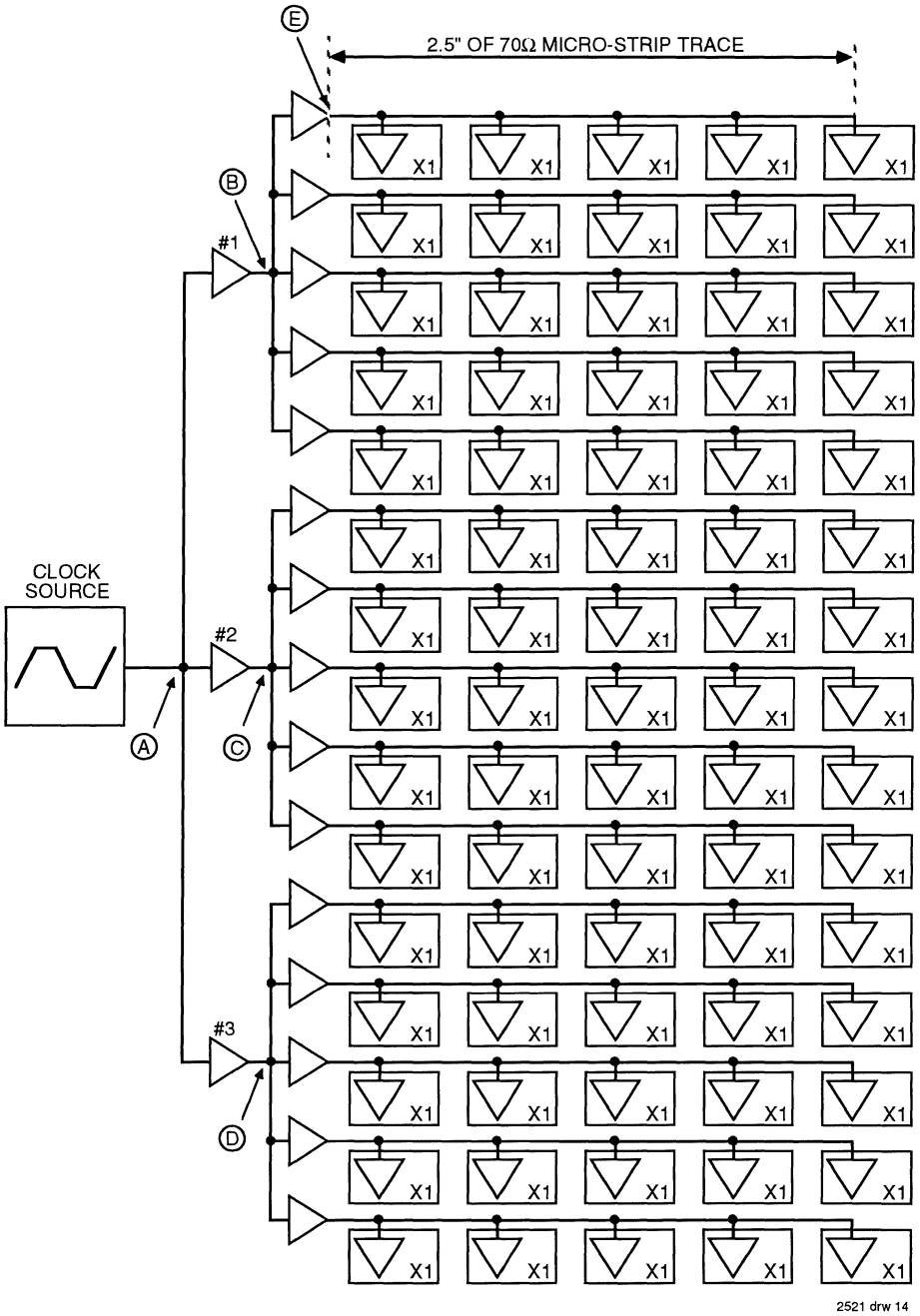


Figure 14. Clock Tree Distribution System Using 244's

CLOCK DISTRIBUTION SYSTEM FOR 75 LOADS
- CLOCK DRIVER TREE CONFIGURATION -

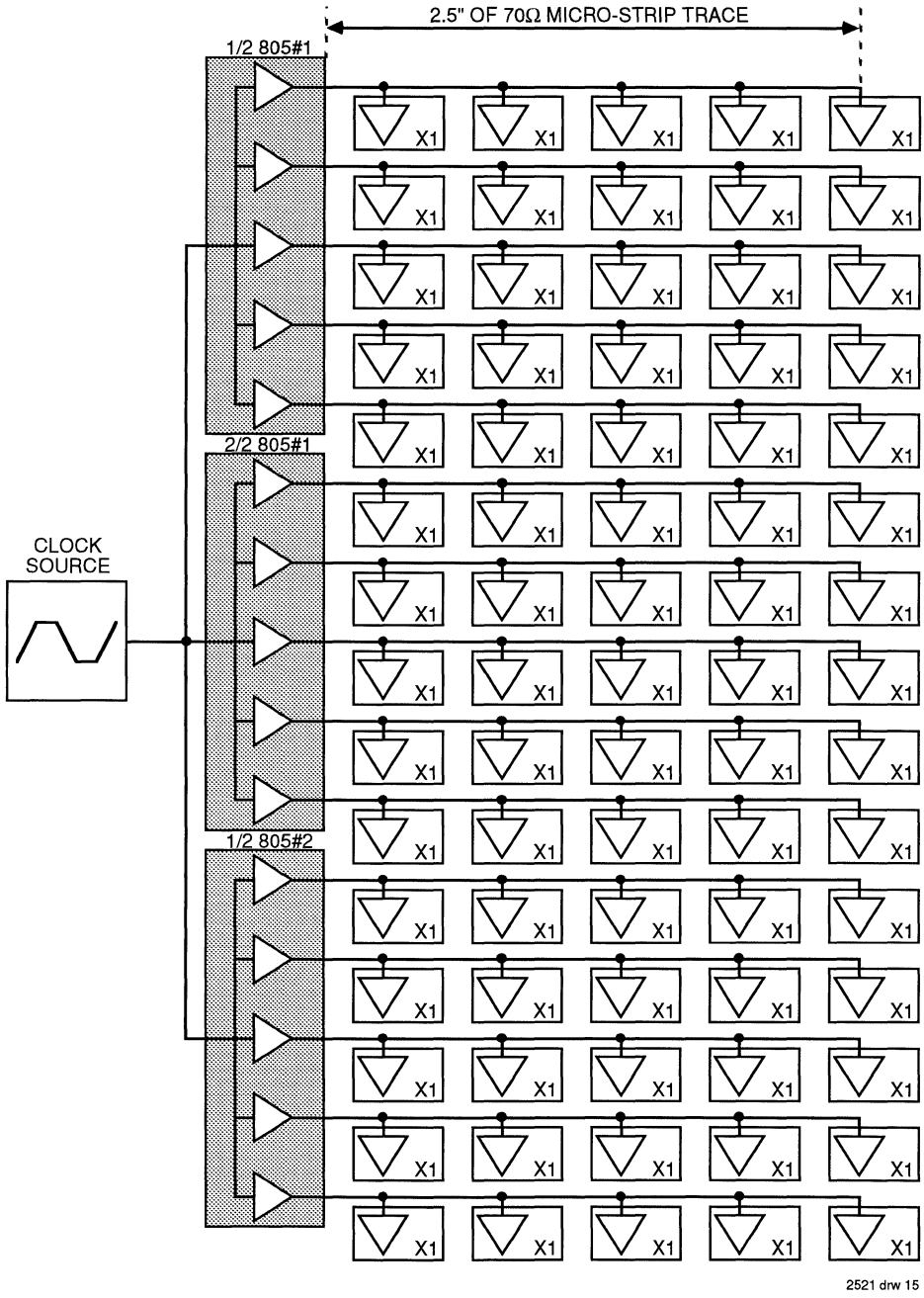


Figure 15. Clock Tree Distribution System Using IDT49FCT805's

required to implement the design. Using the 1.5ns package skew specification reduces the 6.6ns skew window to a 1.5ns skew window. If 0.925ns of loaded trace delay (2.5" X 0.37 ns/inch) is considered the maximum skew is 2.425ns including a 1st order treatment of transmission line effects. For a 20ns cycle time, the penalty imposed by the clock distribution system is reduced to 12% of the cycle time including transmission line effects. Besides reducing the size of the skew window of the second approach by 77%, the IDT49FCT805 increases the level of integration associated with the clock distribution tree. A significant benefit is the reduced loading on previous stages. Reduced loading helps minimize skew and makes the termination of clock lines clean and simple. The reduced chip count also saves valuable board space and simplifies the layout of the board.

SUMMARY

The following features of the IDT49FCT805/806 address clock driver skew and clock distribution problems:

- Circuit design, chip layout, and pin configuration specifically designed for very low output, pulse and package skew.
- Independent power and ground pins for reduced ground bounce and dynamic threshold shift.
- High current drive capability for driving heavily loaded/terminated PCB traces.
- 1:5 input/output ratio for reduced loading on previous stages.
- 11 outputs reduce the need for additional drivers—saves board space and simplifies PCB layout.
- Multiple grounds and Vccs to minimize ground bounce effects on propagation delay and skew.
- Input Hysteresis for increased immunity to system noise.
- Available in SOICs for increased packing density and reduced lead inductance.

RECOMMENDATIONS

To realize the performance benefits offered by the IDT49FCT805/806 clock drivers, IDT recommends the following high speed design practices:

- Use low impedance power and ground planes.
- Keep loading balanced and light.
- Keep trace lengths short, avoiding sharp bends and discontinuities (eg. use two 45° bends vs one 90° bend).
- Decouple both Vcc pins with a combination of capacitors (0.1μF and 0.01μF or 0.005μF) for effective high frequency filtering.
- Use termination for signal lines longer than 3 inches.
- Only use parts of same speed grade (non-A or A speed).

CONCLUSIONS

Clock skew is an important design consideration in today's high-speed systems. For successful and reliable operation, the clock skew must be kept within an acceptably small fraction of the system clock period. The IDT49FCT805 and IDT49FCT806 simplify the design of minimum skew clock distribution networks by specifying guaranteed low-skew performance. The skew specifications allow system designers to control the clock skew at each stage of the design which simplifies the problem of meeting global system requirements. With the IDT49FCT805/806 clock driver and a design methodology that pays close attention to high-speed design issues, maximum system performance can be achieved without risking reliability.

REFERENCES

(1) "Application Note AN-49", High-Speed CMOS Logic Design Guide, Integrated Device Technology Corp., November 1989.

Integrated Device Technology, Inc.

DESIGNING WITH THE IDT49C460 AND IDT39C60 ERROR DETECTION AND CORRECTION UNITS

APPLICATION NOTE AN-24

By Robert Stodieck

INTRODUCTION

The Error Detection and Correction (EDC) chip itself is one element of an EDC system. How it is connected to the surrounding system and controlled is left to the system designer. Because there are so many design variations possible, it is important for the designer to develop a clear idea of the target design before beginning the design process. Basic design approaches and perturbations are enumerated in this application note.

The details of the EDC control logic depend on the configuration of the EDC system, EDC bus topology, the nature of the CPU or system bus involved, and the nature of diagnostic hardware used. The data bus topology is highly dependent on the individual target system.

This application note approaches the bus topology issue first. The advantages and disadvantages of using EDC word widths that are different from the system bus are discussed. The next topic to be covered is the use of EDC in a system with a cache. Then the operational configuration of the EDC system is discussed. This implies answering questions about how the EDC unit handles errors in a particular system is discussed. How an operating system deals with the EDC function is discussed, followed by a practical discussion of some non obvious hardware topics. The final topic is memory system diagnostics and verification. An appendix includes tables and software that are useful in debugging and in writing diagnostic software for an EDC board.

Data Bus Topology

Most contemporary CPUs execute write operations of a byte or other sub-word width types. These cause special problems for all EDC units since EDC transactions with the memory are carried out on whole width EDC words. To facilitate partial word write operations with the IDT39C60 or IDT49C460 type EDC units, a set of tri-state transceivers are normally required between the system bus and the EDC unit. These buffers are required to prevent bus contention between the CPU or system bus drivers and the EDC units data outputs during partial word write operations. Figure 3 shows a bus arrangement appropriate for large DRAM arrays. The need for isolation of the EDC data bus and the system bus is shown by examining the data paths, shown with white arrows. These are used by the final write operation of a partial-word write cycle. In this case, only data bits 0–7 are being written from the processor to memory. If the processor or system bus drivers can be tri-stated on byte boundaries then this set of buffers could be removed, but this is not a common situation.

Depending on the memory size, additional buffering may be required between the EDC and the memory bus proper. The buffer configuration must be determined before beginning the EDC and memory controller design.

An appropriate general purpose bus topology is shown in Figure 1. It is common for one or the other sets of bi-directional buffers to be a latched type such as an IDT74FCT646 instead of the IDT74FCT245 shown. A family of waveforms appropriate for the bus format shown in Figure 1 is shown in Figure 2. The waveform diagrams do not include precise timing considerations which are left to the designer.

In any given system, any of the buffers separating the EDC from the memory IC's may be eliminated if bus capacitance and speed considerations allow.

EDC Bus Width vs. System Bus Width

The width of the EDC bus and the System Bus are normally matched. However, there are valid reasons for making the EDC bus both wider or narrower than the system bus.

Wide EDC words are significantly more efficient than narrower EDC word widths in terms of the amount of check-bit memory used for a given amount of data memory. The amount of check-bit memory required for 64 data bits is 8 bits if the 64 data bits are organized as one word and 14 bits if it is handles as two 32-bit words. Twenty-four bits of check-bit memory would be required for 64 data bits organized as four 16-bit EDC data words.

For the purposes of speed, it would be ideal to have 8-bit EDC words for systems that do byte write operations. This would make it unnecessary to ever have to read a memory location before writing a partial word on these systems. Unfortunately, eight-bit EDC words are grossly inefficient in terms of check-bit memory usage. Therefore, The EDC word widths are normally 16-bits or more.

Since the EDC word widths must generally be 16-bits or more for check-bit memory efficiency, and since general-purpose computers generally use byte or partial-word-write operations, general-purpose computers force the EDC unit to be able to process partial EDC word-width write operations. Partial word-width write operations require the EDC subsystem to execute a read-modify-write type memory cycle. Thus, the EDC controller must take over control of the memory system and execute a read before completing a partial word write. For some applications, where EDC is in use, it may be desirable to speed up processing by prohibiting partial word operations either at the hardware level or software level. Speed critical sections of code should be executed without partial-word write operations.

The read-modify-write EDC cycle executed during a partial-word write is identical to the EDC correction cycle executed during a read cycle when an error has occurred. The read-modify-write EDC cycle should not be confused with the read-modify write cycle executed by some CPU's.

Verification of a memory system using an EDC word wider than the system word is complicated by the fact that all memory write cycles become read-modify-write cycles (i.e. partial-word-write EDC cycles). Careful consideration of diagnostic procedures needs to be made during the design to avoid unnecessarily complex debugging procedures.

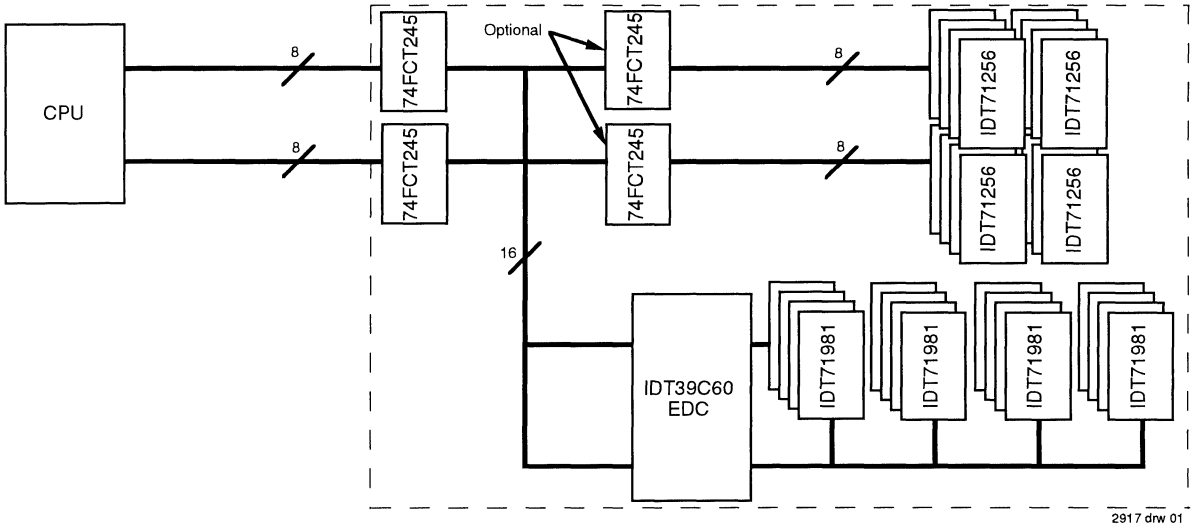


Figure 1. A general purpose 16-bit EDC data bus topology. Corresponding timing waveforms are shown in Figure 2. IDT74FCT245 buffers separate the EDC data bus from the CPU and the Main memory. Separate–I/O RAMs are used in the check-bit memory.

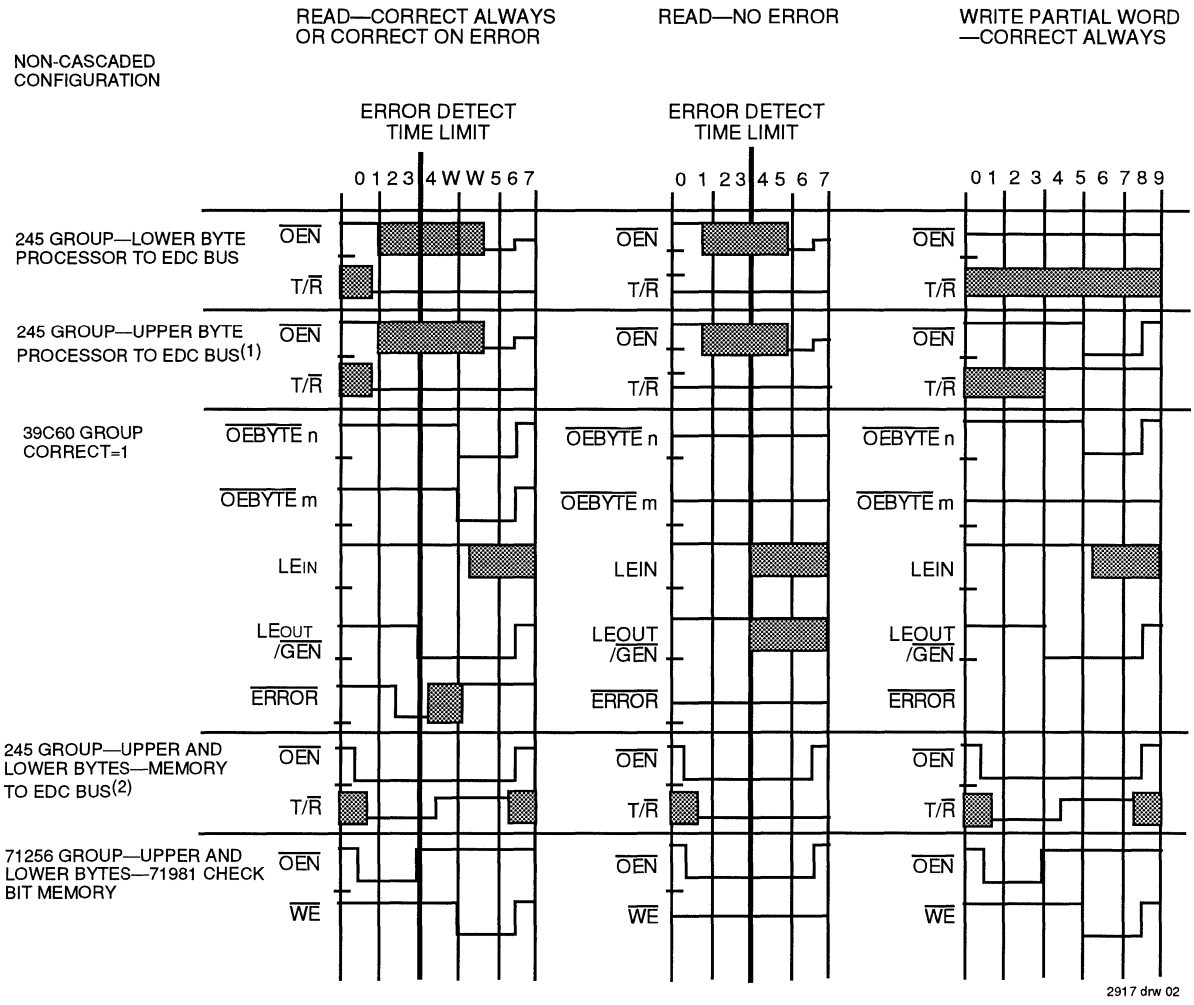


Figure 2. A sample family of timing waveforms for an EDC system. The target system is based on IDT71256 static RAMs for main memory with IDT71981 separate I/O RAMs for check-bit memory. (See Figure 1.) The partial word write case illustrates a low order byte write.

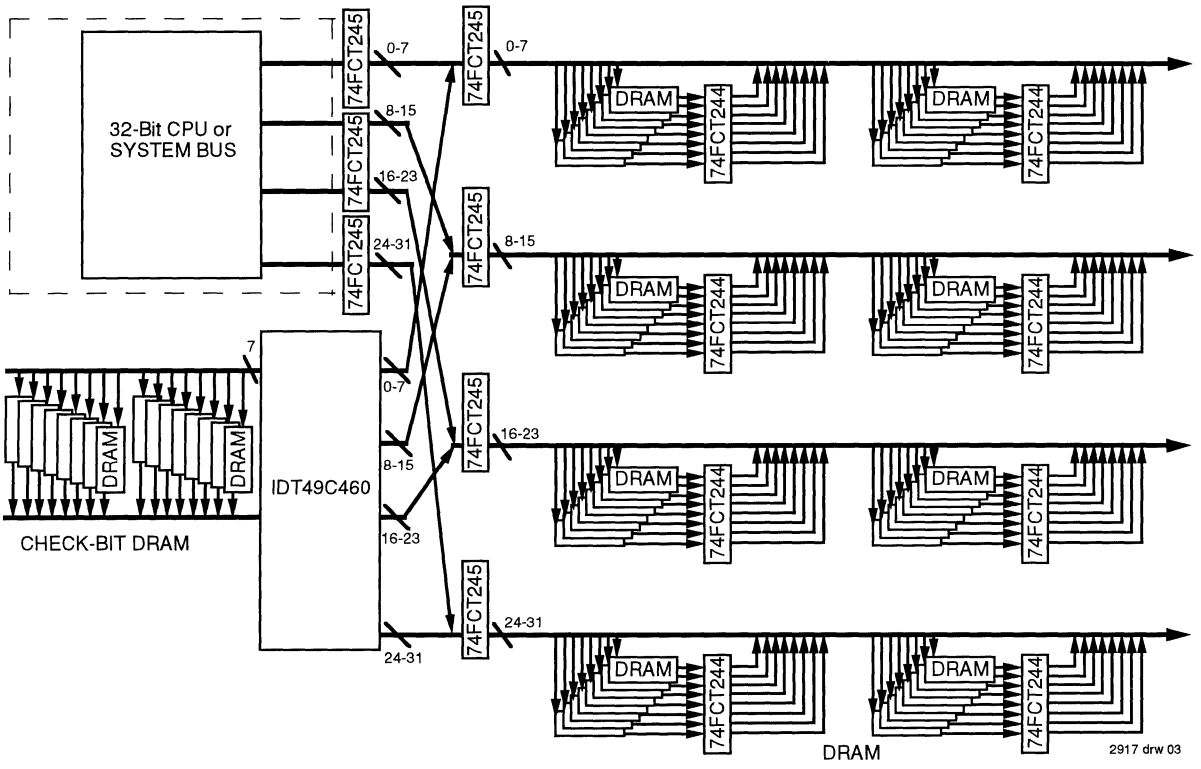


Figure 3. A general purpose 32-bit EDC bus topology for 1 bit wide DRAMs. The white arrows indicate the data flow paths used on the funal write phase of a partial word write cycle. Data bits 0–7 are being written into memory from the processor.

EDC in Systems Using Cache

In systems using cache memory, it may be desirable to place the EDC function between the cache and main memory, as opposed to locating the EDC function between the processing elements and cache. Parity can be used as a single-bit error detection scheme between the CPU and cache. RISC architectures tend to require more memory accesses per unit time than complex-instruction-set processors. This makes the use of cache memory more important in the RISC system. An appropriate bus topology for a RISC type processor with cache memory is shown in Figure 4.

Use of a cache memory also affords the possibility of using a different error correcting philosophy. If the EDC function is located between the cache and main memory, then it may be allowable for data reads to be corrected and sent on to the cache, but not to be immediately written back to main memory, after an error has been discovered. In this approach, corrected memory words are updated in the normal write-back processes of the cache memory.

Instruction reads must be thought of differently than data reads since instructions are normally not written back to memory from the cache. However, it may be possible to not write a corrected instruction word back to memory after detection, since the instruction is usually backed up on a different media. In most systems there is no way for the EDC to know whether it is operating on instructions or data, so a correction philosophy must be selected that can be applied to both instruction and data words.

Diagnostic Hardware

A syndrome latch for capturing syndrome values after errors and transferring them to the system data bus is always recommended. Providing a check-bit memory read-back ability allows direct verification of the gross functionality of the check-bit memory 'on board'. This greatly facilitates check-bit memory verification. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory, or a second latch may be provided to allow this.

Ideally, diagnostic hardware includes address latches to capture the address of an error. However, this may not be practical in any particular application. It may be sufficient to identify the individual RAM in which an error has occurred.

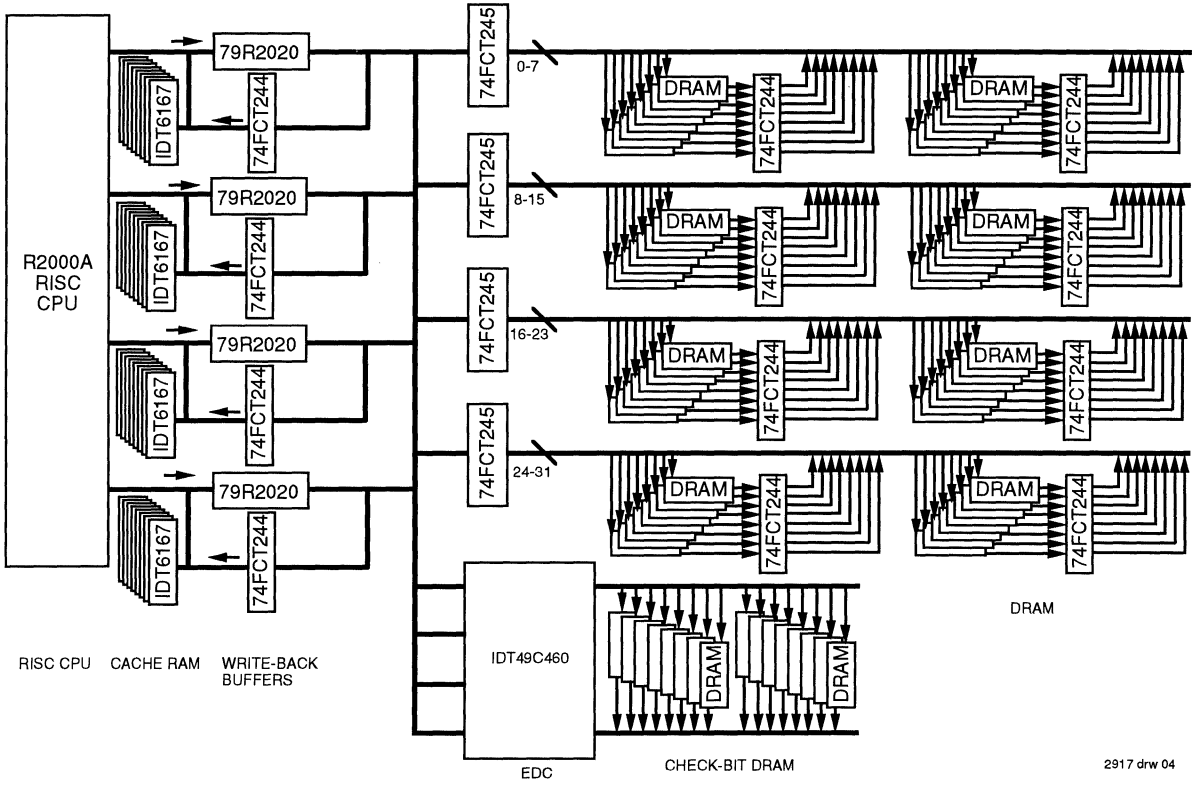


Figure 4. An EDC bus arrangement appropriate for a CPU with caches such as the IDT79R3000 or IDT79R2000 RISC processor.

OVERVIEW OF EDC OPERATIONAL MODES

Bus Watch vs. Correct Always for the Memory Read Cycle

In a bus-watch system, errors are only corrected after they have been detected by the EDC chip. Data is corrected and written back to memory to scrub errors, only after an error has been detected. In theory, the EDC chip only "watches" the bus normally, and does not slow memory read cycles with correction delays unless an error has been detected. Since errors during read operations are normally very rare, read cycle bus-watch systems are normally faster than correct-always systems.

In correct-always systems, data read by the system is always corrected. The EDC control logic is simpler to design and implement because there is only one type of read cycle. Memory cycle timing in correct-always systems can be completely deterministic and thus such systems may lend themselves more effectively to real-time applications.

Bus Watch vs. Correct Always for the Partial Word Write Cycle

A write operation that is of a width less than the EDC word width forces the EDC subsystem to execute a read cycle prior to actually writing to memory. This is required to provide the EDC unit with the whole data word to be written into memory for the purpose of check-bit generation. No time is saved by not correcting the data read from memory prior to the subsequent write operation. The partial-word-write operation is virtually identical to a read cycle in correct-always mode or a read cycle with an error detected. Consequently, a partial word write is usually done in a "correct always" mode.

Operating System Involvement

In systems capable of doing partial-word-write operations, it is necessary to initialize the memory on power up. This can be done in hardware but it is usually done by the operating system. Initialization implies writing every memory location with an arbitrarily chosen constant and thereby writing the check-bit memory with the correct corresponding check-bits. The need to initialize memory results from the nature of the read-modify-write EDC cycle required by the event of a partial-word-write operation. If the memory has not been initialized, the read cycle will normally result in an error indication and an attempt to 'correct' a bit in the data field before writing back to memory. This tends to introduce errors into previously written data bytes or sub-words.

It is possible to design a state machine EDC controller that corrects all single bit errors in a fashion transparent to the CPU. This is not always desirable since it masks hard single-bit errors that indicate hardware problems. In any case, the operating system must become involved in the event of multiple errors if only to issue an appropriate error message to the system operator.

It is desirable to log single bit errors and as much information about the error as is practical. Relevant data ideally includes the syndrome bits to identify the bit location in the word, and the physical address of the error. For complete EDC transparency, such as that desired for real-time systems, error logging must be eliminated or accommodated entirely in hardware. For non real-time systems, interrupting the CPU after an error occurrence is the conventional way to log error data. Syndrome data is collected, and any other error information the system hardware retains is retrieved.

Non-obvious Hardware Topics

In a 32-bit system with a bi-directional check-bit bus or in 64-bit cascaded mode, the check-bit input-output and syndrome functions are time-multiplexed onto the same bus. If the EDC unit is in the correction mode, the input latches are open, and the OESC pins are low, the bus will tend to oscillate. This combination of control inputs would not be appropriate for normal operation but might occur in an idle period between memory cycles unless the designer specifically designs this condition out. The oscillation occurs in this condition because the EDC units are attempting to output syndrome bits based on the data and 'check-bit' inputs. However, the syndrome outputs in this state are being fed back to the check-bit inputs. The result is an oscillation on the check-bit/syndrome bus.

It is an important and sometimes overlooked fact that it is not acceptable to allow inputs on most CMOS parts to 'float'. The result of doing this is increased power consumption, on chip noise and sometimes outright oscillation which can lead to latch-up. The check-bit inputs and the data bus of an EDC unit should not be allowed to float when not being used. In low power systems in particular, all inputs not in use must be brought to logic highs or lows when not in use. This may imply not tri-stating some buffers that would otherwise be tri-stated when not actively driving, or actually including pull-up or pull-down resistors on a bus to bias it when it is not actively being driven.

Basic EDC Unit Operation

Basic 32-bit 49C460 EDC operation with timing diagrams is illustrated in Figures 5, 6, and 7. These timing diagrams are also appropriate for a 16-bit IDT39C60 system. In the IDT39C60, the LEout and the Generate functions have separate pins. In the IDT49C460, they are both controlled by one pin. It is usually convenient when using the IDT39C60 to wire the two pins together.

In the non-expanded case, with either EDC unit, use of the input latch may be convenient but is not logically dictated (i.e., the LEin pin may be tied high). Also, the correct pin may be simply left asserted in normal operation. The "detect" mode is usually only used as a diagnostic aid, which allows the data correction function to be shut off while still generating an error signal based on the input data.

Diagnostic Modes

Since the EDC function introduces a complicating layer between the system bus and the memory, diagnostic modes are provided for the EDC to provide testability for the entire memory subsystem. In memory systems where the EDC word is wider than the system bus memory, verification is complicated by the fact that all writes are partial word writes. Good diagnostic design requires forethought.

The EDC unit's internal diagnostic latches have two distinct and unrelated data fields. The check-bit data field is used to provide check data to be substituted for normal check-bits in the diagnostic modes. These will be written to memory in diagnostic generate mode, or substituted for check-bits read from memory in diagnostic-detect or correct mode. The second field in the diagnostic latch is the control field. The control field is ignored except when the part is placed in the internal control mode.

The control byte is used to control the operating features of the part when the part has been placed in internal control mode. Each bit in the control field corresponds to a pin on the part and overrides the logic sense of that pin when the part is in the internal control mode. For example, we could place the part into the correct mode by setting the correct pin on the EDC unit to a logic high, or we could put the part into the internal control mode and set the correct bit in the diagnostic latch to '1'. Thus there are always two ways to achieve any mode of operation. For example, the diagnostic modes may be entered by setting the external diagnostic inputs appropriately, or entering the internal control mode and setting the diagnostic latch bits appropriately. The internal control mode is provided as a convenience and is useful for controlling operating modes during diagnostic testing and software initialization. Conceptually, it is important to realize that anything that can be done in this mode can be done with external logic as well.

Memory System Verification Strategies

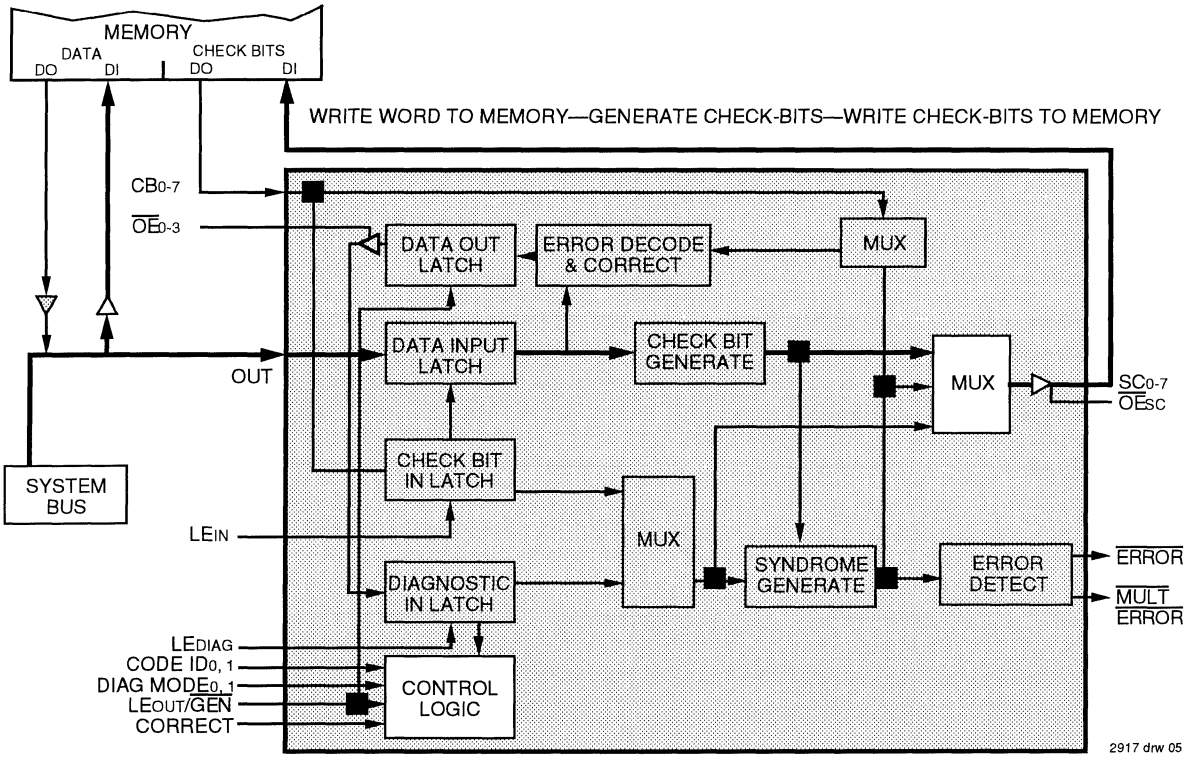
When a new design is being verified, it is critical to isolate different problem factors; this is one function of the EDC diagnostics.

To prove the function of the primary memory array, the EDC unit is placed in the pass-through mode so that it does not interact with the data stream. Once the primary memory array has been verified as functional, the check-bit memory must be verified. The diagnostic generate mode is used to write known data into the check-bit memory. Reading the check-bit memory directly through the EDC is not possible, so gross functional testing must be done via an external latch or with a logic analyzer. Using an external latch greatly facilitates check-bit memory verification.

Collecting syndrome data from error events requires that an external latch be included in the design to capture the syndrome data after an error has occurred. It should be possible to clear this latch after reading its contents from the system bus. Depending on the EDC configuration, it may be possible to use the same latch to capture check-bits from the check-bit memory. More subtle problems can be explored indirectly by interpreting correction patterns on known data or by using syndrome data to interpret failure patterns.

SUMMARY

The error detection and correction unit is located in the critical path between a CPU and the memory. The operational configuration of the EDC intimately affects the speed of the final system. Due to the wide variation between computer architectures that EDC is desirable for, the EDC unit is necessarily a generalized process. The object of this application note has been to illuminate some of the topics that any designer will encounter in the process of designing an EDC system.



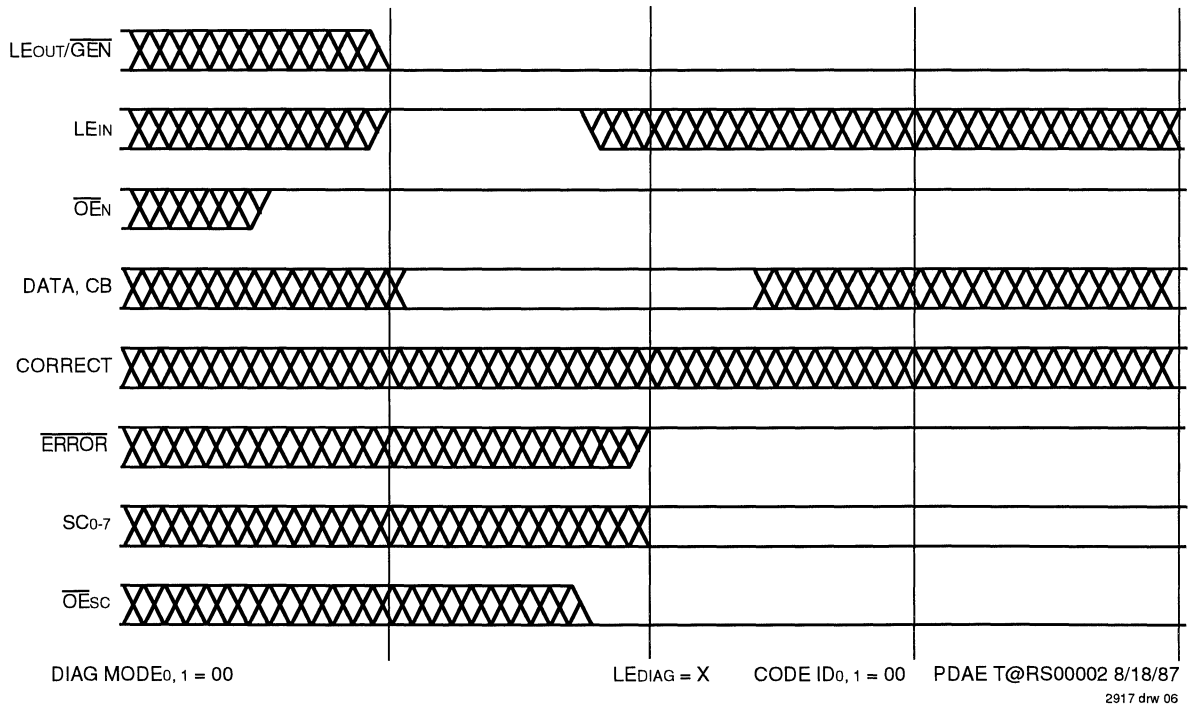


Figure 5. 32-bit full-word-width write operation (generate mode).

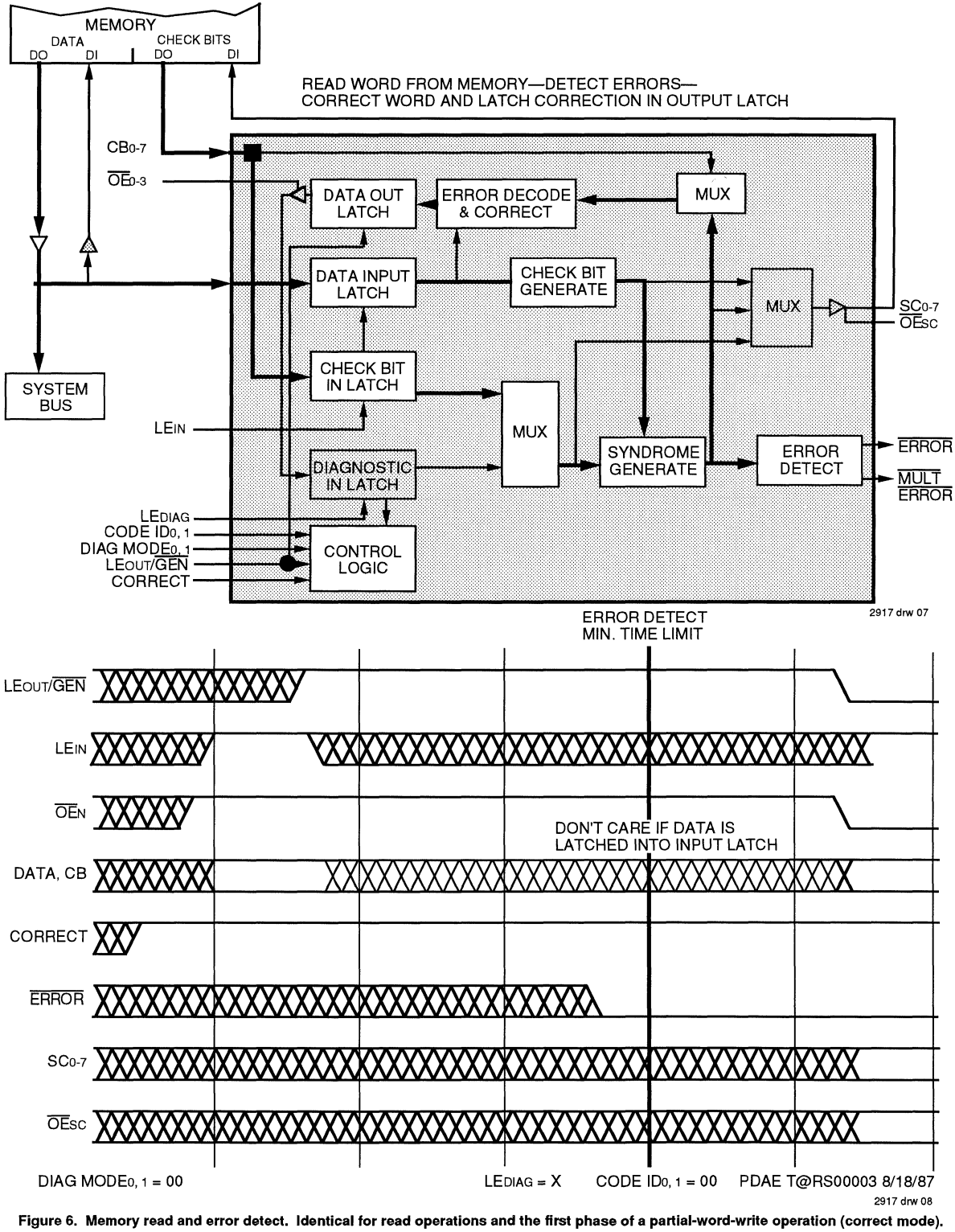
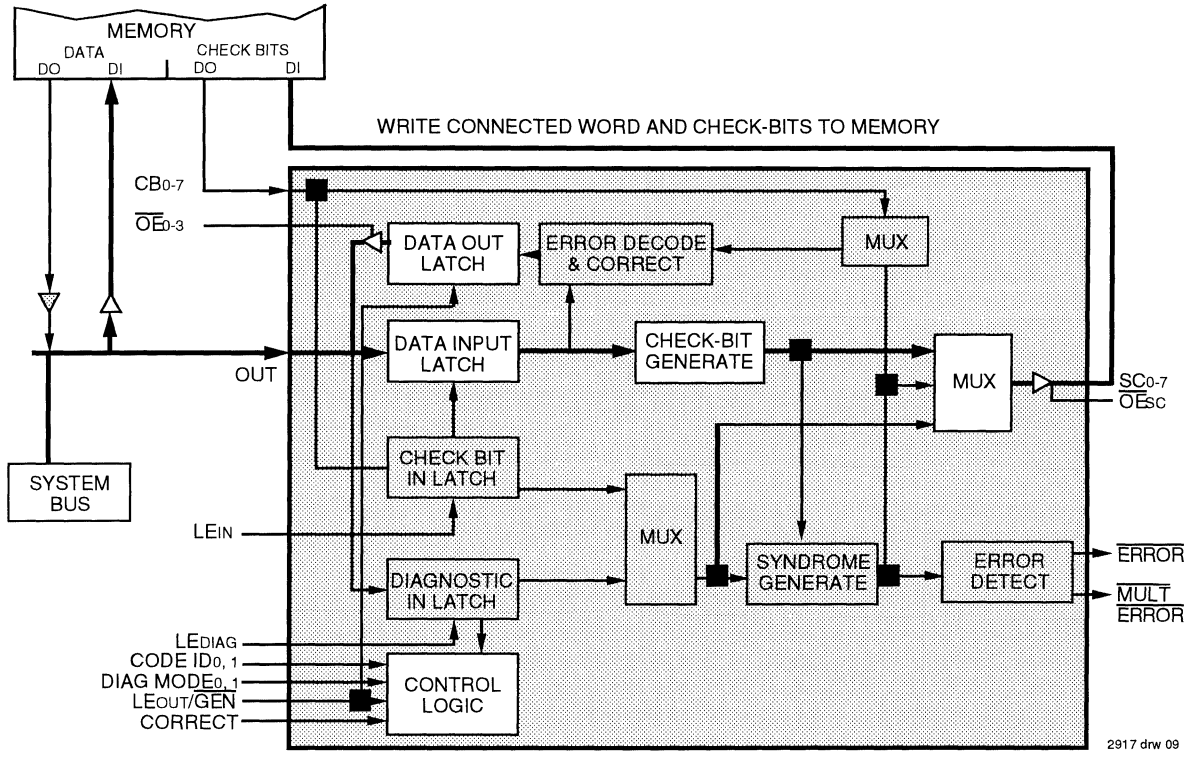


Figure 6. Memory read and error detect. Identical for read operations and the first phase of a partial-word-write operation (correct mode).



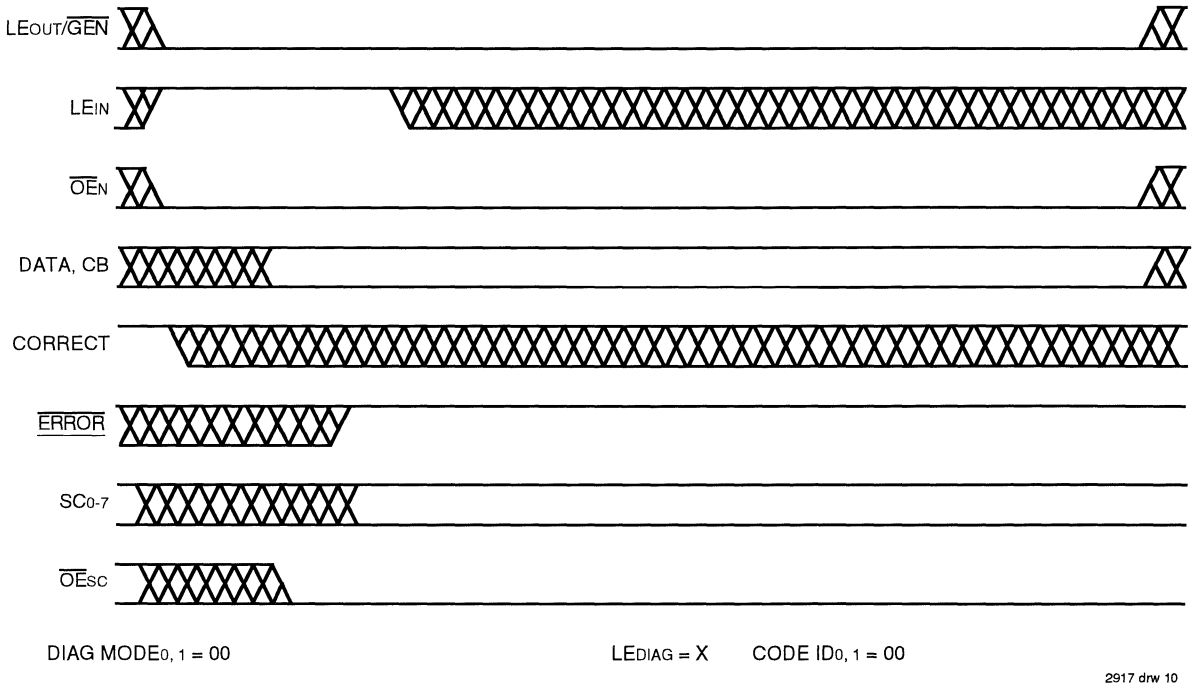


Figure 7. Memory correct and check-bit regenerate. Identical for the second phase of a read operation in which an error has occurred, and for a partial-word-write operation except for the state of the individual byte output enables.

ERROR				HEX	0	1	2	3	4	5	6	7
DECIMAL				S6	0	0	0	0	1	1	1	1
SYNDROME				S5	0	0	1	1	0	0	1	1
HEX				S4	0	1	0	1	0	1	0	1
	S3	S2	S1	S0								
0	0	0	0	0	NE	C4	C5	T	C6	T	T	30
DECIMAL EQUIVALENT>>					0	16	32	48	64	80	96	112
1	0	0	0	1	CO	T	T	14	T	M	M	T
					1	17	33	49	65	81	97	113
2	0	0	1	0	C1	T	T	M	T	2	24	T
					2	18	34	50	66	82	98	114
3	0	0	1	1	T	18	8	T	M	T	T	M
					3	19	35	51	67	83	99	115
4	0	1	0	0	C2	T	T	15	T	3	25	T
					4	20	36	52	68	84	100	116
5	0	1	0	1	T	19	9	T	M	T	T	31
					5	21	37	53	69	85	101	117
6	0	1	1	0	T	20	10	T	M	T	T	M
					6	22	38	54	70	86	102	118
7	0	1	1	1	M	T	T	M	T	4	26	T
					7	23	39	55	71	87	103	119
8	1	0	0	0	C3	T	T	M	T	5	27	T
					8	24	40	56	72	88	104	120
9	1	0	0	1	T	21	11	T	M	T	T	M
					9	25	41	57	73	89	105	121
A	1	0	1	0	T	22	12	T	1	T	T	M
					10	26	42	58	74	90	106	122
B	1	0	1	1	17	T	T	M	T	6	28	T
					11	27	43	59	75	91	107	123
C	1	1	0	0	T	23	13	T	M	T	T	M
					12	28	44	60	76	92	108	124
D	1	1	0	1	M	T	T	M	T	7	29	T
					13	29	45	61	77	93	109	125
E	1	1	1	0	16	T	T	M	T	M	M	T
					14	30	46	62	78	94	110	126
F	1	1	1	1	T	M	M	T	0	T	T	M
					15	31	47	63	79	95	111	127

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

2917 tbl 01

Table 1. 32-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

ERROR				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	NE	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
					0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
1	0	0	0	1	CO	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
					1	17	33	49	65	81	97	113	129	145	161	177	193	209	225	241
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
					2	18	34	50	66	82	98	114	130	146	162	178	194	210	226	242
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
					3	19	35	51	67	83	99	115	131	147	163	179	195	211	227	243
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
					4	20	36	52	68	84	100	116	132	148	164	180	196	212	228	244
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
					5	21	37	53	69	85	101	117	133	149	165	181	197	213	229	245
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
					6	22	38	54	70	86	102	118	134	150	166	182	198	214	230	246
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
					7	23	39	55	71	87	103	119	135	151	167	183	199	215	231	247
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
					8	24	40	56	72	88	104	120	136	152	168	184	200	216	232	248
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
					9	25	41	57	73	89	105	121	137	153	169	185	201	217	233	249
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
					10	26	42	58	74	90	106	122	138	154	170	186	202	218	234	250
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
					11	27	43	59	75	91	107	123	139	155	171	187	203	219	235	251
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
					12	28	44	60	76	92	108	124	140	156	172	188	204	220	236	252
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
					13	29	45	61	77	93	109	125	141	157	173	189	205	221	237	253
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
					14	30	46	62	78	94	110	126	142	158	174	190	206	222	238	254
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T
					15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255

NE = NO ERROR
Cn = check-bit error bit n
n = data-bit error bit n
n = decimal equivalent of the syndrome

T = Two errors
M = Multiple errors

2917 tbl 02

Table 2. 64-bit Syndrome Tables with Hex, Binary and Decimal Equivalents.

CB	DATA	CB	DATA	CB	DATA	CB	DATA
0	28	20	127	40	E	60	101
1	1000F	21	10100	41	10029	61	10126
2	1000	22	1010F	42	10026	62	10129
3	27	23	128	43	1	63	10E
4	1000C	24	10103	44	1002A	64	10125
5	2B	25	124	45	D	65	102
6	24	26	12B	46	2	66	10D
7	10003	27	1010C	47	10025	67	1012A
8	10024	28	1012B	48	1002	68	1010D
9	3	29	10C	49	25	69	12A
A	C	2A	103	4A	2A	6A	125
B	1002B	2B	10124	4B	1000D	6B	10102
C	0	2C	10F	4C	26	6C	129
D	10027	2D	10128	4D	10001	6D	1010E
E	10028	2E	10127	4E	1000E	6E	10101
F	F	2F	100	4F	29	6F	126
10	10022	30	1012D	50	10004	70	1010B
11	5	31	10A	51	23	71	12C
12	A	32	105	52	2C	72	123
13	1002D	33	10122	53	1000B	73	10104
14	6	34	109	54	20	74	12F
15	10021	35	1012E	55	10007	75	10108
16	1002E	36	10121	56	10008	76	10107
17	9	37	106	57	2F	77	120
18	2E	38	121	58	8	78	107
19	10009	39	10106	59	1002F	79	10120
1A	10006	3A	10109	5A	10020	7A	1012F
1B	21	3B	12E	5B	7	7B	108
1C	1000A	3C	10105	5C	1002C	7C	10123
1D	2D	3D	122	5D	B	7D	104
1E	22	3E	12D	5E	4	7E	10B
1F	10005	3F	1010A	5F	10023	7F	1012C

2917 tbl 03

Table 3. Minimal 32-check-bit to data tables for diagnostic use. One data value is listed to generate every possible check-bit pattern.

DATA	CB	DATA	CB	DATA	CB	DATA	CB
0	C	100	2F	10000	2	10100	21
1	43	101	60	10001	4D	10101	6E
2	46	102	65	10002	48	10102	6B
3	9	103	2A	10003	7	10103	24
4	5E	104	7D	10004	50	10104	73
5	11	105	32	10005	1F	10105	3C
6	14	106	37	10006	1A	10106	39
7	5B	107	78	10007	55	10107	76
8	58	108	7B	10008	56	10108	75
9	17	109	34	10009	19	10109	3A
A	12	10A	31	1000A	1C	1010A	3F
B	5D	10B	7E	1000B	53	1010B	70
C	A	10C	29	1000C	4	1010C	27
D	45	10D	66	1000D	4B	1010D	68
E	40	10E	63	1000E	E	1010E	6D
F	F	10F	2C	1000F	1	1010F	1F
20	54	120	77	10020	5A	10120	79
21	1B	121	38	10021	15	10121	36
22	1E	122	3D	10022	10	10122	33
23	51	123	72	10023	5F	10123	7C
24	6	124	25	10024	8	10124	2B
25	49	125	6A	10025	47	10125	64
26	4C	126	6F	10026	42	10126	61
27	3	127	20	10027	D	10127	2E
28	0	128	23	10028	E	10128	2D
29	4F	129	6C	10029	41	10129	62
2A	4A	12A	69	1002A	44	1012A	67
2B	5	12B	26	1002B	B	1012B	28
2C	52	12C	71	1002C	5C	1012C	7F
2D	1D	12D	3E	1002D	13	1012D	30
2E	18	12E	3B	1002E	16	1012E	35
2F	57	12F	74	1002F	59	1012F	7A

2917 tbl 04

Table 4. Minimal 32-bit data to check-bit tables for diagnostic use. At least one data value is listed for every possible check-bit pattern. This table is identical to Table 3 except in sequence of presentation.

Integrated Device Technology, Inc.

PROTECTING YOUR DATA WITH THE IDT49C465 32-BIT Flow-thruEDC™ UNIT

APPLICATION NOTE AN-64

by Tao Lin, Gerard Lyons and Frank Schapfel

INTRODUCTION

A TIME FOR ERROR-FREE MEMORIES

With the advent of high-performance 32-bit RISC and CISC microprocessors, general purpose computing across a wide spectrum of applications software is now easily accessible on a desktop. We can now draw on computer resources which are very sophisticated, multi-task systems with distributed processing power, and we no longer must rely on the centralized mini-computers and mainframes for processing horsepower. Both the technical and the commercial computing environments demand the insatiable hunger for processing power.

This increasing demand for sophisticated applications software requires more system memory on a local level. Tightly coupled microprocessors and cache memory are designed for optimized processing throughput, but the cache memory is no substitute for system memory. Cache memory is typically composed of very high-speed static RAMs, with access times of 35 nanoseconds or less. System or main memory is almost always comprised of slower but very high-density dynamic RAMs, typically with access times of 100 nanoseconds or more, but with four times the density of static RAMs. So, when the state-of-the-art static RAMs are 1 Megabit large, the newest density dynamic RAM is 4 Megabits. Therefore, dynamic RAMs will always provide the most cost-effective implementation for system memory.

Dynamic RAMs, though, are very prone to externally induced errors. These externally induced errors are called soft errors, since they do not cause permanent damage to the memory cell. Soft errors can be induced by system noise, alpha particle and power supply surges, and will cause random data bits to be flipped from "1" to "0", or vice versa. Although these soft error occurrences may be rare and inconsequential when using small amounts of DRAMs, large DRAM arrays are much more error prone. Also, as seen in Figure 1, larger DRAM components are much more susceptible to soft errors by virtue of their smaller memory cell size. Hardware errors may also occur on system memory boards. These hard errors occur if one RAM component or RAM cell fails and is stuck at "0" or stuck at "1". Although less frequent, hard errors may cause a complete system shut down.

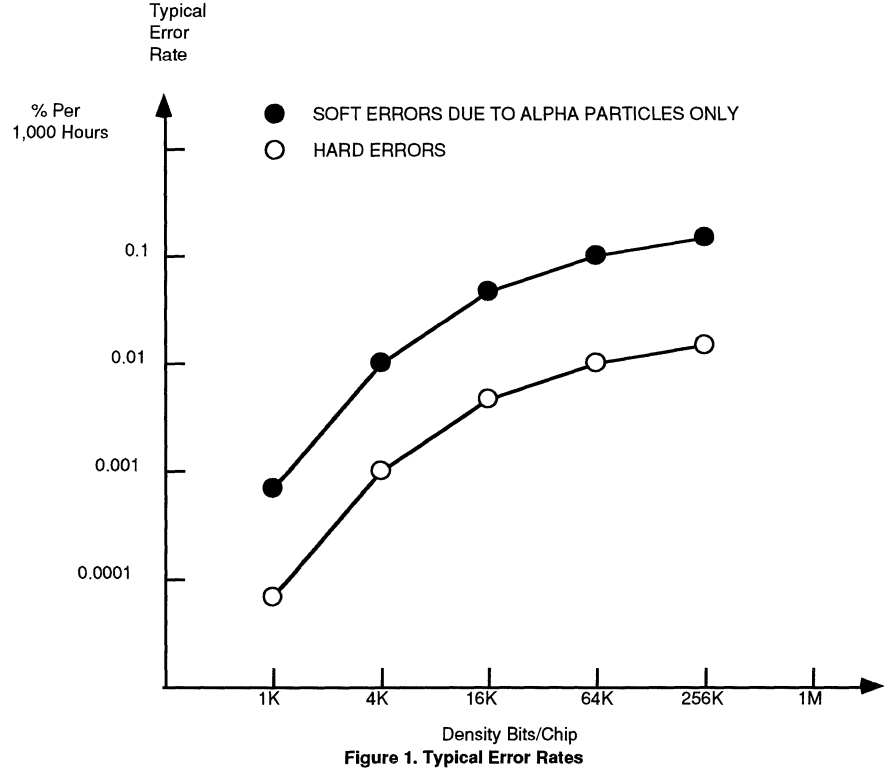


Figure 1. Typical Error Rates

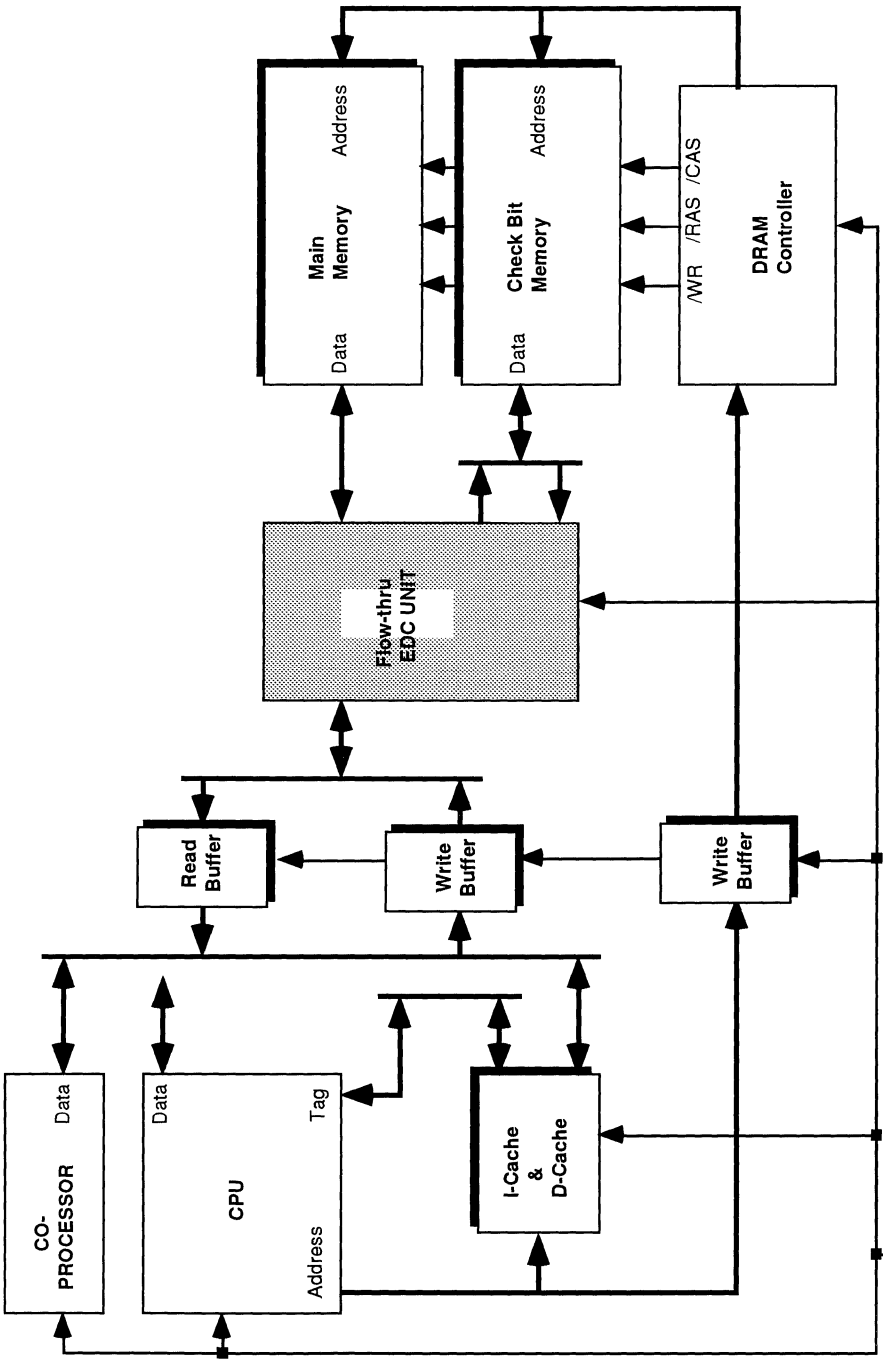


Figure 2. A Typical Architecture of High-performance RISC or CISC Systems

ERROR CORRECTION TO THE RESCUE

A scheme exists that not only is able to detect soft and hard errors, but is capable of correcting the erroneous bits. This scheme is implemented by a family of error detection and correction chips from Integrated Device Technology. Using a modified Hamming code, developed at AT&T Bell Labs, all single-bit errors may be detected and corrected, while all two-bit and most three-bit errors can be detected. IDT pioneered EDC chips, using CMOS technology in 1986, after recognizing the importance of large DRAM memory arrays in distributed computing.

TYPICAL ARCHITECTURE OF HIGH-PERFORMANCE RISC/CISC SYSTEMS

Figure 2 shows a typical architecture of high-performance RISC or CISC systems which have the following features: (1) high-speed cache memory (separate or common, Instruction-cache and Data-cache) for fast access to frequently used instructions and data, (2) write and read buffers to handle the mismatch between the high-speed CPU and the slow-speed main memory and (3) high-speed flow-thru EDC unit to insure data integrity.

While most high-performance computer systems in current market have the first and second features, the third feature is becoming more attractive and important when the main memory space grows and the memory word-length increases. Certainly, using an EDC unit is an effective way to improve the system reliability.

GENERAL EDC OPERATION

The basic function of an EDC device is to check the integrity of data being read from a memory system, flag an error if one has been detected and if possible correct that error. The IDT family of EDC devices implements this function using the same general principles, with some variations from device to device.

The operation of an EDC device can be generally split into:(1) generation of a coded word based on the data-word being written to memory. This coded word is called **The Check-Bit Word.** This operation is called **Generate;** (2) detection of errors in a data-word read from memory by comparing the corresponding check-bit word read from memory and a newly generated check-bit word (based on the data-word read from memory) and if possible correcting this error. The comparison of these two check-bit words (an exclusive-or (XOR) function) produces the so-called **Syndrome Word**. This operation is called **Detect/Correct.**

The coding scheme employed in IDT's EDC devices is a modified **Hamming Code.** For each data-word written to memory, a coded pattern, or check-bit word, is appended to the date-word. The new word (the data-word plus the check-bit word) can be termed a **valid code**. The modified Hamming Code establishes a Distance-of-4 between one valid code and another. This means that to go from one valid code to another, 4-bits have to change. It can be shown that a **Distance-of-4** code enables you to **detect all Single and Double-Bit** errors and **correct all Single-Bit** errors.

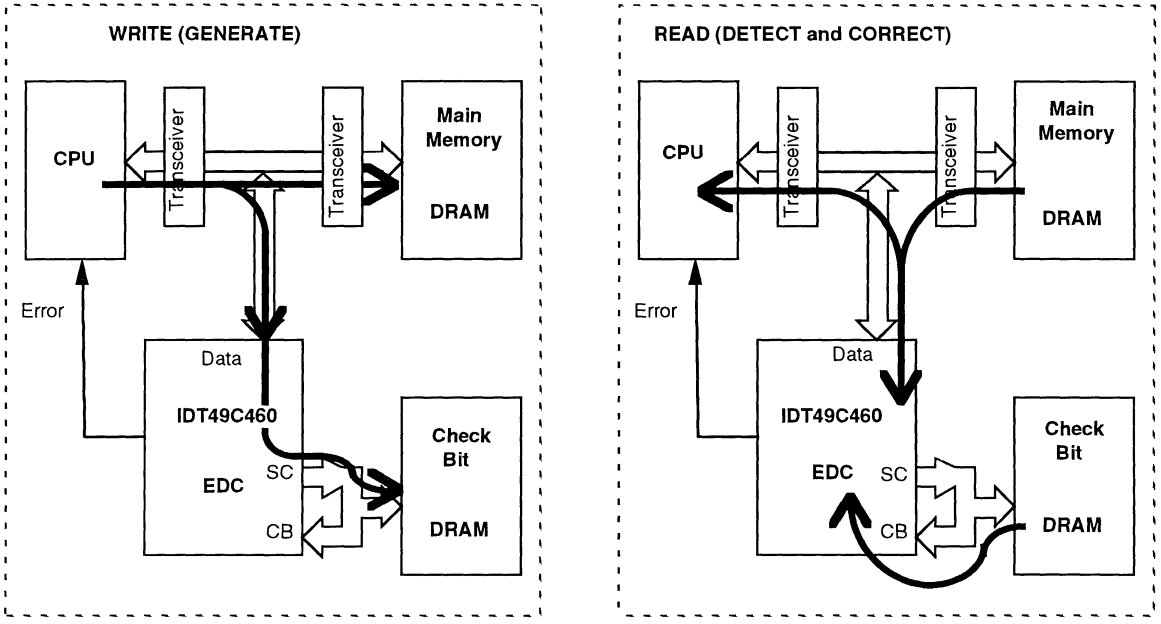
To implement a Distance-of-4 code on a 32-bit data-word, a 7-bit check-bit word must be appended. For a 64-bit word, a 8-bit check-bit word must be appended. The Hamming Code algorithm to generate a check-bit word from a 32-bit data-word or a 64-bit data-word can be found in either IDT49C460 data sheet or IDT49C465 data sheet.

EDC ARCHITECTURES AND WORD-LENGTH

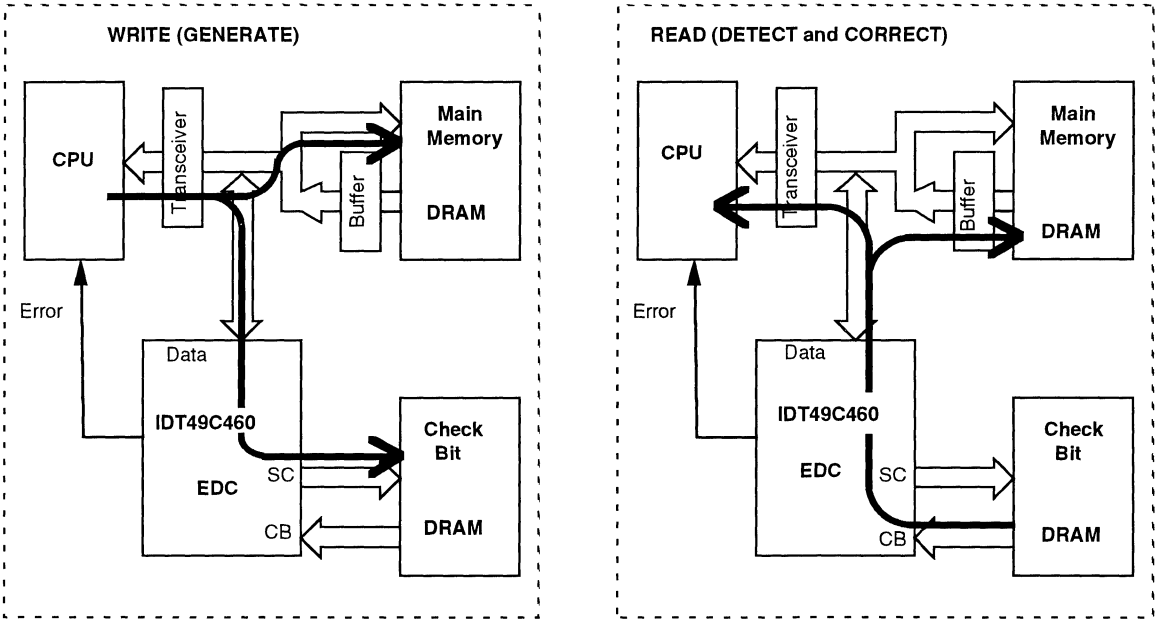
There are two basic architectures for EDC operation: flow-thru and bus-watch. IDT provides a full line of EDC devices to support 16-bit and 32-bit bus-watch architectures and 32-bit and 64-bit flow-thru architectures, as shown in Table 1.

Part Number	Architecture	Word-length	Comment
IDT39C60	Bus-watch	16-bit	Cascadable up to 64-bit using 4 devices
IDT49C460	Bus-watch	32-bit	Cascadable up to 64-bit using 2 devices
IDT49C465	Flow-thru	32-bit	Cascadable up to 64-bit using 2 devices
IDT49C466	Flow-thru	64-bit	

Table 1. IDT EDC Product Line

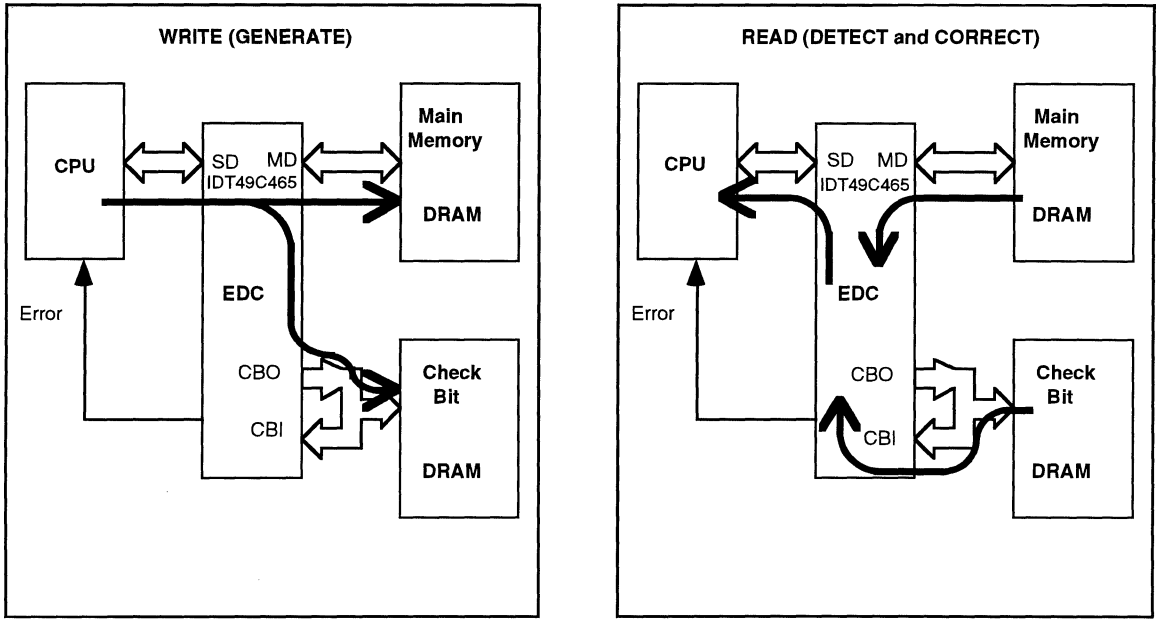


(a) Common I/O Memory System

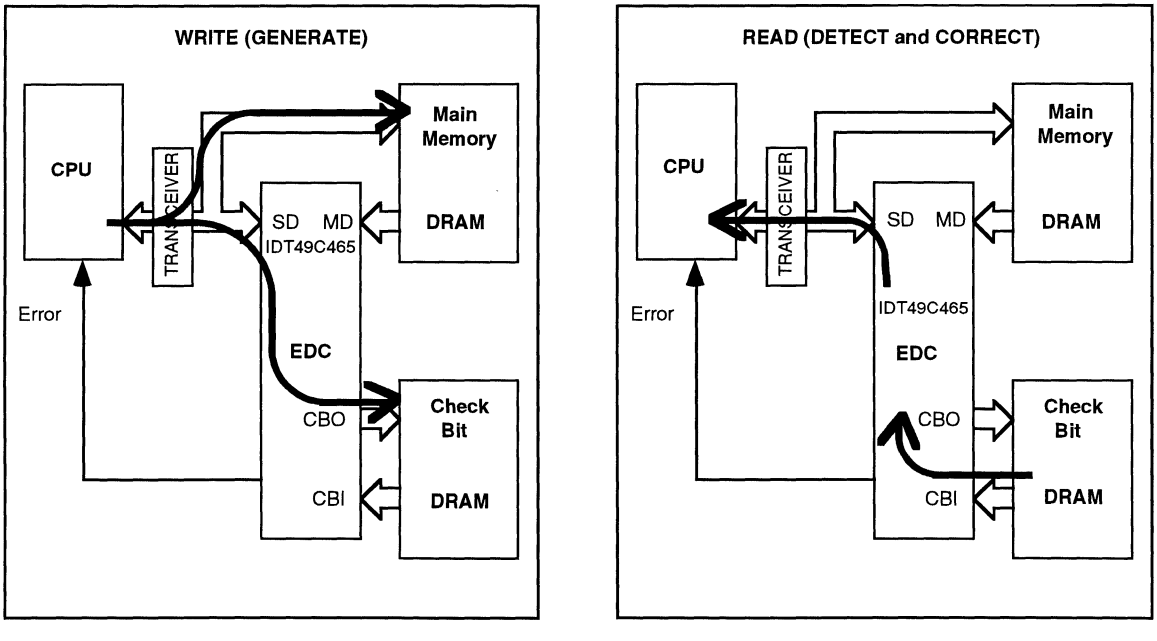


(b) Separate I/O Memory System

Figure 3. Basic Configurations Using a Bus-watch EDC Architecture

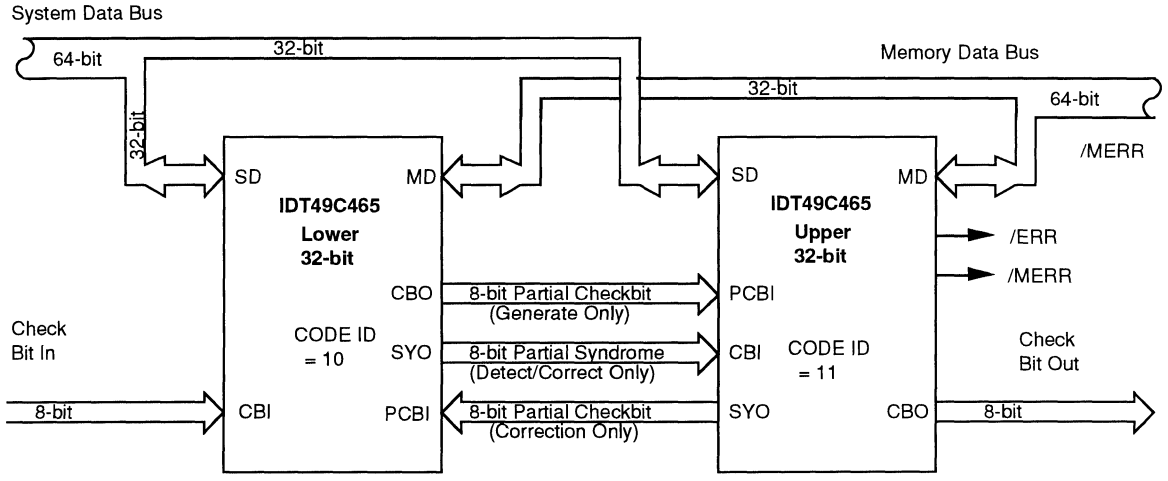


(a) Common I/O Memory System

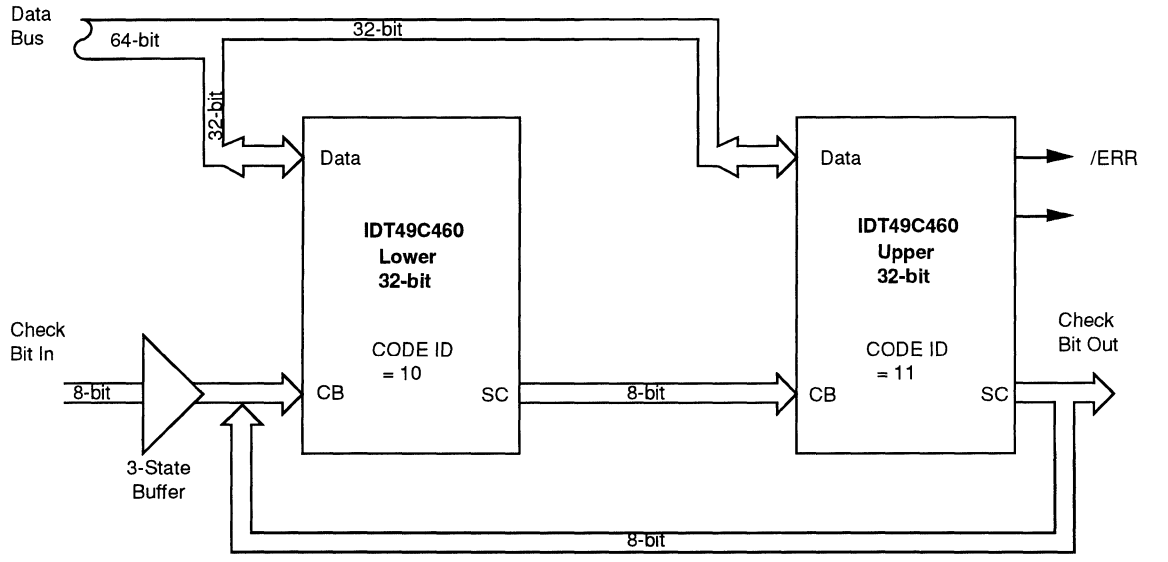


(b) Separate I/O Memory System

Figure 4. Basic Configurations Using a Flow-thru EDC Architecture



(a) Cascading Flow-thru EDC IDT49C465



(b) Cascading Bus-watch EDC IDT49C460

Figure 5. 64-bit Configurations by Cascading Two 32-bit EDC Units

BUS-WATCH ARCHITECTURE

A bus-watch EDC such as the IDT49C460 has a single data bus. The basic configurations, using the IDT49C460 for common I/O memory and separate I/O memory, are illustrated in Figure 3.

During a write (store) operation, the CPU sends data to the main memory. At the same time the data goes to the EDC unit, which then generates the check bits and stores them in the check-bit memory.

On the other hand, during a read (load) operation, the data from the main memory and the check bits from the check-bit memory first go to the EDC unit. Based on the information carried by the check bits, the EDC unit can detect all single-bit and some multiple-bit errors, and correct all single-bit errors. The corrected data is then sent to the CPU.

FLOW-THRU ARCHITECTURE

In contrast to a bus-watch EDC, a flow-thru EDC such as the IDT49C465 provides two data buses: a system data (SD) bus and a memory data (MD) bus. The dual-bus architecture improves the throughput of the EDC operation and simplifies the interface between the CPU system bus and the memory bus. The basic configurations using the IDT49C465 for common I/O memory and separate I/O memory are illustrated in Figure 4.

In the common I/O configuration, during a write (store) operation, the data from CPU flows through the EDC unit and is written to the main memory. When the data flows through the EDC, the check bits are generated and stored into the check-bit memory. During a read (load) operation, the data from the main memory enters the EDC unit through the MD bus while the check bits enter the EDC unit through the CBI bus. The EDC unit then detects any errors and loads the corrected data to the CPU through the SD bus.

In the separate I/O configuration, during a write (store) operation, the data from CPU are directly sent to the main memory. At the same time, the data is sent to the EDC unit through the SD bus. The EDC unit then generates the check bits and stores them into the check-bit memory. During a read (load) operation, the data from the main memory enters the EDC unit through the MD bus while the check bits enter the EDC unit through the CBI bus. The EDC unit then detects any errors and loads the corrected data to the CPU through the SD bus.

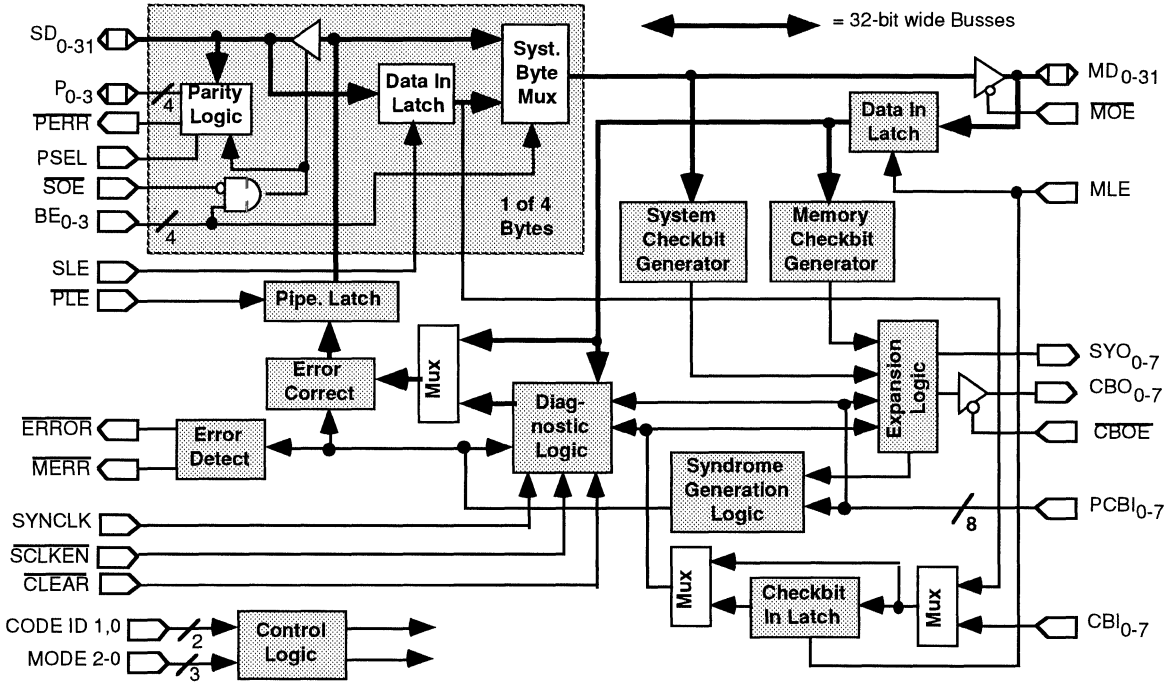


Figure 6. Block Diagram of IDT49C465

CASCADING 32-BIT EDC DEVICES FOR 64-BIT MEMORY SYSTEMS

As mentioned in the previous section, for a 32-bit data word, 7 check bits are necessary, while for a 64-bit data word, 8 check bits are needed. Although the IDT49C460 and the IDT49C465 are both 32-bit EDC units, they have an **8-bit output-bus** for output of generated check-bits to memory and an **8-bit input bus** to read back check-bit from memory. In this way, they can be cascaded to support 64-bit applications. In the 32-bit mode, only 7 bits of the check-bit input and output buses are used, while in the 64-bit mode, all 8 bits are used.

Figure 5 shows how two IDT49C465s (or two IDT49C460s) can be cascaded to build a complete 64-bit EDC unit. In the cascaded 64-bit mode, the EDC operation can be broken into two stages; a **lower 32-bit** stage and an **upper 32-bit** stage.

For the IDT49C465 (see Figure 5a), a general description of the EDC operation is discussed below.

1. Generation starts by generating a **Partially Generated Check-bit Word** in the lower slice, based on the lower 32-bit of the 64-bit data-word, and sending this to the upper slice. The upper slice combines the Partially Generated Check-bit word from the lower slice, with its generated check-bit word (based on the upper 32-bit of the 64-bit data-word), to form a final check-bit word. Thus, the source of check-bit in a cascaded system is the upper-slice device.
2. Detection/Correction starts in the **lower-slice** where the check-bits from memory are input, as well as the lower 32-bit of the 64-bit data-word. Here the inputted check-bits are compared with the newly generated check-bits (based on the lower 32-bit of DATA-word) using an XOR function to produce a **Partial Syndrome Word,** which is passed onto the upper-slice device. At the same time, in the upper slice the upper 32-bits of 64-bit data-word is used to generated a so-called **Partial Check-Bit Word** which is sent to the lower slice. So now we have in both the upper and lower slice devices almost simultaneously two pieces of data; **the Partial Syndrome Word** (generated in the lower-slice) and the **Partial Check-Bit Word** (generated in the upper-slice). In each slice these two pieces of data are XOR'd to produce a **Final Syndrome Word** which is used to detect and correct errors on the 64-bit data word.

The IDT49C460 carries out Detect/Correct slightly differently (see Figure 5b), namely, the Partial Syndrome generated in the lower-slice is sent to the upper slice, then the Final Syndrome is generated in the upper-slice and this Final-Syndrome is now fed back to the lower-slice. Thus Detect/Correct in the IDT49C460 employs a serial approach, whereas the IDT49C465 uses a faster paralleled approach. Moreover, in the IDT49C460 case, an additional tri-state buffer such as the IDT74FCT244 is needed while in the IDT49C465 case, no additional external logic is needed.

OVERVIEW OF THE IDT49C465 ARCHITECTURE

The IDT49C465 architecture is an evolutionary development on the IDT49C460 EDC device. The IDT49C460 is a single-bus 32-bit EDC cascadable to 64-bits. The IDT49C465 draws on this basic architecture to provide a dual-bus or flow-Thru 32-bit EDC cascadable to 64-bits. Figure 6 shows a block diagram of the IDT49C465; the key difference between the IDT49C460 and the IDT49C465 is the presence of a second 32-bit DATA bus to provide the flow-thru path for data through the device.

DATA BUSES

The System Data Bus, or **SD Bus,** is a 32-bit bi-directional bus. Data is written to the EDC using this bus for **Check-Bit Generation,** so that when a data-word is written to memory the corresponding check-bits are written simultaneously. Also when a data-word read from memory is corrected, the corrected data-word is read from the SD Bus by the system processor. The SD Bus has associated with parity-checking and generation and also separate byte enables on the SD Bus' output buffers so that Partial Byte operations can be supported.

The Memory Data Bus, or **MD Bus,** is a 32-bit bi-directional bus. Data written from the system processor through the SD Bus can be written to memory using this bus. When the processor is reading a word from memory, the data word is read in through the MD Bus and the corrected data word (depending on the status of the data) is sent to the processor through the SD Bus.

EXPANSION BUSES

The IDT49C465 has four 8-bit buses that are an integral part in the Detect/Correct path for both a 32-bit EDC system and a 64-bit EDC system.

CBI(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system or is the lower 32-bit slice in a 64-bit EDC system, this 8-bit bus is the input port for Check-Bits read from Memory.
2. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the input port for partial Syndromes from the lower slice.

PCBI(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system, this bus is unused .
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this 8-bit bus is the input port for Partial Check-Bits read from the upper slice.
3. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the input port for Partially Generated Check-Bits from the lower slice.

CBO(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system or is the upper 32-bit slice in a 64-bit EDC system, this 8-bit bus is the output port for Check-Bits being written to Memory
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this bus is the output port for Partially Generated Check-bits being sent to the upper slice.

SYO(7:0)

1. When the IDT49C465 is operating as a 32-bit EDC system, this 8-bit bus outputs the Final Syndrome word associated with the Detect/Correct logic.
2. When the IDT49C465 is operating as the lower 32-bit slice in a 64-bit EDC system, this bus is the output port for Partial Syndrome word being sent to the upper slice.
3. When the IDT49C465 is operating as the upper 32-bit slice in a 64-bit EDC system, this bus is the output port for Partial Check-bit word being sent to the lower slice.

Operating Modes

The IDT49C465 has 3 mode control pins, MODEID(2:0), which enable the user to select which mode the part is operating in. These modes are summarized in Table 2.

	MODE DESCRIPTION
000	ERROR DATE MODE
X01	DIAGNOSTIC OUTPUT MODE
X10	GENERATE-DETECT MODE
100	CHECK-BIT INJECTION MODE
X11	NORMAL OPERATING MODE

Table 2. IDT49C465 Operating Modes

ERROR DATA MODE (000) :

In this mode the contents of the Error-Data Register are output uncorrected on the SD Bus. The Error-Data Register is a 32-bit register which gets latched under the following conditions: 1. an error condition has been detected by the EDC-$\overline{\text{ERROR}}$) and is asserted low, 2. the on-chip 4-bit Error-Counter reads zero 0000 (i.e. no error has occurred since the last clear operation), 3. the input signal, $\overline{\text{SCLKEN}}$), is held low so that the diagnostic clock, SYNCLK, is enabled, 4. the diagnostic clock, SYNCLK, undergoes a LOW-to-HIGH transition.

Data is latched into the Error-Data Register from the output of the Memory Data Latch when and only when these conditions are met. Thus, the Error Data Register contains the Memory Data word corresponding to the first error since a clear operation (assuming SYNCLK has been run continuously). If the Error Data Register has just been cleared, then output of the contents of this register will provide a source of zero-data if that is required.

DIAGNOSTIC OUTPUT MODE (X01) :

In this mode a 32-bit Diagnostic Word is output on the SD Bus. The structure of this word is outlined in Figure 7.

BITS 0:7 The output of the check-bit multiplexer is output directly on the SD Bus at these positions (LSB at bit 0 and MSB at bit 7).

BIT 8:15 Whatever is being forced on the PCBI(7:0) input pins is output on the SD Bus at these positions (LSB at bit 8 MSB at bit 15).

BIT16:23 The contents of the Syndrome Register, which is an 8-bit register within the Diagnostic Unit, is output on the SD Bus at these positions (LSB at bit 16, MSB at bit 23). The Syndrome Register gets latched at the same time as the Error Data Register and contains the Final Syndrome corresponding to the first error to occur since a clear operation.

BIT 24:27 The contents of the on-chip 4-bit Error-Counter are output on the SD Bus at these positions (LSB at bit 23 and MSB at bit 27). The Error-Counter which gets clocked under the following conditions: 1. An error condition has been detected by the EDC, i.e. xto(ERROR) is asserted low, 2. the on-chip 4-bit Error Counter does not read 1111 (or F HEX), therefore, not more than 16 errors have occurred since the last clear operation, 3. the input signal, xto(SCLKEN), is held low so that the diagnostic clock, SYNCLK is enabled and 4. the diagnostic clock, SYNCLK, undergoes a LOW-to-HIGH transition.

The Error Counter will tell the number of errors that have occurred since the last clear operation.

BIT28:29 Reserved

BIT30:31 The contents of the Error Signal Register, which is a 2-bit register is output on the SD Bus at these positions (SB at bit 30 and MSB at bit 31). Bit 0 and bit 1 of the register are set if a Multiple Error has been flagged and bit 1 only is set if a Single Error has been flagged at the same time and under the same conditions as the Error Data and Syndrome Registers are latched.

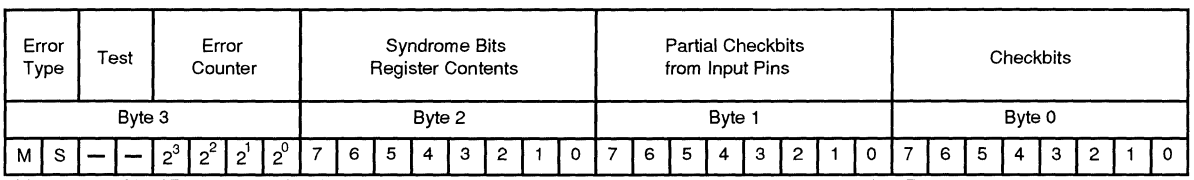


Figure 7. Output Syndrome/Diagnostic Word

GENERATE-DETECT MODE (X10) :

In this mode, detection and generation take place but no correction. Data whether correct or not, passes thru the device from the MD Bus to the SD Bus.

NORMAL OPERATING MODE (X11) :

This is the mode where normal detection/correction and generation takes place for a single-slice device (32-bit EDC system) or for the upper and lower slices in a cascaded 64-bit EDC system.

CHECK-BIT INJECTION MODE (100) :

In this mode the check-bit multiplexer enables bits 0:7 from the output of the System Data Latch to be fed into the EDC as a check-bit input, normal correction is activated. This is a very useful capability for carrying out a diagnostic check on the detect/correct path of the EDC.

PARITY FOR THE SYSTEM BUS

The IDT49C465 supports byte parity on the SD Bus, with the polarity of the parity (even or odd) selectable using the input pin PSEL. If PSEL is low, then parity (both checking and generation) will be even. If SPSEL is high, then parity will be odd. The part has 4 parity I/O lines one for each byte of the SD Bus and a parity error signal, $\overline{PERR}$), which flags a parity error on in-coming data by being asserted low.

PARTIAL BYTE WRITE AND READ-MODIFY-WRITE CAPABILITY

The IDT49C465 supports, through a number of features, **Partial Byte Writes** and **Read-Modify-Writes** cycles. Firstly the SD Bus has 4 Byte Enable signals associated with it, **BE(3:0),** these input lines provide, in conjunction with $\overline{SOE}$), separate output enable control on each byte of SD bus data. The BE bus is also the control input to the Sys-Byte-Mux, this mux enables mixing on a byte-by-byte basis of data from the SD latch (A input to mux) and from the Pipe-Line latch (B input to mux). So, for example, if the processor wanted to do a Partial Write or Partial Store of a byte (byte position 3) to a memory location byte position 3 the following sequence would occur: (1) read the memory location in question through the MD Bus and correct if possible or necessary. The corrected data-word will be latched into the Pipe-Line latch, (2) the byte to be written is latched into the SD Latch at byte position 3, all other byte are undetermined, (3) Now we have both pieces of data necessary to construct the 32-bit word to be written to memory and (4) BE(3) is held low and all other BEs are held high. Thus the output of the Sys-byte-Mux is the correctly constructed 32-bit word which is then written to memory through the MD Bus with it's corresponding check-bits.

64-BIT GENERATE

A very useful and ultimately cost-saving measure associated with the IDT49C465, is its 64-bit generate mode. If the CODE ID of the IDT49C465 is set at 01, the part is configured as a single-slice 64-bit generate EDC. While operating in this mode, the lower 32-bit of the 64-bit data word is input on the MD bus pins and the upper 32-bit of the 64-bit data word is input on the SD bus. The 8-bit generated check bits are output on the CBO bus. In 64-bit generate mode, the EDC is dedicated to check-bit generation, all other features are disabled.

Because the 64-bit generate is executed in a single slice, very fast generate speed can be achieved (15ns as opposed to 30ns in a two-slice 64-bit cascaded system). This feature can also help reduce part count. In 64-bit memory systems, it is common to use 4 32-bit EDC devices; 2 for detect/correct and 2 for generate. With the 64-bit generate capability, this part count is reduced from four to three.

WHY FLOW-THRU EDC

To fully understand the advantages of the IDT49C465 flow-thru EDC over the IDT49C460 bus-watch EDC, it is necessary to first know the architectural differences between the IDT49C465 and the IDT49C460. Figure 8 compares the simplified internal architectures of the two chips. As compared with the IDT49C460, the IDT49C465 has the following unique features:

- Dual data buses
- Dual check-bit generators: one for SD Bus and the other for MD bus
- Independent check-bit generation path
- Independent error detection/correction path
- Dedicated syndrome output
- Dedicated check-bit output
- Output pipeline latch
- Parity check/generation

These features greatly simplify the interface of the EDC unit with the system data bus and the memory data bus, and thus can considerably improve the system performance. Generally speaking, in a single bus EDC architecture like the IDT49C460, the data bus connects to both the processor and the memory system. Thus, in a normal correction cycle, data is read into the EDC from memory through the data bus, and the data is corrected. Then, the data bus is enabled as an output and the corrected data is sent to the processor. Therefore, during a correction cycle, the data bus must be turned around from being an input to being an output. Consequently, a single bus architecture has inherent delays associated with the enable/disable times of the data bus output buffer. On the other hand, separate data buses, as in the IDT49C465, allow us to dedicate buses to a specific direction of data flow and, as such, is a superior architecture.

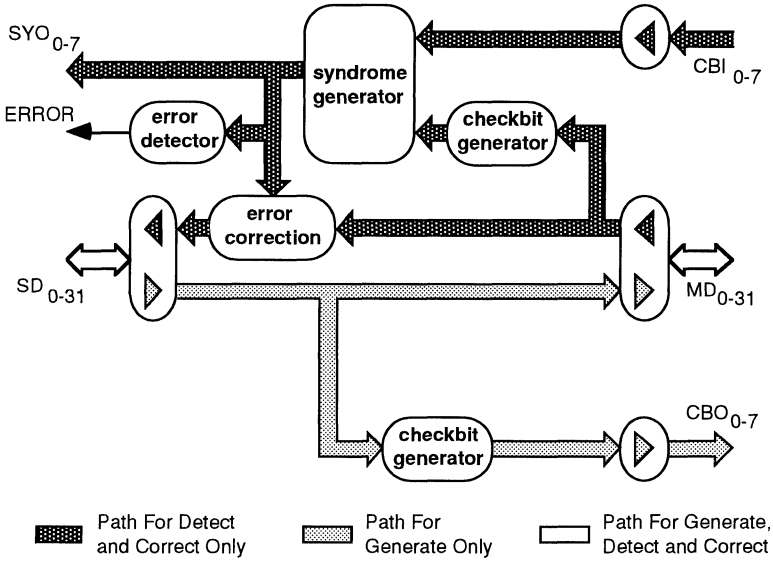
In a 32-bit system using common I/O memory, the dual bus architecture of the IDT49C465 allows direct interface of the flow-thru EDC unit with the system data bus and the memory data bus, as shown in Figure 4a. On the other hand, if the IDT49C460 is used, then two sets of transceivers are needed to buffer both system data bus and memory data bus to the single data bus of the IDT49C460, as shown in Figure 3a.

Similarly, in a 32-bit system using separate I/O memory, the dual bus architecture of the IDT49C465 allows direct interface of the flow-thru EDC unit with the memory data bus. Only a single set of transceivers is used to connect the CPU

system data bus to the EDC unit, as shown in Figure 4b. On the other hand, if the IDT49C460 is used, then a set of transceivers and a set of buffers are needed to hook up both system data bus and memory data bus with the single data bus of the IDT49C460.

In particular, the multi-bus architecture and the independent error generation and detection/correction paths of the IDT49C465 provide significant performance improvement in a 64-bit system using two cascaded EDC units. Figure 9 shows the internal data paths of cascaded IDT49C465s and cascaded IDT49C460s during a read (error detect/correct) operation. In the IDT49C465 case, the entire error detect/correct path can be divided into two steps. In the first step, the lower 32-bit unit generates the partial check bits from the lower 32-bit data, and then compares the partial check bits with the original check bits to generate the partial syndrome bits. At the same time, the upper 32-bit unit generates the partial check bits from the upper 32-bit data. Then, the partial syndrome bits from the lower unit and the partial check bits from the upper unit are exchanged between the two units. In the second step, both lower and upper units generate the final syndrome bits independently and then correct errors in the lower 32-bit data and the upper 32-bit data, respectively, in parallel. Therefore, the total delay time is the sum of MD-to-SYO plus CBI-to-SD. On the other hand, in the IDT49C460 case, the entire error detect/correct path can be divided into three steps. In the first step, like in the IDT49C465 case, the lower 32-bit unit generates the partial check bits from the lower 32-bit data, and then compares the partial check bits with the original check bits to generate the partial syndrome bits. At the same time, the upper 32-bit unit generates the partial check bits from the upper 32-bit data. However, in contrast to the IDT49C465 case, only the partial syndrome bits from the lower unit are sent to the upper unit. In the second step, the upper unit compares the partial check bits from the upper 32-bit data with the partial syndrome bits from the lower unit to generate the final syndrome bits. Then, the final syndrome bits are sent back to the lower unit. Finally, in the third step, the lower unit and the upper unit correct the errors in the lower 32-bit data and the upper 32-bit data, respectively. Consequently, the total delay time is the sum of DATA-to-SC plus BC-to-SC plus CB-to-DATA, which is much longer than the delay in the IDT49C465 case. Moreover, since the IDT49C460 has only one check bit input bus, an external octal tri-state buffer is needed to multiplex the original check bits and the partial check bits.

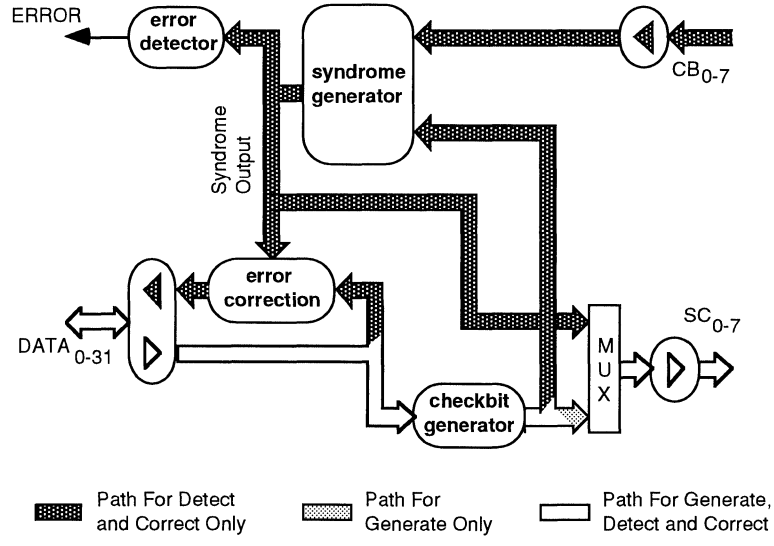
Based on the above discussion, Table 3 summarizes the performance comparison between the IDT49C465 and the IDT49C460D, the fastest version of the IDT49C460. It can be seen that in most situations, the IDT49C465 has significant speed advantage over the IDT49C460.



Features Of IDT49C465

- Dual Data Bus Architecture
- Dual CheckBit(CB) Generators
- Independent CB Generate Path
- Independent Error Detect/Correct Path
- Dedicated Syndrome Output
- Dedicated CB Output
- Output Pipeline Latch
- Parity Check/Generate
- 1 Off-chip Feedback for 64-bit Error Correct
- 144-pin PGA

(a) Simplified Block Diagram of IDT49C465 EDC Unit

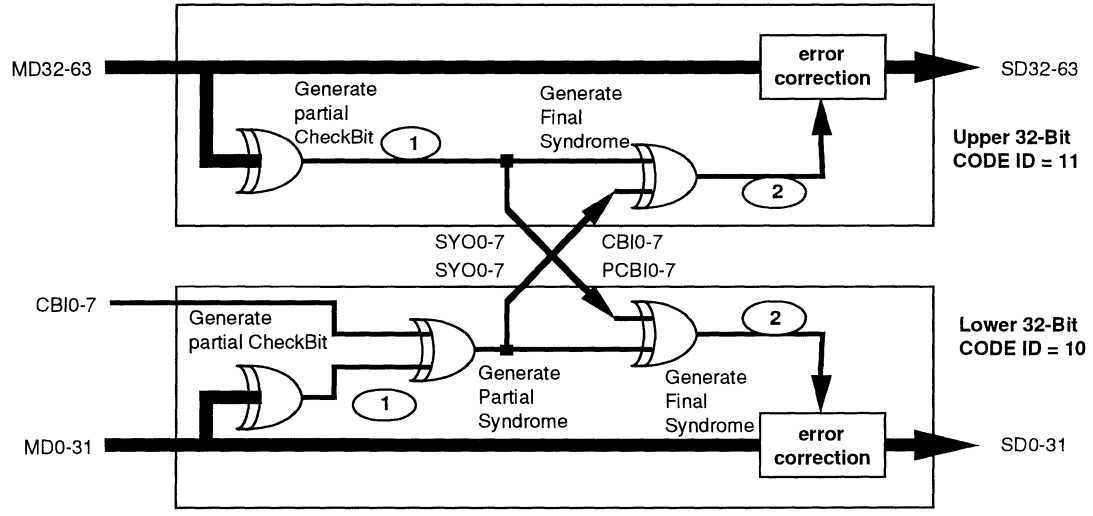


Features Of IDT49C460

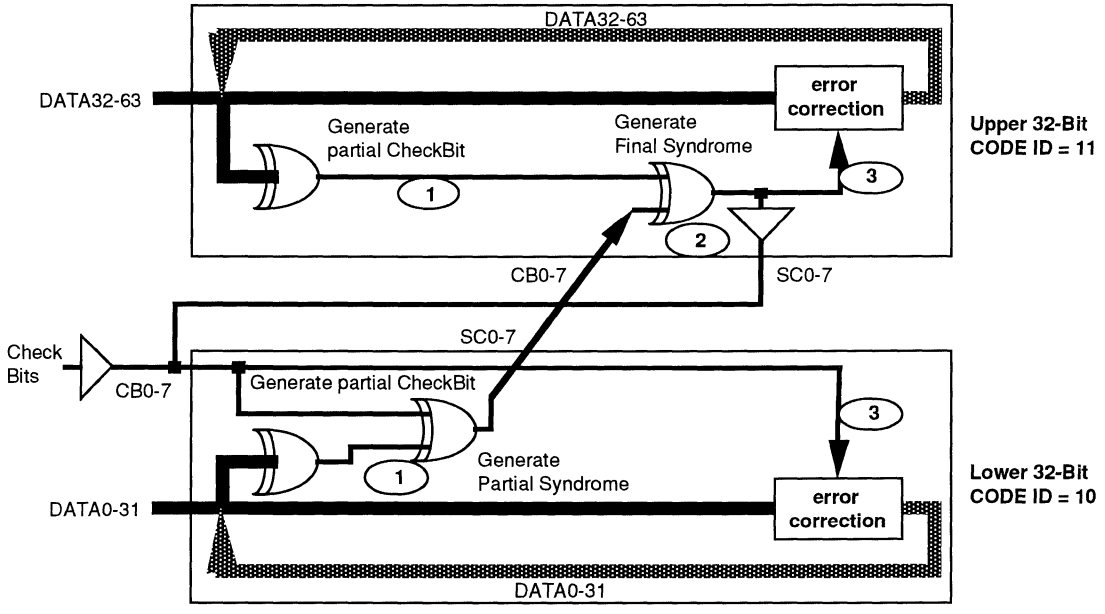
- Single Data Bus Architecture
- Single Checkbit Generator
- Shared Syndrome and CB Output
- 2 off-chip Feedback for 64-bit Error Correct
- 68-pin PGA

(b) Simplified Block Diagram of IDT49C460 EDC Unit

Figure 8. Internal Architecture Differences Between IDT49C465 and IDT49C460



(a) 64-bit Error Detect/Correct Path of Cascading IDT49C465



(b) 64-bit Error Detect/Correct Path of Cascading IDT49C460

Figure 9. Comparison of 64-bit Error Detect/Correct Path Between IDT49C465 and IDT49C460

	Common I/O				Separate I/O			
	32-bit		64-bit Cascade		32-bit		64-bit Cascade	
	Read [1]	Write	Read [1]	Write	Read [1]	Write	Read [1]	Write
IDT49C 465	MD->SD 20ns 20ns *40% Faster*	SD->CBO 15ns 15ns *26% Faster*	MD->SYO 15ns CBI->SD 20ns 35ns *34% Faster*	SD->CBO 15ns PCBI->CBO 15ns 30ns	MD->SD 20ns FCT245 [2] 5ns 25ns *12% Faster*	FCT245 [2] 5ns SD->CBO 15ns 20ns	MD->SYO 15ns CBI->SD 20ns FCT245 [2] 5ns 40ns *18% Faster*	FCT245 [2] 5ns SD->CBO 15ns PCBI->CBO 15ns 35ns
IDT49C 460D	28ns FCT245 [2] 5ns D->D 18ns FCT245 [2] 5ns	19ns FCT245 [2] 5ns D->SC 14ns	47ns FCT245 [2] 5ns D->SC 14ns CB->SC 11ns CB->D 12ns FCT245 [2] 5ns	30ns FCT245 [2] 5ns D->SC 14ns CB->SC 11ns	28ns FCT245 [2] 5ns D->D 18ns FCT245 [2] 5ns	19ns FCT245 [2] 5ns D->SC 14ns	47ns FCT245 [2] 5ns D->SC 14ns CB->SC 11ns CB->D 12ns FCT245 [2] 5ns	30ns FCT245 [2] 5ns D->SC 14ns CB->SC 11ns

NOTES:
1. The EDC units perform correction always.
2. FCT245 is high-speed bidirectional transceiver.

Table 3. Performance Comparison

CONCLUSIONS

Whether designing a correct always (flow-thru) EDC or bus-watch EDC memory systems, IDT offers a high performance solution for keeping memories error free. The key system benefit for using EDC is the continuous system operation, even with hard or soft errors occur. The key benefit for using a flow-thru EDC is the reduced memory design time when performing the correct always function, and improved performance for 64-bit memory systems.

Integrated Device Technology, Inc.

ERROR DETECTION AND CORRECTION WITH IDT49C466

APPLICATION NOTE AN-94

By Anupama Hegde

INTRODUCTION

It is widely accepted that system failures and down time claim a heavy toll in terms of cost and performance. When a system crashes, unrecoverable data may be lost. Even in the best case, the user suffers a great deal of inconvenience. Erroneous data or loss of data integrity is a major cause of system failure. Hence system designers are constantly trying to minimize the occurrence of errors in their systems.

Data errors commonly occur in storage devices such as RAM, disks and magnetic tapes. Hence error handling schemes are commonly aimed at protecting the data in these devices. Dynamic memory is, in particular, highly susceptible to errors. As we move towards systems with larger memories, data protection schemes become increasingly relevant because the error rate is found to increase with the memory size. Till recently parity has been the traditional method of data protection. Parity, however, has several drawbacks: it masks out even bit errors, it cannot locate the bit in error and beyond a certain buswidth it can become inefficient. These factors have lead to the development of a new breed of devices for data protection. Error Detection and Correction circuits (EDCs or EDACs) are today's response to the growing need for greater data reliability.They afford a greater level of protection than that offered by parity, by using a higher order error correction code (Modified Hamming code).

Implementing error detection & correction in a system involves not just the hardware to perform the error checking but also extra memory for storage of "checkbits", which are the basis of error detection and correction. An EDC may add some overhead to a system in terms of speed and cost. This is, however, compensated by a significant improvement in system performance. The following Figures underline this point:

Given a 4M x 64 DRAM memory with an FIT(Failure in time) specification of 252[1]:

MTBF (mean time between failures) without EDC = 1.76 years
MTBF with single-bit error correcting 64-bit EDC = 3935.4 years

The Figures given here are merely a guideline for comparison of the two cases and will depend entirely on the DRAM used and the memory configuration.

Thus EDC can be looked upon as a sophisticated parity system with the capacity to correct. Two primary functions are performed by an EDC unit within the framework of the memory read and write cycles - during a memory read, errors are detected and/or corrected and during a memory write, checkbits are generated.

NOTE: See appendix for further details on calculation of MTBFs.

ERROR DETECTION AND CORRECTION WITH THE 49C466

Choosing the Right EDC

EDC considerably upgrades reliability but, as mentioned earlier, there is a certain amount of overhead associated with implementing EDC. This is because of the checkbit memory required and the nanoseconds it adds to the main memory cycle times. The checkbit overhead can be minimized by increasing the size of the data word used to generate the checkbits. The table below illustrates this point and shows how parity compares with EDC for various data word sizes.

Assuming a distance-of 4 Hamming code for the EDC and byte parity:

As an example, consider a 32-bit EDC and a 64-bit EDC. We see from the table above, the former requires 7 checkbits for each 32-bit data word. Hence every 64 bits of data requires 7+7=14 checkbits in memory. A 64-bit EDC on the other hand requires only 8 checkbits to provide single bit error correction and dual bit error detection. Thus, as far as checkbit efficiency goes, a 64-bit EDC is better than a 32-bit EDC. One other advantage of a wider EDC is that less checkbit memory implies a lower error rate in checkbit memory. Going after even wider EDCs seems tempting in this light, but a compromise has to be made because of two factors.

DATA WORD SIZE	PARITY BITS REQUIRED	EDC CHECKBITS REQUIRED
16	2	6
32	4	7
64	8	8
128	16	9

2596 tbl 01

Prevalent system bus widths impose a practical limitation on how wide a bus can get. It is fairly common nowadays, however, to see a 64-bit memory bus and hence a 64-bit EDC is often easily accomodated. An EDC that is wider than the memory bus needs additional control and logic circuitry to integrate the EDC with the memory system. The greater this difference in (EDC and memory) bus widths, the more complex is this interface. Also, the error handling capacity effectively decreases as the EDC bus gets wider because the same level of protection (1 bit correction,2 bit detection) is provided for a wider word. Two 32-bit EDCs provide this for each 32-bit word, which allows correction of some 2-bit errors and detection of some 4-bit errors for each 64-bit word. Thus, constraints for a given system determine the optimum trade-off.

49C466 Operation and Features

By the nature of its function, the EDC is concerned with data transfers between the processor and memory. The IDT 49C466 has a flowthrough architecture which permits transparent data flow through the EDC. The 49C466 also increases checkbit efficiency by providing two 64-bit wide bidirectional data buses.

The error detection & correction operation in the 49C466 is similar to previous generation IDT devices. A modified Hamming code is used to generate the checkbits and the syndrome decoding is identical to cascaded mode operation in the 32-bit EDC, the 49C465. The modified Hamming code used allows for flagging of all single , dual and three bit errors in the 64-bit data word. Some three bit errors alias as single bit errors, however, and may hence be wrongly decoded by the syndrome decoding logic (MERR* may not be asserted). The code allows for correction of all single bit errors in the data word.

The 49C466 has five modes of operation. In the *normal* mode, two kinds of operations are performed. During a "memory write", checkbits are generated based on the data that is written and during a "memory read" single-bit errors in the data are corrected. In the *detect-only* mode, the "memory write" operation remains the same but during a "memory read" any errors detected are flagged by $\overline{ERR}$ and $\overline{MERR}$ pins. The data is passed though unaltered. The other three modes are useful for testing & diagnostic purposes. The EDC mode of operation is set by the user by loading the mode register through the system data bus.

Read and write paths are independent of each other in the 49C466. In fact, the device has alternate paths for each of these (read and write cycles). One path includes the 8/16-deep data buffer while the other provides a latch in place of this buffer. WBSEL(Write Buffer Select) and RBSEL(Read Buffer Select) pins select the output of either the buffer or the latch (for example - RBSEL=high selects output from the Read Buffer rather than the MD_OUT latch, WBSEL = 0 selects the output of the SD_IN latch rather than the Write Buffer).

Memory Write

During a memory write, the EDC generates checkbits corresponding to the data being written to memory (data flow from SD bus to MD bus). These are output onto the CBSYN bus and written to checkbit memory. This is a necessary part of EDC operation. Unless all checkbits corresponding to the data in memory have been generated and stored in checkbit memory, no error checking is possible.

To prevent contention on the SD bus, the SD output buffer must be disabled, during a memory write. The MD and checkbit output buffers must be enabled to pass data and checkbits to memory.

There are several ways that the "write path" can be configured but the maximum "write time" with input and output latches transparent is 15ns.

Figure 2 illustrates the data path during a write operation. The alternate write path, where the data is buffered, is shown in Figure 3 .

Memory Read

A memory read involves checking data from memory for errors. Given below is a description of what actually takes place during a "read cycle".

Data and checkbits from main memory are fed to the EDC. Checkbits corresponding to the read data are generated within the EDC. The two sets of checkbits are internally compared to produce the syndrome word. The EDC then decodes the syndrome word to check for errors.

The syndrome is also clocked into the syndrome register on the rising edge of SYNCLK. The syndrome register contents can be output on the CBSYN bus. The CBSEL pin controls the output of the CBSYN bus. While CBSEL is low, checkbits generated during a write are output. When CBSEL is high, syndrome generated during a read are output. Figure 4 shows the data path during a normal read operation.

A buffered read operation is illustrated in Figure 5.

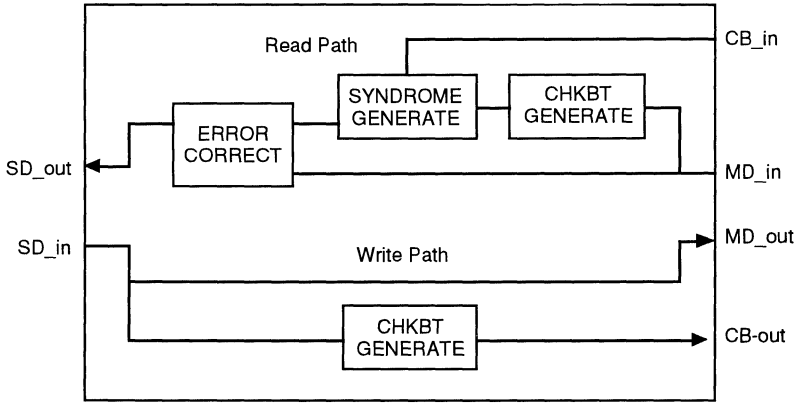


Figure 1. Basic Memory Read and Write paths Through the 49C66

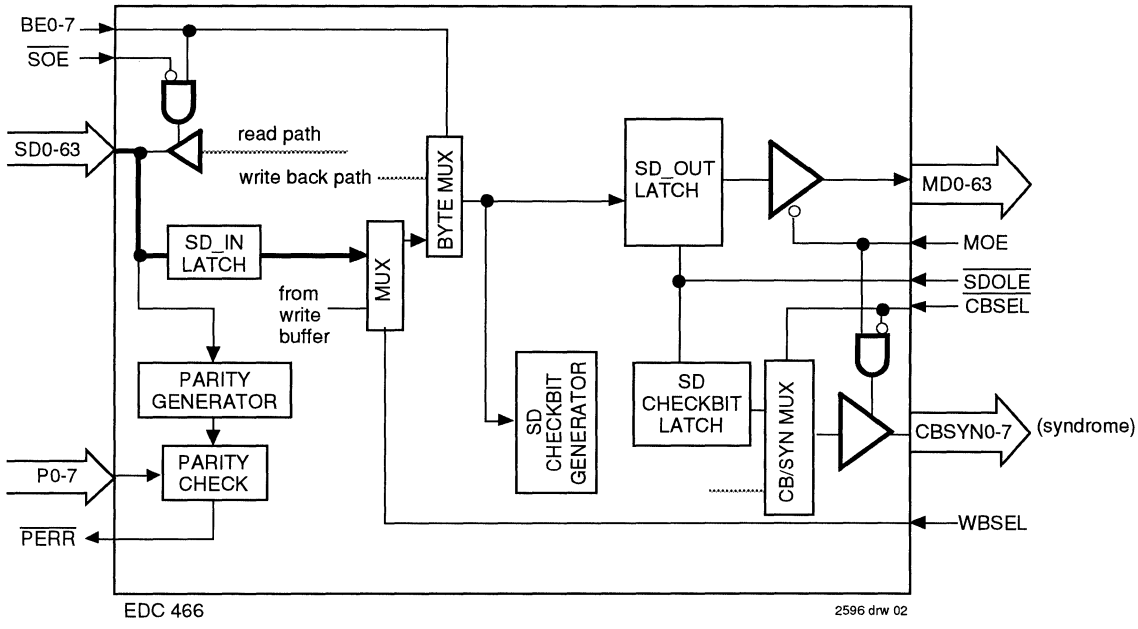


Figure 2. Memory Write without Write Buffer

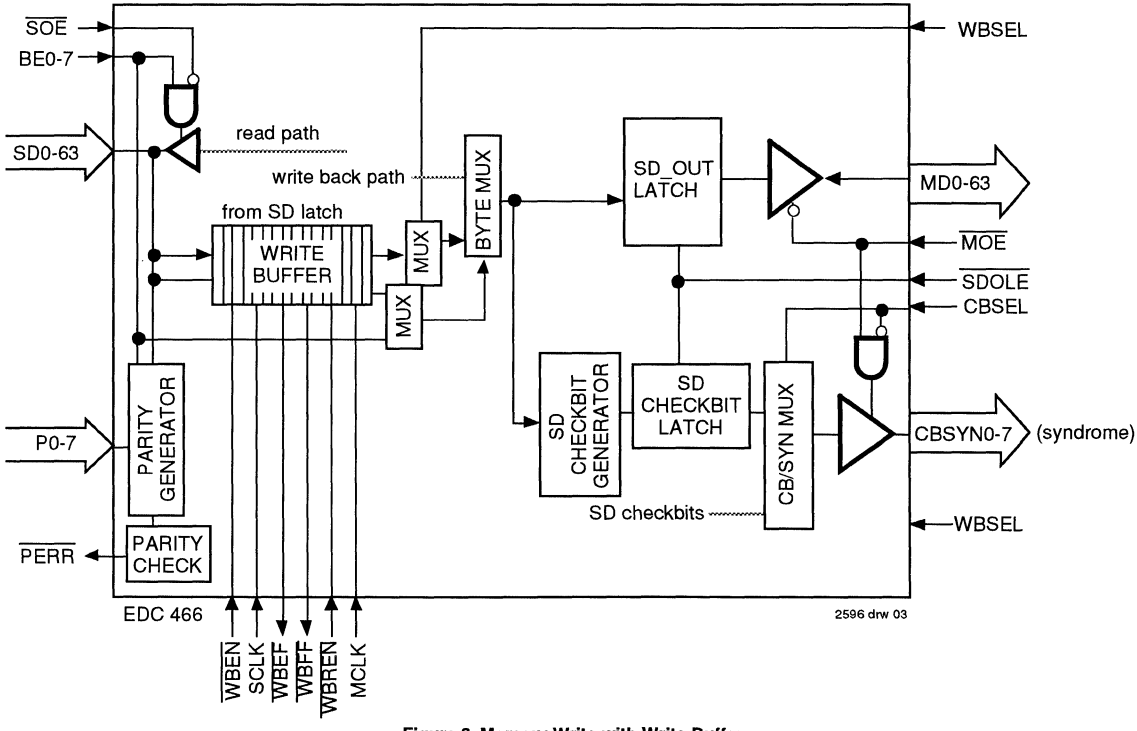


Figure 3. Memory Write with Write Buffer

Beside its primary task of error checking, the 49C466 integrates certain other useful functions on chip. It supports parity checking and generation, partial word writes and diagnostics. It provides the user with flexibility by providing 8/16 deep Read and Write buffers and the facility to latch all data flowing in and out of the part.

The parity generation and checking capability in the 49C466 is very useful in checking the integrity of the data being written to memory. Parity checking is done on data from the system side. The parity bits are input on the EDC P_{0-7} pins. Parity is then generated for the input system data and a comparison of this and the input parity bits is carried out internally. The result of this comparison is reflected in the $\overline{PERR}$ pin output (a discrepancy asserts $\overline{PERR}$). Parity bits are also generated for data read from memory and output on the P_{0-7} pins once again. The parity type (odd or even) is selected using the PSEL pin. The $\overline{PERR}$ signal does not affect any of the other circuitry in the device and hence the user may safely ignore the parity feature if his system does not support parity.

PARTIAL WORD WRITES

The 49C466 supports "partial word writes" or "byte merging". These refer to write operations involving words shorter than 64 bits such as a byte write. Partial word writes are handled in the 49C466 by the byte multiplexer. The 49C466 has eight BE (byte enable) control pins. These control the byte multiplexer and enable the system data output buffer. When a BE input is high, it selects a byte from the MD "write back path" shown in Figure 3 and Figure 4 rather than the normal EDC write path. Each BE input is AND-ed with the $\overline{SOE}$ signal and the result determines which byte is output on the SD bus. A BE pin that is low disables the SD output buffer for the particular byte referenced and selects a byte from the write buffer or SD_in latch rather than one from the MD write back path.

A partial word write or byte merge is analogous to a read-modify-write cycle. The checkbit word generated by a partial data word would be incomplete and hence incorrect. Hence the need to differentiate the "partial word write" case from a normal write operation. The following steps must be followed to ensure correct generation of checkbits for the complete 64 bit word :

1. Read the contents of the location being written to.
2. Merge the partial word with these contents forming a composite 64 bit data word.
3. Generate the 8 checkbits for this composite word.

On account of the dual bus feature of the 49C466, data may be written to the EDC (from processor/cache) while data is read from main memory to the EDC. This feature is useful during partial word writes (writing less than eight bytes) and can buy some time for the designer for whom each nanosecond counts. The time required to turn the external buses around must, however, be taken into consideration.

DESIGNING WITH THE 49C466

As typical application examples, we consider 32-bit and 64-bit processor designs using EDC to protect the slower dynamic main memory. On account of its 64-bit data buses, the 49C466 is easily interfaced to 64-bit systems. As mentioned earlier, providing a 64 bit memory subsystem bus is often advantageous even in 32 bit processor systems. Thus, even though the interface between 32- and 64-bit wide buses may be slightly more complex, it is often worthwhile. Consequently providing a 64-bit EDC may still be an attractive choice.

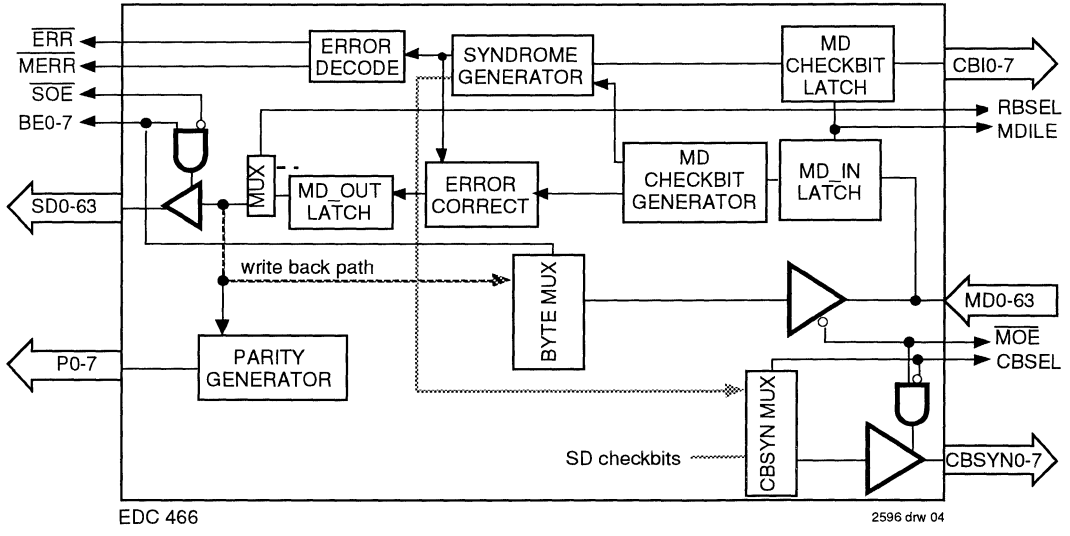


Figure 4. Memory Read without Read Buffer

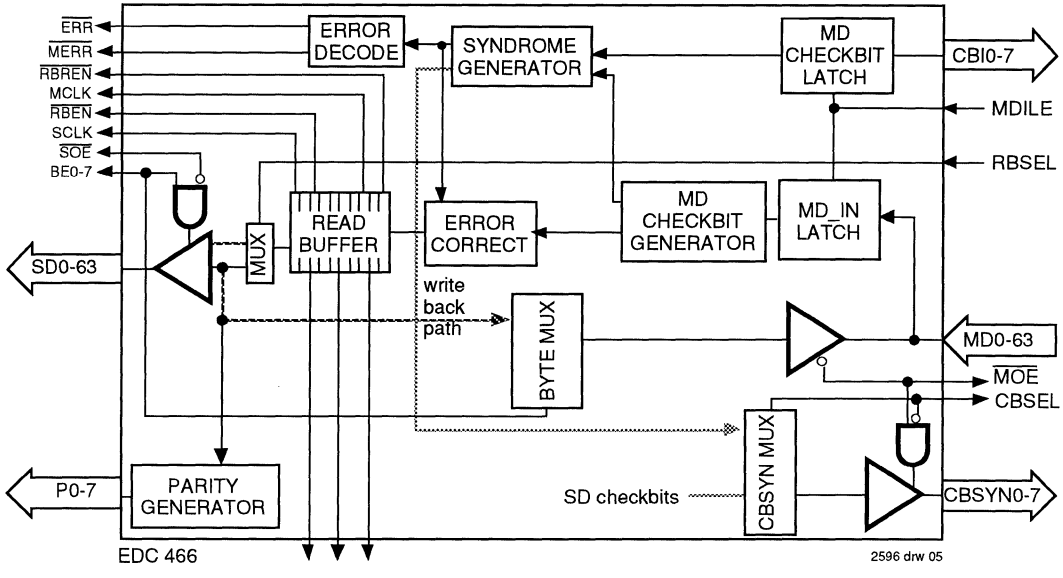


Figure 5 Memory Read with Read Buffer

R3000 BASED SYSTEM

The MIPS R3000 RISC architecture has attained much popularity in recent years. Therefore, we discuss here a design example showing the interface between the 32-bit R3000 and the 64-bit 49C466. This typical R3000 design employs 2 data buses. The high speed "processor" data bus is the interface between processor, caches & buffers while the slower 'memory' data bus links the buffers and I/O devices (peripherals & memory). Providing two separate buses for the processor and memory subsystems, in this manner, serves multiple purposes. It reduces the traffic on each bus and allows for different speeds and widths on the two buses.

In the design shown, the 49C466 is positioned between the 64-bit memory bus and main memory as in Figure 6. Programmable logic is used to generate the control signals for the 49C466 64-bit flowthruEDC™. Appropriate control signals from the R3000 processor provide input to the PAL.

The example considered here does not use the on-chip read/write buffers of the 49C466 and the device is used in a non-pipelined mode. External read/write buffers are provided as the interface between the 32-bit processor bus and the 64-bit memory bus. A 64-bit wide memory bus demands that an appropriate scheme for (32-bit) word gathering be devised. One method of implementing such a scheme is described here.

On write cycles, two 32-bit words are gathered in the two external write buffers and the 64-bit word is output to the memory bus.

Gathering 32-bits words, in this fashion, may not always be permissible because of requirements that the two 32-bit words be written to specific, non-sequential locations. Such cases are treated as partial word writes by the EDC. Each 32-bit word write is handled as an individual partial word write cycle. A partial word write cycle requires that the 32-bit word from the adjoining memory location is read before the whole 64-bit word is written back to memory.

The two categories of writes - "gathering permissible" and "gathering not permissible" - are differentiated by comparing the write addresses generated by the processor for the two words. This demands that the first write address must be latched until the next write request is received. If the two addresses are not consecutive, a partial word write signal is sent to the PAL. This initiates a partial word write cycle for writing the first word to the EDC.

To understand this particular situation better, let us consider a case where two write addresses have been compared and found to be non-sequential. The first write data is buffered in WBufA and the second one in WBufB. Each of these write request are treated as "partial word writes" and handled in the order they were received. In order to support byte access, the memory must be byte addressable. The contents of

WBufA are output to the SD bus of the 49C466. To perform the "partial word write" cycle contents of the location address output from WBufA are simultaneously read

onto the MD bus of the 49C466. Merging of these two 64-bit wide data words is performed inside the 49C466 and the merged 64-bit word is output on the 49C466 MD bus and written back to the same location. When this cycle is complete, the same thing is done for the second write data which is stored in WBufB.

During read cycles, the issue of gathering "reads" and comparing read addresses can be avoided altogether by always reading a 64-bit word from memory.The required 32 bits are selected and the rest ignored.

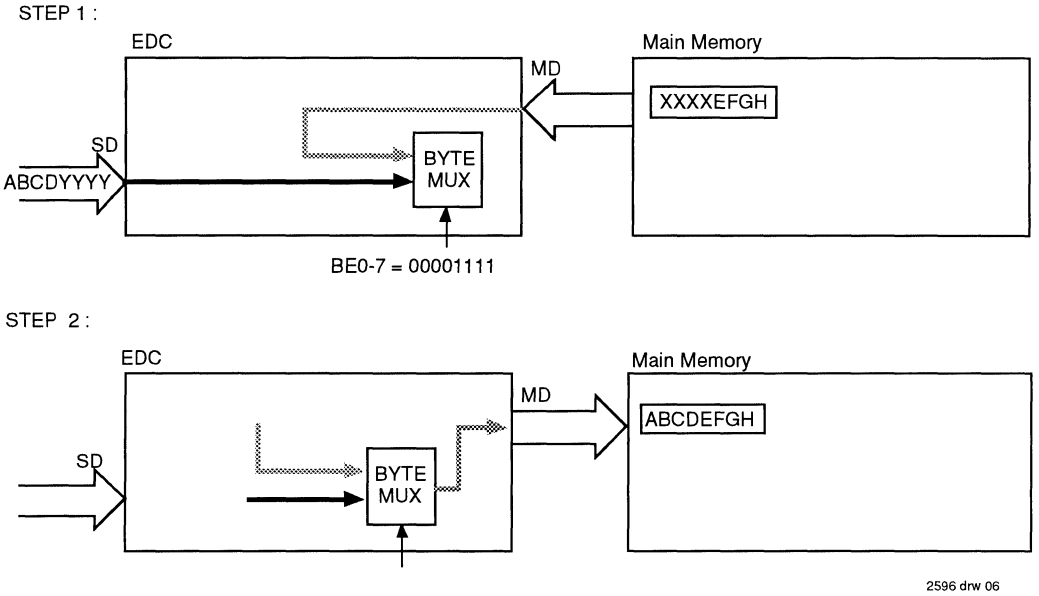


Figure 6. Byte Merge

Details of this scheme, implemented with IDT parts, are shown in Figures 7 and 8.

The design shown, uses a bus multiplexer, the IDT49FCT804 to transfer each 32-bit word to the appropriate SD bus lines (0-31 or 32-63). The write buffer used (IDT 79R3020) buffers both addresses and data. Two bus multiplexers are used to create a crossbar type of arrangement, so that the output of each write buffer can be directed to either the upper or lower SD lines of the 49C466.

64 BIT SYSTEMS

The 49C466 interface to a 64-bit processor is quite straightforward. Intel's i860 and MIPS' R4000 are two popular processors matching this buswidth. Figure 9 shows an i860 based system with EDC. In the system shown all memory accesses go through the 49C466. This kind of a setup would ensure filtering of errors from all memory data accessed. The i860 does not support parity but external parity support circuits (like the AMD280) enable the user to still take advantage of the parity feature of the 49C466. This is particularly useful when caches are employed and some monitoring of data written to main memory is required.

As mentioned earlier, with the trend to segregate processor and memory subsystem designs, a 64 bit memory bus is not unlikely in a 32-bit processor design. In these cases too the 49C466 interface is similar to the one shown above.

MORE EFFECTIVE EDCS

Most present generation EDC units are able to correct only single bit errors. Given the probability of occurrence of multiple bit errors, this is, in most cases, sufficient. The ratio of single bit errors to dual bit errors ranges from 5:1 to 10:1. The probability of multiple bit soft errors occurring is negligible. Also additional hardware is required to correct more than one bit in error. Taking these factors into account, little motivation to move towards multiple bit error correction can exist at this point.

Since hard errors are non-random it is possible for hardware to differentiate them from soft errors. Once this is done it is a simple matter to correct the data provided there is not more than one soft error present. Given below is a brief description of how hard errors can be eliminated.

When an error occurs, the error data is latched in the "error data register" of the 49C466. This data can be read by the processor in the Error Data Mode. In order to filter out hard errors, this data should be inverted and written back to the same location. A subsequent read will serve to identify hard errors, for due to the hard error, the affected bits remain at their original logic level.

Consider a case where bits 3,6 and 7 (shown by bold letters) are affected by hard errors:

Correct Data	= 10101001
Error Data (ED)	= **011**0**0**001
Inverted error data	= 10011110
Inverted error data after subsequent read (SIED)	= 01010110
By XOR-ing the Error Data with the data from the subsequent read, the bits in (hard) error are isolated (indicated by zeroes). (SIED) XOR (ED)	= 00110111

Thus, all that is externally needed to perform this check is XOR logic.

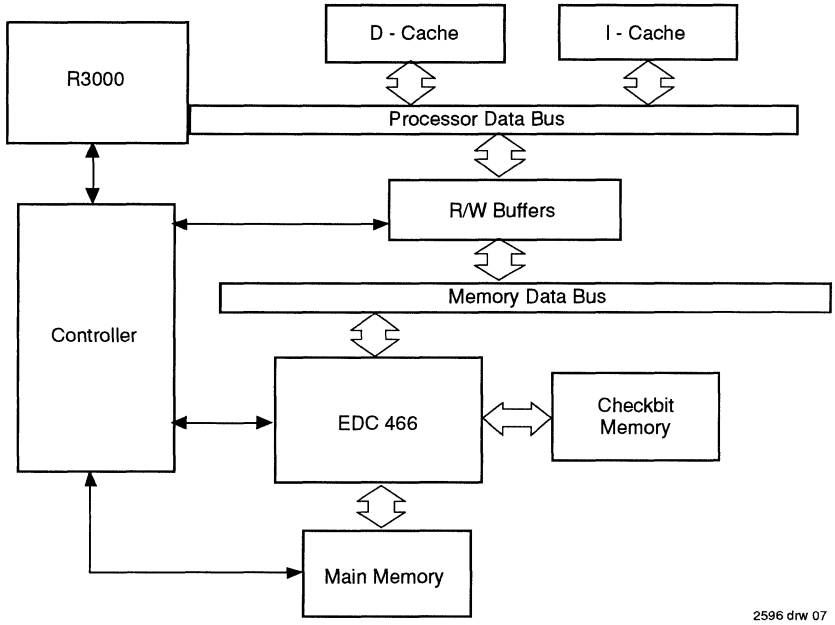


Figure 7. R3000 based System with EDC

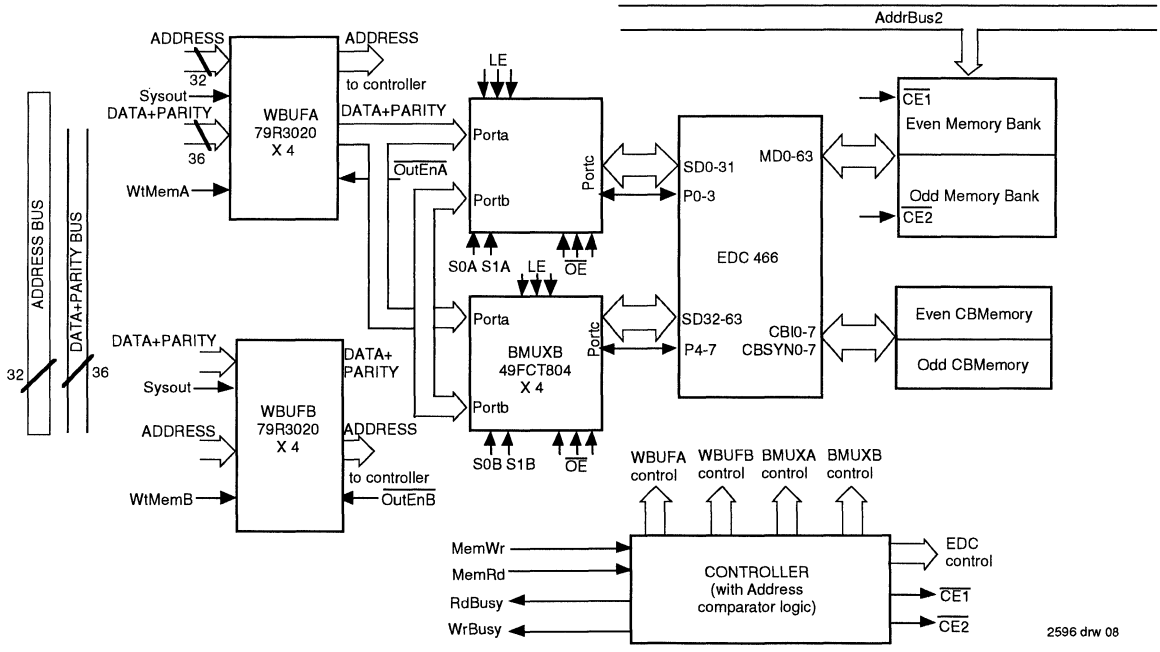


Figure 8. R3000 based EDC System - Memory Write

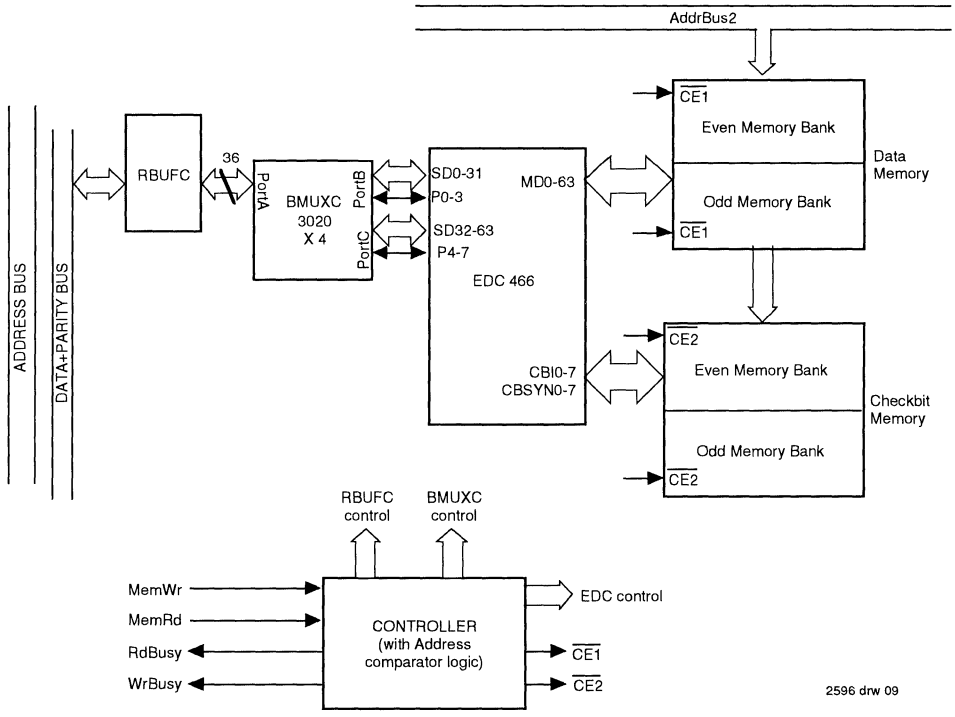


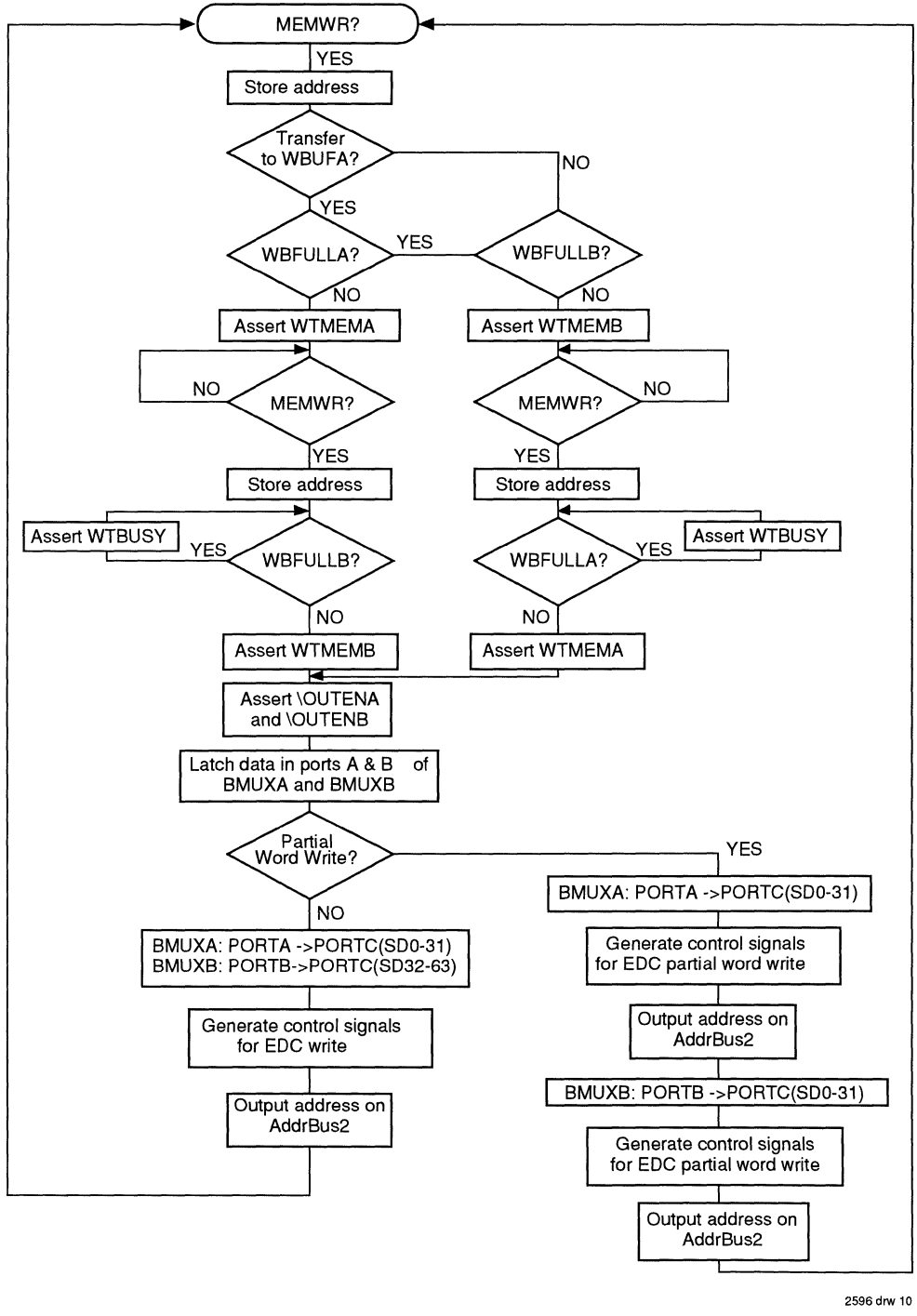
Figure 9. R3000 based EDC System - Memory Read

MEMORY SCRUBBING

An alternative (or in addition) to putting the EDC directly in the read/write path, is putting it in the DRAM refresh path. This ensures that memory is periodically checked for data validity. This is a good practice as it prevents buildup of single bit errors at infrequently accessed memory locations. There are, however, chances of errors slipping through the net in this scheme when an error occurs between a memory refresh and the next memory read or write.

CONCLUSIONS

The urge to provide greater value and reliability in today's competitive computer systems, is likely to make EDC a standard feature in the near future. With the continuing trend towards wider buses, it is only natural to move towards wider EDCs. This also makes the EDC implementation more efficient. IDT is at the forefront of this new generation of EDCs with the powerful new 64-bit flowthruEDC, the 49C466. The 49C466 has an edge over it's competition by providing several useful features such as byte merge capability, 16 deep buffering, latches, diagnostic registers, parity generation and checking and competitive detect and correct times. Currently the device is available in 208 pin PGA and PQFP packages.



2596 drw 10

Figure 10. Flowchart for Write Buffer and Bus Multiplexer Control During Memory Write

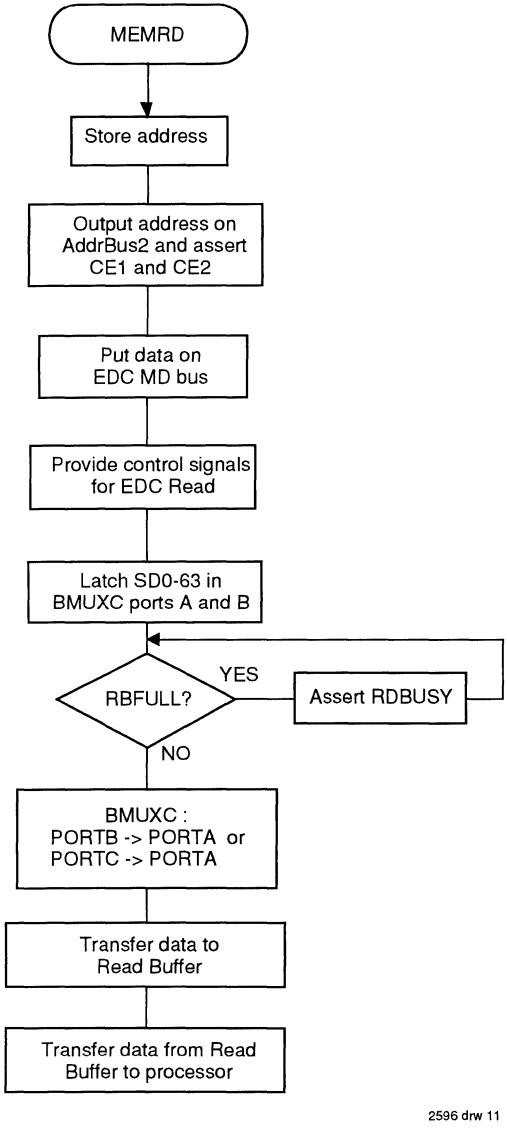


Figure 11. Flowchart for Read Buffer and Bus Multiplexer Control During Memory Read

APPENDIX

MTBF Calculations

DRAM manufacturers specify a soft error rates in terms of FITs (failures in time). Assume a 1M x 1 DRAM with soft error rate = 252 FITs

Thus,

$$\text{MTBF for each 1M x 1 DRAM chip} = \frac{10^9}{252} = 453 \text{ years}$$

$$\text{MTBF for a 4M x 64 memory system (without EDC)} = \frac{453}{4 \times 64} = 1.76 \text{ years}$$

[A memory system without EDC assumes a system failure each time a single bit error occurs. This may not be the reality but this exercise is aimed at showing the difference between two analogous cases, hence such assumptions are in place. Failures due to all higher order (dual, three bit, etc.) errors can be safely ignored in this case due to the overwhelming dominance of single bit errors over other higher order errors.]

With EDC, extra memory is required to store checkbits, hence the number of DRAM chips required for the same memory system goes up.

$$\text{Checkbit memory (with 64 bit EDC) required for the above system} = \frac{1}{8} \times 4 \times 64 = 32 \text{ chips}$$

$$\text{Total memory system chip count} = (4 \times 64) + 32 = 288$$

So now,

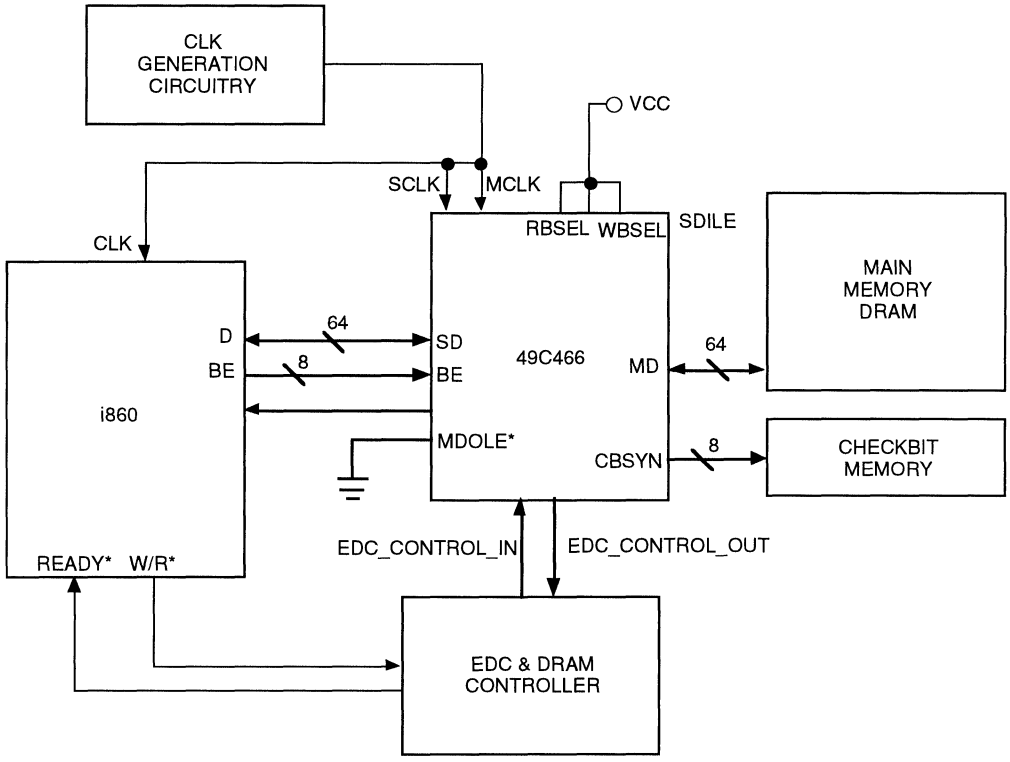
$$\text{Memory system MTBF} = \frac{453}{288} = 1.57 \text{ years}$$

Now if we assume that with EDC, all single bit errors are corrected, failures due to dual bit errors become dominant. Neglecting failures due to higher order errors, we get an approximation of the MTBF using the following formula :

$$\text{MTBF (with EDC)} = \text{(MTBF without EDC)} \times \sqrt{\left(\frac{\pi \times \#\text{ of memory words}}{2}\right)}$$

$$= 1.57 \times \sqrt{\left(\frac{\pi \times 4 \times 10^{12}}{2}\right)} = 3935.4 \text{ years}$$

Thus we see that there is a significant improvement in the MTBF of a system with EDC.



NB : EDC_CONTROL_IN : SDOLE*,MDILE,WBEN*,WBREN*,RBEN*,WBREN*,CBSEL,RS0-1,
EDC_CONTROL_OUT : WBEF*,WBFF*,RBEF*,RBFF*,RBHF*,ERR*,MERR*

2596 drw 12

Figure 10. Flowchart for Write Buffer and Bus Multiplexer Control During Memory Write

Integrated Device Technology, Inc.

CASCADING THE IDT49C460 AND IDT49C465

APPLICATION NOTE AN-96

By Anupama Hegde

INTRODUCTION

Error Detection and Correction units or EDCs are used to check and ensure data integrity in computer systems. Standard off-the-shelf devices do not always meet the needs of the user and need to be cascaded. Cascading EDCs allow the user to expand the EDC bus width. Wider bus operation is advantageous because wider EDCs call for less checkbit memory. On the other hand, an EDC bus wider than the existing system data bus may call for complicated control schemes and hardware overhead. Typically, it is desirable to have the EDC and system bus widths match.

Cascaded EDC operation requires additional logic circuitry. This can be built into the EDC or provided externally by the user. The IDT49C460 and the IDT49C465 each have the required cascading circuitry built into them. This application note explains cascaded EDC operation using the IDT49C460 and IDT49C465.

THE CASCADING PRINCIPLE

When several EDC slices are combined to create a wider data bus, none of the slices can individually produce the complete checkbits. This is because only a part of the complete data word is fed to each slice. Partial checkbits are generated in each slice. The partial checkbits from each slice are XOR-ed to generate the complete checkbit word. The syndrome is produced by an XOR of the complete checkbits and the input checkbits. The sequential order in which these XOR operations occur may vary depending on the implementation. For example, the input checkbits may be XOR-ed with the partial checkbits in any one of the slices rather than after the complete checkbit word is produced. Figure 1 illustrates the operations involved in a cascade.

During a regular memory read with EDC, checkbits and data from memory are fed to the EDC. Checkbits generated from the data are compared with the input checkbits resulting in the syndrome. This is decoded to produce error signals and to correct data. When using a pair of cascaded EDCs, the same operation is done as follows: Partial checkbits are generated from the partial data input to that particular slice. These are XOR-ed to produce the final syndrome. The final syndrome is made available in all the slices. An alternate way of doing things is to simultaneously generate the final syndrome in all the slices. This parallel approach is faster.

CASCADING 32-BIT EDCS FOR 64-BIT OPERATION

Any number of EDCs may be cascaded depending on the available support logic and performance demands. A dual EDC cascade, as supported by the IDT49C460 and IDT49C465 is discussed here.

32-bit checkbit generation logic differs from the 32-bit partial checkbit generation logic that is required for cascading two 32-bit EDCs. Eight checkbits are needed by a 64-bit EDC but the 32-bit checkbit generation logic produces only 7 checkbits. Hence, additional logic is required to generate partial checkbits. The 64-bit checkbit generation scheme (as indicated by 64-bit checkbit generate tables in data sheets) may be split into two 32-bit generation schemes — one

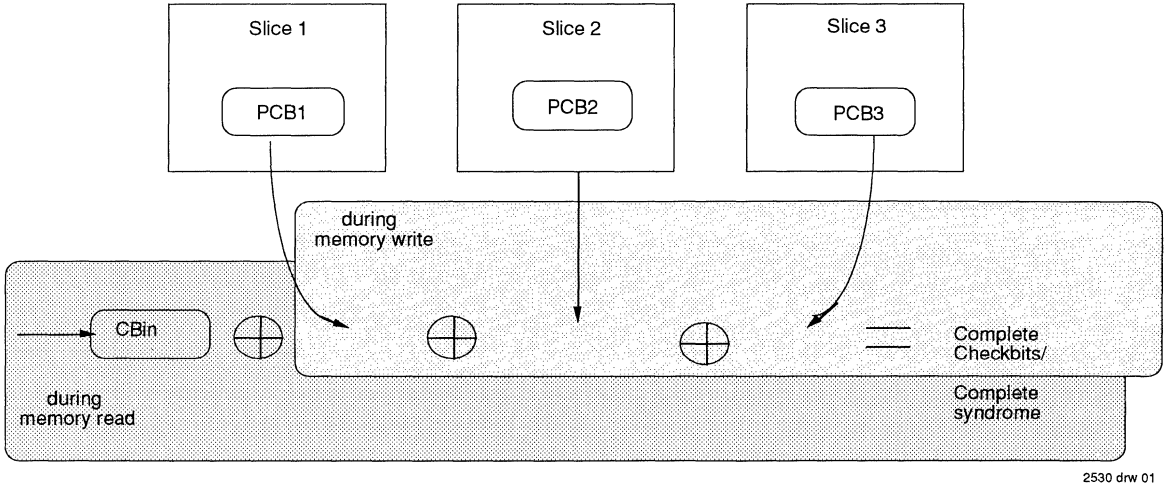


Figure 1. Complete Checkbit Generation From Cascaded Slices

operating on data bits 0-31 and the other on data bits 32-63. This determines the 'partial checkbit generation logic'. Each cascaded slice then produces 8 checkbits which can be XOR-ed to produce the complete checkbit word.

Also, there must be some mechanism to determine whether the EDC is in cascaded mode or not. If it is in cascaded mode, each EDC unit must be identified as a unique slice (first, second, etc.) in the cascade.

The IDT49C460 and the IDT49C465 differ in their architectures. The IDT49C460 has an older 'bus-watch' architecture with one data bus, while the IDT49C465 has a dual data bus Flowthru™ architecture. Both parts have 32-bit wide data buses and use the same basic principle of operation. The IDT49C460 and IDT49C465 have *Code0, 1* lines that program the EDC units to operate in non-cascaded mode or as upper or lower slices in cascaded mode.

CASCADING THE IDT49C460

The figure below shows the correct connections for cascading two 32-bit IDT49C460s. This makes them function as a 64-bit EDC for either **generate** (memory write) or **correct** (memory read) operations. Control signals not shown are common to both units and parallel connections to each slice may be used.

Memory Write

During this kind of operation you need to generate 8 checkbits for a 64-bit data word. In 32-bit mode, the IDT49C460 generates 7 checkbits for each 32-bit data word. In cascaded mode the IDT49C460 must generate **8 partial checkbits** for each set of 32 data bits.

If you compare the checkbit generate tables (Tables 6 and 11) of the IDT49C460 data sheet, you will notice that they are different. For 64-bit cascaded mode operation, Table 11 is to be used. Eight partial checkbits are generated by a logic implementation of the 64-bit checkbit generate table.

In the lower slice; partial checkbit word = 64-bit checkbit generate table applied to data bits 0-31. In the upper slice; partial checkbit word = 64-bit checkbit generate table applied to data bits 32-63.

Example:

Partial Checkbit 0 in lower slice (PCB0_ls) = D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30

Partial Checkbit 0 in upper slice (PCB0_us)= D32 ⊕ D36 ⊕ D38 ⊕ D39 ⊕ D42 ⊕ D44 ⊕ D45 ⊕ D47 ⊕ D48 ⊕ D52 ⊕ D54 ⊕ D55 ⊕ D58 ⊕ D60 ⊕ D61 ⊕ D63

XOR-ing the Partial checkbit 0 from the upper slice and the Partial checkbit #0 from the lower slices gives the final checkbit 0. Thus, check bit 0 for the 64-bit data word = (PCB0_ls) ⊕ (PCB0_us)

D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30 ⊕ D32 ⊕ D36 ⊕ D38 ⊕ D39 ⊕ D42 ⊕ D44 ⊕ D45 ⊕ D47 ⊕ D48 ⊕ D52 ⊕ D54 ⊕ D55 ⊕ D58 ⊕ D60 ⊕ D61 ⊕ D63,

which is what we get from Table 11 for 64-bit data.

The complete checkbit word for the 64-bit data word is generated by XOR-ing each of the partial checkbits from the upper and lower slices. A block diagram illustrating this operation is given in Figure 2.

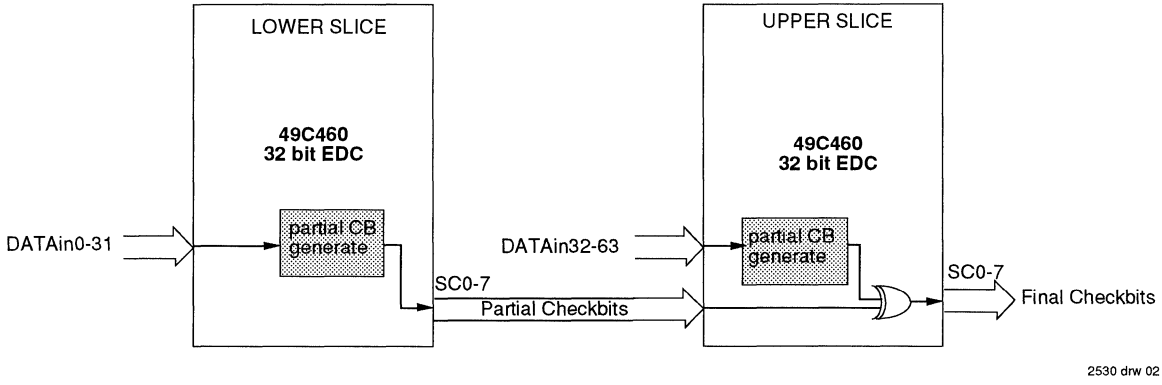


Figure 2. IDT49C460 Cascaded Mode "Memory Write"

Memory Read

A memory read or correct operation involves generation of a complete set of 8 checkbits for the 64-bit data, computation and decoding of the syndrome word, and correction of the data.

A regular 32-bit correct operation involves 7-bit checkbit words and a 7-bit syndrome. Apart from this, the procedure is the same as above.

In 64-bit cascaded mode, you have 8 input checkbits (CB0-7), but each individual slice only generates a 'partial checkbit word'. This is why it is necessary to combine the 'partial checkbit words' from each slice to obtain a complete checkbit word. Once this is done the syndrome can be computed by XOR-ing the 8 input checkbits with the 8 (complete) generated checkbits as usual. Thus,

Final Syndrome = (CB0-7) ⊕ (8 checkbits generated from 64-bit data)

= (CB0-7) ⊕ [(PCB_ls0-7) ⊕ (PCB_us0-7)]

= [(CB0-7) ⊕ [(PCB_ls0-7)] ⊕ PCB_us0-7)

lower slice

upper slice

The first two terms constitute the partial syndrome. In the IDT49C460, the first XOR is done in the lower slice and the result is output on the SC0-7 bus of the lower slice. The second XOR is done in the upper slice and the (final syndrome) result is output on the SC0-7 bus of the upper slice. This final syndrome is then fed back to the lower slice. It must be made available in both slices in order for a correction of either Data0-31 or Data32-63 to be possible.

This entire operation is illustrated in Figure 2. It can be summarized as follows :

1) In the first pass through the lower slice the partial syndrome is generated.
2) The final syndrome is generated in the upper slice. If an error occurs in Data bits 32-63 , the appropriate bit in the lower slice is corrected.
3) The final syndrome is sent back to the lower slice. If an error occurs in the Data bits 0-31, the appropriate bit in the upper slice is corrected.

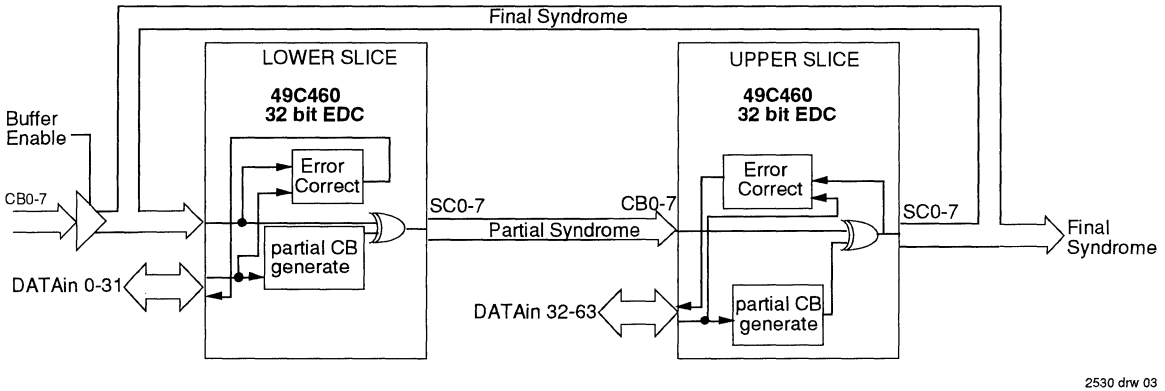


Figure 3. IDT49C460 Cascaded Mode "Memory Read"

USING THE IDT49C465 IN 64-BIT OPERATIONS

In the IDT49C460 the partial checkbits and partial syndrome are output multiplexed on the same bus. In the IDT49C465, however, these are available on separate buses.

During a '**memory write**', the partial checkbits from the lower slice are output on the CBO bus of this slice. They are fed to the PCBI bus of the upper slice. The final checkbits are available on the CBO bus of this upper slice.

While doing a '**memory read**' or detect/correct, the partial syndrome (XOR of input checkbits and checkbits generated in that particular slice) is output on the SYO bus. It is fed to the CBI bus of the upper slice. In this slice, this partial syndrome is XOR-ed with partial checkbits generated in this upper slice to produce the final syndrome. Simultaneously, the partial checkbits produced in the upper slice (from upper 32 data bits) are sent back to the lower slice. They are then XOR-ed with the partial syndrome already available in the lower slice producing the final syndrome in the lower slice as well. Thus, the final syndrome is simultaneously generated in both slices of the IDT49C465 cascade.

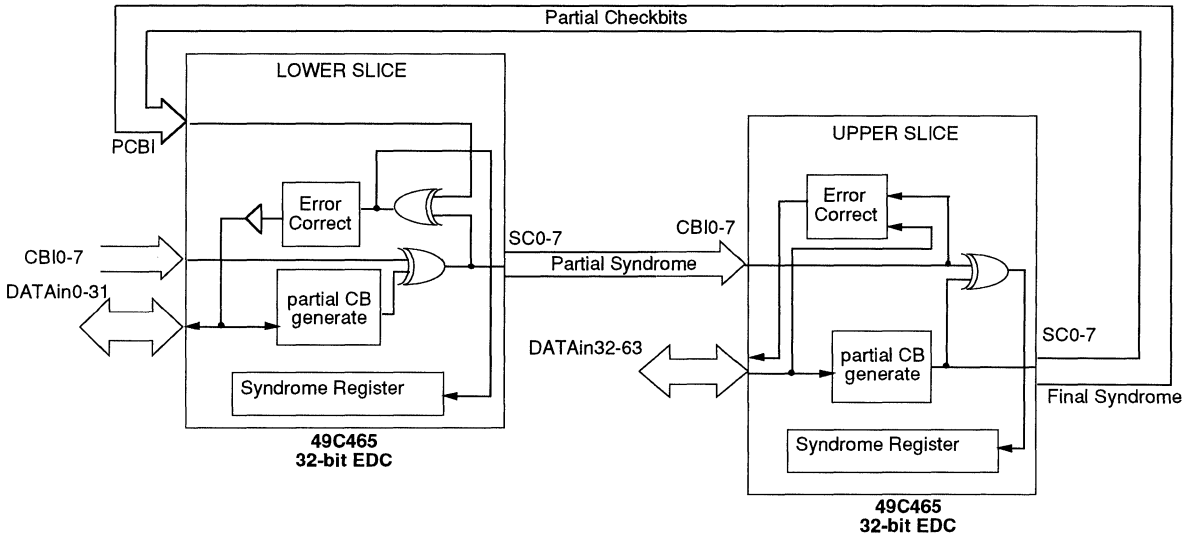


Figure 4. IDT49C465 Cascaded Mode EDC Operation

SUMMARY

As system bus widths continue to grow, cascading EDCs may be necessary. This application note clearly explains the basic principle behind cascading EDCs. It also describes the cascading support available with two 32-bit IDT EDC chips — the IDT49C460 and the IDT49C465.

Integrated Device Technology, Inc.

INTEGRATED LINE TERMINATION SOLUTIONS FOR HIGH-SPEED LOGIC

CONFERENCE PAPER CP-10

By: Stanley Hronik

As logic speeds increase, there is an increase in noise generated by faster edge rates. To reduce noise emissions and generate cleaner waveforms, it is often necessary to terminate signal lines. The need for termination becomes more pronounced when the signals are driven over longer lines, smaller width traces, across backplanes, or at higher frequencies. Properly terminated lines will also reduce noise on the power distribution system which may ease board layout and decoupling.

Termination with external components increases part count, cost and the complexity of board designs. In addressing this problem, component manufacturers have integrated termination schemes into the output buffers of interface circuits which greatly eases the board level design and layout task. By utilizing these traditional and integrated line termination schemes, designers have the ability to increase system performance and reduce costs.

THE NATURE OF THE PROBLEM

With the new families of high speed logic, internal propagation delays have been reduced to the point that the external interface accounts for most of the component propagation delay. In order to increase device speed further, the edge rates and drive capabilities of the devices have been increased. These faster edge rates are adding higher frequency components to the frequency spectrum of the transmitted signal. If the rise/fall time of the signal is shorter than the round trip propagation delay in the signal path, the signal path will act like a transmission line and need termination. The edge rate on high speed logic can be faster than 1 volt/ns. A commonly used equation to determine the maximum unterminated trace length is as follows:

$$L = \frac{Tr}{2Tpd}$$

Tr = Rise/fall time of the signal (ns)
Tpd = Propagation delay of the transmission line (ns/ft)
L = Maximum Unterminated Cable Length (ft)

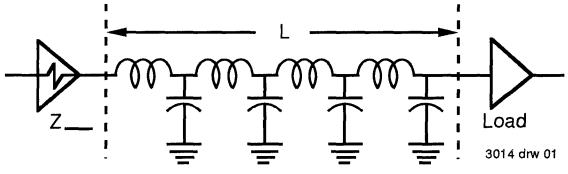


Figure 1. Transmission Line

To maintain good signal quality on a transmission line, the dynamic impedance of the transmission line needs to be constant throughout the line. This means that stubs, unterminated lines and very low source impedances can all contribute to poor signal quality. When a signal passes down a transmission line, if it sees a continuous impedance, it will travel smoothly without reflections. If there are abrupt changes in the impedance at any point in the transmission line, reflections will bounce off of these points and may cause noise if uncontrolled. In designing the transmission line it is best to utilize a single line from source to load. It is acceptable to drive a distributed load by daisy chaining the loads and avoiding stubs. If there is a low impedance load to be driven, it should be at the end of the transmission line.

TRADITIONAL TERMINATION SCHEMES

The following cursory review of the traditional termination methods gives insight into the benefits and drawbacks of each scheme.

Parallel or Shunt Termination:

Parallel termination is the addition of a line matching impedance at the receiver as shown in Figure 2. When the charge from the signal reaches the receiving end of the line, the resistor will drain off excess charge preventing reflections.

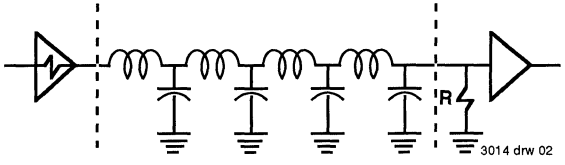


Figure 2. Transmission Line with Shunt Termination

Thevenin Termination:

The Thevenin Termination balances the DC loading on the driver between the logic high state and the logic low state reducing signal distortion. In this scheme, there is a path for DC current to pass directly from the Vcc to Gnd through the termination resistors which will dissipate power regardless of the state of the output driver including the high-impedance state.

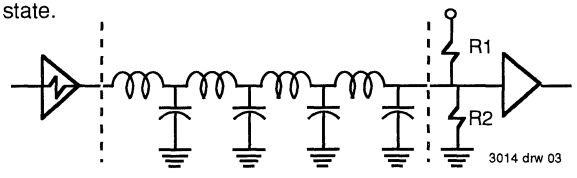


Figure 3. Transmission Line with Thevenin Termination

RC Termination:

An effective method of termination is the RC termination using a 47pf to 200pf capacitor in series with a resistor to ground at the receiver. Larger capacitors give a cleaner waveform but consume more power at high frequencies than lower valued capacitors. The resistor value should equal the characteristic impedance of the transmission line.

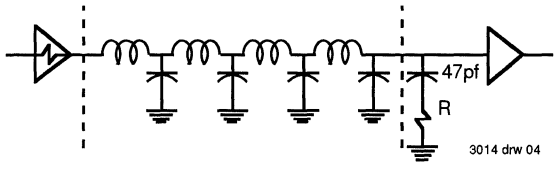


Figure 4. Transmission Line with RC termination

RC termination is very effective for point to point termination over long distances because the signal passes down the transmission line and does not reflect. This makes it possible to use RC termination in cases where the propagation delay of the transmission line exceeds the cycle time of the driving signal. With the AC coupling at the terminating end, there is no DC power consumed by the termination making the scheme useful for low power applications.

Series Termination(1):

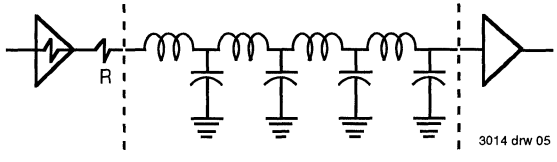


Figure 5. Transmission Line with Series Termination

Series termination is the addition of a resistor between the component output and the transmission line as shown in Figure 5. The combination of the series resistor and the source impedance of the driver act to match the characteristic impedance of the trace.

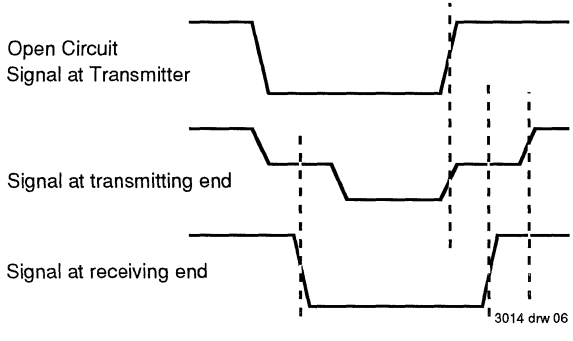


Figure 6. Signals Produced When Using a Series Terminator

As the output driver undergoes a transition, the voltage is divided equally between the output impedance (driver and resistor) and the transmission line, as shown in Figure 6. Because of the matched source impedance, the voltage at the receiver builds up to a level equivalent to the driving voltage and will reflect the signal back from receiver to source and eventually allow a full voltage transition at the source as shown in Figure 6.

Series termination is the simplest, most effective form of reducing signal noise in transmission lines. This method consumes no DC power and helps to reduce dynamic power consumption. Series termination is the only method that handles stubs well and reduces ground bounce. In situations in which the loads on the transmission line are highly capacitive, the series termination may cause time delays due to the RC time constants.

Summary of Traditional Schemes

A relative comparison of the attributes of the four traditional termination schemes is summarized in Table 1.

FEATURES OF THE FOUR TERMINATION SCHEMES

Characteristic	Shunt	Thev	RC	Series
Static Power Dissipation	3	4	1	1
Dynamic Power Dissipation	4	3	2	1
Signal Distortion Due to Unbalance	4	3	1	1
Works with Stubs	4	3	2	1
Distributed Load Driving	1	1	1	2
Parts Count for Termination	1	2	2	1
Works With Heavy Capacitive Loads	1	1	1	2
Good for Low-Impedance Backplanes	1	1	1	2
Works with Tpd > Data Rate	1	1	1	2

tbl 01

INTEGRATED SERIES TERMINATION:

Improvements to the series method can be gained if the series resistor is integrated into the driving component. By integrating the resistor, the output impedances of the driver can be matched to the typical load of a transmission line in both the high and low going cases. Properly designed integrated schemes can outperform external resistor terminations by reducing source follower problems and increasing output drive current. The removal of the external resistors will also reduce part count.

Figure 8A shows a high drive, MOS output structure without any integrated termination. In most component designs with this configuration, the impedance of the pull-up is higher than that of the pull-down. Especially important is the fact that the pull-up loses drive as the output voltages approaches the 5V supply on a low-to-high transition, whereas the pull-down transistor will not suffer this affect on a high to low transition.

Figure 8B shows the same structure with an integrated a series resistor on the output. The effective pull-up and pull-down impedance is now matched better to the line, but the pull-up impedance still remains higher than the pull-down impedance. More importantly, because this configuration creates a source follower, the series resistor exacerbates the relationship between the output voltage and the loss of pull-up drive. An integrated series resistor, directly connected to an output pin, if not properly designed into the component, can easily be damaged by system transients.

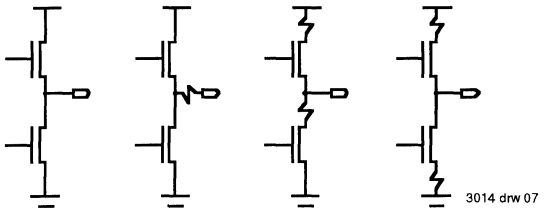


FIG 8A FIG 8B FIG 8C FIG 8D

Figure 8. Various Integrated Output Configurations

Placing the series resistor in the drain of both transistors as shown in Figure 8C alleviates the problems with the source follower created in configuration of 8B. The configuration in 8C will provide good balanced drive and good line termination for both high to low transitions and low to high transitions. The value of the resistors can be adapted to match the line impedance without having to make compromises for the opposite transitions. Despite this, the resistor in the drain of the pull down N channel transistor is still exposed to the output pin and may short if stressed.

In Figure 8D the resistors are sized and placed in the drain of the pull-up and the source of the pull-down transistors to provide good balance between the two paths. The resistors are isolated from the external pin and are now protected against shorting. An added advantage is that a lower value resistor can be used to generate the same drive current that can be generated with a higher value resistor used in configuration 8C.

Several IC manufacturers have introduced components with integrated series resistors. Each of the configurations shown in figure 8 is available from at least one source.

Balanced Output Drive Capability

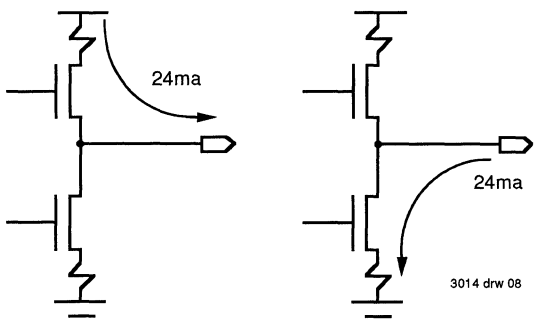


Figure 9. Balanced Drive Output

An additional reason for line termination problems in high speed logic is the fact that some drivers have different drive capability between the high going and low going signals. This makes it difficult to impossible to make a perfectly matched transmission line when the signal has different driving impedances for the two states. To avoid this problem many of the new components that have internal resistors also have a balanced drive capability so that both high going and low going signals demonstrate the same output impedance. Limiting the pull down drive capability of the device also reduces problems with undershoot, ground bounce and general noise generation. Reducing these problems will make the whole task of termination easier.

Benefits of Integrated Series Termination

1) Captures all of the benefits of external series termination
   a) No static power consumption
   b) Reduces dynamic power consumption
   c) Moderately good for stubs
   d) Noise reduction over other termination methods
   e) Reduces component ground bounce
2) Balanced drive produces less signal distortion
3) No external components are needed for termination
   a) Reduced part count, inventory, and costs
   b) Easier board layout
4) Terminated parts are pin compatible with non terminated parts
   a) Plug in replacement.
   b) No new CAD models
5) Higher drive capability than when using external series resistors

Disadvantages of Integrated Series Termination

1) Captures some of the disadvantages of external series termination
   a) May not drive very low impedance backplanes
   b) May not have first incident wave switching with distributed loads
2) Some components are susceptible to damage (Check with manufacturer).

CONCLUSION

Of the methods of termination available, the series termination works best in most applications, especially those situations utilizing shorter distances. Other termination methods have applications in which they will work best, but their overall performance is not as good as series termination in board level applications. When integrating the series resistor into the line driving component there are improvements that can be seen over the use of an external resistor, but careful consideration needs to be given to how the resistor is integrated to achieve optimum results.

(1) "Series Termination," Application Note 50, 1990/91 Logic Data Book, Integrated Device Technology.

Note: This paper was presented at Electro/92, May 12, 1992

Integrated Device Technology, Inc.

NEW OUTPUT STRUCTURE DESIGNS REDUCE SYSTEM NOISE PROBLEMS

CONFERENCE PAPER CP-11

By Stanley Hronik

INTRODUCTION

The new high-speed logic families available in the market place are capable of much higher data rates than earlier families. This is due to a combination of shorter propagation delays in the parts, faster output edge rates, and reduced output switching voltages compared to the CMOS switching levels. These component changes are requiring strict adherance to the design rules to maintain signal integrity. To assist designers in the task of maintaining high speed, low noise operation, many component manufacturers are developing new output structure designs to assist in signal waveform control.

The output structures of the new devices are designed to control internal chip noise and to treat the attached circuitry as a transmission line. Three of the techniques to accomplish this are adjusting the output voltage levels, controlling the output edge rate, and reducing reflections in the transmission line. Each of these techniques will lower the drive current surge in the device output structure which will also assist in controlling ground bounce and Vcc bounce.

Reducing the output voltage swing from CMOS levels to TTL levels allows the signal to acquire state more quickly. The lower voltage swing will reduce the charge dumped into the transmission line which will reduce the energy and noise in the signal transmission. The output edge rate control and the transmission line effects are interrelated and must be approached as a unit.

TRANSMISSION LINE EFFECTS DUE TO FAST EDGE RATES

To determine if a transmission line effect is present, the equation in Figure 1 may be used to determine the maximum unterminated trace length. The equation states that if the rise/fall time of the signal is shorter than the round trip propagation delay in the signal path, the signal path will act like a transmission line and need termination. As an example, IDT's FCT-T family has an edge rate of less than 1V/ns which will require termination on any trace that is over approximately 3 inches.

Because of the speed of newer logic families, the need for proper termination is becoming universal. To simplify board designs a few manufacturers are integrating termination schemes into the output structure of their devices to overcome the need for adding additional termination to the board. By integrating termination schemes into the output structure of the components, other signal quality improvements can also be obtained. To establish the benefits of integrated termination schemes, a few transmission line characteristics need to be understood.

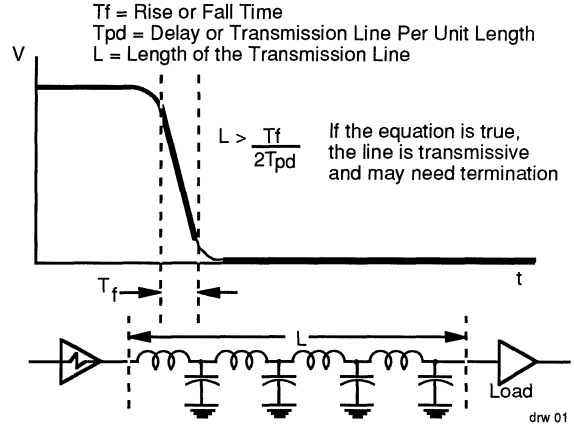


Figure 1. Transmission Line

TRANSMISSION LINE PROBLEMS

To maintain good signal quality on a transmission line, the dynamic impedance of the transmission line needs to be constant throughout the line. This means that very low source impedances, stubs, and high-impedance receivers without line matching termination can all contribute to poor signal quality. If there are abrupt changes in the impedance at any point in the transmission line, reflections will bounce off these points and may cause noise. In designing the transmission line it is best to utilize a single line from the source to the load by daisy chaining distributed high impedance loads and avoiding stubs which cause impedance mismatches. If low-impedance loads are to be driven, they should be at the end of the transmission line opposite the source.

When a driver changes output state and sends a signal down the transmission line, the driver will sense the transmission line but does not have the capability to sense the load at the far end of the line until the signal has had a chance to travel down to the load and reflect back. Because of this the driver for high-speed signals which meet the requirements of the equation for a transmission line as shown in Figure 1 should be optimized to drive the transmission line and not the load.

A transmission line has the same impedance for both high-going and low-going signals. Contrasting this, most transmission line drivers have different drive capabilities in the high and low going directions making it difficult to maintain a high signal integrity for both transitions because of the impedance mismatches between the two directions.

Series Termination

One of the most successful methods of dealing with transmission line effects is the use of series termination. Series termination is the addition of a resistor between the component output and the transmission line, as shown in Figure 2. The combination of the series resistor and the source impedance of the driver act to match the characteristic impedance of the trace or transmission line.

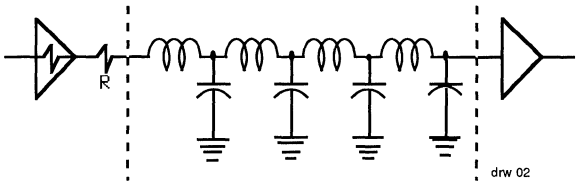


Figure 2. Transmission Line with Series Termination

As the output driver undergoes a transition, the voltage is divided between the output impedance (driver plus the resistor) and the transmission line, as shown in Figure 3. If the output impedance matches the impedance of the transmission line, the output waveform will develop a step at 50% of the voltage transition. If the impedances are not matched, the voltage will divide proportionately to the impedances. To achieve first incident wave switching, the source impedance should be slightly lower than the impedance of the transmission line so that the step appears after crossing the logic threshold of the receiver.

After the driver makes a transition, the signal will propagate down the transmission line and strike the far end. Upon reaching the far end, the signal will look for an impedance matching that of the transmission line. Since the receiver is usually a high-impedance input, the voltage will build up at this point from the current flow until the voltage level has reached a high enough level to counter the inductive nature of the transmission line. If the source impedance matches the line impedance and there were no losses, the voltage would build to twice the driving voltage. At this point, the matching impedance is seen back on the transmission line and the signal will propagate back down the transmission line to the source. Since the driving voltage was about half of the final state voltage, this will bring the voltage in the entire transmission line to the proper level, as shown in Figure 3.

If a designer has a distributed load, and the step voltages shown in Figure 3 do not cross the logic threshold of the daisy-chained load, first incident wave switching may not be achieved. This can be countered by slightly reducing the series resistance values to adjust the step voltage levels so that the steps occur beyond the logic thresholds and first incident wave switching can be guaranteed. This will tend to overdrive the transmission line, but countering this effect will be the "lossy" nature of the line. The series resistor significantly cuts the drive current into the line alleviating most noise problems at the source. Resistive and capacitive elements of the transmission line will absorb portions of the charge which will quickly quiet the signal.

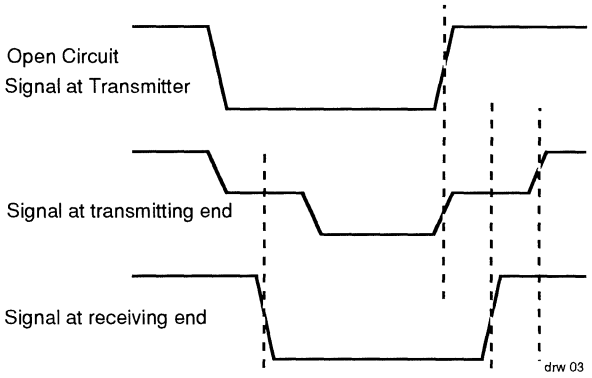


Figure 3. Signals Produced When Using a Series Terminator

Using the series resistor limits, the charge that the source passes into the transmission line reduces the drive current surge of the source. This also reduces the need to dissipate the energy from the charge after the transmission line has reached full voltage levels which will reduce noise spikes on the line, cross talk, power dissipation, noise problems in the power distribution system, and reflection problems.

In most situations, series termination is the simplest, most effective form of reducing signal noise in transmission lines. Series termination consumes no DC power, helps to reduce dynamic power consumption, reduces ground bounce and handles stubs better than most end of the line termination schemes.

INTEGRATED SERIES TERMINATION

Benefits can be received by integrating the series resistor into the output structure of the driving component. By integrating the resistor, the output impedances of the driver can be matched to the typical load of a transmission line for both the high and low going signals, which is not possible with external termination. Properly designed integrated schemes can outperform external resistor terminations by reducing source follower problems and increasing the output drive current. The removal of the external resistors will also reduce part count. To demonstrate the effects of various output structures, a review of several output configurations will be given.

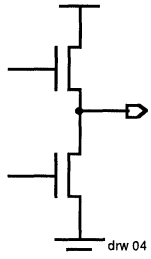


Figure 4. Totem Pole output structure with an N channel pull up transistor. This structure is excellent for backplane driving and low impedance loads.

The configuration in Figure 4 shows a totem pole structure with N channel FETs in both the pull up and pull down positions. The pull up FET requires a Gate to Source turn on voltage of about 1.5V which will drop the typical loaded output voltage to less than 3.5V giving TTL level outputs. In this configuration, the impedance of the pullup is typically higher than that of the pulldown, giving unbalanced drive capabilities in the two directions. With IDT's High Drive components that contain this configuration, the impedance is usually about 6ohms pull down and 22ohms pull up. This structure gives excellent drive capability for low-impedance backplanes and heavy loads that contain external termination.

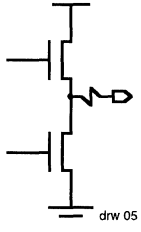


Figure 5. Totem Pole with a series resistor which simulates the addition of an external series resistor.

Figure 5 shows the same structure with a series resistor on the output. The effective output impedance is now matched more closely to the line, but the pull-up impedance remains higher than the pull-down impedance. Because the series resistor degrades the gate to source voltage drop in the pull up FET, the pull up drive capability is reduced, significantly increasing the effective impedance beyond the value of the resistor. The pull down drive is not affected by gate to source degradations. This creates an unbalanced condition, where the pull up drive capability is much lower than the pull down drive strength. The pull up may degrade to an impedance of over 100ohms when utilizing a 25ohm resistor while the pull down will remain at about 31ohms with the same resistor. This problem will be experienced either when an external series resistor is used or when the resistor is integrated into the output structure of the device.

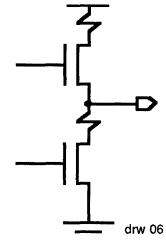


Figure 6. Drain resistors overcome the gain problems with the external resistor.

Placing the series resistor in the drain of both transistors, as shown in Figure 6, alleviates the problems with the gain created in the configuration of Figure 5. The value of each resistor can be adapted to match the line impedance, thus giving similar drive currents in both directions without conflicting with the opposite transition. The configuration in Figure 6 will provide a good balanced drive capability and good line termination for both high-to-low transitions and low-to-high transitions.

In Figure 7, the resistors are sized and placed in the drain of the pull-up and the source of the pull-down transistors. With this configuration the same results as shown in Figure 6 can be achieved by properly sizing the resistors. IDT uses this structure in the Balanced Drive IDTFCT162xxx family.

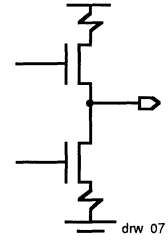


Figure 7. A drain pull up and source pull down allow better drive in the pull down (IDTFCT162xxx).

Using resistors in the output structure of Figure 7 provides a natural internal current limiting capability to the component which will then allow a restructuring of the driving stage. By doing this it is possible to speed up the internal logic of the component to where the output switching will begin more quickly than is possible with the other configurations shown.

Driving Capacitive Loads

In situations in which the loads on the transmission line are highly capacitive, the use of series termination may cause time delays due to the RC time constants. When using IDT's Balanced Drive components, this problem is reduced because of the lower output impedance, quicker response time, and controlled edge rate. IDT's Balanced Drive and High

Drive components have very similar response times for capacitive loads of less than 300pf. Because of its quicker response, the Balanced Drive part will switch faster than a High Drive part for loads of less than 200pf. As the load increases above 200pf, the High Drive part will respond more quickly because of its lower output impedance. Despite these minor differences, the differences in the effects of capacitance on propagation delay between the High Drive and Balanced Drive parts should be less than 0.5ns for any load of less than 300pf. The capacitive derating curves are shown in Figure 8.

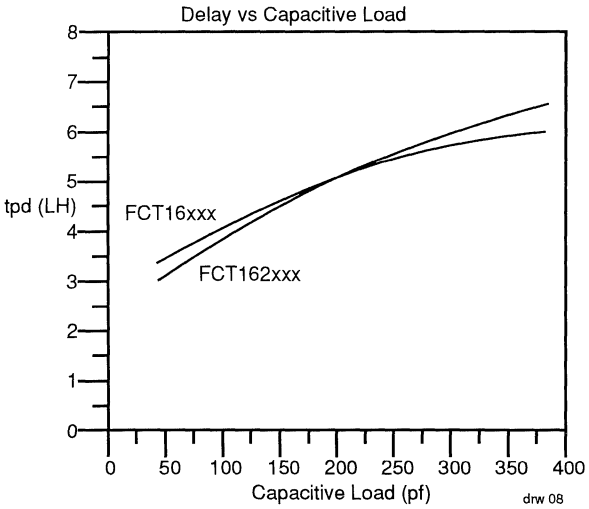


Figure 8, Capacitive Derating for Double Density Balanced Drive and High Drive

When the capacitive load is larger than 400pf at high switching speeds, the load will begin looking like a direct short upon switching and may begin to overdrive the output of both the balanced drive and high drive part. The power dissipation equation is $P = fCV^2$ and should be used to calculate the power consumption for each pin to assure that the total power dissipation in the device does not exceed the maximum rated limits. To avoid exceeding the limit for heavy capacitive loads, a 100ohm series resistor can be used to limit the current to acceptable levels.

Balanced Drive Capability

The output structure of the Balanced Drive part has been specifically designed to give similar transition times with matching absolute edge rates in both the high-going and low-going directions. This means the IDT Balanced Drive family has a matched dynamic drive capability for driving transmission lines, but still has sufficiently low static output impedance to maintain state during during steady state conditions. As shown in Figure 9, during transitions, the Balanced Drive output structure will current limit at about 110ma, typical for both directions, limiting surge current into the transmission line, but still providing sufficient drive current to drive all except the most demanding loads. Limiting the pull down drive capability of the device during transitions also reduces problems with undershoot, ground bounce and general noise generation. During steady state DC conditions, IDT specifies the static drive capability of the devices at 24ma worst case in both directions as shown in Figure 10.

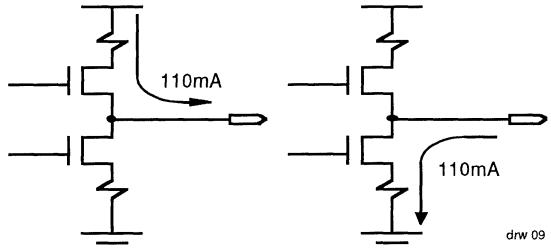


Figure 9, Dynamic Balanced Drive Output

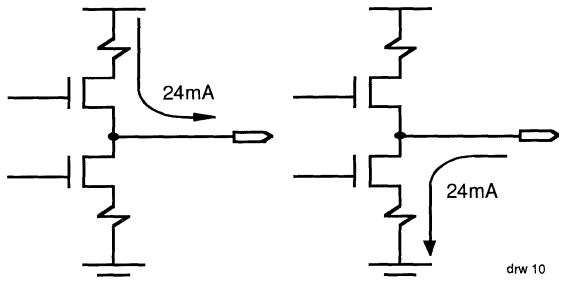


Figure 10. Static Balanced Drive Output

Adding External Resistors to Balanced Drive

With the Balanced Drive components, the effective series termination impedance of about 22ohms is slightly lower than the characteristic impedance of most transmission lines. Backplanes may sometimes approach levels as low as 30ohms, but most lines will have a higher impedance. Despite this difference, the current surge driven into the transmission line will be limited by the output impedance and controlled edge rate. This will usually be sufficient to provide quiet operation without the addition of additional termination.

If it is desirable to further enhance the quiet operation and to achieve a close match between the source impedance and the line impedance, the user may add external resistors to the output of his balanced drive parts. Because of the integrated resistor in the drain of the pull up FET in the Balanced Drive part, the addition of an external resistor will not degrade the gate to source voltage to the extent that the gain degradation

would take place with the standard TTL output of figure 4 for equivalent total resistance values. The voltage drop across the drain resistor will increase the gate to source voltage, partially countering the effect of the external series resistor and retaining some of the balanced drive attributes. As a result, adding an external resistor to a Balance Drive part will not cause a significant impedance mismatch between the high-going and low-going signals, as happens with normal TTL output components.

CONCLUSION

Utilizing the Balanced-Drive family in high-speed bus driving applications will solve most of the problems with noise and line termination experienced with traditional high-speed, low output impedance line drivers. The Balanced Drive logic family provides the benefits of series termination on signal lines while avoiding many of the drawbacks of adding external series termination resistors. The Balanced-Drive family of devices from IDT will generate lower levels of noise than other components in the same speed grade, solve many of the termination line problems encountered by the designer, reduce power consumption and give superior performance to other high-speed logic. Balanced Drive is the logic family of choice for most applications.

Integrated Device Technology, Inc.

DOUBLE-DENSITY™ LOGIC: THE FAST, FLEXIBLE LOGIC FAMILY

CONFERENCE PAPER CP-12

By Wayne T. Yoshimoto

ABSTRACT

This paper discusses how the FCT-T Double-Density™ Logic family addresses the problems faced by PC designers. With microprocessor frequencies rising both in desktops and portables, logic must also rise in performance, but still maintain good noise and power characteristics. High speed/low noise operation for speed-critical paths and high speed/low power operation for battery operated systems are ideal for the designer. Since space is a premium both in portable and desktop PCs, high speed, low power, and low noise must be combined with small packaging.

INTRODUCTION

The level of integration and the rise in frequencies of the microprocessor has had an enormous impact on the PC marketplace. The performance attained only by huge mainframes 15 years ago can now be realized on the desktop. Similarly, the performance and battery life attainable 10 years ago in a 25 pound monster is today far surpassed by a 5 pound, 386-class machine. Correspondingly, the interface logic (buffers, latches, transceivers, etc.) surrounding the microprocessor has gone through significant improvements. Designers are beginning to realize that the older families of interface logic no longer meet the needs of today's and tomorrow's PCs.

Identified shortcomings are in the areas of speed, power consumption (both static and dynamic), packaging, and noise. For example, in a desktop PC running at 50MHz, designers were forced to look elsewhere instead of the popular, but slow, "F" or "AS/ALS" families which were adequate for a 25MHz design. In the case of the newest notebook PCs, designers need to replace the slow "HCT" and high power "ACT" families. Newer families of logic, such as FCT-T Double-Density Logic, can provide designers of both high-performance desktops and low-power notebooks with the best of both worlds, as well as new capabilities, such as 3.3V operation.

FCT-T DOUBLE-DENSITY DEFINED

FCT-T Double-Density is one of the IDT families of high-performance CMOS logic. It is comprised of 16-, 18-, 20-bit wide, extra-quiet, very-low-power, high-performance bus interface logic products. Double-Density is an extension of IDT's earlier family of octal FCT-T devices. Microprocessors' buses have moved beyond 8-bits, creating the need for wider bus interface devices. With the wider devices, partcount is minimized as well board area.

Double-Density is comprised of three distinct versions:

Figure 1. Double-Density Versions

The high-drive version (FCT16XXX) provides –32mA/64mA (Ioh/Iol) drive with ground bounce typically less than 1V. Power-off disable is supported for "live" insertion in fault tolerant systems. This version is a drop-in upgrade for ABT and ACT WideBus™ meeting or exceeding all DC specifications.

The balanced drive version (FCT162XXX) provides –24mA/24mA (Ioh/Iol) drive with integrated series terminating resistors. This reduces ringing/undershoots and ground bounce is typically less than .6V. These are pin-compatible with the high-drive family providing easy upgrade.

The 3.3V version (FCT163XXX) is designed to meet the JEDEC LVTTL standard for 3.3V operation, not a recharacterized or derated 5V device. It provides a drive of -8mA/24mA (Ioh/Iol) and ground bounce typically less than .3V. A number of unidirectional and bidirectional translators are part of this group also to provide solutions for mixed 3.3V/5V hybrid systems.

All three versions of the family are well suited in the following categories and thus provide solutions for PC designers of different types of systems.

PERFORMANCE

In order to keep up with the ever-increasing frequencies of the microprocessor, logic products are constantly pushed to attain faster and faster speeds. Today, with the systems running at 50MHz, logic products with delays of less than 5ns are desirable.

PERFORMANCE OF LOGIC FAMILIES

245 Transceiver	D-Speed	C-Speed	A-Speed	Std-Speed
HCT	—	—	—	29ns
ACT	—	—	—	9.0ns
FAST	—	—	—	7.0ns
FCT-T Octal	3.8ns	4.1ns	4.6ns	7.0ns
DD High Drive	3.8ns	4.1ns	4.6ns	7.0ns
DD Balanced Drive	3.8ns	4.1ns	4.6ns	7.0ns
DD 3.3V	—	—	4.6ns	7.0ns
AS/ALS	—	—	—	7.5ns
ABT	—	—	—	4.6ns

tbl 01

FCT-T Double-Density provides the performance necessary for today's high-performance systems with the power consumption one would expect from CMOS technology. With future systems in mind, IDT has recently announced D-speed logic. A D-speed '244 buffer specifies a maximum of 3.6ns propagation delay. This is ideal for high-performance, 75Mhz and 100Mhz, workstations and 67Mhz+ P5 designs.

Logic has come a long way from the days of LS, TTL, and even HCT. A comparison of the old and new generation of logic is shown in Table 1.

POWER

Running at high frequencies is not without its drawbacks. Since the amount of power dissipated by CMOS is proportional to the frequency, high-frequency operation also means high power. Figure 2 compares the dynamic power consumptions versus frequency of several logic families. As illustrated by the graph, Double-Density provides better power characteristics at all frequency points benefiting both the desktop (high-drive family) and the notebook (balanced drive/3.3V family) designer.

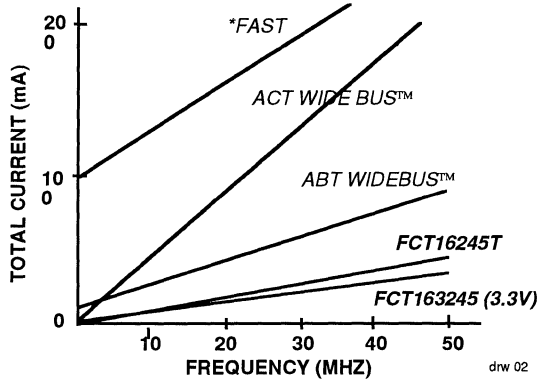


Figure 2. Dynamic Power Comparison

Dynamic power is important when the system is active. During inactivity, static power consumption becomes equally important. The CMOS technology families on the graph, Double-Density and ACT, benefit from very low static power consumption on the order of a few microamps. On the other hand, the other families, FAST (bipolar) and ABT (BiCMOS), suffer from high-static-power consumption. See Figure 3.

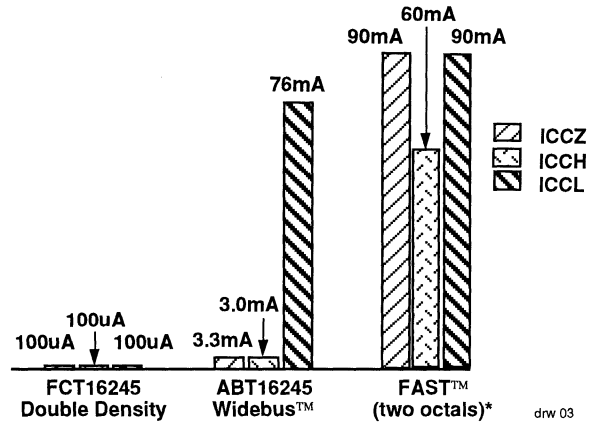


Figure 3. Static Power Comparison

NOISE

Noise issues came to the forefront with the introduction of the first generation of fast CMOS logic in the mid-eighties. Most of these issues were smoothed out by the second generation, with the inclusion of output edge rate controls and reduced output swings. In addition, designers were aware of high-speed design techniques such as series termination and transmission line effects. The Double-Density family makes ground bounce and noise non-issues.

The 48-/56-pin SSOP package provides multiple Vcc (4) and Ground (8) pins for the entire family of 16-bit wide devices. See Figure 4 for the pinouts of a 48-pin SSOP package. As a result, the high-drive version specifies typical ground bounce of less than 1V. The balanced-drive version takes advantage of series termination to reduce noise. They provide integrated series resistors, bringing the typical ground bounce specifications even lower, to less than .6V. The 3.3V version specifies a typical ground bounce of less than .5V due to a smaller output swing of about 3.0V.

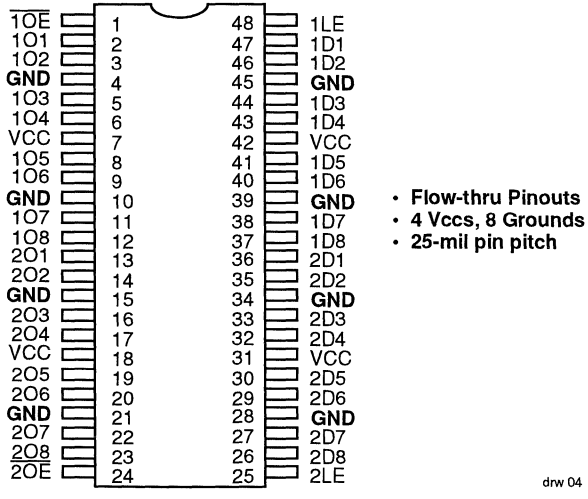


Figure 4. SSOP Package

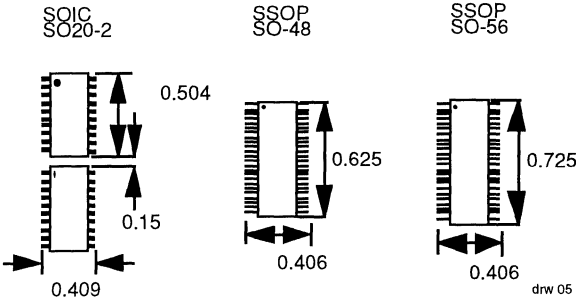


Figure 5. SOIC vs. SSOP Package Comparison

SOIC VS. SSOP PACKAGE

	(2) 20-pin SOIC	(1) 48-pin SSOP	(1) 56-pin SSOP
Area (sq. Inches)	0.474	0.254	0.295
Body Width (Mils)	0.300	0.300	0.300
Area (Normalized)	1.00	0.536	0.523

tbl 02

PACKAGING

Packaging is rapidly becoming an important consideration, due to the integration and size limitations of today's systems. Luckily, packaging technology has not been a limiting factor. Today's highly integrated boards in desktop and notebook PCs have been a result of new packaging technologies. The Double-Density family is packaged in a 25-mil pin pitch 48-/56-pin SSOP package (refer to Figure 4 in the last section). A comparison of the SSOP package versus the standard SOIC package can be seen in Figure 5.

A 47% area-savings can be realized when using the 48-pin SSOP package versus a 20-pin SOIC package. Future packaging capabilities are currently being studied. After all, the trend is toward smaller and smaller packages. Some of the alternatives are: a 210-mil wide, 19.6-mil pin pitch package or a 150-mil wide, 19.6-mil pin pitch package or a 150-mil wide, 15.7-mil pin pitch package. The area savings versus the current SSOP package is 41%, 54%, and 62% respectively. This decision can not be made in a vacuum, since manufacturability must be considered. As the pin pitch and overall package size shrinks, fewer board manufacturers are able to handle production without large investments in new machinery. These considerations will weigh heavily upon where the next step in packaging will be.

SKEW

Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. With processor clock frequencies migrating to 50MHz and 67MHz+, any delay due to skew increasingly becomes a percentage of the clock period. The Double-Density family specifies output skew at typically less than 250 ps, and guaranteed less than 500 ps. These characteristics allow the IDT74FCT16240/244 to be used as minimum skew clock drivers.

3.3V OPERATION

3.3V operation will provide the next step in portable computing. Lighter, smaller, and longer lasting systems will be possible. For example, a 7" x 9" x 2", 4 pound, eight-hour system will be possible in the near future. IDT is ready for the conversion to a 3.3V supply voltage with the 3.3V Double-Density family of bus interface functions, key "glue" logic elements, and 3.3V to 5V interface components. This family will allow designers to develop complete 3.3V or mixed supply 3.3V/5V systems. These devices have been designed to operate from a regulated 3.3V supply for optimal performance and are not simply "recharacterized" or "derated" 5V CMOS parts. Thus, they are able to maintain sub-5ns propagation delays for high-performance portables. See Table 3 for a summary of IDT's 3.3V Double-Density offerings.

DOUBLE-DENSITY 3.3V OFFERINGS

Part #	Function	Avail
FCT163244	Buffer/Line Driver	NOW
FCT163245	Bidirectional Transceiver	NOW
FCT163373	Transparent Latch	NOW
FCT163374	Register (3-State)	NOW
FCT163501	Registered Transceiver	NOW
FCT163646	Transceiver/Registers	NOW

tbl 03

High-speed desktops and fileservers will also benefit from 3.3V operation. Their large memory requirements will force the use of large density DRAMs, 16Mb and 64Mb. Due to the gate geometries of these dense memories, a 3.3V supply voltage will be necessary. Also, at greater than 50MHz, these high-speed systems will benefit from the reduced swings in terms of performance and noise.

3.3V/5V TRANSLATION

Using mixed supply systems will be a necessary transitional phase between the current 5V systems and the upcoming full 3.3V systems. Technological and performance limitations will slow down the conversion of some functions to 3.3V. Therefore, designers must understand the compatibility issues of interfacing between 3.3V and 5V components, as well as what translation functions are available today.

IDT's 3.3V Double-Density family is designed such that any input pin (except I/O) can take an input voltage up to 7V. This feature allows these 3.3V devices to be directly driven by a 5V device. This also allows the unidirectional parts, i.e. FCT163244, FCT163373, FCT163374, to act as one-way 5V-to-3.3V translators. The unidirectional translators accept TTL- or CMOS-compatible signals from 5V components at the inputs, and provide TTL-compatible output levels. These translators avoid any problems associated with a direct interface between a 5V component and a 3.3V bus.

Since not all bus interface applications are unidirectional, there also needs to be bidirectional solutions to the 3.3V to 5V interface. A solution to this is the FCT164245T. This part interfaces between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment, handling all of the 3.3V/5V bidirectional interfacing issues (Figure 6). The FCT164245T is configured as a 16-bit '245 transceiver, giving the designer tri-state capabilities and the ability to select either bidirectional or unidirectional modes. The translator has separate 3.3V and 5V supply and I/O pins both on separate sides of the device. The translator part also features power-off disable, which allows the device to withstand the maximum rated voltages on the inputs and outputs while it is unpowered or partially powered. This is a desirable feature for bus-interface logic in a portable system, because of power management schemes which power down certain subsystems when inactivity is detected. The bus interface device will then have to buffer the active system bus with a powered-off device without damaging itself.

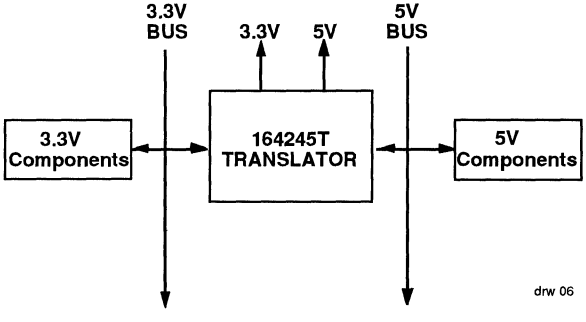


Figure 6. Bidirectional 3.3V/5V Interface

CONCLUSION

As the complexity and frequency of the microprocessor increases, surrounding glue and bus interface logic must keep pace. IDT has done so with the introduction of the Double-Density FCT-T Logic family. This family excels in all categories, including performance, noise reduction, power consumption, skew, and packaging. It also provides innovative 3.3V and 5V/3.3V translation options. The Double-Density Logic family provides solutions for a variety of PC applications ranging from a 3.3V subnotebook to a high-performance fileserver.

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Integrated Device Technology, Inc.

MIXED SUPPLY DESIGN CONSIDERATIONS IN NOTEBOOK PCs

CONFERENCE PAPER CP-13

By Wayne T. Yoshimoto

INTRODUCTION

The explosive growth of the portable Personal Computer (PC) market has manufacturers clamoring for market share by differentiating themselves in battery life and weight from their competitors. The push for longer battery life and lighter weight has reached a point where improvements via traditional design techniques alone are not satisfying users. In order to make the larger, quantum leap to eight or more hours of battery life and weight less than 4 pounds, designers must move to a 3.3V supply voltage. Although most of the components are currently available at 3.3V (i.e. processor, chipset, DRAM, glue logic), the next generation of portable PCs will have to be "hybrid" systems with both 3.3V and 5V supplies until some of the missing components, namely the disk drive and LCD driver, become available. Even after a full 3.3V system is available, the designer must consider the interface with external peripherals, i.e. printers, modems, etc., since these are not likely to move to 3.3V in the near future. The designer will be faced with new challenges pertaining to designing in the mixed supply environment.

MARKET OVERVIEW

1992 marks an explosive point in the portable PC market. Portables have invaded the mainstream and are appearing everywhere from the street corner to the office. Dataquest estimates that by 1994, portables will account for over one-third of the PCs shipped. This shift to portable computing reflects the strides made in the basic technology; they are now powerful enough to replace desktop PCs. There is now no need to have a desktop for the office and a portable for the road.

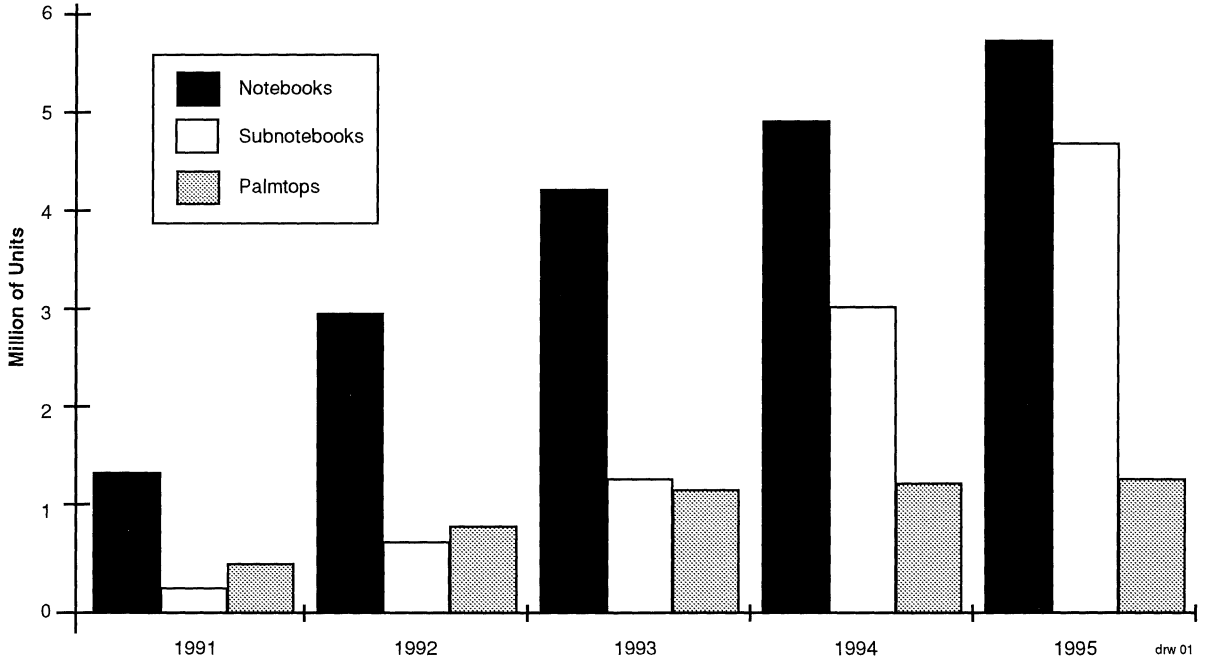

Figure 1. PC Worldwide Market Forecast

Source: Phoenix Technologies Inc.

The market is broken up into a number of segments based on weight: desktops, transportables, laptops, notebooks, subnotebooks, and handhelds. As a whole, the PC market is fast growing with a Compounded Annual Growth Rate (CAGR) of almost 10%. A closer look at the cross section of the market reveals that notebooks and subnotebooks are fueling this growth with a CAGR of 34% and 79% respectively, while the other categories are flat (Figure 1). In order to continue the projected rapid growth, designers must push the battery life and drive the weight down to points way beyond today's limits. To do this, notebook and subnotebook PCs must move to a 3.3V supply voltage.

BENEFITS OF A LOWER SUPPLY VOLTAGE

Moving to a 3.3V supply voltage provides extended battery life and contributes to lighter and smaller systems. Component reliability, and thus, overall reliability is also enhanced resulting from lower heat buildup and a reduction in board-level noise. The end user can expect one of two things: lighter and smaller systems or higher-performance systems with more features, such as built-in fax/modem or color displays, for the same weight.

Decreasing the supply voltage directly increases the battery life. It reduces the power consumption exponentially, leading to a 56% savings [1-(3.3^2/5^2)] at 3.3V versus 5V. The power savings also can amount to less weight because smaller and lighter batteries can be used to provide the same amount of battery life. For example, a 5V notebook typically utilizes five 1.2V NiCd batteries while a 3.3V notebook would use only three batteries, thereby reducing the weight by 40%. On the other hand, the same number of batteries can also be used to provide a system with more built-in features or an even longer battery life. Lower power consumption also results in less heat generation, which leads to fewer cooling requirements and higher reliability of the overall system.

Noise generation has become a problem due to the sharp rise and fall times required by today's high speed systems. By decreasing supply voltage, the voltage swing of the 3.3V parts outputs (typically 3V) is reduced, compared to CMOS (rail-to-rail) swings (typically 4.8V) and TTL-compatible swings (typically 3.3V). This will reduce noise generation, which makes board level design easier, and also will reduce EMI radiation, requiring less shielding to obtain FCC approval. Lighter weight systems will be possible with the reduced shielding requirements.

IDT 3.3V LOGIC CHARACTERISTICS

IDT provides families of optimized low voltage (Vcc = 3.3V±.3V) logic functions which allow designers to develop complete 3.3V systems. These families have been designed to operate from a regulated 3.3V supply for optimal performance and are not simply "recharacterized" or "derated" 5V CMOS parts. These "true" 3.3V families contain 16-bit (IDT74FCT163XXX) and 8-bit (IDT74FCT3XXX) bus interface functions, key "glue" logic elements, and 3.3V to 5V interface components. IDT's leading-edge CEMOS™ 5E process achieves the combination of very low power consumption and high speed. See Table 1 for a comparison between IDT 3.3V FCT and other 3.3V products.

3.3V LOGIC COMPARISON

MFR.	Device	TPD (max)	ICCL(typ)	ICCD(typ)
IDT	FCT3245A	4.6ns	50uA	60uA/MHz
IDT	FCT163245A	4.6ns	50uA	50uA/MHz
TI	LVT	4.6ns	15mA	—
NSC	LVQ245	10.5ns	5uA	221uA/MHz

tbl 01

Although TI's LVT family provides high speed by going to a BiCMOS technology, this is at the expense of static power consumption. National's LVQ family, which is merely a recharacterized version of its FACTQ family, has very slow speeds and high dynamic power. No other 3.3V family provides the high speed and low power combination of IDT's 3.3V logic families.

In addition to speed and low power consumption, IDT's 3.3V logic families provide the following features:

- True TTL compatibility with 400mV noise margin.
- 50% area savings versus standard SOIC packages from SSOP packaging
- Input and Output leakages less than 500 nA.
- Propagation delays match those of 5V FCT logic for like functions
- All inputs (except I/O) can be driven from either 3.3V or 5V components
- Extended commercial temperature range of -40°C to +85°C.
- ESD >2000V per MIL-STD-883, Method 3015.

All of IDT's 3.3V products operate functionally with Vcc as low as 2.5V, allowing them to be used in unregulated battery driven systems.

WHY MIXED SUPPLY VOLTAGES?

Mixed supply systems will be a necessary transitional phase between the current 5V systems and the upcoming full 3.3V systems. Technological and performance limitations will slow down the conversion of some functions to 3.3V. For example, disk drive and LCD driver components will not run off of a 3.3V supply until the end of 1992. Therefore a full 3.3V system will not be available until mid-1993. A mixed supply system, on the other hand, can be realized today. Even a mixed supply system provides enough of a gain in battery life and reduced weight that any manufacturer who waits until a full 3.3V system is possible will be at a competitive disadvantage.

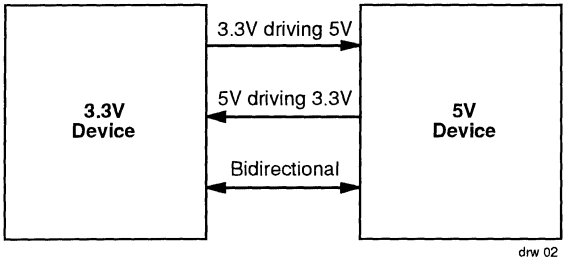

Figure 2. 3V/5V Interface

The mixed supply design concept will not go away once a full 3.3V notebook is possible. The problem of interfacing with external 5V peripherals will still exist. Issues faced while designing the 3.3V/5V interfaces on the motherboard will also be faced in the external interfaces.

INTERFACING 3.3V TO 5V COMPONENTS

In the new design environment of mixed supplies, the designer needs to consider the compatibility issues of interfacing between 3.3V and 5V components. Figure 2 shows the different 3.3V/5V interface scenarios. Although the 3.3V family is TTL-compatible with 3.3V and 5V devices, there are situations where excess current or voltage can develop and damage the components. The designer must understand these situations and provide for them.

For a 3.3V device driving a TTL compatible 5V device, there are no interface problems. The logic input thresholds for the 5V TTL part are V_{IL} = 0.8V and V_{IH} = 2.0V. The 3.3V device is guaranteed to drive a LOW of less than 0.4V and a HIGH of greater than 2.4V at the rated output load currents. This provides ample noise immunity on both ends making this interface problem-free (Figure 3). A 3.3V device will not drive a non-TTL compatible CMOS 5V device, i.e. AC or HC, since the input voltages required are higher than 3.3V, typically 3.85V.

For a 5V device driving a 3.3V device, there are some potential interface problems which must be understood and dealt with; 5V logic will drive 3.3V logic's inputs (except I/O) directly without damage (Figure 4). Some manufacturers have an internal clamp diode from the input or output pin to Vcc in order to boost ESD protection. In these cases, directly driving from a 5V device will forward bias the diode and cause excessive current to flow into the 3.3V supply. IDT's 3.3V Logic family implements ESD protection elsewhere and does not suffer from this problem. Thus, driving from a 5V device is not a problem (Figure 5A).

However, on outputs and I/Os, there is a clamp diode to Vcc limiting the voltage applied to outputs to Vcc+.5V. If a voltage greater than Vcc+.5V is applied, the clamp diode will forward bias and possibly damage the device (Figure 5B). Here the designer must be careful of the output swings of driving devices. Directly driving the 3.3V part from a CMOS swing (rail-to-rail) 5V device could exceed the absolute maximum and damage the device. As long as the 3.3V and 5V supplies track with each other, reduced-swing, TTL-compatible devices can safely drive 3.3V devices.

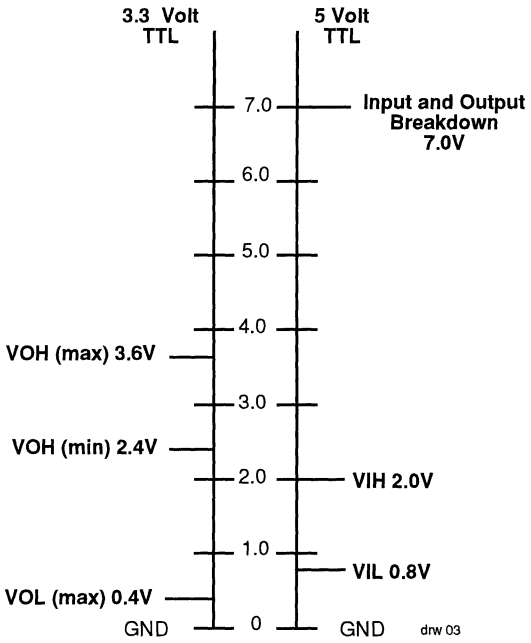

Figure 3. 3.3V Device Driving a 5V System

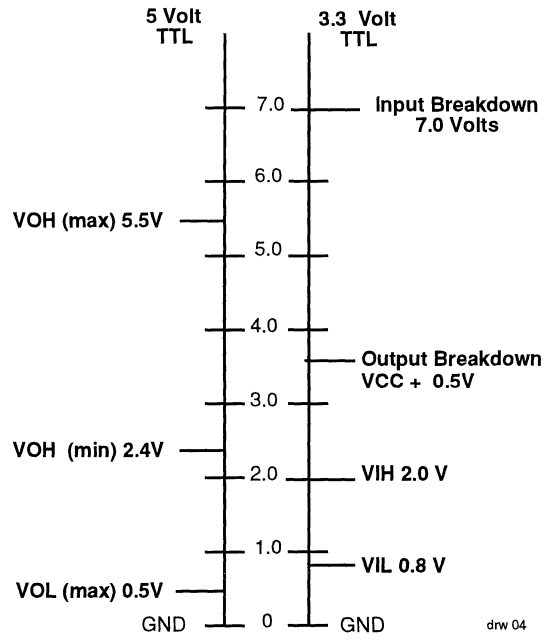

Figure 4. 5V Device Driving a 3.3V Device

UNIDIRECTIONAL TRANSLATORS

As described above, a number of IDT's 3.3V FCT and 5V FCT-T parts can be used as unidirectional 5V-to-3.3V translators. The input pins of the 3.3V FCT family can take an input voltage up to 7V allowing them to be driven by 5V components. Figure 6 contains a list of 3.3V unidirectional translators currently available today. The 5V FCT-T family's reduced output swings, V_{OH} typically 3.3V, allows them to safely drive 3.3V components.

The unidirectional translators accept TTL- or CMOS-compatible signals from 5V components at the inputs and provide TTL-compatible output levels. These translators avoid any problems associated with a direct interface between a 5V component and a 3.3V component or between a 5V component and a 3.3V bus.

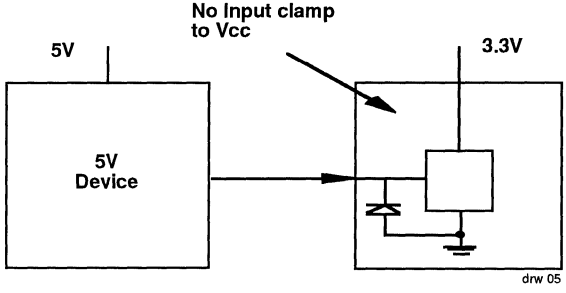

Figure 5A. Simplified Input Structure

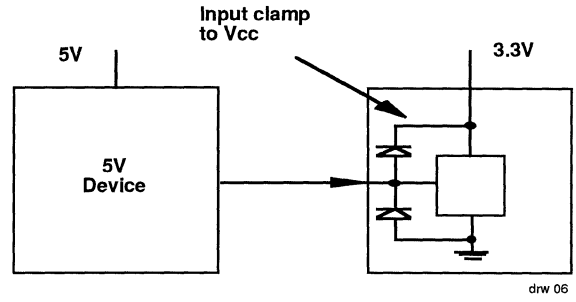

Figure 5B. Simplified Output Structure

3.3V/5V BIDIRECTIONAL TRANSLATOR

Since not all bus interface applications are unidirectional, there needs to also be a bidirectional solution to the 3.3V to 5V interface. A solution to this is the IDT74FCT164245T. It interfaces between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment handling all of the 3.3V/5V bidirectional interfacing issues (Figure 7). It is configured as a 16-bit '245 transceiver, giving the designer tri-state capabilities and the ability to select either bidirectional or unidirectional modes. The translator has separate 3.3V and 5V supply and I/O pins both on separate sides of the device (Figure 8).

All I/O pins and input pins can withstand a maximum input voltage of 7V. This allows both ports to be driven by 3.3V or 5V devices.

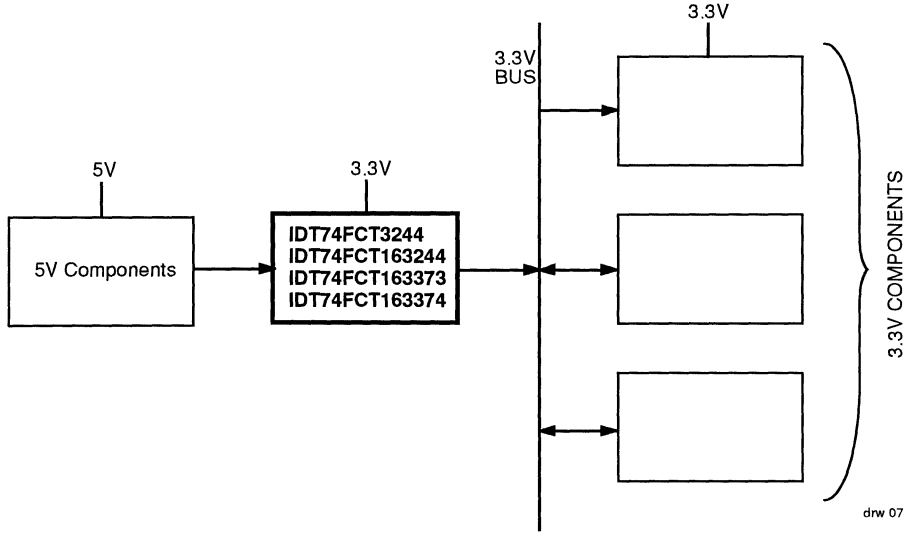

Figure 6. Mixed 5V/3.3V System

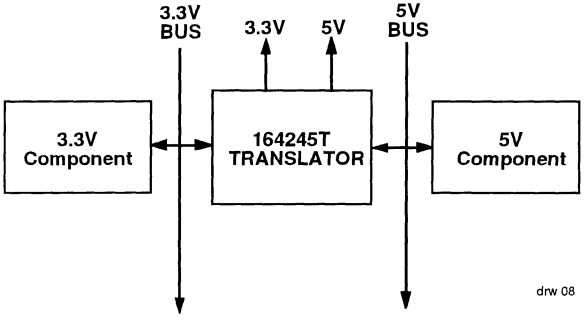

Figure 7. 3.3V to 5V Bidirectional Translator

The translator part also features power-down disable. This allows the device to withstand the maximum rated voltages on the inputs and outputs while it is unpowered or partially powered. This is a desirable feature for bus-interface logic in a portable system because of power management schemes which power down certain subsystems when inactivity is detected. The bus interface device will then have to buffer the active system bus with a powered off device without damaging itself.

To avoid damage to a part which does not support power-down disable, the current from the 5V outputs to the 3.3V outputs or I/O must be limited. The designer may place a resistor between each 5V output and corresponding 3.3V I/O. When the 3.3V I/O is in a high-impedance state, a current will flow from the 5V part to the 3.3V part through the resistor and clamp diode causing a voltage drop between the devices and preventing damage. However, placing a resistor between the 5V and 3.3V part will cause some speed degradation due to the RC time constant which develops between the series resistor and the input capacitance of the 3.3V part and other parts that may be similarly attached.

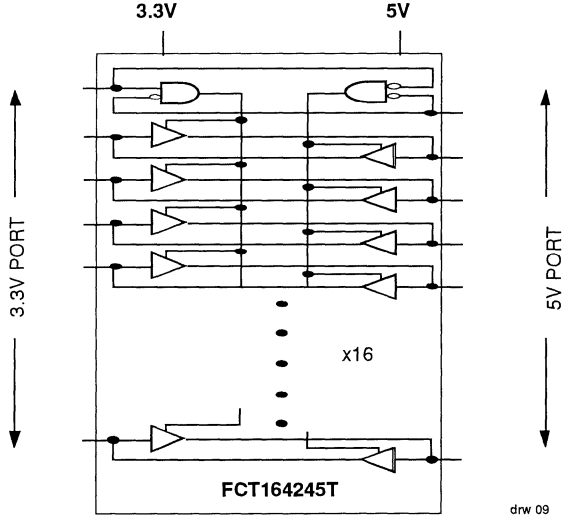

Figure 8. IDTFCT164245T Translator Block Diagram

CONCLUSION

The benefits of a 3.3V supply voltage have forced designers to an interim solution while not all of the components are available at 3.3V. "Hybrid" or mixed supply systems seem to be the interim solution until a full 3.3V system is possible. When the full 3.3V system is possible, the concepts learned must be applied to interfacing with external 5V peripherals. Designing in the mixed supply environment provides new challenges for the designer both in the "hybrid" system and in the external peripheral interface. The compatibility issues of the 3.3V/5V interface and the solutions available today must be understood in order to see notebook PCs with 8 – 12 hour battery life and weight under 4 pounds.

NOTE: This paper was presented at the Silicon Valley Personal Computer (SVPC) Conference on 8/4/92.

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