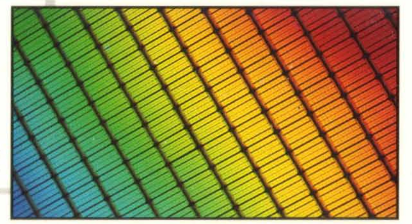
1995 DRAM DATA BOOK



MICRON
TECHNOLOGY, INC.

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MICRON
TECHNOLOGY, INC.

DRAM DATA BOOK

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ABOUT THE COVER:

Front — A variety of features highlight Micron's DRAM product line. Shown at left, a circuitry backdrop rendered from a scanning electron microscope. Bottom right, the intricate memory of a 4 Meg DRAM wafer, etched in silicon, which reflects the many hues of the natural color spectrum.

Back — Micron's Boise, Idaho, headquarters.

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Dear Customer:

Micron Technology, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly reliable memory components. Our corporate mission is:

"To be a world-class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And when you have a design or application question, you can get the answers you need from one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

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ADVANTAGES

Micron Technology brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds. And we establish delivery standards based on customer expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron entered the memory market in 1978, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM) and a variety of other memory products.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many new products, including nonvolatile flash memory, 64 Meg DRAM, and synchronous graphics RAM, and continues to offer the broadest line of 3.3V SRAMs available. Micron is forging ahead into new and exciting frontiers by evaluating 8-inch wafer development and its processing capabilities.

We are pleased to be first to market with our compact, easy-to-install 88-pin DRAM card. Ideal for laptop, notebook and other portable systems, Micron's DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

DIE SALES

In addition to our durable packaging, Micron leads the industry in bare die procurement and the testing of Micron's KGD[Plus]® (known good die). Demand for these is increasing for use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers value-added services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are located in Boise, Idaho, so the component products you need are readily available.

MICRON DATAFAX[SM]

When you can't afford to wait for critical product information or specifications, Micron offers a convenient solution available 24 hours a day, every day. Micron DataFax enables you to make automated requests for data sheets, product literature, and other information from your fax machine. Just dial 208-368-5800 from your fax machine and Micron DataFax will give you instructions on how to order documents, including an index of documents. Once your order is placed, Micron DataFax will process your order, faxing up to two documents per call to your fax machine.

QUALITY

Quality is the most important thing we provide to every Micron customer with each Micron shipment. That's because we believe that quality must be internalized consistently at each level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX intelligent burn-in and test system** gives Micron a unique edge in product reliability.

These quality programs have resulted in Micron becoming one of the first U.S. semiconductor manufacturers to receive ISO 9001 certification. ISO 9001 is the most comprehensive level of certification in the internationally recognized ISO family of specifications. The certification implies that Micron's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and produce consistent results.

*See NOTE, page v.
**For more information on AMBYX, see Section 8.

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ABOUT THIS BOOK

CONTENT

The 1995 *DRAM Data Book* from Micron Technology provides complete specifications on Micron's standard DRAMs, synchronous graphics RAM (SGRAM), DRAM modules and DRAM cards.

The *DRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *SRAM Data Book* and *Flash Memory Data Book.*

SECTION ORGANIZATION

Micron's 1995 *DRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The *Data Book* is organized into twelve sections:

- **Sections 1–6:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 7:** Technical notes.
- **Section 8:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX intelligent burn-in and test system.*
- **Section 9:** Packaging information.
- **Section 10:** Customer service notes and sales information, including a list of sales representatives and distributors worldwide.
- **Section 11:** Micron DataFax index.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the EDO DRAM section begins with the 1 Meg x 4 followed by all other x4 configurations in order of ascending depth. Next come the x8 products, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary (indicated on the top of each data sheet) or Final (final data sheets have no marking). In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of each page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

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DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron uses acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
JEIDA—Japanese Electronics Industry Development Association
PCMCIA—Personal Computer Memory Card International Association

*Micron's *Quality/Reliability Handbook* is available by calling 208-368-3900.

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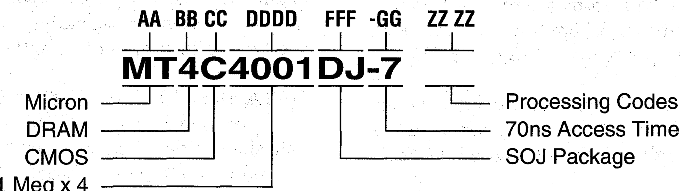
EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product .... MT

BB – PRODUCT FAMILY

DRAM 4
SRAM 5

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM .... Width, Density
TPDRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) .... J
Errata on Base Part .... Q

FFF – PACKAGE CODES

PLASTIC

DIP .... Blank
DIP (Wide Body) .... W
ZIP .... Z
LCC .... EJ
SOP/SOIC .... SG
QFP .... LG
TSOP (Type I) .... VG
TSOP (Type I, Reversed) .... XG
TSOP (Type II) .... TG
TSOP (Reversed) .... RG
TSOP (Longer) .... TL
SOJ .... DJ
SOJ (Reversed) .... DR
SOJ (Longer) .... DL

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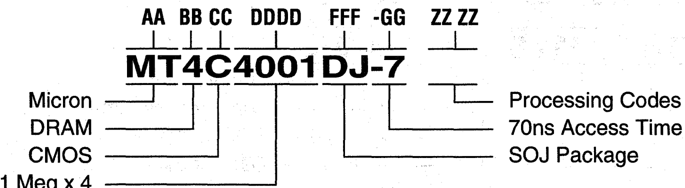
EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

Code	Access Time
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
EPI Wafer	E
Operating Temperature Range	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

*Used in device order codes; this code is not marked on device.

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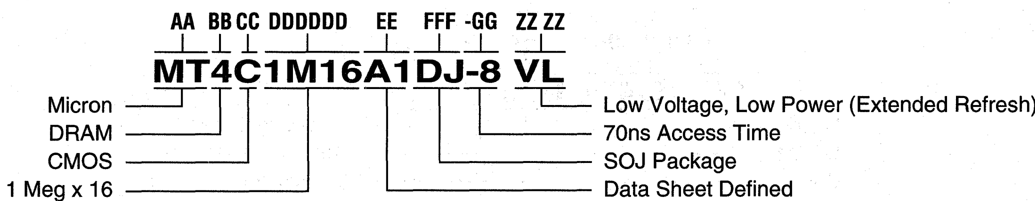
NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product .... MT

BB – PRODUCT FAMILY

Flash (Dual Supply) 28
DRAM 4
SGRAM 41
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS .... B
Low Voltage BiCMOS .... LB
Flash CMOS .... F
Low Voltage Flash CMOS .... LF
AP Flash CMOS .... AF

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits
Flash .... Density, Configuration

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic

DIP .... Blank
DIP (Wide Body) .... W
ZIP .... Z
LCC .... EJ
SOP/SOIC .... SG
QFP .... LG
TSOP (Type II) .... TG
TSOP (Reversed) .... RG
TSOP (Longer) .... TL
SOJ .... DJ
SOJ (Wide) .... DW
SOJ (Reversed) .... DR
SOJ (Longer) .... DL

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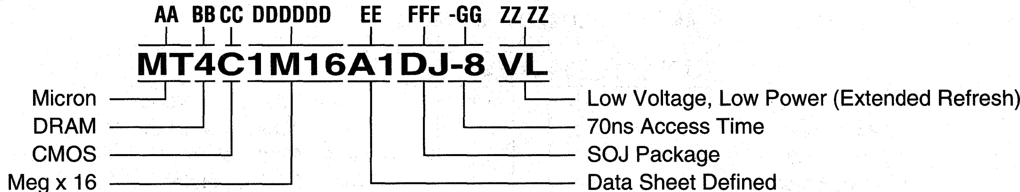
NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

Code	Access Time
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Description	Code
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
Flash	
3.3V Read (AP)	V
Bottom Boot Block	B
Top Boot Block	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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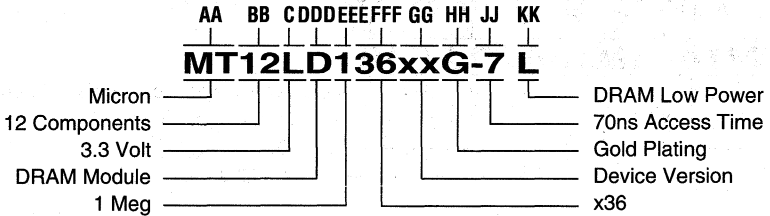
MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY
LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY
DRAM .... D
DRAM TSOP .... DT
SRAM .... S
SRAM TSOP .... ST
SYNCHRONOUS SRAM .... SY
SYNCHRONOUS SRAM TQFP .... SYT

EEE – DEPTH

FFF – WIDTH

GG – DEVICE VERSIONS
Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE
Gold Plated SIMM/DIMM .... G
ZIP .... Z
SIP .... N
SIMM/DIMM .... M
Small Outline DIMM .... H
Small Outline Gold DIMM .... HG
Double-Sided SIMM (1 or 4 Meg x 36 Only) .... DM
Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) .... DG

JJ – ACCESS TIME
-10 .... 10ns
-12 .... 12ns
-15 .... 15ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

KK – MODULE SPECIAL DESIGNATOR
SRAM
2V data retention L
Low Power .... P
Low Power, 2V data retention .... LP
DRAM
Low Power (Extended Refresh) L
ECC C
Extended Data Out X
Self Refresh .... S
16 Meg DRAM 4,096 Refresh .... A

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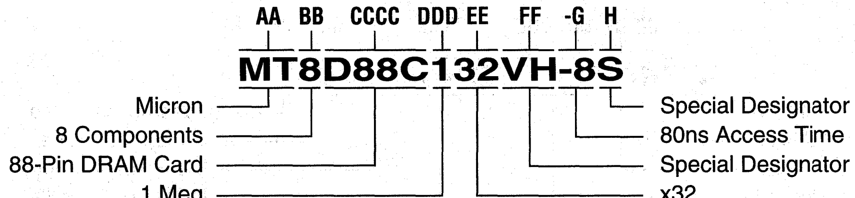
DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier

Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT

88-Pin DRAM Card D88C

DDD – DEPTH

EE – WIDTH

FF – SPECIAL DESIGNATOR

3.3 Volts V
Reduced length (2") .... H

G – ACCESS TIME

-5 .... 50ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

H– SPECIAL DESIGNATOR

Self Refresh .... S

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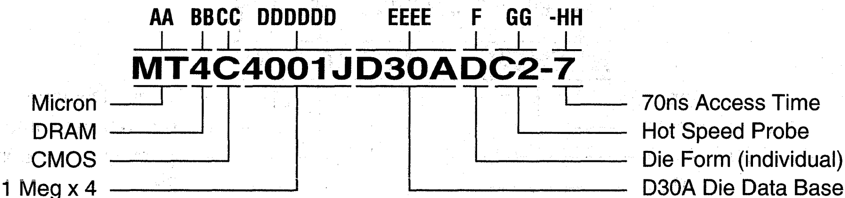
DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Component Product .... MT

BB – PRODUCT FAMILY

SRAM 5
DRAM 4
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER

When *no* alpha character appears as part of this section, the section is defined as:

DRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM

Die Form .... D
Wafer Form (6" Wafer) .... W

GG – TESTING LEVELS

Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3
KGDPlus® C7

HH – ACCESS TIME

(Applicable for C2 and C3 only)

-5 .... 5ns or 50ns
-6 .... 6ns or 60ns
-7 .... 7ns or 70ns
-8 .... 8ns or 80ns
-9 .... 9ns or 90ns
-10 .... 10ns or 100ns
-12 .... 12ns or 120ns
-15 .... 15ns or 150ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-45 .... 45ns
-50 (SRAM only) 50ns
-SS (C2 only) .... speed sorted

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EDO DRAMs

Part	Organization	Features	PAGE
MT4C4007J	1 Meg x 4	5V	1-1
MT4C4007J S	1 Meg x 4	5V, S	1-1
MT4LC4007J	1 Meg x 4	3.3V	1-15
MT4LC4007J S	1 Meg x 4	3.3V, S	1-15
MT4LC4M4E8	4 Meg x 4	3.3V, 2KR	1-31
MT4LC4M4E8 S	4 Meg x 4	3.3V, 2KR, S	1-31
MT4LC16M4G3	16 Meg x 4	3.3V, 8KR	1-47
MT4LC16M4H9	16 Meg x 4	3.3V, 4KR	1-47
MT4LC2M8E7	2 Meg x 8	3.3V, 2KR	1-63
MT4LC2M8E7 S	2 Meg x 8	3.3V, 2KR, S	1-63
MT4LC8M8P4	8 Meg x 8	3.3V, 8KR	1-77
MT4LC8M8C2	8 Meg x 8	3.3V, 4KR	1-77
MT4C16270	256K x 16	5V, DC	1-91
MT4LC16270	256K x 16	3.3V, DC	1-107
MT4LC1M16E5	1 Meg x 16	3.3V, DC, 1KR	1-123
MT4LC1M16E5 S	1 Meg x 16	3.3V, DC, 1KR, S	1-123

DC .... Dual CAS
2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
5V .... 5 volt Vcc
1KR .... 1,024 Refresh
4KR .... 4,096 Refresh
S .... SELF REFRESH
3.3V .... 3.3 volt Vcc

FPM DRAMs

Part	Organization	Features	PAGE
MT4C1004J	4 Meg x 1	5V	2-1
MT4C1004J S	4 Meg x 1	5V, S	2-1
MT4C4001J	1 Meg x 4	5V	2-15
MT4C4001J S	1 Meg x 4	5V, S	2-15
MT4LC4001J	1 Meg x 4	3.3V	2-29
MT4LC4001J S	1 Meg x 4	3.3V, S	2-29
MT4C4004J	1 Meg x 4	5V, QC	2-41
MT4C4M4B1	4 Meg x 4	5V, 2KR	2-53
MT4LC4M4B1	4 Meg x 4	3.3V, 2KR	2-65
MT4LC4M4B1 S	4 Meg x 4	3.3V, 2KR, S	2-65
MT4LC16M4A7	16 Meg x 4	3.3V, 8KR	2-79
MT4LC16M4T8	16 Meg x 4	3.3V, 4KR	2-79
MT4LC2M8B1	2 Meg x 8	3.3V, 2KR	2-91
MT4LC2M8B1 S	2 Meg x 8	3.3V, 2KR, S	2-91
MT4LC8M8E1	8 Meg x 8	3.3V, 8KR	2-105
MT4LC8M8B6	8 Meg x 8	3.3V, 4KR	2-105
MT4C16257	256K x 16	5V, DC	2-117
MT4LC16257	256K x 16	3.3V, DC	2-131
MT4LC16257 S	256K x 16	3.3V, DC, S	2-131
MT4C1M16C3	1 Meg x 16	5V, DC, 1KR	2-147
MT4LC1M16C3	1 Meg x 16	3.3V, DC, 1KR	2-163
MT4LC1M16C3 S	1 Meg x 16	3.3V, DC, 1KR, S	2-163

DC .... Dual CAS
1KR .... 1,024 Refresh
4KR .... 4,096 Refresh
S .... SELF REFRESH
3.3V .... 3.3 volt Vcc
QC .... Quad CAS
2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
5V .... 5 volt Vcc

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SGRAM

Part	Organization	Features	PAGE
MT41LC256K32D4	256K x 32	3.3V	3-1
MT41LC256K32D4 S	256K x 32	3.3V, S	3-1

S .... SELF REFRESH
3.3V .... 3.3 volt Vcc

DRAM SIMMs

Part	Organization	Features	PAGE
MT2D18	1 Meg x 8	5V	4-1
MT2D48	4 Meg x 8	5V	4-11
MT8D48	4 Meg x 8	5V	4-21
MT3D49	4 Meg x 9	5V	4-31
MT9D49	4 Meg x 9	5V	4-41
MT2D25632	256K x 32	5V	4-51
MT4D51232	512K x 32	5V	4-51
MT8D132	1 Meg x 32	5V	4-63
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S .... SELF REFRESH
EDO .... Extended Data-Out
5V .... 5 volt Vcc
3.3V .... 3.3 volt Vcc

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S ... SELF REFRESH **EDO** ... Extended Data-Out
5V ... 5 volt Vcc **3.3V** ... 3.3 volt Vcc

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5V ... 5 volt Vcc **3.3V** ... 3.3 volt Vcc

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EDO DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/No. of Pins		Page
				Standby	Active	SOJ	TSOP	
3.3V EDO DRAMs								
1 Meg x 4	EDO	MT4LC4007J	60, 70, 80	1mW	115mW	20/26	-	1-15
1 Meg x 4	EDO, S	MT4LC4007J S	60, 70, 80	0.25mW	115mW	20/26	-	1-15
4 Meg x 4	EDO, 2KR	MT4LC4M4E8	60, 70	1mW	150mW	24/26	24/26	1-31
4 Meg x 4	EDO, 2KR, S	MT4LC4M4E8 S	60, 70	0.4mW	150mW	24/26	24/26	1-31
16 Meg x 4	EDO, 8KR	MT4LC16M4G3	50, 60, 70	1mW	165mW	34	34	1-47
16 Meg x 4	EDO, 4KR	MT4LC16M4H9	50, 60, 70	1mW	165mW	34	34	1-47
2 Meg x 8	EDO, 2KR	MT4LC2M8E7	60, 70	1mW	150mW	28	28	1-63
2 Meg x 8	EDO, 2KR, S	MT4LC2M8E7 S	60, 70	0.3mW	150mW	28	28	1-63
8 Meg x 8	EDO, 8KR	MT4LC8M8P4	50, 60, 70	1mW	170mW	34	34	1-77
8 Meg x 8	EDO, 4KR	MT4LC8M8C2	50, 60, 70	1mW	170mW	34	34	1-77
256K x 16	EDO, DC	MT4LC16270	60, 70, 80	1mW	85mW	40	40/44	1-107
1 Meg x 16	EDO, DC, 1KR	MT4LC1M16E5	60, 70	0.9mW	180mW	-	44/50	1-123
1 Meg x 16	EDO, DC, 1KR, S	MT4LC1M16E5 S	60, 70	0.3mW	180mW	-	44/50	1-123
5V EDO DRAMs								
1 Meg x 4	EDO	MT4C4007J	60, 70	3mW	175mW	20/26	-	1-1
1 Meg x 4	EDO, S	MT4C4007J S	60, 70	0.8mW	175mW	20/26	-	1-1
256K x 16	EDO, DC	MT4C16270	60, 70, 80	3mW	300mW	40	40/44	1-91

EDO = Extended Data-Out, DC = Dual CAS, 1KR = 1,024 Refresh, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, 8KR = 8,192 Refresh, S = SELF REFRESH

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FPM DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/No. of Pins		Page
				Standby	Active	SOJ	TSOP	
3.3V FPM DRAMs								
1 Meg x 4	FPM	MT4LC4001J	60, 70, 80	1mW	100mW	20/26	20/26	2-29
1 Meg x 4	FPM, S	MT4LC4001J S	60, 70, 80	0.3mW	100mW	20/26	20/26	2-29
4 Meg x 4	FPM, 2KR	MT4LC4M4B1	60, 70	1mW	180mW	24/26	24/26	2-65
4 Meg x 4	FPM, 2KR, S	MT4LC4M4B1 S	60, 70	0.3mW	180mW	24/26	24/26	2-65
16 Meg x 4	FPM, 8KR	MT4LC16M4A7	50, 60, 70	1mW	165mW	34	34	2-79
16 Meg x 4	FPM, 4KR	MT4LC16M4T8	50, 60, 70	1mW	225mW	34	34	2-79
2 Meg x 8	FPM, 2KR	MT4LC2M8B1	60, 70	1mW	200mW	28	28	2-91
2 Meg x 8	FPM, 2KR, S	MT4LC2M8B1 S	60, 70	0.3mW	200mW	28	28	2-91
8 Meg x 8	FPM, 8KR	MT4LC8M8E1	50, 60, 70	1mW	170mW	34	34	2-105
8 Meg x 8	FPM, 4KR	MT4LC8M8B6	50, 60, 70	1mW	230mW	34	34	2-105
256K x 16	FPM, DC	MT4LC16257	60, 70, 80	3mW	150mW	40	40/44	2-131
256K x 16	FPM, DC, S	MT4LC16257 S	60, 70, 80	0.3mW	150mW	40	40/44	2-131
1 Meg x 16	FPM, DC, 1KR	MT4LC1M16C3	60, 70	3mW	250mW	–	44/50	2-163
1 Meg x 16	FPM, DC, 1KR, S	MT4LC1M16C3 S	60, 70	0.3mW	250mW	–	44/50	2-163
5V FPM DRAMs								
4 Meg x 1	FPM	MT4C1004J	60, 70	3mW	225mW	20/26	20/26	2-1
4 Meg x 1	FPM, S	MT4C1004J S	60, 70	0.8mW	225mW	20/26	20/26	2-1
1 Meg x 4	FPM	MT4C4001J	60, 70	3mW	225mW	20/26	20/26	2-15
1 Meg x 4	FPM, S	MT4C4001J S	60, 70	0.8mW	225mW	20/26	20/26	2-15
1 Meg x 4	FPM, QC	MT4C4004J	60, 70	3mW	225mW	24/26	–	2-41
4 Meg x 4	FPM, 2KR	MT4C4M4B1	60, 70	3mW	250mW	24/26	24/26	2-53
256K x 16	FPM, DC	MT4C16257	60, 70, 80	3mW	375mW	40	40/44	2-117
1 Meg x 16	FPM, DC, 1KR	MT4C1M16C3	60, 70	1mW	350mW	42	–	2-147

FPM = FAST PAGE MODE, DC = Dual CAS, QC = Quad CAS, 1KR = 1,024 Refresh, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, 8KR = 8,192 Refresh, S = SELF REFRESH

SGRAM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Speed Grade (ns)	Power Dissipation		No. of Pins	Page
				Standby	Active	TQFP	
256K x 32	3.3V	MT41LC256K32D4	10, 12, 15	TBD	TBD	100	3-1
256K x 32	3.3V	MT41LC256K32D4 S	10, 12, 15	TBD	TBD	100	3-1

S = SELF REFRESH

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DRAM SIMM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Optional Access Cycle	Access Time (ns)	Typical Power Dissipation		No. of Pins	Page
					Standby	Active	SIMM	
3.3V SIMMs								
1 Meg x 32	3.3V	MT8LD(T)132		60, 70, 80	9.6mW	800mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 S	S	60, 70, 80	2.4mW	800mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 X	EDO	60, 70, 80	8mW	920mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 XS	EDO, S	60, 70, 80	2mW	920mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232		60, 70, 80	19.2mW	810mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 S	S	60, 70, 80	4.8mW	802mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 X	EDO	60, 70, 80	16mW	928mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 XS	EDO, S	60, 70, 80	4mW	922mW	72	4-77
2 Meg x 32	3.3V	MT4LD232		60, 70	4mW	800mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 S	S	60, 70	1.2mW	800mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 X	EDO	60, 70	4mW	600mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 XS	EDO, S	60, 70	1.2mW	600mW	72	4-99
4 Meg x 32	3.3V	MT8LD432		60, 70	8mW	1,440mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 S	S	60, 70	2.4mW	1,440mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 X	EDO	60, 70	8mW	1,200mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 XS	EDO, S	60, 70	3.2mW	1,200mW	72	4-133
8 Meg x 32	3.3V	MT16LD832		60, 70	16mW	1,408mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 S	S	60, 70	4.8mW	1,442mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 X	EDO	60, 70	16mW	1,208mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 XS	EDO, S	60, 70	6.4mW	1,203mW	72	4-133
5V SIMMs								
1 Meg x 8	5V	MT2D18		60, 70	6mW	450mW	30	4-1
4 Meg x 8	5V	MT2D48		60, 70	6mW	500mW	30	4-11
4 Meg x 8	5V	MT8D48		60, 70	24mW	1,800mW	30	4-21
4 Meg x 9	5V	MT3D49		60, 70	9mW	725mW	30	4-31
4 Meg x 9	5V	MT9D49		60, 70	27mW	2,025mW	30	4-41
256K x 32	5V	MT2D25632		60, 70	6mW	750mW	72	4-51
512K x 32	5V	MT4D51232		60, 70	12mW	756mW	72	4-51
1 Meg x 32	5V	MT8D132		60, 70	24mW	1,800mW	72	4-63
1 Meg x 32	5V	MT8D132 S	S	60, 70	24mW	1,800mW	72	4-63
2 Meg x 32	5V	MT16D232		60, 70	48mW	1,824mW	72	4-63
2 Meg x 32	5V	MT16D232 S	S	60, 70	48mW	1,824mW	72	4-63
4 Meg x 32	5V	MT8D432		60, 70	24mW	2,000mW	72	4-119
4 Meg x 32	5V	MT8D432 S	S	60, 70	2.4mW	1,440mW	72	4-119
8 Meg x 32	5V	MT16D832		60, 70	48mW	2,024mW	72	4-119
8 Meg x 32	5V	MT16D832 S	S	60, 70	4.8mW	1,443mW	72	4-119
1 Meg x 36	5V	MT9D136		60, 70	27mW	2,025mW	72	4-155
2 Meg x 36	5V	MT18D236		60, 70	54mW	2,052mW	72	4-155
4 Meg x 36	5V	MT12D436		60, 70	36mW	2,500mW	72	4-167
4 Meg x 36	5V	MT12D436 S	S	60, 70	3.6mW	2,340mW	72	4-167
8 Meg x 36	5V	MT24D836		60, 70	72mW	2,536mW	72	4-167
8 Meg x 36	5V	MT24D836 S	S	60, 70	7.2mW	2,348mW	72	4-167

S = SELF REFRESH; EDO = Extended Data-Out

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DRAM DIMM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Optional Access Cycle	Access Time (ns)	Typical Power Dissipation		No. of Pins	Page
					Standby	Active	DIMM	
3.3V DIMMs								
1 Meg x 32	3.3V	MT2LD(T)132H		60, 70	6mW	500mW	72	5-1
1 Meg x 32	3.3V	MT2LD(T)132H S	S	60, 70	.6mW	500mW	72	5-1
2 Meg x 32	3.3V	MT4LD(T)232H		60, 70	12mW	506mW	72	5-1
2 Meg x 32	3.3V	MT4LD(T)232H S	S	60, 70	1.2mW	501mW	72	5-1
4 Meg x 32	3.3V	MT8LD(T)432H		60, 70	8mW	1,440mW	72	5-15
4 Meg x 32	3.3V	MT8LD(T)432H S	S	60, 70	2.4mW	1,440mW	72	5-15
1 Meg x 64	3.3V	MT16LD(T)164		60, 70	19.2mW	1,600mW	168	5-47
1 Meg x 64	3.3V	MT16LD(T)164 S	S	60, 70	4.8mW	1,600mW	168	5-47
2 Meg x 64	3.3V	MT8LD(T)264		60, 70	8mW	1,600mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 S	S	60, 70	2.4mW	1,600mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 X	EDO	60, 70	8mW	1,200mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 XS	EDO, S	60, 70	2.4mW	1,200mW	168	5-69
4 Meg x 64	3.3V	MT16LD(T)464		60, 70	16mW	2,880mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 S	S	60, 70	4.8mW	2,880mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 X	EDO	60, 70	16mW	2,400mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 XS	EDO, S	60, 70	6.4mW	2,400mW	168	5-47
1 Meg x 72	3.3V	MT18LD(T)172		60, 70	21.6mW	1,800mW	168	5-109
1 Meg x 72	3.3V	MT18LD(T)172 S	S	60, 70	5.4mW	1,800mW	168	5-109
2 Meg x 72	3.3V	MT9LD(T)272		60, 70	9mW	1,800mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 S	S	60, 70	2.7mW	1,800mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 X	EDO	60, 70	9mW	1,350mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 XS	EDO, S	60, 70	2.7mW	1,350mW	168	5-131
4 Meg x 72	3.3V	MT18LD(T)472		60, 70	18mW	3,240mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 S	S	60, 70	5.4mW	3,240mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 X	EDO	60, 70	18mW	2,700mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 XS	EDO, S	60, 70	5.4mW	2,700mW	168	5-109
5V DIMMs								
1 Meg x 64	5V	MT16D(T)164		60, 70	48mW	3,600mW	168	5-29
1 Meg x 64	5V	MT16D(T)164 S	S	60, 70	12.8mW	3,600mW	168	5-29
4 Meg x 64	5V	MT16D(T)464		60, 70	48mW	4,000mW	168	5-29
1 Meg x 72	5V	MT18D(T)172		60, 70	54mW	4,050mW	168	5-91
1 Meg x 72	5V	MT18D(T)172 S	S	60, 70	14.4mW	4,050mW	168	5-91
4 Meg x 72	5V	MT18D(T)472		60, 70	54mW	4,500mW	168	5-91

EDO = Extended Data-Out; S = SELF REFRESH

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DRAM CARD PRODUCT SELECTION GUIDE

Memory Configuration			Part Number	Access Time (ns)	Number of Pins Card	Page
3.3V DRAM Cards						
1 Meg x 32	3.3V	4 Megabytes	MT8D88C132V(S)	60, 70, 80	88	6-33
1 Meg x 32	3.3V	4 Megabytes	MT8D88C132VH(S)	60, 70, 80	88	6-49
2 Meg x 32	3.3V	8 Megabytes	MT16D88C232V(S)	60, 70, 80	88	6-33
2 Meg x 32	3.3V	8 Megabytes	MT16D88C232VH(S)	60, 70, 80	88	6-49
4 Meg x 32	3.3V	16 Megabytes	MT8D88C432V(S)	60, 70, 80	88	6-33
4 Meg x 32	3.3V	16 Megabytes	MT8D88C432VH(S)	60, 70, 80	88	6-49
8 Meg x 32	3.3V	32 Megabytes	MT16D88C832V(S)	60, 70, 80	88	6-33
8 Meg x 32	3.3V	32 Megabytes	MT16D88C832VH(S)	60, 70, 80	88	6-49
5V DRAM Cards						
1 Meg x 32	5V	4 Megabytes	MT8D88C132(S)	60, 70	88	6-1
1 Meg x 32	5V	4 Megabytes	MT8D88C132H(S)	60, 70	88	6-17
2 Meg x 32	5V	8 Megabytes	MT16D88C232(S)	60, 70	88	6-1
2 Meg x 32	5V	8 Megabytes	MT16D88C232H(S)	60, 70	88	6-17

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EDO DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/No. of Pins		Page
				Standby	Active	SOJ	TSOP	
3.3V EDO DRAMs								
1 Meg x 4	EDO	MT4LC4007J	60, 70, 80	1mW	115mW	20/26	-	1-15
1 Meg x 4	EDO, S	MT4LC4007J S	60, 70, 80	0.25mW	115mW	20/26	-	1-15
4 Meg x 4	EDO, 2KR	MT4LC4M4E8	60, 70	1mW	150mW	24/26	24/26	1-31
4 Meg x 4	EDO, 2KR, S	MT4LC4M4E8 S	60, 70	0.4mW	150mW	24/26	24/26	1-31
16 Meg x 4	EDO, 8KR	MT4LC16M4G3	50, 60, 70	1mW	165mW	34	34	1-47
16 Meg x 4	EDO, 4KR	MT4LC16M4H9	50, 60, 70	1mW	165mW	34	34	1-47
2 Meg x 8	EDO, 2KR	MT4LC2M8E7	60, 70	1mW	150mW	28	28	1-63
2 Meg x 8	EDO, 2KR, S	MT4LC2M8E7 S	60, 70	0.3mW	150mW	28	28	1-63
8 Meg x 8	EDO, 8KR	MT4LC8M8P4	50, 60, 70	1mW	170mW	34	34	1-77
8 Meg x 8	EDO, 4KR	MT4LC8M8C2	50, 60, 70	1mW	170mW	34	34	1-77
256K x 16	EDO, DC	MT4LC16270	60, 70, 80	1mW	85mW	40	40/44	1-107
1 Meg x 16	EDO, DC, 1KR	MT4LC1M16E5	60, 70	0.9mW	180mW	-	44/50	1-123
1 Meg x 16	EDO, DC, 1KR, S	MT4LC1M16E5 S	60, 70	0.3mW	180mW	-	44/50	1-123
5V EDO DRAMs								
1 Meg x 4	EDO	MT4C4007J	60, 70	3mW	175mW	20/26	-	1-1
1 Meg x 4	EDO, S	MT4C4007J S	60, 70	0.8mW	175mW	20/26	-	1-1
256K x 16	EDO, DC	MT4C16270	60, 70, 80	3mW	300mW	40	40/44	1-91

EDO = Extended Data-Out, DC = Dual CAS, 1KR = 1,024 Refresh, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, 8KR = 8,192 Refresh, S = SELF REFRESH

DRAM

1 MEG x 4 DRAM

5V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Single +5V ±10% power supply
- JEDEC-standard pinout and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- Extended Data-Out (EDO) PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- EDO PAGE MODE cycle times, 25-35ns

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (300 mil)	DJ

- Part Number Example: MT4C4007JDJ-7

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-6	110ns	60ns	25ns	30ns	18ns	10ns
-7	130ns	70ns	33ns	35ns	22ns	15ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1)

Pin	No.	No.	Pin
DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{WE}$	3	24	DQ3
$\overline{RAS}$	4	23	$\overline{CAS}$
A9	5	22	$\overline{OE}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

GENERAL DESCRIPTION

The MT4C4007J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration with optional SELF REFRESH. During READ or WRITE cycles, each of the 4 memory bits (1 bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ latches the first 10 bits and $\overline{CAS}$ latches the latter 10 bits.

A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last, however, only EARLY WRITE cycles are supported. LATE WRITE cycles should not be attempted as the results are not predictable. When $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW (EARLY WRITE cycle), the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

PAGE ACCESS

PAGE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

The PAGE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates PAGE operation.

EDO PAGE MODE

The MT4C4007J provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^{t}CP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO

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EDO PAGE MODE (continued)

operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ^{t}OEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ^{t}OEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 1 for further detail on the toggling OE condition). During cycles other than PAGE-MODE READ, the outputs are disabled at ^{t}OFF time after RAS and CAS are HIGH, or ^{t}WHZ after WE transitions LOW. The ^{t}OFF time is referenced from the rising edge of RAS or CAS, whichever occurs last. WE can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 2.

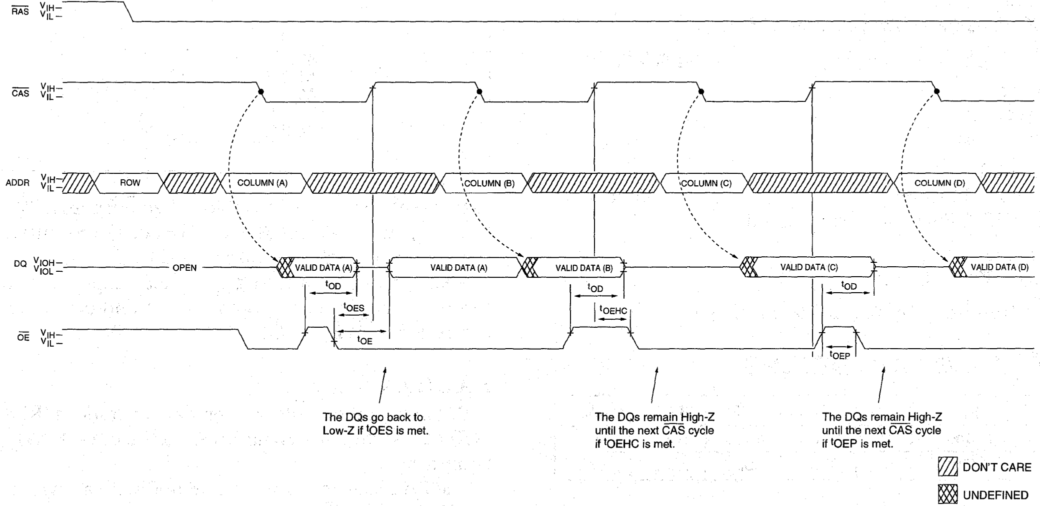

Figure 1
OUTPUT ENABLE AND DISABLE

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REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed within ᵗREF max, regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4C4007J S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" version allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ᵗRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS HIGH time.

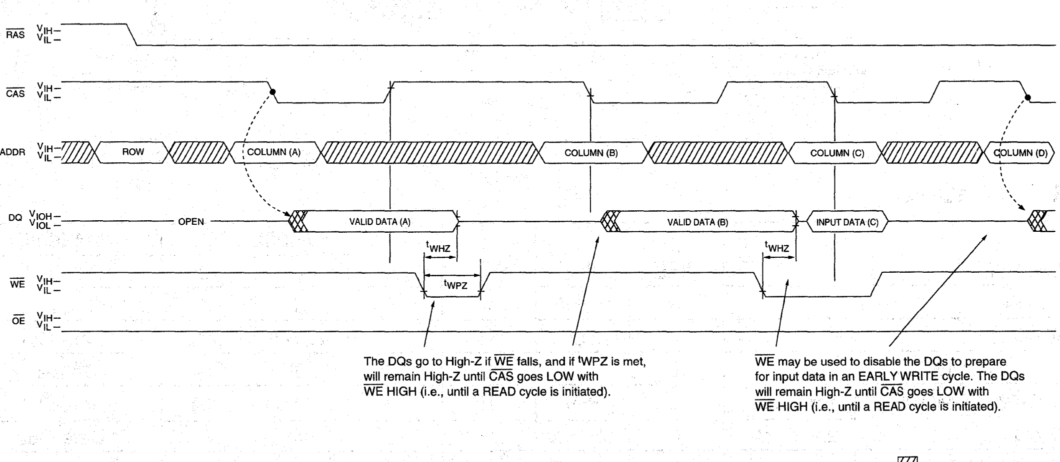

Figure 2
OUTPUT ENABLE AND DISABLE USING WE

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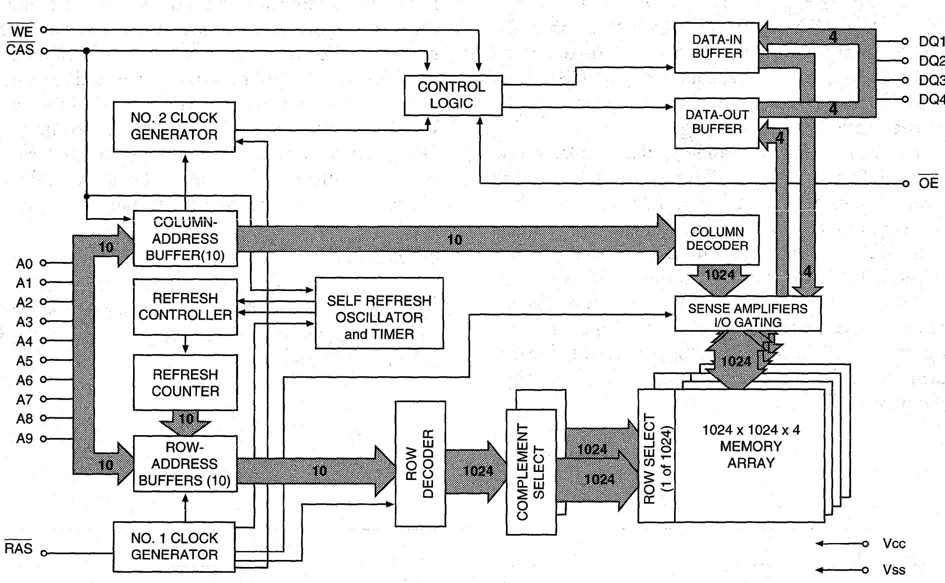
FUNCTIONAL BLOCK DIAGRAM
EDO PAGE MODE



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)		II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)		IOZ	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (IOUT = -5mA)	VOH	2.4		V	
	Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	µA	
	I_{CC2} (S only)	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, address cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	110	100	mA	3, 4, 30
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = V_{IL}, CAS, address cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: RAS ONLY Average power supply current (RAS cycling, CAS = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	110	100	mA	3, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, address cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: CAS = 0.2V or CBR cycling; RAS = ${}^tRAS$ (MIN); WE= Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with ${}^tRAS \geq {}^tRASS$ (MIN) and CAS held LOW; WE = V_{CC} -0.2; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address setup to $\overline{CAS}$ precharge during WRITE	^tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		18		22	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	10	10,000	15	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	10		10		ns	28
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ hold time	^tCSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		13		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD		15		20	ns	26
Output Enable time	^tOE		15		20	ns	23
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	25		33		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH cycle	tRASS	100		100		µs	28
Random READ or WRITE cycle time	tRC	110		130		ns	
RAS to CAS delay time	tRCD	20	45	20	50	ns	17
Read command hold time (referenced to CAS)	tRCH	0		0		ns	19
Read command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (1,024 cycles) S version	tREF		128		128	ms	
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
RAS precharge time during SELF REFRESH cycle	tRPS	110		130		ns	28
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	15		20		ns	
Write command to RAS lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	2	50	2	50	ns	9, 10
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
WE command setup time	tWCS	0		0		ns	21, 26
Output disable delay from WE (CAS HIGH)	tWHZ	3	15	3	20	ns	
Write command pulse width	tWP	10		15		ns	
WE pulse width for output disable when CAS HIGH	tWPZ	10		10		ns	
WE hold time (CBR REFRESH)	tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		ns	25

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +5V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. If the cycle is a READ-MODIFY-WRITE, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
23. Even if $\overline{OE}$ is HIGH, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
26. The DQs open during READ cycles once ^tOD or ^tOFF occur.
27. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
29. Column-address changed once each cycle.

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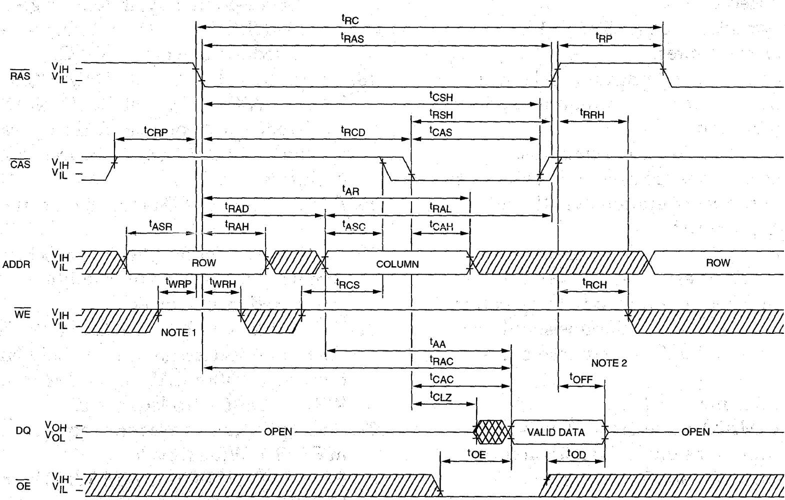
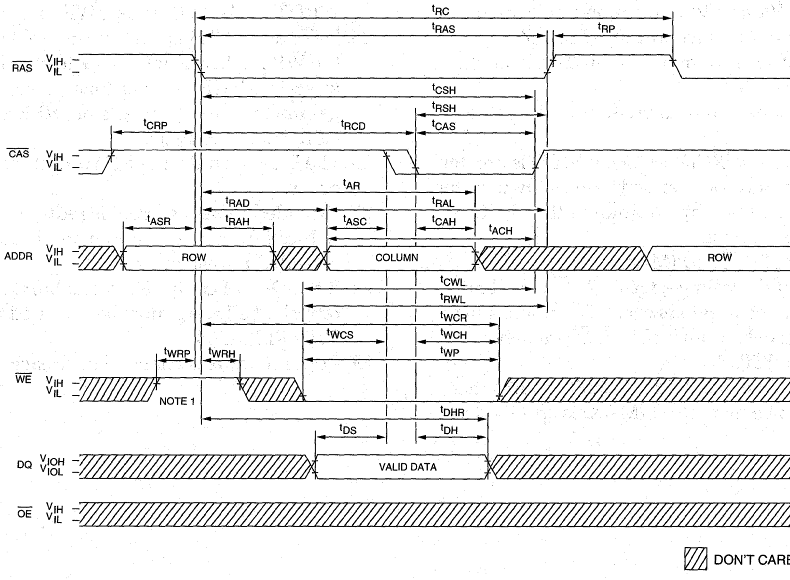
NEW EDO DRAM

READ CYCLE



EARLY WRITE CYCLE



NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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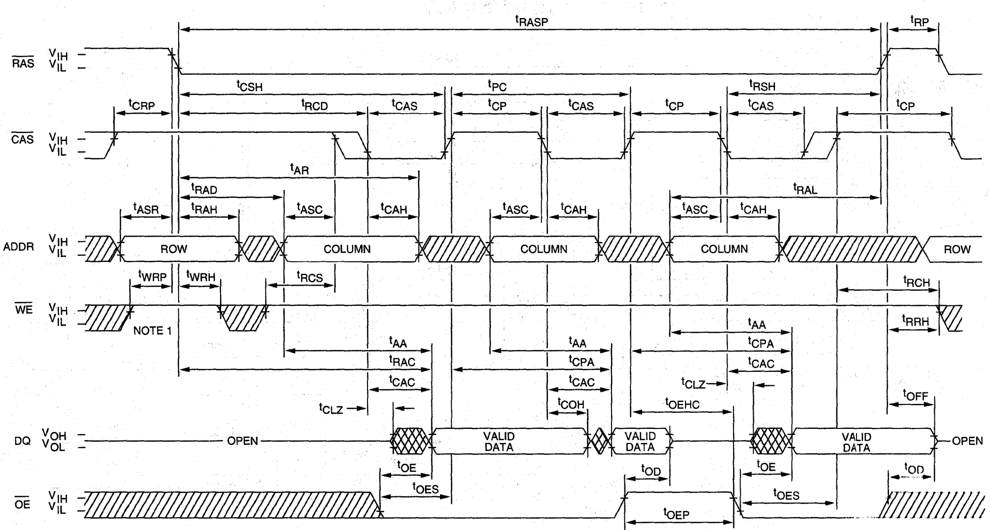
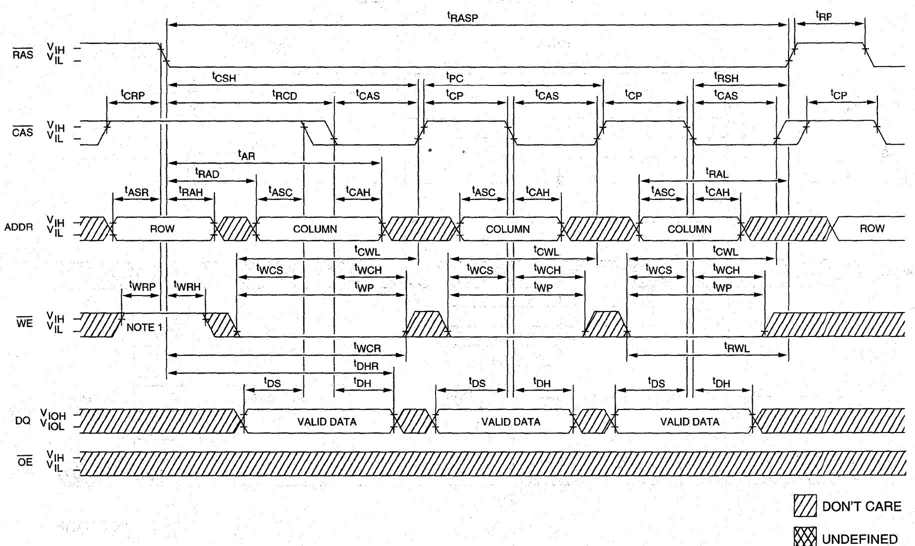
EDO-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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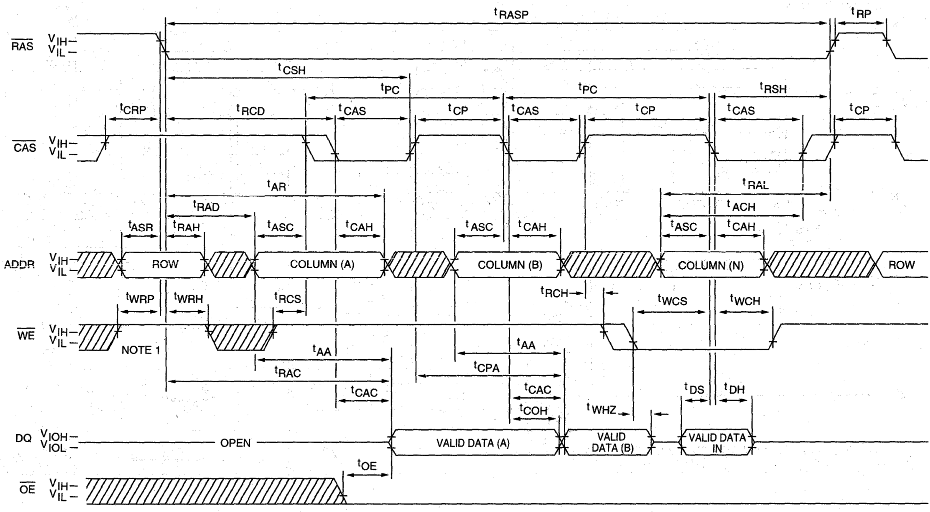
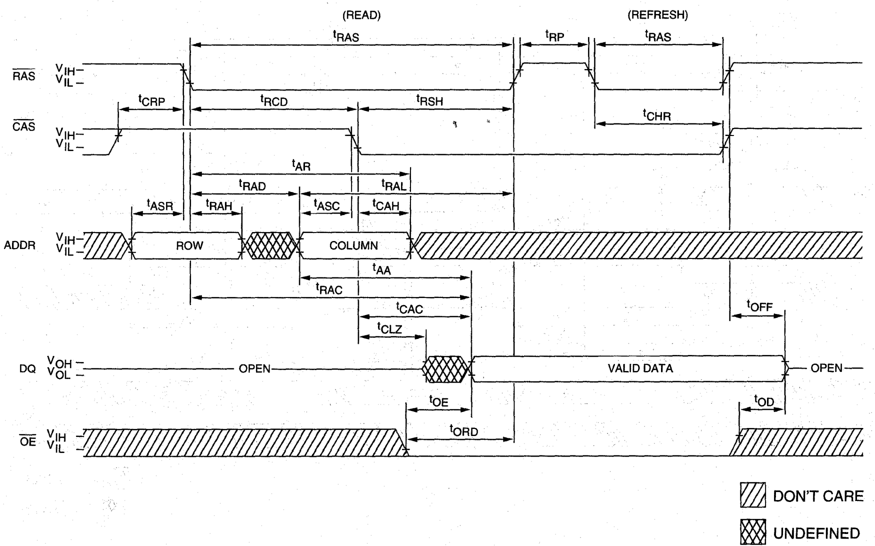
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



HIDDEN REFRESH CYCLE 24
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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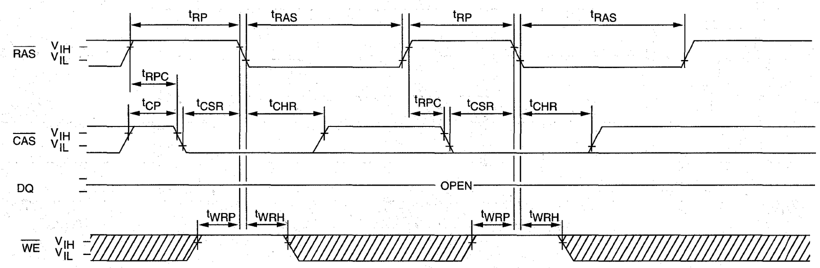
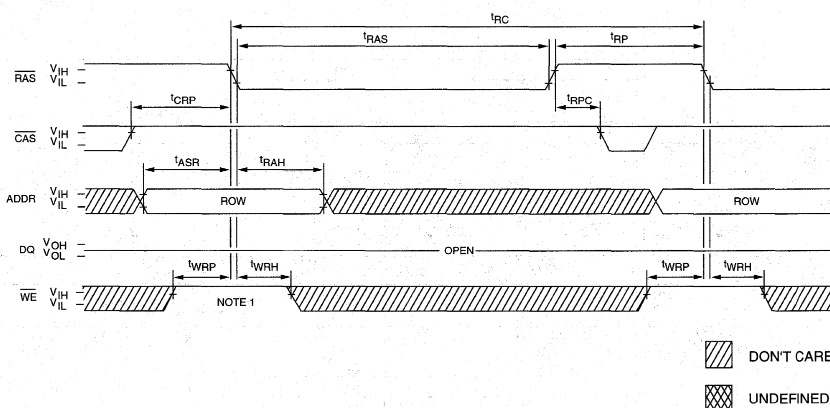
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



$\overline{RAS}$-ONLY REFRESH CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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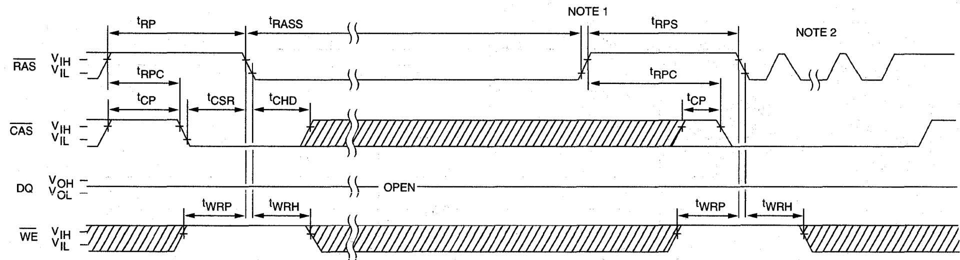
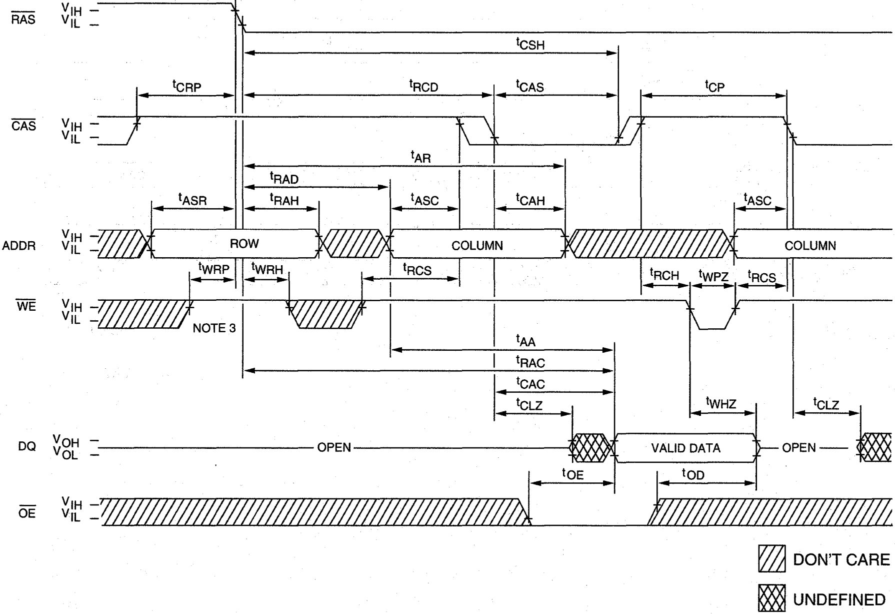
SELF REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



READ CYCLE

(with $\overline{WE}$-controlled disable)



NOTE:
1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.
3. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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1 MEG x 4 DRAM

3.3V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Single +3.3V ±0.3V power supply
- Low power, 0.25mW standby; 115mW active, typical
- JEDEC-standard pinout and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- Extended Data-Out (EDO) PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- Low SELF REFRESH current, 100µA typical, 150µA (MAX)
- EDO PAGE MODE cycle times, 25-35ns

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG

- Part Number Example: MT4LC4007JDJ-7 S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	25ns	30ns	18ns	10ns
-7	130ns	70ns	30ns	35ns	22ns	12ns
-8	150ns	80ns	33ns	40ns	22ns	12ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ
(DA-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{\text{WE}}$	3	24	DQ3
$\overline{\text{RAS}}$	4	23	$\overline{\text{CAS}}$
A9	5	22	$\overline{\text{OE}}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

GENERAL DESCRIPTION

The MT4LC4007J(S) is specially designed to operate from 3.0V to 3.6V for low-voltage memory systems. It is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration with optional SELF REFRESH. During READ or WRITE cycles, each of the 4 memory bits (1 bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{\text{RAS}}$ latches the first 10 bits and $\overline{\text{CAS}}$ latches the latter 10 bits.

A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pins remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle, which is an EARLY WRITE cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary.

The PAGE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates PAGE operation.

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EDO PAGE MODE

The MT4LC4007J provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ^tOEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ^tOEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 1 for further detail on the toggling OE condition). During cycles other than PAGE-MODE READ, the outputs are disabled at ^tOFF time after RAS and CAS are HIGH, or ^tWHZ after WE transitions LOW. The ^tOFF time is referenced from the rising edge of RAS or CAS, whichever occurs last. WE can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 2.

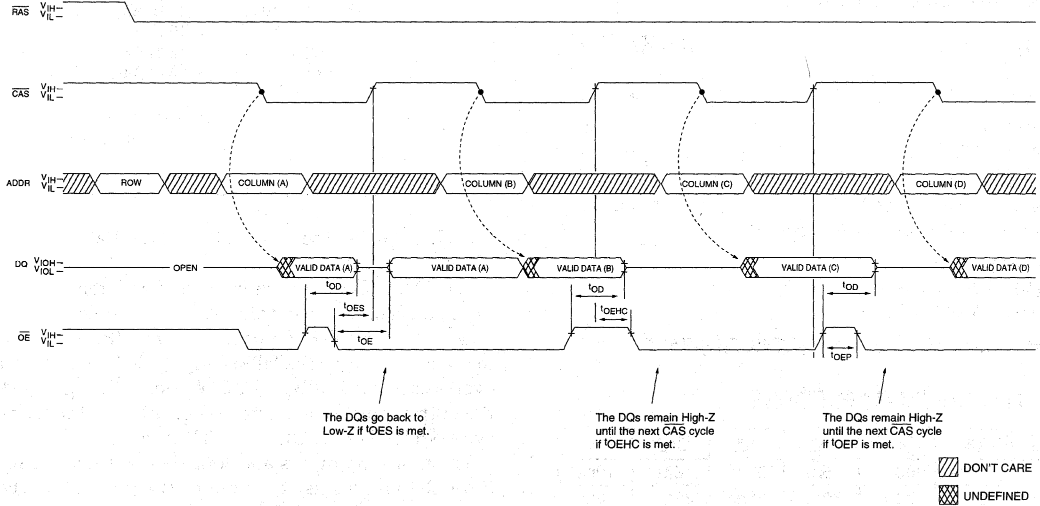

Figure 1
OUTPUT ENABLE AND DISABLE

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REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed within ^{t}REF max, regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC4007J S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS HIGH time.

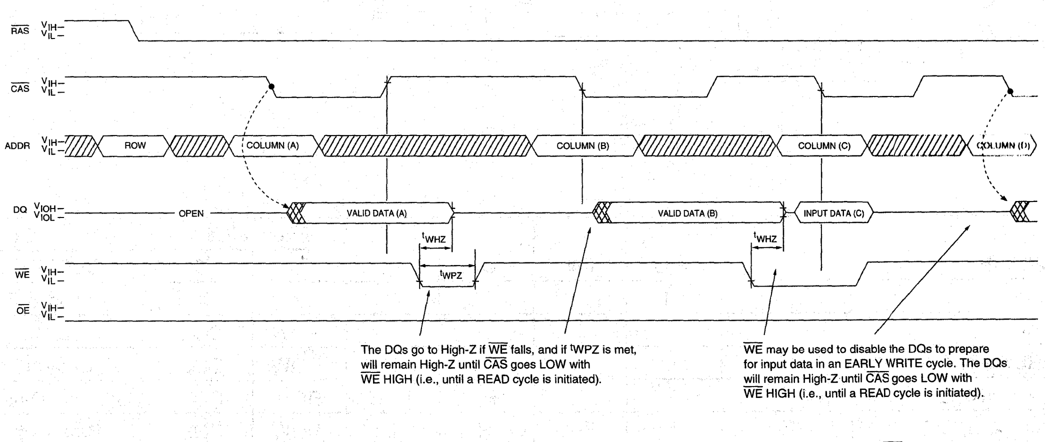

Figure 2
OUTPUT ENABLE AND DISABLE USING WE

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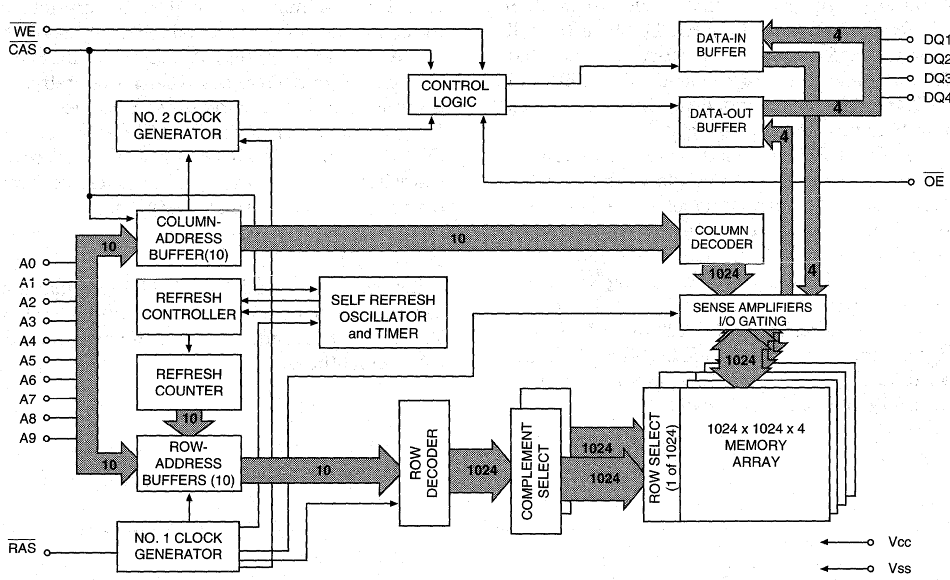
FUNCTIONAL BLOCK DIAGRAM
EDO PAGE MODE



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC}+0.5V (All other pins not under test = 0V)		I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC}+0.5V)		I_{OZ}	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
	Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYM	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	1	mA
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	500	µA	
	I_{CC2} (S only)	100	100	100	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	80	70	60	mA	3, 4, 30
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	60	50	40	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	80	70	60	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	80	70	60	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= Vcc -0.2V; A0-A9, $\overline{OE}$, and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	150	150	150	µA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2; A0-A9,$\overline{OE}$, and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	150	150	150	µA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35		40	ns	
Column-address setup to CAS precharge during WRITE	tACH	15		15		20		ns	
Column-address hold time (referenced to RAS)	tAR	45		50		55		ns	
Column-address setup time	tASC	0		0		0		ns	
Row-address setup time	tASR	0		0		0		ns	
Column-address to WE delay time	tAWD	55		65		70		ns	21
Access time from CAS	tCAC		18		22		22	ns	15
Column-address hold time	tCAH	10		15		15		ns	
CAS pulse width	tCAS	10	10,000	15	10,000	15	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	10		10		10		ns	29
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	5
CAS to output in Low-Z	tCLZ	3		3		3		ns	
Data output hold after CAS LOW	tCOH	5		5		5		ns	
CAS precharge time	tCP	10		10		10		ns	16
Access time from CAS precharge	tCPA		35		40		45	ns	
CAS to RAS precharge time	tCRP	10		10		10		ns	
CAS hold time	tCSH	50		55		65		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
CAS to WE delay time	tCWD	40		50		50		ns	21
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in hold time	tDH	10		15		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Data-in setup time	tDS	0		0		0		ns	22
Output disable	tOD		15		20		20	ns	27
Output Enable time	tOE		15		20		20	ns	23
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	26
OE HIGH hold time from CAS HIGH	tOEHC	10		10		10		ns	
OE HIGH pulse width	tOEP	10		10		10		ns	
OE LOW to CAS HIGH setup time	tOES	5		5		5		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		33		35		ns	
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	85		100		105		ns	
Access time from RAS	tRAC		60		70		80	ns	14
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Row-address hold time	tRAH	10		10		10		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS pulse width (EDO PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width during SELF REFRESH cycle	^{t}RASS	100		100		100		µs	29
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
RAS to CAS delay time	^{t}RCD	20	45	20	50	20	60	ns	17
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
Refresh period (1,024 cycles) S version	^{t}REF		128		128		128	ms	
RAS precharge time	^{t}RP	40		50		60		ns	
RAS to CAS precharge time	^{t}RPC	0		0		0		ns	
RAS precharge time during SELF REFRESH cycle	^{t}RPS	110		130		150		ns	29
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
RAS hold time	^{t}RSH	15		20		20		ns	
READ WRITE cycle time	^{t}RWC	150		180		200		ns	
RAS to WE delay time	^{t}RWD	85		100		110		ns	21
Write command to RAS lead time	^{t}RWL	15		20		20		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	2	50	ns	9, 10
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	^{t}WCR	45		55		60		ns	
WE command setup time	^{t}WCS	0		0		0		ns	21, 27
Output disable delay from WE (CAS HIGH)	^{t}WHZ	3	15	3	15	3	15	ns	
Write command pulse width	^{t}WP	10		15		15		ns	
WE pulse width for output disable when CAS HIGH	^{t}WPZ	10		10		10		ns	
WE hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	25
WE setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	25

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V ±0.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
28. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
29. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
30. Column-address changed once each cycle.

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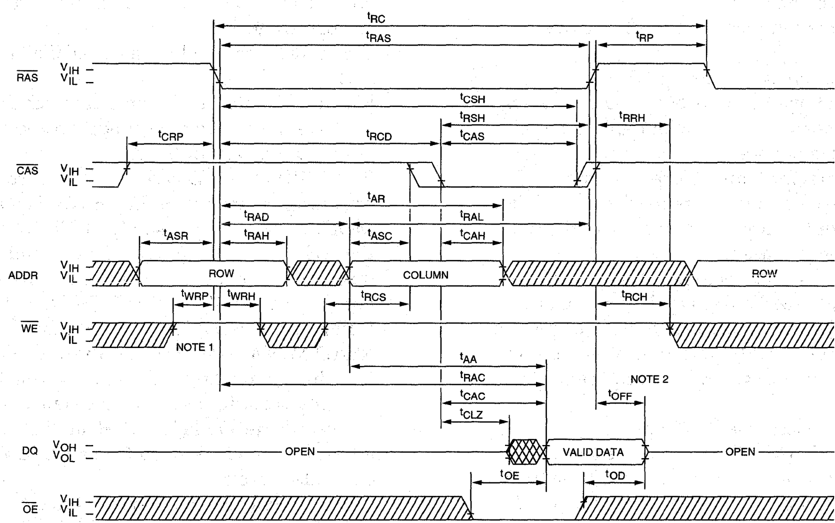
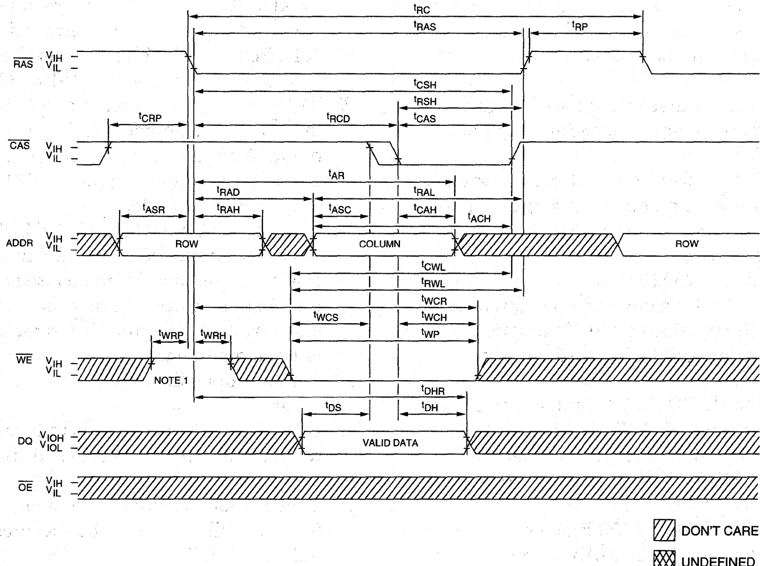
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE:

1. Although $\overline{WE}$ is a “don't care” at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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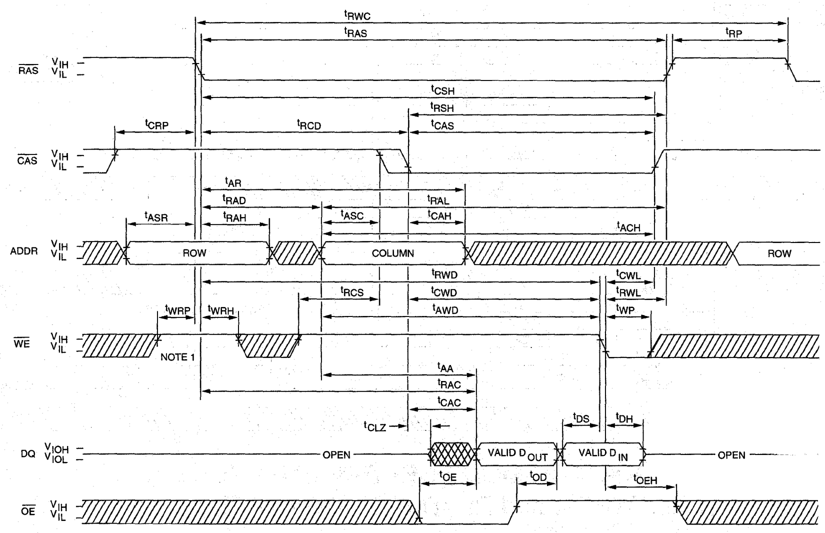
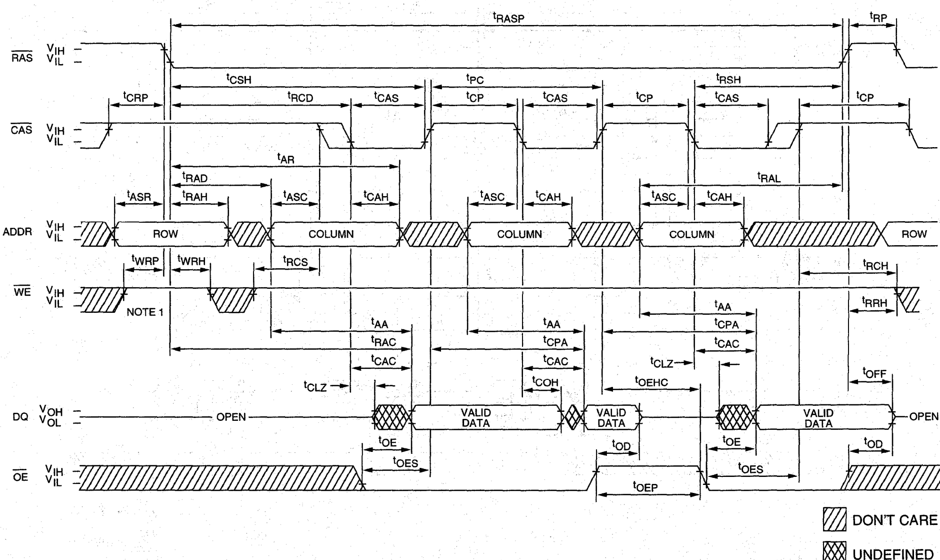
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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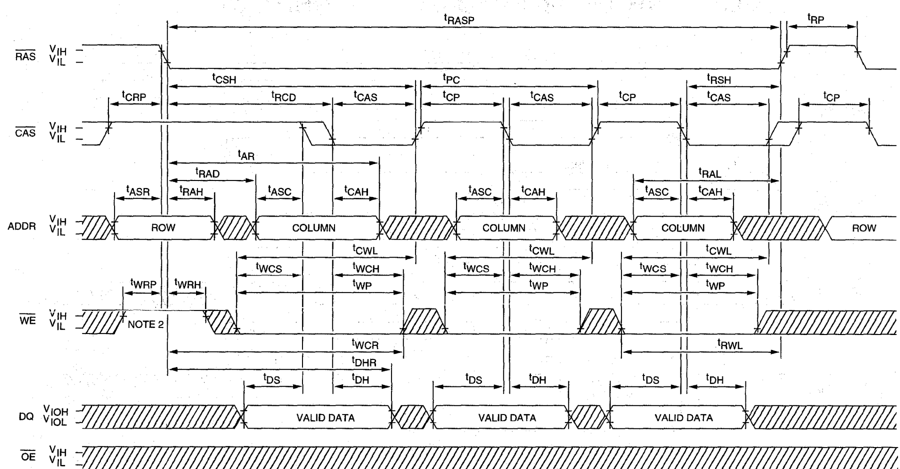
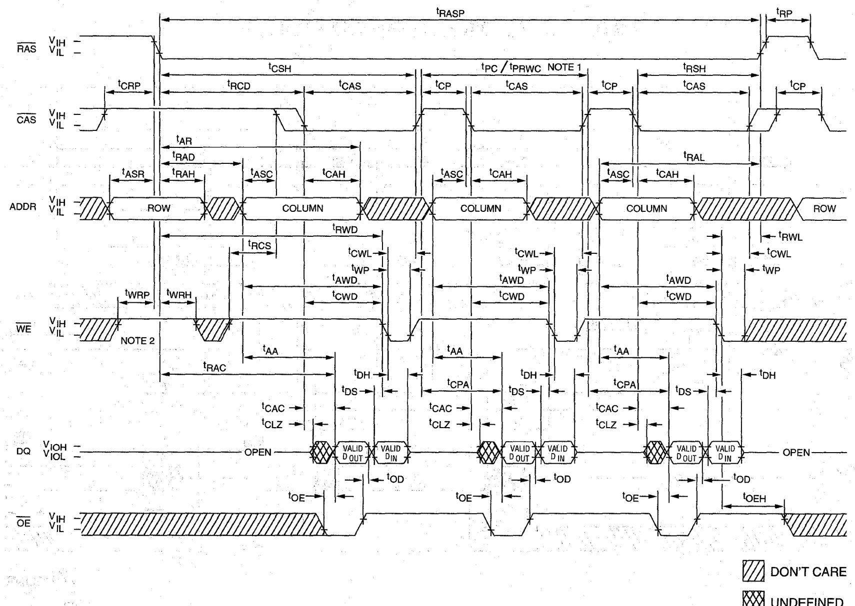
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a “don't care” at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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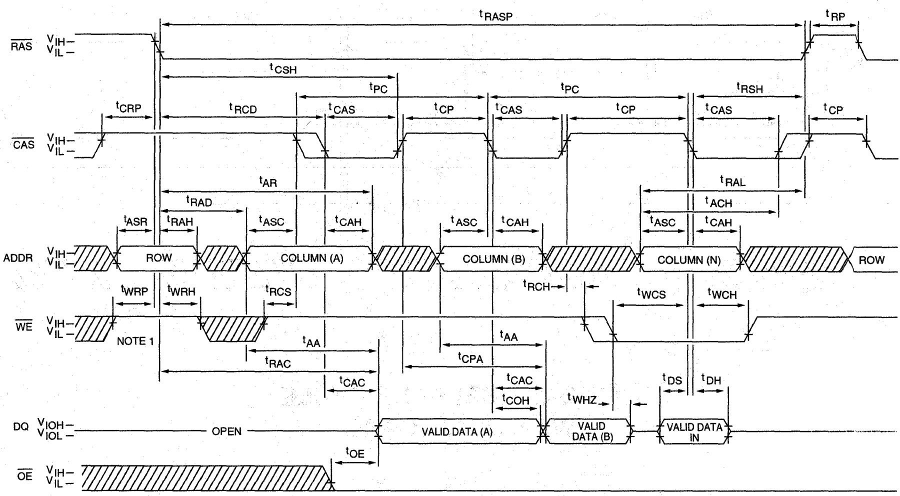
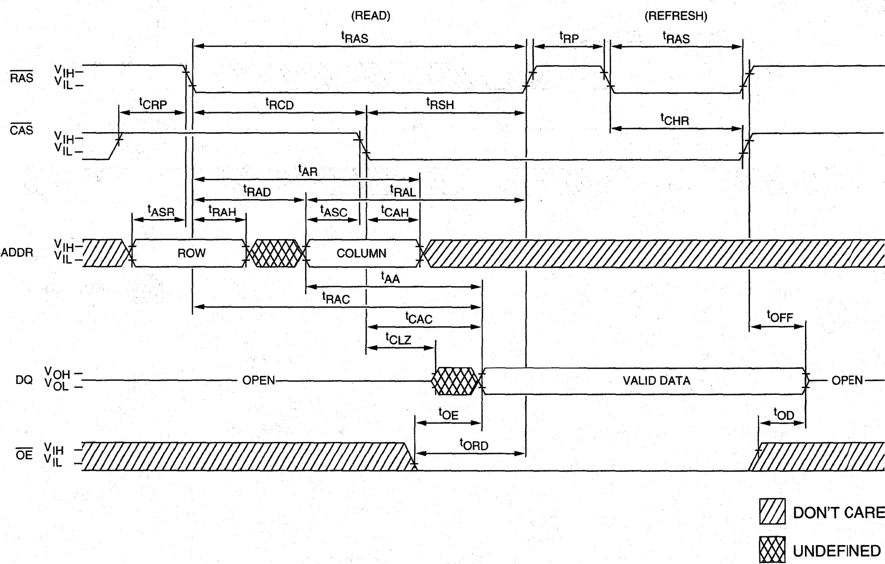
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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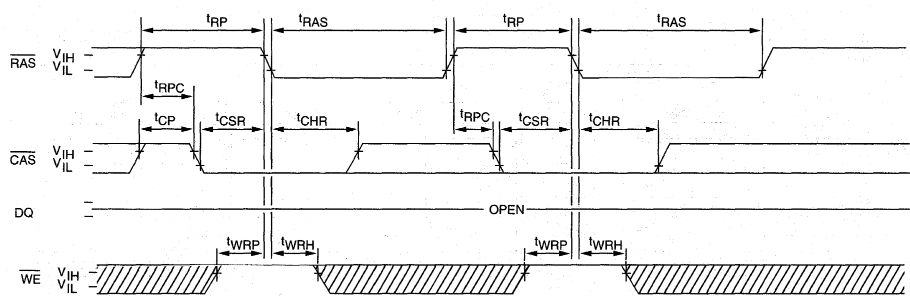
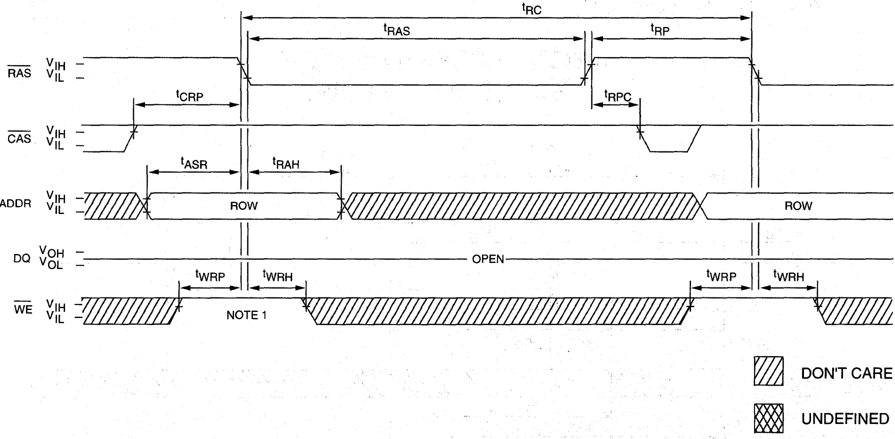
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{WE}$ = DON'T CARE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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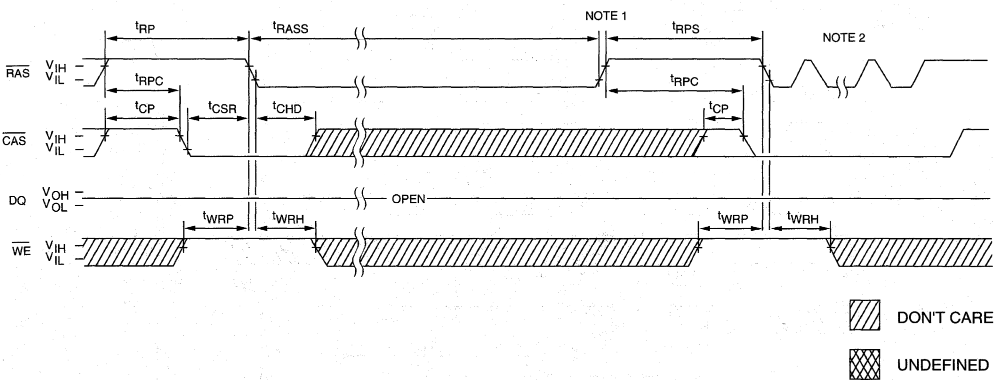
SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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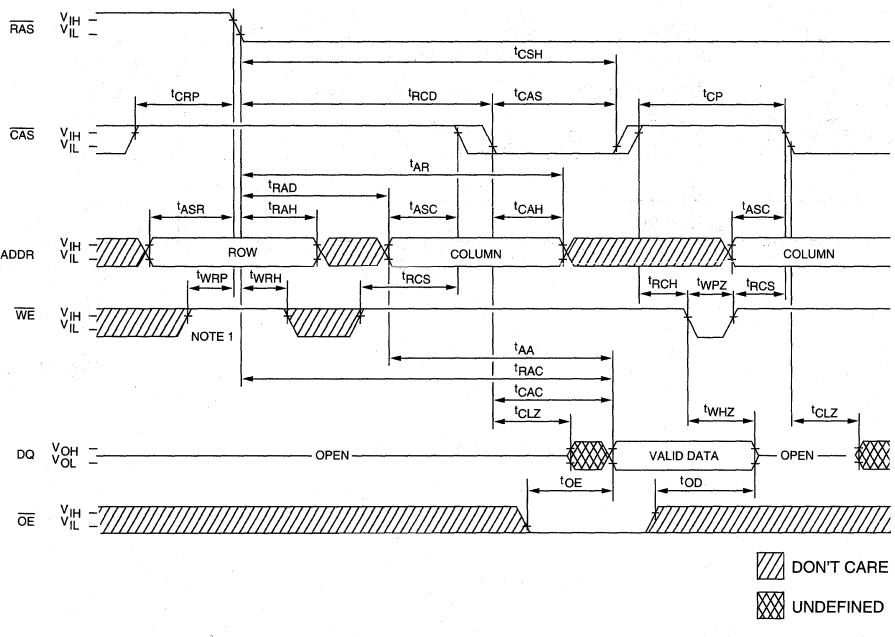
READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM

4 MEG x 4 DRAM

3.3V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- Low power, 0.4mW standby; 150mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 2,048-cycle (11 row-, 11 column-addresses)
- Optional SELF REFRESH, Extended Refresh rate (4x)
- Extended Data-Out (EDO) PAGE access cycle
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh Rate	
Standard 32ms period	None
SELF REFRESH and 128ms period	S

- Part Number Example: MT4LC4M4E8DJ-7 S

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DA-2) — 24/26-Pin TSOP (DB-2)

Pin	Name	Pin	Name
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	NC	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

GENERAL DESCRIPTION

The MT4LC4M4E8(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. The MT4LC4M4E8(S) RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High- Z) until the next CAS cycle, regardless of OE.

If WE goes LOW after CAS goes LOW, data-out (Q) is activated and retains the selected cell data as long as OE remains LOW and RAS or CAS remains LOW (regardless of WE). This late WE pulse results in a READ WRITE cycle. If WE toggles LOW after CAS goes back HIGH, the output pins will open (High- Z) until the next CAS cycle, regardless of OE.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the PAGE MODE of operation.

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EDO PAGE MODE

The MT4LC4M4E8(S) provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO allows CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control allows pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similarly to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z (refer to Figure 1). WE can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS high time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last.

REFRESH

Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC4M4E8 S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms four times longer than the standard 32ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

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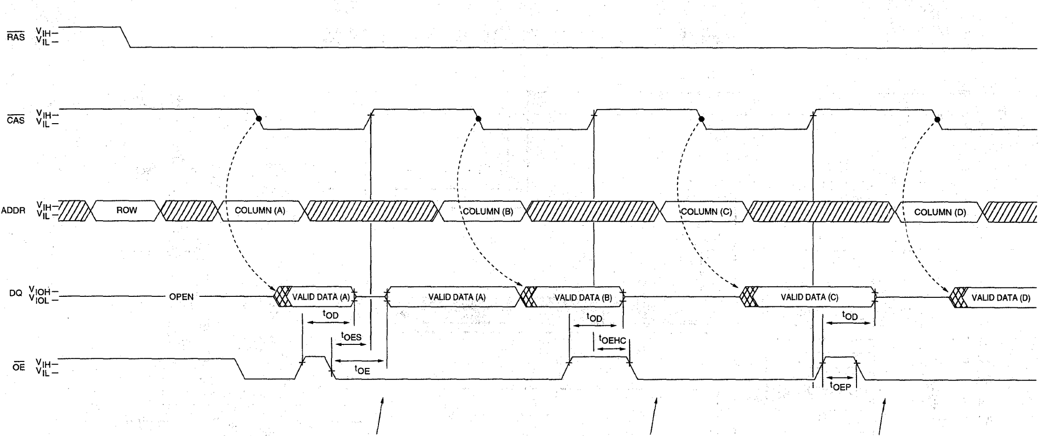

Figure 1
OUTPUT ENABLE AND DISABLE

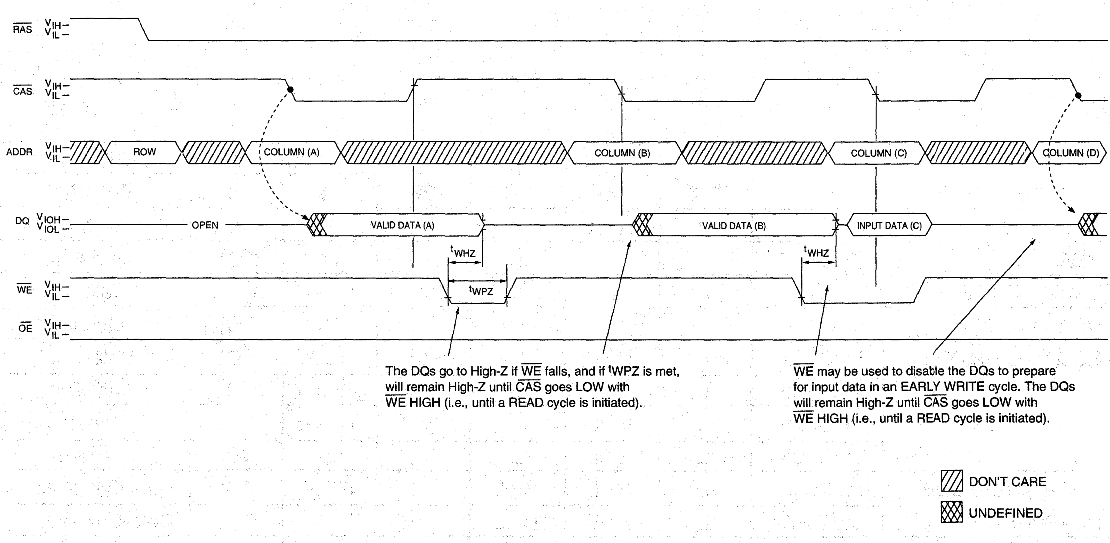

Figure 2
WE CONTROL OF DQs

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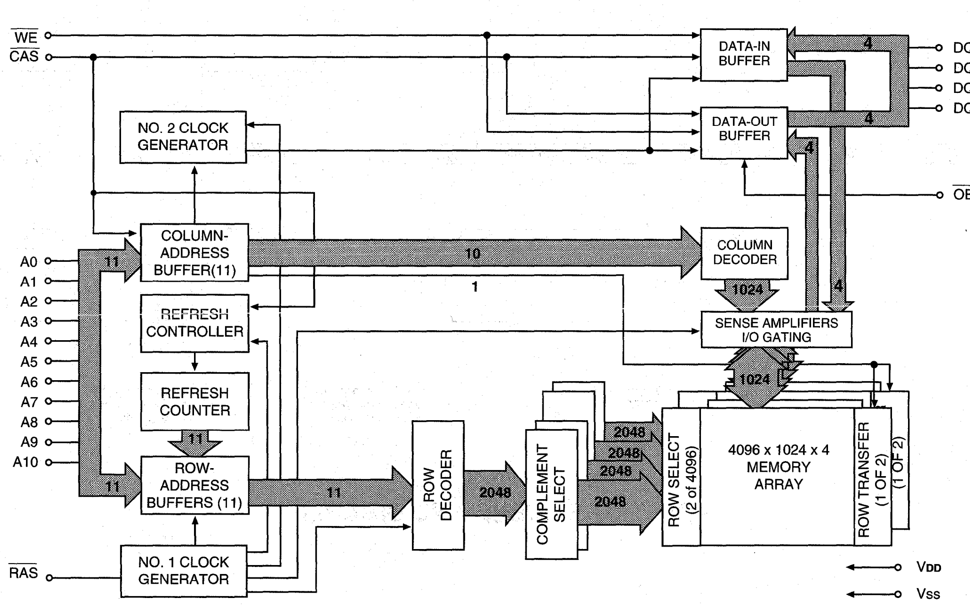
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	µA	
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	110	100	mA	3, 4, 12
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	mA	3, 12
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	120	110	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V(D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS(MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V(D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address set-up to $\overline{CAS}$ precharge during WRITE	^tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		ns	20
Access time from $\overline{CAS}$	^tCAC		15		20	ns	14
Column-address hold time	^tCAH	10		12		ns	
$\overline{CAS}$ pulse width	^tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	15		15		ns	25
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		12		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next $\overline{CAS}$ LOW	^tCOH	5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	15
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		ns	20
Write command to $\overline{CAS}$ lead time	^tCWL	15		15		ns	
Data-in hold time	^tDH	10		12		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21
Output disable	^tOD	0	15	0	15	ns	
Output Enable	^tOE		15		15	ns	22
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		12		ns	
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	^tOEHC	10		10		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{OE}$ HIGH pulse width	tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	3	15	3	15	ns	
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	75		85		ns	
Access time from $\overline{RAS}$	tRAC		60		70	ns	13
$\overline{RAS}$ to column-address delay time	tRAD	12	30	12	35	ns	17
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	tRASS	100		100		µs	25
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	14	45	14	50	ns	16
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	18
Read command setup time	tRCS	0		0		ns	
Refresh period (2,048 cycles)	tREF		32		32	ms	
Refresh period (2,048 cycles) S version	tREF		128		128	ms	
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	tRPS	110		130		ns	25
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	18
$\overline{RAS}$ hold time	tRSH	10		12		ns	
READ WRITE cycle time	tRWC	150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		ns	20
Write command to $\overline{RAS}$ lead time	tRWL	15		15		ns	
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	10		12		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	
$\overline{WE}$ command setup time	tWCS	0		0		ns	20
Output disable delay from $\overline{WE}$	tWHZ	0	13	0	15	ns	
Write command pulse width	tWP	10		12		ns	
$\overline{WE}$ pulse to disable at $\overline{CAS}$ HIGH	tWPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. Column address changed once each cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
14. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
15. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP.
16. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC, provided ^{t}RAD is not exceeded.
17. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA, provided ^{t}RCD is not exceeded.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.
20. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WCS (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
21. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
22. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{\text{WE}}$ must be pulsed during $\overline{\text{CAS}}$ HIGH time in order to place I/O buffers in High-Z.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
25. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.

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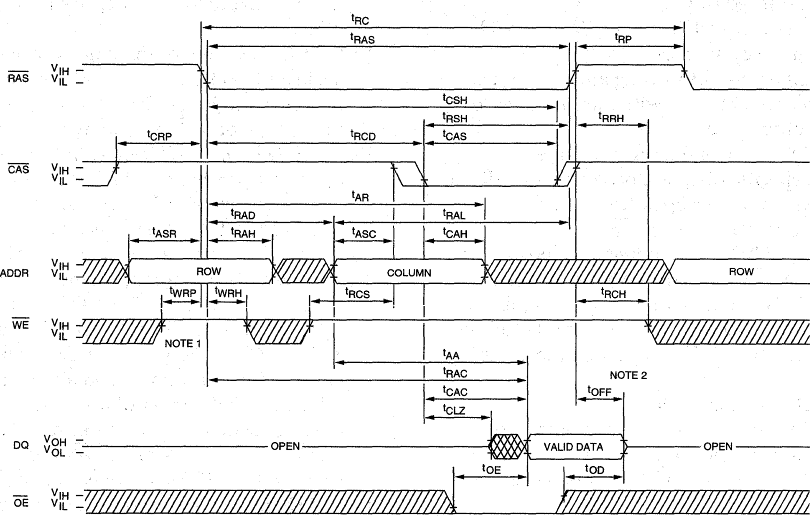
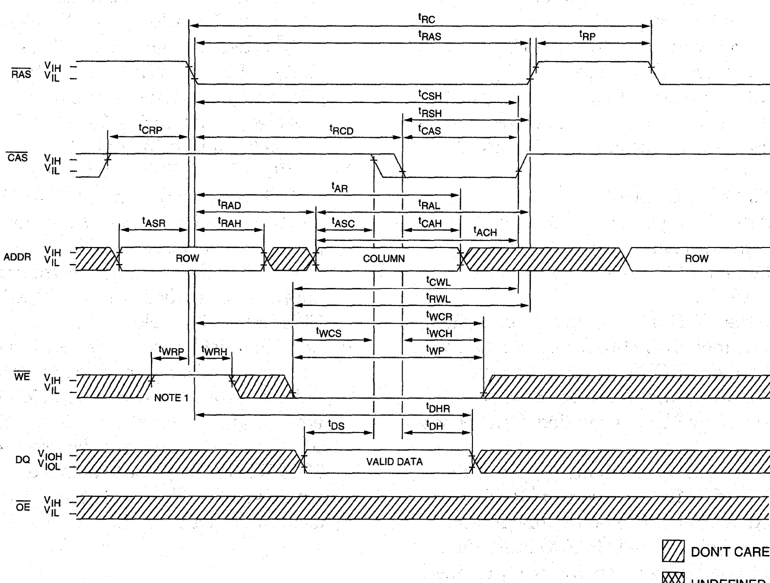
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

2. ^{t}OFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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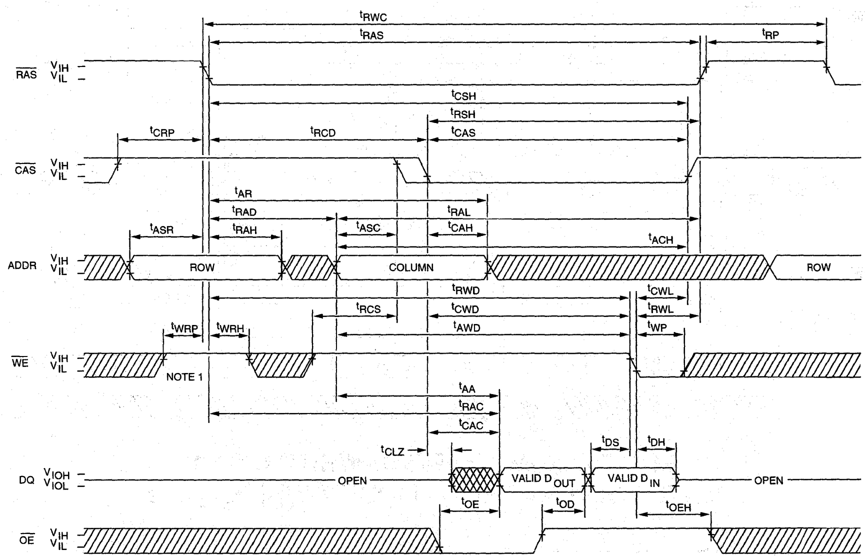
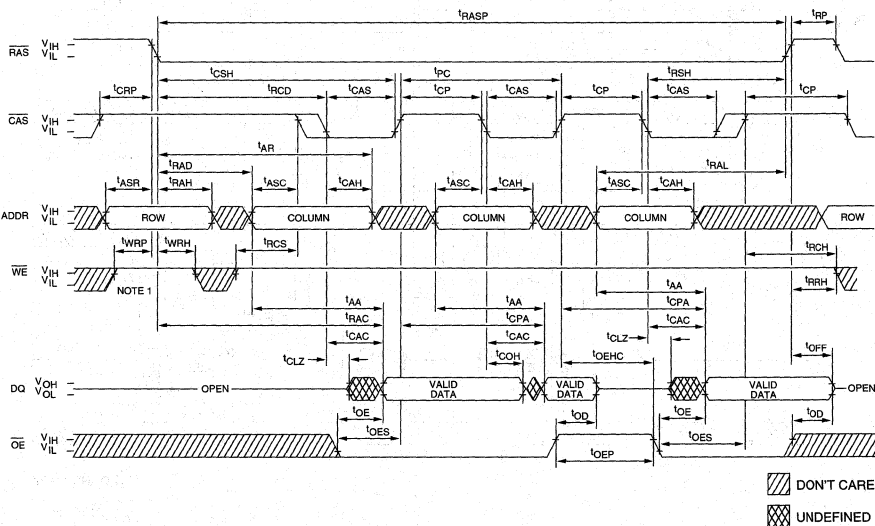
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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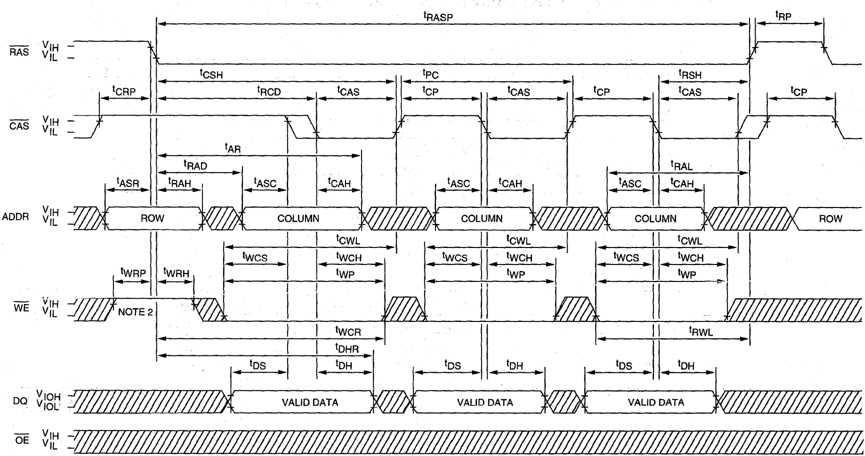
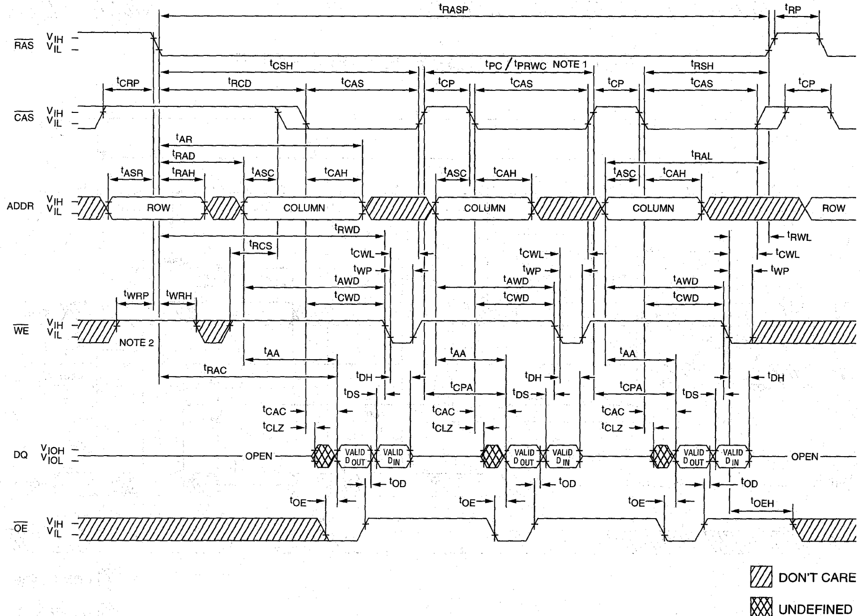
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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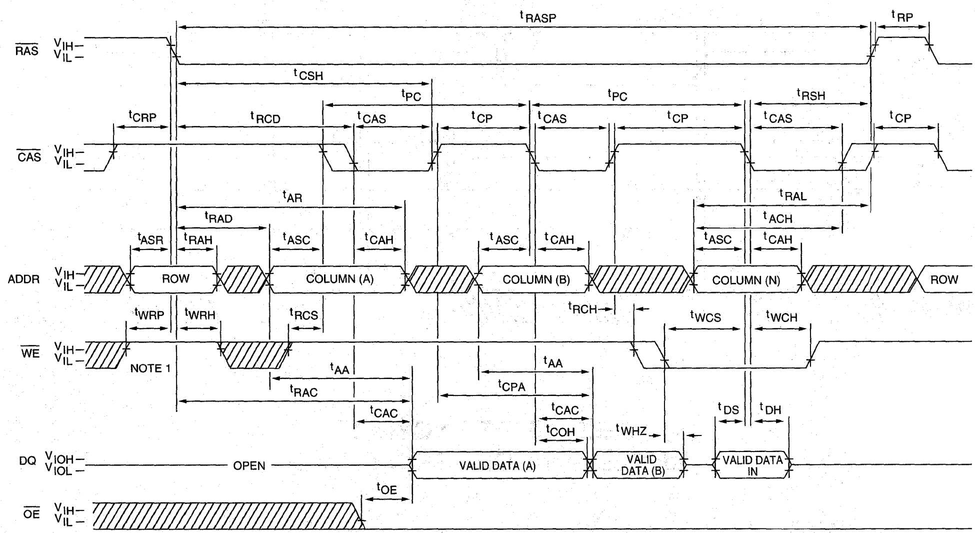
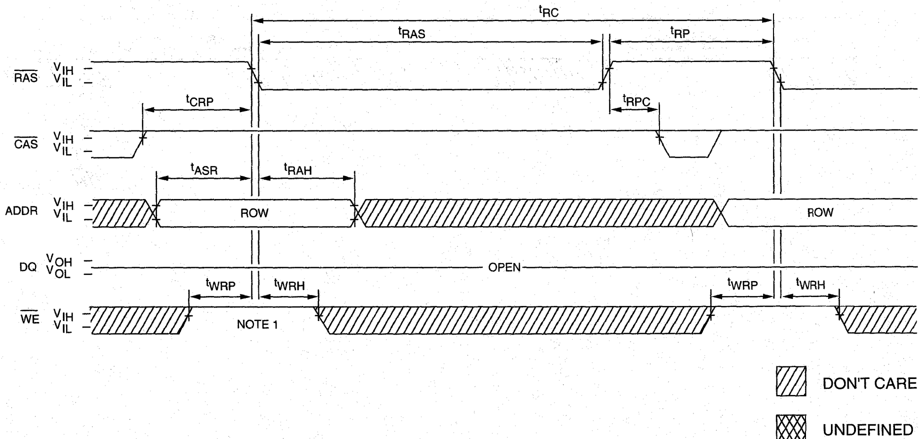
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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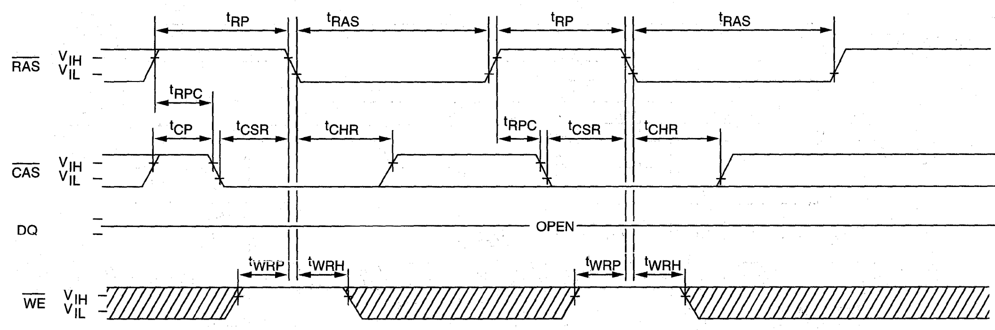
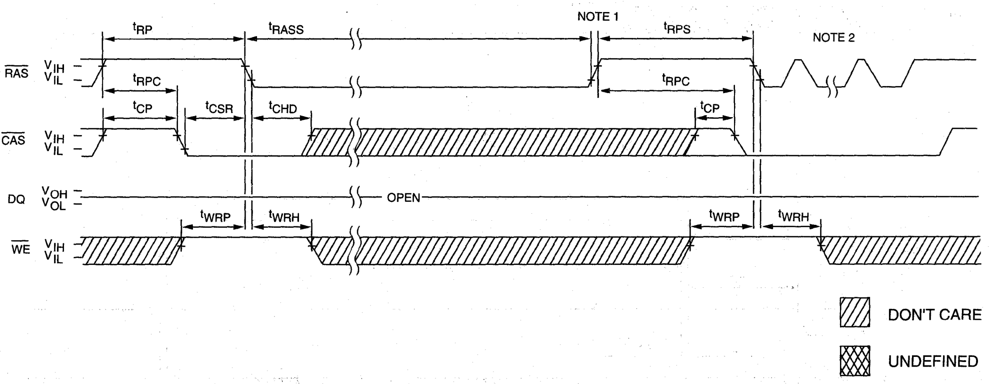
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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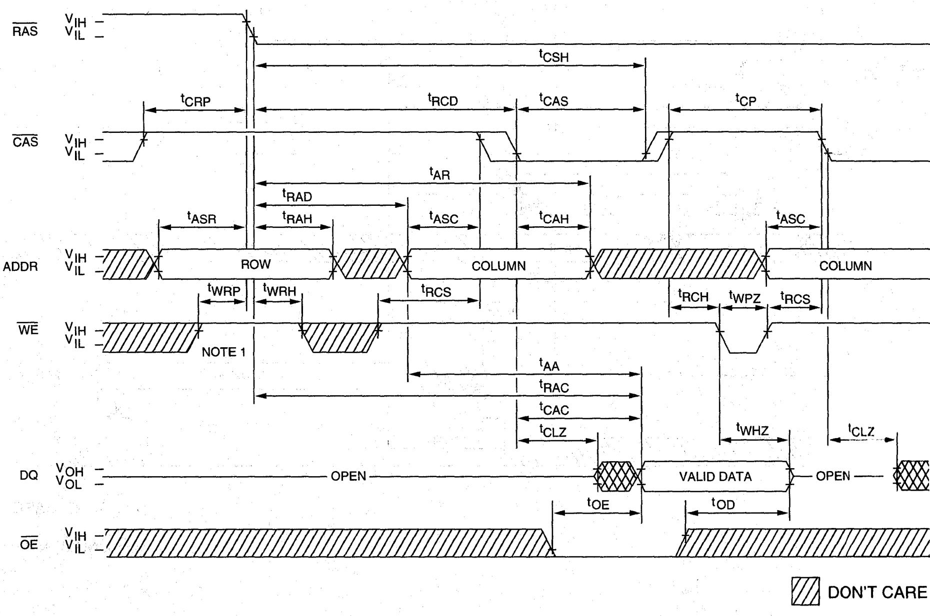
READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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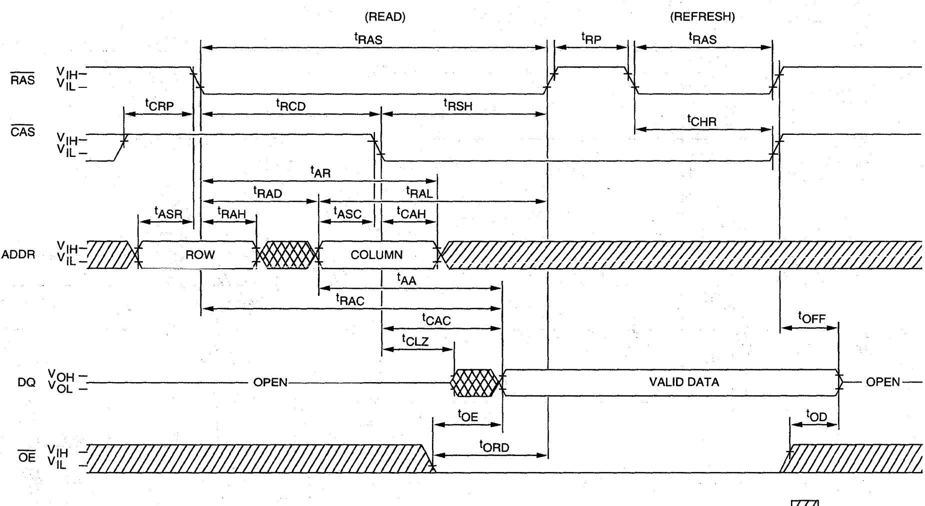
HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



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DRAM

16 MEG x 4 DRAM

3.3V, EDO PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 13 row-addresses, 11 column-addresses (G3) or 12 row-addresses, 12 column-addresses (H9)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH distributed across 64ms

OPTIONS

OPTIONS	MARKING
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (500 mil)	DW
Plastic TSOP (500 mil)	TW

- Part Number Example: MT4LC16M4G3DW-7

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-5	90ns	50ns	20ns	25ns	13ns	8ns
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

PIN ASSIGNMENT (Top View)

34-Pin SOJ (DA-6)

34-Pin TSOP*

Pin	Name	Pin	Name
1	Vcc	34	Vss
2	DQ1	33	DQ4
3	DQ2	32	DQ3
4	NC	31	NC
5	NC	30	NC
6	NC	29	NC
7	NC	28	$\overline{CAS}$
8	$\overline{WE}$	27	$\overline{OE}$
9	$\overline{RAS}$	26	NC
10	NC	25	A12/NC
11	A0	24	A11
12	A1	23	A10
13	A2	22	A9
14	A3	21	A8
15	A4	20	A7
16	A5	19	A6
17	Vcc	18	Vss

*Consult factory for dimensions and availability.

GENERAL DESCRIPTION

The MT4LC16M4G3 and MT4LC16M4H9 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate from 3.0V to 3.6V. The MT4LC16M4G3 and MT4LC16M4H9 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 8,192 rows by 2,048 columns for the MT4LC16M4G3 or 4,096 rows by 4,096 columns for the MT4LC16M4H9. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the $\overline{RAS}$ signal, then the column address by $\overline{CAS}$. Both devices provide EDO PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC16M4G3 and MT4LC16M4H9 must be refreshed periodically in order to retain stored data.

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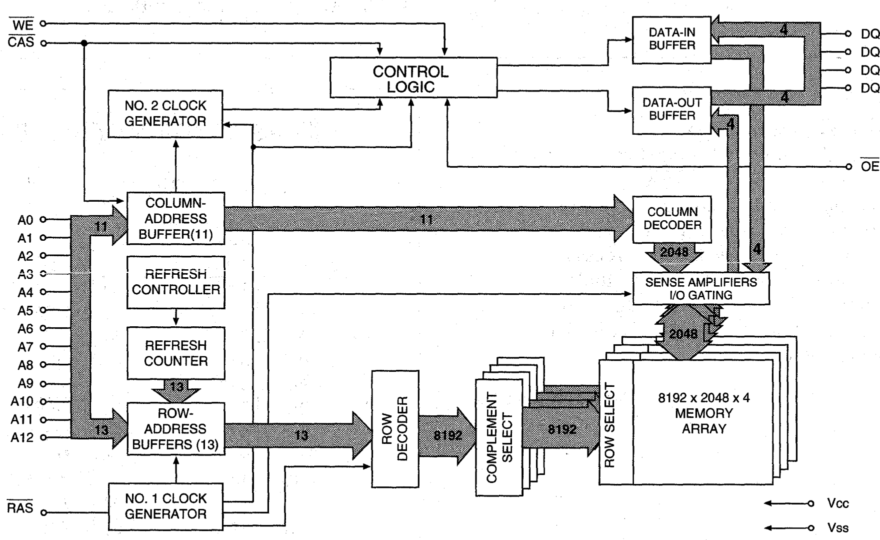
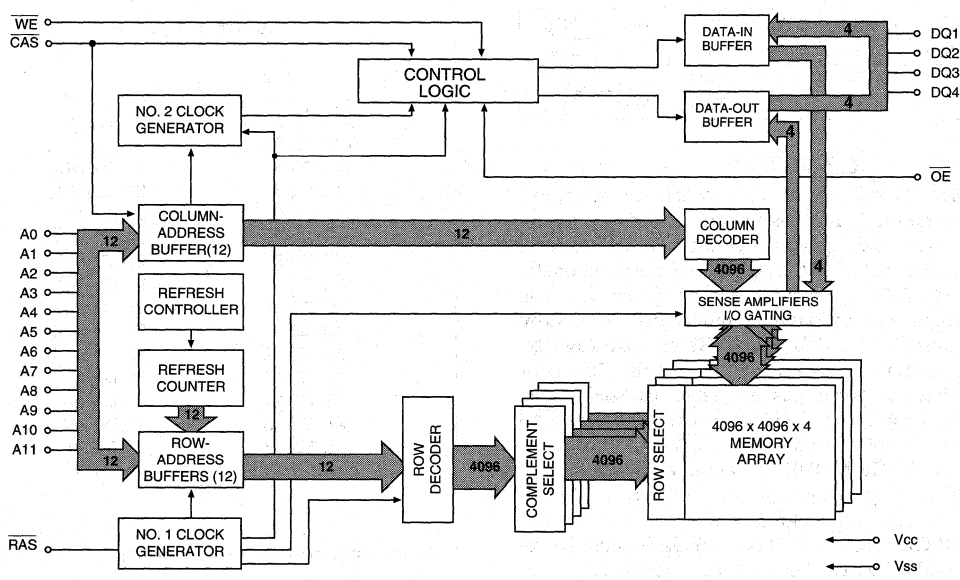
FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4G3 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4H9 (12 row-addresses)



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FUNCTIONAL DESCRIPTION

The functional description for the MT4LC16M4G3 and MT4LC16M4H9 is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet, following the timing specifications tables.

DRAM ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ1-4). The $\overline{WE}$ signal must be activated to execute a write operation, otherwise a read operation will be performed. The $\overline{OE}$ signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ went HIGH, and $\overline{OE}$ was LOW (active), the output buffers would be disabled. The MT4LC16M4G3 and MT4LC16M4H9 offer an accelerated PAGE MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EDO and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH. $\overline{OE}$ can be brought LOW or HIGH while $\overline{CAS}$ and $\overline{RAS}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{OE}$, there are two methods to disable the outputs and keep them disabled during the $\overline{CAS}$ HIGH time. The first method is to have $\overline{OE}$ HIGH when $\overline{CAS}$ transitions HIGH and keep $\overline{OE}$ HIGH for ^tOEHC thereafter. This will disable the DQs and they will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ LOW when $\overline{CAS}$ transitions HIGH. Then bringing $\overline{OE}$ HIGH for a minimum of ^tOEP anytime during the $\overline{CAS}$ HIGH period will disable the DQs; the DQs will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again (please refer to Figure 1). During other cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or ^tWHZ after $\overline{WE}$ transitions LOW. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO PAGE MODE operations are always initiated with a row-address strobed-in by the $\overline{RAS}$ signal, followed by a column-address strobed-in by $\overline{CAS}$, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling $\overline{CAS}$ while holding $\overline{RAS}$ LOW, and entering new column addresses with each $\overline{CAS}$ cycle. Returning $\overline{RAS}$ HIGH terminates the EDO PAGE MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (G3) or all 4,096 rows (H9) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4G3 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4H9 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. Alternatively, $\overline{RAS}$-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time, so for the MT4LC16M4G3, 8,192 $\overline{RAS}$-ONLY REFRESH cycles must be executed every 64ms to cover all rows.

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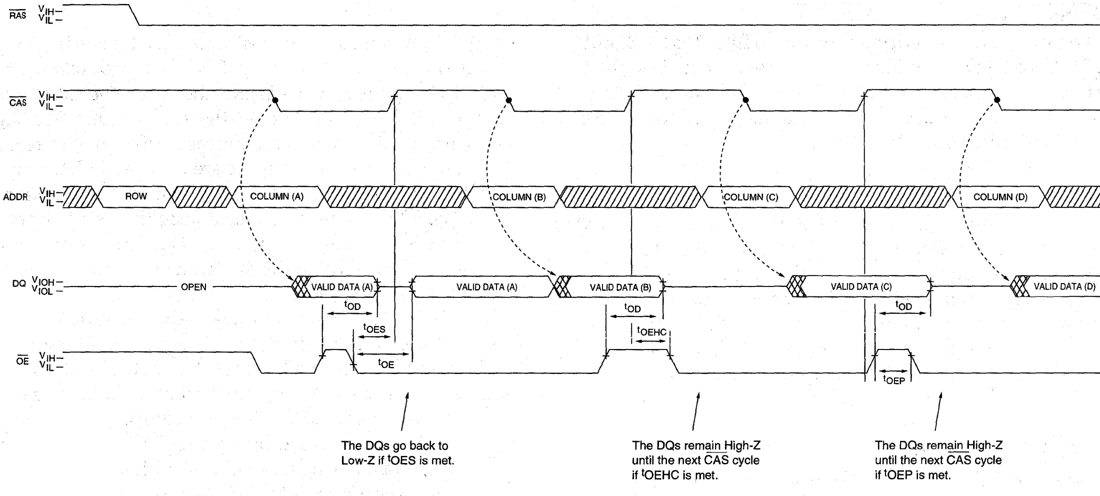

Figure 1
OE CONTROL OF DQs

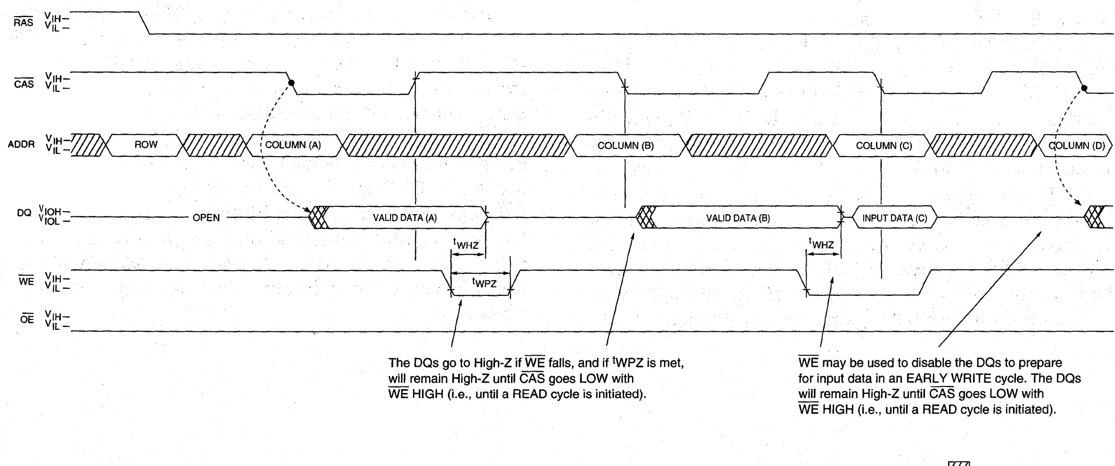

Figure 2
WE CONTROL OF DQs

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} .... -1.0V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} .... -1.0V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -5	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MT4LC16M4G3	I_{CC1}	1	1	1	mA	
	MT4LC16M4H9	I_{CC1}	1	1	1		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2V, DQs may be left open, Other inputs: V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V)	MT4LC16M4G3	I_{CC2}	500	500	500	µA	
	MT4LC16M4H9	I_{CC2}	500	500	500		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC3}	130	120	110	mA	3, 4, 29
	MT4LC16M4H9	I_{CC3}	170	160	150		
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	MT4LC16M4G3	I_{CC4}	150	120	100	mA	3, 4, 29
	MT4LC16M4H9	I_{CC4}	150	120	100		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC5}	130	120	110	mA	3, 26
	MT4LC16M4H9	I_{CC5}	170	160	150		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC16M4G3	I_{CC6}	140	130	120	mA	3, 5
	MT4LC16M4H9	I_{CC6}	170	160	150		

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		25		30		35	ns	
Column-address set-up to CAS going HIGH during WRITE	^tACH	15		15		15		ns	
Column-address hold time (referenced to RAS)	^tAR	40		45		55		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to WE delay time	^tAWD	48		55		65		ns	21
Access time from CAS	^tCAC		13		15		20	ns	15
Column-address hold time	^tCAH	8		10		12		ns	
CAS pulse width	^tCAS	8	10,000	10	10,000	12	10,000	ns	
CAS hold time (CBR REFRESH)	^tCHR	8		10		12		ns	5
CAS to output in Low-Z	^tCLZ	0		0		0		ns	
Data output hold after CAS LOW	^tCOH	5		5		5		ns	
CAS precharge time	^tCP	8		10		10		ns	16
Access time from CAS precharge	^tCPA		28		35		40	ns	
CAS to RAS precharge time	^tCRP	5		5		5		ns	
CAS hold time	^tCSH	44		50		55		ns	
CAS setup time (CBR REFRESH)	^tCSR	5		5		5		ns	5
CAS to WE delay time	^tCWD	30		35		40		ns	21
Write command to CAS lead time	^tCWL	8		15		15		ns	
Data-in hold time	^tDH	8		10		12		ns	22
Data-in hold time (referenced to RAS)	^tDHR	40		45		55		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Output disable	^tOD	0	13	0	15	0	15	ns	27, 28
Output Enable time	^tOE		13		15		15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	8		10		12		ns	28
OE HIGH hold time from CAS HIGH	^tOEHC	7		10		10		ns	
OE HIGH pulse width	^tOEP	7		10		10		ns	
OE LOW to CAS HIGH setup time	^tOES	4		5		5		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^{t}OFF	0	13	0	15	0	15	ns	20, 27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	20		25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	71		75		85		ns	
Access time from $\overline{RAS}$	^{t}RAC		50		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	9	25	12	30	12	35	ns	18
Row-address hold time	^{t}RAH	8		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	25		30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^{t}RASP	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	^{t}RC	90		110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	11	37	14	45	14	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period	^{t}REF		64		64		64	ms	26
$\overline{RAS}$ precharge time	^{t}RP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	8		10		12		ns	
READ WRITE cycle time	^{t}RWC	126		150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	73		80		90		ns	21
Write command to $\overline{RAS}$ lead time	^{t}RWL	8		15		15		ns	
Transition time (rise or fall)	^{t}T	1	50	2	50	2	50	ns	
Write command hold time	^{t}WCH	8		10		12		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	40		45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21
$\overline{WE}$ to outputs in High-Z	^{t}WHZ		10		13		15	ns	
Write command pulse width	^{t}WP	7		10		12		ns	
$\overline{WE}$ pulse width to disable outputs	^{t}WPZ	7		10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	8		10		10		ns	25

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NOTES

1. All voltages referenced to VSS.
2. This parameter is sampled. VCC = +3.3V; f = 1 MHz.
3. ICC is dependent on cycle rates.
4. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}Tof 2ns for -5 and 2.5ns for -6 and -7.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS and RAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. RAS-ONLY REFRESH requires that all 8,192 rows of the MT4LC16M4G3, or all 4,096 rows of the MT4LC16M4H9, be refreshed at least once every 64ms. CBR REFRESH, for either device, requires that at least 4,096 cycles be completed every 64ms.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If CAS stays LOW while OE is brought HIGH, the DQs will open. If OE is brought back LOW (CAS still LOW), the DQs will provide the previously read data.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE is taken back LOW while CAS remains LOW, the DQs will remain open.
29. Column-address changed once each cycle.

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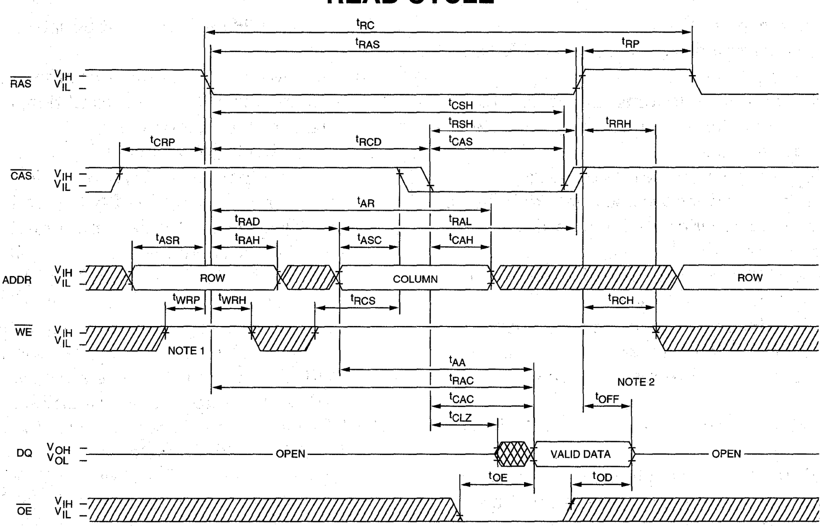
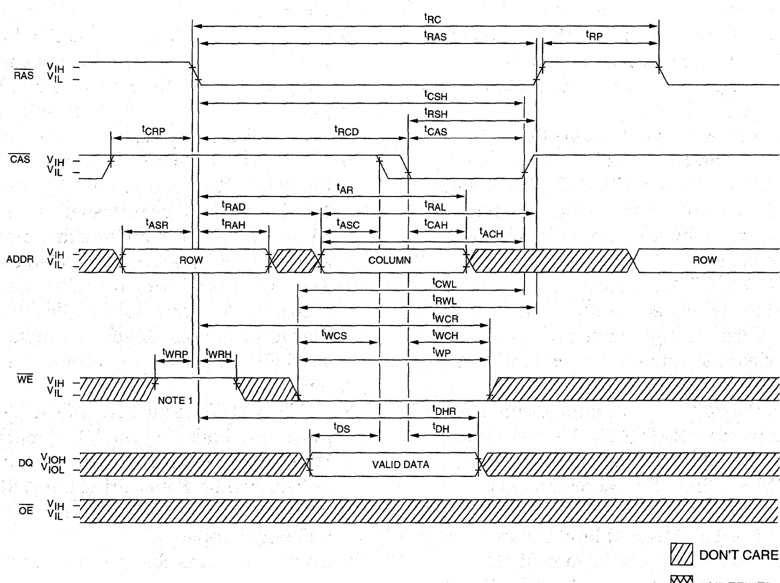
NEW | EDO DRAM

READ CYCLE



EARLY WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

2. ${}^tOFF$ is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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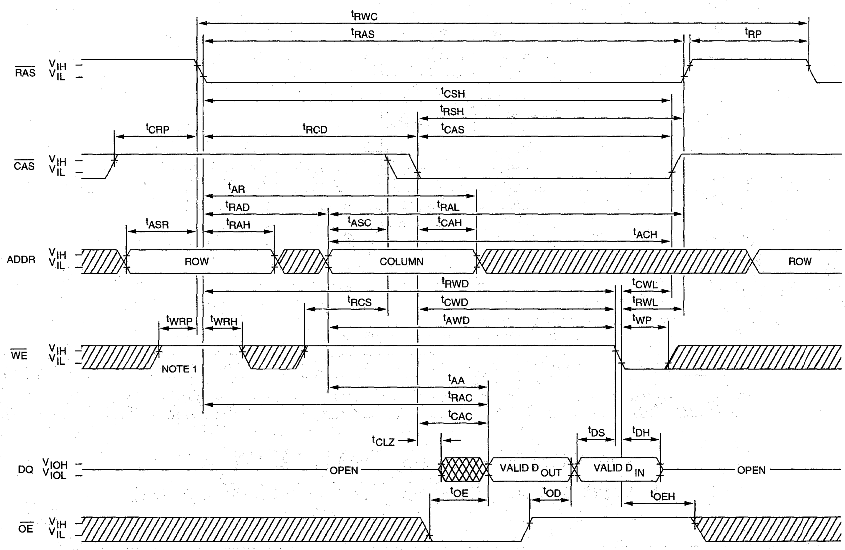
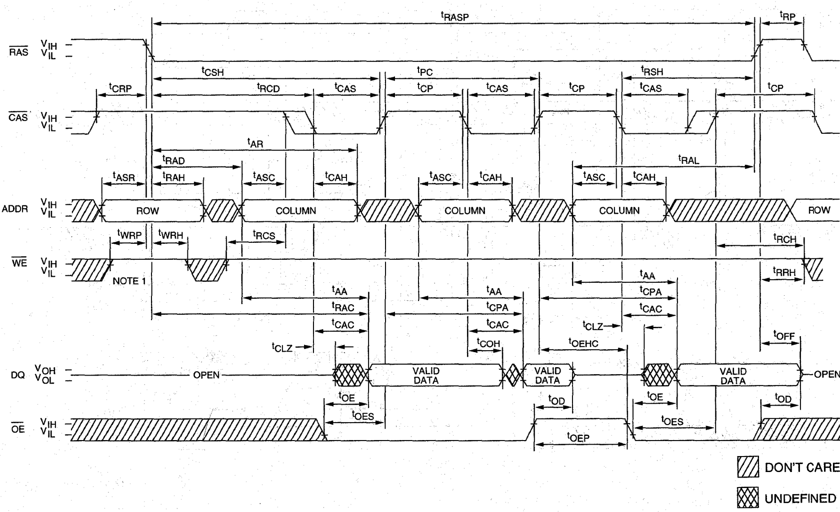
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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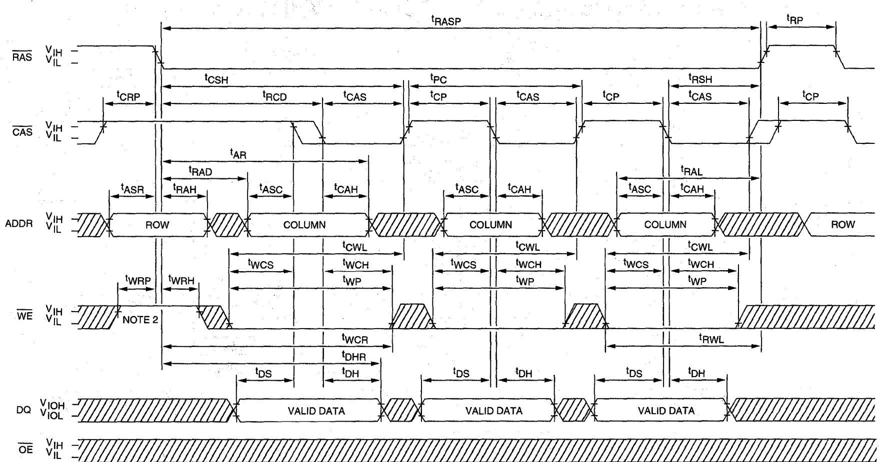
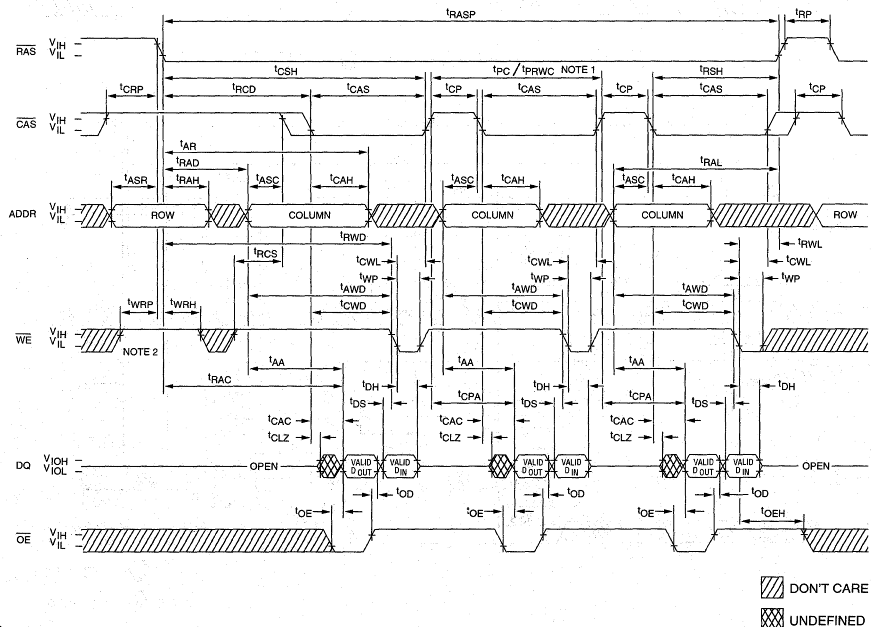
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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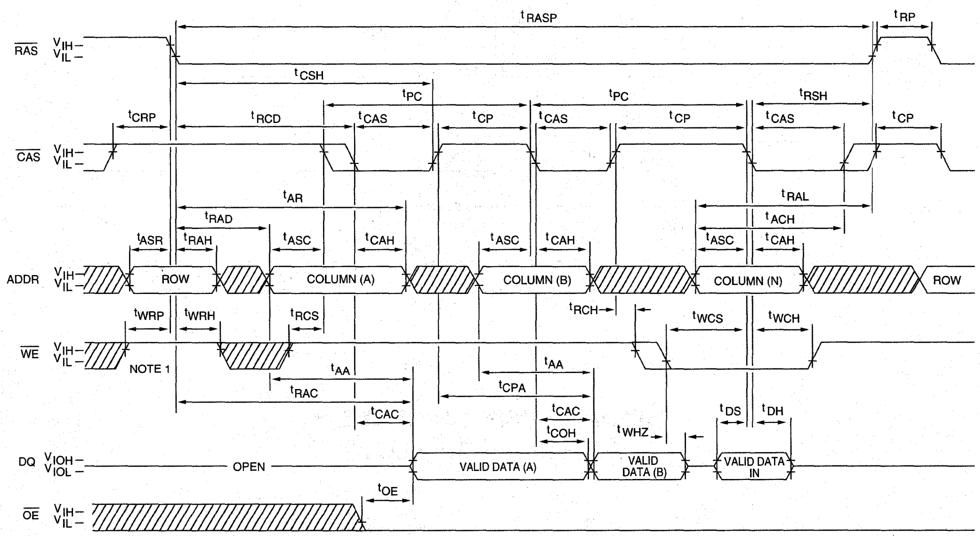
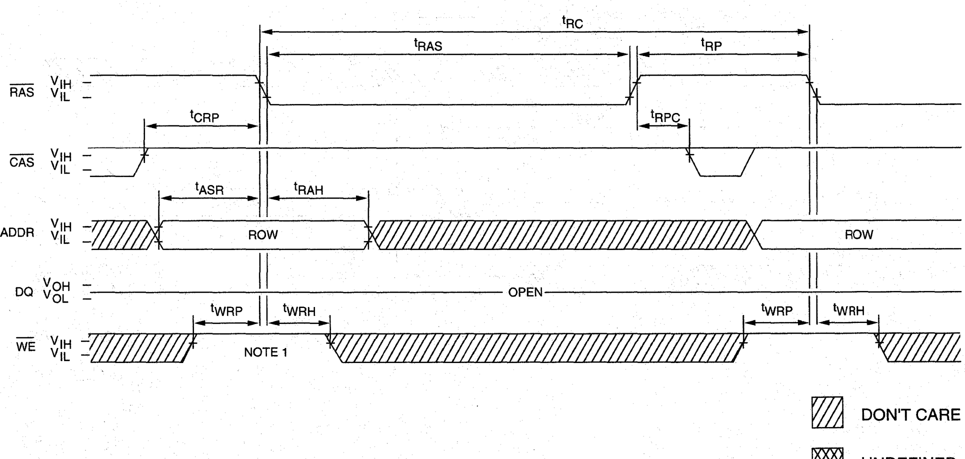
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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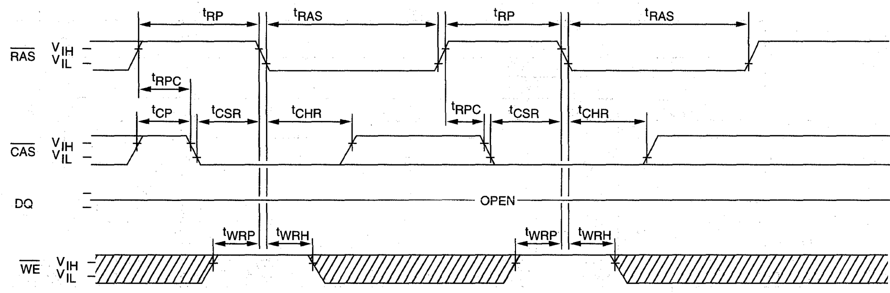
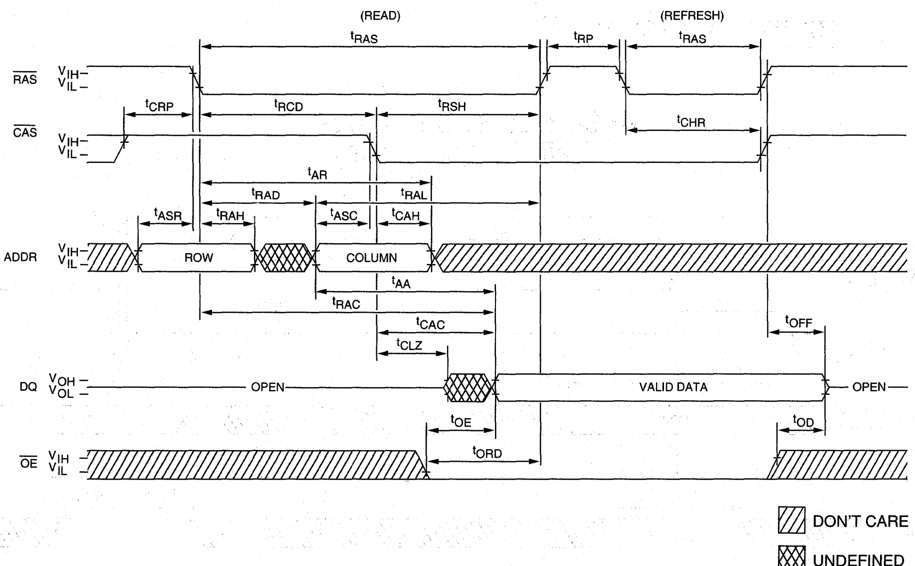
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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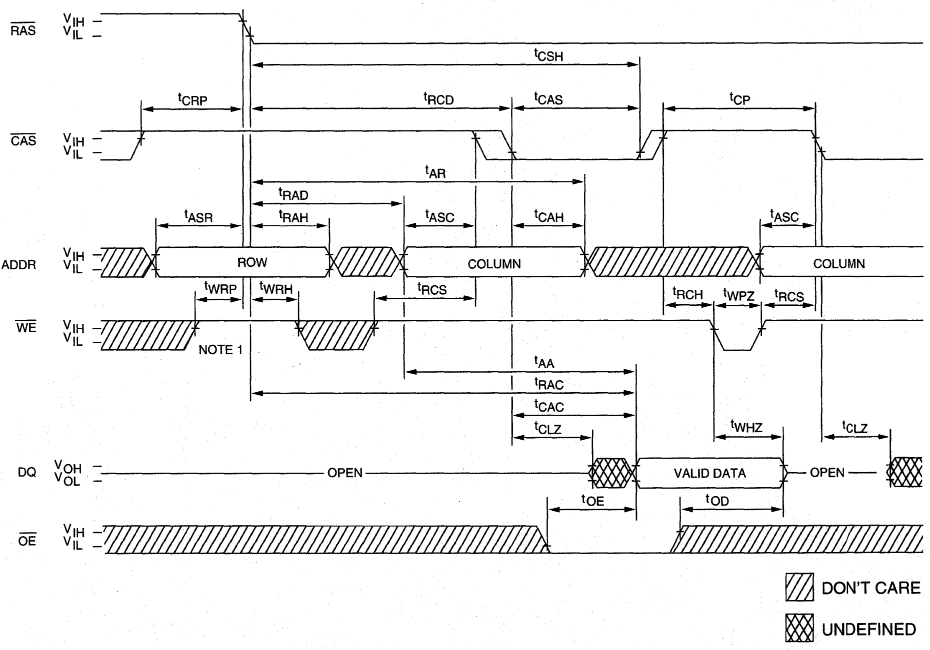
READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM

2 MEG x 8 DRAM

3.3V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x8 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- Low power, 0.3mW standby; 150mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- 2,048-cycle refresh (11 row-, 10 column-addresses)
- Optional SELF REFRESH, Extended Refresh rate (4x)
- Extended Data-Out (EDO) PAGE access cycle
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
Refresh Rate	
Standard 32ms period	None
SELF REFRESH and 128ms periods	S

- Part Number Example: MT4LC2M8E7DJ-7 S

PIN ASSIGNMENT (Top View)

28-Pin SOJ (DA-5) and **28-Pin TSOP (DB-3)** (identical pinout)

Pin	Name	Pin	Name
1	Vcc	28	Vss
2	DQ1	27	DQ8
3	DQ2	26	DQ7
4	DQ3	25	DQ6
5	DQ4	24	DQ5
6	$\overline{WE}$	23	$\overline{CAS}$
7	$\overline{RAS}$	22	$\overline{OE}$
8	NC	21	A9
9	A10	20	A8
10	A0	19	A7
11	A1	18	A6
12	A2	17	A5
13	A3	16	A4
14	Vcc	15	Vss

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

GENERAL DESCRIPTION

The MT4LC2M8E7(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x8 configuration. The MT4LC2M8E7(S) $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 10 bits (A10 is ignored during $\overline{CAS}$ falling edge.) READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, data-out (Q) is activated and retains the selected cell data as long as $\overline{OE}$ remains LOW and $\overline{RAS}$ or $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

If $\overline{WE}$ toggles LOW after $\overline{CAS}$ goes back HIGH, the output pins will open (High- Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

The eight data inputs and the eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the PAGE MODE of operation.

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EDO PAGE MODE

The MT4LC2M8E7(S) provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z (refer to Figure 1).

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS HIGH time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last.

REFRESH

Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC2M8E7 S. The "S" version allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

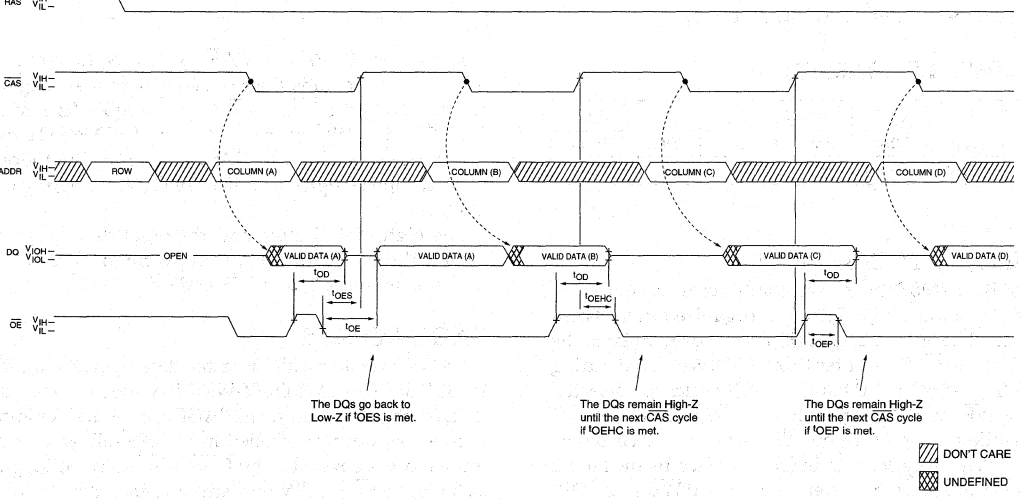

Figure 1
OUTPUT ENABLE AND DISABLE

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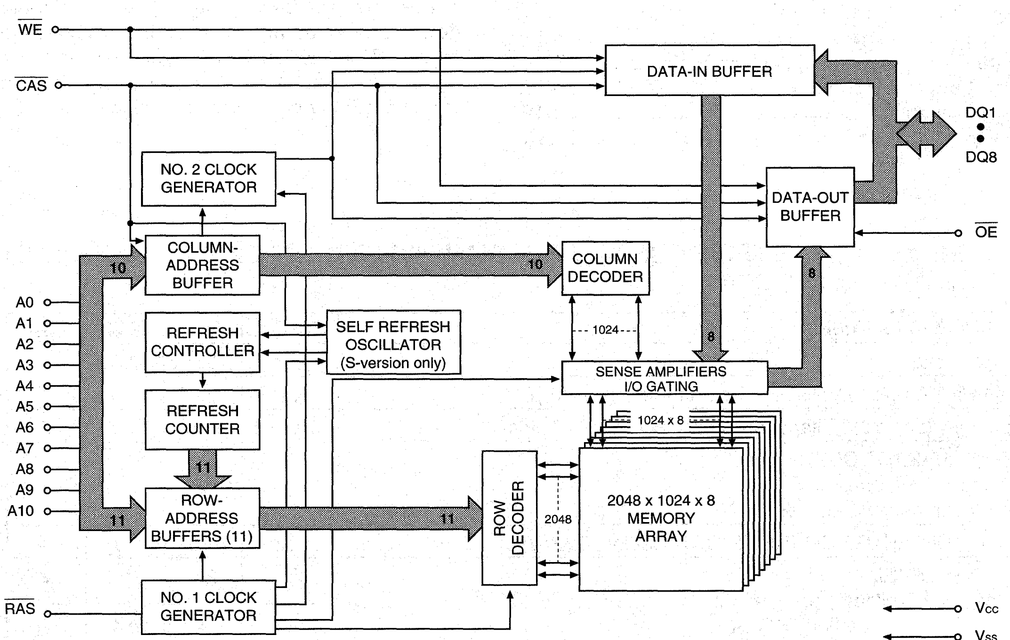
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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EDO DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	µA	
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	130	120	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	120	110	mA	3, 4, 12
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	130	120	mA	3, 12
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	130	120	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS(MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS(MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address set-up to $\overline{CAS}$ precharge during WRITE	^tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		ns	20
Access time from $\overline{CAS}$	^tCAC		15		20	ns	14
Column-address hold time	^tCAH	10		12		ns	
$\overline{CAS}$ pulse width	^tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ LOW to “don't care” during SELF REFRESH cycle	^tCHD	15		15		ns	25
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		12		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next $\overline{CAS}$ LOW	^tCOH	5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	15
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		ns	20
Write command to $\overline{CAS}$ lead time	^tCWL	15		15		ns	
Data-in hold time	^tDH	10		12		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21
Output disable	^tOD	0	15	0	15	ns	
Output Enable	^tOE		15		15	ns	22
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	12		12		ns	
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	^tOEHC	10		10		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		ns	
Output buffer turn-off delay	^tOFF	3	15	3	15	ns	
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	75		85		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	13
$\overline{RAS}$ to column-address delay time	^tRAD	12	30	12	35	ns	17
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	125,000	70	125,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		µs	25
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	14	45	14	50	ns	16
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	18
Read command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles) S version	^tREF		128		128	ms	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		ns	25
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	18
$\overline{RAS}$ hold time	^tRSH	10		12		ns	
READ WRITE cycle time	^tRWC	150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		ns	20
Write command to $\overline{RAS}$ lead time	^tRWL	15		15		ns	
Transition time (rise or fall)	^tT	2	50	2	50	ns	
Write command hold time	^tWCH	10		12		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	20
Output disable delay from $\overline{WE}$	^tWHZ	0	13	0	15	ns	
Write command pulse width	^tWP	10		12		ns	
$\overline{WE}$ pulse to disable at $\overline{CAS}$ HIGH	^tWPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. Column address changed once each cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
14. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
16. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC, provided ^tRAD is not exceeded.
17. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA, provided ^tRCD is not exceeded.
18. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
19. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
20. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tWCS < {}^tWCS$ (MIN) and $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
22. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{WE}$ must be pulsed during $\overline{CAS}$ HIGH time in order to palce I/O buffers in High-Z.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.

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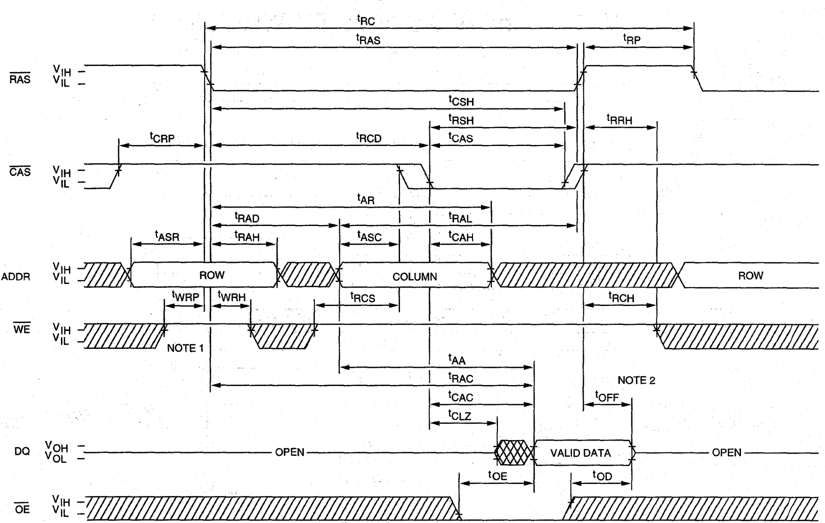
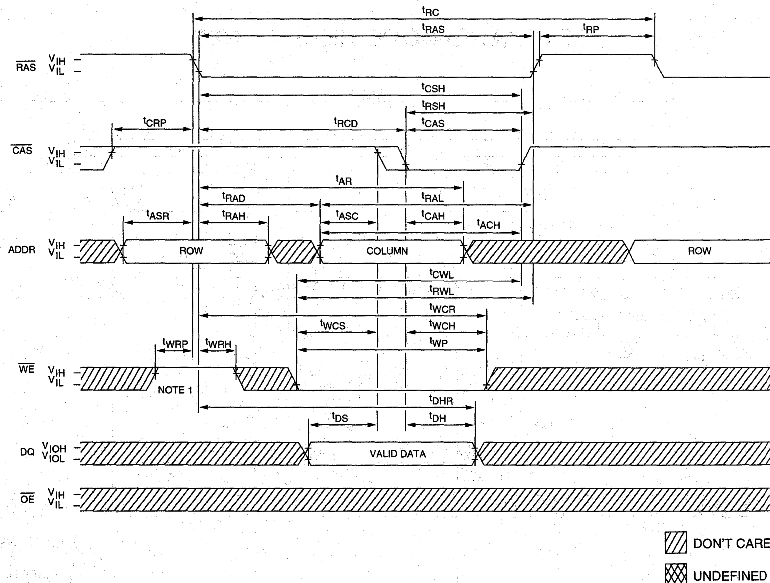
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE:
1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of RAS or CAS, which ever occurs last.

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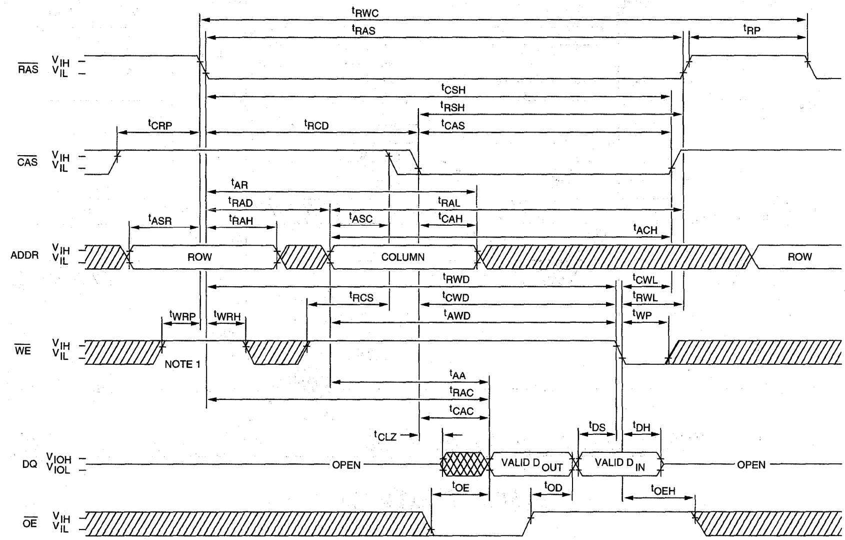
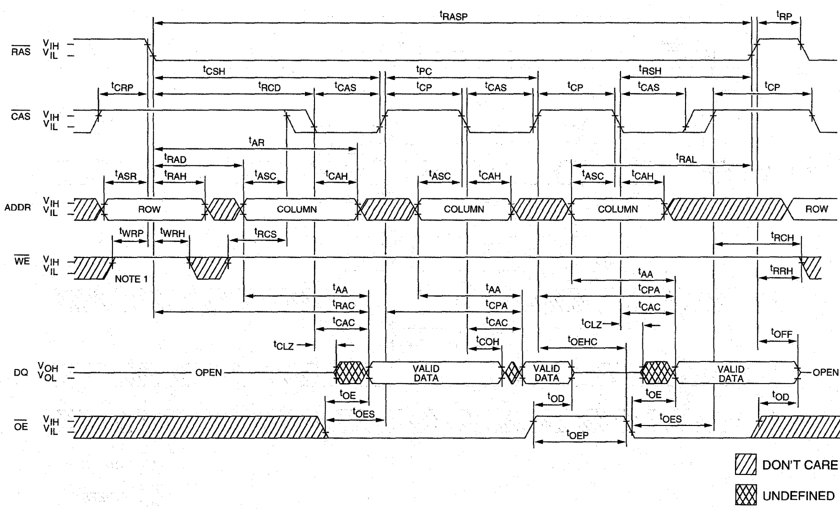
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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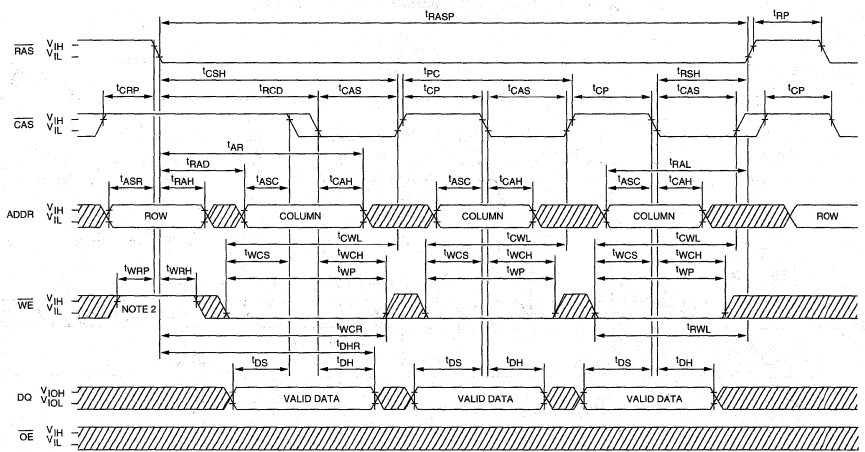
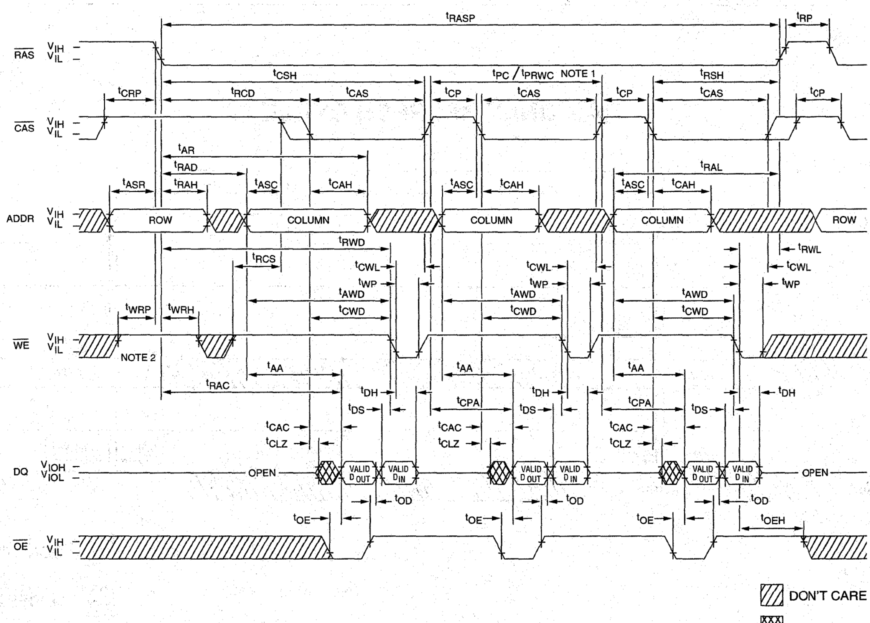
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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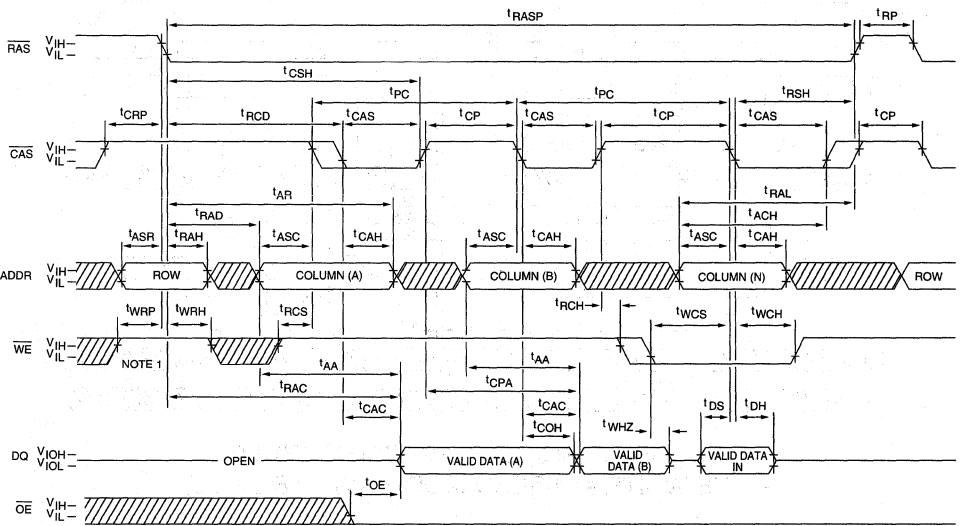
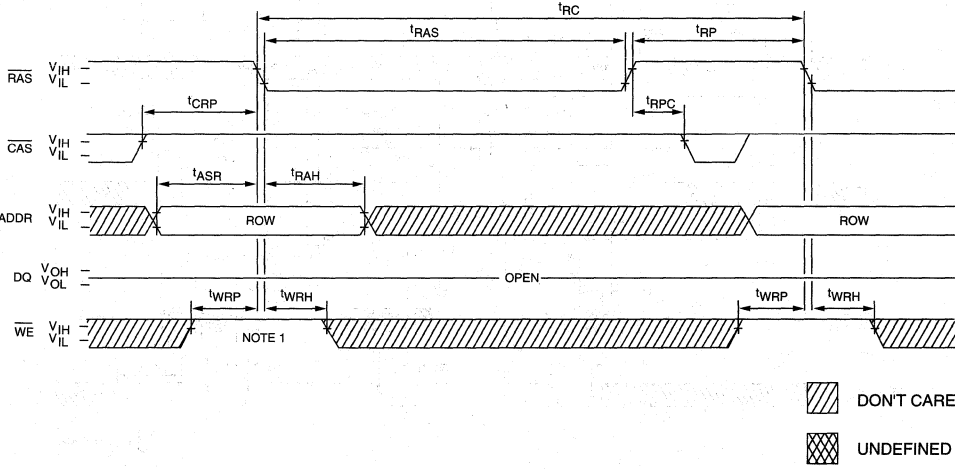
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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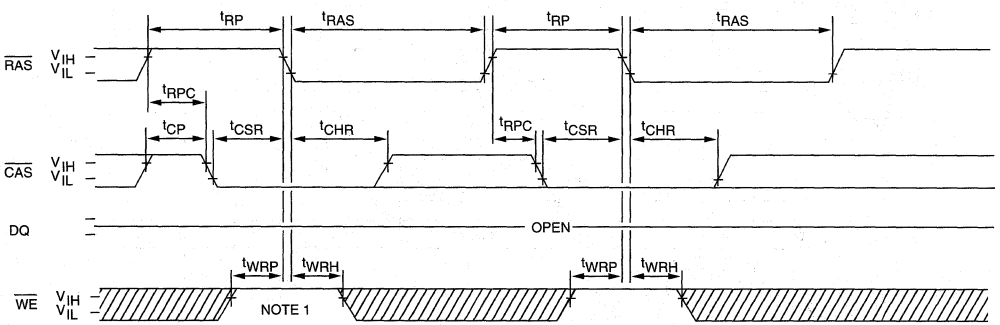
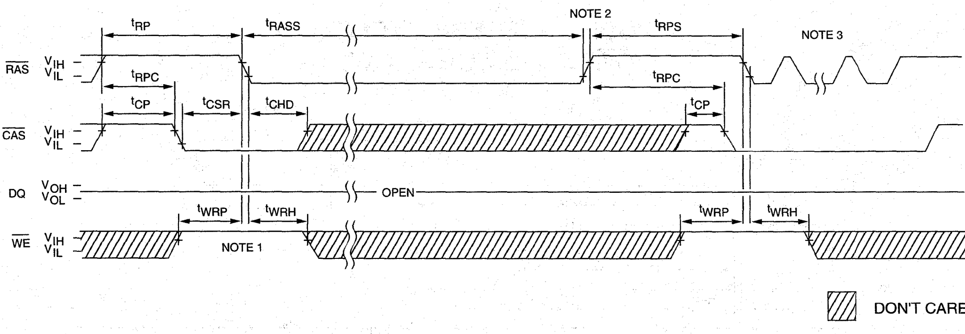
CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE:
1. tWRP and tWRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs that require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.
2. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
3. Once tRPS is satisfied, a complete burst of all rows should be executed.

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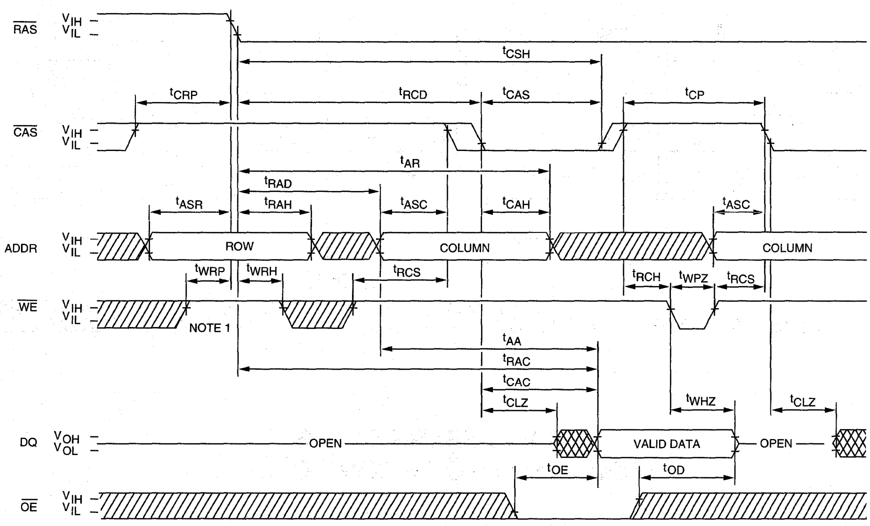
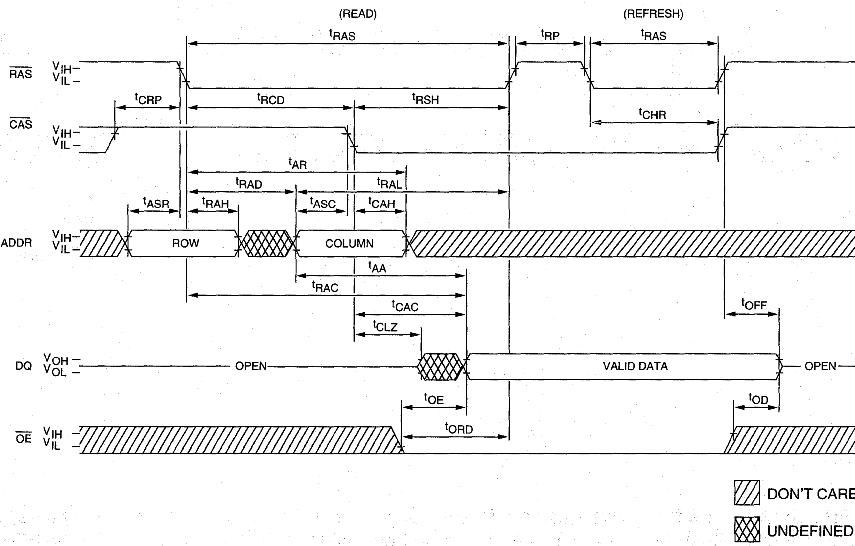
READ CYCLE
(with $\overline{WE}$-controlled disable)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM

8 MEG x 8 DRAM

3.3V, EDO PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x8 pinout, timing, functions and packages
- 13 row-addresses, 10 column-addresses (P4) or 12 row-addresses, 11 column-addresses (C2)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- 4,096-cycle $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH distributed across 64ms

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (500 mil)	DW
Plastic TSOP (500 mil)	TW

- Part Number Example: MT4LC8M8P4DW-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	90ns	50ns	20ns	25ns	13ns	8ns
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

GENERAL DESCRIPTION

The MT4LC8M8P4 and MT4LC8M8C2 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate from 3.0V to 3.6V. The MT4LC8M8P4 and MT4LC8M8C2 are functionally organized as 8,388,608 locations containing 8 bits each. The 8,388,608 memory locations are arranged in 8,192 rows by 1,024 columns for the MT4LC8M8P4 or 4,096 rows by 2,048 columns for the MT4LC8M8C2. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the $\overline{RAS}$ signal, then the column address by $\overline{CAS}$. Both devices provide EDO PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC8M8P4 and MT4LC8M8C2 must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)

34-Pin SOJ (DA-6)

Signal	Pin	Pin	Signal
Vcc	1	34	Vss
DQ1	2	33	DQ8
DQ2	3	32	DQ7
DQ3	4	31	DQ6
DQ4	5	30	DQ5
NC	6	29	VSS
Vcc	7	28	$\overline{CAS}$
$\overline{WE}$	8	27	$\overline{OE}$
$\overline{RAS}$	9	26	NC
NC	10	25	A12/NC
A0	11	24	A11
A1	12	23	A10
A2	13	22	A9
A3	14	21	A8
A4	15	20	A7
A5	16	19	A6
Vcc	17	18	Vss

34-Pin TSOP*

Signal	Pin	Pin	Signal
Vcc	1	34	Vss
DQ1	2	33	DQ8
DQ2	3	32	DQ7
DQ3	4	31	DQ6
DQ4	5	30	DQ5
NC	6	29	Vss
Vcc	7	28	$\overline{CAS}$
$\overline{WE}$	8	27	$\overline{OE}$
$\overline{RAS}$	9	26	NC
NC	10	25	A12/NC
A0	11	24	A11
A1	12	23	A10
A2	13	22	A9
A3	14	21	A8
A4	15	20	A7
A5	16	19	A6
Vcc	17	18	Vss

*Consult factory for dimensions and availability.

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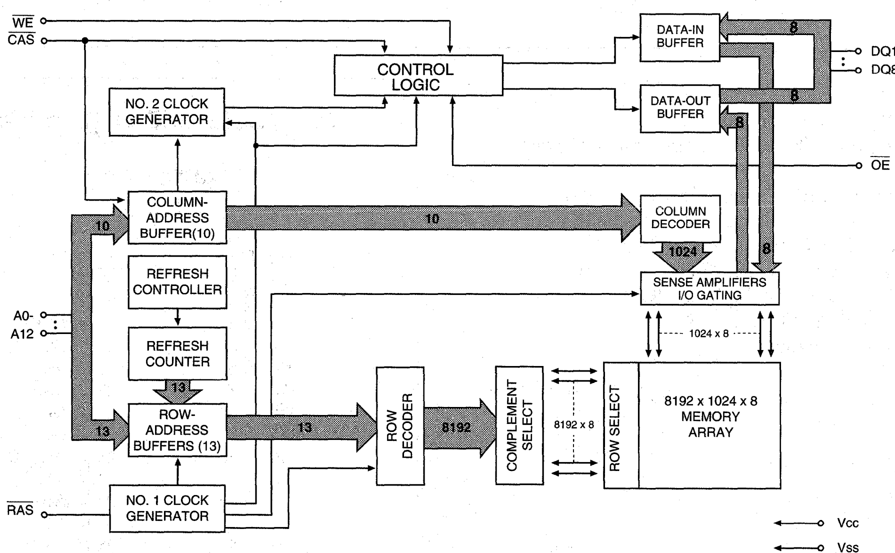
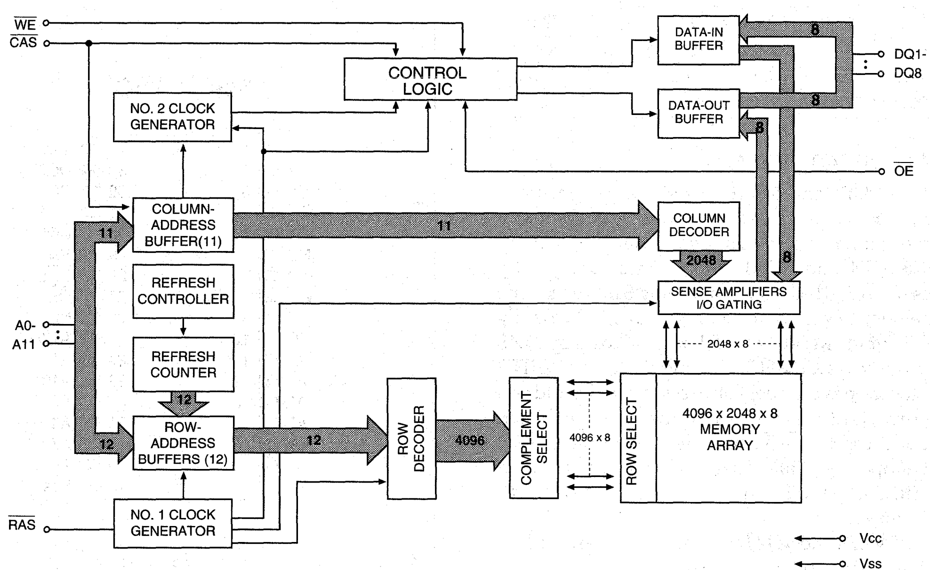
FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8P4 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8C2 (12 row-addresses)



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FUNCTIONAL DESCRIPTION

The functional description for the MT4LC8M8P4 and MT4LC8M8C2 is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet, following the timing specification tables.

DRAM ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the eight I/O pins (DQ1-8). The $\overline{WE}$ signal must be activated to execute a write operation, otherwise a read operation will be performed. The $\overline{OE}$ signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. If $\overline{CAS}$ went HIGH, and $\overline{OE}$ was LOW (active), the output buffers would be disabled. The MT4LC8M8P4 and MT4LC8M8C2 offer an accelerated PAGE MODE cycle by eliminating output disable from $\overline{CAS}$ HIGH. This option is called EDO and it allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms in the noted appendix).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH. $\overline{OE}$ can be brought LOW or HIGH while $\overline{CAS}$ and $\overline{RAS}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{OE}$, there are two methods to disable the outputs and keep them disabled during the $\overline{CAS}$ HIGH time. The first method is to have $\overline{OE}$ HIGH when $\overline{CAS}$ transitions HIGH and keep $\overline{OE}$ HIGH for ^tOEHC thereafter. This will disable the DQs and they will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ LOW when $\overline{CAS}$ transitions HIGH. Then bringing $\overline{OE}$ HIGH for a minimum of ^tOEP anytime during the $\overline{CAS}$ HIGH period will disable the DQs; the DQs will remain disabled (regardless of the state of $\overline{OE}$ after that point) until $\overline{CAS}$ falls again (see Figure 1). During other cycles, the outputs are disabled at ^tOFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or ^tWHZ after $\overline{WE}$ transitions LOW. The ^tOFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO PAGE MODE operations are always initiated with a row-address strobed-in by the $\overline{RAS}$ signal, followed by a column-address strobed-in by $\overline{CAS}$, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling $\overline{CAS}$ while holding $\overline{RAS}$ LOW, and entering new column addresses with each $\overline{CAS}$ cycle. Returning $\overline{RAS}$ HIGH terminates the EDO PAGE MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (P4) or all 4,096 rows (C2) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC8M8P4 internally refreshes two rows for every CBR cycle, whereas the MT4LC8M8C2 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. Alternatively, $\overline{RAS}$-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time, so for the MT4LC8M8P4, 8,192 $\overline{RAS}$-ONLY REFRESH cycles must be executed every 64ms to cover all rows.

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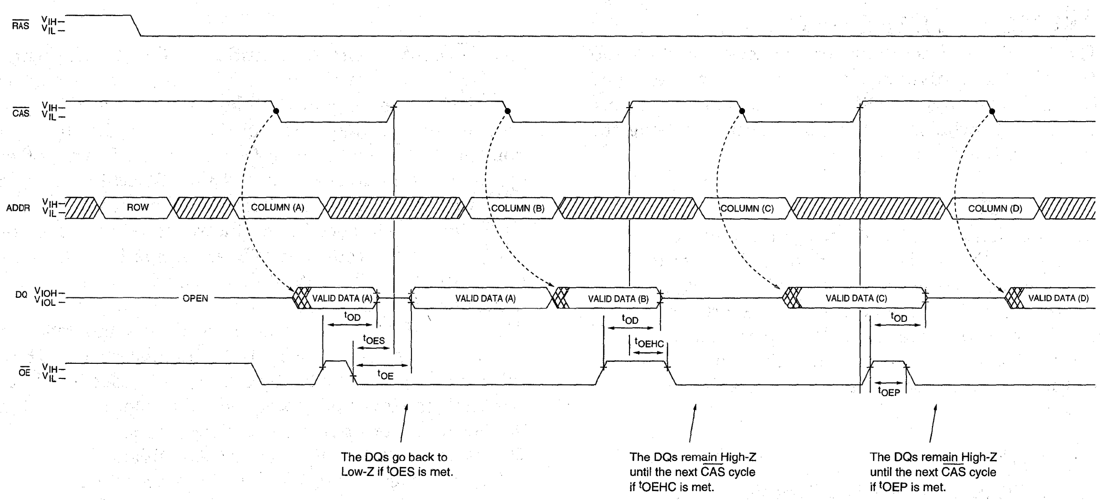

Figure 1
OE CONTROL OF DQs

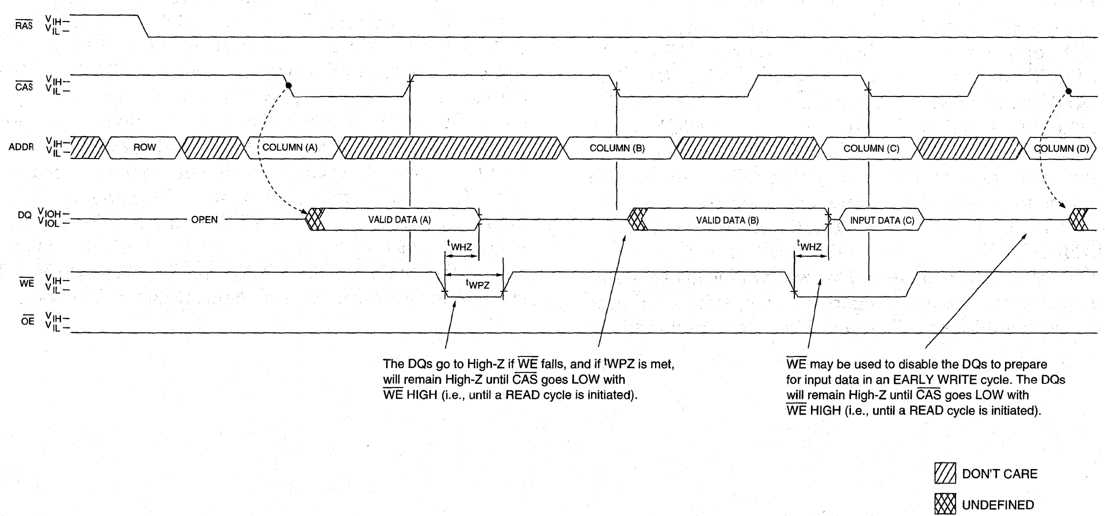

Figure 2
WE CONTROL OF DQs

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} .... -1.0V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} .... -1.0V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -5	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MT4LC8M8P4	I_{CC1}	1	1	1	mA	
	MT4LC8M8C2	I_{CC1}	1	1	1		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2V, DQs may be left open, Other inputs: V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V)	MT4LC8M8P4	I_{CC2}	500	500	500	µA	
	MT4LC8M8C2	I_{CC2}	500	500	500		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC8M8P4	I_{CC3}	135	125	115	mA	3, 4, 29
	MT4LC8M8C2	I_{CC3}	175	165	155		
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	MT4LC8M8P4	I_{CC4}	155	125	105	mA	3, 4, 29
	MT4LC8M8C2	I_{CC4}	155	125	105		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	MT4LC8M8P4	I_{CC5}	135	125	115	mA	3, 26
	MT4LC8M8C2	I_{CC5}	175	165	155		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	MT4LC8M8P4	I_{CC6}	145	135	125	mA	3, 5
	MT4LC8M8C2	I_{CC6}	175	165	155		

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		25		30		35	ns	
Column-address set-up to $\overline{CAS}$ going HIGH during WRITE	^tACH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	40		45		55		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	48		55		65		ns	21
Access time from $\overline{CAS}$	^tCAC		13		15		20	ns	15
Column-address hold time	^tCAH	8		10		12		ns	
$\overline{CAS}$ pulse width	^tCAS	8	10,000	10	10,000	12	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	8		10		12		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		5		ns	
$\overline{CAS}$ precharge time	^tCP	8		10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		28		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
$\overline{CAS}$ hold time	^tCSH	44		50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	30		35		40		ns	21
Write command to $\overline{CAS}$ lead time	^tCWL	8		15		15		ns	
Data-in hold time	^tDH	8		10		12		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		45		55		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Output disable	^tOD	0	13	0	15	0	15	ns	27, 28
Output Enable time	^tOE		13		15		15	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	8		10		12		ns	28
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	7		10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	7		10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	4		5		5		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^{t}OFF	0	13	0	15	0	15	ns	20, 27
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	20		25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	71		75		85		ns	
Access time from RAS	^{t}RAC		50		60		70	ns	14
RAS to column-address delay time	^{t}RAD	9	25	12	30	12	35	ns	18
Row-address hold time	^{t}RAH	8		10		10		ns	
Column-address to RAS lead time	^{t}RAL	25		30		35		ns	
RAS pulse width	^{t}RAS	50	10,000	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	^{t}RASP	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	^{t}RC	90		110		130		ns	
RAS to CAS delay time	^{t}RCD	11	37	14	45	14	50	ns	17
Read command hold time (referenced to CAS)	^{t}RCH	0		0		0		ns	19
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period	^{t}REF		64		64		64	ms	26
RAS precharge time	^{t}RP	30		40		50		ns	
RAS to CAS precharge time	^{t}RPC	0		0		0		ns	
Read command hold time (referenced to RAS)	^{t}RRH	0		0		0		ns	19
RAS hold time	^{t}RSH	8		10		12		ns	
READ WRITE cycle time	^{t}RWC	126		150		177		ns	
RAS to WE delay time	^{t}RWD	73		80		90		ns	21
Write command to RAS lead time	^{t}RWL	8		15		15		ns	
Transition time (rise or fall)	^{t}T	1	50	2	50	2	50	ns	
Write command hold time	^{t}WCH	8		10		12		ns	
Write command hold time (referenced to RAS)	^{t}WCR	40		45		55		ns	
WE command setup time	^{t}WCS	0		0		0		ns	21
WE to outputs in High-Z	^{t}WHZ		10		13		15	ns	
Write command pulse width	^{t}WP	7		10		12		ns	
WE pulse widths to disable outputs	^{t}WPZ	7		10		12		ns	
WE hold time (CBR REFRESH)	^{t}WRH	8		10		10		ns	25
WE setup time (CBR REFRESH)	^{t}WRP	8		10		10		ns	25

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 2ns for -5 and 2.5ns for -6 and -7.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ᵗCP.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are not restrictive operating parameters. ᵗWCS applies to EARLY WRITE cycles. If ᵗWCS > ᵗWCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ᵗRWD, ᵗAWD and ᵗCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ᵗWCS, ᵗRWD, ᵗCWD and ᵗAWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ᵗWTS and ᵗWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
26. $\overline{RAS}$-ONLY REFRESH requires that all 8,192 rows of the MT4LC8M8P4, or all 4,096 rows of the MT4LC8M8C2, be refreshed at least once every 64ms. CBR REFRESH, for either device, requires that at least 4,096 cycles be completed every 64ms.
27. The DQs open during READ cycles once ᵗOD or ᵗOFF occur. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ᵗOD and ᵗOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
29. Column-address changed once each cycle.

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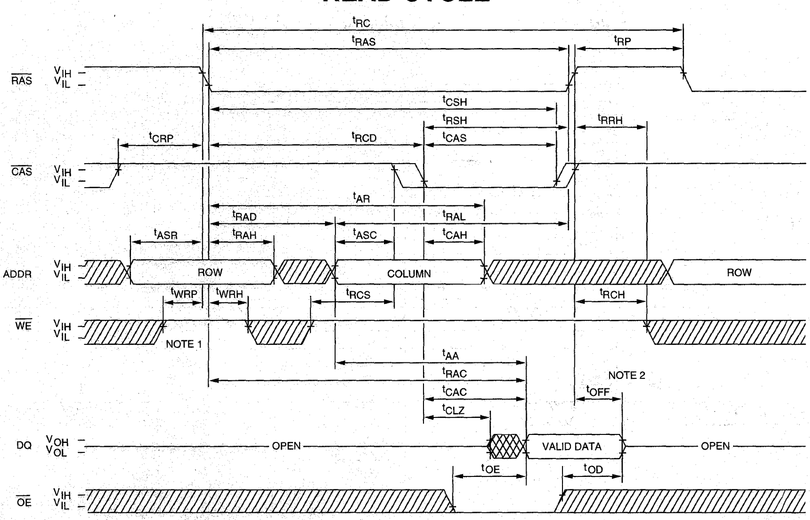
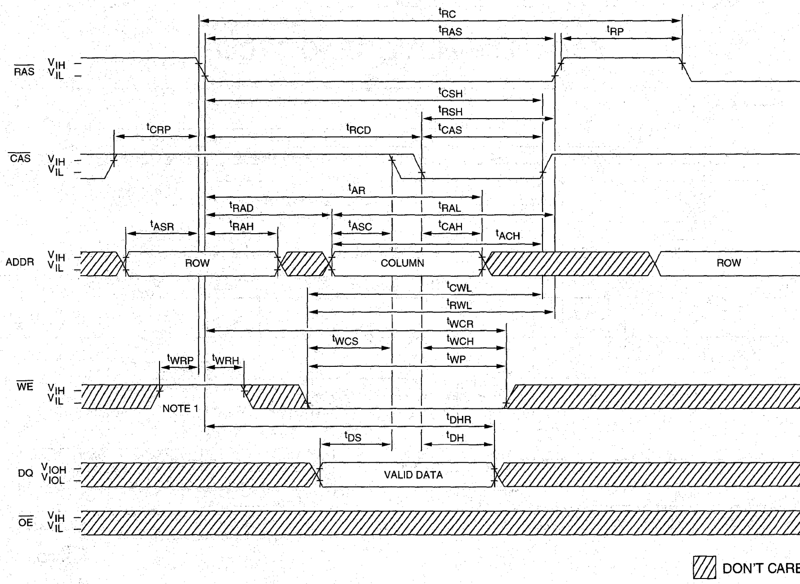
READ CYCLE



EARLY WRITE CYCLE



NOTE:

1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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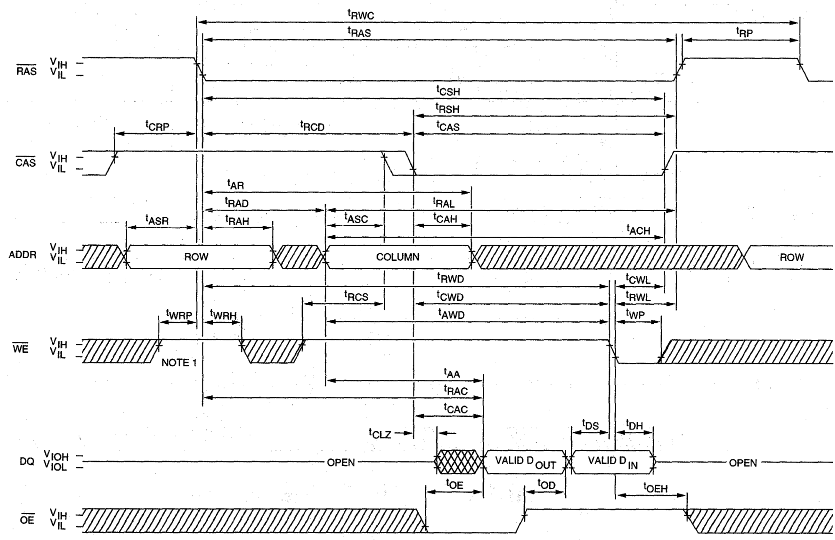
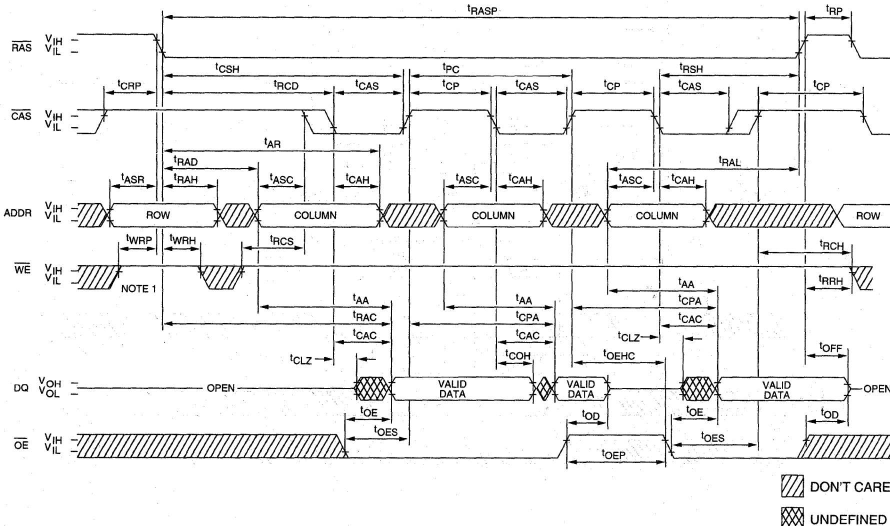
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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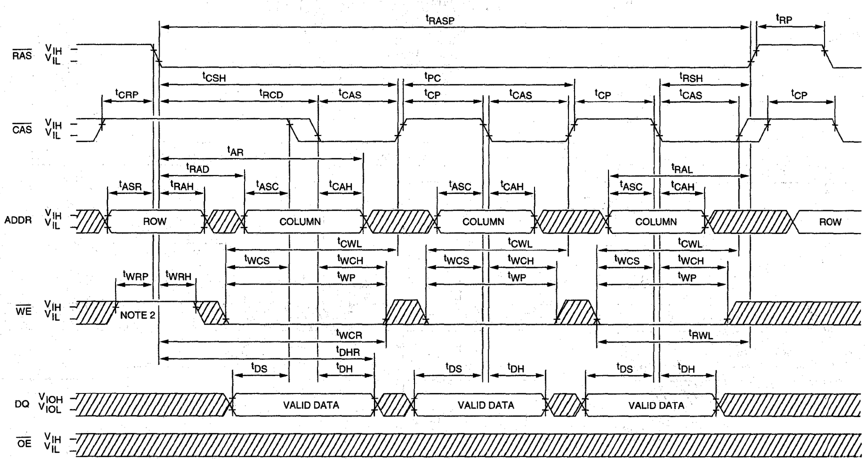
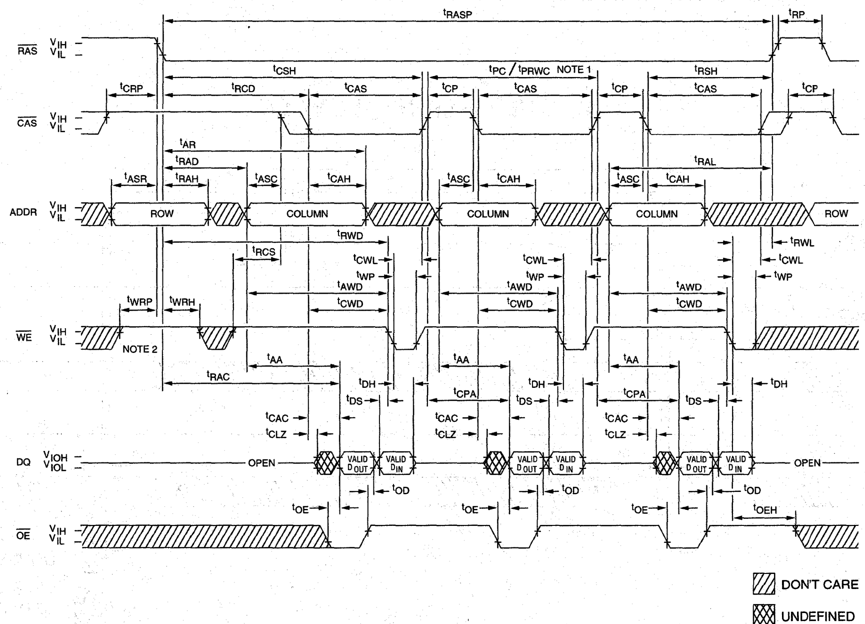
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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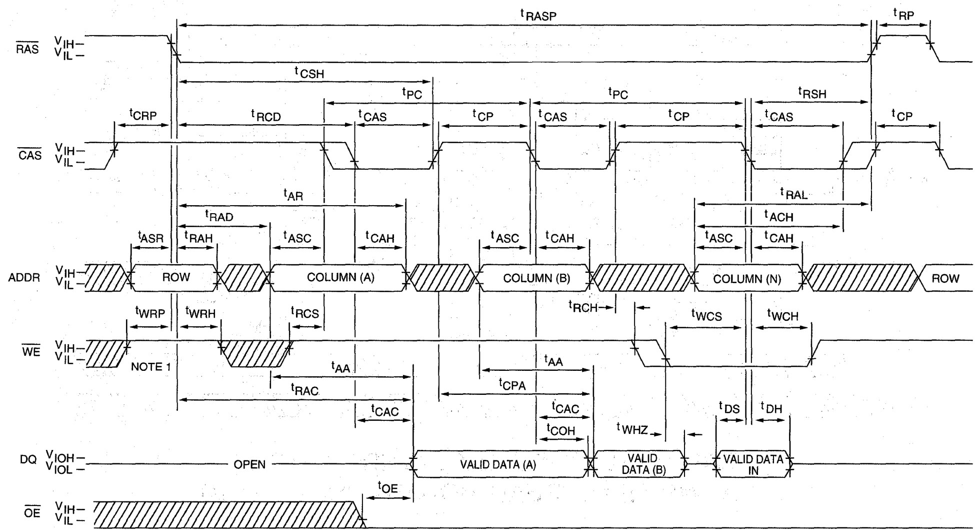
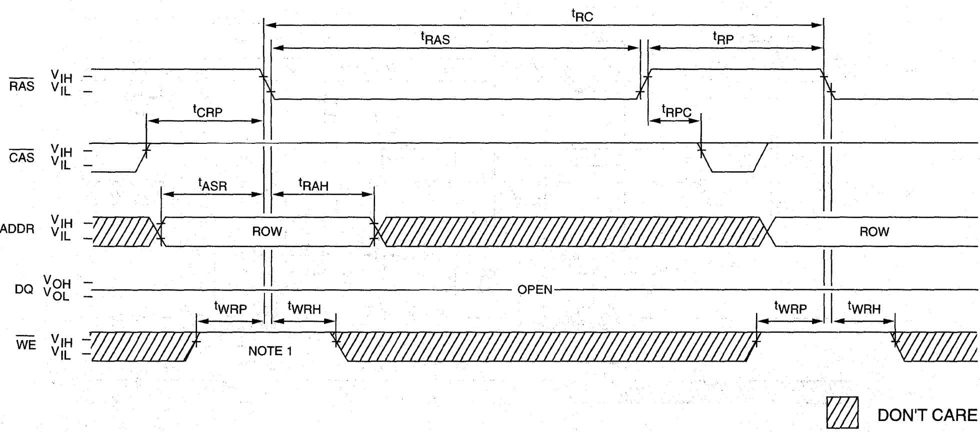
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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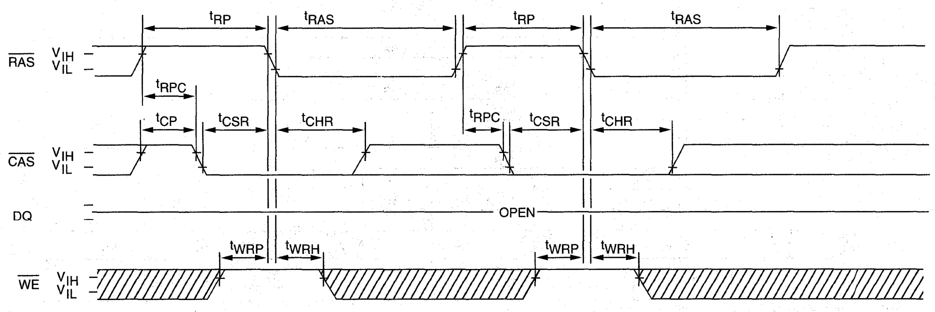
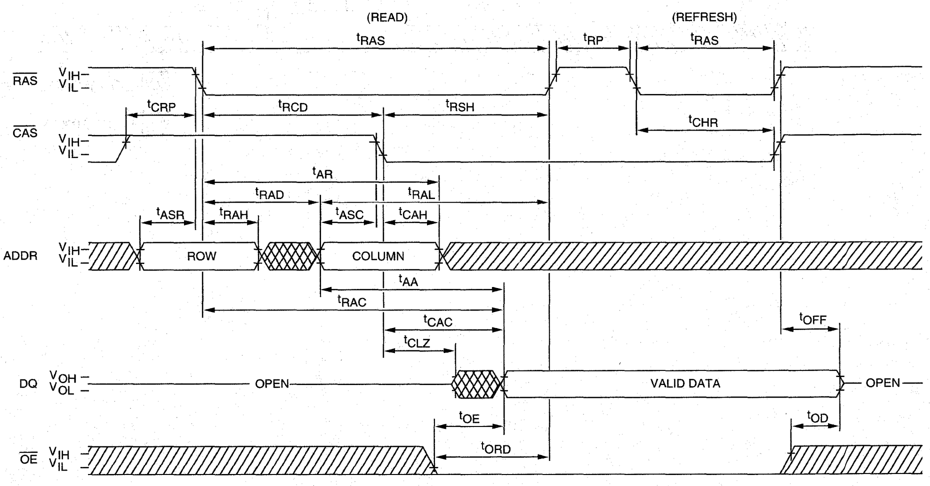
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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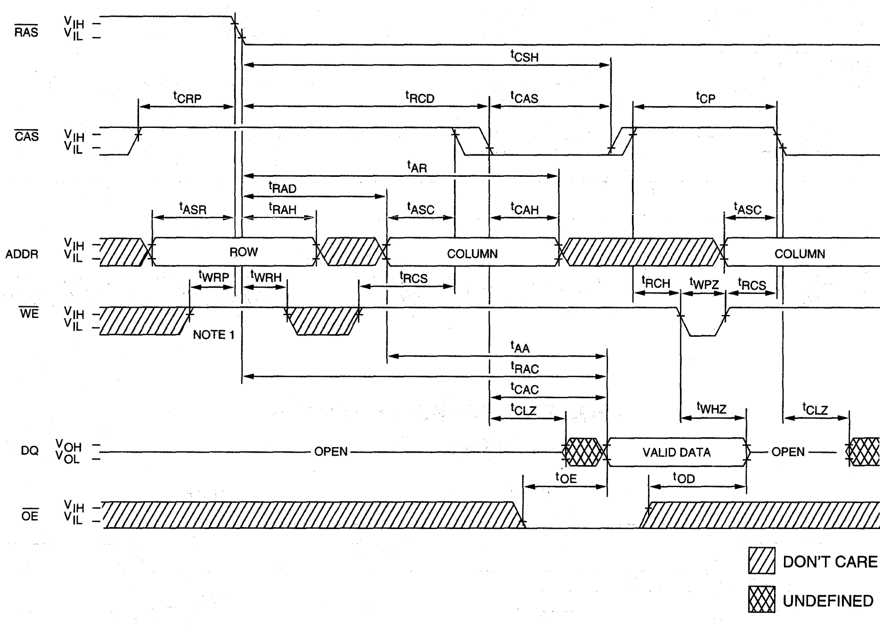
READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM

256K x 16 DRAM

5V, EDO PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 300mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Extended Data-Out (EDO) PAGE MODE access cycle
- BYTE WRITE and BYTE READ access cycles

OPTIONS — MARKING

- Timing
  - 60ns access — -6*
  - 70ns access — -7
  - 80ns access — -8
- Write Cycle Access
  - BYTE or WORD via CAS — 16270
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Part Number Example: MT4C16270DJ-7

*60ns specifications are limited to a Vcc range of ±5%. Contact factory for availability of 60ns.

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns
-8	150ns	80ns	33ns	40ns	20ns	12ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DA-7)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
NC	12	29	CASL
WE	13	28	CASH
RAS	14	27	OE
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DB-4)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
NC	14	31	CASL
WE	15	30	CASH
RAS	16	29	OE
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT4C16270 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16270 has both BYTE WRITE and WORD WRITE access cycles via two CAS pins.

The MT4C16270 offers an accelerated cycle access called EDO PAGE MODE.

The MT4C16270 CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and by the last to transition back HIGH. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS. Use of only one of the two results in a BYTE WRITE cycle. CASL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL or CASH in the same manner.

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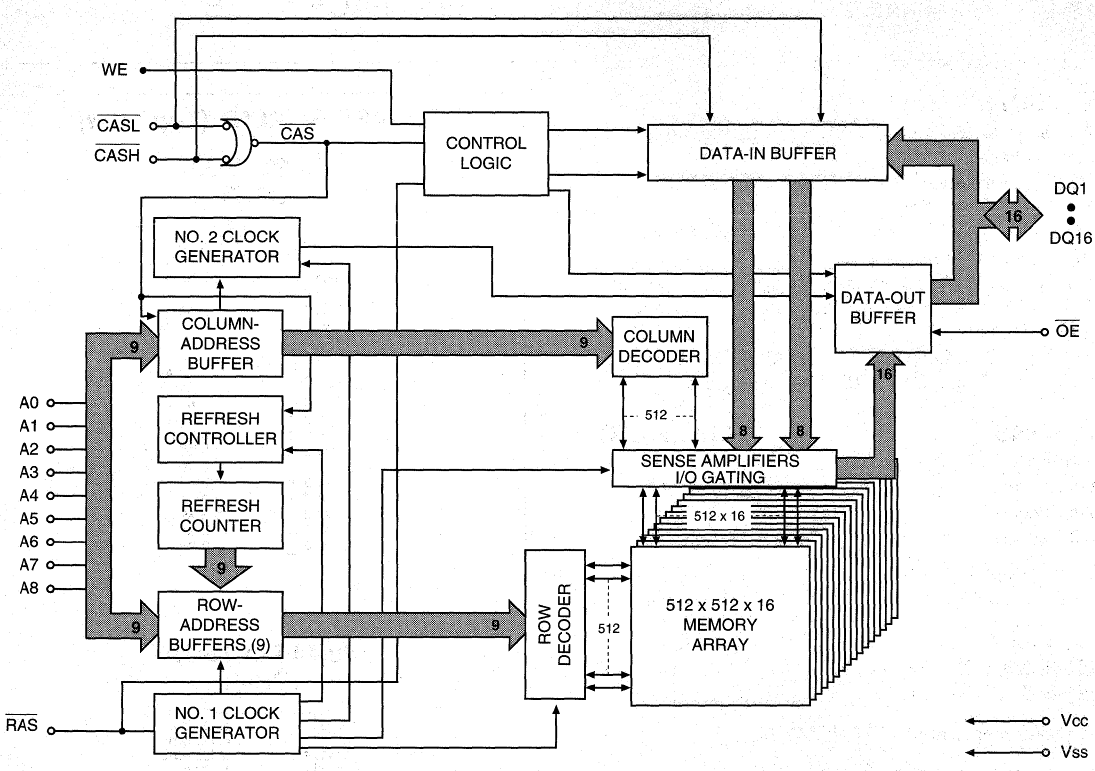
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4C16270 has two CAS controls, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE and RAS). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4C16270 CAS function is determined by the first CAS (CASL or CASH) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the MT4C16270 both byte READ and byte WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE , WE and RAS.

EDO PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the EDO PAGE MODE operation.

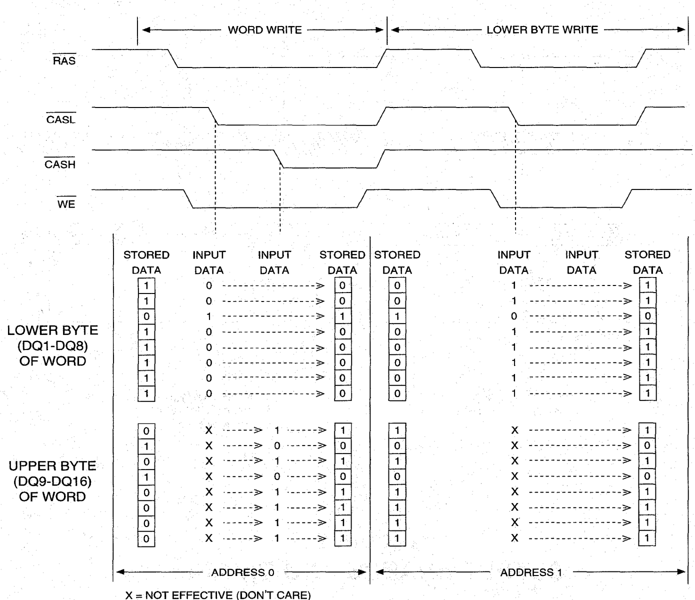

Figure 1
WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4C16270 can be viewed as two 256K x 8 DRAMs which have common input controls. Figure 1 illustrates the MT4C16270 BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. If CAS goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4C16270 offers an accelerated PAGE MODE cycle by eliminating output disable from CAS HIGH. This option is called EDO and it allows CAS precharge time (^tCP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ^tOEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ^tOEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 2 for further detail on the

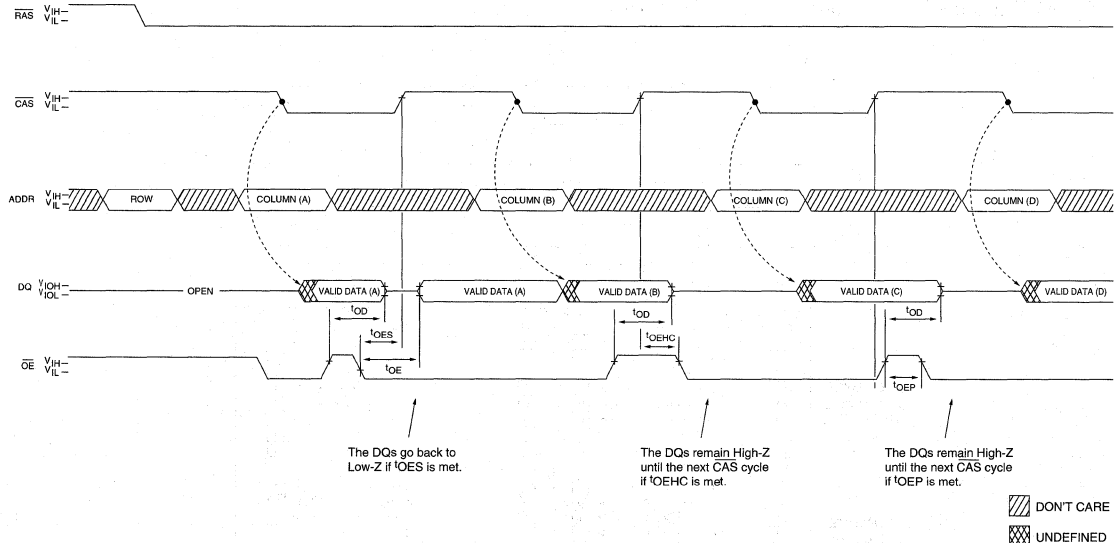

Figure 2
OUTPUT ENABLE AND DISABLE

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toggling OE condition). During other cycles, the outputs are disabled at ᵗOFF time after RAS and CAS are HIGH, or ᵗWHZ after WE transitions LOW. The ᵗOFF time is referenced from the rising edge of RAS or CAS, whichever occurs last. WE can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 3.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

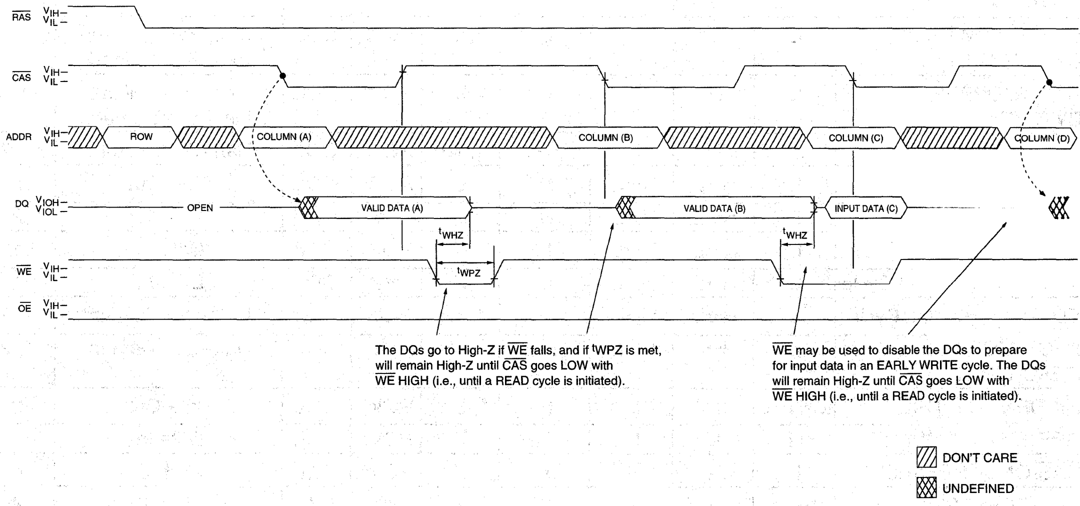

Figure 3
OUTPUT ENABLE AND DISABLE WITH WE

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{CASL}$ or $\overline{CASH}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	195	175	160	mA	3, 4, 40
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	130	125	120	mA	3, 4, 40
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	195	175	160	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS, CASL, CASH, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35		40	ns	
Column-address setup to CAS precharge during WRITE	tACH	15		15		20		ns	
Column-address hold time (referenced to RAS)	tAR	40		40		55		ns	
Column-address setup time	tASC	0		0		0		ns	29
Row-address setup time	tASR	0		0		0		ns	
Column-address to WE delay time	tAWD	55		60		65		ns	21
Access time from CAS	tCAC		15		20		20	ns	15, 31
Column-address hold time	tCAH	10		12		15		ns	29
CAS pulse width	tCAS	10	10,000	12	10,000	12	10,000	ns	37
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	5, 30
Last CAS going LOW to first CAS returning HIGH	tCLCH	10		10		10		ns	32
CAS to output in Low-Z	tCLZ	3		3		3		ns	31, 41
Data output hold after CAS LOW	tCOH	5		5		5		ns	
CAS precharge time	tCP	10		10		10		ns	16, 34
Access time from CAS precharge	tCPA		35		40		45	ns	31
CAS to RAS precharge time	tCRP	5		5		5		ns	30
CAS hold time	tCSH	40		40		60		ns	30
CAS setup time (CBR REFRESH)	tCSR	10		10		110		ns	5, 29
CAS to WE delay time	tCWD	40		45		45		ns	21, 29
Write command to CAS lead time	tCWL	10		12		12		ns	26, 30
Data-in hold time	tDH	10		15		15		ns	22, 31
Data-in hold time (referenced to RAS)	tDHR	40		40		60		ns	
Data-in setup time	tDS	0		0		0		ns	22, 31
Output disable time	tOD	3	15	3	15	3	15	ns	28, 39, 41
Output Enable time	tOE		15		20		20	ns	23, 31
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	27
OE HIGH hold time from CAS HIGH	tOEHC	10		10		10		ns	
OE HIGH pulse width	tOEP	10		10		10		ns	
OE LOW to CAS HIGH setup time	tOES	5		5		5		ns	
Output buffer turn-off delay from CAS or RAS	tOFF	3	15	3	15	3	15	ns	20, 28, 31, 41

*60ns specifications are limited to a Vcc range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		33		ns	33
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	72		79		84		ns	33
Access time from RAS	tRAC		60		70		80	ns	14
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Row-address hold time	tRAH	10		10		10		ns	
Column-address to RAS lead time	tRAL	22		27		30		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (EDO PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	tRC	110		130		150		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26, 30
Read command setup time	tRCS	0		0		0		ns	26, 29
Refresh period (512 cycles)	tREF		8		8		8	ms	
RAS precharge time	tRP	35		40		60		ns	
RAS to CAS precharge time	tRPC	10		10		10		ns	
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
RAS hold time	tRSH	10		15		15		ns	38
READ WRITE cycle time	tRWC	140		157		187		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Write command to RAS lead time	tRWL	10		12		12		ns	26
Transition time (rise or fall)	tT	2	50	2	50	2	50	ns	9, 10
Write command hold time	tWCH	10		10		10		ns	26, 38
Write command hold time (referenced to RAS)	tWCR	40		40		60		ns	26
Write command setup time	tWCS	0		0		0		ns	21, 26, 29
Output disable delay from WE	tWHZ	3	15	3	15	3	15	ns	
Write command pulse width	tWP	10		10		10		ns	26

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ${}^tREF$ refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ${}^tRCD$ < ${}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed HIGH for ${}^tCP$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ limit ensures that ${}^tRCD$ (MAX) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ${}^tWCS$, ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ${}^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^tRWD \geq {}^tRWD$ (MIN), ${}^tAWD \geq {}^tAWD$ (MIN) and ${}^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ${}^tOD$ and ${}^tOEH$ met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ${}^tOEH$ is met.
28. The DQs open during READ cycles once ${}^tOD$ or ${}^tOFF$ occur.
29. The first $\overline{CASx}$ edge to transition LOW.
30. The last $\overline{CASx}$ edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
32. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
33. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.
34. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
35. First DQs controlled by the first $\overline{CASx}$ to go LOW.
36. Last DQs controlled by the last $\overline{CASx}$ to go HIGH.
37. Each $\overline{CASx}$ must meet minimum pulse width.
38. Last $\overline{CASx}$ to go LOW.
39. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
40. Column-address changed once each cycle.
41. The 3ns minimum is a parameter guaranteed by design.

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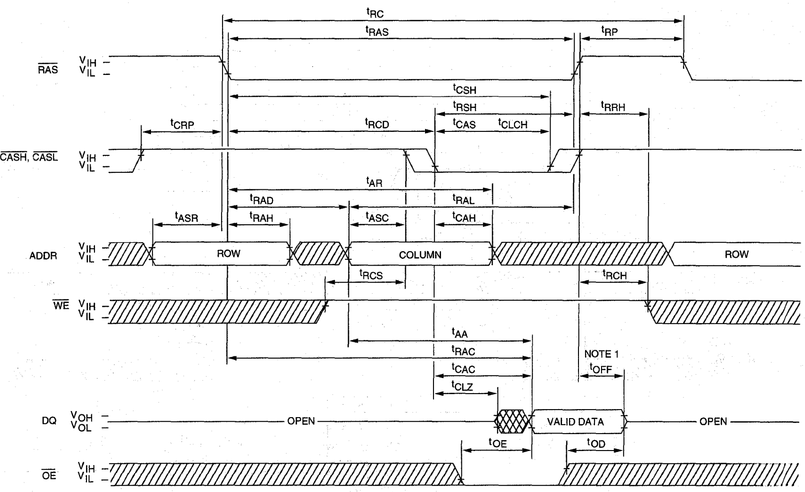
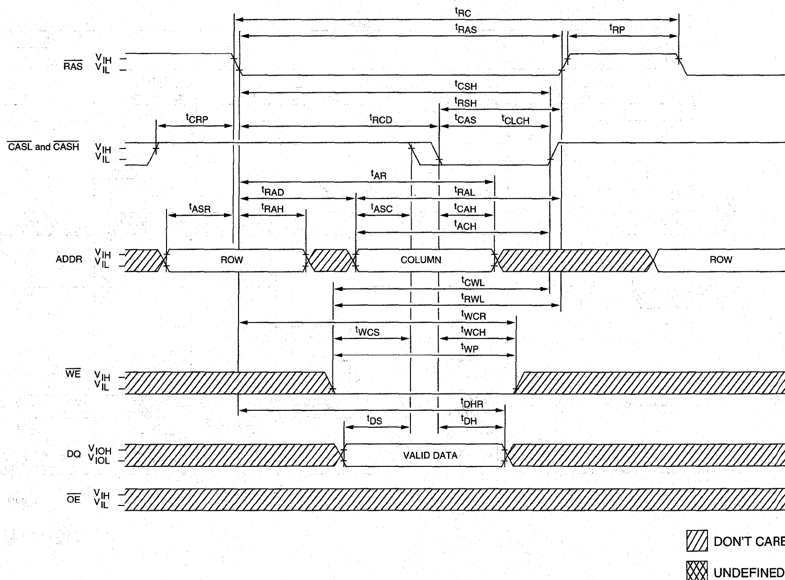
EDO DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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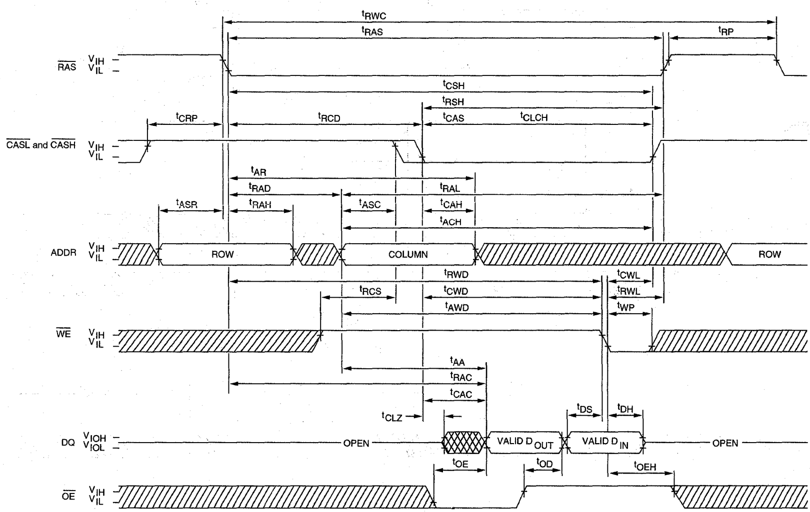
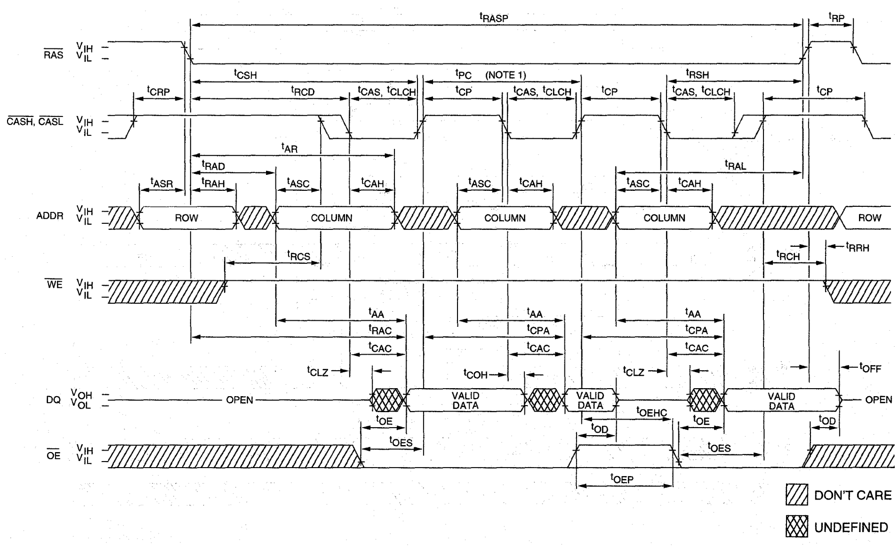
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



DON'T CARE
UNDEFINED

NOTE: 1. ^{t}PC can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the ^{t}PC specification.

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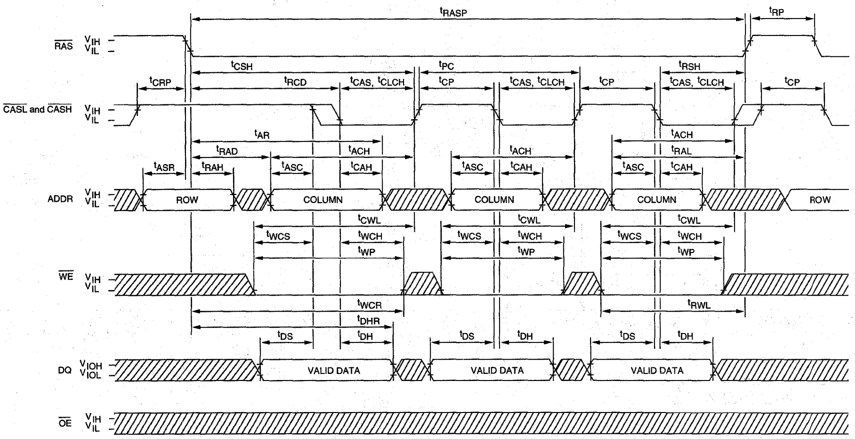
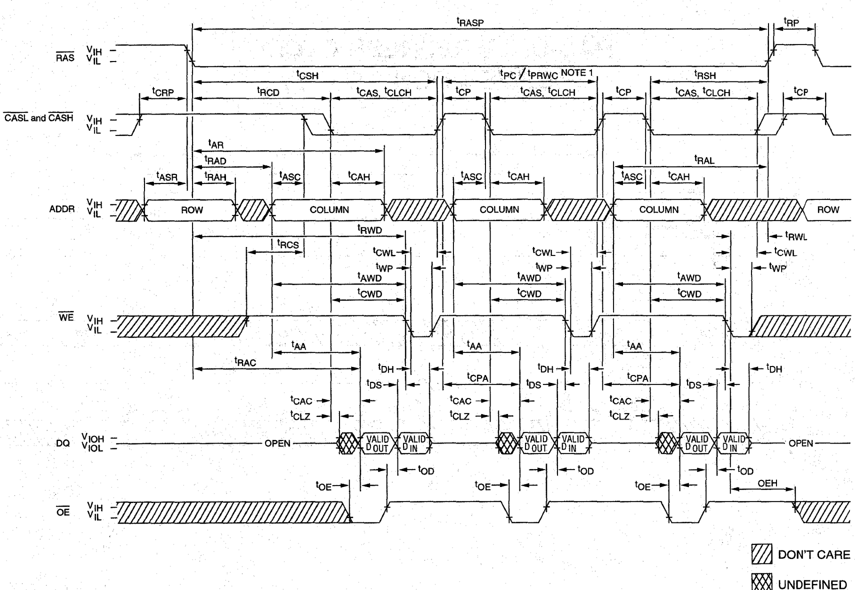
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. tPC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specification.

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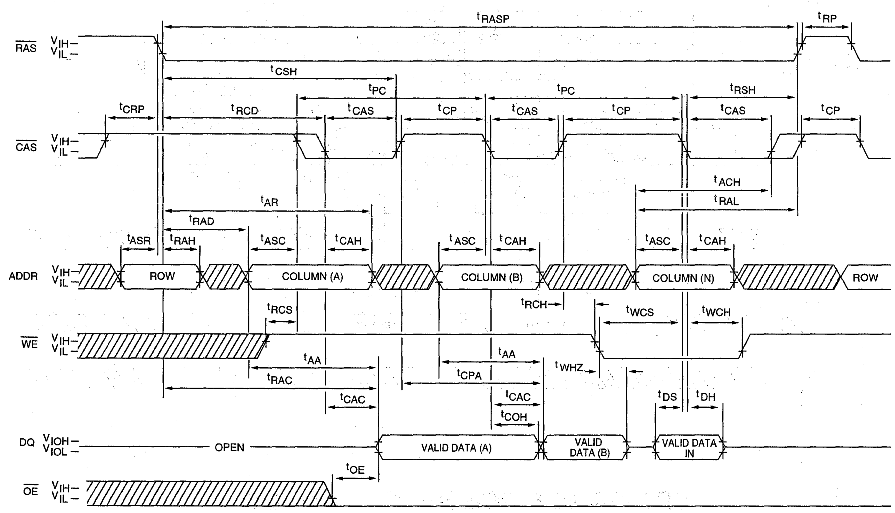
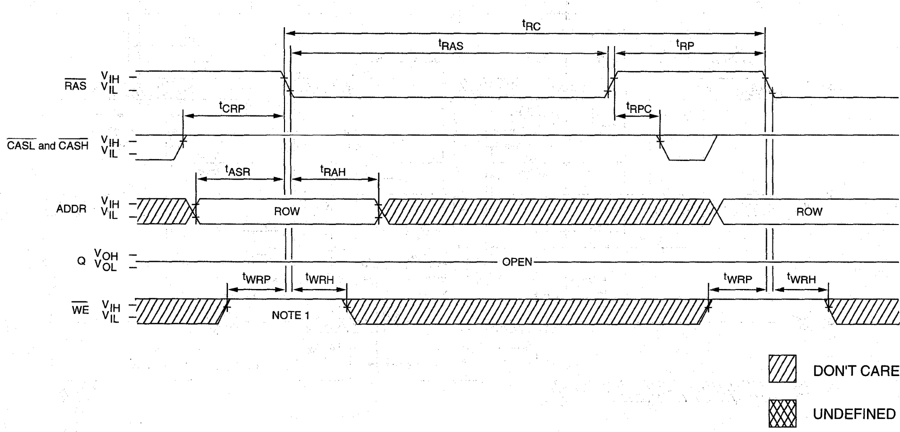
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE
(OE, WE = DON'T CARE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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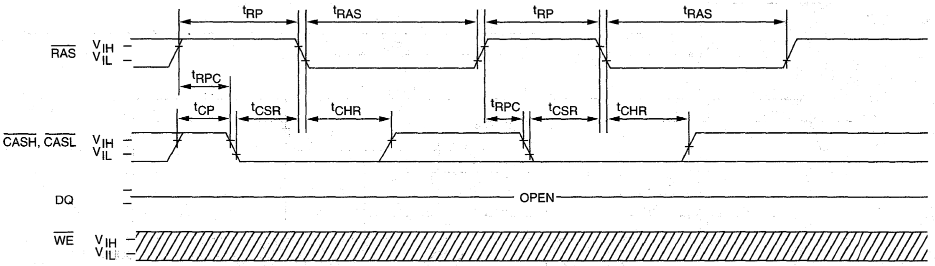
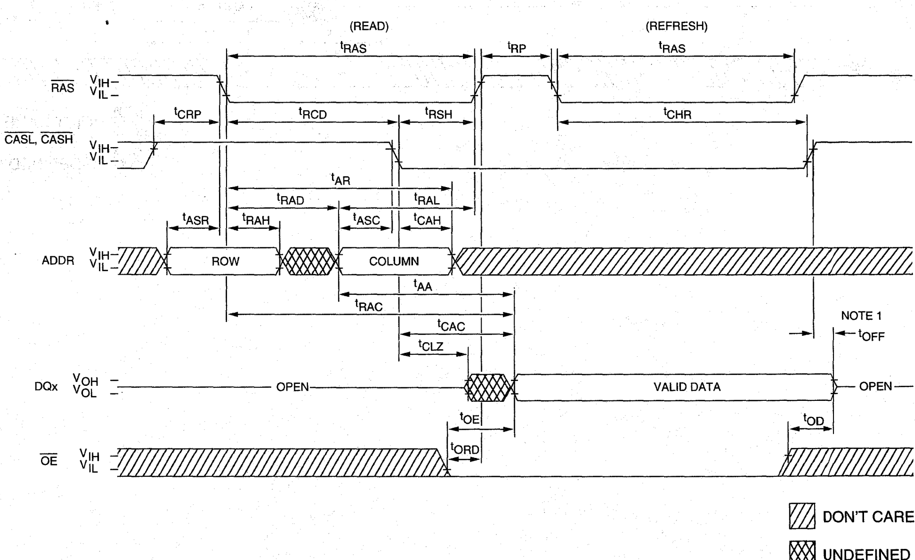
CBR REFRESH CYCLE
(Addresses; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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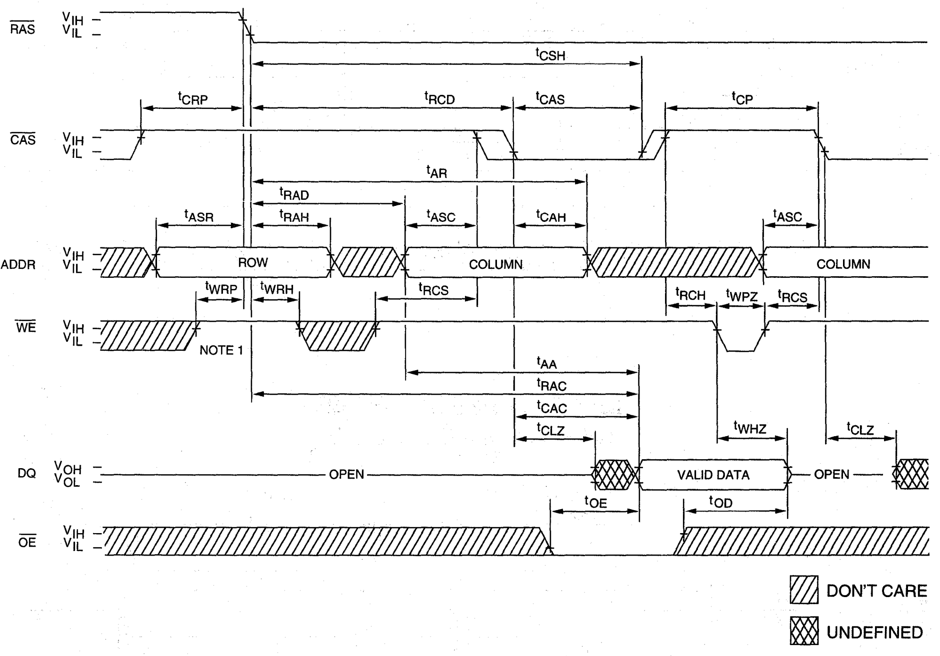
EDO DRAM

READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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ADVANCE

DRAM

256K x 16 DRAM

3.3V, EDO PAGE MODE

EDO DRAM

FEATURES

- Single +3.3V ±0.3V power supply*
- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Low power, 1mW standby; 85mW active, typical
- All device pins are TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- Extended Data-Out (EDO) PAGE MODE access cycle
- BYTE WRITE and BYTE READ access cycles

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC16270DJ-7

*60ns specifications are limited to a Vcc range of ±0.15V. Contact factory for availability of 60ns.

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns
-8	150ns	80ns	33ns	40ns	20ns	12ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DA-7)

Signal	Pin	Pin	Signal
Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
Vcc	6	35	Vss
DQ5	7	34	DQ12
DQ6	8	33	DQ11
DQ7	9	32	DQ10
DQ8	10	31	DQ9
NC	11	30	NC
NC	12	29	$\overline{CASL}$
$\overline{WE}$	13	28	$\overline{CASH}$
$\overline{RAS}$	14	27	$\overline{OE}$
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
Vcc	20	21	Vss

40/44-Pin TSOP (DB-4)

Signal	Pin	Pin	Signal
Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
Vcc	6	39	Vss
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
NC	14	31	$\overline{CASL}$
$\overline{WE}$	15	30	$\overline{CASH}$
$\overline{RAS}$	16	29	$\overline{OE}$
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
Vcc	22	23	Vss

GENERAL DESCRIPTION

The MT4LC16270 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4LC16270 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins.

The MT4LC16270 offers an accelerated access cycle called EDO PAGE MODE.

The MT4LC16270 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. $\overline{CASL}$ and $\overline{CASH}$ function in an identical manner to $\overline{CAS}$ in that either $\overline{CASL}$ or $\overline{CASH}$ will generate an internal $\overline{CAS}$. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner.

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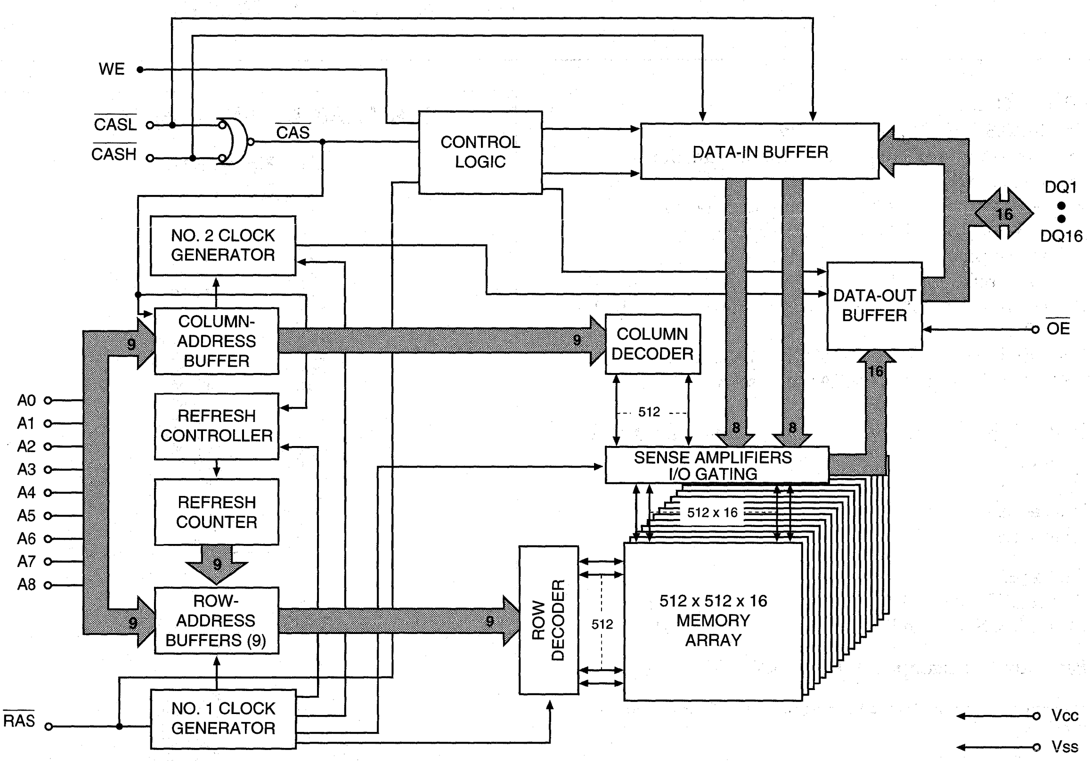
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW. The MT4LC16270 has two CAS controls, CASL and CASH.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE and RAS). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4LC16270 CAS function is determined by the first CAS (CASL or CASH) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the MT4LC16270 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE, WE and RAS.

EDO PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The EDO PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the EDO PAGE MODE operation.

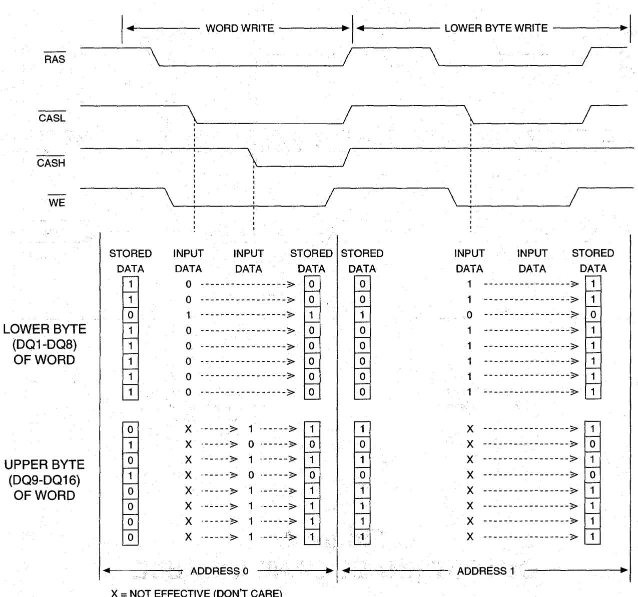

Figure 1
WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITE cycle is determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4LC16270 can be viewed as two 256K x 8 DRAMs which have common input controls. Figure 1 illustrates the MT4LC16270 BYTE WRITE and WORD WRITE cycles. The BYTE READ is accomplished in the same manner.

EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. If CAS goes HIGH, and OE is LOW (active), the output buffers will be disabled. The MT4LC16270 offer an accelerated PAGE MODE cycle by eliminating output disable from CAS HIGH. This option is called EDO and it allows CAS precharge time (^{t}CP) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

Extended data-out operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z. Using OE, there are two methods to disable the outputs and keep them disabled during the CAS HIGH time. The first method is to have OE HIGH when CAS transitions HIGH and keep OE HIGH for ^{t}OEHC. This will tristate the DQs and they will remain tristate, regardless of OE, until CAS falls again. The second method is to have OE LOW when CAS transitions HIGH. Then OE can pulse HIGH for a minimum of ^{t}OEP anytime during the CAS HIGH period and the DQs will tristate and remain tristate, regardless of OE, until CAS falls again (please reference Figure 2 for further detail on the

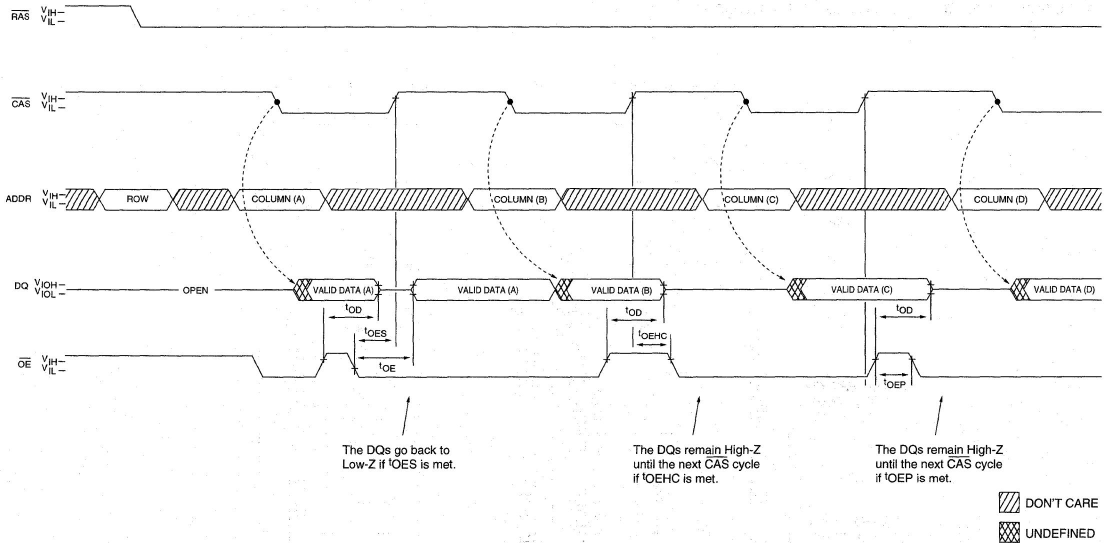

Figure 2
OUTPUT ENABLE AND DISABLE

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toggling $\overline{OE}$ condition). During other cycles, the outputs are disabled at ${}^tOFF$ time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH or ${}^tWHZ$ after $\overline{WE}$ transitions LOW. The ${}^tOFF$ time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 3.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

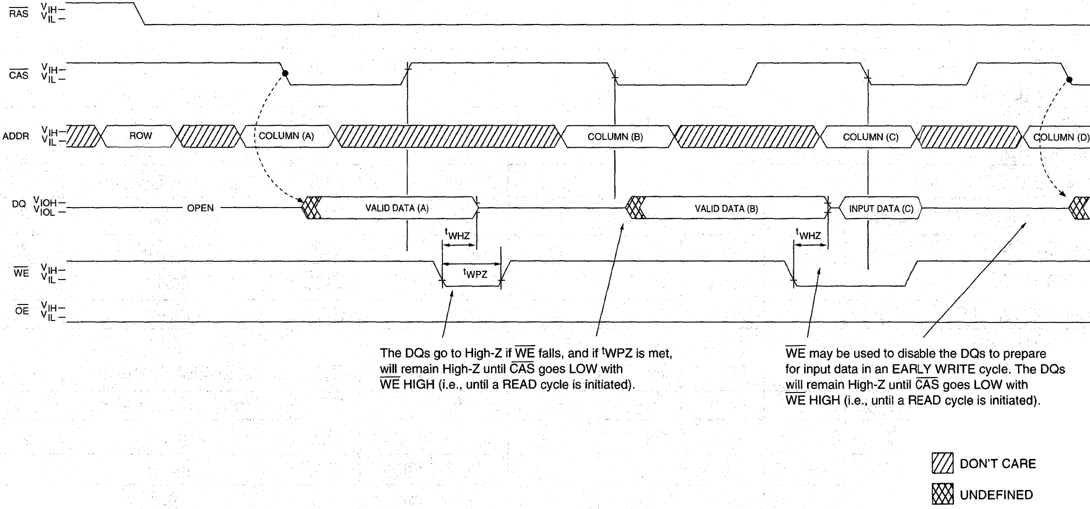

Figure 3
OUTPUT ENABLE AND DISABLE WITH $\overline{WE}$

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TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQs	NOTES
							^{t}R	^{t}C		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss........... -1V to +4.6V
Operating Temperature, T_A (ambient).......... 0°C to +70°C
Storage Temperature (plastic).................... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)**

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ Vcc+.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	Icc1	1	1	1	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	Icc2	500	500	500	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	Icc3	120	110	100	mA	3, 4, 40
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	Icc4	70	60	50	mA	3, 4, 40
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS=VIH: tRC = tRC [MIN])	Icc5	120	110	100	mA	3
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	Icc6	120	110	100	mA	3, 5

**60ns specifications are limited to a Vcc range of ±0.15V.

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CASL}}$, $\overline{\text{CASH}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35		40	ns	
Column-address setup to $\overline{\text{CAS}}$ precharge during WRITE	^{t}ACH	15		15		20		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	40		40		55		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	29
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	55		60		65		ns	21
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20		20	ns	15, 31
Column-address hold time	^{t}CAH	10		12		15		ns	29
$\overline{\text{CAS}}$ pulse width	^{t}CAS	10	10,000	12	10,000	12	10,000	ns	37
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5, 30
Last $\overline{\text{CAS}}$ going LOW to first $\overline{\text{CAS}}$ returning HIGH	^{t}CLCH	10		10		10		ns	32
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	31, 41
Data output hold after $\overline{\text{CAS}}$ LOW	^{t}COH	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		10		ns	16, 34
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40		45	ns	31
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	5		5		5		ns	30
$\overline{\text{CAS}}$ hold time	^{t}CSH	40		40		60		ns	30
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		110		ns	5, 29
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	40		45		45		ns	21, 29
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	10		12		12		ns	26, 30
Data-in hold time	^{t}DH	10		15		15		ns	22, 31
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	40		40		60		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22, 31
Output disable time	^{t}OD	3	15	3	15	3	15	ns	28, 39, 41
Output Enable time	^{t}OE		15		20		20	ns	23, 31
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	27
$\overline{\text{OE}}$ HIGH hold time from $\overline{\text{CAS}}$ HIGH	^{t}OEHC	10		10		10		ns	
$\overline{\text{OE}}$ HIGH pulse width	^{t}OEP	10		10		10		ns	
$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH setup time	^{t}OES	5		5		5		ns	

*60ns specifications are limited to a V_{CC} range of ±0.15V.

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EDO DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)*

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay from $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	^{t}OFF	3	15	3	15	3	15	ns	20, 28, 31, 41
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		33		ns	33
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	72		79		84		ns	33
Access time from $\overline{\text{RAS}}$	^{t}RAC		60	70		80	ns	14	
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Row-address hold time	^{t}RAH	10		10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	22		27		30		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ pulse width (EDO PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		0		ns	19, 26, 30
Read command setup time	^{t}RCS	0		0		0		ns	26, 29
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
$\overline{\text{RAS}}$ precharge time	^{t}RP	35		40		60		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	10		10		10		ns	
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		0		ns	19
$\overline{\text{RAS}}$ hold time	^{t}RSH	10		15		15		ns	38
READ WRITE cycle time	^{t}RWC	140		157		187		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	85		95		105		ns	21
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	10		12		12		ns	26
Transition time (rise or fall)	^{t}T	2	50	2	50	2	50	ns	
Write command hold time	^{t}WCH	10		10		10		ns	26, 38
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	40		40		60		ns	26
Write command setup time	^{t}WCS	0		0		0		ns	21, 26, 29
Output disable delay from $\overline{\text{WE}}$	^{t}WHZ	3	15	3	15	3	15	ns	
Write command pulse width	^{t}WP	10		10		10		ns	26

*60ns specifications are limited to a Vcc range of ±0.15V.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS and RAS = V_{IH}, data output is High-Z.
12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF, V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS and RAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS and RAS or OE go back to V_{IH}) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW result in a LATE WRITE (OE-controlled) cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as WE going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if CAS remains LOW and OE is taken back LOW after ^{t}OEH is met.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
29. The first CASx edge to transition LOW.
30. The last CASx edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding CAS input, DQ1-DQ8 by CASL and DQ9-DQ16 by CASH.
32. Last falling CASx edge to first rising CASx edge.
33. Last rising CASx edge to next cycle's last rising CASx edge.
34. Last rising CASx edge to first falling CASx edge.
35. First DQs controlled by the first CASx to go LOW.
36. Last DQs controlled by the last CASx to go HIGH.
37. Each CASx must meet minimum pulse width.
38. Last CASx to go LOW.
39. All DQs controlled, regardless CASL and CASH.
40. Column-address changed once each cycle.
41. The 3ns minimum is a parameter guaranteed by design.

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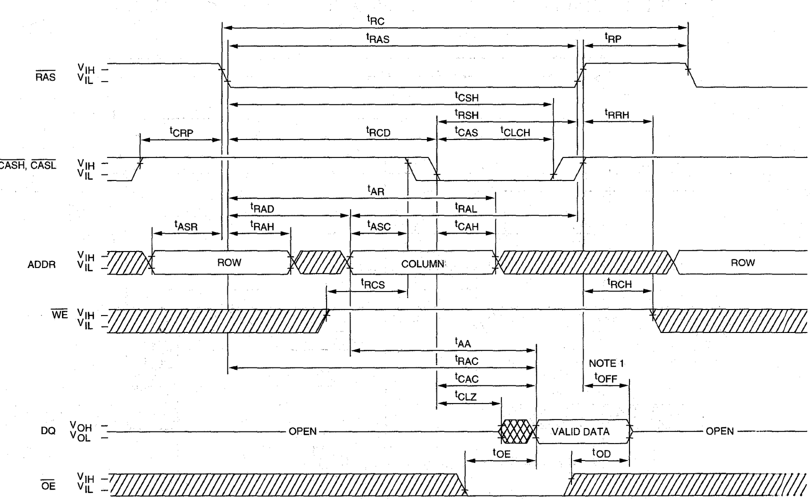
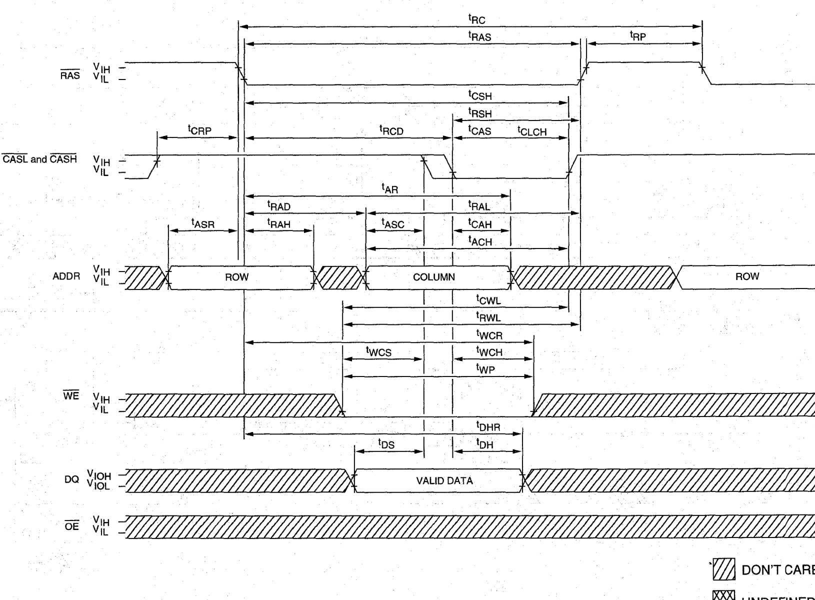
READ CYCLE



EARLY WRITE CYCLE



NOTE: 1. ^{t}OFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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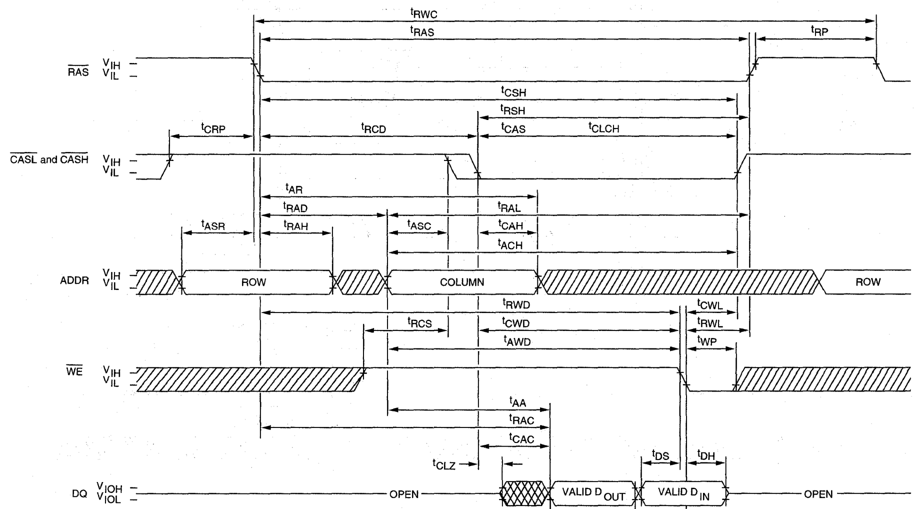
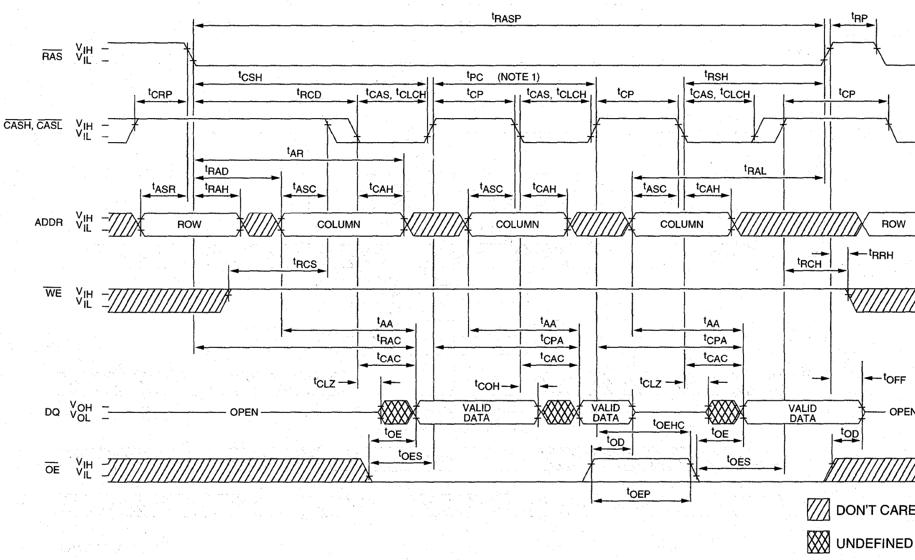
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. ^{t}PC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the ^{t}PC specification.

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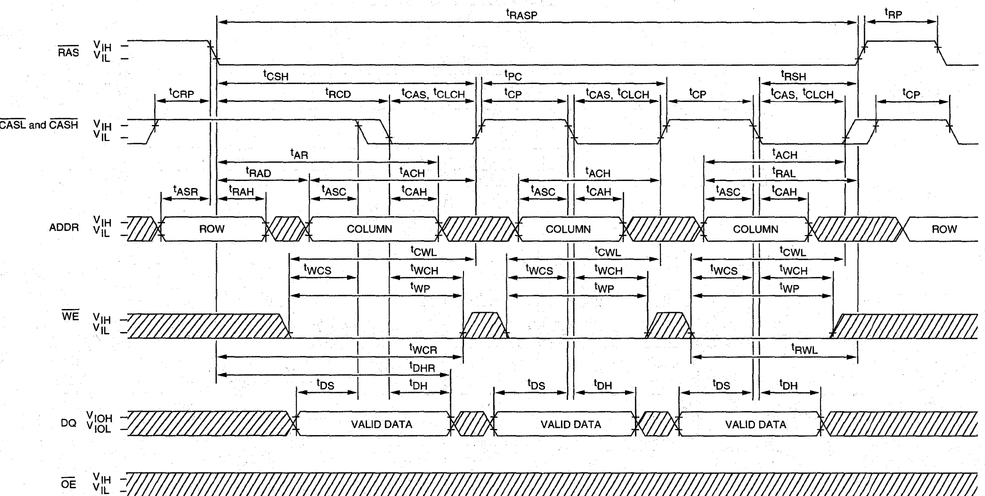
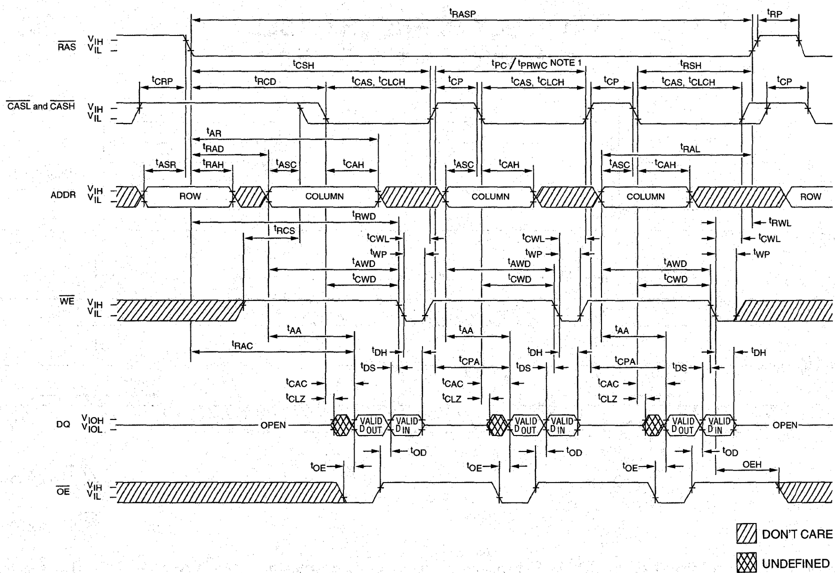
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. tPC can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specification.

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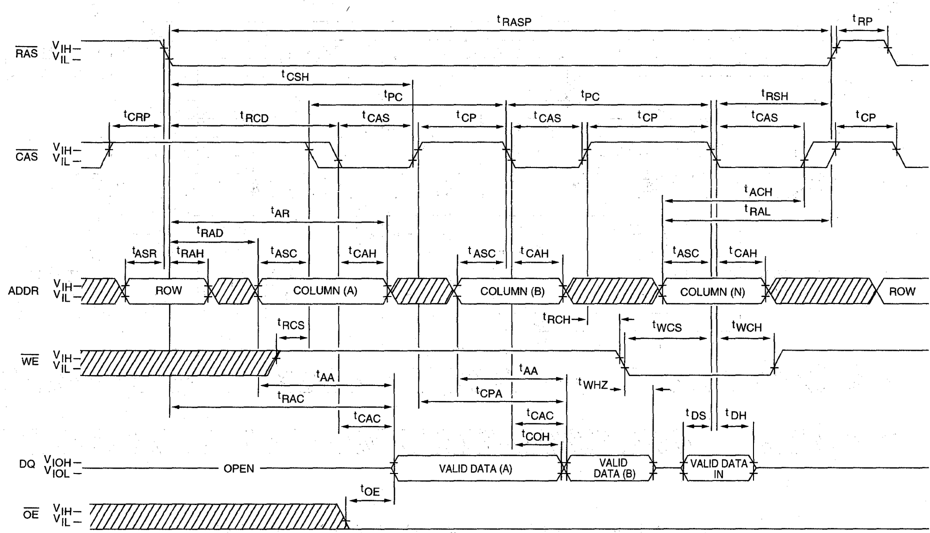
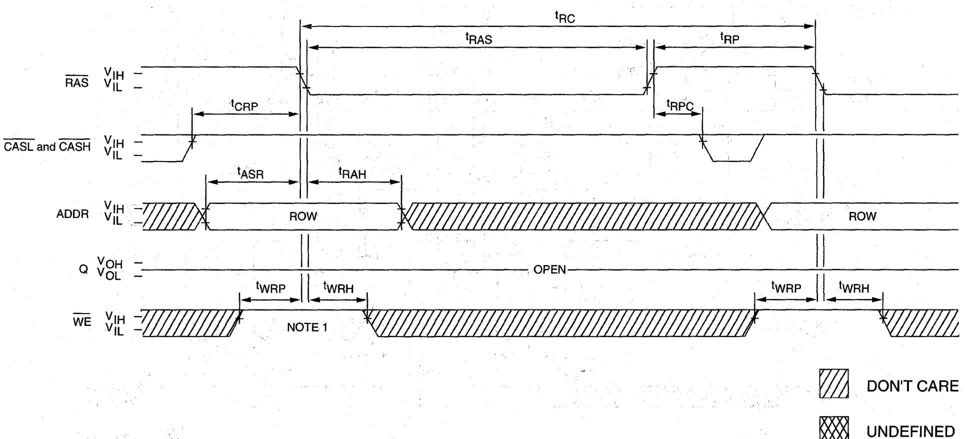
EDO DRAM

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE
(OE, WE = DON'T CARE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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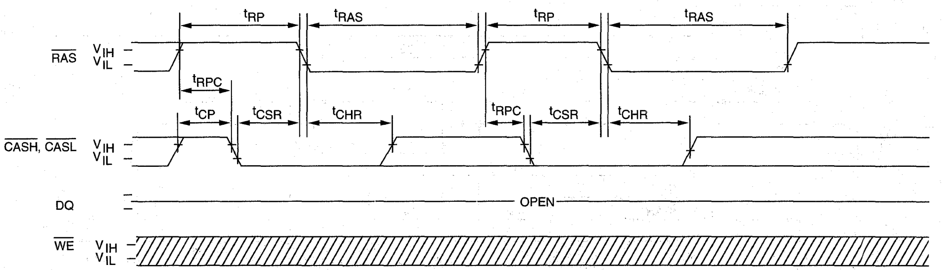
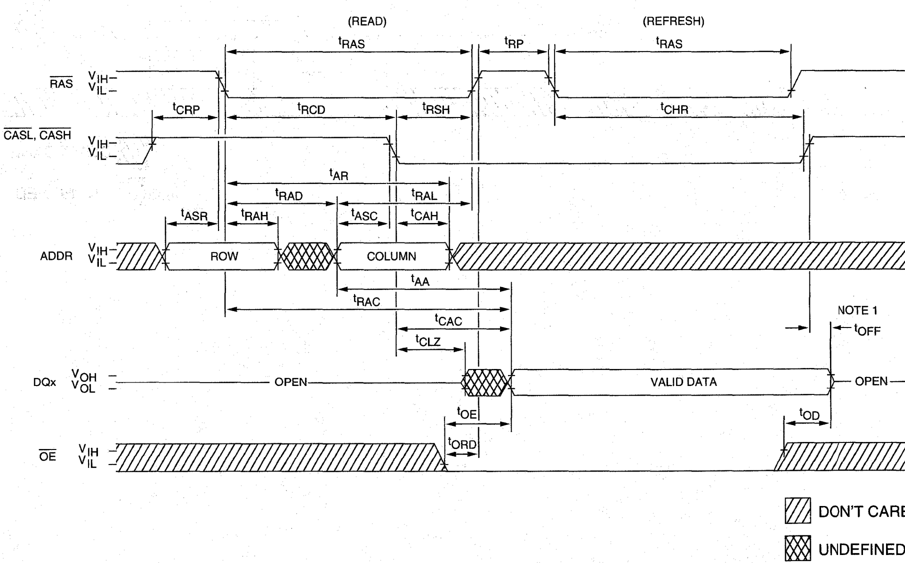
CBR REFRESH CYCLE
(Addresses; $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE 24
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. tOFF is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

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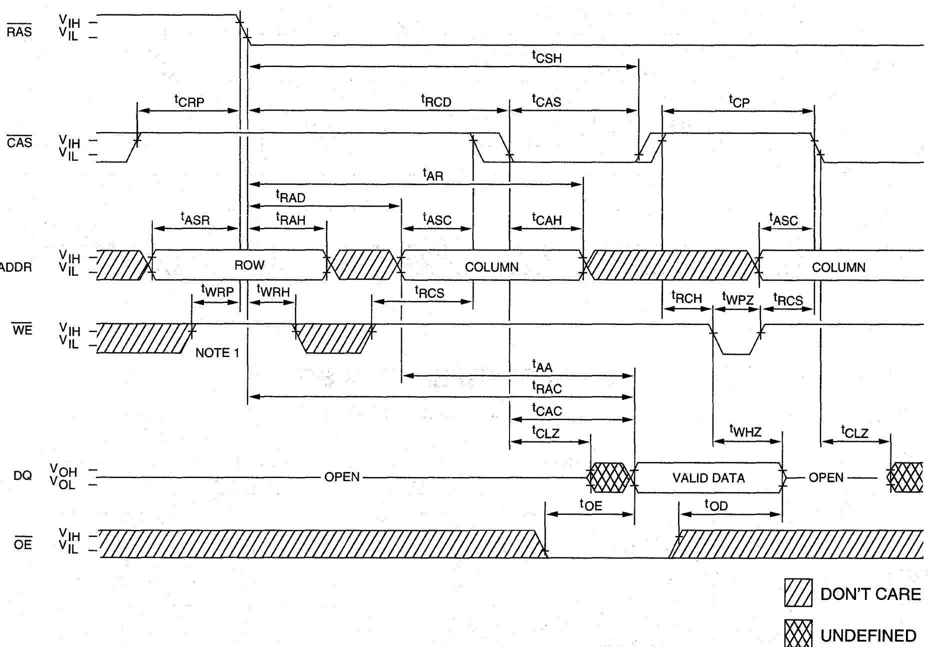
READ CYCLE
(with WE-controlled disable)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM

1 MEG x 16 DRAM

3.3V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 180mW active, typical
- Optional SELF REFRESH mode, with Extended Refresh rate (8x)
- Extended Data-Out (EDO) PAGE access cycle
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic TSOP (400 mil)	TG

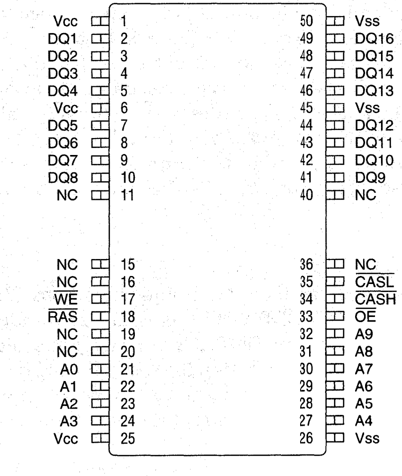
- Part Number Example: MT4LC1M16E5TG-7 S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP
(DB-5)



GENERAL DESCRIPTION

The MT4LC1M16E5(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16E5(S) has both BYTE WRITE and WORD WRITE access cycles via two CAS pins (CASL and CASH). These function in an identical manner to a single CAS of other DRAMs in that either CASL or CASH will generate an internal CAS.

The MT4LC1M16E5(S) CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and the last CAS to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. The CAS function also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

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GENERAL DESCRIPTION (continued)

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4LC1M16E5(S) both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the PAGE MODE of operation.

EDO PAGE MODE

The MT4LC1M16E5(S) provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS returns HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z (refer to Figure 1). WE can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS HIGH time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last.

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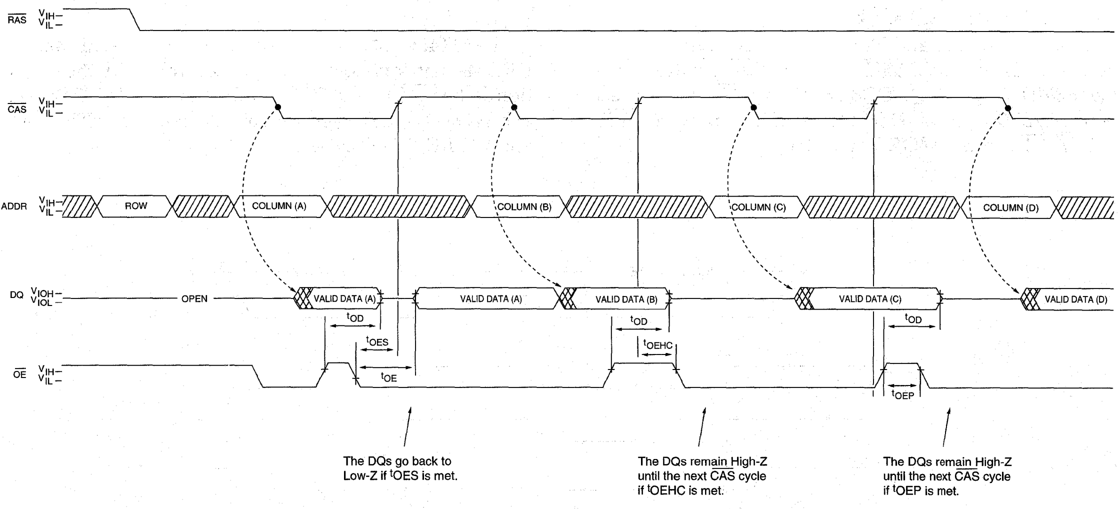

Figure 1
OUTPUT ENABLE AND DISABLE

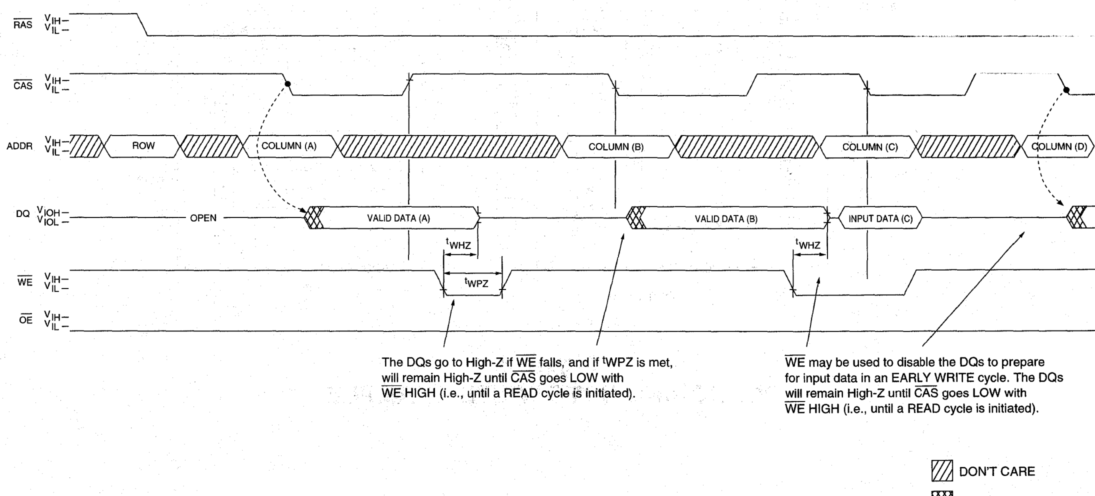

Figure 2
WE CONTROL OF DQs

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BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE access (DQ1-DQ8). Enabling CASH will select an upper BYTE access (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4LC1M16E5(S) may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 3 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 4 illustrates BYTE READ and WORD READ cycles.

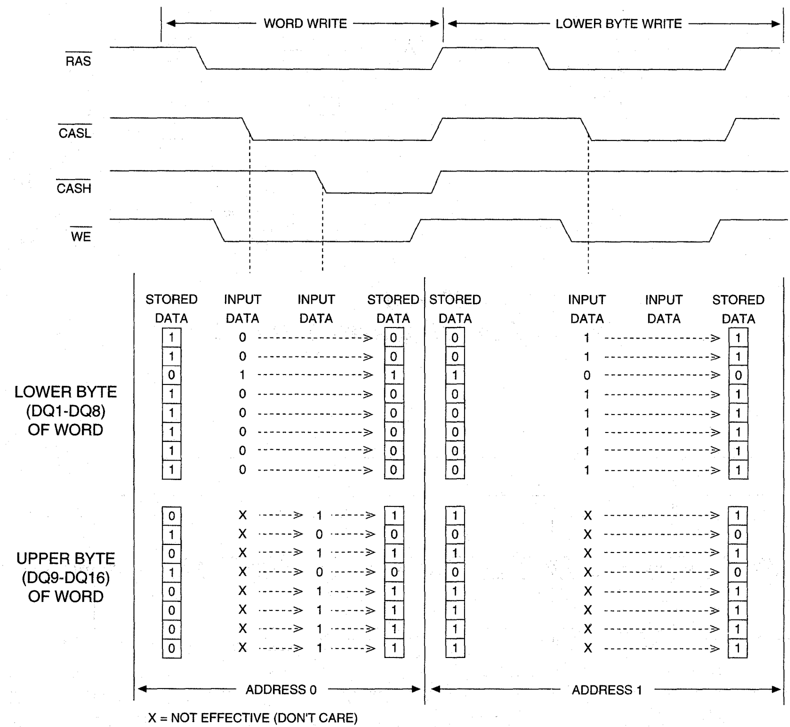

Figure 3
WORD AND BYTE WRITE EXAMPLE

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REFRESH

Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC1M16E5 S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms four times longer than the standard 16ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs prior to the resumption of normal operation.

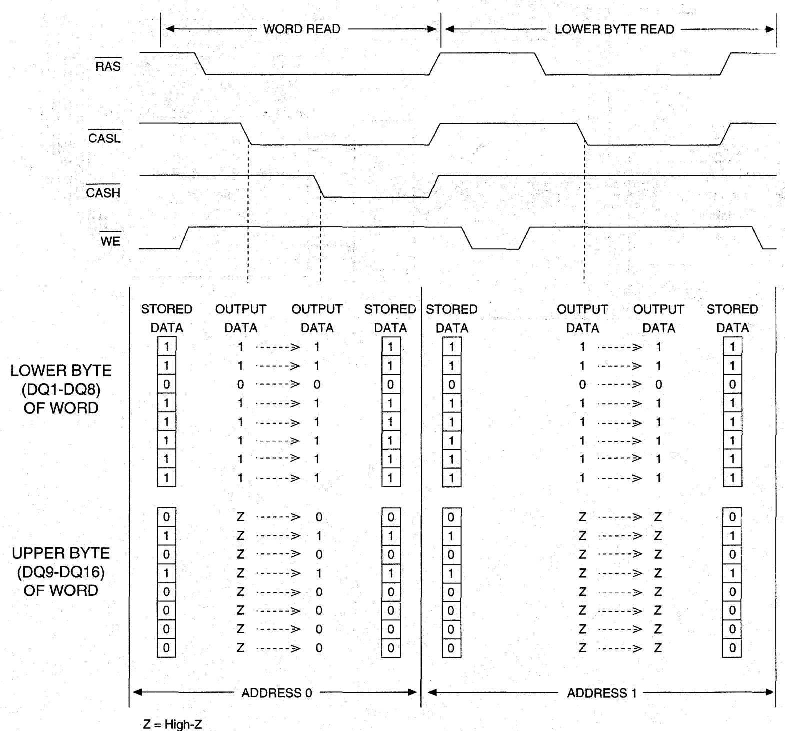

Figure 4
WORD AND BYTE READ EXAMPLE

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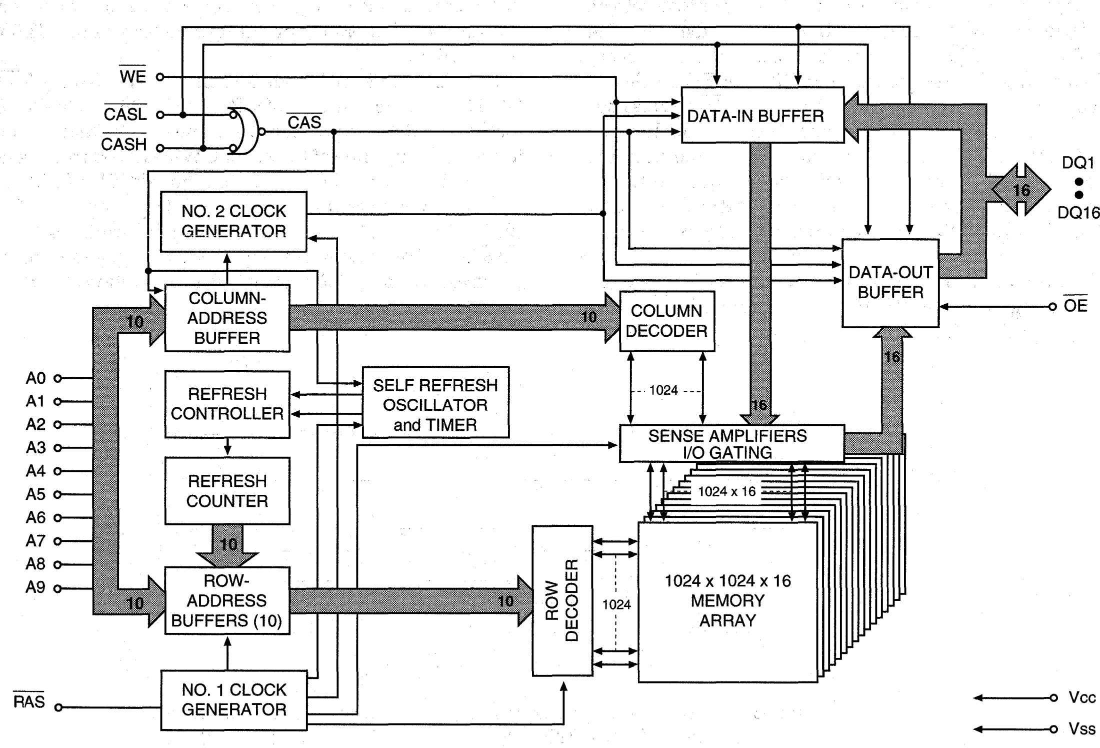
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
EDO-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{CASL}$ or $\overline{CASH}$ active).
3. EARLY WRITE only.
4. Only one $\overline{CAS}$ must be active ($\overline{CASL}$ or $\overline{CASH}$).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.0mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	500	500	µA	25
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	155	mA	3, 4, 26
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	140	130	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	160	145	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	150	140	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; $\overline{OE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0-A9, $\overline{OE}$, and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$,$\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address set-up to $\overline{CAS}$ precharge during WRITE	^tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		ns	
Column-address setup time	^tASC	0		0		ns	30
Row-address setup time	^tASR	0		0		ns	30
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15, 32
Column-address hold time	^tCAH	10		12		ns	30
$\overline{CAS}$ pulse width	^tCAS	10	10,000	12	10,000	ns	38
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	15		15		ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		12		ns	5, 31
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		ns	33
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	32
Data output hold after next $\overline{CAS}$ LOW	^tCOH	5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	35
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	32
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	31
$\overline{CAS}$ hold time	^tCSH	50		55		ns	31
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5, 30
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		ns	21, 30
Write command to $\overline{CAS}$ lead time	^tCWL	15		15		ns	26, 31
Data-in hold time	^tDH	10		12		ns	22, 32
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22, 32
Output disable	^tOD	0	15	0	15	ns	29, 41
Output Enable	^tOE		15		15	ns	32
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		12		ns	28
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	^tOEHC	10		10		ns	28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ HIGH pulse width	tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	0	15	0	15	ns	20, 32
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	75		85		ns	34
Access time from $\overline{RAS}$	tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	tRAD	12	30	12	35	ns	18
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	tRASS	100		100		µs	27
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	14	45	14	50	ns	17, 30
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19, 26, 31
Read command setup time	tRCS	0		0		ns	26, 30
Refresh period (1,024 cycles)	tREF		16		16	ms	28
Refresh period (1,024 cycles) S version	tREF		128		128	ms	28
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	tRPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{RAS}$ hold time	tRSH	10		12		ns	39
READ WRITE cycle time	tRWC	150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	80		90		ns	21
Write command to $\overline{RAS}$ lead time	tRWL	15		15		ns	26
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	10		12		ns	26, 39
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	26
$\overline{WE}$ command setup time	tWCS	0		0		ns	21, 26, 30
Output disable delay from $\overline{WE}$	tWHZ	0	10	0	15	ns	
Write command pulse width	tWP	10		12		ns	26
$\overline{WE}$ pulse width to disable at $\overline{CAS}$ HIGH	tWPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	26
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	26

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate, 50pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at 0.2V or V_{CC} -0.2V.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR REFRESH cycles are employed.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.

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NOTES (continued)

30. The first $\overline{CAS}$x edge to transition LOW.
31. The last $\overline{CAS}$x edge to transition HIGH.
32. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
33. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
36. First DQs controlled by the first $\overline{CAS}$x to go LOW.
37. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
38. Each $\overline{CAS}$x must meet minimum pulse width.
39. Last $\overline{CAS}$x to go LOW.
40. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

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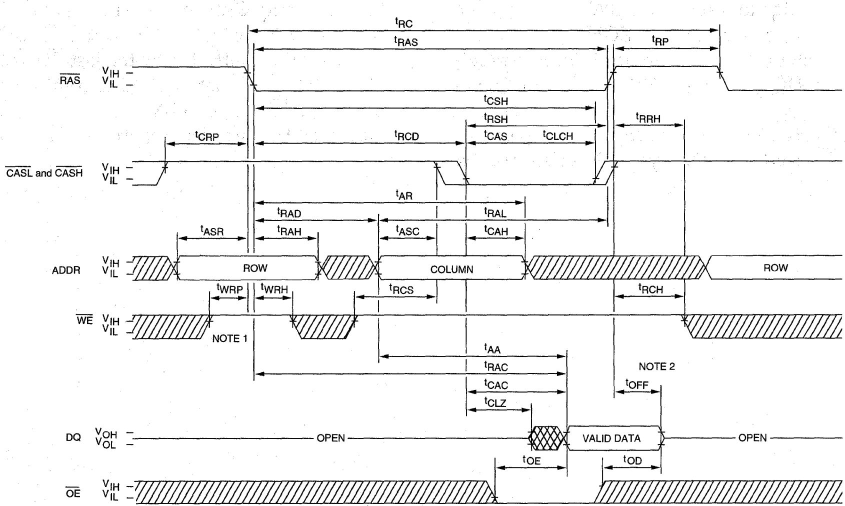
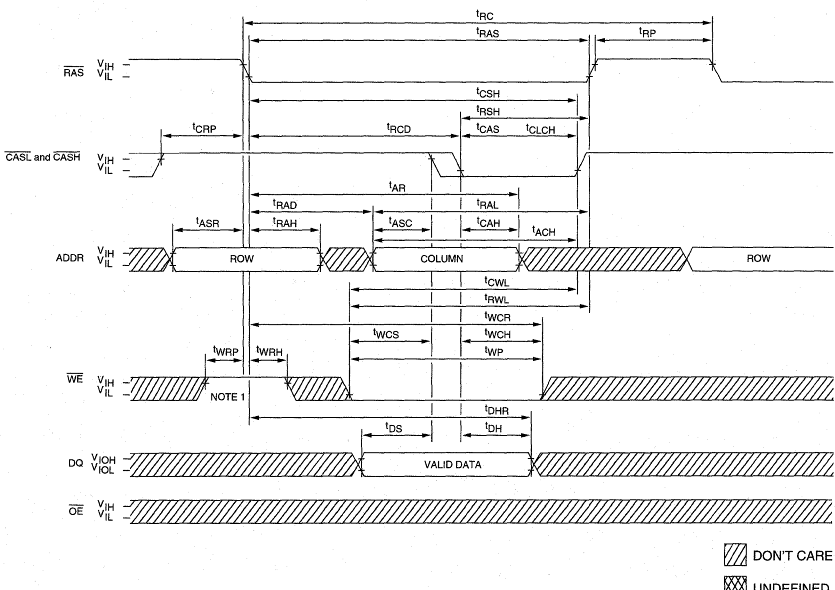
READ CYCLE



EARLY WRITE CYCLE



NOTE:

1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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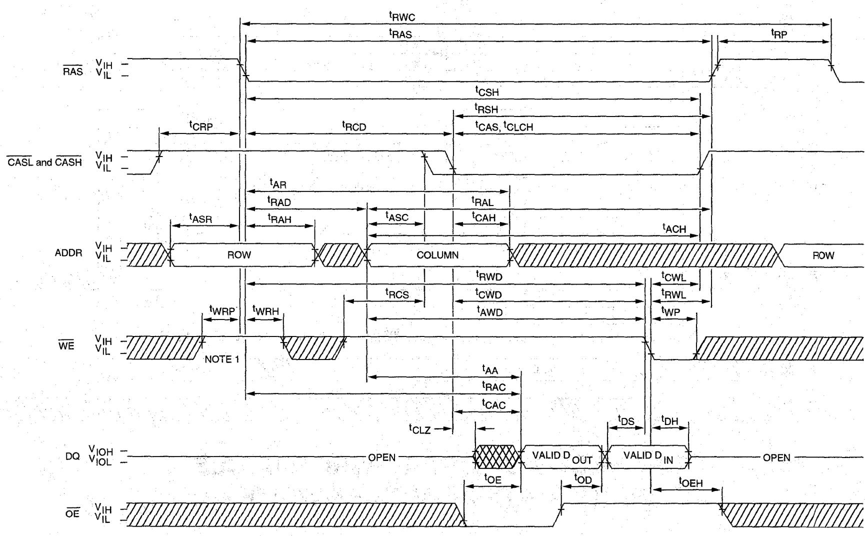
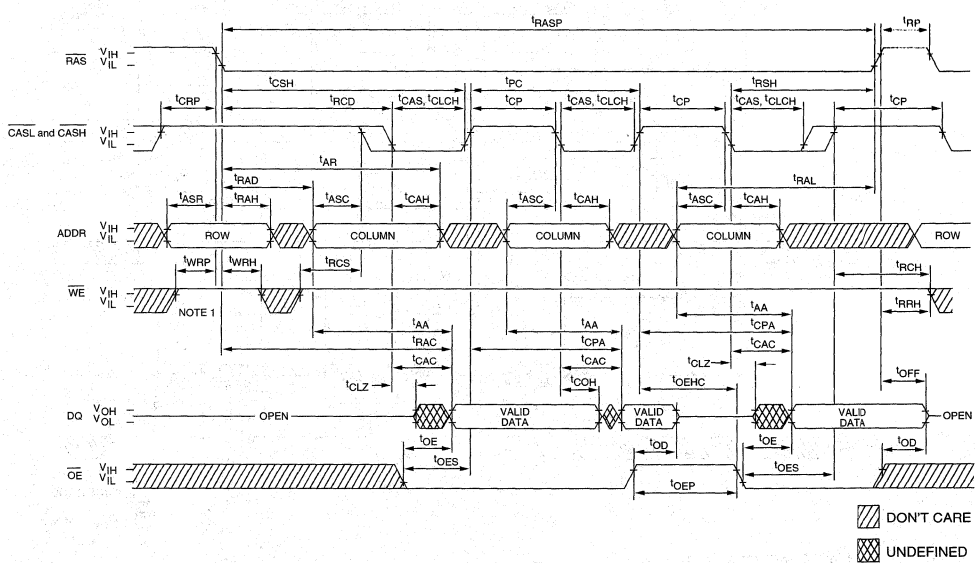
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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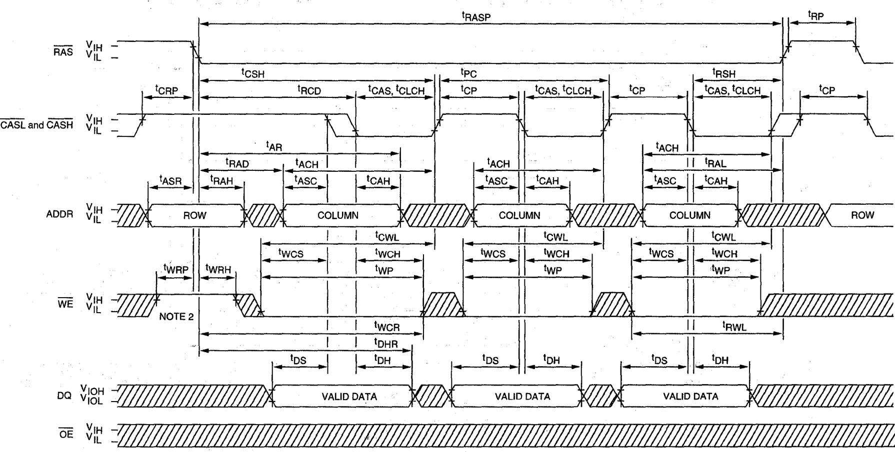
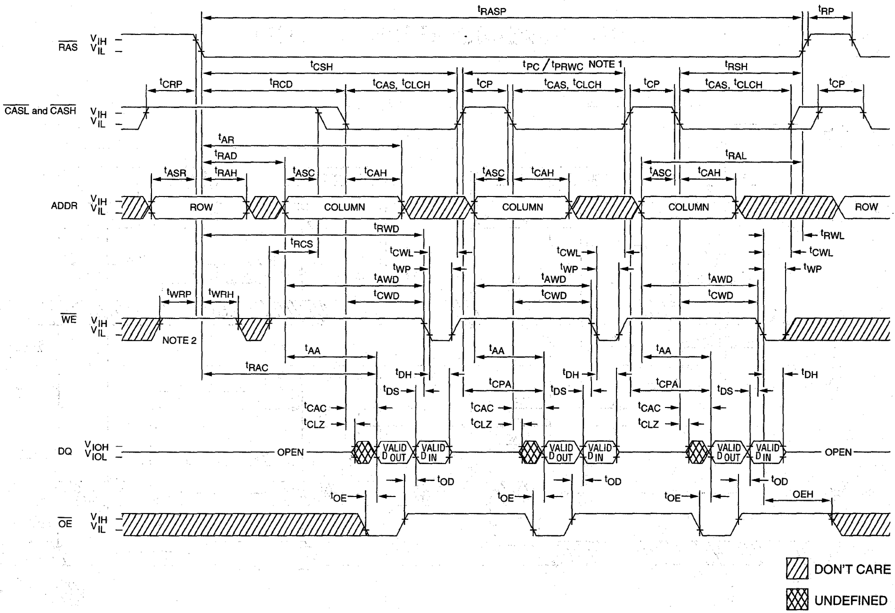
EDO-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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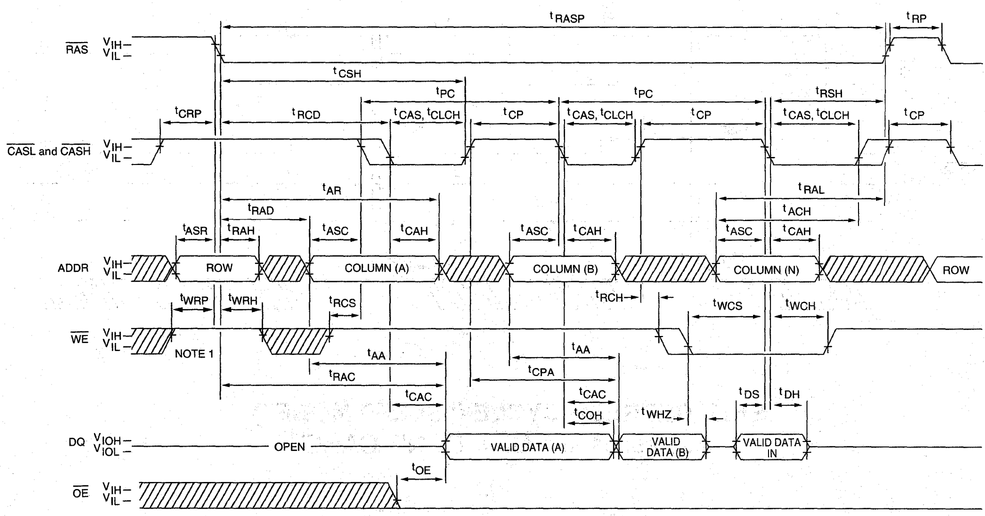
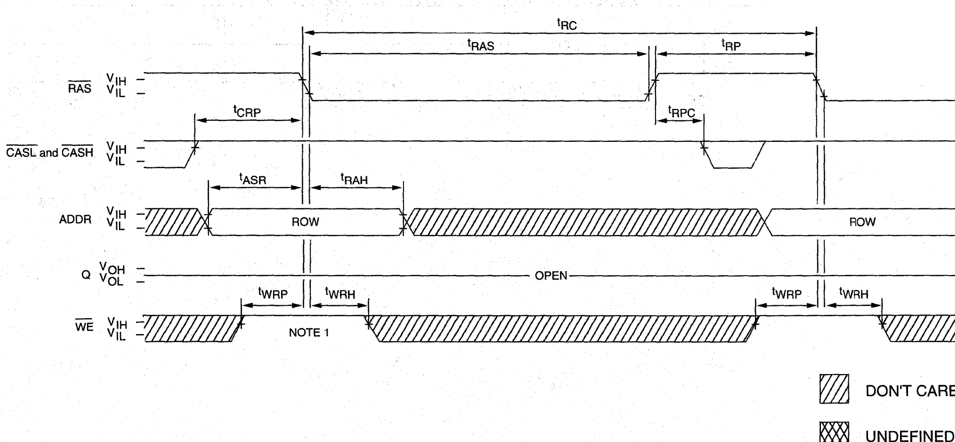
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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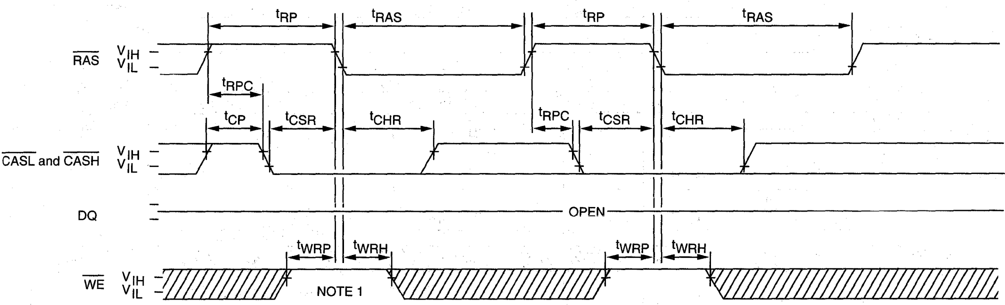
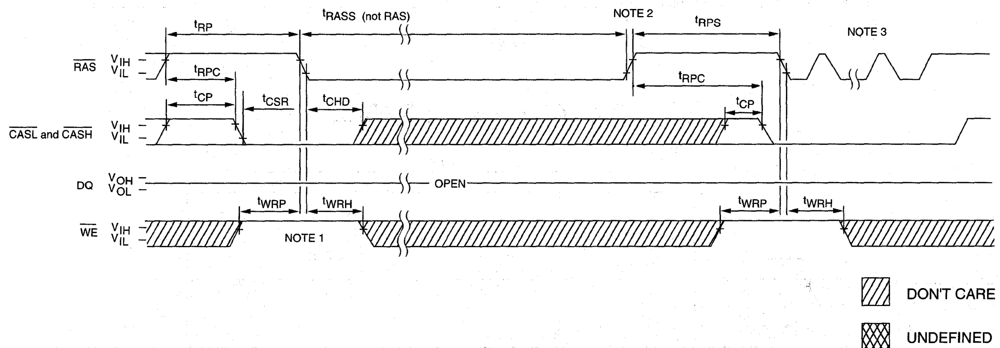
CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE:

1. ^{t}WRP and ^{t}WRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs that require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.
2. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
3. Once ^{t}RPS is satisfied, a compete burst of all rows should be executed.

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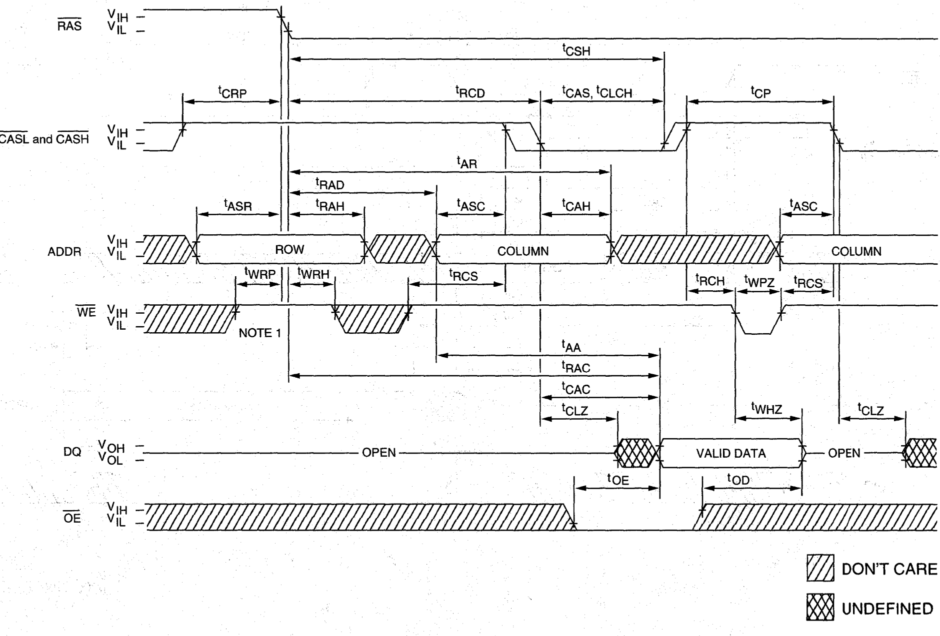
READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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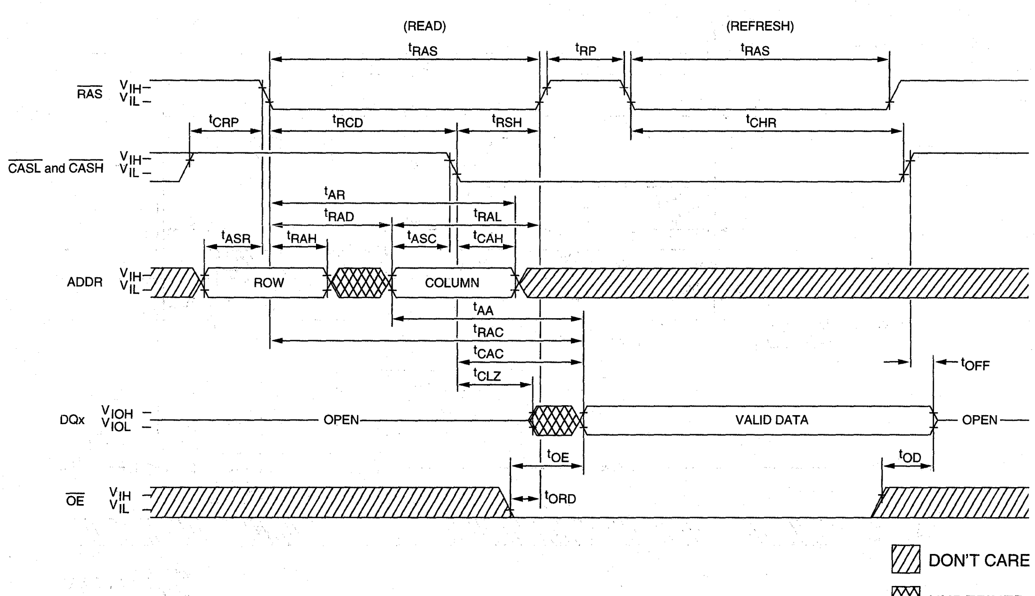
HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



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FPM DRAM PRODUCT SELECTION GUIDE

Memory Configuration	Optional Access Cycle	Part Number	Access Time (ns)	Typical Power Dissipation		Package/No. of Pins		Page
				Standby	Active	SOJ	TSOP	
3.3V FPM DRAMs								
1 Meg x 4	FPM	MT4LC4001J	60, 70, 80	1mW	100mW	20/26	20/26	2-29
1 Meg x 4	FPM, S	MT4LC4001J S	60, 70, 80	0.3mW	100mW	20/26	20/26	2-29
4 Meg x 4	FPM, 2KR	MT4LC4M4B1	60, 70	1mW	180mW	24/26	24/26	2-65
4 Meg x 4	FPM, 2KR, S	MT4LC4M4B1 S	60, 70	0.3mW	180mW	24/26	24/26	2-65
16 Meg x 4	FPM, 8KR	MT4LC16M4A7	50, 60, 70	1mW	165mW	34	34	2-79
16 Meg x 4	FPM, 4KR	MT4LC16M4T8	50, 60, 70	1mW	225mW	34	34	2-79
2 Meg x 8	FPM, 2KR	MT4LC2M8B1	60, 70	1mW	200mW	28	28	2-91
2 Meg x 8	FPM, 2KR, S	MT4LC2M8B1 S	60, 70	0.3mW	200mW	28	28	2-91
8 Meg x 8	FPM, 8KR	MT4LC8M8E1	50, 60, 70	1mW	170mW	34	34	2-105
8 Meg x 8	FPM, 4KR	MT4LC8M8B6	50, 60, 70	1mW	230mW	34	34	2-105
256K x 16	FPM, DC	MT4LC16257	60, 70, 80	3mW	150mW	40	40/44	2-131
256K x 16	FPM, DC, S	MT4LC16257 S	60, 70, 80	0.3mW	150mW	40	40/44	2-131
1 Meg x 16	FPM, DC, 1KR	MT4LC1M16C3	60, 70	3mW	250mW	–	44/50	2-163
1 Meg x 16	FPM, DC, 1KR, S	MT4LC1M16C3 S	60, 70	0.3mW	250mW	–	44/50	2-163
5V FPM DRAMs								
4 Meg x 1	FPM	MT4C1004J	60, 70	3mW	225mW	20/26	20/26	2-1
4 Meg x 1	FPM, S	MT4C1004J S	60, 70	0.8mW	225mW	20/26	20/26	2-1
1 Meg x 4	FPM	MT4C4001J	60, 70	3mW	225mW	20/26	20/26	2-15
1 Meg x 4	FPM, S	MT4C4001J S	60, 70	0.8mW	225mW	20/26	20/26	2-15
1 Meg x 4	FPM, QC	MT4C4004J	60, 70	3mW	225mW	24/26	–	2-41
4 Meg x 4	FPM, 2KR	MT4C4M4B1	60, 70	3mW	250mW	24/26	24/26	2-53
256K x 16	FPM, DC	MT4C16257	60, 70, 80	3mW	375mW	40	40/44	2-117
1 Meg x 16	FPM, DC, 1KR	MT4C1M16C3	60, 70	1mW	350mW	42	–	2-147

FPM = FAST PAGE MODE, DC = Dual CAS, QC = Quad CAS, 1KR = 1,024 Refresh, 2KR = 2,048 Refresh, 4KR = 4,096 Refresh, 8KR = 8,192 Refresh, S = SELF REFRESH

DRAM

4 MEG x 1 DRAM

5V, STANDARD OR SELF REFRESH

FPM DRAM

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C1004J) or 128ms (MT4C1004J S only)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes (MT4C1004J S only)
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C1004J S)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S

- Part Number Example: MT4C1004JDJ-6 S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1) / **20/26-Pin TSOP (DB-1)**

Signal	Pin	Pin	Signal
D	1	26	Vss
WE	2	25	Q
RAS	3	24	CAS
NC	4	23	NC
*A10	5	22	A9
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

*Address not used for RAS-ONLY REFRESH

GENERAL DESCRIPTION

The MT4C1004J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin remains open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms for the MT4C1004J and every 128ms for the MT4C1004J S, regardless of sequence. The CBR and extended refresh cycles will invoke the internal refresh counter for automatic RAS addressing.

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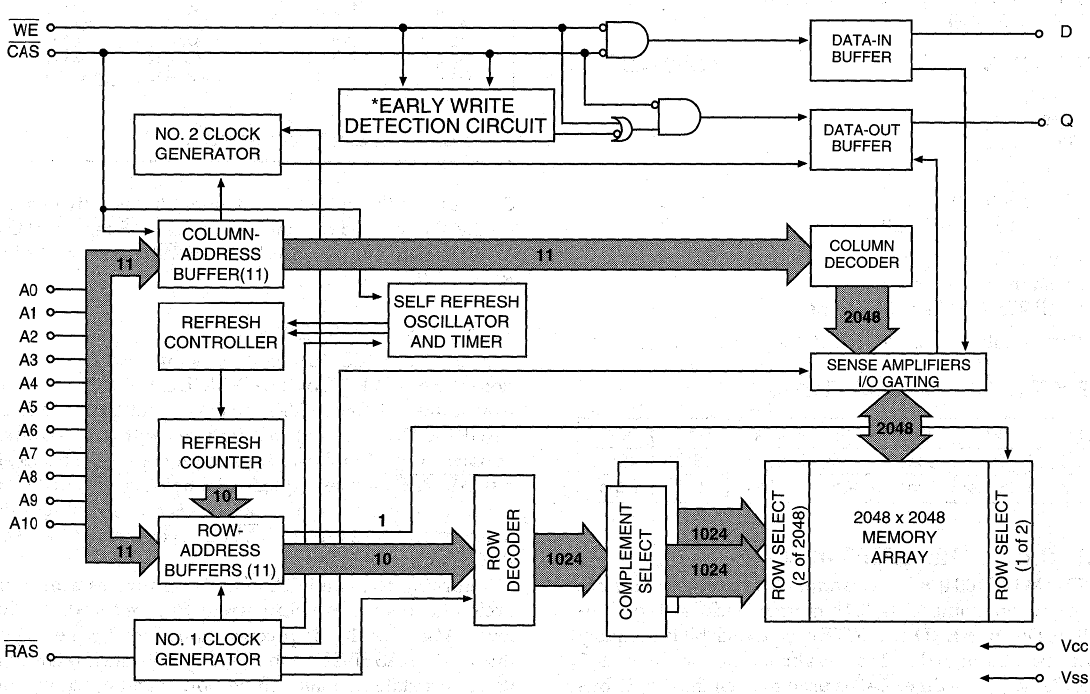
REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ${}^tRASS$. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ${}^tRPS$ ($\approx {}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$-ONLY REFRESH or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA	
					^tR	^tC	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	"don't care"	High-Z
SELF REFRESH (MT4C1004J S only)		H→L	L	H	X	X	"don't care"	High-Z

FPM DRAM

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
	I_{CC2} (S only)	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	110	100	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	80	70	mA	3, 4, 27
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	110	100	mA	3, 27
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: CAS = 0.2V or CBR cycling; RAS = ${}^tRAS$ (MIN); WE = V_{CC} -0.2V; A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5, 7, 25
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with ${}^tRAS \geq {}^tRASS$ (MIN) and CAS held LOW; WE = V_{CC} -0.2; A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 28

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, D	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	30		35		ns	21
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20	ns	15
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	10		10		ns	28
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	5
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	0		0		ns	
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	15		20		ns	21
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	22
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	22
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 26
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	60		70		ns	
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	14
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	25
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	25
$\overline{\text{RAS}}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	28
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		ns	19
Read command setup time	^{t}RCS	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (1,024 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		ns	28
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	130		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	60		70		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit through-out the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in late WRITE or READ WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.

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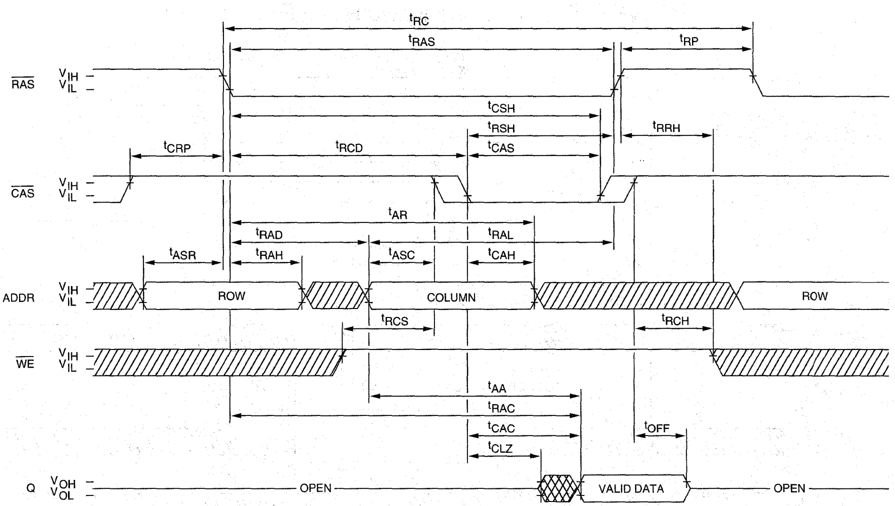
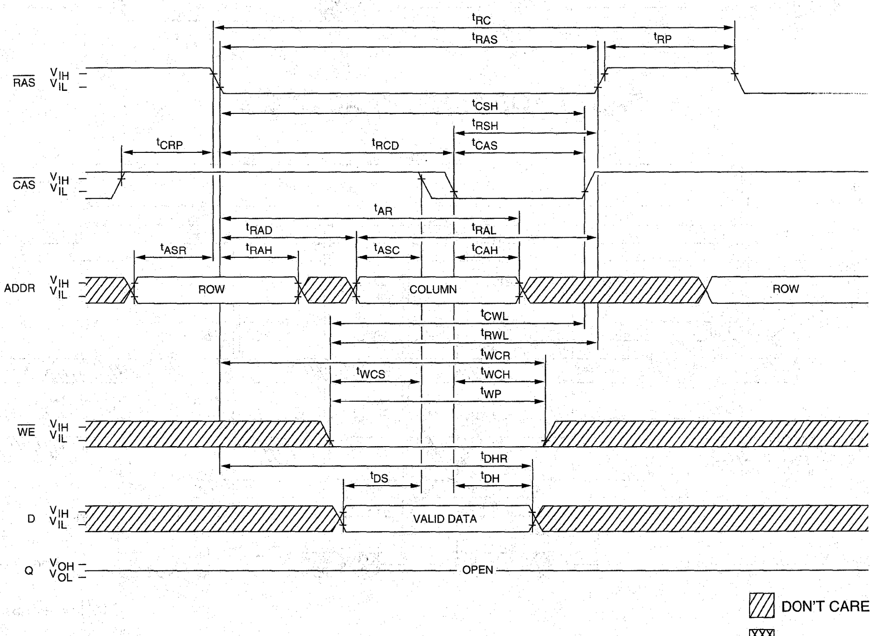
FPM DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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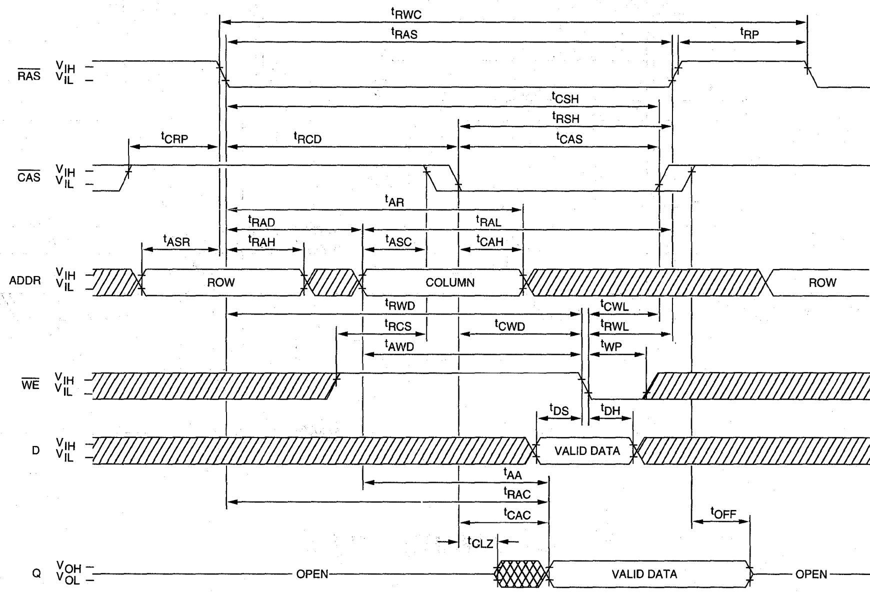
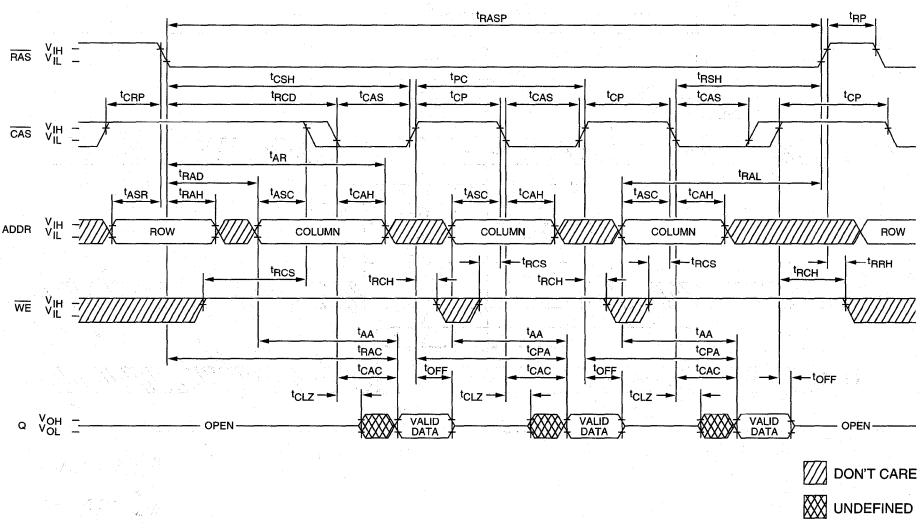
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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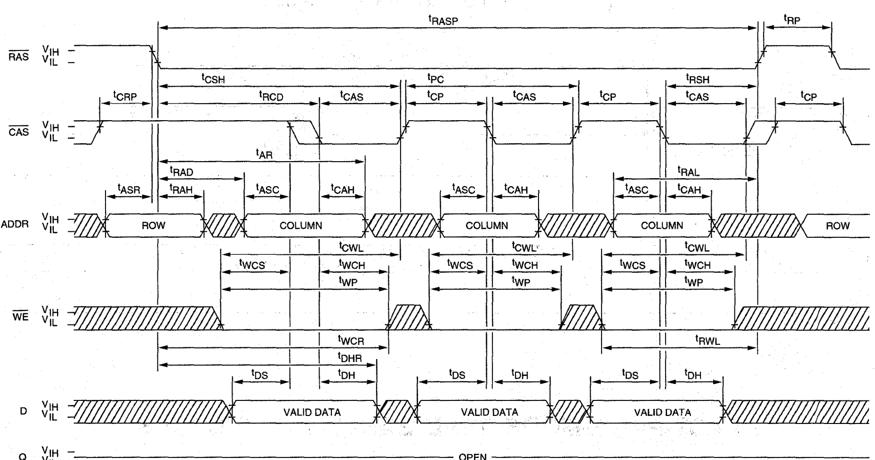
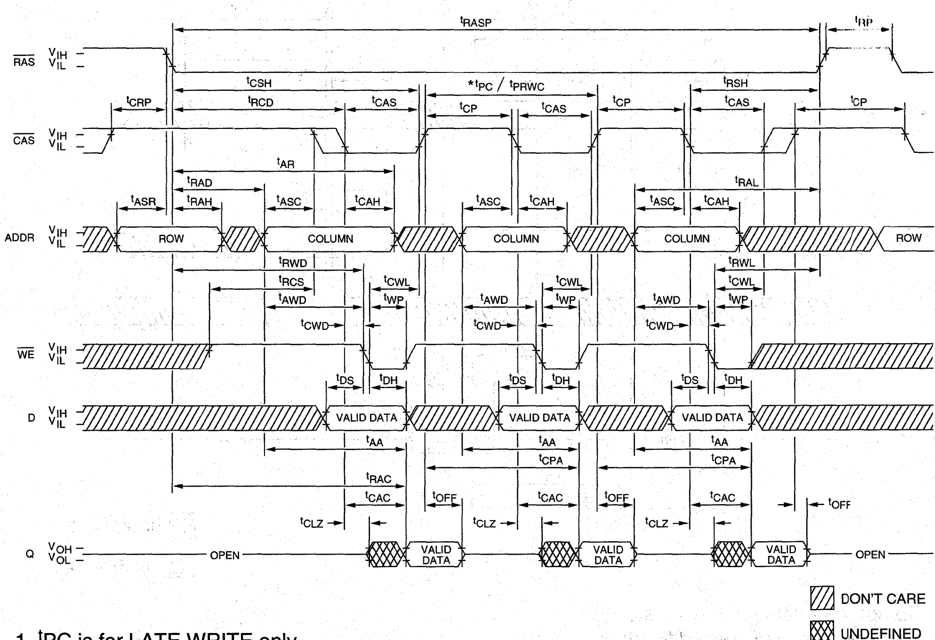
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. ᵗPC is for LATE WRITE only.

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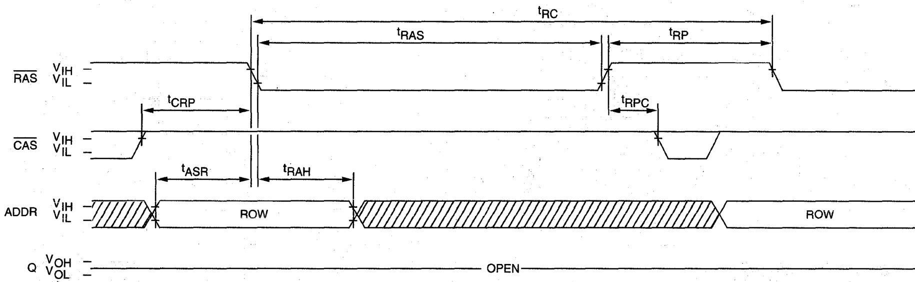
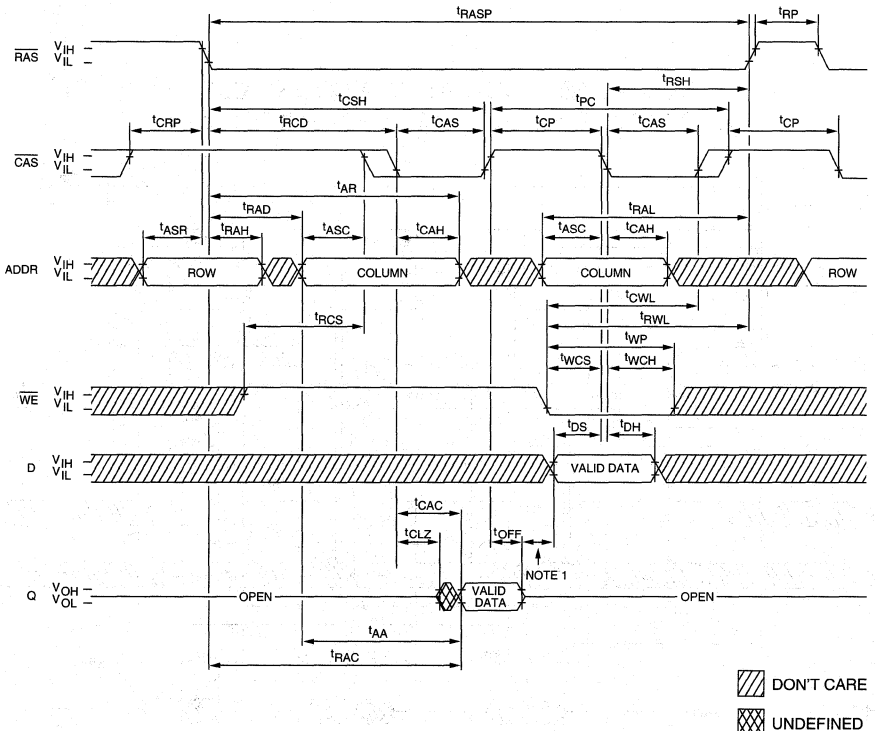
RAS-ONLY REFRESH CYCLE
(WE and A10 = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



NOTE:
1. Do not drive data prior to tristate.
2. Assumes D and Q are tied together.

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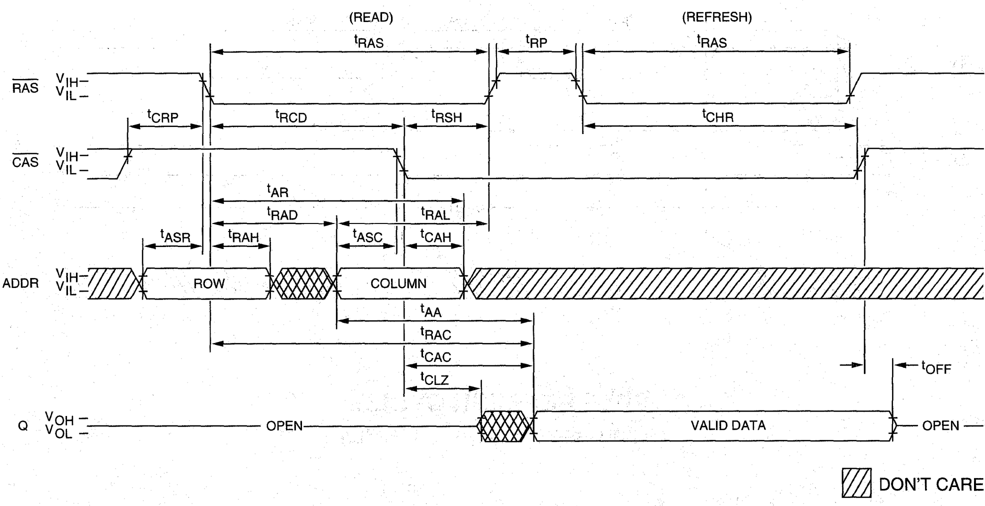
HIDDEN REFRESH CYCLE [23]

($\overline{WE}$ = HIGH)



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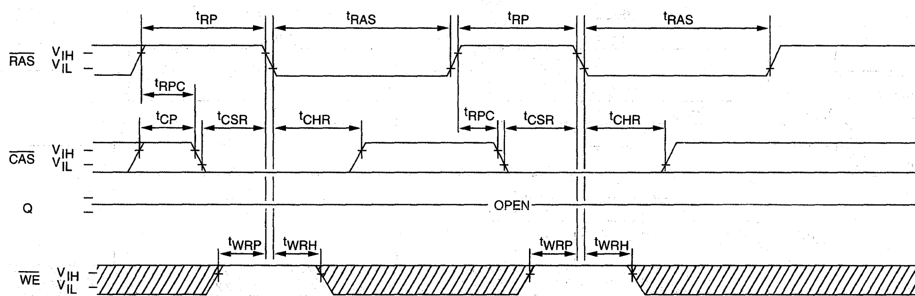
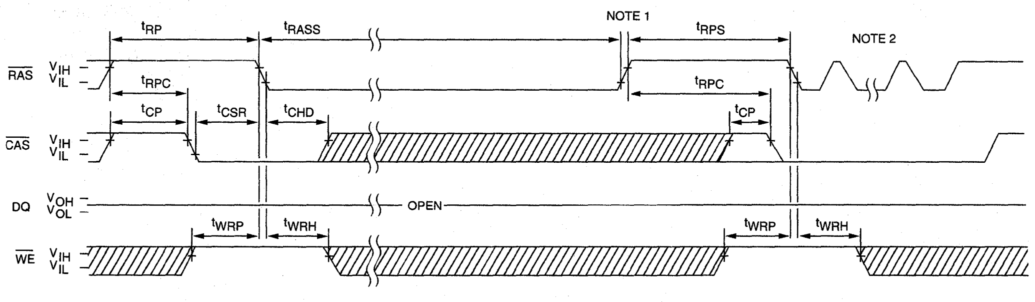
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



SELF REFRESH CYCLE
(Addresses = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE:
1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

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DRAM

1 MEG x 4 DRAM

5V, STANDARD OR SELF REFRESH

FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C4001J) or 128ms (MT4C4001J S)
- Industry-standard pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes (MT4C4001J S only)
- FAST PAGE MODE access cycle
- Low power, 0.8mW standby; 225mW active, typical (MT4C4001J S)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S

- Part Number Example: MT4C4001JDJ-6 S

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{\text{WE}}$	3	24	DQ3
$\overline{\text{RAS}}$	4	23	$\overline{\text{CAS}}$
A9	5	22	$\overline{\text{OE}}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

20/26-Pin TSOP (DB-1)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
$\overline{\text{WE}}$	3	24	DQ3
$\overline{\text{RAS}}$	4	23	$\overline{\text{CAS}}$
A9	5	22	$\overline{\text{OE}}$
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

GENERAL DESCRIPTION

The MT4C4001J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. $\overline{\text{RAS}}$ is used to latch the first 10 bits and $\overline{\text{CAS}}$ the latter 10 bits. READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pins remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle.

If $\overline{\text{WE}}$ goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{\text{WE}}$ and $\overline{\text{OE}}$.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

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FPM DRAM

REFRESH

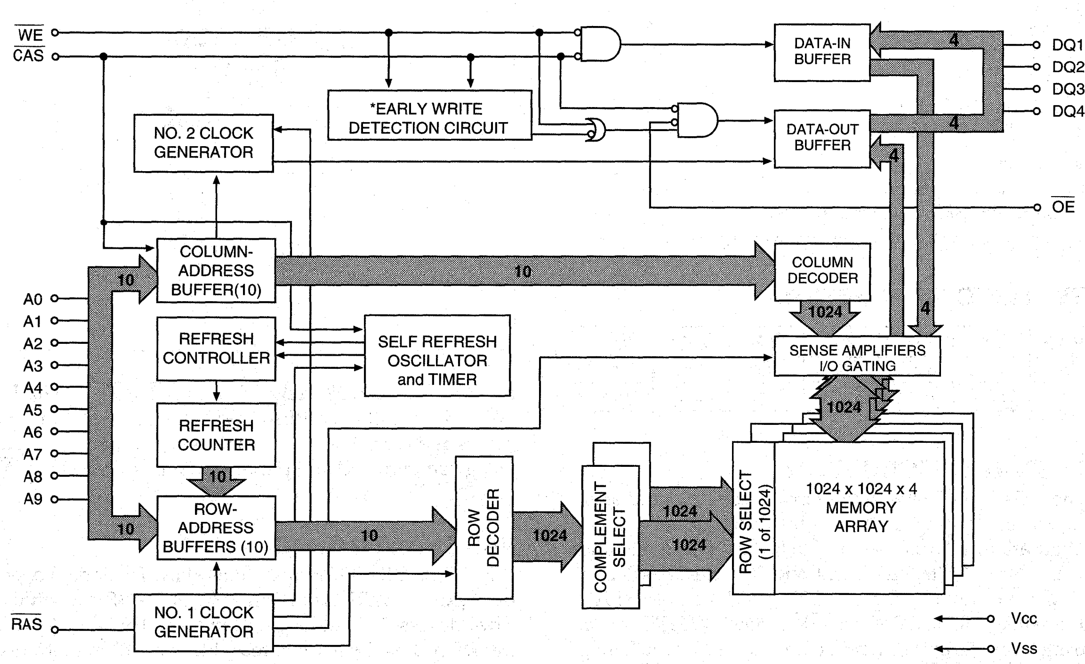
Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4C4001J(S). The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, eight times longer than the standard 16ms specifications.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^tRPS ($\approx {^tRC}$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH (MT4C4001J S only)		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
	I_{CC2} (S only)	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; $\overline{OE}$, A0-A9 and D_{IN} = Vcc -0.2V or 0.2V; (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2; A0-A9, $\overline{OE}$ and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 31

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

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FPM DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address hold time (referenced to RAS)	tAR	45		50		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to WE delay time	tAWD	55		65		ns	21
Access time from CAS	tCAC		15		20	ns	15
Column-address hold time	tCAH	10		15		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	10		10		ns	31
CAS hold time (CBR REFRESH)	tCHR	10		10		ns	5
CAS to output in Low-Z	tCLZ	0		0		ns	
CAS precharge time	tCP	10		10		ns	16
Access time from CAS precharge	tCPA		35		40	ns	
CAS to RAS precharge time	tCRP	10		10		ns	
CAS hold time	tCSH	60		70		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		ns	5
CAS to WE delay time	tCWD	40		50		ns	21
Write command to CAS lead time	tCWL	15		20		ns	
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	22
Output disable	tOD		15		20	ns	27
Output Enable	tOE		15		20	ns	23
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		ns	26
Output buffer turn-off delay	tOFF	3	15	3	20	ns	20, 29
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		100		ns	
Access time from RAS	tRAC		60		70	ns	14

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS to column-address delay time	tRAD	15	30	15	35	ns	18
Row-address hold time	tRAH	10		10		ns	
Column-address to RAS lead time	tRAL	30		35		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH cycle	tRASS	100		100		µs	31
Random READ or WRITE cycle time	tRC	110		130		ns	
RAS to CAS delay time	tRCD	20	45	20	50	ns	17
Read command hold time (referenced to CAS)	tRCH	0		0		ns	19
Read command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (1,024 cycles) S version	tREF		128		128	ms	
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
RAS precharge time during SELF REFRESH cycle	tRPS	110		130		ns	31
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	15		20		ns	
READ WRITE cycle time	tRWC	150		180		ns	
RAS to WE delay time	tRWD	90		100		ns	21
Write command to RAS lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS)	tWCR	45		55		ns	
WE command setup time	tWCS	0		0		ns	21, 27
Write command pulse width	tWP	10		15		ns	
WE hold time (CBR REFRESH)	tWRH	10		10		ns	25
WE setup time (CBR REFRESH)	tWRP	10		10		ns	25

FPM DRAM

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$=HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{\text{OE}}$ is taken back LOW while $\overline{\text{CAS}}$ remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{\text{CAS}}$ goes HIGH before $\overline{\text{OE}}$, the DQs will open regardless of the state of $\overline{\text{OE}}$. If $\overline{\text{CAS}}$ stays LOW while $\overline{\text{OE}}$ is brought HIGH, the DQs will open. If $\overline{\text{OE}}$ is brought back LOW ($\overline{\text{CAS}}$ still LOW), the DQs will provide the previously read data.
28. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
29. The 3ns minimum is a parameter guaranteed by design.
30. Column-address changed once each cycle.
31. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.

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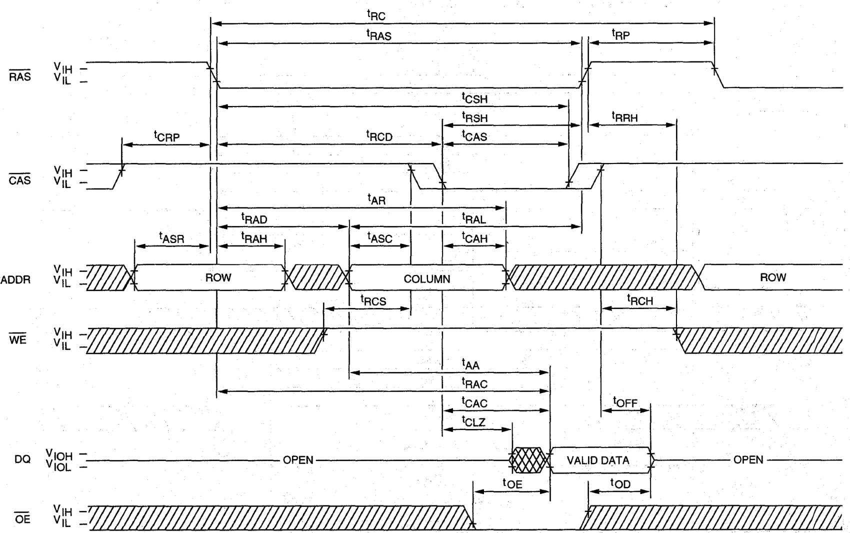
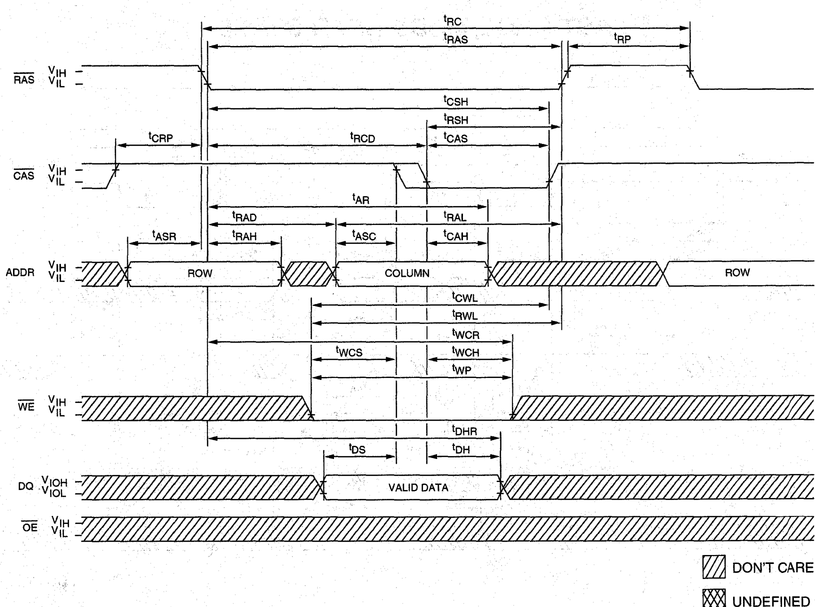
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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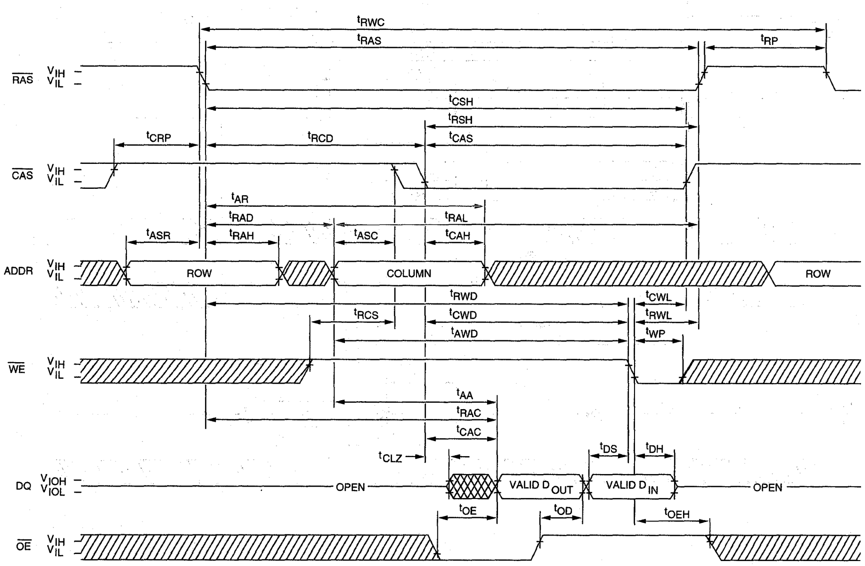
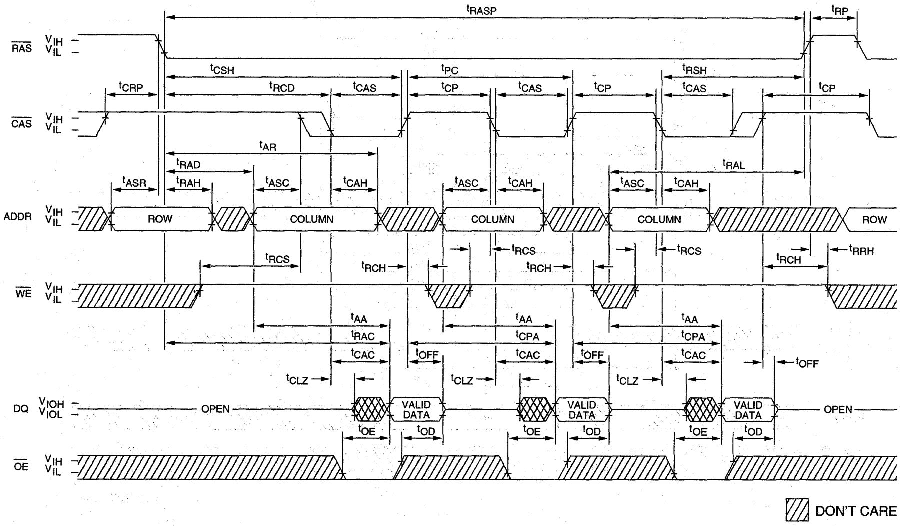
FPM DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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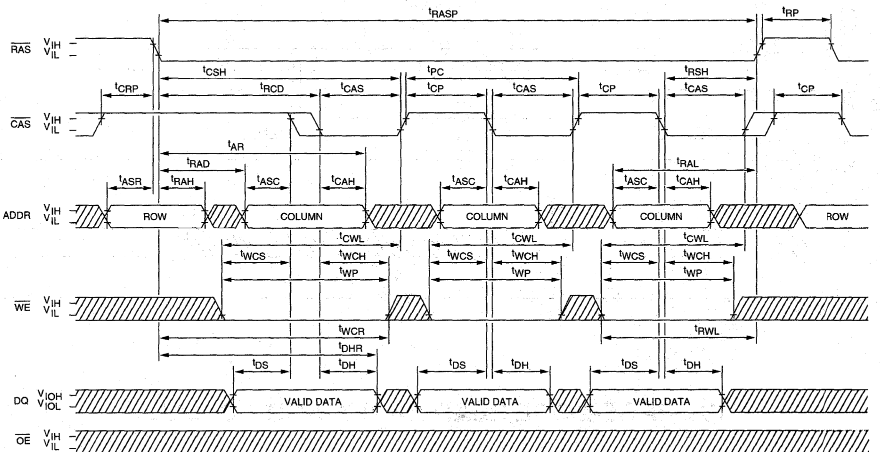
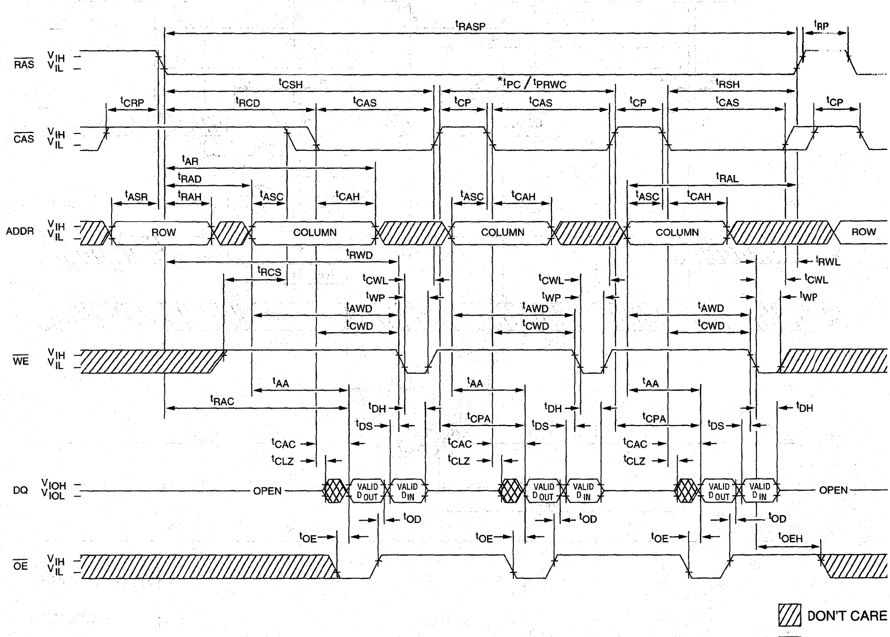
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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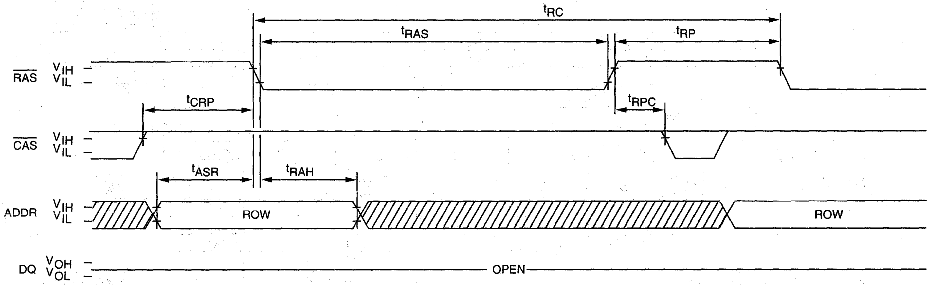
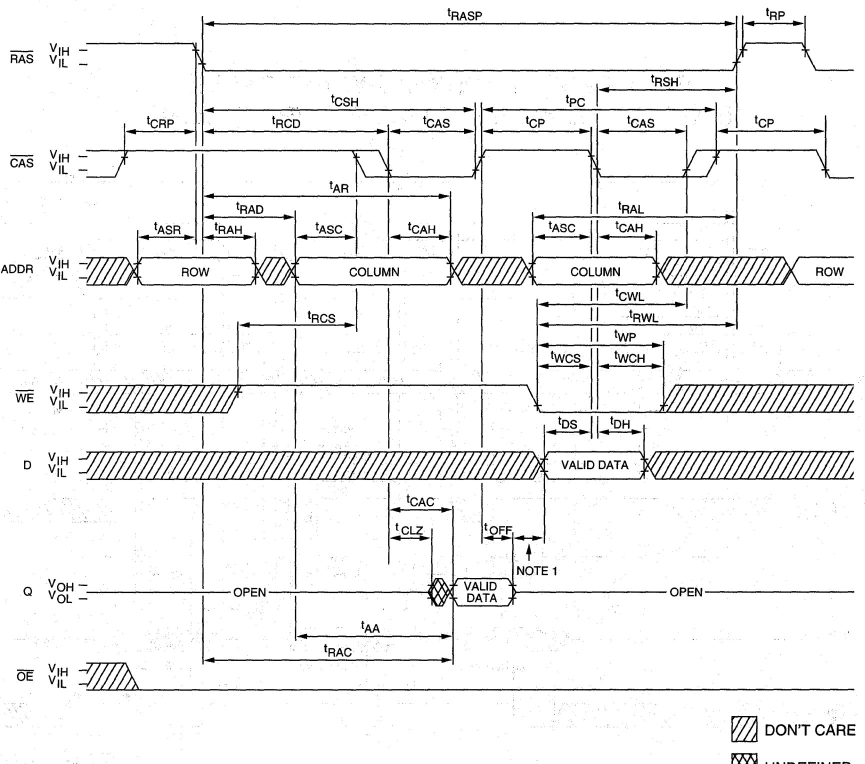
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE



NOTE: 1. Do not drive data prior to tristate.

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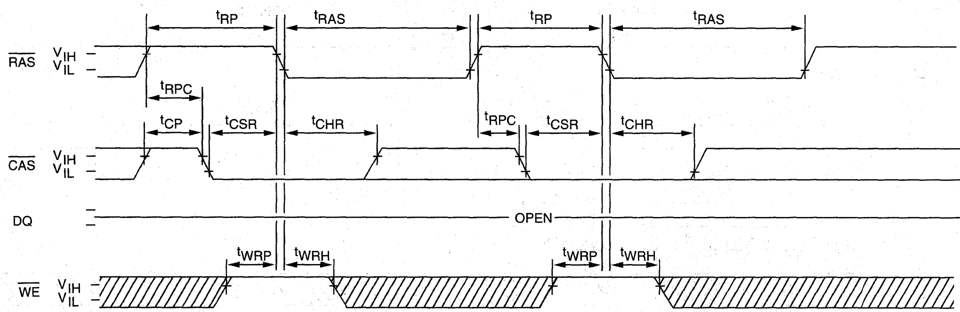
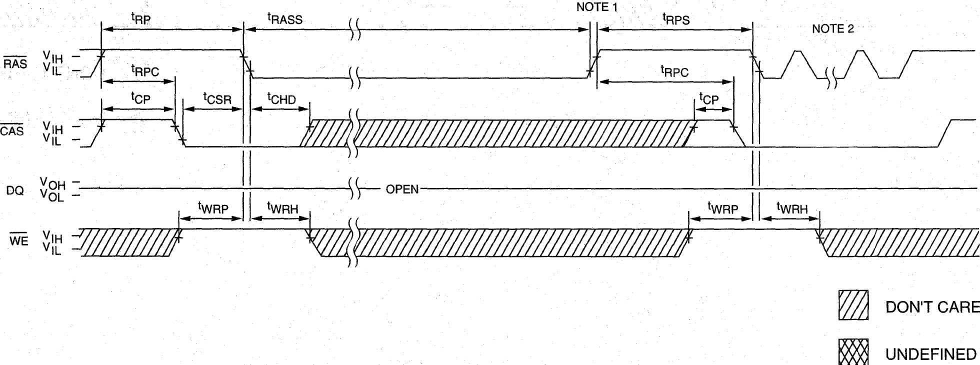
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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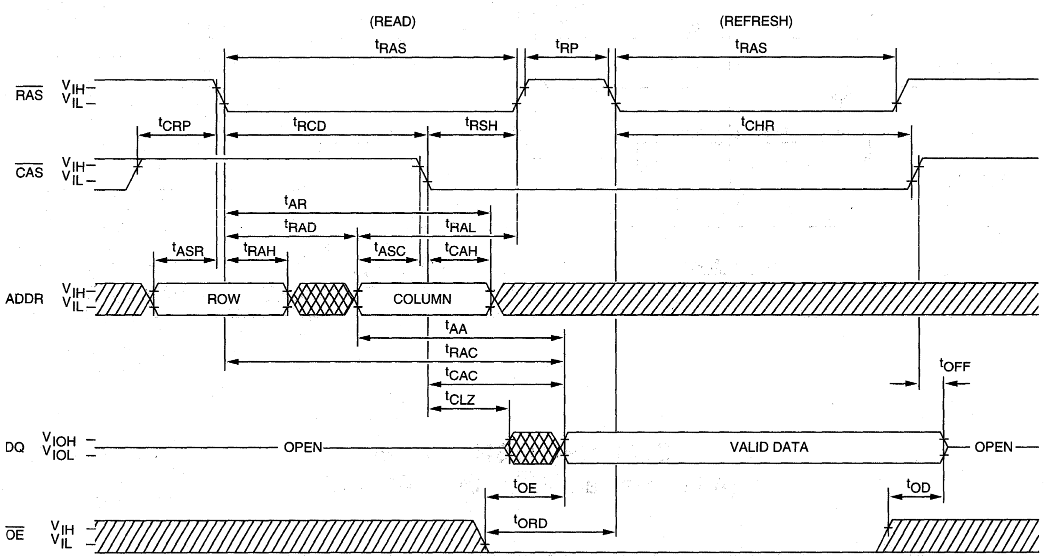
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

1 MEG x 4 DRAM

3.3V, FAST PAGE MODE OPTIONAL SELF REFRESH

FPM DRAM

FEATURES

- Single +3.3V ±0.3V power supply
- Low power, 0.3mW standby; 100mW active, typical
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- FAST PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- Low SELF REFRESH current, 100µA typical, 150µA (MAX)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG

- Part Number Example: MT4LC4001JDJ-7 S

KEY TIMING PARAMETERS

SPEED	ᵗRC	ᵗRAC	ᵗPC	ᵗAA	ᵗCAC	ᵗRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	20ns	60ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ (DA-1) / **20/26-Pin TSOP (DB-1)**

Pin	Name	Pin	Name
1	DQ1	26	Vss
2	DQ2	25	DQ4
3	WE	24	DQ3
4	RAS	23	CAS
5	A9	22	OE
9	A0	18	A8
10	A1	17	A7
11	A2	16	A6
12	A3	15	A5
13	Vcc	14	A4

GENERAL DESCRIPTION

The MT4LC4001J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle.

If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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REFRESH

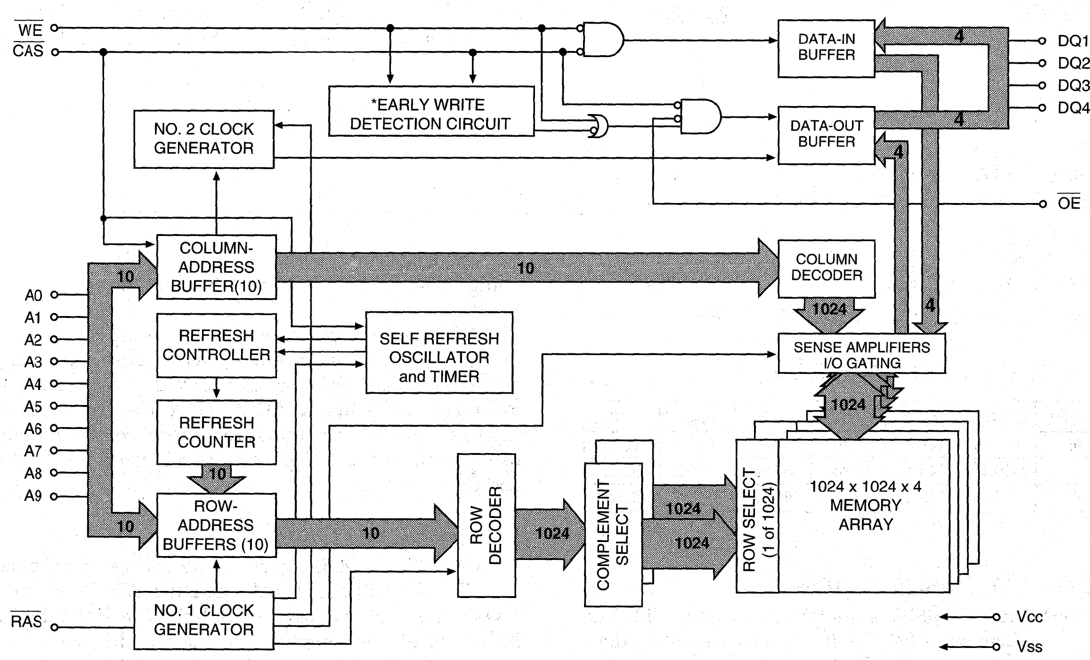
Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4C4001 J(S). The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, eight times longer than the standard 16ms specifications.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^tRPS ($\approx {}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1.0V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC}+0.5V (All other pins not under test = 0V)		I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ V_{CC}+0.5V)		I_{OZ}	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
	Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	**SYM**	**-6**	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	1	1	1	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	500	µA	
	I_{CC2} (S only)	100	100	100	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	80	70	60	mA	3, 4, 30
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	60	50	40	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	80	70	60	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	80	70	60	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; ^tRAS = ^tRAS (MIN); $\overline{WE}$ = V_{CC} - 0.2V; A0-A9,$\overline{OE}$, and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	150	150	150	µA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with ^tRAS ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9,$\overline{OE}$, and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	150	150	150	µA	5, 29

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35		40	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		55		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		65		70		ns	21
Access time from $\overline{CAS}$	^{t}CAC		15		20		20	ns	15
Column-address hold time	^{t}CAH	10		15		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	10		10		10		ns	29
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		80		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		10		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		50		50		ns	21
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Output disable	^{t}OD		15		20		20	ns	27
Output Enable time	^{t}OE		15		20		20	ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	26
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	20
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		100		105		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70		80	ns	14

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Row-address hold time	^{t}RAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		100		µs	29
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
Refresh period (1,024 cycles) S version	^{t}REF		128		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		150		ns	29
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	15		20		20		ns	
READ WRITE cycle time	^{t}RWC	150		180		200		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		100		110		ns	21
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21, 27
Write command pulse width	^{t}WP	10		15		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	25

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE is taken back LOW while CAS remains LOW, the DQs will remain open.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If CAS goes HIGH before OE, the DQs will open regardless of the state of OE. If CAS stays LOW while OE is brought HIGH, the DQs will open. If OE is brought back LOW (CAS still LOW), the DQs will provide the previously read data.
28. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
29. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
30. Column-address changed once each cycle.

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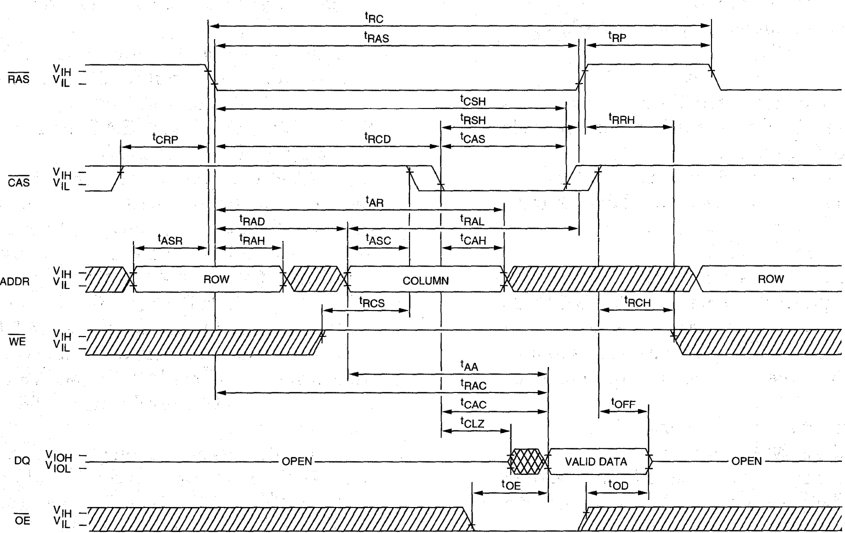
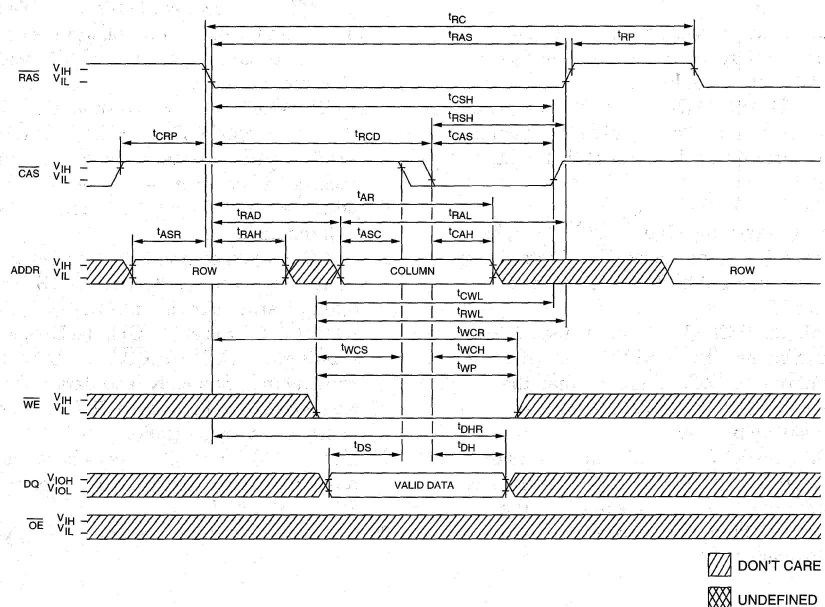
FPM DRAM

READ CYCLE



EARLY WRITE CYCLE



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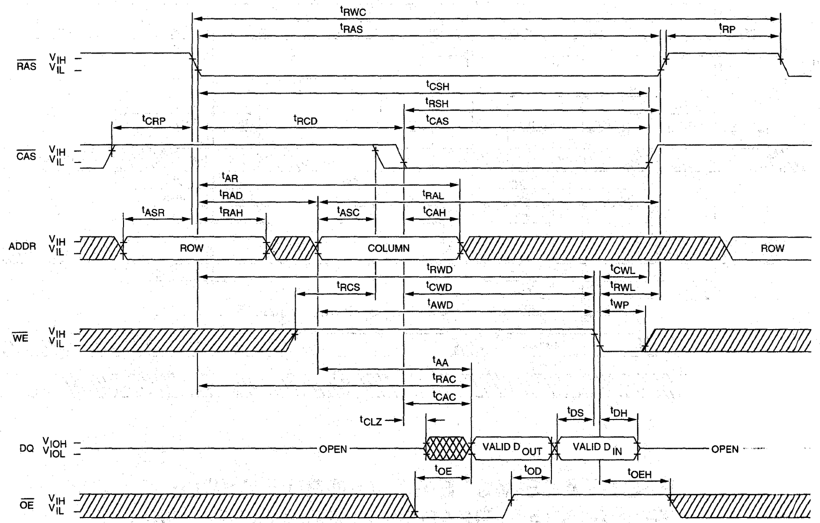
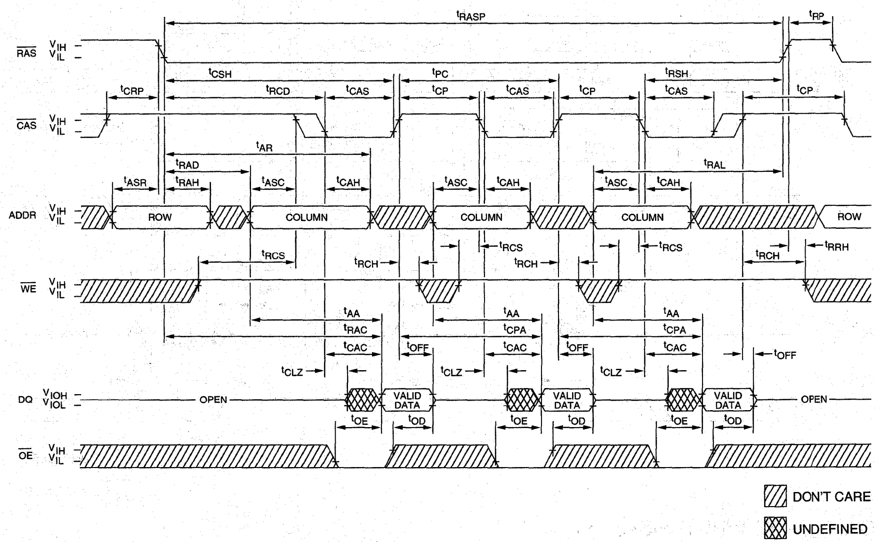
FPM DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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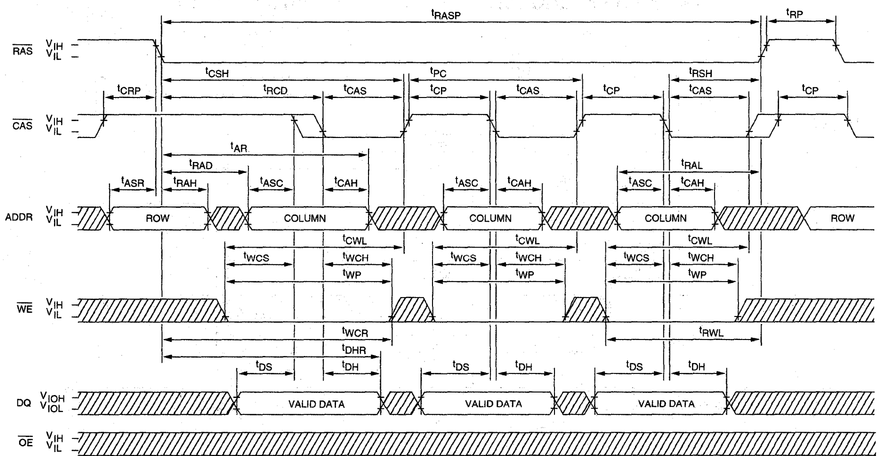
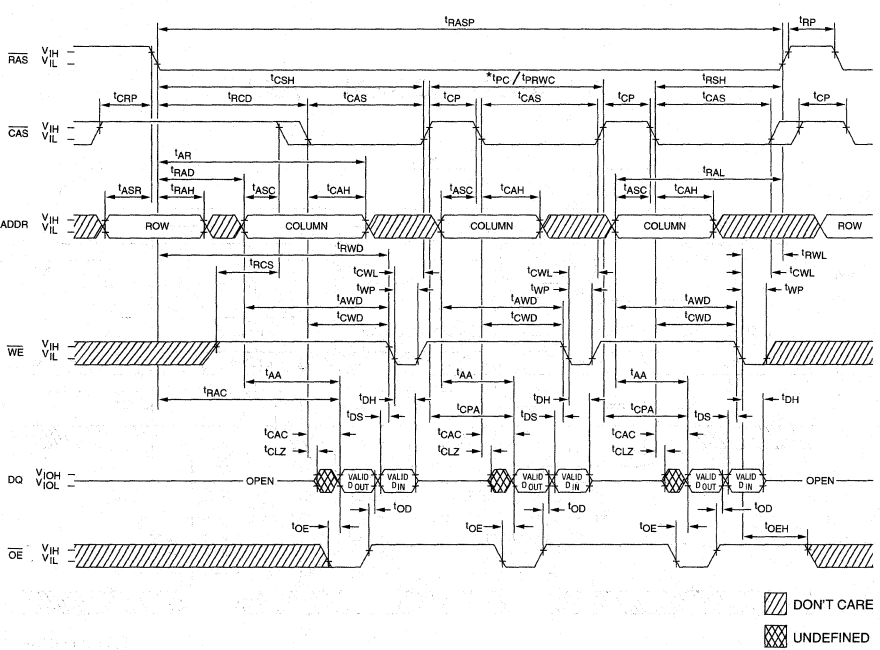
FPM DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. ᵗPC is for LATE WRITE cycles only.

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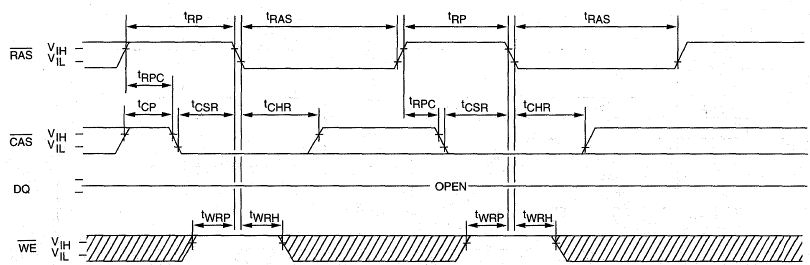
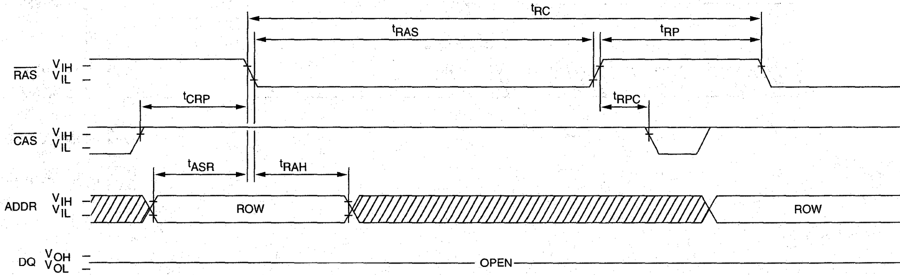
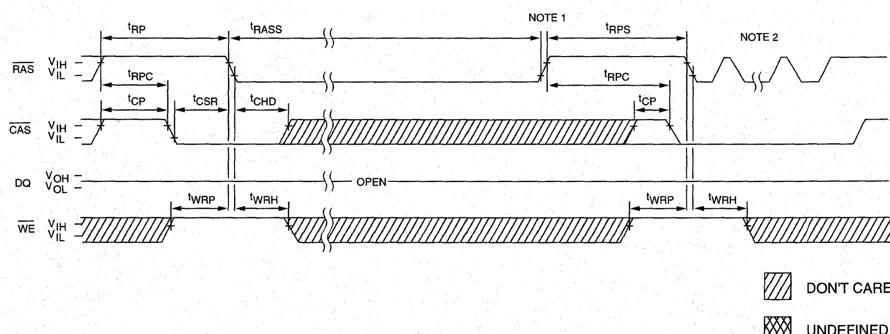
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{WE}$ = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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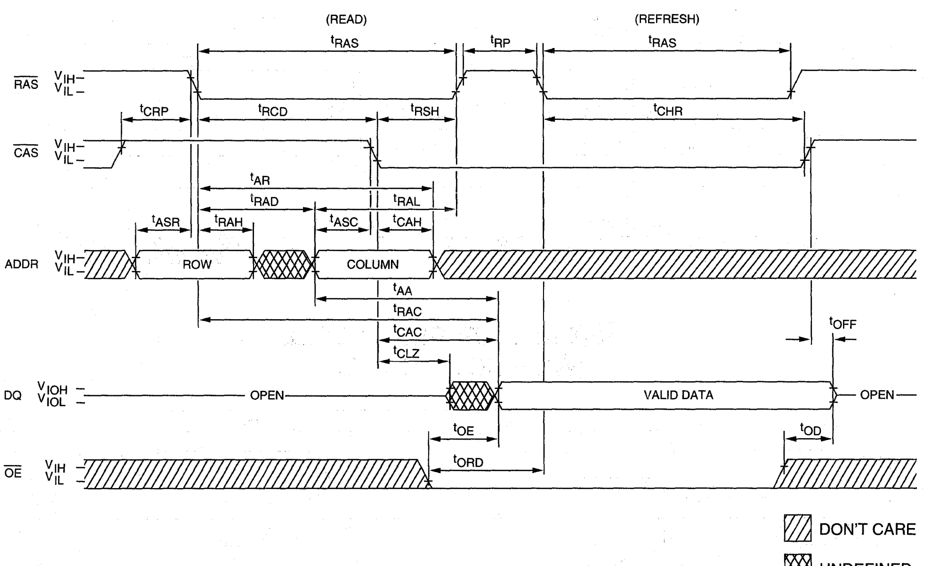
HIDDEN REFRESH CYCLE [24]
(WE = HIGH; OE = LOW)



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DRAM

1 MEG x 4 DRAM

5V, QUAD CAS PARITY, FAST PAGE MODE

FEATURES

- Four independent CAS controls, allowing individual manipulation to each of the four data input/output ports (DQ1 through DQ4).
- Offers a single chip solution to byte-level parity for 36-bit words when using 1 Meg x 4 DRAMs for memory
- Emulates WRITE-PER-BIT at design-in level, with simplified timing constraints
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 1,024-cycle refresh in 16ms
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic SOJ (300 mil) — DJ
- Part Number Example: MT4C4004JDJ-7

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ
(DA-2)

Signal	Pin	Pin	Signal
DQ1	1	26	Vss
DQ2	2	25	DQ4
WE	3	24	DQ3
RAS	4	23	CAS4
CAS1	5	22	OE
CAS2	6	21	CAS3
A9	8	19	NC
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
Vcc	13	14	A4

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

GENERAL DESCRIPTION

The MT4C4004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. This 1 Meg x 4 DRAM is unique in that each CAS (CAS1 through CAS4) controls its corresponding data I/O port in conjunction with OE (that is, CAS1 controls DQ1 I/O port, CAS2 controls DQ2, CAS3 controls DQ3 and CAS4 controls DQ4).

The best way to view the Quad CAS function is to imagine the CAS inputs going into an OR gate to obtain an internally generated CAS signal functioning in an identical manner to the single CAS input on a standard 1 Meg x 4 DRAM device. The key difference is that each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE) on the Quad CAS DRAM.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits, and the first CAS is used to latch the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode.

During a WRITE cycle, data-in (Dx) is latched by the falling edge of WE or the first CAS, whichever occurs last. If WE goes LOW prior to the first CAS going LOW, the output pin(s) remain open until the next CAS cycle. If WE goes LOW after data reaches the output buffer, data-out (Q) is activated and retains the selected cell data until the trailing edge of its corresponding CAS occurs (regardless of WE or RAS). This late WE pulse results in a READ-WRITE cycle (OE switching the device from a READ to a WRITE function). The four data inputs and four data outputs are routed through four pins using common I/O, with pin direction controlled by WE and OE.

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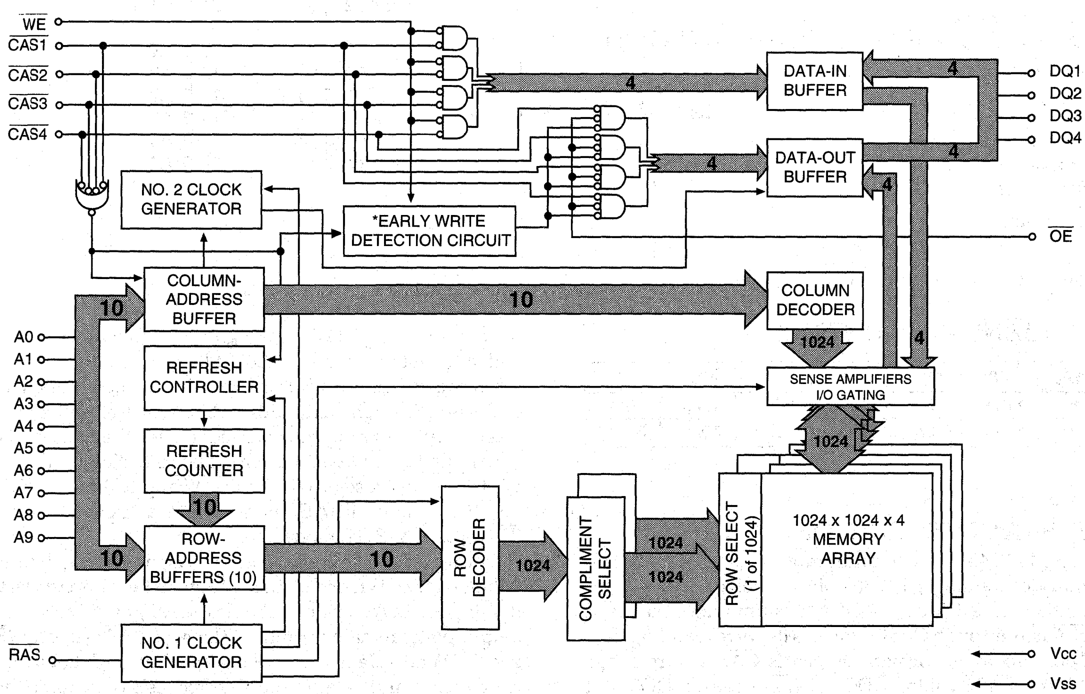
GENERAL DESCRIPTION (continued)

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by the first CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and all four CAS controls HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

FUNCTIONAL BLOCK DIAGRAM
QUAD CAS



***NOTE:** 1. WE LOW prior to first CAS LOW, EW detection circuit output is a 1.
2. First CAS LOW while WE HIGH, EW detection circuit output is a 0; (OE will now determine I/O).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CASx}$	$\overline{CASy}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DQx (DQy always High-Z)
Standby		H	H→X	H→X	X	X	X	X	High-Z
READ		L	L	H	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	H	L	X	ROW	COL	Data-In
READ-WRITE		L	L	H	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	H	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	H	X	X	X	High-Z

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NEW FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX			
PARAMETER/CONDITION	SYMBOL	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2.5	2.5	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	26	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ${}^tRC$= ${}^tRC$ [MIN])	I_{CC3}	110	100	mA	3, 4, 39
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ${}^tPC$= ${}^tPC$ [MIN])	I_{CC4}	80	70	mA	3, 4, 39
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC$= ${}^tRC$ [MIN])	I_{CC5}	110	100	mA	3, 39
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$= ${}^tRC$ [MIN])	I_{CC6}	110	100	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		5	pF	2
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$1-4, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23, 25) (V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	27
Row-address setup time	^{t}ASR	0		0		ns	
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	55		65		ns	21
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20	ns	15, 29
Column-address hold time	^{t}CAH	10		15		ns	27
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	35
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	5, 25, 28
Last $\overline{\text{CAS}}$ going LOW to first $\overline{\text{CAS}}$ to return HIGH	^{t}CLCH	10		10		ns	30
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	0		0		ns	29
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		ns	16, 32
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40	ns	29
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		ns	28
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		ns	28
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5, 25, 27
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	40		50		ns	21, 27
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		ns	28
Data-in hold time	^{t}DH	10		15		ns	22, 29
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	22, 29
Output disable	^{t}OD		15		20	ns	38
Output Enable	^{t}OE		15		20	ns	23
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		ns	37
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 29, 38
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	31

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23, 25) (Vcc = 5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		100		ns	31
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	14
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	ns	17, 27
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		ns	19, 28
Read command setup time	^{t}RCS	0		0		ns	27
Refresh period (1,024 cycles)	^{t}REF		16		16	ms	
$\overline{\text{RAS}}$ precharge time	^{t}RP	40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		ns	
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		ns	19
$\overline{\text{RAS}}$ hold time	^{t}RSH	15		20		ns	36
READ-WRITE cycle time	^{t}RWC	150		180		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	90		100		ns	21
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		ns	36
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		ns	
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		ns	21, 27
Write command pulse width	^{t}WP	10		15		ns	
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial 100µs pause is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CASx}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CASx}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If at least one $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, all four $\overline{\text{CAS}}$ controls must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. The 3ns minimum is a parameter guaranteed by design.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{\text{CASx}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, READ-WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$=HIGH.
25. One to three $\overline{\text{CAS}}$ controls may be HIGH throughout any given $\overline{\text{CAS}}$ cycle, even though the timing waveforms show all $\overline{\text{CAS}}$ controls going LOW. If one goes LOW, it must meet all the timing requirements listed or the data for that I/O buffer may be invalid. At least one of the four $\overline{\text{CAS}}$ controls must be LOW for a valid $\overline{\text{CAS}}$ cycle to occur.
26. All other inputs at V_{CC} -0.2V.
27. The first $\overline{\text{CASx}}$ edge to transition LOW.
28. The last $\overline{\text{CASx}}$ edge to transition HIGH.
29. Output parameters (DQx) are referenced to corresponding $\overline{\text{CASx}}$ input; DQ1 by $\overline{\text{CAS1}}$, DQ2 by $\overline{\text{CAS2}}$, etc.
30. Last falling $\overline{\text{CASx}}$ edge to first rising $\overline{\text{CASx}}$ edge.
31. Last rising $\overline{\text{CASx}}$ edge to next cycle's last rising $\overline{\text{CASx}}$ edge.
32. Last rising $\overline{\text{CASx}}$ edge to first falling $\overline{\text{CASx}}$ edge.
33. First DQx controlled by the first $\overline{\text{CASx}}$ to go LOW.
34. Last DQx controlled by the last $\overline{\text{CASx}}$ to go HIGH.

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NOTES (continued)

35. Each $\overline{CAS}$x must meet minimum pulse width.
36. Last $\overline{CAS}$x to go LOW.
37. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
38. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$x goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$x stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. IF $\overline{OE}$ is brought back LOW ($\overline{CAS}$x still LOW), the DQs will provide the previously read data.
39. Column-address changed once each cycle.

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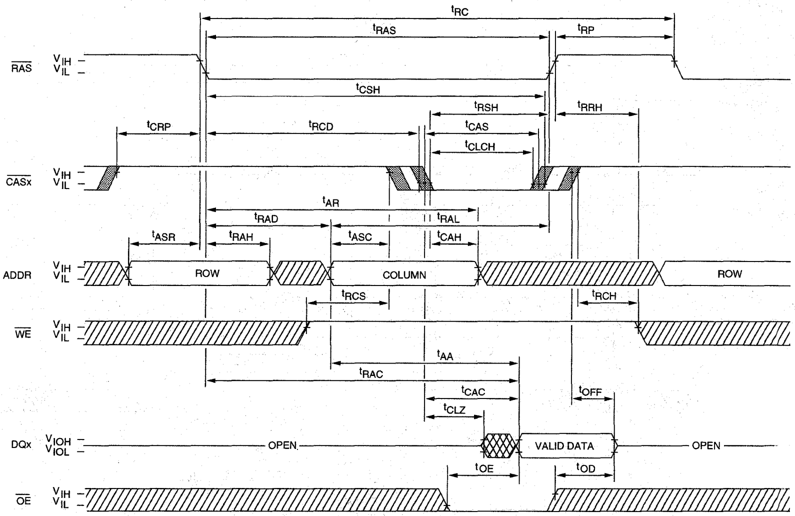
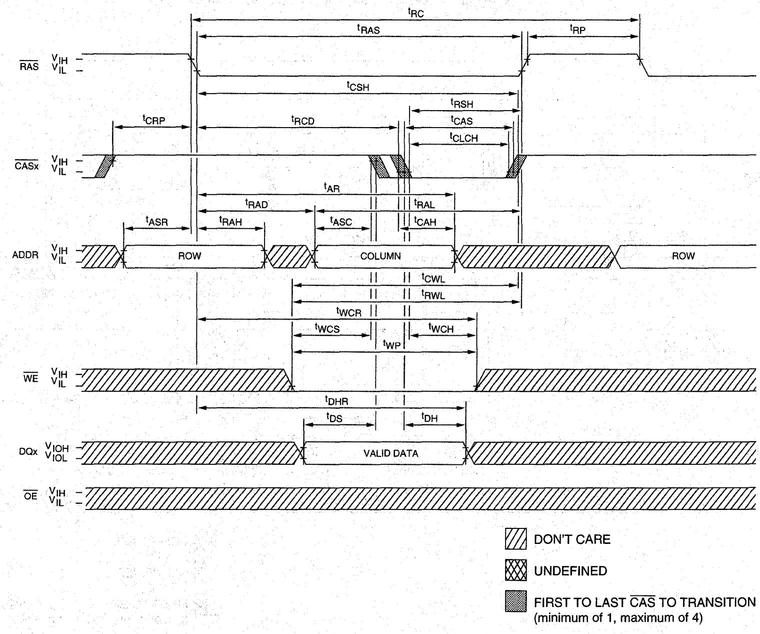
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION
(minimum of 1, maximum of 4)

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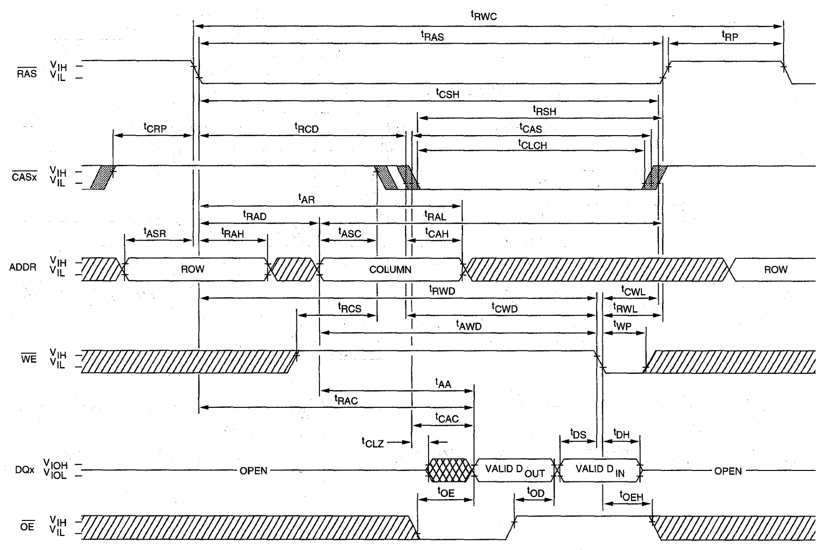
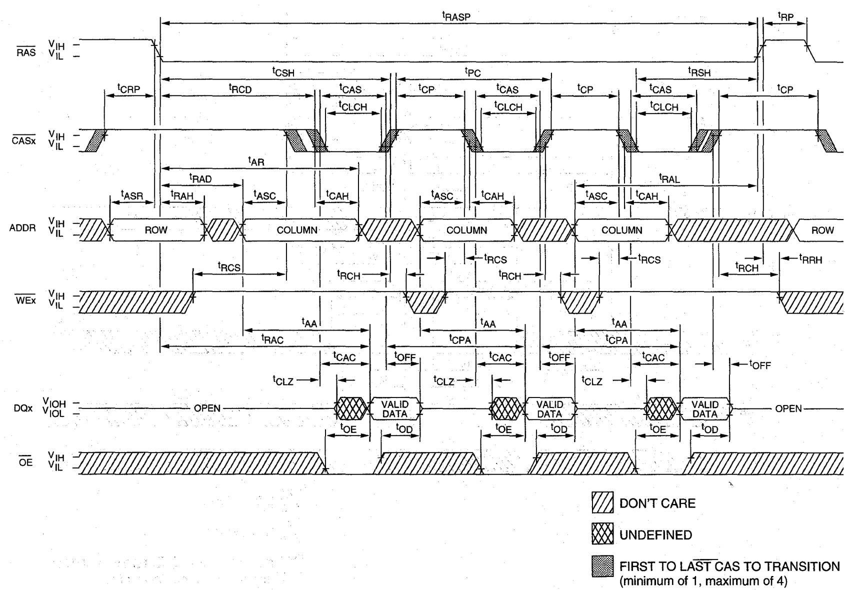
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

FIRST TO LAST CAS TO TRANSITION
(minimum of 1, maximum of 4)

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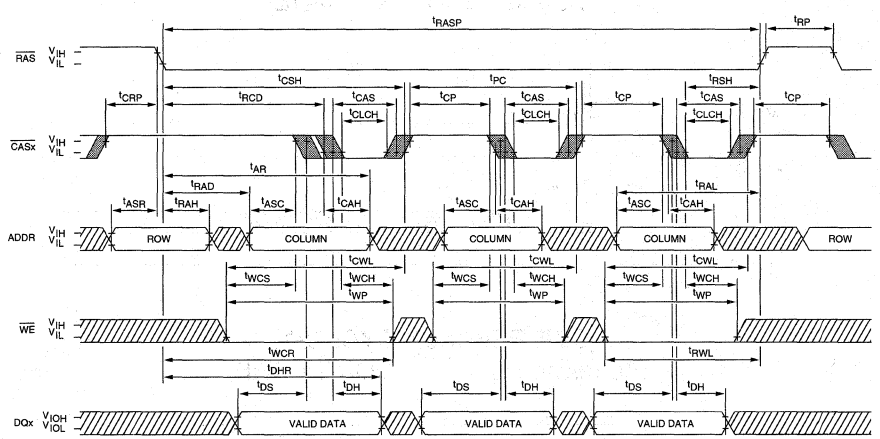
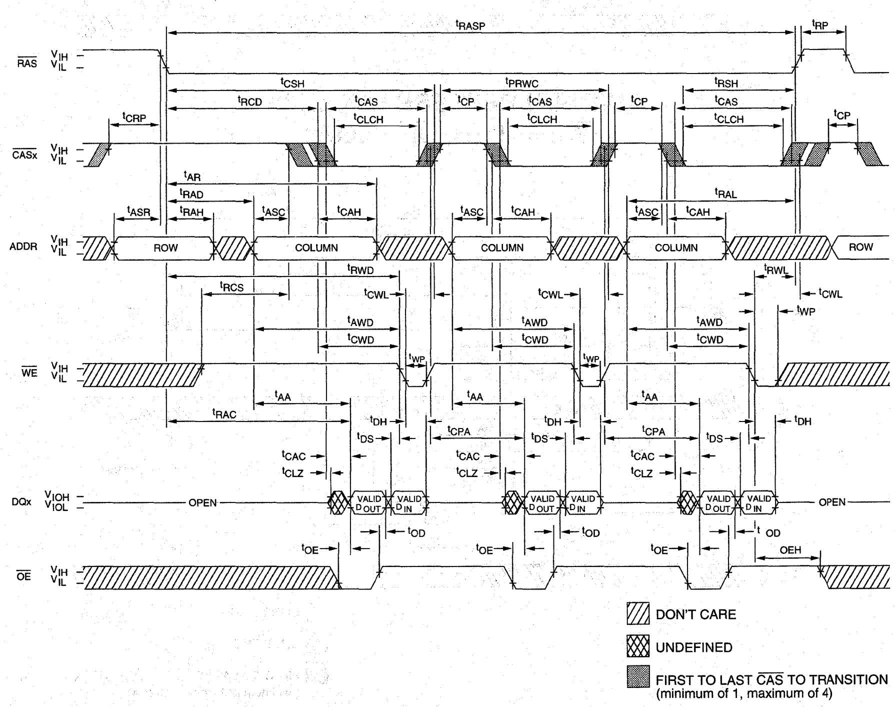
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE

(LATE-WRITE and READ-MODIFY-WRITE cycles)



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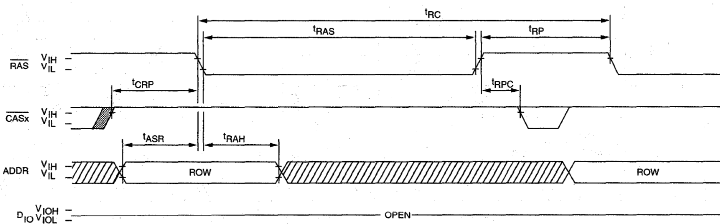
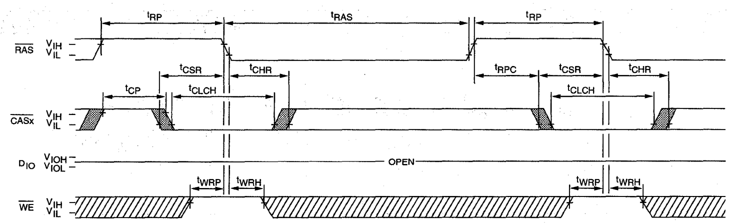
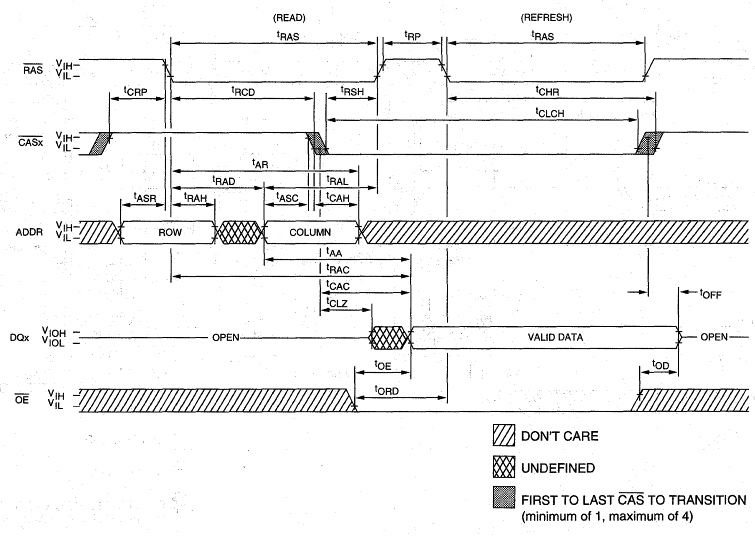
$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



CBR REFRESH CYCLE [25]
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

4 MEG x 4 DRAM

5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5.0V ±10% power supply
- Low power, 3mW standby; 250mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle (11 row-, 11 column-addresses)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh Rate	
Standard at 32ms period	None

- Part Number Example: MT4C4M4B1DJ-6

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DA-2) and **24/26-Pin TSOP (DB-2)**

Pin	Name	Pin	Name
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	NC	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

GENERAL DESCRIPTION

The MT4C4M4B1 is randomly accessed solid-state memories containing 16,777,216 bits organized in a x4 configuration. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle.

If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

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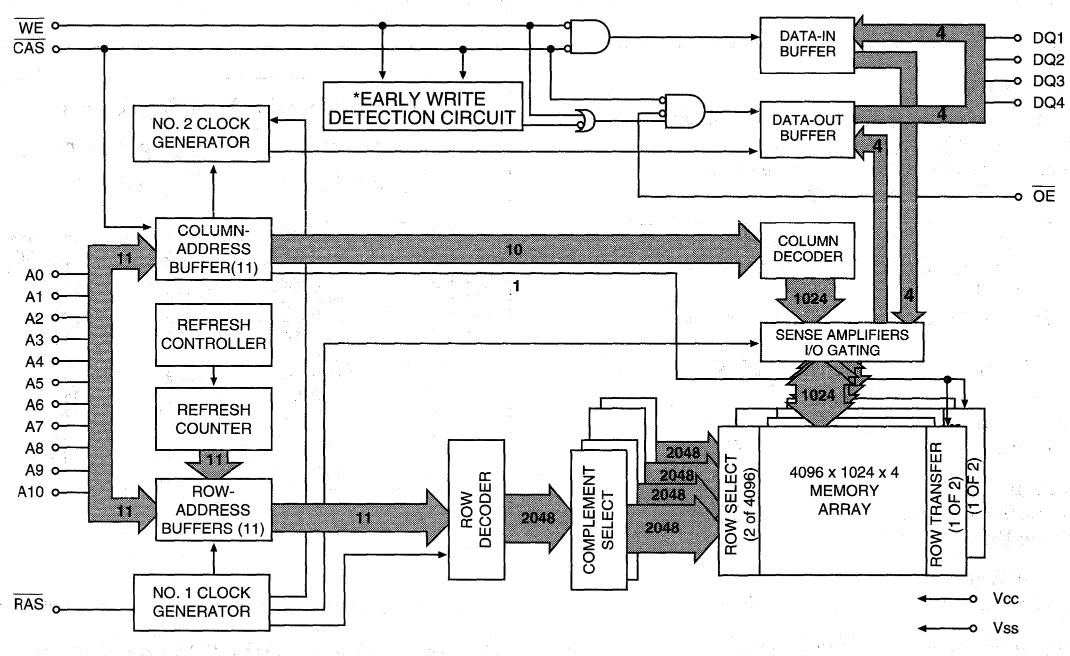
FPM DRAM

FUNCTIONAL BLOCK DIAGRAM
(11 row-addresses)



***NOTE:** 1. If WE goes LOW prior to CAS going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If CAS goes LOW prior to WE going LOW, EW detection circuit output is a LOW (LATE WRITE).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

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FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .. .. -1.0V to +7.0V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5.0mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)	VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	120	110	mA	3, 4, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	90	80	mA	3, 4, 28
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	120	110	mA	3, 28
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	120	110	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	7
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD	3	15	3	20	ns	
Output Enable	^tOE		15		20	ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18

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FPM DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	26
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	150		180		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transistion time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	25

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5.0V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ${}^tREF$ refresh requirement is exceeded.
8. AC characteristics assume ${}^tT$ = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ${}^tRCD$ < ${}^tRCD$ (MAX). If ${}^tRCD$ is greater than the maximum recommended value shown in this table, ${}^tRAC$ will increase by the amount that ${}^tRCD$ exceeds the value shown.
15. Assumes that ${}^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ${}^tCP$.
17. Operation within the ${}^tRCD$ (MAX) limit ensures that ${}^tRAC$ (MAX) can be met. ${}^tRCD$ (MAX) is specified as a reference point only; if ${}^tRCD$ is greater than the specified ${}^tRCD$ (MAX) limit, then access time is controlled exclusively by ${}^tCAC$.
18. Operation within the ${}^tRAD$ (MAX) limit ensures that ${}^tRAC$ (MIN) and ${}^tCAC$ (MIN) can be met. ${}^tRAD$ (MAX) is specified as a reference point only; if ${}^tRAD$ is greater than the specified ${}^tRAD$ (MAX) limit, then access time is controlled exclusively by ${}^tAA$.
19. Either ${}^tRCH$ or ${}^tRRH$ must be satisfied for a READ cycle.
20. ${}^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ${}^tWCS$, ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ are not restrictive operating parameters. ${}^tWCS$ applies to EARLY WRITE cycles. ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ apply to READ-MODIFY-WRITE cycles. If ${}^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ${}^tRWD \geq {}^tRWD$ (MIN), ${}^tAWD \geq {}^tAWD$ (MIN) and ${}^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ${}^tWCS$, ${}^tRWD$, ${}^tCWD$ and ${}^tAWD$ are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ${}^tWTS$ and ${}^tWTH$ are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ${}^tWRP$ and ${}^tWRH$ in the CBR REFRESH cycle.
26. 32ms is 2,048-cycle refresh.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.

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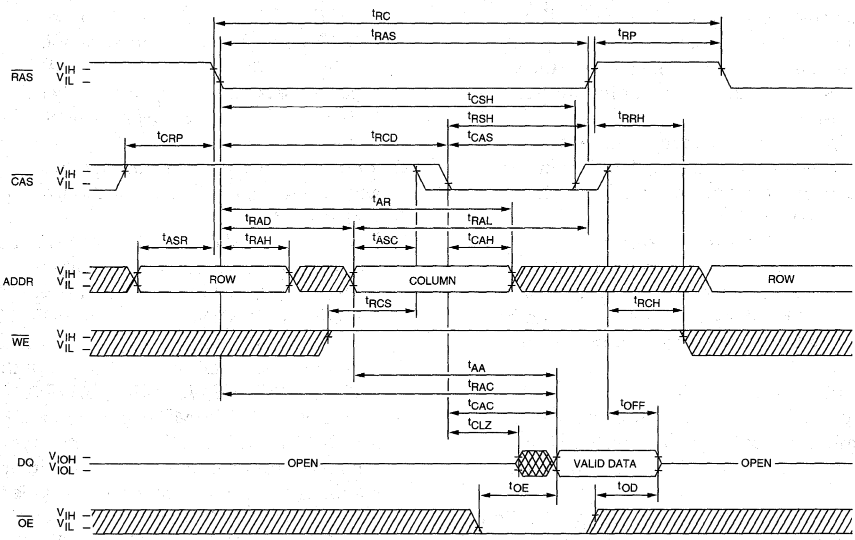
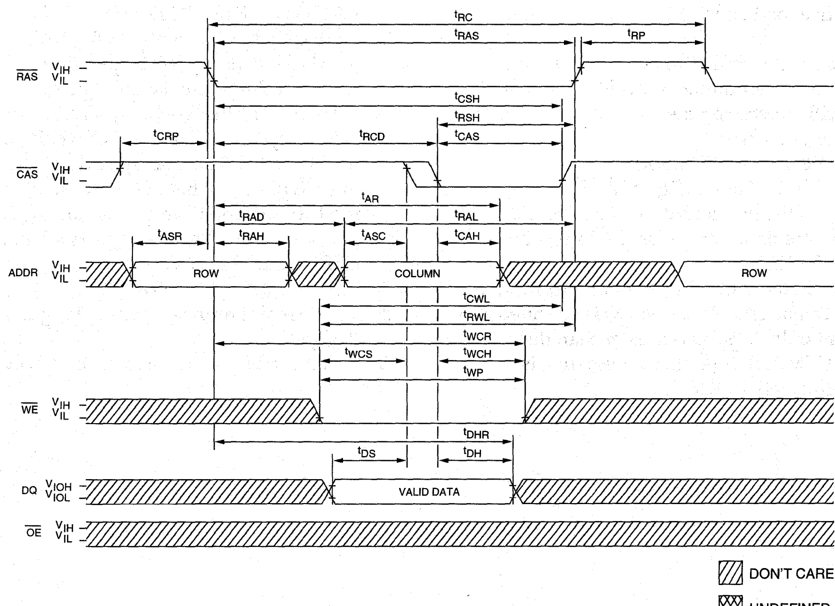
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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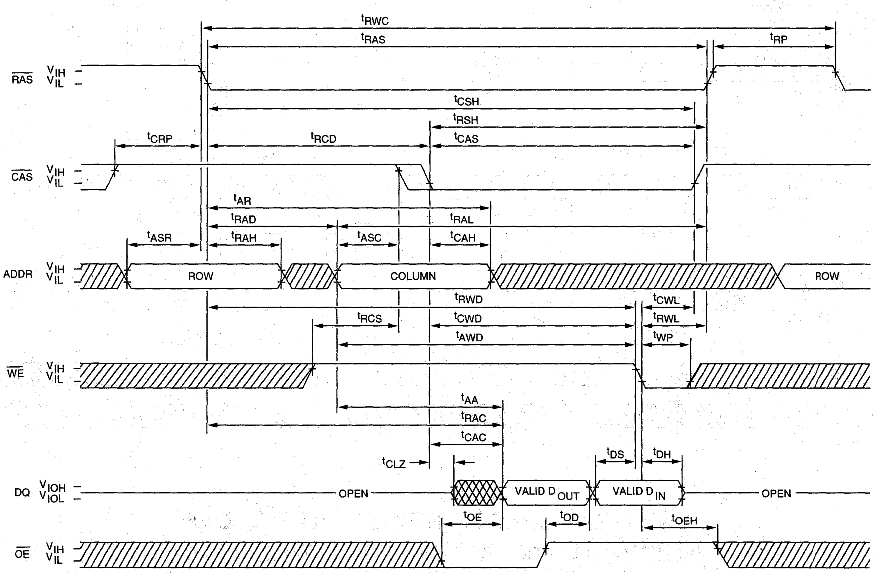
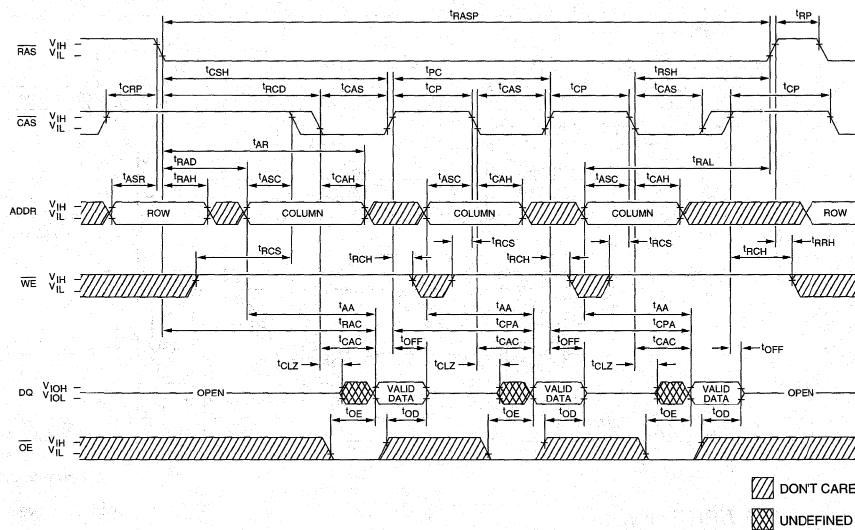
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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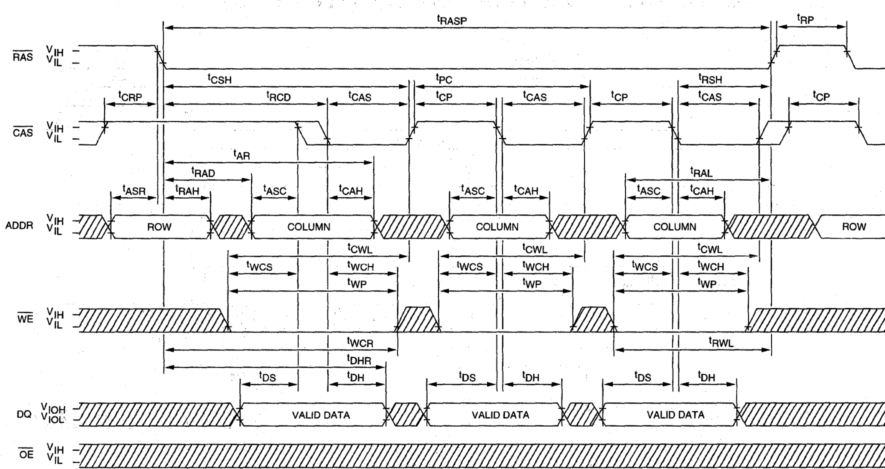
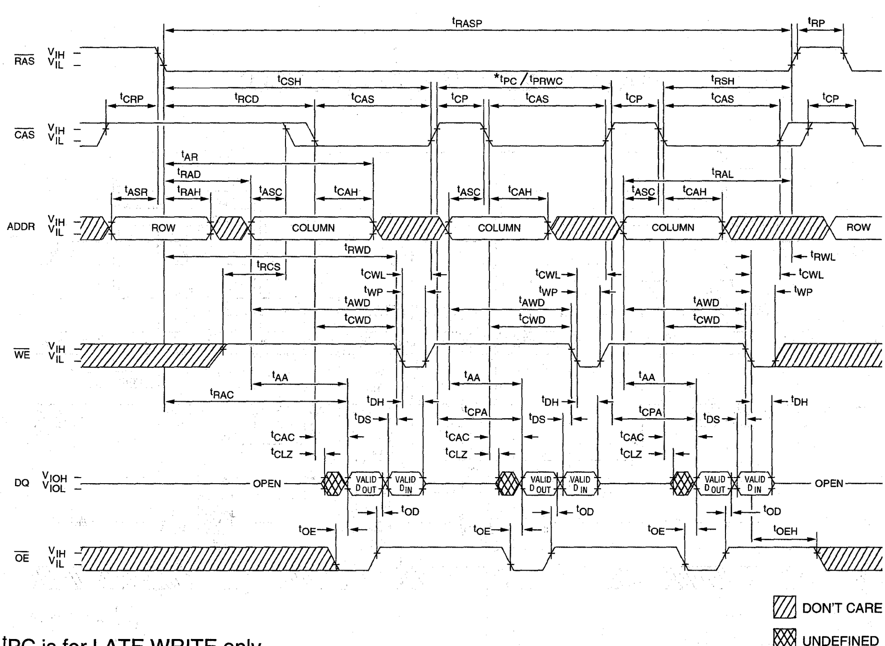
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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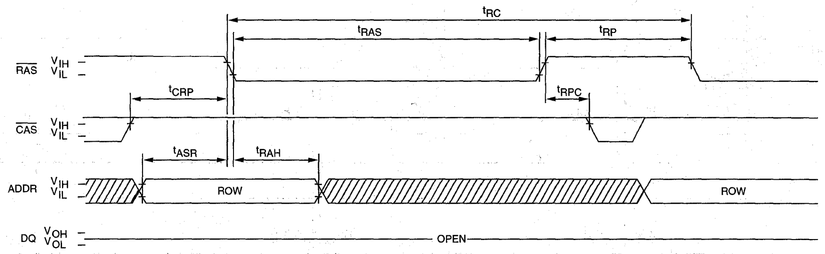
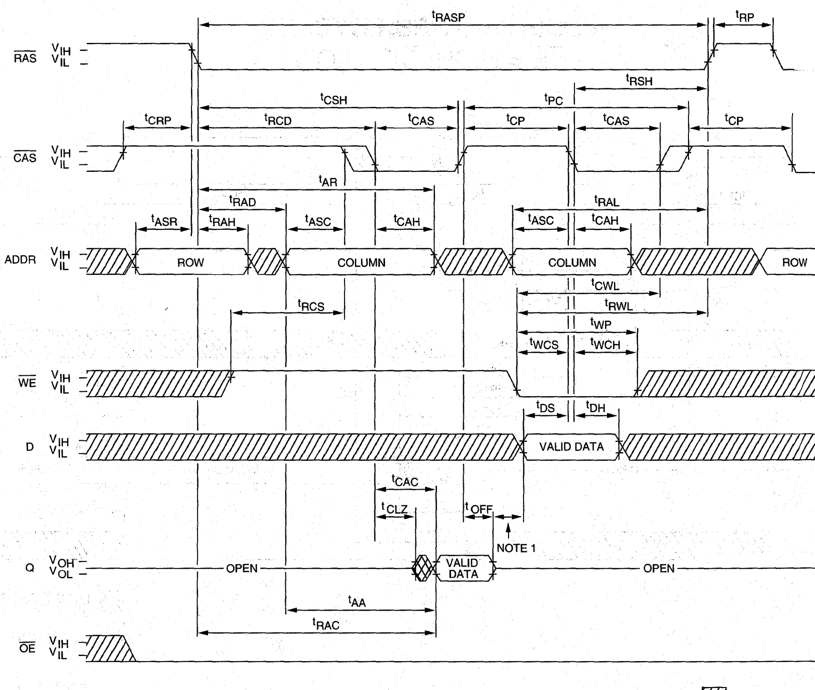
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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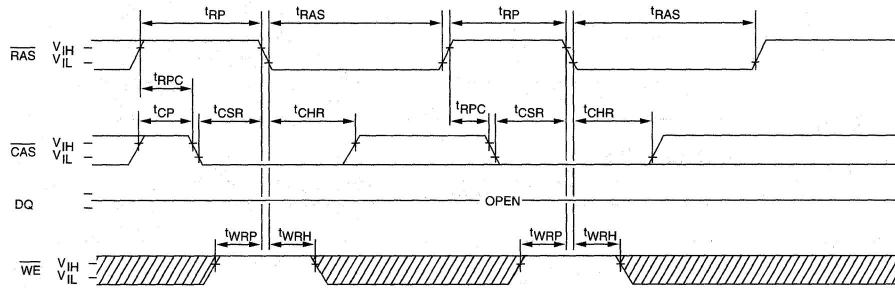
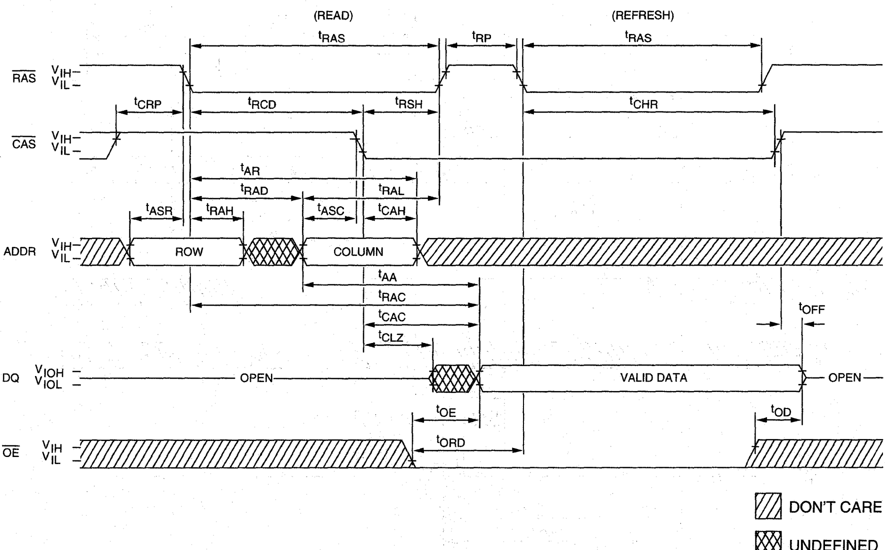
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

4 MEG x 4 DRAM

3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- Low power, 0.3mW standby; 180mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- 2,048-cycle (11 row-, 11 column-addresses)
- Optional SELF REFRESH mode, with Extended Refresh rate (4x)
- 5V tolerant I/Os (5.5V maximum VIH level)

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
• Refresh Rate	
Standard 32ms period	None
SELF REFRESH and 128ms period	S

- Part Number Example: MT4LC4M4B1DJ-7 S

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ (DA-2) and **24/26-Pin TSOP (DB-2)**

Pin	Name	Pin	Name
1	Vcc	26	Vss
2	DQ1	25	DQ4
3	DQ2	24	DQ3
4	WE	23	CAS
5	RAS	22	OE
6	NC	21	A9
8	A10	19	A8
9	A0	18	A7
10	A1	17	A6
11	A2	16	A5
12	A3	15	A4
13	Vcc	14	Vss

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

GENERAL DESCRIPTION

The MT4LC4M4B1(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle.

If WE goes LOW after data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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REFRESH

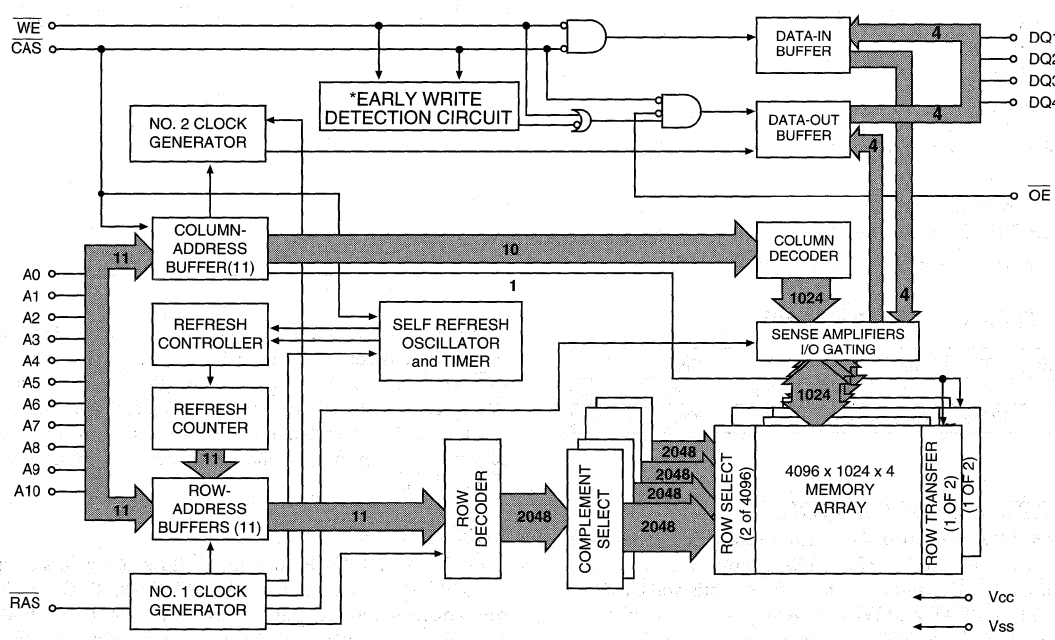
Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC4M4B1(S). The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms four times longer than the standard 32ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^tRPS ($\approx {}^tRC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
MT4LC4M4B1 (11 row-addresses)



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).
3. SELF REFRESH oscillator and timer (S version only).

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply Relative to Vss .... -1.0V to +4.6V
Voltage on Inputs or I/O Relative to Vss .... -1.0V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	VIH	2.0	5.5V	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	500	500	µA	
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	90	80	mA	3, 4, 29
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	mA	3, 29
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	120	110	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current, CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$, and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5

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FPM DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	CI1	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	CI2	7	pF	2
Input/Output Capacitance: DQ	CIO	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address hold time (referenced to RAS)	tAR	50		55		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to WE delay time	tAWD	55		60		ns	21
Access time from CAS	tCAC		15		20	ns	15
Column-address hold time	tCAH	10		15		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	ns	
CAS hold time entering SELF REFRESH	tCHD	15		15		ns	28
CAS hold time (CBR REFRESH)	tCHR	15		15		ns	5
CAS to output in Low-Z	tCLZ	3		3		ns	28
CAS precharge time	tCP	10		10		ns	16
Access time from CAS precharge	tCPA		35		40	ns	
CAS to RAS precharge time	tCRP	5		5		ns	
CAS hold time	tCSH	60		70		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		ns	5
CAS to WE delay time	tCWD	40		45		ns	21
Write command to CAS lead time	tCWL	15		20		ns	
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	22
Output disable	tOD	3	15	3	20	ns	28
Output Enable	tOE		15		20	ns	23
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	ns	20, 27
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		ns	
Access time from RAS	tRAC		60		70	ns	14

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{\text{RAS}}$ to column-address delay time	tRAD	15	30	15	35	ns	18
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ pulse width entering SELF REFRESH	tRASS	100		100		µs	28
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{\text{CAS}}$)	tRCH	0		0		ns	19
Read command setup time	tRCS	0		0		ns	
Refresh period (2,048 cycles)	tREF		32		32	ms	26
Refresh period (2,048 cycles) S version	tREF		128		128	ms	
$\overline{\text{RAS}}$ precharge time	tRP	40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	0		0		ns	
$\overline{\text{RAS}}$ precharge time exiting SELF REFRESH	tRPS	110		130		ns	28
Read command hold time (referenced to $\overline{\text{RAS}}$)	tRRH	0		0		ns	19
$\overline{\text{RAS}}$ hold time	tRSH	15		20		ns	
READ WRITE cycle time	tRWC	150		180		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	tRWD	85		95		ns	21
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	tWCR	45		55		ns	
$\overline{\text{WE}}$ command setup time	tWCS	0		0		ns	21
Write command pulse width	tWP	10		15		ns	
$\overline{\text{WE}}$ hold time (CBR REFRESH)	tWRH	10		10		ns	25
$\overline{\text{WE}}$ setup time (CBR REFRESH)	tWRP	10		10		ns	25

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. 32ms is a 2,048-cycle refresh.
27. The 3ns minimum is a parameter guaranteed by design.
28. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
29. Column-address changed once each cycle.

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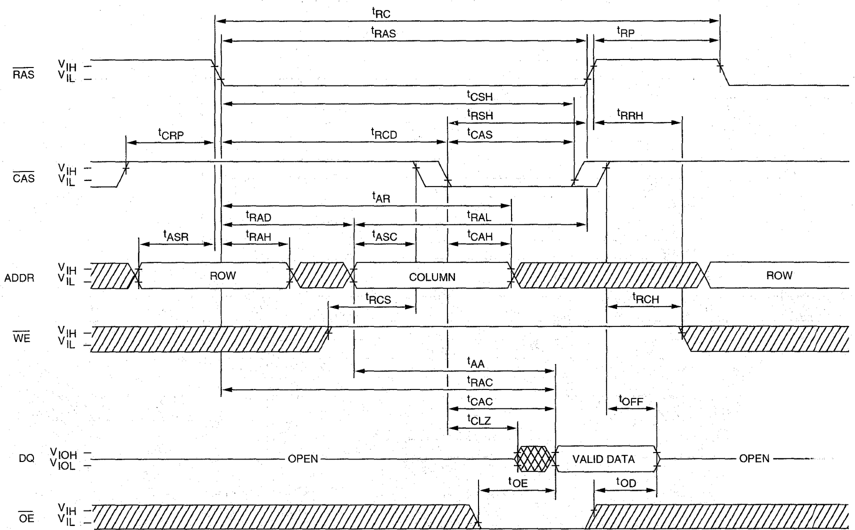
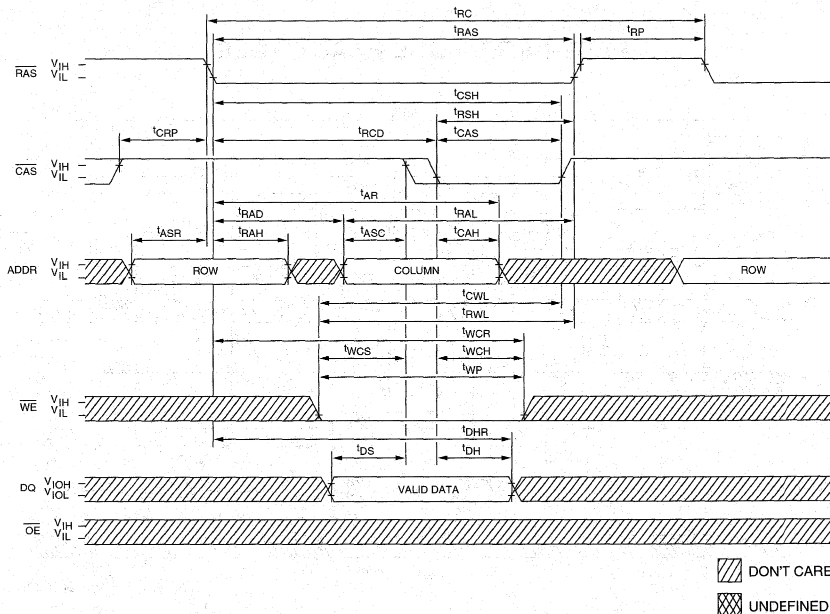
READ CYCLE



EARLY WRITE CYCLE



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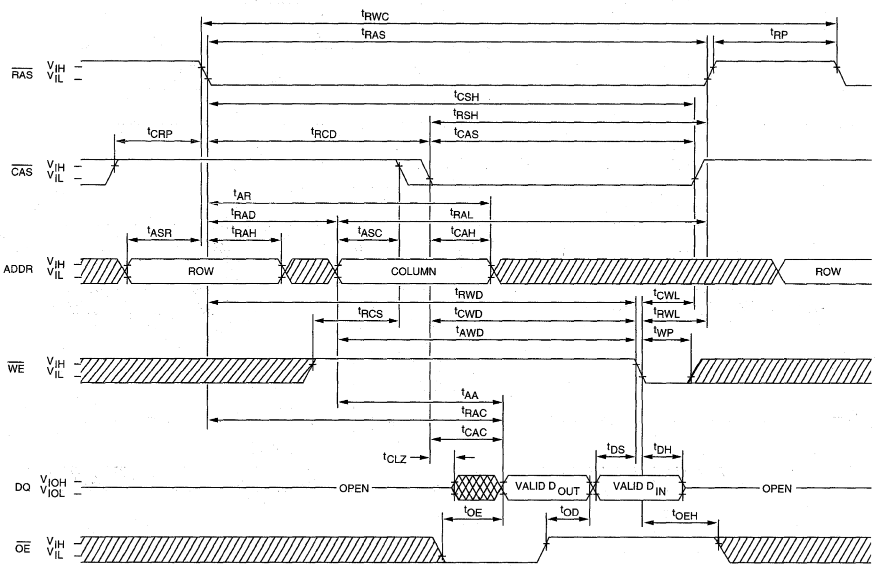
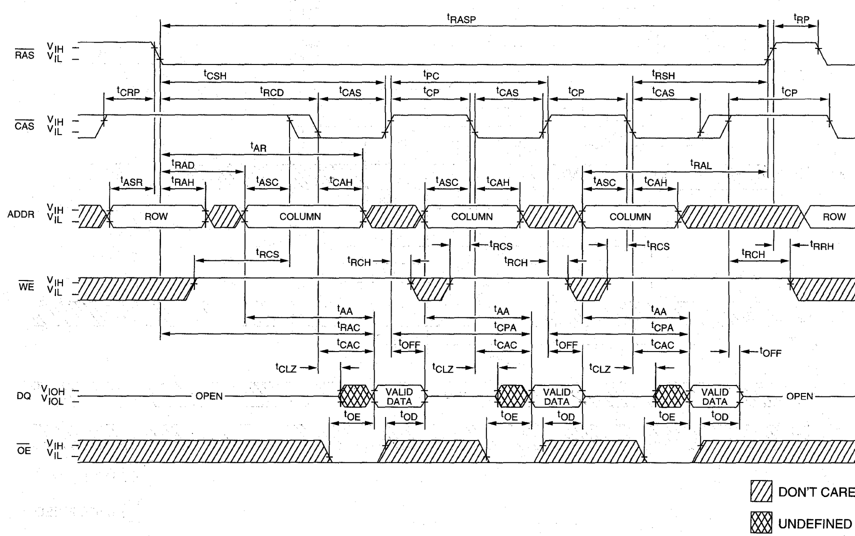
READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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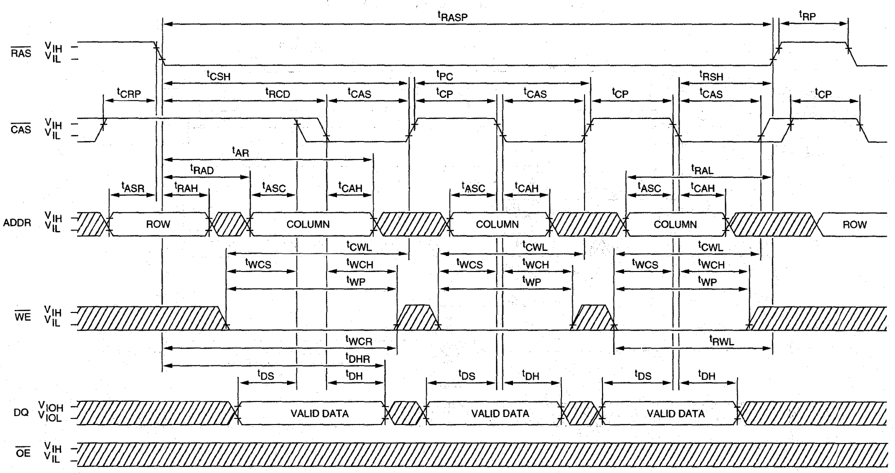
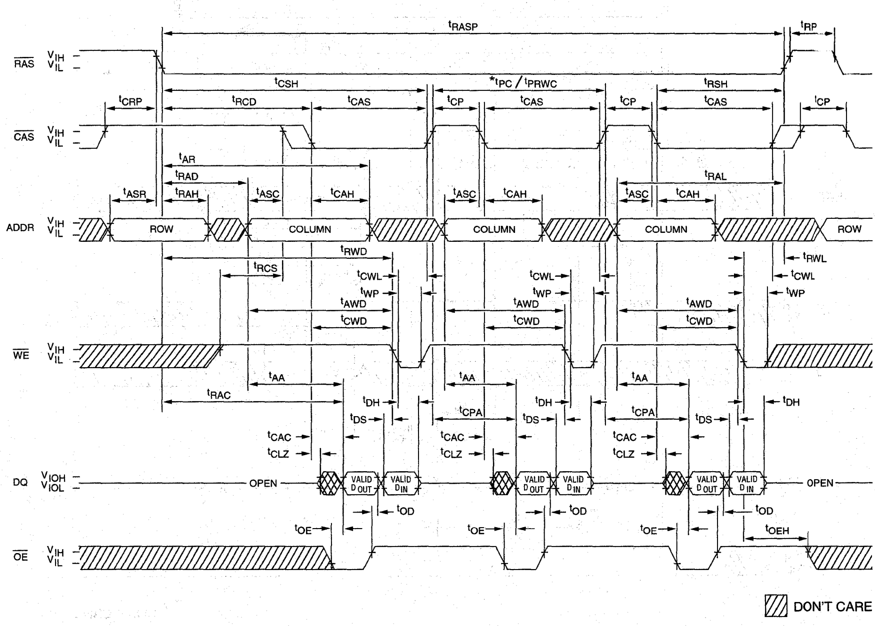
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



DON'T CARE

UNDEFINED

***NOTE:** 1. tPC is for LATE WRITE only.

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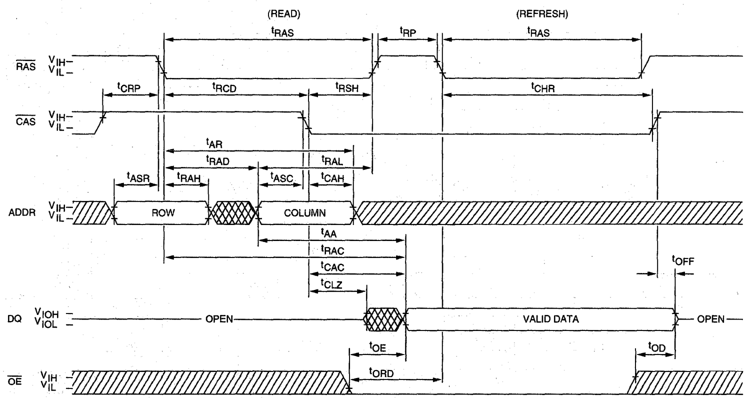
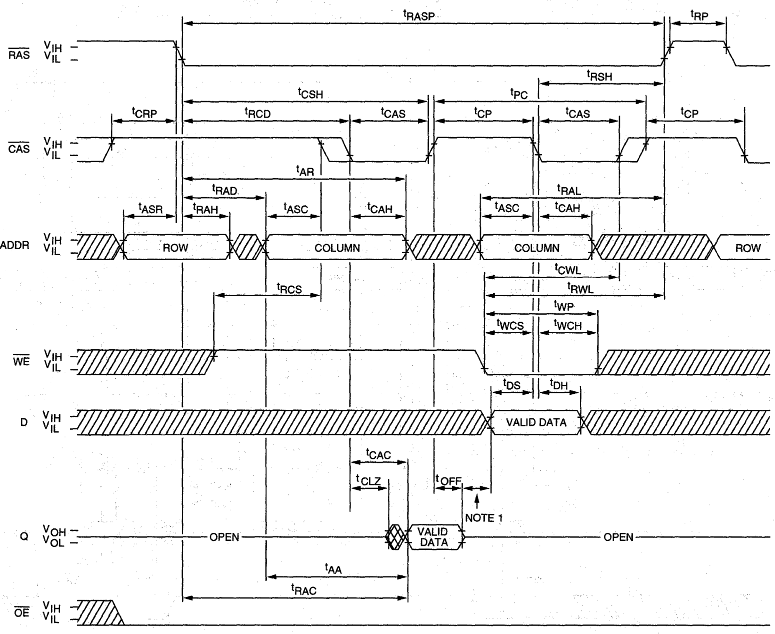
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



DON'T CARE

UNDEFINED

NOTE: 1. Do not drive data prior to tristate.

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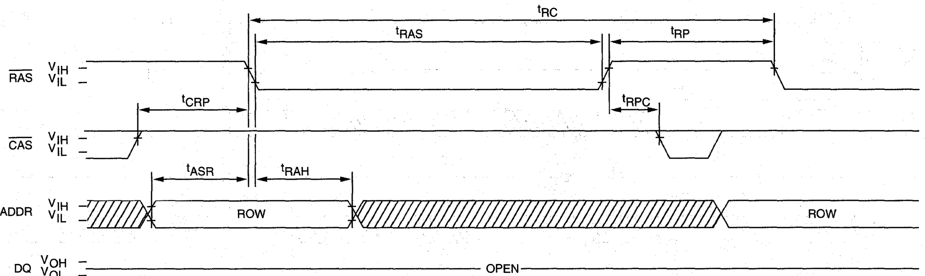
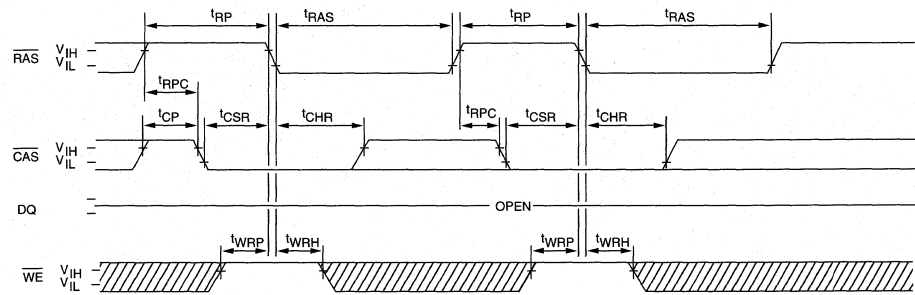
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



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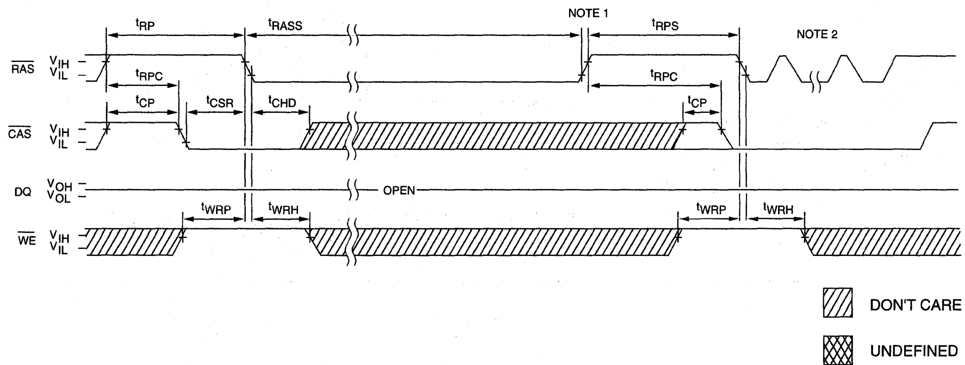
SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ^tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM

16 MEG x 4 DRAM

3.3V, FAST PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions and packages
- 13 row-addresses, 11 column-addresses (A7) or 12 row-addresses, 12 column-addresses (T8)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- FAST PAGE MODE access
- 4,096-cycle $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH distributed across 64ms

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (500 mil)	DW
Plastic TSOP (500 mil)	TW

- Part Number Example: MT4LC16M4A7DW-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns
-7	130ns	70ns	40ns	35ns	20ns

GENERAL DESCRIPTION

The MT4LC16M4A7 and MT4LC16M4T8 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate from 3.0V to 3.6V. The MT4LC16M4A7 and MT4LC16M4T8 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 8,192 rows by 2,048 columns for the MT4LC16M4A7 or 4,096 rows by 4,096 columns for the MT4LC16M4T8. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the $\overline{RAS}$ signal, then the column address by $\overline{CAS}$. Both devices provide FAST PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC16M4A7 and MT4LC16M4T8 must be refreshed periodically in order to retain stored data.

PIN ASSIGNMENT (Top View)

34-Pin SOJ (DA-6)

Signal	Pin	Pin	Signal
Vcc	1	34	Vss
DQ1	2	33	DQ4
DQ2	3	32	DQ3
NC	4	31	NC
NC	5	30	NC
NC	6	29	NC
NC	7	28	$\overline{CAS}$
$\overline{WE}$	8	27	$\overline{OE}$
$\overline{RAS}$	9	26	NC
NC	10	25	A12/NC
A0	11	24	A11
A1	12	23	A10
A2	13	22	A9
A3	14	21	A8
A4	15	20	A7
A5	16	19	A6
Vcc	17	18	Vss

34-Pin TSOP*

Signal	Pin	Pin	Signal
Vcc	1	34	Vss
DQ1	2	33	DQ4
DQ2	3	32	DQ3
NC	4	31	NC
NC	5	30	NC
NC	6	29	NC
NC	7	28	$\overline{CAS}$
$\overline{WE}$	8	27	$\overline{OE}$
$\overline{RAS}$	9	26	NC
NC	10	25	A12/NC
A0	11	24	A11
A1	12	23	A10
A2	13	22	A9
A3	14	21	A8
A4	15	20	A7
A5	16	19	A6
Vcc	17	18	Vss

*Consult factory for dimensions and availability.

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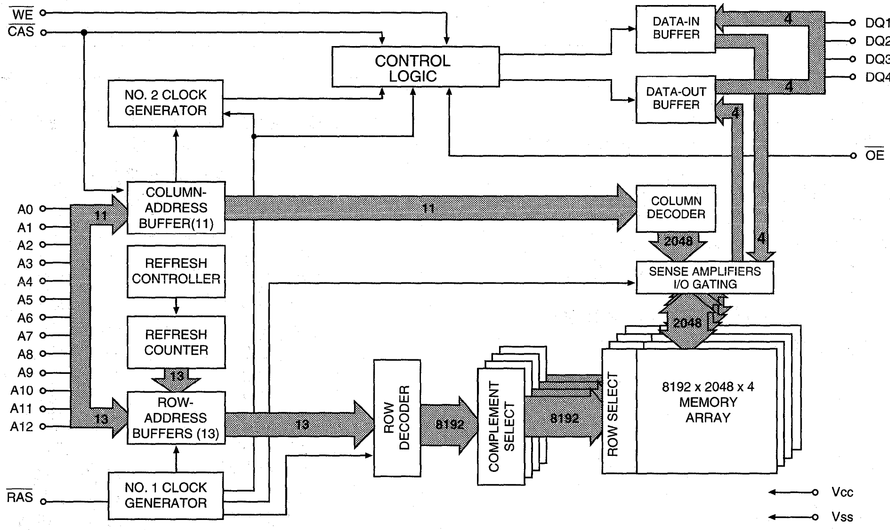
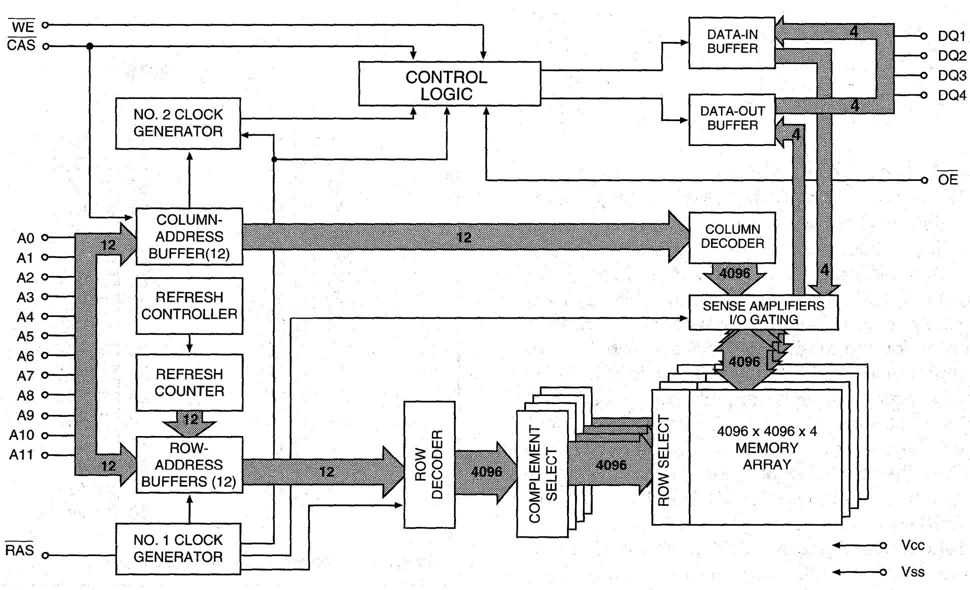
FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4A7 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC16M4T8 (12 row-addresses)



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FUNCTIONAL DESCRIPTION

The functional description for the MT4LC16M4A7 and MT4LC16M4T8 is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet following the timing specifications tables.

DRAM ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ1-4). The $\overline{WE}$ signal must be activated to execute a write operation, otherwise a read operation will be performed. The $\overline{OE}$ signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST PAGE MODE operations are always initiated with a row-address strobed-in by the $\overline{RAS}$ signal, followed by a column-address strobed-in by $\overline{CAS}$, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page-mode cycle time. This is accomplished by cycling $\overline{CAS}$ while holding $\overline{RAS}$ LOW, and entering new column addresses with each $\overline{CAS}$ cycle. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (A7) or all 4,096 rows (T8) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4A7 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4T8 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. Alternatively, $\overline{RAS}$-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time, so for the MT4LC16M4A7, 8,192 $\overline{RAS}$-ONLY REFRESH cycles must be executed every 64ms to cover all rows.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss .... -1.0V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1.0V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 3.6V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 3.6V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -5	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MT4LC4M16A7	I_{CC1}	1	1	1	mA	
	MT4LC4M16T8	I_{CC1}	1	1	1		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ ≥ Vcc -0.2V, DQs may be left open, Other inputs: V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V)	MT4LC4M16A7	I_{CC2}	500	500	500	µA	
	MT4LC4M16T8	I_{CC2}	500	500	500		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC = {}^tRC$ [MIN])	MT4LC4M16A7	I_{CC3}	130	120	110	mA	3, 4, 29
	MT4LC4M16T8	I_{CC3}	170	160	150		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC = {}^tPC$ [MIN])	MT4LC4M16A7	I_{CC4}	100	90	80	mA	3, 4, 29
	MT4LC4M16T8	I_{CC4}	100	90	80		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC = {}^tRC$ [MIN])	MT4LC4M16A7	I_{CC5}	130	120	110	mA	3, 26
	MT4LC4M16T8	I_{CC5}	170	160	150		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC = {}^tRC$ [MIN])	MT4LC4M16A7	I_{CC6}	140	130	120	mA	3, 5
	MT4LC4M16T8	I_{CC6}	170	160	150		

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		25		30		35	ns	
Column-address hold time (referenced to RAS)	^tAR	40		45		55		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to WE delay time	^tAWD	48		55		65		ns	21
Access time from CAS	^tCAC		13		15		20	ns	15
Column-address hold time	^tCAH	8		10		15		ns	
CAS pulse width	^tCAS	13	10,000	15	10,000	20	10,000	ns	
CAS hold time (CBR REFRESH)	^tCHR	15		15		15		ns	5
CAS to output in Low-Z	^tCLZ	0		0		0		ns	
CAS precharge time (FAST PAGE MODE)	^tCP	8		10		10		ns	16
Access time from CAS precharge	^tCPA		30		35		40	ns	
CAS to RAS precharge time	^tCRP	5		5		5		ns	
CAS hold time	^tCSH	50		60		70		ns	
CAS setup time (CBR REFRESH)	^tCSR	5		5		5		ns	5
CAS to WE delay time	^tCWD	36		40		50		ns	21
Write command to CAS lead time	^tCWL	13		15		20		ns	
Data-in hold time	^tDH	8		10		15		ns	22
Data-in hold time (referenced to RAS)	^tDHR	40		45		55		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Output disable	^tOD	0	13	0	15	0	20	ns	27, 28
Output Enable time	^tOE		13		15		20	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	13		15		20		ns	28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	ᵗOFF	0	13	0	15	0	20	ns	20, 27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	ᵗORD	0		0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	ᵗPC	30		35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	ᵗPRWC	76		85		100		ns	
Access time from $\overline{RAS}$	ᵗRAC		50		60		70	ns	14
$\overline{RAS}$ to column-address delay time	ᵗRAD	13	25	15	30	15	35	ns	18
Row-address hold time	ᵗRAH	8		10		10		ns	
Column-address to $\overline{RAS}$ lead time	ᵗRAL	25		30		35		ns	
$\overline{RAS}$ pulse width	ᵗRAS	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	ᵗRASP	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	ᵗRC	90		110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	ᵗRCD	18	37	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	ᵗRCH	0		0		0		ns	19
Read command setup time	ᵗRCS	0		0		0		ns	
Refresh period	ᵗREF		64		64		64	ms	26
$\overline{RAS}$ precharge time	ᵗRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	ᵗRPC	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	ᵗRRH	0		0		0		ns	19
$\overline{RAS}$ hold time	ᵗRSH	13		15		20		ns	
READ WRITE cycle time	ᵗRWC	131		155		185		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	ᵗRWD	73		85		100		ns	21
Write command to $\overline{RAS}$ lead time	ᵗRWL	13		15		20		ns	
Transition time (rise or fall)	ᵗT	1	50	1	50	1	50	ns	
Write command hold time	ᵗWCH	8		10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	ᵗWCR	40		45		55		ns	
$\overline{WE}$ command setup time	ᵗWCS	0		0		0		ns	21
Write command pulse width	ᵗWP	8		10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	ᵗWRH	10		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	ᵗWRP	10		10		10		ns	25

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. The values shown were calculated for reference allowing 10ns for the external latching of read data and application of write data. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. $\overline{RAS}$-ONLY REFRESH requires that all 8,192 rows of the MT4LC16M4A7, or all 4,096 rows of the MT4LC16M4T8, be refreshed at least once every 64ms. CBR REFRESH, for either device, requires that at least 4,096 cycles be completed every 64ms.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
29. Column-address changed once each cycle.

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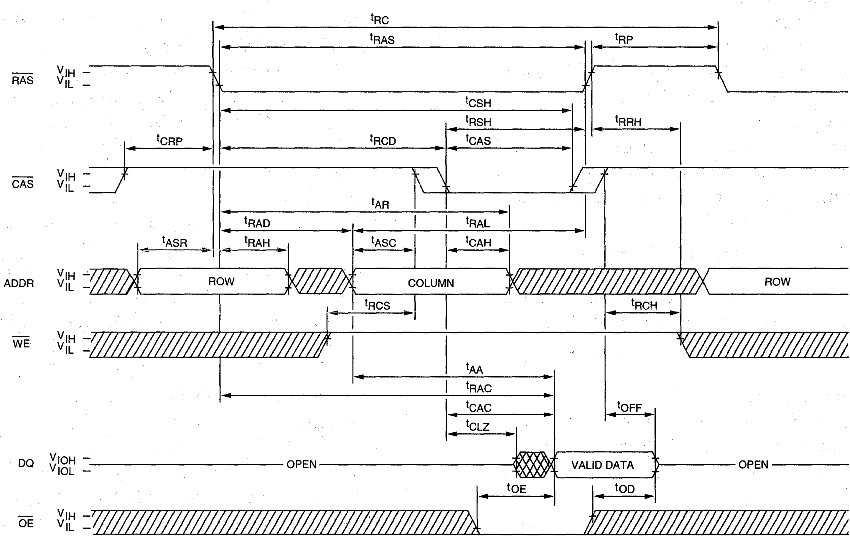
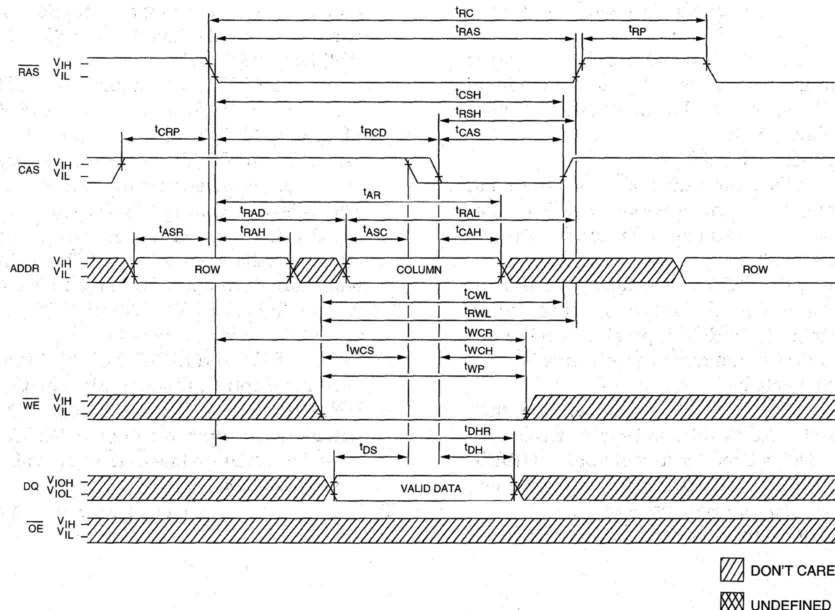
NEW FPM DRAM

READ CYCLE



EARLY WRITE CYCLE



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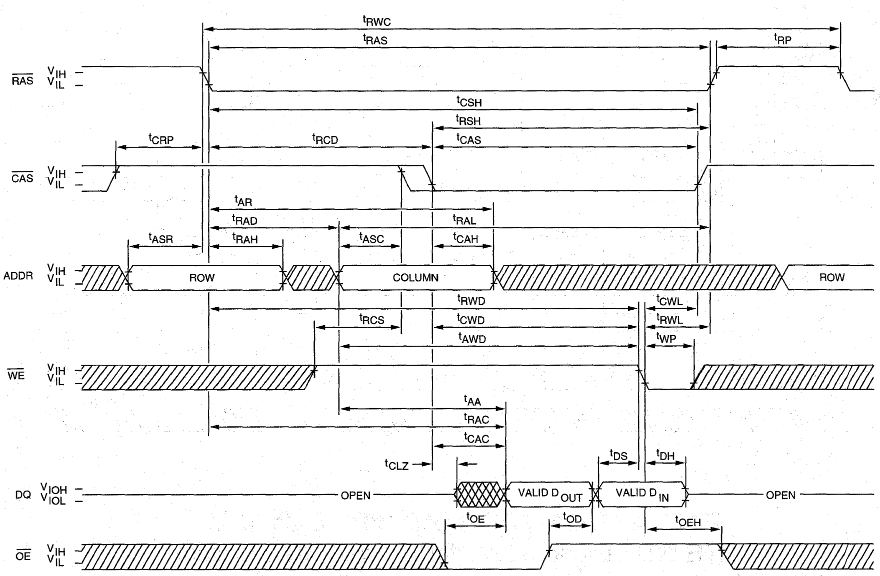
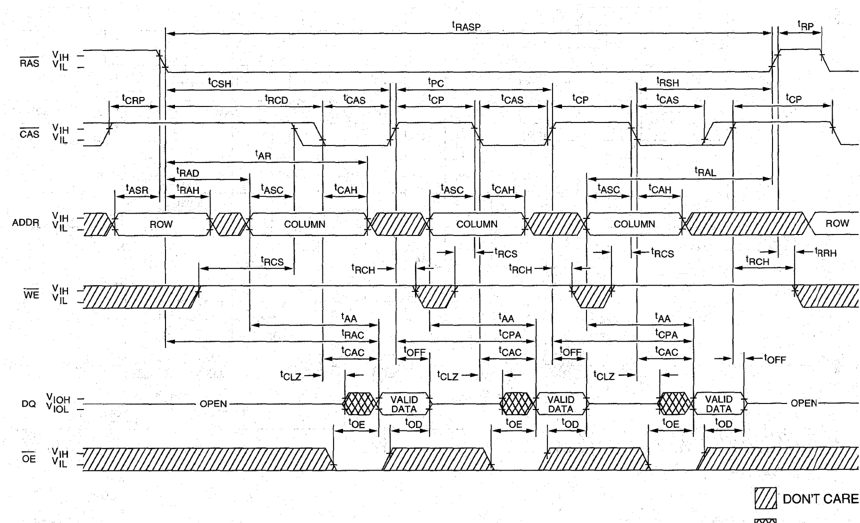
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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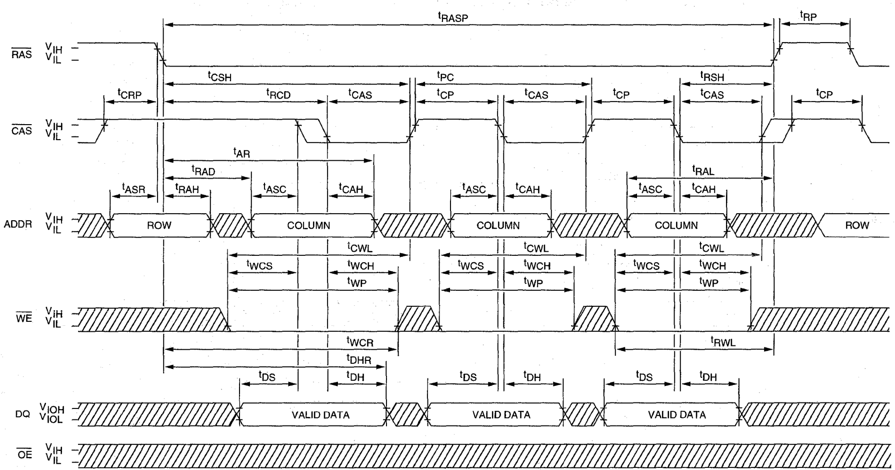
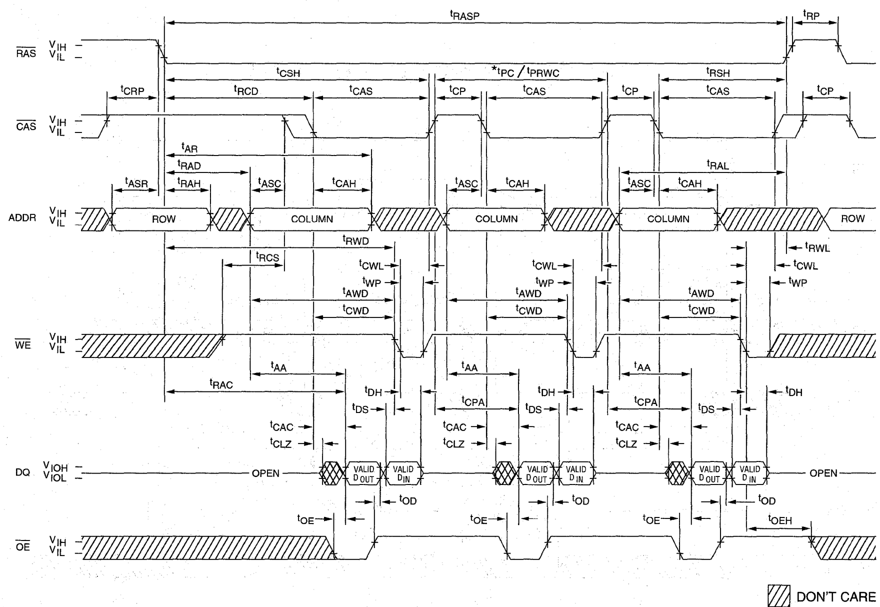
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



*NOTE: 1. tPC is for LATE WRITE only.

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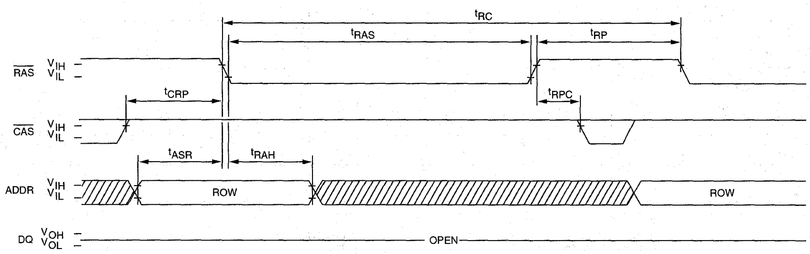
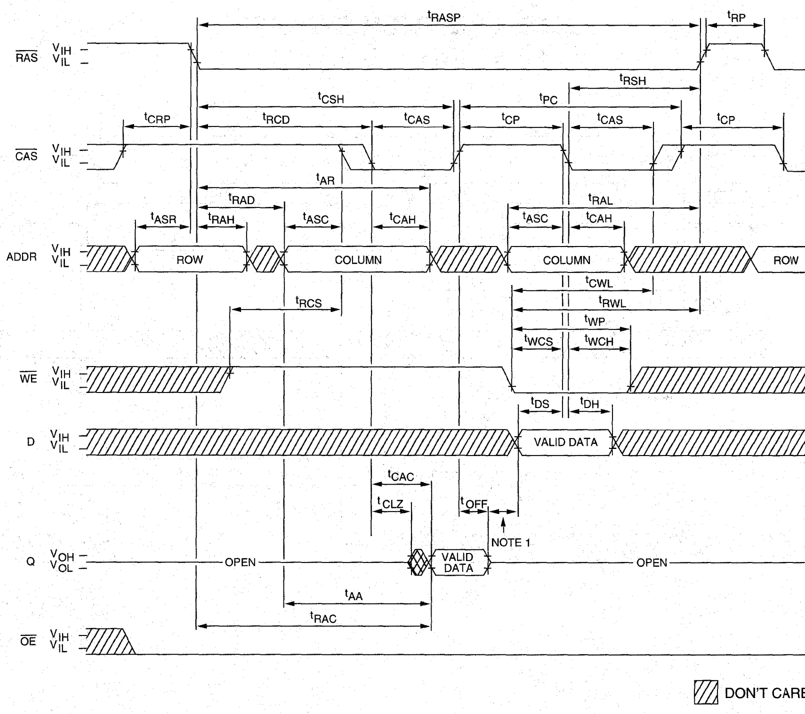
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive input data prior to output data going High-Z.

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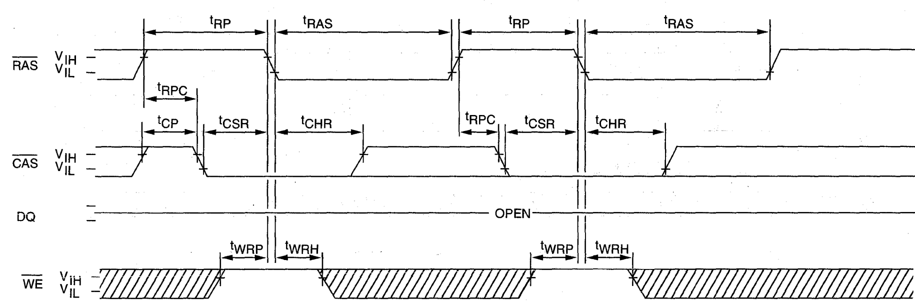
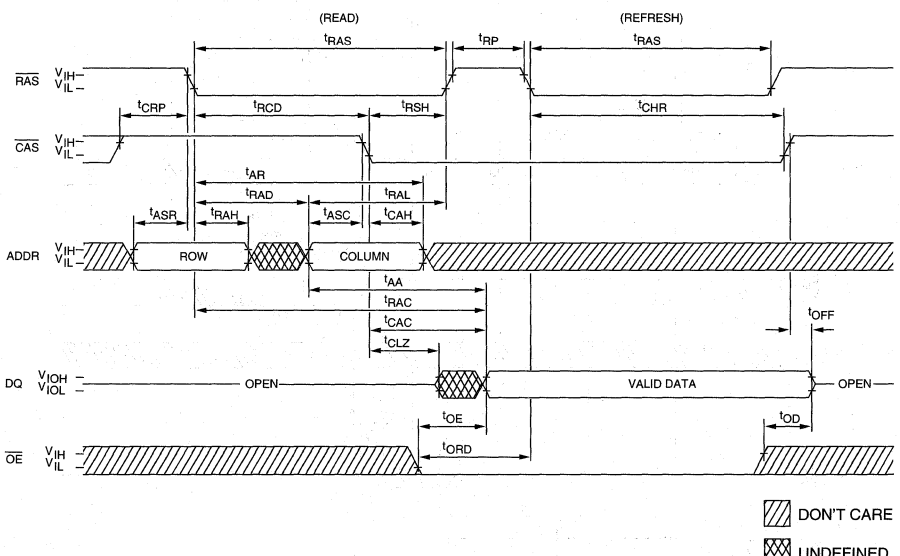
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

2 MEG x 8 DRAM

3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x8 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- Low power, 0.3mW standby; 200mW active, typical
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and SELF
- 2,048-cycle refresh (11 row-, 10 column-addresses)
- Optional SELF REFRESH mode, with Extended Refresh rate (4x)
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic 28-pin SOJ (300 mil) — DJ
  - Plastic 28-pin TSOP (300 mil) — TG
- Refresh Rate
  - Standard 32ms period — None
  - SELF REFRESH and 128ms period — S
- Part Number Example: MT4LC2M8B1DJ-7 S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

28-Pin SOJ (DA-4) and **28-Pin TSOP (DB-3)**

Pin	Name	Pin	Name
1	Vcc	28	Vss
2	DQ1	27	DQ8
3	DQ2	26	DQ7
4	DQ3	25	DQ6
5	DQ4	24	DQ5
6	$\overline{WE}$	23	$\overline{CAS}$
7	$\overline{RAS}$	22	$\overline{OE}$
8	NC	21	A9
9	A10	20	A8
10	A0	19	A7
11	A1	18	A6
12	A2	17	A5
13	A3	16	A4
14	Vcc	15	Vss

GENERAL DESCRIPTION

The MT4LC2M8B1(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x8 configuration. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 11 bits (A0-A10) and then $\overline{CAS}$ latching 10 bits (A0-A9).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

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FAST PAGE MODE (continued)

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

REFRESH

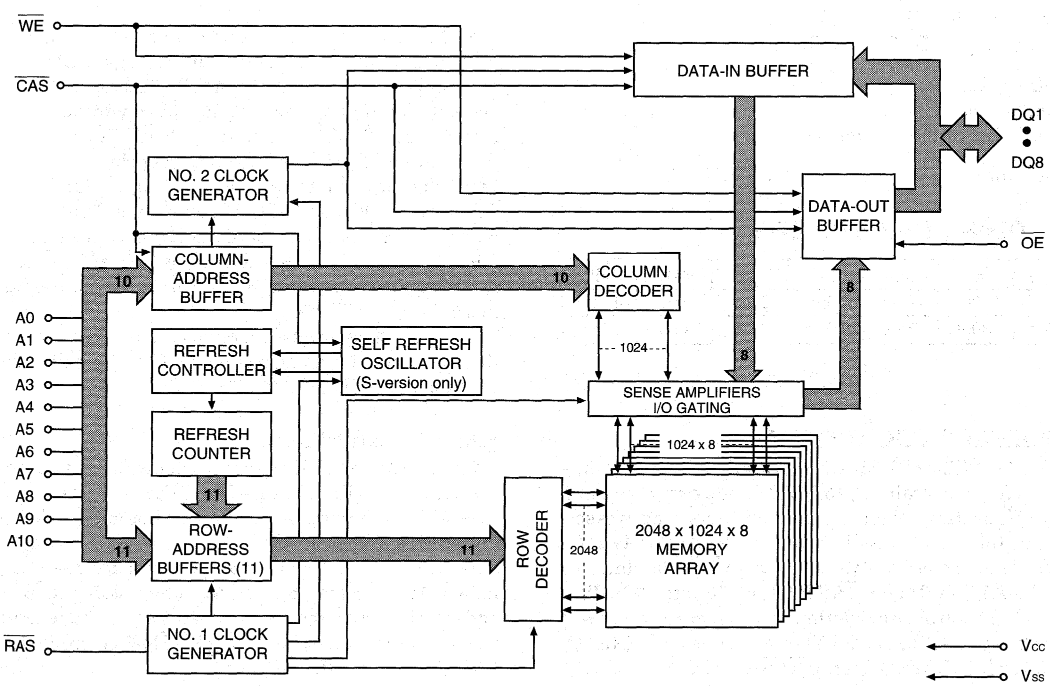
Preserve correct memory cell data by maintaining power and executing a RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available on the MT4LC2M8B1 S. The "S" version allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ᵗRPS (≈ᵗRC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
2,048 ROWS



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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DQs
						^tR	^tC	
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	5.5V	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

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FPM DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	500	500	µA	
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	130	120	mA	3, 4, 27
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	90	80	mA	3, 4, 27
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	130	120	mA	3, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	130	120	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$ = V_{CC} -0.2V, $\overline{OE}$, A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open), ^tRC = 62.5µs (2,048 rows at 62.5µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A10,$\overline{OE}$ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5

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FPM DRAM

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	15		15		ns	26
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	28
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD	3	15	3	20	ns	28
Output Enable	^tOE		15		20	ns	23
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 28
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +3.3V to 0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Row-address hold time	tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width entering SELF REFRESH	tRASS	100		100		µs	26
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		ns	19
Read command setup time	tRCS	0		0		ns	
Refresh period (2,048 cycles)	tREF		32		32	ms	26
Refresh period (2,048 cycles) S version	tREF		128		128	ms	
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{RAS}$ precharge time exiting SELF REFRESH	tRPS	110		130		ns	26
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{RAS}$ hold time	tRSH	15		20		ns	
READ WRITE cycle time	tRWC	150		180		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		95		ns	21
Write command to $\overline{RAS}$ lead time	tRWL	15		20		ns	
Transistion time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	
$\overline{WE}$ command setup time	tWCS	0		0		ns	21
Write command pulse width	tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	25

FPM DRAM

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gate, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR refresh cycle.
26. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
27. Column-address changed once each cycle.
28. The 3ns minimum is guaranteed by design.

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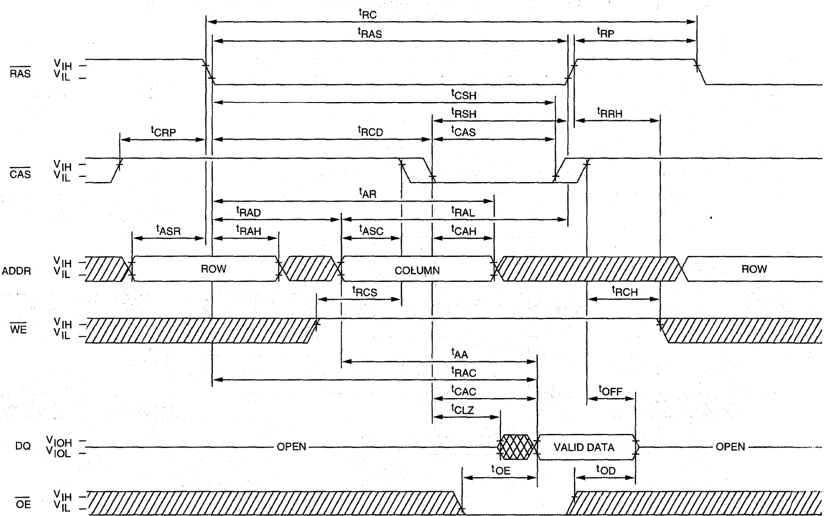
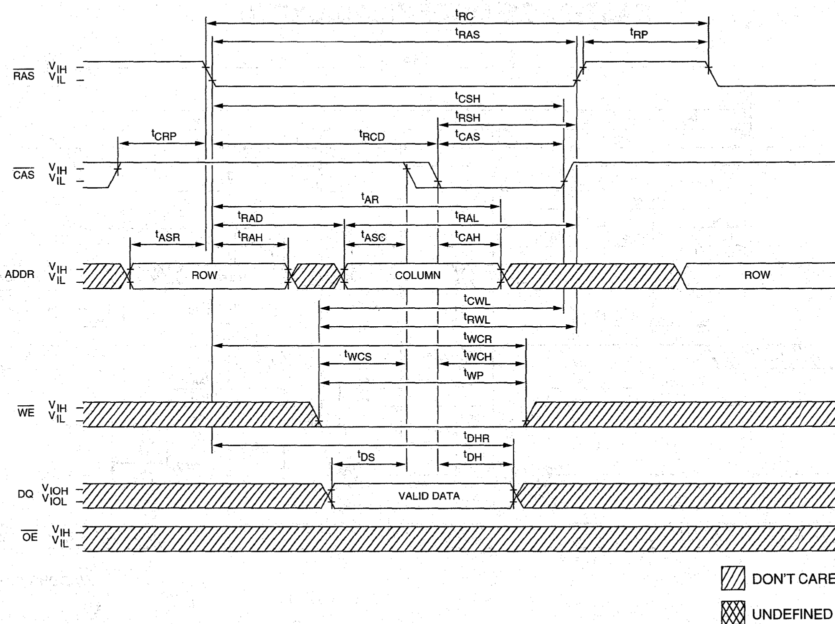
READ CYCLE



EARLY WRITE CYCLE



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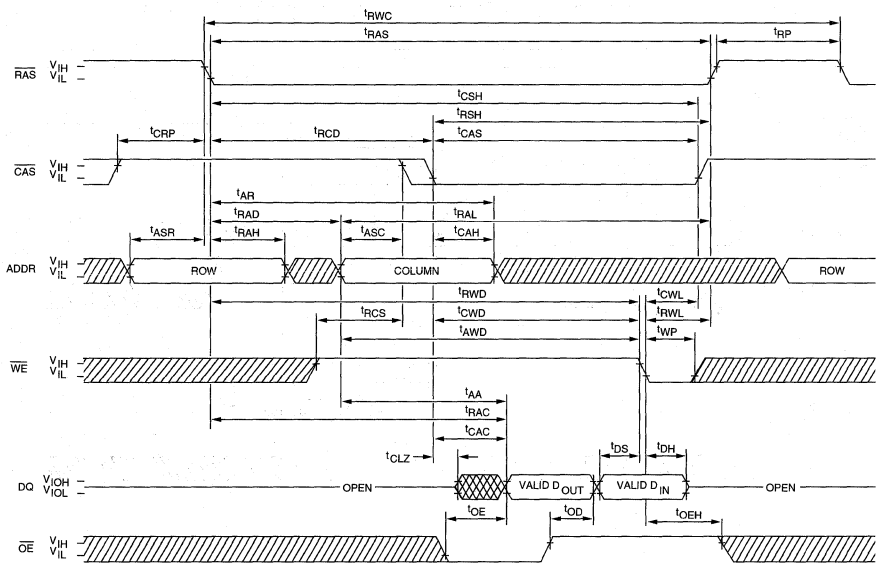
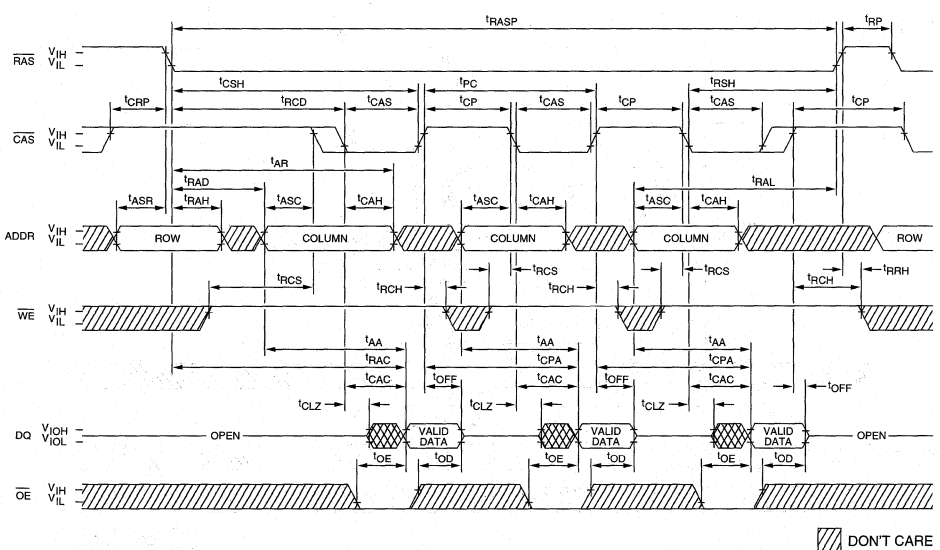
FPM DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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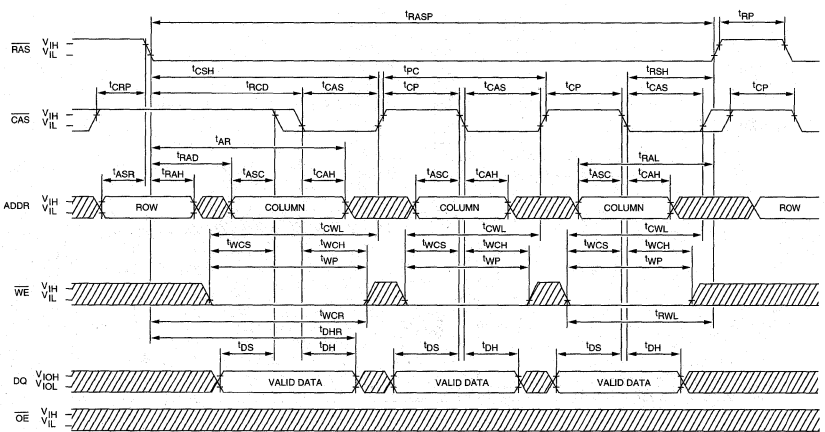
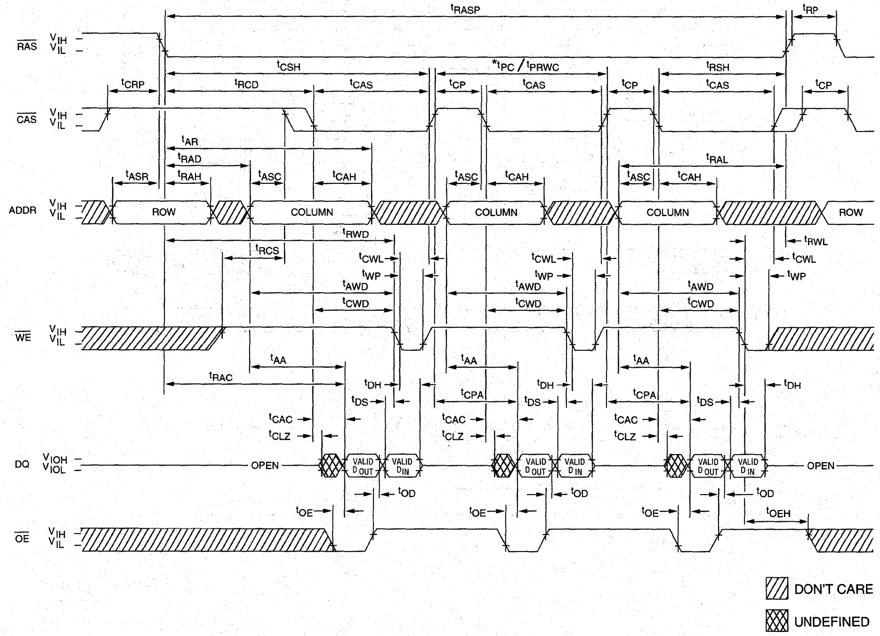
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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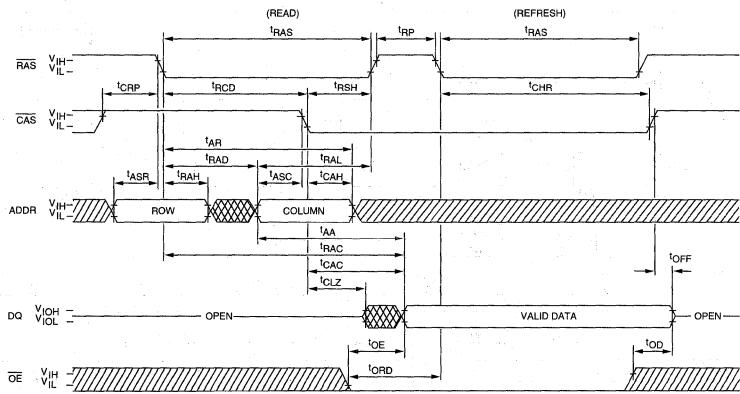
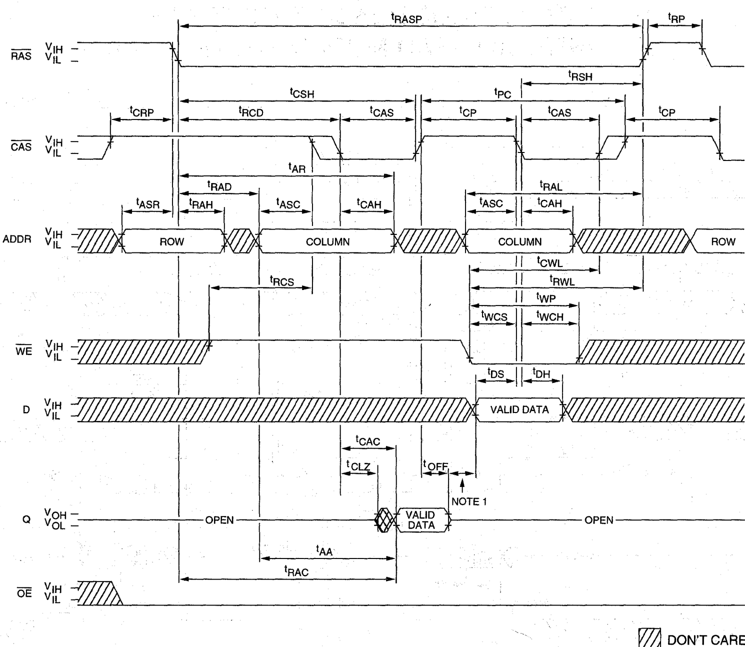
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to High-Z.

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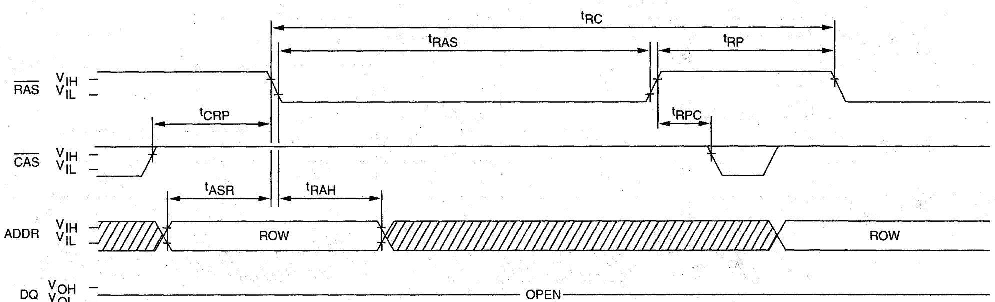
$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{OE}$ and $\overline{WE}$ = DON'T CARE)



FPM DRAM

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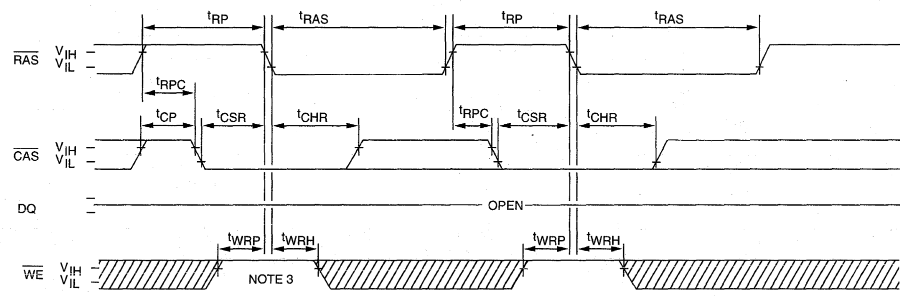
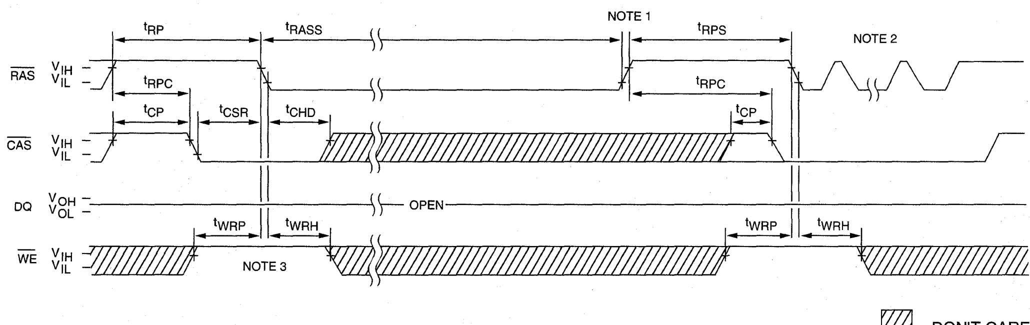
CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE:

1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a compete burst of all rows should be executed.
3. ^{t}WRP and ^{t}WRH are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.

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DRAM

8 MEG x 8 DRAM

3.3V, FAST PAGE MODE

FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x8 pinout, timing, functions and packages
- 13 row-addresses, 10 column-addresses (E1) or 12 row-addresses, 11 column-addresses (B6)
- High-performance CMOS silicon-gate process
- All inputs and outputs are LVTTL-compatible
- FAST PAGE MODE access
- 4,096-cycle CAS-BEFORE-RAS (CBR) REFRESH distributed across 64ms

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
50ns access	-5
60ns access	-6
70ns access	-7
• Packages	
Plastic SOJ (500 mil)	DW
Plastic TSOP (500 mil)	TW

- Part Number Example: MT4LC8M8E1DW-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns
-7	130ns	70ns	40ns	35ns	20ns

PIN ASSIGNMENT (Top View)

34-Pin SOJ (DA-6)

Pin	Name	Pin	Name
1	Vcc	34	Vss
2	DQ1	33	DQ8
3	DQ2	32	DQ7
4	DQ3	31	DQ6
5	DQ4	30	DQ5
6	NC	29	VSS
7	Vcc	28	CAS
8	WE	27	OE
9	RAS	26	NC
10	NC	25	A12/NC
11	A0	24	A11
12	A1	23	A10
13	A2	22	A9
14	A3	21	A8
15	A4	20	A7
16	A5	19	A6
17	Vcc	18	Vss

34-Pin TSOP*

Pin	Name	Pin	Name
1	Vcc	34	Vss
2	DQ1	33	DQ8
3	DQ2	32	DQ7
4	DQ3	31	DQ6
5	DQ4	30	DQ5
6	NC	29	Vss
7	Vcc	28	CAS
8	WE	27	OE
9	RAS	26	NC
10	NC	25	A12/NC
11	A0	24	A11
12	A1	23	A10
13	A2	22	A9
14	A3	21	A8
15	A4	20	A7
16	A5	19	A6
17	Vcc	18	Vss

*Consult factory for dimensions and availability.

GENERAL DESCRIPTION

The MT4LC8M8E1 and MT4LC8M8B6 are high-speed CMOS dynamic random access memory devices containing 67,108,864 bits, and designed to operate from 3.0V to 3.6V. The MT4LC8M8E1 and MT4LC8M8B6 are functionally organized as 8,388,608 locations containing 8 bits each. The 8,388,608 memory locations are arranged in 8,192 rows by 1,024 columns for the MT4LC8M8E1 or 4,096 rows by 2,048 columns for the MT4LC8M8B6. During READ or WRITE cycles, each location is uniquely addressed via the address bits. First, the row address is latched by the RAS signal, then the column address by CAS. Both devices provide FAST PAGE MODE operation, allowing for fast successive data operations (READ, WRITE or READ-MODIFY-WRITE) within a given row.

The MT4LC8M8E1 and MT4LC8M8B6 must be refreshed periodically in order to retain stored data.

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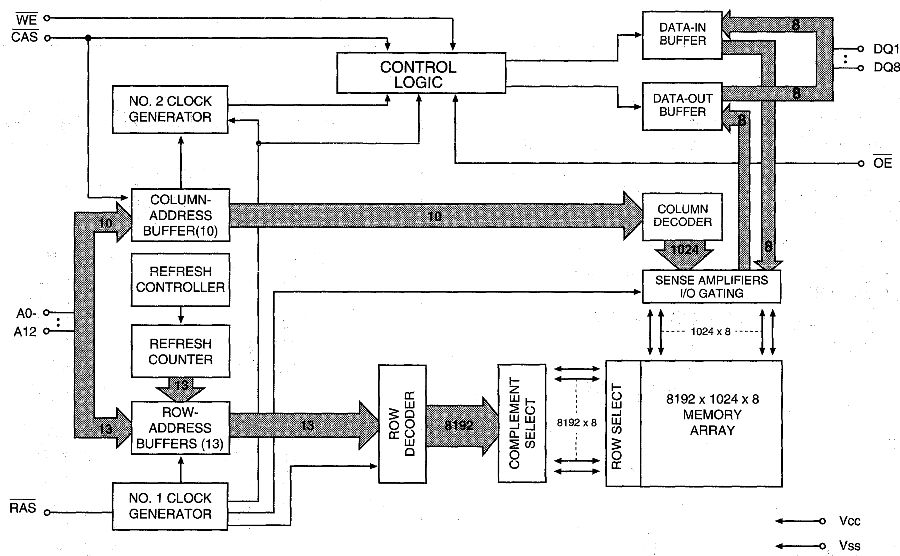
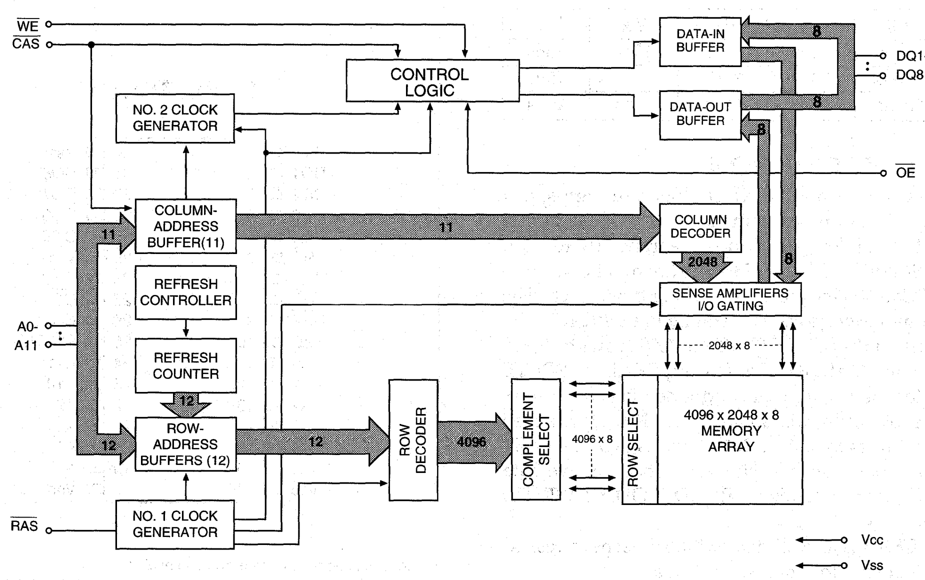
NEW FPM DRAM

FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8E1 (13 row-addresses)



FUNCTIONAL BLOCK DIAGRAM
MT4LC8M8B6 (12 row-addresses)



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FUNCTIONAL DESCRIPTION

The functional description for the MT4LC8M8E1 and MT4LC8M8B6 is divided into the two areas described below (DRAM access and DRAM refresh). Relevant timing diagrams are included in this data sheet, following the timing specification tables.

DRAM ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the eight I/O pins (DQ1-8). The WE signal must be activated to execute a write operation, otherwise a read operation will be performed. The OE signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST PAGE MODE operations are always initiated with a row-address strobed-in by the RAS signal, followed by a column-address strobed-in by CAS, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page-mode cycle time. This is accomplished by cycling CAS while holding RAS LOW, and entering new column addresses with each CAS cycle. Returning RAS HIGH terminates the FAST PAGE MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (E1) or all 4,096 rows (B6) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC8M8E1 internally refreshes two rows for every CBR cycle, whereas the MT4LC8M8B6 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. Alternatively, RAS-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time, so for the MT4LC8M8E1, 8,192 RAS-ONLY REFRESH cycles must be executed every 64ms to cover all rows.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss .... -1.0V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1.0V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 3.6V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX -5	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	MT4LC8M8E1	ICC1	1	1	1	mA	
	MT4LC8M8B6	ICC1	1	1	1		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ ≥ Vcc -0.2V, DQs may be left open, Other inputs: VIN ≥ Vcc -0.2V or VIN ≤ 0.2V)	MT4LC8M8E1	ICC2	500	500	500	µA	
	MT4LC8M8B6	ICC2	500	500	500		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	MT4LC8M8E1	ICC3	135	125	115	mA	3, 4, 29
	MT4LC8M8B6	ICC3	175	165	155		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN])	MT4LC8M8E1	ICC4	105	95	85	mA	3, 4, 29
	MT4LC8M8B6	ICC4	105	95	85		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: tRC = tRC [MIN])	MT4LC8M8E1	ICC5	135	125	115	mA	3, 26
	MT4LC8M8B6	ICC5	175	165	155		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	MT4LC8M8E1	ICC6	145	135	125	mA	3, 5
	MT4LC8M8B6	ICC6	175	165	155		

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		25		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	40		45		55		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^{t}AWD	48		55		65		ns	21
Access time from $\overline{CAS}$	^{t}CAC		13		15		20	ns	15
Column-address hold time	^{t}CAH	8		10		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	13	10,000	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		0		ns	
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^{t}CP	8		10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		30		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		5		ns	
$\overline{CAS}$ hold time	^{t}CSH	50		60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		5		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	36		40		50		ns	21
Write command to $\overline{CAS}$ lead time	^{t}CWL	13		15		20		ns	
Data-in hold time	^{t}DH	8		10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	40		45		55		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22
Output disable	^{t}OD	0	13	0	15	0	20	ns	27, 28
Output Enable time	^{t}OE		13		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	13		15		20		ns	28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^{t}OFF	0	13	0	15	0	20	ns	20, 27
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	30		35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	76		85		100		ns	
Access time from $\overline{RAS}$	^{t}RAC		50		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	13	25	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	8		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	25		30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	50	125,000	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	^{t}RC	90		110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	18	37	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	19
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period	^{t}REF		64		64		64	ms	26
$\overline{RAS}$ precharge time	^{t}RP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	13		15		20		ns	
READ WRITE cycle time	^{t}RWC	131		155		185		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	73		85		100		ns	21
Write command to $\overline{RAS}$ lead time	^{t}RWL	13		15		20		ns	
Transition time (rise or fall)	^{t}T	1	50	1	50	1	50	ns	
Write command hold time	^{t}WCH	8		10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	40		45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21
Write command pulse width	^{t}WP	8		10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	25

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates, 100pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to VOH or VOL.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. If ^{t}WCS > ^{t}WCS MIN, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. ^{t}RWD, ^{t}AWD and ^{t}CWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. The values shown were calculated for reference allowing 10ns for the external latching of read data and application of write data. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
26. RAS-ONLY REFRESH requires that all 8,192 rows of the MT4LC8M8E1, or all 4,096 rows of the MT4LC8M8B6, be refreshed at least once every 64ms. CBR REFRESH, for either device, requires that at least 4,096 cycles be completed every 64ms.
27. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If CAS goes HIGH before OE, the DQs will open regardless of the state of OE. If CAS stays LOW while OE is brought HIGH, the DQs will open. If OE is brought back LOW (CAS still LOW), the DQs will provide the previously read data.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE is taken back LOW while CAS remains LOW, the DQs will remain open.
30. Column-address changed once each cycle.

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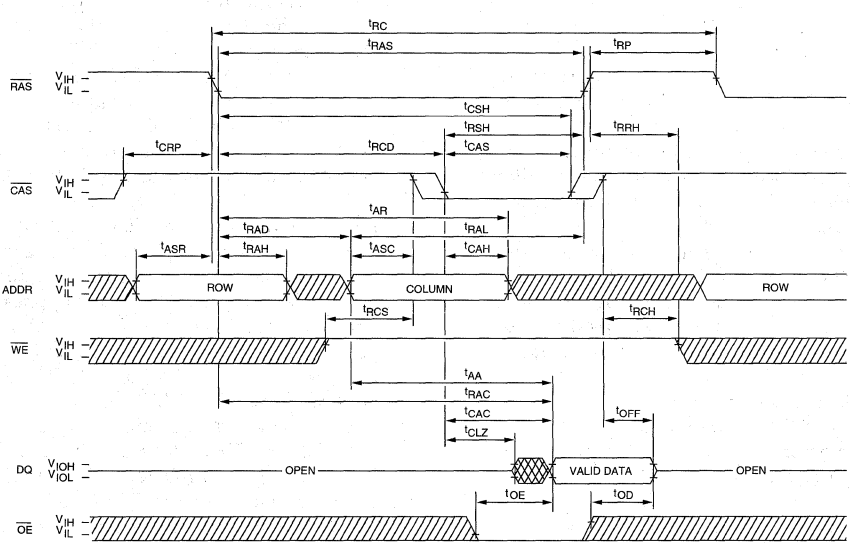
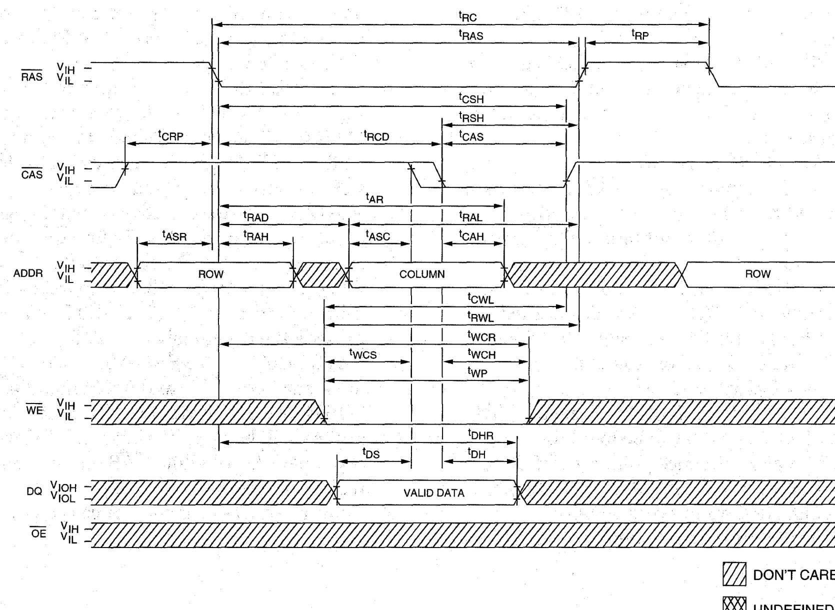
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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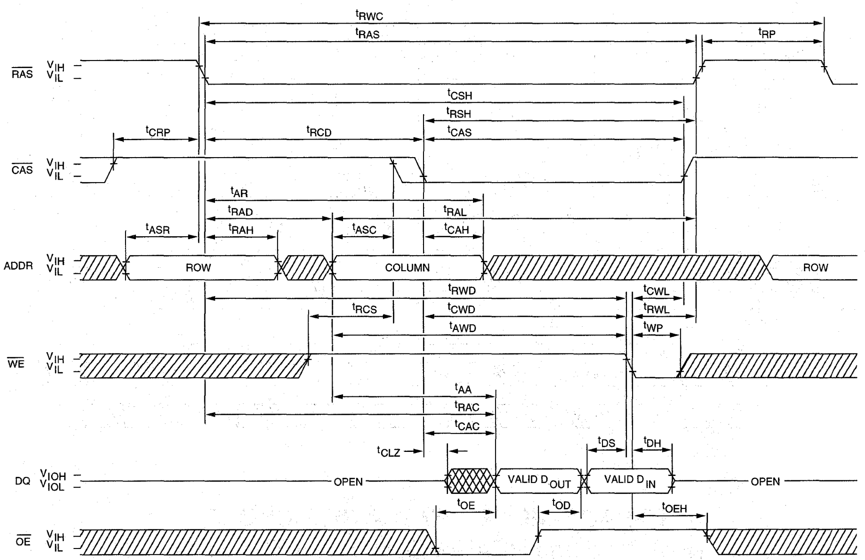
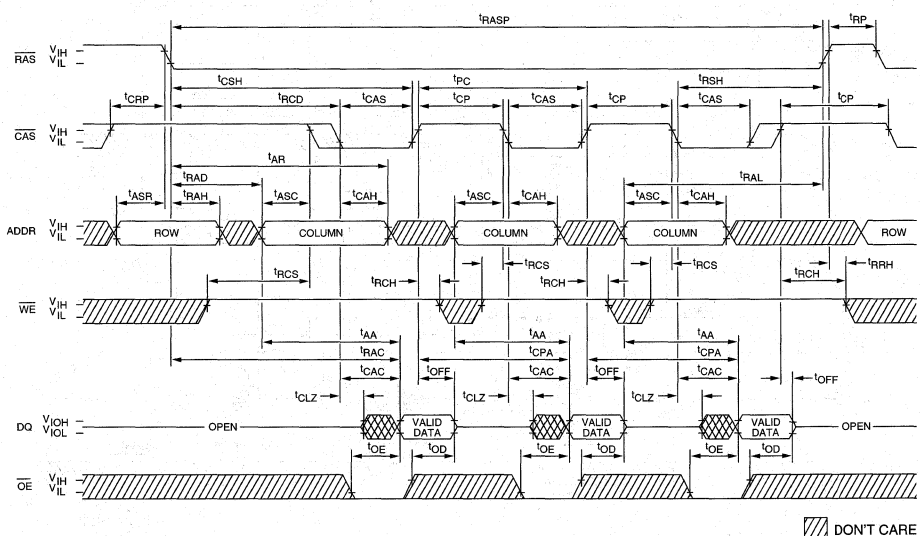
NEW FPM DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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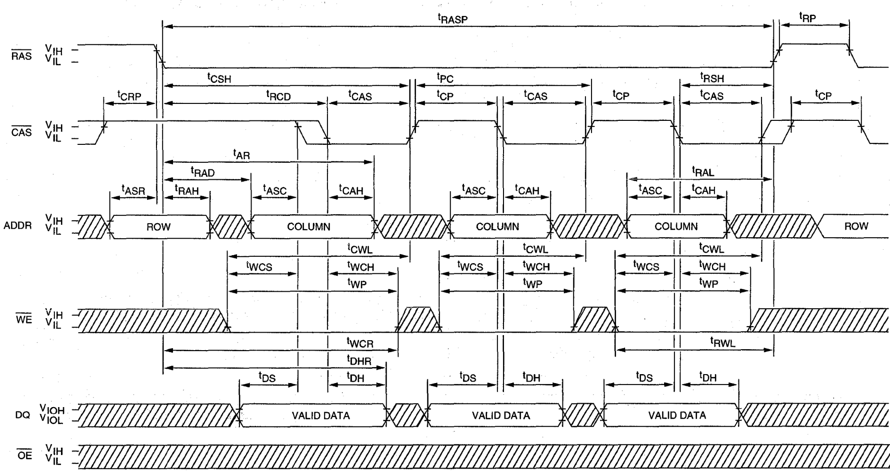
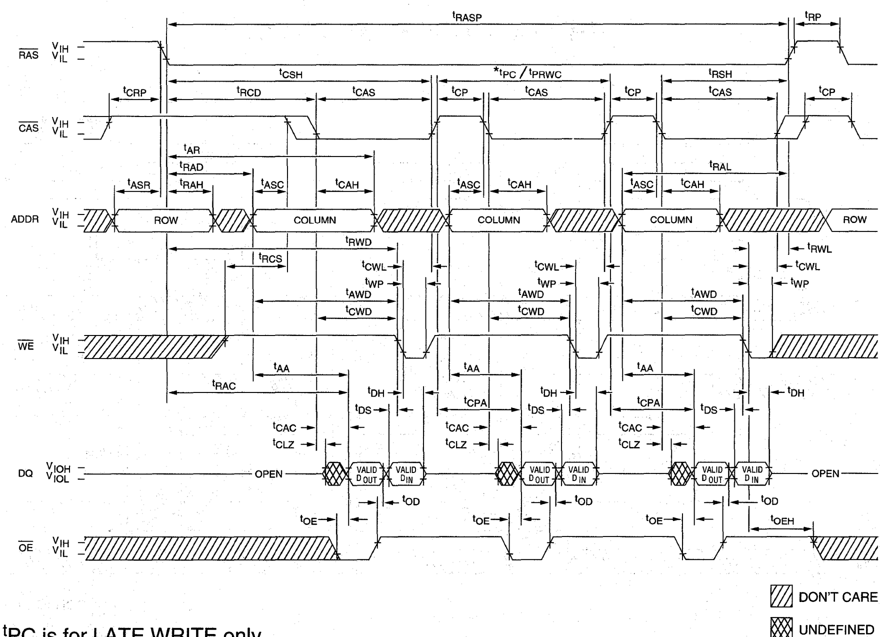
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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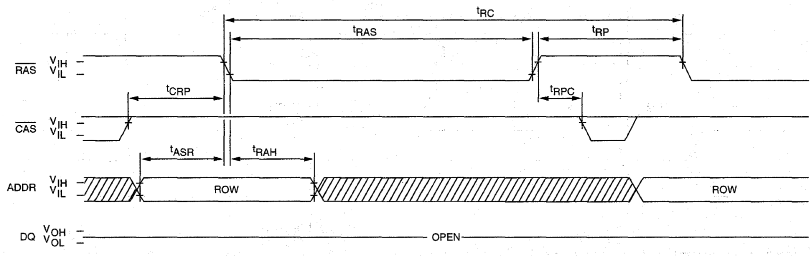
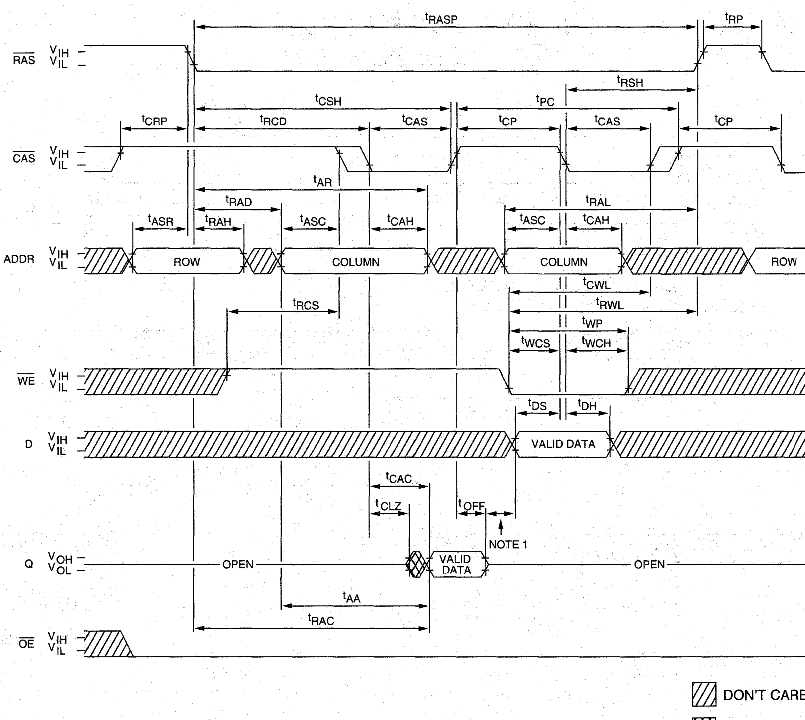
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive input data prior to output data going High-Z.

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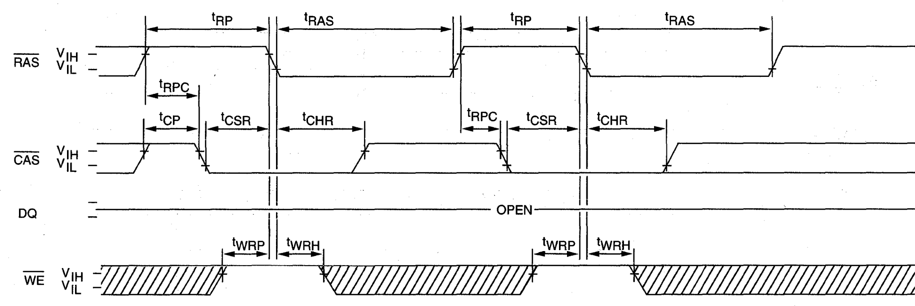
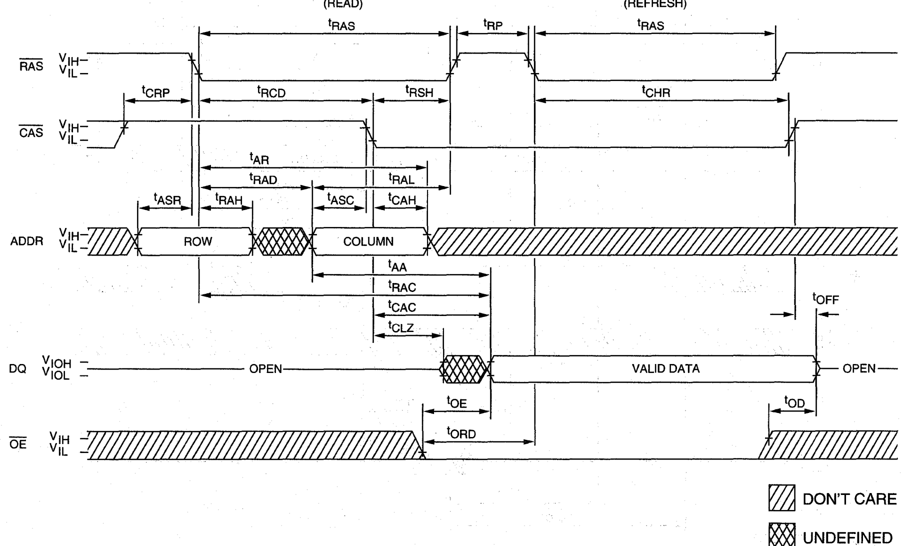
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



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DRAM

256K x 16 DRAM

5V, FAST PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 375mW active, typical
- All device pins are fully TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4C16257DJ-7

*60ns specifications are limited to a Vcc range of ±5%.

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	20ns	60ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DA-7)

Pin	Name	Pin	Name
1	Vcc	40	Vss
2	DQ1	39	DQ16
3	DQ2	38	DQ15
4	DQ3	37	DQ14
5	DQ4	36	DQ13
6	Vcc	35	Vss
7	DQ5	34	DQ12
8	DQ6	33	DQ11
9	DQ7	32	DQ10
10	DQ8	31	DQ9
11	NC	30	NC
12	NC	29	$\overline{CASL}$
13	$\overline{WE}$	28	$\overline{CASH}$
14	$\overline{RAS}$	27	$\overline{OE}$
15	NC	26	A8
16	A0	25	A7
17	A1	24	A6
18	A2	23	A5
19	A3	22	A4
20	Vcc	21	Vss

40/44-Pin TSOP (DB-4)

Pin	Name	Pin	Name
1	Vcc	44	Vss
2	DQ1	43	DQ16
3	DQ2	42	DQ15
4	DQ3	41	DQ14
5	DQ4	40	DQ13
6	Vcc	39	Vss
7	DQ5	38	DQ12
8	DQ6	37	DQ11
9	DQ7	36	DQ10
10	DQ8	35	DQ9
13	NC	32	NC
14	NC	31	$\overline{CASL}$
15	$\overline{WE}$	30	$\overline{CASH}$
16	$\overline{RAS}$	29	$\overline{OE}$
17	NC	28	A8
18	A0	27	A7
19	A1	26	A6
20	A2	25	A5
21	A3	24	A4
22	Vcc	23	Vss

GENERAL DESCRIPTION

The MT4C16257 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16257 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins.

The MT4C16257 $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257.

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FUNCTIONAL BLOCK DIAGRAM

WE
CASL
CASH
CAS
DATA-IN BUFFER
UPPER BYTE (DQ9-DQ16)
LOWER BYTE (DQ1-DQ8)
DQ1
16
DQ16
NO. 2 CLOCK GENERATOR
COLUMN-ADDRESS BUFFER
9
COLUMN DECODER
DATA-OUT BUFFER
OE
A0
A1
A2
A3
A4
A5
A6
A7
A8
REFRESH CONTROLLER
SELF REFRESH OSCILLATOR and TIMER
512
8
8
16
SENSE AMPLIFIERS I/O GATING
REFRESH COUNTER
512 x 16
ROW-ADDRESS BUFFERS (9)
ROW DECODER
512
512 x 512 x 16 MEMORY ARRAY
RAS
NO. 1 CLOCK GENERATOR
Vcc
Vss

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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The MT4C16257 CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls give the MT4C16257 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4C16257 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles. Figure 2 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

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FPM DRAM

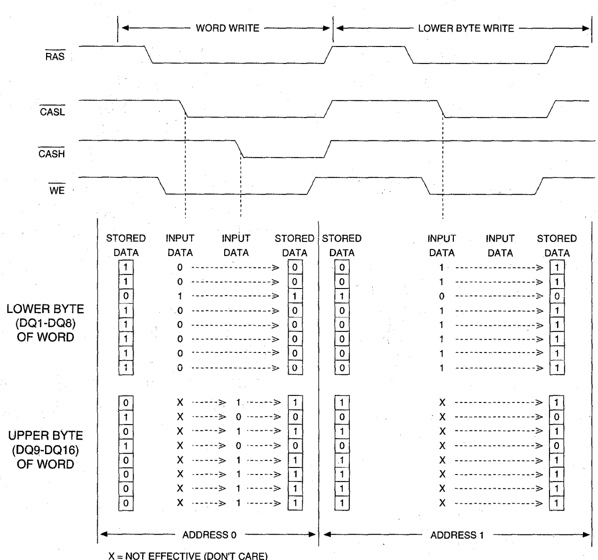

Figure 1
WORD AND BYTE WRITE EXAMPLE

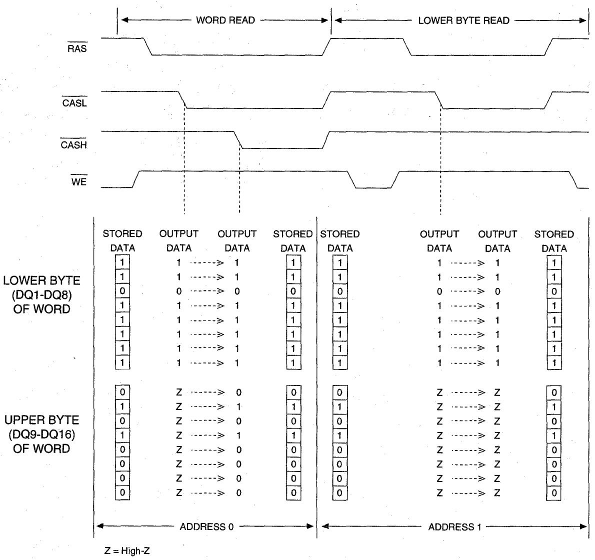

Figure 2
WORD AND BYTE READ EXAMPLE

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TRUTH TABLE

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES ᵗR	ADDRESSES ᵗC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active (CASL or CASH).

FPM DRAM

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ Vcc (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	195	175	160	mA	3, 4, 41
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 41
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	195	175	160	mA	3, 41
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	160	140	mA	3, 5

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ (SOJ, TSOP)	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35		40	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address setup time	^tASC	0		0		0		ns	29
Row-address setup time	^tASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 31
Column-address hold time	^tCAH	10		15		15		ns	29
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	20	10,000	ns	37
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 30
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	32
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	31
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	16, 34
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	30
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	30
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 29
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 29
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 30
Data-in hold time	^tDH	10		15		15		ns	22, 31
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Data-in setup time	^tDS	0		0		0		ns	22, 31
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 39
Output Enable time	^tOE		15		20		20	ns	31
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 31

*60ns specifications are limited to a V_{CC} range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	33
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		100		ns	33
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Row-address hold time	^tRAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26, 30
Read command setup time	^tRCS	0		0		0		ns	26, 29
Refresh period (512 cycles)	^tREF		8		8		8	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		10		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	38
READ WRITE cycle time	^tRWC	150		175		195		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		105		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	26
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Write command hold time	^tWCH	10		10		10		ns	26, 38
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	26
Write command setup time	^tWCS	0		0		0		ns	21, 26, 29
Write command pulse width	^tWP	10		10		10		ns	26

*60ns specifications are limited to a Vcc range of ±5%.

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.80 and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The 3ns minimum is a parameter guaranteed by design.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^{t}OEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.

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NOTES (continued)

29. The first $\overline{CAS}$x edge to transition LOW.
30. The last $\overline{CAS}$x edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
32. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
33. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
34. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
35. First DQs controlled by the first $\overline{CAS}$x to go LOW.
36. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
37. Each $\overline{CAS}$x must meet minimum pulse width.
38. Last $\overline{CAS}$x to go LOW.
39. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
40. Column-address changed once each cycle.

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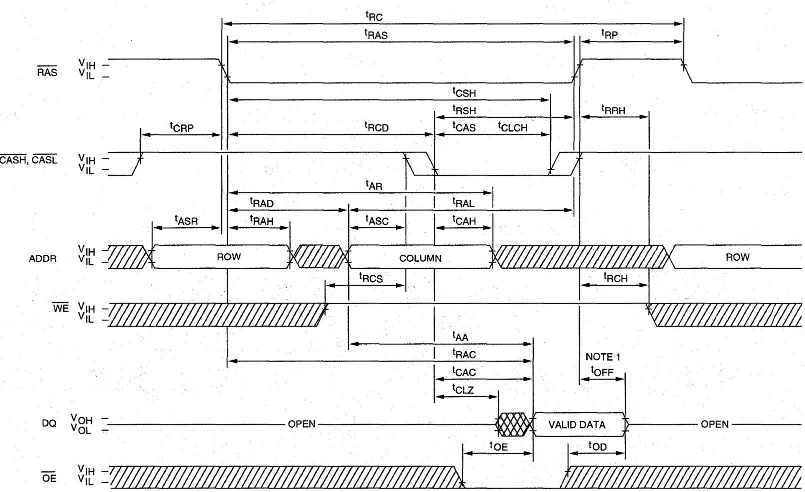
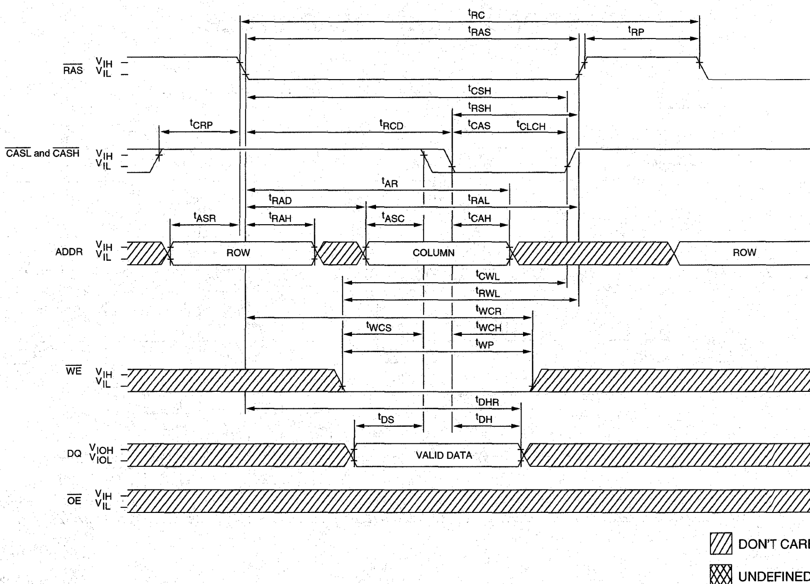
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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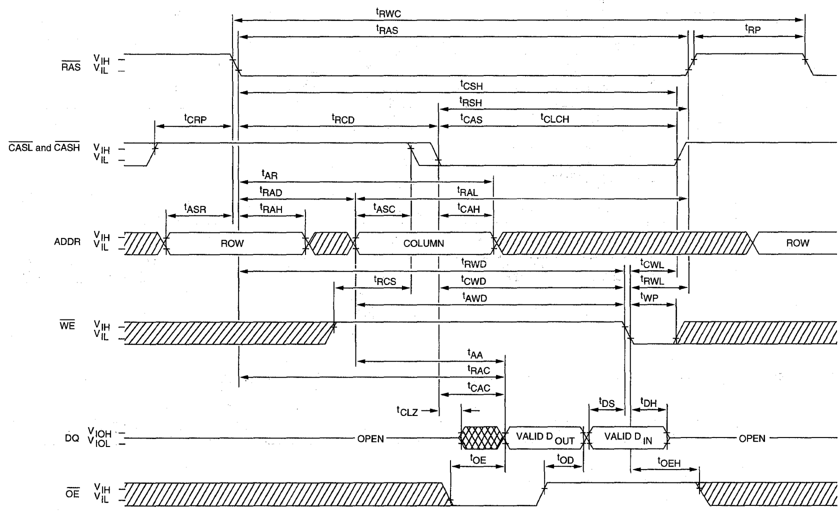
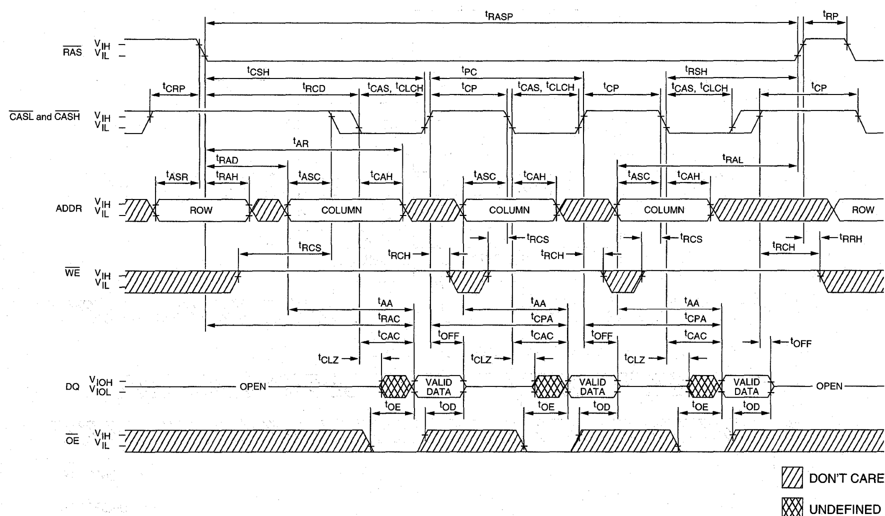
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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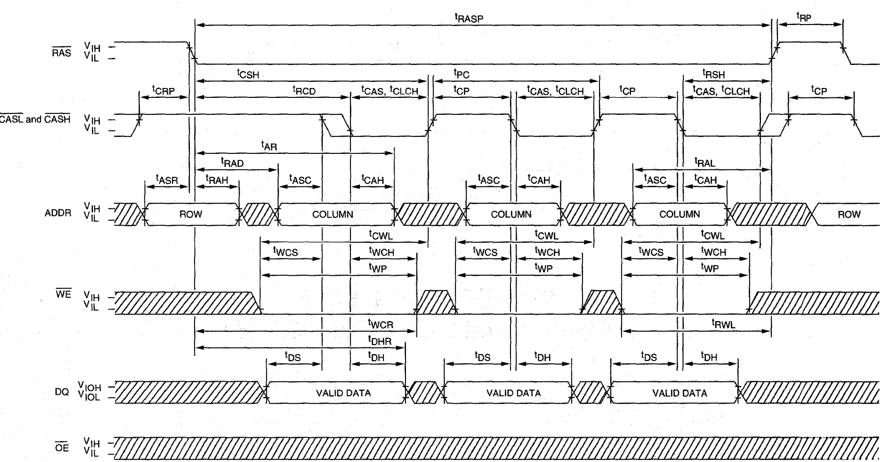
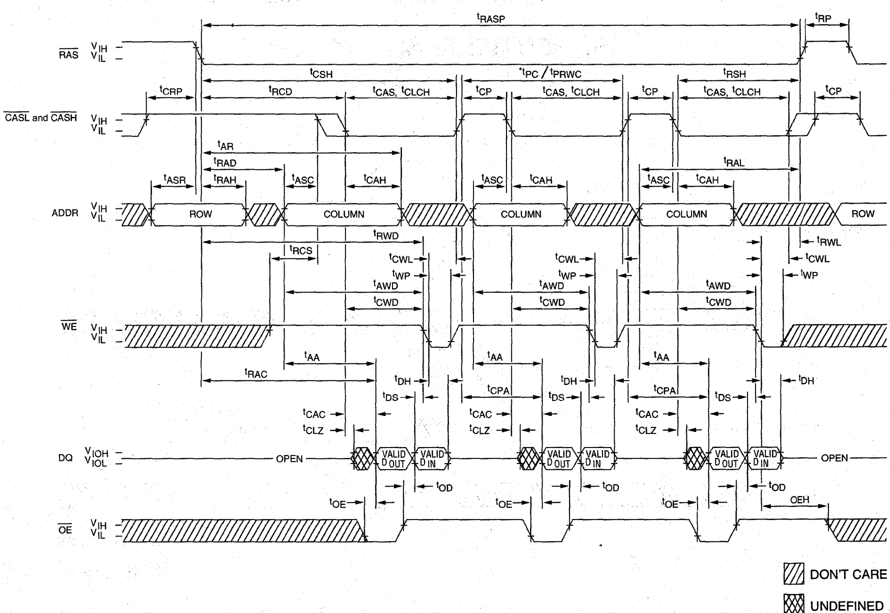
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** ^tPC is for LATE WRITE only.

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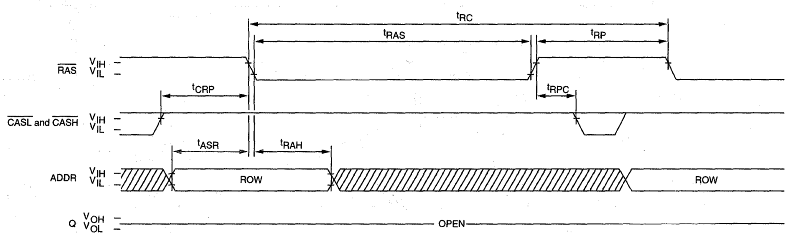
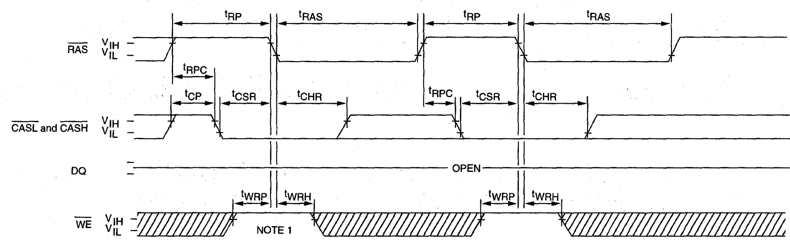
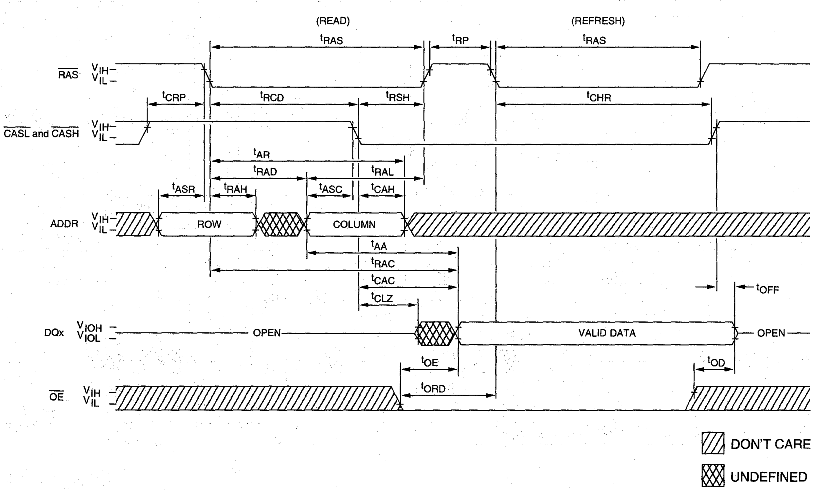
RAS-ONLY REFRESH CYCLE
(Addresses; OE, WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



HIDDEN REFRESH CYCLE 24
(WE = HIGH; OE = LOW)



NOTE: 1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.

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DRAM

256K x 16 DRAM

3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply*
- Low power, 0.3mW standby; 150mW active, typical
- All device pins are fully LVTTL-compatible
- 512-cycle refresh in 8ms (MT4LC16257) or 64ms (MT4LC16257 S)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN and optional Extended and SELF
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle
- Symmetrical addressing (nine rows, nine columns)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Refresh Rate	
512-cycle refresh in 8ms	None
512-cycle refresh in 64ms, SELF REFRESH	S
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC16257DJ-7 S

*60ns specifications are limited to a Vcc range of ±0.15V.

KEY TIMING PARAMETERS

SPEED	ᵗRC	ᵗRAC	ᵗPC	ᵗAA	ᵗCAC	ᵗRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	20ns	60ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ (DA-7)

Pin	Name	Pin	Name
1	Vcc	40	Vss
2	DQ1	39	DQ16
3	DQ2	38	DQ15
4	DQ3	37	DQ14
5	DQ4	36	DQ13
6	Vcc	35	Vss
7	DQ5	34	DQ12
8	DQ6	33	DQ11
9	DQ7	32	DQ10
10	DQ8	31	DQ9
11	NC	30	NC
12	NC	29	$\overline{\text{CASL}}$
13	$\overline{\text{WE}}$	28	$\overline{\text{CASH}}$
14	$\overline{\text{RAS}}$	27	$\overline{\text{OE}}$
15	NC	26	A8
16	A0	25	A7
17	A1	24	A6
18	A2	23	A5
19	A3	22	A4
20	Vcc	21	Vss

40/44-Pin TSOP (DB-4)

Pin	Name	Pin	Name
1	Vcc	44	Vss
2	DQ1	43	DQ16
3	DQ2	42	DQ15
4	DQ3	41	DQ14
5	DQ4	40	DQ13
6	Vcc	39	Vss
7	DQ5	38	DQ12
8	DQ6	37	DQ11
9	DQ7	36	DQ10
10	DQ8	35	DQ9
13	NC	32	NC
14	NC	31	$\overline{\text{CASL}}$
15	$\overline{\text{WE}}$	30	$\overline{\text{CASH}}$
16	$\overline{\text{RAS}}$	29	$\overline{\text{OE}}$
17	NC	28	A8
18	A0	27	A7
19	A1	26	A6
20	A2	25	A5
21	A3	24	A4
22	Vcc	23	Vss

GENERAL DESCRIPTION

The MT4LC16257(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4LC16257(S) has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ function in an identical manner to $\overline{\text{CAS}}$ in that either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ will generate an internal $\overline{\text{CAS}}$.

The MT4LC16257(S) $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner during READ cycles for the MT4LC16257(S).

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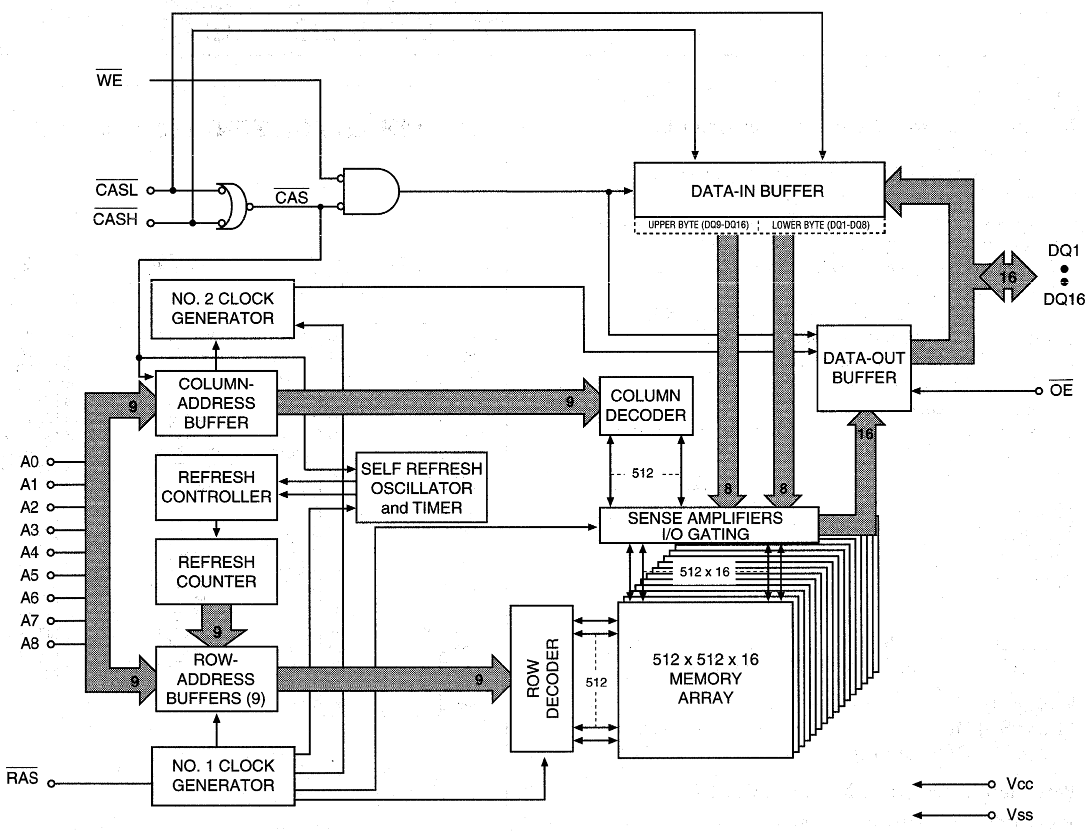
FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits.

The CAS control also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is each CAS controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16.

The CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The two CAS controls provide BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by OE.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

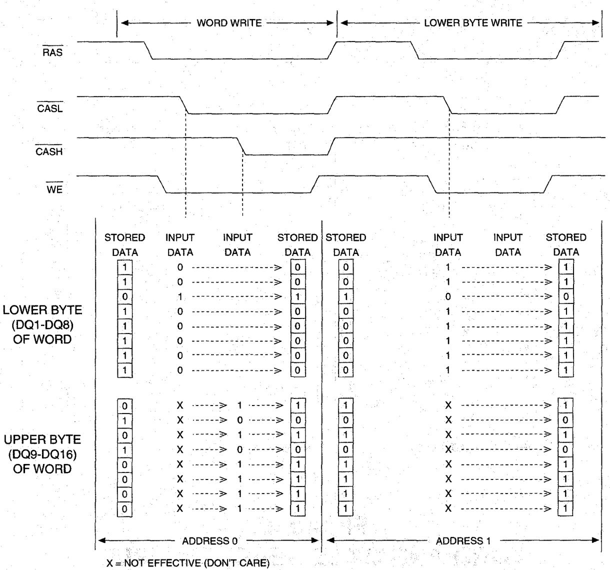

Figure 1
WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4LC16257(S) can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the MT4LC16257(S) BYTE WRITE and WORD WRITE cycles.

The MT4LC16257(S) also has BYTE READ and WORD READ cycles, since it uses two CAS inputs to control its byte accesses. Figure 2 illustrates the MT4LC16257(S) BYTE READ and WORD READ cycles.

REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ${}^{t}RASS$. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ${}^{t}RPS$ ($\approx {}^{t}RC$). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

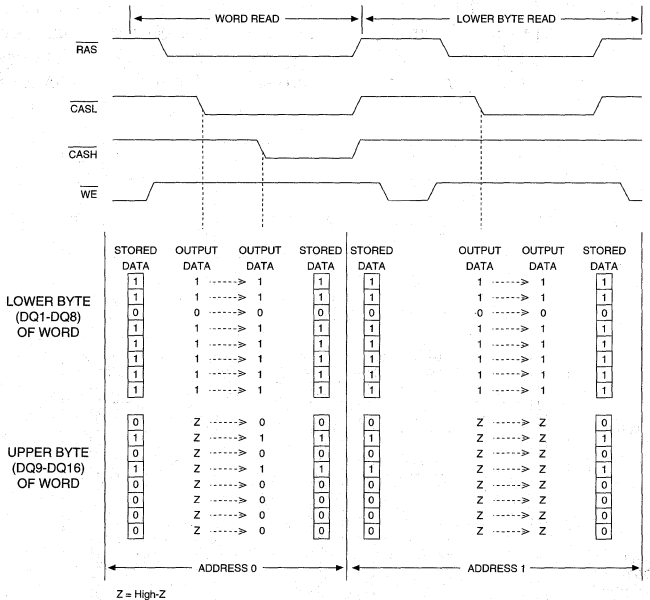

Figure 2
WORD AND BYTE READ EXAMPLE

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TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQs	NOTES
							^{t}R	^{t}C		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
READ	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
WRITE	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4
SELF REFRESH (MT4C16257 S only)		H→L	L	X	X	X	X	X	High-Z	

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$).

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FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = +3.3V ±0.3V**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc**	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

**60ns specifications are limited to a Vcc range of ±0.15V.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V**)

PARAMETER/CONDITION	SYMBOL	MAX -6**	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	1	1	1	mA
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	500	500	500	µA	25
	I_{CC2} (S only)	100	100	100	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	100	mA	3, 4, 40
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	70	60	50	mA	3, 4, 40
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	100	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	120	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current, $\overline{CAS}$ = 0.2V or CBR cycling; ^tRAS = ^tRAS (MIN); $\overline{WE}$, A0-A8 and D_{IN} = Vcc-0.2V or 0.2V (D_{IN} may be left open)	I_{CC7} (S only)	150	150	150	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current, CBR cycling with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A8 and D_{IN} = Vcc-0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	150	150	150	µA	5, 41

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ (SOJ, TSOP)	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35		40	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		60		ns	
Column-address setup time	^tASC	0		0		0		ns	29
Row-address setup time	^tASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		65		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	15, 31
Column-address hold time	^tCAH	10		15		15		ns	29
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	20	10,000	ns	37
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	10		10		10		ns	41
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		10		ns	5, 30
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ returning HIGH	^tCLCH	10		10		10		ns	32
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	31
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	16, 34
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	8		10		10		ns	30
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	30
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		10		ns	5, 29
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		45		ns	21, 29
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	26, 30
Data-in hold time	^tDH	10		15		15		ns	22, 31
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Data-in setup time	^tDS	0		0		0		ns	22, 31
Output disable time	^tOD	3	15	3	15	3	15	ns	28, 39
Output Enable time	^tOE		15		20		20	ns	31
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		20		ns	27
Output buffer turn-off delay	^tOFF	3	15	3	15	3	15	ns	20, 28, 31
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	

*60ns specifications are limited to a V_{CC} range of ±0.15V.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	33
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		100		ns	33
Access time from RAS	tRAC		60		70		80	ns	14
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Row-address hold time	tRAH	10		10		10		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width entering SELF REFRESH	tRASS	100		100		100		µs	41
Random READ or WRITE cycle time	tRC	110		130		150		ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26, 30
Read command setup time	tRCS	0		0		0		ns	26, 29
Refresh period (512 cycles) MT4LC16257 / MT4LC16257 S	tREF		8/64		8/64		8/64	ms	
RAS precharge time	tRP	40		50		60		ns	
RAS to CAS precharge time	tRPC	10		10		10		ns	
RAS precharge time exiting SELF REFRESH	tRPS	110		130		150		µs	41
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
RAS hold time	tRSH	15		20		20		ns	38
READ WRITE cycle time	tRWC	150		175		195		ns	
RAS to WE delay time	tRWD	85		95		105		ns	21
Write command to RAS lead time	tRWL	15		20		20		ns	26
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	
Write command hold time	tWCH	10		10		10		ns	26, 38
Write command hold time (referenced to RAS)	tWCR	45		55		60		ns	26
Write command setup time	tWCS	0		0		0		ns	21, 26, 29
Write command pulse width	tWP	10		10		10		ns	26

*60ns specifications are limited to a Vcc range of ±0.15V.

FPM DRAM

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FPM DRAM

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gates and 50pF, V_{OL} = 0.80 and V_{OH} = 2.0V.
14. Assumes that $^tRCD < {^tRCD}$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {^tRCD}$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The 3ns minimum is a parameter guaranteed by design.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {^tWCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {^tRWD}$ (MIN), $^tAWD \geq {^tAWD}$ (MIN) and $^tCWD \geq {^tCWD}$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW on the MT4LC16257(S).
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of the $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
29. The first $\overline{CAS}$x edge to transition LOW.
30. The last $\overline{CAS}$x edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input, DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.

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NOTES (continued)

32. Last falling CASx edge to first rising CASx edge.
33. Last rising CASx edge to next cycle's last rising CASx edge.
34. Last rising CASx edge to first falling CASx edge.
35. First DQs controlled by the first CASx to go LOW.
36. Last DQs controlled by the last CASx to go HIGH.
37. Each CASx must meet minimum pulse width.
38. Last CASx to go LOW.
39. All DQs controlled, regardless of CASL and CASH.
40. Column-address changed once while RAS = V_{IL} and CAS = V_{IH}.
41. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.

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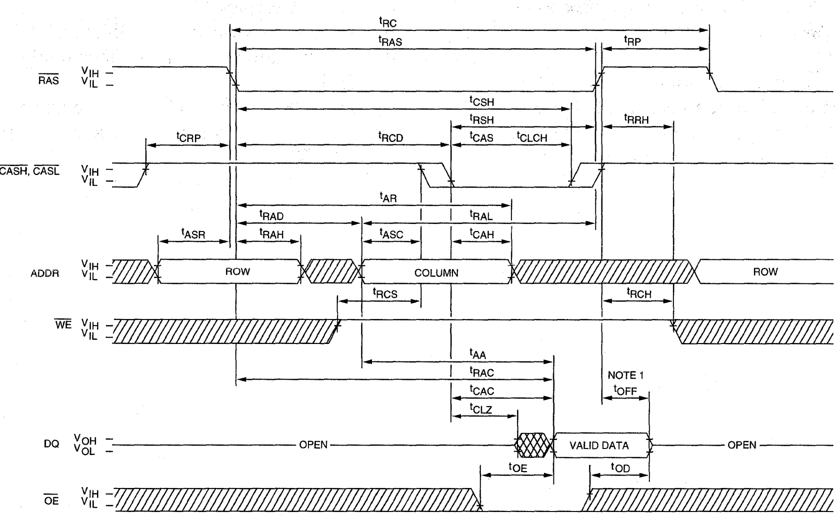
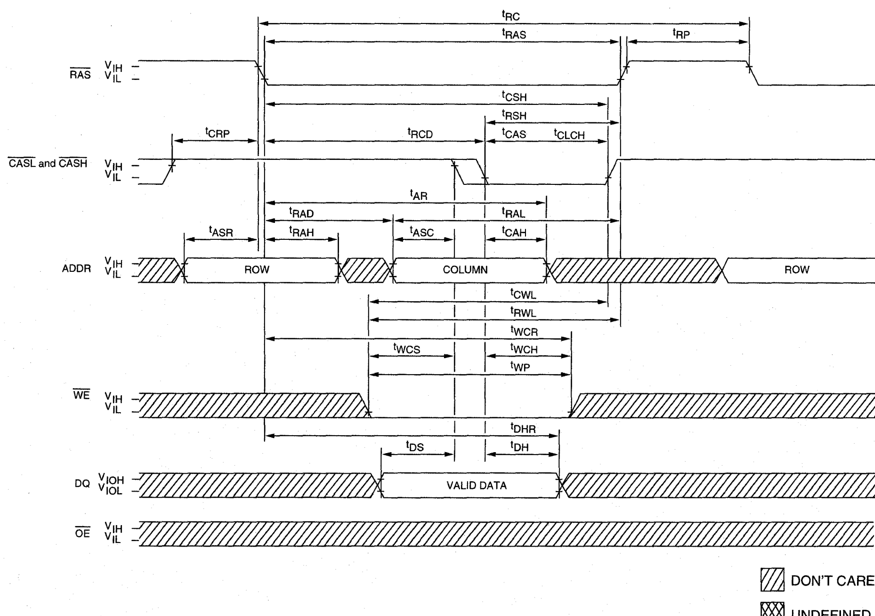
FPM DRAM

READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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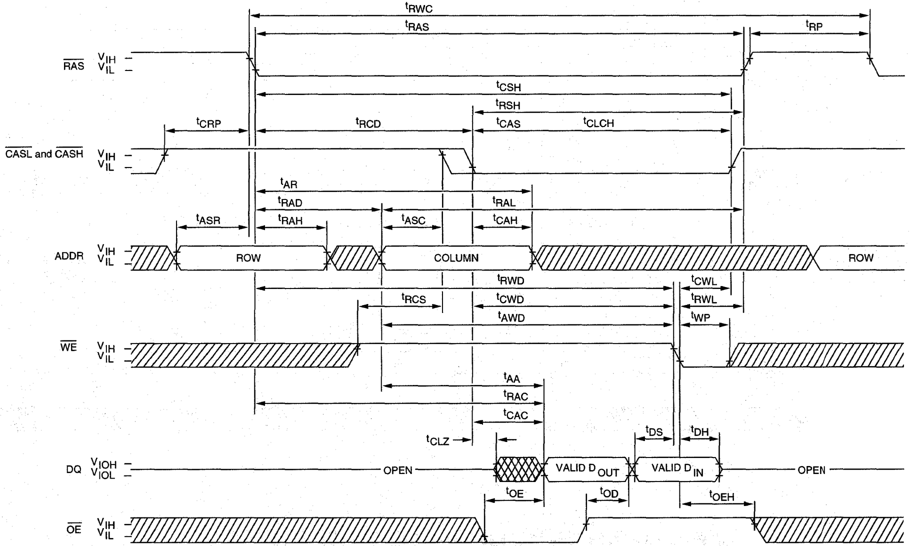
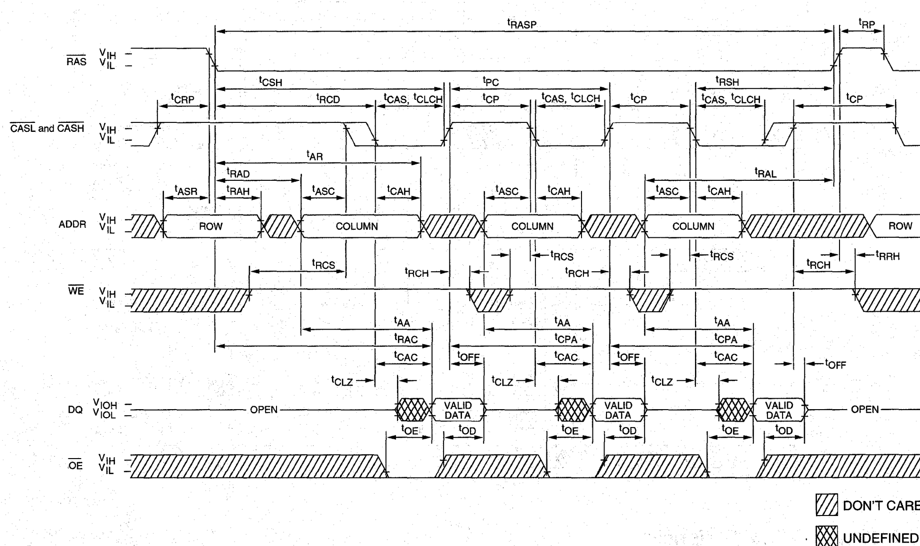
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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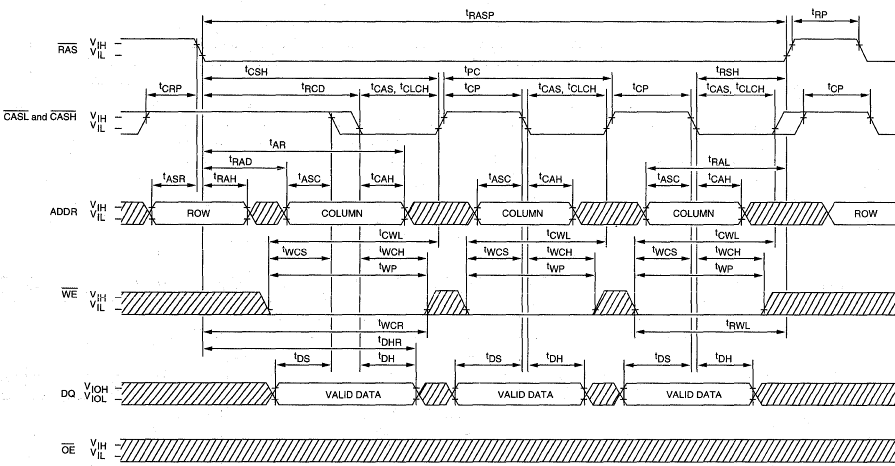
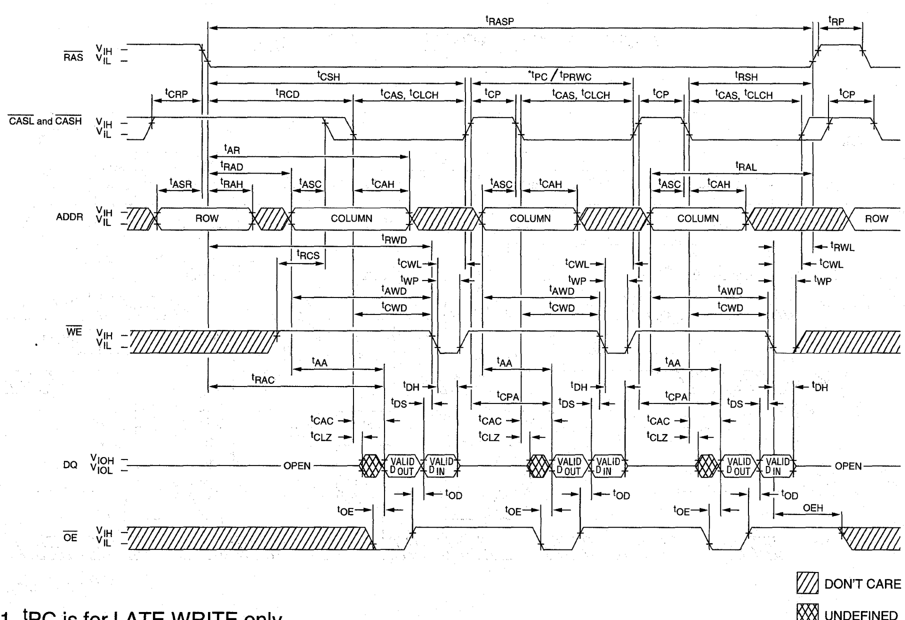
FPM DRAM

FAST-PAGE-MODE EARLY WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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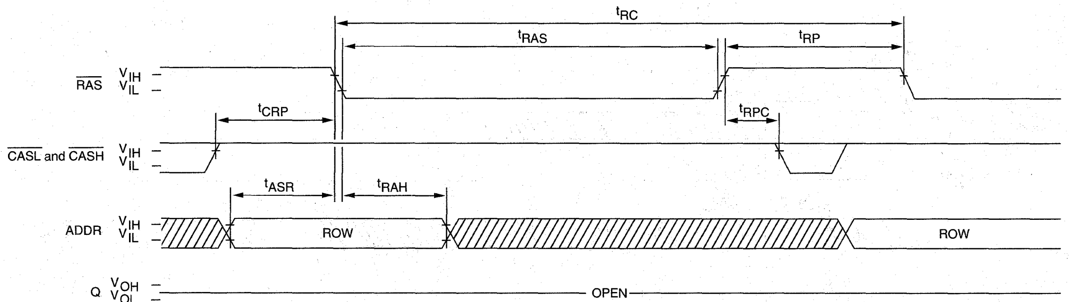
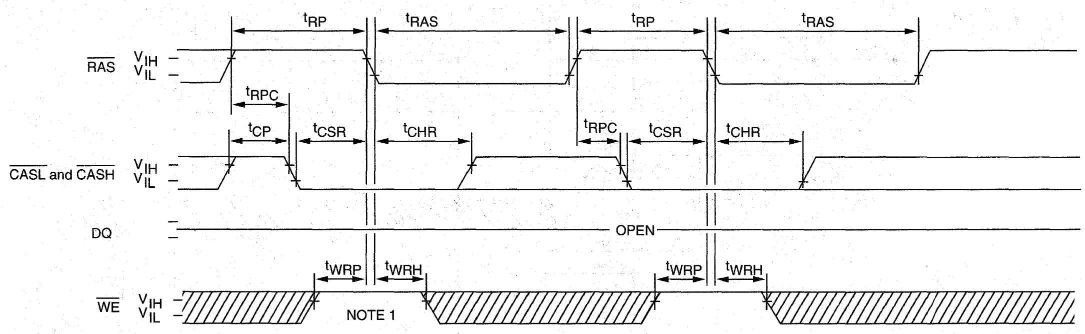
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.

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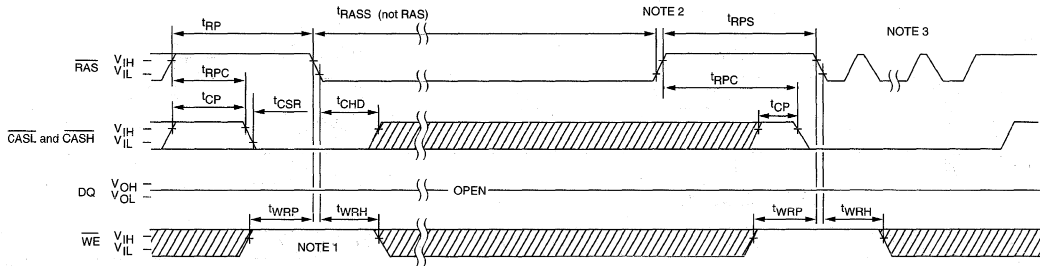
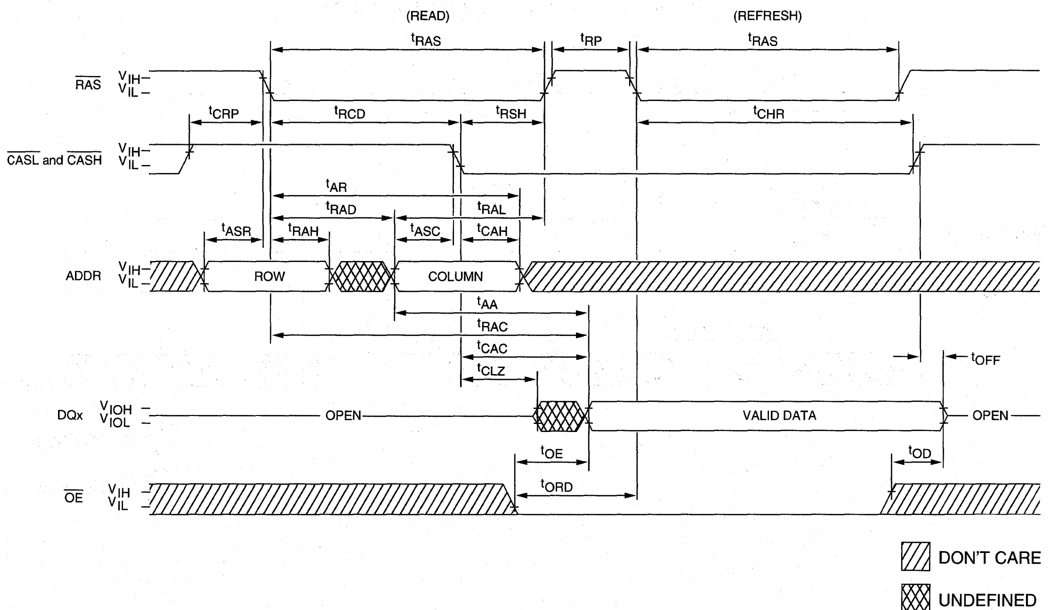
FPM DRAM

SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE 24
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE:
1. ${}^tWRP$ and ${}^tWRH$ are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at $\overline{RAS}$ time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at $\overline{RAS}$ time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{WE}$ HIGH at $\overline{RAS}$ time during a CBR REFRESH.
2. Once ${}^tRASS$ (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
3. Once ${}^tRPS$ is satisfied, a compete burst of all rows should be executed.

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DRAM

1 MEG x 16 DRAM

5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 1mW standby; 350mW active, typical

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Refresh Rate
  - Standard 16ms period — None
- Packages
  - Plastic SOJ (400 mil) — DJ
- Part Number Example: MT4C1M16C3DJ-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

42-Pin SOJ (DA-8)

Signal	Pin	Pin	Signal
Vcc	1	42	Vss
DQ1	2	41	DQ16
DQ2	3	40	DQ15
DQ3	4	39	DQ14
DQ4	5	38	DQ13
Vcc	6	37	Vss
DQ5	7	36	DQ12
DQ6	8	35	DQ11
DQ7	9	34	DQ10
DQ8	10	33	DQ9
NC	11	32	NC
NC	12	31	CASL
WE	13	30	CASH
RAS	14	29	OE
NC	15	28	A9
NC	16	27	A8
A0	17	26	A7
A1	18	25	A6
A2	19	24	A5
A3	20	23	A4
Vcc	21	22	Vss

GENERAL DESCRIPTION

The MT4C1M16C3 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4C1M16C3 has both BYTE WRITE and WORD WRITE access cycles via two CAS pins (CASL and CASH). These function in an identical manner to a single CAS of other DRAMs in that either CASL or CASH will generate an internal CAS.

The MT4C1M16C3 CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and the last CAS to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. The CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The CAS function also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4C1M16C3 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain

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GENERAL DESCRIPTION (continued)

open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

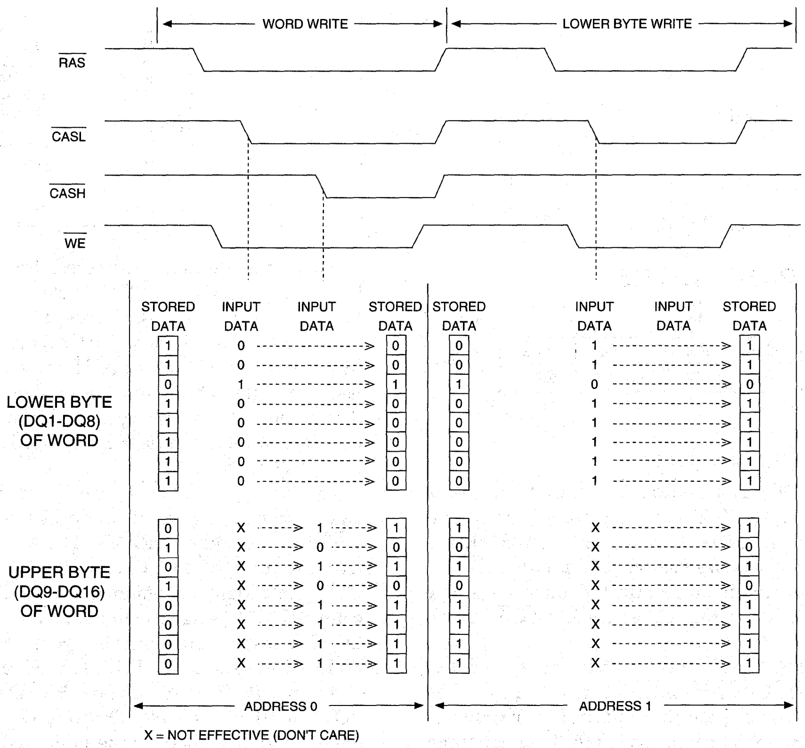

Figure 1
WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{CASL}$ will select a lower BYTE access (DQ1-DQ8). Enabling $\overline{CASH}$ will select an upper BYTE access (DQ9-DQ16). Enabling both $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C1M16C3 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the $\overline{CAS}$ inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

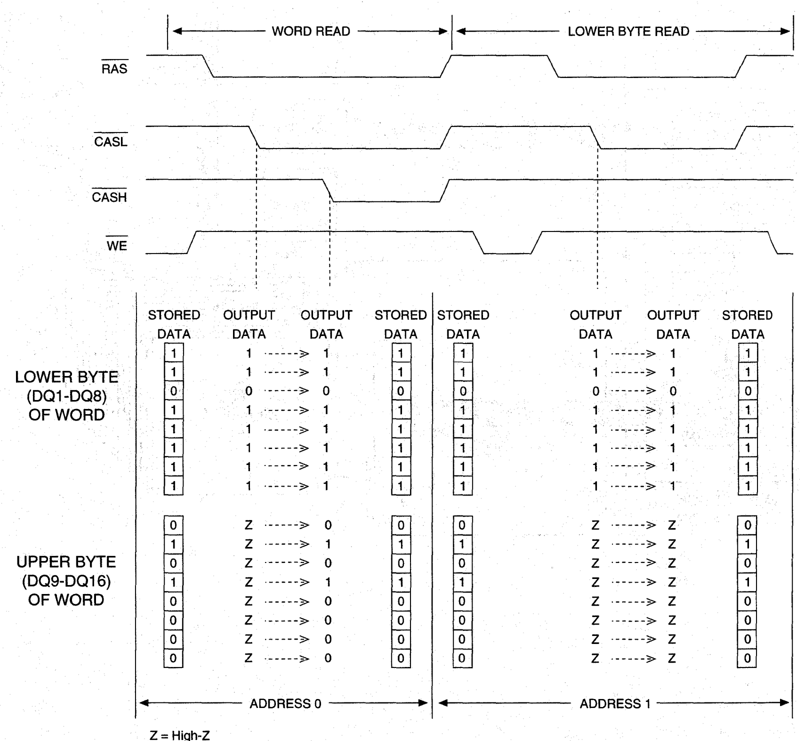

Figure 2
WORD AND BYTE READ EXAMPLE

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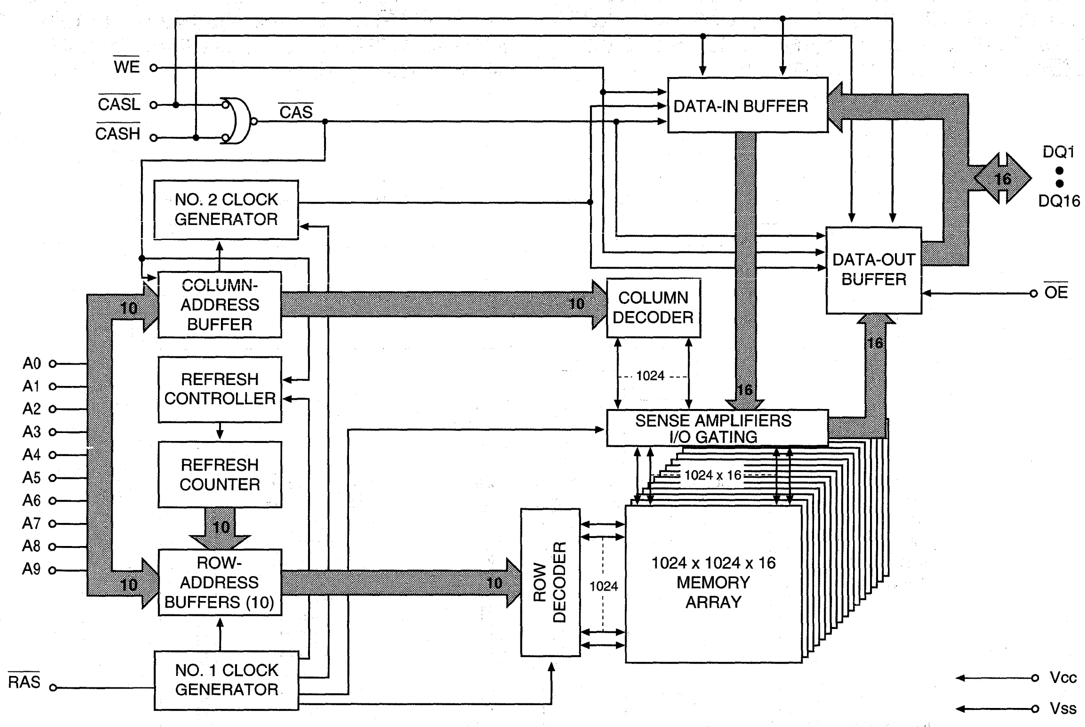
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES		DQs	NOTES
							tR	tC		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY WRITE only.
4. Only one CAS must be active (CASL or CASH).

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ABSOLUTE MAXIMUM RATINGS*

Voltage on a Pin Relative to Vss .... -1V to 7.0V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	V_{CC} + 1V	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)		I_I	-2	2	µA
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} > 5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5.0mA)		V_{OH}	2.4		V
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	180	165	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	160	145	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	150	140	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	31
Row-address setup time	^tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		60		ns	21
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15, 33
Column-address hold time	^tCAH	10		15		ns	31
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	39
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5, 32
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^tCLCH	10		10		ns	34
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	33, 30
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16, 36
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	33
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	32
$\overline{CAS}$ hold time	^tCSH	60		70		ns	32
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5, 31
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	40		45		ns	21, 31
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	26, 32
Data-in hold time	^tDH	10		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22, 33
Output disable	^tOD	3	15	3	15	ns	29, 30, 41
Output Enable	^tOE		15		15	ns	33
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		15		ns	28
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 30, 33
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5.0V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		ns	35
Access time from RAS	tRAC		60		70	ns	14
RAS to column-address delay time	tRAD	15	30	15	35	ns	18
Row-address hold time	tRAH	10		10		ns	
Column-address to RAS lead time	tRAL	30		35		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	tRC	110		130		ns	
RAS to CAS delay time	tRCD	20	45	20	50	ns	17, 31
Read command hold time (referenced to CAS)	tRCH	0		0		ns	19, 26, 32
Read command setup time	tRCS	0		0		ns	26, 31
Refresh period (1,024 cycles)	tREF		16		16	ms	28
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	15		20		ns	40
READ WRITE cycle time	tRWC	150		180		ns	
RAS to WE delay time	tRWD	85		95		ns	21
Write command to RAS lead time	tRWL	15		20		ns	26
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	26, 40
Write command hold time (referenced to RAS)	tWCR	45		55		ns	26
WE command setup time	tWCS	0		0		ns	21, 26, 31
Write command pulse width	tWP	10		15		ns	
WE hold time (CBR REFRESH)	tWRH	10		10		ns	
WE setup time (CBR REFRESH)	tWRP	10		10		ns	

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +5.0V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gate, 100pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS must be pulsed HIGH for tCP.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, access time is controlled exclusively by tCAC.
18. Operation within the tRAD limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
21. tWCS, tRWD, tAWD and tCWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS or OE goes back to VIH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, Q goes open. If OE is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. All other inputs at 0.2V or Vcc -0.2V.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR REFRESH cycles are employed.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both tOD and tOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after tOEH is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once tOD or tOFF occur.

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NOTES (continued)

30. The 3ns minimum is a parameter guaranteed by design.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

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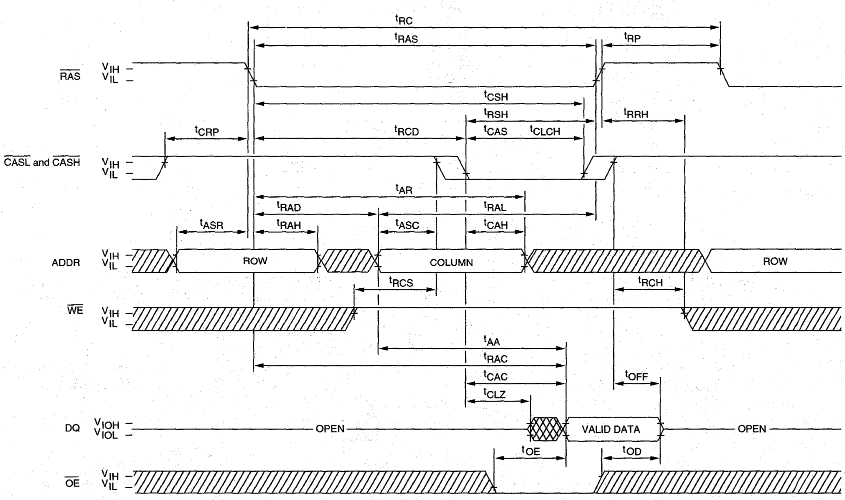
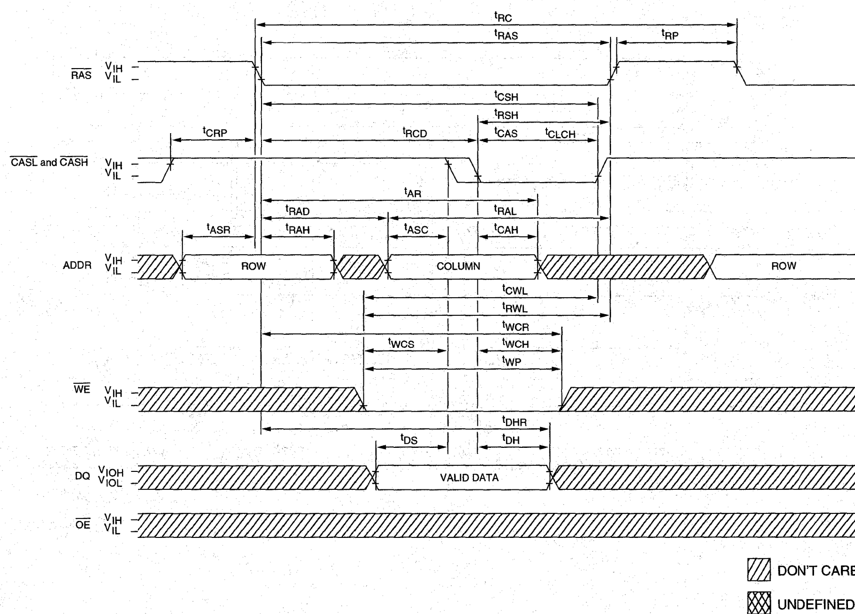
READ CYCLE



EARLY WRITE CYCLE



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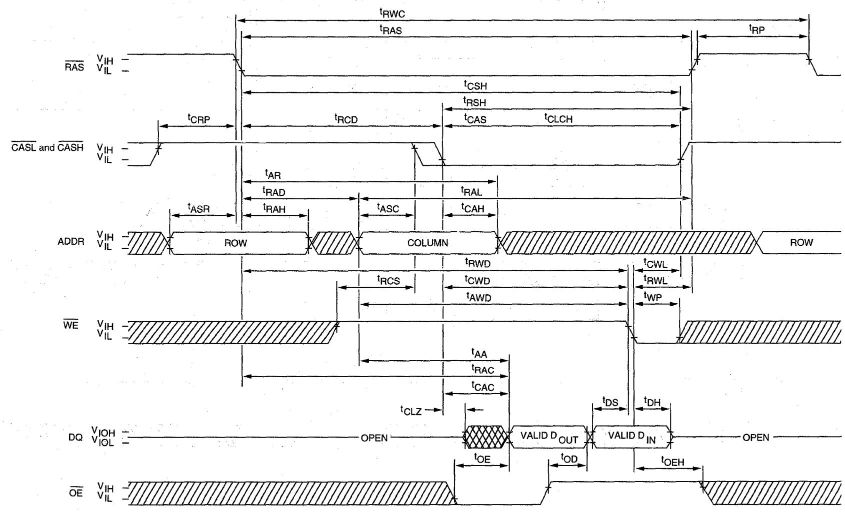
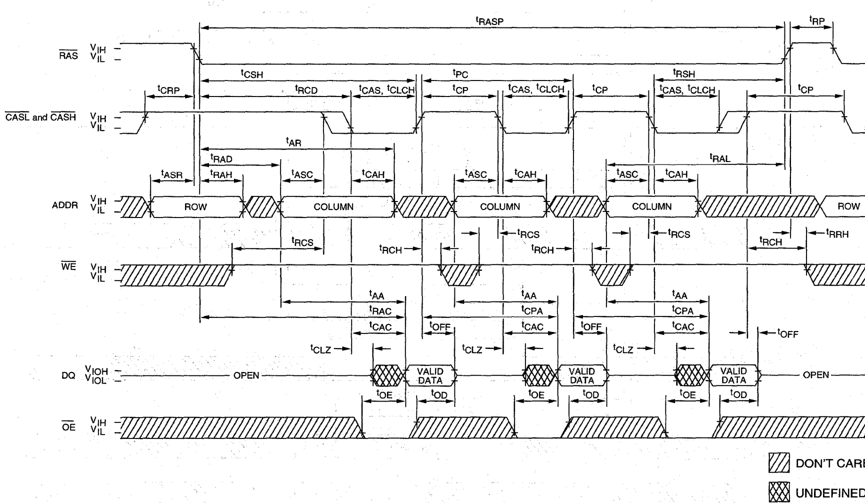
NEW FPM DRAM

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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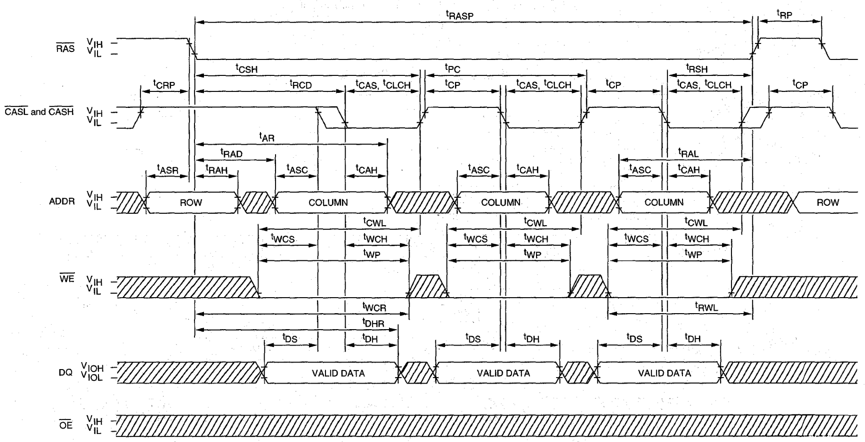
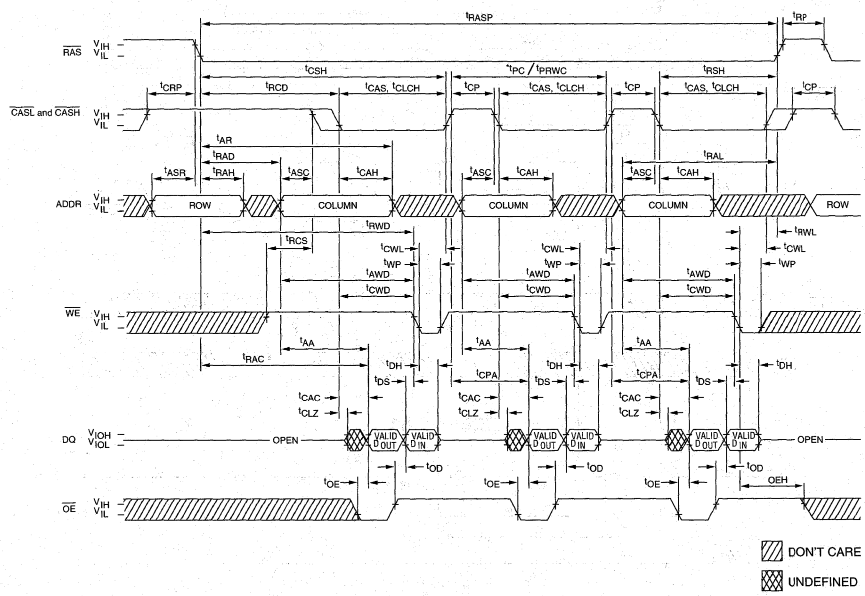
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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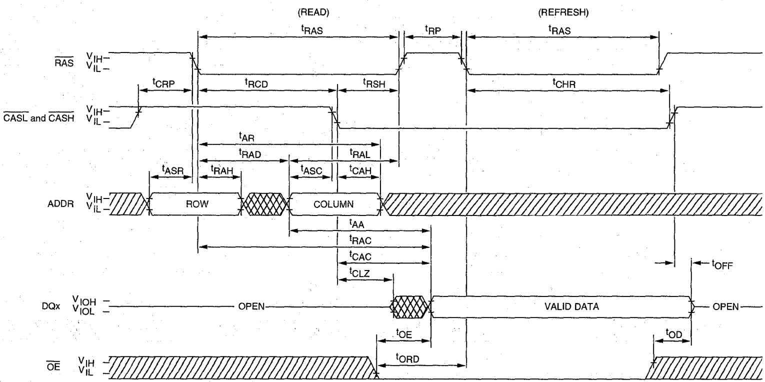
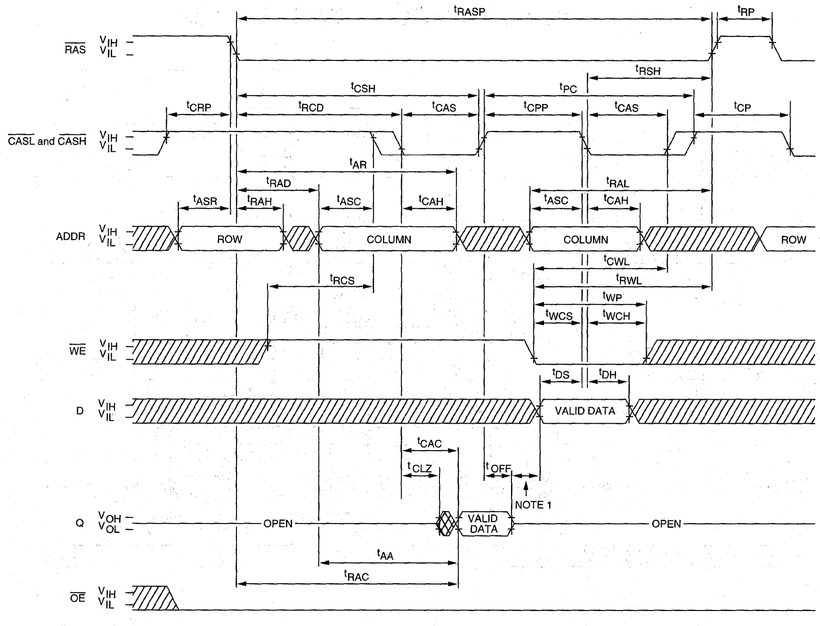
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to High-Z.

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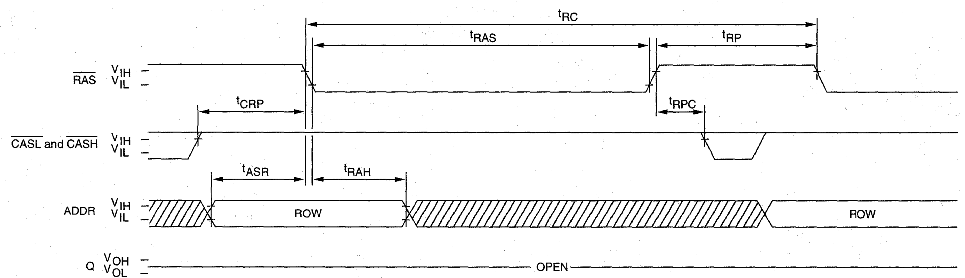
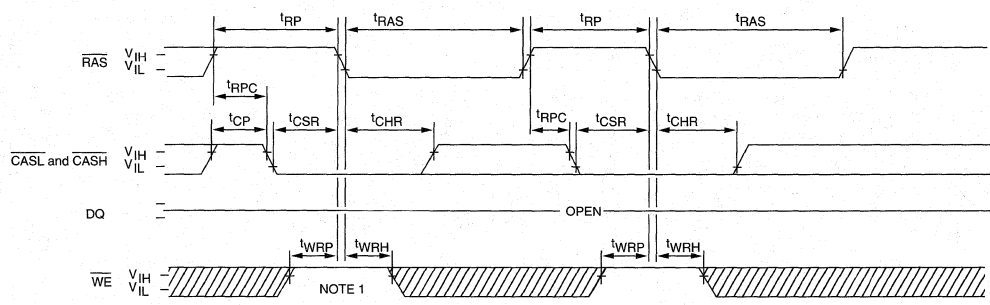
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.

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DRAM

1 MEG x 16 DRAM

3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and SELF
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Low power, 0.3mW standby; 250mW active, typical
- Optional SELF REFRESH mode, with Extended Refresh rate (8x)
- 5V tolerant I/O (5.5V maximum V_{IH} level)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic TSOP (400 mil)	TG

- Part Number Example: MT4LC1M16C3TG-7 S

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP
(DB-5)

Signal	Pin	Pin	Signal
Vcc	1	50	Vss
DQ1	2	49	DQ16
DQ2	3	48	DQ15
DQ3	4	47	DQ14
DQ4	5	46	DQ13
Vcc	6	45	Vss
DQ5	7	44	DQ12
DQ6	8	43	DQ11
DQ7	9	42	DQ10
DQ8	10	41	DQ9
NC	11	40	NC
NC	15	36	NC
NC	16	35	CASL
WE	17	34	CASH
RAS	18	33	OE
NC	19	32	A9
NC	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
Vcc	25	26	Vss

GENERAL DESCRIPTION

The MT4LC1M16C3(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. The MT4LC1M16C3(S) has both BYTE WRITE and WORD WRITE access cycles via two CAS pins (CASL and CASH). These function in an identical manner to a single CAS of other DRAMs in that either CASL or CASH will generate an internal CAS.

The MT4LC1M16C3(S) CAS function and timing are determined by the first CAS (CASL or CASH) to transition LOW and the last CAS to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL transitioning LOW selects an access cycle for the lower byte (DQ1-DQ8) and CASH transitioning LOW selects an access cycle for the upper byte (DQ9-DQ16).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. The CAS function is determined by the first CAS (CASL or CASH) to transition LOW and the last one to transition back HIGH. The CAS function also determines whether the cycle will be a refresh cycle (RAS ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS goes LOW.

The CASL and CASH inputs internally generate a CAS signal functioning in an identical manner to the single CAS input of other DRAMs. The key difference is each CAS input (CASL and CASH) controls its corresponding DQ tristate logic (in conjunction with OE and WE). CASL controls DQ1 through DQ8 and CASH controls DQ9 through DQ16. The two CAS controls give the MT4LC1M16C3(S) both BYTE READ and BYTE WRITE cycle capabilities.

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GENERAL DESCRIPTION (continued)

A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Taking WE LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High- Z) until the next CAS cycle. If WE goes LOW after CAS goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS and OE remain LOW (regardless of WE or RAS). This late WE pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE and WE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on the S version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL and CASH. Enabling CASL will select a lower BYTE access (DQ1-DQ8). Enabling CASH will select an upper BYTE access (DQ9-DQ16). Enabling both CASL and CASH selects a WORD WRITE cycle.

The MT4LC1M16C3 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS inputs. Figure 1 illustrates the BYTE WRITE

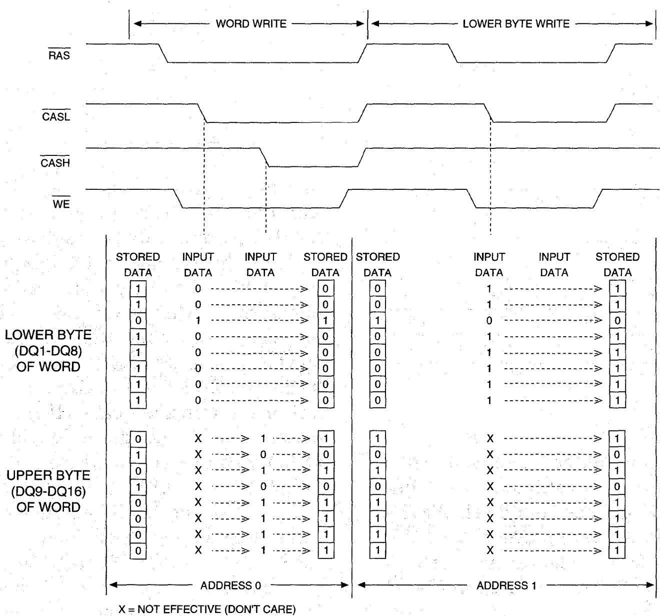

Figure 1
WORD AND BYTE WRITE EXAMPLE

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BYTE ACCESS CYCLE (continued)

and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses are executed at least every 16ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4LC1M16C3 S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms four times longer than the standard 16ms specification.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding $\overline{RAS}$ LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS (≈^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs prior to the resumption of normal operation.

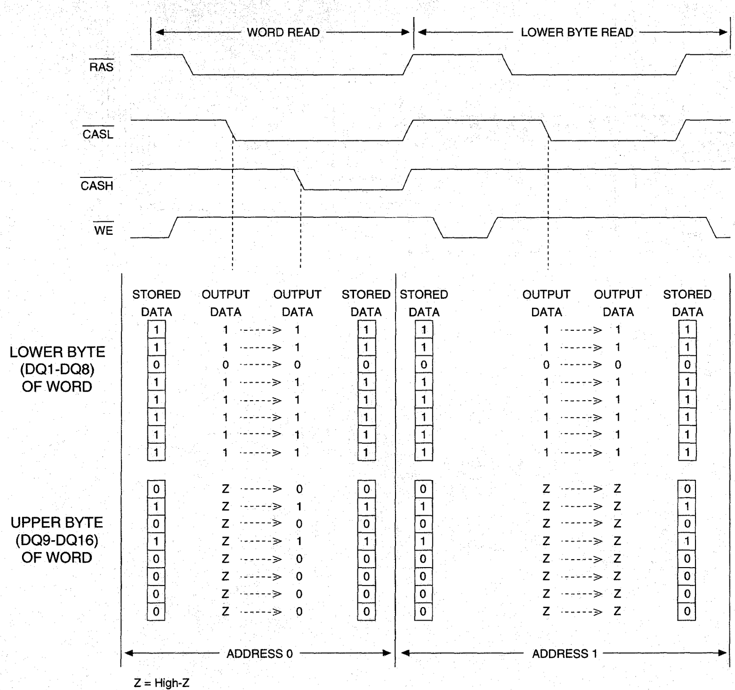

Figure 2
WORD AND BYTE READ EXAMPLE

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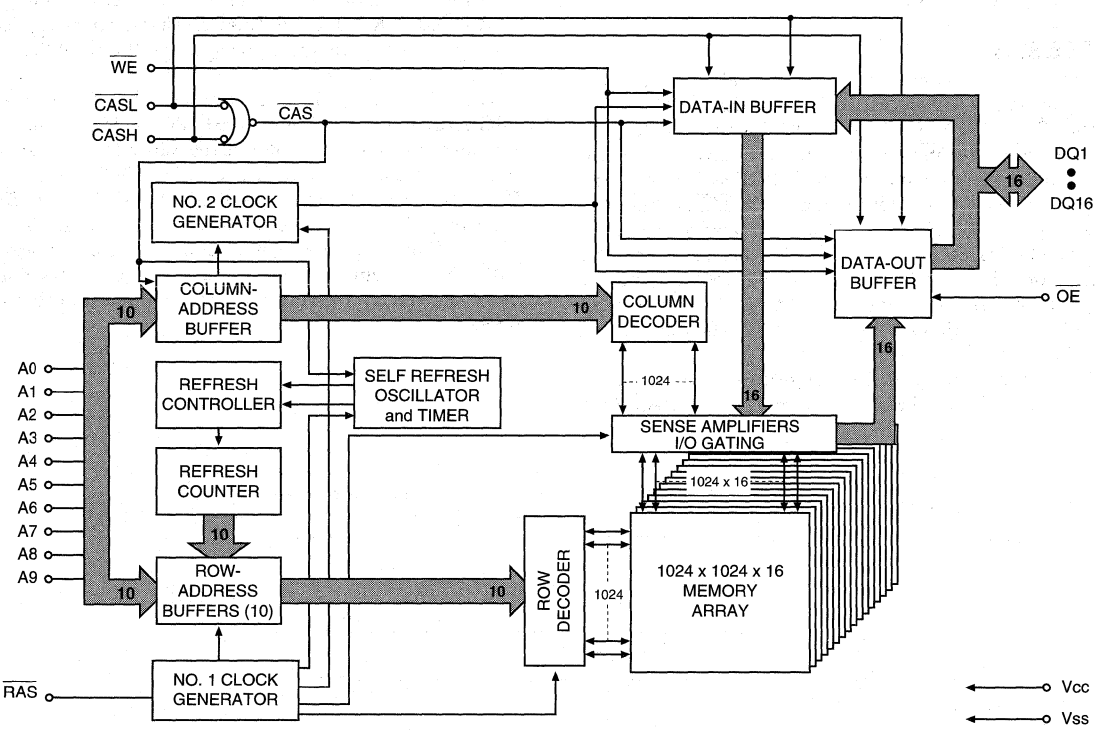
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	H	X	X	X	High-Z	4
SELF REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
3. EARLY WRITE only.
4. Only one $\overline{\text{CAS}}$ must be active ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$).

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FPM DRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc pin Relative to Vss .... -1V to 4.6V
Voltage on Inputs or I/O pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	5.5V	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.0mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.0mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	500	500	µA	25
	I_{CC2} (S only)	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	170	155	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	100	90	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	160	145	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	150	140	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A9, $\overline{OE}$ and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} - 0.2V; A0-A9, $\overline{OE}$ and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CASL}$, $\overline{CASH}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address setup time	^{t}ASC	0		0		ns	31
Row-address setup time	^{t}ASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		60		ns	21
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15, 33
Column-address hold time	^{t}CAH	10		15		ns	31
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	39
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	15		15		ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5, 32
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^{t}CLCH	10		10		ns	34
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	33, 30
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	16, 36
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	33
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		ns	32
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	32
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		ns	5, 31
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		45		ns	21, 31
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	26, 32
Data-in hold time	^{t}DH	10		15		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	22, 33
Output disable	^{t}OD	3	15	3	15	ns	29, 30, 41
Output Enable	^{t}OE		15		15	ns	33
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		15		ns	28
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 30, 33
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		95		ns	35
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		µs	27
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19, 32
Read command setup time	^tRCS	0		0		ns	31
Refresh period (1,024 cycles)	^tREF		16		16	ms	28
Refresh period (1,024 cycles) S version	^tREF		128		128	ms	28
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	40
READ WRITE cycle time	^tRWC	150		180		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		95		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	40
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21, 31
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gate, 100pF and VOL = 0.8V and VOH = 2.0V.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at 0.2V or Vcc -0.2V.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR REFRESH cycles are employed.
28. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur.

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NOTES (continued)

30. The 3ns minimum is a parameter guaranteed by design.
31. The first $\overline{CAS}$x edge to transition LOW.
32. The last $\overline{CAS}$x edge to transition HIGH.
33. Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. Each $\overline{CAS}$x must meet minimum pulse width.
40. Last $\overline{CAS}$x to go LOW.
41. All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.

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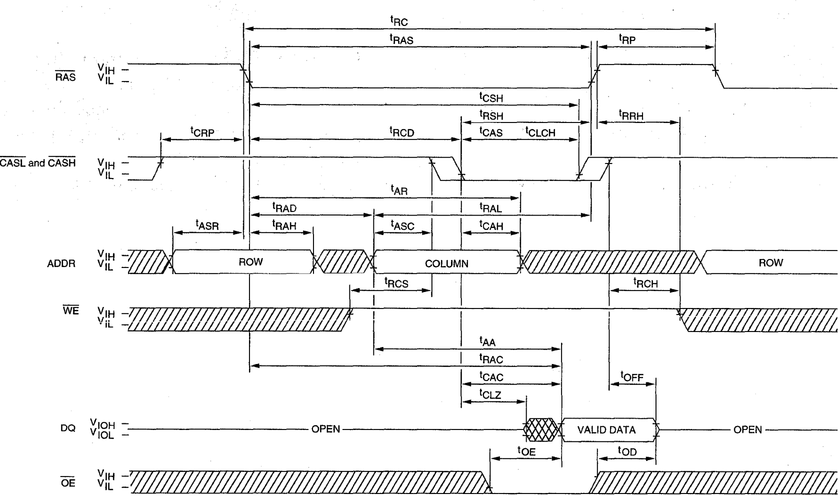
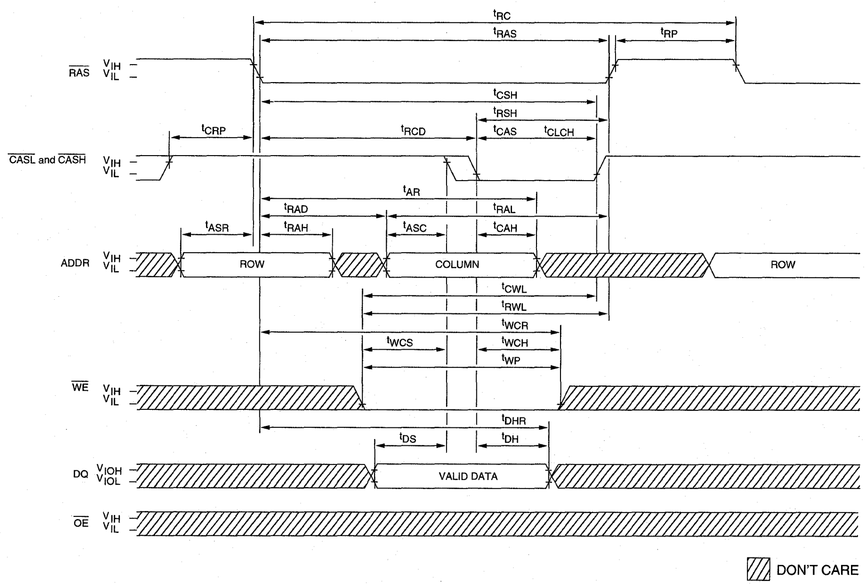
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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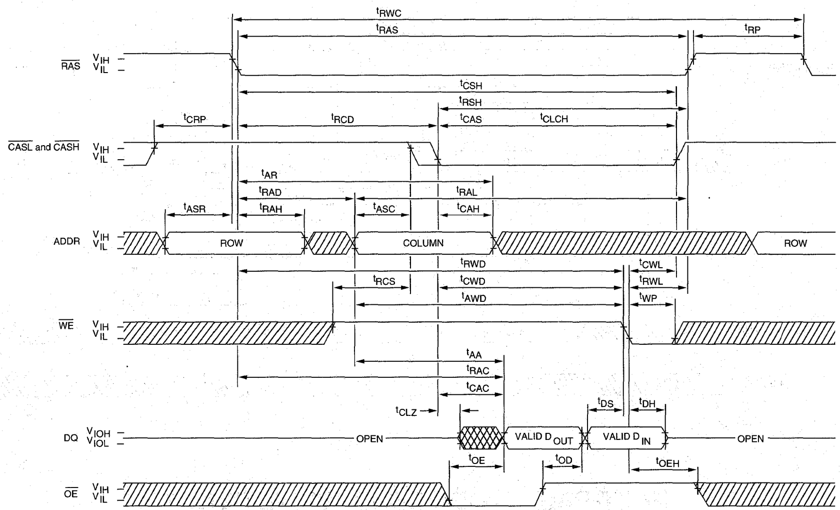
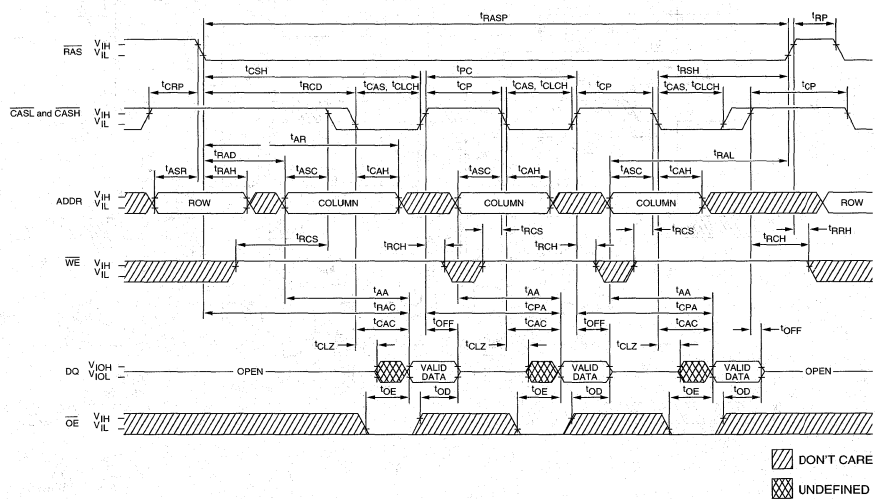
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



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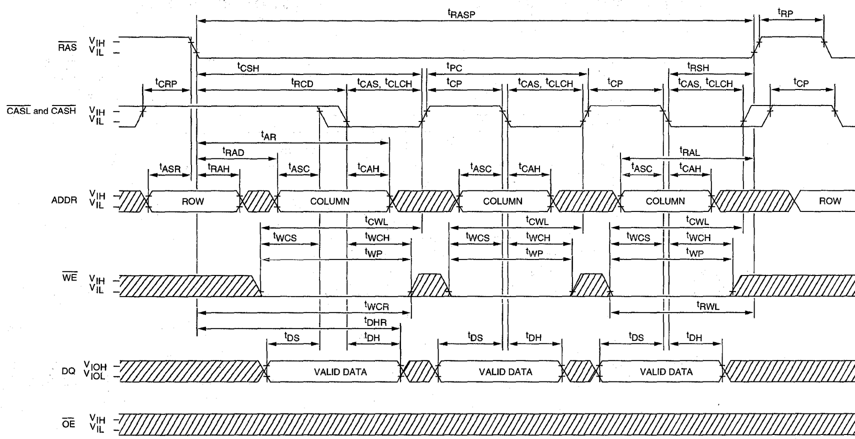
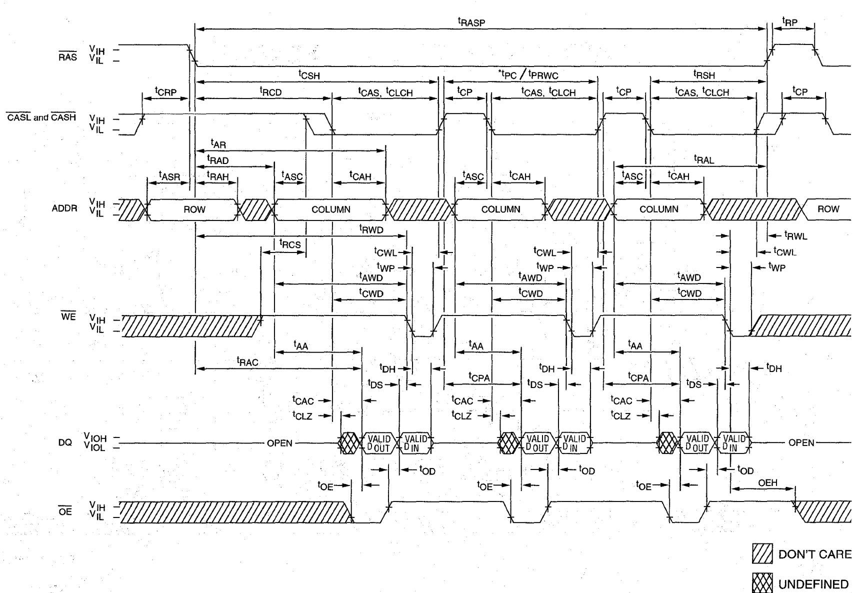
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE only.

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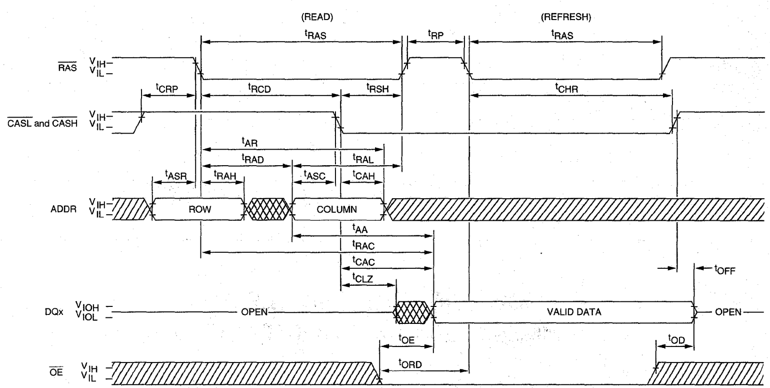
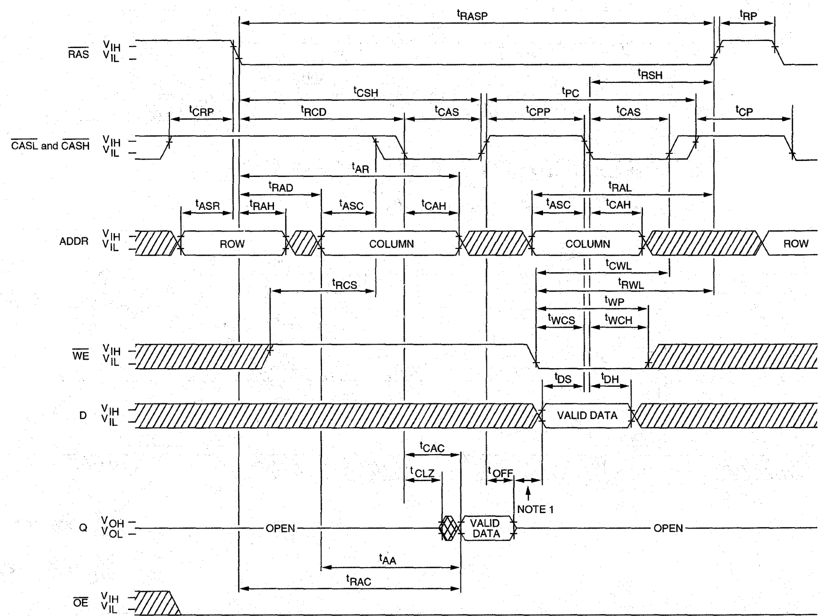
HIDDEN REFRESH CYCLE [24]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to High-Z.

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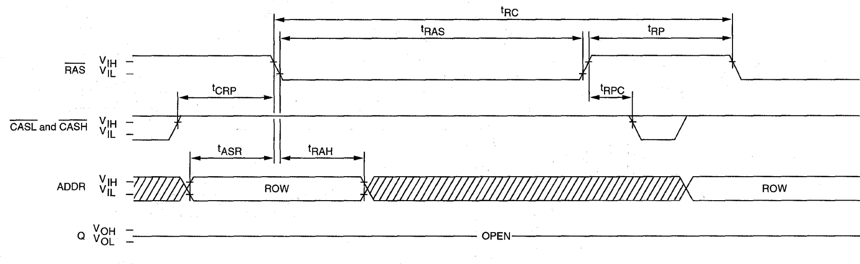
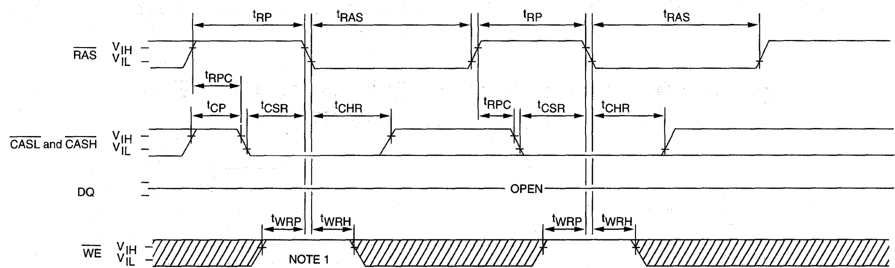
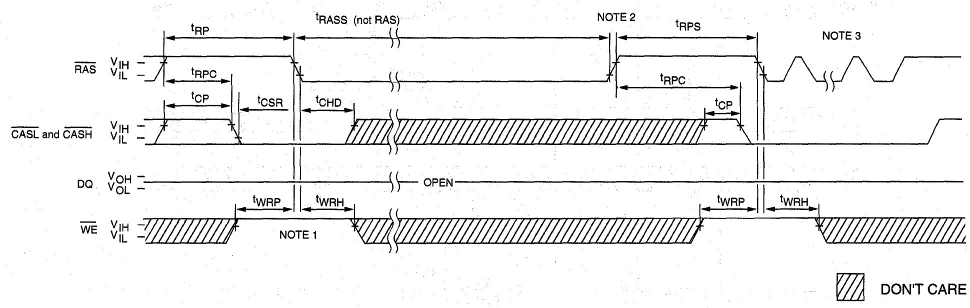
RAS-ONLY REFRESH CYCLE
(OE and WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE = DON'T CARE)



SELF REFRESH CYCLE ("SLEEP MODE")
(Addresses and OE = DON'T CARE)



NOTE:

1. tWRP and tWRH are for system design reference only. The WE signal is actually a "don't care" at RAS time during a CBR REFRESH. However, WE should be held HIGH at RAS time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE HIGH at RAS time during a CBR REFRESH.
2. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
3. Once tRPS is satisfied, a compete burst of all rows should be executed.

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SGRAM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Speed Grade (ns)	Power Dissipation		No. of Pins	Page
				Standby	Active	TQFP	
256K x 32	3.3V	MT41LC256K32D4	10, 12, 15	TBD	TBD	100	3-1
256K x 32	3.3V	MT41LC256K32D4 S	10, 12, 15	TBD	TBD	100	3-1

S = SELF REFRESH

SYNCHRONOUS GRAPHICS RAM

256K x 32 SGRAM

PULSED $\overline{RAS}$, DUAL BANK, PIPELINED, 3.3V OPERATION

FEATURES

- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Dual internal banks for hiding row access/precharge; dual 128K x 32 architecture
- Programmable burst lengths: 2, 4, 8 or full page
- BLOCK WRITE and WRITE-PER-BIT modes
- Independent byte operation via DQM0-3
- AUTO PRECHARGE and AUTO REFRESH modes
- 17ms, 1,024-cycle refresh (16.6µs/row)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS — MARKING

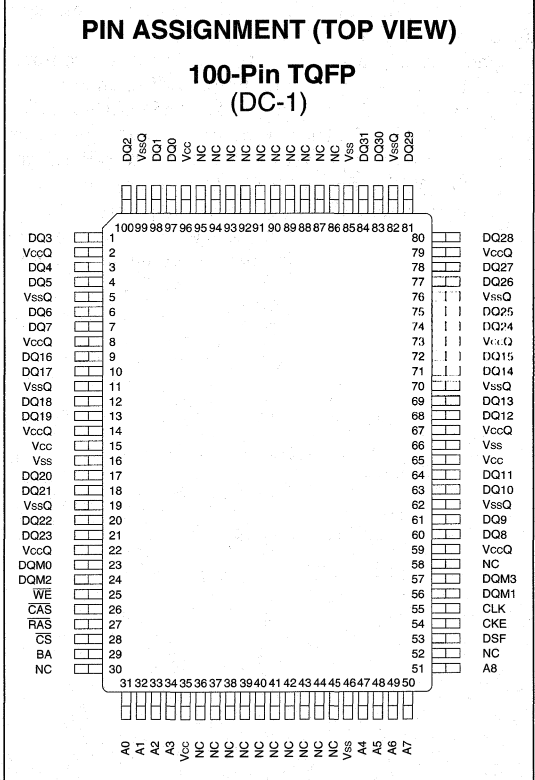
- Timing
  - 10ns access (≤100 MHz clock rate) — -10
  - 12ns access (≤83 MHz clock rate) — -12
  - 15ns access (≤66 MHz clock rate) — -15
- Self Refresh — S
- Plastic Packages
  - 100-pin TQFP (0.65mm lead pitch) — LG
- Part Number Example: MT41LC256K32D4LG -15

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME	SET-UP TIMES	HOLD TIMES
-10	100 MHZ	9ns	3ns	1ns
-12	83 MHZ	11ns	3.5ns	1.5ns
-15	66 MHZ	13ns	4ns	2ns

PIN ASSIGNMENT (TOP VIEW)

100-Pin TQFP (DC-1)



GENERAL DESCRIPTION

The MT41LC256K32D4(S) SGRAM is a high-speed CMOS dynamic random access memory containing 8,388,608 bits. It is internally configured as a dual 128K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 128K x 32 bit banks is organized as 512 rows by 256 columns by 32 bits. Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SGRAM provides for programmable READ or WRITE burst lengths of 2, 4 or 8 locations, or the full page, with burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

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NEW SGRAM

GENERAL DESCRIPTION (continued)

The MT41LC256K32D4(S) uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles, and provide seamless high-speed random access operation.

Synchronous graphics RAMs (SGRAMs) differ from synchronous DRAMs (SDRAMs) by providing an eight-column BLOCK WRITE function and a MASKED WRITE (or WRITE-PER-BIT) function to accommodate high-performance graphics applications. The BLOCK WRITE and MASKED WRITE functions may be combined with individual byte enables (DQ mask, or DQM, pins).

The CMOS dynamic memory structure of the MT41LC256K32D4(S) is designed to operate in 3.3V, low-power memory systems. An AUTO REFRESH mode is provided along with a power saving POWER-DOWN mode. All inputs and outputs are LVTTL-compatible.

The two-bank synchronous DRAM and x32 configuration provided by the SGRAM are well suited for applications requiring high memory bandwidth, and when combined with special graphics functions result in a device particularly well suited to high performance graphics applications.

SGRAMs offer substantial advances in dynamic memory operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, the capability to randomly change column addresses on each clock cycle during a burst access, and special functions such as MASKED WRITEs and BLOCK WRITEs.

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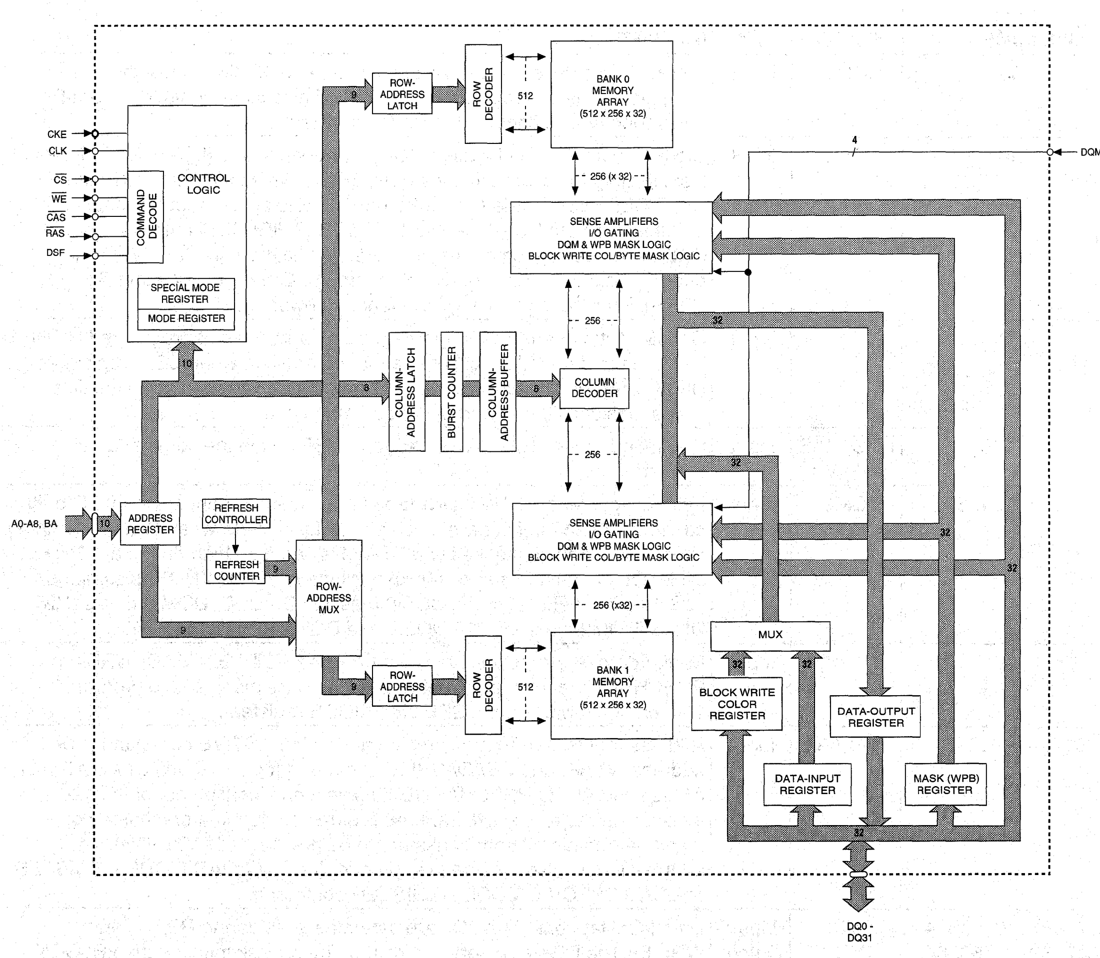
FUNCTIONAL BLOCK DIAGRAM



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NEW ■ SGRAM

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
55	CLK	Input	Clock: CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
54	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides POWER-DOWN mode (all banks idle) and SELF REFRESH mode (all banks idle). CKE is synchronous except after the device enters POWER-DOWN and SELF REFRESH modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during POWER-DOWN and SELF REFRESH modes providing low standby power.
28	$\overline{CS}$	Input	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
27, 26 53, 25	$\overline{RAS}$, $\overline{CAS}$ DSF, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$, and DSF define the command being entered.
23, 56, 24, 57	DQM0 - DQM3	Input	Input/Output Mask: DQM0-DQM3 are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a High-Z state when DQM is sampled HIGH. Input data is masked when DQM is sampled high during a WRITE cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQM0 masks DQ0-DQ7, DQM1 masks DQ8-DQ15, DQM2 masks DQ16-DQ23, and DQM3 masks DQ24-DQ31.
29	BA	Input	Bank Address: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the 10th bit of the MODE and SPECIAL MODE registers.
31-34, 47-50, 51	A0-A8	Input	Address Inputs: A0-A8 are sampled during the ACTIVE command (row-address A0-A8) and READ/WRITE command (column-address A0-A7 with A8 defining AUTO PRECHARGE) to select one location out of the 128K available in the respective bank.A8 is sampled during a precharge command determining if both banks are to be precharged (A8 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER or LOAD SPECIAL MODE REGISTER command.
97, 98, 100, 1, 3, 4, 6, 7, 60, 61, 63, 64, 68, 69, 71, 72, 9, 10, 12, 13, 17, 18, 20, 21, 74, 75, 77, 78, 80, 81, 83, 84	DQ0-DQ31	Input/ Output	Data I/O: Data bus. The I/Os are byte-maskable during READs and WRITEs.The DQs also serve as column/byte mask inputs during BLOCK WRITEs.
30, 36-45, 52, 58, 86-95	NC	—	No Connect: These pins should be left unconnected.
2, 8, 14, 22, 59, 67, 73, 79	VccQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
5, 11, 19, 62, 70, 76, 82, 99	VssQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
15, 35, 65, 96	Vcc	Supply	Power Supply: +3.3V ±0.3V.
16, 46, 66, 85	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

In general, the SGRAM is a dual 128K x 32 DRAM with graphics features (BLOCK WRITE and MASKED WRITE) which operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 128K x 32 bit banks is organized as 512 rows by 256 columns by 32 bits.

Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A8 select the row). Then the address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

BLOCK WRITE accesses are performed in a manner similar to WRITEs, except that BLOCK WRITEs are not burst oriented, and always apply to the eight column locations selected by A3-A7.

MASKED WRITEs or MASKED BLOCK WRITEs are similar to the unmasked versions except that the write-per-bit mask enabled with the ACTIVE command is applied to the data being written.

Prior to normal operation, the SGRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SGRAMs must be powered-up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to Vcc and VccQ (simultaneously) the SGRAM requires a 100µs delay prior to activating CKE. All other inputs should be held HIGH during this phase of power-up.

Once the 100µs delay has been satisfied, the CKE pin must be driven HIGH ^{t}CKS before a positive clock edge, after meeting ^{t}CKH from the previous clock edge. The first command will be registered on the clock edge following ^{t}CKS.

Both banks must then be precharged, thereby placing the device in the "all bank idle" state. Once in the idle state, two AUTO REFRESH cycles must be performed. Once the AUTO REFRESH cycles are complete, the SGRAM is ready for mode register programming. Because the mode register will power-up in an unknown state, it should be loaded prior to performing any operational command.

Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SGRAM. This definition includes the selection of a burst length, a burst type, a read latency and an operating mode, as shown in Figure 1. The mode register is programmed via the LOAD MODE REGISTER command, and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0 through M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4 through M6 specify the READ latency, and M7 through M9 specify the operating mode.

The mode register must be loaded when both banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements may result in unknown operation.

Burst Length

Read and write accesses to the SGRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is defined by A1-A7 when the burst length is set to two, by A2-A7 when the burst length is set to four and by A3-A7 when the burst length is set to eight. The lower order address bit(s) are used to select the starting location within the block. Full page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or "interleaved"; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

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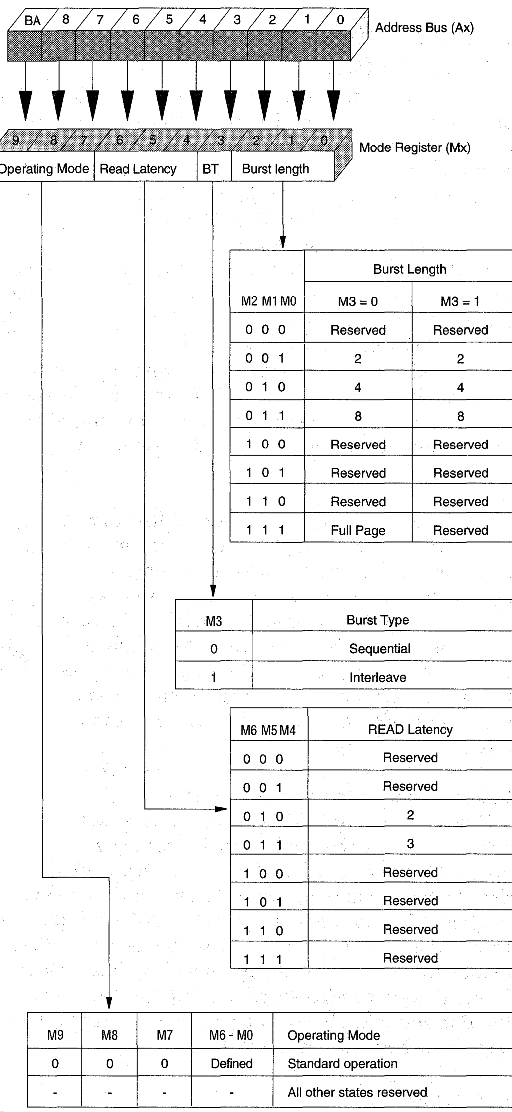
NEW SGRAM



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleave

M6 M5 M4	READ Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M9	M8	M7	M6 - M0	Operating Mode
0	0	0	Defined	Standard operation
-	-	-	-	All other states reserved

Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address:	Order of Accesses within a Burst: Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0 - A7 (location 0 - 255)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1 (Cn+256), Cn (Cn+257)...	Not supported

NOTE:
1. For a burst length of two, A1-A7 select the block of two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A7 select the block of eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0-A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

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Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 2 or 3 clocks.

If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available by clock edge $n + m$. The DQs will start driving as a result of the clock edge one cycle earlier ($n + m - 1$) and, provided that the relevant access times are met, the data will be valid by clock edge $n + m$. For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0, and the latency is programmed to 2 clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 2 below indicates the operating frequencies at which each READ latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Operating Mode

In normal operation (M7 – M9 = 0), the programmed burst length applies to both read and write bursts.

M7 = 1 is used for vendor specific testing. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

SPECIAL MODE REGISTER

The special mode register is used to load the color and mask registers, which are used in BLOCK WRITE and MASKED WRITE cycles. The control information being written to the special mode register is applied to the address inputs and the data to be written to either the color register or the mask register is applied to the DQs. As shown in Figure 3, when input A6 is "1", and all other address inputs are "0" during a LOAD SPECIAL MODE REGISTER cycle, the color register will be loaded with the data on the DQs. Similarly, when input A5 is "1", and all other address inputs are "0" during a LOAD SPECIAL MODE REGISTER cycle, the mask register will be loaded with the data on the DQs. Applying a "1" to both A5 and A6 (when all other address inputs are "0") or applying a "1" to any address input other than A5 or A6, during a LOAD SPECIAL MODE REGISTER cycle is illegal and unknown operation may result.

The special mode register can be loaded when one or both banks are either active or idle. Successive LOAD SPECIAL MODE REGISTER cycles to load the same register can be performed by applying a "1" to either A5 or A6, even if a "1" was previously written to that bit (i.e., the bits do not need to be cleared between loads).

COLOR REGISTER

The color register is a 32-bit register which supplies the data during BLOCK WRITE cycles. The color register is loaded via a LOAD SPECIAL MODE REGISTER cycle (described in the previous section) and will retain data until loaded again or until power is removed from the SGRAM.

MASK REGISTER

The mask register (or write-per-bit mask register) is a 32-bit register which acts as a per-DQ mask during MASKED WRITE and MASKED BLOCK WRITE cycles. This operation is described under the respective headings later in this data sheet. The mask register is loaded via a LOAD SPECIAL MODE REGISTER cycle (described previously, under the Special Mode Register heading) and will retain data until loaded again or until power is removed from the SGRAM.

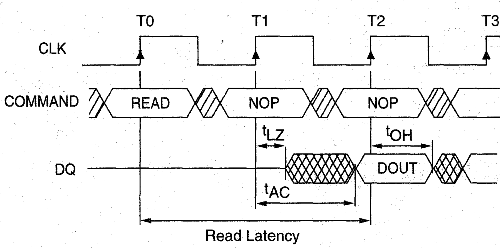

Figure 2
TWO CLOCK READ LATENCY EXAMPLE

Table 2
READ LATENCY

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	READ LATENCY = 2	READ LATENCY = 3
-10	≤ 66	≤ 100
-12	≤ 55	≤ 83
-15	≤ 44	≤ 66

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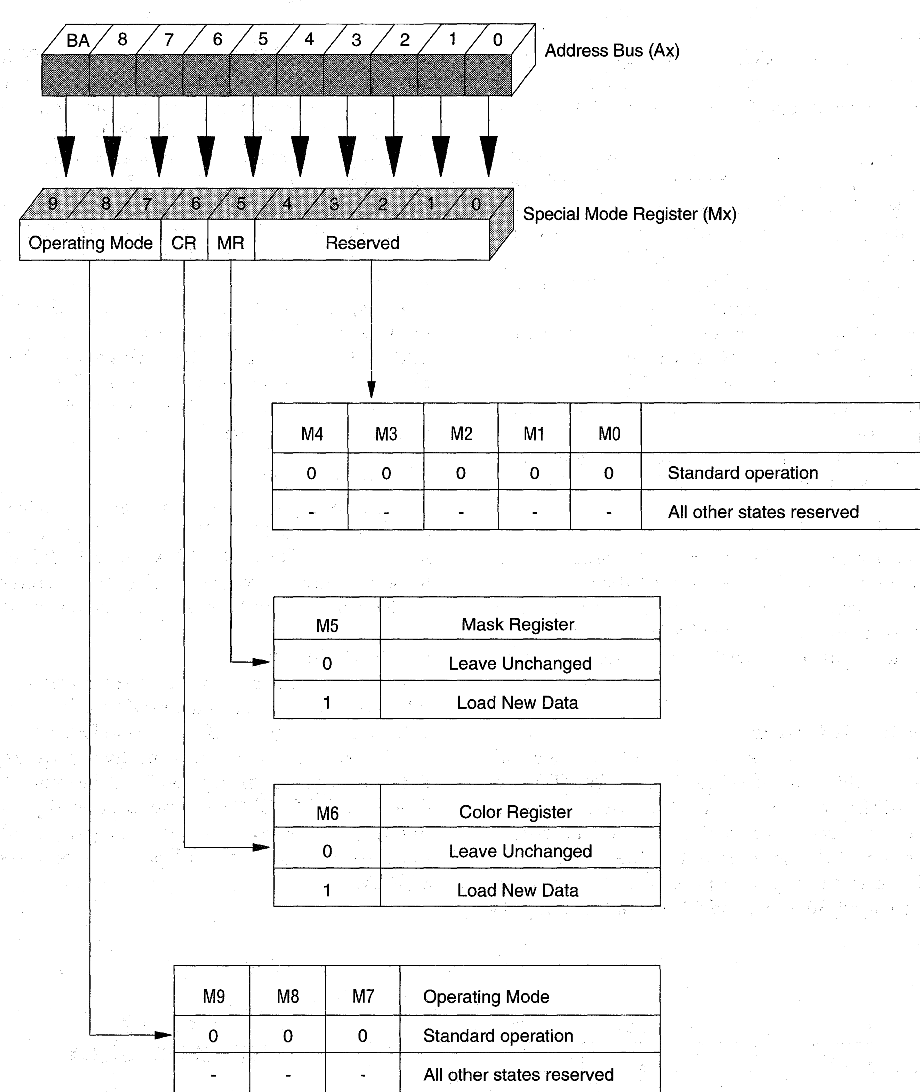

Figure 3
SPECIAL MODE REGISTER DEFINITION

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Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the Operation section; these tables provide current state/ next state information.

TRUTH TABLE 1 – Commands and DQM Operation

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	L	X	X	X	13
ACTIVE (Select bank and activate row)	L	L	H	H	L	X	bank/row	X	3
ACTIVE with WPB (Select bank, activate row and WPB)	L	L	H	H	H	X	bank/row	X	3, 11
READ (Select bank & column and start READ burst)	L	H	L	H	L	X	bank/col	X	4, 13
WRITE (Select bank & column and start WRITE burst)	L	H	L	L	L	X	bank/col	VALID	4
BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	L	H	L	L	H	X	bank/col	MASK	4, 12
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	L	X	Code	X	5, 13
BURST TERMINATE	L	H	H	L	L	X	X	Active	13
AUTO REFRESH or SELF REFRESH (enter SELF REFRESH mode)	L	L	L	H	L	X	X	X	6, 7, 13
LOAD MODE REGISTER	L	L	L	L	L	X	OpCode	X	2
LOAD SPECIAL MODE REGISTER	L	L	L	L	H	X	OpCode	VALID	10
Write enable/output enable	-	-	-	-	-	L	-	Active	8
Write inhibit/output High-Z	-	-	-	-	-	H	-	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0 through A8 and BA define the op-code written to the mode register.
3. A0 through A8 provide row-address and BA determines which bank is made active (BA LOW = Bank 0 and BA HIGH = Bank 1).
4. A0 through A7 provide column-address; A8 HIGH enables the AUTO PRECHARGE feature (nonpersistent) while A8 LOW disables the AUTO PRECHARGE feature; BA determines which bank is being read from or written to (BA LOW = Bank 0 and BA HIGH = Bank 1).
5. A8 LOW: BA determines bank being precharged (BA LOW = Bank 0 and BA HIGH = Bank 1). A8 HIGH: both banks precharged and BA is a "don't care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "don't care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).
9. Illegal on non-S version.
10. DQs contain either color data or WPB mask data.
11. Any WRITE or BLOCK WRITE cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals and the column/byte mask information (the latter for BLOCK WRITEs only).
12. DQs contain the column/byte mask data for the BLOCK WRITE.
13. DSF is actually "don't care", but it is recommended to be LOW for compatibility with future devices.

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COMMAND INHIBIT

The COMMAND INHIBIT function prevents commands from being executed by the SGRAM, regardless of whether the CLK signal is enabled. The SGRAM is effectively deactivated, or deselected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SGRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states.

LOAD MODE REGISTER

The mode register is loaded via inputs A0-A8 and BA. See Mode Register heading in Register Definition section. The LOAD MODE REGISTER command can only be issued when both banks are idle, and a subsequent executable command cannot be issued until ^{t}MTC is met.

LOAD SPECIAL MODE REGISTER

This command is used to load either the color register or mask register by activating the appropriate bit in the special mode register. The control information is provided on inputs A0-A8 and BA, while the data for the color or mask register is provided on the DQs. See Special Mode Register heading in Register Definition section. The LOAD SPECIAL MODE REGISTER command can be issued when both banks are idle, or one or both are active, but with no READ, WRITE or BLOCK WRITE accesses in progress. A subsequent executable command cannot be issued until ^{t}SML is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA input selects the bank, and the address provided on inputs A0-A8 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE WITH WPB

This command is similar to the ACTIVE command, except that the write-per-bit mask is activated. Any WRITE or BLOCK WRITE cycles to the selected bank/row while active will be masked according to the contents of the mask register, in addition to the DQM signals, and the column/byte mask information (the latter for BLOCK WRITEs only).

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A8 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the read burst; if it is not selected, the row will remain open for subsequent accesses. READ data appears on the DQs subject to the values on the DQM inputs two clocks earlier. If a particular DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A8 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of the write burst; if it is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM signals registered coincident with the data. If a particular DQM signal is registered LOW, the corresponding data will be written to memory (subject also to the write-per-bit mask, if activated); if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and the write will not be executed to that byte location.

BLOCK WRITE

The BLOCK WRITE command is used to write a single data value to the block of eight consecutive column locations addressed by inputs A3-A7. The source of the data is the color register, which must be loaded prior to the BLOCK WRITE. The information on the DQs which is registered coincident with the BLOCK WRITE command is used to mask specific column/byte combinations within the block, as described in the Operation section of this data sheet. The DQM signals operate as for WRITE cycles, but are applied to all eight columns.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank, or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the precharge command is issued. Input A8 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as a "don't care". Once a bank has been precharged, it is in the idle state and must be activated prior to any READ, WRITE or BLOCK WRITE commands being issued to that bank.

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AUTO PRECHARGE

AUTO PRECHARGE is a nonpersistent feature which performs all of the same individual-bank precharge functions as previously described. The AUTO PRECHARGE feature allows the user to issue a READ, WRITE or BLOCK WRITE command that automatically performs a precharge upon the completion of the BLOCK WRITE access or READ or WRITE burst, except in the full-page burst mode, where it has no effect.

The use of this feature eliminates the need to "manually" issue a PRECHARGE command during the functional operation of the SGRAM. AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command until the precharge time (^{t}RP) is completed. This is determined as if a manual PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SGRAM and is analagous to $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AUTO REFRESH command. The MT41LC256K32D4(S) requires all of its 1,024 rows to be refreshed every 17ms (^{t}REF). Providing a distributed AUTO REFRESH command every 16.6µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, all 1,024 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RC) once every 17ms.

SELF REFRESH

The SELF REFRESH command (on the "S" version) can be used to retain data in the SGRAM, even if the rest of the system is powered down. When in the SELF REFRESH mode, the SGRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SGRAM become "don't cares" with the exception of CKE, which must remain LOW.

Once SELF REFRESH mode is engaged, the SGRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SGRAM may remain in SELF REFRESH mode for an indefinite period.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, the system clock must be stable prior to CKE going back HIGH. Once CKE is HIGH, the SGRAM must have NOP commands issued for ^{t}XSR, because time is required for the completion of any bank currently being internally refreshed.

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Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SGRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

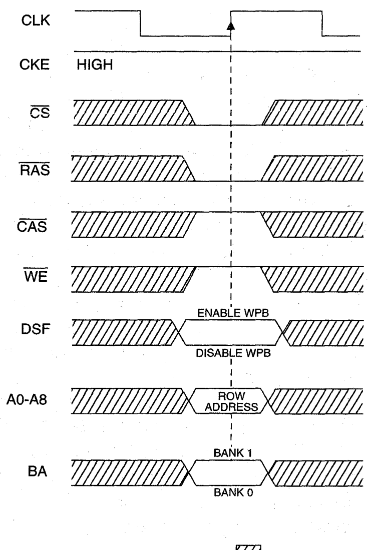

Figure 4
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

The ACTIVE command is also used to determine whether or not the write-per-bit mask is to be applied during WRITE and BLOCK WRITE cycles within that row (see Figure 4). If DSF is HIGH at the time the ACTIVE command is registered (ACTIVE with WPB) then the mask will be applied to all WRITE and BLOCK WRITE cycles to that row until the row is "closed"(precharged).

After opening a row (issuing an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD MIN should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 30ns with a 90 MHz clock (11.11ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 5, which covers any case where $3 > {}^{t}\text{RCD MIN}/{}^{t}\text{CK} > 2$. (The same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to the other bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

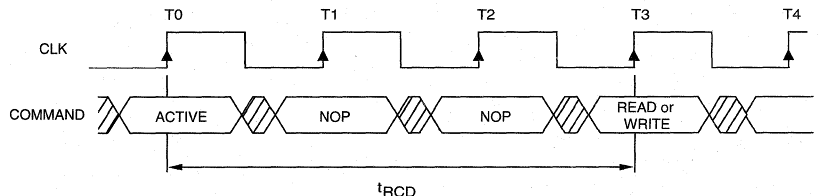

Figure 5
EXAMPLE: MEETING ^{t}RCD MIN WHEN 2 < ^{t}RCD MIN/^{t}CK < 3

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READs

READ bursts are initiated with a READ command, as shown in Figure 6.

The starting column and bank addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, AUTO PRECHARGE is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the READ latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 7 shows the case where the READ latency is set to two, and Figure 8 shows a READ latency of three.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

A fixed-length READ burst may be followed by, or truncated with, a subsequent READ burst (provided that AUTO PRECHARGE is not activated) and a full-page READ burst can be truncated with a subsequent READ burst. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst, or the last desired data element of a longer burst which is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where

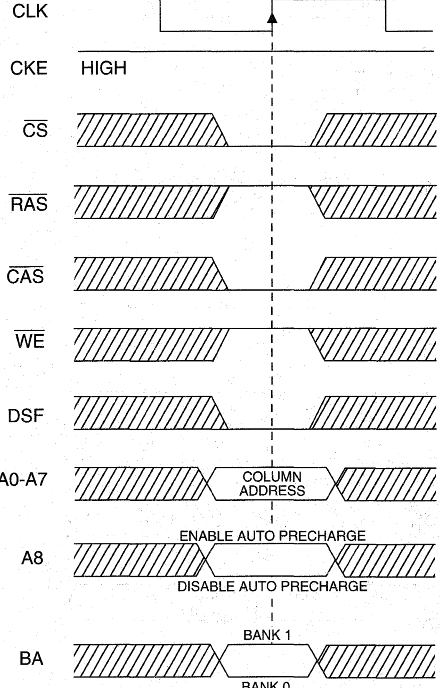

Figure 6
READ COMMAND

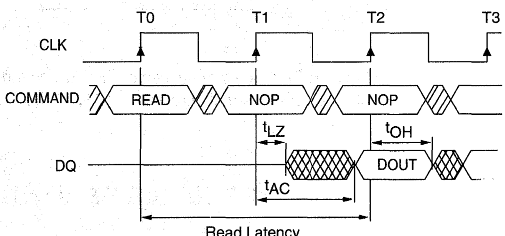

Figure 7
READ BURST WITH READ LATENCY OF TWO

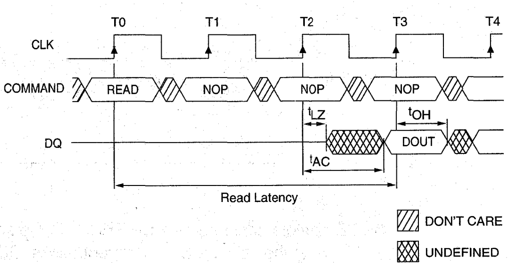

Figure 8
READ BURST WITH READ LATENCY OF THREE

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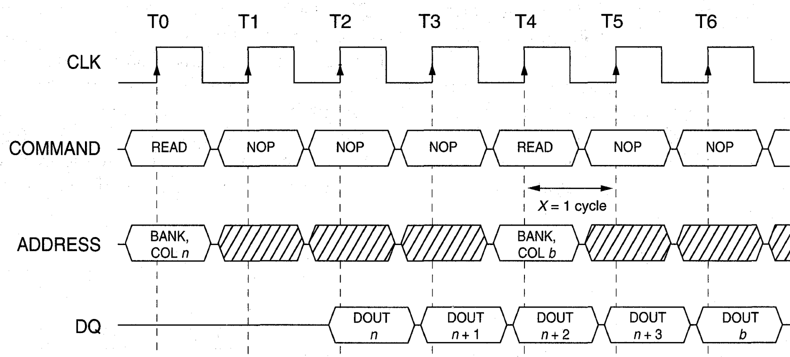
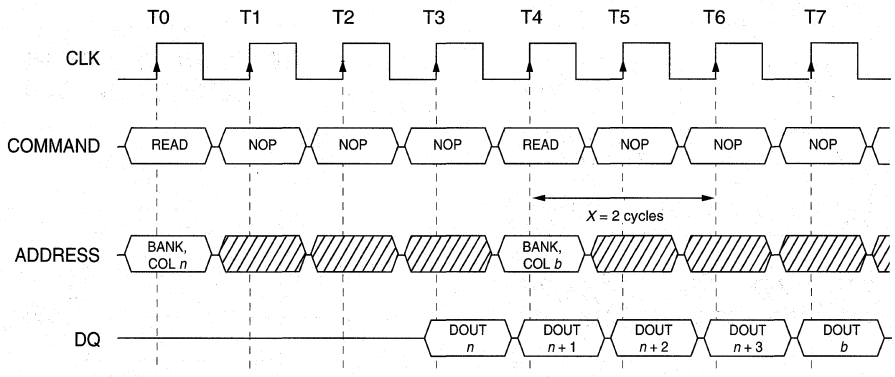
x equals the read latency minus one. This is shown in Figure 9 for a read latency of two and Figure 10 for a read latency of three; data element $n + 3$ is either the last of a burst of four, or the last desired of a longer burst. The SGRAM does not require the $2n$ rule of prefetch architectures, so a READ command can be initiated on any clock cycle following a previous READ command. Full speed random read accesses within a page can be performed as shown in Figures 11 and 12.



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 9
CONSECUTIVE READ BURSTS, READ LATENCY OF TWO



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 10
CONSECUTIVE READ BURSTS, READ LATENCY OF THREE

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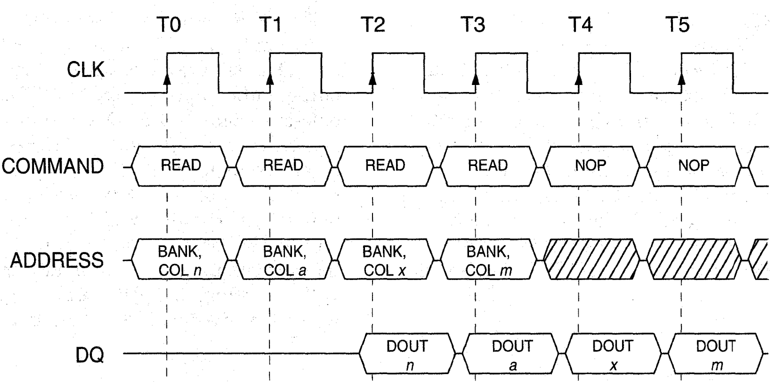
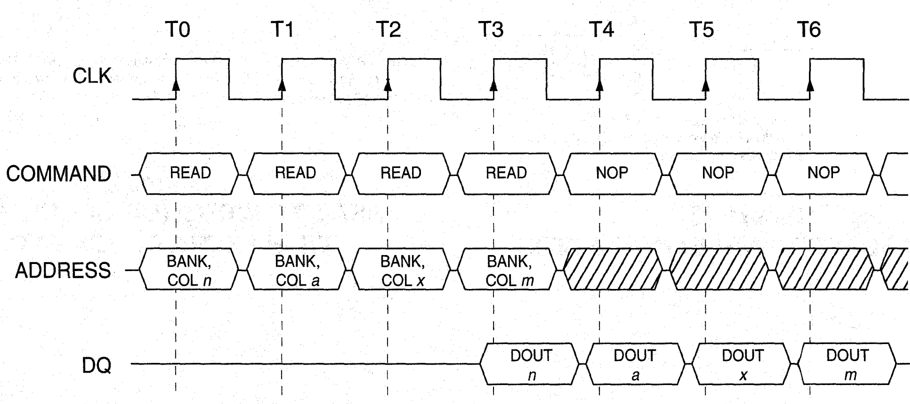


NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 11
RANDOM READ ACCESSES WITHIN A PAGE, READ LATENCY OF TWO



NOTE: Covers either successive READs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

DON'T CARE

Figure 12
RANDOM READ ACCESSES WITHIN A PAGE, READ LATENCY OF THREE

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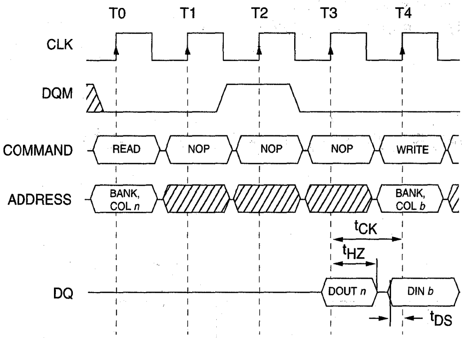
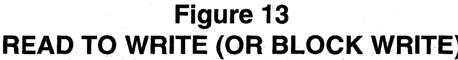
A fixed-length READ burst may be followed by, or truncated with, a WRITE burst or BLOCK WRITE command (provided that AUTO PRECHARGE was not activated) and a full page READ burst may be truncated by a WRITE burst or BLOCK WRITE command. The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. If the specifications for a given speed grade do not allow for contention to be avoided at a particular operating frequency, a single cycle delay must occur between the last READ data and the WRITE command.

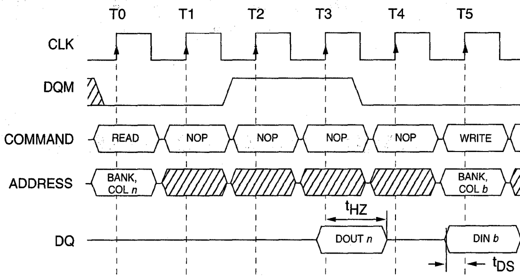
The DQM inputs are used to avoid I/O contention as shown in Figures 13 and 14. The DQMs must be asserted (HIGH) at least two clocks (DQM latency is two clocks for output buffers) prior to the WRITE command to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z) regardless of the state of the DQM signals. The DQM signals must be de-asserted (DQM latency is zero clocks for input buffers) prior to the WRITE command to ensure that the written data is not masked. Figure 13 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 14 shows the case where the additional NOP is needed.





NOTE: A READ LATENCY of 3 is used for illustration. A BLOCK WRITE can be substituted for the WRITE, in which case column/byte mask data would be applied to the data inputs.

Figure 13
READ TO WRITE (OR BLOCK WRITE)



NOTE: A READ LATENCY of 3 is used for illustration. A BLOCK WRITE can be substituted for the WRITE, in which case column/byte mask data would be applied to the data inputs.

DON'T CARE

Figure 14
READ TO WRITE (OR BLOCK WRITE) WITH EXTRA CLOCK CYCLE

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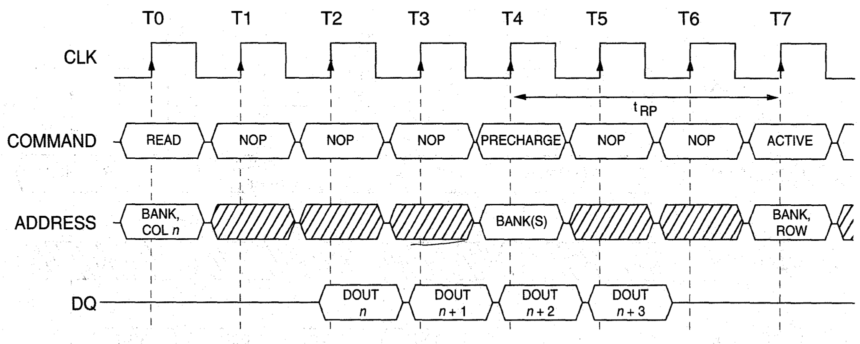
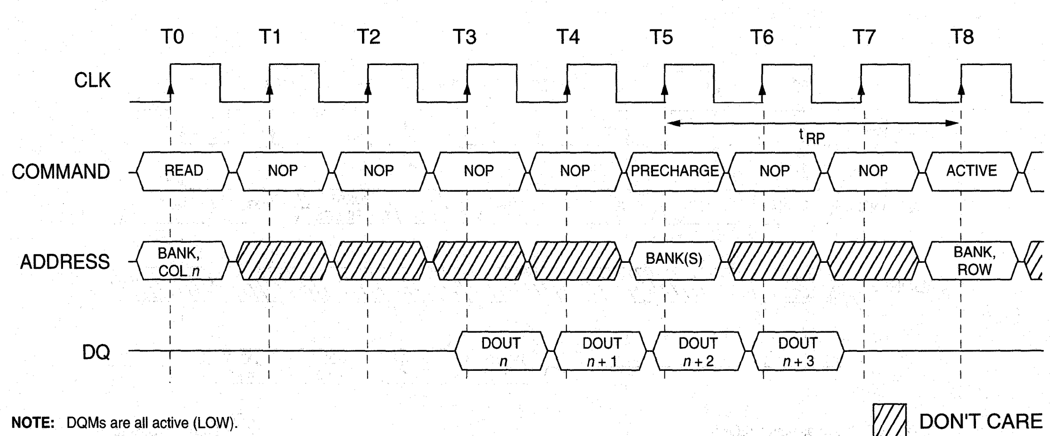
A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated) and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued one cycle before the clock edge at which the last desired data element is valid. This is shown in Figure 15 for a read latency of two and Figure 16 for a read latency of three; data element $n + 3$ is either the last of a burst of four, or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^tRP is met. Note that part of the row precharge time is hidden during the access of the last data element.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst



NOTE: DQMs are all active (LOW).

Figure 15
READ TO PRECHARGE, READ LATENCY OF TWO



NOTE: DQMs are all active (LOW).

DON'T CARE

Figure 16
READ TO PRECHARGE, READ LATENCY OF THREE

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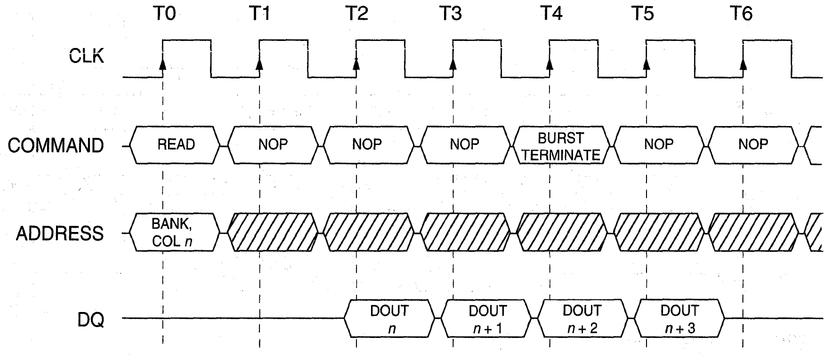
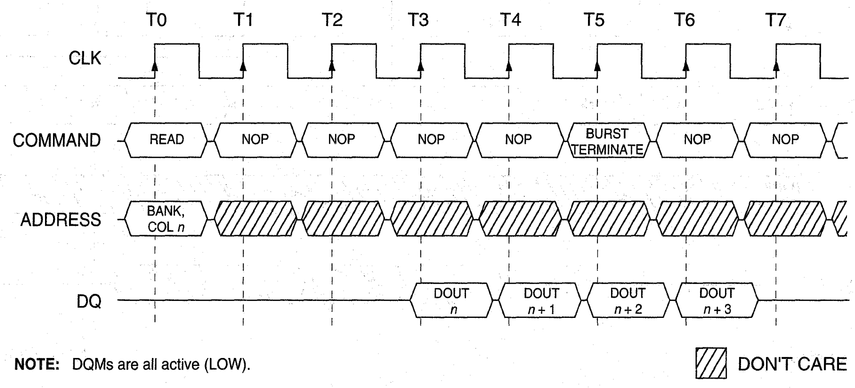
with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is it requires that the command and address busses be available at the appropriate time to issue the command, but the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. The AUTO PRECHARGE command does not truncate fixed-length bursts and does not apply to full page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto-precharge was not activated. When truncating a READ burst, the BURST TERMINATE command should be issued 1 cycle before the clock edge at which the last desired data element is valid. This is shown in Figure 17 for a read latency of two and Figure 18 for a read latency of three; data element $n + 3$ is either the last of a burst of four, or the last desired of a longer burst.



NOTE: DQMs are all active (LOW).

Figure 17
TERMINATING A READ BURST, READ LATENCY OF TWO



NOTE: DQMs are all active (LOW).

DON'T CARE

Figure 18
TERMINATING A READ BURST, READ LATENCY OF THREE

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WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 19.

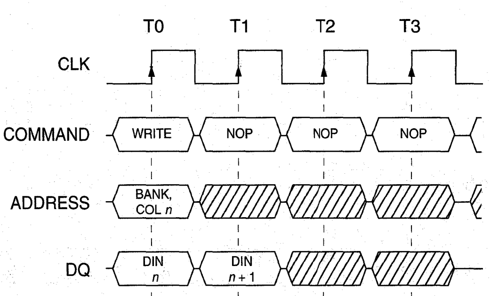
The starting column and bank addresses are provided with the WRITE command, normal or BLOCK WRITE is selected, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is precharged at the completion of the burst. BLOCK WRITEs are covered later in this section. For the generic WRITE commands used in the following illustrations, AUTO PRECHARGE is disabled, and all WRITEs are normal WRITEs unless noted.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional input data will be ignored (see Figure 20). A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

A fixed-length WRITE burst may be followed by, or truncated with, a subsequent WRITE burst or BLOCK WRITE command (provided that AUTO PRECHARGE was not activated) and a full page WRITE burst can be truncated with a subsequent WRITE burst or BLOCK WRITE command. The new WRITE or BLOCK WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 21. Data $n + 1$ is either the last of a burst of two, or the last desired of a longer burst. The SGRAM does

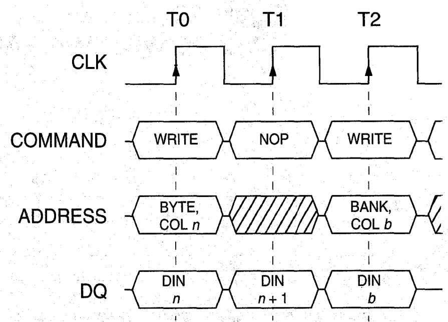
CLK
CKE HIGH
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
DSF: BLOCK WRITE / NORMAL WRITE
A0-A7: COLUMN ADDRESS
A8: ENABLE AUTO-PRECHARGE / DISABLE AUTO-PRECHARGE
BA: BANK 1 / BANK 0

Figure 19
WRITE COMMAND



NOTE: Burst Length = 2.
DQMs are all active (LOW).

Figure 20
WRITE BURST



NOTE: DQMs are all active (LOW). The second WRITE can be a BLOCK WRITE, in which case column/byte mask data would be applied to the data inputs.

DON'T CARE

Figure 21
WRITE TO WRITE (OR BLOCK WRITE)

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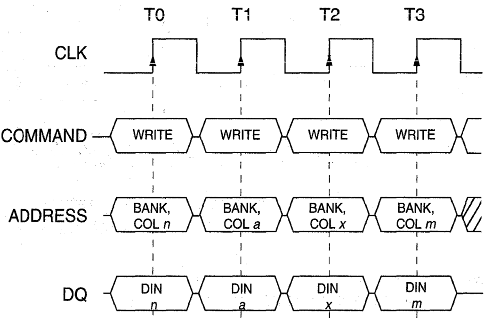
not require the 2*n* rule of prefetch architectures, so a WRITE command can be initiated on any clock cycle following a previous WRITE command. Full speed random write accesses within a page can be performed as shown in Figure 22.

A fixed-length WRITE burst may be followed by, or truncated with, a subsequent READ burst (provided that AUTO PRECHARGE was not activated) and a full-page WRITE burst can be truncated with a subsequent READ burst. Once the READ command is registered, the data inputs will be ignored, and writes will not be executed. An example is shown in Figure 23. Data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst.

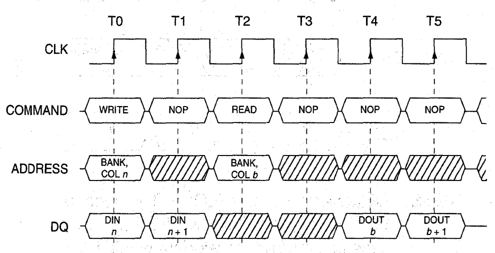
A fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that AUTO PRECHARGE was not activated) and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *y* cycles after the clock edge at which the last desired input data element is registered, where *y* equals $^tWR/^tCK$ rounded up to the next whole number. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last desired data element and ending with the clock edge on which the PRECHARGE command is entered. An example is shown in Figure 24. Data *n* + 1 is either the last of a burst of two, or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^tRP is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with AUTO PRECHARGE. The disadvantage of the PRECHARGE command is it requires that the command and address busses be available at the appropriate time to issue the command, but the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. The AUTO PRECHARGE command does not truncate fixed-length bursts and does not apply to full page bursts.



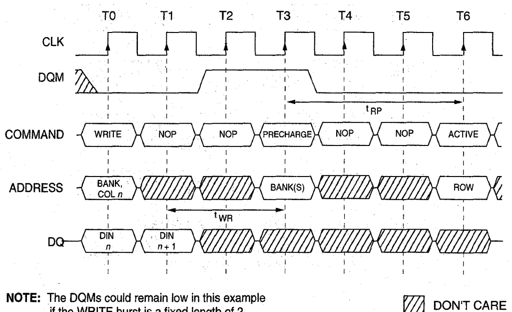
NOTE: Covers either successive WRITEs to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW).

Figure 22
RANDOM WRITE CYCLES WITHIN A PAGE



NOTE: Covers either a WRITE and READ to the active row in a given bank, or to the active rows in different banks. DQMs are all active (LOW). READ LATENCY = 2 for illustration.

Figure 23
WRITE TO READ



NOTE: The DQMs could remain low in this example if the WRITE burst is a fixed length of 2.

Figure 24
WRITE TO PRECHARGE

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Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied one clock edge prior to the BURST TERMINATE command will be the last data written. This is shown in Figure 25, where data $n + 1$ is either the last of a burst of two, or the last desired of a longer burst.

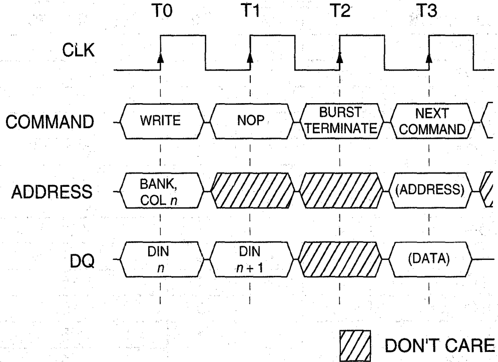

Figure 25
TERMINATING A WRITE BURST

MASKED WRITES

Any WRITE performed to a row that was opened via an ACTIVE with WPB command is a MASKED WRITE (Write-Per-Bit). Data is written to the 32 cells (bits) at the selected column location subject to the mask stored in the WPB mask register. If a particular bit in the WPB mask register is a "0", the data appearing on the corresponding DQ input will be ignored, and the existing data in the corresponding DRAM cell will remain unchanged. If a mask bit is a "1", the data appearing on the corresponding DQ input will be written to the corresponding DRAM cell.

The overall WRITE mask consists of a combination of the DQM inputs, which mask on a per-byte basis, and the WPB mask register, which masks on a per-bit basis. This is shown in Figure 26. If a particular DQM signal was registered HIGH, the corresponding byte will be masked. A given bit is written only if the corresponding DQM signal registered is "0" and the corresponding WPB mask register bit is "1".

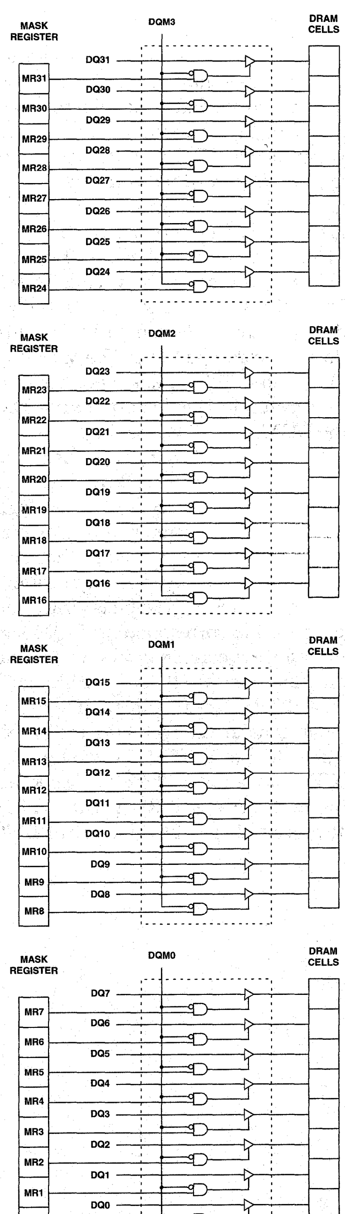

Figure 26
WRITE MASKING – FUNCTIONAL REPRESENTATION

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BLOCK WRITES

BLOCK WRITEs are non-burst accesses that write to eight column locations simultaneously. A single data value, which was previously loaded in the color register, is written to the block of eight consecutive column locations addressed by inputs A3-A7. The information on the DQs which is registered coincident with the BLOCK WRITE command is used to mask specific column/byte combinations within the block. The mapping of the DQ inputs to the column/byte combinations is shown in Table 3.

When a "0" is registered on a particular DQ signal coincident with a BLOCK WRITE command, the write to the corresponding column/byte combination is masked (the existing data in the corresponding DRAM cells will remain unchanged). When a "1" is registered, the color register data will be written to the corresponding DRAM cells, subject to the DQM and WPB masking.

The overall BLOCK WRITE mask consists of a combination of the DQM signals, the WPB mask register and the column/byte mask information, as shown in Figure 27. The DQM and WPB mask register masking operates as for normal WRITEs, with the exception that the mask information is applied simultaneously to all eight columns. Therefore, in a BLOCK WRITE, a given bit is written only if a "0" was registered for the corresponding DQM signal, a "1" was registered for the corresponding DQ signal, and the corresponding bit in the WPB mask register is "1".

A BLOCK WRITE access requires a time period of ^{t}BWC to execute, so in general, the cycle after the BLOCK WRITE command should be a NOP. However, ACTIVE or PRECHARGE commands to the other bank are allowed. When following a BLOCK WRITE with a PRECHARGE command to the same bank, ^{t}BPL (instead of ^{t}BWC) must be met.

Table 3
MAPPING OF DQs TO COLUMN/BYTE LOCATIONS WITHIN A BLOCK

DQ INPUTS	COLUMN-ADDRESS CONTROLLED			DQ PLANES CONTROLLED
	A2	A1	A0	
DQ0	0	0	0	0-7
DQ1	0	0	1	0-7
DQ2	0	1	0	0-7
DQ3	0	1	1	0-7
DQ4	1	0	0	0-7
DQ5	1	0	1	0-7
DQ6	1	1	0	0-7
DQ7	1	1	1	0-7
DQ8	0	0	0	8-15
DQ9	0	0	1	8-15
DQ10	0	1	0	8-15
DQ11	0	1	1	8-15
DQ12	1	0	0	8-15
DQ13	1	0	1	8-15
DQ14	1	1	0	8-15
DQ15	1	1	1	8-15
DQ16	0	0	0	16-23
DQ17	0	0	1	16-23
DQ18	0	1	0	16-23
DQ19	0	1	1	16-23
DQ20	1	0	0	16-23
DQ21	1	0	1	16-23
DQ22	1	1	0	16-23
DQ23	1	1	1	16-23
DQ24	0	0	0	24-31
DQ25	0	0	1	24-31
DQ26	0	1	0	24-31
DQ27	0	1	1	24-31
DQ28	1	0	0	24-31
DQ29	1	0	1	24-31
DQ30	1	1	0	24-31
DQ31	1	1	1	24-31

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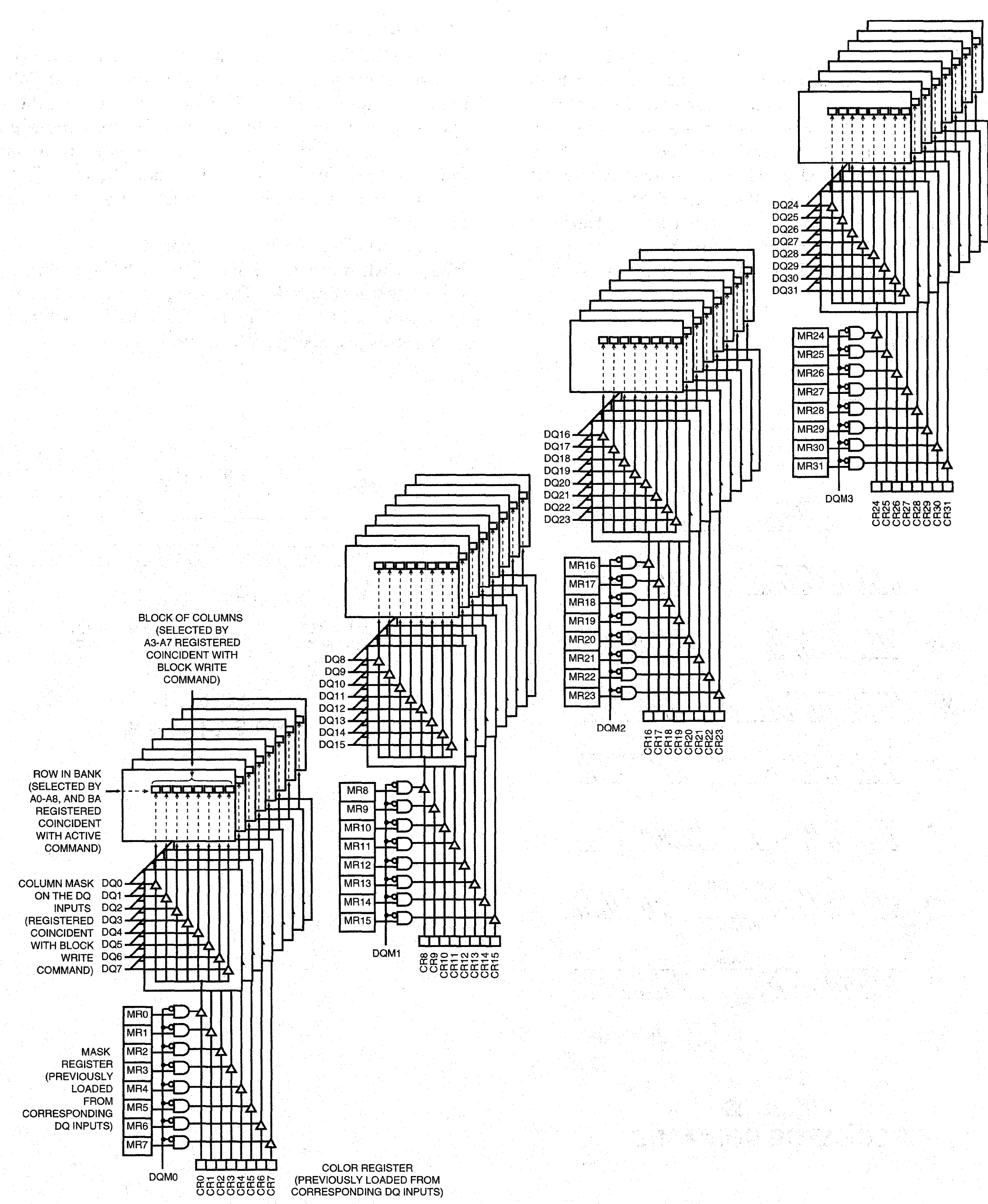

Figure 27
BLOCK WRITE MASKING – FUNCTIONAL REPRESENTATION

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PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank, or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the precharge command is issued. Input A8 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as a "don't care". Once a bank has been precharged, it is in the idle state and must be activated prior to any READ, WRITE or BLOCK WRITE commands being issued to that bank.

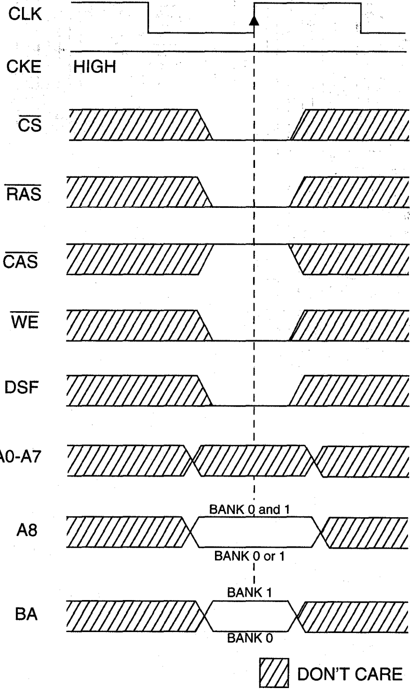

Figure 28
PRECHARGE COMMAND

POWER-DOWN

POWER-DOWN occurs when both banks are in the idle state (precharged) and CKE is registered LOW (see Figure 29). Entering POWER-DOWN deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the POWER-DOWN state longer than the refresh period (17ms) since the command does not perform any refresh operations.

The POWER-DOWN state is exited by taking CKE back HIGH. CKE must go HIGH ^{t}CKS before a positive clock edge, after meeting ^{t}CKH from the previous clock edge. The first command after exiting POWER-DOWN will be registered on the clock edge following ^{t}CKS.

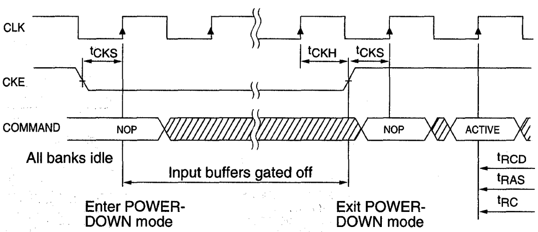

Figure 29
POWER-DOWN

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TRUTH TABLE 2 – CKE

(Notes 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMMAND_n$	$ACTION_n$	NOTES
L	L	POWER-DOWN	X	Maintain POWER-DOWN	
		SELF REFRESH	X	Maintain SELF REFRESH	6
L	H	POWER-DOWN	COMMAND INHIBIT or NOP	Exit POWER-DOWN	7
		SELF REFRESH	COMMAND INHIBIT or NOP	Exit SELF REFRESH	6, 8
H	L	Both Banks Idle	COMMAND INHIBIT or NOP	POWER-DOWN Entry	
		Both Banks Idle	AUTO REFRESH	SELF REFRESH Entry	5
H	H	See Truth Table 3			

NOTE:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. CURRENT STATE is the state of the SGRAM immediately prior to clock edge n.
3. $COMMAND_n$ is the command registered at clock edge n and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Illegal on non "S" devices.
6. Not available on non "S" devices.
7. Exiting POWER-DOWN at clock edge n will put the device in the "all banks idle" state in time for clock edge n+1.
8. Exiting SELF REFRESH at clock edge n will put the device in the "all banks idle" state once ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occuring during the ^tXSR period.

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TRUTH TABLE 3 – Current State

(Notes 1-3; notes appear on next page)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	COMMAND/ACTION	NOTES
Any	H	X	X	X	X	COMMAND INHIBIT (NOP/ continue previous operation)	
	L	H	H	H	L	NO OPERATION (NOP/ continue previous operation)	
Idle	L	L	H	H	L	ACTIVE (Select bank and activate row)	
	L	L	H	H	H	ACTIVE w/WPB (Select bank, activate row and WPB)	
	L	L	L	H	L	AUTO REFRESH	5
	L	L	L	L	L	LOAD MODE REGISTER	5
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER	6
Row Active	L	H	L	H	L	READ (Select bank and column and start READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access	7
	L	L	H	L	L	PRECHARGE (Deactivate row in bank or banks)	8
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER	6
READ (AUTO-PRECHARGE DISABLED)	L	H	L	H	L	READ (Select bank and column and start new READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	7
	L	L	H	L	L	PRECHARGE (Truncate READ burst, start precharge)	8
	L	H	H	L	L	BURST TERMINATE	9
WRITE (AUTO-PRECHARGE DISABLED)	L	H	L	H	L	READ (Select bank and column and start READ burst)	7
	L	H	L	L	L	WRITE (Select bank and column and start new WRITE burst)	7
	L	H	L	L	H	BLOCK WRITE (Select bank & column and start BLOCK WRITE access)	7
	L	L	H	L	L	PRECHARGE (Truncate WRITE burst, start precharge)	8
	L	H	H	L	L	BURST TERMINATE	9

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NOTE:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was SELF REFRESH).
2. This table is bank specific, except where noted; i.e., the CURRENT STATE is for a specific bank and the commands shown are those allowed to be issued to that bank, when in that state. Exceptions are covered in the notes below.
3. CURRENT STATE definitions:
   - Idle: the bank has been precharged and ^tRP has been met.
   - Row Active: a row in the bank has been activated and ^tRCD has been met. No data bursts/ accesses and no register accesses are in progress.
   - Read: a READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   - Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occuring during these states. Allowable commands to the other bank are determined by it's CURRENT STATE; refer to Truth Table 3 and these notes.
   - Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. Once ^tRP is met, the bank will be in the Idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the Row Active state.
   - Read/Precharge: Starts with registration of a READ command with AUTO PRECHARGE enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the Idle state.
   - Write/Precharge: Starts with registration of a WRITE command with AUTO PRECHARGE enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the Idle state.
   - Block Write/ Precharge: Starts with registration of a BLOCK WRITE command with AUTO PRECHARGE enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the Idle state.
   - Block Write: Starts with registration of a BLOCK WRITE command and ends when either ^tBPL or ^tBWC has been met. ^tBPL applies when the BLOCK WRITE is to be followed by a PRECHARGE and ^tBWC applies when it is to be followed by any other allowable command. Once ^tBWC is met, the bank will be in the Row Active state.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^tRC is met. Once ^tRC is met, the SGRAM will be in the "all banks idle" state.
   - Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command, and ends when ^tMTC has been met. Once ^tMTC is met, the SGRAM will be in the "all banks idle" state.
   - Accessing Special Mode Register: Starts with registration of a LOAD SPECIAL MODE REGISTER command, and ends when ^tSML has been met.
5. Requires that both banks are idle.
6. Requires that the other bank is either idle or in the Row Active state.
7. READ, WRITE and BLOCK WRITE accesses will interact between banks as they do within a bank.
8. If both banks are to be precharged, both must be in a valid state for precharging.
9. BURST TERMINATE is not bank specific; it affects the most recent READ or WRITE burst, regardless of bank.

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NEW SGRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc/VccQ supply relative to Vss. -1V to +4.6V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note: 1) (0°C ≤ T_A ≤ 70°C; Vcc/VccQ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc/VccQ	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs	VIL	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	II	-1	1	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ 3.6V)	IOZ	-2	2	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

Icc SPECIFICATIONS AND CONDITIONS

(Note: 1) (0°C ≤ T_A ≤ 70°C; Vcc/VccQ = +3.3V ±0.3V)

		MAX				
PARAMETER/CONDITION	SYMBOL	-10	-12	-15	UNITS	NOTES
SELF REFRESH CURRENT: CKE ≤ 0.2V (S version only)	ICC1 (S only)	TBD	TBD	TBD	µA	5
STANDBY CURRENT: POWER-DOWN mode, CKE ≤ VIL (MAX), both banks idle	ICC2	TBD	TBD	TBD	mA	
	ICC2 (S only)	TBD	TBD	TBD	µA	
STANDBY CURRENT: $\overline{CS}$ ≥ VIH (MIN), tCK ≥ tCK (MIN), CKE ≥ VIH (MIN), both banks idle	ICC3	TBD	TBD	TBD	mA	3, 4, 13
STANDBY CURRENT: $\overline{CS}$ ≥ VIH (MIN), tCK ≥ tCK (MIN), CKE ≥ VIH (MIN), both banks active after tRCD met	ICC4	TBD	TBD	TBD	mA	3, 4, 13
AUTO REFRESH CURRENT (tRC = 16.6µs)	ICC5	TBD	TBD	TBD	mA	4
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, tRC ≥ tRC (MIN), one bank active	ICC6	TBD	TBD	TBD	mA	3, 4
OPERATING CURRENT: ACTIVE mode, burst = 2, READ or WRITE, tRC ≥ tRC (MIN), two banks active	ICC7	TBD	TBD	TBD	mA	3, 4
OPERATING CURRENT: BURST mode, full-page burst after tRCD met READ or WRITE, tCK ≥ tCK (MIN), other bank idle	ICC8	TBD	TBD	TBD	mA	3, 4

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CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8, BA	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CLK, CKE, $\overline{CS}$, DSF	C_{I2}	5	pF	2
Input/Output Capacitance: DQs	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 8, 9, 10, 12) (0°C ≤ T_A ≤ +70°C) Listed alphabetically by symbol subscript.

AC CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	^tAC		9		11		13	ns	
Address hold time	^tAH	1		1.5		2		ns	
Address setup time	^tAS	3		3.5		4		ns	
BLOCK WRITE to PRECHARGE delay	^tBPL	30		36		45		ns	
BLOCK WRITE cycle time	^tBWC	20		24		30		ns	
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM hold time	^tCH	1		1.5		2		ns	
CLK high level width	^tCHI	3.5		4		5		ns	
System clock cycle time	^tCK	10		12		15		ns	
CKE hold time	^tCKH	1		1.5		2		ns	
CKE setup time	^tCKS	3		3.5		4		ns	
CLK low level width	^tCL	3.5		4		5		ns	
$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM setup time	^tCS	3		3.5		4		ns	
Data-in hold time	^tDH	1		1.5		2		ns	
Data-in setup time	^tDS	3		3.5		4		ns	
Data-out high-impedance time	^tHZ	4	10	4	10	4	10	ns	11
Data-out low-impedance time	^tLZ	3		3		3		ns	
LOAD MODE REGISTER command to command	^tMTC	2		2		2		^tCK	
Data-out hold time	^tOH	4		4		4		ns	
ACTIVE to PRECHARGE command period	^tRAS	60	120K	72	120K	90	120K	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period	^tRC	100		100		110		ns	
ACTIVE to READ, WRITE or BLOCK WRITE delay	^tRCD	30		36		45		ns	
Refresh period (1,024 cycles)	^tREF		17		17		17	ms	7
PRECHARGE command period	^tRP	30		36		45		ns	
ACTIVE bank A to ACTIVE bank B command period	^tRRD	30		36		45		ns	
LOAD SPECIAL MODE REGISTER command to command	^tSML	2		2		2		^tCK	
Transition time	^tT	1	30	1	30	1	30	ns	
Write recovery time	^tWR	15		15		15		ns	
Exit SELF REFRESH to ACTIVE command	^tXSR	100		100		110		ns	

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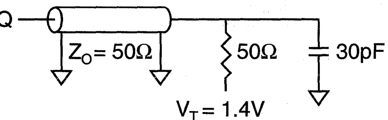
NEW SGRAM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc/VccQ = +3.3V±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands before proper device operation is assured. The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 1ns.
9. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. Outputs measured at 1.4V with equivalent load:



11. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
12. AC timing tests have V_{IL} = 0V and V_{IH} = 3.0V with timing referenced to 1.4V crossover point.
13. All other inputs at CMOS levels.

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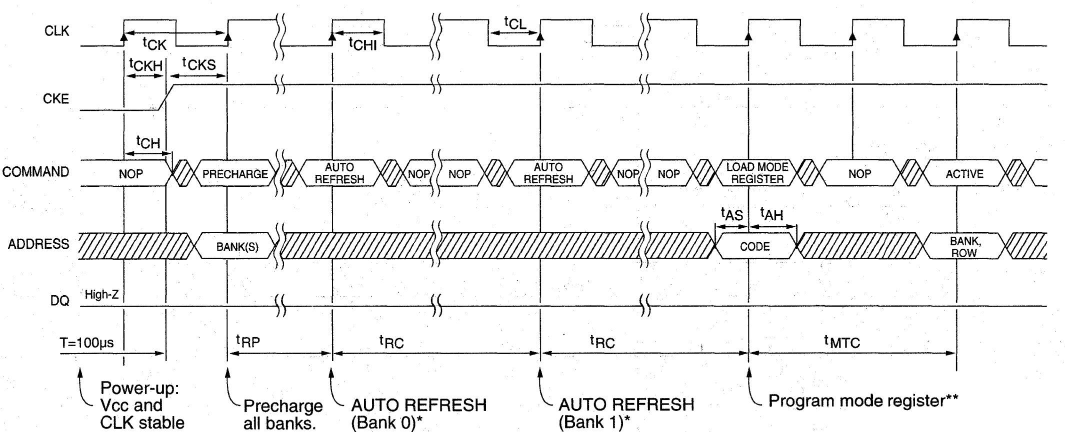
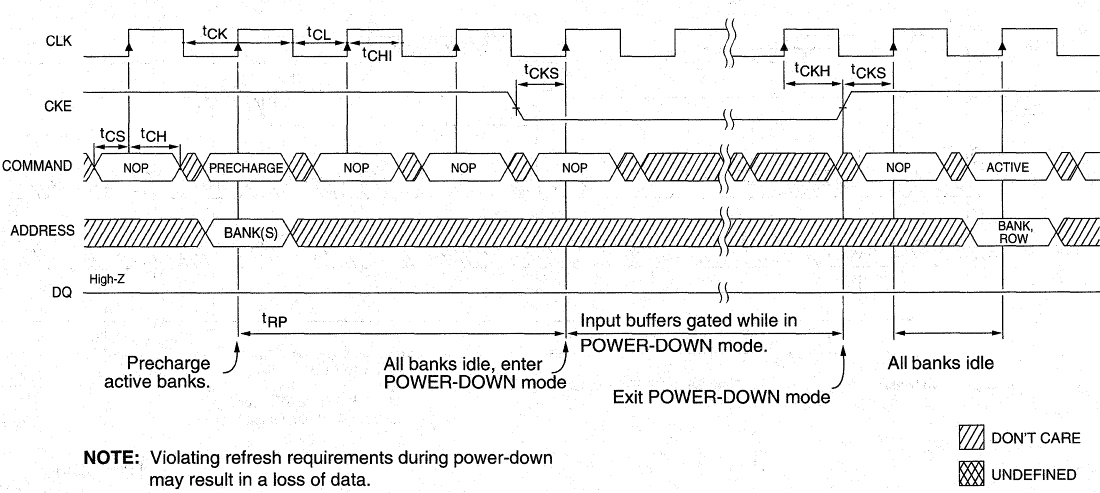
INITIALIZE AND LOAD MODE REGISTER



*Starts at Bank 0 and alternates banks.

**The mode register may be loaded prior to the AUTO REFRESH cycles if desired.

POWER-DOWN MODE



NOTE: Violating refresh requirements during power-down may result in a loss of data.

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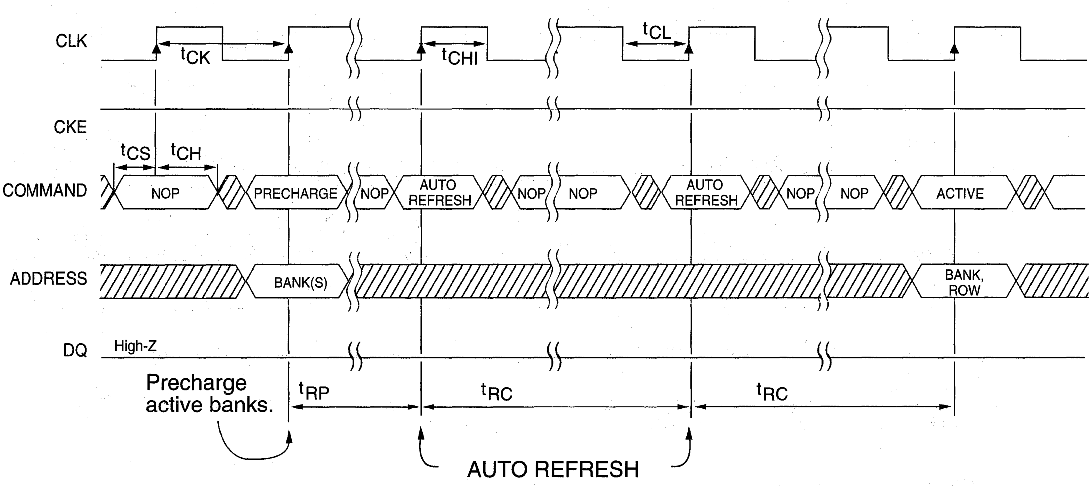
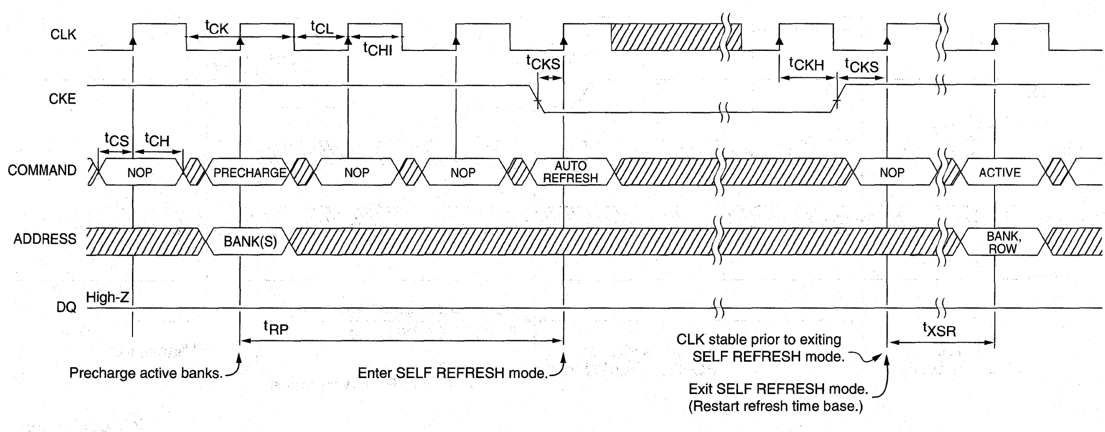
NEW SGRAM

AUTO REFRESH MODE



SELF REFRESH MODE



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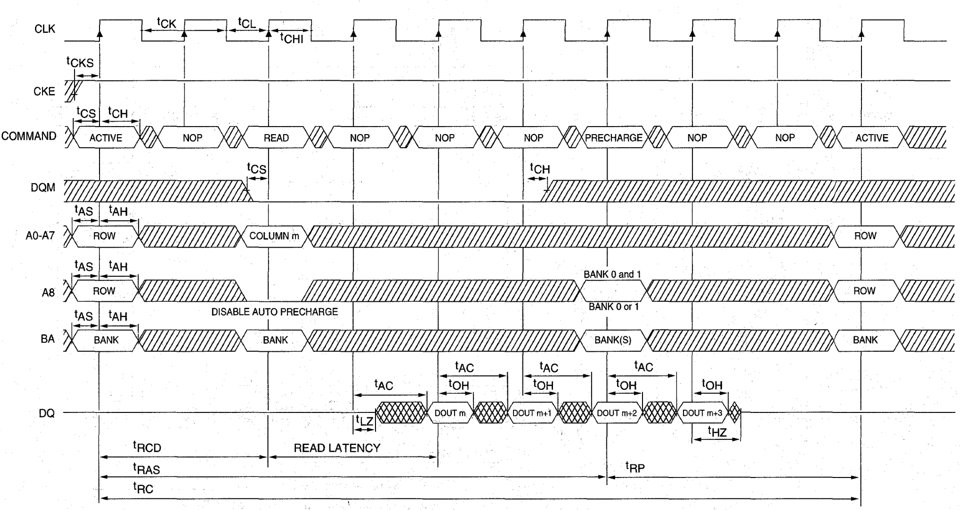
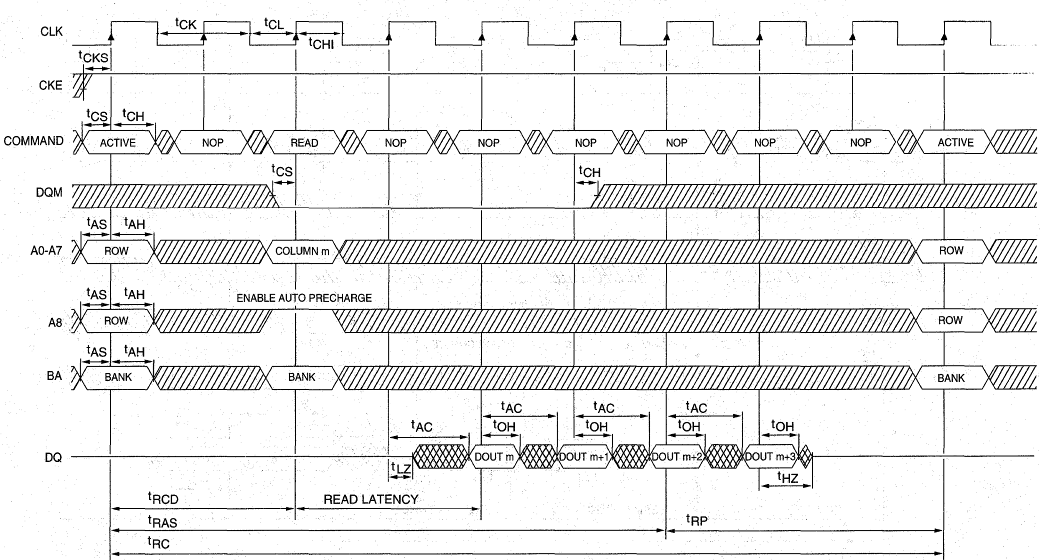
READ – WITHOUT AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4, the READ LATENCY = 2 and the READ burst is followed by a "manual" PRECHARGE.

READ – WITH AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4, and the READ LATENCY = 2.

DON'T CARE

UNDEFINED

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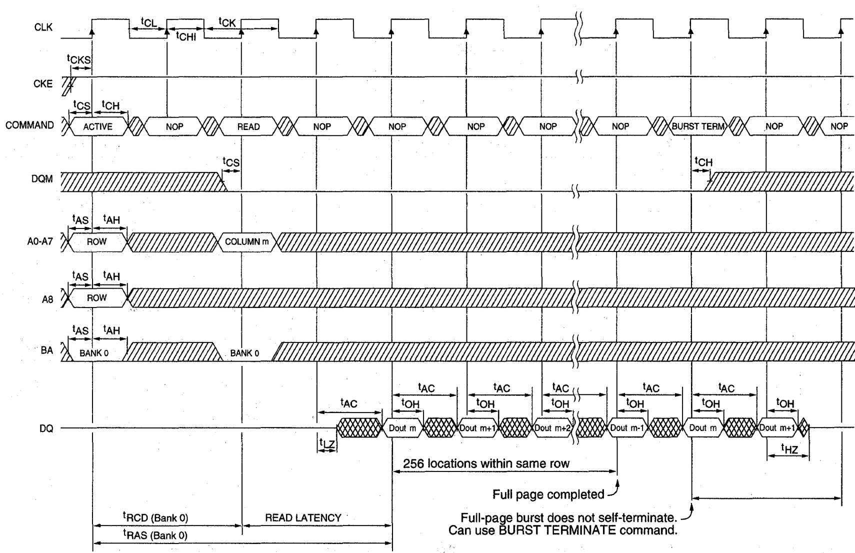
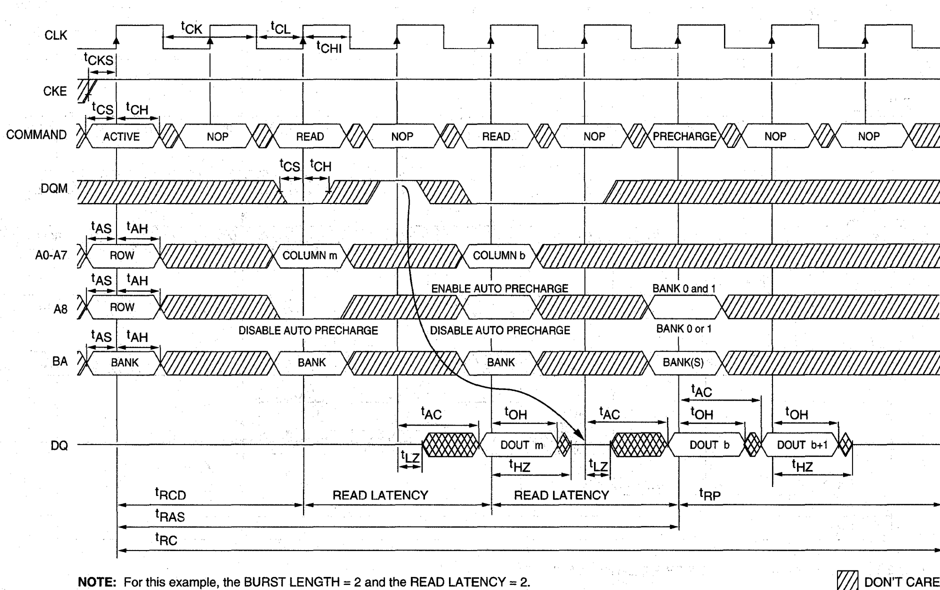
READ – FULL-PAGE BURST



NOTE: For this example, BANK 0 is being accessed and the READ LATENCY = 2.

READ – DQM OPERATION



NOTE: For this example, the BURST LENGTH = 2 and the READ LATENCY = 2.

DON'T CARE

UNDEFINED

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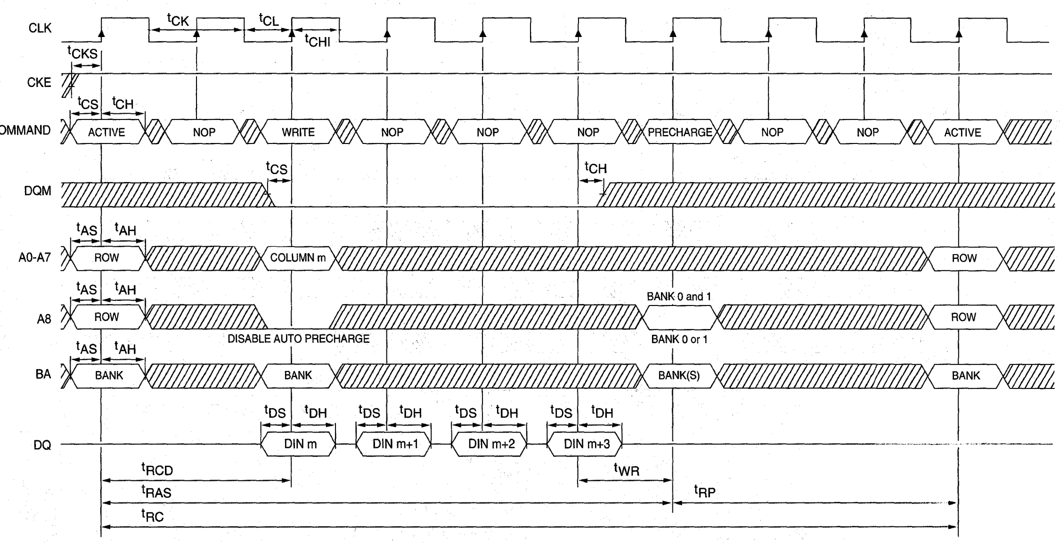
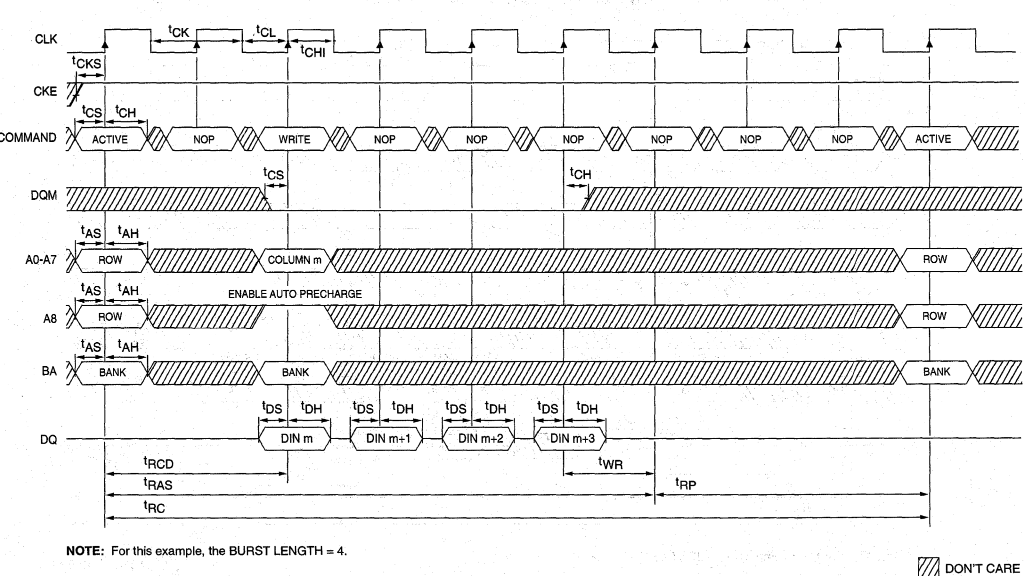
WRITE – WITHOUT AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4 and the WRITE burst is followed by a "manual" PRECHARGE.

WRITE – WITH AUTO PRECHARGE



NOTE: For this example, the BURST LENGTH = 4.

DON'T CARE

UNDEFINED

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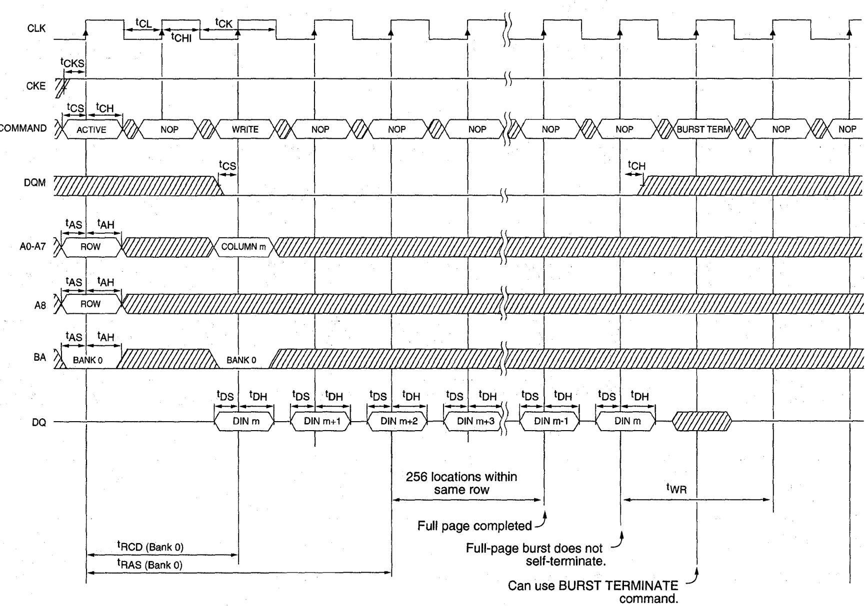
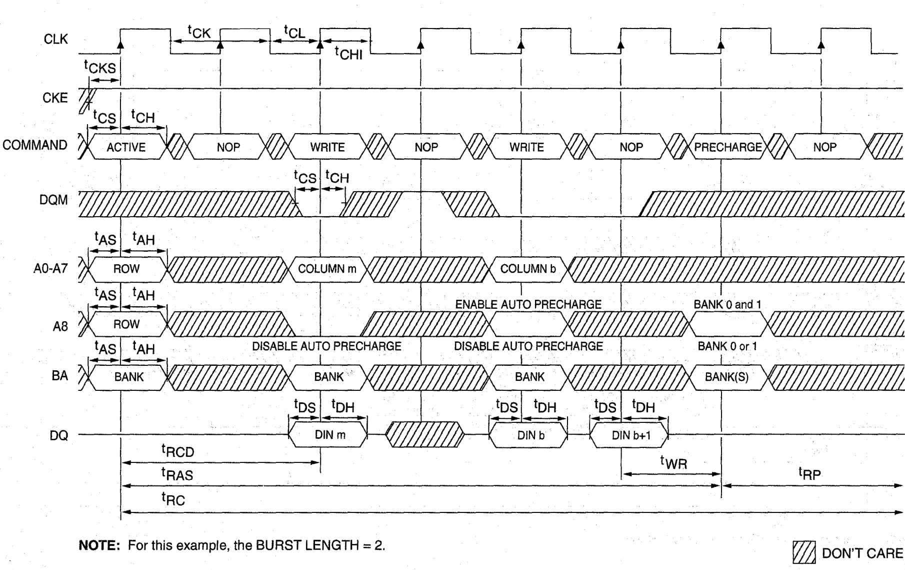
WRITE – FULL-PAGE BURST



NOTE: For this example, BANK 0 is being accessed.

WRITE – DQM OPERATION



NOTE: For this example, the BURST LENGTH = 2.

DON'T CARE
UNDEFINED

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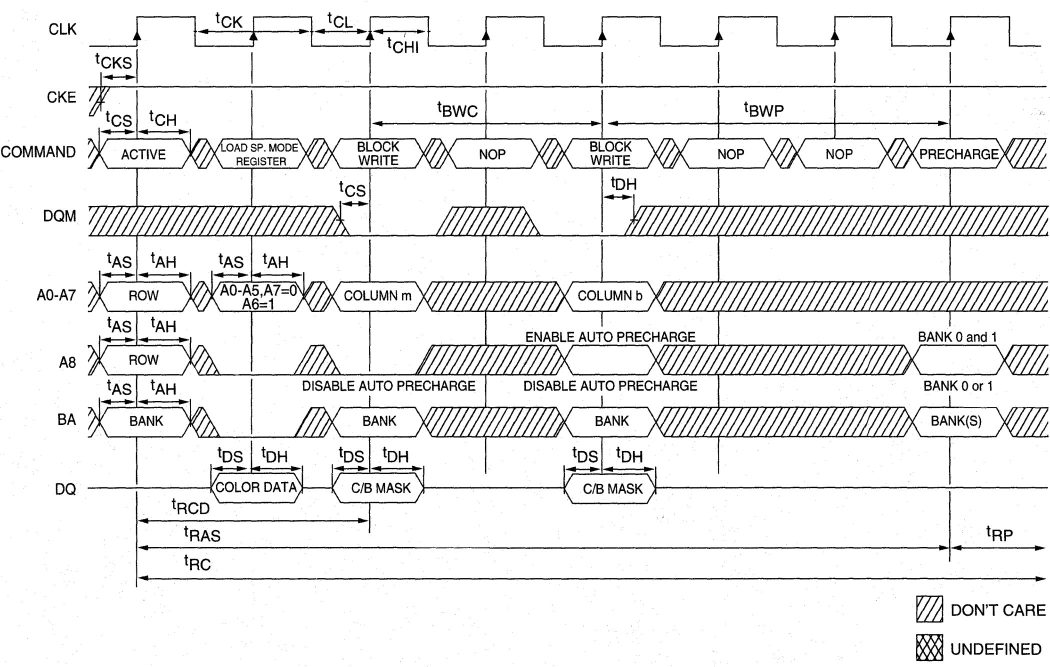
BLOCK WRITE



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MICRON TECHNOLOGY, INC.

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DRAM SIMM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Optional Access Cycle	Access Time (ns)	Typical Power Dissipation		No. of Pins SIMM	Page
					Standby	Active		
3.3V SIMMs								
1 Meg x 32	3.3V	MT8LD(T)132		60, 70, 80	9.6mW	800mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 S	S	60, 70, 80	2.4mW	800mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 X	EDO	60, 70, 80	8mW	920mW	72	4-77
1 Meg x 32	3.3V	MT8LD(T)132 XS	EDO, S	60, 70, 80	2mW	920mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232		60, 70, 80	19.2mW	810mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 S	S	60, 70, 80	4.8mW	802mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 X	EDO	60, 70, 80	16mW	928mW	72	4-77
2 Meg x 32	3.3V	MT16LD(T)232 XS	EDO, S	60, 70, 80	4mW	922mW	72	4-77
2 Meg x 32	3.3V	MT4LD232		60, 70	4mW	800mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 S	S	60, 70	1.2mW	800mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 X	EDO	60, 70	4mW	600mW	72	4-99
2 Meg x 32	3.3V	MT4LD232 XS	EDO, S	60, 70	1.2mW	600mW	72	4-99
4 Meg x 32	3.3V	MT8LD432		60, 70	8mW	1,440mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 S	S	60, 70	2.4mW	1,440mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 X	EDO	60, 70	8mW	1,200mW	72	4-133
4 Meg x 32	3.3V	MT8LD432 XS	EDO, S	60, 70	3.2mW	1,200mW	72	4-133
8 Meg x 32	3.3V	MT16LD832		60, 70	16mW	1,408mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 S	S	60, 70	4.8mW	1,442mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 X	EDO	60, 70	16mW	1,208mW	72	4-133
8 Meg x 32	3.3V	MT16LD832 XS	EDO, S	60, 70	6.4mW	1,203mW	72	4-133
5V SIMMs								
1 Meg x 8	5V	MT2D18		60, 70	6mW	450mW	30	4-1
4 Meg x 8	5V	MT2D48		60, 70	6mW	500mW	30	4-11
4 Meg x 8	5V	MT8D48		60, 70	24mW	1,800mW	30	4-21
4 Meg x 9	5V	MT3D49		60, 70	9mW	725mW	30	4-31
4 Meg x 9	5V	MT9D49		60, 70	27mW	2,025mW	30	4-41
256K x 32	5V	MT2D25632		60, 70	6mW	750mW	72	4-51
512K x 32	5V	MT4D51232		60, 70	12mW	756mW	72	4-51
1 Meg x 32	5V	MT8D132		60, 70	24mW	1,800mW	72	4-63
1 Meg x 32	5V	MT8D132 S	S	60, 70	24mW	1,800mW	72	4-63
2 Meg x 32	5V	MT16D232		60, 70	48mW	1,824mW	72	4-63
2 Meg x 32	5V	MT16D232 S	S	60, 70	48mW	1,824mW	72	4-63
4 Meg x 32	5V	MT8D432		60, 70	24mW	2,000mW	72	4-119
4 Meg x 32	5V	MT8D432 S	S	60, 70	2.4mW	1,440mW	72	4-119
8 Meg x 32	5V	MT16D832		60, 70	48mW	2,024mW	72	4-119
8 Meg x 32	5V	MT16D832 S	S	60, 70	4.8mW	1,443mW	72	4-119
1 Meg x 36	5V	MT9D136		60, 70	27mW	2,025mW	72	4-155
2 Meg x 36	5V	MT18D236		60, 70	54mW	2,052mW	72	4-155
4 Meg x 36	5V	MT12D436		60, 70	36mW	2,500mW	72	4-167
4 Meg x 36	5V	MT12D436 S	S	60, 70	3.6mW	2,340mW	72	4-167
8 Meg x 36	5V	MT24D836		60, 70	72mW	2,536mW	72	4-167
8 Meg x 36	5V	MT24D836 S	S	60, 70	7.2mW	2,348mW	72	4-167

S = SELF REFRESH; EDO = Extended Data-Out

DRAM MODULE

1 MEG x 8

1 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 450mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE (FPM) access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
30-pin SIMM	M

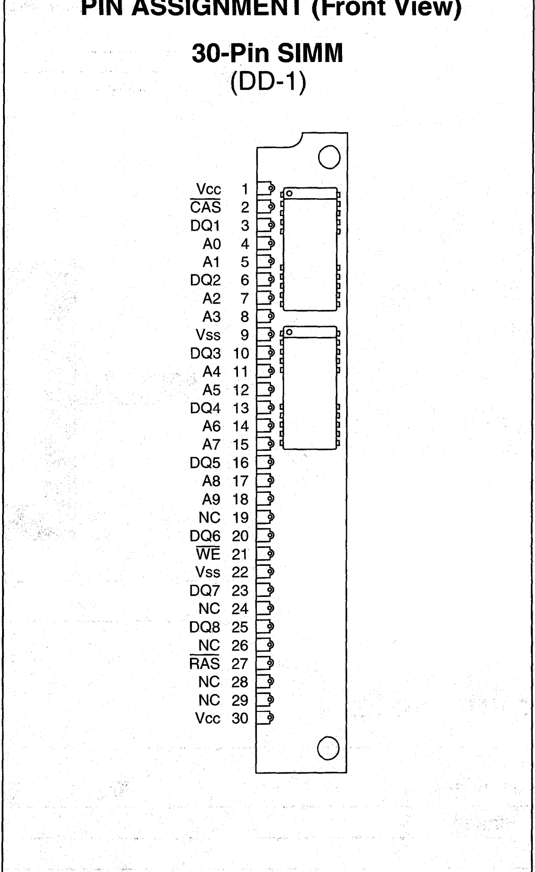
- Part Number Example: MT2D18M-6

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

30-Pin SIMM
(DD-1)



GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Early WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles.

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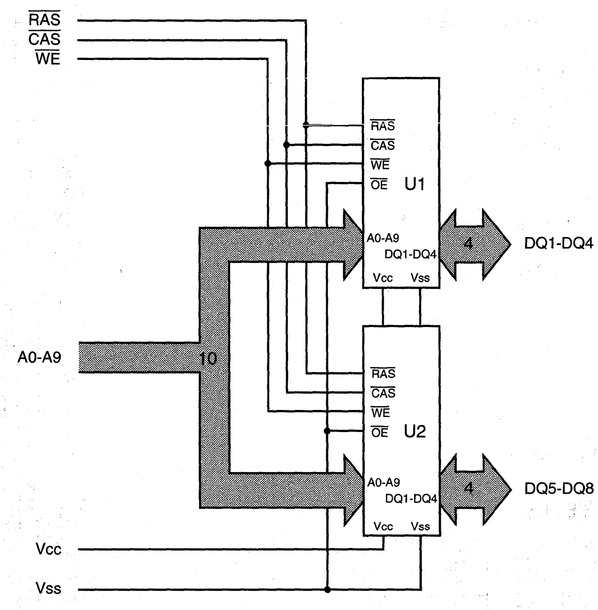
REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4001JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DATA-IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	A0-A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I_I	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low (Logic 0) Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	220	200	mA	2, 26, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	160	140	mA	2, 26, 28
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	220	200	mA	26, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	220	200	mA	19, 26

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		13	pF	17
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	C_{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20	s	9
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	0		0		ns	
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		ns	18
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	19
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	15
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	15
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	12, 27
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a	21
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	8
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	22
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	24
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	24
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	23
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	23

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DRAM SIMM

NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that ^tRCD ≥ ^tRCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1 and U2.
22. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
23. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
24. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
25. All other inputs at Vcc -0.2V.
26. Icc is dependent on cycle rates.
27. The 3ns minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.

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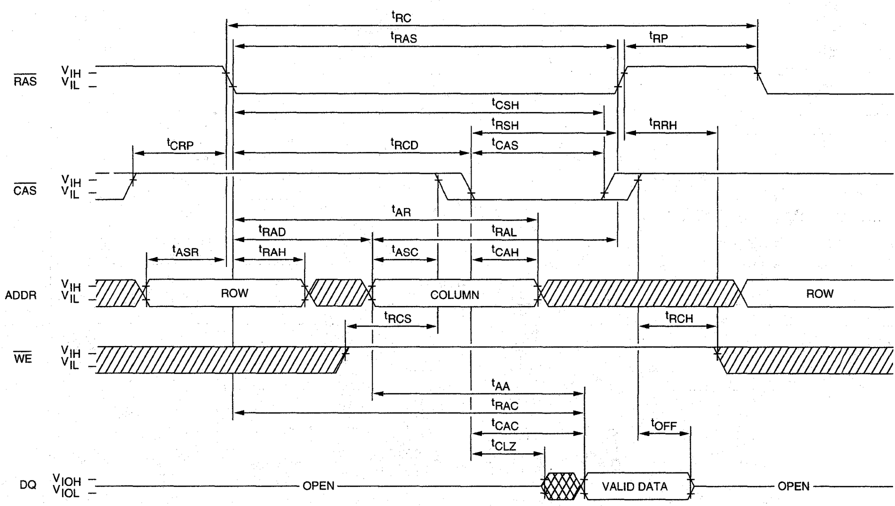
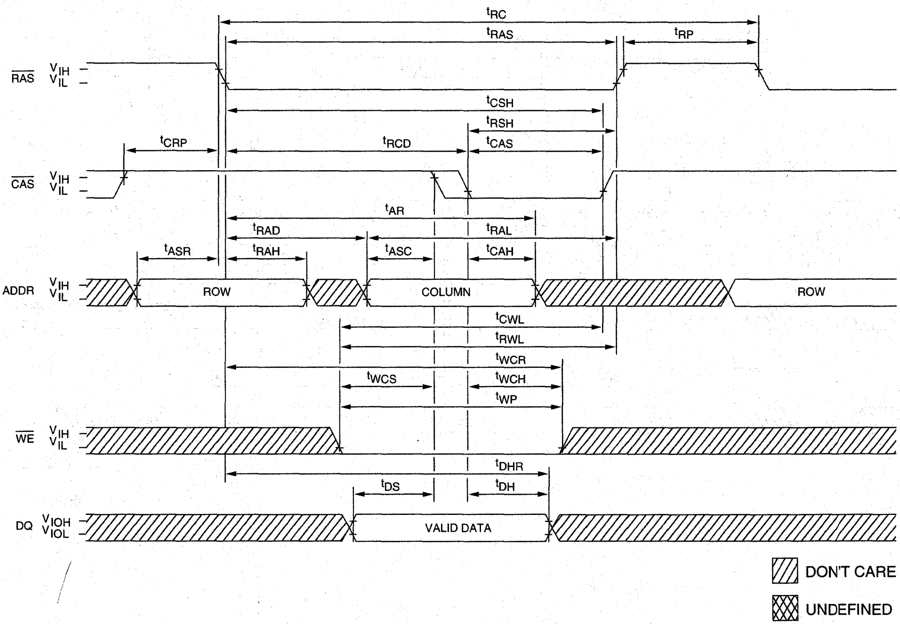
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

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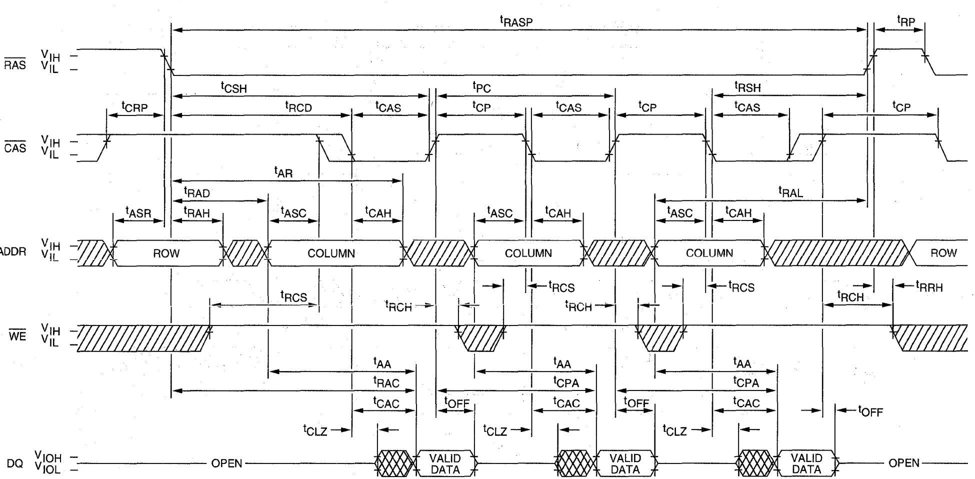
FAST-PAGE-MODE READ CYCLE



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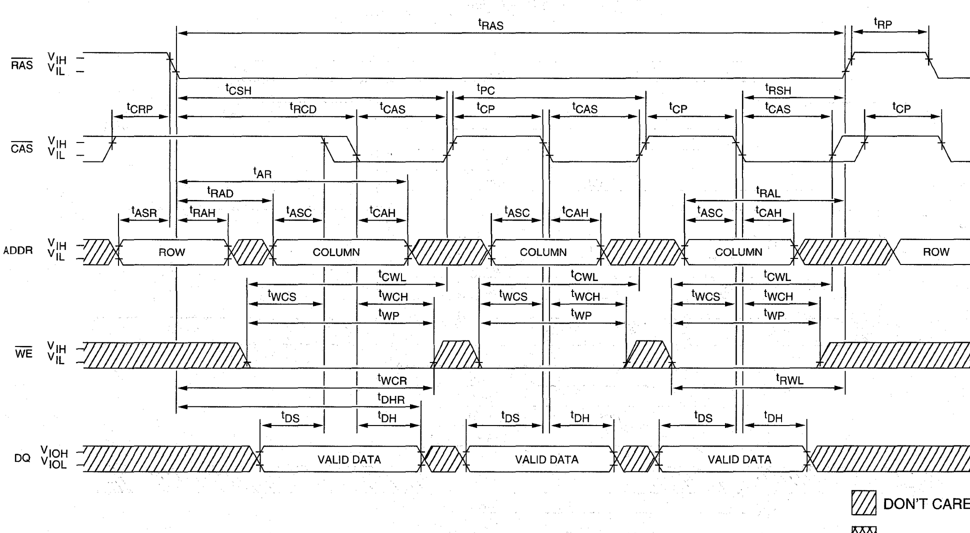
FAST-PAGE-MODE EARLY-WRITE CYCLE



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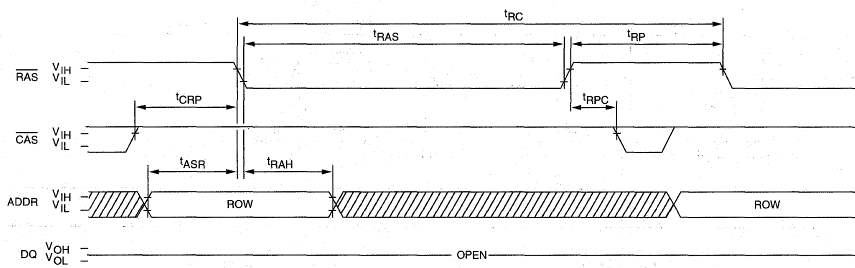
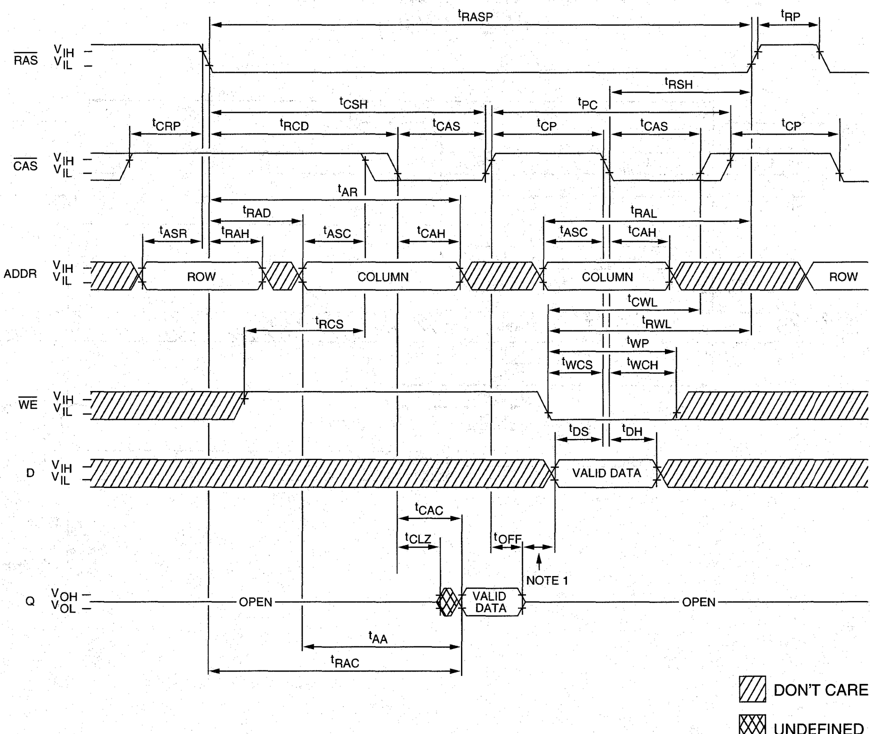
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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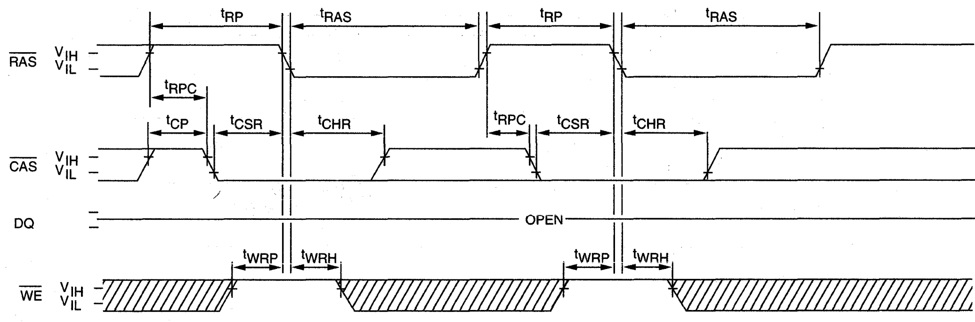
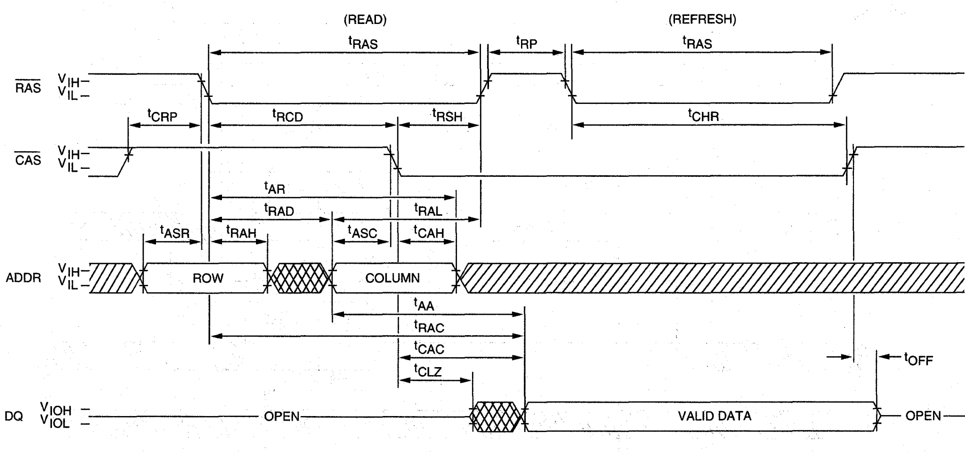
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



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DRAM MODULE

4 MEG x 8

4 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

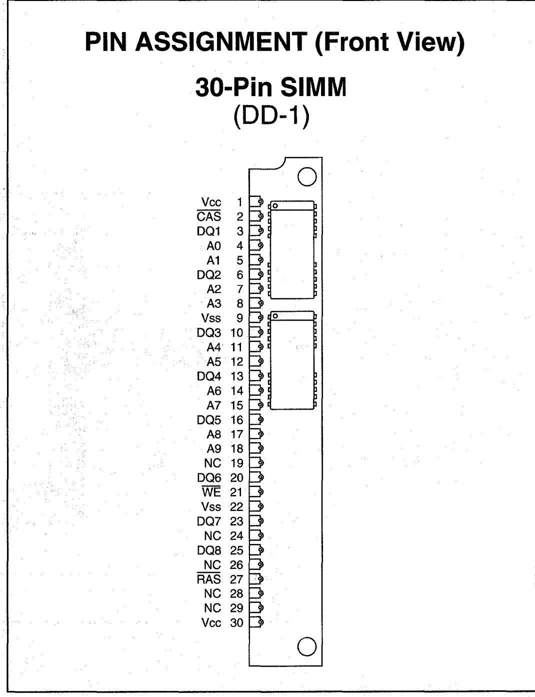
- JEDEC- and industry-standard pinout in a 30-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 6mW standby; 500mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE (FPM) access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - 30-pin SIMM — M
- Part Number Example: MT2D48M-6

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns



GENERAL DESCRIPTION

The MT2D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. Since $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operations.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$-ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

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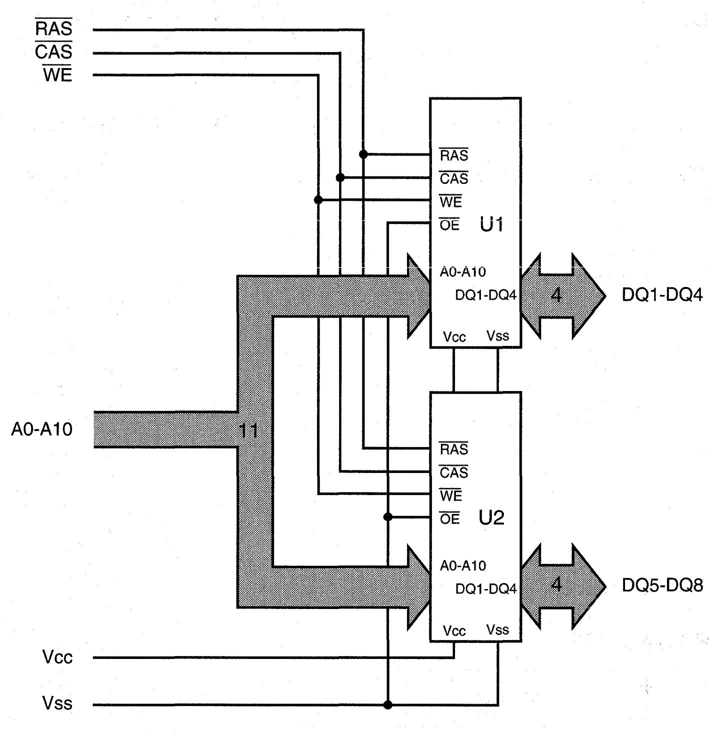
DRAM SIMM

FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4M4B1DJ

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES tR	ADDRESSES tC	DATA-IN/OUT DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	A0-A10, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	II	-4	4	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8	IOZ	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low (Logic 0) Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	ICC2	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC3	240	220	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	ICC4	180	160	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = VIH: ^tRC = ^tRC [MIN])	ICC5	240	220	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	ICC6	240	220	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		13	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		17	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODEREAD or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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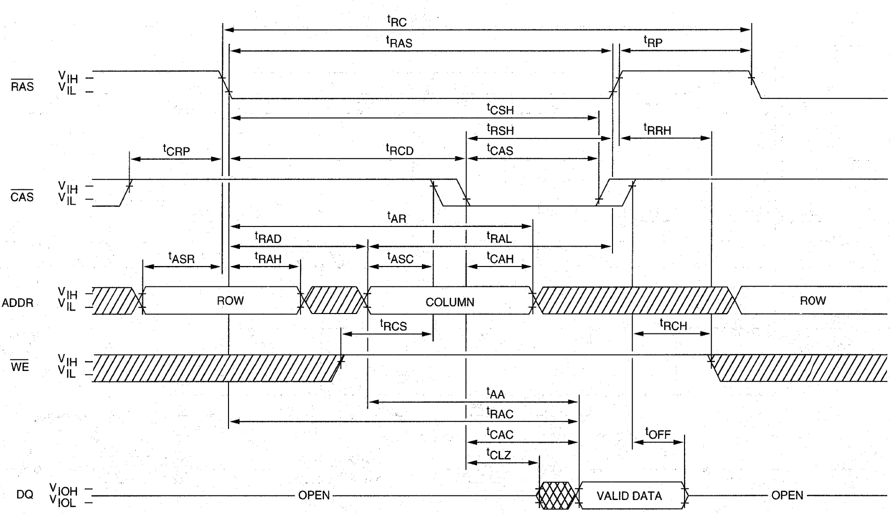
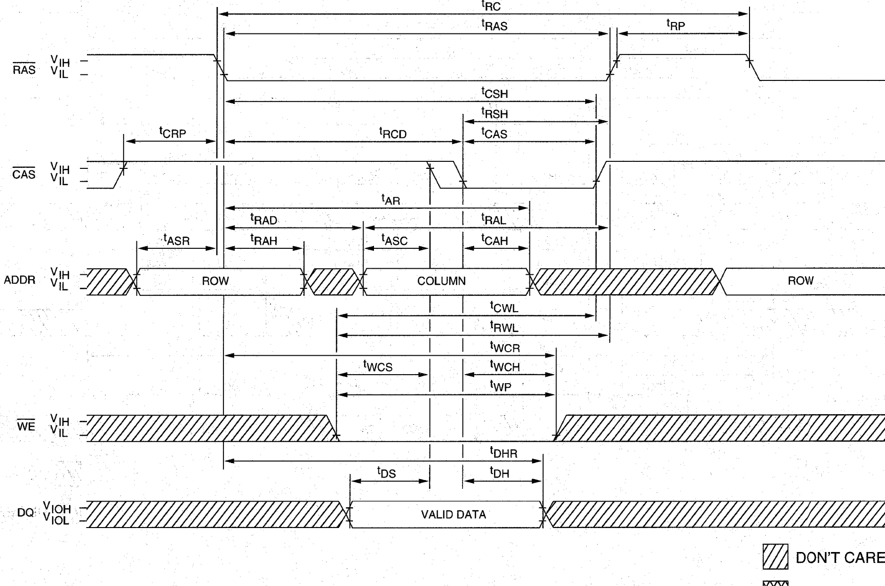
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

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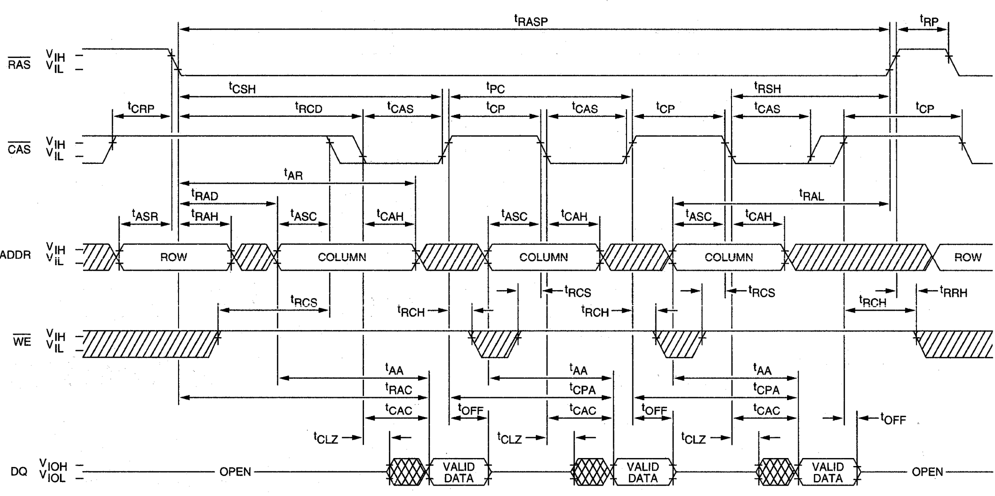
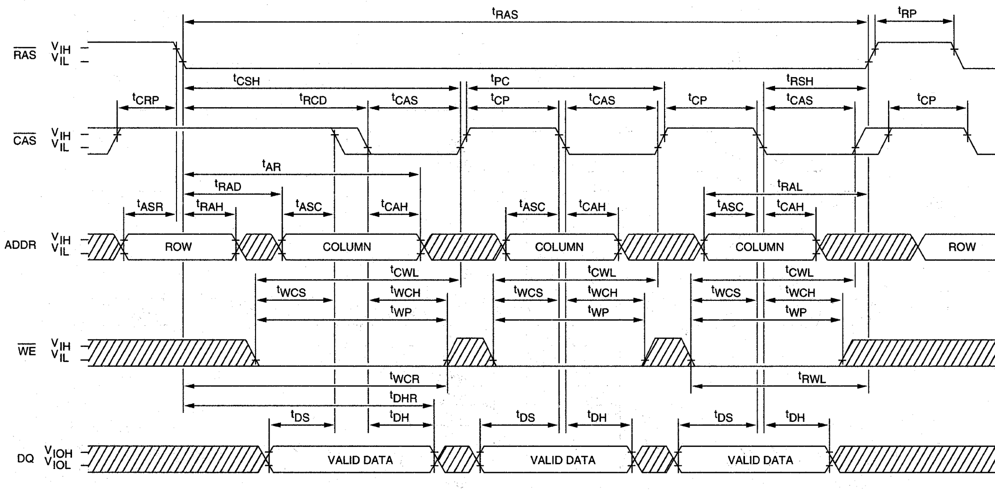
DRAM SIMM

FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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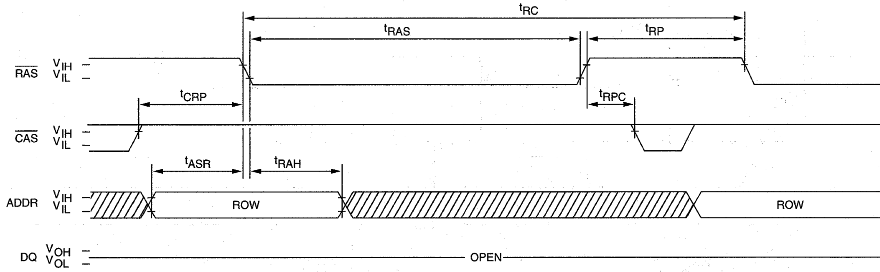
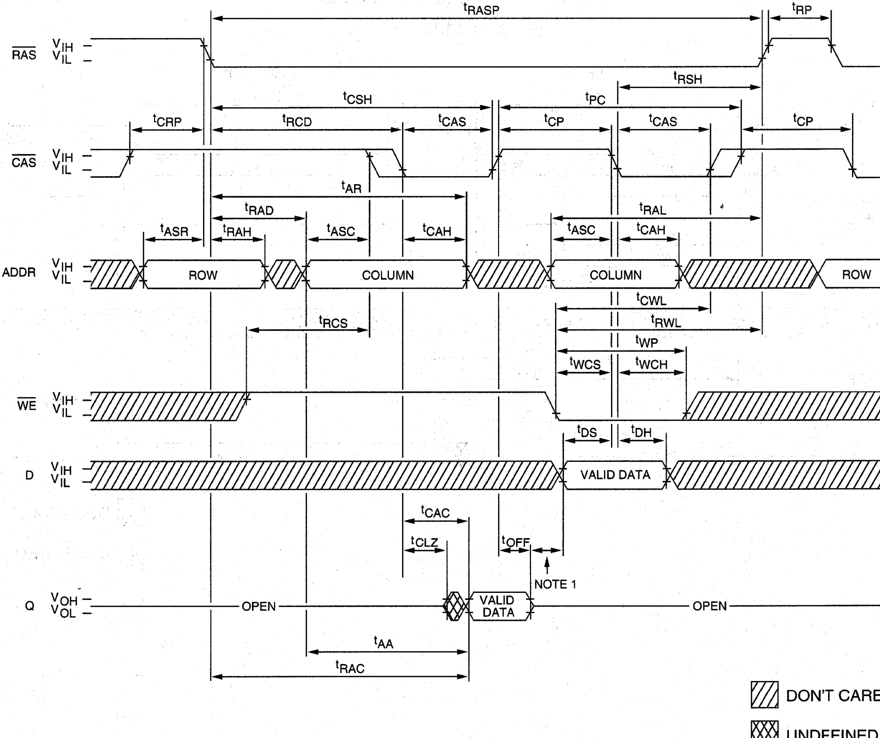
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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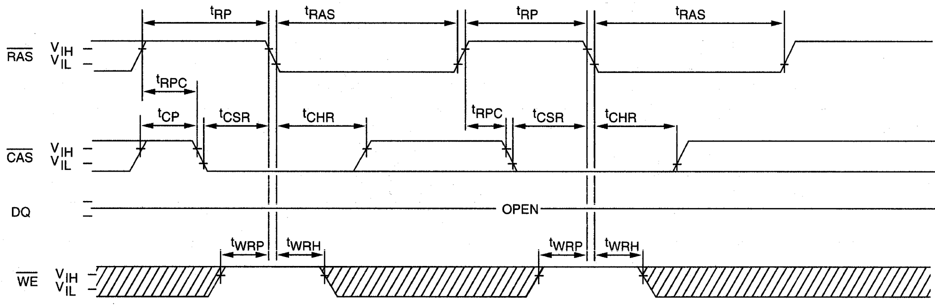
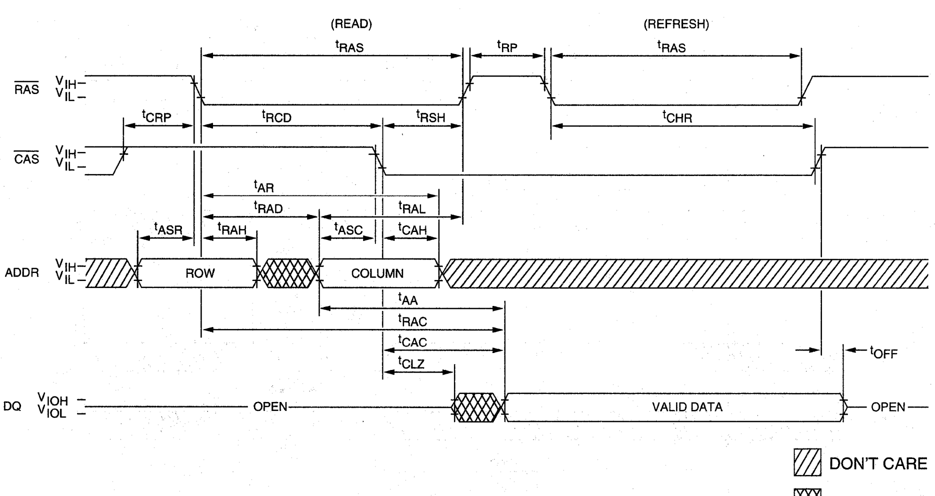
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



DRAM SIMM

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DRAM MODULE

4 MEG x 8

4 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 24mW standby; 1,800mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
30-pin SIMM	M

- Part Number Example: MT8D48M-6

KEY TIMING PARAMETERS

SPEED	${}^tRC$	${}^tRAC$	${}^tPC$	${}^tAA$	${}^tCAC$	${}^tRP$
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

30-Pin SIMM
(DD-3)

Pin	Name
1	Vcc
2	CAS
3	DQ1
4	A0
5	A1
6	DQ2
7	A2
8	A3
9	Vss
10	DQ3
11	A4
12	A5
13	DQ4
14	A6
15	A7
16	DQ5
17	A8
18	A9
19	*A10
20	DQ6
21	WE
22	Vss
23	DQ7
24	NC
25	DQ8
26	NC
27	RAS
28	NC
29	NC
30	Vcc

*Address not used for RAS-ONLY REFRESH

GENERAL DESCRIPTION

The MT8D48 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x8 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the ouput remains open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every16ms regardless of sequence.

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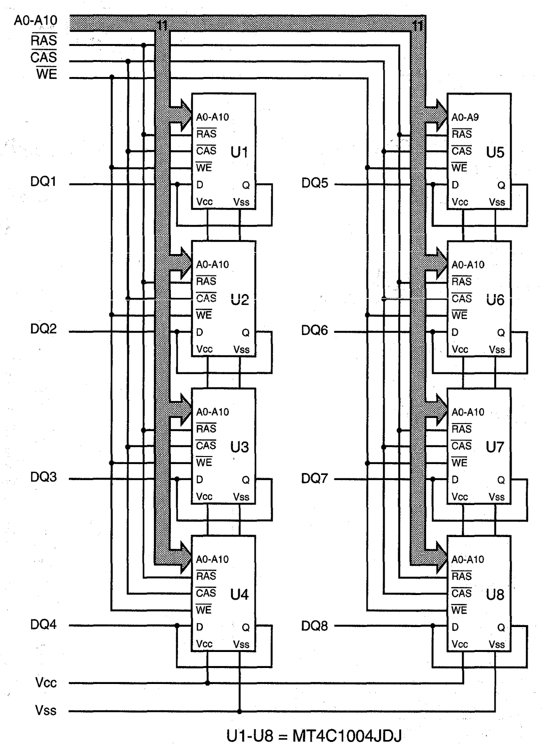
FUNCTIONAL BLOCK DIAGRAM



U1-U8 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
					${}^tR$	${}^tC$	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	A0-A10, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$	II	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	8	8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	ICC3	880	800	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: $^tPC = {}^tPC$ [MIN])	ICC4	640	560	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: $^tRC = {}^tRC$ [MIN])	ICC5	880	800	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC = {}^tRC$ [MIN])	ICC6	880	800	mA	3, 5

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DRAM SIMM

CAPACITANCE

DESCRIPTION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$	C_{I2}	67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}	15	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	5
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	21
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a	23
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a	23
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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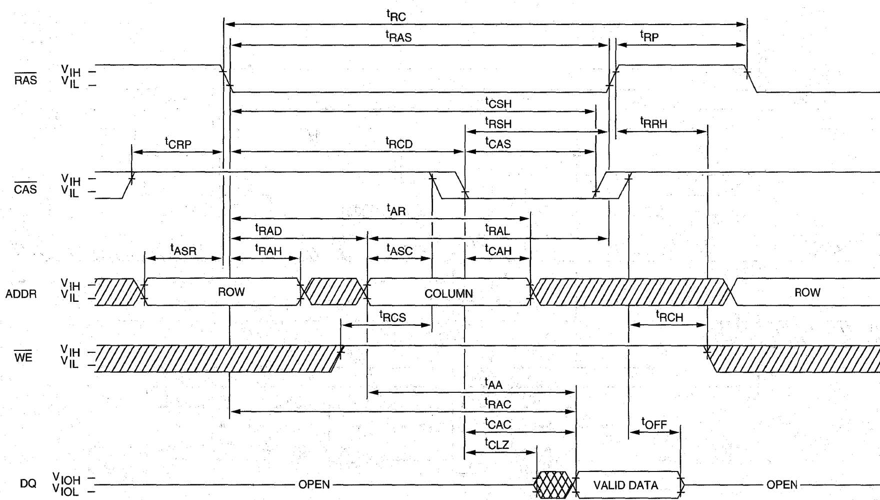
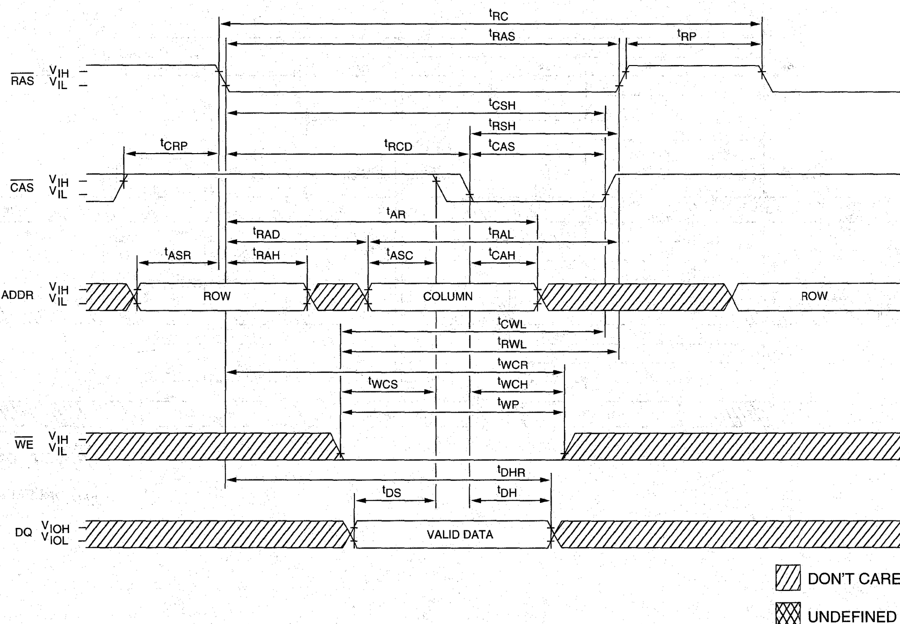
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM SIMM

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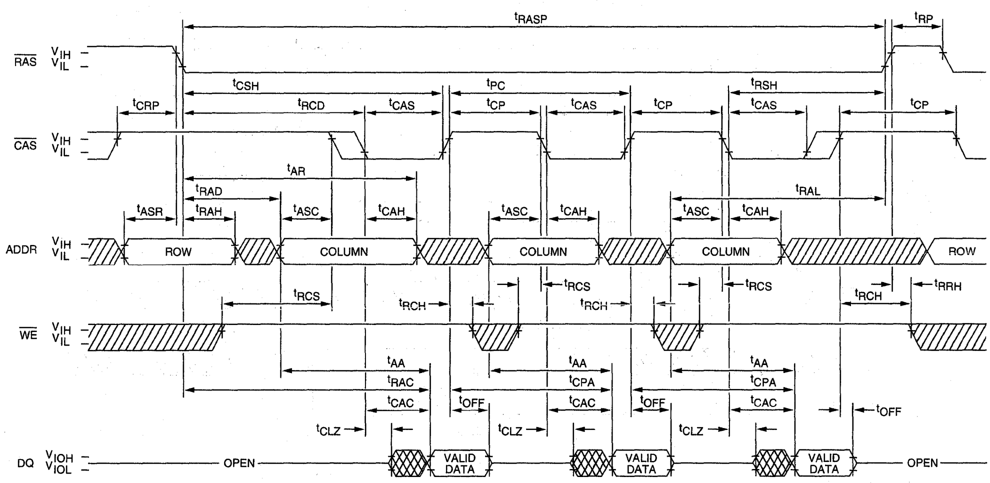
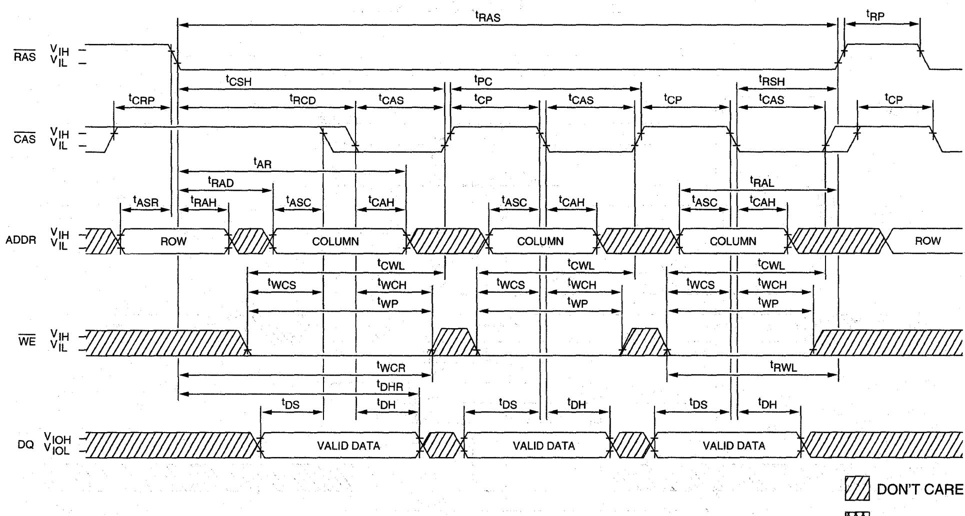
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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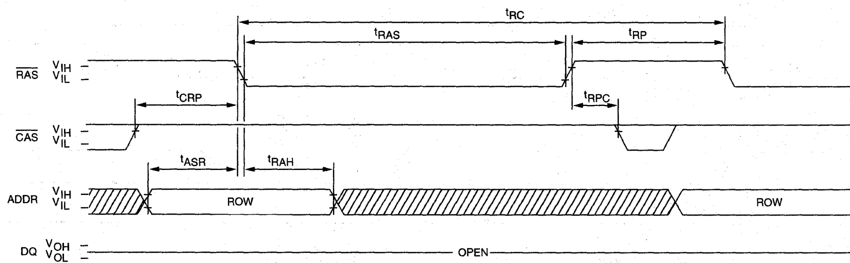
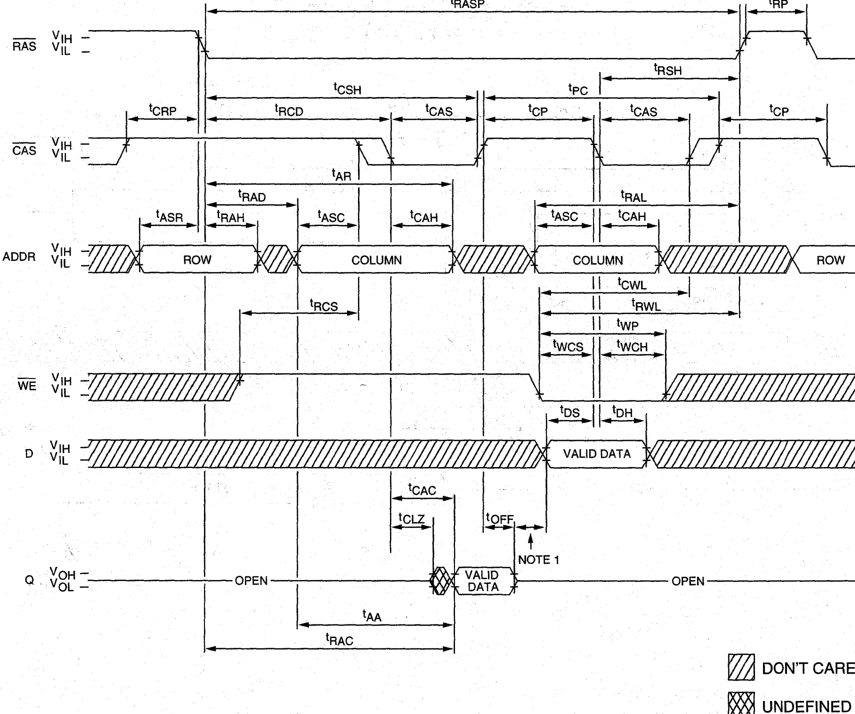
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A9; A10 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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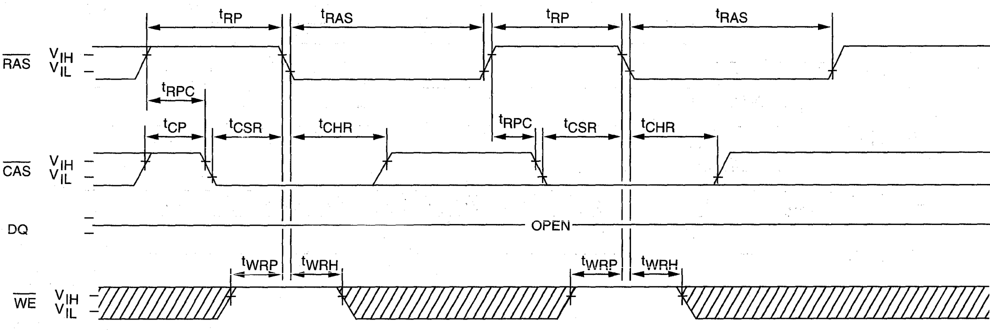
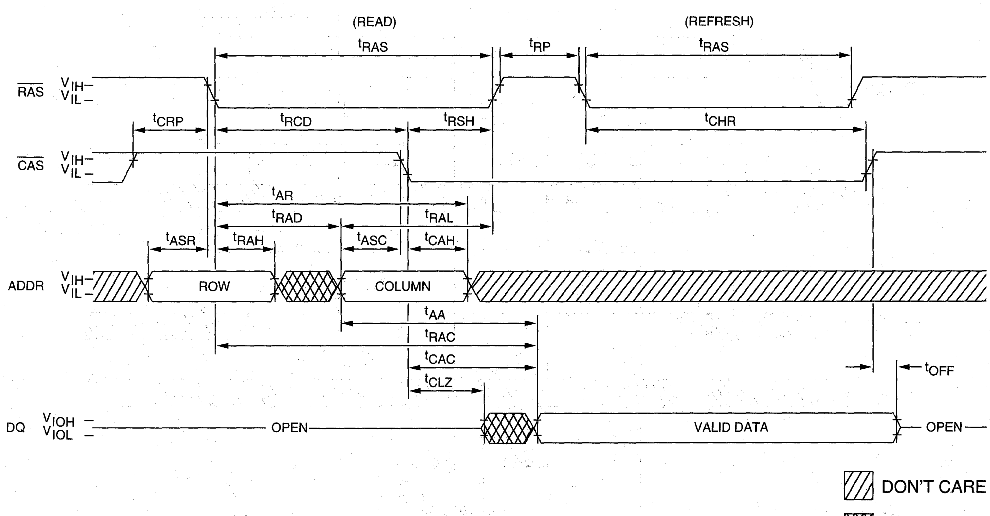
DRAM SIMM

CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
(WE = HIGH)



DRAM SIMM

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DRAM MODULE

4 MEG x 9

4 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 9mW standby; 725mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE (FPM) access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- Low profile

OPTIONS — MARKING

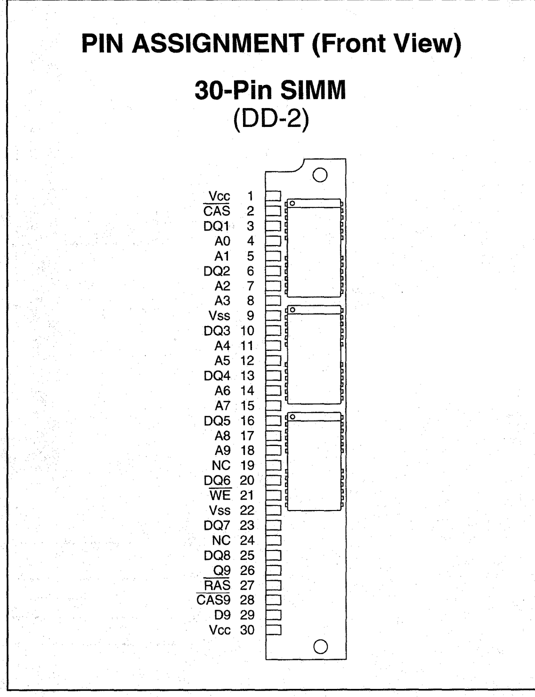
- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - 30-pin SIMM — M
- Part Number Example: MT3D49M-6

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

30-Pin SIMM
(DD-2)



GENERAL DESCRIPTION

The MT3D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pins remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operations.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

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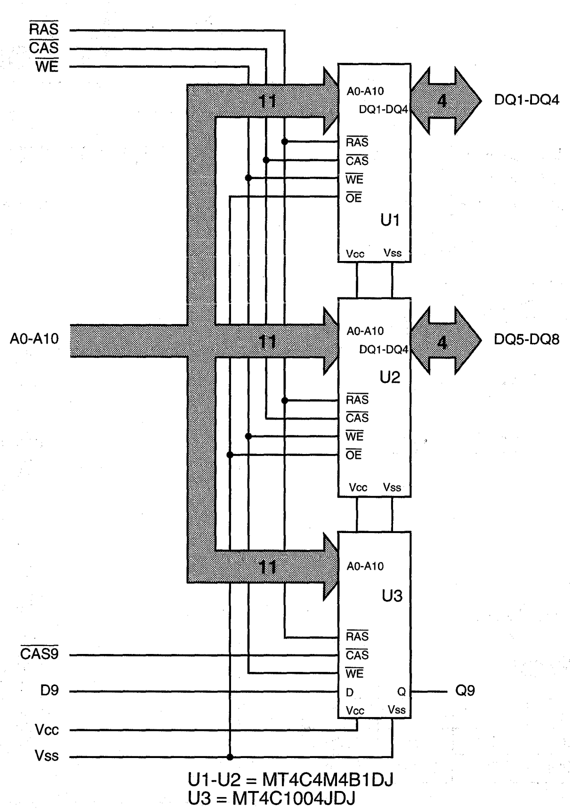
FUNCTIONAL BLOCK DIAGRAM



U1-U2 = MT4C4M4B1DJ
U3 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature .... -55°C to +125°C
Power Dissipation 3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V)	D9, $\overline{CAS9}$	II	-2	2	µA	
	A0-A10, $\overline{RAS}$, $\overline{WE}$	II	-6	6	µA	
OUTPUT LEAKAGE (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8, Q9	IOZ	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low (Logic 0) Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	6	6	mA	
STANDBY CURRENT: (CMOS) Average power supply current ($\overline{RAS}$ = $\overline{CAS}$ = 'Other Inputs = Vcc -0.2V)	ICC2	3	3	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; tRC = tRC [MIN])	ICC3	350	320	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL; $\overline{CAS}$ = Cycling; tPC = tPC [MIN])	ICC4	260	230	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = VIH; tRC = tRC [MIN])	ICC5	350	320	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling = tRC = tRC [MIN])	ICC6	350	320	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		19	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		25	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		10	pF	2
Input Capacitance: DQ9	C_{I3}		10	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command setup time	^tRCS	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Refresh period (2,048 cycles)	^tREF		32		32	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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DRAM SIMM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. $\overline{OE}$ is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not possible.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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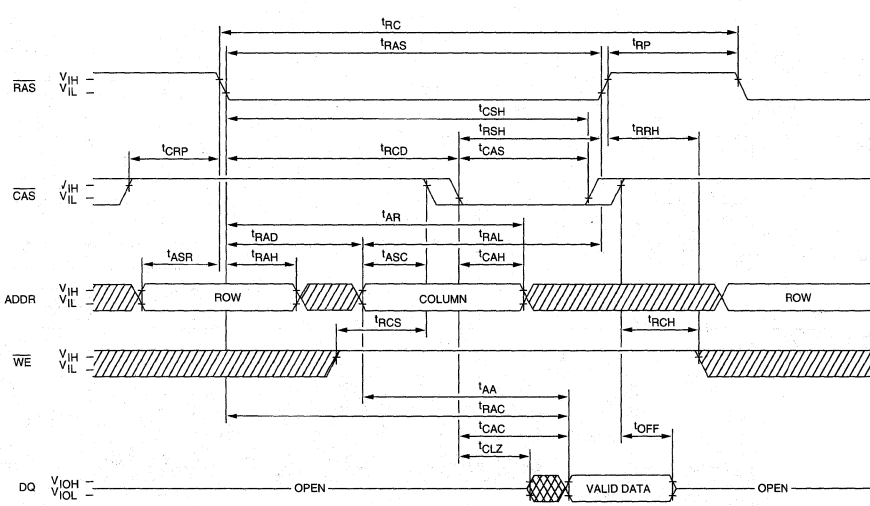
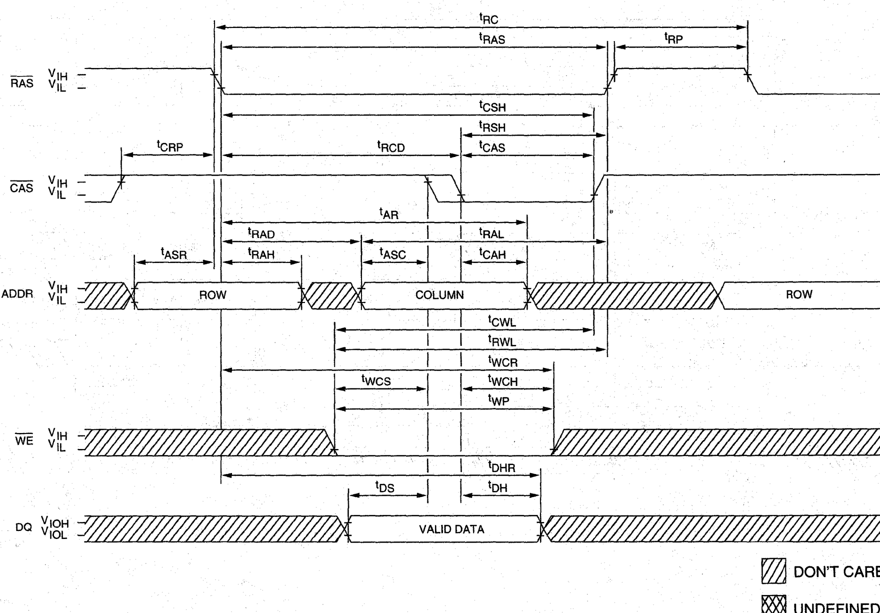
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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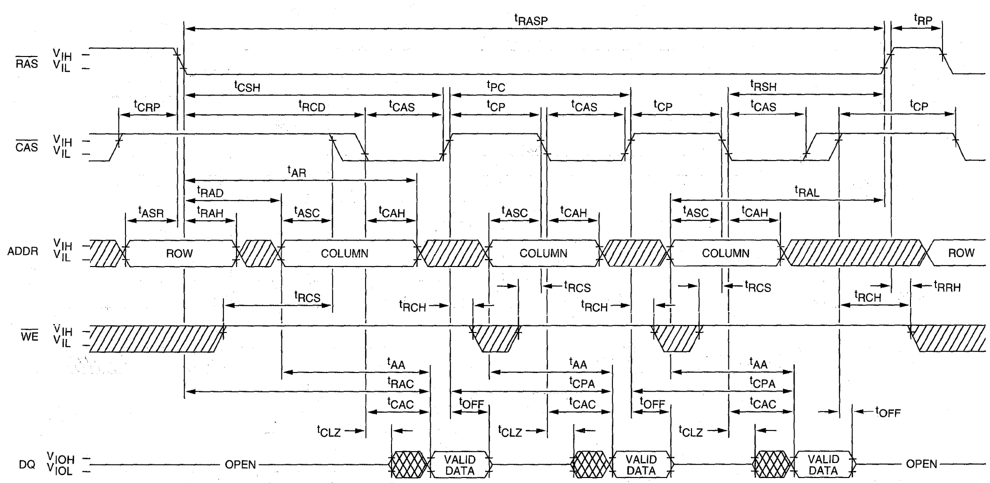
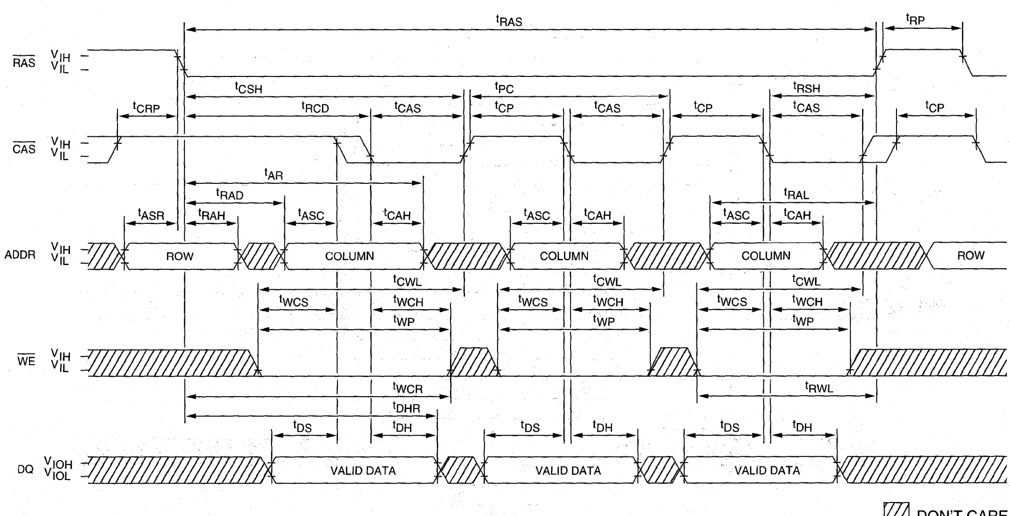
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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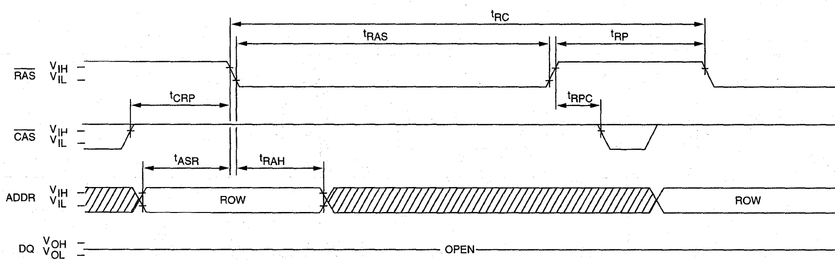
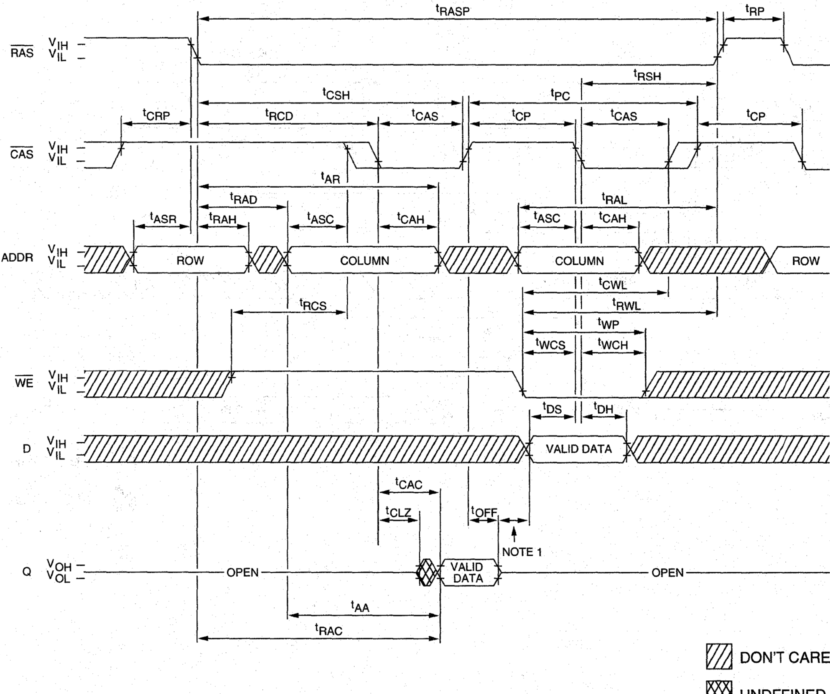
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

DRAM SIMM

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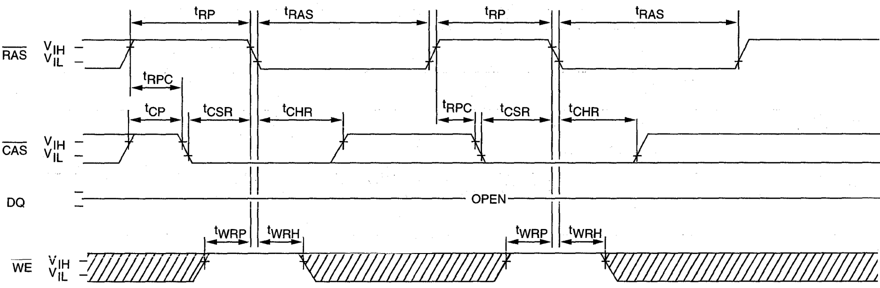
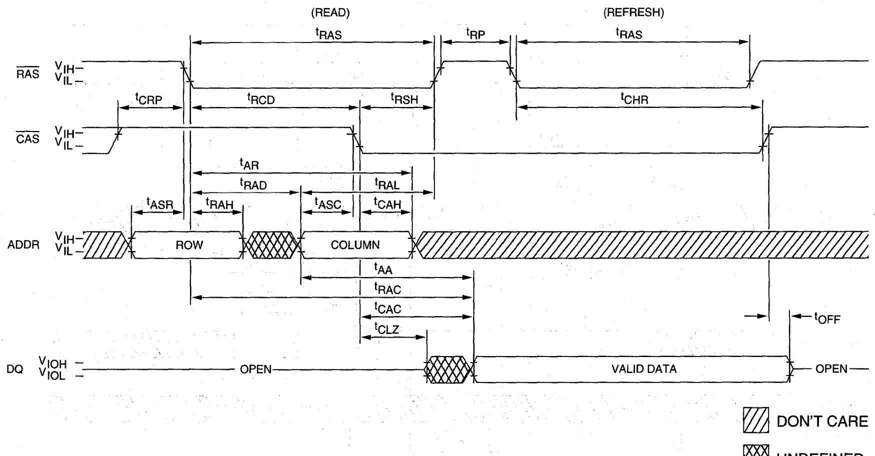
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
(WE = HIGH)



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DRAM MODULE

4 MEG x 9

4 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 27mW standby; 2,025mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
30-pin SIMM	M

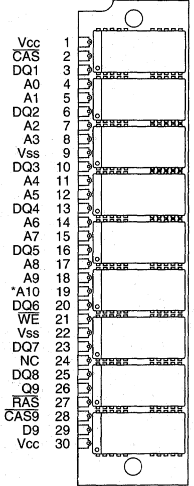
- Part Number Example: MT9D49M-6

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

30-Pin SIMM
(DD-4)



*Address not used for $\overline{RAS}$-ONLY REFRESH

GENERAL DESCRIPTION

The MT9D49 is a randomly accessed solid-state memory containing 4,194,304 words organized in a x9 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the ouput remains open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms regardless of sequence.

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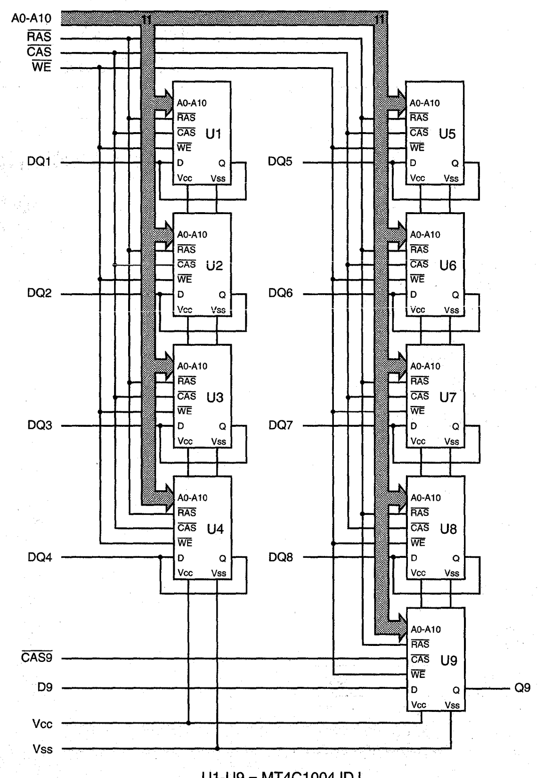
FUNCTIONAL BLOCK DIAGRAM



U1-U9 = MT4C1004JDJ

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{CAS9}$	$\overline{WE}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	L	H	X	X	High-Z

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	D9, CAS9	II	-2	2	µA	
Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V)	A0-A10, WE, CAS, RAS	II	-18	18	µA	
OUTPUT LEAKAGE CURRENT	Q9	IOZ	-10	10	µA	
(Q is disabled; 0V ≤ VOUT ≤ 5.5V)	DQ1-DQ8	IOZ	-12	12	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	18	18	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Vcc -0.2V)	ICC2	9	9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	990	900	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	720	630	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	990	900	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC6	990	900	mA	3, 5

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		55	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$	C_{I2}		73	pF	2
Input Capacitance: D9, $\overline{CAS9}$	C_{I3}		10	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		15	pF	2
Output Capacitance: Q9	C_O		10	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Column-address hold time	^{t}CAH	10		15		ns	
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	5
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	21
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		n/a	23
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		n/a	23
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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DRAM SIMM

NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ᵗCP.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRAC (MIN) and ᵗCAC (MIN) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
24. ᵗWTS and ᵗWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

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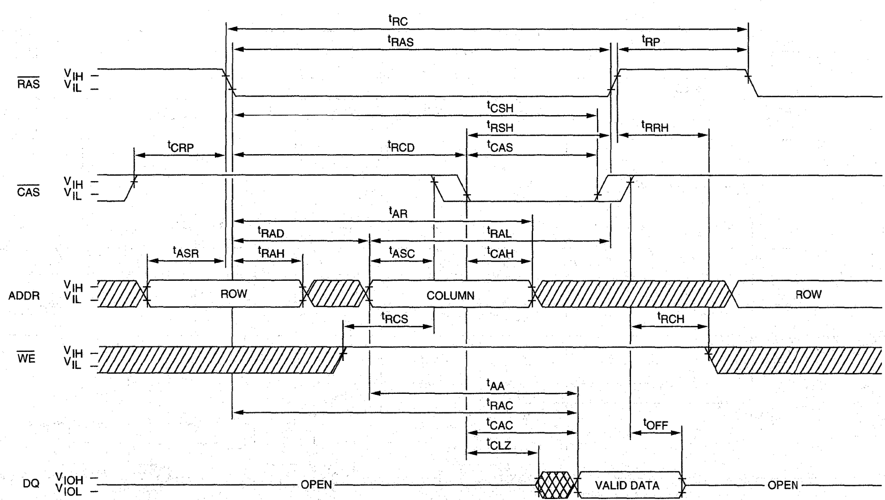
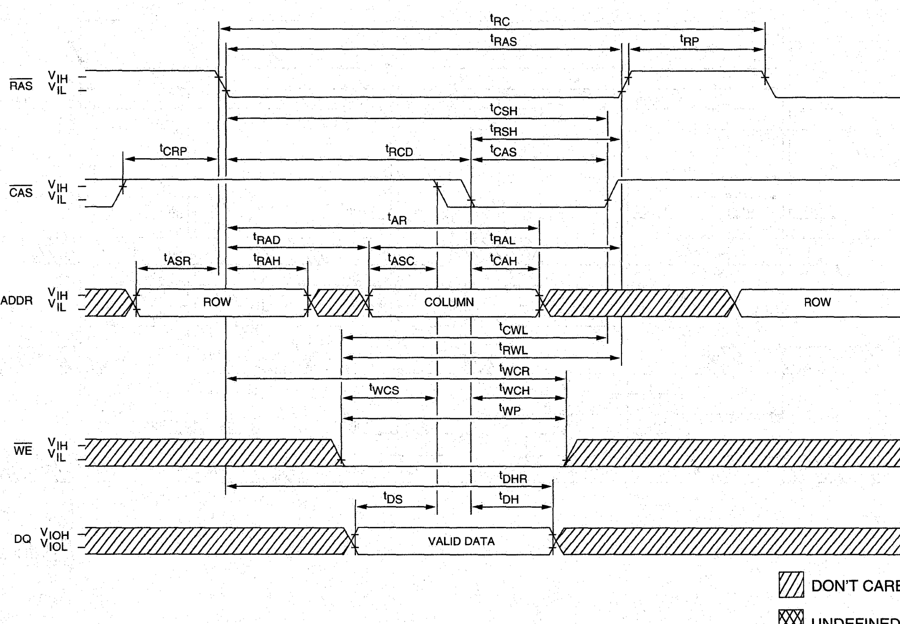
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM SIMM

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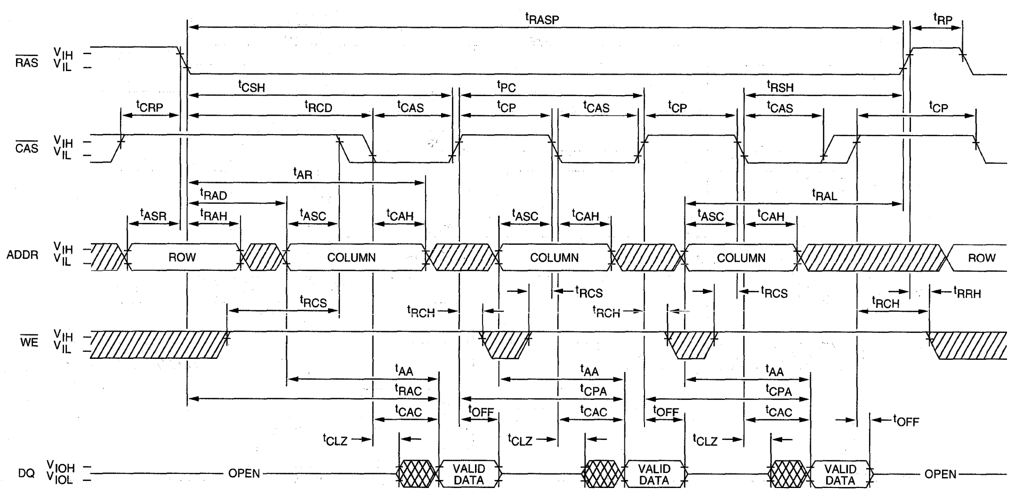
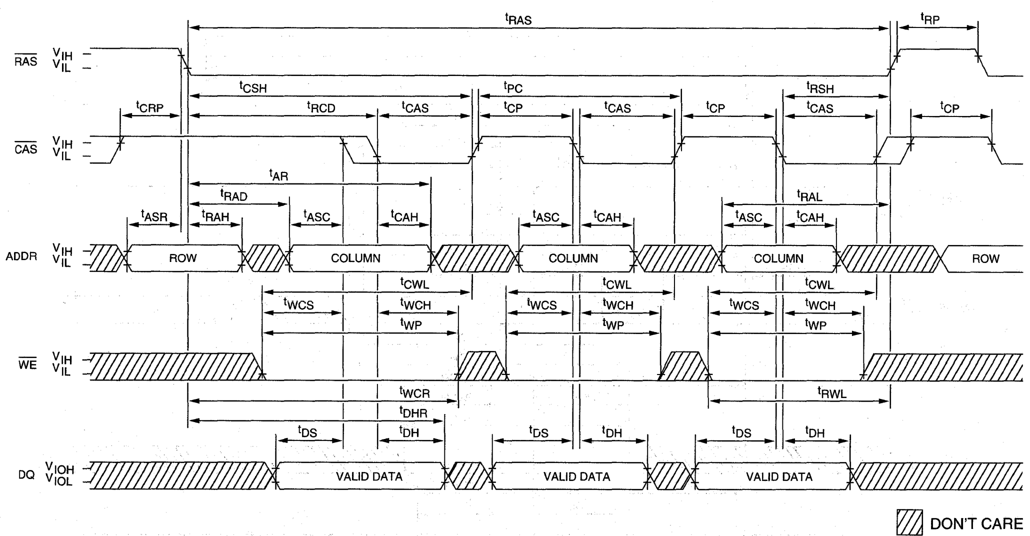
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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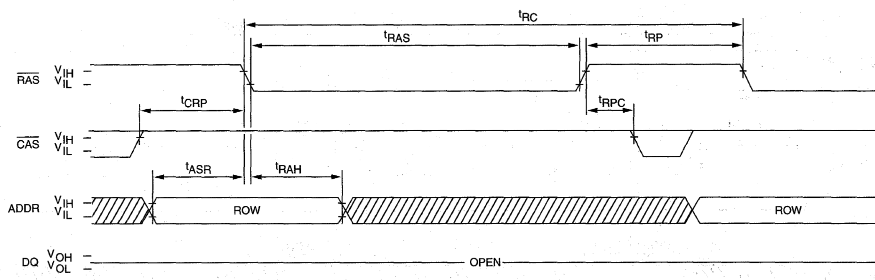
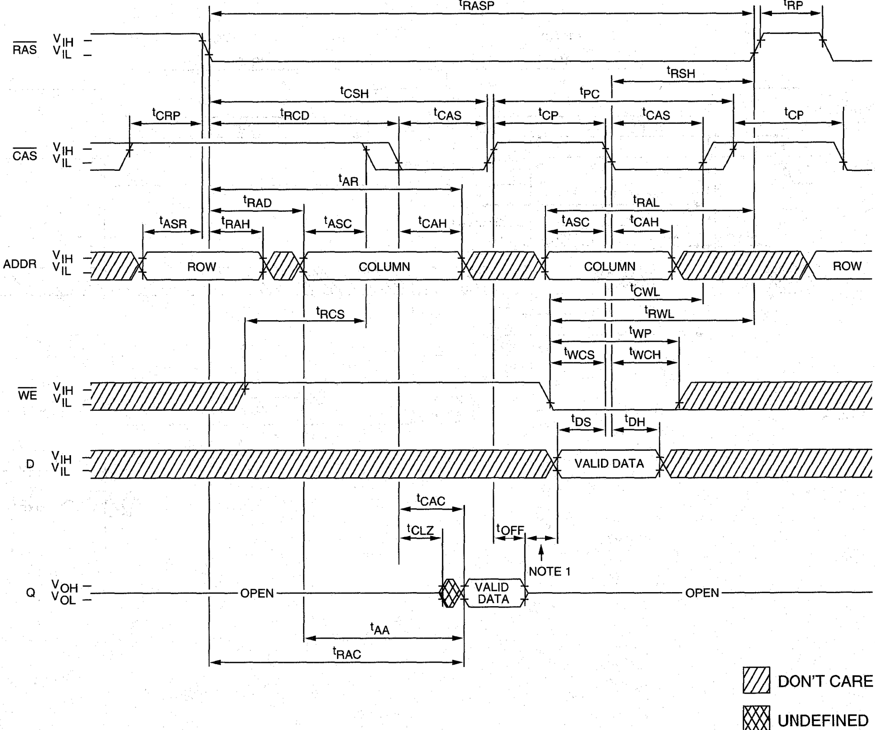
RAS-ONLY REFRESH CYCLE
(A10 and WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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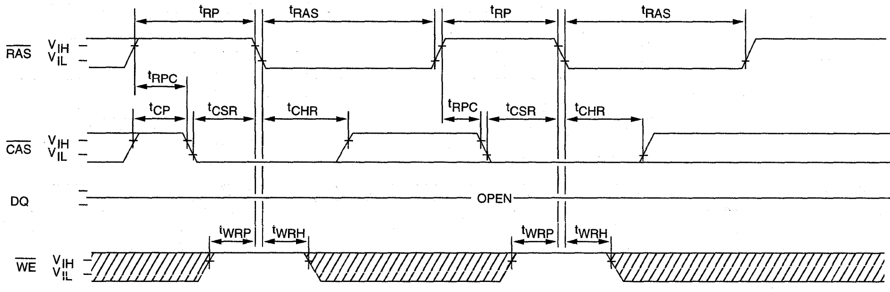
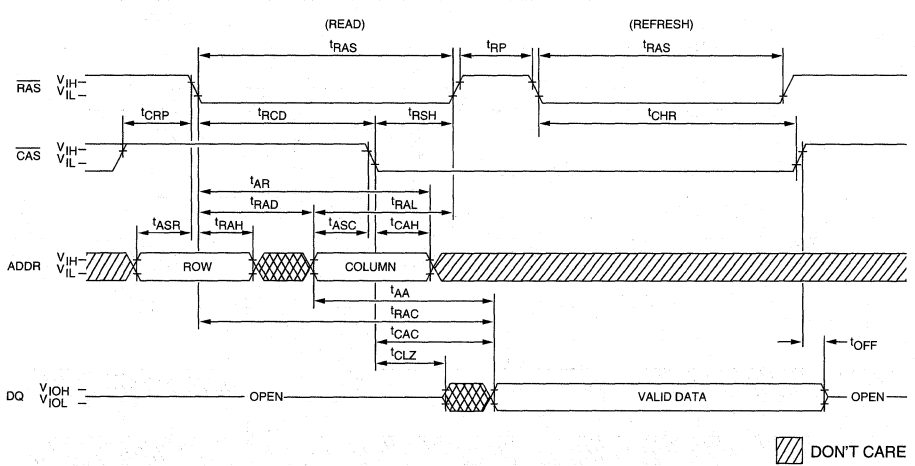
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
(WE = HIGH)



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DRAM MODULE

256K, 512K x 32

1, 2 MEGABYTE, 5V, FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 12mW standby; 756mW active, typical (2MB)
- Multiple RAS lines offer x16 or x32 widths
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6**
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G

**60ns specifications are limited to a Vcc range of ±5%.

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT2D25632G-xx	256K x 32, Gold
MT2D25632M-xx	256K x 32, Tin/Lead
MT4D51232G-xx	512K x 32, Gold
MT4D51232M-xx	512K x 32, Tin/Lead

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-5) 256K x 32
(DD-6) 512K x 32

1 36 37 72

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC/RAS1*	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ25	68	PRD2
15	A3	33	NC/RAS3*	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*2MB version only

GENERAL DESCRIPTION

The MT2D25632 and MT4D51232 are randomly accessed 1MB and 2MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS is used to latch the first 9 bits and CAS the latter 9 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode, while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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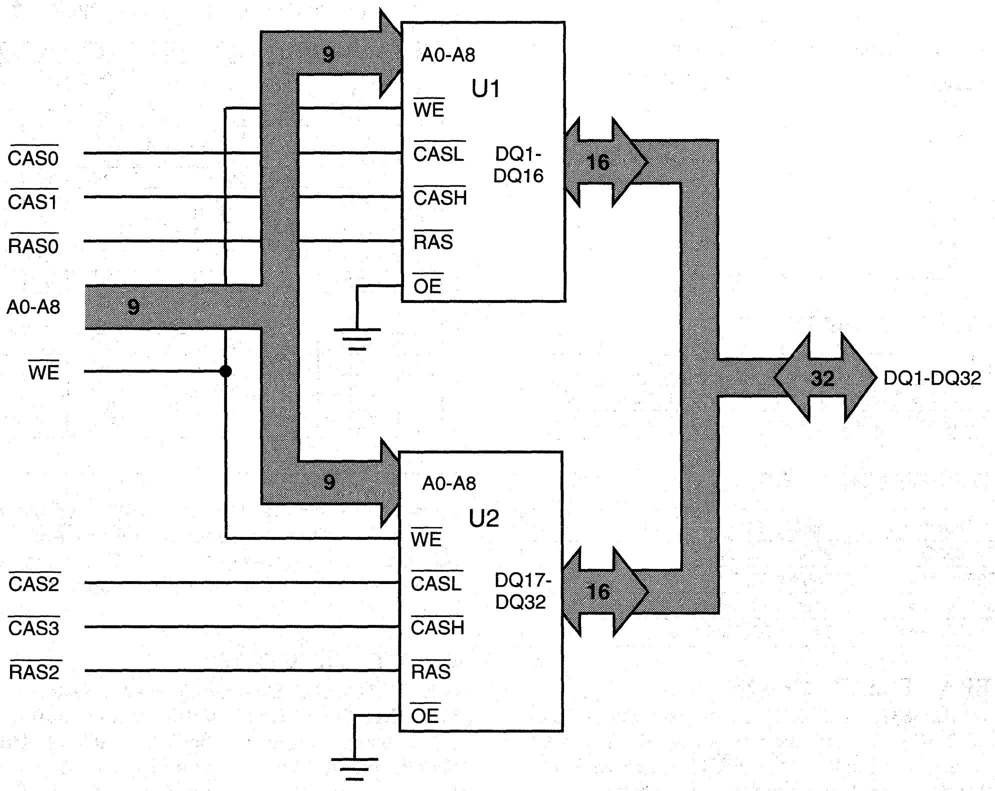
REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS-ONLY, CBR or HIDDEN) so that all 512 combinations of RAS addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT2D25632 (1MB)



U1-U2 = MT4C16257DJ

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FUNCTIONAL BLOCK DIAGRAM
MT4D51232 (2MB)

U1-U4 = MT4C16257DJ

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY-WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	L→H	H	ROW	COL	Data-Out
	2nd Cycle	L	L→H	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	L→H	L	ROW	COL	Data-In
	2nd Cycle	L	L→H	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT2D25632 (1MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT4D51232 (2MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +5V ±10%**)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0- RAS3	II1	-2	2	µA	
Any input 0V ≤ VIN ≤ Vcc	A0-A8, WE	II2	-8	8	µA	27
(All other pins not under test = 0V) for each package input	CAS0-CAS3	II3	-4	4	µA	27
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	27
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6**	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	1MB 2MB	4 8	4 8	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	1MB 2MB	2 4	2 4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	1MB 2MB	380 384	340 344	mA	2, 22, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN]; tCP, tASC = 10ns)	ICC4	1MB 2MB	240 244	220 224	mA	2, 22, 25
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	1MB 2MB	380 384	340 344	mA	22, 25
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling; tRC = tRC [MIN])	ICC6	1MB 2MB	360 364	320 324	mA	19, 22

**60ns specifications are limited to a Vcc range of ±5%.

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CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		1MB	2MB		
Input Capacitance: A0-A8	C_{I1}	12	24	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	16	32	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}	10	10	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	10	20	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO1}	10	18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	9
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	19
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^{t}CLCH	10		10		ns	26
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	24
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	8		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	19
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	15
Output buffer turn-off delay	^{t}OFF	3	15	3	15	ns	12, 24
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		ns	21
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	23
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		130		ns	

*60ns specifications are limited to a V_{CC} range of ±5%.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command setup time	^tRCS	0		0		ns	
Refresh period (512 cycles)	^tREF		8		8	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	10		10		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	14
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		10		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		10		ns	

*60ns specifications are limited to a Vcc range of ±5%.

DRAM SIMM

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U2/U4.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Column-address changed once each cycle.
26. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
27. 1MB module values will be half of those shown.

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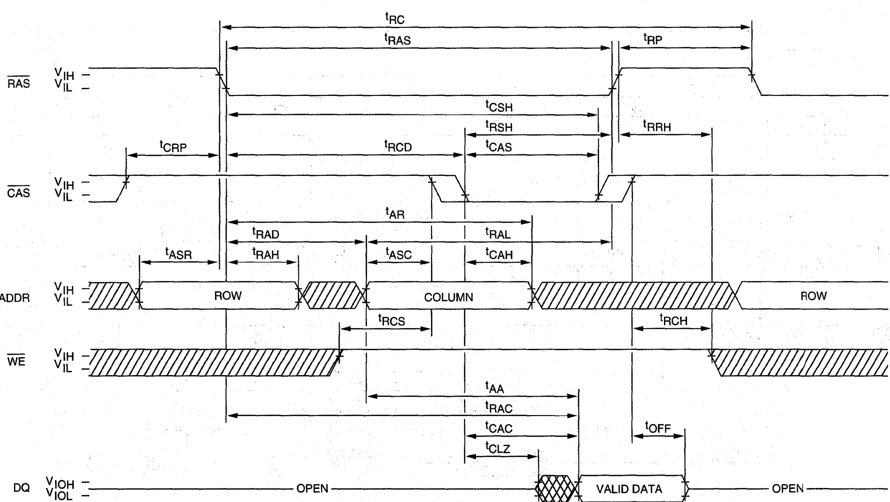
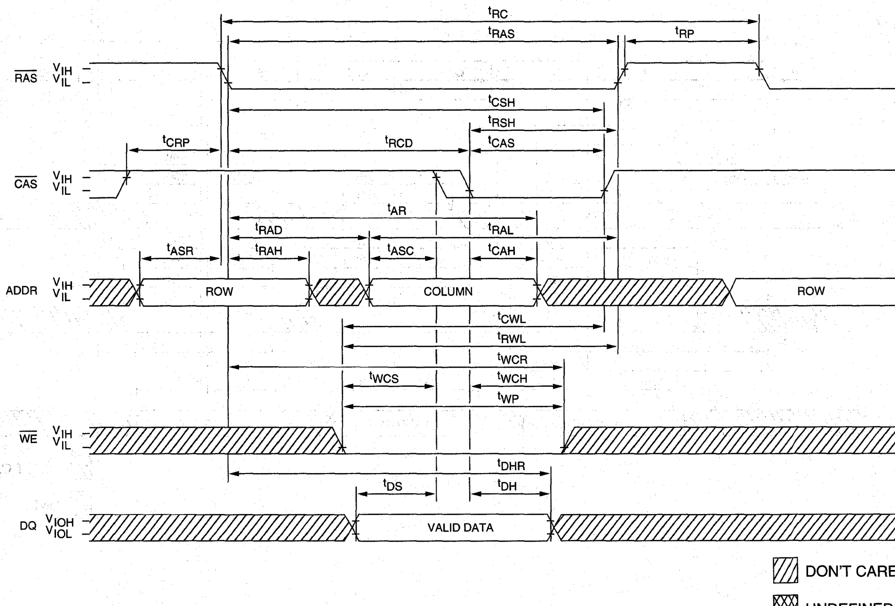
READ CYCLE



EARLY WRITE CYCLE



DRAM SIMM

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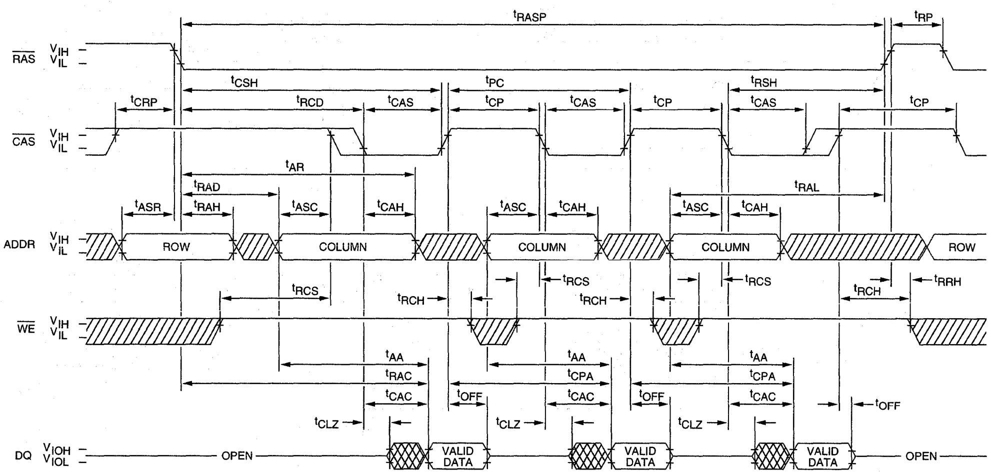
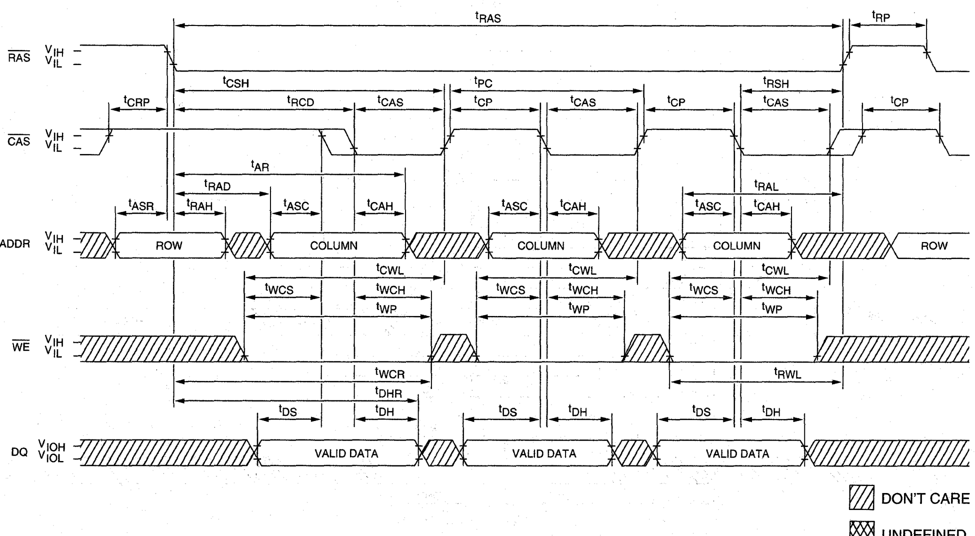
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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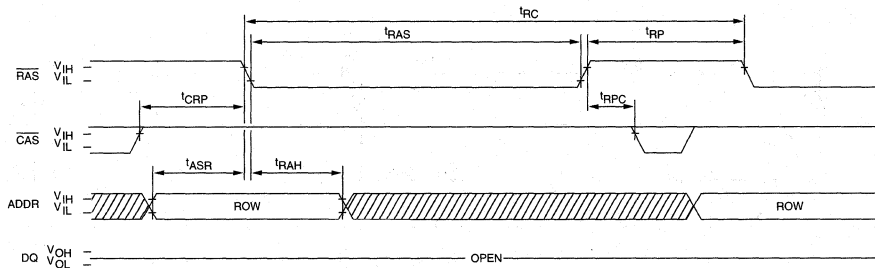
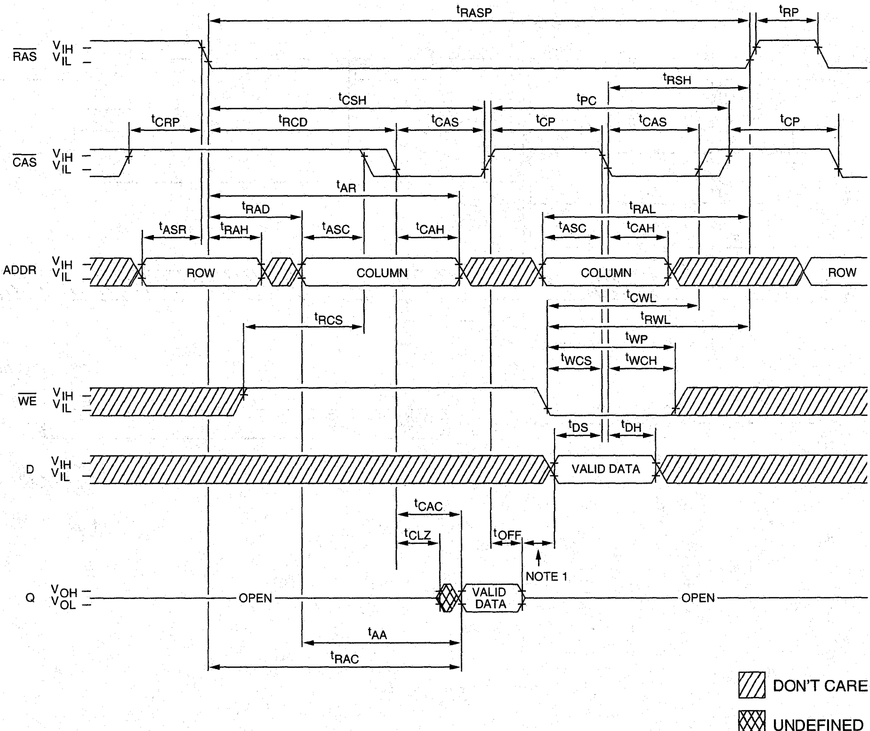
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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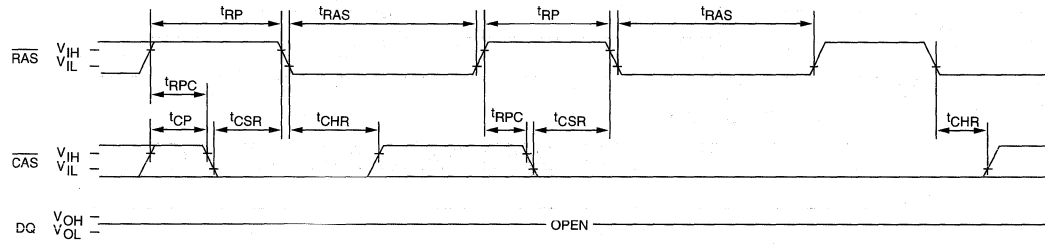
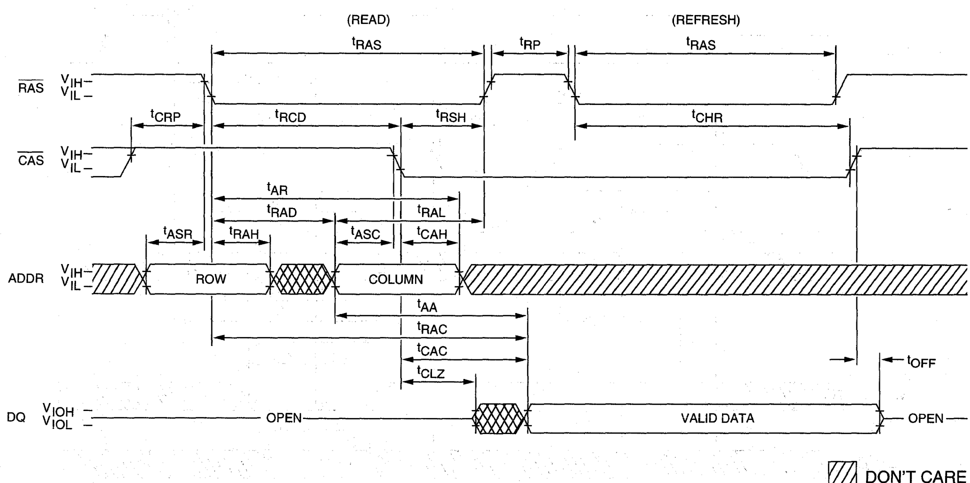
CBR REFRESH CYCLE
(Addresses, WE = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



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DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTES, 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 1,824mW active, typical (8MB)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF Refresh
- Multiple $\overline{RAS}$ lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Power/Refresh	
Normal Power/16ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8D132G-xx	1 Meg x 32, Gold
MT8D132G-xx S	1 Meg x 32, S**, Gold
MT8D132M-xx	1 Meg x 32, Tin/Lead
MT8D132M-xx S	1 Meg x 32, S**, Tin/Lead
MT16D232G-xx	2 Meg x 32, Gold
MT16D232G-xx S	2 Meg x 32, S**, Gold
MT16D232M-xx	2 Meg x 32, Tin/Lead
MT16D232M-xx S	2 Meg x 32, S**, Tin/Lead

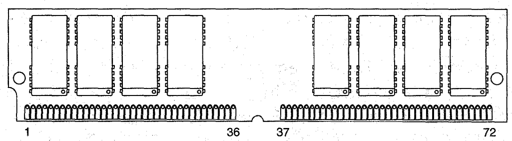
**S = SELF REFRESH

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-7) 1 Meg x 32

(DD-8) 2 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC/$\overline{RAS1}$*	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC/$\overline{RAS3}$*	51	DQ10	69	PRD3
16	A4	34	$\overline{RAS2}$	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*8MB version only

GENERAL DESCRIPTION

The MT8D132(S) and MT16D232(S) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

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FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combination of RAS addresses (A0-A9) are executed at least every 16ms (128ms on S version), regardless of sequence.

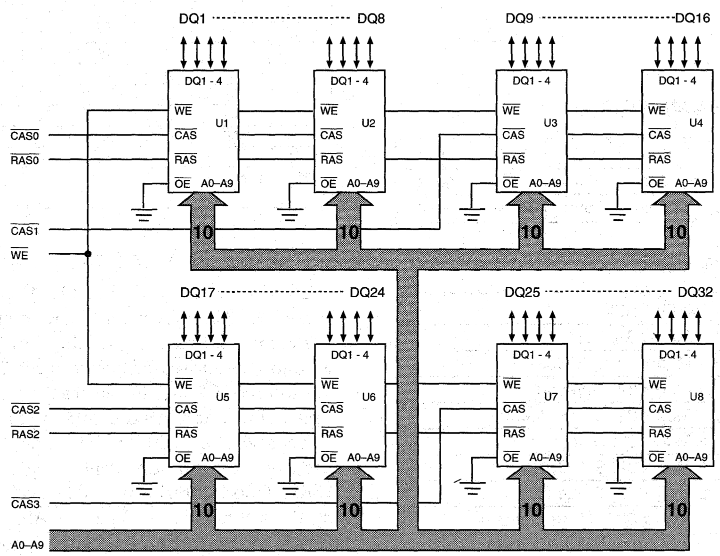
An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" version allows for an extended refresh period of 128ms, or 125ms per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum ᵗRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes burst refresh sequence, all 1,024 rows must be refreshed within 300µs, prior to the resumption of normal operation.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT8D132 (4MB)



U1-U8 = MT4C4001JDJ
U1-U8 = MT4C4001JDJ S (S version)

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FUNCTIONAL BLOCK DIAGRAM
MT16D232 (8MB)

U1-U16 = MT4C4001J or
U1-U16 = MT4C4001J S (S version)

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT8D132 (4MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT16D232 (8MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 6.5V	A0-A9, $\overline{WE}$	II2	-32	32	µA	29
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	II3	-8	8	µA	29
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	29
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

DRAM SIMM

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-6	-7		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4MB 8MB	16 32	16 32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	4MB 8MB	8 16	8 16	mA	
	I_{CC2} (S only)	4MB 8MB	1.6 3.2	1.6 3.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	4MB 8MB	880 896	800 816	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	4MB 8MB	640 656	560 576	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB	880 896	800 816	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB	880 896	800 816	mA	19, 22
REFRESH CURRENT: Extended (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	4MB 8MB	2 3.6	2 3.6	mA	19, 22 24
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB 8MB	2 3.6	2 3.6	mA	19, 27

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		4MB	8MB		
Input Capacitance: A0-A9	C_{I1}	48	95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	17
Input Capacitance: $\overline{RAS0-RAS3}$	C_{I4}	32	32	pF	17
Input Capacitance: $\overline{CAS0-CAS3}$	C_{I5}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	18	pF	17

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	9
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	10		10		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	19
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	15
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	12, 25
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	23
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		ms	27
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (1,024 cycles) S version	^tREF		128		128	ms	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	tRPS	110		130		ns	27
Read command hold time	tRRH	0		0		ns	14
$\overline{RAS}$ hold time	tRSH	15		20		ns	
READ WRITE cycle time	tRWC	n/a		n/a		ns	21
Write command to $\overline{RAS}$ lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		ns	
$\overline{WE}$ command setup time	tWCS	0		0		ns	
Write command pulse width	tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	10		10		ns	28

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If CAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U8/U16.
22. Icc is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to S version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
28. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
29. 4MB module values will be half of those shown.

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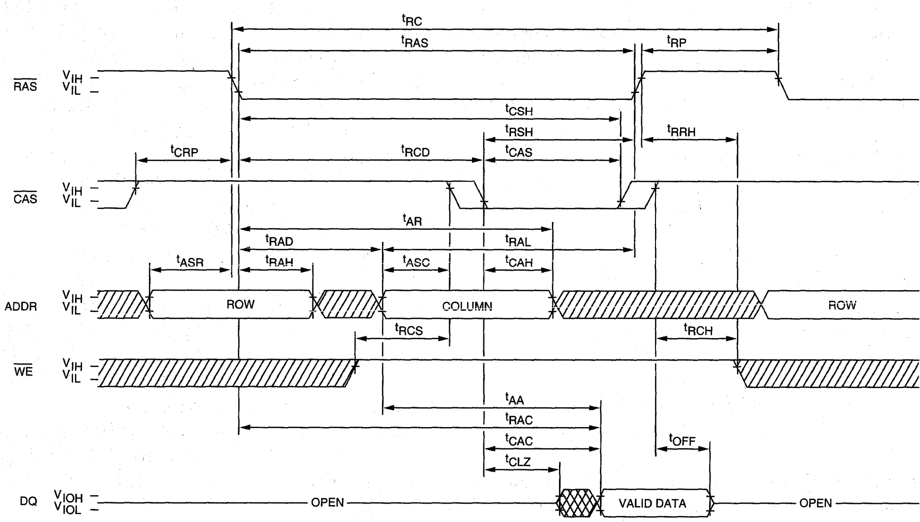
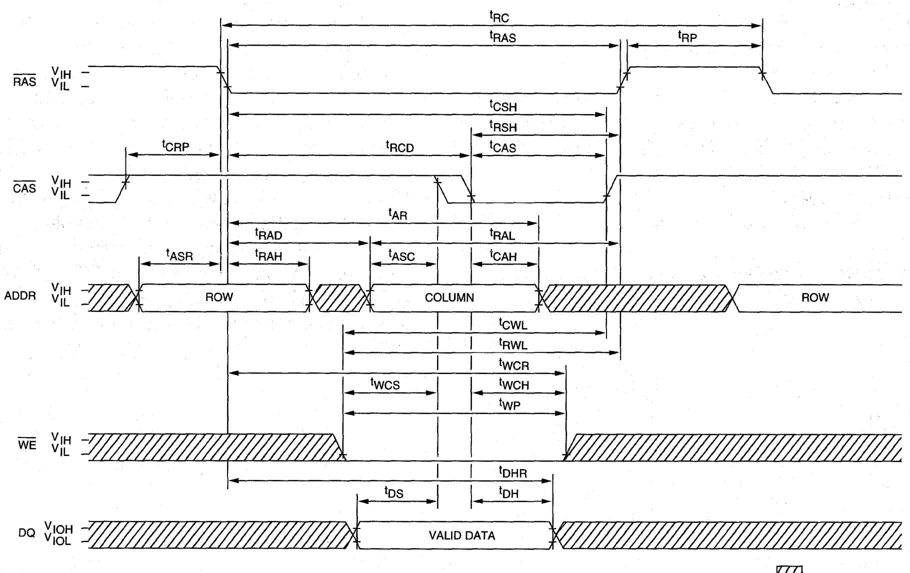
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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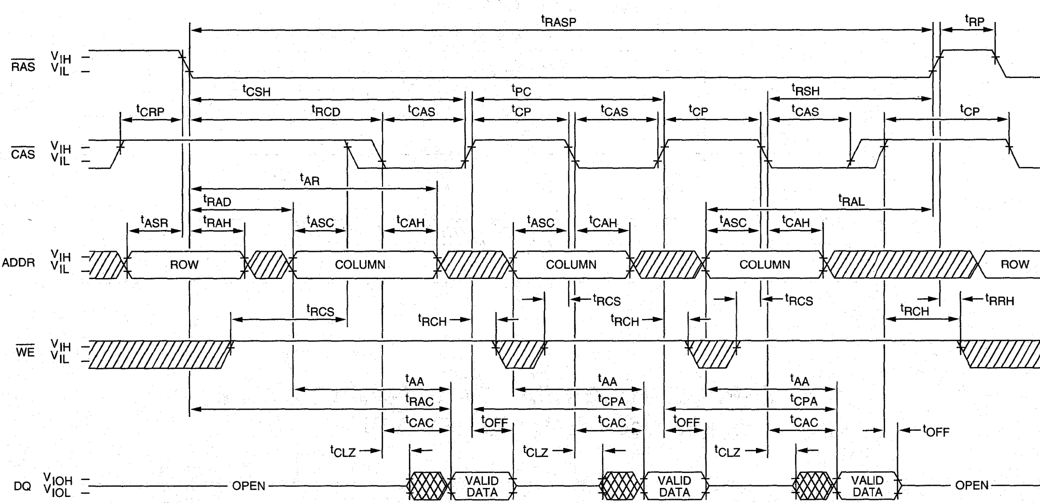
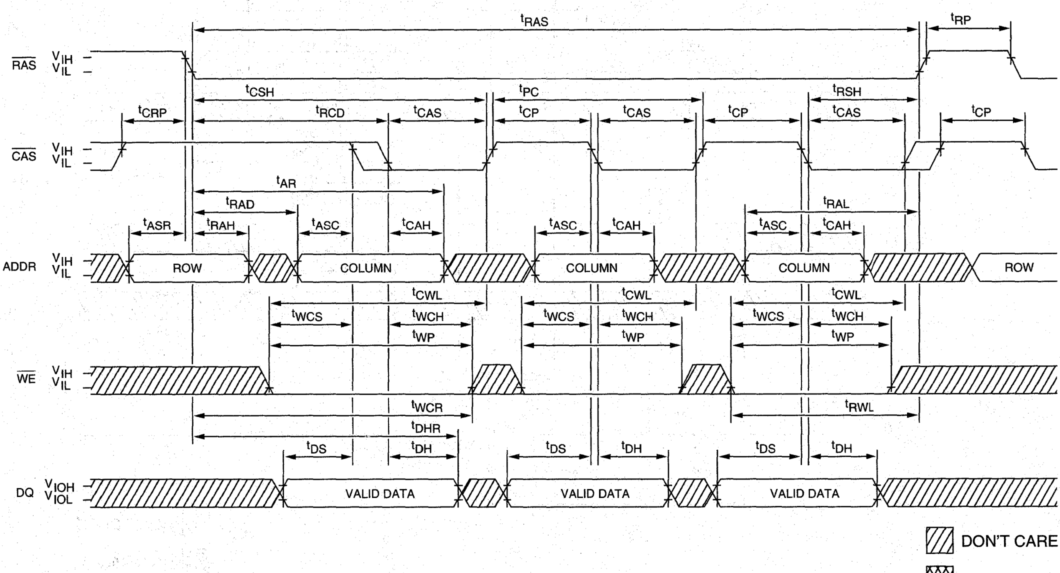
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DRAM SIMM

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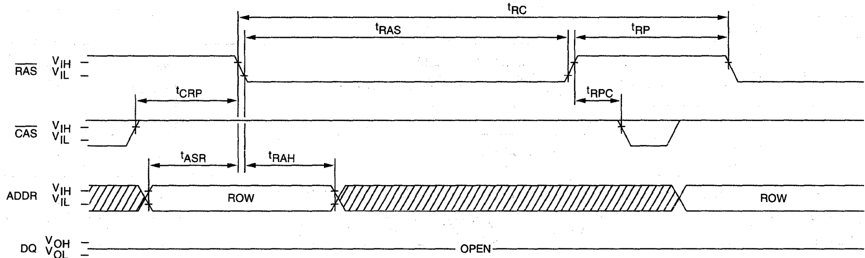
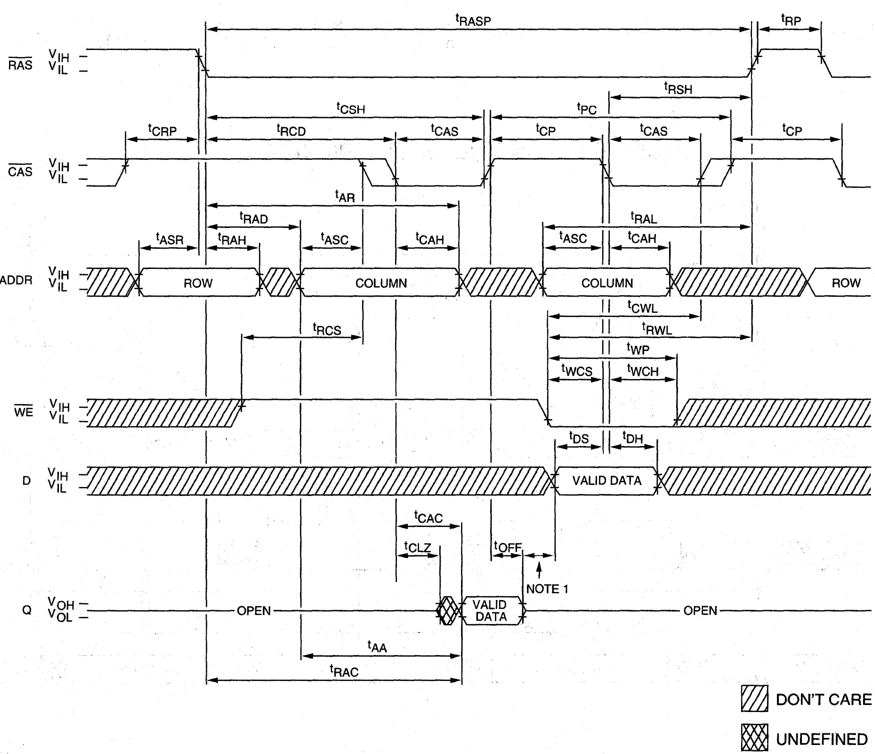
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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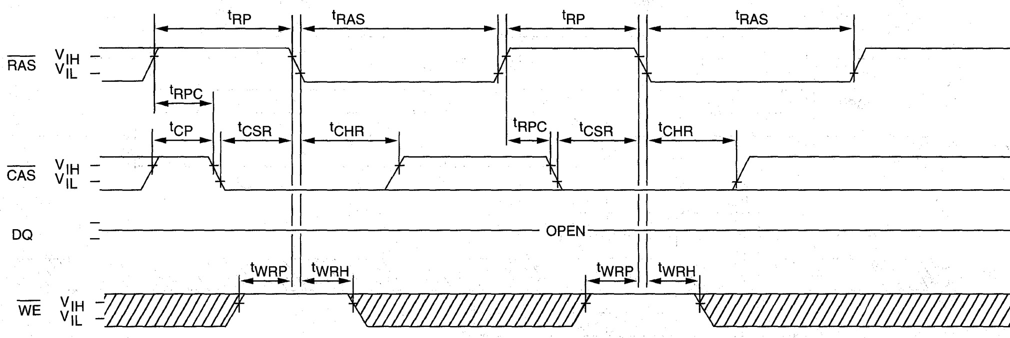
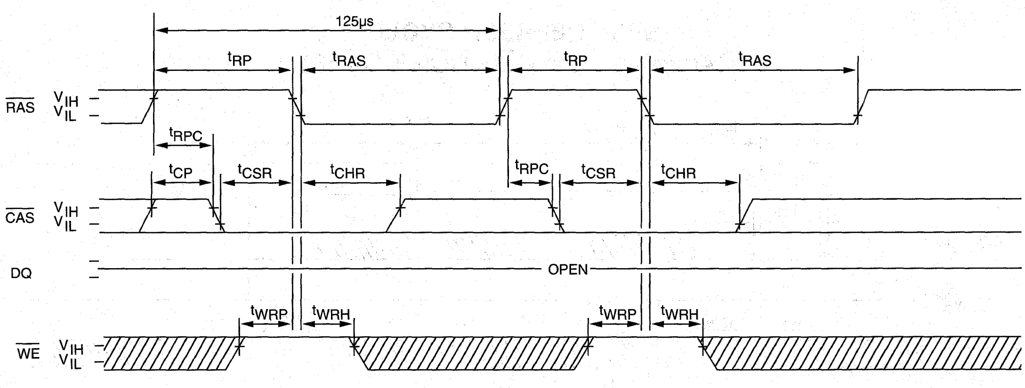
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(Addresses = DON'T CARE)



DON'T CARE

UNDEFINED

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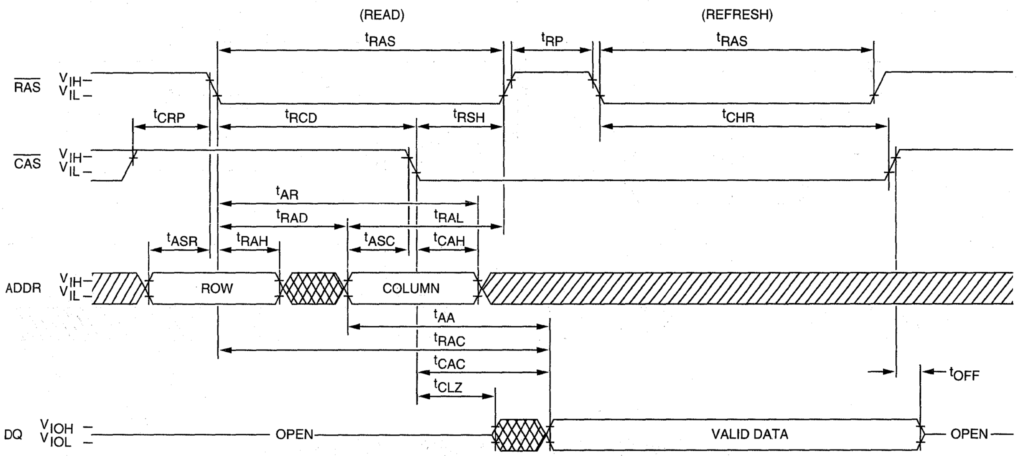
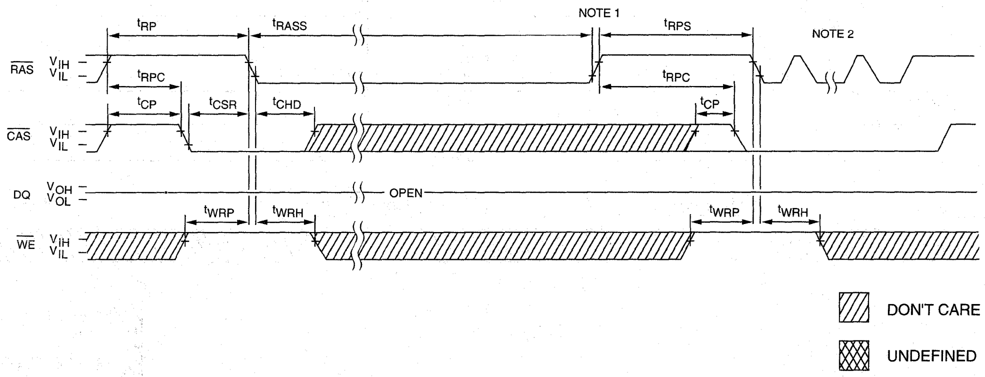
HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



SELF REFRESH CYCLE
(Addresses and OE = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTE, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC-standard pinout in a 72-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 9.6mW standby; 800mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF REFRESH
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)
- 3.3V mechanical key

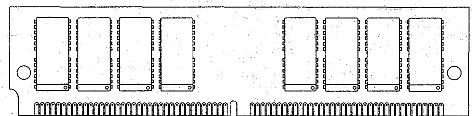
OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Components	
SOJ	D
TSOP	DT
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE	X
• Refresh	
Standard/16ms	Blank
SELF REFRESH/128ms	S

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-14) TSOP, (DD-16) SOJ - 1 Meg x 32
(DD-15) TSOP, (DD-17) SOJ - 2 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$*	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

*8MB version only

KEY TIMING PARAMETERS

EDO option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	18ns	10ns
-7	130ns	70ns	30ns	35ns	22ns	15ns
-8	150ns	80ns	35ns	40ns	22ns	15ns

FPM option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	25ns	60ns

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VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8LDT132G-xx	1 Meg x 32 FPM, TSOP, Gold
MT8LDT132G-xx S	1 Meg x 32 FPM, S*, TSOP, Gold
MT8LD132G-xx X	1 Meg x 32 EDO, SOJ, Gold
MT8LD132G-xx XS	1 Meg x 32 EDO, S*, SOJ, Gold
MT8LDT132M-xx	1 Meg x 32 FPM, TSOP, Tin/Lead
MT8LDT132M-xx S	1 Meg x 32 FPM, S*, TSOP, Tin/Lead
MT8LD132M-xx X	1 Meg x 32 EDO, SOJ, Tin/Lead
MT8LD132M-xx XS	1 Meg x 32 EDO, S*, SOJ, Tin/Lead
MT16LDT232G-xx	2 Meg x 32 FPM, TSOP, Gold
MT16LDT232G-xx S	2 Meg x 32 FPM, S*, TSOP, Gold
MT16LD232G-xx X	2 Meg x 32 EDO, SOJ, Gold
MT16LD232G-xx XS	2 Meg x 32 EDO, S*, SOJ, Gold
MT16LDT232M-xx	2 Meg x 32 FPM, TSOP, Tin/Lead
MT16LDT232M-xx S	2 Meg x 32 FPM, S*, TSOP, Tin/Lead
MT16LD232M-xx X	2 Meg x 32 EDO, SOJ, Tin/Lead
MT16LD232M-xx XS	2 Meg x 32 EDO, S*, SOJ, Tin/Lead

*S = SELF REFRESH

GENERAL DESCRIPTION

The MT8LD(T)132(X)(S) and MT16LD(T)232(X)(S) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration with optional SELF REFRESH. They are specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS latches the first 10 bits and CAS latches the latter 10 bits.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z (reference MT4LC4007J(S) DRAM data sheet for additional information on EDO functionality).

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS addresses (A0-A9) are executed at least every 16ms (128ms on "S" version), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs, prior to the resumption of normal operation.

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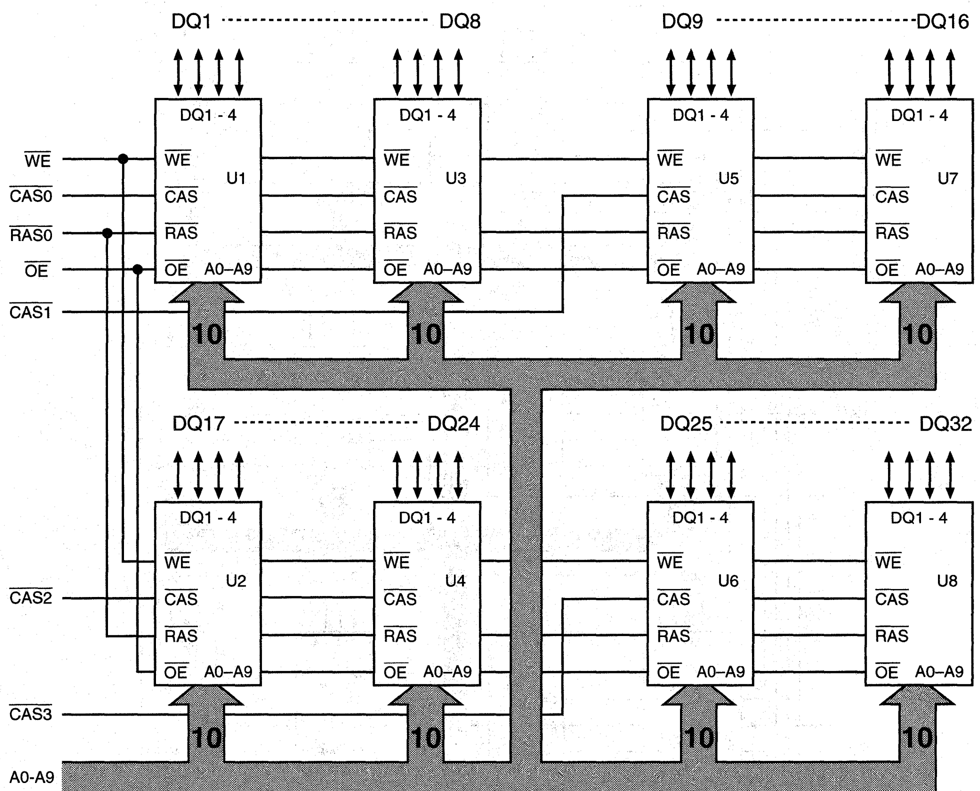
FUNCTIONAL BLOCK DIAGRAM
MT8LD(T)132 (4MB)



1 Meg x 32 EDO PAGE MODE
U1-U8 = MT4LC4007J(S)

1 Meg x 32 FAST PAGE MODE
U1-U8 = MT4LC4001J(S)

NOTE: 1. See package drawing for U1-U8 placement locations.
2. $\overline{OE}$ must be tied to Vss if not required.

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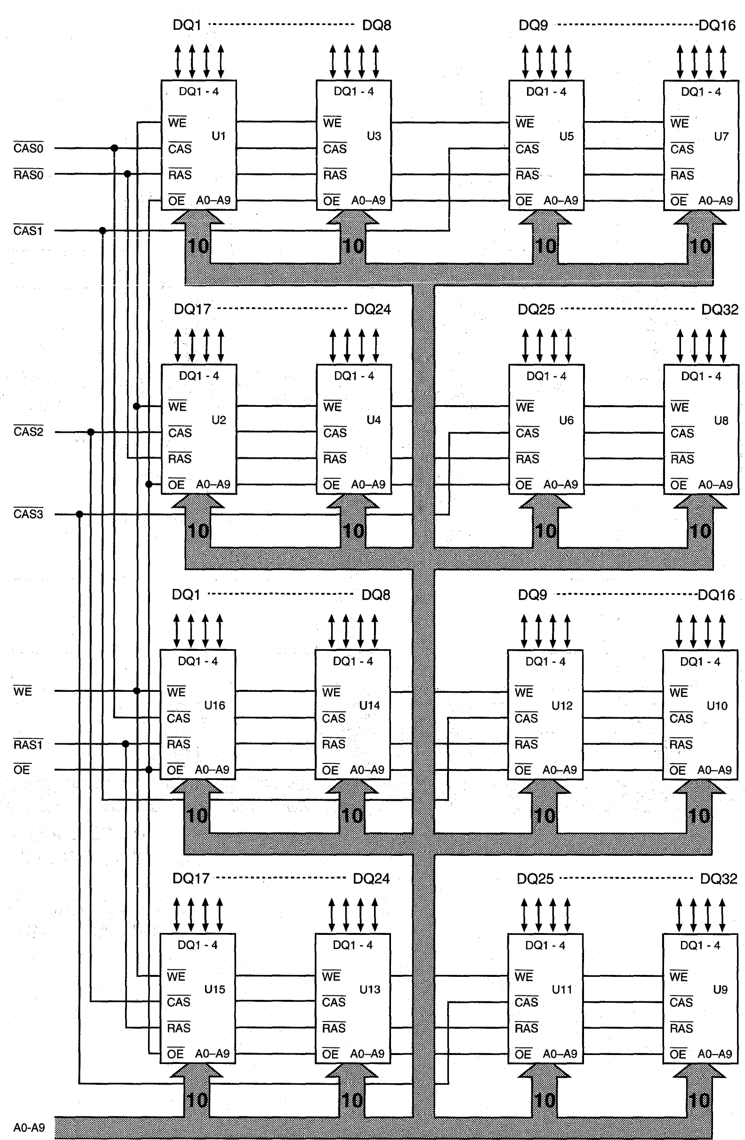
FUNCTIONAL BLOCK DIAGRAM
MT16LD(T)232 (8MB)



2 Meg x 32 EDO PAGE MODE
U1-U16 = MT4LC4007J(S)

2 Meg x 32 FAST PAGE MODE
U1-U16 = MT4LC4001J(S)

NOTE: 1. See package drawing for U1-U16 placement locations.
2. $\overline{OE}$ must be tied to Vss if not required.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	High-Z

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)						
Module Density	Module Organization	Row/Column Addresses			BANKS	1	2	5	3	4	
0MB	No module installed	X			X	NC	NC	NC			
2MB	512K x 32/36	9/9			2	Vss	NC	Vss			
2MB	512K x 32/36	10/9			1	Vss	NC	NC			
• 4MB	1 Meg x 32/36	10/10			1	Vss	Vss	NC			
4MB	1 Meg x 32/36	10/9			2	Vss	Vss	Vss			
• 8MB	2 Meg x 32/36	10/10			2	NC	NC	NC			
8MB	2 Meg x 32/36	11/10			1	NC	NC	Vss			
16MB	4 Meg x 32/36	12/11			1	NC	Vss	Vss			
16MB	4 Meg x 32/36	11/10			2	Vss	NC	Vss			
32MB	8 Meg x 32/36	12/11			2	NC	Vss	NC			
32MB	8 Meg x 32/36	12/11			1	NC	Vss	Vss			
Access Timing Detect		80ns							NC	Vss	
		70ns							Vss	NC	
		60ns							NC	NC	
		50ns							Vss	Vss	
Refresh Detect		Standard		Vss							
		Self		NC							
Fast Page Mode/EDO Detect		Fast Page	Vss								
		EDO	NC								
ECC/Parity Detect		ECC									Vss
		Parity/Non-Parity									NC

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +4.6V
Voltage on Any Inputs or I/O Pins
Relative to V_{SS} .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	I_{I1}	-8	8	µA	33
Any input 0V ≤ V_{IN} ≤ 5.5V	A0-A9, $\overline{WE}$, $\overline{OE}$	I_{I2}	-32	32	µA	33
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS1}$	I_{I3}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ1-DQ32	I_{OZ}	-20	20	µA	33
OUTPUT LEVELS	High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
	Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	4MB	8	8	8	mA	
		8MB	16	16	16		
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	4MB	4	4	4	mA	
		8MB	8	8	8		
	ICC2 (S only)	4MB	0.8	0.8	0.8	mA	
		8MB	1.6	1.6	1.6		
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	4MB	640	560	480	mA	2, 22, 26
		8MB	648	568	488		
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	4MB	480	400	320	mA	2, 22, 26
		8MB	488	408	328		
OPERATING CURRENT: EDO PAGE MODE (X-version only) Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC5 (X only)	4MB	480	400	320	mA	2, 22, 26
		8MB	488	408	328		
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC6	4MB	640	560	480	mA	22, 26
		8MB	648	568	488		
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC7	4MB	640	560	480	mA	22, 19
		8MB	648	568	488		
REFRESH CURRENT: Extended (S-version only) Average power supply current CAS = 0.2V or CBR cycling; RAS = tRAS (MIN); WE = Vcc -0.2V; OE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); tRC = 125µs (1,024 rows at 125µs = 128ms)	ICC8 (S only)	4MB	1.2	1.2	1.2	mA	19, 22
		8MB	2.0	2.0	2.0		
REFRESH CURRENT: SELF (S-version only) Average power supply current during SELF REFRESH; CBR cycling with RAS ≥ tRASS (MIN) and CAS held LOW; WE = Vcc -0.2V; OE, A0-A9 and DIN = Vcc -0.2V or 0.2V (DIN may be left open)	ICC9 (S only)	4MB	1.2	1.2	1.2	mA	19
		8MB	2.0	2.0	2.0		

CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A9	CI1	48	95	pF	17
Input Capacitance: WE	CI2	64	127	pF	17
Input Capacitance: RAS0-RAS1	CI3	64	64	pF	17
Input Capacitance: CAS0-CAS3	CI4	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	CIO	10	18	pF	17

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35		40	ns	
Column-address hold time (referenced to RAS)	tAR	45		50		55		ns	
Column-address setup time	tASC	0		0		0		ns	
Row-address setup time	tASR	0		0		0		ns	
Column-address to WE delay time	tAWD	55		65		70		ns	29
Access time from CAS	tCAC		15		20		20	ns	9
Column-address hold time	tCAH	10		15		15		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	10		10		10		ns	27
CAS hold time (CBR REFRESH)	tCHR	10		10		10		ns	19
CAS to output in Low-Z	tCLZ	3		3		3		ns	24
CAS precharge time	tCP	10		10		10		ns	18
Access time from CAS precharge	tCPA		35		40		45	ns	
CAS to RAS precharge time	tCRP	10		10		10		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	19
CAS to WE delay time	tCWD	40		50		50		ns	29
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in hold time	tDH	10		15		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Data-in setup time	tDS	0		0		0		ns	15
Output disable	tOD		15		20		20	ns	24, 31
Output Enable Time	tOE		15		20		20	ns	21
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	12, 24, 32
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		0		ns	12
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		100		105		ns	
Access time from RAS	tRAC		60		70		80	ns	8
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	23
Row-address hold time	tRAH	10		10		10		ns	

DRAM SIMM

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		0		ns	14
Read command setup time	^{t}RCS	0		0		0		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
Refresh period (1,024 cycles) S version	^{t}REF		128		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		150		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		0		ns	14
$\overline{RAS}$ hold time	^{t}RSH	15		20		20		ns	
READ WRITE cycle time	^{t}RWC	150		180		200		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		100		110		ns	29
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	29, 31
Write command pulse width	^{t}WP	10		15		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	28

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35		40	ns	
Column-address setup to $\overline{CAS}$ precharge during WRITE	^{t}ACH	15		15		20		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		55		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		65		70		ns	29
Access time from $\overline{CAS}$	^{t}CAC		18		22		22	ns	9
Column-address hold time	^{t}CAH	10		15		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	10	10,000	15	10,000	15	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	10		10		10		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	24
Data output hold after $\overline{CAS}$ LOW	^{t}COH	5		5		5		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		10		ns	18
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40		45	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	50		55		65		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		10		ns	19
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		50		50		ns	29
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	
Data-in hold time	^{t}DH	10		15		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
Data-in setup time	^{t}DS	0		0		0		ns	15
Output disable	^{t}OD		15		20		20	ns	31
Output Enable Time	^{t}OE		15		20		20	ns	21
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^{t}OEHC	10		10		10		ns	
$\overline{OE}$ HIGH pulse width	^{t}OEP	10		10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^{t}OES	5		5		5		ns	
Output buffer turn-off delay	^{t}OFF	3	15	3	20	3	20	ns	12, 24, 32
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		33		35		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		100		105		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	23
Row-address hold time	^tRAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		100		µs	27
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	14
Read command setup time	^tRCS	0		0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16		16	ms	
Refresh period (1,024 cycles) S version	^tREF		128		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		150		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	14
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
READ WRITE cycle time	^tRWC	150		180		200		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	85		100		110		ns	29
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Transition time (rise or fall)	^tT	2	50	2	50	2	50	ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	29, 31
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	^tWHZ	3	15	3	15	3	15	ns	
Write command pulse width	^tWP	10		15		15		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	^tWPZ	10		10		10		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	28

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 5ns for FPM and 2.5ns for EDO.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If CAS and RAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
21. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
22. Icc is dependent on cycle rates.
23. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Refresh current increases if ᵗRAS is extended beyond its minimum specification.
26. Column-address changed once each cycle.
27. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
28. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
29. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are not restrictive operating parameters. ᵗWCS applies to EARLY WRITE cycles. ᵗRWD, ᵗAWD and ᵗCWD apply to READ-MODIFY-WRITE cycles. If ᵗWCS ≥ ᵗWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ᵗWCS < ᵗWCS (MIN) and ᵗRWD ≥ ᵗRWD (MIN), ᵗAWD ≥ ᵗAWD (MIN) and ᵗCWD ≥ ᵗCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ᵗWCS, ᵗRWD, ᵗCWD and ᵗAWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

30. LATE WRITE and READ-MODIFY-WRITE cycles must have both ᵗOD and ᵗOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ᵗOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
31. The DQs open during READ cycles once ᵗOD or ᵗOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
32. For FAST-PAGE-MODE option, ᵗOFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ᵗOFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
33. 4MB modules will have values half of those shown.
34. Applies to both EDO and FAST PAGE MODEs.

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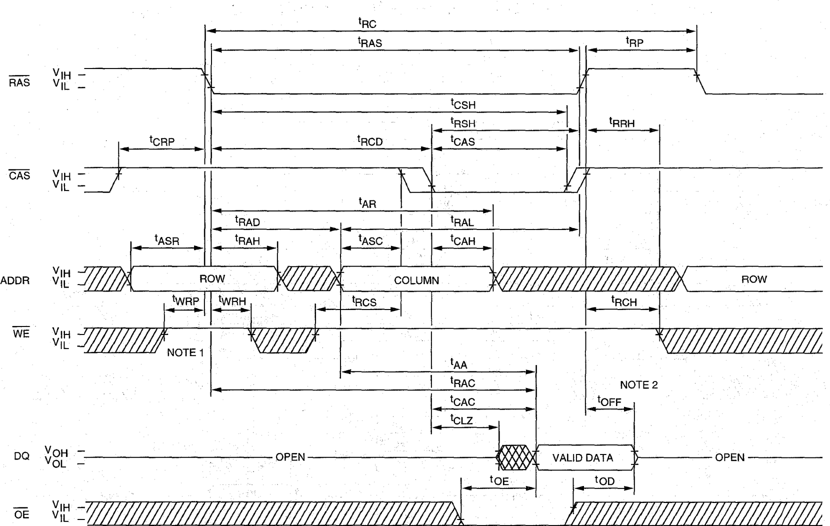
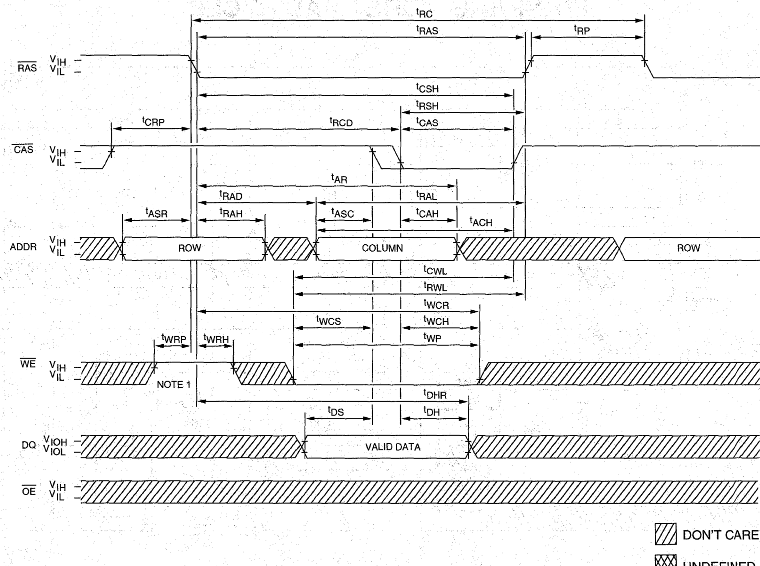
READ CYCLE [34]



EARLY WRITE CYCLE [34]



NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ${}^tOFF$ is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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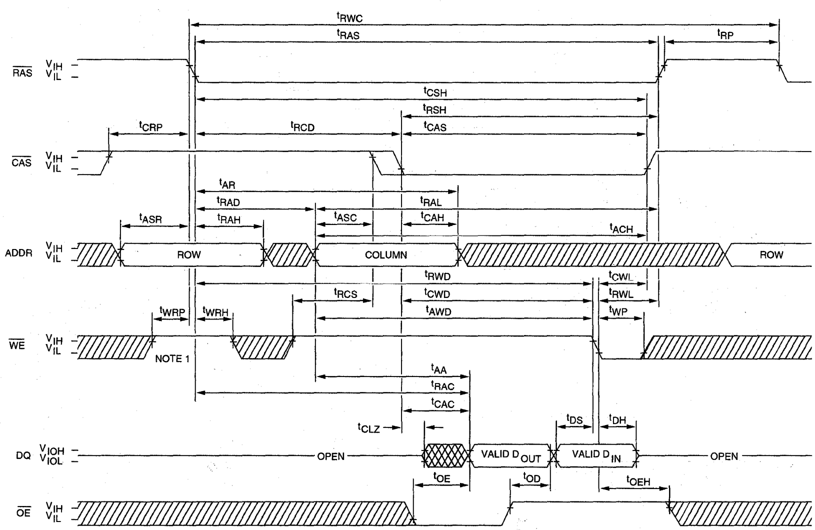
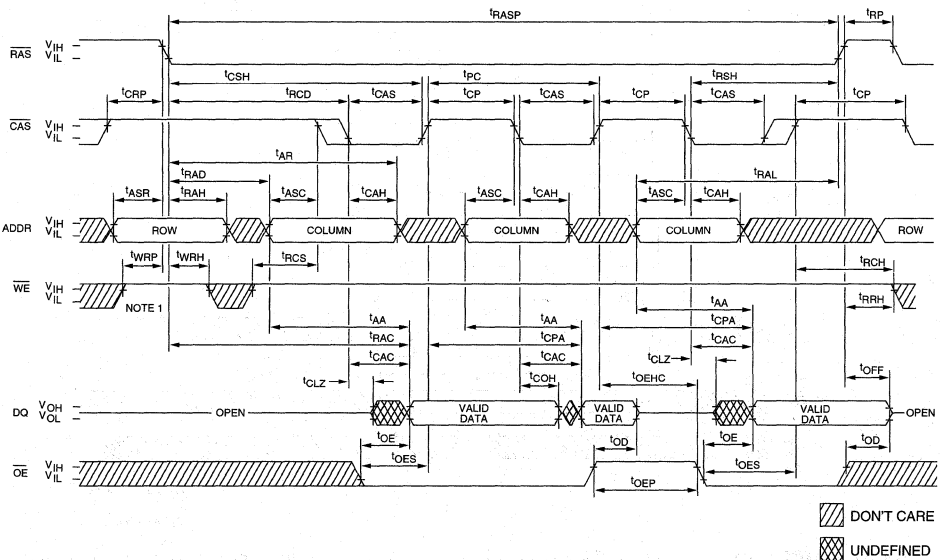
READ WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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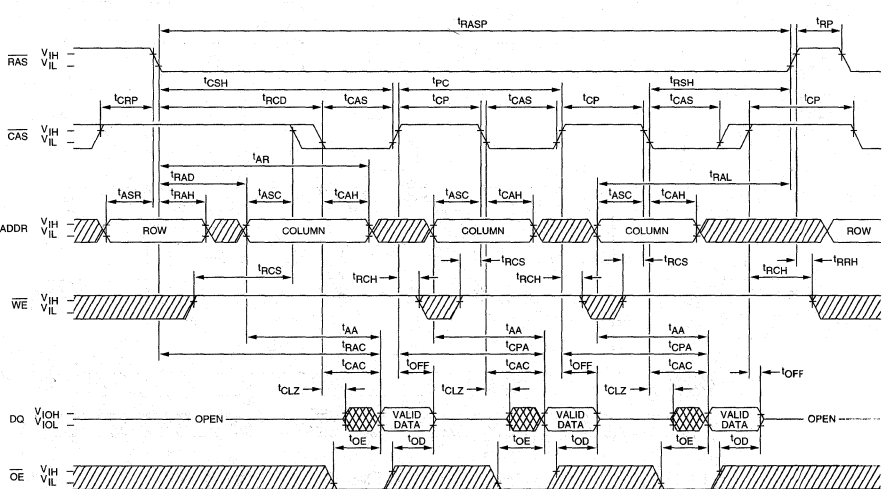
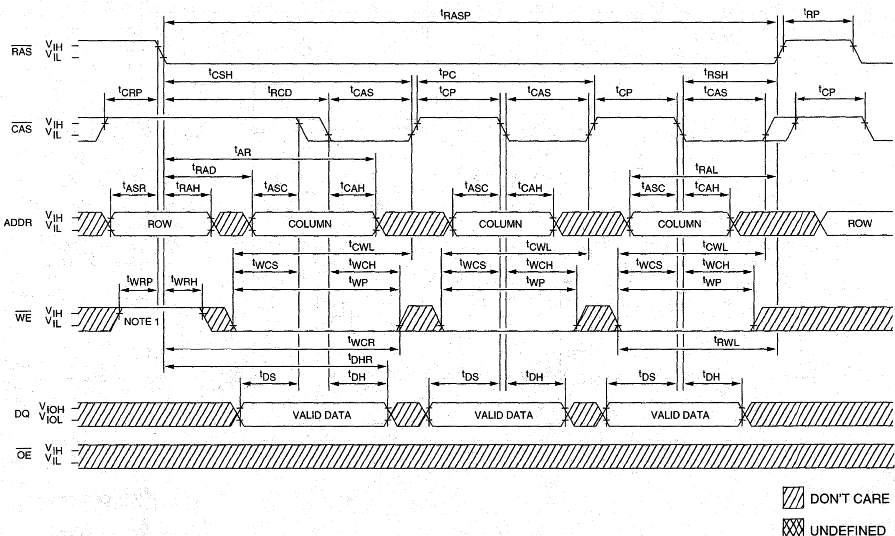
FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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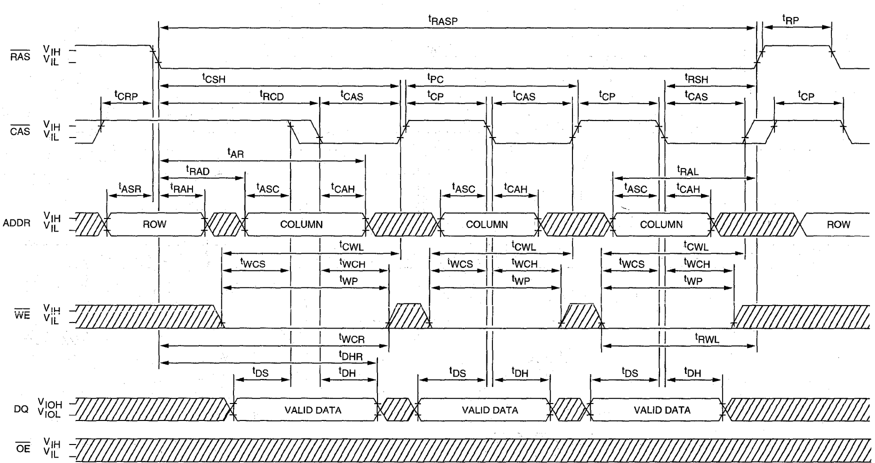
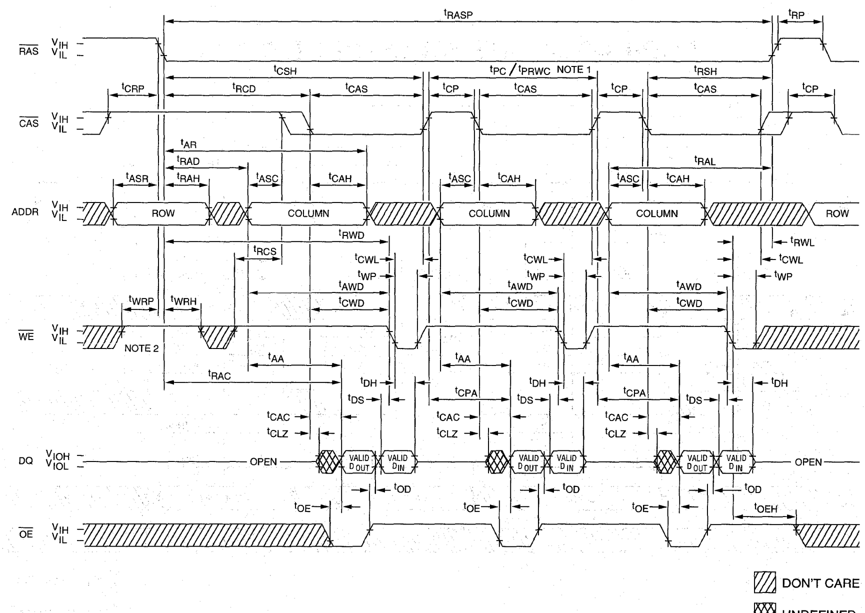
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO/FAST PAGE-MODE READ-WRITE CYCLE [34]
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. ᵗPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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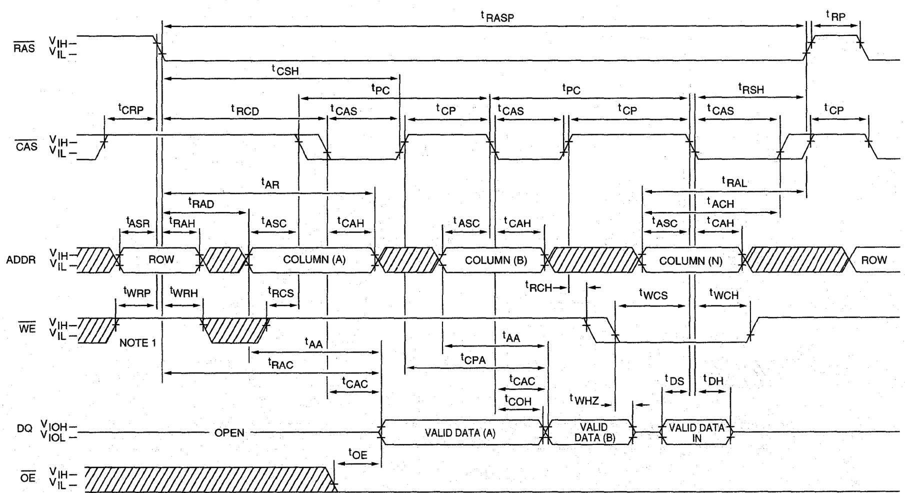
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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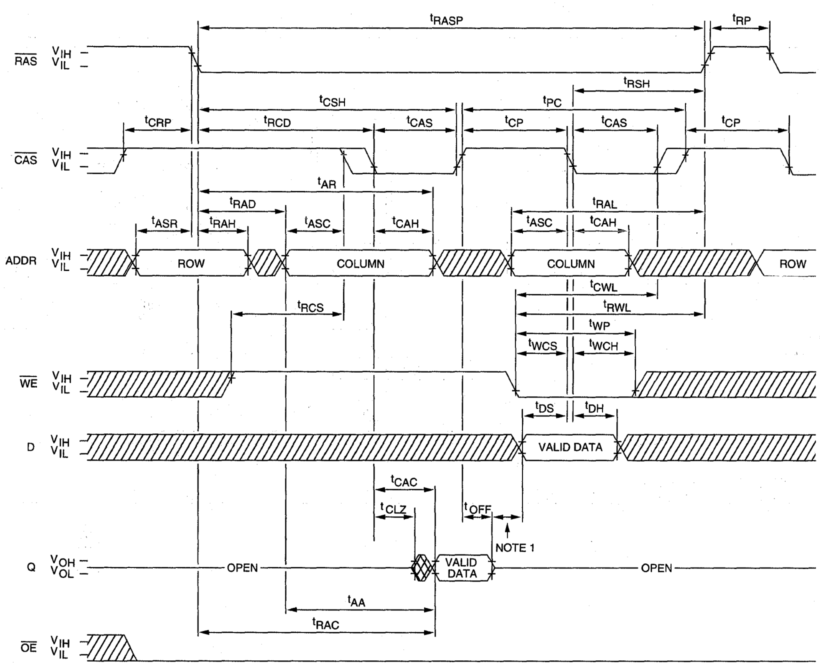
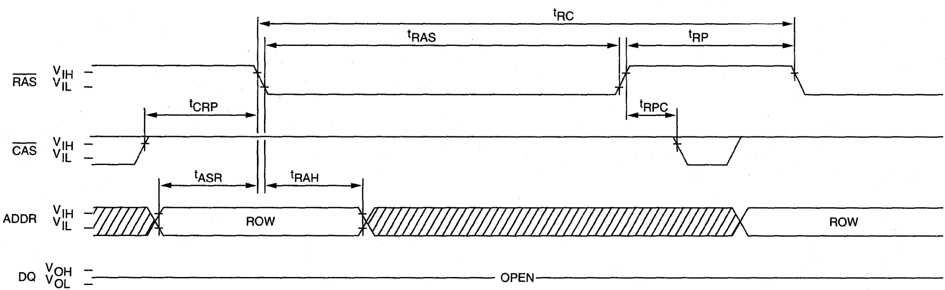
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE [34]
(WE = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Do not drive data prior to tristate.

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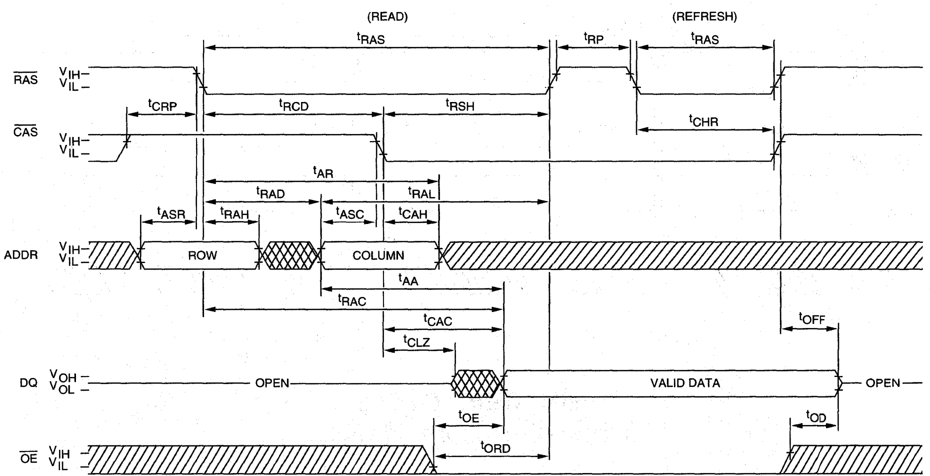
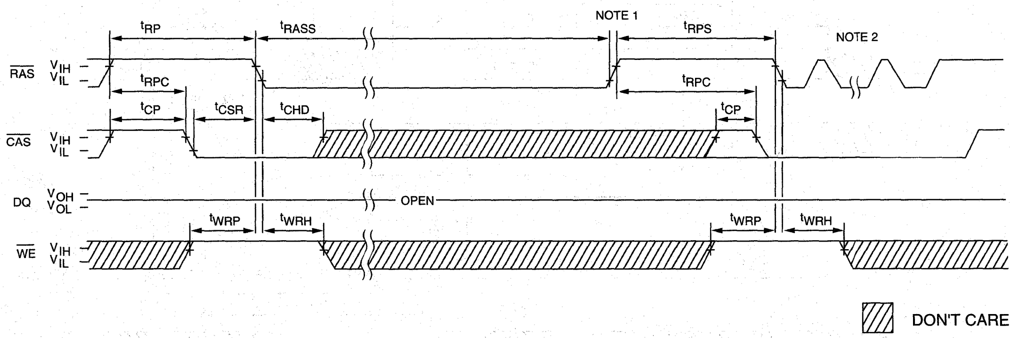
HIDDEN REFRESH CYCLE [20, 34]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



SELF REFRESH CYCLE [34]

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

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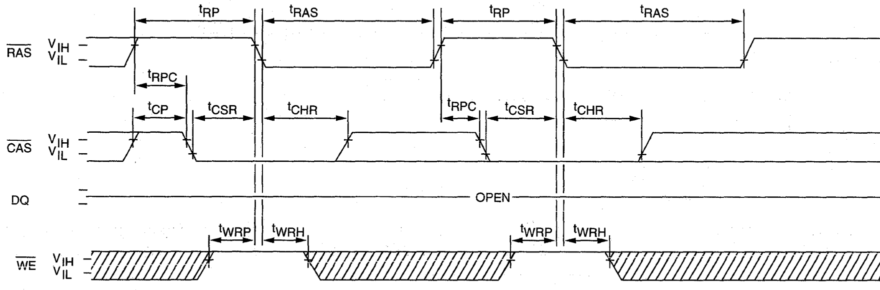
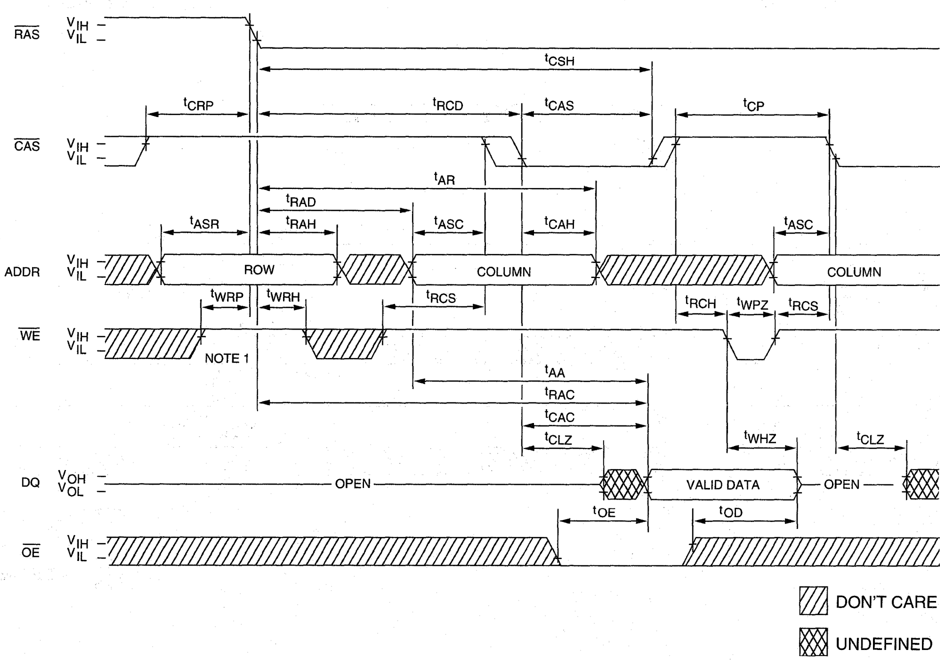
CBR REFRESH CYCLE [34]
(Addresses and $\overline{OE}$ = DON'T CARE)



EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM MODULE

2 MEG x 32

8 MEGABYTE, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC-standard pinout in a 72-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 4mW standby; 800mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF REFRESH modes
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)
- 3.3V mechanical key

OPTIONS — MARKING

OPTIONS	MARKING
Timing	
60ns access	-6
70ns access	-7
Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE	X
Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

EDO option

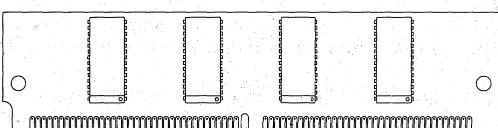
SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

FPM option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

72-Pin SIMM
(DD-18)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	NC	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT4LD232G-xx	2 Meg x 32 FPM, SOJ, Gold
MT4LD232G-xx S	2 Meg x 32 FPM, S*, SOJ, Gold
MT4LD232G-xx X	2 Meg x 32 EDO, SOJ, Gold
MT4LD232G-xx XS	2 Meg x 32 EDO, S*, SOJ, Gold
MT4LD232M-xx	2 Meg x 32 FPM, SOJ, Tin/Lead
MT4LD232M-xx S	2 Meg x 32 FPM, S*, SOJ, Tin/Lead
MT4LD232M-xx X	2 Meg x 32 EDO, SOJ, Tin/Lead
MT4LD232M-xx XS	2 Meg x 32 EDO, S*, SOJ, Tin/Lead

*S = SELF REFRESH

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GENERAL DESCRIPTION

The MT4LD232 (X)(S) is a randomly accessed 16MB and 32MB solid-state memory organized in a x32 configuration with optional SELF REFRESH. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles each bit is uniquely addressed through the address bits, RAS latches the first 11 bits and CAS latches the latter 10 bits (A10 is ignored during CAS falling edge). READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

If WE goes LOW after CAS goes LOW, data-out (Q) is activated and retains the selected cell data as long as OE remains LOW and RAS and CAS remains LOW (regardless of WE). This late WE pulse results in a READ WRITE cycle. If WE toggles LOW after CAS goes back HIGH, the output pins will open (High-Z) until the next CAS cycle, regardless of OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z (reference the MT4LC2M8E7(S) DRAM data sheet for additional information on EDO functionality).

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms (128ms on "S" version), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs, prior to the resumption of normal operation.

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FUNCTIONAL BLOCK DIAGRAM
8MB

$\overline{\text{CAS0}}$
$\overline{\text{RAS}}$
$\overline{\text{OE}}$
$\overline{\text{WE}}$
$\overline{\text{CAS1}}$
A0-A10
$\overline{\text{CAS2}}$
$\overline{\text{CAS3}}$

11
A0-A10
U1
$\overline{\text{WE}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
$\overline{\text{OE}}$
DQ1-DQ8
8

11
A0-A10
U2
$\overline{\text{WE}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
$\overline{\text{OE}}$
DQ9-DQ16
8

11
A0-A10
U3
$\overline{\text{WE}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
$\overline{\text{OE}}$
DQ17-DQ24
8

11
A0-A10
U4
$\overline{\text{WE}}$
$\overline{\text{CAS}}$
$\overline{\text{RAS}}$
$\overline{\text{OE}}$
DQ25-DQ32
8

32
DQ1-DQ32

EDO PAGE MODE
U1-U4 = MT4LC2M8E7DJ(S)

FAST PAGE MODE
U1-U4 = MT4LC2M8B1DJ(S)

NOTE: 1. $\overline{\text{OE}}$ must be tied to Vss if not required.

NEW ■ DRAM SIMM

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA-IN/OUT
						${}^{t}R$	${}^{t}C$	DQ1-DQ32
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	High-Z

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)						
Module Density	Module Organization	Row/Column Addresses			BANKS	1	2	5	3	4	
0MB	No module installed	X			X	NC	NC	NC			
2MB	512K x 32/36	9/9			2	Vss	NC	Vss			
2MB	512K x 32/36	10/9			1	Vss	NC	NC			
4MB	1 Meg x 32/36	10/10			1	Vss	Vss	NC			
4MB	1 Meg x 32/36	10/9			2	Vss	Vss	Vss			
8MB	2 Meg x 32/36	10/10			2	NC	NC	NC			
• 8MB	2 Meg x 32/36	11/10			1	NC	NC	Vss			
16MB	4 Meg x 32/36	12/11			1	NC	Vss	Vss			
16MB	4 Meg x 32/36	11/10			2	Vss	NC	Vss			
32MB	8 Meg x 32/36	12/11			2	NC	Vss	NC			
32MB	8 Meg x 32/36	12/11			1	NC	Vss	Vss			
Access Timing Detect		80ns							NC	Vss	
		70ns							Vss	NC	
		60ns							NC	NC	
		50ns							Vss	Vss	
Refresh Detect		Standard		Vss							
		Self		NC							
Fast Page Mode/EDO Detect		Fast Page	Vss								
		EDO	NC								
ECC/Parity Detect		ECC									Vss
		Parity/Non-Parity									NC

NOTE: Vss = ground.

NEW DRAM SIMM

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{CAS0}$-$\overline{CAS3}$	II1	-2	2	µA	
Any input 0V ≤ VIN ≤ 5.5V	A0-A9, $\overline{WE}$, $\overline{OE}$	II2	-8	8	µA	
(All other pins not under test = 0V) for each package input	$\overline{RAS0}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (IOUT = -2mA)	VOH	2.4		V	
	Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB	8	8	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	8MB	2	2	mA	
	I_{CC2} (S only)	8MB	.6	.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB	520	480	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB	360	320	mA	2, 22, 26
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4} (X only)	8MB	480	440	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	8MB	520	480	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	8MB	520	480	mA	22, 19
REFRESH CURRENT: Extended (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cyclig; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; $\overline{OE}$, A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	8MB	1.2	1.2	mA	19, 22
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; $\overline{OE}$,A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	8MB	1.2	1.2	mA	19

NEW DRAM SIMM

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}		24	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}		32	pF	17
Input Capacitance: $\overline{RAS0}$	C_{I3}		32	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}		10	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}		10	pF	17

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address hold time (referenced to RAS)	tAR	50		55		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to WE delay time	tAWD	55		60		ns	29
Access time from CAS	tCAC		15		20	ns	9
Column-address hold time	tCAH	10		15		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH cycle	tCHD	15		15		ns	27
CAS hold time (CBR REFRESH)	tCHR	15		15		ns	19
CAS to output in Low-Z	tCLZ	3		3		ns	24
CAS precharge time	tCP	10		10		ns	18
Access time from CAS precharge	tCPA		35		40	ns	
CAS to RAS precharge time	tCRP	5		5		ns	
CAS hold time	tCSH	60		70		ns	
CAS setup time (CBR REFRESH)	tCSR	5		5		ns	19
CAS to WE delay time	tCWD	40		45		ns	29
Write command to CAS lead time	tCWL	15		20		ns	
Data-in hold time	tDH	10		15		ns	15
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	15
Output disable	tOD	3	15	3	20	ns	24
Output Enable Time	tOE		15		20	ns	21
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	15		15		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	ns	12, 24, 31
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	12
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		ns	
Access time from RAS	tRAC		60		70	ns	8
RAS to column-address delay time	tRAD	15	30	15	35	ns	23
Row-address hold time	tRAH	10		10		ns	

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	14
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	14
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
READ WRITE cycle time	^{t}RWC	150		180		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		95		ns	29
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		ns	29
Write command pulse width	^{t}WP	10		15		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	^{t}WPZ	10		10		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	28

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	^{t}AA		30		35	ns	
Column-address setup to $\overline{CAS}$ precharge during WRITE	^{t}ACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		55		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		65		ns	29
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	9
Column-address hold time	^{t}CAH	10		12		ns	
$\overline{CAS}$ pulse width	^{t}CAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		12		ns	19
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		ns	
Data output hold after $\overline{CAS}$ LOW	^{t}COH	5		5		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		ns	
$\overline{CAS}$ hold time	^{t}CSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		ns	19
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	35		40		ns	29
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		15		ns	
Data-in hold time	^{t}DH	10		12		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	15
Output disable	^{t}OD	0	15	0	15	ns	
Output Enable Time	^{t}OE		15		15	ns	21
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	12		12		ns	
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^{t}OEHC	10		10		ns	
$\overline{OE}$ HIGH pulse width	^{t}OEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^{t}OES	5		5		ns	
Output buffer turn-off delay	^{t}OFF	3	15	3	15	ns	12, 24, 31
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	75		85		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	8
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	12	30	12	35	ns	23
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (EDO PAGE MODE)	^{t}RASP	60	125,000	70	125,000	ns	
$\overline{\text{RAS}}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	14	45	14	50	ns	13
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		ns	14
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) S version	^{t}REF		128		128	ms	
$\overline{\text{RAS}}$ precharge time	^{t}RP	40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		ns	
$\overline{\text{RAS}}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		ns	27
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		ns	14
$\overline{\text{RAS}}$ hold time	^{t}RSH	10		12		ns	
READ WRITE cycle time	^{t}RWC	150		177		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	80		90		ns	29
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
Write command hold time	^{t}WCH	10		12		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		ns	
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		ns	29
Output disable delay from $\overline{\text{WE}}$ ($\overline{\text{CAS}}$ HIGH)	^{t}WHZ	0	13	0	15	ns	
Write command pulse width	^{t}WP	10		12		ns	
$\overline{\text{WE}}$ pulse width for output disable when $\overline{\text{CAS}}$ HIGH	^{t}WPZ	10		12		ns	
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	28
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	28

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NEW DRAM SIMM

NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 2.5ns for EDO and 5ns for FPM.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If CAS and RAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Vcc = 3.3V ±0.3V; f = 1 MHz.
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
21. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
22. Icc is dependent on cycle rates.
23. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Refresh current increases if ᵗRAS is extended beyond its minimum specification.
26. Column-address changed once each cycle.
27. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
28. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
29. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are not restrictive operating parameters. ᵗWCS applies to EARLY WRITE cycles. ᵗRWD, ᵗAWD and ᵗCWD apply to READ-MODIFY-WRITE cycles. If ᵗWCS ≥ ᵗWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ᵗWCS < ᵗWCS (MIN) and ᵗRWD ≥ ᵗRWD (MIN), ᵗAWD ≥ ᵗAWD (MIN) and ᵗCWD ≥ ᵗCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ᵗWCS, ᵗRWD, ᵗCWD and ᵗAWD are not applicable in a LATE WRITE cycle.
30. LATE WRITE and READ-MODIFY-WRITE cycles must have both ᵗOD and ᵗOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE is taken back LOW while CAS remains LOW, the DQs will remain open.
31. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
32. Applies to both EDO and FAST PAGE MODEs.

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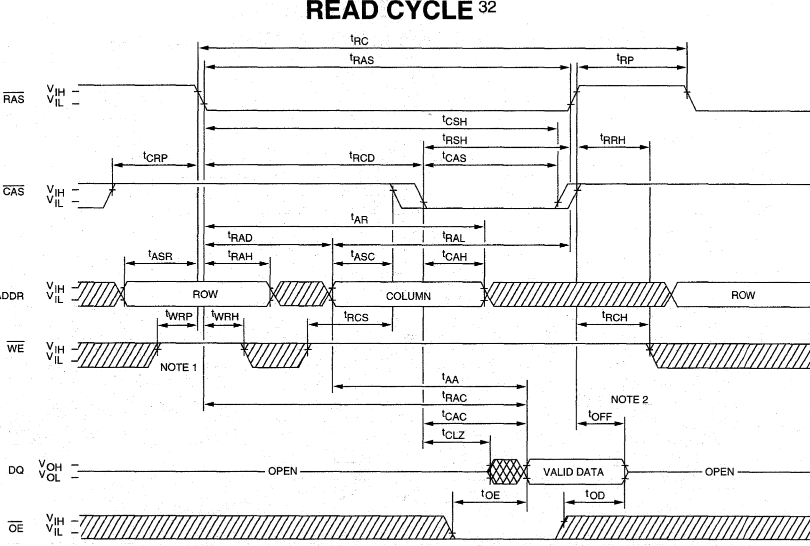
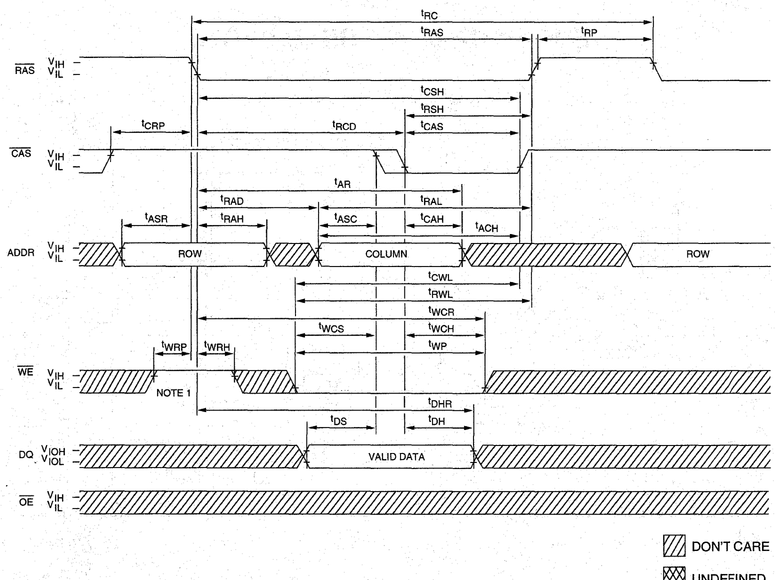
READ CYCLE [32]



EARLY WRITE CYCLE [32]



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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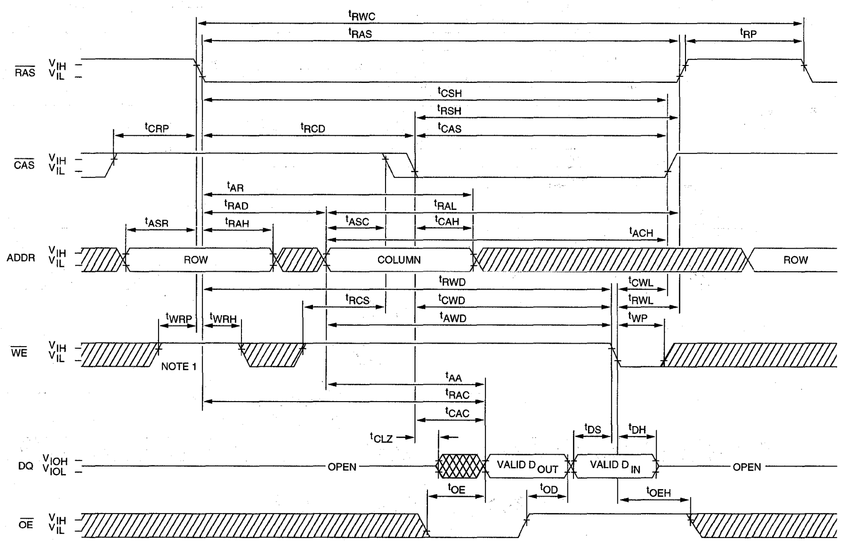
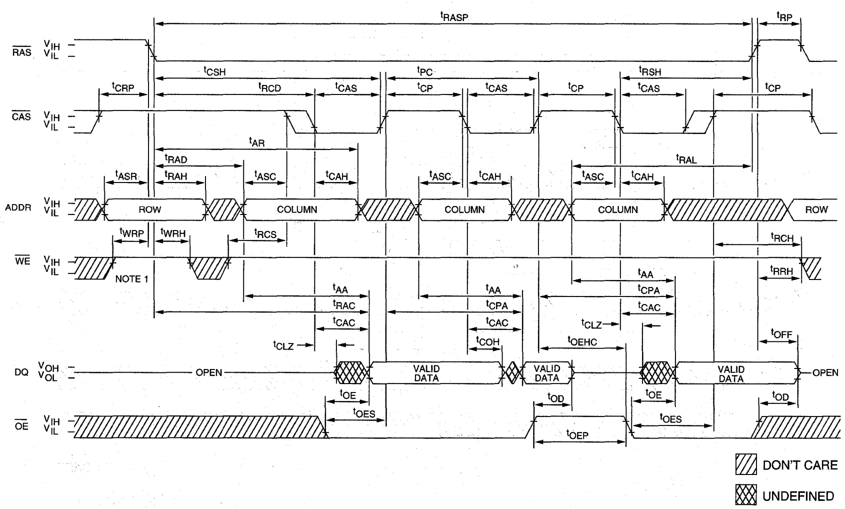
READ WRITE CYCLE [32]

(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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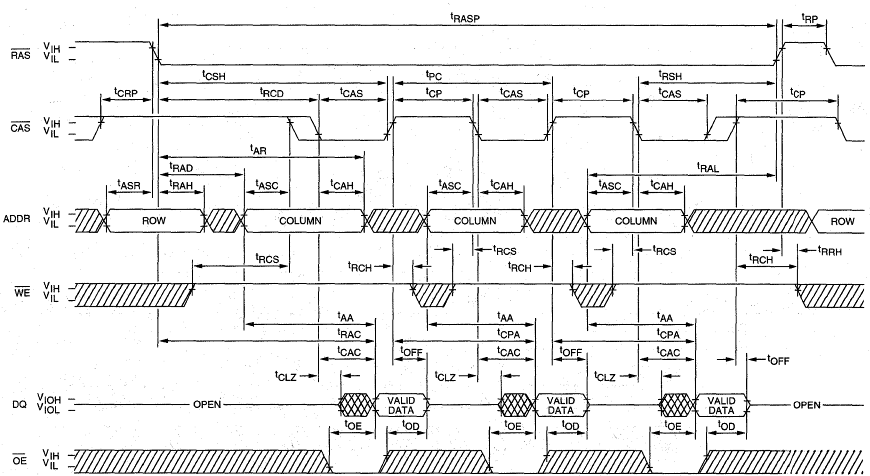
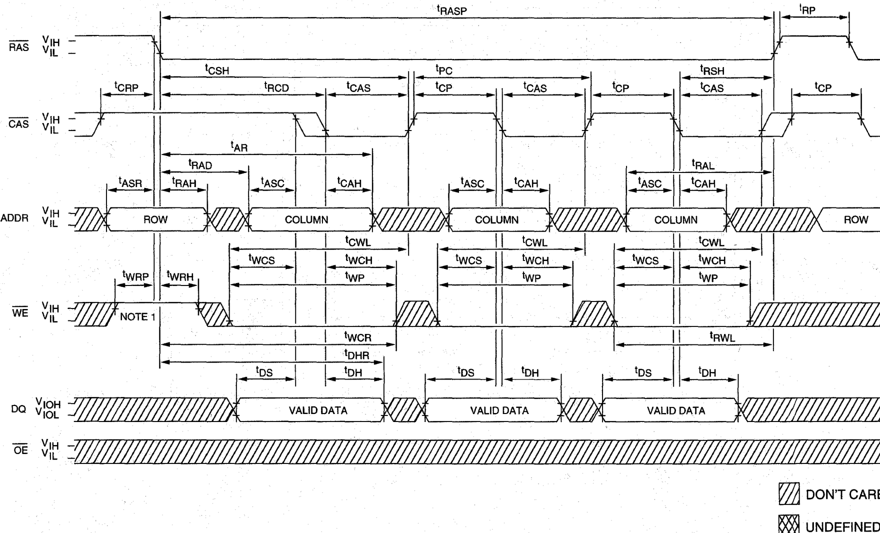
FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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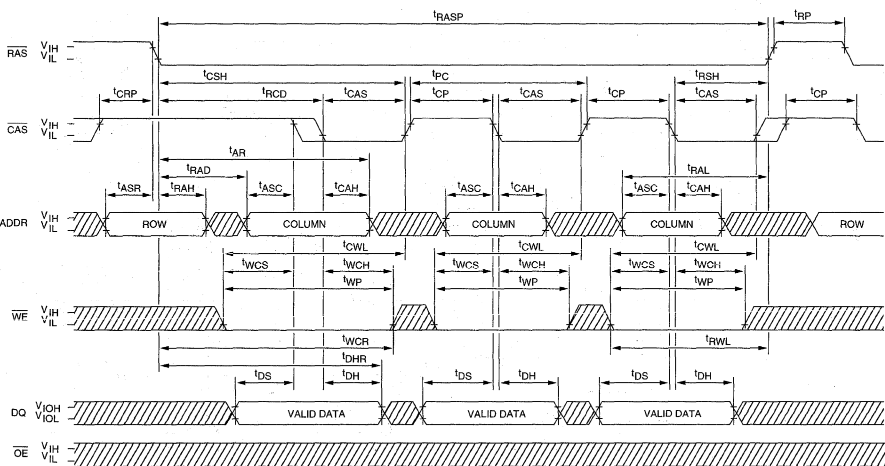
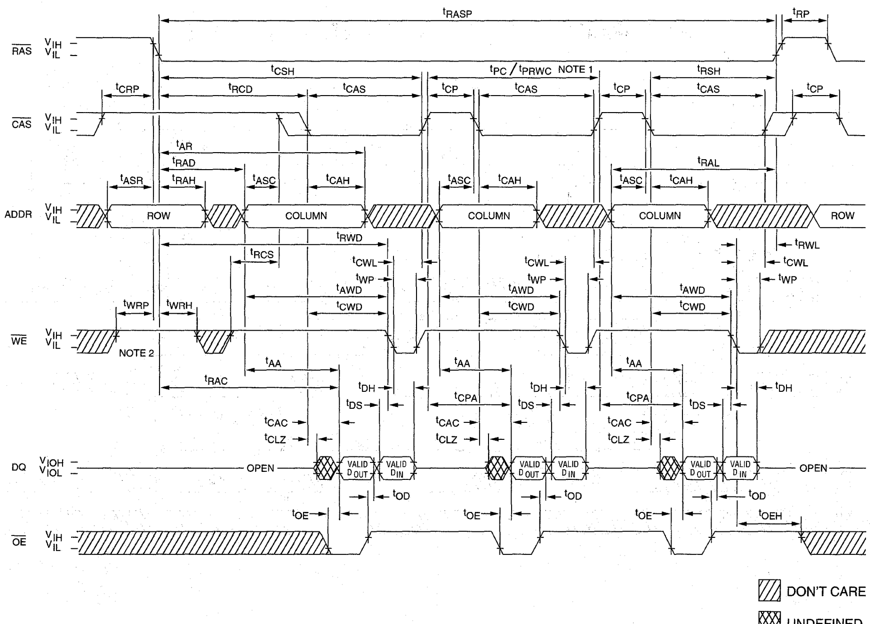
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO/FAST PAGE-MODE READ-WRITE CYCLE [32]
(LATE WRITE and READ-MODIFY-WRITE cycles)



DON'T CARE

UNDEFINED

NOTE:
1. ^{t}PC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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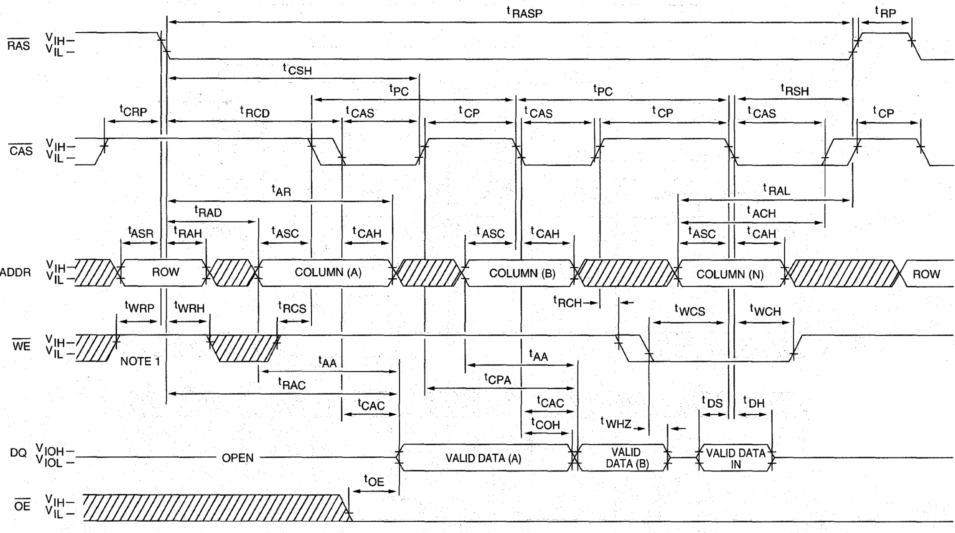
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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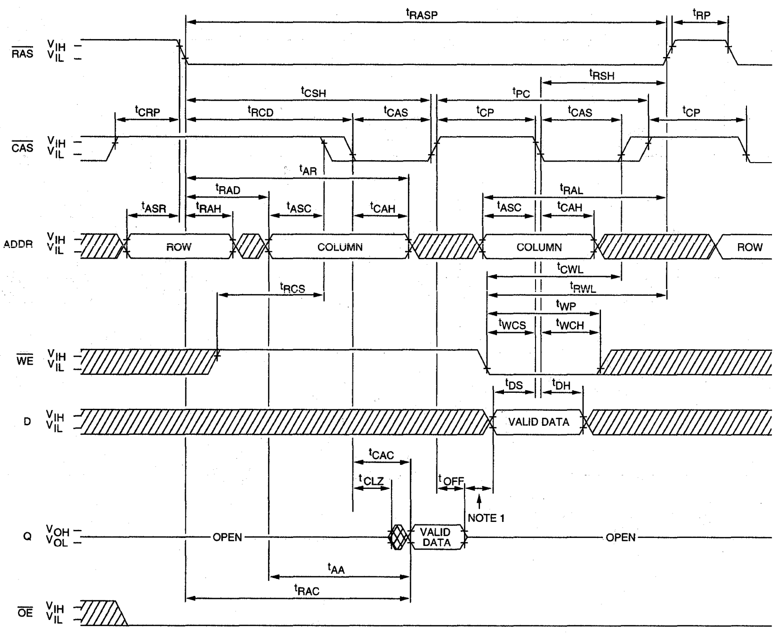
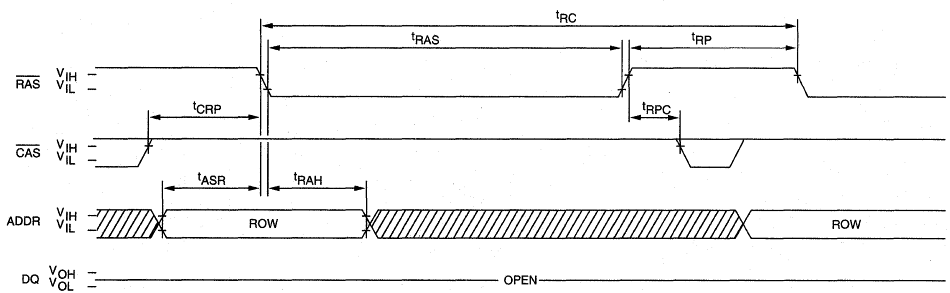
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



RAS-ONLY REFRESH CYCLE [32]
(WE = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Do not drive data prior to tristate.

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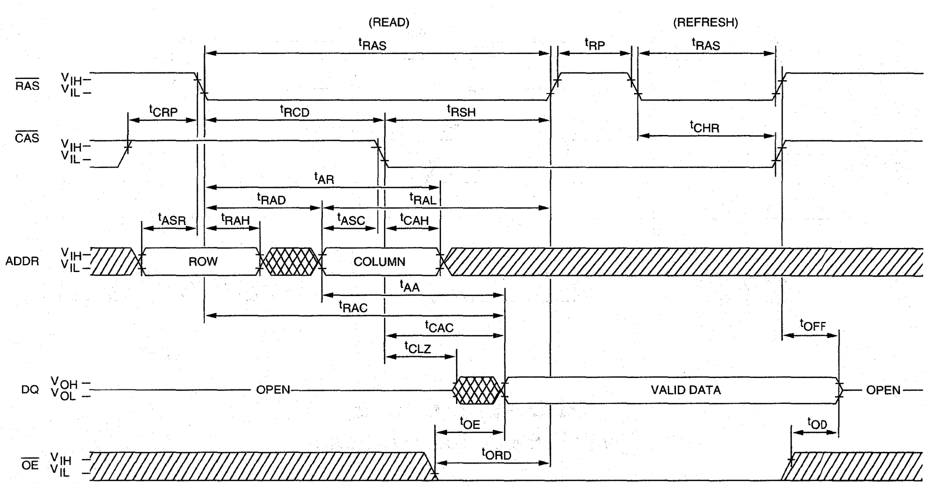
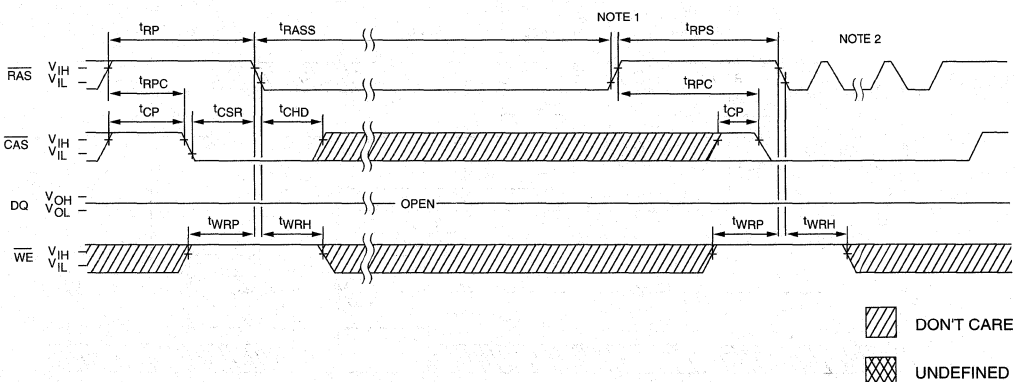
HIDDEN REFRESH CYCLE [20, 32]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



SELF REFRESH CYCLE [32]
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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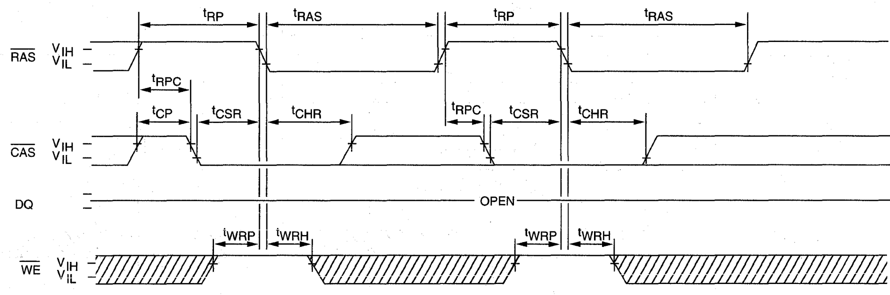
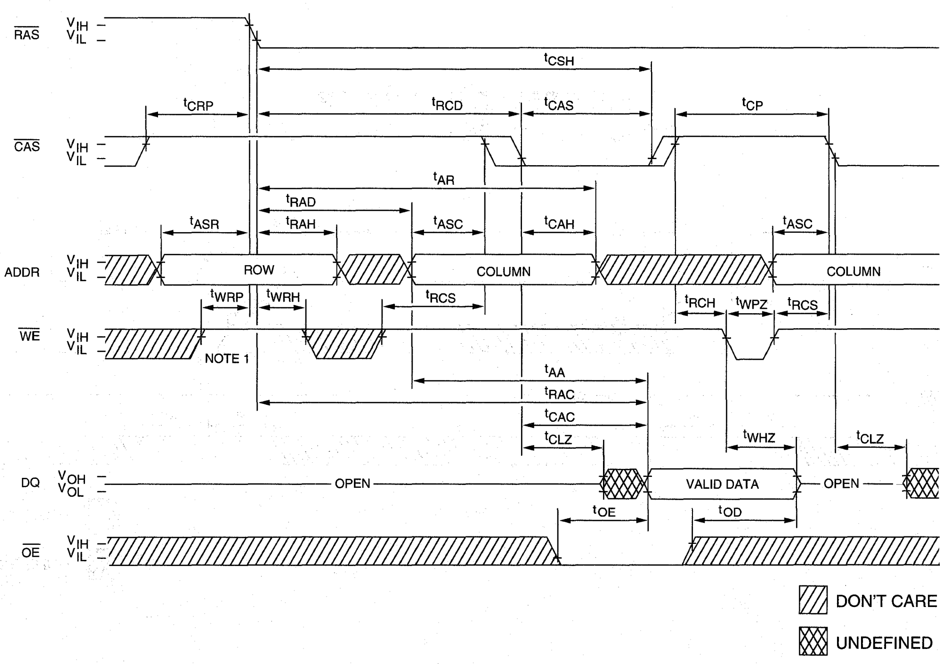
CBR REFRESH CYCLE [32]

(Addresses and $\overline{OE}$ = DON'T CARE)



EDO READ CYCLE

(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM MODULE

4 MEG,8 MEG x32

16, 32 MEGABYTE, 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 2,024mW active, typical (32MB)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional Extended and SELF REFRESH
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) access cycle
- Multiple RAS lines allow x16 or x32 width

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

VALID PART NUMBERS

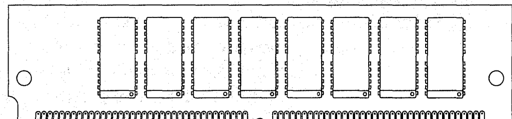
PART NUMBER	DESCRIPTION
MT8D432G-xx	4 Meg x 32, Gold
MT8D432G- xx S	4 Meg x 32, Gold, S**
MT8D432M-xx	4 Meg x 32, Tin/Lead
MT8D432M- xx S	4 Meg x 32, Tin/Lead, S**
MT16D832G-xx	8 Meg x 32, Gold
MT16D832G-xx S	8 Meg x 32, Gold, S**
MT16D832M-xx	8 Meg x 32, Tin/Lead
MT16D832M-xx S	8 Meg x 32, Tin/Lead, S**

**S = SELF REFRESH

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-7) 4 Meg x 32
(DD-8) 8 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC/RAS1*	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC/RAS3*	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

*32MB version only

GENERAL DESCRIPTION

The MT8D432(S) and MT16D832(S) are randomly accessed 16MB and 32MB solid-state memories organized in a x32 configuration.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

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FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

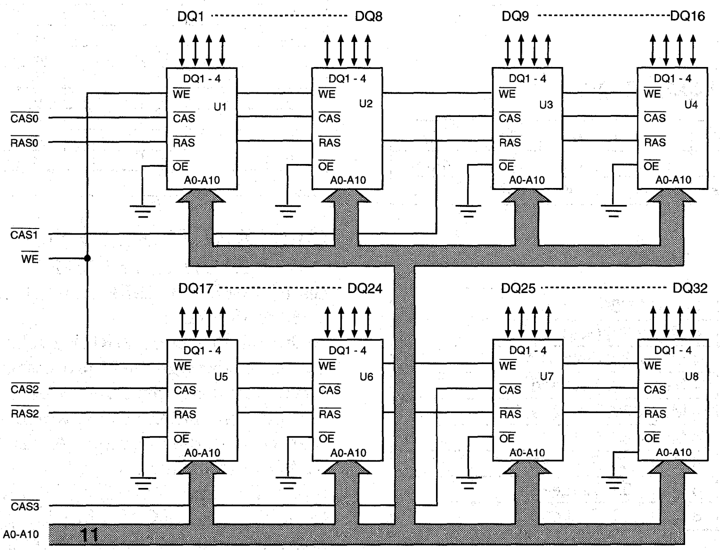
An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ᵗRASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ᵗRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT8D432 (16MB)



U1-U8 = 4 Meg x 4 DRAMs

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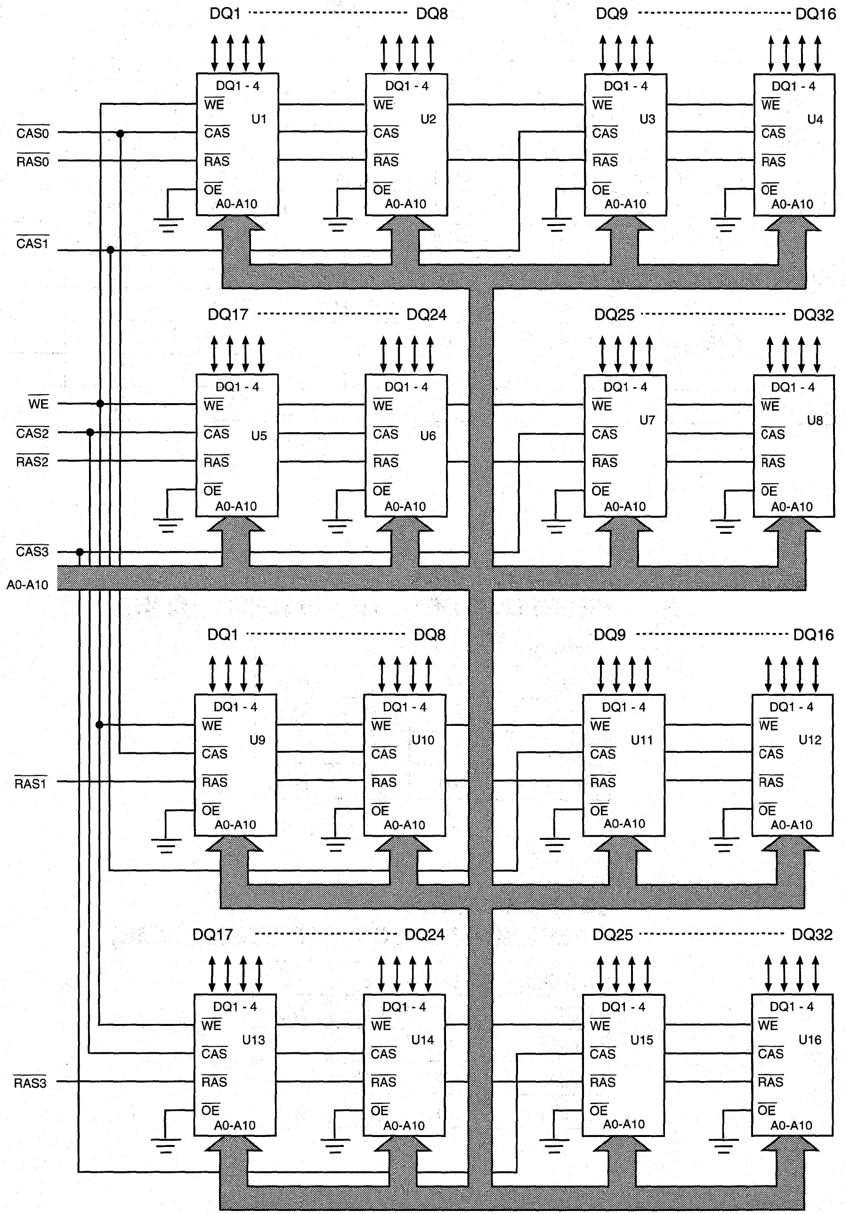
FUNCTIONAL BLOCK DIAGRAM
MT16D832 (32MB)



U1-U16 = 4 Meg x 4 DRAMs

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TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

DRAM SIMM

JEDEC DEFINED PRESENCE-DETECT - MT8D432 (16MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT16D832 (32MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 5.5V	A0-A10, $\overline{WE}$	II2	-32	32	µA	28
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	II3	-8	8	µA	28
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	28
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	16MB 32MB	26 52	26 52	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	16MB 32MB	14 28	14 28	mA	
	ICC2 (S only)	16MB 32MB	12 24	12 24	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])	ICC3	16MB 32MB	960 986	800 826	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: ^tPC = ^tPC [MIN])	ICC4	16MB 32MB	720 746	640 666	mA	3, 4, 26
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: ^tRC = ^tRC [MIN])	ICC5	16MB 32MB	960 986	800 826	mA	3, 26
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])	ICC6	16MB 32MB	960 986	800 826	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current CAS = 0.2V or CBR cycling; RAS = ^tRAS (MIN); WE = 0.2V; A0-A10 and DIN = Vcc -0.2V or 0.2V (DIN may be left open); ^tRC = 62.5µs	ICC7 (S only)	16MB 32MB	2.4 4.8	2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH CBR cycling with RAS ≥ ^tRASS (MIN) and CAS held LOW; WE = Vcc -0.2V; A0-A10 and DIN = Vcc -0.2V or 0.2V (DIN may be left open)	ICC8 (S only)	16MB 32MB	2.4 4.8	2.4 4.8	mA	5, 27

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CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	MAX 32MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	48	95	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}	32	32	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	16	32	pF	2
Input/Output Capacitance: DQ1-DQ32	C_{IO1}	10	16	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	50		55		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	15
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^{t}CHD	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	3		3		ns	25
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	5		5		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		ns	5
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	21
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	19
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	15		20		ns	
READ WRITE cycle time	^{t}RWC	n/a		n/a		ns	22
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		ns	
Write command pulse width	^{t}WP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	24

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS = V_{IH}, data output is High-Z.
12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
22. OE is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
28. 16MB module values will be half of those shown.

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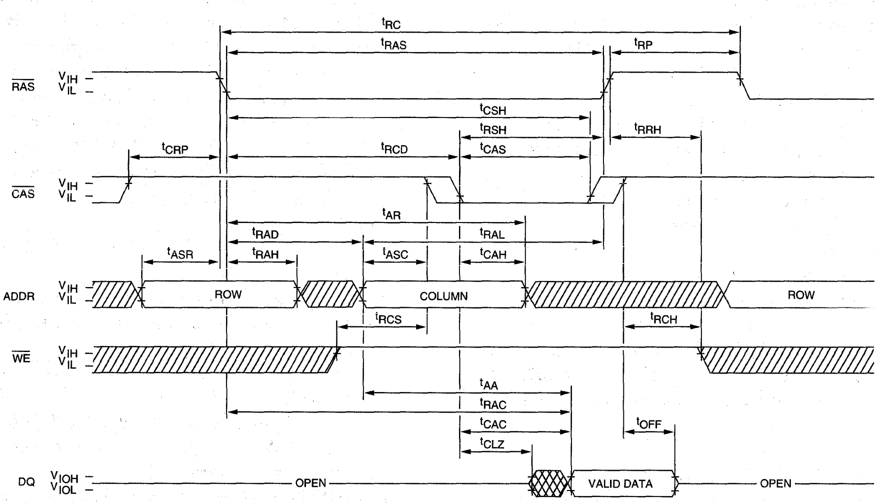
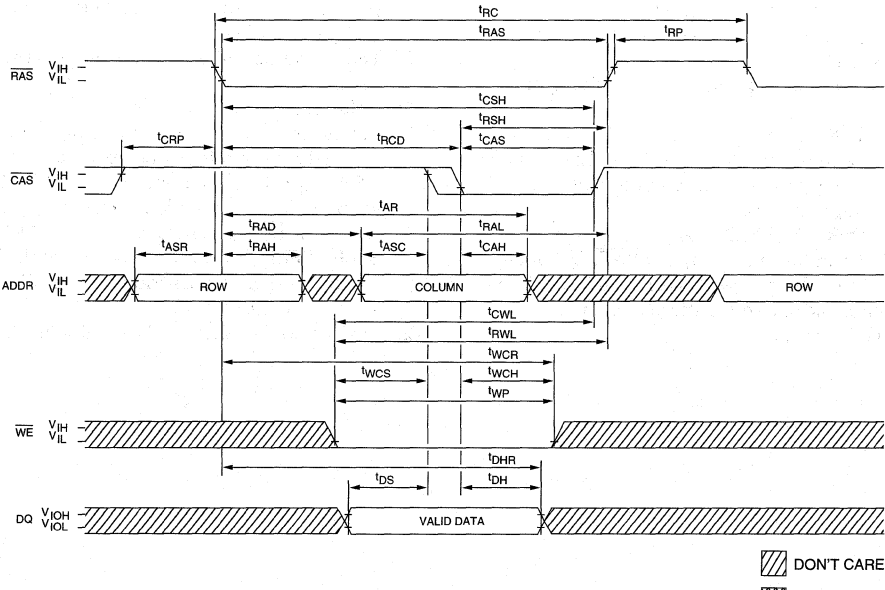
READ CYCLE



EARLY WRITE CYCLE



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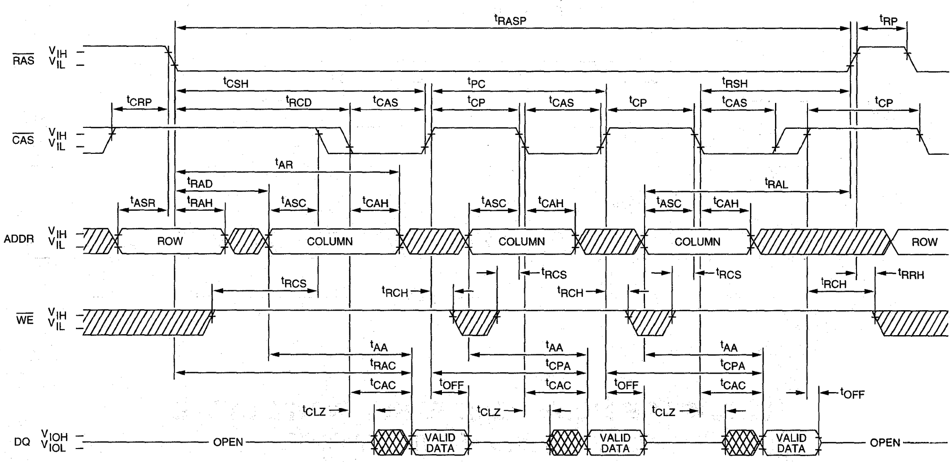
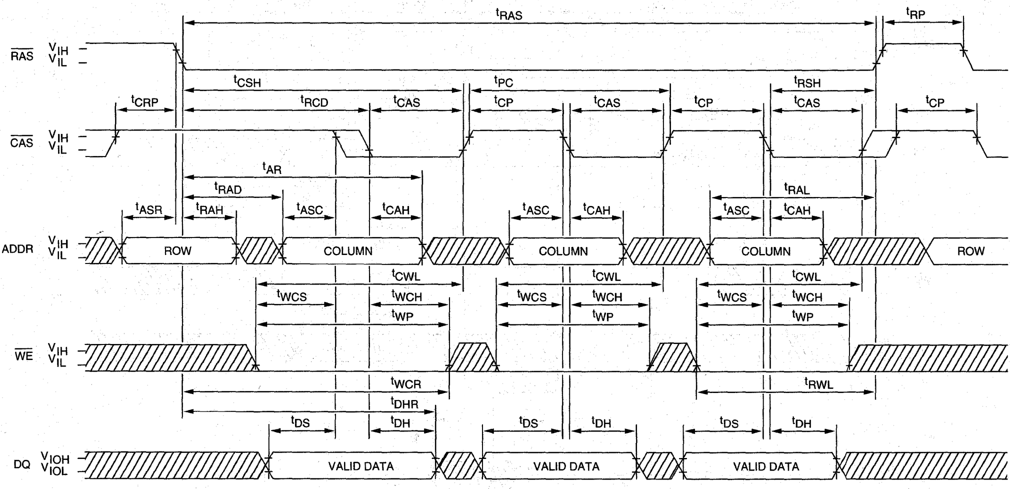
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM SIMM

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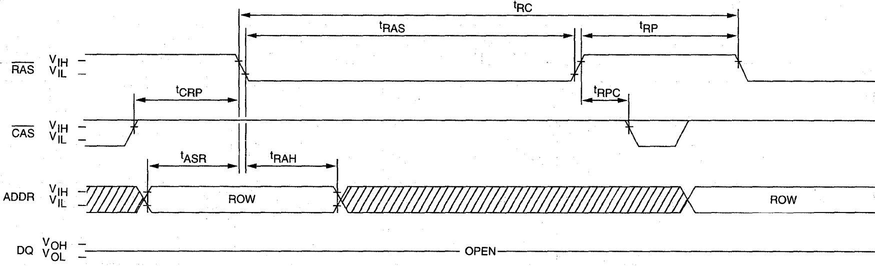
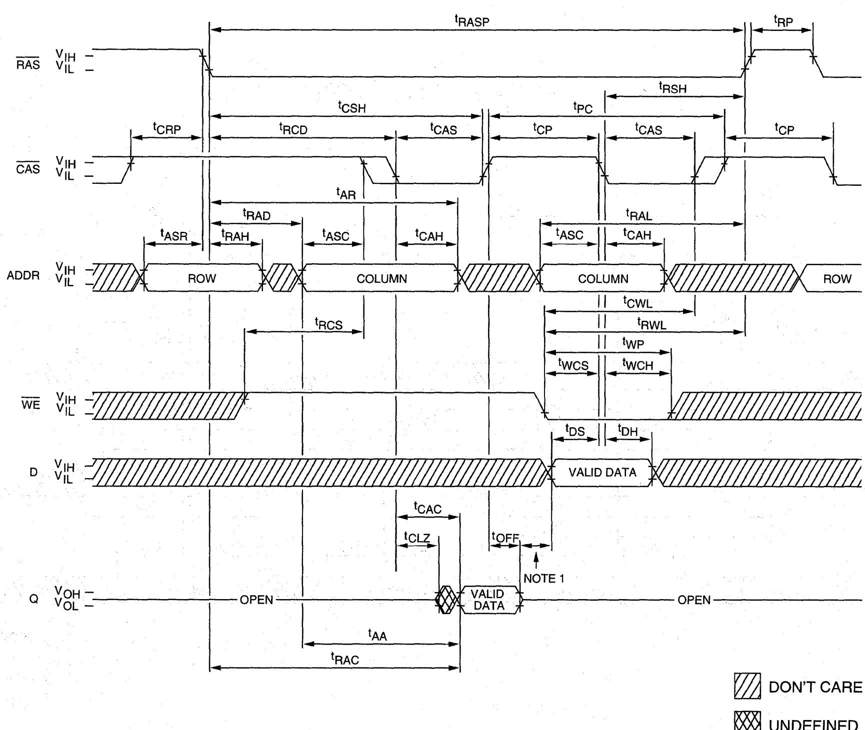
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

DRAM SIMM

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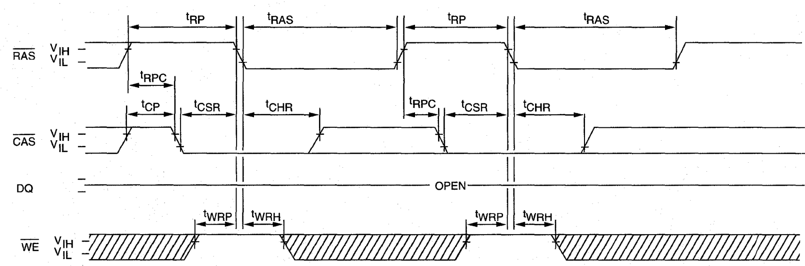
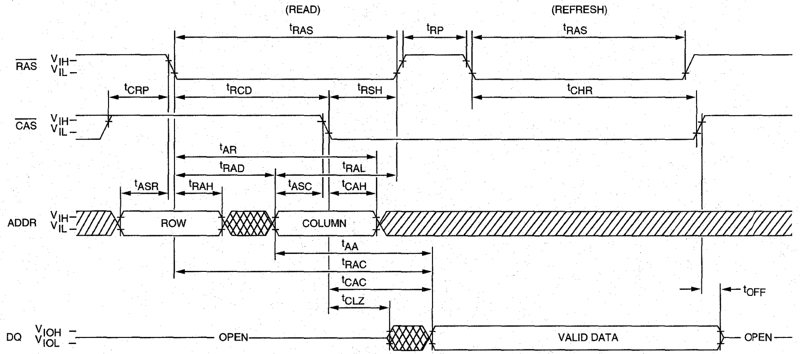
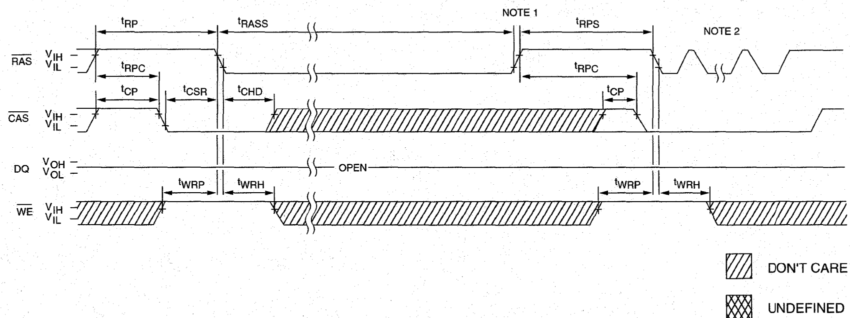
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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DRAM MODULE

4 MEG, 8 MEG x 32

16, 32 MEGABYTE, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC-standard pinout in a 72-pin single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 16mW standby; 1,408mW active, typical (32MB)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF REFRESH
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)
- 3.3V mechanical key

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S
• Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE	X

KEY TIMING PARAMETERS

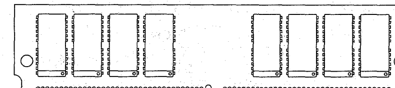
EDO option

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}CAS
-6	110ns	60ns	25ns	30ns	15ns	10ns
-7	130ns	70ns	30ns	35ns	20ns	12ns

FPM option

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)
72-Pin SIMM
(DD-16) 4 Meg x 32, (DD-17) 8 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$*	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

*32MB version only

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8LD432G-xx X	4 Meg x 32 EDO, SOJ, Gold
MT8LD432G-xx XS	4 Meg x 32 EDO, S**, SOJ, Gold
MT8LD432M-xx X	4 Meg x 32 EDO, SOJ, Tin/Lead
MT8LD432M-xx XS	4 Meg x 32 EDO, S**, SOJ, Tin/Lead
MT8LD432G-xx	4 Meg x 32 FPM, SOJ, Gold
MT8LD432G-xx S	4 Meg x 32 FPM, S**, SOJ, Gold
MT8LD432M-xx	4 Meg x 32 FPM, SOJ, Tin/Lead
MT8LD432M-xx S	4 Meg x 32 FPM, S**, SOJ, Tin/Lead
MT16LD832G-xx X	8 Meg x 32 EDO, SOJ, Gold
MT16LD832G-xx XS	8 Meg x 32 EDO, S**, SOJ, Gold
MT16LD832M-xx X	8 Meg x 32 EDO, SOJ, Tin/Lead
MT16LD832M-xx XS	8 Meg x 32 EDO, S**, SOJ, Tin/Lead
MT16LD832G-xx	8 Meg x 32 FPM, SOJ, Gold
MT16LD832G-xx S	8 Meg x 32 FPM, S**, SOJ, Gold
MT16LD832M-xx	8 Meg x 32 FPM, SOJ, Tin/Lead
MT16LD832M-xx S	8 Meg x 32 FPM, S**, SOJ, Tin/Lead

**S = SELF REFRESH

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GENERAL DESCRIPTION

The MT8LD432 (X)(S) and MT16LD832 (X)(S) are randomly accessed 16MB and 32MB solid-state memories organized in a x32 configuration with optional SELF REFRESH. They are specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles each bit is uniquely addressed through the address bits, RAS latches the first 11 bits and CAS latches the latter 11 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

If WE goes LOW after CAS goes LOW, data-out (Q) is activated and retains the selected cell data as long as OE remains LOW and RAS and CAS remains LOW (regardless of WE). This late WE pulse results in a READ WRITE cycle. If WE toggles LOW after CAS goes back HIGH, the output pins will open (High-Z) until the next CAS cycle, regardless of OE.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" option, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after CAS goes HIGH, as long as RAS and OE are held LOW and WE is held HIGH. OE can be brought LOW or HIGH while CAS and RAS are LOW, and the DQs will transition between valid data and High-Z (reference the MT4LC4M4E8(S) DRAM data sheet for additional information on EDO functionality).

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses are executed at least every 32ms (128ms on "S" version), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh period of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed 300µS, prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

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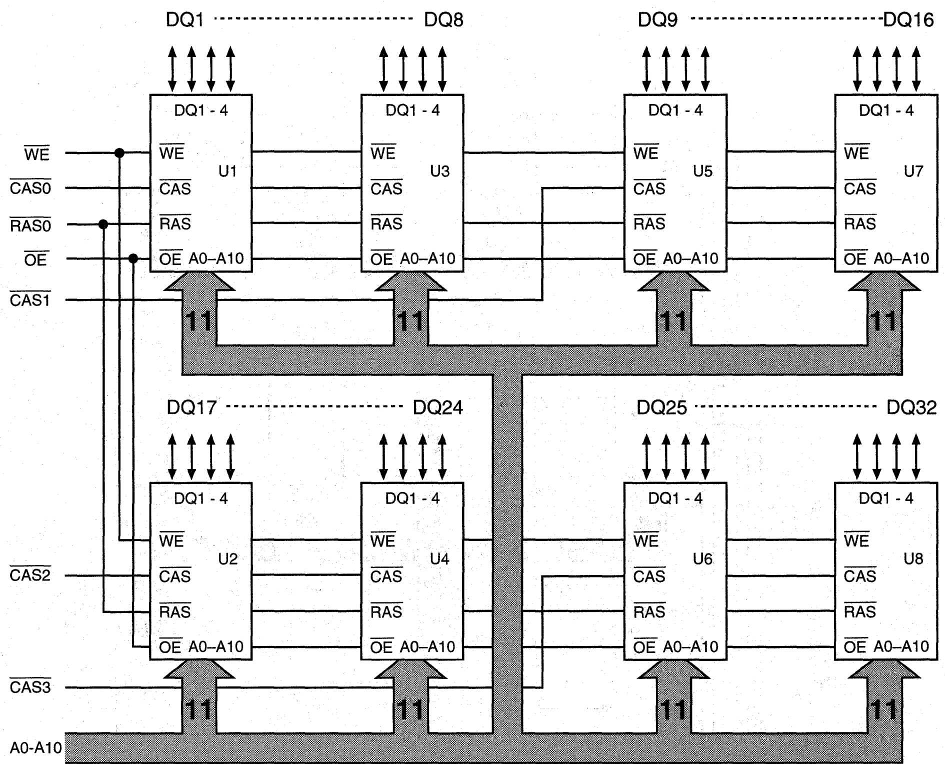
FUNCTIONAL BLOCK DIAGRAM
MT8LD432 (16MB)



1 Meg x 32 EDO PAGE MODE
U1-U8 = MT4LC4M4E8DJ(S)

1 Meg x 32 FAST PAGE MODE
U1-U8 = MT4LC4M4B1DJ(S)

NOTE: 1. See package drawing for U1-U8 placement locations.
2. $\overline{\text{OE}}$ must be tied to Vss if not required.

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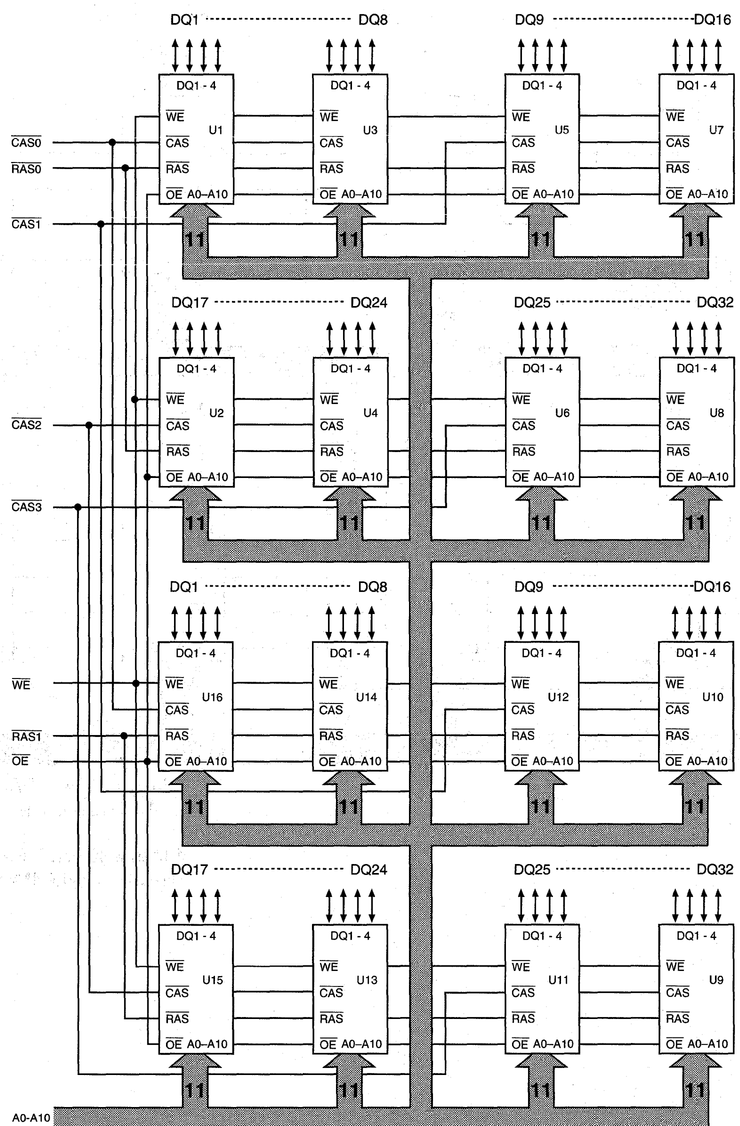
FUNCTIONAL BLOCK DIAGRAM
MT16LD832 (32MB)



8 Meg x 32 EDO PAGE MODE
U1-U16 = MT4LC4M4E8DJ(S)

8 Meg x 32 FAST PAGE MODE
U1-U16 = MT4LC4M4B1DJ(S)

NOTE: 1. See package drawing for U1-U16 placement locations.
2. $\overline{OE}$ must be tied to Vss if not required.

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)						
Module Density	Module Organization	Row/Column Addresses			BANKS	1	2	5	3	4	
0MB	No module installed	X			X	NC	NC	NC			
2MB	512K x 32/36	9/9			2	Vss	NC	Vss			
2MB	512K x 32/36	10/9			1	Vss	NC	NC			
4MB	1 Meg x 32/36	10/10			1	Vss	Vss	NC			
4MB	1 Meg x 32/36	10/9			2	Vss	Vss	Vss			
8MB	2 Meg x 32/36	10/10			2	NC	NC	NC			
8MB	2 Meg x 32/36	11/10			1	NC	NC	Vss			
• 16MB	4 Meg x 32/36	12*/11*			1	NC	Vss	Vss			
16MB	4 Meg x 32/36	11/10			2	Vss	NC	Vss			
• 32MB	8 Meg x 32/36	12*/11*			2	NC	Vss	NC			
32MB	8 Meg x 32/36	12/11			1	NC	Vss	Vss			
Access Timing Detect		80ns							NC	Vss	
		70ns							Vss	NC	
		60ns							NC	NC	
		50ns							Vss	Vss	
Refresh Detect		Standard		Vss							
		Self		NC							
Fast Page Mode/EDO Detect		Fast Page	Vss								
		EDO	NC								
ECC/Parity Detect		ECC									Vss
		Parity/Non-Parity									NC

NOTE: Vss = ground.
*This addressing includes a redundant address to allow mixing 12/10 and 11/11 DRAMs. The modules in this data sheet use 11/11 DRAMs.

DRAM SIMM

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ32
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	High-Z

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	CAS0-CAS3	II1	-8	8	µA	32
Any input 0V ≤ VIN ≤ 5.5V	A0-A9, WE, OE	II2	-32	32	µA	32
(All other pins not under test = 0V) for each package input	RAS0-RAS1	II3	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-20	20	µA	32
TTL OUTPUT LEVELS	High Voltage (IOUT = -2mA)	VOH	2.4		V	
	Low Voltage (IOUT = 2mA)	VOL		0.4	V	

DRAM SIMM

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB 32MB	16 32	16 32	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	16MB 32MB	4 8	4 8	mA	
	I_{CC2} (S only)	16MB 32MB	1.2 2.4	1.2 2.4	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB 32MB	960 976	880 896	mA	2, 22, 26
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4} (X only)	16MB 32MB	880 896	800 816	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC5}	16MB 32MB	720 736	640 656	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC6}	16MB 32MB	960 976	880 896	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	16MB 32MB	960 976	880 896	mA	22, 19
REFRESH CURRENT: Extended (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; $\overline{OE}$, A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC8} (S only)	16MB 32MB	2.4 3.6	2.4 3.6	mA	19, 22
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; $\overline{OE}$, A0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC9} (S only)	16MB 32MB	2.4 3.6	2.4 3.6	mA	19

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CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	MAX 32MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	48	95	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	64	127	pF	17
Input Capacitance: $\overline{RAS0}$-$\overline{RAS1}$	C_{I3}	64	64	pF	17
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I4}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C_{IO}	10	18	pF	17

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	${}^tAA$		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	${}^tAR$	50		55		ns	
Column-address setup time	${}^tASC$	0		0		ns	
Row-address setup time	${}^tASR$	0		0		ns	
Column-address to $\overline{WE}$ delay time	${}^tAWD$	55		60		ns	29
Access time from $\overline{CAS}$	${}^tCAC$		15		20	ns	9
Column-address hold time	${}^tCAH$	10		15		ns	
$\overline{CAS}$ pulse width	${}^tCAS$	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	${}^tCHD$	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	${}^tCHR$	15		15		ns	19
$\overline{CAS}$ to output in Low-Z	${}^tCLZ$	3		3		ns	24
$\overline{CAS}$ precharge time	${}^tCP$	10		10		ns	18
Access time from $\overline{CAS}$ precharge	${}^tCPA$		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	${}^tCRP$	5		5		ns	
$\overline{CAS}$ hold time	${}^tCSH$	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	${}^tCSR$	5		5		ns	19
$\overline{CAS}$ to $\overline{WE}$ delay time	${}^tCWD$	40		45		ns	29
Write command to $\overline{CAS}$ lead time	${}^tCWL$	15		20		ns	
Data-in hold time	${}^tDH$	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	${}^tDHR$	45		55		ns	
Data-in setup time	${}^tDS$	0		0		ns	15
Output disable	${}^tOD$	3	15	3	20	ns	24
Output Enable Time	${}^tOE$		15		20	ns	21
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	${}^tOEH$	15		15		ns	
Output buffer turn-off delay	${}^tOFF$	3	15	3	20	ns	12, 24, 33
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	${}^tORD$	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	${}^tPC$	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	${}^tPRWC$	85		95		ns	

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	8
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	23
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		ns	14
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) S version	^{t}REF		128		128	ms	
$\overline{\text{RAS}}$ precharge time	^{t}RP	40		50		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		ns	
$\overline{\text{RAS}}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		ns	27
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		ns	14
$\overline{\text{RAS}}$ hold time	^{t}RSH	15		20		ns	
READ WRITE cycle time	^{t}RWC	150		180		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	85		95		ns	29
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		20		ns	
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		15		ns	
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		ns	
$\overline{\text{WE}}$ command setup time	^{t}WCS	0		0		ns	29
Write command pulse width	^{t}WP	10		15		ns	
$\overline{\text{WE}}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	28
$\overline{\text{WE}}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	28

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 16, 26) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address set-up to $\overline{CAS}$ precharge during WRITE	tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to $\overline{WE}$ delay time	tAWD	55		65		ns	29
Access time from $\overline{CAS}$	tCAC		15		20	ns	9
Column-address hold time	tCAH	10		12		ns	
$\overline{CAS}$ pulse width	tCAS	10	10,000	12	10,000	ns	
$\overline{CAS}$ LOW to "don't care" during SELF REFRESH cycle	tCHD	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		12		ns	19
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		ns	
Data output hold after next $\overline{CAS}$ LOW	tCOH	5		5		ns	
$\overline{CAS}$ precharge time (EDO PAGE MODE)	tCP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
$\overline{CAS}$ hold time	tCSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	5		5		ns	19
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	35		40		ns	29
Write command to $\overline{CAS}$ lead time	tCWL	15		15		ns	
Data-in hold time	tDH	10		12		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	15
Output disable	tOD	0	15	0	15	ns	
Output Enable	tOE		15		15	ns	21
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	10		12		ns	
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	tOEHC	10		10		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 16, 26) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ HIGH pulse width	^{t}OEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^{t}OES	5		5		ns	
Output buffer turn-off delay	^{t}OFF	3	15	3	15	ns	12, 24, 33
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	75		85		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^{t}RAD	12	30	12	35	ns	23
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^{t}RASP	60	125,000	70	125,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	14	45	14	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	0		0		ns	14
Read command setup time	^{t}RCS	0		0		ns	
Refresh period (2,048 cycles)	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	14
$\overline{RAS}$ hold time	^{t}RSH	10		12		ns	
READ WRITE cycle time	^{t}RWC	150		177		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	80		90		ns	29
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
Write command hold time	^{t}WCH	10		12		ns	
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		ns	
$\overline{WE}$ command setup time	^{t}WCS	0		0		ns	29
Output disable delay from $\overline{WE}$	^{t}WHZ	0	13	0	15	ns	
Write command pulse width	^{t}WP	10		12		ns	
$\overline{WE}$ pulse to disable at $\overline{CAS}$ HIGH	^{t}WPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		ns	28

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by eight RAS REFRESH cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
4. AC characteristics assume ᵗT = 2.5ns for EDO and 5ns for FPM.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF. Output reference voltages are 0.8V for a low level and 2.0V for a high level.
8. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
9. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
10. If CAS and RAS = V_{IH}, data output is High-Z.
11. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
12. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, then access time is controlled exclusively by ᵗCAC.
14. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Vcc = 3.3V ±0.3V; f = 1 MHz.
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
21. If OE is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
22. Icc is dependent on cycle rates.
23. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, then access time is controlled exclusively by ᵗAA.
24. The 3ns minimum is a parameter guaranteed by design.
25. Refresh current increases if ᵗRAS is extended beyond its minimum specification.
26. Column-address changed once each cycle.
27. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
28. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
29. ᵗWCS, ᵗRWD, ᵗAWD and ᵗCWD are not restrictive operating parameters. ᵗWCS applies to EARLY WRITE cycles. ᵗRWD, ᵗAWD and ᵗCWD apply to READ-MODIFY-WRITE cycles. If ᵗWCS ≥ ᵗWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ᵗWCS < ᵗWCS (MIN) and ᵗRWD ≥ ᵗRWD (MIN), ᵗAWD ≥ ᵗAWD (MIN) and ᵗCWD ≥ ᵗCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. ᵗWCS, ᵗRWD, ᵗCWD and ᵗAWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

30. LATE WRITE and READ-MODIFY-WRITE cycles must have both ᵗOD and ᵗOEH met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE is taken back LOW while CAS remains LOW, the DQs will remain open.
31. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
32. 16MB module will be half of the values shown.
33. For FAST-PAGE-MODE option, ᵗOFF is determined by the first RAS or CAS signal to transition HIGH. In comparison, ᵗOFF on an EDO option is determined by the latter of the RAS and CAS signal to transition HIGH.
34. Applies to both EDO and FAST PAGE MODEs.

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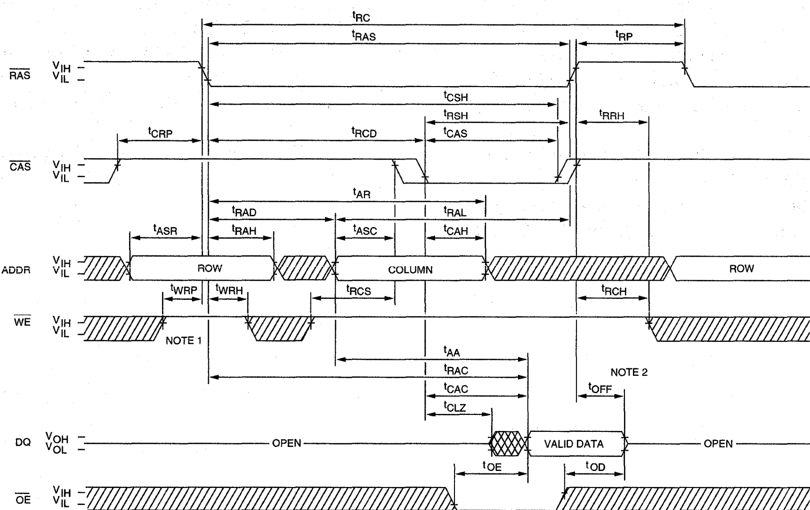
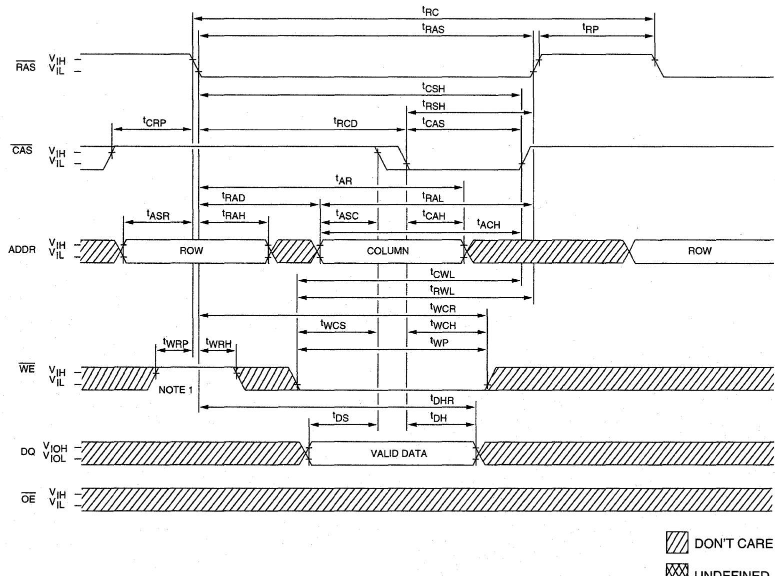
READ CYCLE [34]



EARLY WRITE CYCLE [34]



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

2. ${}^tOFF$ is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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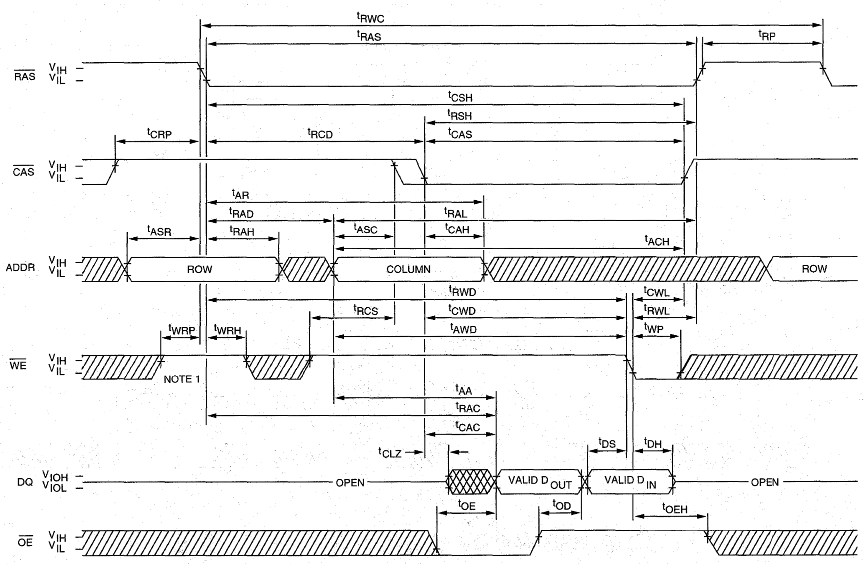
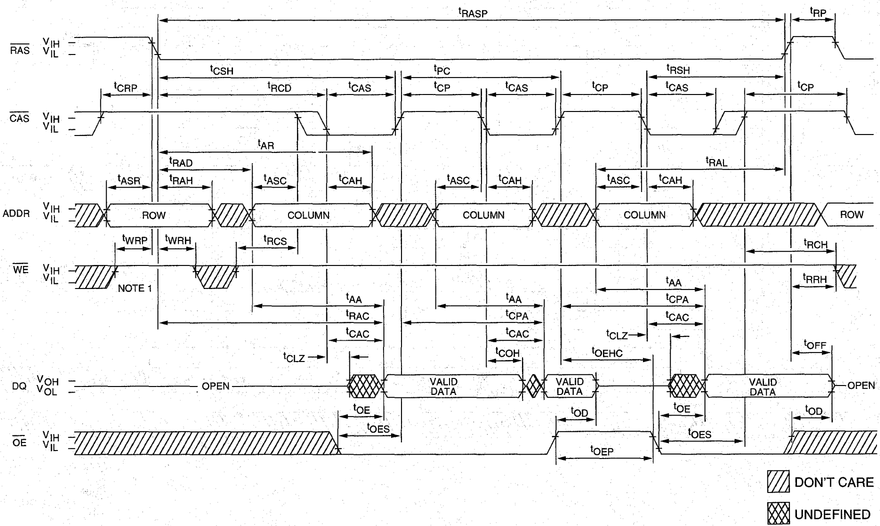
READ WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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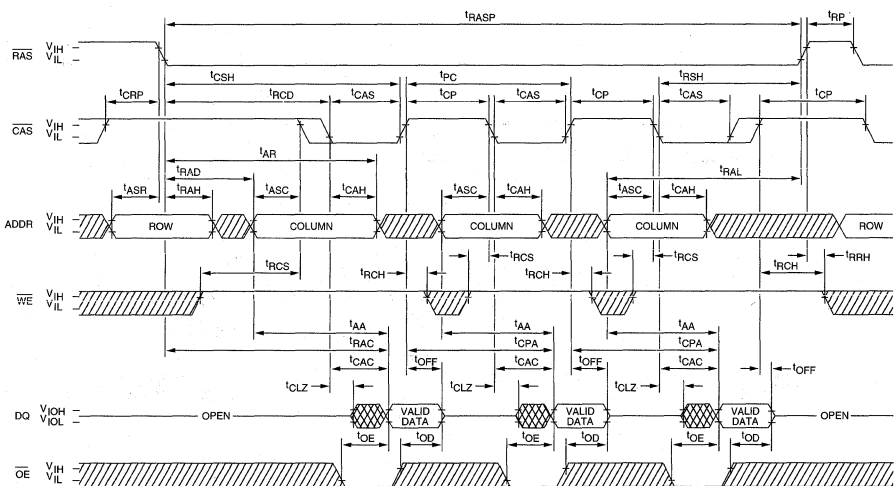
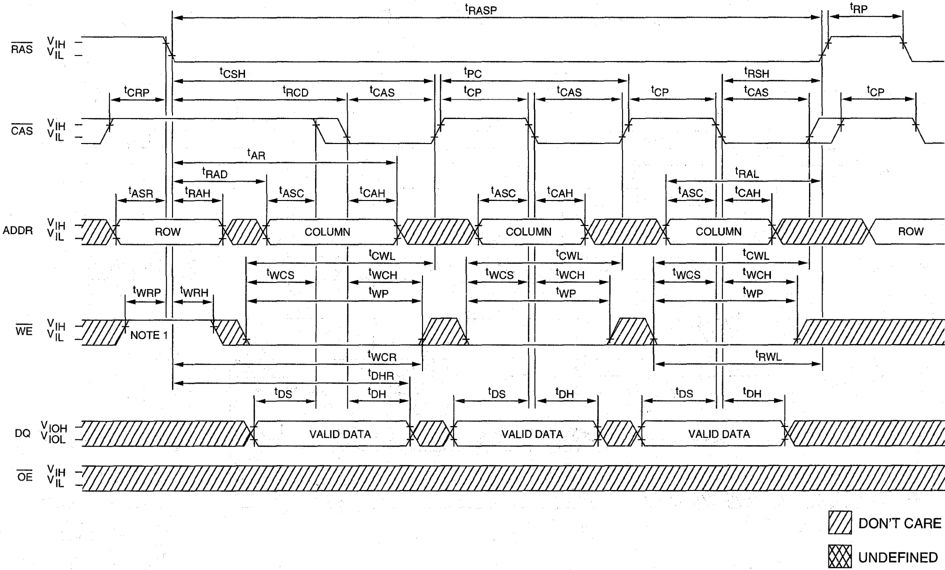
FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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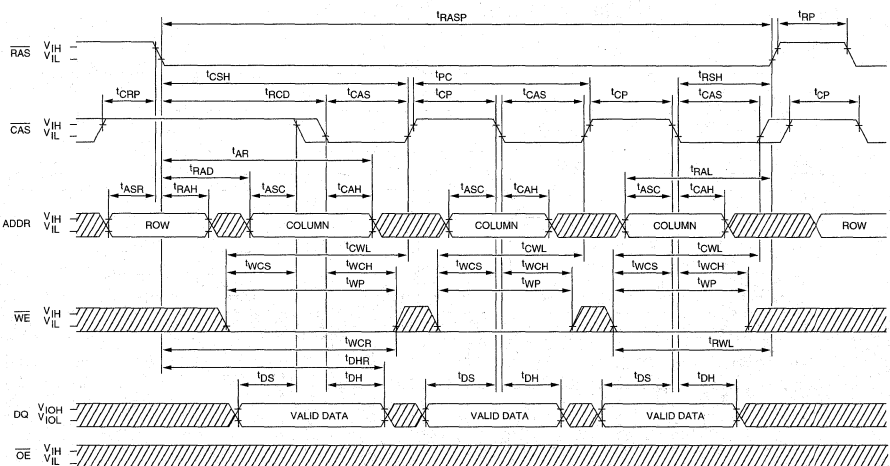
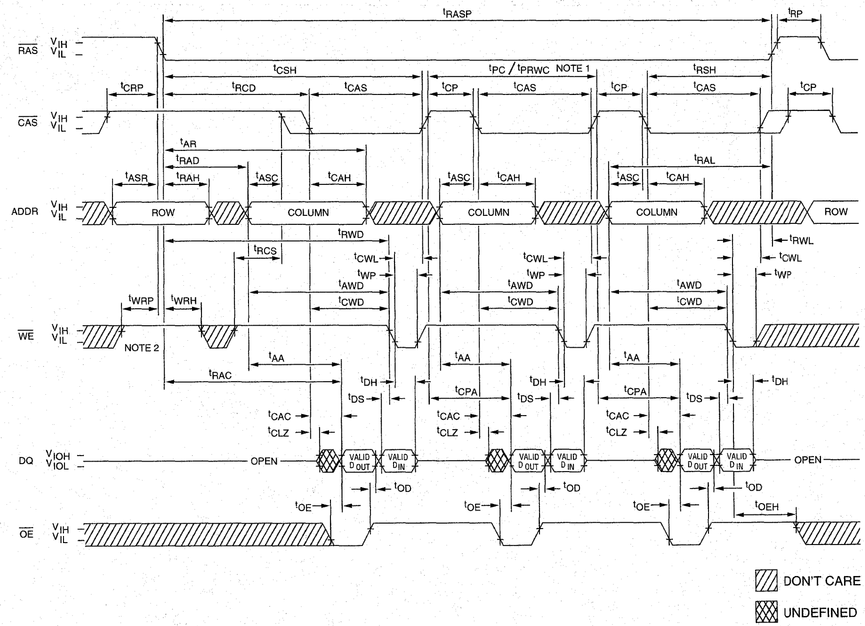
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO/FASTPAGE-MODE READ-WRITE CYCLE [34]

(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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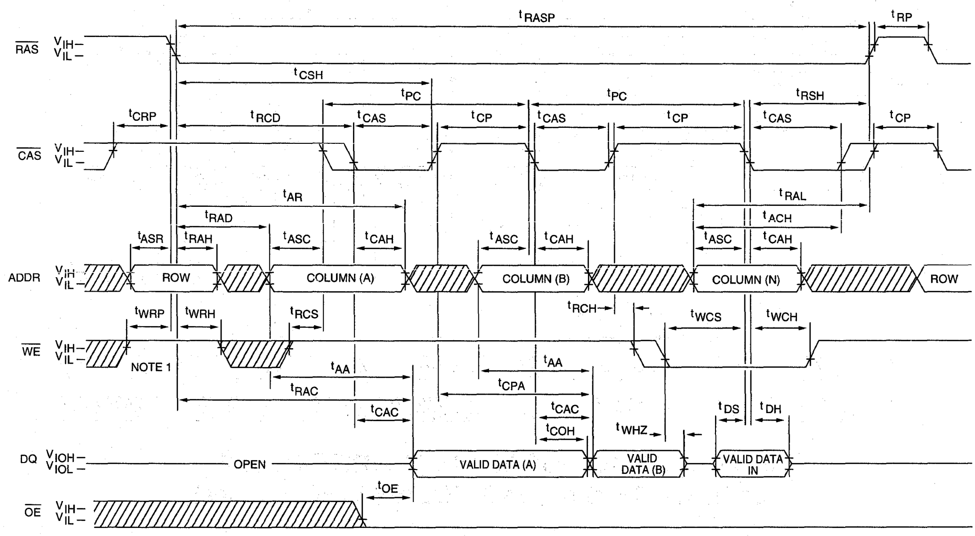
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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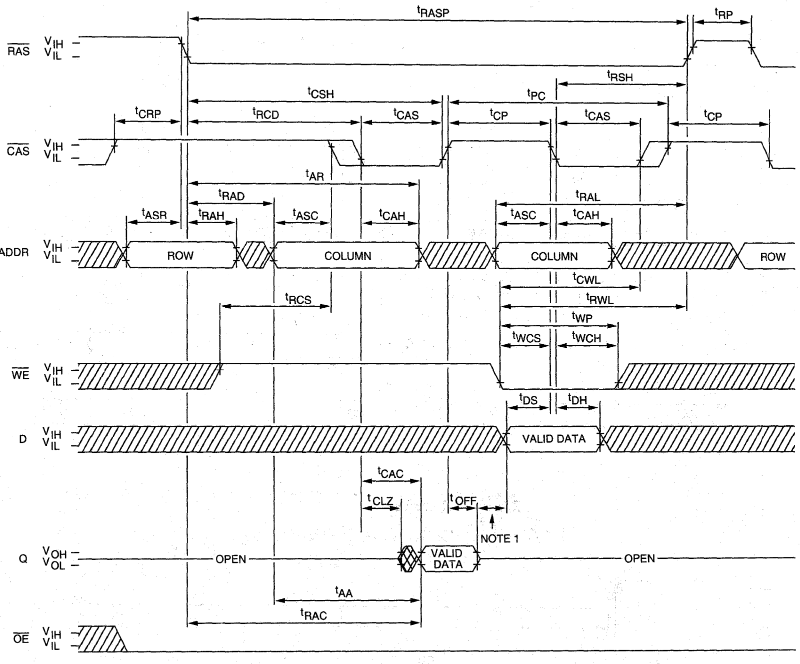
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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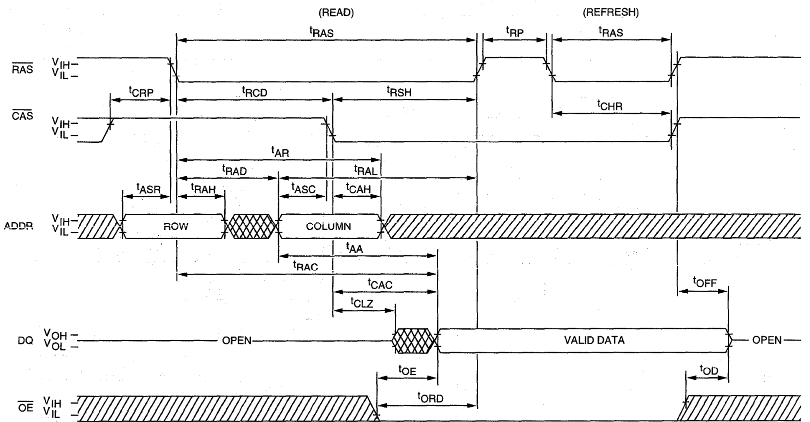
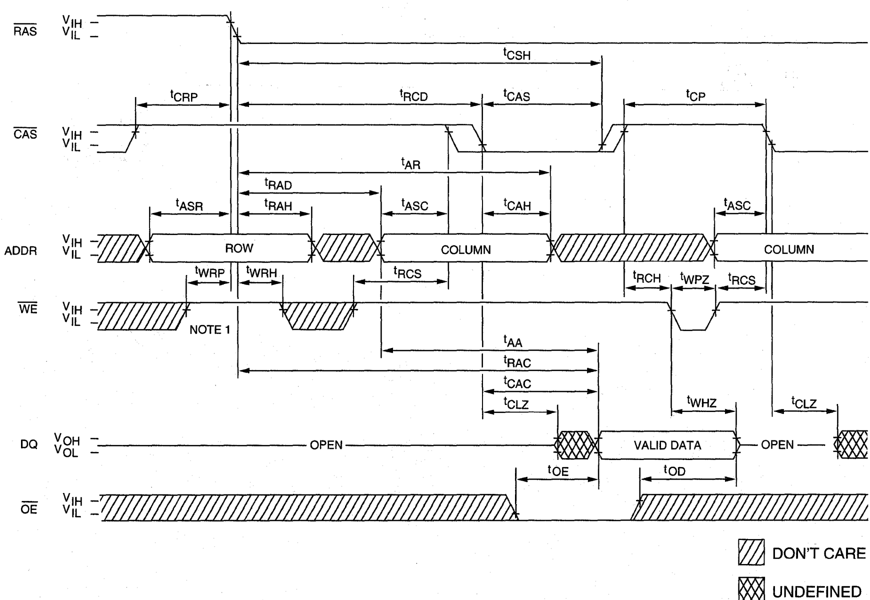
HIDDEN REFRESH CYCLE [20, 34]
(WE = HIGH; OE = LOW)



EDO READ CYCLE
(with WE-controlled disable)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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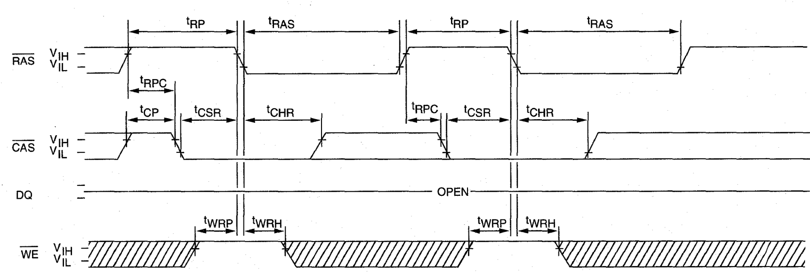
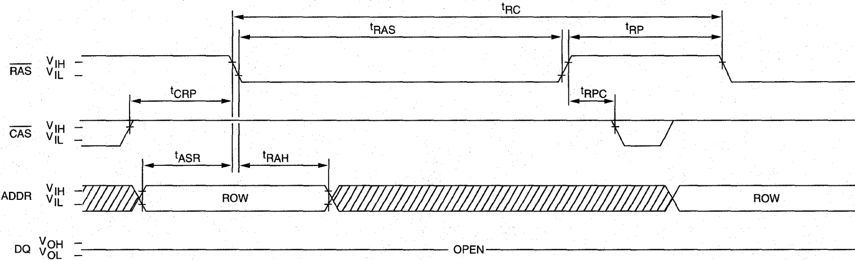
CBR REFRESH CYCLE [34]

(Addresses and $\overline{OE}$ = DON'T CARE)



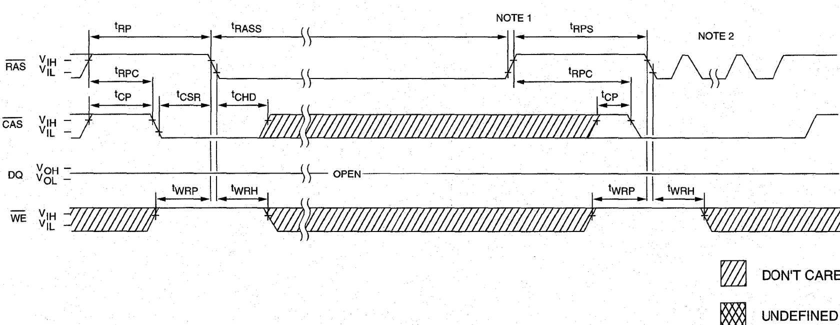
$\overline{RAS}$-ONLY REFRESH CYCLE [34]

($\overline{WE}$ = DON'T CARE)



SELF REFRESH CYCLE [34]

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

DRAM SIMM

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DRAM MODULE

1 MEG, 2 MEG x 36

4, 8 MEGABYTE, 5V, FAST PAGE MODE

NEW DRAM SIMM

FEATURES

- Common RAS control per side pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process.
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 54mW standby; 2,052mW active, typical (8MB)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

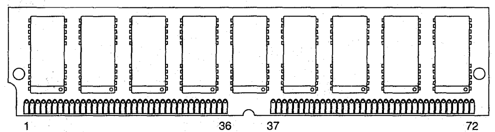
PART NUMBER EXAMPLES

VALID PART NUMBERS	DESCRIPTION
MT9D136G-xx	1 Meg x 36, Gold
MT9D136M-xx	1 Meg x 36, Tin/Lead
MT18D236G-xx	2 Meg x 36, Gold
MT18D236M-xx	2 Meg x 36, Tin/Lead

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-9) 1 Meg x 36, (DD-10) 2 Meg x 36



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	NC	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC/RAS1*	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC/RAS1*	51	DQ11	69	PRD3
16	A4	34	RAS0	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

*8MB version only

GENERAL DESCRIPTION

The MT9D136 and MT18D236 are randomly accessed 4MB and 8MB solid-state memories organized in a x36 configuration. The modules use 1 Meg x 4 Quad CAS DRAM(s) to replace the typical 1 Meg x 1 DRAMs used for parity.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

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REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM
MT9D136 (4MB)

U1-U4, U6-U9 = MT4C4001JDJ
U5 = MT4C4004JDJ

NOTE: Due to the use of a Quad $\overline{CAS}$ parity DRAM, $\overline{RAS0}$ is common to all DRAMs.

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FUNCTIONAL BLOCK DIAGRAM
MT18D236 (8MB)

U1-U4, U6-U13, U15-U18 = MT4C4001JDJ
U5, U14 = MT4C4004JDJ

NOTE: Due to the use of a Quad CAS parity DRAM, RAS0 is common to Side 1 and RAS1 is common to Side 2.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT9D136 (4MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT18D236 (8MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V) for each package input	CAS0-CAS3	II1	-12	12	µA	26
	A0-A9, WE	II2	-36	36	µA	26
	RAS0, RAS1	II3	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ36	IOZ	-20	20	µA	26
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS = CAS = VIH)	ICC1	4MB 8MB	18 36	18 36	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	ICC2	4MB 8MB	9 18	9 18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: tRC = tRC [MIN])	ICC3	4MB 8MB	990 1,008	900 918	mA	2, 23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = VIL, CAS, Address Cycling: tPC = tPC [MIN])	ICC4	4MB 8MB	720 738	630 648	mA	2, 23
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = VIH: tRC = tRC [MIN])	ICC5	4MB 8MB	990 1,008	900 918	mA	2
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling; WE = Vcc -0.2; tRC = tRC [MIN])	ICC6	4MB 8MB	990 1,008	900 918	mA	2, 19

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CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	55	105	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	70	140	pF	17
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}	70	70	pF	17
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	25	50	pF	17
Input/Output Capacitance: DQ1-DQ36	C_{IO1}	10	16	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{CAS}$	^{t}CAC		15		20	ns	9
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	19
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	^{t}CLCH	10		10		ns	
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	0		0		ns	
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^{t}CPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	10		10		ns	
$\overline{CAS}$ hold time	^{t}CSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	19
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	15
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	12, 25
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	24
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^{t}RAL	30		35		ns	
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	14
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$-ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
11. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 5V, DC bias = 2.4V at 15mV RMS).
18. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW.
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{\text{OE}}$ being grounded on U1-U9/U18.
22. Last falling $\overline{\text{CAS}}$x edge to first rising $\overline{\text{CAS}}$x edge.
23. I_{CC} is dependent on cycle rates.
24. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
25. The 3ns minimum is a parameter guaranteed by design.
26. 4MB module values will be half of those shown.

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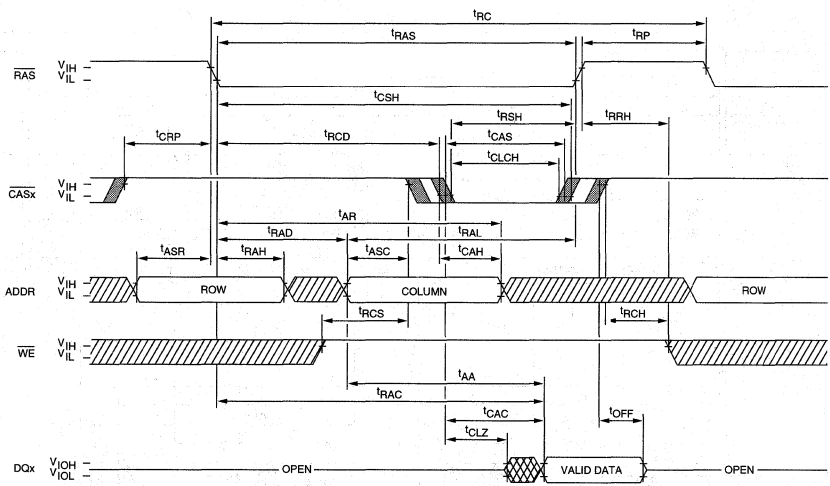
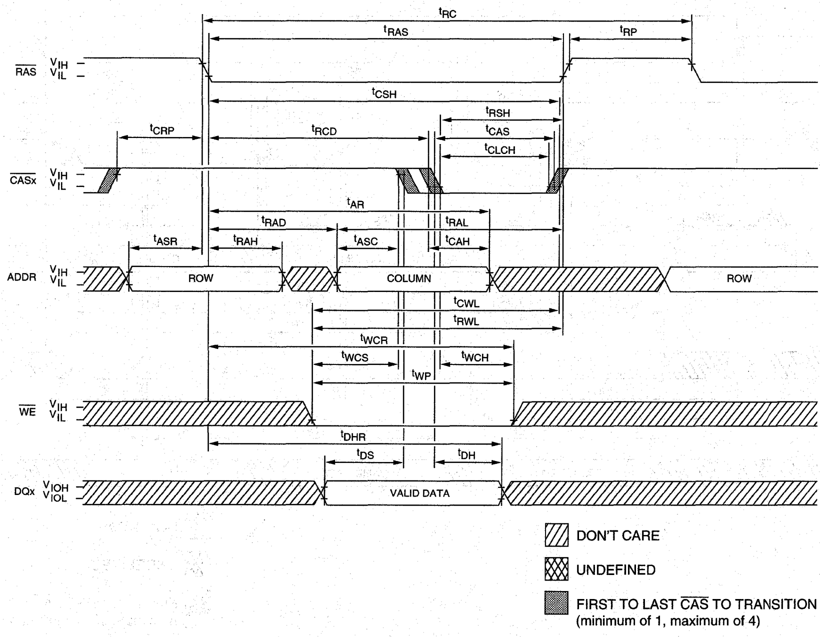
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

FIRST TO LAST $\overline{CAS}$ TO TRANSITION (minimum of 1, maximum of 4)

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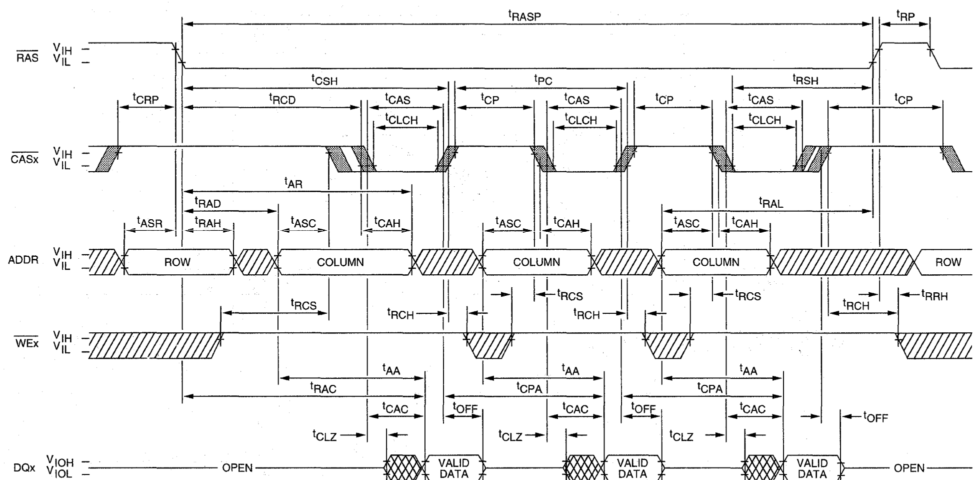
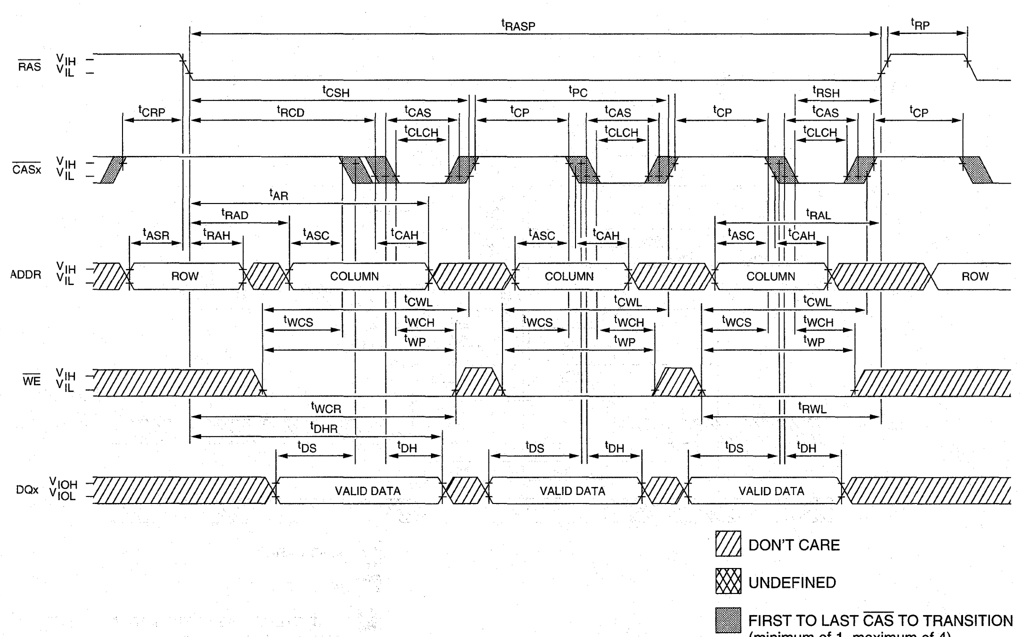
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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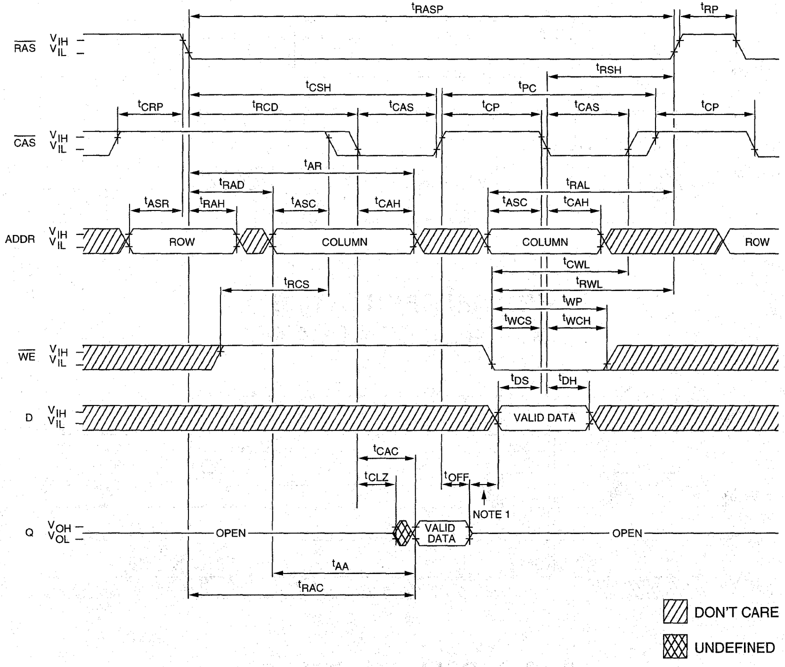
NEW DRAM SIMM

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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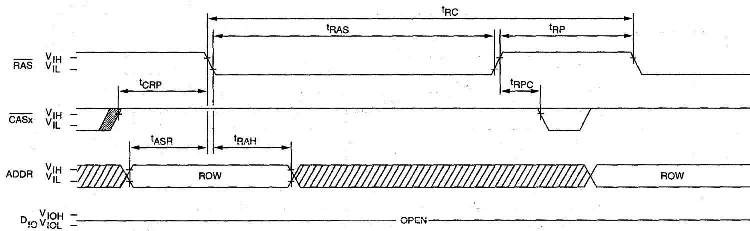
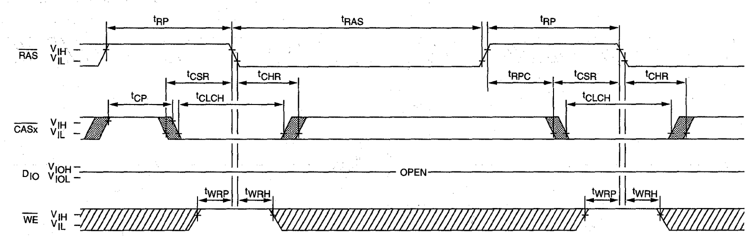
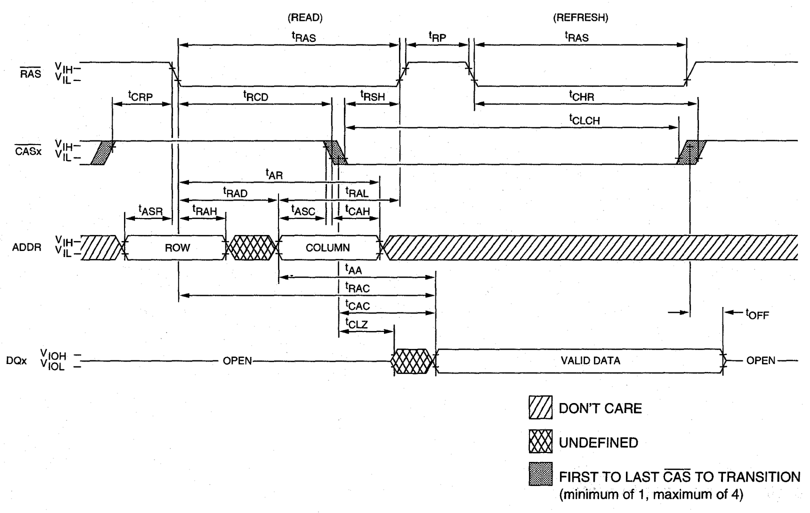
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



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DRAM MODULE

4 MEG, 8 MEG x 36

16, 32 MEGABYTE, 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 72mW standby; 2,536mW active, typical (32MB)
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN; optional Extended and SELF REFRESH
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) access cycle
- Multiple RAS lines allow x18 or x36 widths

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Packages	
72-pin SIMM	M
72-pin SIMM (gold)	G
72-pin SIMM low profile (1.00")	DM
72-pin SIMM (gold) low profile (1.00")	DG
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

VALID PART NUMBERS

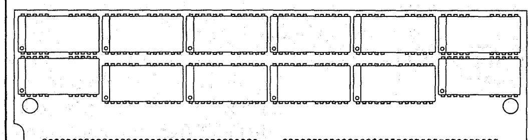
PART NUMBER	DESCRIPTION
MT12D436DG-xx	4 Meg x 36, Gold
MT12D436DG- xx S	4 Meg x 36, Gold, S**
MT12D436DM-xx	4 Meg x 36, Tin/Lead
MT12D436DM- xx S	4 Meg x 36, Tin/Lead, S**
MT24D836G-xx	8 Meg x 36, Gold
MT24D836G-xx S	8 Meg x 36, Gold, S**
MT24D836M-xx	8 Meg x 36, Tin/Lead
MT24D836M-xx S	8 Meg x 36, Tin/Lead, S**

**S = SELF REFRESH

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-11) 4 Meg x 36
(DD-12) 8 Meg x 36
(DD-13) 4 Meg x 36 Low Profile



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0	58	DQ32
5	DQ20	23	DQ24	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ33
7	DQ21	25	DQ25	43	CAS1	61	DQ15
8	DQ4	26	DQ8	44	RAS0	62	DQ34
9	DQ22	27	DQ26	45	NC/RAS1*	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC	47	WE	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC/RAS3*	51	DQ11	69	PRD3
16	A4	34	RAS2	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

*32MB version only

DRAM SIMM

GENERAL DESCRIPTION

The MT12D436(S) and MT24D836(S) are randomly accessed 16MB and 32MB solid-state memories organized in a x36 configuration.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits. A READ or WRITE cycle is selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. Since WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

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FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0 - A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS addressing.

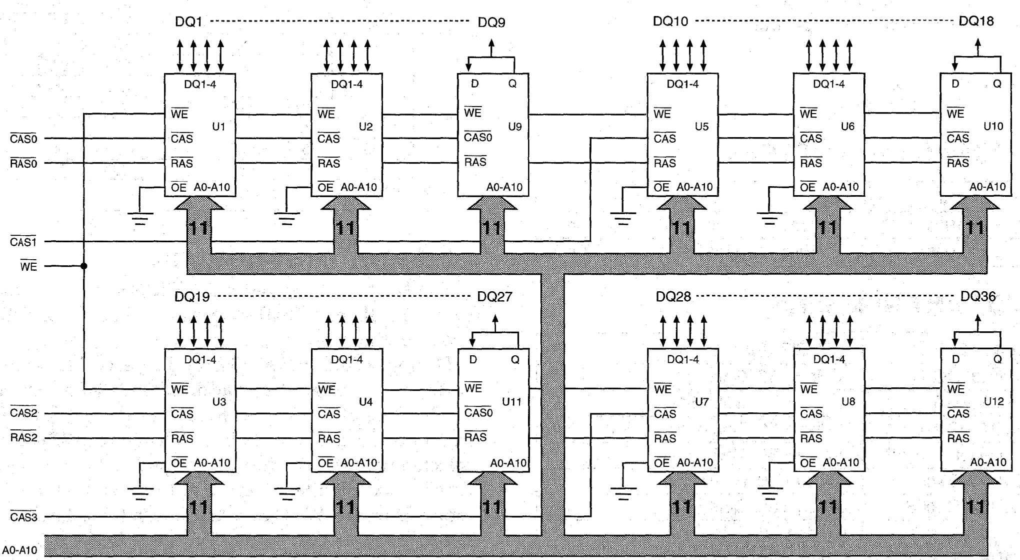
An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

x18 CONFIGURATION

For x18 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ19, DQ2 to DQ20 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x18 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT12D436 (16MB)



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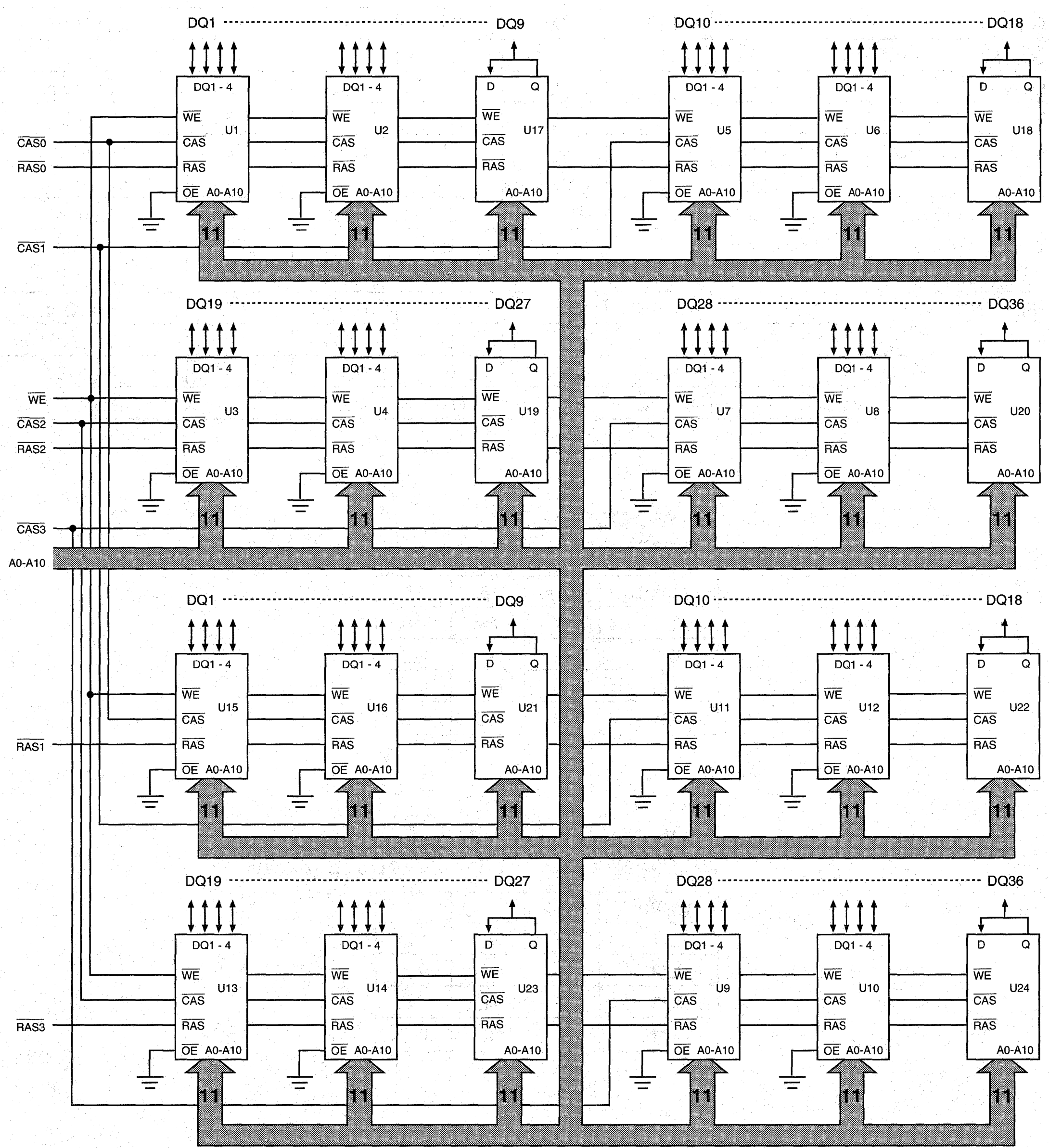
FUNCTIONAL BLOCK DIAGRAM
MT24D836 (32MB)



U1-U16 = 4 Meg x 4 DRAMs
U17-U24 = 4 Meg x 1 DRAMs

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT12D436 (16MB)

SYMBOL	PIN #	-6	-7
PRD1	67	Vss	Vss
PRD2	68	NC	NC
PRD3	69	NC	Vss
PRD4	70	NC	NC

JEDEC DEFINED PRESENCE-DETECT - MT24D836 (32MB)

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	Vss	Vss
PRD3	69	NC	Vss
PRD4	70	NC	NC

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$	II1	-12	12	µA	
Any input 0V ≤ VIN ≤ 5.5V	A0-A10, $\overline{\text{WE}}$	II2	-48	48	µA	28
(All other pins not under test = 0V) for each package input	$\overline{\text{CAS0}}$-$\overline{\text{CAS3}}$	II3	-12	12	µA	28
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ36	IOZ	-20	20	µA	28
OUTPUT LEVELS Output High Voltage (IOUT = -5mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB 32MB	34 68	34 68	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	16MB 32MB	18 36	18 36	mA	
	I_{CC2} (S only)	16MB 32MB	13 26	13 26	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB 32MB	1,400 1,434	1,200 1,234	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	16MB 32MB	1,040 1,074	920 954	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	16MB 32MB	1,400 1,434	1,200 1,234	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	16MB 32MB	1,400 1,434	1,200 1,234	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = 0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	16MB 32MB	3.6 7.2	3.6 7.2	mA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	16MB 32MB	3.6 7.2	3.6 7.2	mA	5

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CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	MAX 32MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	70	140	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	94	188	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$	C_{I3}	50	50	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}	25	50	pF	2
Input/Output Capacitance: DQ1-DQ8, DQ10-DQ17, DQ19-DQ26, DQ28-DQ35	C_{IO1}	10	18	pF	2
Input/Output Capacitance: DQ9, DQ18, DQ27, DQ36	C_{IO2}	16	28	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	5
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	21
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20, 25
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	22
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		µs	27
Random READ or WRITE cycle time	^tRC	110		130		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
Refresh period (2,048 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ WRITE cycle time	^tRWC	n/a		n/a		ns	22
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	24

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
22. OE is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
24. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode). Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
28. 16MB module values will be half of those shown.

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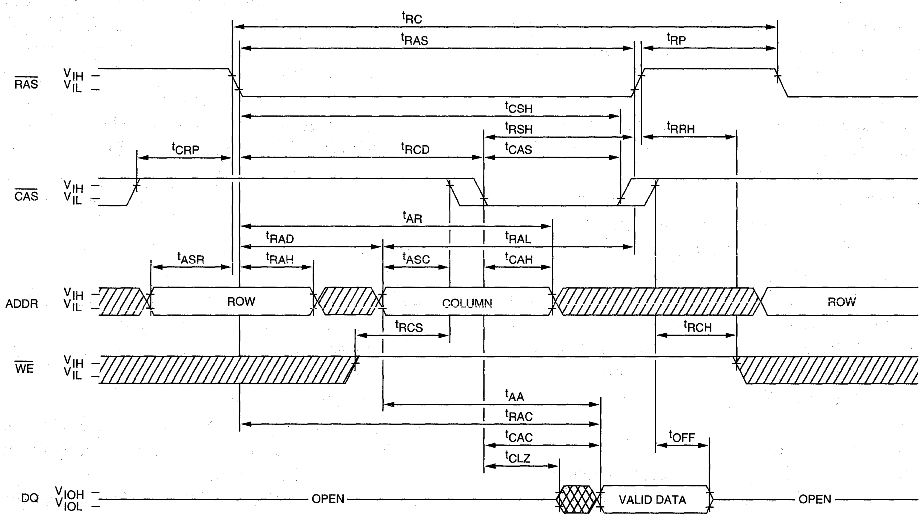
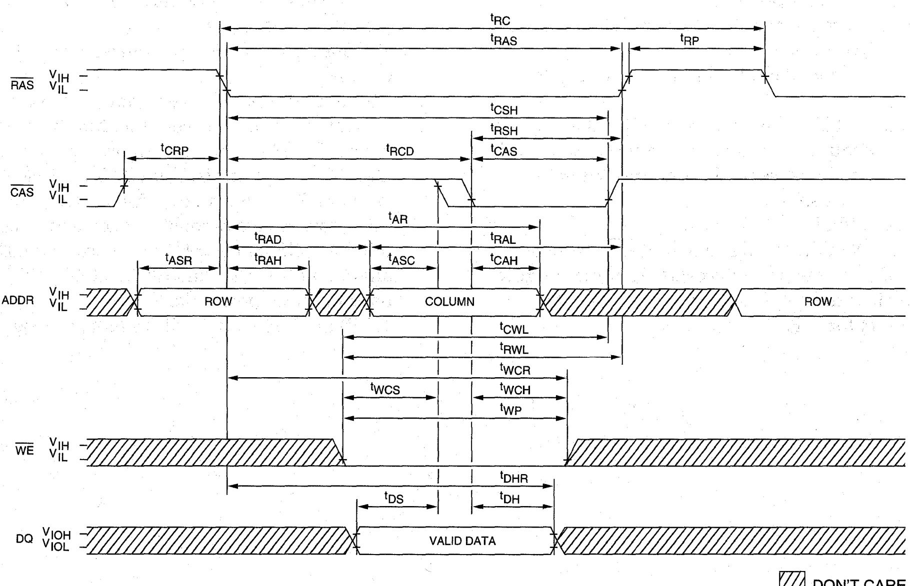
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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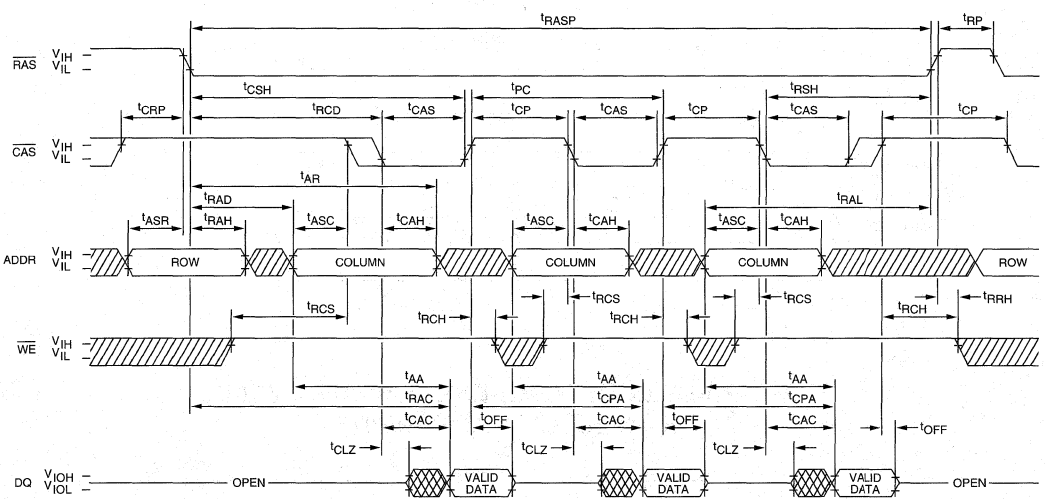
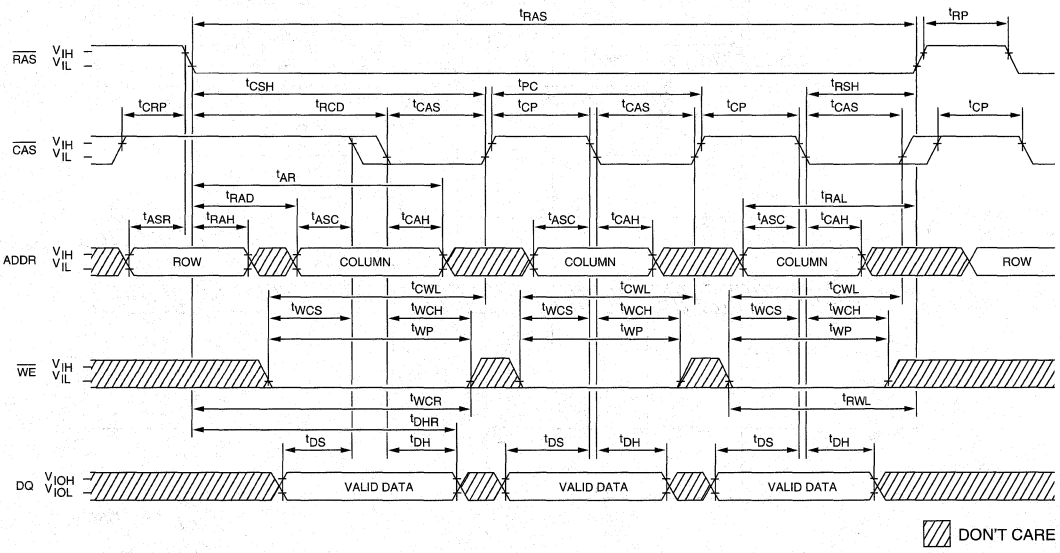
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DRAM SIMM

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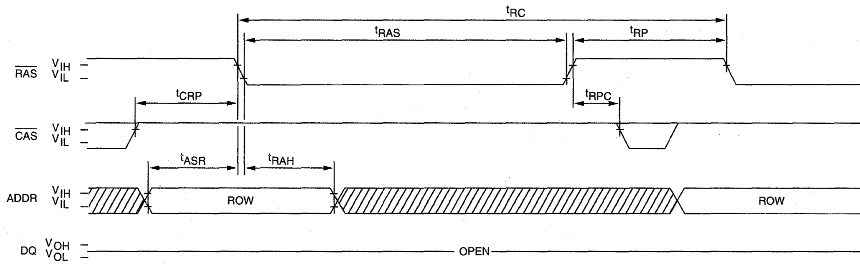
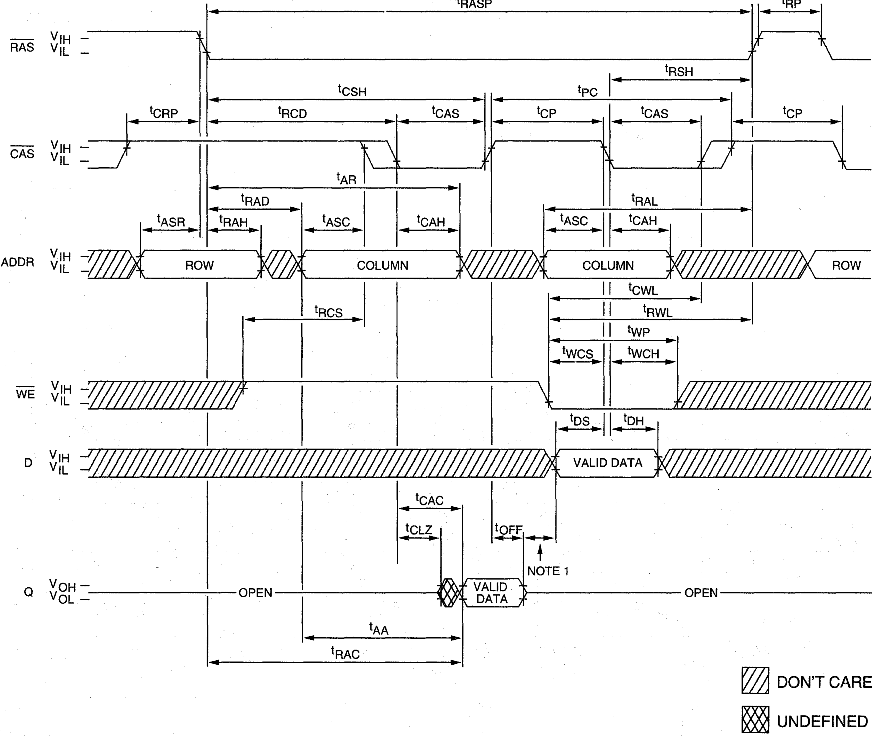
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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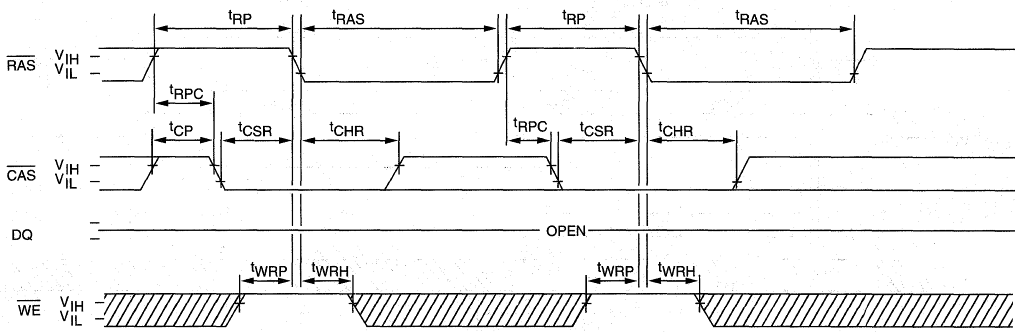
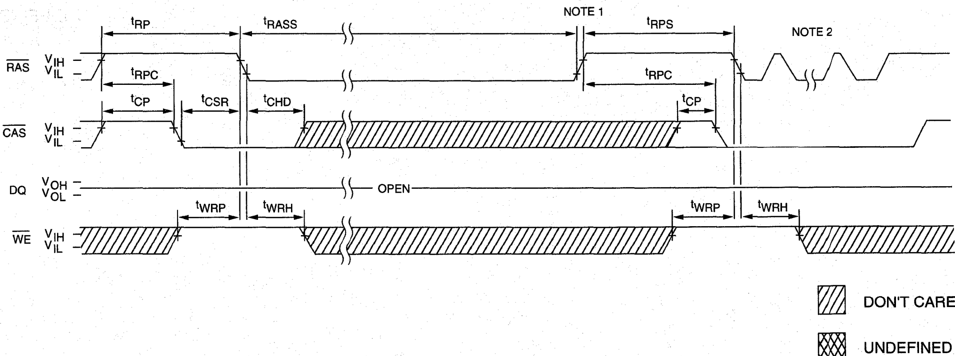
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



DRAM SIMM

NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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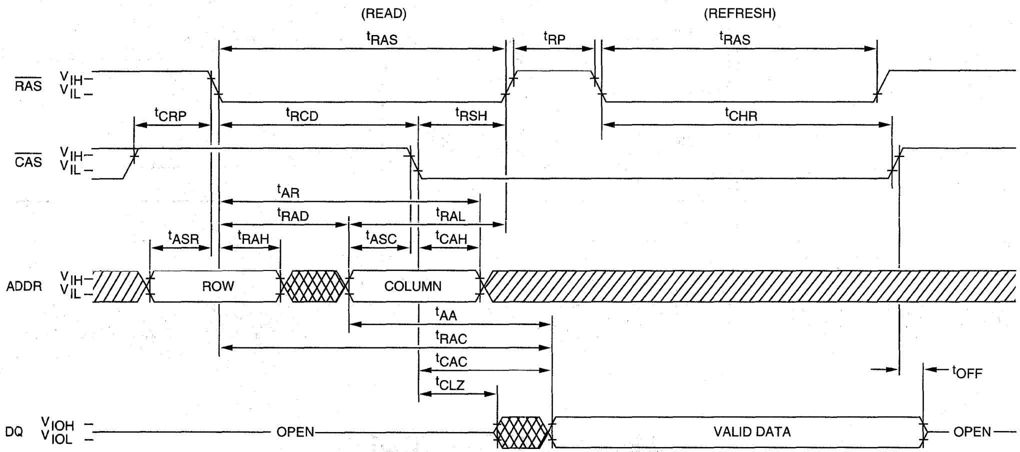
HIDDEN REFRESH CYCLE [23]

(WE = HIGH)



DRAM SIMM

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DRAM DIMM PRODUCT SELECTION GUIDE

Memory Configuration		Part Number	Optional Access Cycle	Access Time (ns)	Typical Power Dissipation		No. of Pins DIMM	Page
					Standby	Active		
3.3V DIMMs								
1 Meg x 32	3.3V	MT2LD(T)132H		60, 70	6mW	500mW	72	5-1
1 Meg x 32	3.3V	MT2LD(T)132H S	S	60, 70	.6mW	500mW	72	5-1
2 Meg x 32	3.3V	MT4LD(T)232H		60, 70	12mW	506mW	72	5-1
2 Meg x 32	3.3V	MT4LD(T)232H S	S	60, 70	1.2mW	501mW	72	5-1
4 Meg x 32	3.3V	MT8LD(T)432H		60, 70	8mW	1,440mW	72	5-15
4 Meg x 32	3.3V	MT8LD(T)432H S	S	60, 70	2.4mW	1,440mW	72	5-15
1 Meg x 64	3.3V	MT16LD(T)164		60, 70	19.2mW	1,600mW	168	5-47
1 Meg x 64	3.3V	MT16LD(T)164 S	S	60, 70	4.8mW	1,600mW	168	5-47
2 Meg x 64	3.3V	MT8LD(T)264		60, 70	8mW	1,600mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 S	S	60, 70	2.4mW	1,600mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 X	EDO	60, 70	8mW	1,200mW	168	5-69
2 Meg x 64	3.3V	MT8LD(T)264 XS	EDO, S	60, 70	2.4mW	1,200mW	168	5-69
4 Meg x 64	3.3V	MT16LD(T)464		60, 70	16mW	2,880mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 S	S	60, 70	4.8mW	2,880mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 X	EDO	60, 70	16mW	2,400mW	168	5-47
4 Meg x 64	3.3V	MT16LD(T)464 XS	EDO, S	60, 70	6.4mW	2,400mW	168	5-47
1 Meg x 72	3.3V	MT18LD(T)172		60, 70	21.6mW	1,800mW	168	5-109
1 Meg x 72	3.3V	MT18LD(T)172 S	S	60, 70	5.4mW	1,800mW	168	5-109
2 Meg x 72	3.3V	MT9LD(T)272		60, 70	9mW	1,800mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 S	S	60, 70	2.7mW	1,800mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 X	EDO	60, 70	9mW	1,350mW	168	5-131
2 Meg x 72	3.3V	MT9LD(T)272 XS	EDO, S	60, 70	2.7mW	1,350mW	168	5-131
4 Meg x 72	3.3V	MT18LD(T)472		60, 70	18mW	3,240mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 S	S	60, 70	5.4mW	3,240mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 X	EDO	60, 70	18mW	2,700mW	168	5-109
4 Meg x 72	3.3V	MT18LD(T)472 XS	EDO, S	60, 70	5.4mW	2,700mW	168	5-109
5V DIMMs								
1 Meg x 64	5V	MT16D(T)164		60, 70	48mW	3,600mW	168	5-29
1 Meg x 64	5V	MT16D(T)164 S	S	60, 70	12.8mW	3,600mW	168	5-29
4 Meg x 64	5V	MT16D(T)464		60, 70	48mW	4,000mW	168	5-29
1 Meg x 72	5V	MT18D(T)172		60, 70	54mW	4,050mW	168	5-91
1 Meg x 72	5V	MT18D(T)172 S	S	60, 70	14.4mW	4,050mW	168	5-91
4 Meg x 72	5V	MT18D(T)472		60, 70	54mW	4,500mW	168	5-91

EDO = Extended Data-Out; S = SELF REFRESH

SMALL-OUTLINE DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTE, 3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, small-outline, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process.
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 12mW standby; 506mW active, typical (8MB)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended CBR and SELF
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle extended refresh distributed across 128ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
72-pin Small-Outline DIMM (gold)	G
• Refresh	
Standard/16ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

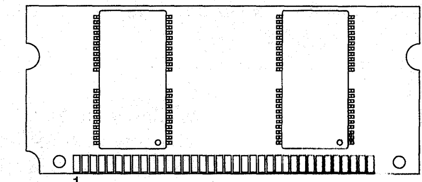
VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT2LDT132HG-xx	1 Meg x 32, TSOP
MT2LDT132HG-xx S	1 Meg x 32, SELF REFRESH, TSOP
MT2LD132HG-xx	1 Meg x 32, SOJ
MT2LD132HG-xx S	1 Meg x 32, SELF REFRESH, SOJ
MT4LDT232HG-xx	2 Meg x 32, TSOP
MT4LDT232HG-xx S	2 Meg x 32, SELF REFRESH, TSOP
MT4LD232HG-xx	2 Meg x 32, SOJ
MT4LD232HG-xx S	2 Meg x 32, SELF REFRESH, SOJ

PIN ASSIGNMENT (Front View)

72-Pin Small-Outline DIMM

(DE-4) SOJ, (DE-1) TSOP 1 Meg x 32
(DE-6) SOJ, (DE-2) TSOP 2 Meg x 32



PIN #	FRONT	PIN #	BACK	PIN #	FRONT	PIN #	BACK
1	Vss	2	DQ0	37	DQ16	38	DQ17
3	DQ1	4	DQ2	39	Vss	40	$\overline{CAS0}$
5	DQ3	6	DQ4	41	$\overline{CAS2}$	42	$\overline{CAS3}$
7	DQ5	8	DQ6	43	$\overline{CAS1}$	44	$\overline{RAS0}$
9	DQ7	10	Vcc	45	NC/$\overline{RAS1}$*	46	NC
11	PRD1	12	A0	47	$\overline{WE}$	48	NC
13	A1	14	A2	49	DQ18	50	DQ19
15	A3	16	A4	51	DQ20	52	DQ21
17	A5	18	A6	53	DQ22	54	DQ23
19	NC	20	NC	55	NC	56	DQ24
21	DQ8	22	DQ9	57	DQ25	58	DQ26
23	DQ10	24	DQ11	59	DQ27	60	DQ28
25	DQ12	26	DQ13	61	Vcc	62	DQ29
27	DQ14	28	A7	63	DQ30	64	DQ31
29	NC	30	Vcc	65	NC	66	PRD2
31	A8	32	A9	67	PRD3	68	PRD4
33	NC/$\overline{RAS3}$*	34	$\overline{RAS2}$	69	PRD5	70	PRD6
35	DQ15	36	NC	71	PRD7	72	Vss

*8MB version only

GENERAL DESCRIPTION

The MT2LD(T)132H(S) and MT4LD(T)232H(S) are randomly accessed 4MB and 8MB solid-state memories organized in a small outline x32 configuration. They are specially processed to operate from +3.0V to 3.6V for low voltage memory systems. The modules have optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

The wider voltage range on these modules allows them to be used in +3.3V ±0.3V memory designs. On the SELF REFRESH version, the refresh period is also extended from the standard 16ms to 128ms to provide maximum power

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GENERAL DESCRIPTION (continued)

savings. The SELF REFRESH cycle allows the module to perform the extended refresh by itself. This eliminates the need to toggle the RAS clock during a sleep mode.

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

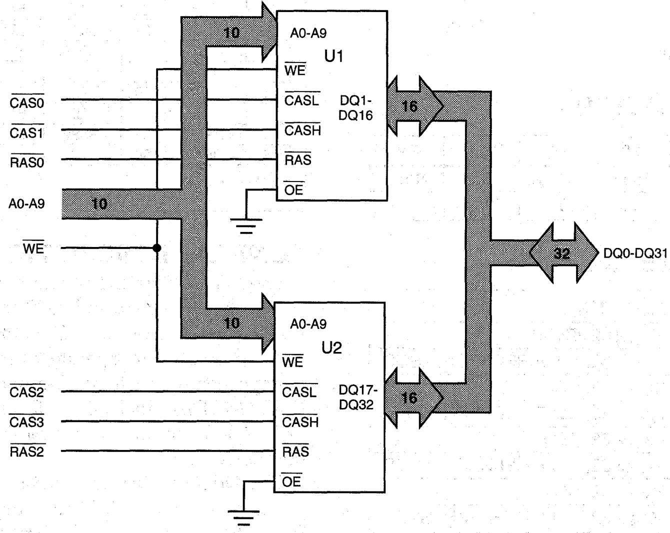
REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes burst refresh sequence, all 1,024 rows must be refreshed within 300µs, prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM
MT2LD(T)132H (4MB)



U1-U2 = MT4LC1M16C3 (S)

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STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ0 to DQ16, DQ1 to DQ17 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT4LD(T)232H (8MB)

CAS0
CAS1
RAS0
WE
CAS2
CAS3
RAS2
A0-A9
RAS1
RAS3

U1: A0-A9, WE, CASL, CASH, RAS, OE, DQ1-DQ16
U2: A0-A9, WE, CASL, CASH, RAS, OE, DQ17-DQ32
U3: A0-A9, WE, CASL, CASH, RAS, OE, DQ1-DQ16
U4: A0-A9, WE, CASL, CASH, RAS, OE, DQ17-DQ32

DQ0-DQ31
DQ0-DQ31

U1-U4 = MT4LC1M16C3 (S)

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT2LD(T)132H (4MB)

SYMBOL	PIN #	-6	-7
PRD1	11	NC	NC
PRD2	66	Vss	Vss
PRD3	67	Vss	Vss
PRD4	68	NC	NC
PRD5	69	NC	Vss
PRD6	70	NC	NC
PRD7	71	X*	X*

* NC= Normal Refresh / Vss = S version only

JEDEC DEFINED PRESENCE-DETECT - MT4LD(T)232H (8MB)

SYMBOL	PIN #	-6	-7
PRD1	11	NC	NC
PRD2	66	Vss	Vss
PRD3	67	Vss	Vss
PRD4	68	Vss	Vss
PRD5	69	NC	Vss
PRD6	70	NC	NC
PRD7	71	X*	X*

* NC= Normal Refresh / Vss = S version only

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O pins
relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	II1	-2	2	µA	
Any input 0V ≤ VIN ≤ 5.5V	A0-A9, $\overline{WE}$	II2	-8	8	µA	29
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	II3	-4	4	µA	29
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ0-DQ31	IOZ	-20	20	µA	29
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	4MB 8MB	4 8	4 8	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	4MB 8MB	1 2	1 2	mA	30
	I_{CC2} (S only)	4MB 8MB	0.3 0.6	0.3 0.6	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	4MB 8MB	340 344	310 314	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	4MB 8MB	200 204	180 184	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB	320 324	290 294	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB	300 304	280 284	mA	19, 22
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = Vcc -2V, A0-A9 and D_{IN} = Vcc -0.2V (D_{IN} may be left open); ^tRC = 125µs	I_{CC7} (S only)	4MB 8MB	0.6 1.2	0.6 1.2	mA	19, 22
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB 8MB	0.6 1.2	0.6 1.2	mA	19

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CAPACITANCE

PARAMETER	SYMBOL	4MB	8MB	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	14	26	pF	17
Input Capacitance: $\overline{WE}$	C_{I2}	18	34	pF	17
Input Capacitance: $\overline{RAS0}$ - $\overline{RAS3}$	C_{I3}	10	10	pF	17
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS3}$	C_{I4}	10	20	pF	17
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35	ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	50		55		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		15		20	ns	9
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	27
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	15		15		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	25
$\overline{CAS}$ precharge time	^tCP	10		10		ns	18
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		ns	
$\overline{CAS}$ hold time	^tCSH	60		70		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		ns	19
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		15		ns	15
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	15
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	12, 25
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	n/a		n/a		ns	21
Access time from $\overline{RAS}$	^tRAC		60		70	ns	8
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	23
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	^tRASS	100		100		µs	27
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	13
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	14
Read command setup time	^tRCS	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (1,024 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^tRPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	14
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
READ-WRITE cycle time	^tRWC	n/a		n/a		ns	21
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	28

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NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ refresh ycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
14. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. V_{CC} = +3.3V ±0.3V; f = 1 MHz.
18. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
21. LATE WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to $\overline{OE}$ being grounded on U1-U2/U4.
22. I_{CC} is dependent on cycle rates.
23. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
24. Applies to S version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. When exiting the SELF REFRESH mode, a complete set of row refreshes should be executed in order to ensure that the DRAM will be fully refreshed. Alternatively, distributed refreshes may be utilized, provided CBR refreshes are employed.
28. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
29. 4MB module values will be half of those shown.
30. All other inputs at 0.2V or V_{CC} -0.2V.

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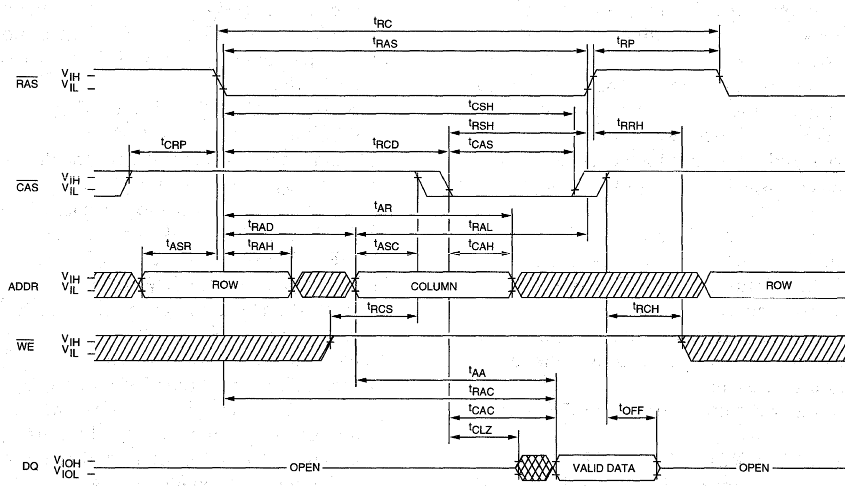
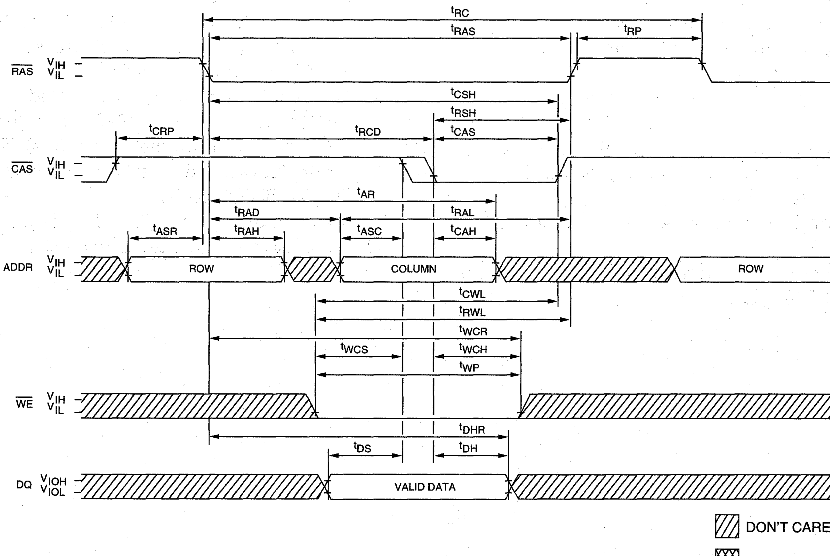
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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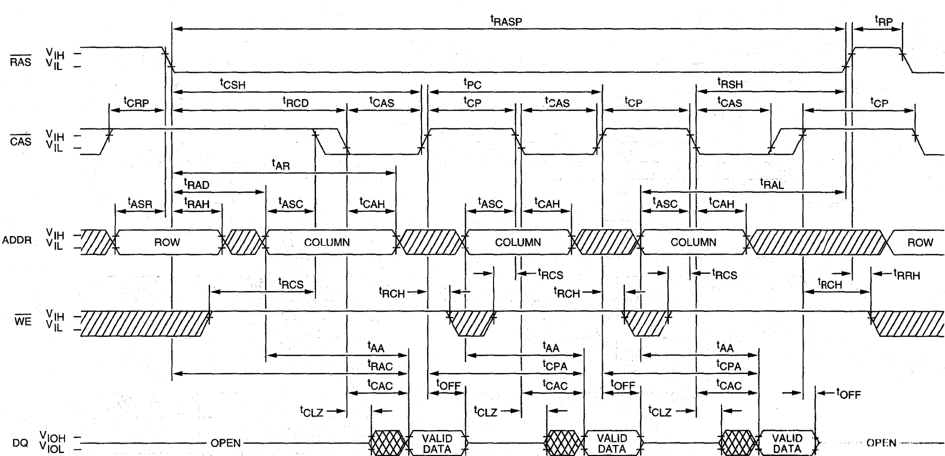
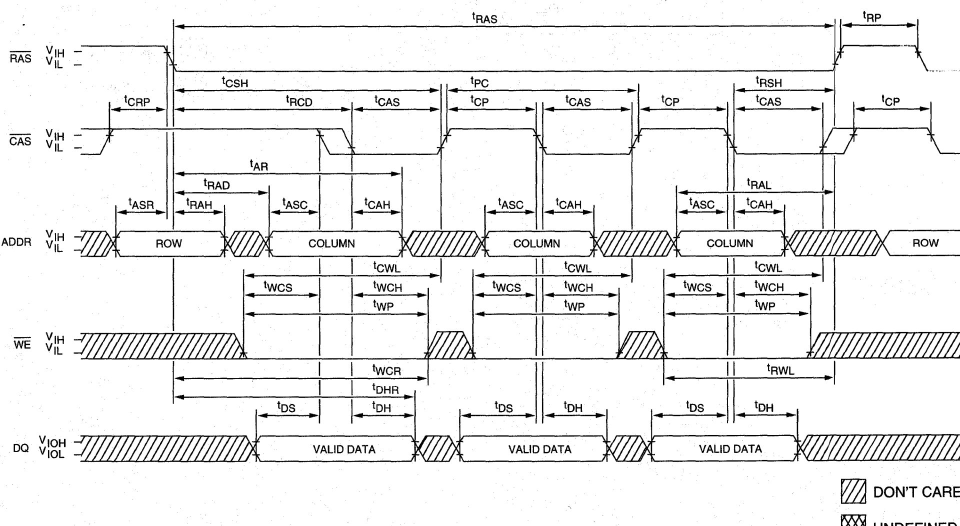
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



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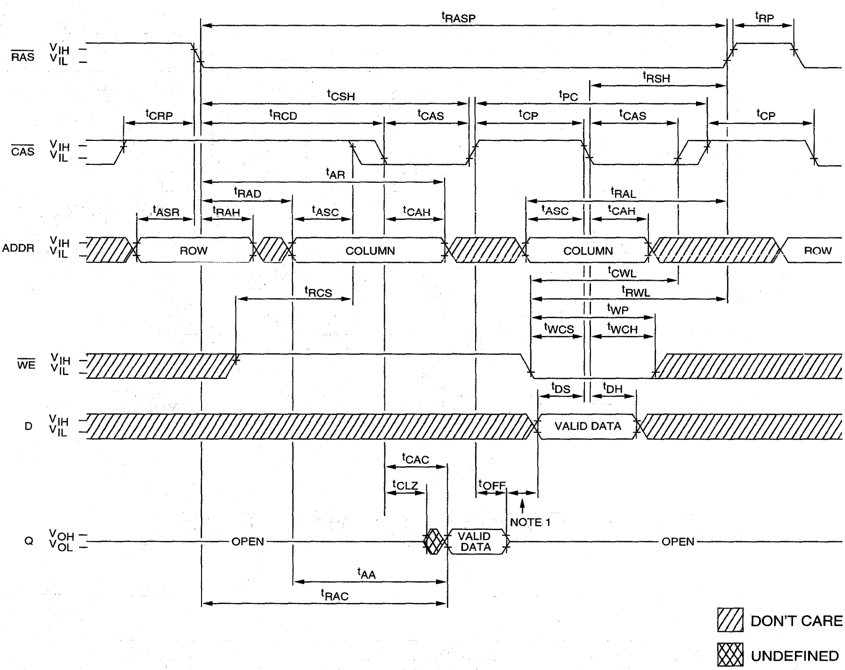
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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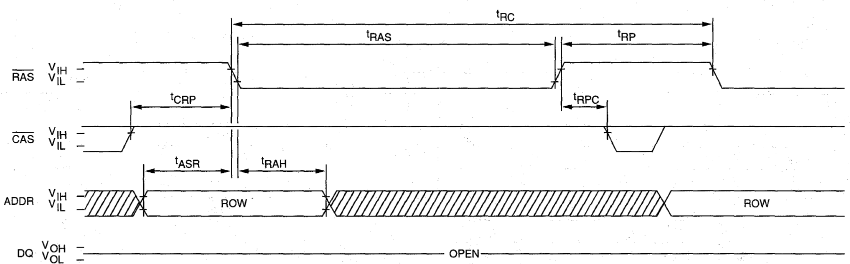
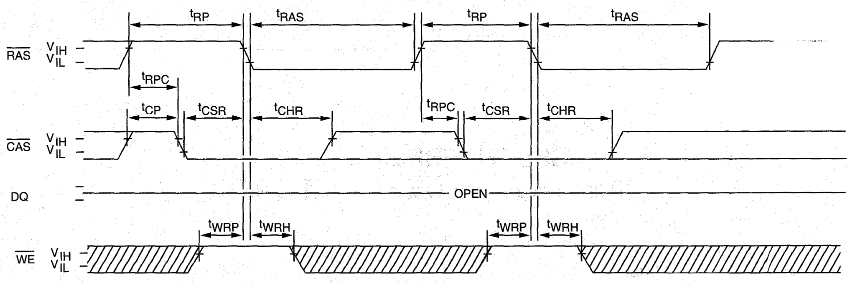
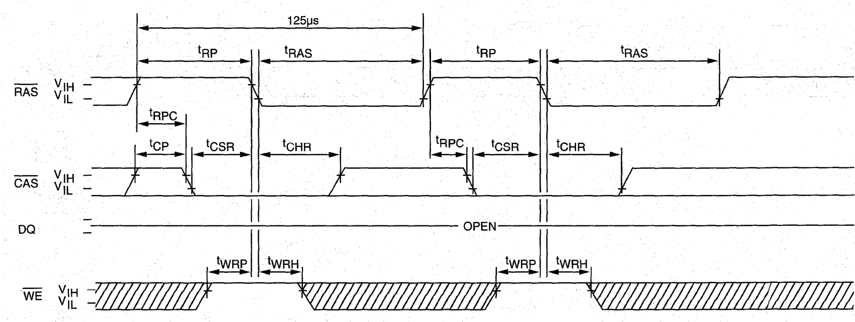
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses = DON'T CARE)



EXTENDED CBR REFRESH CYCLE [24]
(Addresses = DON'T CARE)



DON'T CARE
UNDEFINED

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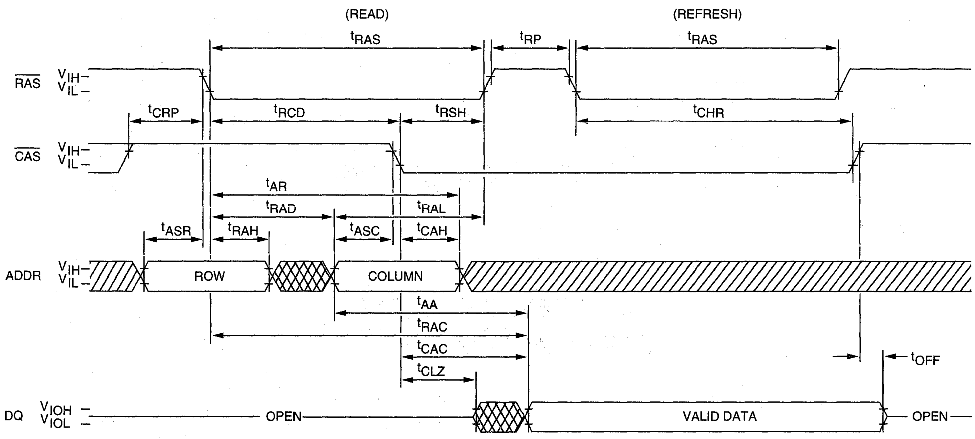
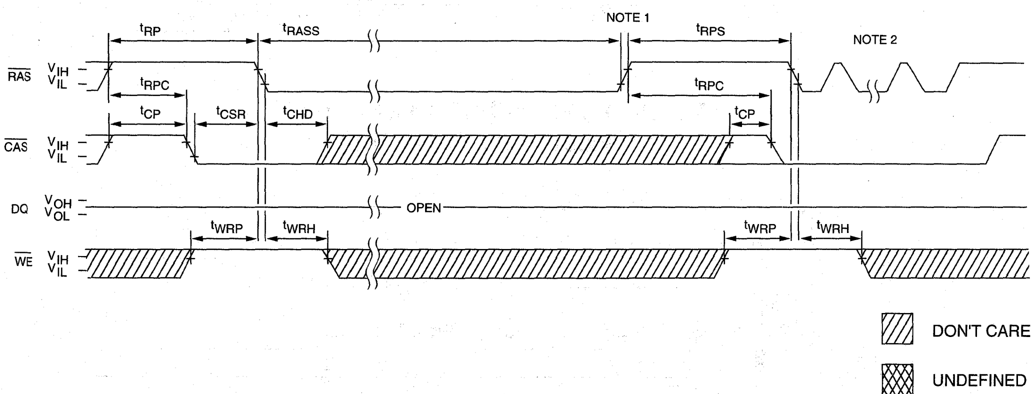
NEW DRAM DIMM

HIDDEN REFRESH CYCLE [20]
(WE = HIGH)



SELF REFRESH CYCLE
(Addresses and OE = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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SMALL-OUTLINE DRAM MODULE

4 MEG x 32

16 MEGABYTE, 3.3V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, small-outline, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process.
- Single +3.3V ±3V power supply
- All device pins are TTL-compatible
- Low power, 2.4mW standby; 1,440mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional Extended and SELF REFRESH
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle extended refresh distributed across 128ms
- FAST PAGE MODE (FPM) access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
72-pin Small-Outline DIMM (gold)	G
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

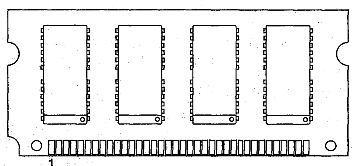
VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8LD432HG-xx	4 Meg x 32, SOJ
MT8LD432HG- xx S	4 Meg x 32, S*, SOJ
MT8LDT432HG-xx	4 Meg x 32, TSOP
MT8LDT432HG- xx S	4 Meg x 32, S*, TSOP

*S = SELF REFRESH

PIN ASSIGNMENT (Front View)

72-Pin Small-Outline DIMM
(DE-5) SOJ version
(DE-3) TSOP version



PIN #	FRONT	PIN #	BACK	PIN #	FRONT	PIN #	BACK
1	Vss	2	DQ0	37	DQ16	38	DQ17
3	DQ1	4	DQ2	39	Vss	40	$\overline{CAS0}$
5	DQ3	6	DQ4	41	$\overline{CAS2}$	42	$\overline{CAS3}$
7	DQ5	8	DQ6	43	$\overline{CAS1}$	44	$\overline{RAS0}$
9	DQ7	10	Vcc	45	NC	46	NC
11	PD1	12	A0	47	$\overline{WE}$	48	NC
13	A1	14	A2	49	DQ18	50	DQ19
15	A3	16	A4	51	DQ20	52	DQ21
17	A5	18	A6	53	DQ22	54	DQ23
19	A10	20	NC	55	NC	56	DQ24
21	DQ8	22	DQ9	57	DQ25	58	DQ26
23	DQ10	24	DQ11	59	DQ27	60	DQ28
25	DQ12	26	DQ13	61	Vcc	62	DQ29
27	DQ14	28	A7	63	DQ30	64	DQ31
29	NC	30	Vcc	65	NC	66	PRD2
31	A8	32	A9	67	PRD3	68	PRD4
33	NC	34	$\overline{RAS2}$	69	PRD5	70	PRD6
35	DQ15	36	NC	71	PRD7	72	Vss

GENERAL DESCRIPTION

The MT8LD(T)432 is a randomly accessed 16MB solid-state memory organized in a small outline x32 configuration. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems. The module has an optional FAST PAGE MODE, which allows faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary.

The wider voltage range on this module allows them to be used in +3.3V ±0.3V memory designs. On the SELF REFRESH version, the refresh period is also extended from the standard 32ms to 128ms to provide maximum power savings.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered

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GENERAL DESCRIPTION (continued)

11 bits (A0-A10) at a time. RAS is used to latch the first 11 bits and CAS the latter 11 bits.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all combinations of RAS addresses (A0-A10) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes burst refresh sequence, all 2,048 rows must be refreshed within 300µs, prior to the resumption of normal operation.

STANDBY

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

x16 OPERATION

For x16 applications, the corresponding DQ and CAS pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organization.

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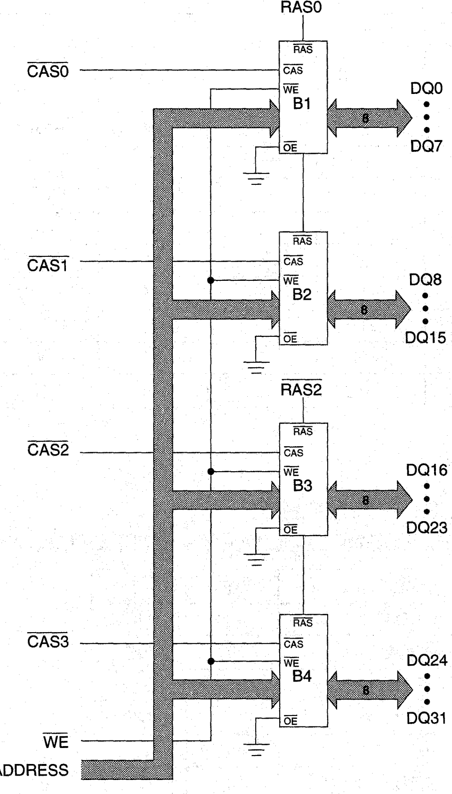
FUNCTIONAL BLOCK DIAGRAM
MT8LD(T)432H (16MB)



NOTE: 1. B1 - B4 are x8 memory blocks consisting of 2-MT4C4M4B1(S) DRAMs each.

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

JEDEC DEFINED PRESENCE-DETECT - MT8LD(T)432H (16MB)

SYMBOL	-6	-7
PRD1	NC	NC
PRD2	NC	NC
PRD3	Vss	Vss
PRD4	NC	NC
PRD5	NC	Vss
PRD6	NC	NC
PRD7	X*	X*

* NC = Normal Refresh / Vss = S version only

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O pins
relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 6, 22) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$, $\overline{RAS2}$	II1	-8	8	µA	
Any input 0V ≤ VIN ≤ 5.5V	A0-A10, $\overline{WE}$	II2	-16	16	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	II3	-4	4	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ1-DQ32	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = other inputs = V_{CC} -0.2V)	I_{CC2}	16MB	4	4	mA	
	I_{CC2} (S only)	16MB	1.2	1.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB	960	880	mA	2, 22, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	16MB	720	640	mA	2, 22, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	16MB	960	880	mA	22, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	16MB	960	880	mA	19, 22
REFRESH CURRENT: EXTENDED (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs	I_{CC7} (S only)	16MB	2.4	2.4	mA	19, 22
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A10 and D_{IN} = Vcc -0.2V or 0.2V (Din may be left open)	I_{CC7} (S only)	16MB	2.4	2.4	mA	19

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CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	48	pF	17
Input Capacitance: WE	C_{I2}	64	pF	17
Input Capacitance: RAS0, RAS2	C_{I3}	32	pF	17
Input Capacitance: CAS0, CAS1, CAS2, CAS3	C_{I4}	16	pF	17
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	pF	17

NEW DRAM DIMM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to RAS)	^{t}AR	50		55		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from CAS	^{t}CAC		15		20	ns	9
Column-address hold time	^{t}CAH	10		15		ns	
CAS pulse width	^{t}CAS	15	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	^{t}CHD	15		15		ns	27
CAS hold time (CBR REFRESH)	^{t}CHR	15		15		ns	19
CAS to output in Low-Z	^{t}CLZ	3		3		ns	25
CAS precharge time	^{t}CP	10		10		ns	18
Access time from CAS precharge	^{t}CPA		35		40	ns	
CAS to RAS precharge time	^{t}CRP	5		5		ns	
CAS hold time	^{t}CSH	60		70		ns	
CAS setup time (CBR REFRESH)	^{t}CSR	5		5		ns	19
Write command to CAS lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	15
Data-in hold time (referenced to RAS)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	15
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	12, 25
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
Access time from RAS	^{t}RAC		60		70	ns	8
RAS to column-address delay time	^{t}RAD	15	30	15	35	ns	23
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to RAS lead time	^{t}RAL	30		35		ns	
RAS pulse width	^{t}RAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	$^{t}RASP$	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH	$^{t}RASS$	100		100		µs	27
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
RAS to CAS delay time	^{t}RCD	20	45	20	50	ns	13
Read command hold time (referenced to CAS)	^{t}RCH	0		0		ns	14
Read command setup time	^{t}RCS	0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Refresh period (2,048 cycles)	^tREF		32		32	ms	
Refresh period (2,048 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^tRPS	110		130		ns	27
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	14
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	28
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	28

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NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
4. AC characteristics assume tT = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. Measured with a load equivalent to two TTL gates and 100pF and VOL = 0.8 and VOH = 2.0V.
8. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
9. Assumes that tRCD ≥ tRCD (MAX).
10. If CAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
14. Either tRCH or tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U8.
22. Icc is dependent on cycle rates.
23. Operation within the tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, then access time is controlled exclusively by tAA.
24. Applies to S version only.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.
27. If the DRAM controller uses a burst refresh, a burst refresh must be executed upon exiting SELF REFRESH.
28. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of tWRP and tWRH in the CBR REFRESH cycle.

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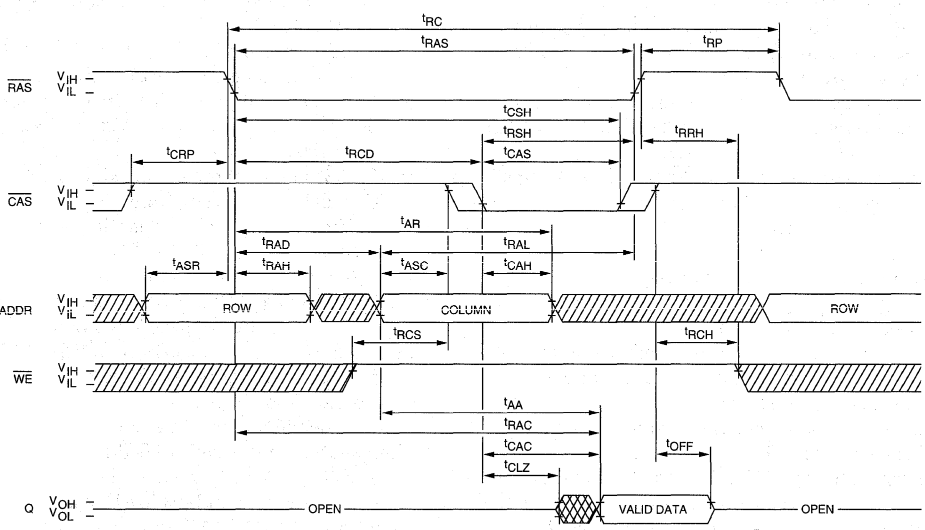
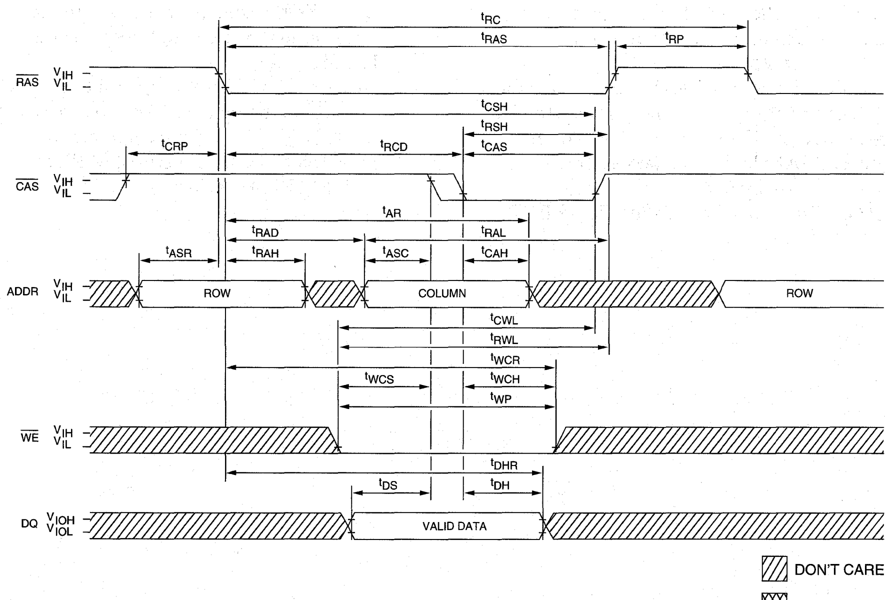
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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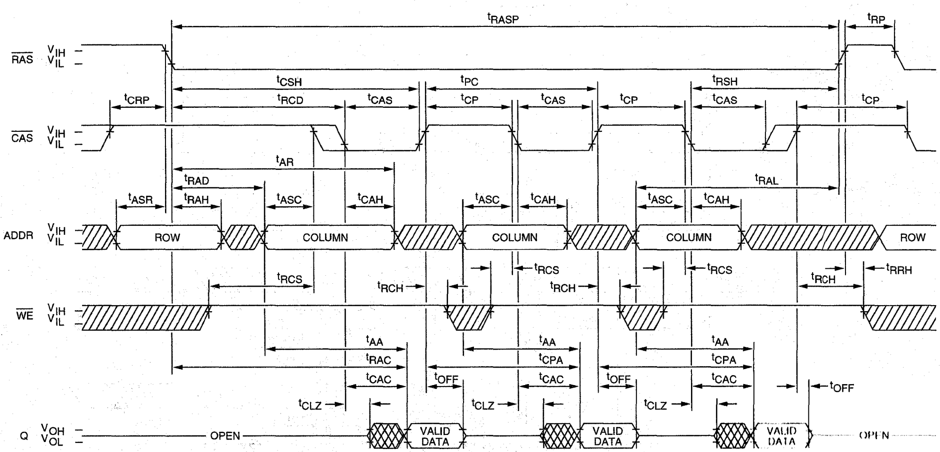
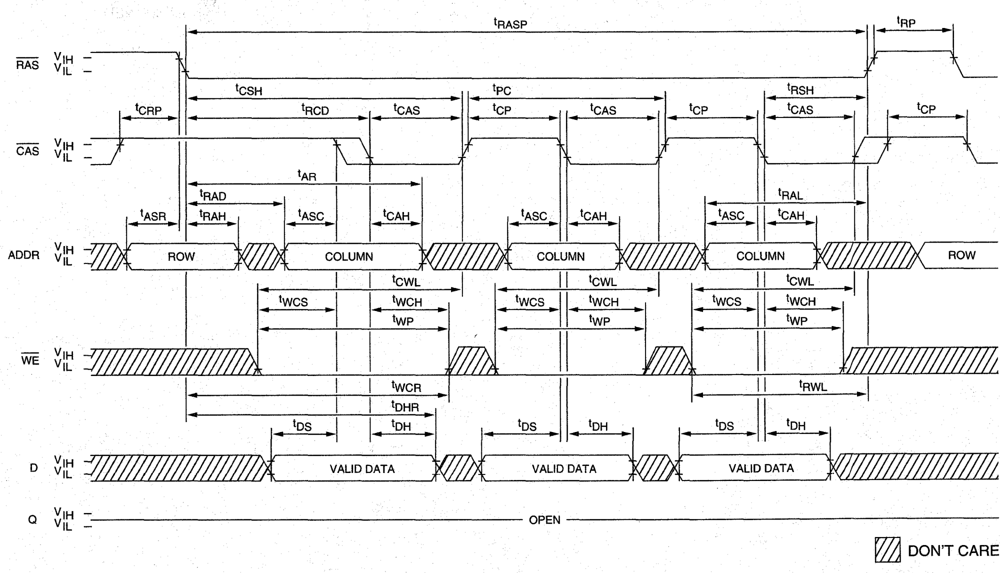
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



NEW DRAM DIMM

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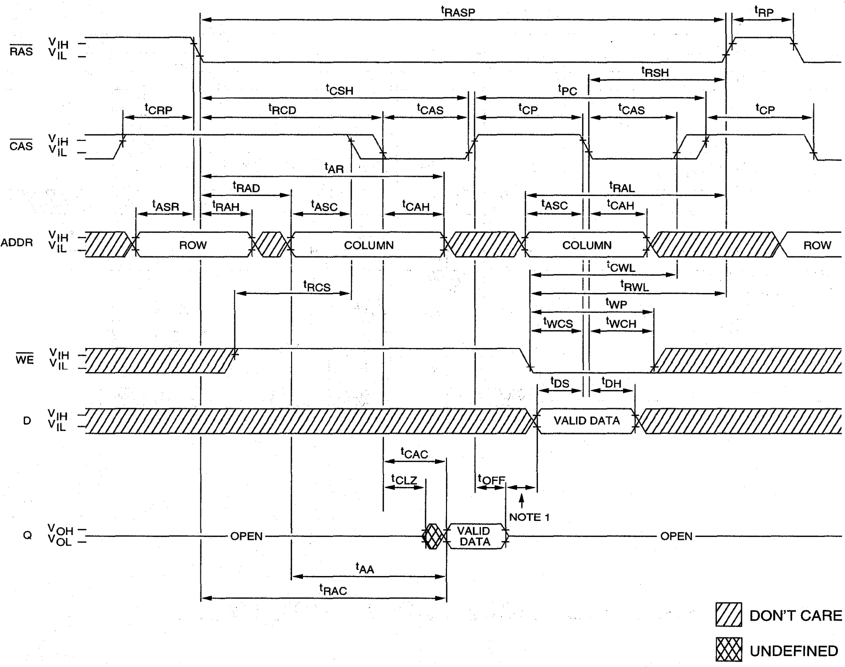
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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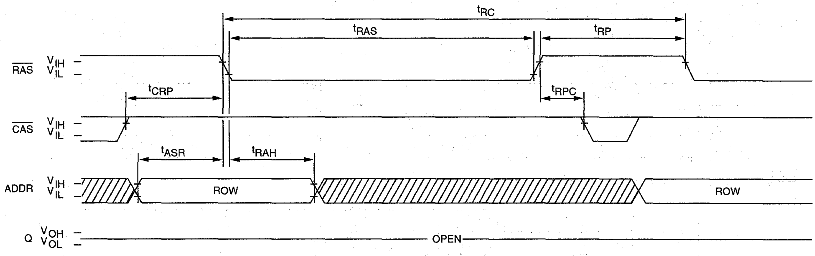
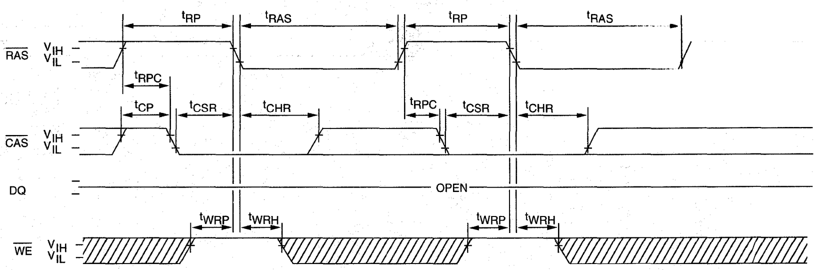
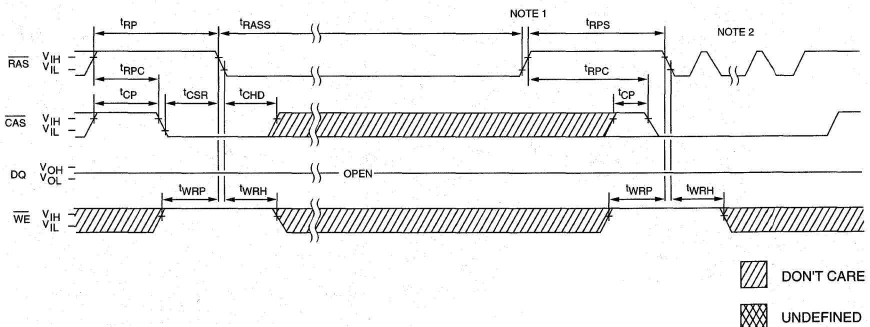
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



CBR REFRESH CYCLE
(Addresses = DON'T CARE)



SELF REFRESH CYCLE 24
(Addresses = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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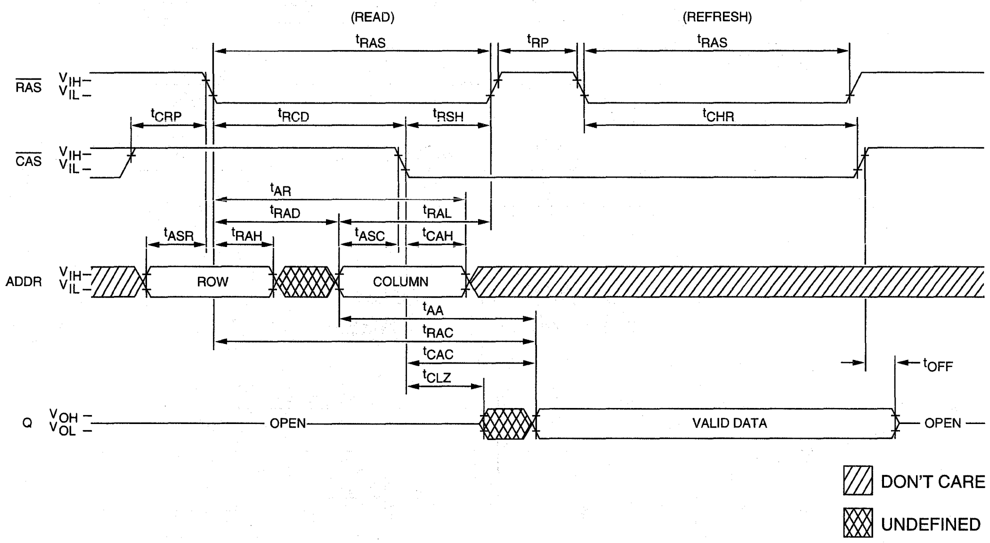
HIDDEN REFRESH CYCLE [20]

($\overline{WE}$ = HIGH)



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DRAM MODULE

1 MEG, 4 MEG x 64

8, 32 MEGABYTE, 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 12.8mW standby; 3,600mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN; optional Extended and SELF REFRESH
- All inputs are buffered except RAS
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms (1 Meg x 64)
- 2,048-cycle refresh distributed across 32ms (4 Meg x 64)
- FAST PAGE MODE (FPM) access cycle

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Refresh	
Standard/16ms or 32	Blank
SELFREFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT16D164G-xx	1 Meg x 64, SOJ
MT16D164G-xx S	1 Meg x 64, S*, SOJ
MT16DT164G-xx	1 Meg x 64, TSOP
MT16DT164G-xx S	1 Meg x 64, S*, TSOP
MT16D464G-xx	4 Meg x 64, SOJ
MT16DT464G-xx	4 Meg x 64, TSOP

*S = SELF REFRESH

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-7) SOJ version
(DE-8) TSOP version

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ32	128	RFU
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS4	88	DQ34	130	CAS5
5	DQ3	47	CAS6	89	DQ35	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ25	111	RFU	153	DQ57
28	CAS0	70	DQ26	112	CAS1	154	DQ58
29	CAS2	71	DQ27	113	CAS3	155	DQ59
30	RAS0	72	DQ28	11	NC	156	DQ60
31	OE0	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC/A10**	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

**4 Meg x 64 version only

DRAM DIMM

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GENERAL DESCRIPTION

The MT16D(T)164(S) and MT16D(T)464 are randomly accessed 8MB and 32MB solid-state memories organized in a x64 configuration.

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0/B0-A10) at a time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63. $\overline{RAS}$ is used to latch the first 10/11 bits and $\overline{CAS}$ the latter 10/11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Correct memory cell data is preserved by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0/B0-A10) are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for extended refresh rates of 125µs (8MB) per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs prior to the resumption of normal operation.

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FUNCTIONAL BLOCK DIAGRAM

DQ0 -- DQ3 DQ4 -- DQ7 DQ8 -- DQ11 DQ12 -- DQ15 DQ16 -- DQ19 DQ20 -- DQ23 DQ24 -- DQ27 DQ28 -- DQ31

DQ32 -- DQ35 DQ36 -- DQ39 DQ40 -- DQ43 DQ44 -- DQ47 DQ48 -- DQ51 DQ52 -- DQ55 DQ56 -- DQ59 DQ60 -- DQ63

PRESENCE-DETECT GENERATOR → PD1-PD8

PDE

1 Meg x 64
U1-U16 = 1 Meg x 4 DRAMs

4 Meg x 64
U1-U16 = 4 Meg x 4 DRAMs

NOTE: 1. All inputs with the exception of $\overline{RAS}$ are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10/11 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149, 151, 153-156, 158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +5V ± 10%
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V_{SS}	Supply	Ground

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	—	No connect.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ0-63
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
• 8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT16D(T)464 uses 11/11 DRAMs.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+0.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0-CAS7}$ A0-A10, B0, $\overline{PDE}$ $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0,2}$	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63 PD1-PD8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB 32MB	32 52	32 52	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8MB 32MB	16 28	16 28	mA	28
	I_{CC2} (S only)	8MB 32MB	3.2 —	3.2 —		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB 32MB	1,760 1,920	1,600 1,760	mA	3, 4, 28, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB 32MB	1,280 1,440	1,120 1,280	mA	3, 4, 28, 32
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	8MB 32MB	1,760 1,920	1,600 1,760	mA	3, 28, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	8MB 32MB	1,760 1,920	1,600 1,760	mA	3, 5, 28
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= V_{CC} -0.2V; A0/B0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (8MB)	I_{CC7} (S only)	8MB 32MB	4.8 —	4.8 —	mA	3, 5, 31
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0/B0-A10 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	8MB 32MB	4.8 —	4.8 —	mA	5, 36

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		64	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		10	pF	2

DRAM DIMM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to $\overline{WE}$ delay time	^tAWD	57		67		ns	23, 30
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		20		ns	25
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	36
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	13		13		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		ns	23, 33
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		ns	25
$\overline{CAS}$ hold time	^tCSH	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	12		12		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	42		52		ns	23, 30
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	15		20		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD		15		20	ns	
Output enable	^tOE		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	15		20		ns	24
Output buffer turn-off delay	^tOFF	5	20	5	25	ns	20, 27

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
$\overline{PDE}$ to valid presence-detect data	^{t}PD		10		10	ns	35
$\overline{PDE}$ inactive to presence-detects inactive	^{t}PDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	87		97		ns	23
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	13	25	13	30	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	^{t}RAL	35		40		ns	25
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	^{t}RASS	100		100		µs	36
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	2		2		ns	19, 23
Read command setup time	^{t}RCS	2		2		ns	23
Refresh period (1,024 cycles) - 1 Meg x 64	^{t}REF		16		16	ms	
Refresh period (2,048 cycles) - 4 Meg x 64	^{t}REF		32		32	ms	
Refresh period (2,048 or 1,024 cycles) S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^{t}RPS	110		130		ns	36
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	20		25		ns	25
READ WRITE cycle time	^{t}RWC	155		185		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	92		102		ns	23, 30
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		25		ns	25
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	15		20		ns	25
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	43		53		ns	24
$\overline{WE}$ command setup time	^{t}WCS	2		2		ns	23
Write command pulse width	^{t}WP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
32. Column-address changed once each cycle.
33. The 3ns minimum parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.

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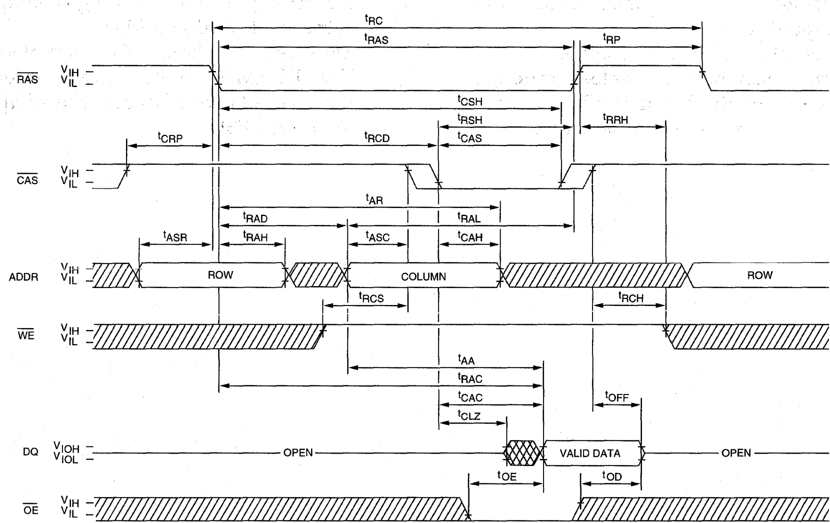
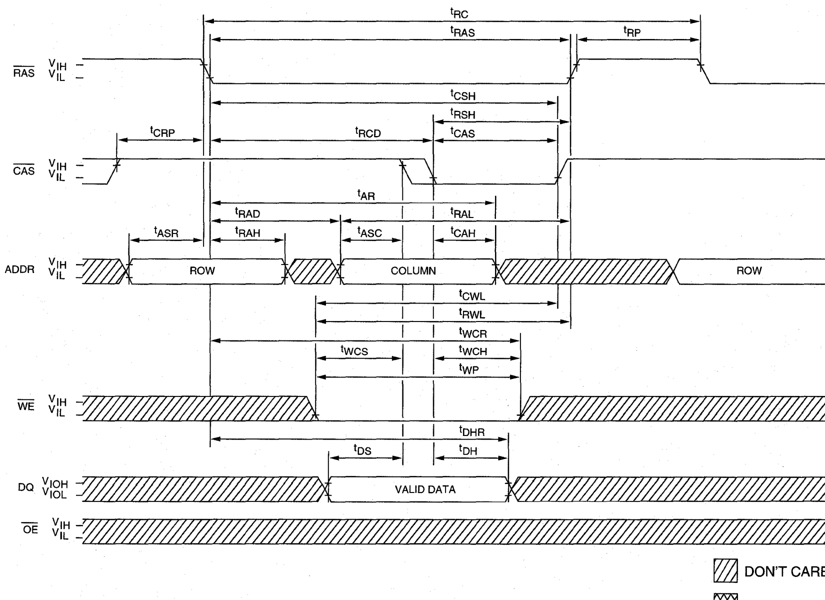
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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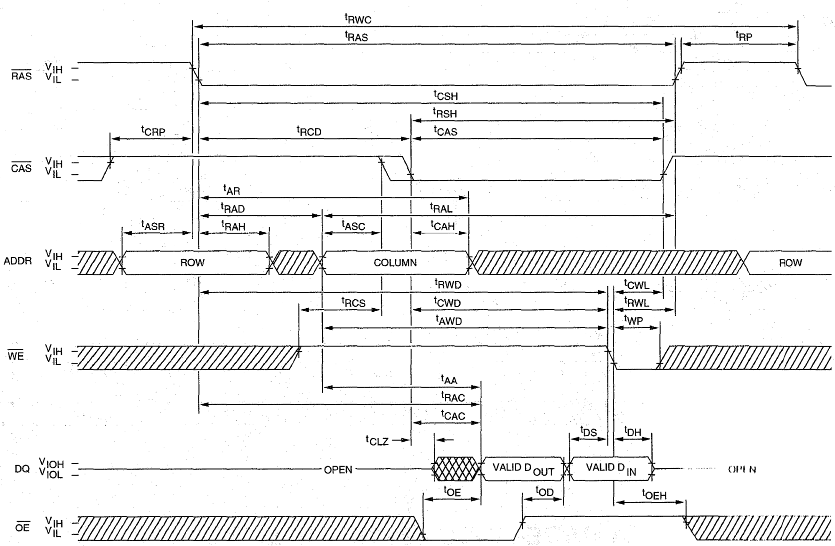
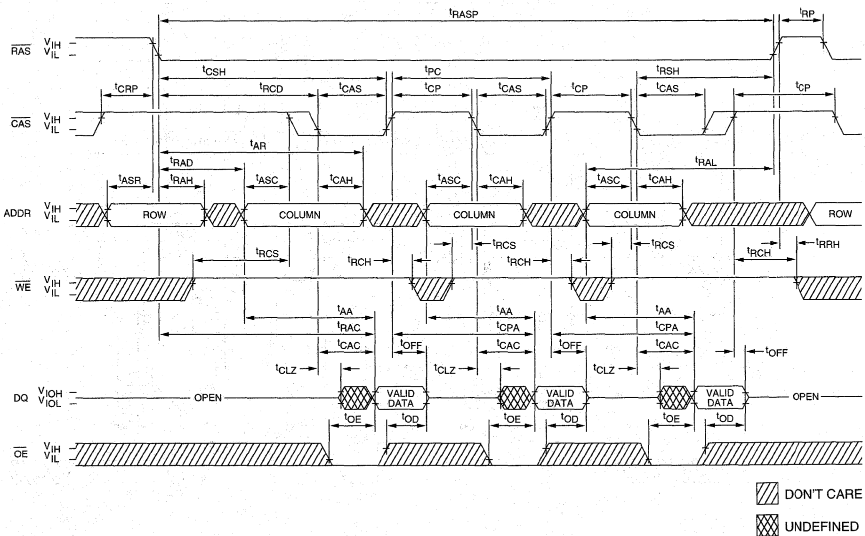
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DRAM DIMM

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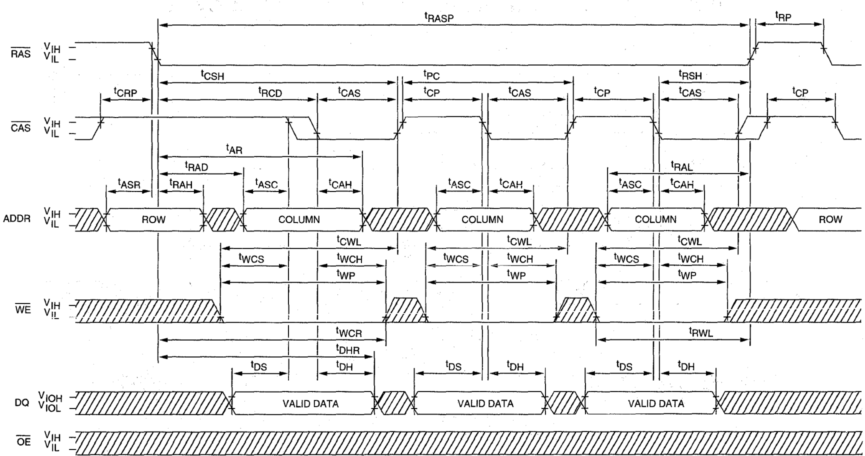
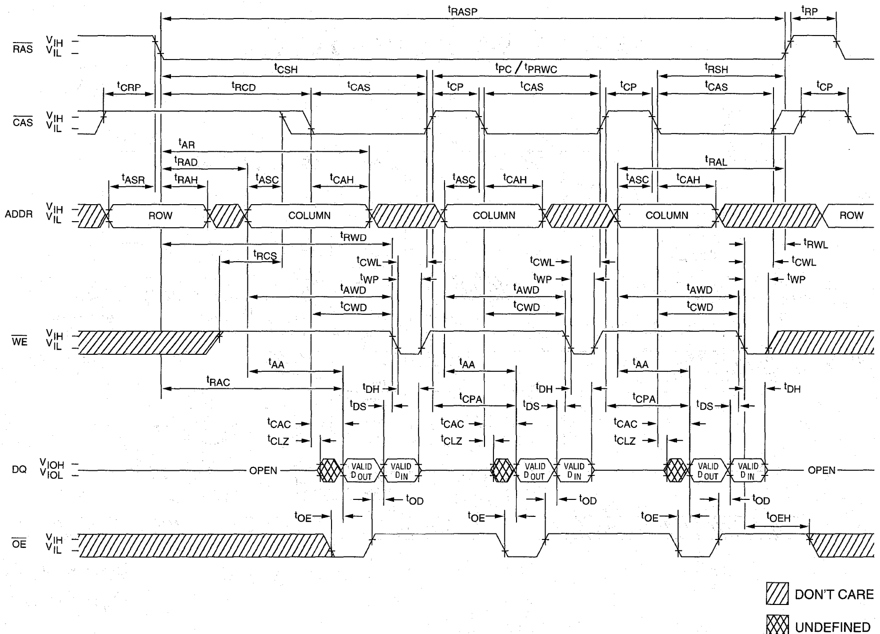
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



DRAM DIMM

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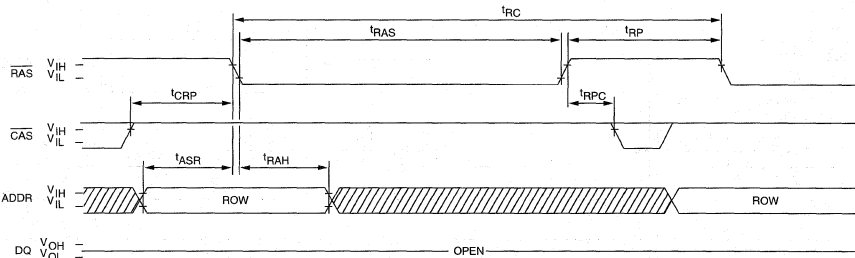
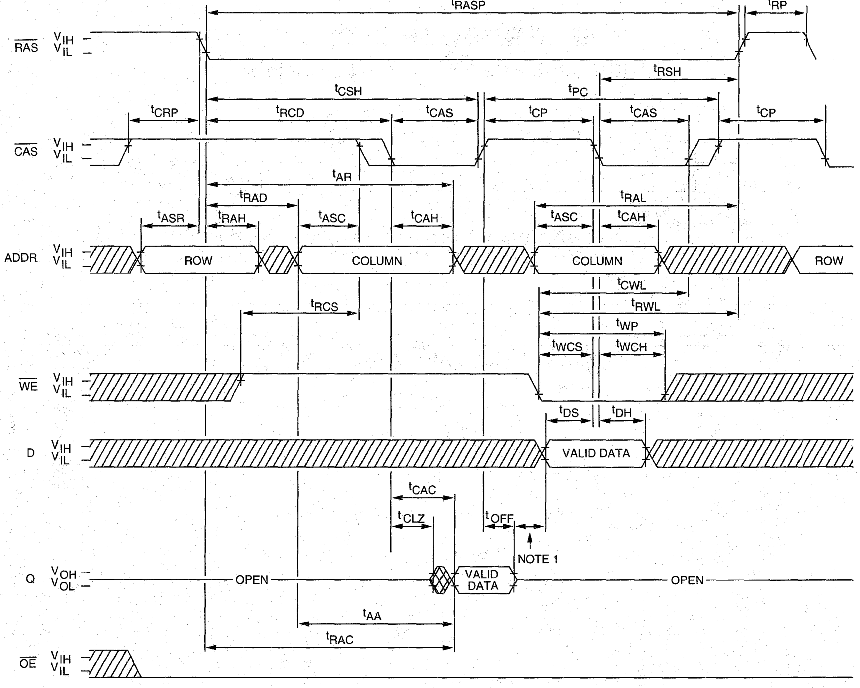
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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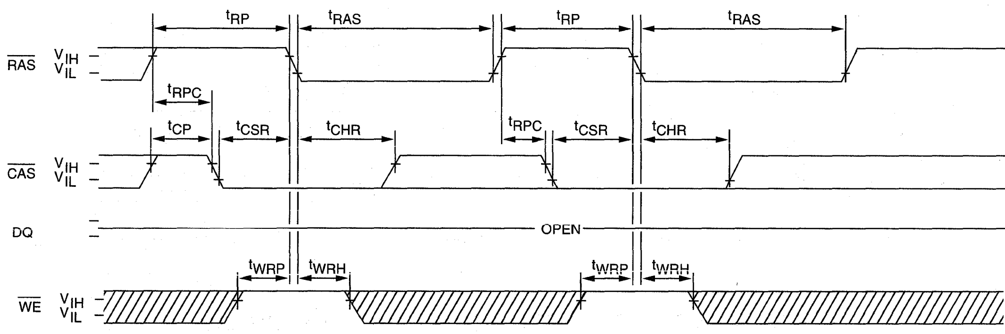
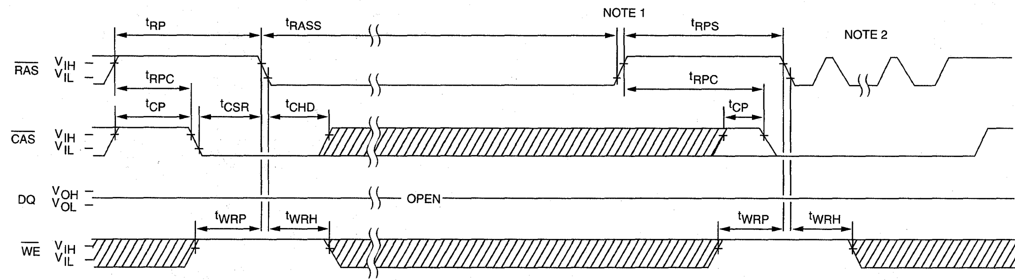
CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

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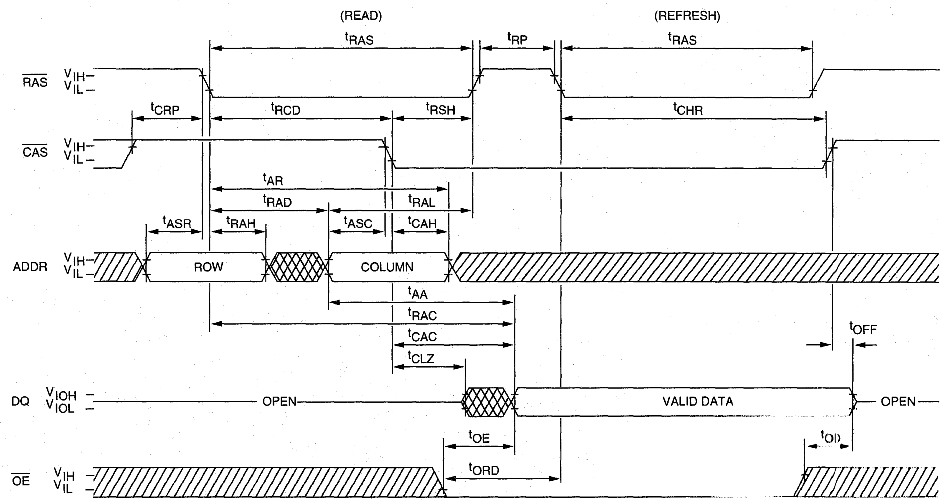
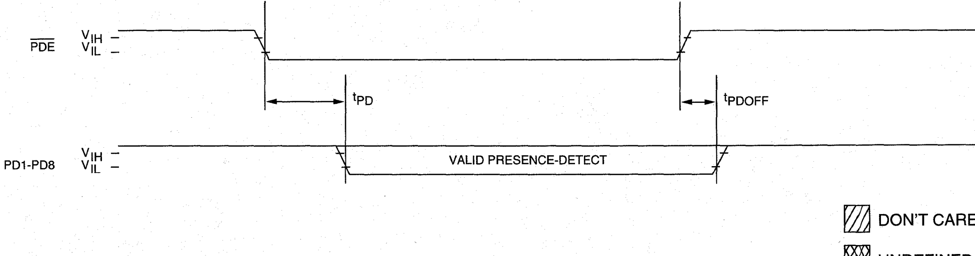
HIDDEN REFRESH CYCLE [21]

(WE = HIGH; OE = LOW)



PRESENCE-DETECT READ CYCLE



DON'T CARE

UNDEFINED

DRAM DIMM

NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

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DRAM MODULE

1 MEG, 4 MEG x 64

8, 32 MEGABYTE, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 16mW standby; 2,880mW active, typical (32MB)
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended and SELF REFRESH
- All inputs are buffered except $\overline{RAS}$
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms (1 Meg x 64)
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms (4 Meg x 64)
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE (4 Meg x 64 only)	X
• Refresh	
Standard/16ms or 32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

EDO option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	35ns	20ns	10ns
-7	130ns	70ns	30ns	40ns	25ns	12ns

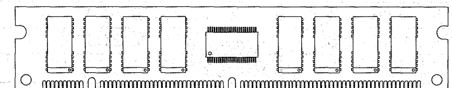
FPM option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-9) SOJ Version
(DE-10) TSOP Version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	CAS7
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	PDF
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC/A10*	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

*4 Meg x 64 version only

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VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT16LD164G-xx	1 Meg x 64 FPM, SOJ
MT16LD164G-xx S	1 Meg x 64 FPM, SOJ, S*
MT16LDT164G-xx	1 Meg x 64 FPM, TSOP
MT16LDT164G-xx S	1 Meg x 64 FPM, TSOP, S*
MT16LDT464G-xx	4 Meg x 64 FPM, TSOP
MT16LDT464G-xx X	4 Meg x 64 EDO, TSOP
MT16LDT464G-xx S	4 Meg x 64 FPM, TSOP, S*
MT16LDT464G-xx XS	4 Meg x 64 EDO, TSOP, S*
MT16LD464G-xx	4 Meg x 64 FPM, SOJ
MT16LD464G-xx X	4 Meg x 64 EDO, SOJ
MT16LD464G-xx S	4 Meg x 64 FPM, SOJ, S*
MT16LD464G-xx XS	4 Meg x 64 EDO, SOJ, S*

*S = SELF REFRESH

GENERAL DESCRIPTION

The MT16LD(T)164(S) and MT16LD(T)464(X)(S) are randomly accessed 8MB and 32MB solid-state memories organized in a x64 configuration. They are specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0 /B0-A10) at a time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63. $\overline{RAS}$ is used to latch the first 10/11 bits and $\overline{CAS}$ the latter 10/11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE - 4 Meg x 64 only

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^{t}CP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z.

If the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last (reference the MT4LC4M4E8(S) DRAM data sheet for additional information on EDO functionality).

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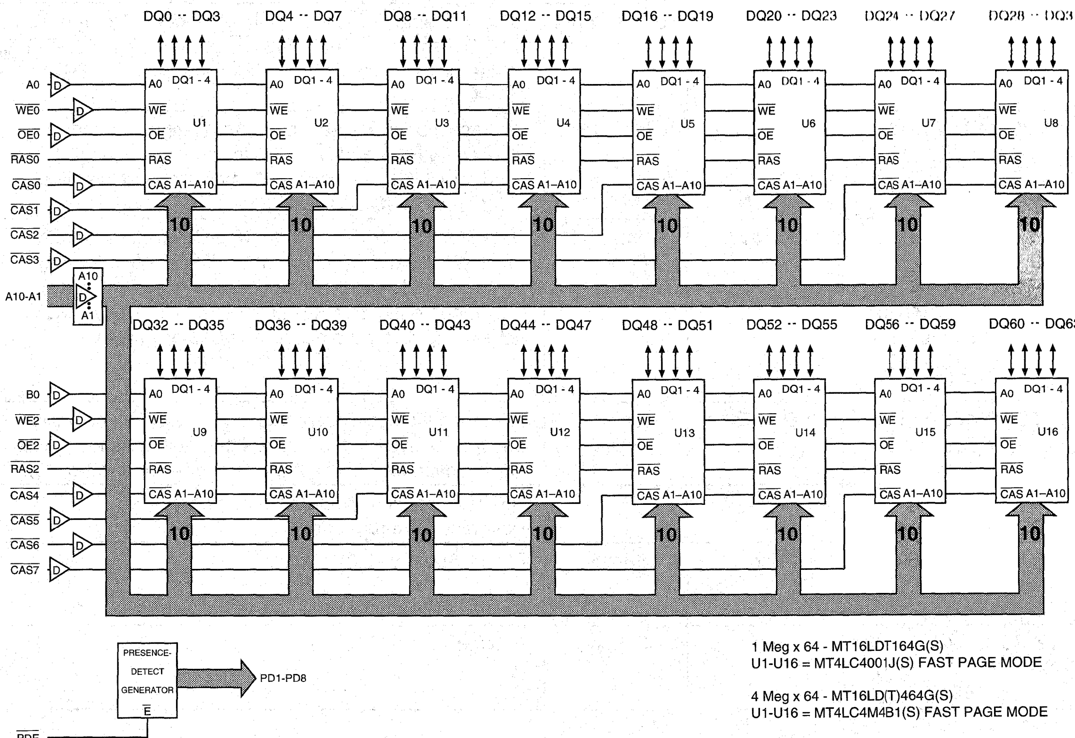
REFRESH

Returning RAS and CAS HIGH terminates a memory cycle, and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is perserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all combinations of RAS addresses (A0/B0-A10) are executed at least every tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An optional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified tRASS. Additionally, the "S" version allows for extended refresh rates of 62.5µs (32MB) and 125µs (8MB) per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024/2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of RAS are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10/11 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149, 151, 153-156, 158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ± 0.3V
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	V_{SS}	Supply	Ground

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	—	No connect.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ0-63
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
• 8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.
* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT16LD(T)464 uses 11/11 DRAMs.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS7}$ A0-A10, B0 $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0,2}$	I_{I2}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB 32MB	16 32	16 32	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	ALL	8	8	mA	28
	I_{CC2} (S only)	8MB 32MB	1.6 2.4	1.6 2.4		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB	1,280	1,120	mA	3, 4, 28,32
		32MB	1,920	1,760		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB	960	800	mA	3, 4, 28,32
		32MB	1,440	1,280		
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC5} (X only)	8MB	—	—	mA	3, 4, 28,32
		32MB	1,760	1,600		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC6}	8MB	1,280	1,120	mA	3, 28, 32
		32MB	1,920	1,760		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	8MB	1,280	1,120	mA	3, 5, 28
		32MB	1,920	1,760		
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs (32MB)/125µs (8MB)	I_{CC8} (S only)	8MB	2.4	2.4	mA	3, 5, 31
		32MB	4.8	4.8		
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC9} (S only)	8MB	2.4	2.4	mA	5, 36
		32MB	4.8	4.8		

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MT16LD(T)164(S), MT16LD(T)464(X)(S) 1 MEG, 4 MEG x 64 DRAM MODULES

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 16W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		64	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ63	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		10	pF	2

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	${}^tAA$		35		40	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	${}^tAR$	48		53		ns	24
Column-address setup time	${}^tASC$	2		2		ns	23
Row-address setup time	${}^tASR$	5		5		ns	25
Column-address to $\overline{WE}$ delay time	${}^tAWD$	57		67		ns	23, 30
Access time from $\overline{CAS}$	${}^tCAC$		20		25	ns	15, 25
Column-address hold time	${}^tCAH$	15		20		ns	25
$\overline{CAS}$ pulse width	${}^tCAS$	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	${}^tCHD$	15		15		ns	36
$\overline{CAS}$ hold time (CBR REFRESH)	${}^tCHR$	8		8		ns	5, 24
$\overline{CAS}$ to output in Low-Z	${}^tCLZ$	5		5		ns	23
$\overline{CAS}$ precharge time	${}^tCP$	10		10		ns	16
Access time from $\overline{CAS}$ precharge	${}^tCPA$		40		45	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	${}^tCRP$	15		15		ns	25
$\overline{CAS}$ hold time	${}^tCSH$	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	${}^tCSR$	12		12		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	${}^tCWD$	42		47		ns	23, 30
Write command to $\overline{CAS}$ lead time	${}^tCWL$	15		20		ns	
Data-in hold time	${}^tDH$	15		20		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	${}^tDHR$	45		55		ns	
Data-in setup time	${}^tDS$	-2		-2		ns	24, 29
Output disable	${}^tOD$		15		20	ns	
Output enable	${}^tOE$		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	${}^tOEH$	13		18		ns	24
Output buffer turn-off delay	${}^tOFF$	5	20	5	25	ns	20,27,38

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
PDE to Valid Presence-Detect Data	^{t}PD		10		10	ns	35
PDE Inactive to Presence-Detects Inactive	^{t}PDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	87		97		ns	23
Access time from RAS	^{t}RAC		60		70	ns	14
RAS to column-address delay time	^{t}RAD	13	25	13	30	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to RAS lead time	^{t}RAL	35		40		ns	25
RAS pulse width	^{t}RAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH	^{t}RASS	100		100		µs	36
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
RAS to CAS delay time	^{t}RCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to CAS)	^{t}RCH	2		2		ns	19, 23
Read command setup time	^{t}RCS	2		2		ns	23
Refresh period (2,048 cycles) - 4 Meg x 64	^{t}REF		32		32	ms	
Refresh period (1,024 cycles) - 1 Meg x 64	^{t}REF		16		16	ms	
Refresh period (1,024 or 2,048 cycles) S version	^{t}REF		128		128	ms	
RAS precharge time	^{t}RP	40		50		ns	
RAS to CAS precharge time	^{t}RPC	0		0		ns	
RAS precharge time during SELF REFRESH	^{t}RPS	110		130		ns	36
Read command hold time (referenced to RAS)	^{t}RRH	0		0		ns	19
RAS hold time	^{t}RSH	20		25		ns	25
READ WRITE cycle time	^{t}RWC	155		185		ns	25
RAS to WE delay time	^{t}RWD	87		97		ns	23, 30
Write command to RAS lead time	^{t}RWL	20		25		ns	25
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	15		20		ns	25
Write command hold time (referenced to RAS)	^{t}WCR	43		53		ns	24
WE command setup time	^{t}WCS	2		2		ns	23, 30
Write command pulse width	^{t}WP	10		15		ns	
WE hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 23

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address setup to CAS precharge during writes	^tACH	15		15		ns	
Column-address hold time (referenced to RAS)	^tAR	43		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to WE delay time	^tAWD	57		67		ns	23, 30
Access time from CAS	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		17		ns	25
CAS pulse width	^tCAS	10	10,000	12	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	36
CAS hold time (CBR REFRESH)	^tCHR	8		10		ns	5, 24
CAS to output in Low-Z	^tCLZ	2		2		ns	23
Data output hold after CAS LOW	^tCOH	7		7		ns	23
CAS precharge time	^tCP	10		10		ns	16
Access time from CAS precharge	^tCPA		40		45	ns	25, 37
CAS to RAS precharge time	^tCRP	10		10		ns	25
CAS hold time	^tCSH	48		53		ns	24
CAS setup time (CBR REFRESH)	^tCSR	7		7		ns	5, 23
CAS to WE delay time	^tCWD	37		42		ns	23, 30
Write command to CAS lead time	^tCWL	15		15		ns	
Data-in hold time	^tDH	15		17		ns	25, 29
Data-in hold time (referenced to RAS)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD	0	15	0	15	ns	
Output enable	^tOE		15		15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	24
OE HIGH hold time from CAS HIGH	^tOEHC	10		10		ns	
OE HIGH pulse width	^tOEP	10		10		ns	
OE LOW to CAS HIGH setup time	^tOES	5		5		ns	
Output buffer turn-off delay	^tOFF	5	20	5	20	ns	20,27,38
OE setup prior to RAS during HIDDEN REFRESH cycle	^tORD	0		0		ns	20
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	25		30		ns	
PDE to valid presence-detect data	^tPD		10		10	ns	35
PDE inactive to presence-detects inactive	^tPDOFF	2		2		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	77		87		ns	23
Access time from RAS	^tRAC		60		70	ns	14
RAS to column-address delay time	^tRAD	10	25	10	30	ns	18, 26
Row-address hold time	^tRAH	8		8		ns	24
Column-address to RAS lead time	^tRAL	35		40		ns	25
RAS pulse width	^tRAS	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	^tRASP	60	125,000	70	125,000	ns	
RAS pulse width during SELF REFRESH	^tRASS	100		100		µs	36
Random READ or WRITE cycle time	^tRC	110		130		ns	
RAS to CAS delay time	^tRCD	12	40	12	45	ns	17, 26

DRAM DIMM

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command hold time (referenced to CAS)	tRCH	2		2		ns	19, 23
Read command setup time	tRCS	2		2		ns	23
Refresh period (2,048 cycles) - 4 Meg x 64	tREF		32		32	ms	
Refresh period (2,048 cycles) S version	tREF		128		128	ms	
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
RAS precharge time during SELF REFRESH	tRPS	110		130		ns	36
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	15		17		ns	25
READ WRITE cycle time	tRWC	155		182		ns	25
RAS to WE delay time	tRWD	82		92		ns	23, 30
Write command to RAS lead time	tRWL	20		20		ns	25
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	15		17		ns	25
Write command hold time (referenced to RAS)	tWCR	43		53		ns	24
WE command setup time	tWCS	2		2		ns	23
Output disable delay from WE (CAS HIGH)	tWHZ	2	18	2	20	ns	27
Write command pulse width	tWP	10		12		ns	
WE pulse width for output disable when CAS HIGH	tWPZ	10		12		ns	
WE hold time (CBR REFRESH)	tWRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	tWRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume tT = 5ns for FPM and 2.5ns for EDO.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If CAS = VIH, data output is High-Z.
12. If CAS = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for tCP.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, access time is controlled exclusively by tCAC.
18. Operation within the tRAD (MAX) limit ensures that tRAC (MIN) and tCAC (MIN) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
22. tWTS and tWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
29. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE WRITE (OE-controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh current increases if ^tRAS is extended beyond its minimum specification.
32. Column-address changed once each cycle.
33. The 3ns minimum parameter guaranteed by design.
34. ^tPDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
37. ^tCAC (MIN), ^tCPA (MIN) and ^tAA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^tCAC (MAX), ^tCPA (MAX) and ^tAA (MAX) are guaranteed.
38. For FAST PAGE MODE option, ^tOFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^tOFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
39. Applies to both EDO and FAST PAGE MODEs.

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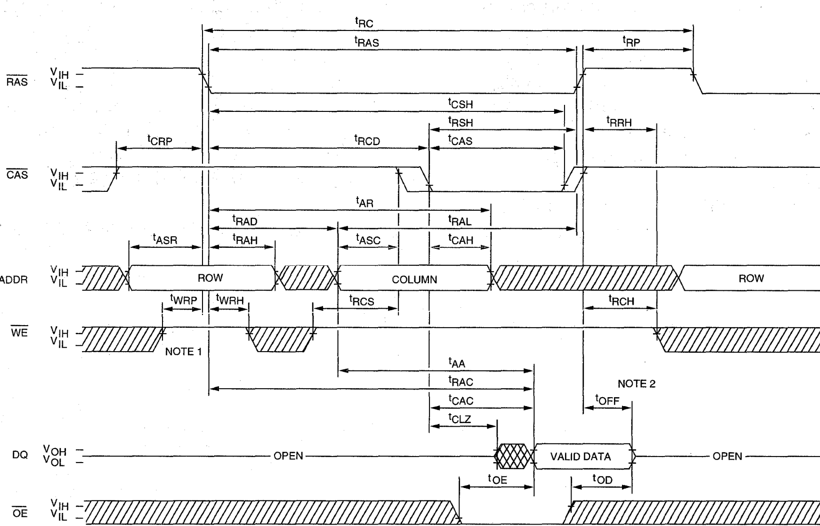
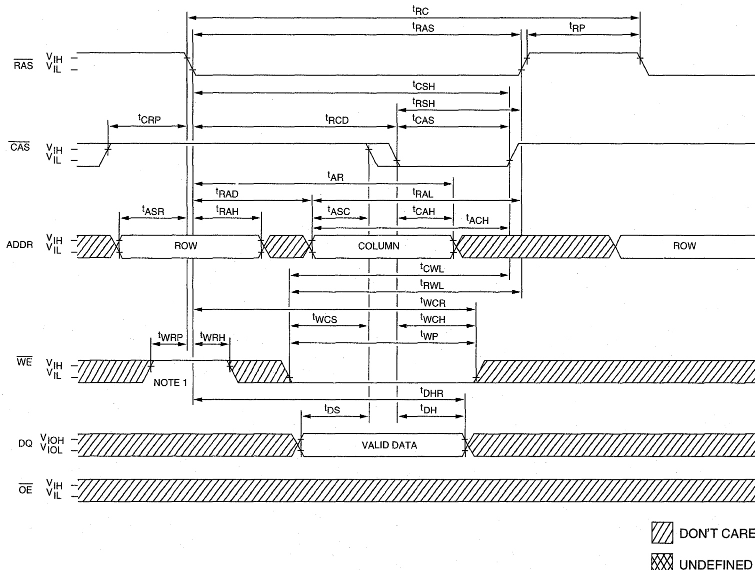
READ CYCLE [39]



EARLY WRITE CYCLE [39]



DON'T CARE

UNDEFINED

NOTE:

1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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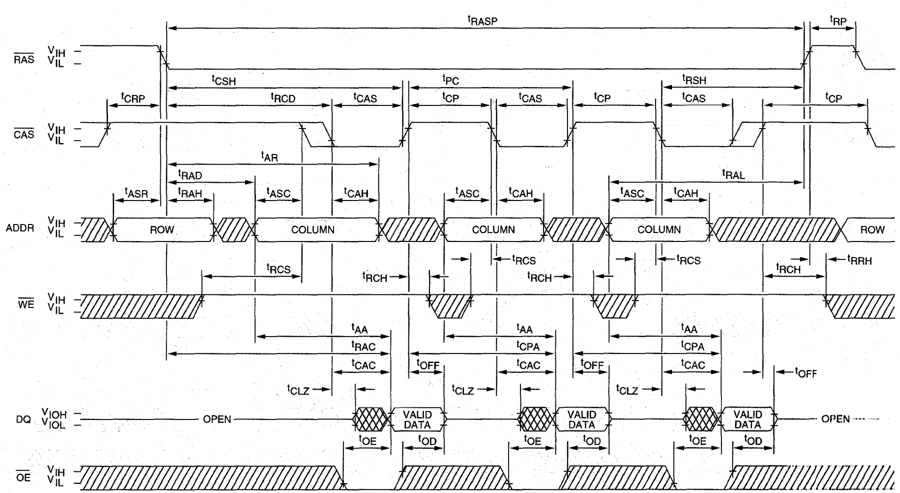
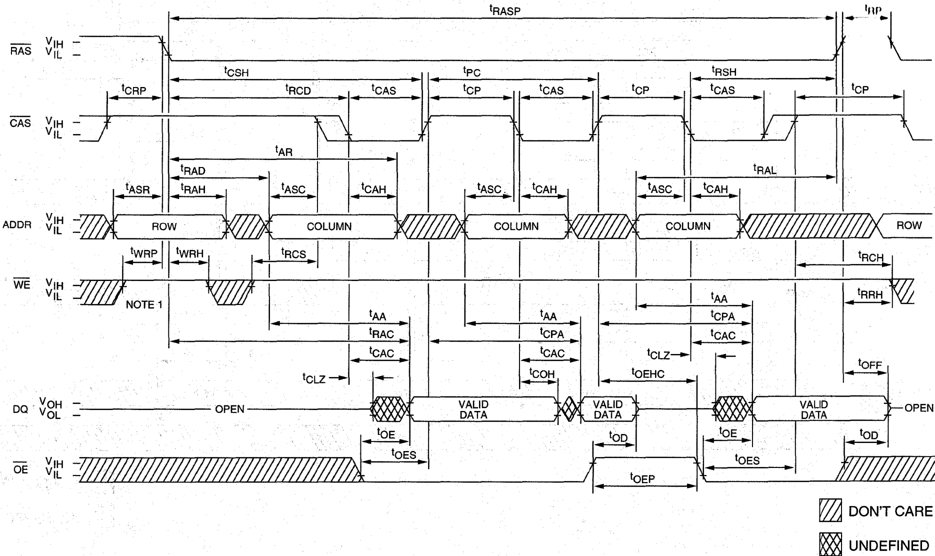
FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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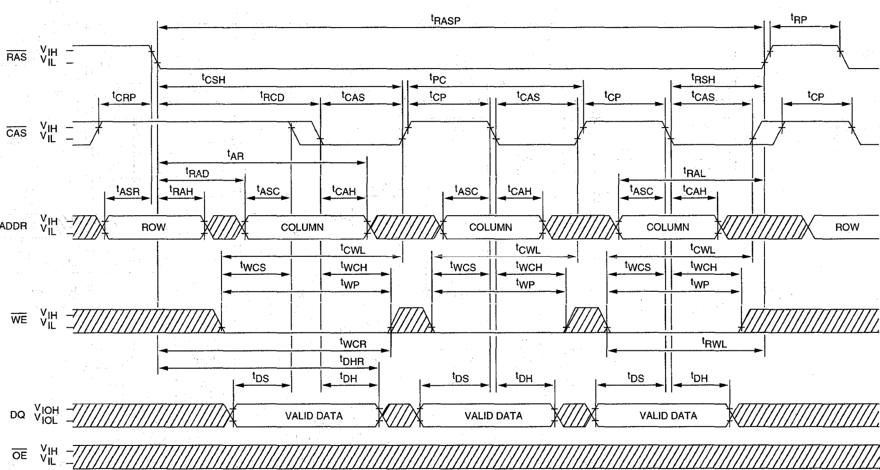
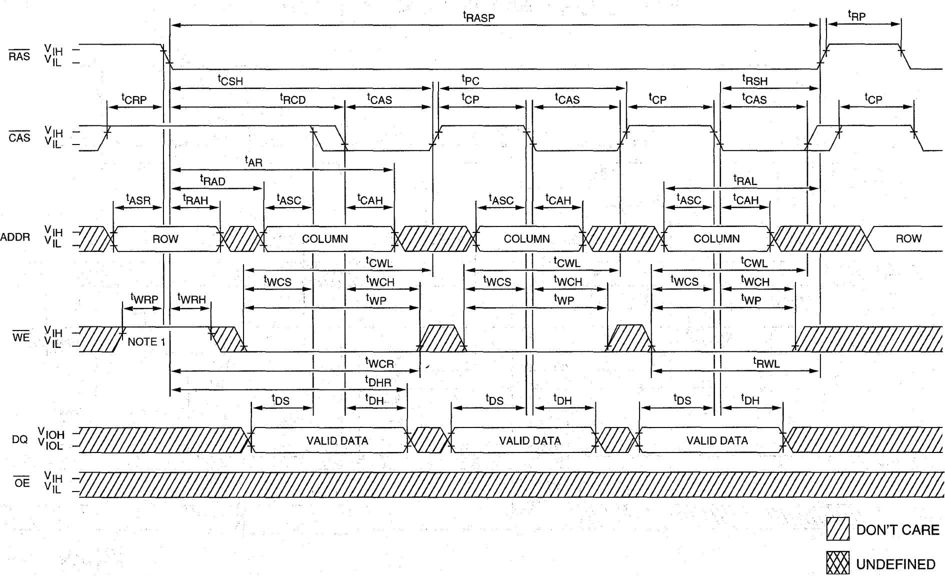
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

DRAM DIMM

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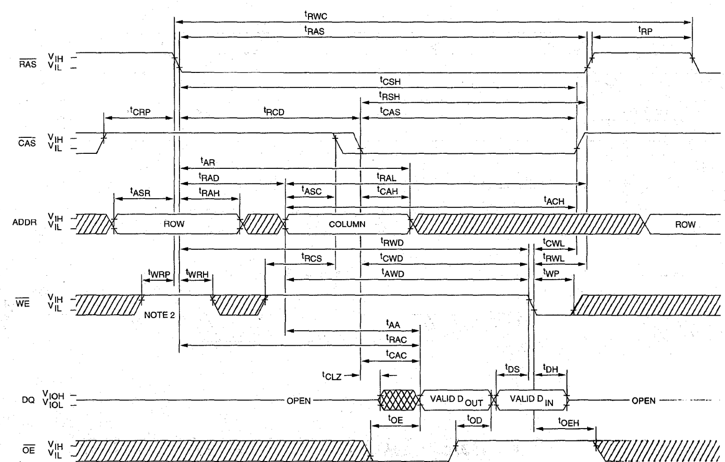
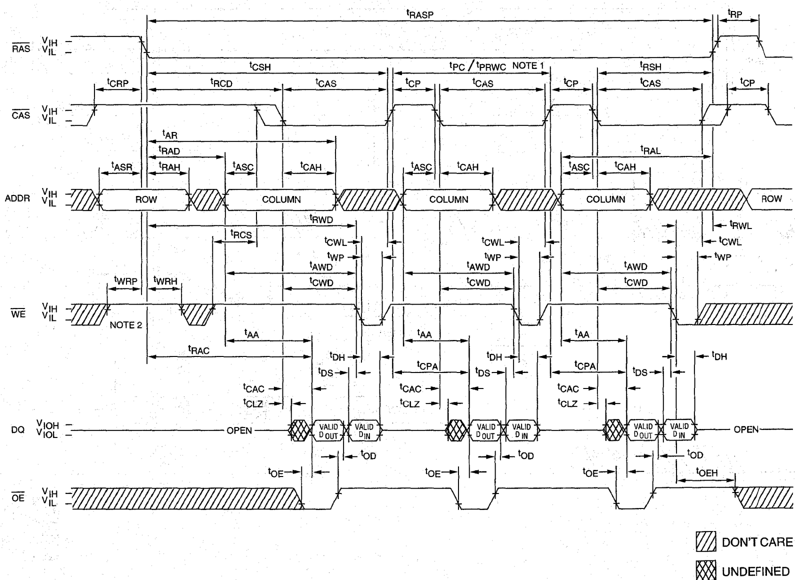
READ WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO/PAGE-MODE READ-WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)



DON'T CARE

UNDEFINED

NOTE:

1. ^tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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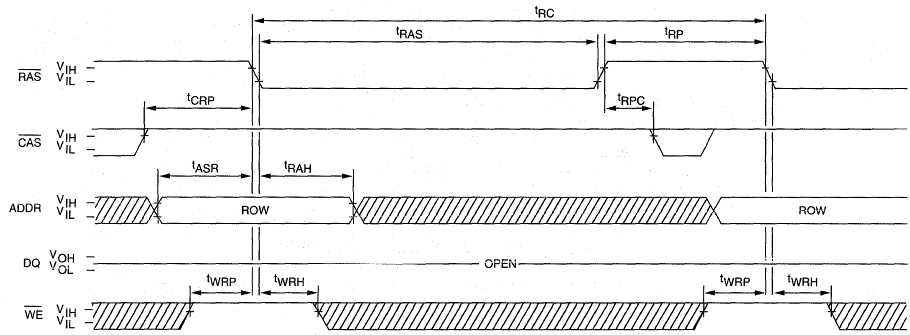
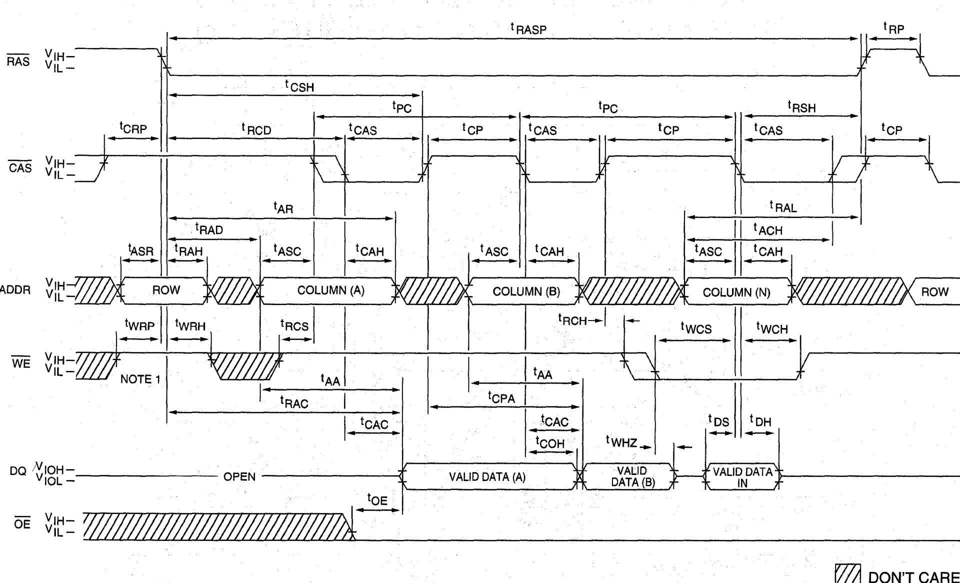
RAS-ONLY REFRESH CYCLE [39]
(WE = DON'T CARE)



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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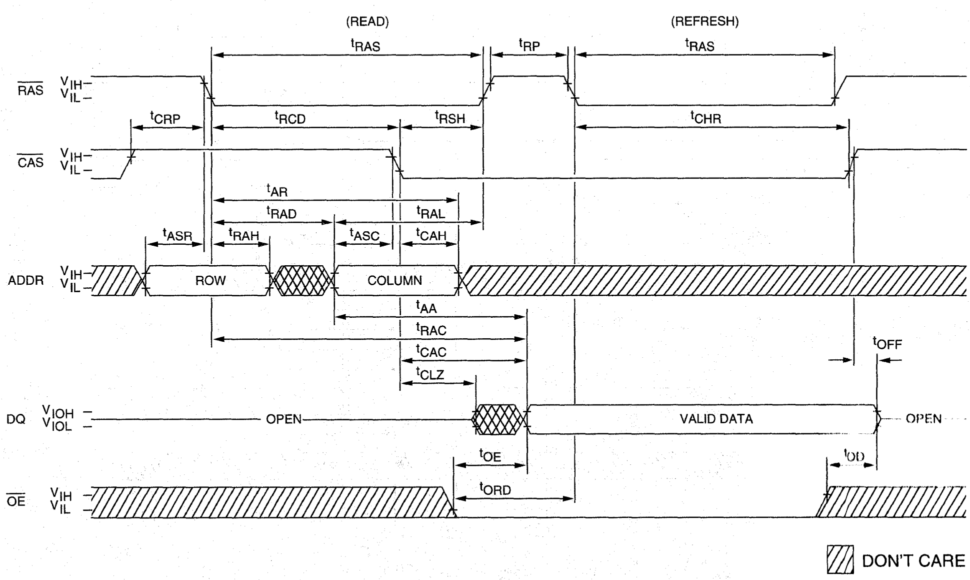
HIDDEN REFRESH CYCLE [21, 39]
(WE = HIGH; OE = LOW)



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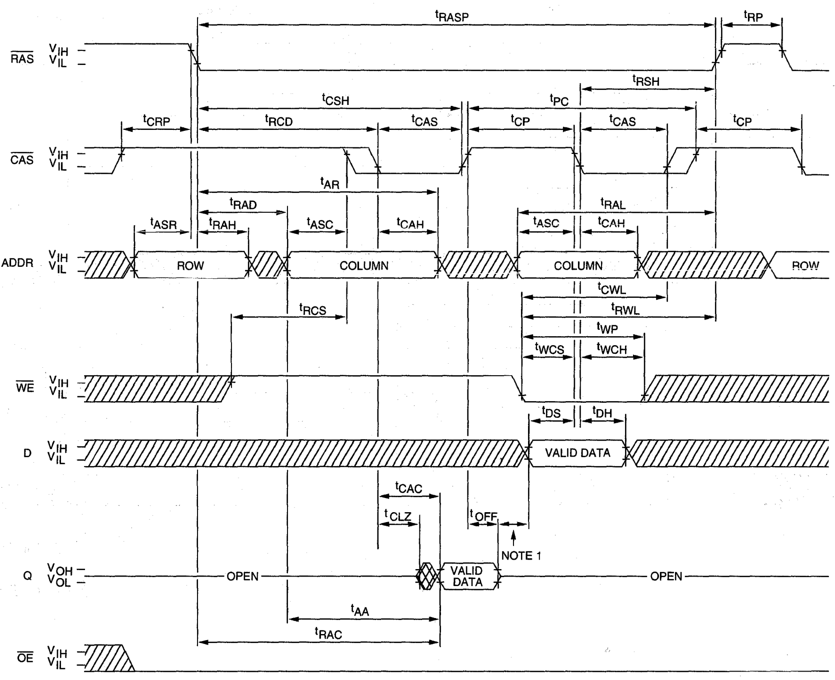
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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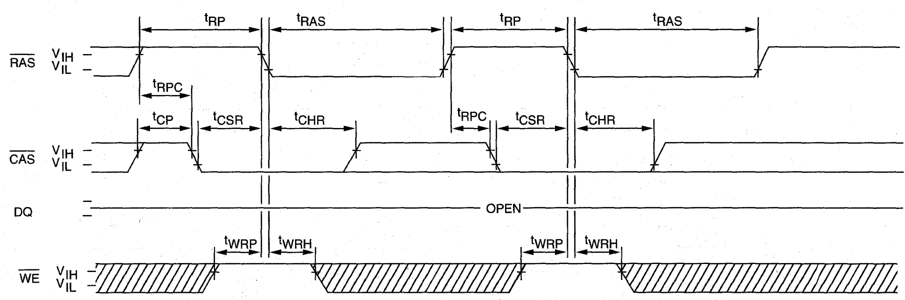
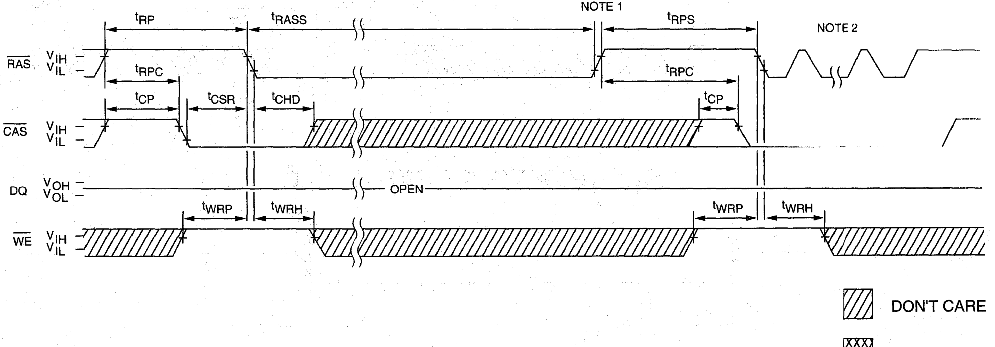
CBR REFRESH CYCLE [39]

(Addresses, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE [39]

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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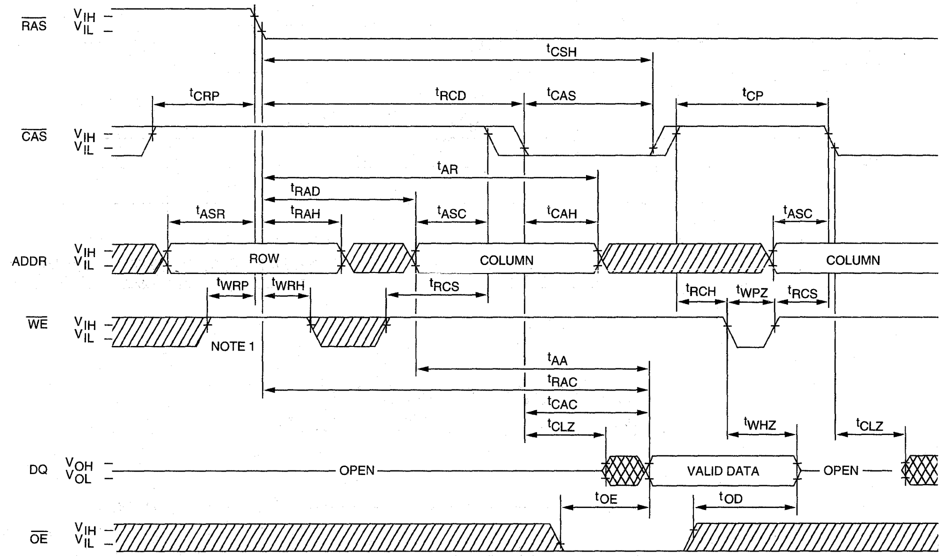
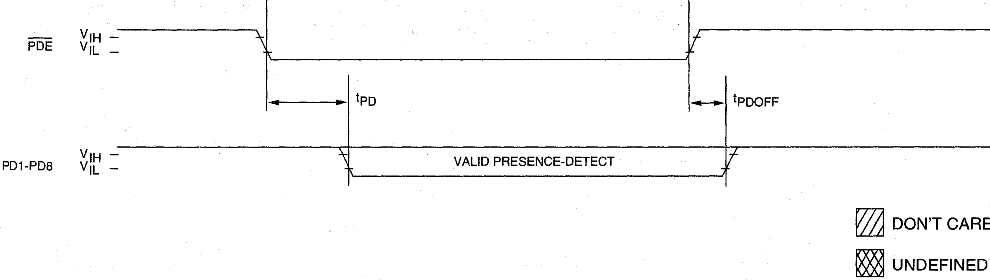
EDO READ CYCLE
(with WE-controlled disable)



PRESENCE-DETECT READ CYCLE [39]



DON'T CARE
UNDEFINED

NOTE:
1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. PD pins must be pulled HIGH at next level.

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DRAM MODULE

2 MEG x 64

16 MEGABYTE, 3.3V, FAST PAGE OR EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- JEDEC- and industry-standard pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 8mW standby; 1,600mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; Extended and SELF REFRESH
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

EDO option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	35ns	20ns	10ns
-7	130ns	70ns	30ns	40ns	25ns	12ns

FPM option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-11) SOJ Version
(DE-12) TSOP Version

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	$\overline{CAS5}$
5	DQ3	47	$\overline{CAS6}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ25	111	RFU	153	DQ57
28	$\overline{CAS0}$	70	DQ26	112	$\overline{CAS1}$	154	DQ58
29	$\overline{CAS2}$	71	DQ27	113	$\overline{CAS3}$	155	DQ59
30	$\overline{RAS0}$	72	DQ28	11	NC	156	DQ60
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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MT8LD(T)264(X)(S) 2 MEG x 64 DRAM MODULE

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8LDT264G-xx	2 Meg x 64, FPM, TSOP
MT8LDT264G-xx S	2 Meg x 64, FPM, S*, TSOP
MT8LDT264G-xx X	2 Meg x 64, EDO, TSOP
MT8LDT264G-xx XS	2 Meg x 64, EDO, S*, TSOP
MT8LD264G-xx	2 Meg x 64, FPM, SOJ
MT8LD264G-xx S	2 Meg x 64, FPM, S*, SOJ
MT8LD264G-xx X	2 Meg x 64, EDO, SOJ
MT8LD264G-xx XS	2 Meg x 64, EDO, S*, SOJ

*S = SELF REFRESH

GENERAL DESCRIPTION

The MT8LD(T)264(X)(S) is a randomly accessed solid-state memory containing 2,097,152 words organized in a x64 configuration. It is specially processed to operate from 3.0V to 3.6V for low voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 21 address bits. The address is entered first by RAS latching 11 bits and then CAS latching 10 bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z.

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS HIGH time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last (reference the MT4LC2M8E7(S) DRAM data sheet for additional information on EDO functionality).

REFRESH

Returning RAS and CAS HIGH terminates a memory cycle, and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms (128ms "S" version), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specifications. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

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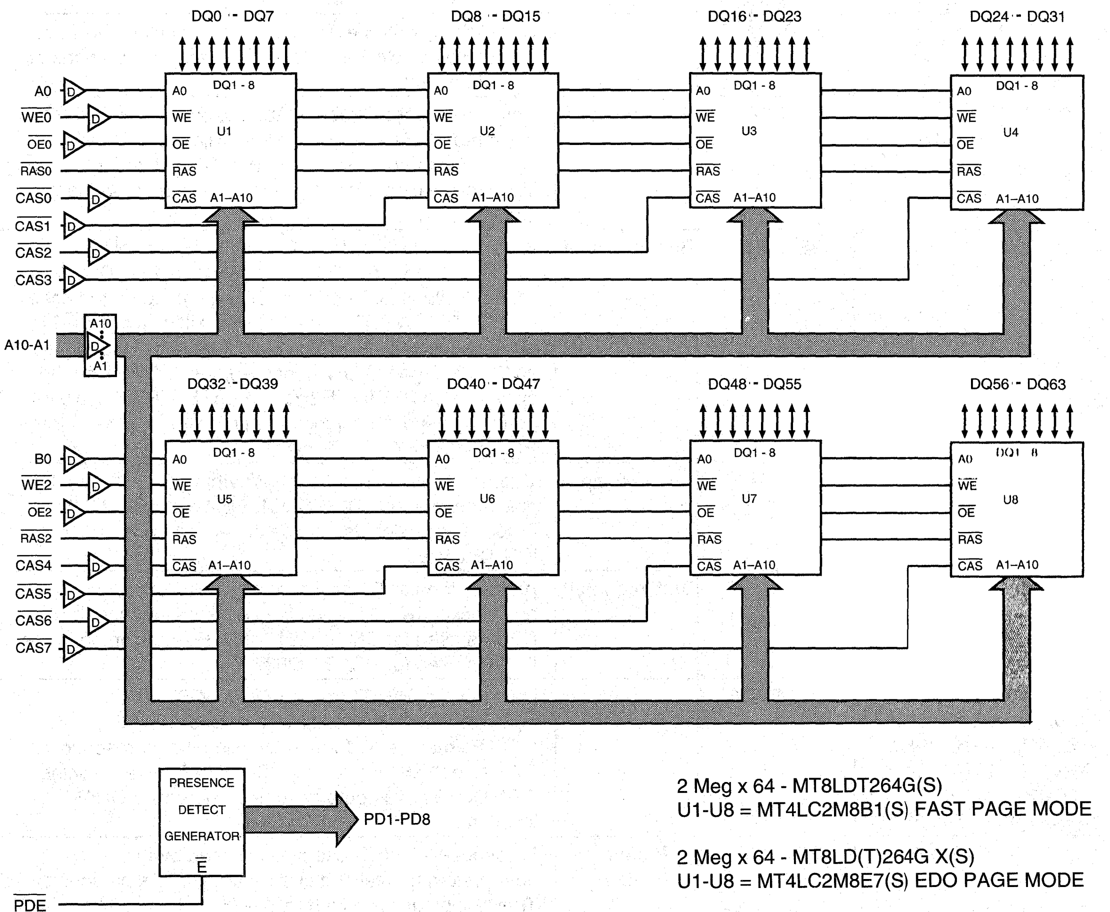
FUNCTIONAL BLOCK DIAGRAM



NEW DRAM DIMM

NOTE: 1. All inputs with the exception of RAS are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits. Two $\overline{RAS}$ inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{CAS0-7}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ31. $\overline{WE2}$ controls DQ32-DQ63. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ31. $\overline{OE2}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149,151,153-156,158-160	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ± 0.3V
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152,162	V_{SS}	Supply	Ground

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
11, 22, 24-25, 38-39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150,161	NC	—	No connect.

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES ${}^tR$	ADDRESSES ${}^tC$	DATA-IN/OUT DQ0-63
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$ - $\overline{CAS7}$ A0-A10, B0 $\overline{WE0,2}$, $\overline{OE0,2}$	II1	-2	2	µA	
	$\overline{RAS0,2}$	II2	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ0 - DQ63	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB	16	16	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	16MB	4	4	mA	28
	I_{CC2} (S only)	16MB	1.2	1.2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB	1,040	960	mA	3, 4, 28, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	16MB	720	640	mA	3, 4, 28, 32
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC5} (X only)	16MB	960	880	mA	3, 4, 28, 32
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC6}	16MB	1,040	960	mA	3, 32, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC7}	16MB	1,040	960	mA	3, 5, 28
REFRESH CURRENT: Extended CBR (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs (2,048 rows at 62.5µs = 128ms)	I_{CC8} (S only)	16MB	2.4	2.4	mA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC9} (S only)	16MB	2.4	2.4	mA	5, 28

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		40	pF	2
Input Capacitance: $\overline{CAS0}$ - $\overline{CAS7}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0 - DQ63	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		10	pF	2

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to $\overline{WE}$ delay time	^tAWD	57		62		ns	23, 30
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		20		ns	25
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	13		13		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		ns	23, 33
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	25
$\overline{CAS}$ hold time	^tCSH	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	7		7		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	42		47		ns	23, 30
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	15		20		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD	3	15	3	20	ns	33
Output enable	^tOE		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	13		13		ns	24

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^{t}OFF	5	20	5	25	ns	20, 27, 36
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
$\overline{PDE}$ to valid presence-detect data	^{t}PD		10		10	ns	35
$\overline{PDE}$ inactive to presence-detects inactive	^{t}PDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	87		97		ns	23
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	13	25	13	30	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	^{t}RAL	35		40		ns	25
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	^{t}RASS	100		100		µs	31
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	2		2		ns	19, 23
Read command setup time	^{t}RCS	2		2		ns	23
Refresh period (2,048 cycles) - 2 Meg x 64	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) - 2 Meg x 64 S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^{t}RPS	110		130		ns	31
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	20		25		ns	25
READ WRITE cycle time	^{t}RWC	155		185		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	87		97		ns	23, 30
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		25		ns	25
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	15		20		ns	25
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	43		53		ns	24
$\overline{WE}$ command setup time	^{t}WCS	2		2		ns	23, 30
Write command pulse width	^{t}WP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 23

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		35		40	ns	25
Column-address setup to CAS precharge during writes	tACH	15		15		ns	
Column-address hold time (referenced to RAS)	tAR	43		53		ns	24
Column-address setup time	tASC	2		2		ns	23
Row-address setup time	tASR	5		5		ns	25
Column-address to WE delay time	tAWD	57		67		ns	23, 30
Access time from CAS	tCAC		20		25	ns	15, 25
Column-address hold time	tCAH	15		17		ns	25
CAS pulse width	tCAS	10	10,000	12	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	tCHD	15		15		ns	31
CAS hold time (CBR REFRESH)	tCHR	8		10		ns	5, 24
CAS to output in Low-Z	tCLZ	2		2		ns	23
Data output hold after CAS LOW	tCOH	7		7		ns	23
CAS precharge time	tCP	10		10		ns	16
Access time from CAS precharge	tCPA		40		45	ns	25
CAS to RAS precharge time	tCRP	10		10		ns	25
CAS hold time	tCSH	48		53		ns	24
CAS setup time (CBR REFRESH)	tCSR	7		7		ns	5, 23
CAS to WE delay time	tCWD	37		42		ns	23, 30
Write command to CAS lead time	tCWL	15		15		ns	
Data-in hold time	tDH	15		17		ns	25, 29
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Data-in setup time	tDS	-2		-2		ns	24, 29
Output disable	tOD	0	15	0	15	ns	
Output enable	tOE		15		15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	10		10		ns	24
OE HIGH hold time from CAS HIGH	tOEHC	10		10		ns	
OE HIGH pulse width	tOEP	10		10		ns	
OE LOW to CAS HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	5	20	5	20	ns	20, 27, 36
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	20
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	
PDE to Valid Presence-Detect Data	tPD		10		10	ns	35
PDE Inactive to Presence-Detects Inactive	tPDOFF	2		2		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	77		87		ns	23
Access time from RAS	tRAC		60		70	ns	14
RAS to column-address delay time	tRAD	10	25	10	30	ns	18, 26
Row-address hold time	tRAH	8		8		ns	24
Column-address to RAS lead time	tRAL	35		40		ns	25
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
RAS pulse width during SELF REFRESH	tRASS	100		100		µs	31
Random READ or WRITE cycle time	tRC	110		130		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS to CAS delay time	tRCD	12	40	12	45	ns	17, 26
Read command hold time (referenced to CAS)	tRCH	2		2		ns	19, 23
Read command setup time	tRCS	2		2		ns	23
Refresh period (2,048 cycles) - 2 Meg x 64	tREF		32		32	ms	
Refresh period (2,048 cycles) - 2 Meg x 64 S version	tREF		128		128	ms	
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
RAS precharge time during SELF REFRESH	tRPS	110		130		ns	31
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	15		17		ns	25
READ WRITE cycle time	tRWC	155		182		ns	25
RAS to WE delay time	tRWD	82		92		ns	23, 30
Write command to RAS lead time	tRWL	20		20		ns	25
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	15		17		ns	25
Write command hold time (referenced to RAS)	tWCR	43		53		ns	24
WE command setup time	tWCS	2		2		ns	23, 30
Output disable delay from WE (CAS HIGH)	tWHZ	2	18	2	20	ns	27
Write command pulse width	tWP	10		12		ns	
WE pulse width for output disable when CAS HIGH	tWPZ	10		12		ns	
WE hold time (CBR REFRESH)	tWRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	tWRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns for FPM and 2.5ns for EDO.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than thespecified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by one-half when used in the x32 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode.) Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
32. Column-address changed once each cycle.
33. The 3ns minimum is a parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pullup resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. For FAST PAGE MODE option, ^{t}OFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
37. Applies to both EDO and FAST PAGE MODEs.

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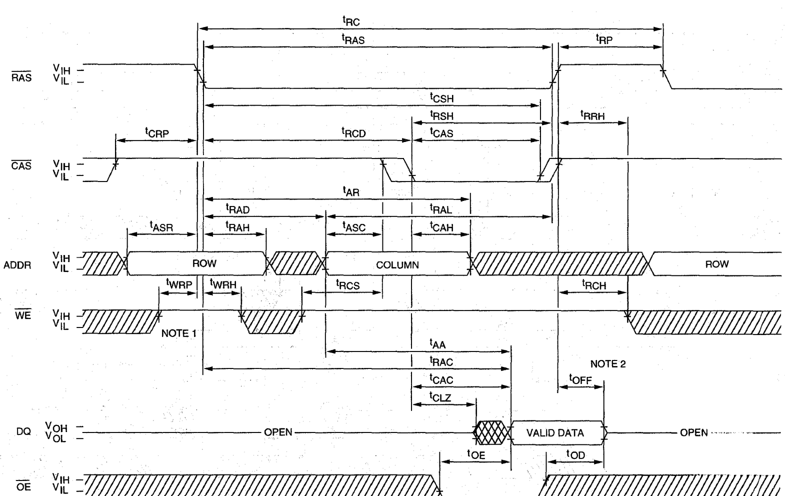
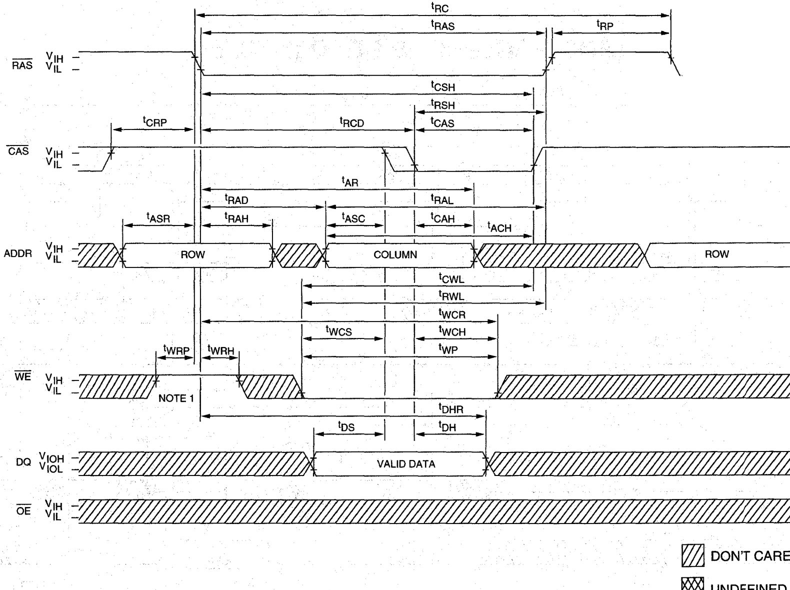
READ CYCLE [37]



EARLY WRITE CYCLE [37]



NOTE:

1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of RAS or CAS, which ever occurs last.

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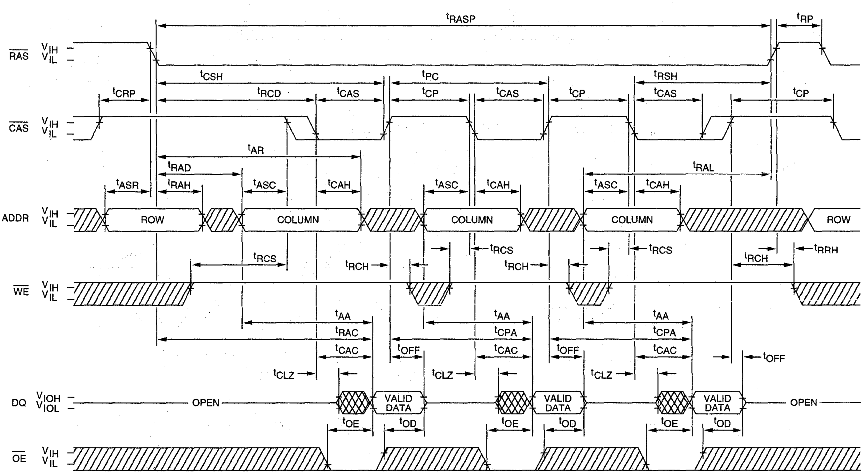
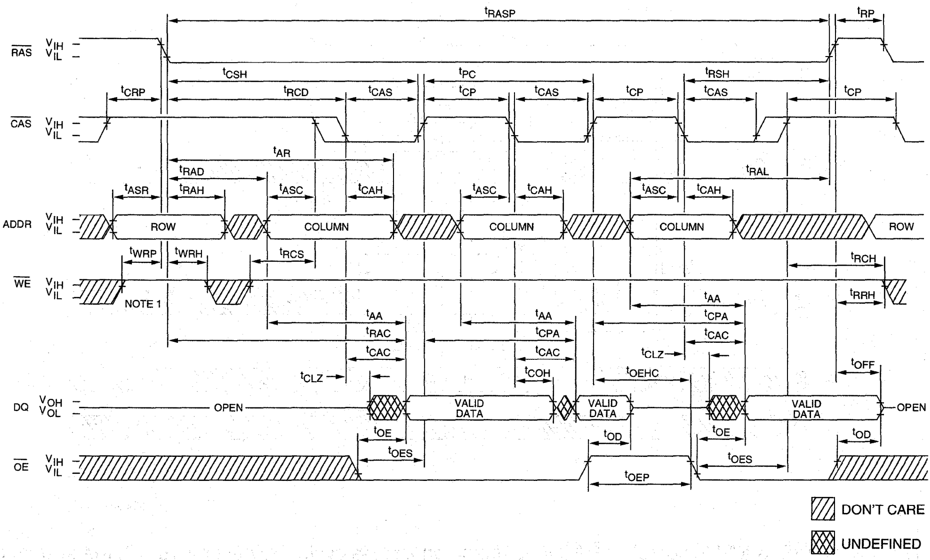
NEW DRAM DIMM

FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE READ CYCLE [37]



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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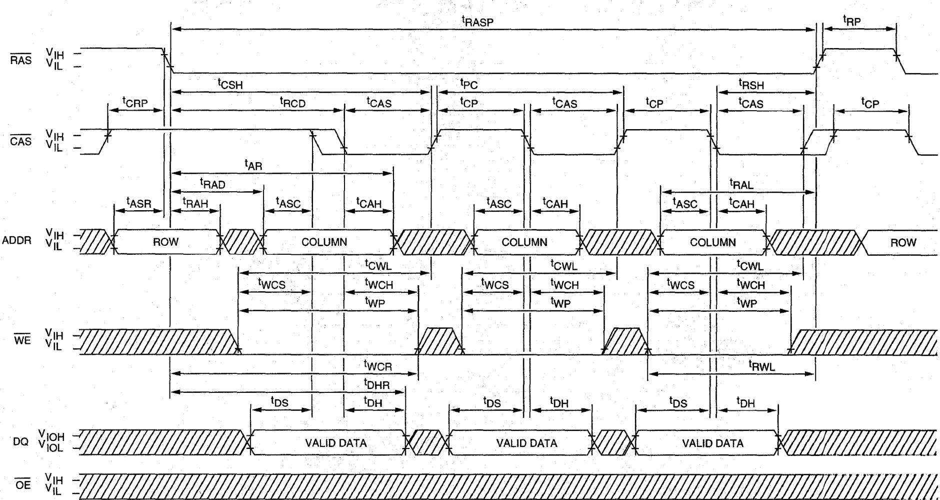
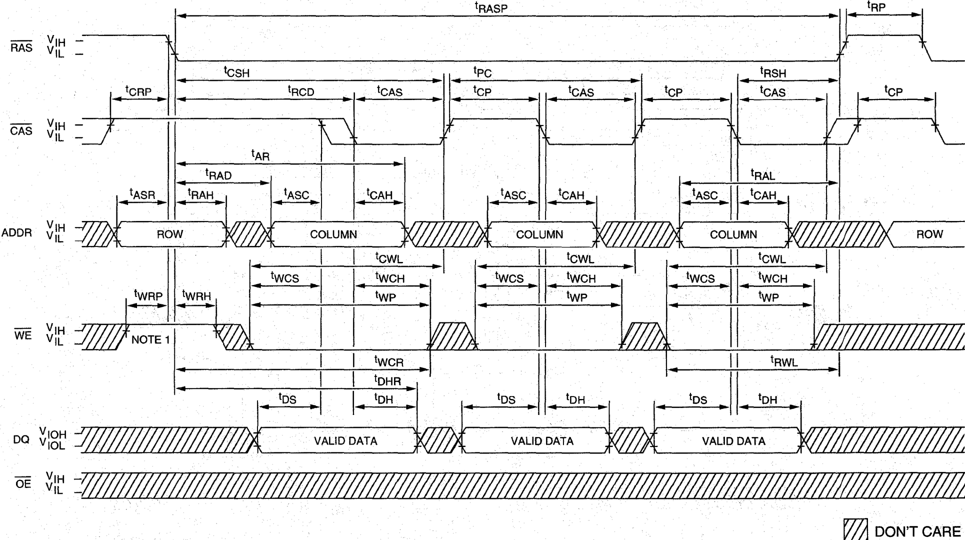
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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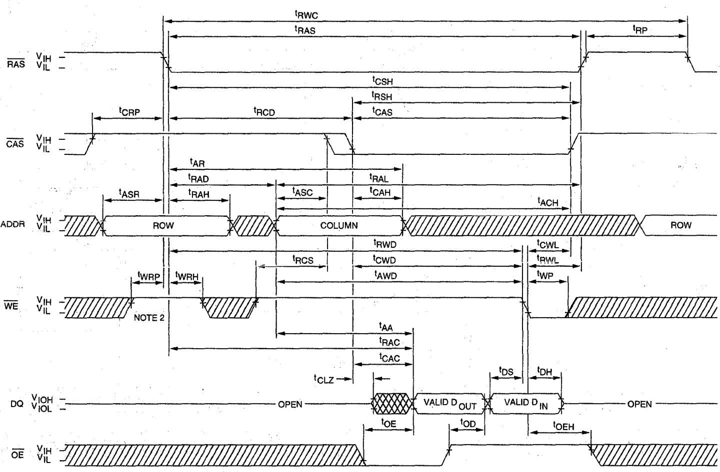
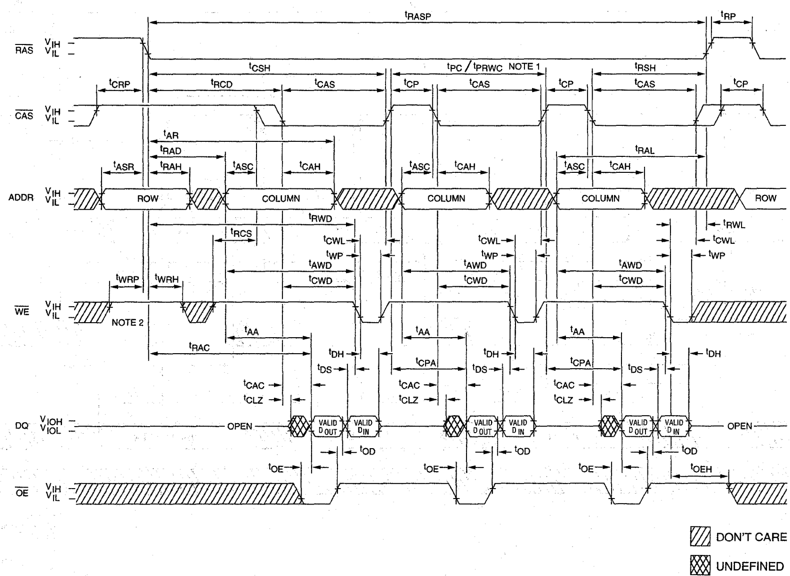
READ WRITE CYCLE [37]
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO/FAST-PAGE-MODE READ-WRITE CYCLE [37]
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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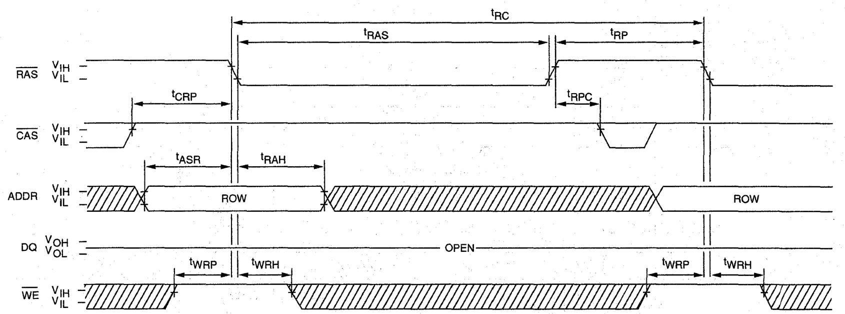
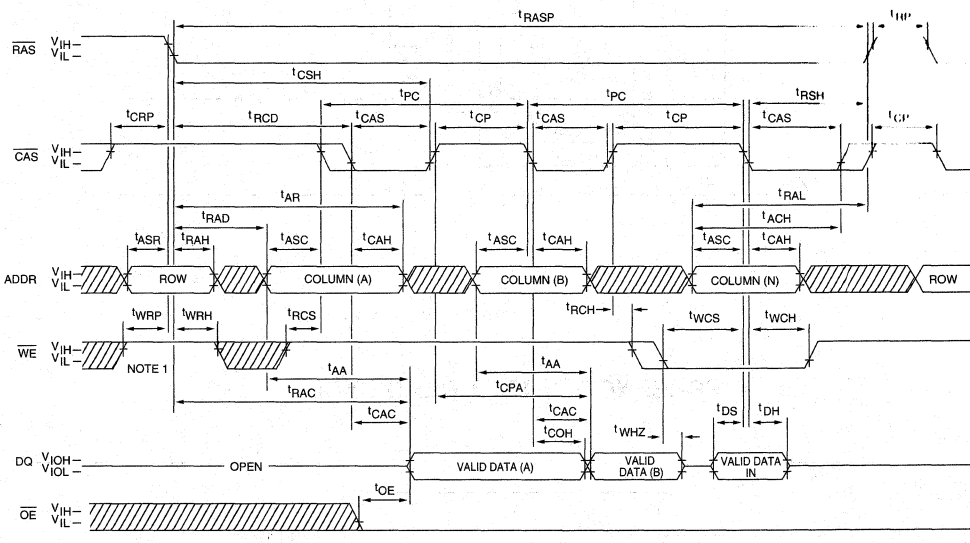
$\overline{RAS}$-ONLY REFRESH CYCLE [37]

(WE = DON'T CARE)



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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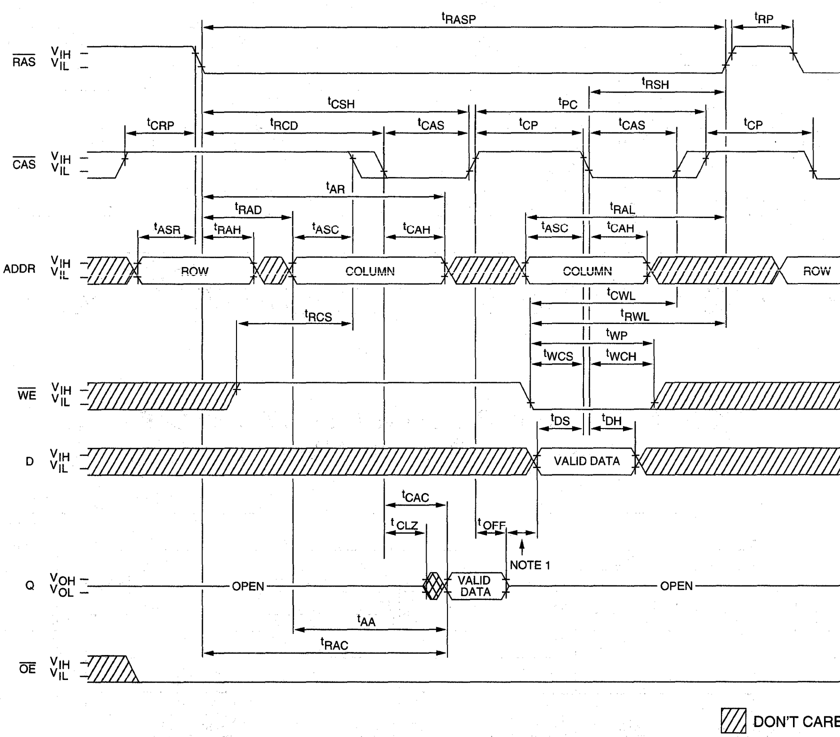
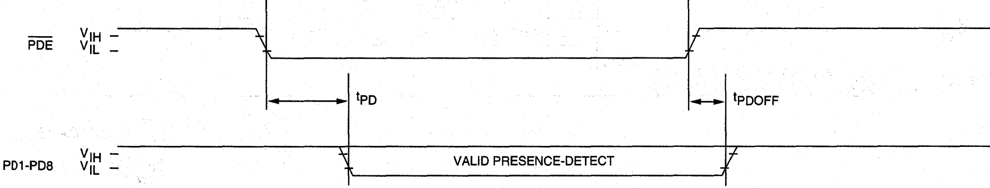
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



PRESENCE-DETECT READ CYCLE [37]



NOTE: 1. Do not drive data prior to tristate.
2. PD pins must be pulled HIGH at next level.

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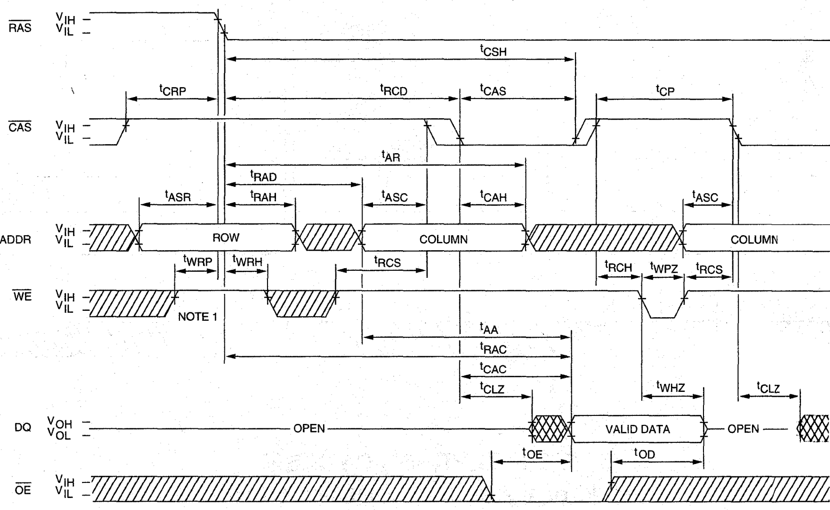
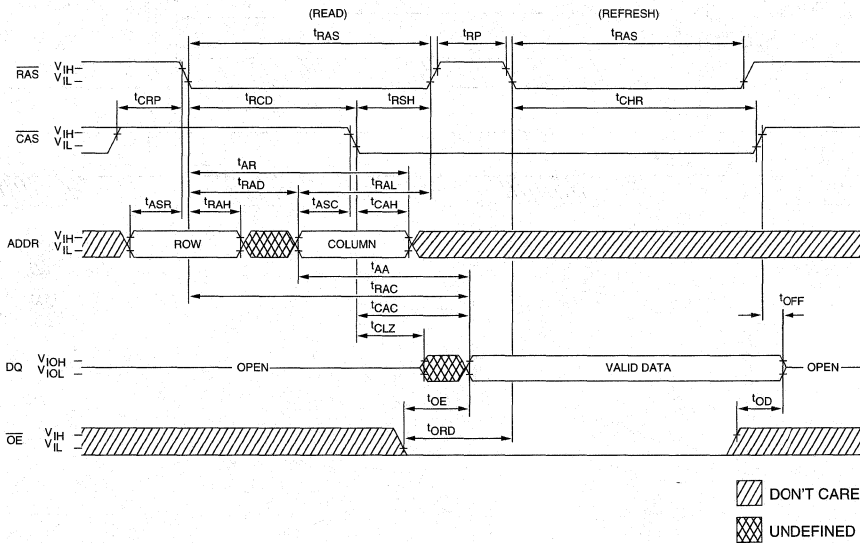
EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



HIDDEN REFRESH CYCLE [21, 37]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ${}^tWRP$ and ${}^tWRH$. This design implementation will facilitate compatibility with future EDO DRAMs.

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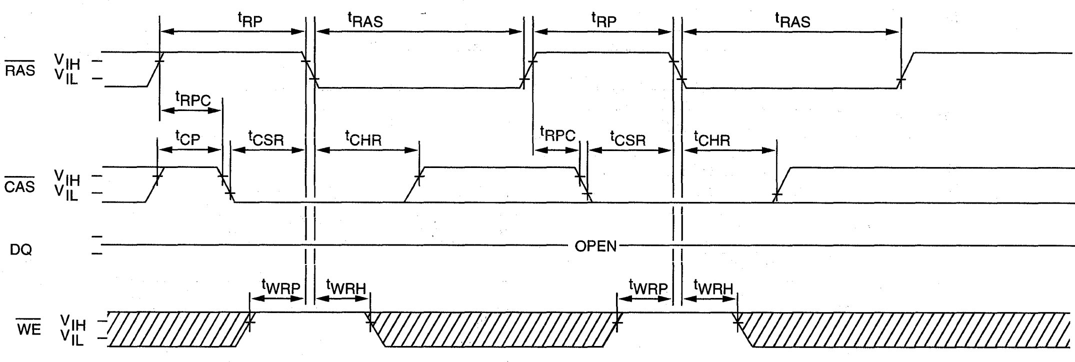
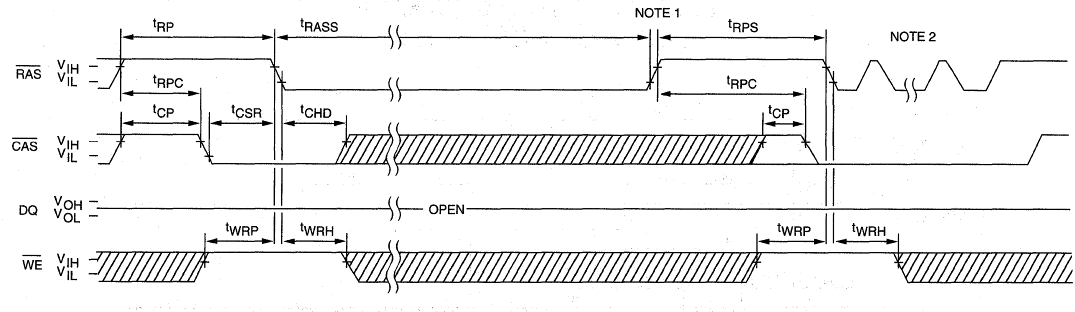
CBR REFRESH CYCLE [37]

(Addresses, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE [37]

(Addresses and $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE:
1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a compete burst of all rows should be executed.

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MT18D(T)172(S), MT18D(T)472
1 MEG, 4 MEG x 72 DRAM MODULES

DRAM MODULE

1 MEG, 4 MEG x 72

8, 32 MEGABYTE, ECC, 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

NEW DRAM DIMM

FEATURES

- JEDEC- and industry-standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are TTL-compatible
- Low power, 54mW standby; 4,050mW active, typical (8MB)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended and SELF REFRESH
- All inputs are buffered except $\overline{\text{RAS}}$
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms (1 Meg x 72)
- 2,048-cycle refresh distributed across 32ms (4 Meg x 72)
- FAST PAGE MODE (FPM) access cycle

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Refresh	
Standard Refresh/16ms or 32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT18DT172G-xx	1 Meg x 72 ECC, TSOP
MT18DT172G-xx S	1 Meg x 72 ECC, S**, TSOP
MT18D172G-xx	1 Meg x 72 ECC, SOJ
MT18D172G-xx S	1 Meg x 72 ECC, S**, SOJ
MT18DT472G-xx	4 Meg x 72 ECC, TSOP
MT18D472G-xx	4 Meg x 72 ECC, SOJ

**S = SELF REFRESH

PIN ASSIGNMENT (Front View)

168-Pin DIMM
(DE-13) SOJ version
(DE-14) TSOP version

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ38	130	NC
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	$\overline{\text{PDE}}$
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ28	111	RFU	153	DQ64
28	$\overline{\text{CAS0}}$	70	DQ29	112	NC	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	$\overline{\text{RAS0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC/A10*	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

*4 Meg x 72 version only

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GENERAL DESCRIPTION

The MT18D(T)172(S) and MT18D(T)472 are randomly accessed 8MB and 32MB solid-state memories organized in a x72 configuration.

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0 /B0-A10) at a time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. $\overline{RAS}$ is used to latch the first 10/11 bits and $\overline{CAS}$ the latter 10/11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Correct memory cell data is preserved by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0/B0-A9/A10) are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An additional SELF REFRESH mode is also available on the 1 Meg x 72. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for extended refresh rate of 125µs (8MB) per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within 300µs, prior to the resumption of normal operation.

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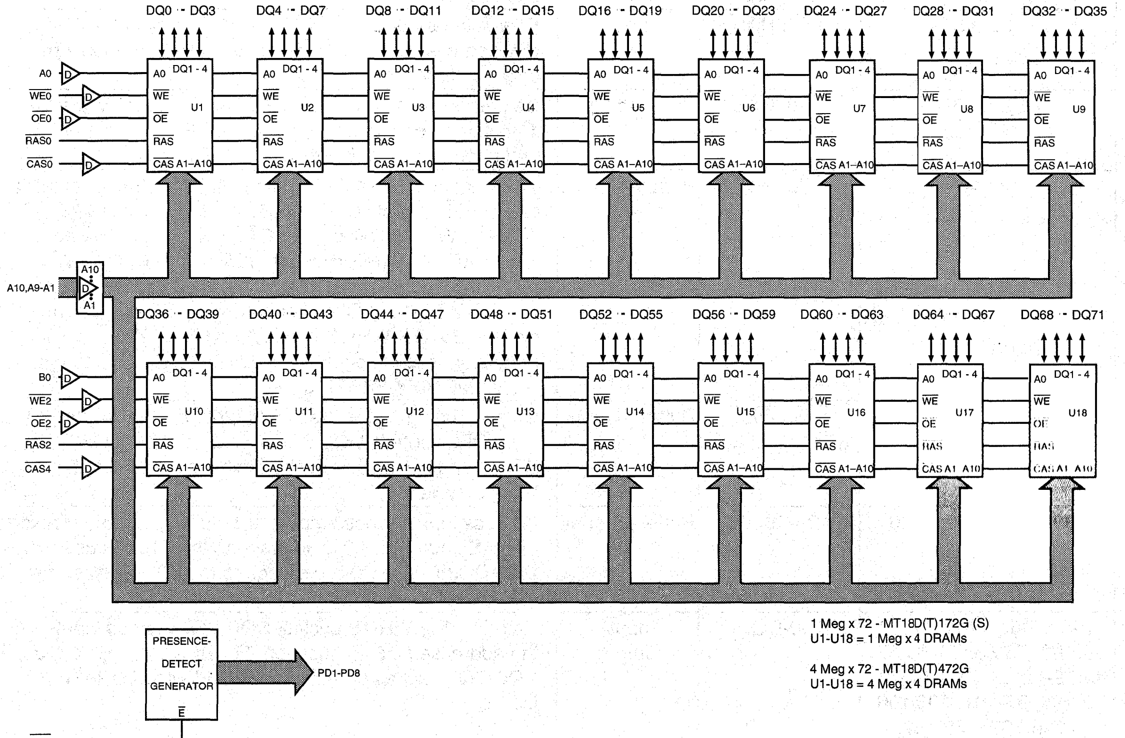
FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of $\overline{RAS}$ are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10/11 row-address bits. Two $\overline{RAS}$ inputs allow for one x72 bank or two x36 banks.
28, 46	$\overline{CAS0}$, $\overline{CAS4}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ35. $\overline{WE2}$ controls DQ36-DQ71. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ35. $\overline{OE2}$ controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133,143, 157, 168	Vcc	Supply	Power Supply: +5.0V ± 10%

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ0-71
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
• 8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT18D(T)472 uses 11/11 DRAMs.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$, $\overline{CAS4}$ A0-A10, B0, $\overline{PDE}$ $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0}$, $\overline{RAS2}$	I_{I2}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ71, PD1-PD8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB 32MB	36 56	36 56	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8MB 32MB	18 29	18 29	mA	28
	I_{CC2} (S only)	8MB 32MB	3.6 —	3.6 —	mA	28
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB	1,980	1,800	mA	3, 4, 28, 32
		32MB	2,160	1,980		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB	1,440	1,260	mA	3, 4, 28, 32
		32MB	1,620	1,440		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	8MB	1,980	1,800	mA	3, 28 32
		32MB	2,160	1,980		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	8MB	1,980	1,800	mA	3, 5, 28
		32MB	2,160	1,980		
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (8MB)	I_{CC7} (S only)	8MB	5.4	5.4	mA	3, 5, 28, 31
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	8MB	5.4	5.4	mA	5, 28

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0, PDE	C_{I1}		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2, CAS0, CAS4	C_{I2}		9	pF	2
Input Capacitance: RAS0, RAS2	C_{I3}		70	pF	2
Input/Output Capacitance: DQ0-DQ71	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address hold time (referenced to RAS)	^tAR	48		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to WE delay time	^tAWD	57		67		ns	23, 30
Access time from CAS	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		20		ns	25
CAS pulse width	^tCAS	15	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	^tCHD	10		10		ns	36
CAS hold time (CBR REFRESH)	^tCHR	8		8		ns	5, 24
CAS to output in Low-Z	^tCLZ	5		5		ns	23, 33
CAS precharge time	^tCP	10		10		ns	16
Access time from CAS precharge	^tCPA		40		45	ns	25
CAS to RAS precharge time	^tCRP	15		15		ns	25
CAS hold time	^tCSH	58		68		ns	24
CAS setup time (CBR REFRESH)	^tCSR	12		12		ns	5, 23
CAS to WE delay time	^tCWD	42		52		ns	23, 30
Write command to CAS lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	15		20		ns	25, 29
Data-in hold time (referenced to RAS)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD	3	15	3	20	ns	33
Output enable	^tOE		15		20	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^tOEH	13		18		ns	24
Output buffer turn-off delay	^tOFF	5	20	5	25	ns	20, 27

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
PDE to valid presence-detect data	tPD		10		10	ns	35
PDE inactive to presence-detects inactive	tPDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	87		97		ns	23
Access time from RAS	tRAC		60		70	ns	14
RAS to column-address delay time	tRAD	13	25	13	30	ns	18, 26
Row-address hold time	tRAH	8		8		ns	24
Column-address to RAS lead time	tRAL	35		40		ns	25
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH	tRASS	100		100		µs	36
Random READ or WRITE cycle time	tRC	110		130		ns	
RAS to CAS delay time	tRCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to CAS)	tRCH	2		2		ns	19, 23
Read command setup time	tRCS	2		2		ns	23
Refresh period (2,048 cycles) - 4 Meg x 72	tREF		32		32	ms	
Refresh period (1,024 cycles) - 1 Meg x 72	tREF		16		16	ms	
Refresh period (1,024 cycles) - 1 Meg x 72 S version	tREF		128		128	ms	
RAS precharge time	tRP	40		50		ns	
RAS to CAS precharge time	tRPC	0		0		ns	
RAS precharge time during SELF REFRESH	tRPS	110		130		ns	36
Read command hold time (referenced to RAS)	tRRH	0		0		ns	19
RAS hold time	tRSH	20		25		ns	25
READ WRITE cycle time	tRWC	155		185		ns	25
RAS to WE delay time	tRWD	87		97		ns	23, 30
Write command to RAS lead time	tRWL	20		25		ns	25
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	15		20		ns	25
Write command hold time (referenced to RAS)	tWCR	43		53		ns	24
WE command setup time	tWCS	2		2		ns	23, 30
Write command pulse width	tWP	10		15		ns	
WE hold time (CBR REFRESH)	tWRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	tWRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
32. Column-address changed once each cycle.
33. The 3ns minimum parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
37. ^{t}CAC (MIN), ^{t}CPA (MIN) and ^{t}AA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^{t}CAC (MAX), ^{t}CPA (MAX) and ^{t}AA (MAX) are guaranteed.

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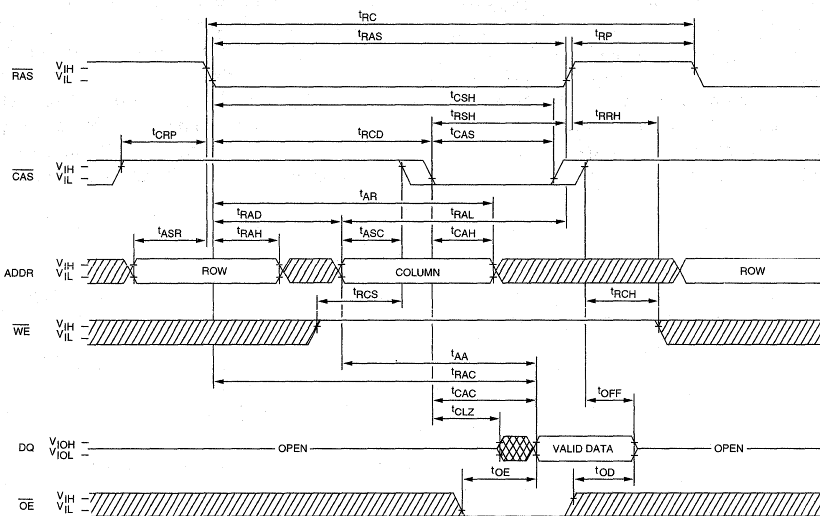
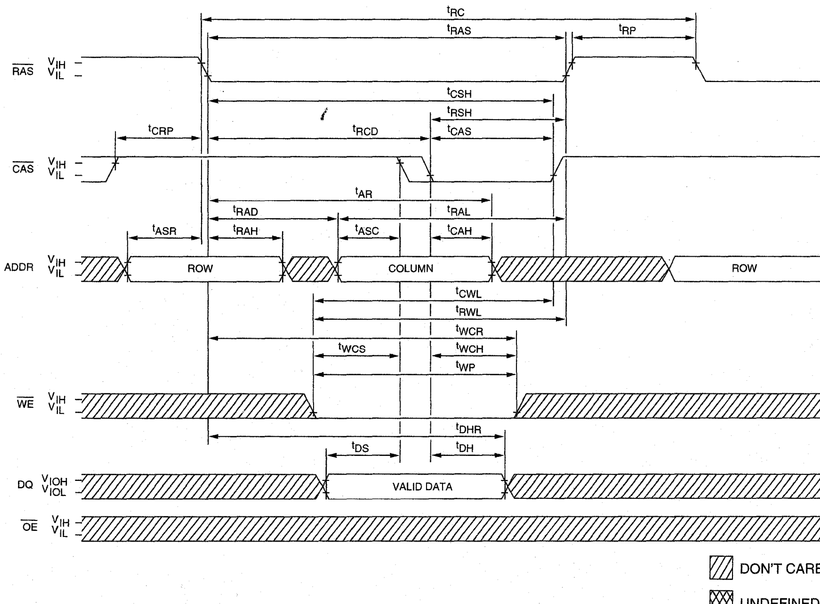
READ CYCLE



EARLY WRITE CYCLE



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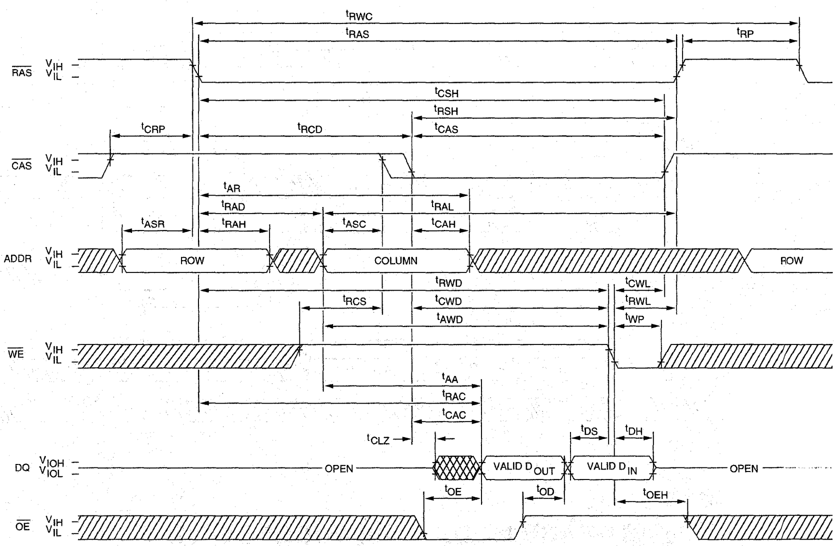
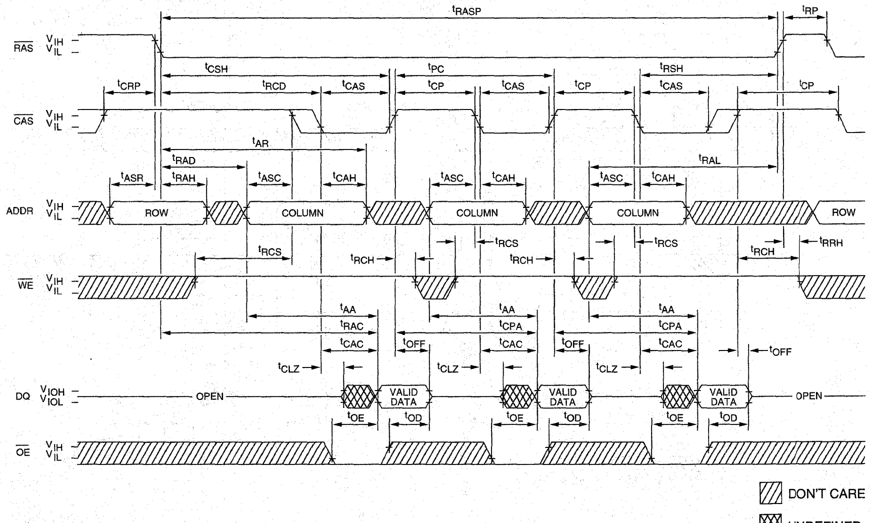
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST-PAGE-MODE READ CYCLE



DON'T CARE

UNDEFINED

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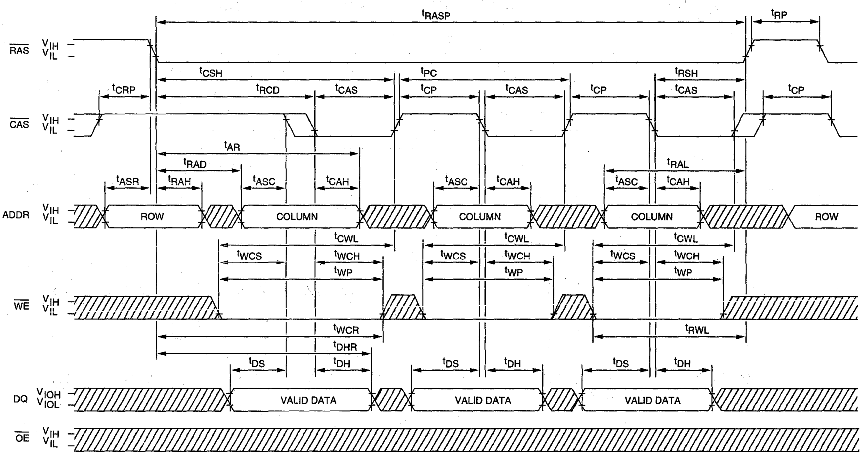
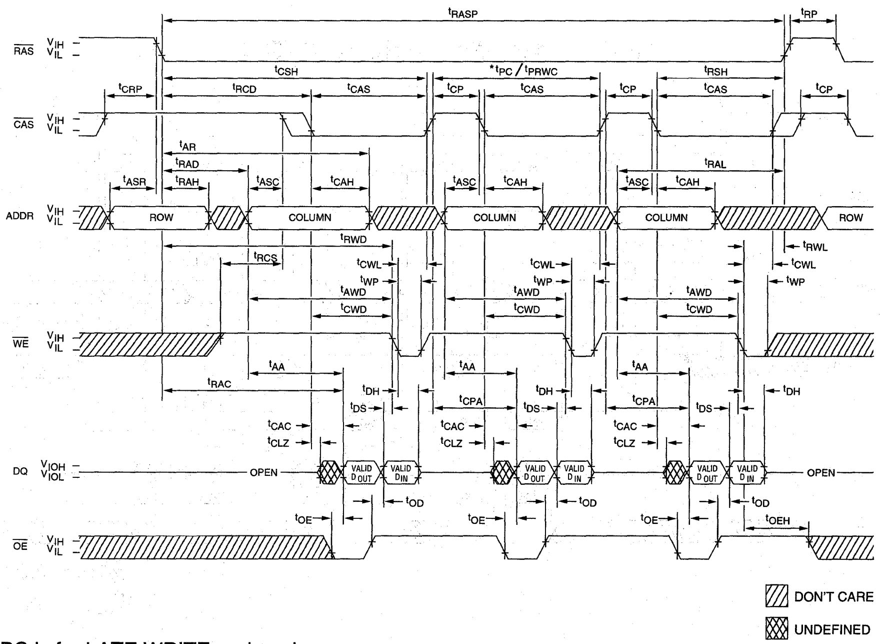
FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



***NOTE:** 1. tPC is for LATE WRITE cycle only.

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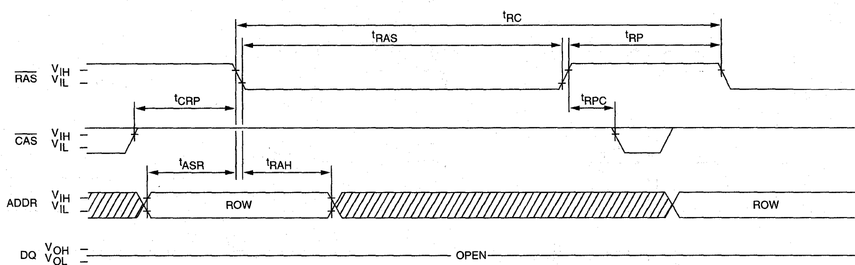
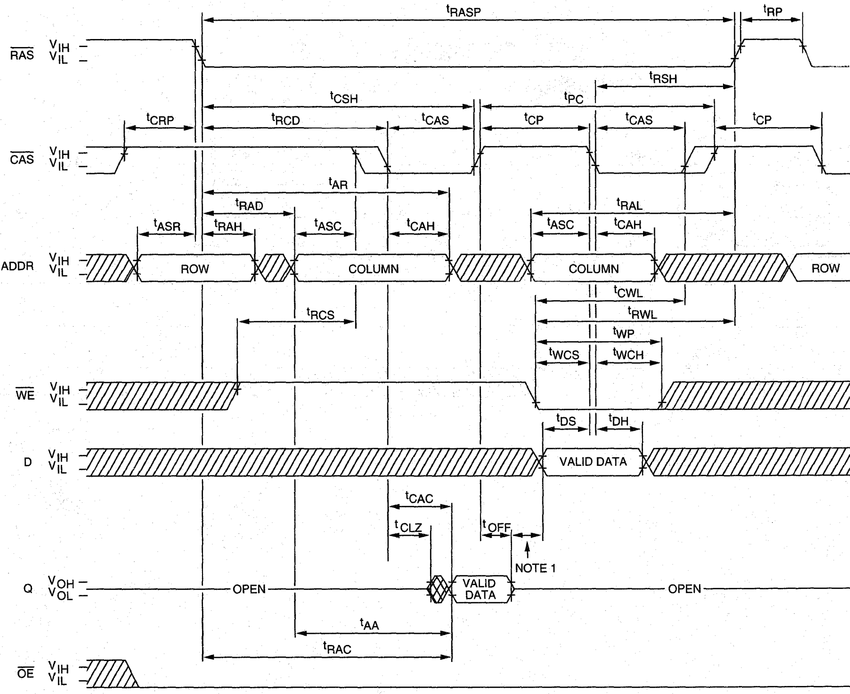
RAS ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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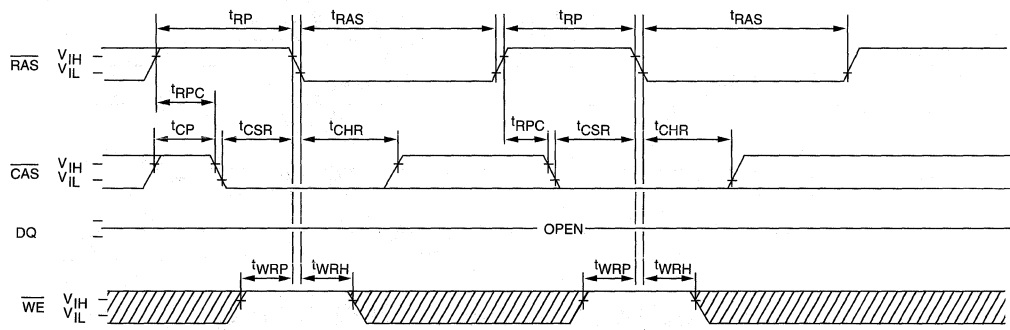
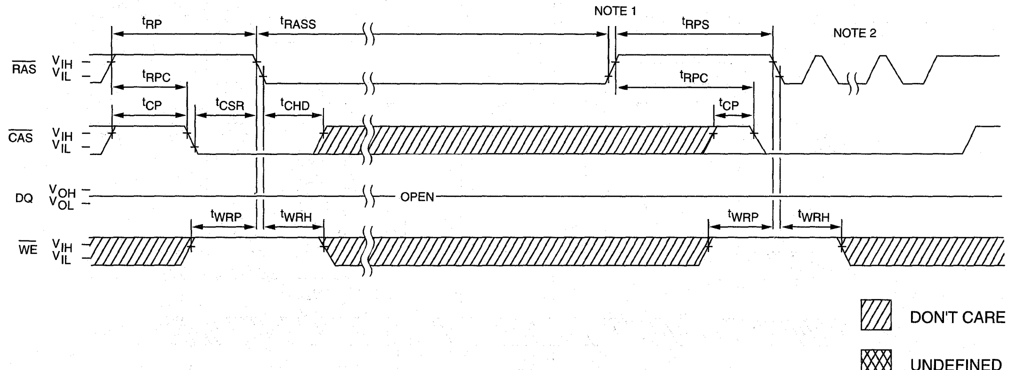
NEW DRAM DIMM

CBR REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE:
1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

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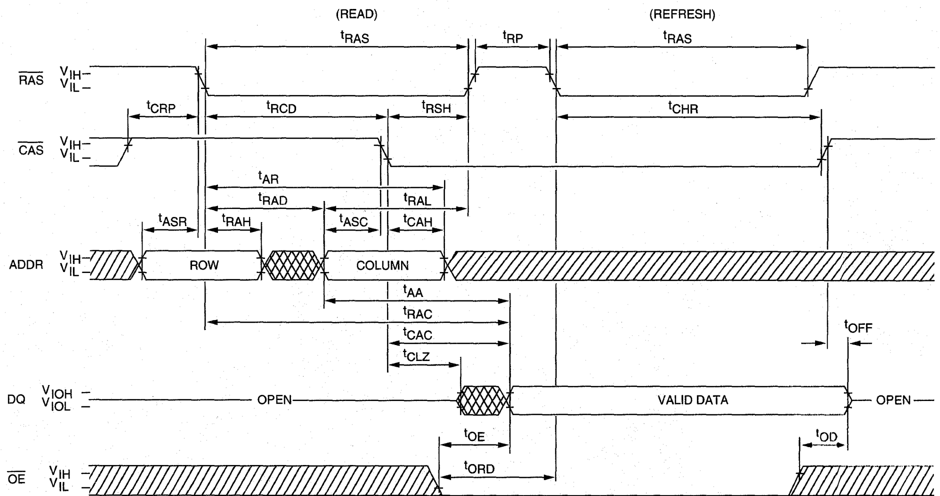
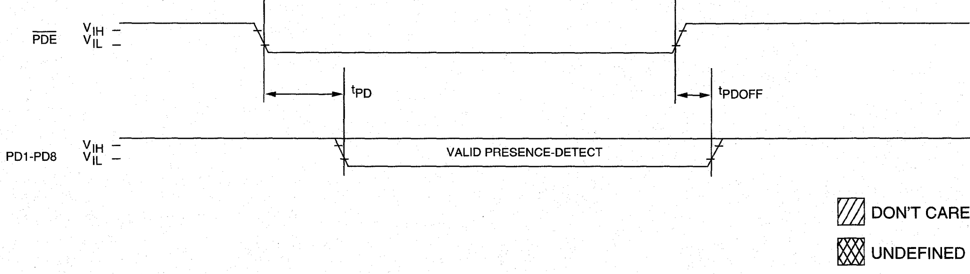
HIDDEN REFRESH CYCLE[21]

(WE = HIGH; OE = LOW)



PRESENCE-DETECT READ CYCLE



NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

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DRAM MODULE

1 MEG, 4 MEG x 72

8, 32 MEGABYTE, ECC, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 18mW standby; 3,240mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN; optional Extended and SELF REFRESH
- All inputs are buffered except $\overline{\text{RAS}}$
- 1,024-cycle refresh distributed across 16ms or 1,024-cycle Extended Refresh distributed across 128ms (1 Meg x 72)
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms (4 Meg x 72)
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE (4 Meg x 72 only)	X
• Refresh	
Standard/16ms or 32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

EDO option

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-6	110ns	60ns	25ns	35ns	20ns	10ns
-7	130ns	70ns	30ns	40ns	25ns	12ns

FPM option

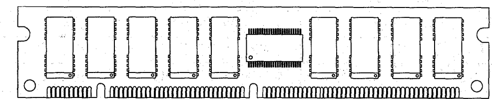
SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-15) SOJ version

(DE-16) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ38	130	NC
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ28	111	RFU	153	DQ64
28	$\overline{\text{CAS0}}$	70	DQ29	112	NC	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	$\overline{\text{RAS0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC/A10*	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

*4 Meg x 72 version only

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MT18LD(T)172(S), MT18LD(T)472(X)(S) 1 MEG, 4 MEG x 72 DRAM MODULES

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT18LD172G-xx	1 Meg x 72 ECC, FPM, SOJ
MT18LD172G-xx S	1 Meg x 72 ECC, FPM, SOJ, S*
MT18LDT172G-xx	1 Meg x 72 ECC, FPM, TSOP
MT18LDT172G-xx S	1 Meg x 72 ECC, FPM, TSOP, S*
MT18LDT472G-xx	4 Meg x 72 ECC, FPM, TSOP
MT18LDT472G-xx X	4 Meg x 72 ECC, EDO, TSOP
MT18LDT472G-xx S	4 Meg x 72 ECC, FPM, TSOP, S*
MT18LDT472G-xx XS	4 Meg x 72 ECC, EDO, TSOP, S*
MT18LD472G-xx	4 Meg x 72 ECC, FPM, SOJ
MT18LD472G-xx X	4 Meg x 72 ECC, EDO, SOJ
MT18LD472G-xx S	4 Meg x 72 ECC, FPM, SOJ, S*
MT18LD472G-xx XS	4 Meg x 72 ECC, EDO, SOJ, S*

*S = SELF REFRESH

GENERAL DESCRIPTION

The MT18LD(T)172(S) and MT18LD(T)472(X)(S) are randomly accessed 8MB and 32MB solid-state memories organized in a x72 configuration. They are specially processed to operate from 3.0V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0/B0-A10) at a time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. $\overline{RAS}$ is used to latch the first 10/11 bits and $\overline{CAS}$ the latter 10/11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE - 4 Meg x 72 only

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^{t}CP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z.

If the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last (reference the MT4LC4M4E8(S) DRAM data sheet for additional information on EDO functionality).

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REFRESH

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all combinations of RAS addresses (A0/B0-A9/A10) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for extended refresh rates of 62.5µs (32MB) and 125µs (8MB) per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 1,024/2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM

DQ0 - DQ3 | DQ4 - DQ7 | DQ8 - DQ11 | DQ12 - DQ15 | DQ16 - DQ19 | DQ20 - DQ23 | DQ24 - DQ27 | DQ28 - DQ31 | DQ32 - DQ35

A0, WE0, OE0, RAS0, CAS0 → U1–U9 (A0, DQ1 - 4, WE, OE, RAS, CAS A1–A10)

A10,A9-A1

DQ36 - DQ39 | DQ40 - DQ43 | DQ44 - DQ47 | DQ48 - DQ51 | DQ52 - DQ55 | DQ56 - DQ59 | DQ60 - DQ63 | DQ64 - DQ67 | DQ68 - DQ71

B0, WE2, OE2, RAS2, CAS4 → U10–U18 (A0, DQ1 - 4, WE, OE, RAS, CAS A1–A10)

PRESENCE-DETECT GENERATOR (E) → PD1-PD8; PDE

1 Meg x 72 - MT18LD172G(S)
U1-U18 = MT4LC4001J(S) FAST PAGE MODE

4 Meg x 72 - MT18LD(T)472G(S)
U1-U18 = MT4LC4M4B1(S) FAST PAGE MODE

4 Meg x 72 - MT18LD(T)472GX(S)
U1-U18 = MT4LC4M4E8(S) EDO PAGE MODE

NOTE: 1. All inputs with the exception of RAS are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 10/11 row-address bits. Two $\overline{RAS}$ inputs allow for one x72 bank or two x36 banks.
28, 46	$\overline{CAS0}$, $\overline{CAS4}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ35. $\overline{WE2}$ controls DQ36-DQ71. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ35. $\overline{OE2}$ controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ± 0.3V

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{\text{PDE}}$	Input	Presence-Detect Enable: $\overline{\text{PDE}}$ is the READ control for the buffered presence-detect pins.
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{PDE}}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ0-71
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
MODE READ	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
EDO/FAST-PAGE-	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
MODE EARLY-WRITE	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
MODE READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{\text{RAS}}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	**Module Organization**	**Row/Column Addresses**	**ID0**	**ID1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
• 8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.
* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT18LD(T)472 uses 11/11 DRAMs.

DRAM DIMM

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$, $\overline{CAS4}$ A0-A10, B0, $\overline{PDE}$ $\overline{WE0,2}$, $\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0}$, $\overline{RAS2}$	I_{I2}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ71, PD1-PD8	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	8MB 32MB	18 32	18 32	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	ALL	9	9	mA	28
	I_{CC2} (S only)	8MB 32MB	1.8 2.7	1.8 2.7		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB	1,440	1,260	mA	3, 4, 28, 32
		32MB	2,160	1,980		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB	1,080	900	mA	3, 4, 28, 32
		32MB	1,620	1,440		
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4} (X only)	8MB	—	—	mA	3, 4, 28, 32
		32MB	1,980	1,800		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	8MB	1,440	1,260	mA	3, 28 32
		32MB	2,160	1,980		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	8MB	1,440	1,260	mA	3, 5, 28
		32MB	2,160	1,980		
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 62.5µs (32MB)/125µs (8MB)	I_{CC7} (S only)	8MB	2.7	2.7	mA	3, 5, 28, 31
		32MB	5.4	5.4		
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2V; A0/B0-A10, $\overline{OE}$ and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	8MB	2.7	2.7	mA	5, 28
		32MB	5.4	5.4		

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0, PDE	CI1		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2, CAS0, CAS4	CI2		9	pF	2
Input Capacitance: RAS0, RAS2	CI3		70	pF	2
Input/Output Capacitance: DQ0-DQ71	CIO		10	pF	2
Output Capacitance: PD1-PD8	CO		9	pF	2

DRAM DIMM

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	${}^tAA$		35		40	ns	25
Column-address hold time (referenced to RAS)	${}^tAR$	48		53		ns	24
Column-address setup time	${}^tASC$	2		2		ns	23
Row-address setup time	${}^tASR$	5		5		ns	25
Column-address to WE delay time	${}^tAWD$	57		67		ns	23, 30
Access time from CAS	${}^tCAC$		20		25	ns	15, 25
Column-address hold time	${}^tCAH$	15		20		ns	25
CAS pulse width	${}^tCAS$	15	10,000	20	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	${}^tCHD$	15		15		ns	36
CAS hold time (CBR REFRESH)	${}^tCHR$	8		8		ns	5, 24
CAS to output in Low-Z	${}^tCLZ$	5		5		ns	23, 33
CAS precharge time	${}^tCP$	10		10		ns	16
Access time from CAS precharge	${}^tCPA$		40		45	ns	25
CAS to RAS precharge time	${}^tCRP$	15		15		ns	25
CAS hold time	${}^tCSH$	58		68		ns	24
CAS setup time (CBR REFRESH)	${}^tCSR$	12		12		ns	5, 23
CAS to WE delay time	${}^tCWD$	42		47		ns	23, 30
Write command to CAS lead time	${}^tCWL$	15		20		ns	
Data-in hold time	${}^tDH$	15		20		ns	25, 29
Data-in hold time (referenced to RAS)	${}^tDHR$	45		55		ns	
Data-in setup time	${}^tDS$	-2		-2		ns	24, 29
Output disable	${}^tOD$		15		20	ns	
Output enable	${}^tOE$		15		20	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	${}^tOEH$	13		18		ns	24
Output buffer turn-off delay	${}^tOFF$	5	20	5	25	ns	20,27,38

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FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		ns	
$\overline{PDE}$ to valid presence-detect data	^tPD		10		10	ns	35
$\overline{PDE}$ inactive to presence-detects inactive	^tPDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	87		97		ns	23
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	13	25	13	30	ns	18, 26
Row-address hold time	^tRAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	^tRAL	35		40		ns	25
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	^tRASS	100		100		µs	36
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	2		2		ns	19, 23
Read command setup time	^tRCS	2		2		ns	23
Refresh period (2,048 cycles) - 4 Meg x 72	^tREF		32		32	ms	
Refresh period (1,024 cycles) - 1 Meg x 72	^tREF		16		16	ms	
Refresh period (1,024 or 2,048 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^tRPS	110		130		ns	36
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	20		25		ns	25
READ WRITE cycle time	^tRWC	155		185		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	87		97		ns	23, 30
Write command to $\overline{RAS}$ lead time	^tRWL	20		25		ns	25
Transition time (rise or fall)	^tT	3	50	3	50	ns	
Write command hold time	^tWCH	15		20		ns	25
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	43		53		ns	24
$\overline{WE}$ command setup time	^tWCS	2		2		ns	23, 30
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	12		12		ns	22, 23

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		35		40	ns	25
Column-address setup to CAS precharge during writes	^{t}ACH	15		15		ns	
Column-address hold time (referenced to RAS)	^{t}AR	43		53		ns	24
Column-address setup time	^{t}ASC	2		2		ns	23
Row-address setup time	^{t}ASR	5		5		ns	25
Column-address to WE delay time	^{t}AWD	57		67		ns	23, 30
Access time from CAS	^{t}CAC		20		25	ns	15, 25
Column-address hold time	^{t}CAH	15		17		ns	25
CAS pulse width	^{t}CAS	10	10,000	12	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	^{t}CHD	15		15		ns	36
CAS hold time (CBR REFRESH)	^{t}CHR	8		10		ns	5, 24
CAS to output in Low-Z	^{t}CLZ	2		2		ns	23
Data output hold after CAS LOW	^{t}COH	7		7		ns	23
CAS precharge time	^{t}CP	10		10		ns	16
Access time from CAS precharge	^{t}CPA		40		45	ns	25, 37
CAS to RAS precharge time	^{t}CRP	10		10		ns	25
CAS hold time	^{t}CSH	48		53		ns	24
CAS setup time (CBR REFRESH)	^{t}CSR	7		7		ns	5, 23
CAS to WE delay time	^{t}CWD	37		42		ns	23, 30
Write command to CAS lead time	^{t}CWL	15		15		ns	
Data-in hold time	^{t}DH	15		17		ns	25, 29
Data-in hold time (referenced to RAS)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	-2		-2		ns	24, 29
Output disable	^{t}OD	0	15	0	15	ns	
Output enable	^{t}OE		15		15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	^{t}OEH	8		10		ns	24
OE HIGH hold time from CAS HIGH	^{t}OEHC	10		10		ns	
OE HIGH pulse width	^{t}OEP	10		10		ns	
OE LOW to CAS HIGH setup time	^{t}OES	5		5		ns	
Output buffer turn-off delay	^{t}OFF	5	20	5	20	ns	20,27,38
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
EDO-PAGE-MODE READ or WRITE cycle time	^{t}PC	25		30		ns	
PDE to valid presence-detect data	^{t}PD		10		10	ns	35
PDE inactive to presence-detects inactive	^{t}PDOFF	2		2		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	77		87		ns	23
Access time from RAS	^{t}RAC		60		70	ns	14
RAS to column-address delay time	^{t}RAD	10	25	10	30	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to RAS lead time	^{t}RAL	35		40		ns	25
RAS pulse width	^{t}RAS	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	^{t}RASP	60	125,000	70	125,000	ns	
RAS pulse width during SELF REFRESH	^{t}RASS	100		100		µs	36
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
RAS to CAS delay time	^{t}RCD	12	40	12	45	ns	17, 26

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	2		2		ns	19, 23
Read command setup time	^tRCS	2		2		ns	23
Refresh period (2,048 cycles) - 4 Meg x 72	^tREF		32		32	ms	
Refresh period (2,048 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^tRPS	110		130		ns	36
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		17		ns	25
READ WRITE cycle time	^tRWC	155		182		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	82		92		ns	23, 30
Write command to $\overline{RAS}$ lead time	^tRWL	20		20		ns	25
Transition time (rise or fall)	^tT	2	50	2	50	ns	
Write command hold time	^tWCH	15		17		ns	25
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	43		53		ns	24
$\overline{WE}$ command setup time	^tWCS	2		2		ns	23
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	^tWHZ	2	18	2	20	ns	27
Write command pulse width	^tWP	10		12		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	^tWPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume tT = 5ns for FPM and 2.5ns for EDO.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for tCP.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, access time is controlled exclusively by tCAC.
18. Operation within the tRAD (MAX) limit ensures that tRAC (MIN) and tCAC (MIN) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. tWTS and tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of tWRP and tWRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
32. Column-address changed once each cycle.
33. The 3ns minimum parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
37. ^{t}CAC (MIN), ^{t}CPA (MIN) and ^{t}AA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^{t}CAC (MAX), ^{t}CPA (MAX) and ^{t}AA (MAX) are guaranteed.
38. For FAST PAGE MODE option, ^{t}OFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
39. Applies to both EDO and FAST PAGE MODEs.

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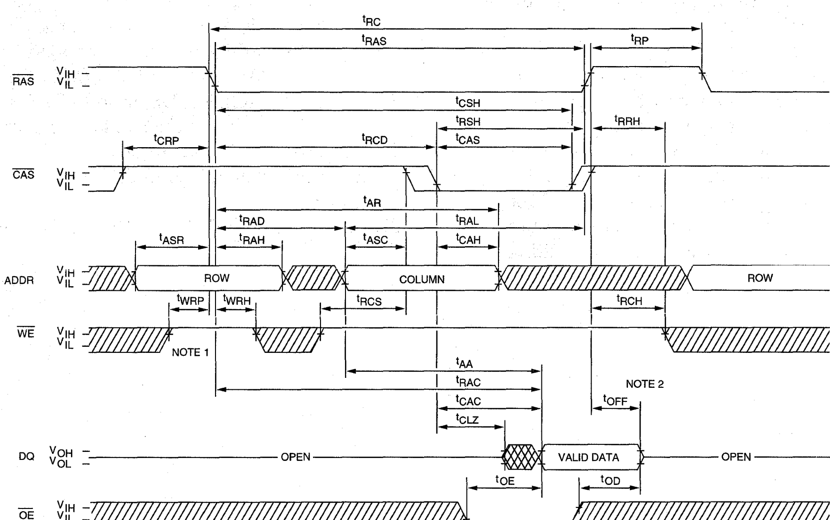
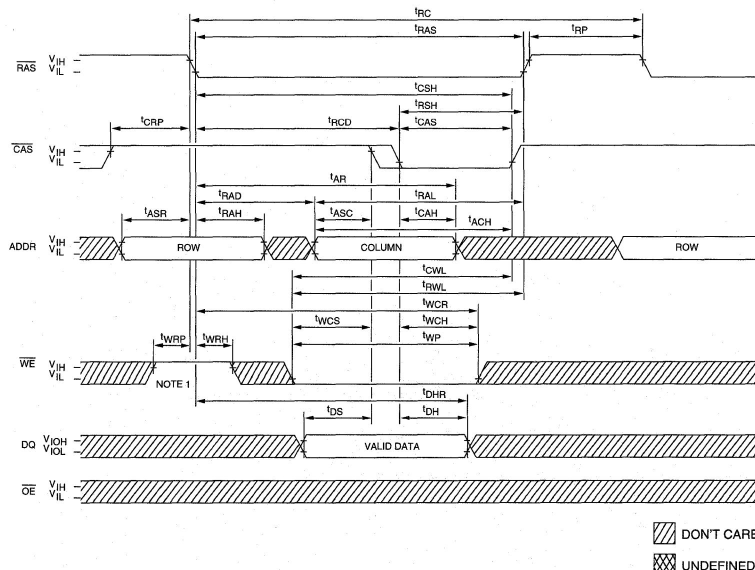
READ CYCLE [39]



EARLY WRITE CYCLE [39]



NOTE:

1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^{t}OFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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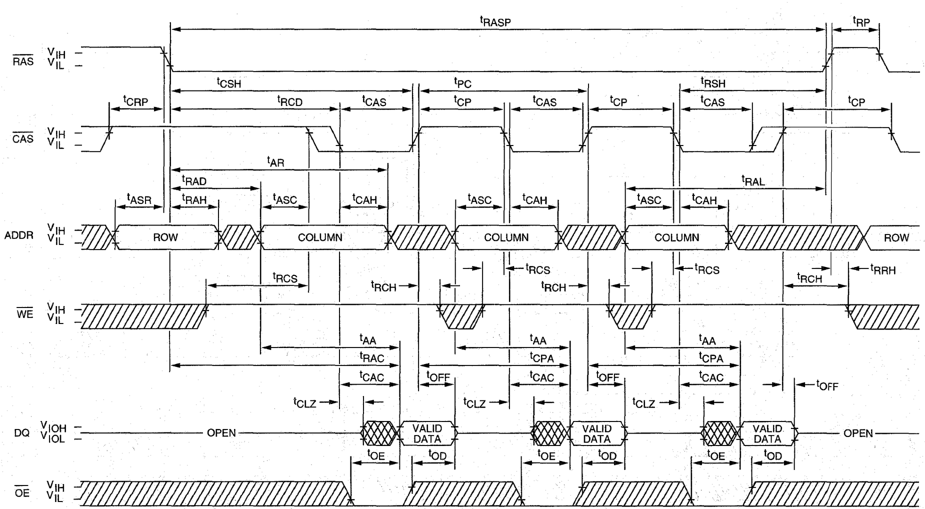
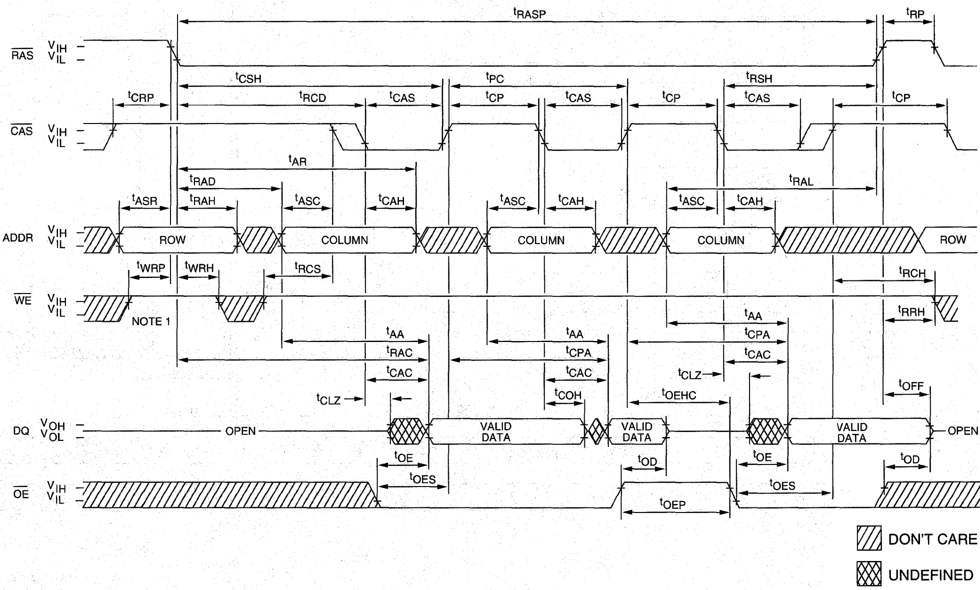
FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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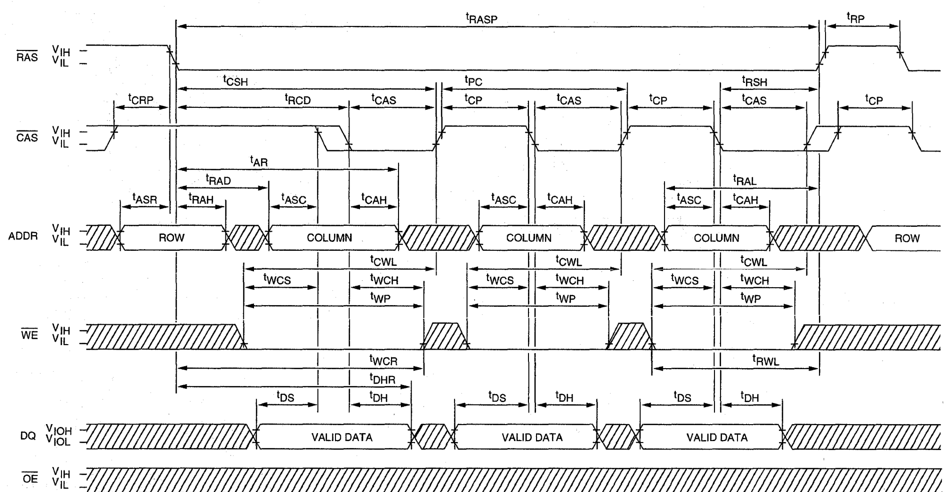
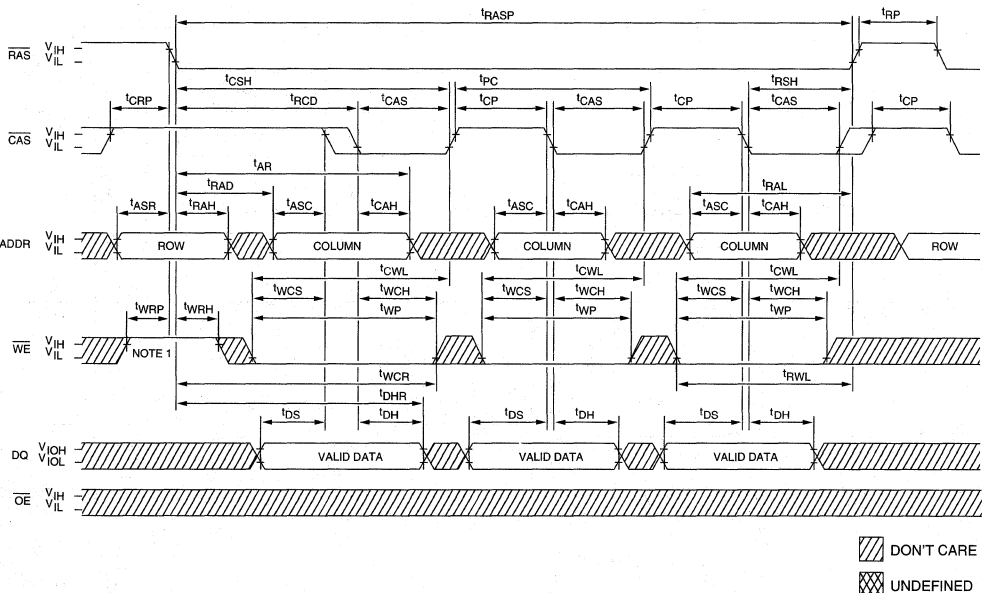
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

DRAM DIMM

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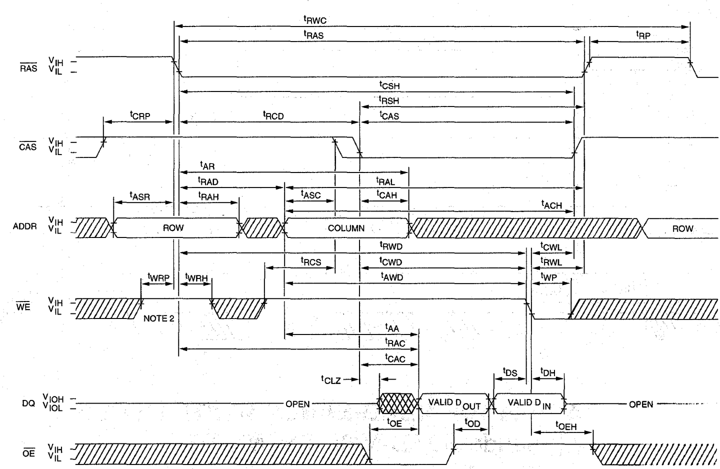
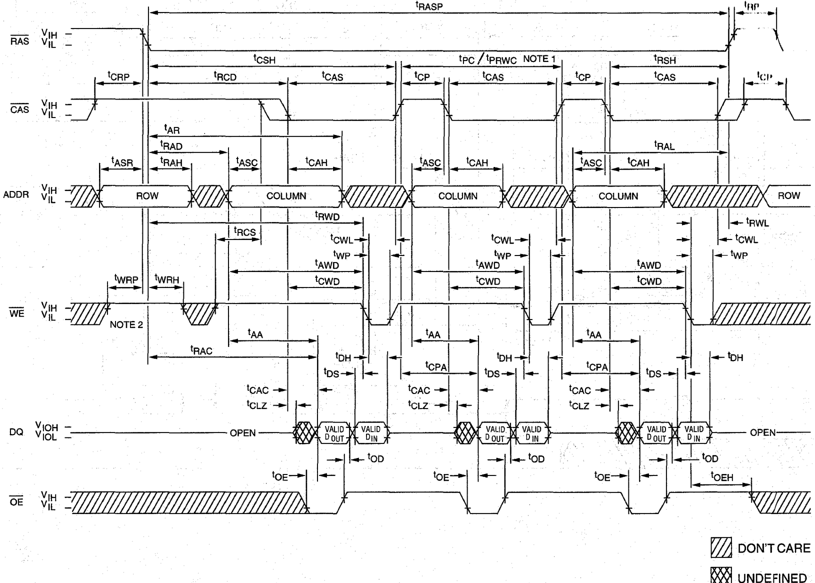
READ WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO/FAST PAGE MODE-PAGE-MODE READ-WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)



DON'T CARE

UNDEFINED

NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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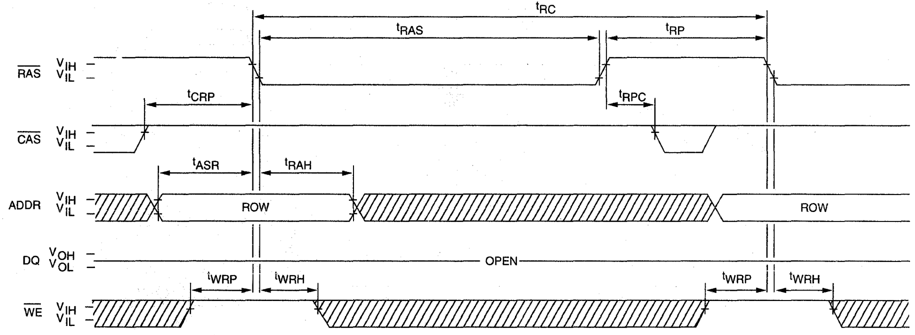
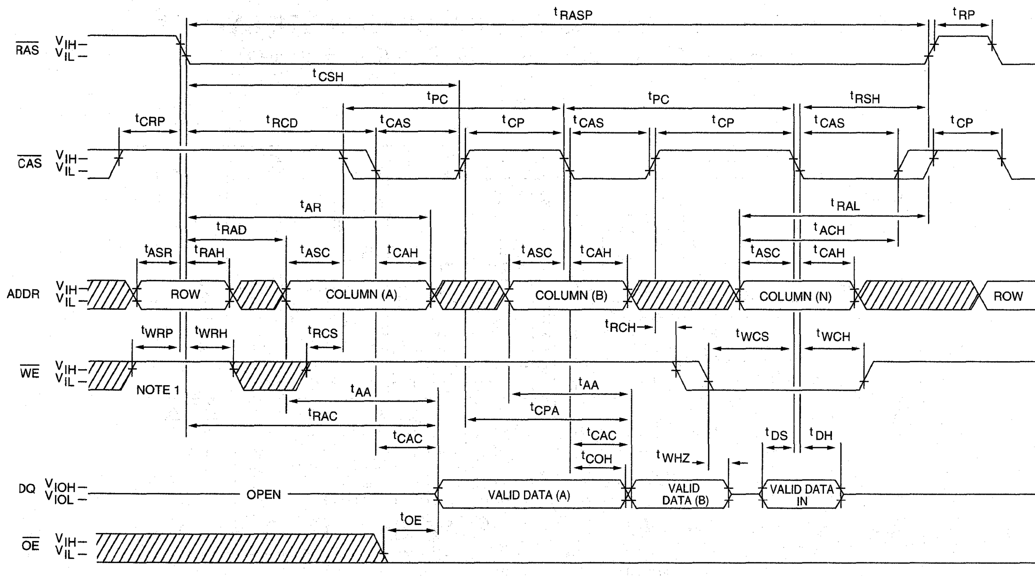
RAS-ONLY REFRESH CYCLE [39]
(WE = DON'T CARE)



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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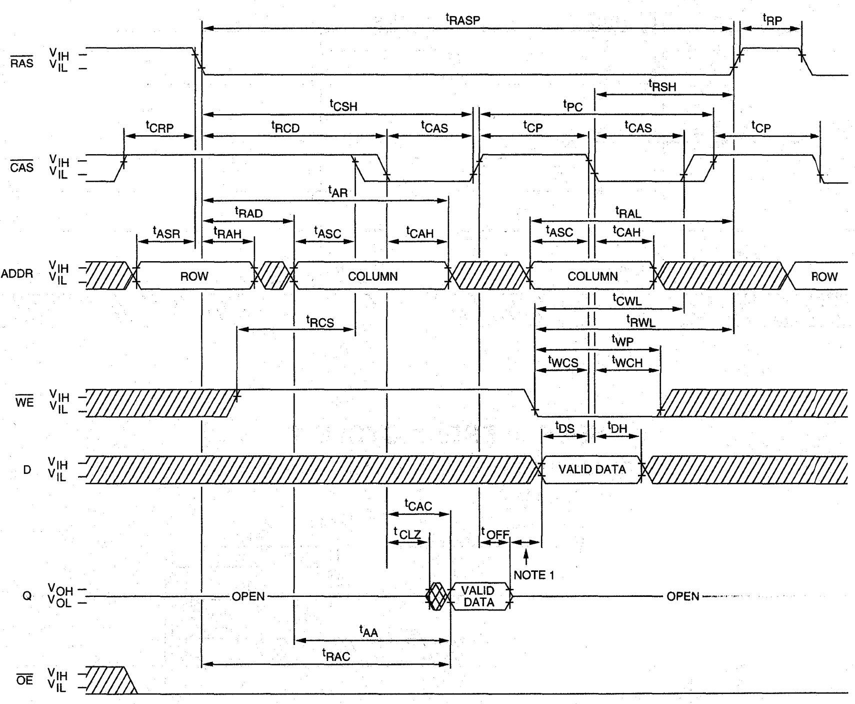
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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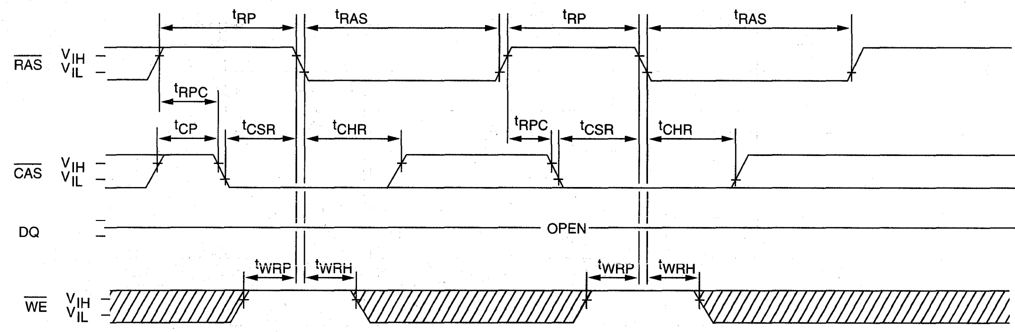
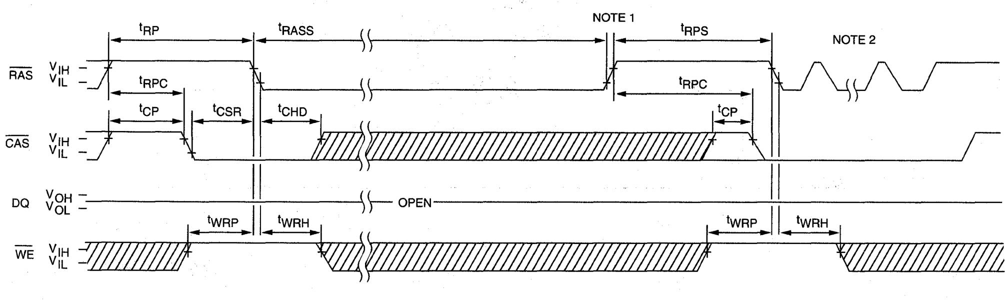
CBR REFRESH CYCLE [39]

(Addresses, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE [39]

(Addresses and $\overline{OE}$ = DON'T CARE)



DON'T CARE

UNDEFINED

NOTE: 1. Once ᵗRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a complete burst of all rows should be executed.

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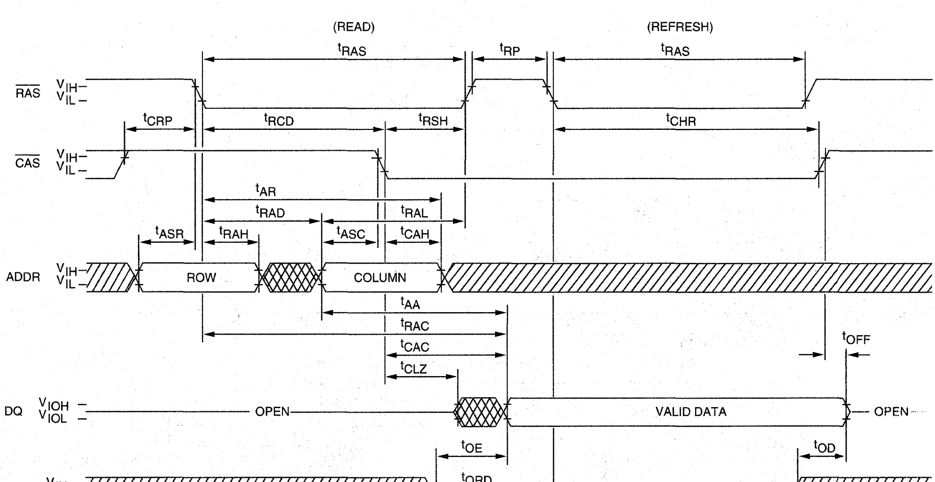
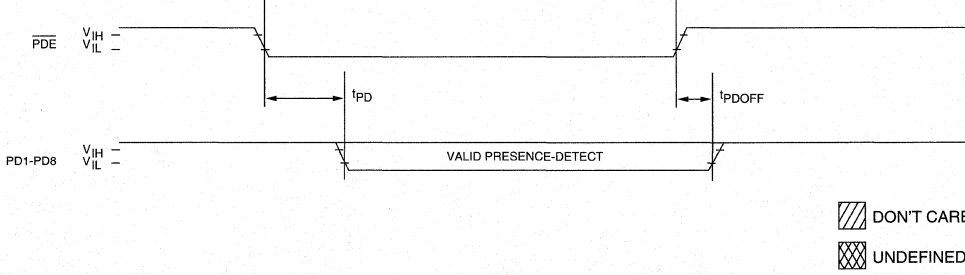
HIDDEN REFRESH CYCLE [21, 39]

(WE = HIGH; OE = LOW)



PRESENCE-DETECT READ CYCLE [39]



DRAM DIMM

NOTE: 1. PD pins must be pulled HIGH at next level of assembly.

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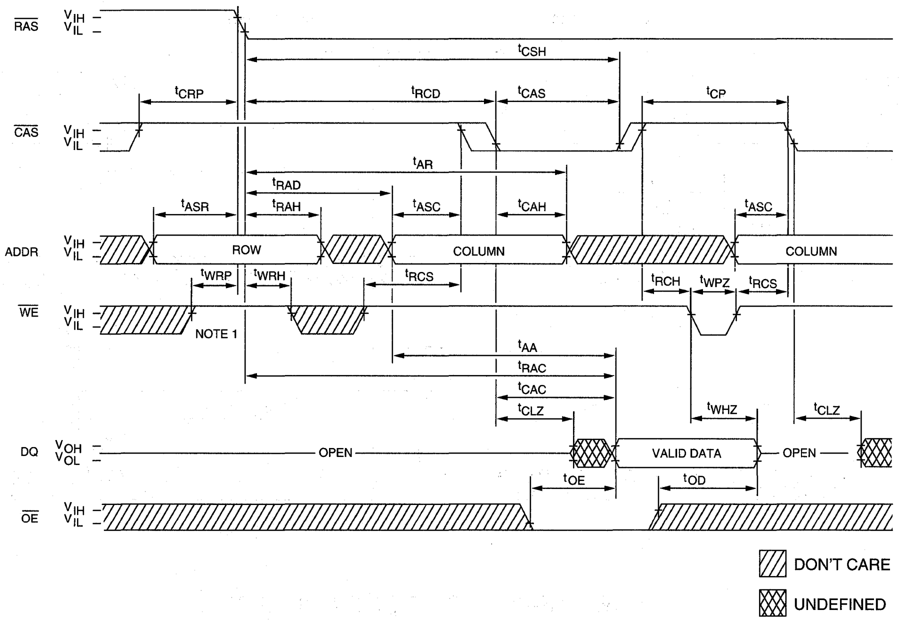
EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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DRAM MODULE

2 MEG x 72

16 MEGABYTE, ECC, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 9mW standby; 1,800mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR), HIDDEN: Extended and SELF REFRESH
- All inputs are buffered except $\overline{\text{RAS}}$
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP	DT
• Packages	
168-pin DIMM (gold)	G
• Refresh	
Standard/32ms	Blank
SELF REFRESH/128ms	S

KEY TIMING PARAMETERS

EDO option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	35ns	20ns	10ns
-7	130ns	70ns	30ns	40ns	25ns	12ns

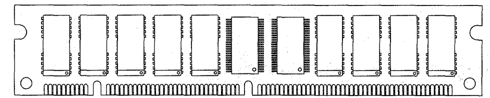
FPM option

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-17) SOJ Version
(DE-18) TSOP Version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ38	130	NC
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ28	111	RFU	153	DQ64
28	$\overline{\text{CAS0}}$	70	DQ29	112	NC	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	$\overline{\text{RAS0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

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VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT9LDT272G-xx	2 Meg x 72, FPM, TSOP
MT9LDT272G-xx S	2 Meg x 72, FPM, S*, TSOP
MT9LDT272G-xx X	2 Meg x 72, EDO, TSOP
MT9LDT272G-xx XS	2 Meg x 72, EDO, S*, TSOP
MT9LD272G-xx	2 Meg x 72, FPM, SOJ
MT9LD272G-xx S	2 Meg x 72, FPM, S*, SOJ
MT9LD272G-xx X	2 Meg x 72, EDO, SOJ
MT9LD272G-xx XS	2 Meg x 72, EDO, S*, SOJ

*S = SELF REFRESH

GENERAL DESCRIPTION

The MT9LD(T)272(X)(S) is a randomly accessed solid-state memory containing 2,097,152 words respectively organized in a x72 configuration. It is specially processed to operate from 3.0V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 21 address bits. The address is entered first by RAS latching 11 bits and then CAS latching 10 bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71.

READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. EARLY WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pin(s) remain open (High-Z) until the next CAS cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability ofdata-out even after CAS goes back HIGH. EDO provides for CAS precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS goes HIGH during READs, provided RAS and OE are held LOW. If OE is pulsed while RAS and CAS are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE is toggled or pulsed after CAS goes HIGH while RAS remains LOW, data will transition to and remain High-Z.

If the DQ outputs are wire OR'd, OE must be used to disable idle banks of DRAMs. Alternatively, pulsing WE to the idle banks during CAS HIGH time will also High-Z the outputs. Independent of OE control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS or CAS, whichever occurs last (reference the MT4LC2M8E7(S) DRAM data sheet for additional information on EDO functionality).

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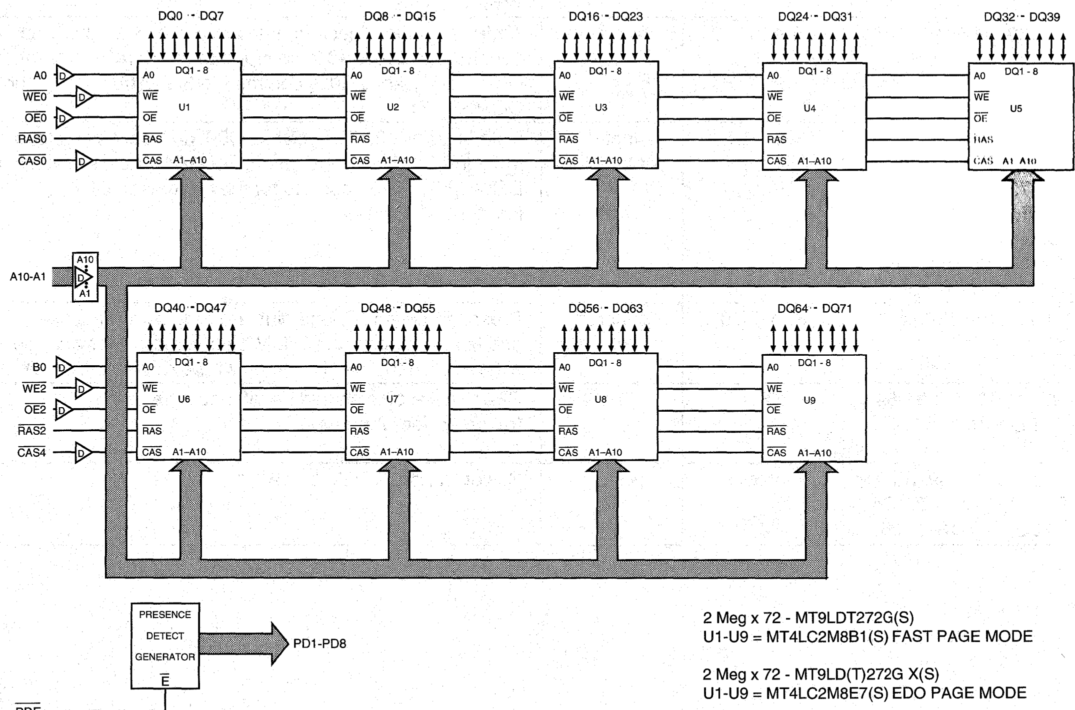
REFRESH

Returning RAS and CAS HIGH terminates a memory cycle, and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS addresses (A0-A10) are executed at least every 32ms (128ms "S" version), regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static, low-power, data-retention mode, or a dynamic refresh mode at the extended refresh period of 128ms, four times longer than the standard 32ms specifications. The module's SELF REFRESH mode is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified tRASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR refresh. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for the time minimum of an operation cycle, typically tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM



2 Meg x 72 - MT9LDT272G(S)
U1-U9 = MT4LC2M8B1(S) FAST PAGE MODE

2 Meg x 72 - MT9LD(T)272G X(S)
U1-U9 = MT4LC2M8E7(S) EDO PAGE MODE

NOTE: 1. All inputs with the exception of RAS are redriven.
2. D = line buffers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0, RAS2	Input	Row-Address Strobe: RAS is used to clock-in the 11 row-address bits. Two RAS inputs allow for one x72 bank or two x36 banks.
28, 46	CAS0, CAS4	Buffered Input	Column-Address Strobe: CAS is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	WE0, WE2	Buffered Input	Write Enable: WE is the READ/WRITE control for the DQ pins. WE0 controls DQ0-DQ35. WE2 controls DQ36-DQ71. If WE is LOW prior to CAS going LOW, the access is an EARLY WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0, OE2	Buffered Input	Output Enable: OE is the input/output control for the DQ pins. OE0 controls DQ0-DQ35. OE2 controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71.
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +3.3V ± 0.3V

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PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence Detect-Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES ᵗR	ADDRESSES ᵗC	DATA-IN/OUT DQ0-71
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

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PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: V_{SS} = ground; 0 = V_{OL}; 1 = V_{OH}.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss .... -1V to +4.5V
Voltage on Inputs or I/O Pins
Relative to Vss .... -1V to +5.5V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5V	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$, $\overline{CAS4}$ A0-A10, B0 $\overline{WE0,2}$,$\overline{OE0,2}$	I_{I1}	-2	2	µA	
	$\overline{RAS0}$, $\overline{RAS2}$	I_{I2}	-10	10	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ71	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB	18	18	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	16MB	4.5	4.5	mA	28
	I_{CC2} (S only)	16MB	1.3	1.3	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC3}	16MB	1,170	1,080	mA	3, 4, 28, 32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC4}	16MB	810	720	mA	3, 4, 28, 32
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC5} (X only)	16MB	1,080	990	mA	3, 4, 28, 32
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	16MB	1,170	1,080	mA	3, 28, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC7}	16MB	1,170	1,080	mA	3, 5, 28
REFRESH CURRENT: Extended CBR (S version only) Average power supply current $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); $\overline{WE}$ = Vcc -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ${}^tRC$ = 62.5µs (2,048 rows at 62.5µs = 128ms)	I_{CC8} (S only)	16MB	2.7	2.7	mA	3, 5, 28, 31
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH; CBR cycling with $\overline{RAS}$ ≥ ${}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0-A10, $\overline{OE}$ and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC9} (S only)	16MB	2.7	2.7	mA	5, 28

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CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		40	pF	2
Input Capacitance: $\overline{CAS0}$, $\overline{CAS4}$	C_{I4}		9	pF	2
Input/Output Capacitance: DQ0-DQ71	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		10	pF	2

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to $\overline{WE}$ delay time	^tAWD	57		62		ns	23, 30
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		20		ns	25
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	13		13		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		ns	23, 33
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	25
$\overline{CAS}$ hold time	^tCSH	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	7		7		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	42		47		ns	23, 30
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	15		20		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD	3	15	3	20	ns	33
Output enable	^tOE		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	13		13		ns	24

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NEW DRAM DIMM

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^{t}OFF	5	20	5	25	ns	20, 27, 36
OE setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
PDE to valid presence-detect data	^{t}PD		10		10	ns	35
PDE inactive to presence-detects inactive	^{t}PDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	87		97		ns	23
Access time from RAS	^{t}RAC		60		70	ns	14
RAS to column-address delay time	^{t}RAD	13	25	13	30	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to RAS lead time	^{t}RAL	35		40		ns	25
RAS pulse width	^{t}RAS	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
RAS pulse width during SELF REFRESH	^{t}RASS	100		100		µs	31
Random READ or WRITE cycle time	^{t}RC	110		130		ns	
RAS to CAS delay time	^{t}RCD	18	40	18	45	ns	17, 26
Read command hold time (referenced to CAS)	^{t}RCH	2		2		ns	19, 23
Read command setup time	^{t}RCS	2		2		ns	23
Refresh period (2,048 cycles) - 2 Meg x 72	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) - 2 Meg x 72 S version	^{t}REF		128		128	ms	
RAS precharge time	^{t}RP	40		50		ns	
RAS to CAS precharge time	^{t}RPC	0		0		ns	
RAS precharge time during SELF REFRESH	^{t}RPS	110		130		ns	31
Read command hold time (referenced to RAS)	^{t}RRH	0		0		ns	19
RAS hold time	^{t}RSH	20		25		ns	25
READ WRITE cycle time	^{t}RWC	155		185		ns	25
RAS to WE delay time	^{t}RWD	87		97		ns	23, 30
Write command to RAS lead time	^{t}RWL	20		25		ns	25
Transition time (rise or fall)	^{t}T	3	50	3	50	ns	
Write command hold time	^{t}WCH	15		20		ns	25
Write command hold time (referenced to RAS)	^{t}WCR	43		53		ns	24
WE command setup time	^{t}WCS	2		2		ns	23, 30
Write command pulse width	^{t}WP	10		15		ns	
WE hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 23

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		35		40	ns	25
Column-address setup to CAS precharge during writes	tACH	15		15		ns	
Column-address hold time (referenced to RAS)	tAR	43		53		ns	24
Column-address setup time	tASC	2		2		ns	23
Row-address setup time	tASR	5		5		ns	25
Column-address to WE delay time	tAWD	57		67		ns	23, 30
Access time from CAS	tCAC		20		25	ns	15, 25
Column-address hold time	tCAH	15		17		ns	25
CAS pulse width	tCAS	10	10,000	12	10,000	ns	
RAS LOW to "don't care" during SELF REFRESH	tCHD	15		15		ns	31
CAS hold time (CBR REFRESH)	tCHR	8		10		ns	5, 24
CAS to output in Low-Z	tCLZ	2		2		ns	23
Data output hold after CAS LOW	tCOH	7		7		ns	23
CAS precharge time	tCP	10		10		ns	16
Access time from CAS precharge	tCPA		40		45	ns	25, 37
CAS to RAS precharge time	tCRP	10		10		ns	25
CAS hold time	tCSH	48		53		ns	24
CAS setup time (CBR REFRESH)	tCSR	7		7		ns	5, 23
CAS to WE delay time	tCWD	37		42		ns	23, 30
Write command to CAS lead time	tCWL	15		15		ns	
Data-in hold time	tDH	15		17		ns	25, 29
Data-in hold time (referenced to RAS)	tDHR	45		55		ns	
Data-in setup time	tDS	-2		-2		ns	24, 29
Output disable	tOD	0	15	0	15	ns	
Output enable	tOE		15		15	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	10		10		ns	24
OE HIGH hold time from CAS HIGH	tOEHC	10		10		ns	
OE HIGH pulse width	tOEP	10		10		ns	
OE LOW to CAS HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	5	20	5	20	ns	20, 27, 36
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		0		ns	20
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	
PDE to Valid Presence-Detect Data	tPD		10		10	ns	35
PDE Inactive to Presence-Detects Inactive	tPDOFF	2		2		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	77		87		ns	23
Access time from RAS	tRAC		60		70	ns	14
RAS to column-address delay time	tRAD	10	25	10	30	ns	18, 26
Row-address hold time	tRAH	8		8		ns	24
Column-address to RAS lead time	tRAL	35		40		ns	25
RAS pulse width	tRAS	60	10,000	70	10,000	ns	
RAS pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
RAS pulse width during SELF REFRESH	tRASS	100		100		µs	31
Random READ or WRITE cycle time	tRC	110		130		ns	

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EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ to $\overline{CAS}$ delay time	^{t}RCD	12	40	12	45	ns	17, 26
Read command hold time (referenced to $\overline{CAS}$)	^{t}RCH	2		2		ns	19, 23
Read command setup time	^{t}RCS	2		2		ns	23
Refresh period (2,048 cycles) - 2 Meg x 72	^{t}REF		32		32	ms	
Refresh period (2,048 cycles) - 2 Meg x 72 S version	^{t}REF		128		128	ms	
$\overline{RAS}$ precharge time	^{t}RP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	^{t}RPS	110		130		ns	31
Read command hold time (referenced to $\overline{RAS}$)	^{t}RRH	0		0		ns	19
$\overline{RAS}$ hold time	^{t}RSH	15		17		ns	25
READ WRITE cycle time	^{t}RWC	155		182		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	82		92		ns	23, 30
Write command to $\overline{RAS}$ lead time	^{t}RWL	20		20		ns	25
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
Write command hold time	^{t}WCH	15		17		ns	25
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	43		53		ns	24
$\overline{WE}$ command setup time	^{t}WCS	2		2		ns	23
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	^{t}WHZ	2	18	2	20	ns	27
Write command pulse width	^{t}WP	10		12		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	^{t}WPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^{t}WRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR with $\overline{\text{WE}}$ HIGH) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns for FPM and 2.5ns for EDO.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{\text{WE}}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by one-half when used in the x36 mode.
29. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.

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NOTES (continued)

31. Refresh must be completed within the time of three external refresh rate periods prior to active use of the DRAM (provided distributed CBR REFRESH is used when in the active mode.) Alternatively, a complete set of row refreshes must be executed when exiting SELF REFRESH prior to active use of the DRAM if anything other than distributed CBR REFRESH is used in the active mode.
32. Column-address changed once each cycle.
33. The 3ns minimum is a parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pullup resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. For FAST PAGE MODE option, ^{t}OFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
37. Applies to both EDO and FAST PAGE MODEs.

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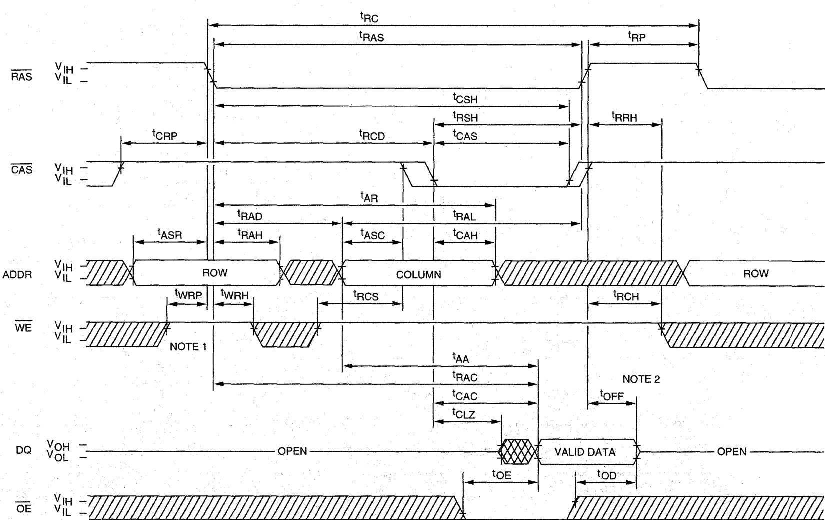
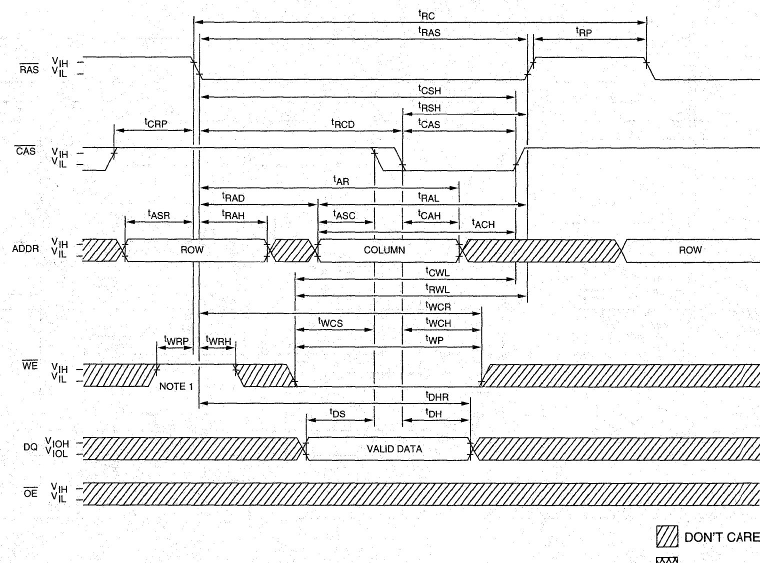
READ CYCLE [37]



EARLY WRITE CYCLE [37]



NEW DRAM DIMM

NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

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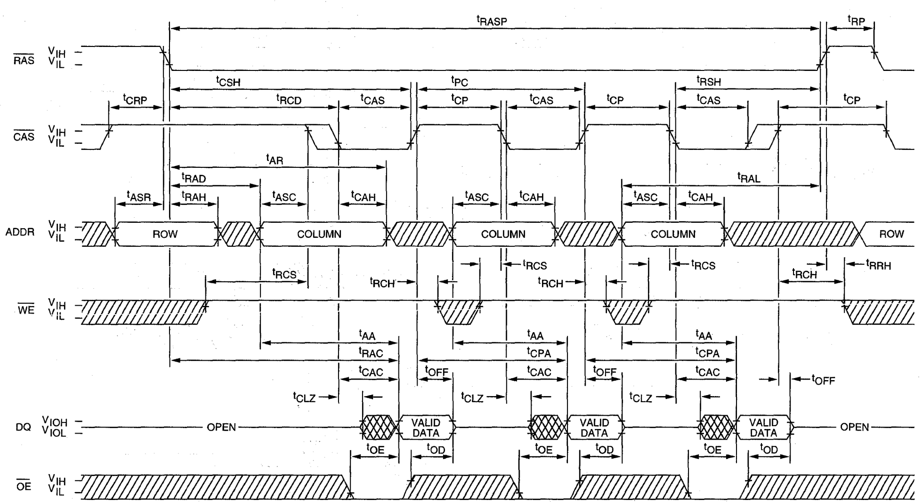
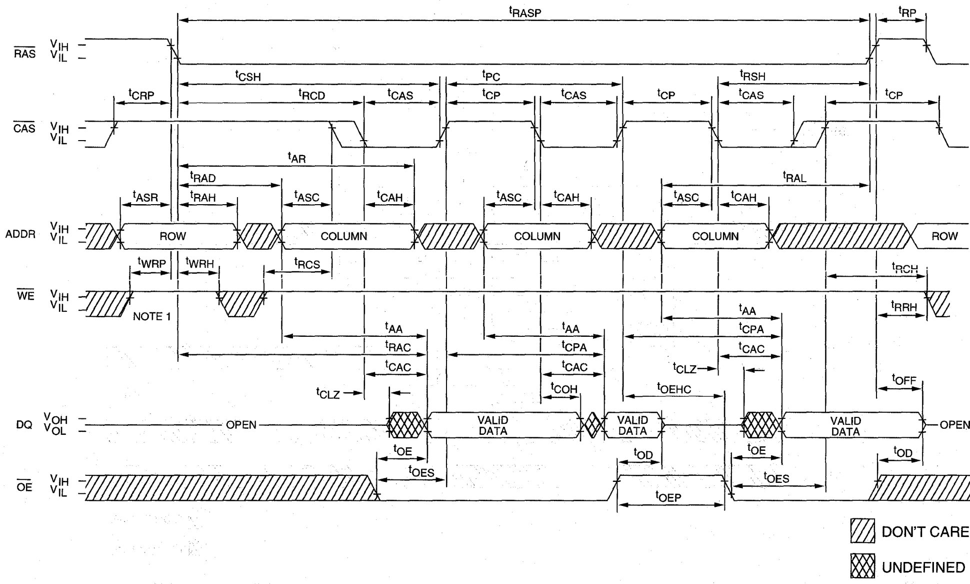
NEW DRAM DIMM

FAST-PAGE-MODE READ CYCLE



EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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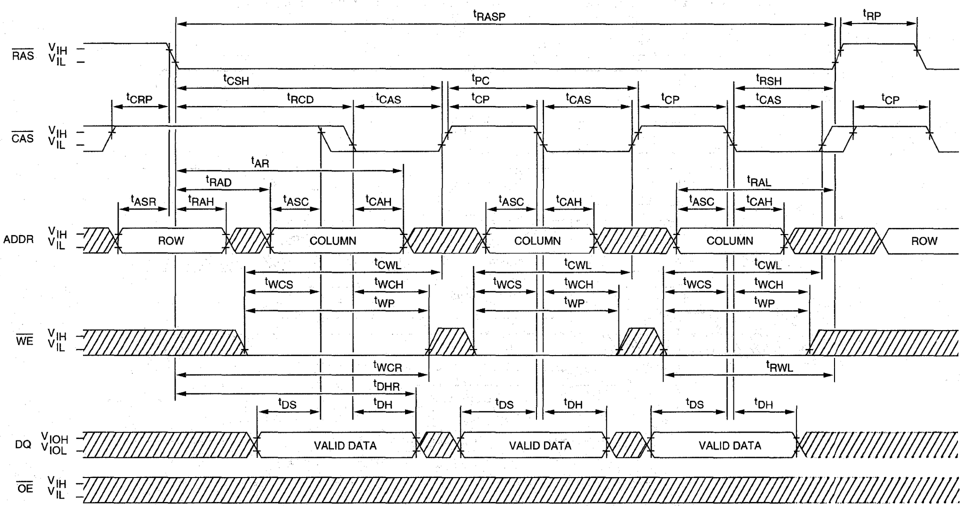
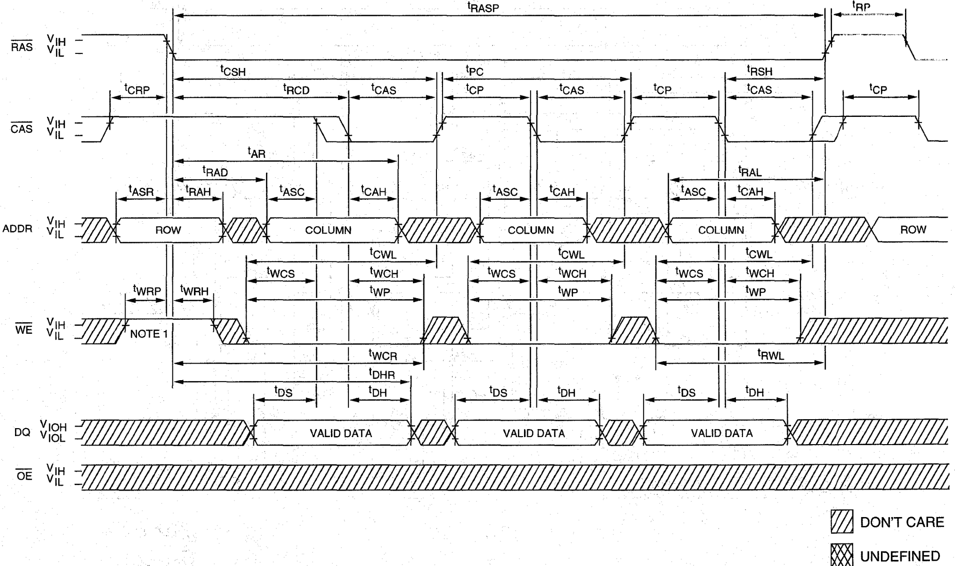
FAST-PAGE-MODE EARLY-WRITE CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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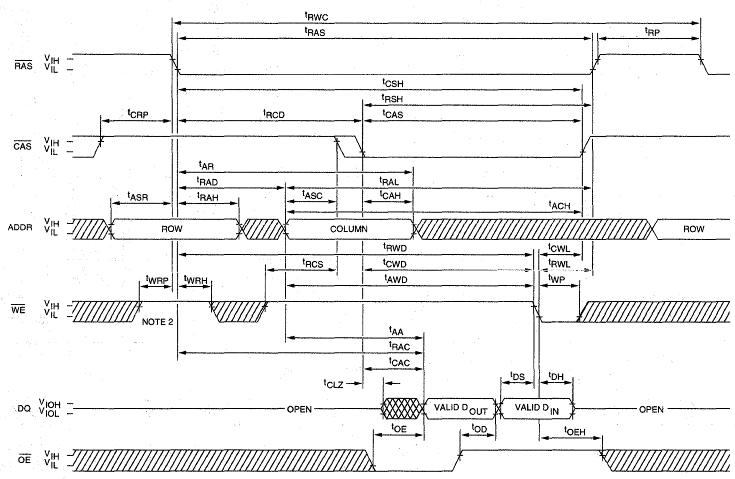
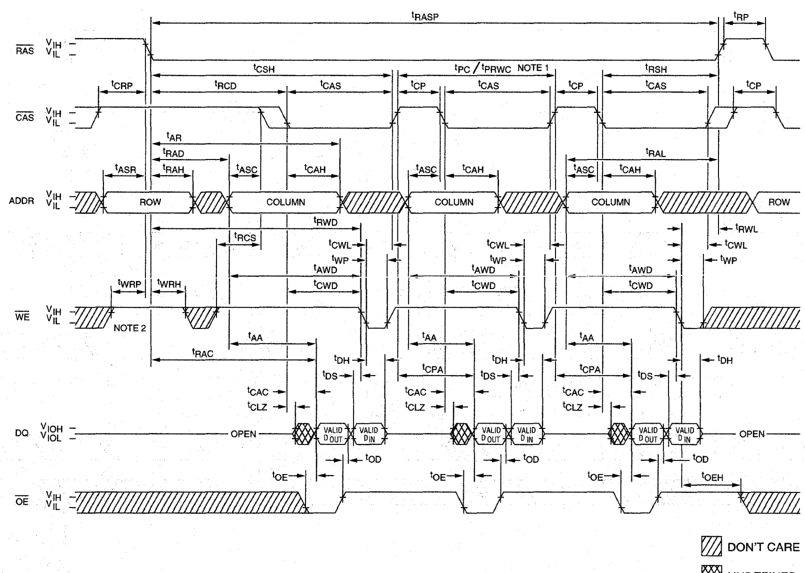
READ WRITE CYCLE [37]
(LATE WRITE and READ-MODIFY-WRITE cycles)



EDO/FAST-PAGE-MODE READ-WRITE CYCLE [37]
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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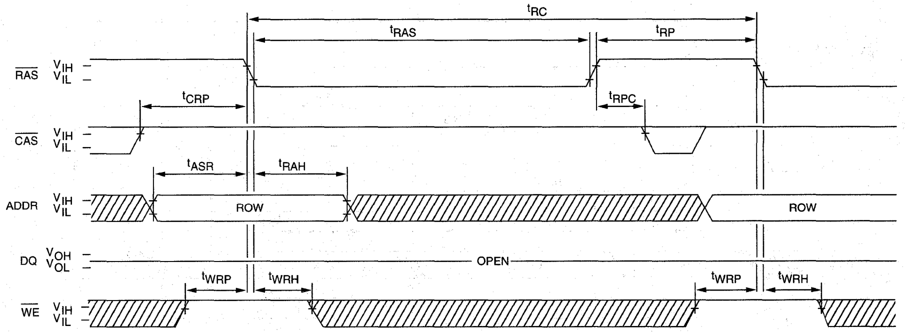
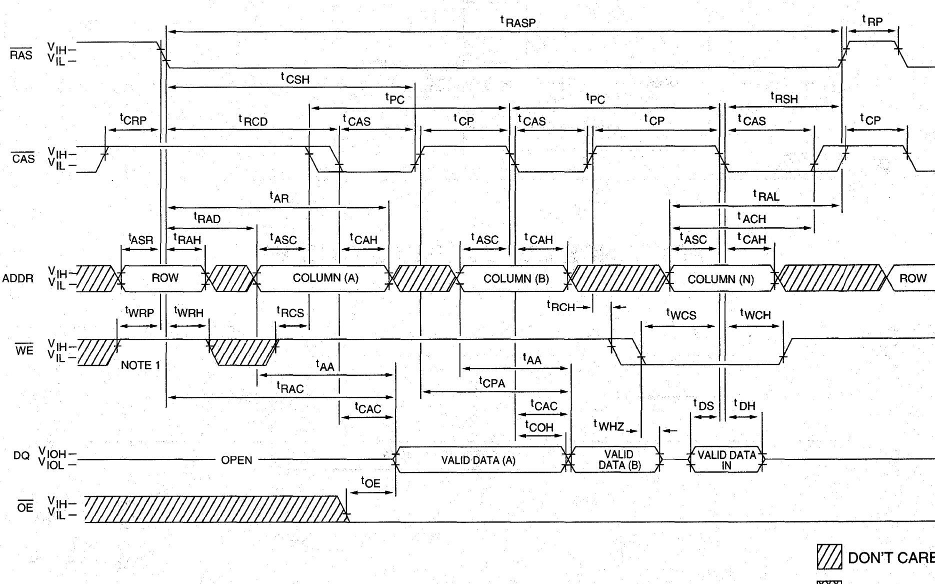
RAS-ONLY REFRESH CYCLE [37]
(WE = DON'T CARE)



EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



DON'T CARE

UNDEFINED

NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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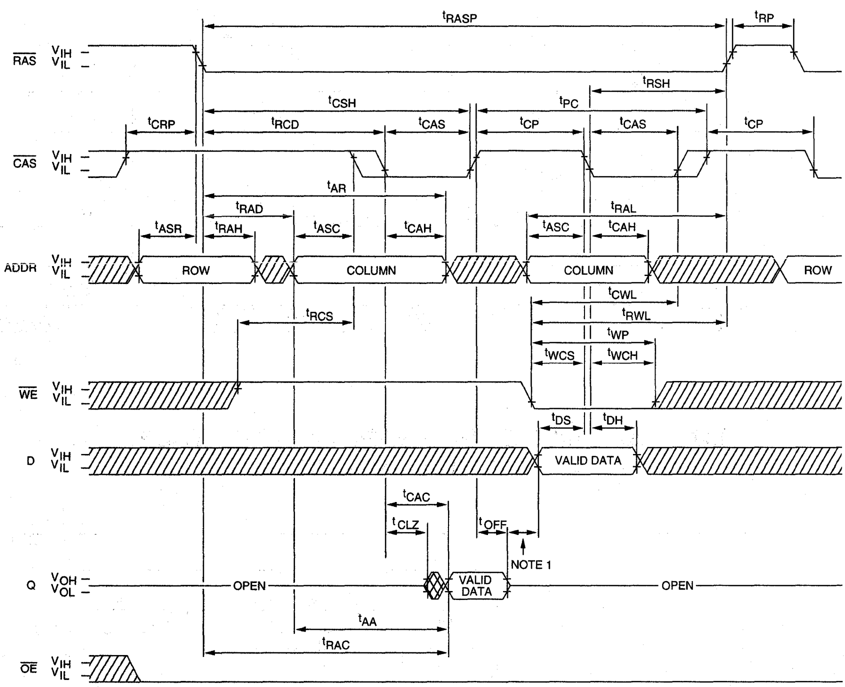
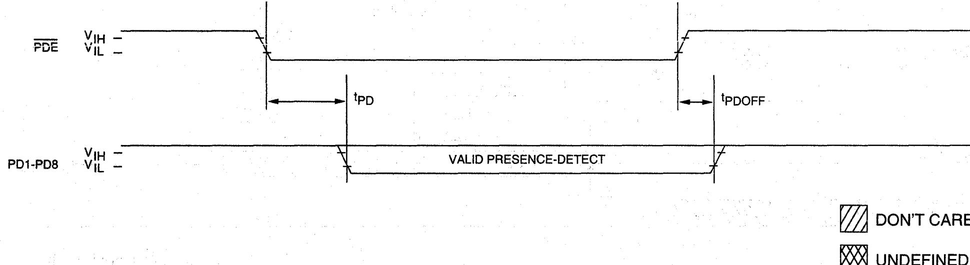
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



PRESENCE-DETECT READ CYCLE [37]



DON'T CARE
UNDEFINED

NOTE: 1. Do not drive data prior to tristate.
2. PD pins must be pulled HIGH at next level of assembly.

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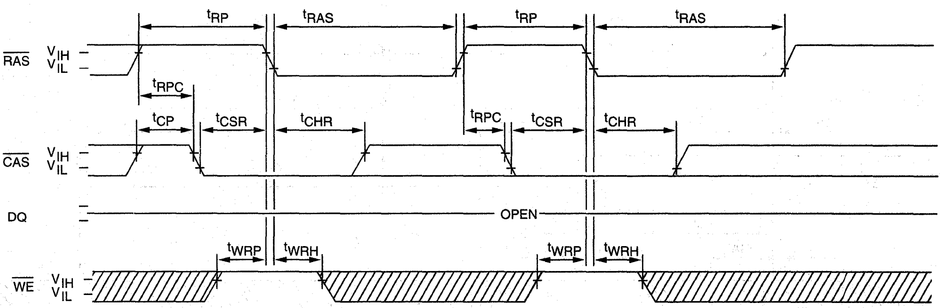
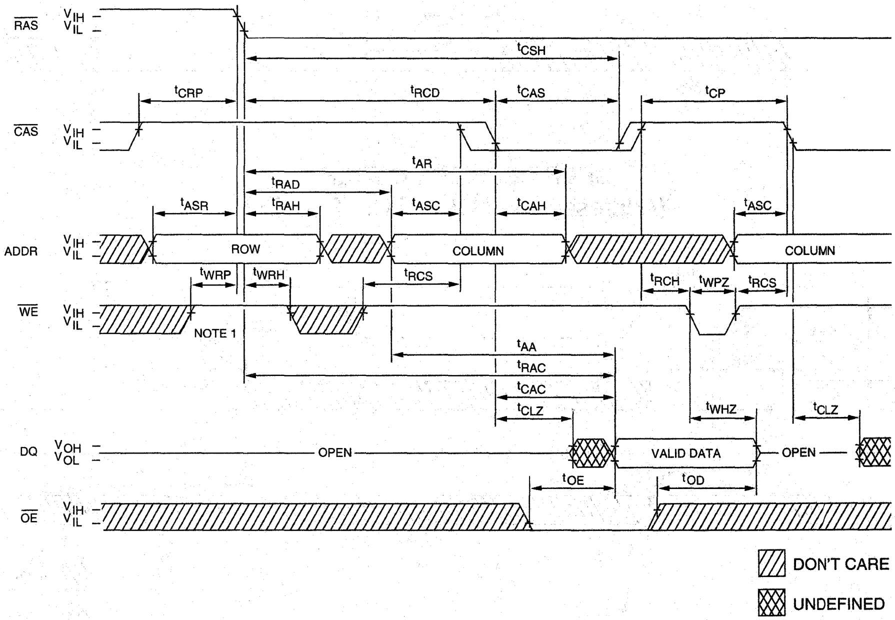
CBR REFRESH CYCLE [37]

(Addresses, $\overline{OE}$ = DON'T CARE)



EDO READ CYCLE

(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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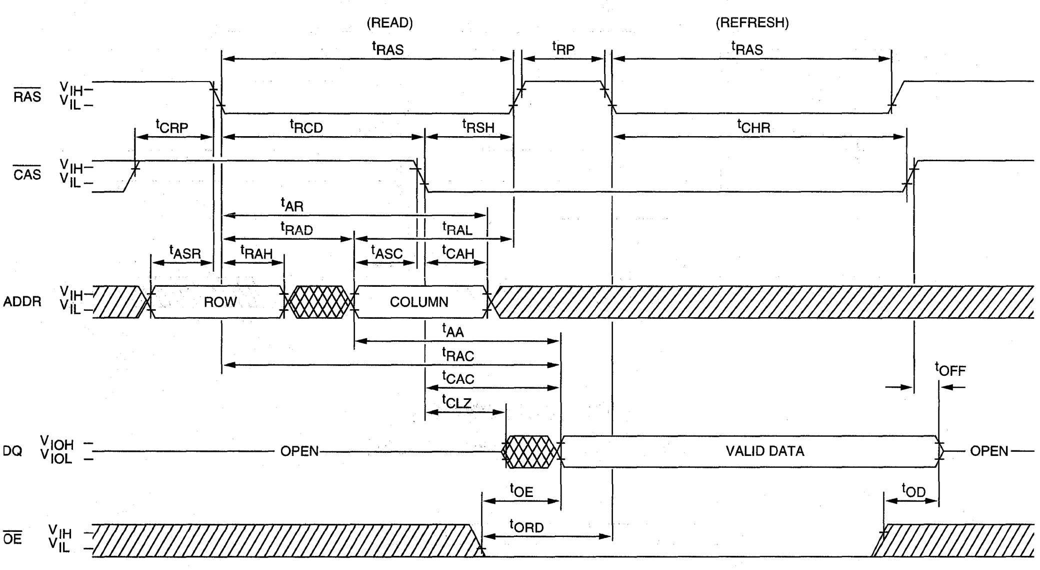
NEW DRAM DIMM

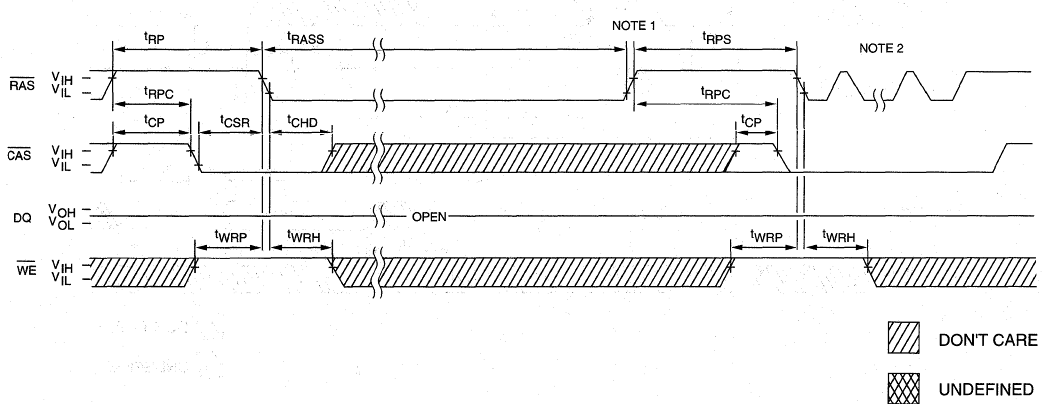
HIDDEN REFRESH CYCLE [21, 37]

(WE = HIGH; OE = LOW)



SELF REFRESH CYCLE [37]

(Addresses and OE = DON'T CARE)



NOTE:

1. Once ᵗRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ᵗRPS is satisfied, a compete burst of all rows should be executed.

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DRAM CARD PRODUCT SELECTION GUIDE

Memory Configuration			Part Number	Access Time (ns)	Number of Pins Card	Page
3.3V DRAM Cards						
1 Meg x 32	3.3V	4 Megabytes	MT8D88C132V(S)	60, 70, 80	88	6-33
1 Meg x 32	3.3V	4 Megabytes	MT8D88C132VH(S)	60, 70, 80	88	6-49
2 Meg x 32	3.3V	8 Megabytes	MT16D88C232V(S)	60, 70, 80	88	6-33
2 Meg x 32	3.3V	8 Megabytes	MT16D88C232VH(S)	60, 70, 80	88	6-49
4 Meg x 32	3.3V	16 Megabytes	MT8D88C432V(S)	60, 70, 80	88	6-33
4 Meg x 32	3.3V	16 Megabytes	MT8D88C432VH(S)	60, 70, 80	88	6-49
8 Meg x 32	3.3V	32 Megabytes	MT16D88C832V(S)	60, 70, 80	88	6-33
8 Meg x 32	3.3V	32 Megabytes	MT16D88C832VH(S)	60, 70, 80	88	6-49
5V DRAM Cards						
1 Meg x 32	5V	4 Megabytes	MT8D88C132(S)	60, 70	88	6-1
1 Meg x 32	5V	4 Megabytes	MT8D88C132H(S)	60, 70	88	6-17
2 Meg x 32	5V	8 Megabytes	MT16D88C232(S)	60, 70	88	6-1
2 Meg x 32	5V	8 Megabytes	MT16D88C232H(S)	60, 70	88	6-17

DRAM CARD

4, 8 MEGABYTES

1 MEG, 2 MEG x 32; 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Low power
- JEDEC-standard 88-pin DRAM card pinout
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE (FPM) access cycle
- Single +5V ±5% power supply
- Extended Refresh

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	37ns	22ns	40ns
-7	130ns	70ns	40ns	42ns	27ns	50ns

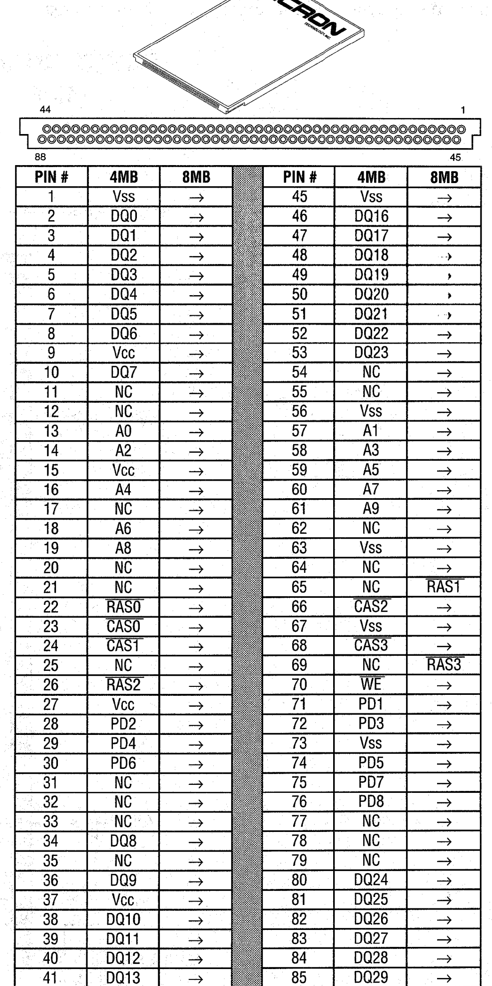
VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8D88C132-xx	1 Meg x 32
MT8D88C132-xx S	1 Meg x 32, SELF REFRESH
MT16D88C232-xx	2 Meg x 32
MT16D88C232-xx S	2 Meg x 32, SELF REFRESH

GENERAL DESCRIPTION

The MT8D88C132(S) and MT16D88C232(S) comprise a family of JEDEC standard DRAM cards organized in x32-bit memory arrays. The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

PIN ASSIGNMENT (End View)
88-Pin Card (DF-1)



PIN #	4MB	8MB	PIN #	4MB	8MB
1	Vss	→	45	Vss	→
2	DQ0	→	46	DQ16	→
3	DQ1	→	47	DQ17	→
4	DQ2	→	48	DQ18	→
5	DQ3	→	49	DQ19	→
6	DQ4	→	50	DQ20	→
7	DQ5	→	51	DQ21	→
8	DQ6	→	52	DQ22	→
9	Vcc	→	53	DQ23	→
10	DQ7	→	54	NC	→
11	NC	→	55	NC	→
12	NC	→	56	Vss	→
13	A0	→	57	A1	→
14	A2	→	58	A3	→
15	Vcc	→	59	A5	→
16	A4	→	60	A7	→
17	NC	→	61	A9	→
18	A6	→	62	NC	→
19	A8	→	63	Vss	→
20	NC	→	64	NC	→
21	NC	→	65	NC	$\overline{RAS1}$
22	$\overline{RAS0}$	→	66	$\overline{CAS2}$	→
23	$\overline{CAS0}$	→	67	Vss	→
24	$\overline{CAS1}$	→	68	$\overline{CAS3}$	→
25	NC	→	69	NC	$\overline{RAS3}$
26	$\overline{RAS2}$	→	70	$\overline{WE}$	→
27	Vcc	→	71	PD1	→
28	PD2	→	72	PD3	→
29	PD4	→	73	Vss	→
30	PD6	→	74	PD5	→
31	NC	→	75	PD7	→
32	NC	→	76	PD8	→
33	NC	→	77	NC	→
34	DQ8	→	78	NC	→
35	NC	→	79	NC	→
36	DQ9	→	80	DQ24	→
37	Vcc	→	81	DQ25	→
38	DQ10	→	82	DQ26	→
39	DQ11	→	83	DQ27	→
40	DQ12	→	84	DQ28	→
41	DQ13	→	85	DQ29	→
42	DQ14	→	86	DQ30	→
43	DQ15	→	87	DQ31	→
44	Vss	→	88	Vss	→

DRAM CARD

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GENERAL DESCRIPTION (continued)

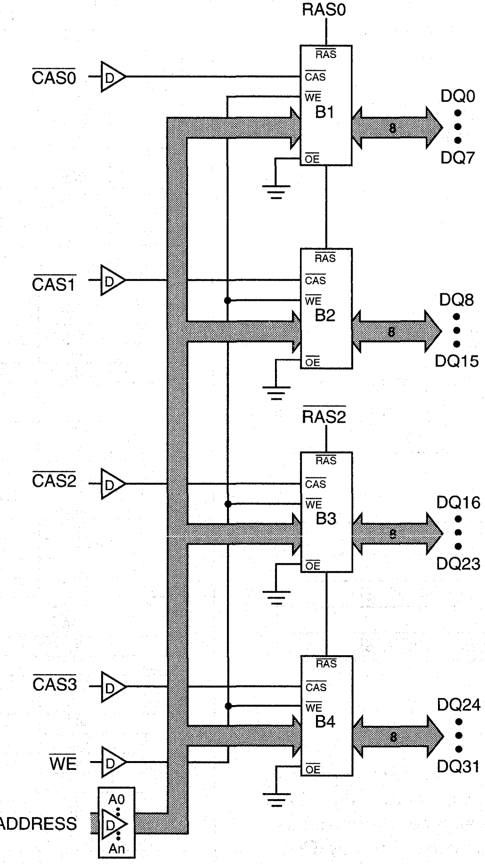
These cards are designed for low-power operation using low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with 2 separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the card's advanced power-saving features.

These Micron DRAM Cards are built with 3.370-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132)



NOTE: 1. B1 through B4 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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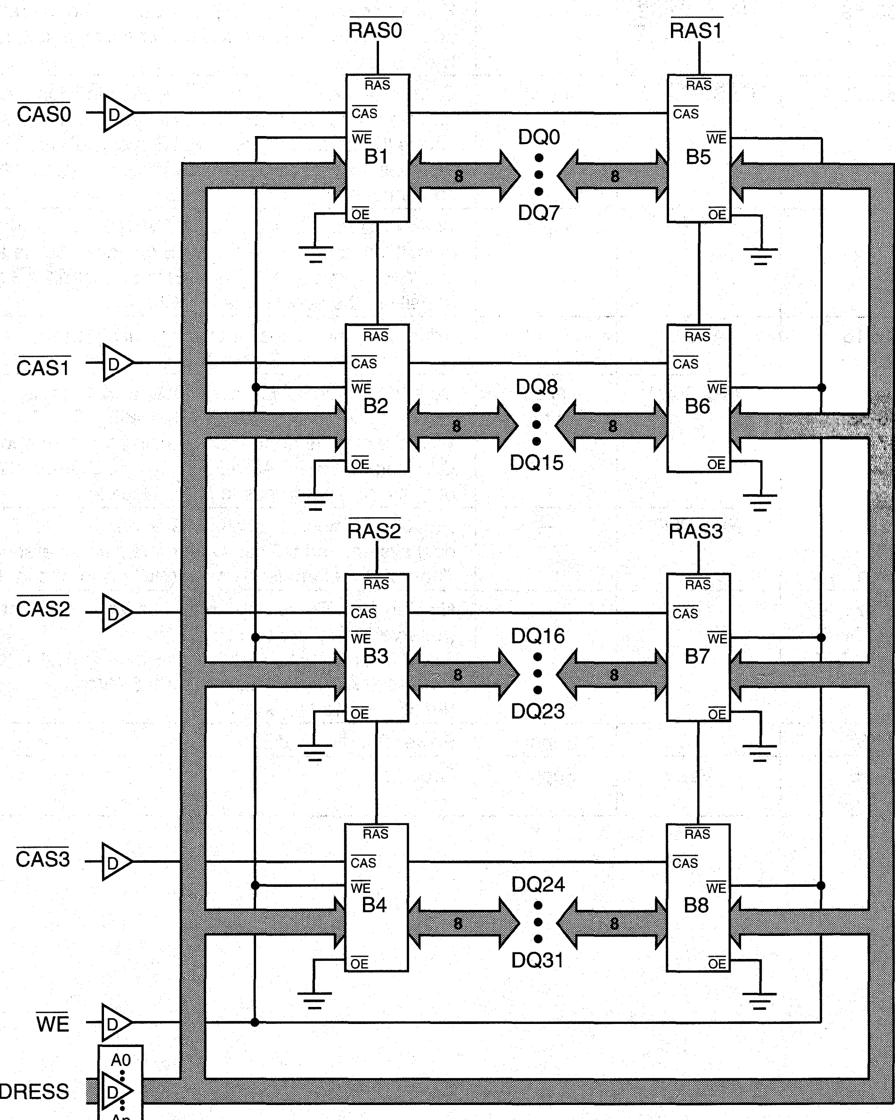
FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232)



NOTE: 1. B1 through B8 = x8 memory blocks.
2. D = 74AC11244 line drivers.

DRAM CARD

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0}$-$\overline{CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	—	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
11, 12, 17, 20, 21, 25, 31, 32, 33, 35, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	—	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. Pins 11, 17, 25, 35 reserved for 3.3V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

DRAM CARD

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FUNCTIONAL DESCRIPTION

The MT8D88C132(S) and MT16D88C232(S) comprise a family of DRAM cards organized in x32-bit memory arrays (RAS0 = RAS2). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32-bit applications use the same signal to control the CAS inputs. RAS0 and RAS1 control the lower 16 bits and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and CAS pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, extended CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits, and CAS latches the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx {}^{t}$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM Cards are constructed with a 3.370-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{RAS}$ Address	$\overline{CAS}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^tRAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

DRAM CARD

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +7V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.75	5.25	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.4	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input: 0V ≤ VIN ≤ 6.5V (All other pins not under test = 0V) for each package input	$\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$	II1	-8	8	µA	
	Buffered	II2	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ 5.5V) for each package input	DQ0-DQ31	IOZ	-20	20	µA	33
OUTPUT LEVELS Output High Voltage (IOUT = -5 mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 4.2 mA)		VOL		0.4	V	

DRAM CARD

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	4MB 8MB	880 896	800 816	mA	3, 4, 30
STANDBY CURRENT: (TTL) (RAS = CAS = V_{IH})	I_{CC2}	4MB 8MB	16 32	16 32	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V_{IL}, CAS, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC3}	4MB 8MB	640 656	560 576	mA	3, 4, 30
STANDBY CURRENT: (CMOS) (RAS = CAS = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB 8MB	1.6 3.2	1.6 3.2	mA	
REFRESH CURRENT: RAS ONLY Average power supply current (RAS Cycling, CAS = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB	880 896	800 816	mA	3, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB	880 960	800 880	mA	3, 5
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR; CAS = 0.2V or CBR cycling; RAS = ^tRAS (MIN); ^tRC = 125µs; WE = Vcc-0.2V; A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB 8MB	2.4 4.8	2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with RAS ≥ ^tRASS (MIN) and CAS held LOW; WE = Vcc-0.2V; A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB 8MB	2.4 4.8	2.4 4.8	mA	5, 31

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CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I1}	9	9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	13	13	pF	2
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addressess	C_{I3}	9	9	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C $\leq T_A \leq$ 55°C; Vcc = +5V ±5%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		37		42	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^{t}AR	43		48		ns	24
Column-address setup time	^{t}ASC	2		2		ns	23
Row-address setup time	^{t}ASR	7		7		ns	25
Access time from $\overline{CAS}$	^{t}CAC		22		27	ns	15, 25
Column-address hold time	^{t}CAH	17		22		ns	25
$\overline{CAS}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time entering SELF REFRESH	^{t}CHD	10		10		ns	31
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	8		8		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^{t}CLZ	5		5		ns	23, 32
$\overline{CAS}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^{t}CPA		42		47	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^{t}CRP	17		17		ns	25
$\overline{CAS}$ hold time	^{t}CSH	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	12		12		ns	5, 23
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	17		22		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	-2		-2		ns	24
Output buffer turn-off delay	^{t}OFF	5	22	5	27	ns	19, 27
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
Access time from $\overline{RAS}$	^{t}RAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^{t}RAD	13	23	13	28	ns	18, 26
Row-address hold time	^{t}RAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	^{t}RAL	37		42		ns	25
$\overline{RAS}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width entering SELF REFRESH	^{t}RASS	100		100		µs	31

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	ᵗRC	110		130		ns	
RAS to CAS delay time	ᵗRCD	18	38	18	43	ns	17, 26
Read command hold time (referenced to CAS)	ᵗRCH	2		2		ns	19, 23
Read command setup time	ᵗRCS	2		2		ns	23
Refresh period (1,024 cycles)	ᵗREF		128		128	ms	
RAS precharge time	ᵗRP	40		50		ns	
RAS to CAS precharge time	ᵗRPC	0		0		ns	
RAS precharge time exiting SELF REFRESH	ᵗRPS	110		130		ns	31
Read command hold time (referenced to RAS)	ᵗRRH	0		0		ns	19
RAS hold time	ᵗRSH	22		27		ns	25
Write command to RAS lead time	ᵗRWL	22		27		ns	25
Transition time (rise or fall)	ᵗT	3	50	3	50	ns	
Write command hold time	ᵗWCH	17		22		ns	25
Write command hold time (referenced to RAS)	ᵗWCR	43		53		ns	24
WE command setup time	ᵗWCS	2		2		ns	23
Write command pulse width	ᵗWP	10		15		ns	
WE hold time (CBR REFRESH)	ᵗWRH	8		8		ns	22, 24
WE setup time (CBR REFRESH)	ᵗWRP	12		12		ns	22, 23

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +5V ±10%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. If $\overline{CAS}$ = VIH, data output is High-Z.
12. If $\overline{CAS}$ = VIL, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^tWRP and ^tWRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A +7ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A -2ns (MIN) and a -7ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A +2ns (MIN) and a +7ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. The maximum current ratings are based on one of the two banks operating or being refreshed in a x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
30. Column-address changed once each cycle.
31. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
32. The 3ns minimum is a parameter guaranteed by design.
33. 4MB version is half of values shown.

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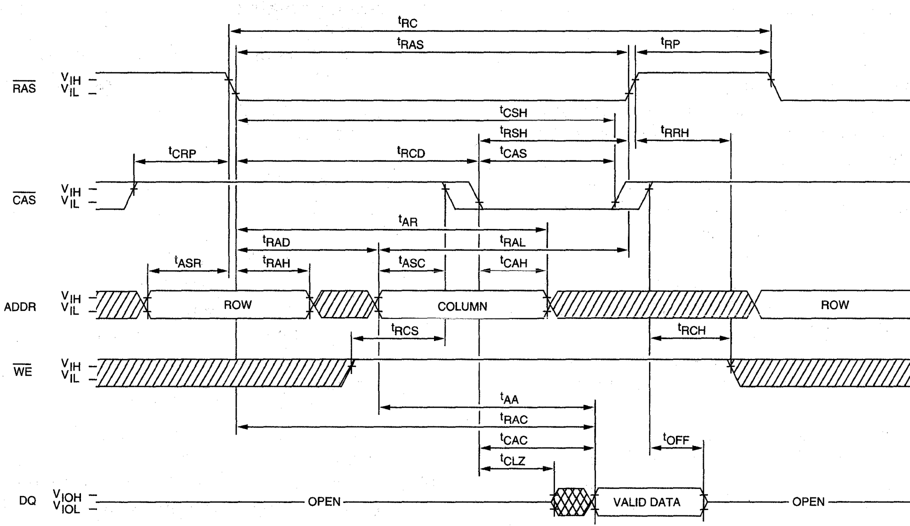
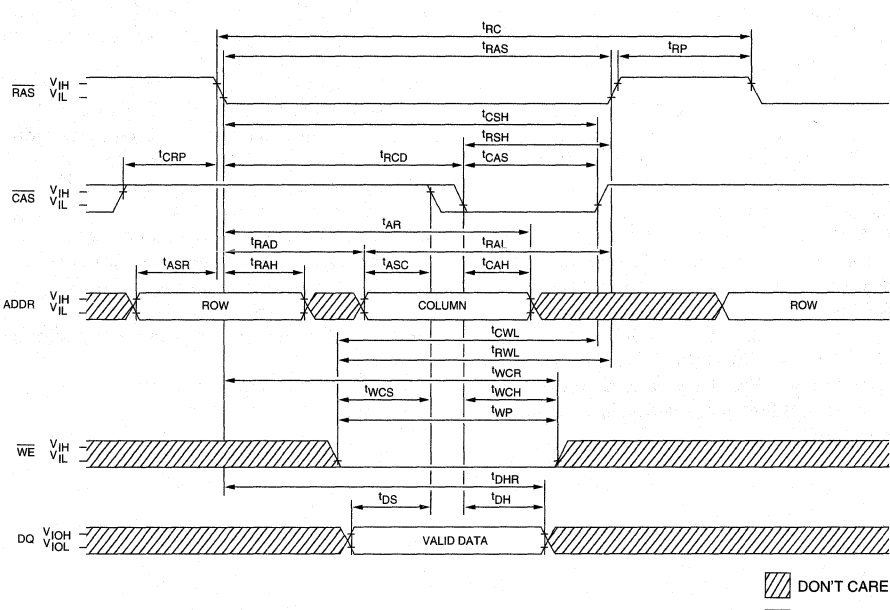
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM CARD

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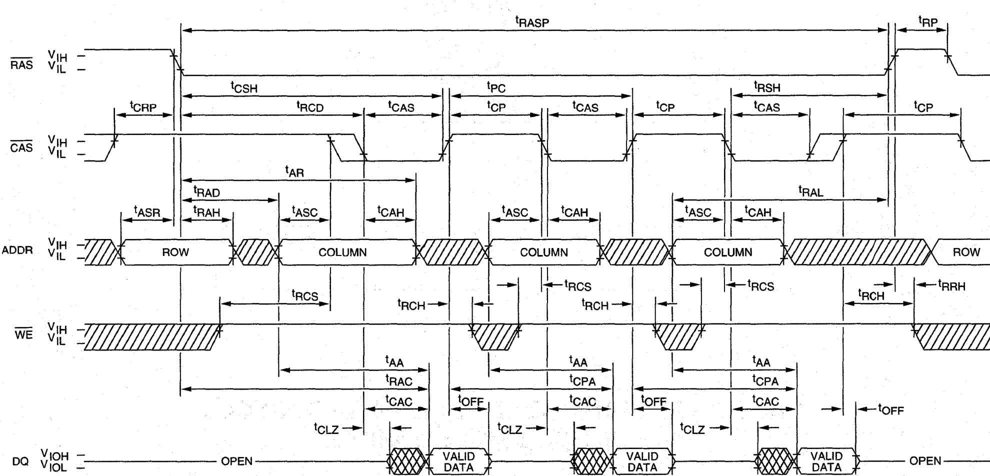
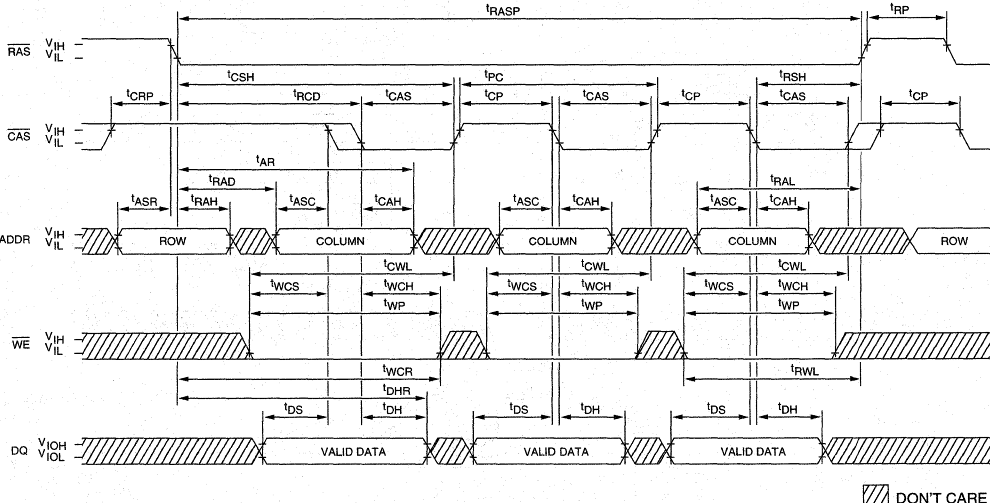
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM CARD

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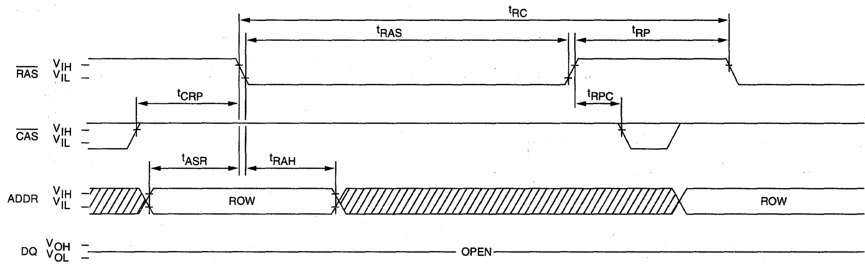
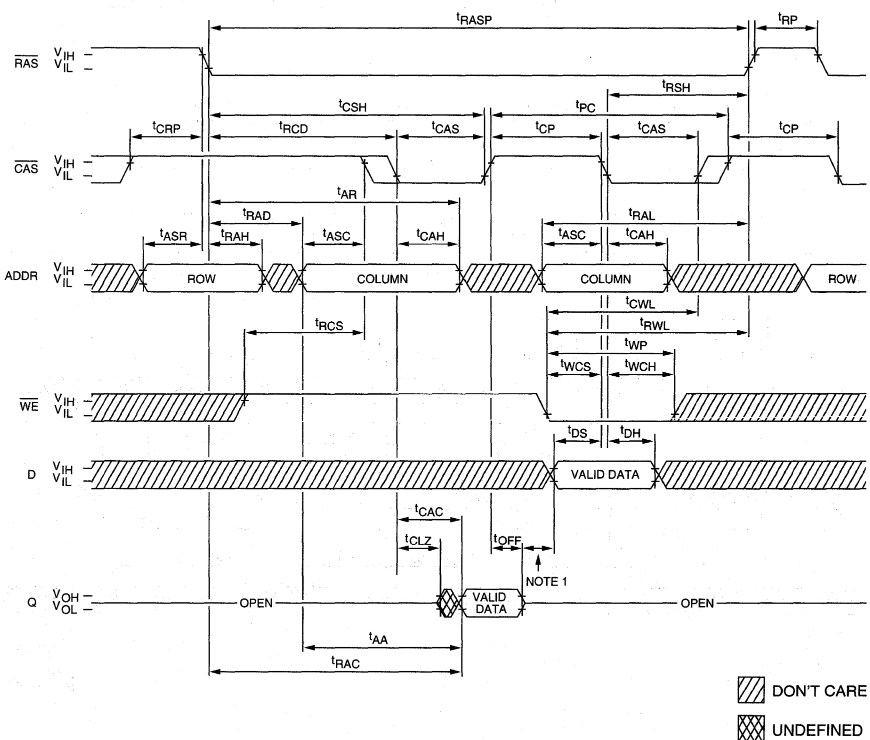
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
($\overline{\text{WE}}$ = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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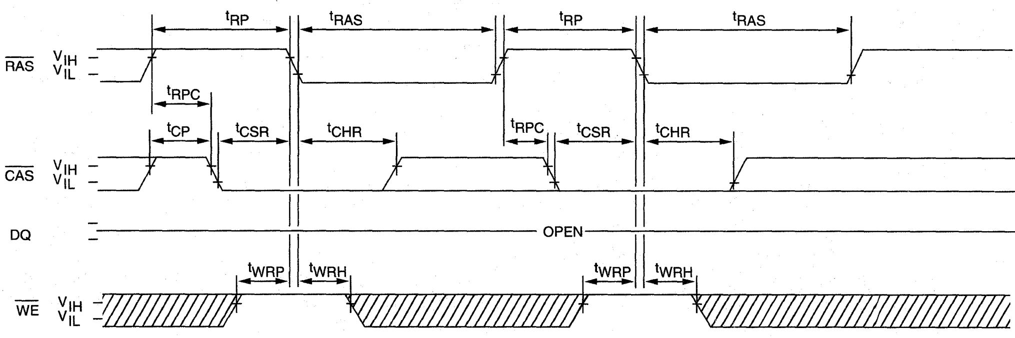
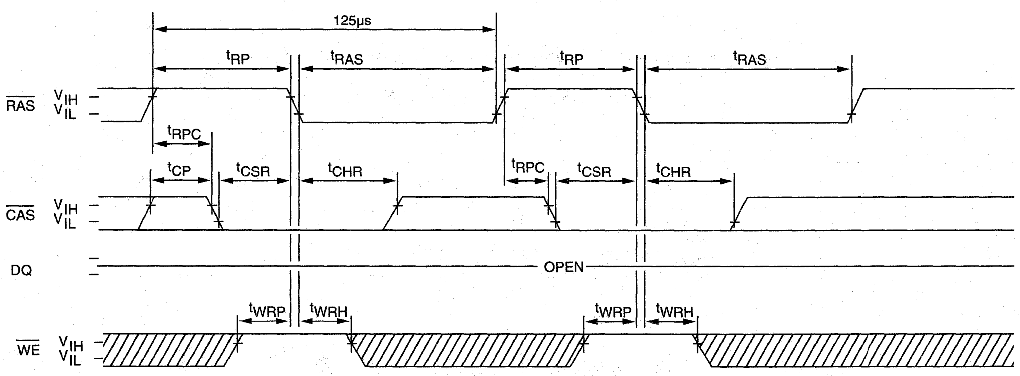
CBR REFRESH CYCLE
(Address = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(Address = DON'T CARE)



DON'T CARE

UNDEFINED

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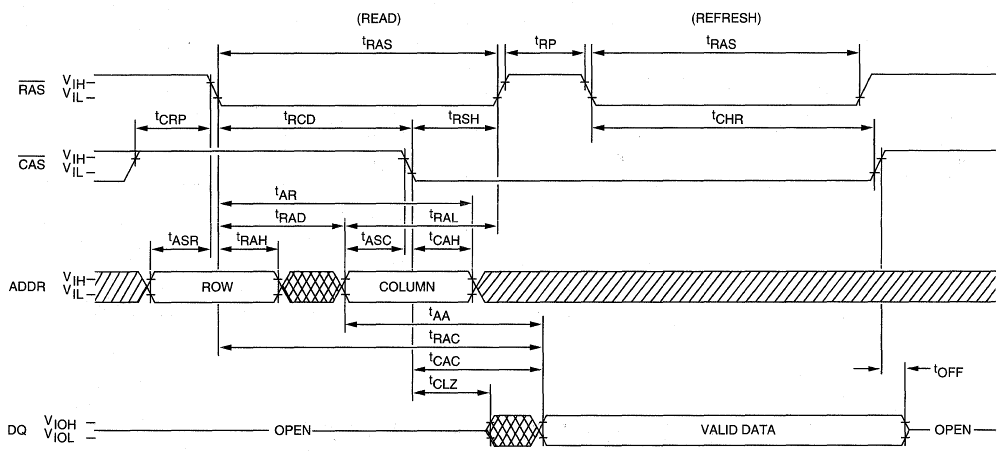
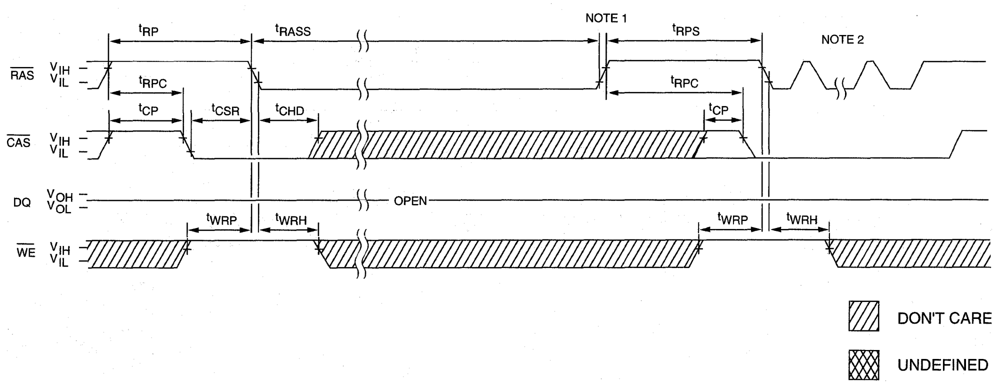
HIDDEN REFRESH CYCLE [21]
(WE = HIGH)



SELF REFRESH CYCLE (S VERSION ONLY)
(Addresses = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

DRAM CARD

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DRAM MINICARD 4, 8 MEGABYTES

1 MEG, 2 MEG x 32; 5V, FAST PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Low power
- JEDEC-standard 88-pin DRAM card pinout
- 2-inch (50.8mm)-long nonbuffered DRAM cards
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{\text{RAS}}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE (FPM) access cycle
- Single +5V ±5% power supply
- Extended Refresh

OPTIONS — MARKING

- Timing
  - 60ns access: -6
  - 70ns access: -7
- Refresh
  - Extended Refresh: Blank
  - SELF REFRESH: S

KEY TIMING PARAMETERS

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

VALID PART NUMBERS

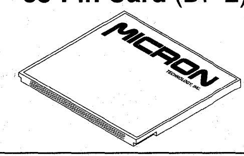
PART NUMBER	DESCRIPTION
MT8D88C132H-xx	1 Meg x 32
MT8D88C132H-xx S	1 Meg x 32, SELF REFRESH
MT16D88C232H-xx	2 Meg x 32
MT16D88C232H-xx S	2 Meg x 32, SELF REFRESH

GENERAL DESCRIPTION

The MT8D88C132H(S) and MT16D88C232H(S) comprise a family of DRAM cards organized in x32-bit memory arrays. These DRAM cards are 2-inch-long bufferless versions of the JEDEC-standard 3.37-inch (85.6mm), 88-pin x32 DRAM cards. Buffers are not included on these cards, so the on-board timing delays have been eliminated. Redrive circuitry may be implemented on the system board.

PIN ASSIGNMENT (End View)

88-Pin Card (DF-2)



44 — 1
88 — 45

PIN #	4MB	8MB	PIN #	4MB	8MB
1	Vss	→	45	Vss	→
2	DQ0	→	46	DQ16	→
3	DQ1	→	47	DQ17	→
4	DQ2	→	48	DQ18	→
5	DQ3	→	49	DQ19	→
6	DQ4	→	50	DQ20	→
7	DQ5	→	51	DQ21	→
8	DQ6	→	52	DQ22	→
9	Vcc	→	53	DQ23	→
10	DQ7	→	54	NC	→
11	NC	→	55	NC	→
12	NC	→	56	Vss	→
13	A0	→	57	A1	→
14	A2	→	58	A3	→
15	Vcc	→	59	A5	→
16	A4	→	60	A7	→
17	NC	→	61	A9	→
18	A6	→	62	NC	→
19	A8	→	63	Vss	→
20	NC	→	64	NC	→
21	NC	→	65	NC	$\overline{\text{RAS1}}$
22	$\overline{\text{RAS0}}$	→	66	$\overline{\text{CAS2}}$	→
23	$\overline{\text{CAS0}}$	→	67	Vss	→
24	$\overline{\text{CAS1}}$	→	68	$\overline{\text{CAS3}}$	→
25	NC	→	69	NC	$\overline{\text{RAS3}}$
26	$\overline{\text{RAS2}}$	→	70	$\overline{\text{WE}}$	→
27	Vcc	→	71	PD1	→
28	PD2	→	72	PD3	→
29	PD4	→	73	Vss	→
30	PD6	→	74	PD5	→
31	NC	→	75	PD7	→
32	NC	→	76	PD8	→
33	NC	→	77	NC	→
34	DQ8	→	78	NC	→
35	NC	→	79	NC	→
36	DQ9	→	80	DQ24	→
37	Vcc	→	81	DQ25	→
38	DQ10	→	82	DQ26	→
39	DQ11	→	83	DQ27	→
40	DQ12	→	84	DQ28	→
41	DQ13	→	85	DQ29	→
42	DQ14	→	86	DQ30	→
43	DQ15	→	87	DQ31	→
44	Vss	→	88	Vss	→

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GENERAL DESCRIPTION (continued)

These cards may also be configured as a x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{\text{CAS}}$ inputs allow byte accesses.

These MiniCards are designed for low-power operation using low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{\text{RAS}}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into 4 separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{\text{RAS}}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM Cards are built with 2-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132H)

$\overline{\text{RAS0}}$
$\overline{\text{CAS0}}$
$\overline{\text{CAS1}}$
$\overline{\text{CAS2}}$
$\overline{\text{CAS3}}$
$\overline{\text{RAS2}}$
$\overline{\text{WE}}$
ADDRESS
B1: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ — 8 — DQ0 … DQ7
B2: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ — 8 — DQ8 … DQ15
B3: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ — 8 — DQ16 … DQ23
B4: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ — 8 — DQ24 … DQ31

NOTE: 1. B1 through B4 = x8 memory blocks.

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FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232H)

NOTE: 1. B1 through B8 = x8 memory blocks.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	RAS0, RAS2 RAS1, RAS3	Input	Row-Address Strobe: RAS is used to latch the row-address. Two RAS inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	CAS0-CAS3	Input	Column-Address Strobe: CAS is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four CAS inputs allow byte access control for any memory bank configuration.
70	WE	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is a WRITE cycle. If WE is HIGH during the CAS LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A9	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	—	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 11, 12, 15, 17, 20, 21, 25, 27, 31, 32, 33, 35, 37, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	—	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. Pins 11, 17, 25, 35 reserved for 3.3V Vcc. Pin 55 reserved for x40 OE.
9, 15, 27, 37	Vcc	Supply	Power Supply: +5V ±5%
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

DRAM CARD

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FUNCTIONAL DESCRIPTION

The MT8D88C132H(S) and MT16D88C232H(S) comprise a family of DRAM cards organized in x32-bit memory arrays ($\overline{RAS0}$ = $\overline{RAS2}$). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both $\overline{RAS}$ lines.

Most x32-bit applications use the same signal to control the $\overline{CAS}$ inputs. $\overline{RAS0}$ and $\overline{RAS1}$ control the lower 16 bits and $\overline{RAS2}$ and $\overline{RAS3}$ control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and $\overline{CAS}$ pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each $\overline{RAS}$ is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, extended CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits, and $\overline{CAS}$ latches the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must fall prior to $\overline{CAS}$ (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by $\overline{WE}$.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS ($\approx$^{t}RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM MiniCards are constructed with a 2-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{\text{RAS}}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

Card Density	DRAM Organizations	# of Address	$\overline{\text{RAS}}$ Address	$\overline{\text{CAS}}$ Address	Page Depth	PDx 1	PDx 2	PDx 3	PDx 4	PDx 5	PDx 6	PDx 7	PDx 8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^tRAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1.0V to +7V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = +5V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.75	5.25	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	I_{I1}	-8	8	µA	
Any input: 0V ≤ V_{IN} ≤ 6.5V	A0-A9, $\overline{WE}$	I_{I2}	-10	10	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	I_{I3}	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ31	I_{OZ}	-20	20	µA	29
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5 mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2 mA)		V_{OL}		0.4	V	

DRAM CARD

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	4MB 8MB	880 896	800 816	mA	3, 4, 27
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB 8MB	16 32	16 32	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC3}	4MB 8MB	640 656	560 576	mA	3, 4, 27
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB 8MB	1.6 3.2	1.6 3.2	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB	880 896	800 816	mA	3, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB	880 896	800 816	mA	3, 5
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); ^tRC = 125µs; $\overline{WE}$ = Vcc-0.2V; A0-A9 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB 8MB	2.4 4.8	2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB 8MB	2.4 4.8	2.4 4.8	mA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX 4MB	MAX 8MB	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I1}	17	32	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	66	66	pF	2
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addresses	C_{I3}	51	90	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	^{t}AA		30		35	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	45		50		ns	
Column-address setup time	^{t}ASC	0		0		ns	
Row-address setup time	^{t}ASR	0		0		ns	
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20	ns	15
Column-address hold time	^{t}CAH	10		15		ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time entering SELF REFRESH	^{t}CHD	10		10		ns	28
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		ns	5
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	3		3		ns	26
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		ns	16
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		ns	5
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		ns	
Data-in hold time	^{t}DH	10		15		ns	24
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		ns	
Data-in setup time	^{t}DS	0		0		ns	24
Output buffer turn-off delay	^{t}OFF	3	15	3	20	ns	20, 26
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		ns	
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70	ns	14
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	ns	18
Row-address hold time	^{t}RAH	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	^{t}RASP	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ pulse width entering SELF REFRESH	^{t}RASS	100		100		µs	28

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +5V ±5%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	${}^tRC$	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	${}^tRCD$	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	${}^tRCH$	0		0		ns	19
Read command setup time	${}^tRCS$	0		0		ns	
Refresh period (1,024 cycles)	${}^tREF$		128		128	ms	
$\overline{RAS}$ precharge time	${}^tRP$	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	${}^tRPC$	0		0		ns	
$\overline{RAS}$ precharge time exiting SELF REFRESH	${}^tRPS$	110		130		ns	28
Read command hold time (referenced to $\overline{RAS}$)	${}^tRRH$	0		0		ns	19
$\overline{RAS}$ hold time	${}^tRSH$	15		20		ns	
Write command to $\overline{RAS}$ lead time	${}^tRWL$	15		20		ns	
Transition time (rise or fall)	${}^tT$	3	50	3	50	ns	
Write command hold time	${}^tWCH$	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	${}^tWCR$	45		55		ns	
$\overline{WE}$ command setup time	${}^tWCS$	0		0		ns	
Write command pulse width	${}^tWP$	10		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	${}^tWRH$	10		10		ns	22
$\overline{WE}$ setup time (CBR REFRESH)	${}^tWRP$	10		10		ns	22

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1. V_{CC} = +5V ±5%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS = V_{IH}, data output is High-Z.
12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
24. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
25. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being tied permanently LOW on all 4 Meg DRAMs.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
29. 4MB version is half of values shown.

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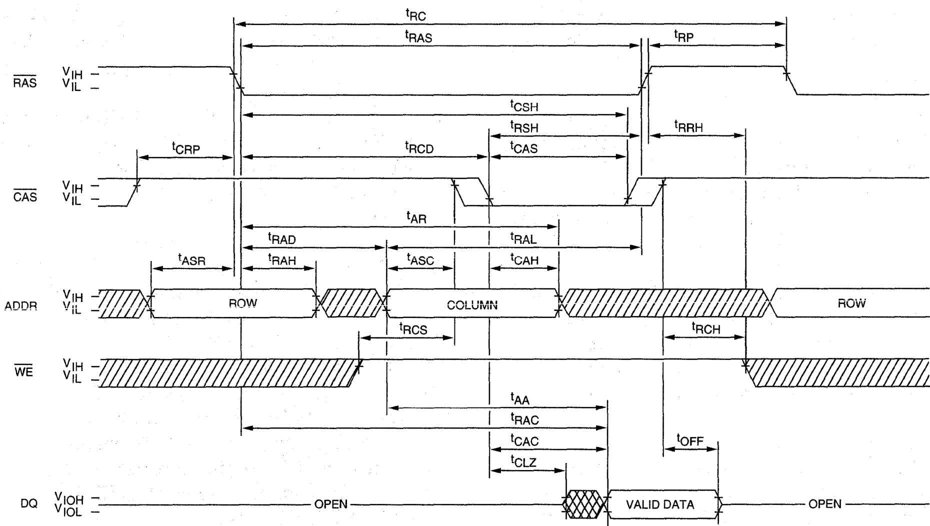
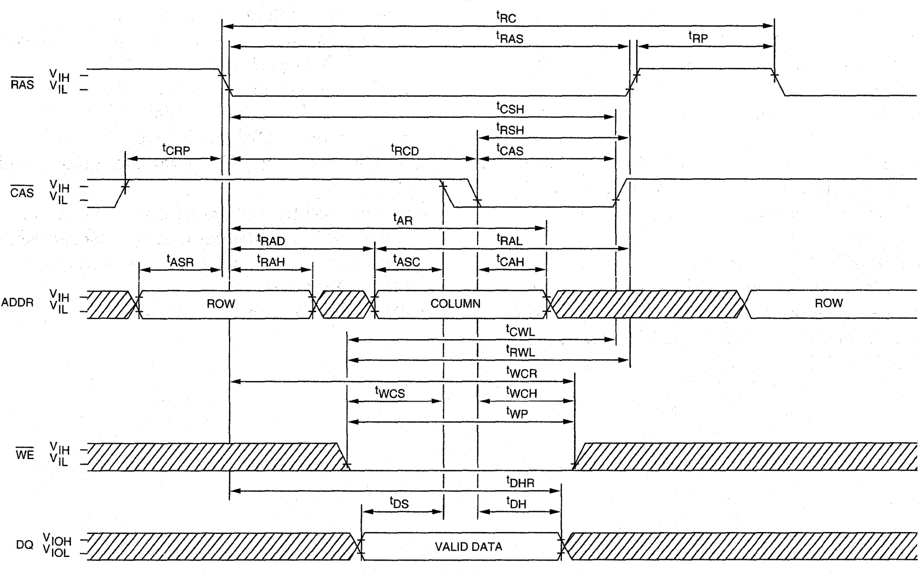
READ CYCLE



EARLY WRITE CYCLE



DRAM CARD

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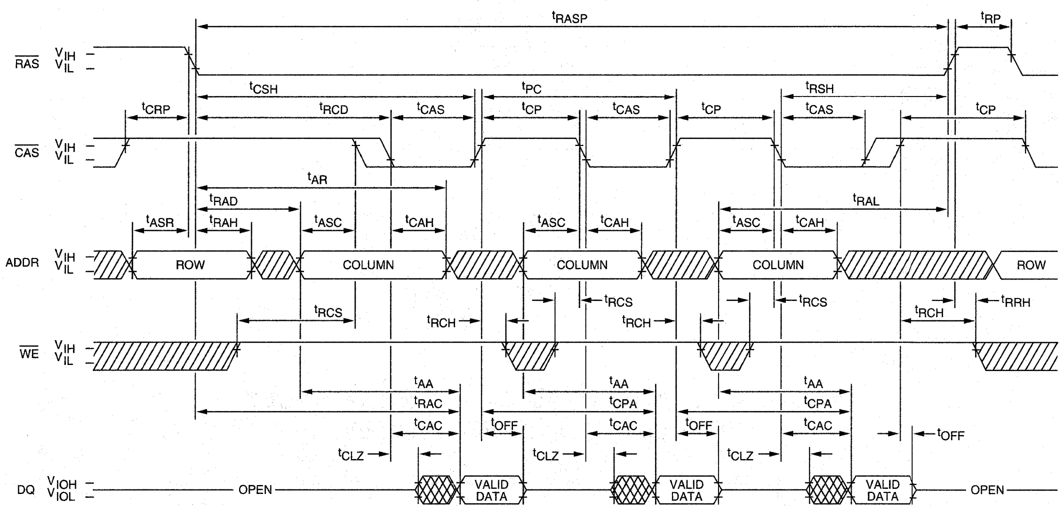
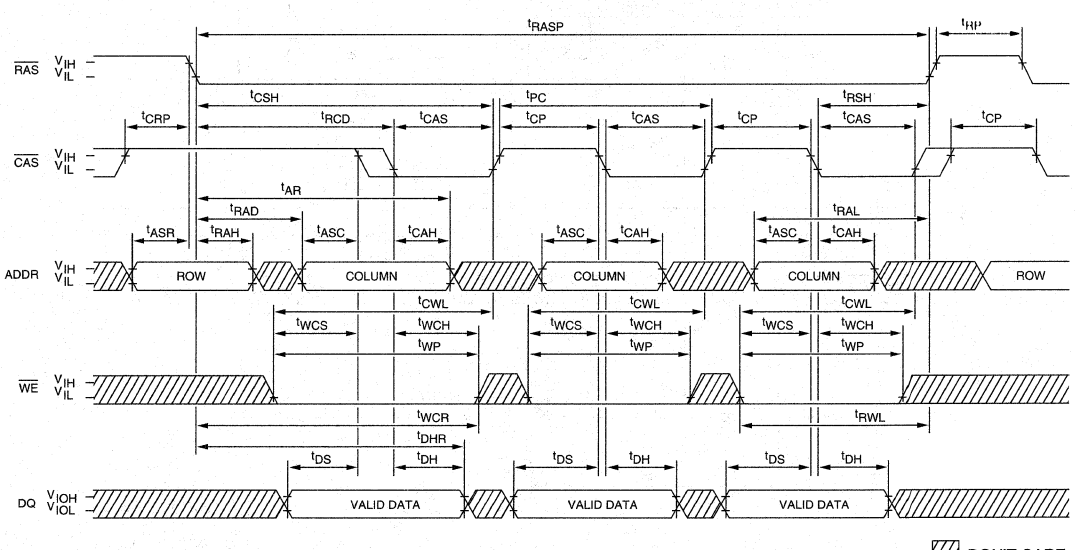
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

UNDEFINED

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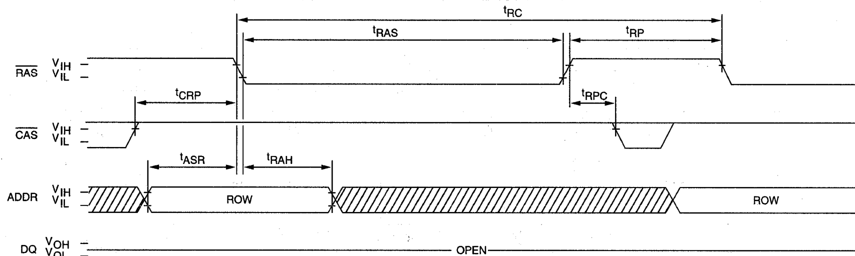
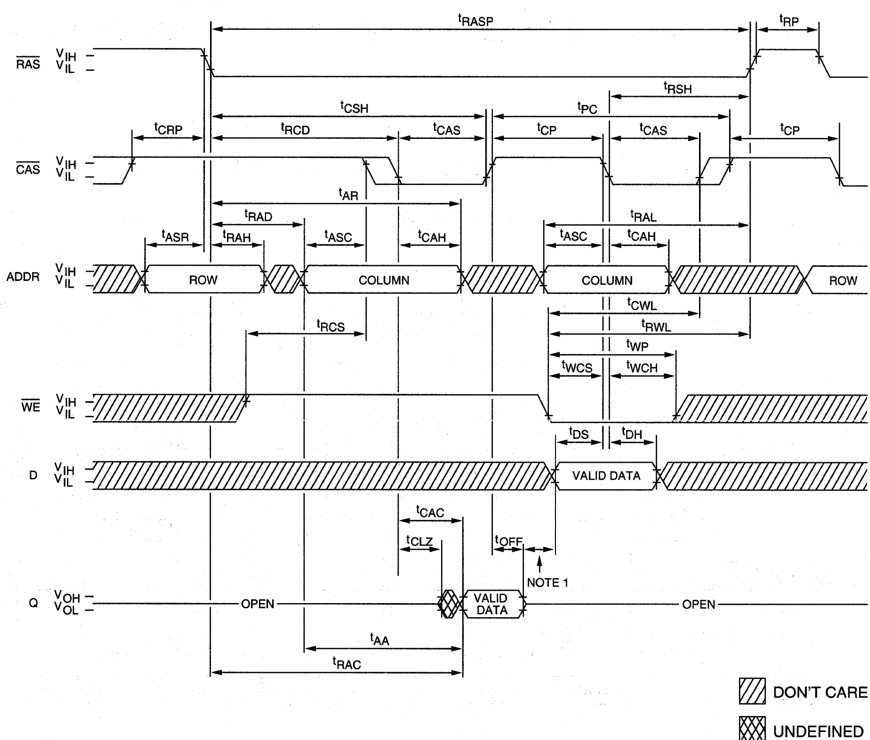
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

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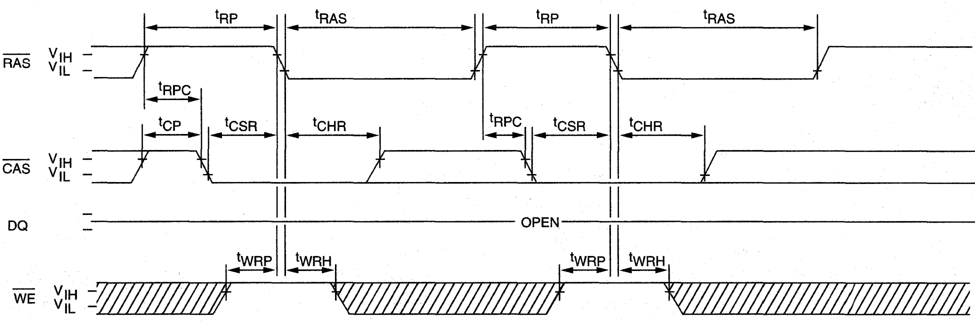
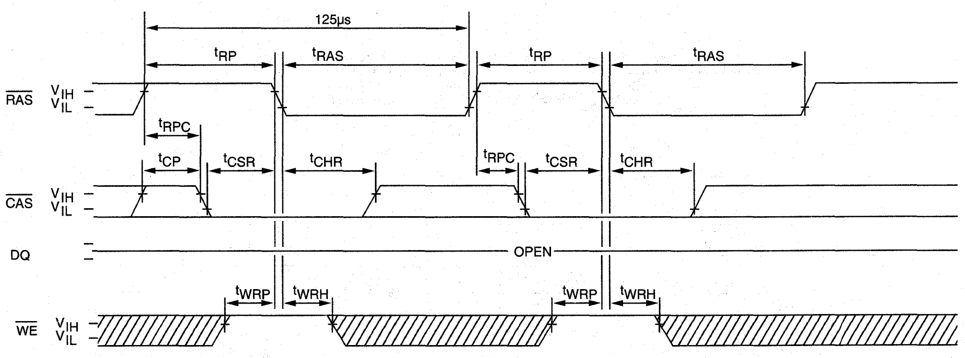
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(Addresses = DON'T CARE)



DON'T CARE

UNDEFINED

DRAM CARD

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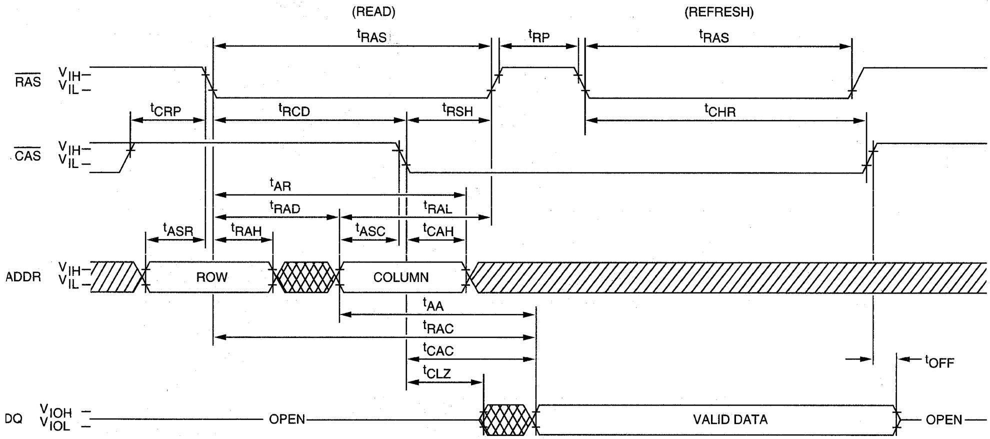
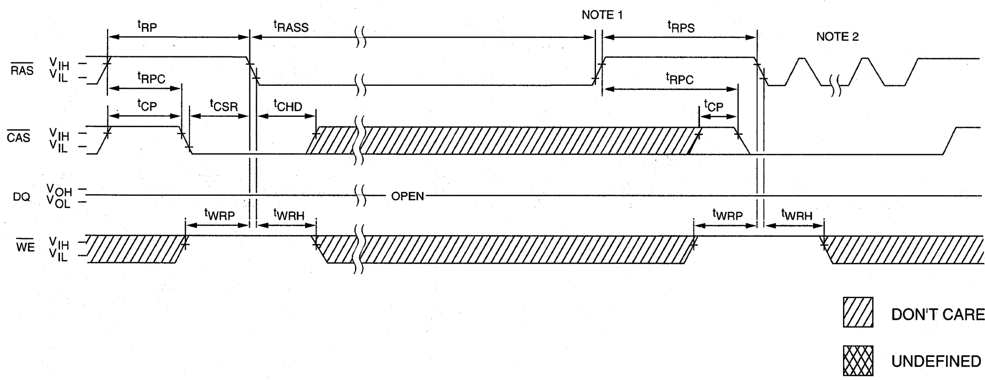
HIDDEN REFRESH CYCLE [21]
(WE = HIGH)



SELF REFRESH CYCLE (S VERSION ONLY)
(Addresses = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

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DRAM CARD

4, 8, 16*, 32* MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
3.3V, FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- JEDEC-standard 88-pin DRAM card
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- All inputs buffered except $\overline{RAS}$ inputs
- Multiple $\overline{RAS}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN; optional SELF REFRESH mode
- FAST PAGE MODE (FPM) access cycle
- Single +3.3V ±0.3V power supply
- Low power
- Extended Refresh

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	41ns	26ns	40ns
-7	130ns	70ns	40ns	46ns	31ns	50ns
-8	150ns	80ns	45ns	51ns	31ns	60ns

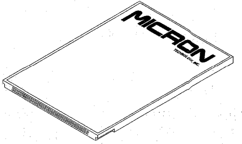
VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8D88C132V-xx	1 Meg x 32
MT8D88C132V-xx S	1 Meg x 32, SELF REFRESH
MT16D88C232V-xx	2 Meg x 32
MT16D88C232V-xx S	2 Meg x 32, SELF REFRESH
MT8D88C432V-xx	4 Meg x 32
MT8D88C432V-xx S	4 Meg x 32, SELF REFRESH
MT16D88C832V-xx	8 Meg x 32
MT16D88C832V-xx S	8 Meg x 32, SELF REFRESH

*Contact factory for availability.

PIN ASSIGNMENT (End View)

88-Pin Card (DF-3)



44 1
88 45

PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	NC	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	3.3V Vcc	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	NC	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	3.3V Vcc	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	$\overline{RAS1}$	NC	$\overline{RAS1}$
22	$\overline{RAS0}$	→	→	→	66	$\overline{CAS2}$	→	→	→
23	$\overline{CAS0}$	→	→	→	67	Vss	→	→	→
24	$\overline{CAS1}$	→	→	→	68	$\overline{CAS3}$	→	→	→
25	3.3V Vcc	→	→	→	69	NC	$\overline{RAS3}$	NC	$\overline{RAS3}$
26	$\overline{RAS2}$	→	→	→	70	$\overline{WE}$	→	→	→
27	NC	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	3.3V Vcc	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	NC	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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MT8D88C132V/432V(S), MT16D88C232V/832V(S) 4MB, 8MB, 16MB, 32MB DRAM CARDS

GENERAL DESCRIPTION

The MT8D88C132V/432V(S) and MT16D88C232V/832V(S) comprise a family of JEDEC-standard DRAM cards organized in x32-bit memory arrays. The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

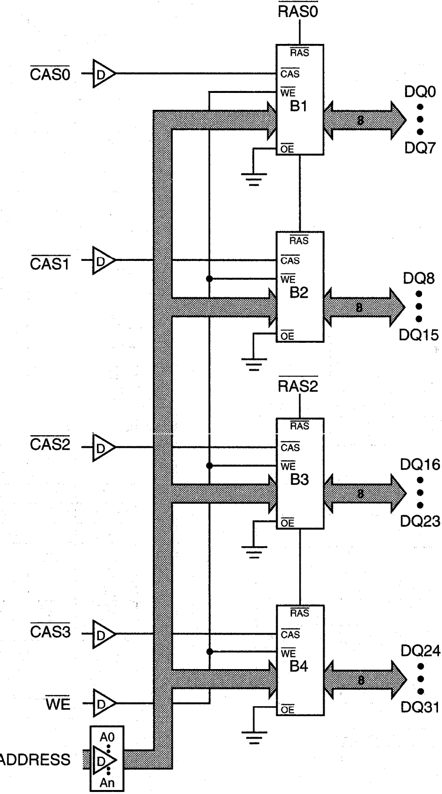
These 3.3V cards are designed for low-power operation using 3.3V, low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into four separate bytes. In the x16 organization, up to two banks, each with 2 separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM Cards are built with 3.370-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132V, 16MB - MT8D88C432V)



NOTE: 1. B1 through B4 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232V, 32MB - MT16D88C832V)

RAS0 RAS1
CAS0 CAS1 CAS2 CAS3
RAS2 RAS3
B1 B2 B3 B4 B5 B6 B7 B8
DQ0 • • • DQ7
DQ8 • • • DQ15
DQ16 • • • DQ23
DQ24 • • • DQ31
WE
ADDRESS A0 • • An

NOTE: 1. B1 through B8 = x8 memory blocks.
2. D = 74AC11244 line drivers.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0}$-$\overline{CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	—	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 12, 15, 21, 27, 31, 32, 33, 37, 54, 55, 62, 64, 65, 69, 77, 78, 79	NC	—	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. PIns 9, 15, 27, 37 reserved for 5V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
11, 17, 25, 35	Vcc	Supply	Power Supply: +3.3V ±0.3V
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

The MT8D88C132V/432V(S) and MT16D88C232V/832V(S) comprise a family of DRAM cards organized in x32-bit memory arrays (RAS0 = RAS2). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32-bit applications use the same signal to control the CAS inputs. RAS0 and RAS1 control the lower 16 bits and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and CAS pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, extended CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9/A10) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (I_{CC7}).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. RAS is used to latch the first 10/11 bits, and CAS latches the latter 10/11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx ^{t}$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron 3.3V DRAM Cards are constructed with a 3.370-inch long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^{t}R	ADDRESSES ^{t}C	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{RAS}$ Address	$\overline{CAS}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^{t}RAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +4.5V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) ($0°C \le T_A \le 55°C$; Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.15	3.45	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.1	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input: 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V) for each package input	$\overline{RAS0}$-$\overline{RAS3}$	II1	-8	8	µA	
	Buffered	II2	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) for each package input	DQ0-DQ31	IOZ	-20	20	µA	35
OUTPUT LEVELS Output High Voltage (IOUT = -2.0 mA)		VOH	2.0		V	
Output Low Voltage (IOUT = 2.0 mA)		VOL		0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC1}	4MB	640	560	480	mA	3, 4, 30
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB	8	8	8	mA	
		8MB	16	16	16		
		16MB	8	8	-		
		32MB	16	16	-		
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ${}^tPC$ = ${}^tPC$ [MIN])	I_{CC3}	4MB	480	400	320	mA	3, 4, 30
		8MB	488	408	328		
		16MB	720	640	-		
		32MB	728	648	-		
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC4}	4MB	4	4	4	mA	
		8MB	8	8	8		
		16MB	4	4	-		
		32MB	8	8	-		
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC5}	4MB	640	560	480	mA	3, 30
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ${}^tRC$ = ${}^tRC$ [MIN])	I_{CC6}	4MB	640	560	480	mA	3, 5
		8MB	648	568	488		
		16MB	960	880	-		
		32MB	968	888	-		
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ${}^tRAS$ (MIN); ${}^tRC$ = 125µs; $\overline{WE}$ = V_{CC} -0.2V; A0-A10 and DQ = V_{CC} -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB	1.2	1.2	1.2	mA	3, 5
		8MB	2.4	2.4	2.4		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ${}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC}-0.2V; A0-A10 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB	1.2	1.2	1.2	mA	5, 31
		8MB	2.4	2.4	2.4		
		16MB	2.4	2.4	2.4		
		32MB	4.8	4.8	4.8		

CAPACITANCE

PARAMETER	SYMBOL	MAX 4,16MB	MAX 8, 32MB	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I1}	9	9	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	13	13	pF	2
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addresses	C_{I3}	9	9	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		41		46		51	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		53		ns	24
Column-address setup time	^tASC	2		2		2		ns	23
Row-address setup time	^tASR	7		7		7		ns	25
Access time from $\overline{CAS}$	^tCAC		26		31		31	ns	15, 25
Column-address hold time	^tCAH	10		15		15		ns	25
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time entering SELF REFRESH	^tCHD	15		15		15		ns	31
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	13		13		13		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		5		ns	23, 32
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		46		51		56	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	21		21		21		ns	25
$\overline{CAS}$ hold time	^tCSH	58		68		78		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	12		12		12		ns	5, 23
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		20		ns	
Data-in hold time	^tDH	21		26		26		ns	25
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		60		ns	
Data-in setup time	^tDS	-2		-2		-2		ns	24
Output buffer turn-off delay	^tOFF	5	26	5	31	5	31	ns	20, 27, 32
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from RAS	tRAC		60		70		80	ns	14
RAS to column-address delay time	tRAD	13	19	13	24	13	29	ns	18, 26
Row-address hold time	tRAH	8		8		8		ns	24
Column-address to RAS lead time	tRAL	41		46		51		ns	25
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width entering SELF REFRESH	tRASS	100		100		100		µs	31
Random READ or WRITE cycle time	tRC	110		130		150		ns	
RAS to CAS delay time	tRCD	18	34	18	39	18	49	ns	17, 26
Read command hold time (referenced to CAS)	tRCH	2		2		2		ns	19, 23
Read command setup time	tRCS	2		2		2		ns	23
Refresh period (1,024 cycles)	tREF		128		128		128	ms	34
Refresh period (2,048 cycles)	tREF		128		128		128	ms	33
RAS precharge time	tRP	40		50		60		ns	
RAS to CAS precharge time	tRPC	0		0		0		ns	
RAS precharge time exiting SELF REFRESH	tRPS	110		130		150		ns	31
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
RAS hold time	tRSH	26		31		31		ns	25
Write command to RAS lead time	tRWL	26		31		31		ns	25
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	
Write command hold time	tWCH	21		26		26		ns	25
Write command hold time (referenced to RAS)	tWCR	43		53		58		ns	24
WE command setup time	tWCS	2		2		2		ns	23
Write command pulse width	tWP	10		15		15		ns	
WE hold time (CBR REFRESH)	tWRH	8		8		8		ns	22, 24
WE setup time (CBR REFRESH)	tWRP	12		12		12		ns	22, 23

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V ±0.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
25. A +11ns timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
26. A -2ns (MIN) and a -11ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
27. A +2ns (MIN) and a +11ns (MAX) timing skew from the DRAM to the DRAM card resulted from the addition of line drivers.
28. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
30. Column-address changed once each cycle.
31. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
32. The 3ns minimum is a parameter guaranteed by design.
33. 16MB and 32MB only.
34. 4MB and 8MB only.
35. 4MB is half of values shown.

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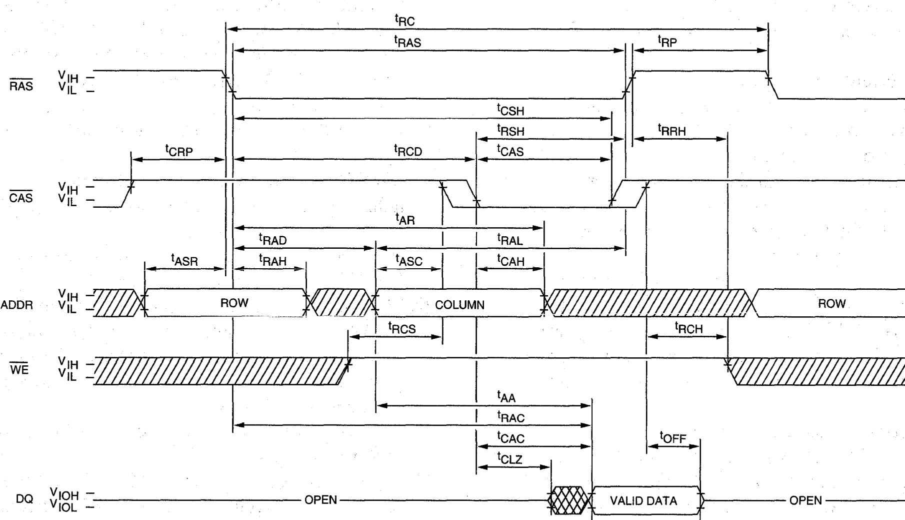
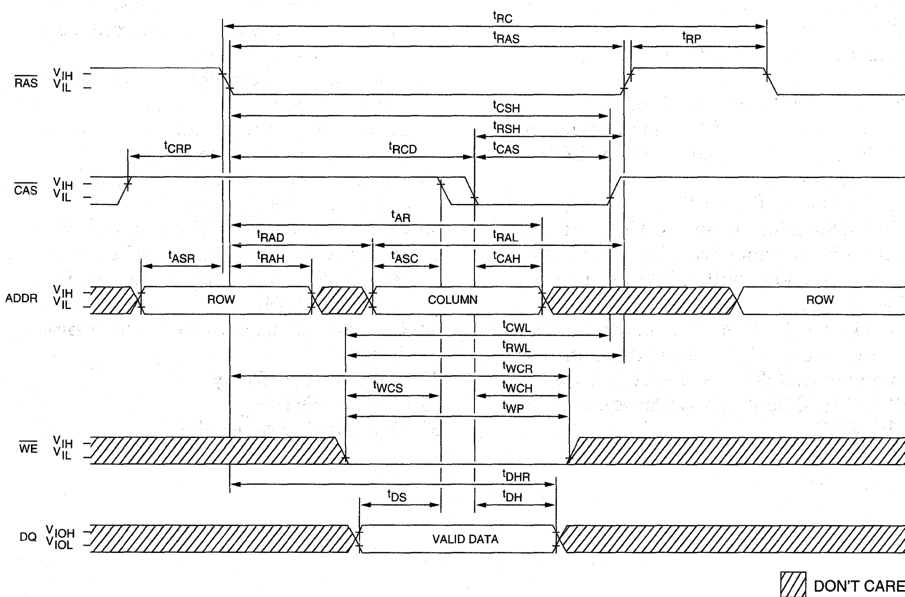
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

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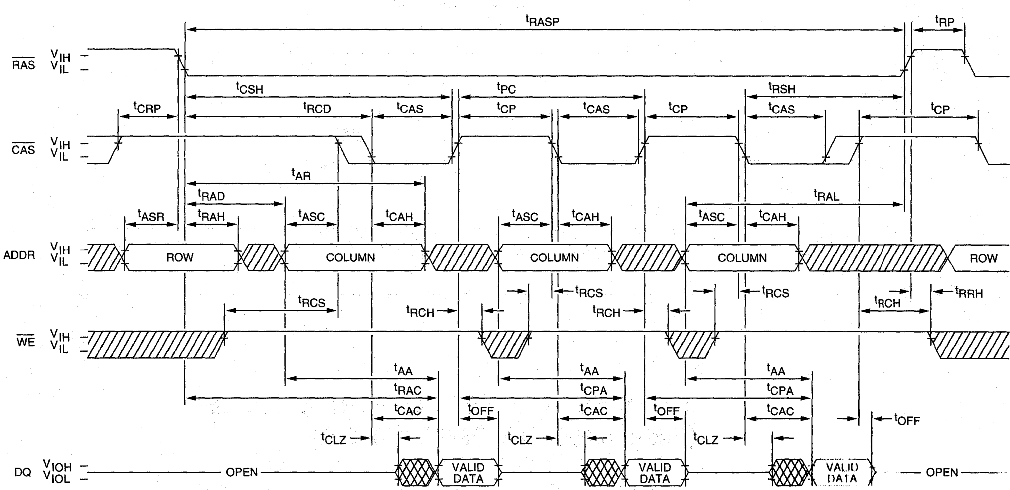
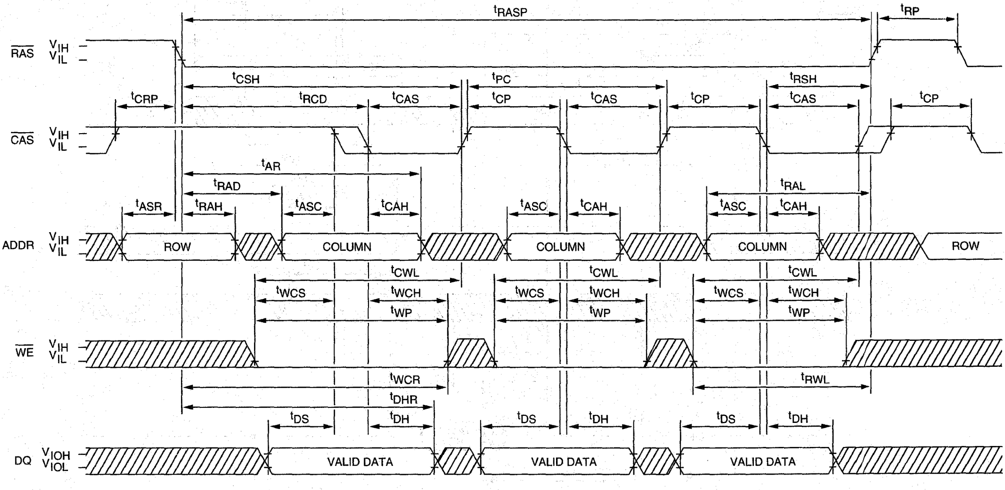
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DON'T CARE

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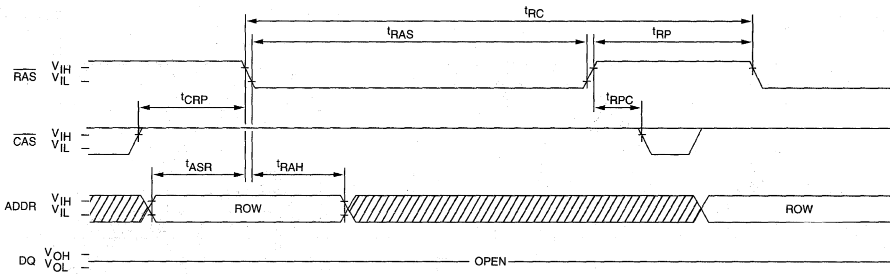
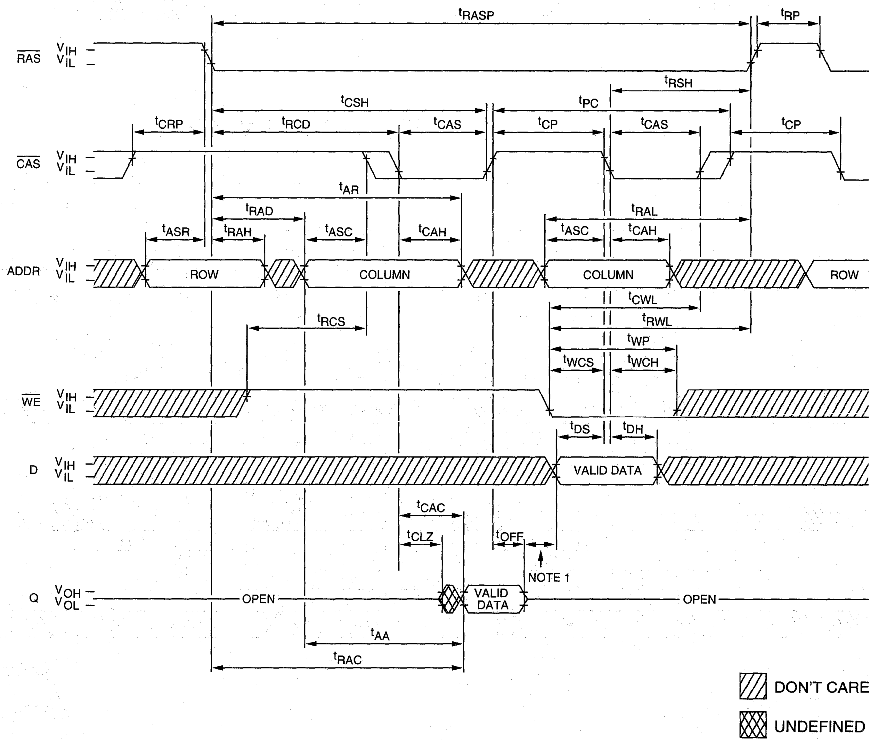
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

DRAM CARD

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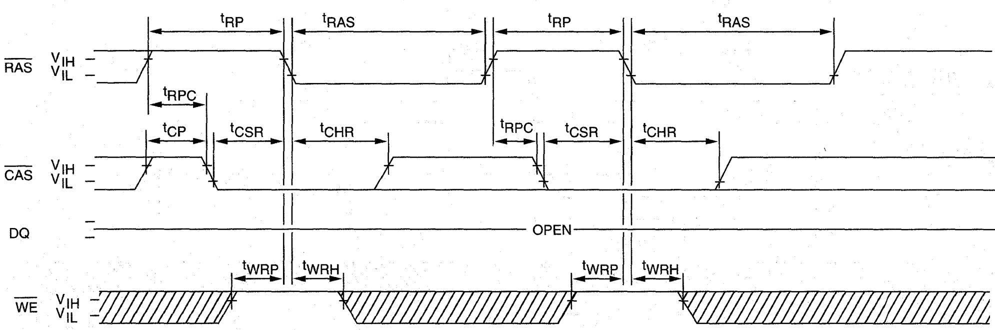
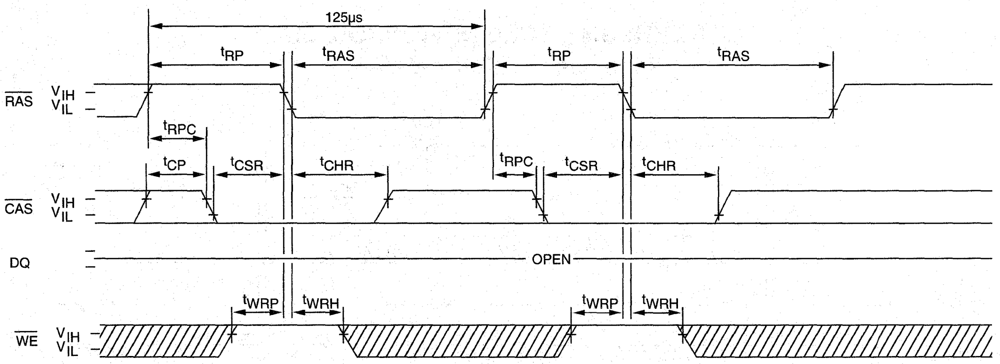
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(Addresses = DON'T CARE)



DON'T CARE

UNDEFINED

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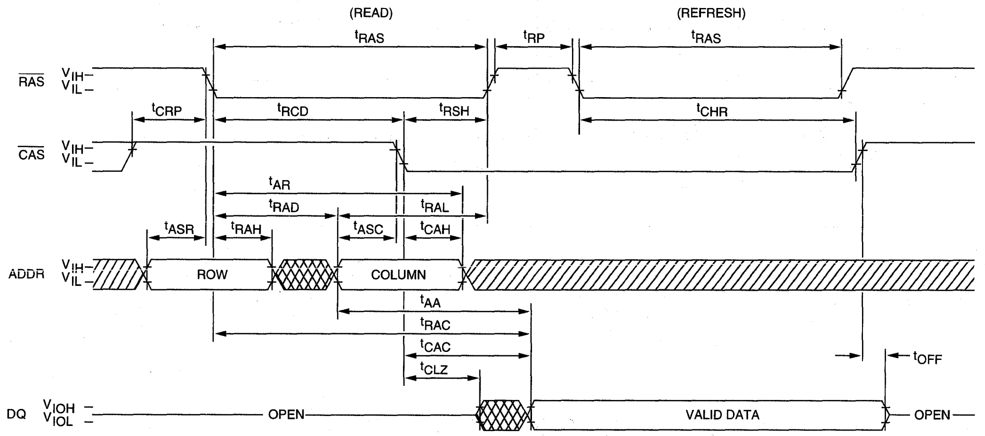
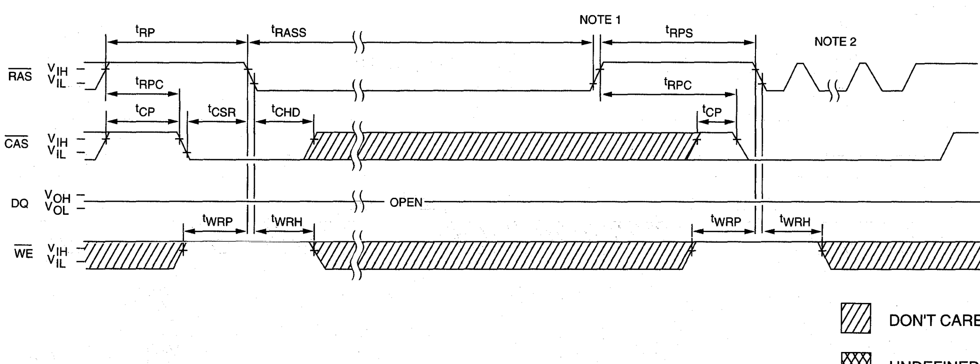
HIDDEN REFRESH CYCLE [21]

($\overline{WE}$ = HIGH)



SELF REFRESH CYCLE (S VERSION ONLY)

(Addresses = DON'T CARE)



NOTE: 1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.

DRAM CARD

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DRAM MINICARD

4, 8, 16*, 32* MEGABYTES

1 MEG, 2 MEG, 4 MEG, 8 MEG x 32;
3.3V, FAST PAGE MODE,
OPTIONAL SELF REFRESH

FEATURES

- JEDEC-standard 88-pin DRAM card pinout
- 2-inch (50.8mm)-long nonbuffered DRAM cards
- Polarized receptacle connector
- Industry-standard DRAM FAST PAGE MODE operation
- High reliability, gold-plated connector
- All outputs fully TTL-compatible
- Multiple $\overline{\text{RAS}}$ inputs for x16 or x32 selectability
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN; optional SELF REFRESH
- FAST PAGE MODE (FPM) access cycle
- Single +3.3V ±0.3V power supply
- Low power
- Extended Refresh

OPTIONS

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
80ns access	-8
• Refresh	
Extended Refresh	Blank
SELF REFRESH	S

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	20ns	60ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT8D88C132VH-xx	1 Meg x 32
MT8D88C132VH-xx S	1 Meg x 32, SELF REFRESH
MT16D88C232VH-xx	2 Meg x 32
MT16D88C232VH-xx S	2 Meg x 32, SELF REFRESH
MT8D88C432VH-xx	4 Meg x 32
MT8D88C432VH-xx S	4 Meg x 32, SELF REFRESH
MT16D88C832VH-xx	8 Meg x 32
MT16D88C832VH-xx S	8 Meg x 32, SELF REFRESH

*Contact factory for availability.

PIN ASSIGNMENT (End View)
88-Pin Card (DF-4)

PIN #	4MB	8MB	16MB	32MB	PIN #	4MB	8MB	16MB	32MB
1	Vss	→	→	→	45	Vss	→	→	→
2	DQ0	→	→	→	46	DQ16	→	→	→
3	DQ1	→	→	→	47	DQ17	→	→	→
4	DQ2	→	→	→	48	DQ18	→	→	→
5	DQ3	→	→	→	49	DQ19	→	→	→
6	DQ4	→	→	→	50	DQ20	→	→	→
7	DQ5	→	→	→	51	DQ21	→	→	→
8	DQ6	→	→	→	52	DQ22	→	→	→
9	NC	→	→	→	53	DQ23	→	→	→
10	DQ7	→	→	→	54	NC	→	→	→
11	3.3V Vcc	→	→	→	55	NC	→	→	→
12	NC	→	→	→	56	Vss	→	→	→
13	A0	→	→	→	57	A1	→	→	→
14	A2	→	→	→	58	A3	→	→	→
15	NC	→	→	→	59	A5	→	→	→
16	A4	→	→	→	60	A7	→	→	→
17	3.3V Vcc	→	→	→	61	A9	→	→	→
18	A6	→	→	→	62	NC	→	→	→
19	A8	→	→	→	63	Vss	→	→	→
20	NC	→	A10	→	64	NC	→	→	→
21	NC	→	→	→	65	NC	$\overline{\text{RAS1}}$	NC	$\overline{\text{RAS1}}$
22	$\overline{\text{RAS0}}$	→	→	→	66	$\overline{\text{CAS2}}$	→	→	→
23	$\overline{\text{CAS0}}$	→	→	→	67	Vss	→	→	→
24	$\overline{\text{CAS1}}$	→	→	→	68	$\overline{\text{CAS3}}$	→	→	→
25	3.3V Vcc	→	→	→	69	NC	$\overline{\text{RAS3}}$	NC	$\overline{\text{RAS3}}$
26	$\overline{\text{RAS2}}$	→	→	→	70	$\overline{\text{WE}}$	→	→	→
27	NC	→	→	→	71	PD1	→	→	→
28	PD2	→	→	→	72	PD3	→	→	→
29	PD4	→	→	→	73	Vss	→	→	→
30	PD6	→	→	→	74	PD5	→	→	→
31	NC	→	→	→	75	PD7	→	→	→
32	NC	→	→	→	76	PD8	→	→	→
33	NC	→	→	→	77	NC	→	→	→
34	DQ8	→	→	→	78	NC	→	→	→
35	3.3V Vcc	→	→	→	79	NC	→	→	→
36	DQ9	→	→	→	80	DQ24	→	→	→
37	NC	→	→	→	81	DQ25	→	→	→
38	DQ10	→	→	→	82	DQ26	→	→	→
39	DQ11	→	→	→	83	DQ27	→	→	→
40	DQ12	→	→	→	84	DQ28	→	→	→
41	DQ13	→	→	→	85	DQ29	→	→	→
42	DQ14	→	→	→	86	DQ30	→	→	→
43	DQ15	→	→	→	87	DQ31	→	→	→
44	Vss	→	→	→	88	Vss	→	→	→

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GENERAL DESCRIPTION

The MT8D88C132VH/432VH(S), MT16D88C232VH/832VH(S) comprise a family of DRAM cards organized in x32-bit memory arrays. These DRAM cards are 2-inch-long bufferless versions of the JEDEC-standard 3.37-inch (85.6mm), 88-pin x32 DRAM cards. Buffers are not included on these cards, so the on-board timing delays have been eliminated. Redrive circuitry may be implemented on the system board.

The cards may also be configured as x16-bit memory arrays, provided the corresponding DQs on the host system are made common, and memory bank control procedures are implemented. Four separate $\overline{CAS}$ inputs allow byte accesses.

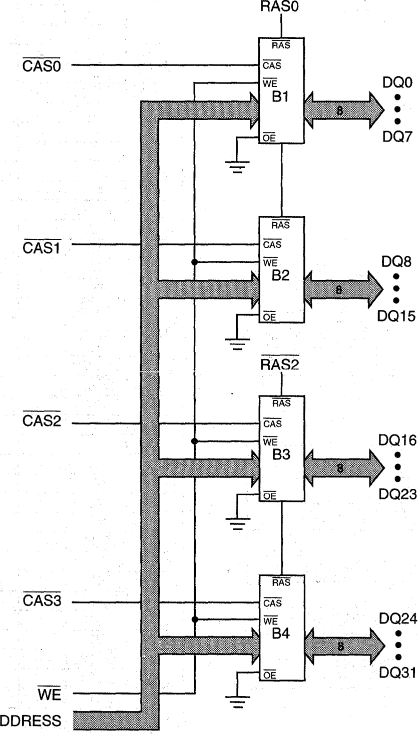
These 3.3V MiniCards are designed for low-power operation using 3.3V, low-power, extended refresh DRAMs. Standard component DRAM refresh modes are supported as well.

Multiple $\overline{RAS}$ inputs conserve power by allowing individual bank selection. In the x32 organization, the memory is a single array that may be divided into 4 separate bytes. In the x16 organization, up to two banks, each with two separate bytes, may be independently selected. One bank is activated by each $\overline{RAS}$ selection; the others not selected remain in standby mode, drawing minimum power.

Eight presence-detect pins may be read by the host to identify the card's organization, number of banks, access time and refresh operation. These extensive presence-detect functions allow systems to take full advantage of the advanced power-saving features.

These Micron DRAM Cards are built with 2-inch-long static dissipative plastic frames covered by metal panels. Packages containing 88-pin receptacle connectors are keyed to prevent improper installation or insertion into other types of IC card sockets.

FUNCTIONAL BLOCK DIAGRAM
(4MB - MT8D88C132VH, 16MB - MT8D88C432VH)



NOTE: 1. B1 through B4 = x8 memory blocks.

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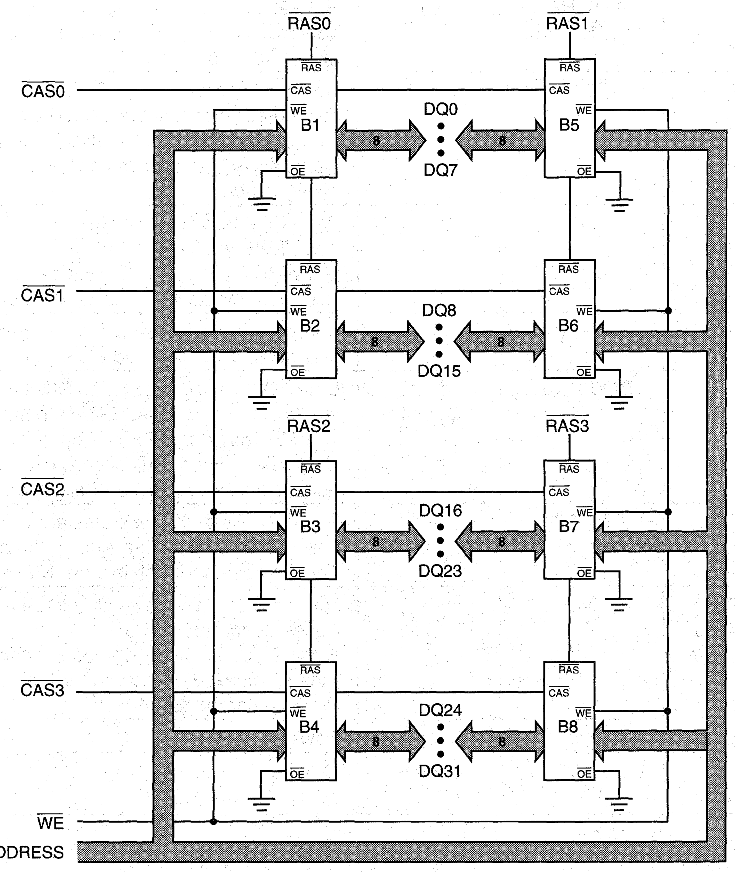
FUNCTIONAL BLOCK DIAGRAM
(8MB - MT16D88C232VH, 32MB - MT16D88C832VH)



NOTE: 1. B1 through B8 = x8 memory blocks.

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
22, 26, 65, 69	$\overline{RAS0}$, $\overline{RAS2}$ $\overline{RAS1}$, $\overline{RAS3}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to latch the row-address. Two $\overline{RAS}$ inputs allow for a single x32 bank or two x16 banks.
23, 24, 66, 68	$\overline{CAS0}$-$\overline{CAS3}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to latch the column-address, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Four $\overline{CAS}$ inputs allow byte access control for any memory bank configuration.
70	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is a WRITE cycle. If $\overline{WE}$ is HIGH during the $\overline{CAS}$ LOW transition, the access is a READ cycle.
13, 57, 14, 58, 16, 59, 18, 60, 19, 61, 20	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$.
2-8, 10, 34, 36, 38-43, 46-53, 80-87	DQ0-DQ31	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ31 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding $\overline{CAS}$ select. For READ access cycles, DQ0-DQ31 act as outputs for the addressed DRAM location.
71, 28, 72, 29, 74, 30, 75, 76	PD1-PD8	—	Presence-Detect: These pins are read by the host system and tell the system the card's personality. They will be either left floating (NC) or grounded (Vss).
9, 12, 15, 21, 27, 31, 32, 33, 37, 54, 55, 62, 64, 65, 69, 77, 78 79	NC	—	No Connect: These pins should be left unconnected (reserved for future use). Pins 12, 31-33, 54, 77-79 reserved for x36/x40 DQs. Pins 9, 15, 27, 37 reserved for 5V Vcc. Pin 55 reserved for x40 $\overline{OE}$.
11, 17, 25, 35	Vcc	Supply	Power Supply: +3.3V ±0.3V
1, 44, 45, 56, 63, 67, 73, 88	Vss	Supply	Ground

DRAM CARD

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FUNCTIONAL DESCRIPTION

The MT8D88C132VH/432VH(S), MT16D88C232VH/832VH(S) comprise a family of DRAM cards organized in x32-bit memory arrays (RAS0 = RAS2). They also may be configured as x16-bit memory arrays provided the corresponding DQs on the host are connected and memory bank control procedures are implemented by interleaving both RAS lines.

Most x32-bit applications use the same signal to control the CAS inputs. RAS0 and RAS1 control the lower 16 bits and RAS2 and RAS3 control the upper 16 bits to obtain a x32 memory array. For x16 applications, the corresponding DQ and CAS pins must be connected (DQ0 to DQ15, DQ1 to DQ16 and so forth, CAS0 to CAS2 and CAS1 to CAS3). Each RAS is then a bank select for the x16 memory organizations.

DRAM OPERATION

DRAM REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or RAS refresh cycle (RAS ONLY, CBR, extended CBR or HIDDEN) so that all combinations of RAS addresses (A0-A9, A10) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS addressing.

The implied method of choice for refreshing the memory card is the extended CBR cycle. This is a very low-current, data retention mode made possible by using the CBR REFRESH cycle over the extended refresh range (Icc7).

The memory card may be used with the other refresh modes common to standard DRAMs. This allows the memory card to be used on existing systems that do not utilize the extended CBR REFRESH cycle. However, the memory card will draw more current in the standby mode.

DRAM READ AND WRITE CYCLES

During READ or WRITE cycles, each bit is uniquely addressed through the 20/22 address bits, which are entered 10/11 bits (A0-A9/A10) at a time. RAS is used to latch the first 10/11 bits, and CAS latches the latter 10/11 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS. WE must fall prior to CAS (EARLY WRITE). The data inputs and data outputs are routed through pins using common I/O and pin direction is controlled by WE.

FAST PAGE MODE operation allows faster data operations (READ or WRITE) within a row-address-defined (A0-A9/A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST PAGE MODE operation. Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS HIGH time.

REFRESH

An optional SELF REFRESH mode is also available. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period.

The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle and holding RAS LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh rate of 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation or during a standby mode.

The SELF REFRESH mode is terminated by driving RAS HIGH for a minimum time of ^{t}RPS ($\approx{}^t$RC). This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes RAS ONLY or burst refresh sequence, all rows must be refreshed within 300µs prior to the resumption of normal operation.

PHYSICAL DESIGN

These Micron DRAM MiniCards are constructed with a 2-inch-long static dissipative plastic frame covered by metal panels. Inside, thin small-outline package (TSOP) DRAMs are mounted on an ultrathin printed circuit board. The board is attached to a high-insertion, 88-pin receptacle connector. The package is keyed to prevent improper installation, including insertion into other types of IC card sockets. The DRAM cards operate reliably up to 55°C.

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MEMORY TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA IN/OUT DQ0-DQ31
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
READ WRITE		L	L	H→L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H→L	n/a	COL	Data-Out
$\overline{RAS}$-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	High-Z

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS						PRESENCE-DETECT PIN (PDx)							
Card Density	DRAM Organizations	# of Address	$\overline{RAS}$ Address	$\overline{CAS}$ Address	Page Depth	1	2	3	4	5	6	7	8
0MB	No card installed	X	X	X	X	NC	NC	NC	NC	NC			
1MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	NC			
2MB	256K x 4 or x16	18	9	9	512	Vss	Vss	Vss	Vss	Vss			
2MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	NC			
4MB	512K x 8	19	10	9	512	NC	Vss	Vss	Vss	Vss			
•4MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	NC			
•8MB	1 Meg x 4 or x16	20	10	10	1,024	Vss	NC	Vss	Vss	Vss			
8MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	NC			
16MB	2 Meg x 8	21	11	10	1,024	NC	NC	Vss	Vss	Vss			
•16MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	NC			
•32MB	4 Meg x 4 or x16	22	11/12	11/10	2,048	Vss	Vss	NC	Vss	Vss			
Access Timing ^tRAC Max		100ns									Vss	Vss	
		80ns									NC	Vss	
		70ns									Vss	NC	
		60ns									NC	NC	
		50ns									Vss	Vss	
Refresh Control		Extended											NC
		SELF, Extended											Vss

NOTE: Vss = ground.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1.0V to +4.5V
Operating Temperature T_A (ambient) .... 0°C to 55°C
Storage Temperature .... -40°C to +70°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Card Insertions (connector's life cycle) 10,000

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.15	3.45	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	Vcc+1	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	$\overline{RAS0}$-$\overline{RAS3}$	II1	-8	8	µA	
Any input: 0V ≤ VIN ≤ Vcc	A0-A10, $\overline{WE}$	II2	-10	10	µA	
(All other pins not under test = 0V) for each package input	$\overline{CAS0}$-$\overline{CAS3}$	II3	-8	8	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ VOUT ≤ Vcc) for each package input	DQ0-DQ31	IOZ	-20	20	µA	31
OUTPUT LEVELS Output High Voltage (IOUT = -2.0 mA)		VOH	2.0		V	
Output Low Voltage (IOUT = 2.0 mA)		VOL		0.4	V	

DRAM CARD

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	MAX -7	MAX -8	UNITS	NOTES
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC1}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 4, 27
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	4MB 8MB 16MB 32MB	8 16 8 16	8 16 8 16	8 16 - -	mA	
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC3}	4MB 8MB 16MB 32MB	480 488 720 728	400 408 640 648	320 328 - -	mA	3, 4, 27
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = Vcc -0.2V)	I_{CC4}	4MB 8MB 16MB 32MB	4 8 4 8	4 8 4 8	4 8 - -	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 27
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	4MB 8MB 16MB 32MB	640 648 960 968	560 568 880 888	480 488 - -	mA	3, 5
REFRESH CURRENT: Extended CBR Average power supply current during extended CBR; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); ^tRC = 125µs; $\overline{WE}$ = Vcc -0.2V; A0-A10 and DQ = Vcc -0.2V or 0.2V (DQ may be left open)	I_{CC7}	4MB 8MB 16MB 32MB	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	mA	3, 5
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc-0.2V; A0-A10 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	4MB 8MB 16MB 32MB	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	1.2 2.4 2.4 4.8	mA	5, 28

CAPACITANCE

PARAMETER	SYMBOL	MAX 4,16MB	MAX 8, 32MB	UNITS	NOTES
Input Capacitance: $\overline{CAS0}$-$\overline{CAS3}$	C_{I1}	17	34	pF	2
Input Capacitance: $\overline{WE}$	C_{I2}	66	66	pF	2
Input Capacitance: $\overline{RAS0}$-$\overline{RAS3}$	C_{I3}	34	34	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2
Input Capacitance: Addresses	C_{I3}	51	90	pF	2

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	tAA		30		35		40	ns	
Column-address hold time (referenced to RAS)	tAR	50		55		55		ns	
Column-address setup time	tASC	0		0		0		ns	
Row-address setup time	tASR	0		0		0		ns	
Access time from CAS	tCAC		15		20		20	ns	15
Column-address hold time	tCAH	10		15		15		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
CAS hold time entering SELF REFRESH	tCHD	15		15		15		ns	28
CAS hold time (CBR REFRESH)	tCHR	15		15		15		ns	5
CAS to output in Low-Z	tCLZ	3		3		3		ns	26
CAS precharge time	tCP	10		10		10		ns	16
Access time from CAS precharge	tCPA		35		40		45	ns	
CAS to RAS precharge time	tCRP	10		10		10		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
Write command to CAS lead time	tCWL	15		20		20		ns	
Data-in hold time	tDH	10		15		15		ns	24
Data-in hold time (referenced to RAS)	tDHR	45		55		60		ns	
Data-in setup time	tDS	0		0		0		ns	24
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 26
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 55°C; Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Row-address hold time	^tRAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width entering SELF REFRESH	^tRASS	100		100		100		µs	28
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	20	60	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command setup time	^tRCS	0		0		0		ns	
Refresh period (1,024 cycles)	^tREF		128		128		128	ms	30
Refresh period (2,048 cycles)	^tREF		128		128		128	ms	29
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		0		ns	
$\overline{RAS}$ precharge time exiting SELF REFRESH	^tRPS	110		130		150		ns	28
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		20		ns	
Transition time (rise or fall)	^tT	3	50	3	50	3	50	ns	
Write command hold time	^tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	
Write command pulse width	^tWP	10		15		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	22
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	22

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NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1. Vcc = +3.3V ±5%; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the ᵗREF refresh requirement is exceeded.
8. AC characteristics assume ᵗT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If CAS = V_{IH}, data output is High-Z.
12. If CAS = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ᵗRCD < ᵗRCD (MAX). If ᵗRCD is greater than the maximum recommended value shown in this table, ᵗRAC will increase by the amount that ᵗRCD exceeds the value shown.
15. Assumes that ᵗRCD ≥ ᵗRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for ᵗCP.
17. Operation within the ᵗRCD (MAX) limit ensures that ᵗRAC (MAX) can be met. ᵗRCD (MAX) is specified as a reference point only; if ᵗRCD is greater than the specified ᵗRCD (MAX) limit, access time is controlled exclusively by ᵗCAC.
18. Operation within the ᵗRAD (MAX) limit ensures that ᵗRCD (MAX) can be met. ᵗRAD (MAX) is specified as a reference point only; if ᵗRAD is greater than the specified ᵗRAD (MAX) limit, access time is controlled exclusively by ᵗAA.
19. Either ᵗRCH or ᵗRRH must be satisfied for a READ cycle.
20. ᵗOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
22. ᵗWTS and ᵗWTH are setup and hold specifications for the WE pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ᵗWRP and ᵗWRH in the CBR REFRESH cycle.
23. The maximum current ratings are based on the memory operating or being refreshed in the x32 mode. The stated maximums may be reduced by one-half when used in the x16 mode.
24. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
25. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being tied permanently LOW on all 4 Meg DRAMs.
26. The 3ns minimum is a parameter guaranteed by design.
27. Column-address changed once each cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
29. 16MB and 32MB versions only.
30. 4MB and 8MB versions only.
31. 4MB version is half of values shown.

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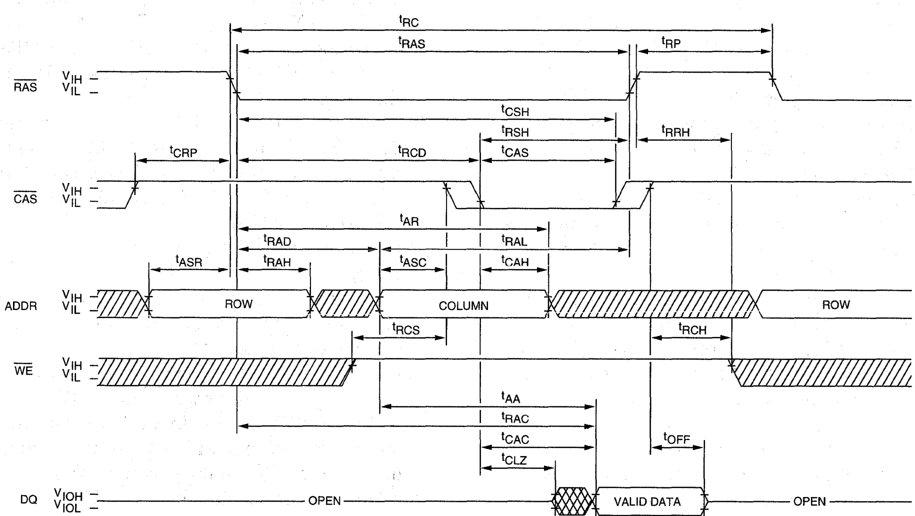
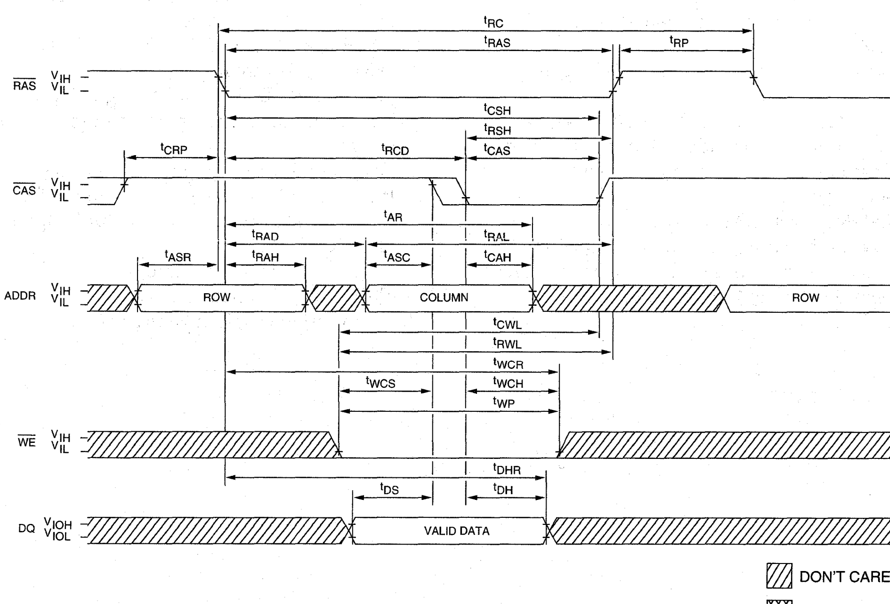
READ CYCLE



EARLY WRITE CYCLE



DON'T CARE

UNDEFINED

DRAM CARD

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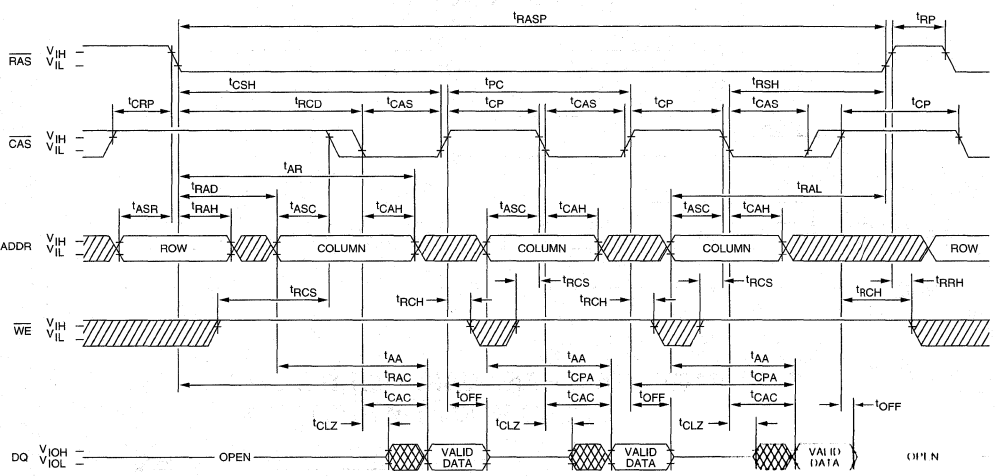
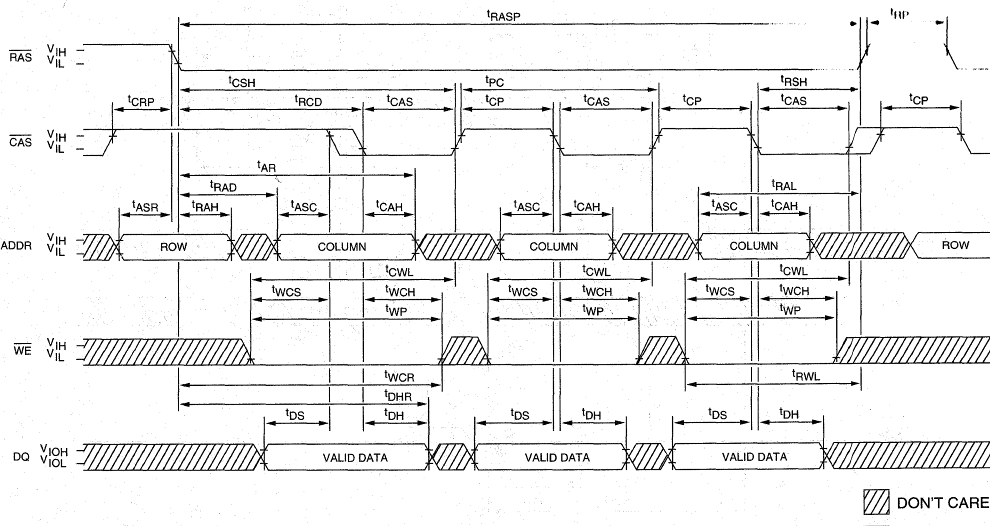
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



DRAM CARD

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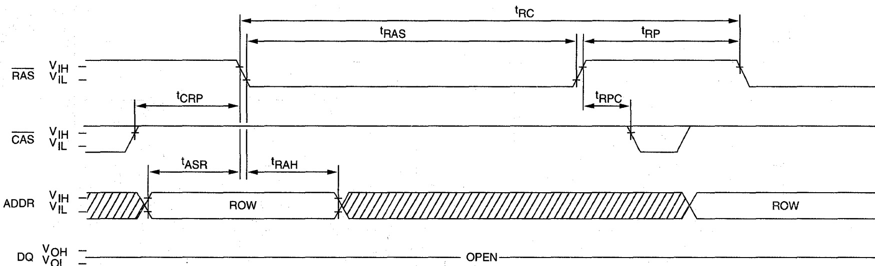
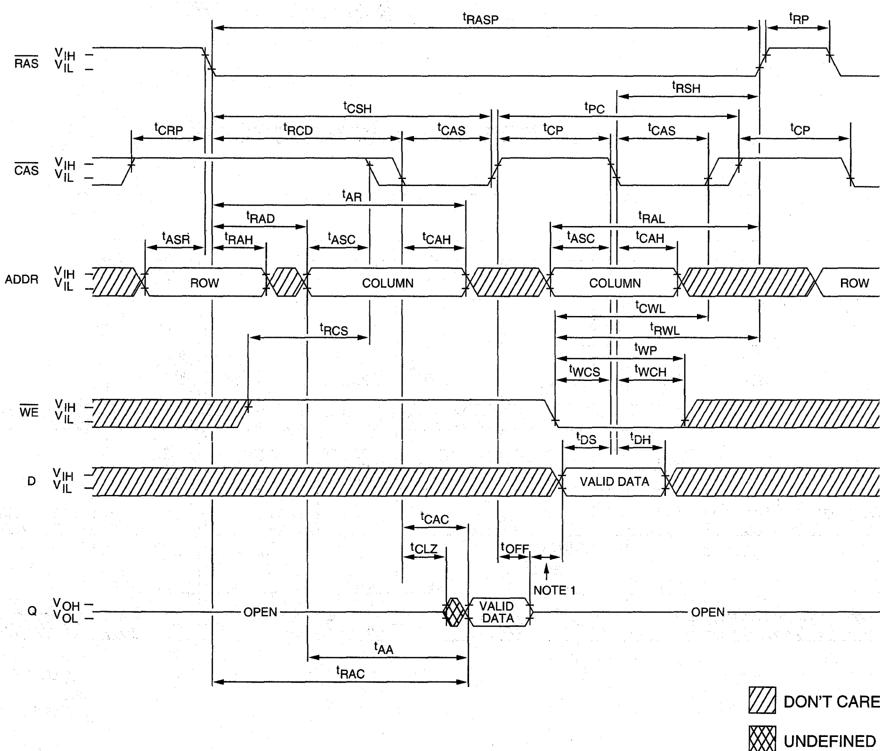
RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)



FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

DRAM CARD

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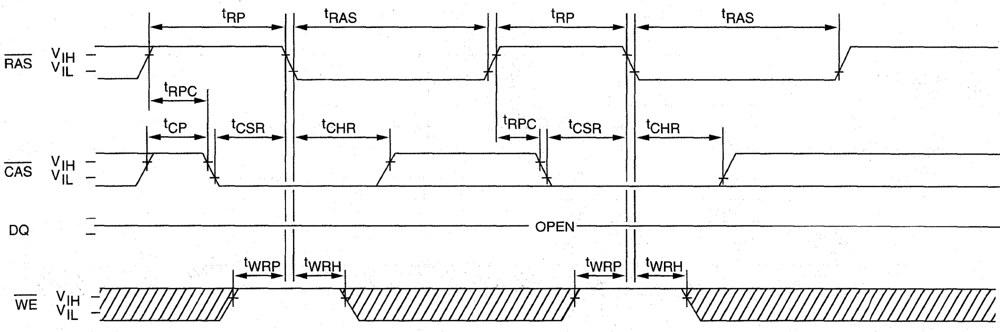
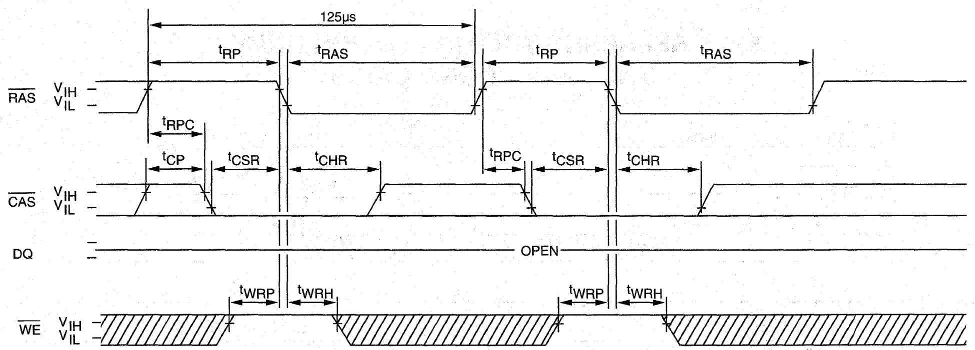
CBR REFRESH CYCLE
(Addresses = DON'T CARE)



EXTENDED CBR REFRESH CYCLE
(Addresses = DON'T CARE)



DON'T CARE

UNDEFINED

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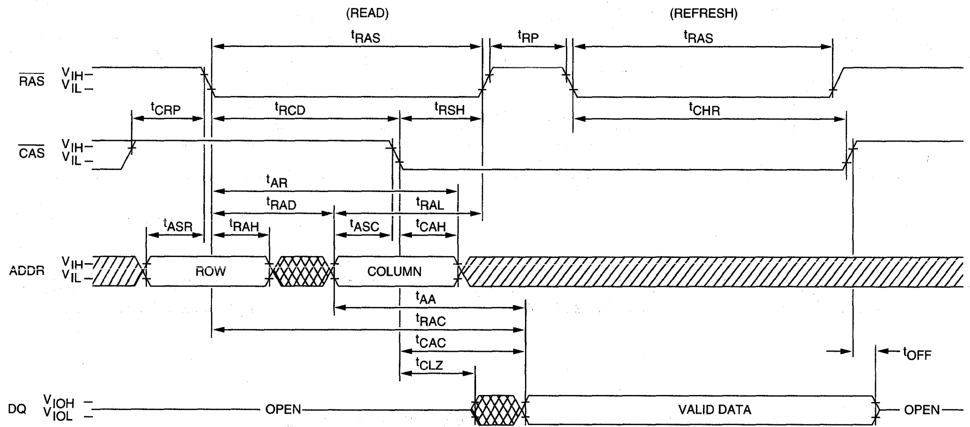
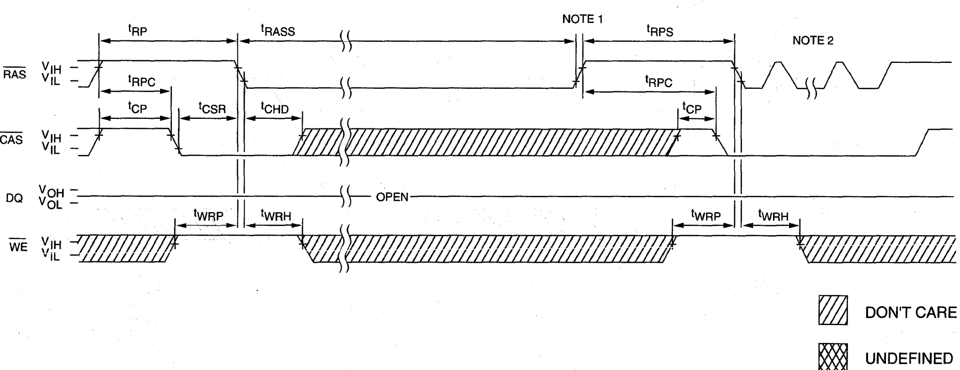
HIDDEN REFRESH CYCLE [21]

(WE = HIGH)



SELF REFRESH CYCLE (S VERSION ONLY)

(Addresses = DON'T CARE)



NOTE:
1. Once tRASS (MIN) is met and RAS remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

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TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated-circuit packages have a tendency to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks which might not be harmful initially could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron's customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year, and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K., et al.: 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et al.: 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et al.: 26th Annual Proceeding, Reliability Physics, 1988.

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TECHNICAL NOTE

TAPE-AND-REEL PROCEDURES

GENERAL DESCRIPTION

Tape-and-reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape-and-reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
32 Pin	24	16	500
52 Pin	32	24	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
32 Pin	32	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500
TSOP (300 mil)			
20/26 Pin	24	12	1,000
TSOP (400 mil)			
40/44 Pin	32	16	1,000

*These are examples of tape-and-reel sizes available. Please contact Micron for all available options.

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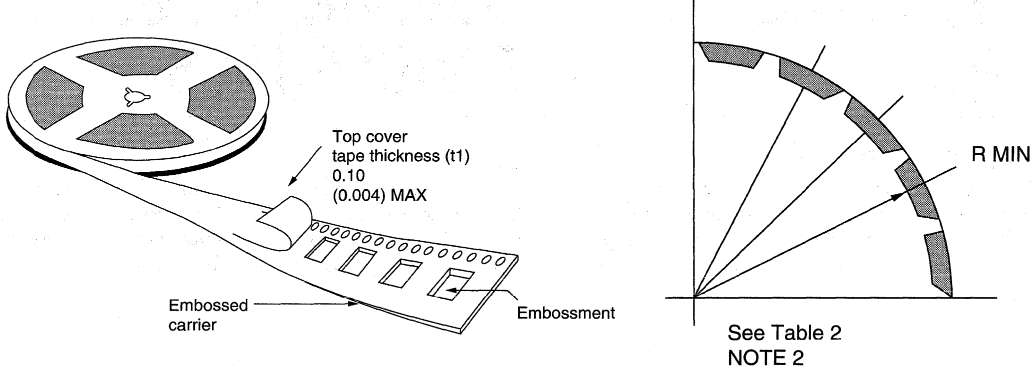
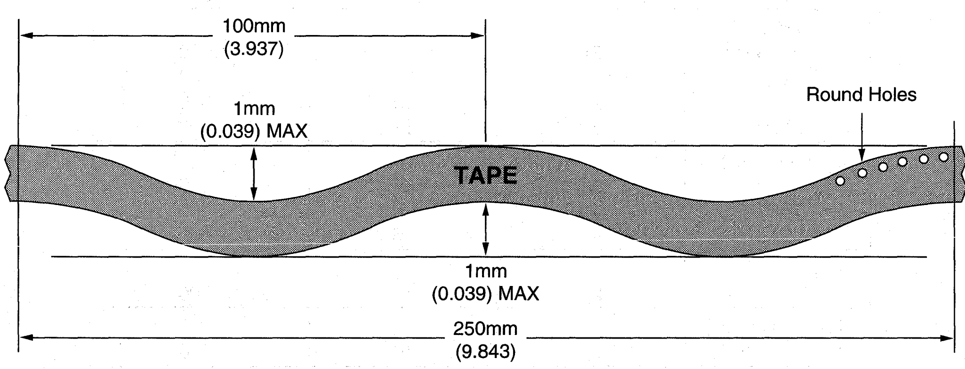


Figure 1
REEL

Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

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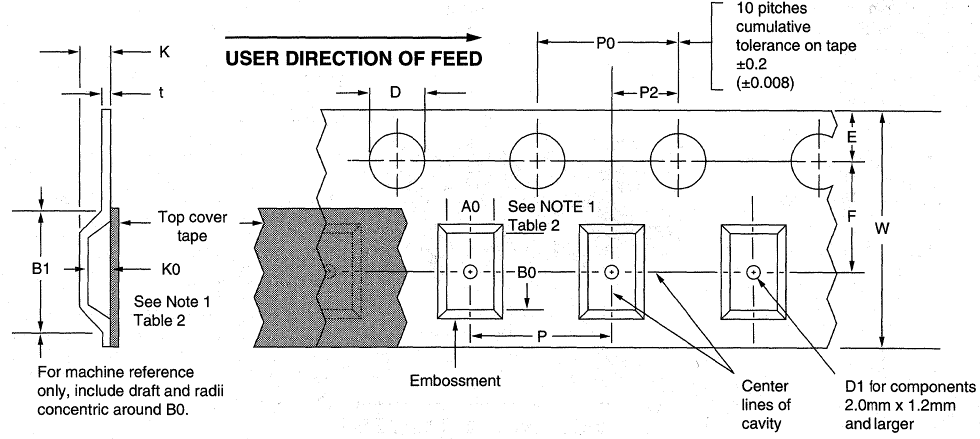

Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	Note 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius “R” without damage.
3. All dimensions in millimeters, (inches).

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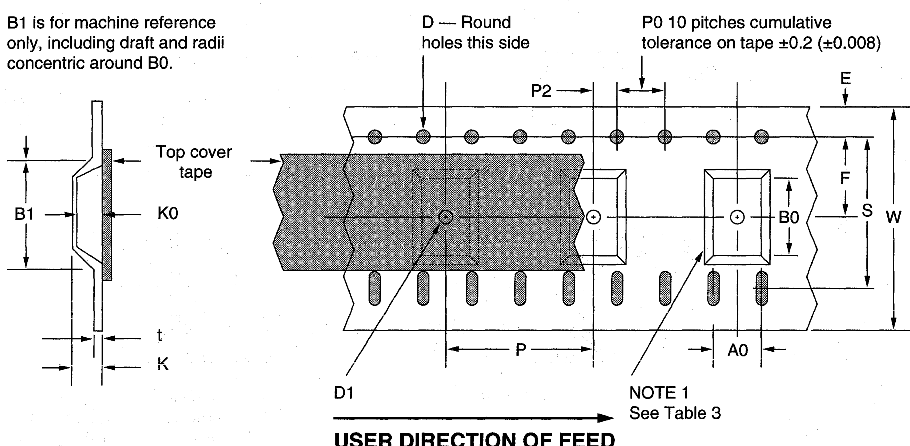

Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm tape only)

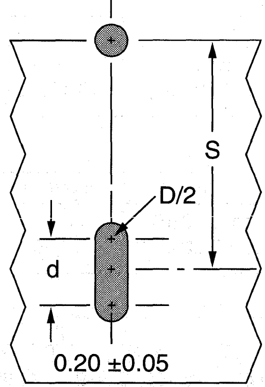

Figure 6
DETAIL ELONGATED HOLE

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Table 3
32 AND 44mm EMBOSSED TAPE[3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	1.5 $^{+0.10}_{+0.00}$ (0.059) $^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

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TECHNICAL NOTE

USING GEL-PAK® PACKAGING WITH MICRON DIE

INTRODUCTION

In order to provide a robust packaging environment when shipping die products, Micron uses Gel-Pak® packages. This Technical Note describes the Gel-Pak package, the advantages it has over other forms of packaging and how customers can store and use die from this package.

THE GEL-PAK

The Gel-Pak was chosen because of its advantages over other methods of packaging. Although die can be stored in traditional waffle-packs or chip trays, these packages cannot be used for shipping die. In these packages, the die may easily move within the storage cavity during shipment. This movement can be abrasive to the die and can cause chipping or breakage.

The Gel-Pak eliminates these problems. Figure 1 shows a side view of a Gel-Pak containing die. Right below the die is a gel membrane that uses surface tension to rigidly hold the die in place. Because the die cannot move, the chances of damage are greatly reduced. In addition, the topside of the die which contains the device circuitry is not in contact with any surface that could damage the die.

Micron uses conductive Gel-Paks. The plastic used in the construction of the tray and cover is electrically conducting and protects the die from harmful static electricity. We still recommend that ESD precautions be taken whenever handling or moving the Gel-Pak tray.

STORAGE REQUIREMENTS

Micron die are packaged for shipping within a cleanroom environment and packaged in a vacuum sealed bag to minimize exposure to humidity. Upon receipt, the customer should transfer the Gel-Pak package to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times during inspection and assembly.

USING GEL-PAKS

Figure 2 shows a Gel-Pak being used when die are being removed during an assembly process. Underneath the gel membrane is a release pattern formed of fabric mesh or molded pattern which defines a series of voids underneath the die. When a vacuum is applied to the tray, the gel membrane is deformed and the amount of surface area in contact with the die is greatly reduced. A holding fixture should be provided for positive positioning of the tray so that a leak-free vacuum can be delivered to the underside of the tray. Empirical tests show that the surface tension force is reduced by over two orders of magnitude allowing the die to be easily removed.

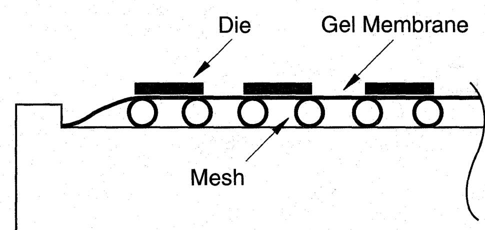

Figure 1
CROSS-SECTIONAL VIEW OF A GEL-PAK

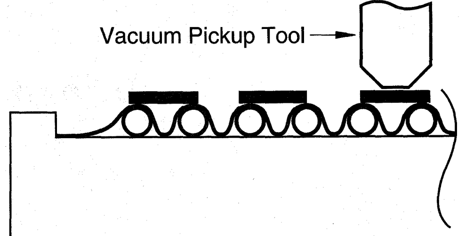

Figure 2
VACUUM APPLIED TO GEL-PAK

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Once the vacuum is applied to the container, it is recommended that a vacuum pickup tool be used to remove and place the die. This will minimize the risk of breakage or chipping. Replaceable rubber tips for pickup tools may provide for a more positive device removal from vacuum release trays. The maximum tip size compatible with the device should be used.

With some pick and place machines, the vacuum is activated by the contact pressure of the pickup tool on the die. This may result in the die being pushed slightly into the gel, which in turn reduces the ease with which the die can be picked from the gel. Some equipment manufacturers have indicated that their pick and place machines can be easily modified to automatically activate the vacuum with very low contact pressure, or manually by the operator with essentially no contact pressure.

Vacuum Work Stations are available from Gel-Pak which provide an easy way to apply the vacuum to the Gel-Pak. Micron uses 2- and 4-inch Gel-Paks. The 4-inch Vacuum Work Station can be used with both types.

Figure 3 shows a typical orientation of die in a Gel-Pak. All die are placed in the Gel-Pak with identical orientation. Refer to individual die data sheets for the exact orientation for a particular die and part number.

CONCLUSION

By using the methods outlined above, customers will be able to use Micron die shipped in Gel-Paks. Following these guidelines will ensure minimum breakage and ease of use.

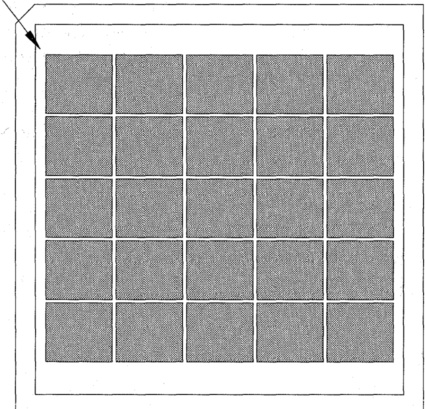

Figure 3
ORIENTATION OF DIE IN GEL-PAK

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TECHNICAL NOTE

DRAM POWER-UP AND REFRESH CONSTRAINTS

INTRODUCTION

The JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding and addressing these incompatibilities and providing for them will offer designers and system users greater compatibility between the 1 Meg and 4 Meg.

REFRESH

The most commonly used refresh mode of the 1 Meg is the CAS-BEFORE-RAS (CBR) REFRESH cycle. The CBR for the 1 Meg specifies the WE pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the WE pin held at a voltage HIGH level.

A CBR cycle with WE LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR). In contrast, the 1 Meg test mode is entered by applying a HIGH signal to the test pin (pin 4 on DIPs, pin 5 on SOJs and pin 8 on ZIPs). This HIGH signal is usually a "super voltage" ($V_{IN} \geq 7.5V$), so normal TTL or CMOS HIGH levels will not cause the part to enter TEST MODE.

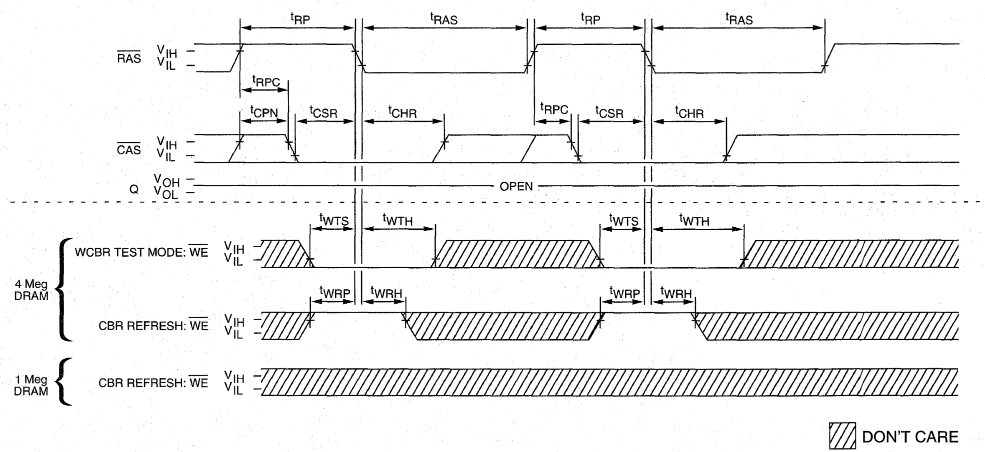
POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight RAS cycles. The 4 Meg POWER-UP cycle is more restrictive in that eight RAS ONLY or CBR REFRESH (WE held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the TEST MODE. The only way to exit the 4 Meg JEDEC TEST MODE is with either a RAS ONLY or a CBR REFRESH cycle (WE held HIGH).

SUMMARY

The 1 Meg and 4 Meg are compatible, with the following exceptions:

1. For standard TEST MODE, the 1 Meg requires a valid HIGH on the test pin while the 4 Meg requires a CBR cycle with WE LOW.
2. The 1 Meg CBR REFRESH allows the WE pin to be a "don't care" while the 4 Meg CBR requires WE to be HIGH.
3. The eight RAS wake-up cycles on the 1 Meg may be any valid RAS cycle while the 4 Meg may only use RAS ONLY or CBR REFRESH cycles (WE held HIGH).



COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

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TECHNICAL NOTE

OE-CONTROLLED/LATE WRITE CYCLES (DRAM)

INTRODUCTION

There are three cycles available to write to a DRAM: EARLY WRITE cycles, READ-MODIFY-WRITE cycles and LATE WRITE cycles. The industry-standard definitions for DRAM WRITE cycles are fairly consistent for both the EARLY WRITE and READ-MODIFY-WRITE cycles. An exception exists for the LATE WRITE cycle.

COMMON DQ DRAM (x4, x8, etc.)

A LATE WRITE cycle is a READ-MODIFY-WRITE (see Figure 1) except that the READ portion is not utilized. This is accomplished by keeping the output enable pin (OE) HIGH throughout the cycle. The timing parameters ${}^tRWD$, ${}^tAWD$ and ${}^tCWD$ no longer apply since OE is HIGH.

This condition may be viewed as an EARLY WRITE with ${}^tWCS$ "sliding" past the CAS time and violating the 0ns setup time (WE going LOW prior to CAS going LOW). However, since the output buffers are not being used (OE is HIGH), ${}^tWCS$ and ${}^tCWD$ are no longer required.

If WE transitions LOW after CAS transitions LOW, do not bring OE LOW (a noise spike may occur), because the output buffers could turn on and cause contention with the data bus, which could corrupt input data.

The term used for such a WRITE cycle varies throughout the industry. The use of "OE-controlled WRITE," "delayed WRITE" and "LATE WRITE" all signify the same WRITE cycle described.

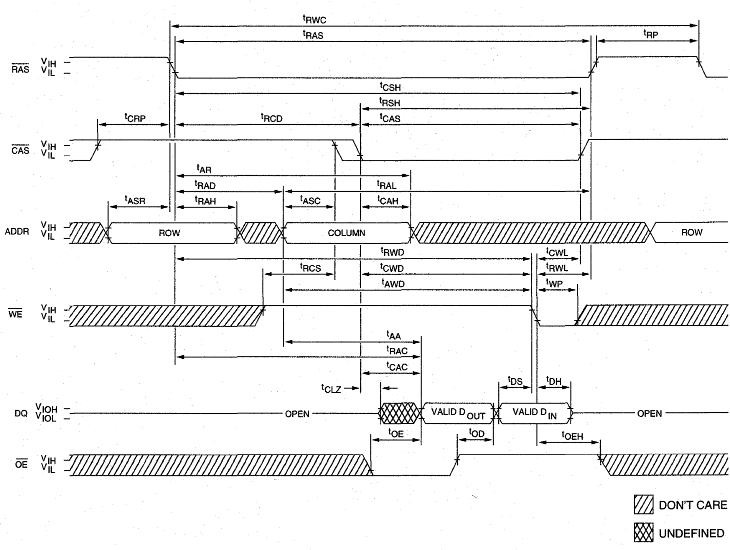

Figure 1
READ-MODIFY-WRITE (MULTIPLE DQ) TIMING

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SPLIT D AND Q DRAM (x1)

A LATE-WRITE cycle is a READ-MODIFY-WRITE, except the READ portion is not guaranteed and the D and Q pins are separate paths (D and Q cannot be connected). This is accomplished by ignoring the timing parameters tRWD, tAWD and tCWD.

This condition can be viewed as an EARLY WRITE with tWCS "sliding" past the CAS time and violating the 0ns setup time (WE going LOW prior to CAS going LOW). However, since the output buffers are "don't care," tWCS and tCWD are no longer required.

This cycle is not available on applications that have the D and Q connected together, because the output will contend with the input.

SUMMARY

A LATE WRITE cycle is most useful on common DQ DRAMs. Use caution to ensure that the output enable pin is properly controlled.

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TECHNICAL NOTE

LPDRAM EXTENDED REFRESH CURRENT vs. RAS ACTIVE TIME (4 MEG)

INTRODUCTION

One of the most significant features of the low-power extended refresh DRAM (LPDRAM) is its cycle. Extended refresh is essentially a CAS-BEFORE-RAS (CBR) REFRESH at an extended refresh rate of 125µs per cycle.

RAS pulse width (ᵗRAS) affects the extended refresh current and should be considered when designing a low-power system. The longer RAS is held LOW, the more current an LPDRAM will consume while in the extended refresh mode. Therefore, keeping ᵗRAS at a minimum will maximize power savings.

Figure 1, a typical curve of Micron's 4 Meg LPDRAM (MT4C4001J S and MT4C1004J S), shows the relationship between its extended refresh standby current and the width of ᵗRAS.

SUMMARY

The ᵗRAS time should be kept as short as possible when designing memory array timing. This will result in lower standby currents, especially for the extended refresh cycle.

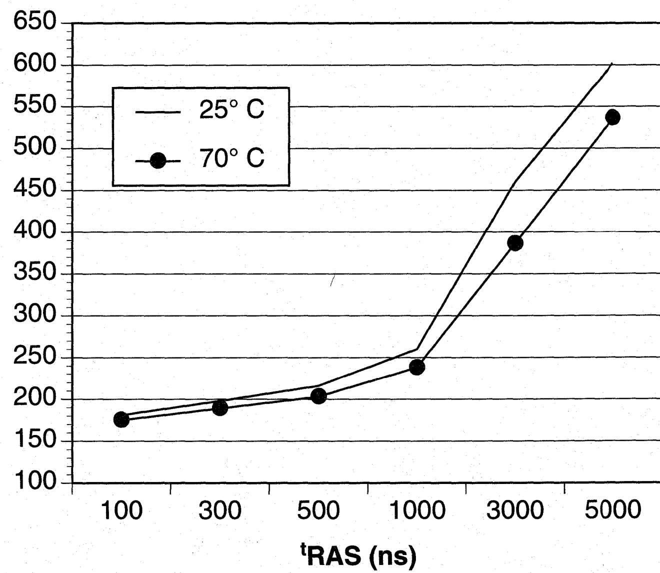

Figure 1
TYPICAL EXTENDED REFRESH CURRENT AS A FUNCTION OF ᵗRAS

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TECHNICAL NOTE

DRAM CONSIDERATIONS FOR PC MEMORY DESIGN

INTRODUCTION

The demand for DRAM memory in personal computers (PCs) has been mainly for desktop personal computers. When designing main memory, PC designers have primarily focused on three requirements: availability, cost and speed.

The new and growing field of portable personal computers has introduced seven additional issues:

- Parity
- Lower power (Extended Refresh)
- SELF REFRESH
- Package size
- Operating current
- 3.3V operating voltage
- DRAM cards (88-pin)

The first three issues (availability, cost and speed) are well understood. This technical note discusses the remaining issues in order to help memory designers choose the best solution for their portable or desktop system designs.

OFFERINGS

To design main memory, five basic offerings of DRAM are or will be available in the near future:

1 Meg x 4	(plus 1 Meg x 4 Quad CAS for parity)
512K x 8	(512K x 9 for parity)
2 Meg x 8	(4 Meg x 1 for parity)
256K x 16	(256K x 18 for parity)
1 Meg x 16	(1 Meg x 4 Quad CAS for parity)

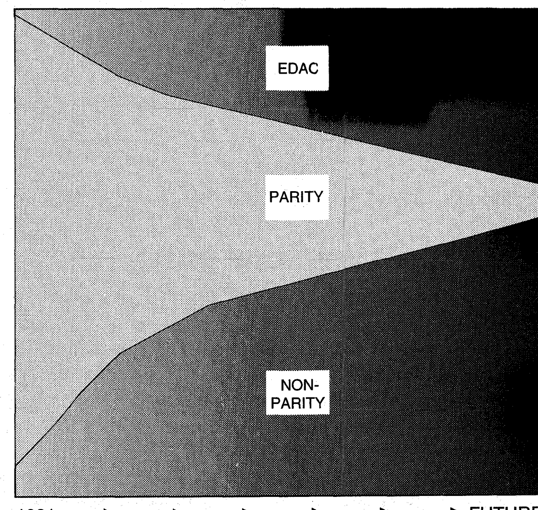
The first offering is referred to as "standard DRAMs," and the remaining are referred to as "wide DRAMs." Generally, standard DRAMs are more readily available and have more sources. Wide DRAM development is usually a generation behind the standard DRAM and is not expected to catch up until the third generation of 16 Meg DRAMs and the first generation of 64 Meg DRAMs.

PARITY (OR NO PARITY)

There is a growing trend to build notebook and low-end to mid-range desktop PCs without parity. Within a few years, most parity-based systems will switch to either nonparity-based systems (as in most PCs) or error detection and correction (EDAC) based systems (high-end PCs).

Some of the reasons for this trend away from parity are listed below:

1. Parity does not significantly improve reliability.
2. DRAMs from a quality manufacturer now have very low soft error rates (SERs).
3. Parity increases memory costs 10 to 15 percent.
4. Some chipsets allow turning off the parity bit.
5. Parity requires extra board space as well as previous generation devices or less available parity chips.
6. Some software does not use parity.



Past, Present and Future Trends

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The most important of these factors is the memory system's reliability. In the early days of semiconductor DRAM memories, the high SER of 4K and 16K DRAMs, coupled with the high cost of implementing EDAC (8-bit buses), made implementing parity critical. DRAM manufacturers, however, have significantly reduced SER during the last five generations (Fig. 1). For example, the SER on a 16K DRAM was approximately 1 to 5 FITs per bit, whereas the SER on a 4 Meg DRAM is closer to 0.0002 to 0.0004 FITs per bit—a 10,000x improvement. (FIT is a failure in time, where time is 1 billion device hours.)

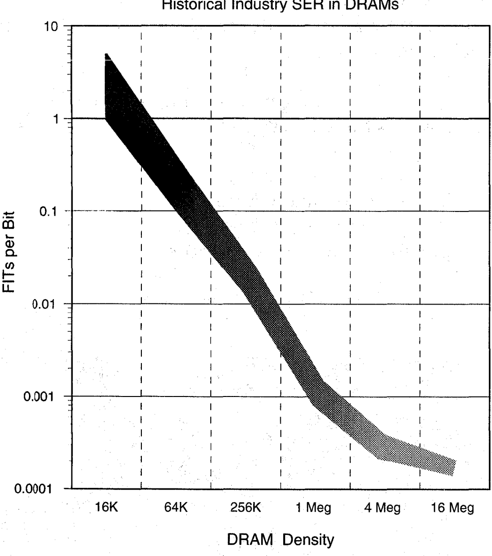

Figure 1
HISTORICAL DRAM SER

By taking these industry SER averages and applying them to a 2MB, 16-bit wide memory system, meaningful benchmarks for PCs can be obtained. Most systems measure errors in mean time between failures (MTBF). Applying the SER numbers from the previous figure, the improvement in MTBF for a typical 2MB, 16-bit wide memory system can be demonstrated (Fig. 2).

It is obvious why parity was instituted in the 16K DRAM days. A memory system made of 16K DRAMs would experience a SER hit every 60 to 70 hours. Because of this, it has been standard operating procedure to design in parity. But changes are ahead. System designers are starting to ask, "Why?" Using today's high-quality 4 Meg DRAMs rather than yesterday's 16K DRAMs extends the MTBF from approximately 60 hours to an MTBF of 30 to 35 years on a 2MB by 16-bit wide memory system.

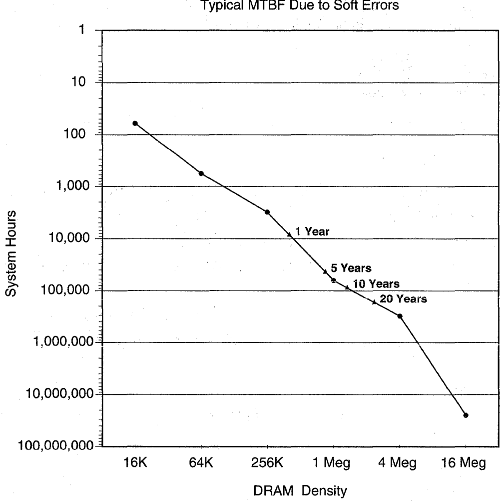

Figure 2
MTBF FOR 2MB MEMORY SYSTEM

Another way to look at this same data is to calculate the number of SER hits a user would see after ten years of continuous use (Fig. 3). As expected, the SER is negligible after ten years of continuous use when using today's high-quality DRAMs.

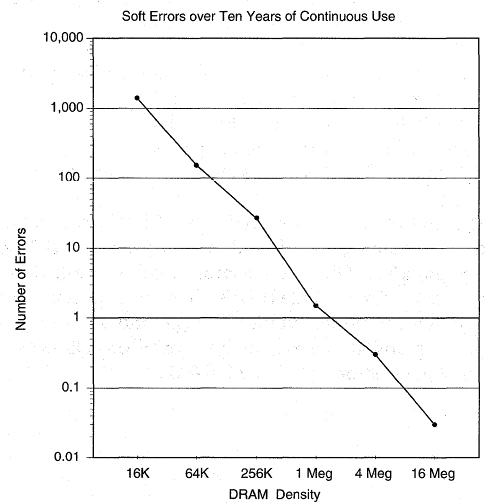

Figure 3
2MB MEMORY SYSTEM SER

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It is important to note that the SER and MTBF must be carefully calculated for any given system and its application. The DRAM's SER is dependent on Vcc (power supply voltage), operating speed (cycle rate) and memory configuration. By taking the previous 2MB example and doubling it to 4MB, the SER will either increase slightly or double. If the width of the memory system is increased to 32 bits, the SER would double since all DRAM bits are active. If, on the other hand, the memory is interleaved and the bus remains 16 bits wide, the SER increases only slightly. This is because the bank not being accessed is in standby mode and is much less susceptible to SER hits. (The faster the cycle rate, the more susceptible a DRAM is to SER.) Technical note TN-04-28 provides an in-depth analysis to determine system MTBF to soft error.

Table 1
PARITY AND EDAC OVERHEAD

	EXTRA BITS REQUIRED		BUS WIDTH INCREASE	
BUS SIZE (BITS)	PARITY	EDAC	PARITY	EDAC
8	1	5	12.5%	62.5%
16	2	6	12.5%	37.5%
32	4	8	12.5%	25%
64	8	8	12.5%	12.5%

Although the need for parity would appear to be greater for wider buses, the additional cost to implement EDAC, rather than parity, decreases substantially as the bus width increases. In fact, the DRAM memory cost is the same for a 64-bit wide bus (Table 1). Besides detecting two errors for a given word, EDAC will also correct any single bit error.

Most applications with buses no more than 32 bits wide do not require parity, whereas applications using bus widths of 32 bits or more may require some kind of bit-checking for errors. The choice is usually EDAC rather than parity.

Table 2
SELECTION FOR ERROR CHECKING

ERROR CHECKING	BUS SIZE (BITS)		
	16	32	64
Nonparity	1 Meg x 4	1 Meg x 4	1 Meg x 4
Parity	n/a	1 Meg x 4	1 Meg x 4
EDAC	n/a	1 Meg x 4	1 Meg x 4

Table 2 summarizes which DRAM would be the optimum choice, considering price, performance and space. It takes into account the typical PC which ships with a minimum of 4MB of memory. The 64-bit bus choice of 1 Meg x 4 DRAMs is based on memory size increase from 4MB to 8MB.

The 1 Meg x 16 will be the part of choice once the premium reaches 10 percent above four 1 Meg x 4 DRAMs. As the minimum memory requirements increase, the 2 Meg x 8 will offer the optimum support: 16- and 32-bit buses at 8MB and 64-bit buses at 16MB.

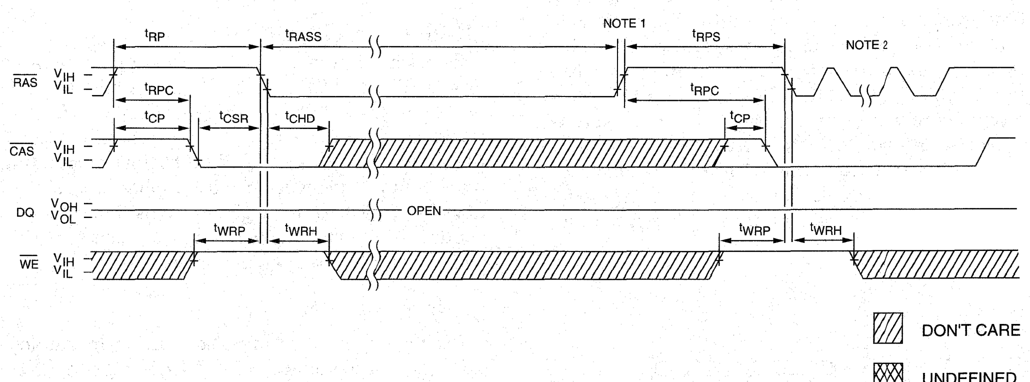

Figure 4
SELF REFRESH OPERATION

NOTE: 1. Once ^{t}RASSmin is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst refresh of all rows should be executed. Distributed refreshes at the specified refresh rate are acceptable, provided CBR REFRESH cycles are utilized.

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LOW-POWER, EXTENDED REFRESH

A low-power, extended refresh DRAM (LPDRAM) has a reduced CMOS standby current limit (typically from 1mA to 200µA) and refresh interval eight times longer (from 15µs per row to 62.5µs or 125µs per row). The extended refresh offers an extended mode, which is a low-current, data-retention cycle. Each of the five DRAM options in this technical note have low power, extended refresh versions available.

On a per-bit basis, the 1 Meg x 16 (1K refresh version) generally offers the best standby and refresh power savings compared to the other four DRAM organizations. The DRAM standby current is important in battery-operated systems, since DRAMs usually draw a large percentage (50 to 70 percent) of the total system current when the system is in sleep or suspend mode.

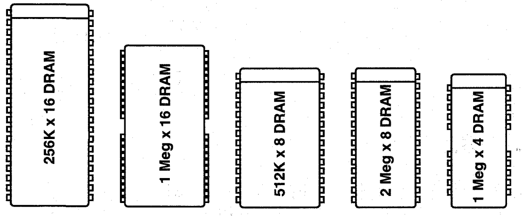
SELF REFRESH

The SELF REFRESH feature built into some DRAMs is usually indicated by an LL or S suffix. This feature performs an extended refresh mode, with the exception that no external clocking is required; that is, the DRAM will refresh itself via its own internal refresh clock (Fig. 4).

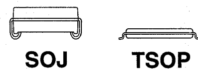
Control of SELF REFRESH is defined by JEDEC and the following defacto standard timing specifications: ${}^tRASS$ = 100µs, ${}^tRPS \approx {}^tRC$, ${}^tCHD$ = 10ns.

PACKAGE SIZE

Conserving board space is always an important design consideration, especially for laptop and notebook computers. Functionally, DRAMs require more board space than most other devices. The size between the five options in small outline J-lead package (SOJ) vary greatly. The 512K x 8 DRAM requires approximately 50 percent more area than a 1 Meg x 4 DRAM. The 256K x 16 requires approximately 110 percent more area than a 1 Meg x 4 DRAM and 44 percent more area than a 512K x 8. Use of 16 Meg DRAMs result in significant space savings: 1 Meg x 16 equals 2.5 times and 2 Meg x 8 equals 4 times space savings over use of 1 Meg x 4. Full-sized outlines are shown here for comparison:



These are also available in a thin, small-outline, gull-lead package (TSOP). The length and width of a TSOP are the same as the corresponding SOJ package (same board area) except that the x16 length TSOP is reduced because of a smaller lead pitch (50mil to 32mil). The TSOP's key attraction is that it is one-third the thickness of the SOJ (47 mils compared to 142 mils), as illustrated below:



Notebooks and other compact designs which have height or layout restrictions can sometimes justify the current cost premium required to use TSOPs. Additionally, in TSOP, the x16 does not impose as severe a board space penalty, as does a x16 SOJ. Table 3 lists the dimensions (length and width) for the various packages.

Table 3
PACKAGE DIMENSIONS (in mils)

	SOJ		TSOP	
Device Type	**Width**	**Length**	**Width**	**Length**
1 Meg x 4	340	679	367	677
512K x 8	445	729	467	727
2 Meg x 8	340	729	340	727
256K x 16	445	1029	467	727
1 Meg x 16	n/a	n/a	467	827

OPERATING CURRENT

Operating current is usually of less importance in system design. When a PC is in the active mode, the DRAM's portion of current draw is minimal (typically from four to six percent) compared to the total system current consumption. Wider DRAMs generally offer lower operating currents (10 to 20 percent) in most applications, since fewer devices are active for a given access, but generally not enough to outweigh the cost increase, board space increase and performance reduction they impose.

3.3 VOLTS

Personal computers are also starting to employ 3.3V DRAMs. A low-voltage (3.3V) DRAM consumes approximately half the power of a 5V version. The choice of whether to use 5V or 3.3V DRAMs is dictated by the voltage platform selected, which is determined by the CPU and chipset specifications. Systems requiring memory support beyond a few years are employing 3.3V DRAMs to ensure long term support.

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FUTURE FEATURES

Many new features will be available in the near future. Some of the more important features will be extended data-out (EDO) and synchronous DRAMs. The EDO DRAM is a FAST PAGE DRAM with the exception that the data outputs (DQ) are not tristated by $\overline{CAS}$.

The key advantage with EDO is a PAGE-MODE READ cycle up to 30 percent faster. Since $\overline{CAS}$ does not tristate the DQs, ᵗCAS can be minimized and $\overline{CAS}$ precharge can occur while the output data is being latched. EDO is considered a bridge for performance increase until synchronous DRAMs are a cost effective solution for the very high-end performance system.

System designs should control $\overline{WE}$ HIGH at $\overline{RAS}$ time during READ and WRITE cycles (see Figure 6) in today's FAST-PAGE-MODE and EDO designs. Such controlling of $\overline{WE}$ will facilitate compatibility with future EDO DRAMs.

The synchronous DRAM is a radical change from the standard DRAM. Rather than being dependent on time delays, the synchronous DRAM's inputs will all be clocked-in on the positive edge of the system clock. The synchronous DRAM is expected to provide the speed performance required for 100 MHz and above systems.

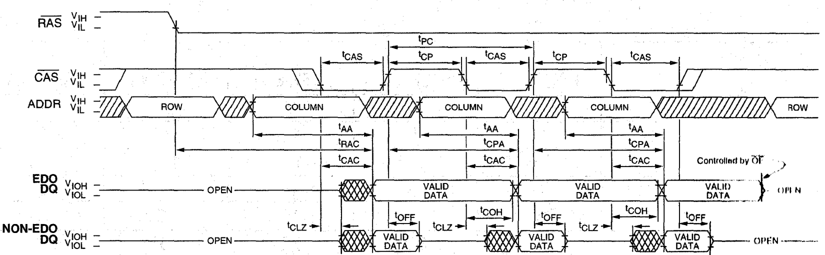

Figure 5
EDO vs. NON-EDO (FAST-PAGE-MODE) DRAMS

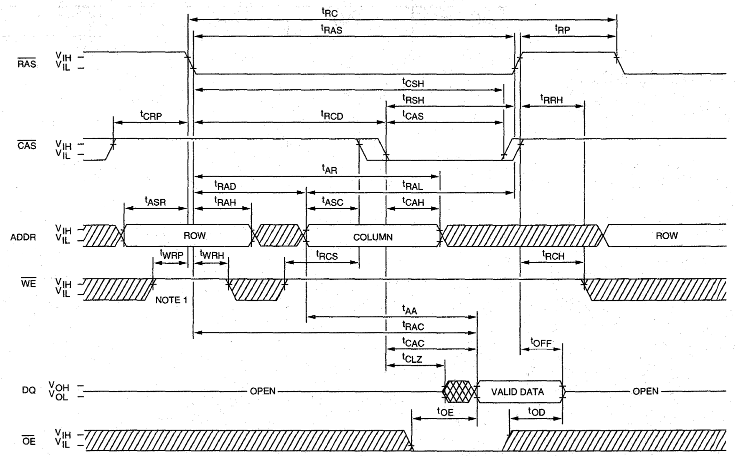

Figure 6
EDO READ CYCLE

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ᵗWRP and ᵗWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

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SUMMARY

The 1 Meg x 4 (desktops) and 1 Meg x 16 DRAM (notebooks) are today's best choices for main memory in personal computers. With minimum memory requirements growing, the 2 Meg x 8 DRAM is becoming the best choice for main memory in both desktop and notebook PCs. Table 3 summarizes and compares the issues involved in selecting DRAMs for PC memories.

Wider DRAMs are best suited to systems which require shallow and wide arrays. The 256K x 16 is a good choice for high-end video graphics and printer buffers requiring up to 256K bits deep and 16 or more bits wide.

Most PC systems do not require the burden of parity when using 4 or 16 Meg DRAMs. High-end systems should use EDAC for the best reliability.

Table 3
4 MEGABYTE MODULE (1 MEG x 32)

PARAMETERS		1 MEG x 4	512K x 8	256K x 16	2 MEG x 8	1 MEG x 16	UNITS
Number of Devices Required		8	8	8	n/a	2	Devices
Availability (Market Volume)		40	1	10	3	2	Relative to
	Base Price	1.0	1.25	1.2	1.1	1.4	1 Meg x 4
Costs	Low Power Adder	5	5	5	5	5	% of Base
	TSOP Adder	10	10	10	10	5	% of Base
Minimum Speed (Typical)		70	80	70	70[1]	70[1]	ns @ 5V
BBU ICC	Maximum Spec	2.4	3.2	3.2	n/a	0.6[1]	mA @ 5V
	Typical	1.2	2.4	2.4	n/a	0.4[1]	mA @ 5V
Minimum Board Space Used		12	18	26	n/a	5	cm^2
Active ICC	Maximum Spec	680	400	280	n/a	310[1]	mA @ 5V
	Typical	400	340	240	n/a	200[1]	mA @ 5V

NOTE: 1. 3.3V with 5V tolerant I/O.

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TECHNICAL NOTE

16 MEG DRAM—2K vs. 4K REFRESH COMPARISON

INTRODUCTION

Micron Technology, Inc., offers its 4 Meg x 4 DRAM in two JEDEC-approved versions. The MT4C4M4A1 requires 12 row-address bits and 10 column-address bits for 4,096 (4K) cycle refresh in 64ms. The MT4C4M4B1 requires 11 row-address bits and 11 column-address bits for 2,048 (2K) cycle refresh in 32ms. Excluding this difference, the timing and performance of the two devices are identical.

Industry demand for decreased power consumption led JEDEC to approve 4K refresh in addition to 2K refresh at the 16 Meg level. At minimum random cycle time (^tRC = 110ns), A 4 Meg x 4 device with 4K refresh draws ≈30mA less operating current than a device with 2K refresh. The current is decreased by increasing the number of rows and decreasing the number of columns in the DRAM array. A 4 Meg x 4 with 4K refresh has 4,096 rows and 1,024 columns, whereas one with 2K refresh has 2,048 rows and 2,048 columns. The number of columns defines the "depth" of a page. The drawing below shows how 2K and 4K refresh devices are different. Notice that the 2K device has a page depth of 2,048, while the 4K device has a page depth of 1,024, or half the page depth of the 2K device.

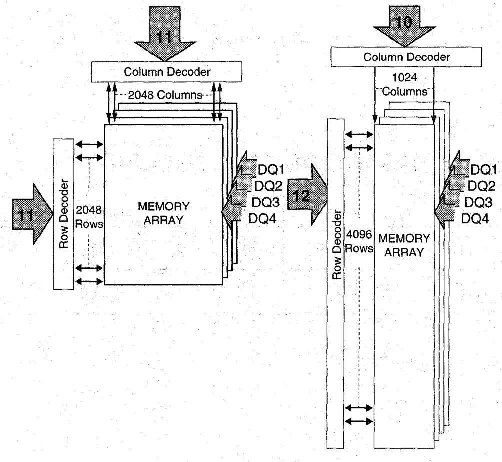

Figure 1

CHOOSING 2K OR 4K REFRESH

There are several factors to consider when deciding which refresh standard is best for an application:

1. Addressing supported by your DRAM controller—11 row/11 column, 12 row/12 column, or both?
2. Frequency and length of page accesses
3. Average cycle rates

Some DRAM controllers have only 11 address drivers, so they are limited to 2K refresh. Many newer DRAM controllers, including some of the 3.3V controllers, are being designed to support both standards, so this limitation should be short-lived.

Your choice of 2K or 4K refresh will probably be based on the importance of power consumption versus page depth. A system requiring frequent page accesses may not benefit by sacrificing page depth in exchange for the power savings of a 4K refresh. In a portable system, the benefits of 20mA less current may easily override concerns about decreased page depth.

Additionally, the difference in power consumption decreases with longer cycle times. If the DRAMs spend much of their time idle, as in systems using SRAM caches, the power savings may be negligible. See Figure 2.

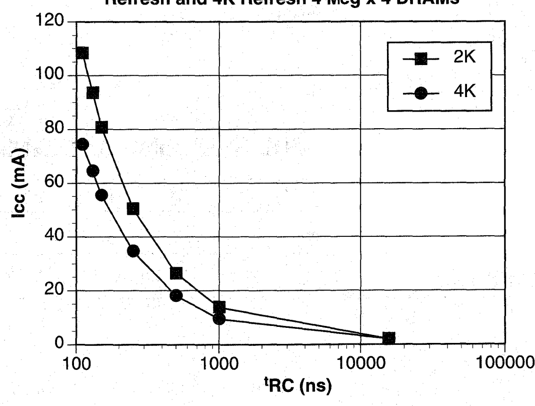

Figure 2

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MODULES

Modules may use both 2K and 4K refresh depending on whether or not they have twelve address inputs. If a module uses parity, such as the 4 Meg x 9 or the 4 Meg x 36, it probably mixes 4 Meg x 4 and 4 Meg x 1 DRAMs on the same module. Because the 4 Meg x 1 DRAM requires symmetric addressing (11 row-addresses and 11 column-addresses), using a 4K refresh 4 Meg x 4 DRAM requires that the DRAM controller support both addressing decodes simultaneously. This is possible using "redundant addressing," whereby one of the address bits is duplicated as both a row-address and as a column-address. Most modules that have parity will simply use the 2K refresh 4 Meg x 4 DRAM in order to avoid changes to existing controllers. As shown in Figure 3, when a 4 Meg x 4 with 2K refresh is employed, the numbers of rows and columns match the 4 Meg x 1, allowing use of the 4 Meg x 1 for parity.

If the 4 Meg x 4 with 4K rows is implemented, redundant addressing must be employed, or use of the 4 Meg x 1 for parity becomes impossible because the number of rows and columns does not match. The shaded areas shown in Figure 4 are the portions of the DRAM that can't be used because of the difference in the number of rows and columns. Table 1 shows an example of redundant addressing. If bit 23 is set to equal bit 22, it can serve as both the 12th row-address on the 16 Meg and the 11th column-address on the 4 Meg.

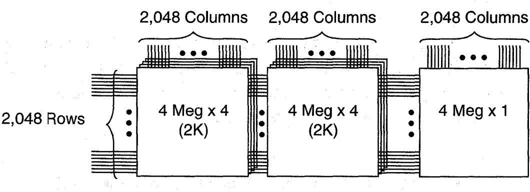

Figure 3

SUMMARY

1. JEDEC has approved two refresh standards at the 16 Meg level, 2K and 4K.
2. 2K refresh is 2,048 cycles in 32ms; 4K refresh is 4,096 cycles in 64ms.
3. Devices with 4K refresh cut current consumption by 20mA under worst-case operating conditions.
4. Devices with 4K refresh have half the page depth of a 2K device.
5. Existing 5V standard modules generally will use the 2K refresh standard DRAM.

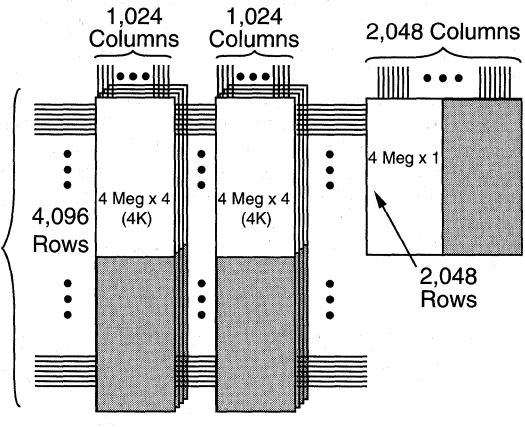

Figure 4

Table 1
ADDRESS MULTIPLEXING ASSIGNMENT FOR DRAM ROWS AND COLUMNS

DRAM Adress		A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
Memory Controller Address	Column	1	2	3	4	5	6	7	8	9	20	23	
	Row	10	11	12	13	14	15	16	17	18	19	21	22

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TECHNICAL NOTE

LOW-POWER DRAMS vs. SLOW SRAMS FOR MAIN MEMORY

INTRODUCTION

The market for portable computers such as notebooks, laptops and palmtops is extremely competitive and fast-paced. Designers of these systems are continually trying to minimize power, cost and size without compromising performance. One of the most challenging areas is memory design. To meet their design constraints, manufacturers are using either low-power DRAMs or slow SRAMs for memory. This technical note discusses memory design and the trade-offs associated with each of these types of memory.

LPDRAMs AND SLOW SRAMs

Users of portable devices want long battery life. Reducing power consumption to meet this need is critical. This is why portables use low-power extended refresh DRAMs (LPDRAMs) instead of standard DRAMs. A standard DRAM has standby currents of 3mA at a 15µs refresh cycle. LPDRAMs have standby currents ranging from 1mA to 200µA, and a refresh interval of 125µs (extended refresh).

LPDRAMs offer a very low-power standby power mode called BATTERY BACKUP (BBU) mode. BBU is the lowest DRAM power mode possible that still retains data. It consists of a $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) REFRESH cycle at the slowest possible cycle rate.

Some designers have used slow SRAMs in their designs since they offer low standby currents. Slow SRAMs are usually defined as SRAMs with a cycle speed of 80ns or slower. They have low standby currents when compared to standard DRAMs.

A standard memory configuration was chosen in order to compare the two types of memory. In portables, a 2MB memory in a x16 configuration is quite common. Memory will typically be a 4 Meg DRAM (x4 or x8) or a 1 Meg SRAM (x8). These memory arrays are compared in the following paragraphs and in Table 1 on the next page.

COST

In the highly competitive notebook market, reduction of cost is crucial. Because an SRAM bit cell uses four times as many transistors as a DRAM, the amount of silicon area used is much larger. Cost is proportional to silicon area, so for a given amount of memory the SRAM takes up more area and costs more. This is clearly seen in the marketplace since 256K SRAMs are more expensive than 256K DRAMs, 1 Meg SRAMs are more expensive than 1 Meg DRAMs, etc.

Of course, the size of a chip can be increased only so far before yield drops. When 4 Meg DRAMs were the highest density DRAM being manufactured, only 1 Meg SRAMs were available. A designer would only need one-fourth the number of 4 Meg DRAM parts over 1 Meg SRAMs. Table 1 compares the relative cost of several arrays; DRAMs always have the cost advantage.

SIZE AND WEIGHT

Typically, DRAMs are a generation ahead of SRAMs and are thus a factor of four ahead in density. This is because SRAMs take up much more silicon die area for a given memory density. For a typical memory size, SRAMs require four times as many devices and four times the board area (see Table 1).

DRAMs use multiplexed row and column addressing whereas SRAMs use unmultiplexed addressing. For an identical size of memory, DRAM packages use less pins and are smaller. This contributes to their effectiveness in minimizing space.

A designer should be cautious in choosing a slow SRAM for a portable application due to the board space required to implement the memory system. Similarly, the increased number of devices will make the portable heavier.

POWER

One of the main problems with notebook computers today is that the battery life is too short. Even with the large batteries used today, battery life can be less than two hours–users are demanding eight hours or more.

Slow SRAMs have an advantage in standby and active currents (typical). As you can see from Table 1, slow SRAM standby current can be much lower than that of DRAMs. This is because only a portion of the memory is accessed at any given time, so much of the memory is in standby mode.

SUMMARY

The portable market is so competitive that cost is usually the overriding consideration. Even if battery time can be extended slightly with slow SRAMs, cost and increased board space usually prohibit their use. DRAMs have been and will likely continue to be the part of choice in portable applications.

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Table 1
2MB, 16-BIT-WIDE MEMORY

PART TYPES		1 MEG x 4 DRAMS	512K x 8 DRAMS	128K x 8 SLOW SRAM[4]	128K x 8 SLOW SRAM[5]	UNITS
Number of Devices Required		4	4	16	16	No. of Devices
Total Cost[1]		1.0	1.1	4.3	4.3	Relative Cost
Minimum Speed		70	70	85	85	ns
Standby/BBU Current[2]	(MAX)	1.2	1.2	1.6	0.8	mA
	(Typical)	600	600	32	32	µA
Active Icc Current[2, 3]	(MAX)	240	160	140	140	mA
	(Typical)	141	94	90	90	mA
Minimum Board Space Used		0.9	1.3	7.4	7.4	(TSOP) in²
Weight[6]		1.0	1.4	5.8	5.8	Relative Weight

NOTE:
1. Costs are relative to the 1 Meg x 4 DRAM.
2. Assumes an 80ns part in FAST PAGE MODE for DRAMs, 85ns part for SRAMs.
3. For the x8 devices, only a portion of the array is active at any one time.
4. Standard slow SRAMs
5. Low-power slow SRAMs
6. Weight is relative to the 1 Meg x 4 DRAM.

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TECHNICAL NOTE

SELF REFRESH DRAMS

INTRODUCTION

DRAM memories targeted for the low-power, portable market are providing several new features to help maximize power savings. One of these new features is the SELF REFRESH mode. DRAMs having this new feature are referred to as SELF REFRESH DRAMs and provide the user with a very low-current, data-retention mode.

This mode has been approved by JEDEC and is quickly becoming an industry-standard feature. Most 3.3V DRAMs will be offered with this feature, as will many future 5V DRAMs.

SELF REFRESH DRAMs vs LPDRAMs

Low-power, extended-refresh DRAMs (LPDRAMs) have the same functionality as a standard DRAM, except they have been tested to meet the lower CMOS standby current and the extended refresh specifications. SELF REFRESH DRAMs, on the other hand, require additional circuitry be added to the standard DRAM to perform the SELF REFRESH function.

SELF REFRESH MODE

SELF REFRESH mode provides the DRAM with the ability to refresh itself while in an extended standby mode (sleep or suspend). It is similar to the extended refresh mode of an LPDRAM except the SELF REFRESH DRAM utilizes an internally generated refresh clock while in the SELF REFRESH mode.

During a system's suspend mode, the internally generated refresh clock on the DRAM replaces the DRAM controller refresh signals. Therefore, it is no longer necessary to power-up the DRAM controller while the system is in the suspend mode. Consulting the devices' data sheets will determine the power savings achieved.

USING SELF REFRESH

SELF REFRESH introduces the new parameters ᵗRASS, ᵗCHD and ᵗRPS. These new parameters are shown in Figure 1. The DRAM's SELF REFRESH mode is initiated by executing a $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH cycle and holding both $\overline{RAS}$ and $\overline{CAS}$ LOW for a specified period. The industry standard for this value is 100µs minimum (ᵗRASS). The DRAM will remain in the SELF REFRESH mode while $\overline{RAS}$ and $\overline{CAS}$ remain LOW. Once $\overline{CAS}$ has been held LOW for ᵗCHD, $\overline{CAS}$ is no longer required to remain LOW and becomes a "don't care."

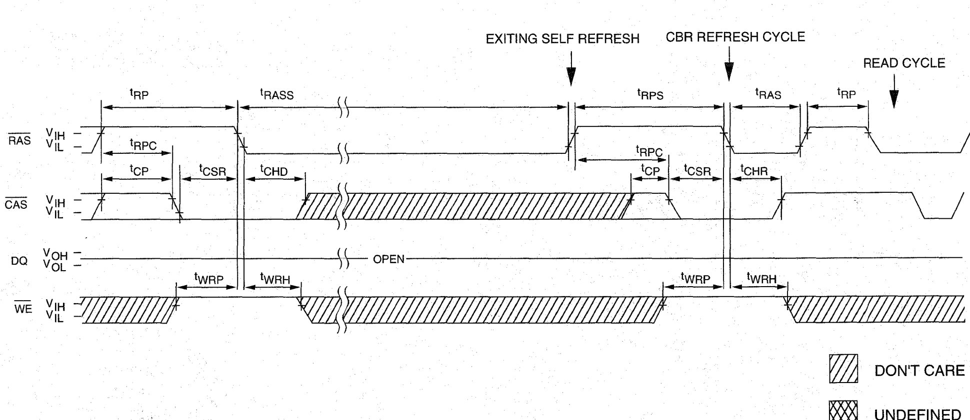

Figure 1
SELF REFRESH CYCLE UTILIZING DISTRIBUTED CBR REFRESH

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The SELF REFRESH mode is terminated by taking RAS HIGH for ᵗRPS (the minimum time of an operation cycle). Once the SELF REFRESH mode has been terminated, the user can access the DRAM normally.

HOW IS SELF-REFRESH DONE?

SELF REFRESH can be implemented on the device in two ways. One method utilizes a distributed method and the second uses a wait and burst method. Micron devices use the distributed method.

Devices that utilize the distributed method will refresh the rows at a regular rate, utilizing the CBR REFRESH counter to turn on rows. In a system that utilizes distributed CBR REFRESH as the standard refresh, accesses to the DRAM can begin as soon as SELF REFRESH is exited. The first CBR pulse should occur within the time of the external refresh rate prior to active use of the DRAM to ensure maximum data integrity and must be executed within three external refresh rate periods. Since CBR REFRESH is commonly implemented as the standard refresh, this ability to access the DRAM immediately after exiting SELF REFRESH is a big benefit over the burst scheme described later. If anything other than CBR REFRESH is used as the standard refresh, a burst of all rows needs to be executed when exiting SELF REFRESH. This is because the CBR counter and the DRAM controller counter will not likely be at the same count. If they're not at the same count and both are being used in the distributed method, then refresh will be violated and data will eventually be lost.

An alternative way to implement SELF REFRESH is to use an internal burst refresh scheme. Instead of turning on a row at regular intervals, a circuit would sense when the array needs to be refreshed and then sequence through the rows until all had been refreshed. When exiting a burst type SELF REFRESH, the entire array must be refreshed before any accesses are allowed, regardless of the type of refresh used (see Figure 2). This full burst is necessary because you may have exited SELF REFRESH just before the entire array was going to be refreshed. If the burst is not performed when exiting this type of SELF REFRESH, you may violate refresh requirements and lose data.

Micron's devices allow you to access the DRAM as soon as SELF REFRESH is exited, while other manufacturers' devices may require a full burst when exiting, regardless of the refresh used. To prevent possible compatibility problems, you may want to design the controller to perform the burst when exiting SELF REFRESH.

SUMMARY

1. SELF REFRESH mode allows additional power savings for portable applications since the DRAM controller is no longer required to remain powered-up while the system is in the suspend mode.
2. The mode is initiated by executing a CBR REFRESH with RAS and CAS remaining LOW for at least 100µs.
3. The SELF REFRESH mode remains active until RAS is taken HIGH.
4. You may access the DRAM as soon as SELF REFRESH has been exited, provided you use distributed CBR REFRESH as the standard refresh.

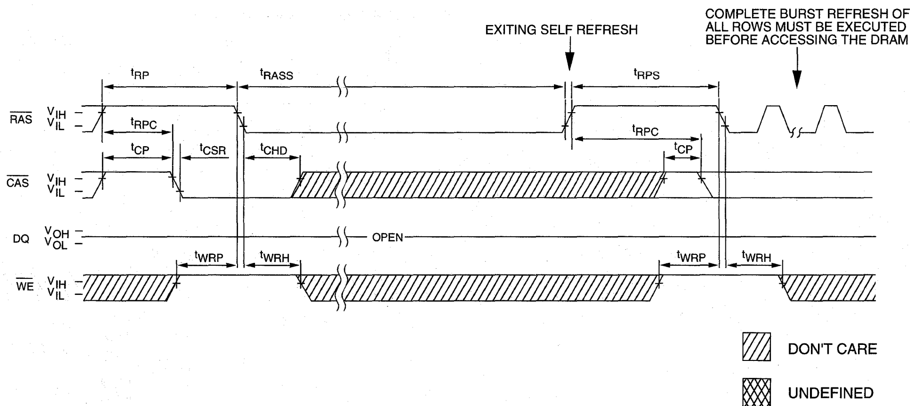

Figure 2
SELF REFRESH CYCLE UTILIZING BURST REFRESH SCHEME

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TECHNICAL NOTE

REDUCE DRAM CYCLE TIMES WITH EXTENDED DATA-OUT

INTRODUCTION

As system speeds increase, DRAM manufacturers are developing methods to decrease the cycle times of DRAMs. The most common version of DRAM is FAST PAGE MODE (FPM) but the addition of a feature known as extended data-out (EDO) may become more common because it allows shorter page cycle times with only a minor functional change from FP. Because the device with EDO doesn't turn off the output drivers when $\overline{CAS}$ goes HIGH, it can have a shorter cycle time than FP.

EDO OFFERS ADVANTAGES

- It has a shorter PAGE READ cycle time than FPM devices.
- Data is valid on the falling edge of $\overline{CAS}$, so the designer can use that edge to strobe data.
- A 70ns EDO device has the same PAGE READ cycle time as a 40/50ns FPM DRAM.
- Implementing EDO in place of FPM devices in a system can be as easy as knowing when the bus needs to be deactivated and using $\overline{OE}$ or $\overline{WE}$ instead of $\overline{CAS}$ to accomplish it.

This article first covers some basic differences between FPM and EDO during a PAGE READ cycle. Then a comparison of cycle times between FPM and EDO is done, followed by a few examples under different address setup conditions. When moving from a PAGE READ into a PAGE WRITE, the timing differs slightly between FPM and EDO; this difference is discussed. Finally, the issues involved when replacing an FPM device with an EDO device are addressed.

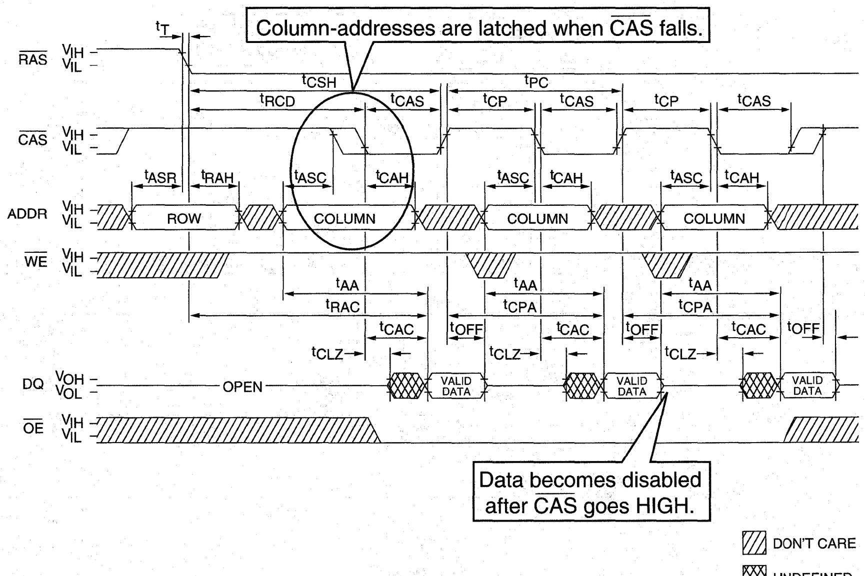

Figure 1
FPM READ CYCLE

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BASIC DESCRIPTION

FPM and EDO allow fast data operations within a row. The differences are in the deactivation of data-out when CAS goes HIGH and the operation of OE and WE. The following section highlights differences between the FPM and EDO when reading within a page.

FPM

Characteristics:

- The column-address is latched when CAS falls.
- The output drivers are turned off when CAS goes HIGH.
- Minimum FPM READ cycle time is $^tPC = {}^tCPA + {}^tT$, ($^tCPA = {}^tAA + {}^tT$)

The cycle begins with RAS strobing-in a row address, followed by CAS strobing-in a column-address. To continue to access columns within that row, CAS is toggled as addresses change.

Figure 1 shows a typical FPM READ cycle. The column-address is latched into the part when CAS falls, so column-address setup and hold times are referenced to the falling edge of CAS. Notice ^tOFF; this specification tells you that CAS going HIGH turns off the output drivers.

EDO

Characteristics:

- The column-address is latched when CAS falls.
- The output drivers are not turned off when CAS goes HIGH.
- Minimum EDO read cycle time is determined by the greater of the two equations below.

Equation 1: $^tPC = {}^tCAS + {}^tCP + 2{}^tT$
Equation 2: $^tPC = {}^tCPA - ({}^tCP + {}^tT)$

- OE and CAS work together to enable and disable the outputs.
- WE can disable the outputs.

EDO allows fast access within a row and uses CAS to latch the column-address, as does FP, but does not turn off the output when CAS goes HIGH. This last feature allows EDO to cycle faster than FPM because the user does not have to wait for valid data to appear before starting the next access. In other words, data can appear after CAS has been pulled HIGH, and it will stay valid for 5ns after CAS transitions LOW again (^tCOH), as shown in Figure 2. The output will deactivate when both RAS and CAS are

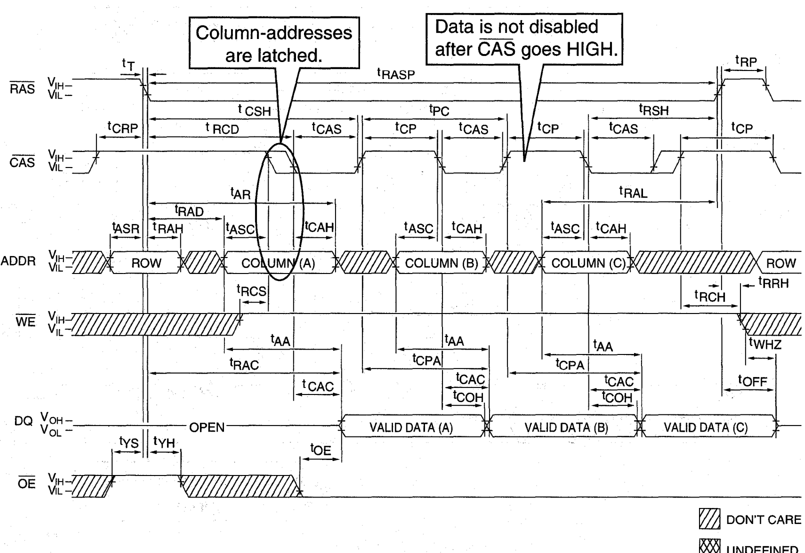

Figure 2
FPM READ WITH EDO

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HIGH, so ^{t}OFF will now be referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{OE}$ will also deactivate the outputs, as shown in Figure 3. In order to accomodate systems where $\overline{OE}$ is tied LOW, $\overline{WE}$ now has the ability to turn off the output drivers as well (see Figure 4).

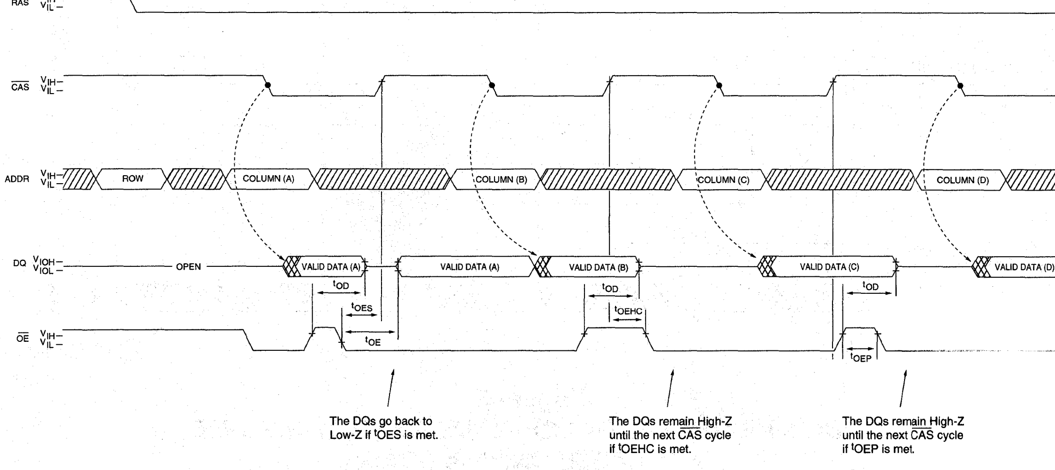

Figure 3
OUTPUT ENABLE AND DISABLE USING $\overline{OE}$

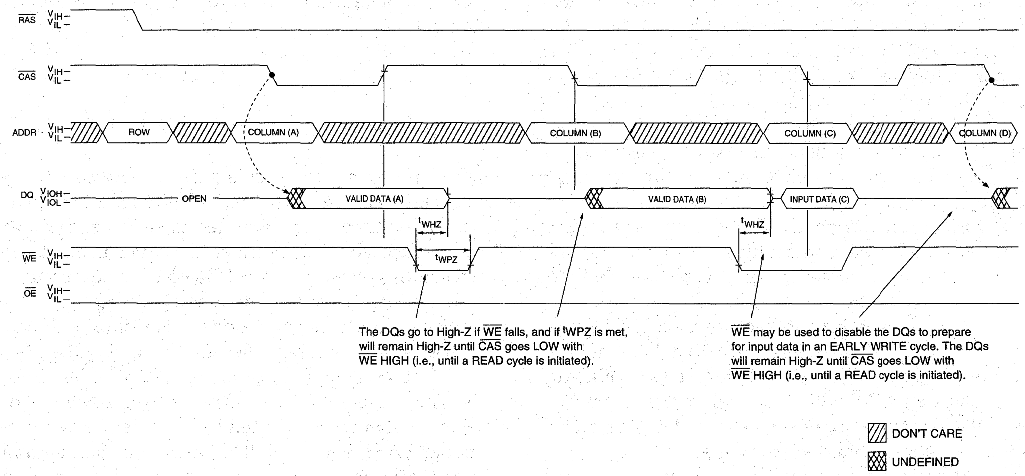

Figure 4
OUTPUT DISABLE USING $\overline{WE}$

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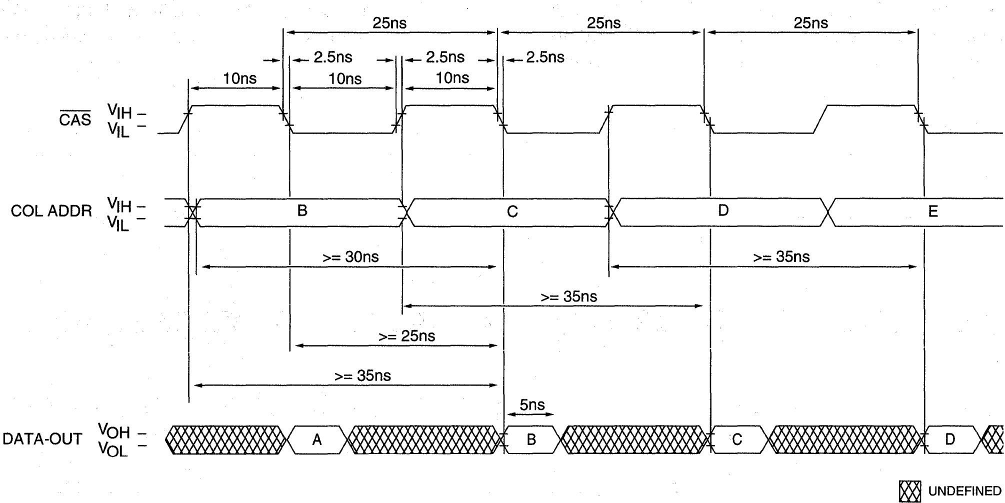

Figure 5
EDO MINIMUM FAST-PAGE-MODE READ CYCLE TIME AVAILABLE ON 60ns DRAMs

PAGE READ CYCLE TIMES

This section examines the different cycle times of FPM and EDO to see how they are generated. Figure 1 shows that $\overline{CAS}$ must stay LOW until data-out becomes valid (if $\overline{CAS}$ goes HIGH before valid data, then the output buffers would turn off). The longest access time specified for the device is from $\overline{CAS}$ HIGH to data-out (^tCPA). $\overline{CAS}$ can't go HIGH before ^tCPA, or data-out will not fire. Add a transition time to pull $\overline{CAS}$ HIGH and you have the cycle time $^tPC_{FPM}$ = ^tCPA + ^tT.

EDO works a bit differently. ^tCPA is still the longest access time, but is no longer the limiting parameter in cycle time. This is because some of this access time includes $\overline{CAS}$ precharge ($\overline{CAS}$ HIGH time). In FP, you can't bring $\overline{CAS}$ HIGH before data is valid because $\overline{CAS}$ HIGH turns data off. Since $\overline{CAS}$ HIGH doesn't turn off data in the EDO device, you can bring $\overline{CAS}$ HIGH before data is valid and begin precharging $\overline{CAS}$ while you wait for data-out. This overlap of $\overline{CAS}$ precharge and getting data-out means ^tCPA is no longer the limiting parameter.

The theoretical minimum page-mode cycle time is determined by one of the two equations below, whichever is greater (see Figure 2). ^tLH is the $\overline{CAS}$ LOW-to-HIGH transition time and the ^tHL is the $\overline{CAS}$ HIGH-to-LOW transition time.

Equation 1: $^tPC = {^tCAS} + {^tCP} + {^tLH} + {^tHL}$

Equation 2: $^tPC = {^tCPA} - ({^tCP} + {^tHL})$

The minimum cycle is achieved by providing valid column addresses early enough that ^tAA is not limiting. In the past, transition times were assumed to be 5ns each for the purpose of specifying cycle times. However, in many cases, the transitions between 0.8 and 2.4 volts do not require 5ns, so the EDO devices allow for 2ns transitions.

For example, a page-mode cycle time of 25ns can be achieved when using Micron 60ns EDO DRAMs with a ^tCPA of 35ns when transitions are 2.5ns or less (see Figure 5). This represents a 40 to 60 percent improvement over the same cycle times provided by 60ns devices with conventional FAST PAGE MODE operation. Similar improvements are provided on the 50ns and 70ns speed grades, which have theoretical minimum cycle times of 20ns and 30ns, respectively.

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EXAMPLES: EDO AND FP

The table below compares page READ cycles of FPM and EDO under two different conditions: minimum column-address setup and maximum column-address setup time. The timing diagrams for the following examples assume that $\overline{RAS}$ is already LOW, $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW. A 70ns DRAM is used with the following timing:

DESCRIPTION	FP	EDO
^{t}PC (MIN)	45	30
^{t}CAS (MIN)	20	12
^{t}CLZ (MIN)	0	0
^{t}OFF	0-20	0-20
^{t}T	5	5

Figures 6 and 7 show FPM and EDO cycles with plenty of address setup time. On an FPM device with plenty of address setup time, we can operate at ^{t}PC = 45ns (the minimum allowed), and data is valid for 5ns.

EDO under the same address setup time looks different (see Figure 5). Now the minimum cycle time is 32ns. Notice that data doesn't appear on the bus until you are already into the second access (8ns of $\overline{CAS}$ precharge for the next cycle is already completed when data appears). This is the overlap that allows the shorter cycle time. ^{t}PC is 32ns and data is valid for 12ns.

Under these conditions, EDO cuts the cycle time over a FPM device by 29 percent, or increases burst rate by 41 percent (22 MHz to 31 MHz). In addition, even with the shorter cycle time, data-out is valid for 12ns on the EDO as opposed

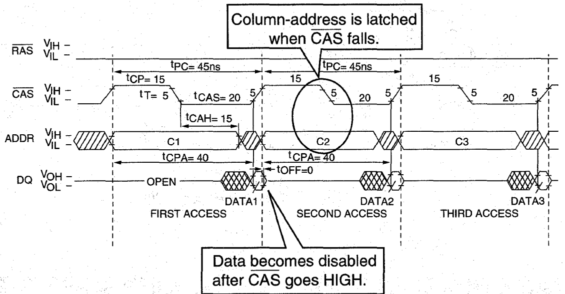

Figure 6
FPM PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 45ns; DATA VALID FOR 5ns

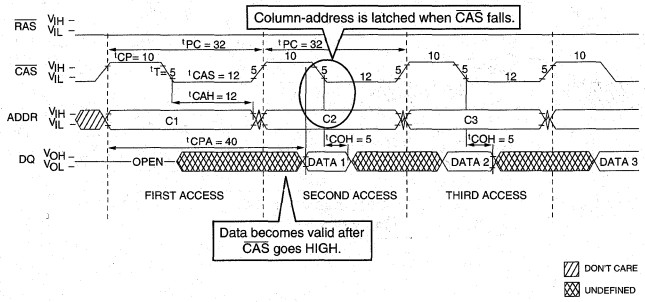

Figure 7
EDO-PAGE READ CYCLE WITH MAXIMUM ADDRESS SETUP
^{t}PC = 32ns; DATA VALID FOR 12ns

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to only 5ns on the FPM device. We could get more performance by using shorter transition times on the EDO device, but we used 5ns to make the comparison between FPM and EDO easily understandable.

Figures 8 and 9 show FPM and EDO cycles with minimum address setup time. In this case, the address becomes valid coincident with CAS falling. For FP, data won't be valid for ᵗAA(35ns), so CAS must be held LOW until that time (see Figure 8). Since the minimum CAS HIGH time is 10ns, the cycle time is 50ns (ᵗAA + ᵗCP + ᵗT). Data-out is valid for 5ns.

Looking at EDO under the same conditions, (Figure 9) it still takes ᵗAA (35ns) after the addresses are valid to get valid data-out, but now you don't have to wait before pulling CAS HIGH. Notice that CAS has been pulled HIGH and precharge has been completed for the next cycle, before Data 1 appears on the bus. Just before data becomes valid, CAS drops and the second address is latched. Again, there is an overlap of starting one cycle and finishing the other. Now ᵗPC = 32ns, and data-out is valid for 7ns.

In this case, EDO cycle time is 36 percent less than the FPM cycle time (providing a 55 percent improvement in burst rate); EDO data is valid 2ns longer.

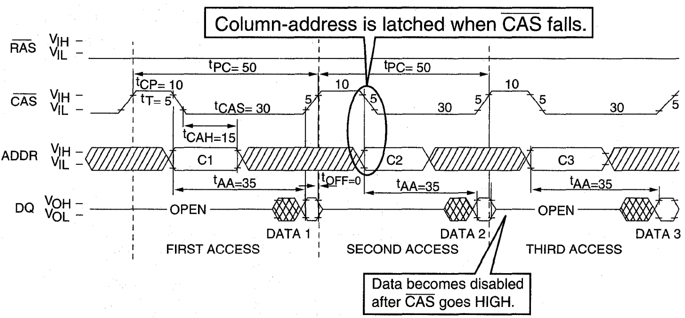

Figure 8
PAGE READ WITH MINIMUM ADDRESS SETUP
ᵗPC = 50ns; DATA VALID FOR 5ns

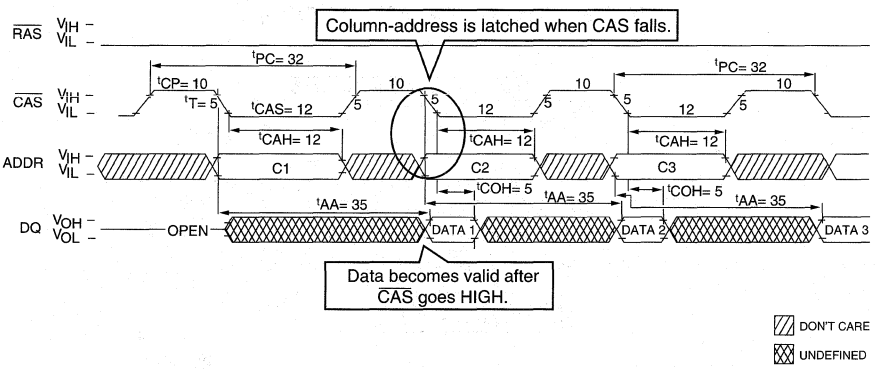

Figure 9
EDO-PAGE READ CYCLE WITH MINIMUM ADDRESS SETUP
ᵗPC = 32ns; DATA VALID FOR 7ns

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These examples should point out another big advantage of EDO. Not only can you operate at a shorter cycle time, but data is available longer for the system to sample. Since data is guaranteed to be valid as $\overline{CAS}$ falls, that edge may be used to sample data.

70ns EDO INSTEAD OF 40/50ns DRAMs

EDO can provide the FPM READ speed of a 40/50ns DRAM. Even though a 40/50ns DRAM has a 40/50ns ^{t}RAC, the FPM READ cycle time is 30-35ns, which is the same page READ cycle time as that of a 70ns EDO device.

EASY TO IMPLEMENT

An additional benefit of EDO is the ease of implementation. PAGE READ or WRITE cycle time is cut but the major difference between FPM and EDO is that the FPM device will stop driving data-out when $\overline{CAS}$ goes HIGH and the EDO device must have the correct combination of $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$ and $\overline{WE}$ to deactivate the output. This means that any time the designer is counting on $\overline{CAS}$ by itself to turn off the output drivers, bus contention may occur if something else tries to drive the bus. This may occur in the following situations:

- PAGE interleave memory banks
- Moving from PAGE READ directly into a PAGE WRITE (within the same page)
- Whenever anything other than the DRAM is driving the bus, and $\overline{OE}$ and $\overline{RAS}$ are LOW while $\overline{CAS}$ is HIGH

(This last case is uncommon and should not mandate a change for most systems.) Interleaved memory need only make use of $\overline{OE}$ or $\overline{WE}$ instead of $\overline{CAS}$ when turning off the output drivers; then EDO can be used in place of FPM DRAMS.

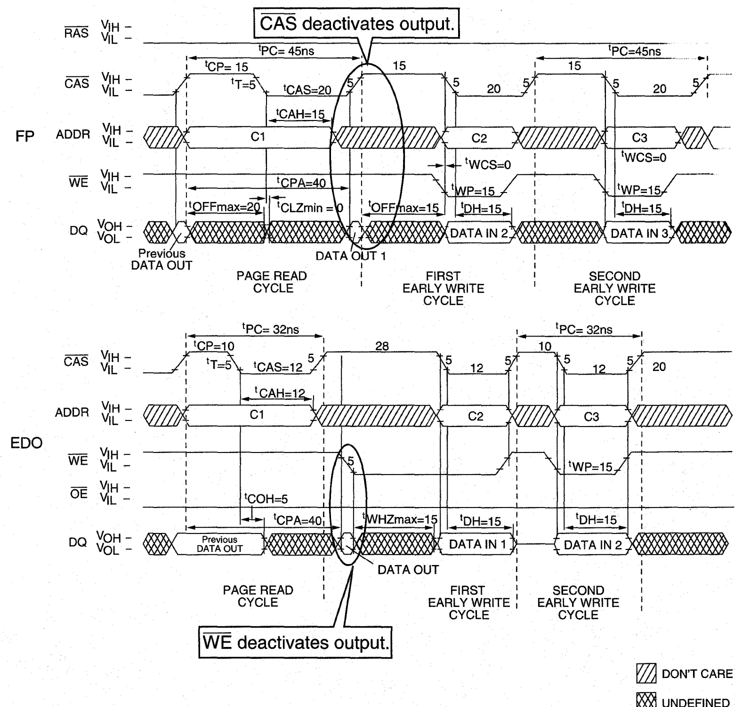

Figure 10
EXAMPLE FPM AND EDO READ TO WRITE CYCLES
^{t}PC = 45ns

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READ TO WRITE CYCLES

Since $\overline{CAS}$ doesn't turn off the output devices on an EDO device, caution should be used when turning the bus around on a shared IO device. To demonstrate the difference, Figure 8 shows the transition from a PAGE READ to a PAGE EARLY WRITE on the same page. When using the FPM version, $\overline{OE}$ can be tied LOW and $\overline{CAS}$ can be used to deactivate the output. Notice that $\overline{OE}$ is also tied low on the EDO device and this cycle is still possible.

SUMMARY

EDO is simply a modified FPM cycle and can be used in systems to increase performance. It allows system designers to improve their cycle times and system performance since data is present for a much longer time, even during short cycle times. Because each generation device has different timing limitations, be sure to consult the data sheet for exact timing.

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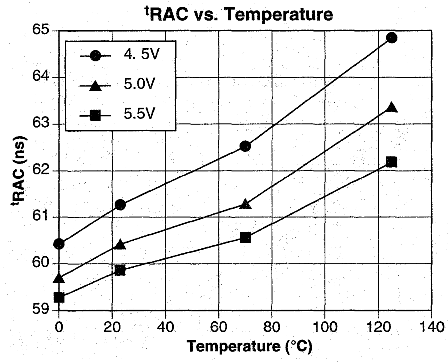
TECHNICAL NOTE

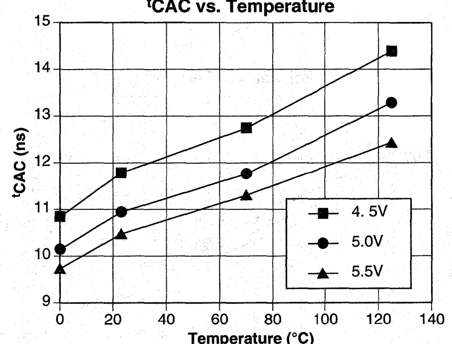
256K x 16 DRAM TYPICAL OPERATING CURVES

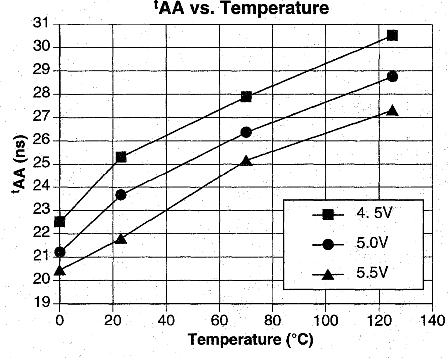
INTRODUCTION

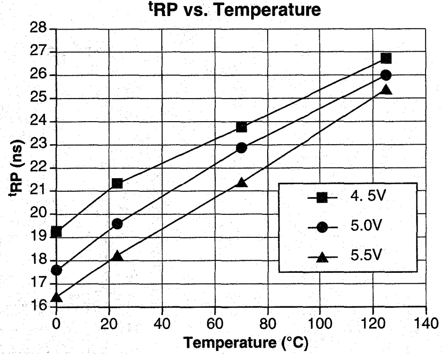
These curves represent the typical operating characteristics of Micron's 70ns 256K x 16 DRAMs. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets.

256K x 16 OPERATING CURVES









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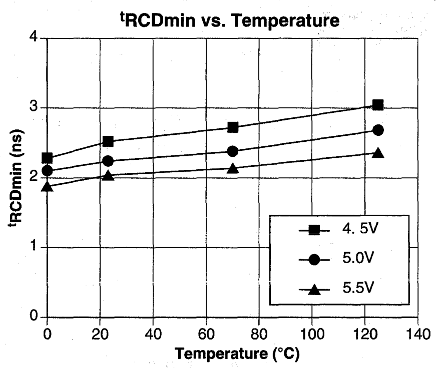
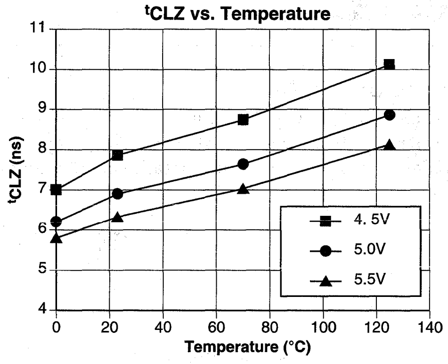
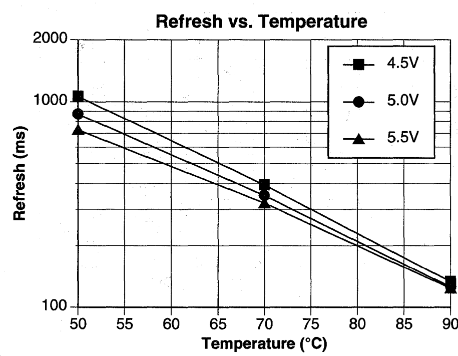
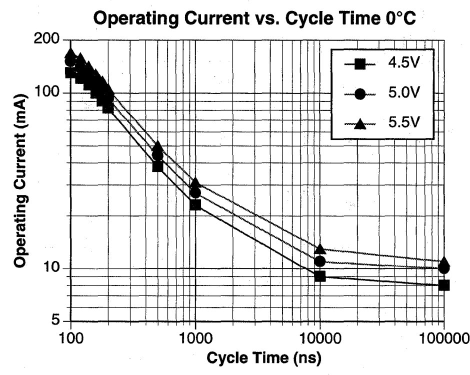
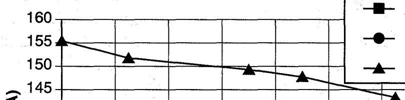
256K x 16 OPERATING CURVES (continued)

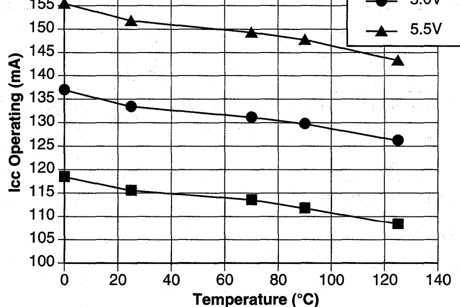












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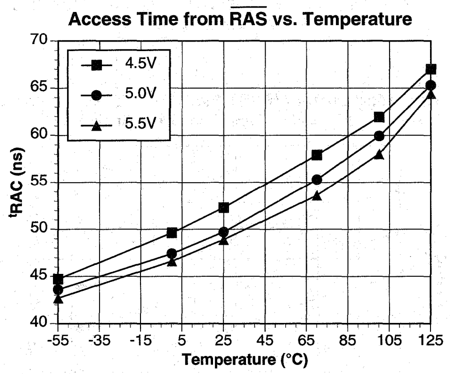
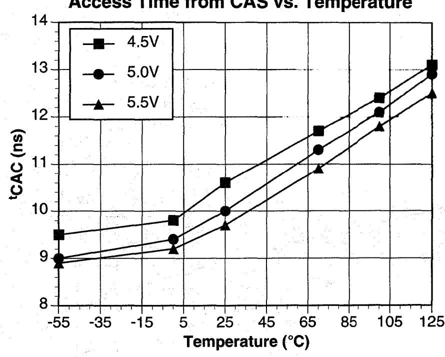
4 MEG DRAM TYPICAL OPERATING CURVES

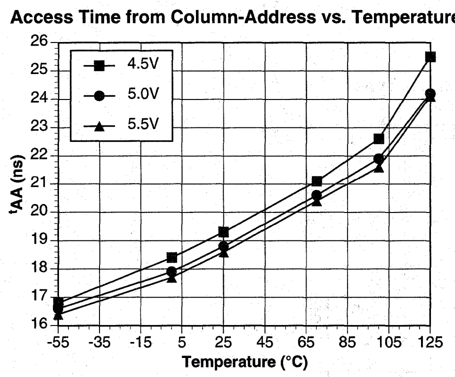
INTRODUCTION

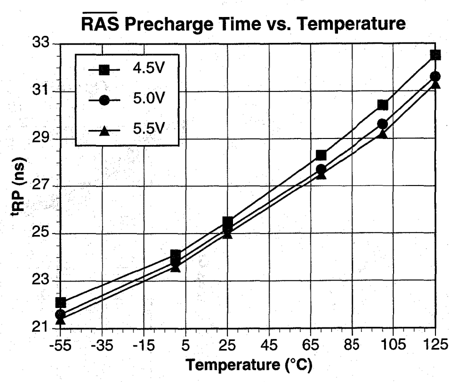
These curves represent the typical operating characteristics of Micron's 70ns 4 Meg DRAMs. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets.

5V PRODUCT DC AND AC PARAMETER PERFORMANCE









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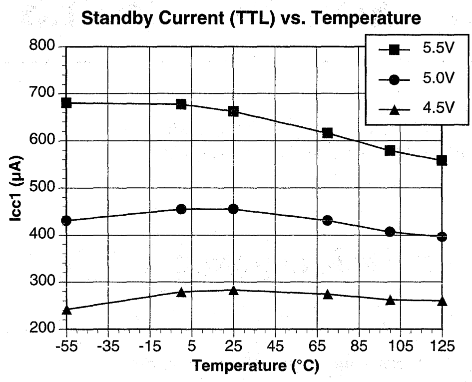

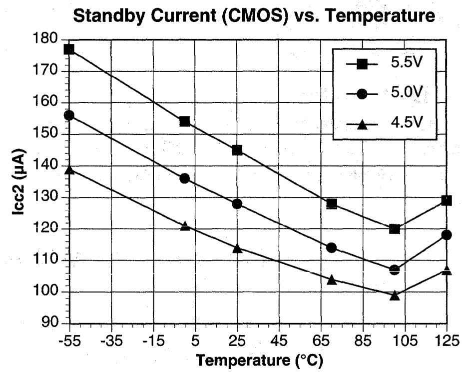

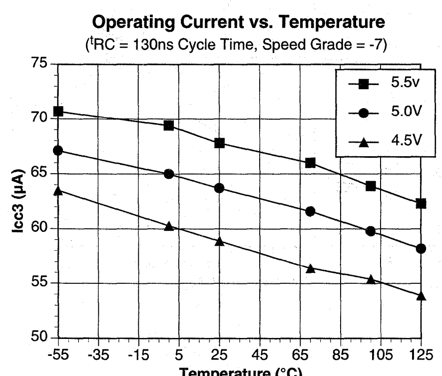

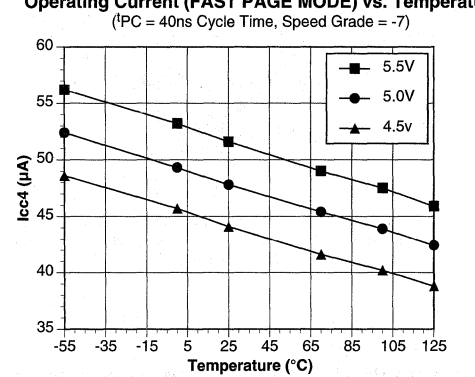

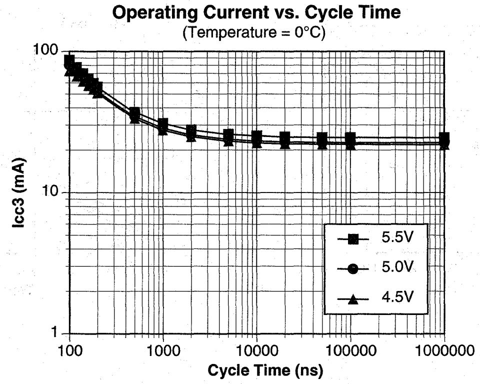

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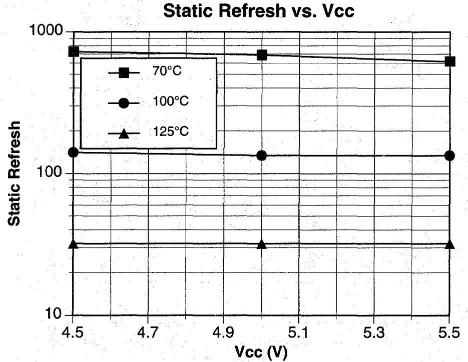

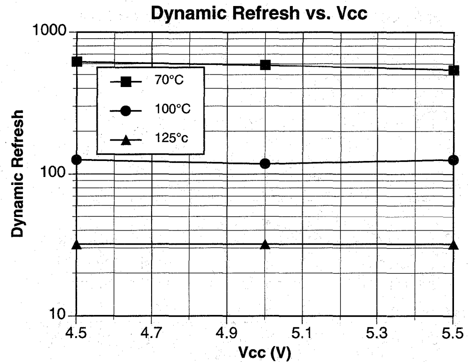

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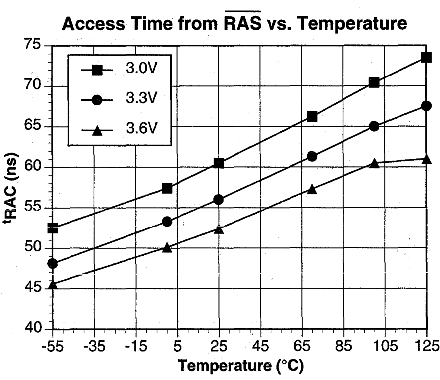
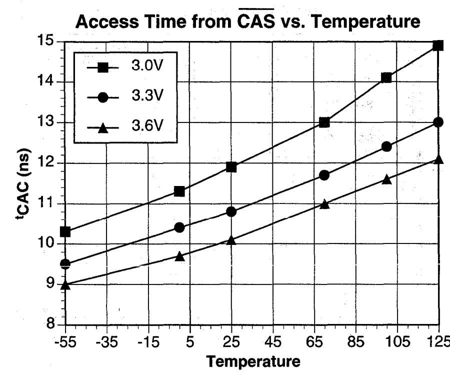
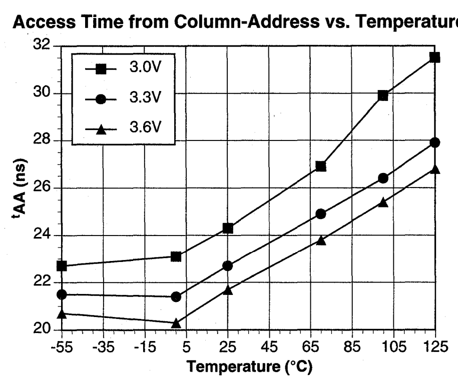
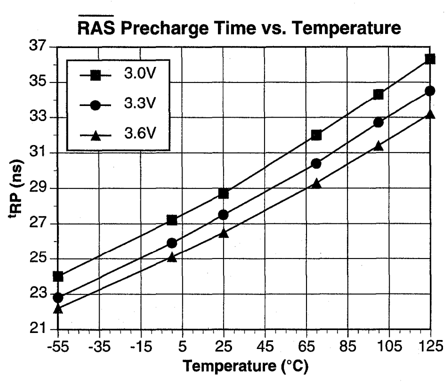
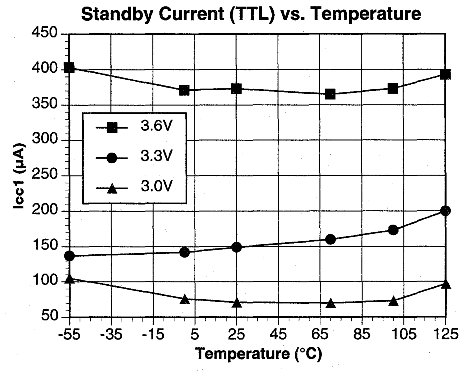
3.3V PRODUCT DC AND AC PARAMETER PERFORMANCE

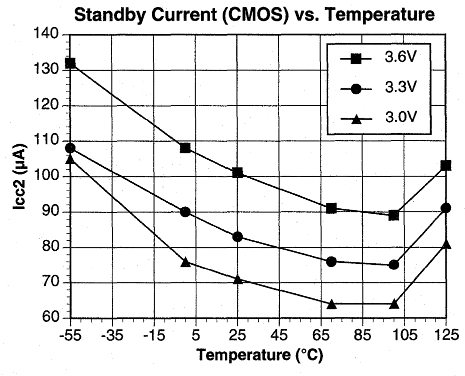












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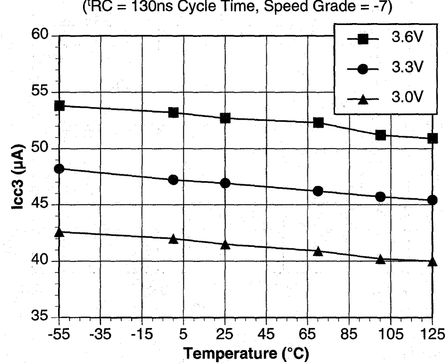
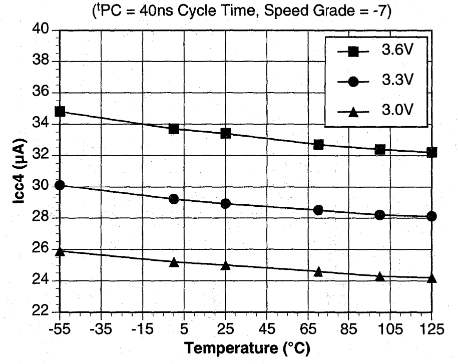
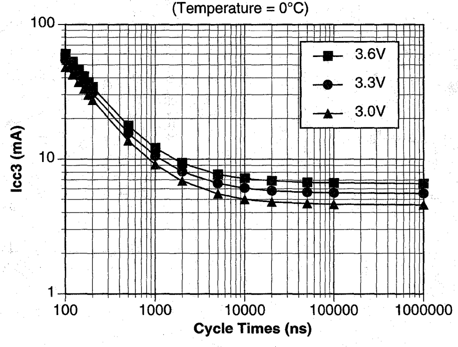
3.3V PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)







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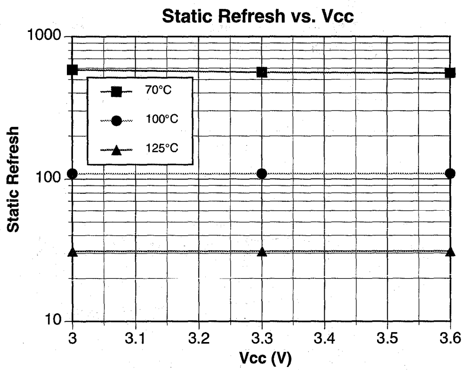
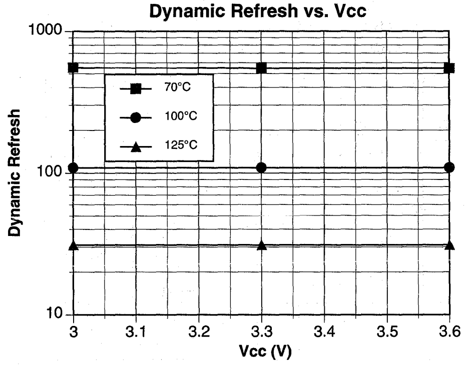
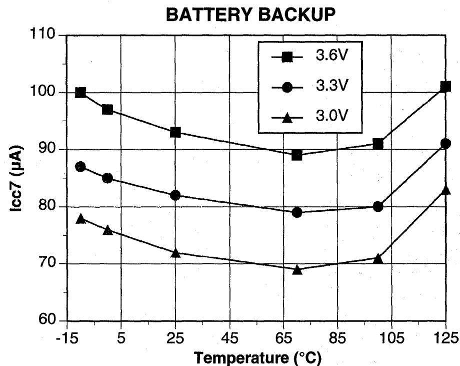
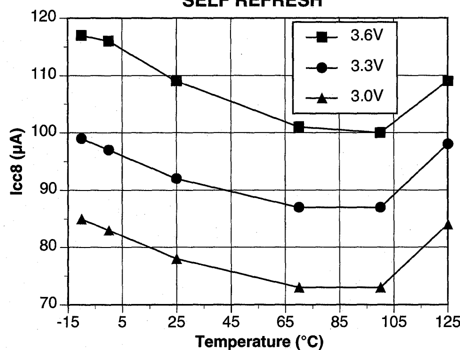
3.3V PRODUCT DC AND AC PARAMETER PERFORMANCE (continued)









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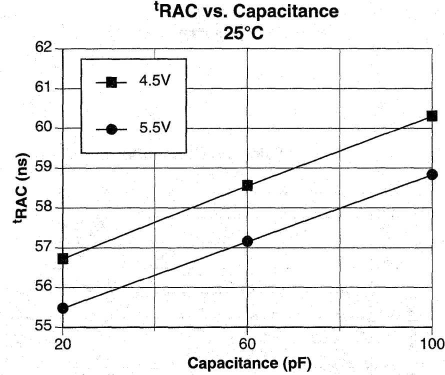
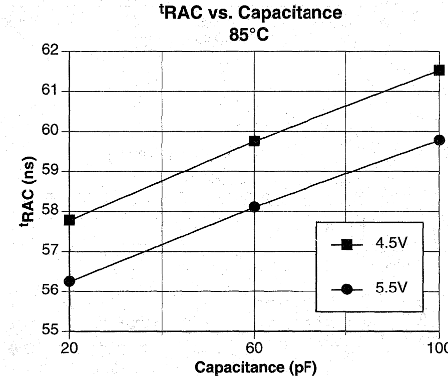
TECHNICAL NOTE

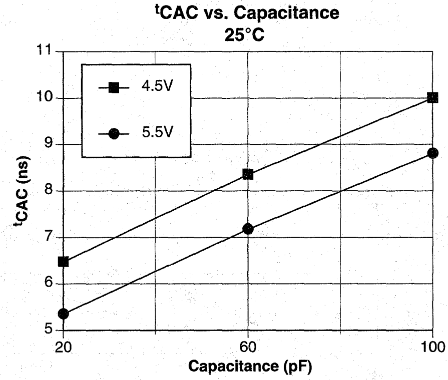
4 MEG DRAM—ACCESS TIME vs. CAPACITANCE

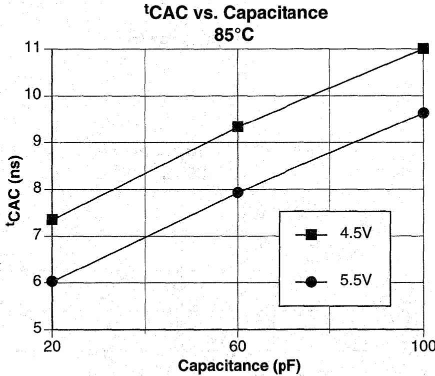
INTRODUCTION

These curves for the 4 Meg DRAM show typical access times with different capacitive loading. For worst-case design limits, the system designer should refer to the individual data sheets.









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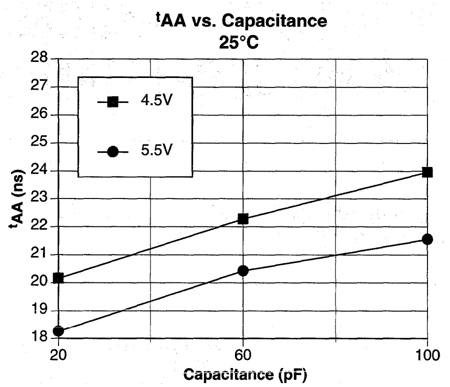

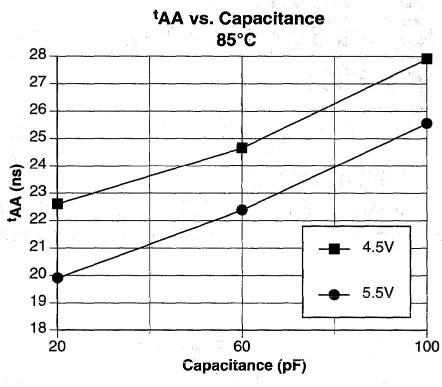

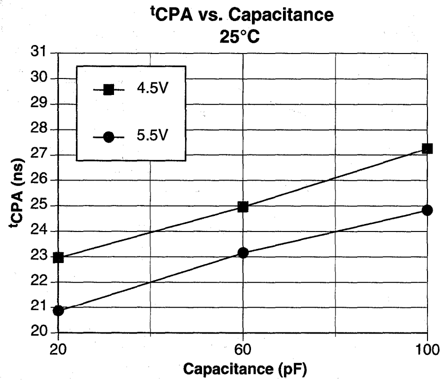

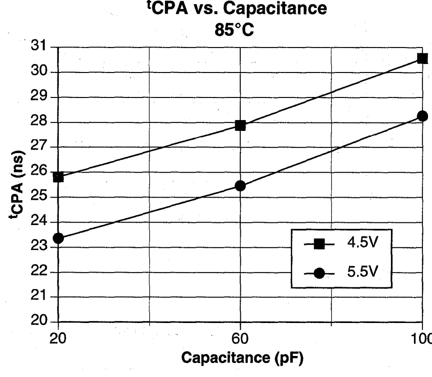

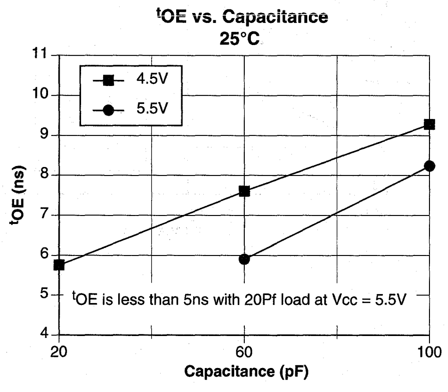

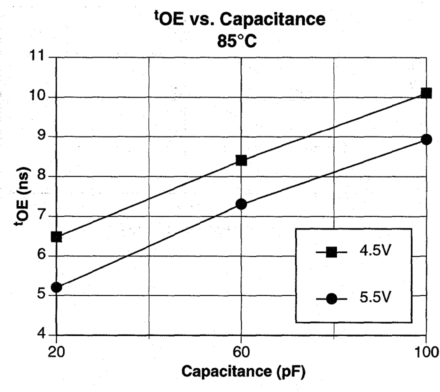

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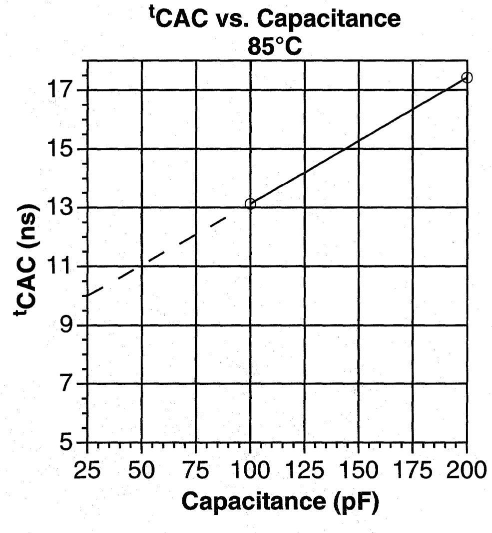
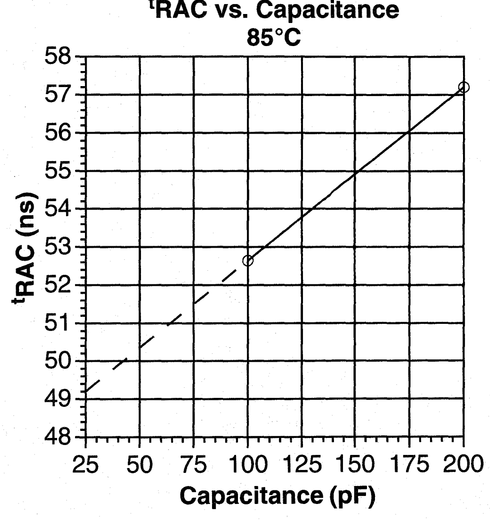
TECHNICAL NOTE

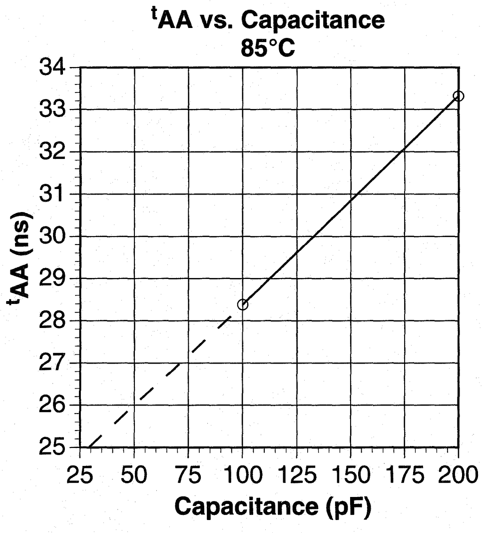
256K x 16—ACCESS TIME vs. CAPACITANCE

INTRODUCTION

These curves for the 256K x 16 DRAM show typical access times at Vcc = 4.5V with different capactive loading. For worst-case design limits, the system designer should refer to the individual data sheets.







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TECHNICAL NOTE

DRAM SOFT ERROR RATE CALCULATIONS

INTRODUCTION

Micron technical note TN-04-15, "DRAM Considerations for PC Memory Design", presents a discussion on the use of parity. This technical note may have led some readers to conclude that parity is no longer of value. Although this conclusion is understandable (see Figure 1), the fact is that the need for parity can be determined only after design goals have been thoroughly analyzed.

Herein lies the problem: how to get from point A (DRAM manufacturer's reported soft error rate [SER]) to point B (system mean time between failures [MTBF]). This article's purpose is to solve the problem by showing how to take SER data reported by the manufacturer and determine a system's memory susceptibility to DRAM soft errors.

The SER data for the Micron 4 Meg DRAM, as reported in the Micron *4 Meg DRAM Reliability Monitor* (dated 2/93), will be used throughout this article for illustrative purposes.

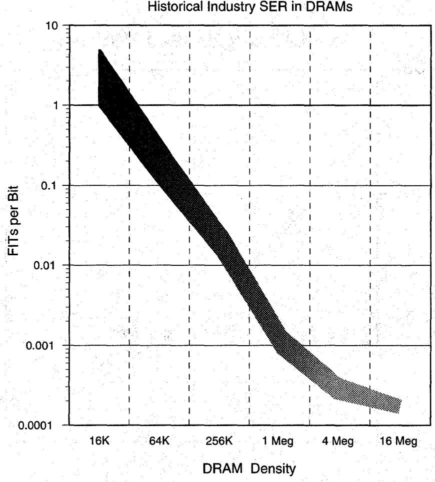

Figure 1
HISTORICAL DRAM SER

DRAM SER RATES

DRAM SER is a measurement of a DRAM's susceptibility to a nonrecurrent, single-bit output error. Although there is not a defined industry standard for measuring a component's SER, Micron has adopted a widely accepted methodology:

- Accelerated SER testing using an alpha radiation source.
- Realtime, system-level SER testing. Micron uses its AMBYX® intelligent burn-in and test system.

The accelerated test data provides the only practical, real time means to determine the relative increase or decrease in the component's SER for various test conditions.

Micron records a DRAM's realtime SER when the device is operating at a 5V Vcc with 15.625µs cycle rate (refresh rate). Micron's *4 Meg DRAM Reliability Monitor* lists an SER of 41 FITs at a 90 percent confidence level. A FIT is a failure in time (1 billion device hours).

SER CALCULATIONS - REFRESH MODE

To begin, let's examine a memory buffer using only one 4 Meg DRAM (1 Meg x 4) at a 15µs refresh rate. The system's MTBF-due-to-soft-error rate is the DRAM's SER rate, 41 FITs. Mean-time-between-failures is calculated by dividing one billion device hours by 41 FITs, which equals one error every 24,390,000 system hours or 2,784 years.

Now, let's take the previous example and add three additional 4 Meg DRAMs for a 16-bit-wide memory array (2MB). Since there are four components, the SER rate is increased by the same ratio in order to obtain a system hourly rating. The system's memory MTBF-due-to-soft-error rate is now one billion device hours divided by four devices (41 FITs per device), equaling one error every 6,098,000 system hours, or 696 years.

Seven, rather than three, additional 4 Meg DRAMs provide a 32-bit wide memory array (4MB). In this case, the system's MTBF-due-to-soft-error rate is one billion device hours divided by 8 devices (41 FITs per device), equaling one error every 3,048,800 system hours or 348 years.

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The previous calculations assume a single bank architecture. If any of the above examples had two banks, then SER would be twice as high and the MTBF would be half of the single-bank value. For example, a dual bank, 32-bit wide (8MB) memory system's MTBF-due-to-soft-error rate is one billion device hours divided by 16 devices (41 FITs per device), equaling one error every 1,524,400 system hours or 174 years.

SER CALCULATION - ACTIVE MODE

DRAM memory is not always in refresh mode. Rather, it is active (accessing data via READs and WRITEs) during a portion of its ON time. It is necessary to determine the memory's overall SER, or "operating SER," before determining a system's MTBF-due-to-soft-error rate during DRAM access.

First, the percentage of time the DRAMs are active and in refresh must be determined. The next step is to determine the refresh SER rate. As performed in the previous 32-bit, single-bank example using eight 4 Meg DRAMs, the refresh SER rate based on eight devices (41 FITs per device) is 328 FITs.

The active SER rate must now to be determined. This is where acceleration curves are required. Micron provides three types in the *4 Meg DRAM Reliability Monitor:* checkerboard pattern, solid ones pattern and solid zeros pattern. The graph that provides the worst-case slope, typically the checkerboard pattern, is usually selected.

Referring to the 5V checkerboard pattern curve from the Micron *4 Meg DRAM Reliability Monitor* (Figure 2), let's assume the DRAMs are being cycled at a 200ns (0.2µs) cycle rate. The alpha hits at 15µs is selected from the checkerboard pattern curve—3.4 hits. The alpha hits at 200ns are then selected from the same curve—160 hits. Taking 160 hits and dividing by 3.4 hits gives a ratio of 47. Thus, the SER can be expected to increase by a factor of 47 times when operating at 200ns as compared to refreshing at 15µs. By taking the real-time SER at 15µs and using the ratio from the acceleration curves just acquired, the SER at 200ns can be determined at 328 FITs times 47, which equals 15,416 FITs.

MTBF DUE TO SOFT ERRORS

Now, let's assume the 32-bit, single-bank DRAM memory array is active 15 percent of the time and is in refresh the remaining 85 percent of the time. The operating SER rate is now obtainable—15 percent of 15,416 FITs plus 85 percent of 328 FITs yields a FIT rate of 2,591 FITs. The system's memory MTBF for soft errors is obtained by dividing one billion device hours by 2,591 FITs for an MTBF of 385,950 system hours or 44 years.

For a dual-bank memory non-interleaved array, the operating SER rate would not be twice the single bank amount, as was the case with the refresh SER rate. This is because only one bank at a time is actively being written or read. The other bank(s) are in standby (refresh only). For example, let's determine the operating SER and MTBF for the 32-bit, dual bank memory array. The operating SER rate is 2,591 FITs (active bank from previous example) plus 328 FITs (additional bank in standby), which equals 2,919 FITs. The system's memory MTBF for soft errors is 342,580 system hours or 39 years.

SYSTEM-INDUCED SOFT ERRORS

So far, this discussion has focused on DRAM-related soft errors (i.e., alpha particle induced). System-induced soft-error calculations are beyond the scope of this article but warrant some discussion.

System-induced soft errors are those not generated by the DRAM memory itself. They are most commonly due to noise sources such as undershoot/overshoot, as well as timing issues due to hardware and/or software problems. System-induced soft errors are usually overlooked because they have been negligible contributors on a well-designed, clean system. Improvements made in DRAM SER by quality DRAM manufacturers, as well as faster operating speeds and board design requirements, have shifted the primary cause of soft errors to the system design itself.

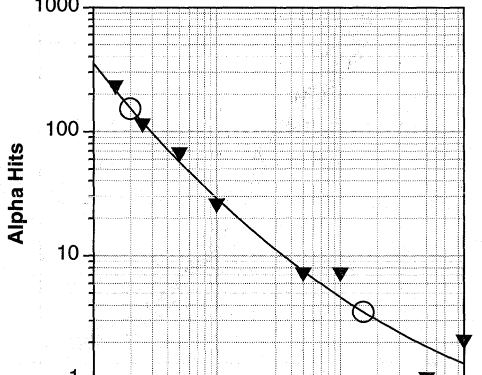

Figure 2
CHECKERBOARD PATTERN

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Conventional parity-based systems check for soft errors stemming from the data, both alpha particles (DRAM) and data I/O bus noise (system). However, there are other sources of system-induced soft errors that are overlooked because they cannot be detected with conventional parity. For example, noise on the address bus can result in the wrong data being written to, or read from, the DRAM. The data itself will be unaffected by the address bus noise, but the wrong location is accessed. Even though these types of system soft errors are not checked for, they are just as harmful as data-I/O induced soft errors.

Parity checking can be useful in the prototype stage by helping to identify initial design problems. Such parity checking can include DRAM, address bus and data bus parity checking. There are strong arguments for eliminating DRAM parity memory and providing parity checking on the address and data bus only. In either case, the DRAM parity memory and bus parity checking circuits could be eliminated once the system's design has been qualified to meet overall system soft-error requirements.

Even if a DRAM memory's alpha-particle-induced soft-error rate is at an acceptable level, some sort of parity checking may be desired. Bus-parity checking circuits could remain in the system at a lower cost and provide a greater safeguard against soft errors than that obtainable with DRAM parity memory.

Many of today's systems are designed to offer upgradability from the low-end to high-end of the performance spectrum. For these systems, where the low-end version does not require DRAM parity memory but the high-end upgrade does; designing-in flexibility to allow either choice is advantageous.

SUMMARY

In determining the parity requirements for a given memory system, the memory designer cannot assume parity is or is not required. Rather, the memory designer must analyze the system's reliability requirements and determine what soft error rate is expected and what MTBF for soft errors the system can tolerate.

The memory designer must "engineer" the SER numbers to his specific conditions to obtain numbers relevant to the design itself. Following the procedures outlined in this technical note will allow any memory system designer to determine expected memory MTBF-due-to-soft-error rates.

It should be noted that measured and accelerated SER data provides a "ball-park" number for general expectations. In the last example—a 32-bit, dual-bank memory array using 4 Meg DRAMs—the memory system was shown to experience one soft error every 39 years.

If a system required an MTBF of at least 38 years per soft error, the system using 4 Meg DRAMs would suffice technically. But since the expected MTBF is a typical expectation and not an absolute minimum, the number should be guard-banded. There is no industry rule for what guard band to use, but a memory designer should feel safe in using a 25 percent guard band. For the foregoing example, any system specifying an MTBF of 30 years or less should not jeopardize its reliability to DRAM-related soft errors by eliminating parity memory.

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TECHNICAL NOTE

MAXIMIZING EDO ADVANTAGES AT THE SYSTEM LEVEL

INTRODUCTION

Extended data-out (EDO) DRAMs, while representing only a slight modification to conventional FAST PAGE MODE (FPM) components, can provide substantial advantages at the system level. The primary benefit is that EDO allows for a shorter PAGE MODE cycle time (or faster data rate) while accessing data within a single page in memory. Other advantages include relaxed system timing constraints and in some cases, less total overhead during page accesses. In general, the design complexity for an EDO-based system will be less than that for a system based on FPM components, and much less than that for systems based on any of the other alternative DRAM technologies now being introduced.

This article reviews the physical differences between EDO and FPM components and then describes the timing implications of those differences. This discussion is then extended to cover the increase in performance and other advantages at the system level; examples using typical system timing are shown. Finally, additional system design implications are discussed.

EDO vs. FPM—COMPONENT LEVEL DIFFERENCES

Simply stated, EDO means that data is not disabled when $\overline{CAS}$ goes HIGH during a PAGE-MODE READ access. Instead, data remains available until such time that data from the subsequent access begins to appear. This is indicated by the presence of a ^tCOH specification and the lack of a ^tOFF specification when compared to conventional FPM (as shown in Figure 1). Other changes include related modifications to $\overline{RAS}$, $\overline{OE}$ and $\overline{WE}$ functionality, to provide for the disabling of data when necessary and when no longer accomplished by $\overline{CAS}$ alone. This related operation is further detailed in subsequent sections of this article.

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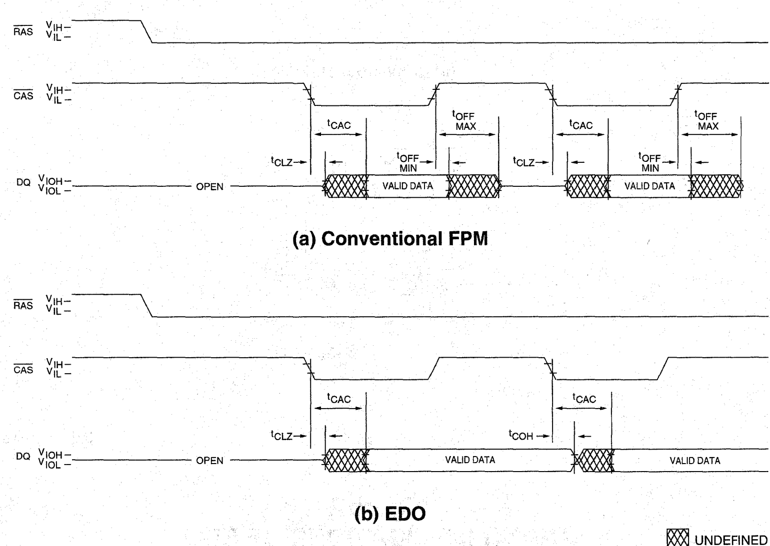

Figure 1
PHYSICAL DIFFERENCE BETWEEN FPM AND EDO

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TIMING IMPLICATIONS

The real advantage of EDO is not necessarily that data can remain valid once $\overline{CAS}$ goes HIGH, as shown in Figure 1, but that $\overline{CAS}$ is allowed to go HIGH prior to valid data appearing on the outputs (this is shown, again compared to conventional FPM, in Figure 2). For FPM devices, the $\overline{CAS}$ pulse width (^{t}CAS) is specified to be equal to ^{t}CAC since anything shorter would disable data before it became valid. In fact, ^{t}CAS typically must be longer than ^{t}CAC in the system because many DRAM vendors specify a minimum ^{t}OFF of 0ns. With EDO devices, ^{t}CAS is no longer limited by ^{t}CAC or the data valid time required by the system and is therefore typically specified at 10ns for the -6 speed grade.

The shorter ^{t}CAS specification associated with EDO allows the $\overline{CAS}$ or PAGE MODE cycle time to be tightened. As shown in Figure 2, EDO allows for a portion of the access time in one cycle to overlap a part of the access time, as well as all of the data valid time, for the previous cycle. In contrast, the only such overlap in a FPM access is the portion, if any, of the data valid time which is provided by a nonzero ^{t}OFF MIN specification. Specific system timing will determine the extent of the overlap that can be achieved, but the following theoretical example will illustrate the point.

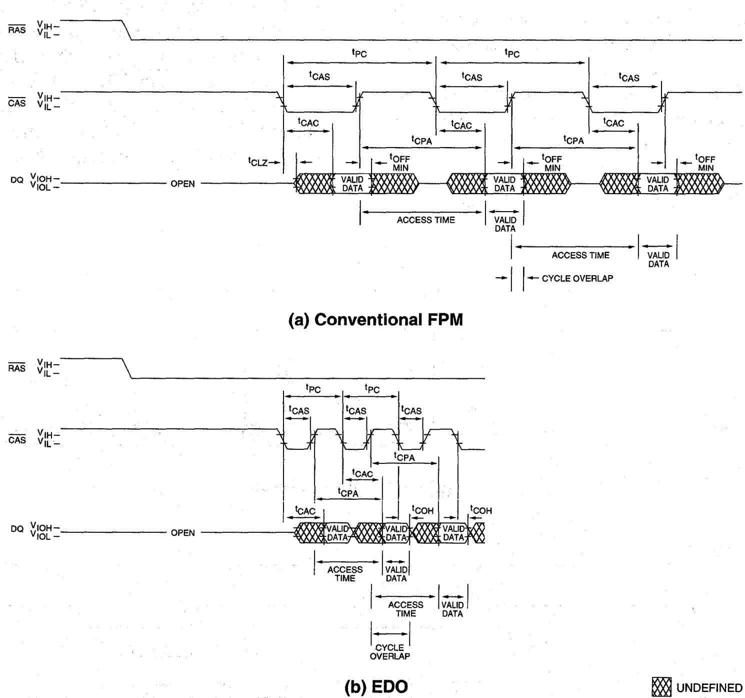

Figure 2
TIMING IMPLICATIONS OF EDO

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For now, let's ignore propagation delays from the system clock, system clock resolution, address timing and signal transition times. Let's assume that we have a -6 FPM version and a -6 EDO version of an otherwise identical device. For illustration, the timing for Micron's 256K x 16 DRAMs will be used (see Table 1.) This timing will be used in all of the examples that follow.

The PAGE MODE cycle timing for the two devices is shown in Figure 3. The difference between the FPM cycle time (35ns) and the EDO cycle time (25ns) can be accounted for by noting that the FPM cycle can be computed as 35ns of access time (^{t}CPA) plus 3ns of data valid time, minus the 3ns of data valid time that overlaps the next access. The EDO cycle can be computed as 35ns of access time plus 10ns of data valid time, minus 20ns of overlap with the next access. Note in this case that in addition to a shorter cycle, the EDO device also provides a longer data valid window, thereby simplifying system design.

Table 1
RELEVANT SPECIFICATIONS FOR THE MICRON 256K x 16 DRAMS

Parameter		MT4C16257 (FPM) (ns)	MT4C16270 (EDO) (ns)
^{t}CAC	MAX	15	15
^{t}CPA	MAX	35	35
^{t}AA	MAX	30	30
^{t}CP	MIN	10	10
^{t}OFF	MIN	3	3
^{t}CAS	MIN	15	10
^{t}CLZ	MIN	3	3
^{t}COH	MIN	-	5
^{t}PC	MIN	35	25
^{t}CSH	MIN	60	40
^{t}RSH	MIN	15	10
^{t}RAL	MIN	30	22
^{t}ASC	MIN	0	0
^{t}CAH	MIN	10	10
^{t}RP	MIN	40	35
^{t}DS	MIN	0	0
^{t}DH	MIN	10	10

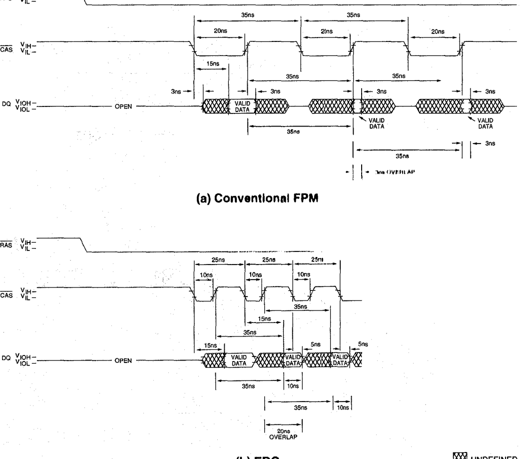

Figure 3
EDO vs. FPM MINIMUM CYCLE TIMES

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The overlapping of accesses described above leads to a pipelined effect in page mode read accesses, as shown in Figure 4. Ideally, data from one access is latched by the controller at the same time the controller fires $\overline{CAS}$ for the next access. A PAGE-MODE WRITE access does not benefit from EDO, but can be executed with the same minimum cycle times as shown in Figure 5.

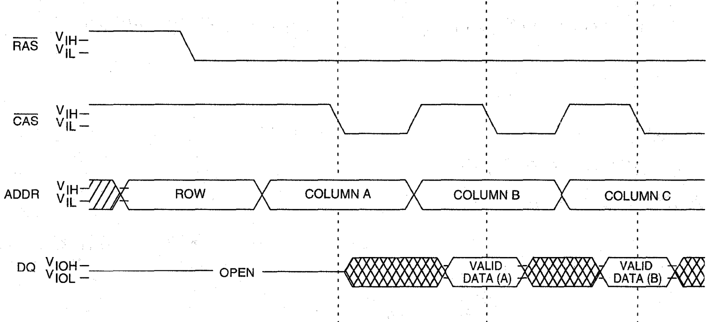

FIGURE 4
PIPELINED EFFECT IN EDO PAGE-MODE READs

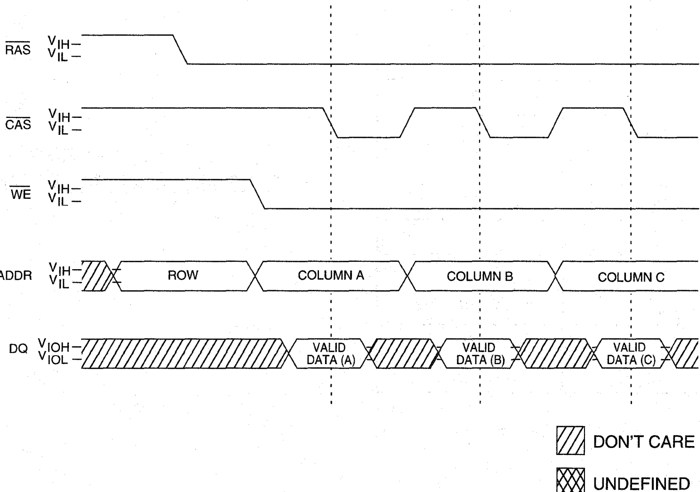

FIGURE 5
EDO PAGE-MODE WRITEs

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SYSTEM PERFORMANCE INCREASE FROM EDO

To examine the system performance advantage provided by EDO and factor system clock resolution into the discussion, a noninterleaved design based on a 66 MHz system clock driven by the positive clock edges only, will be considered. Figures 6 and 7 show, respectively, the FPM and EDO PAGE-MODE READ cycle timing resulting from the 15ns clock resolution (bursts of three locations were used strictly for the convenience of graphic illustration). Note that while a 30ns cycle time can be achieved with EDO, only a 45ns cycle can be achieved with FPM. Converting the cycle times to peak burst rates results in 33 MHz for EDO and 22 MHz for FPM. In this case, EDO provides a 50

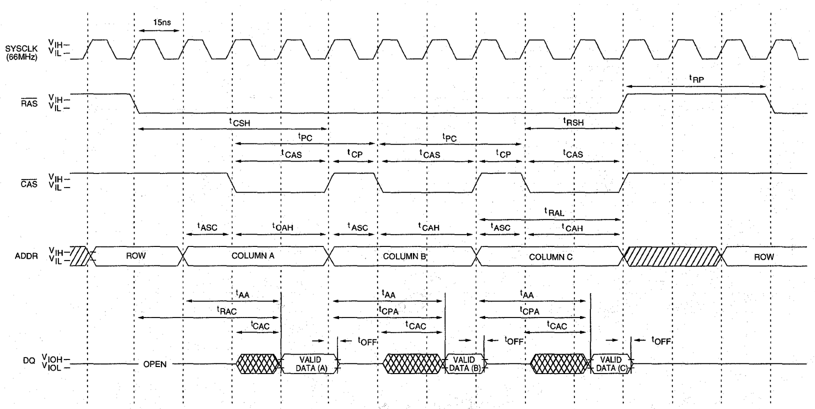

Figure 6
FPM READ CYCLE - 66 MHz SYSTEM CLOCK

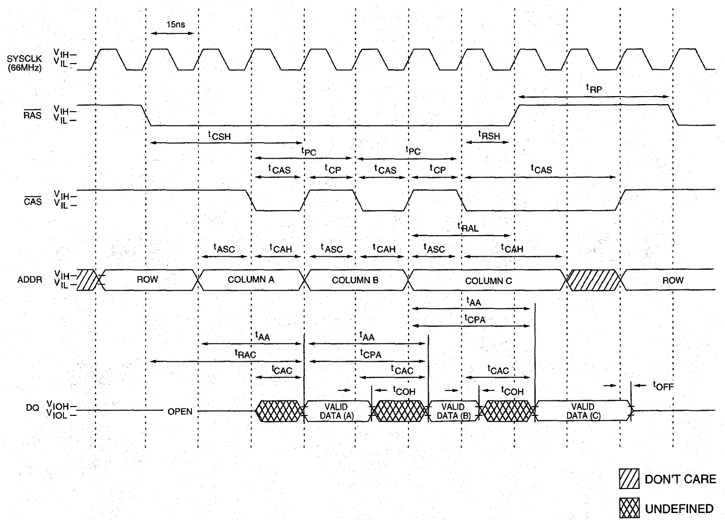

Figure 7
EDO READ CYCLE - 66 MHz SYSTEM CLOCK

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percent improvement in peak burst rate in the system. For reference, Figures 8 and 9 show the corresponding PAGE-MODE WRITE cycle timing. Figure 9 shows that although the write cycles do not benefit from the EDO behavior itself, they can still match the cycle times for the EDO READs.

Also shown in Figure 7 is the fact that unlike operation within a page access, once the page access is terminated by $\overline{RAS}$ going HIGH, $\overline{CAS}$ going HIGH will disable data. This results in the ability to hide some row precharge time, as discussed below.

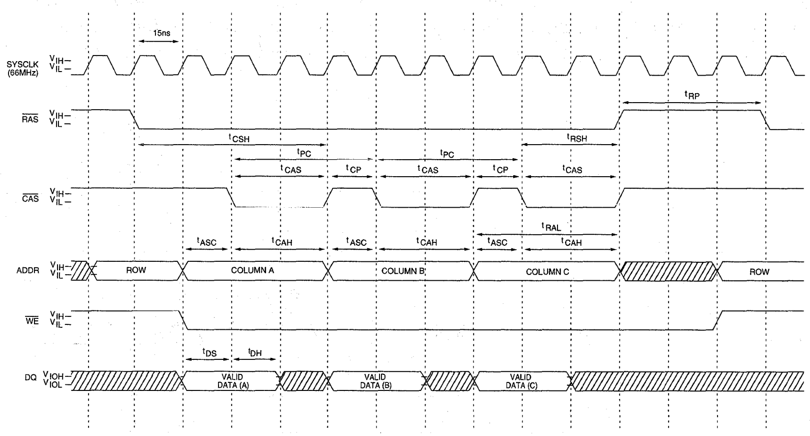

Figure 8
FPM WRITE CYCLE - 66 MHz SYSTEM CLOCK

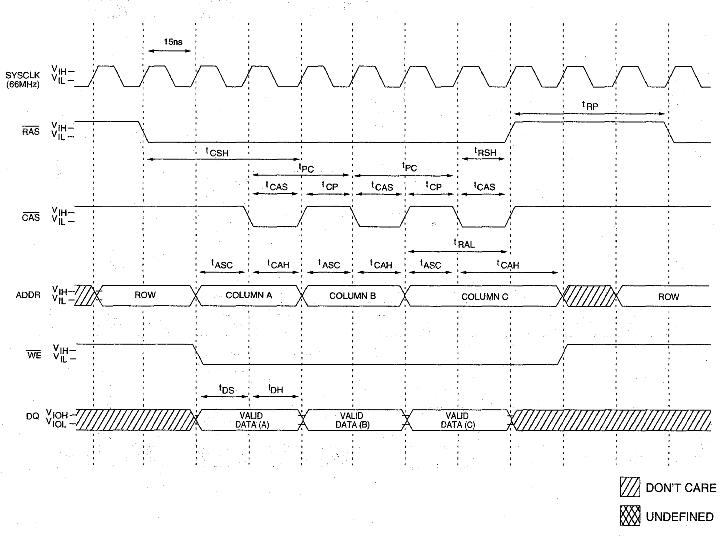

Figure 9
EDO WRITE CYCLE - 66 MHz SYSTEM CLOCK

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Table 2
POPULAR SYSTEM CLOCK RATES AND RESULTING PAGE MODE CYCLE TIMES

SYSTEM CLOCK		PAGE MODE CYCLE TIME	
Frequency (MHz)	Period (ns)	FPM (ns)	EDO (ns)
50	20.0	40	40
60	16.7	50	33
66	15.0	45	30
80	12.5	50	25

Table 2 lists popular system clock rates along with the corresponding FPM and EDO PAGE MODE cycle times that would result from system clock resolution alone. Not only does EDO provide a faster peak data rate in almost every case, but an increase in system clock rate is much more likely to result in a corresponding faster peak burst rate (shorter PAGE MODE cycle time) when EDO devices are used. This continuous increase will extend to 90 and 100 MHz systems with the introduction in the near future of EDO parts, which provide PAGE MODE cycle times down to 20ns.

Also related to system performance is the fact that the use of EDO typically results in the same total page mode overhead (row access time plus row precharge time) as with FPM. This is possible because ^{t}CSH, like ^{t}CAS, is not physically limiting on the devices as specified for FPM and would therefore be an artificial limiter if carried over directly from FPM and applied to EDO devices. Instead, Micron is adjusting the ^{t}CSH specification on EDO devices to allow for the first $\overline{CAS}$ pulse to go HIGH earlier in the page access, and it is expected that other vendors will make this adjustment as well. This specification will typically be 40ns for -6 and -7 speed grades. Another parameter which would be a limiter if carried over is ^{t}RSH. This parameter will also be respecified for EDO; ideally it would be set equal to the EDO ^{t}CAS specification. There are also several other parameters, many device or vendor specific, that will be adjusted to accommodate EDO designs.

Figures 7 and 9 reflect the adjusted ^{t}CSH and ^{t}RSH specifications and the result is that the page mode overhead for the EDO devices is equal to that for the FPM devices. This is seen by noting that the total number of clock cycles for the page access for the FPM devices is 13. Three locations of data require three clocks each, for a total of nine, leaving four as overhead. For the EDO, ten total cycles are needed, six of which are required for data, again leaving four as overhead.

SYSTEM ADVANTAGES OF EDO

After reviewing the theoretical FPM and EDO PAGE MODE cycle times listed in Table 2, the next logical question is, can those cycle times actually be achieved in a real system, and with how much effort? The answer is that achieving these cycle times with EDO devices will require equal or less design complexity than that required with FPM devices. The biggest problem in designing with FPM devices, once the propagation delays from the system clock are taken into consideration, has been trying to align the read data valid window around a system clock edge that can be used to latch that data into the memory controller.

A 50 MHz system clock and the device timing mentioned earlier will be used to illustrate this point. Typical propagation delays that might be found in a graphics subsystem with a controller implemented in an ASIC will also be used. These include a clock-to-Q delay for the controller plus routing delays, together totaling 12ns, and routing delays plus setup time back to the controller, together equaling 7ns.

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In Figure 10, the FPM case, the data valid window for the controller starts 3ns before, and ends 5ns after, a negative system clock edge, which also means that the window ends 5ns prior to the next positive system clock edge. The choices here are to work with a skewed and/or inverted internal clock or with internal data delays to extend hold time to beyond the positive edge, or use an alternate external signal as a clock to the data input latch on the controller. Either way, these multiple/skewed clocks add design complexity.

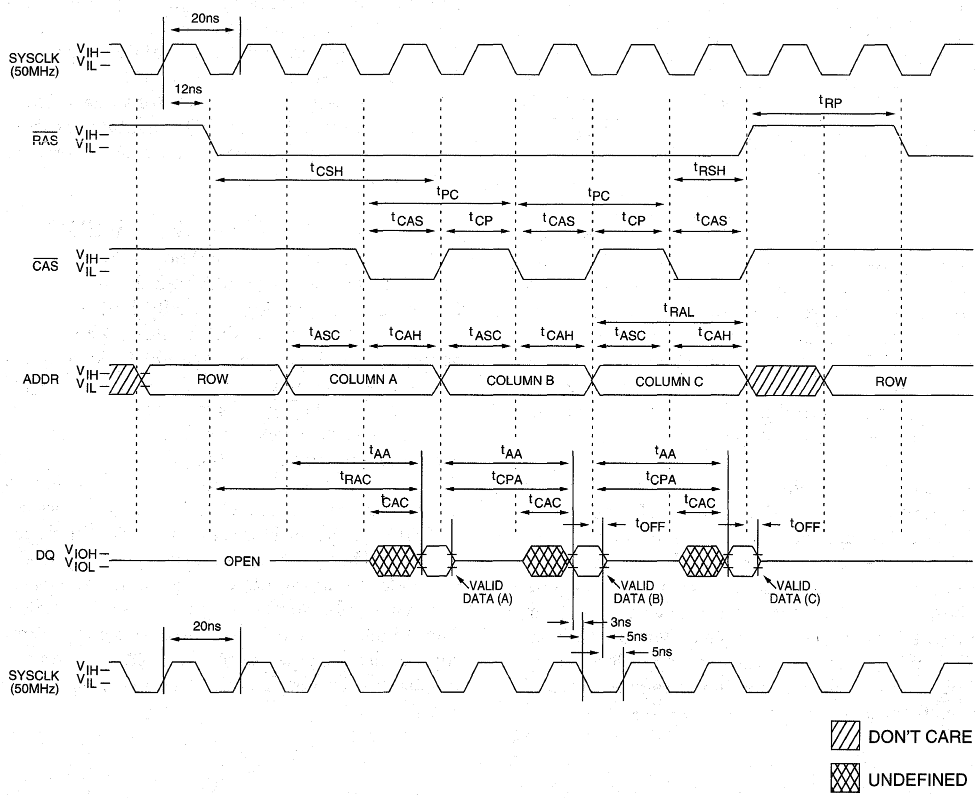

Figure 10
FPM READ CYCLE WITH PROPAGATION DELAYS - 50 MHz SYSTEM CLOCK

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In contrast, when EDO devices are used with the same system timing, the data valid window begins at the same point but extends until ᵗCOH (5ns) after the next $\overline{CAS}$ falling edge, shown in Figure 11. This total window is equal to 30ns or 1.5 system clock cycles; therefore, data can easily be latched in by an existing positive edge of the system clock with no additional design complexity.

Note that the page mode overhead for this example also happens to be less for EDO than for FPM. Since both methods use the same number of system clock cycles for each column (data) access, this overhead savings is seen by noting that the total number of clocks required for the page access is ten in the FPM case and nine in the EDO case.

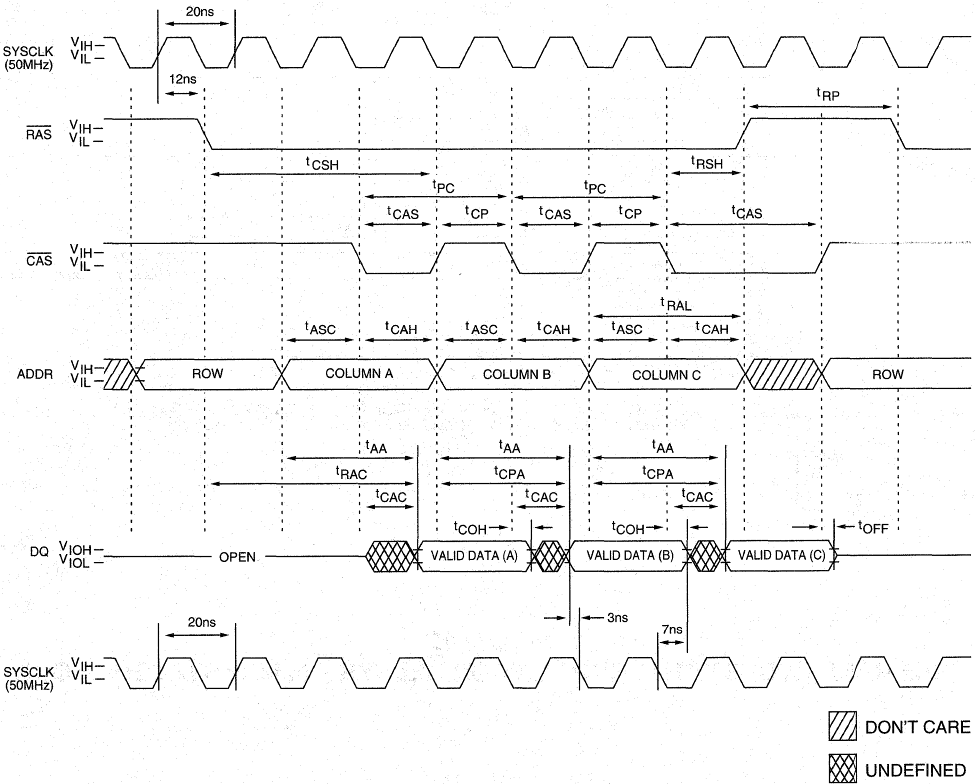

Figure 11
EDO READ CYCLE WITH PROPAGATION DELAYS - 50 MHz SYSTEM CLOCK

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Now that we've shown that EDO can be substantially faster than FPM, and that at a given speed, an EDO-based system can be implemented with equal or less design complexity, the next question is, can an EDO-based system be designed to be faster with equal or less design complexity? The answer, again, is "yes." To see this, let's revisit the 66 MHz example (where EDO was previously shown to provide a 50 percent improvement in peak memory bandwidth), but now typical system propagation delays will be included. A system clock-to-Q plus trace delay of 9ns and a delay and setup time back to the controller of 5ns will be used. The resulting timing is shown in Figures 12 and 13.

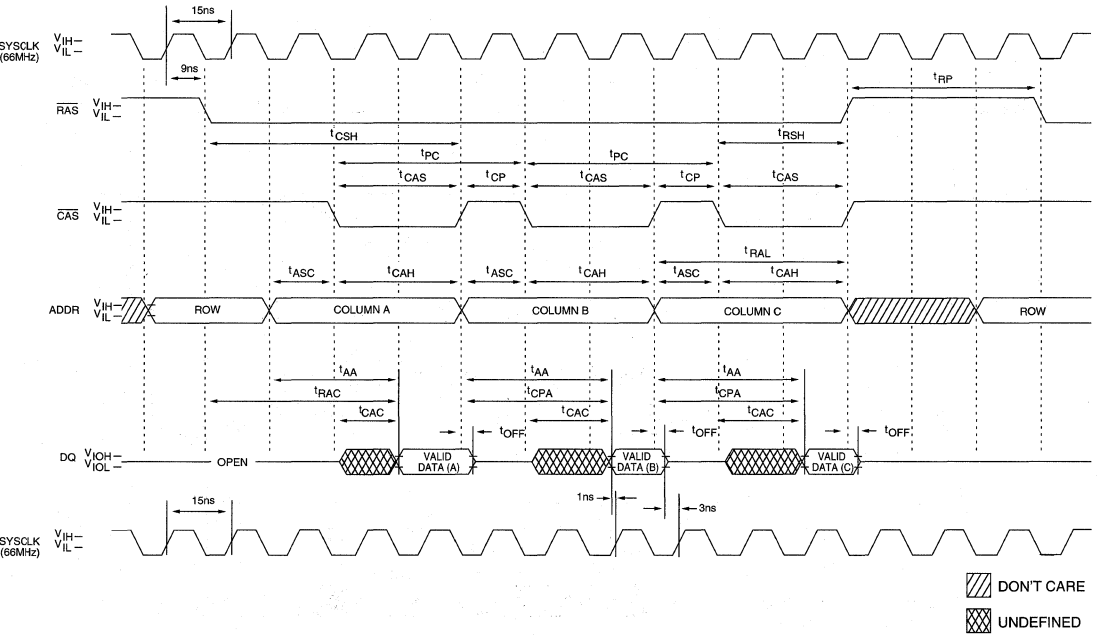

Figure 12
FPM READ CYCLE WITH PROPAGATION DELAYS - 66 MHz SYSTEM CLOCK

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Once again for the FPM case, the data valid window (13ns) does not line up with an existing positive edge of the system clock (while meeting the required set-up time) so one of the design techniques mentioned above will need to be employed. The data valid window for the EDO case also does not align with an existing positive clock edge, and will also require one of the above design techniques. However, in the EDO case, the data valid window is longer than for the FPM case (15ns vs 13ns) and is therefore simpler to design for. Here we have a case where EDO provides a 50 percent improvement in peak memory bandwidth, but with reduced design complexity.

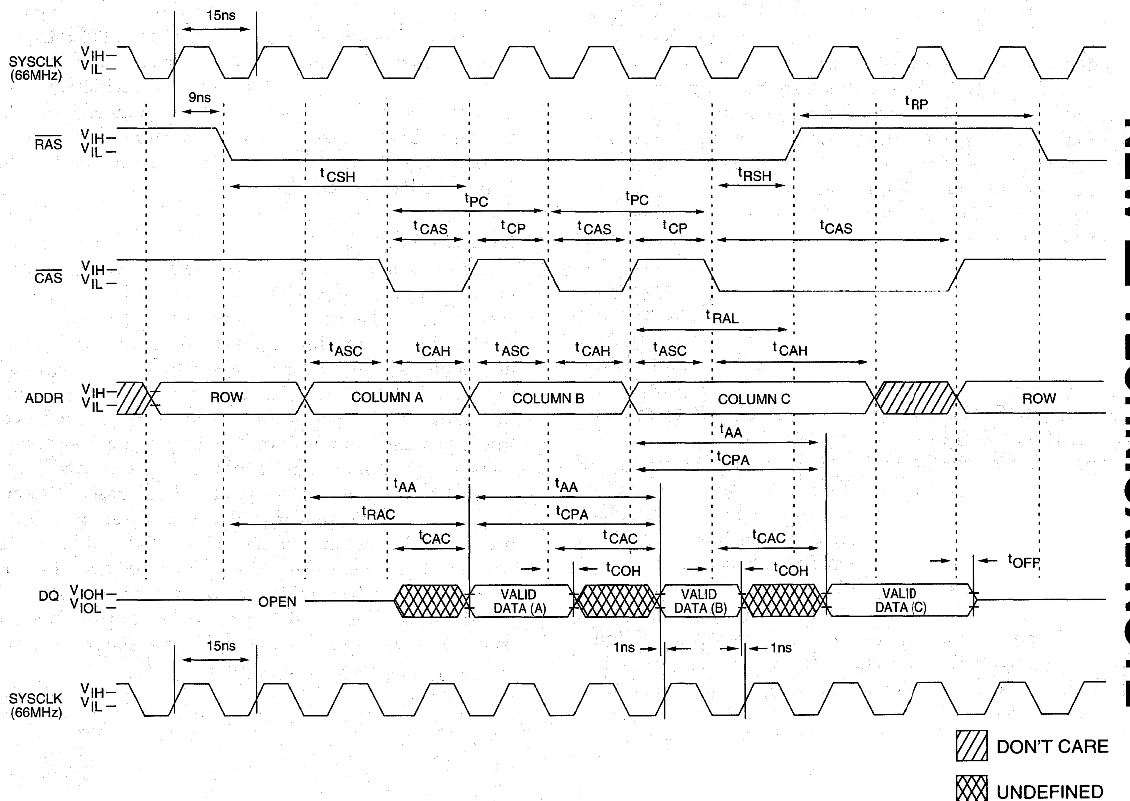

Figure 13
EDO READ CYCLE WITH PROPAGATION DELAYS - 66 MHz SYSTEM CLOCK

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DESIGN IMPLICATIONS

Address Setup Time: In order to achieve maximum performance with EDO, it is necessary to provide valid column-addresses with sufficient setup time to the falling edge of $\overline{\text{CAS}}$ so that ^{t}AA is not a limiting parameter. This leaves ^{t}CPA as the limiting parameter for PAGE-MODE READ cycle times. This is true for FPM as well, but there, either ^{t}CAC or ^{t}CPA may be limiting.

With the device timing shown, the column-addresses should transition after meeting the hold time (^{t}CAH) from the previous access. This means that the same system clock edge that drives $\overline{\text{CAS}}$ HIGH will drive the new address. Since ^{t}CPA is typically specified to be 5ns longer than ^{t}AA, if the $\overline{\text{CAS}}$ and column address lines transition at the same time, ^{t}CPA will always be limiting. However, the address lines may be more heavily loaded and may transition later. This is not an issue unless the address signals take over 5ns longer than the $\overline{\text{CAS}}$ signal to become valid, and will actually provide additional guardband in meeting ^{t}CAH.

$\overline{\text{OE}}$ and $\overline{\text{WE}}$ Operation: In certain situations it is necessary to disable the data outputs while within a page mode access (for example, when switching from a READ cycle to a WRITE cycle or when interleaving banks of memory). For EDO, since $\overline{\text{CAS}}$ alone will not disable the outputs, either $\overline{\text{OE}}$ or $\overline{\text{WE}}$ must be used.

As with FPM devices, the data outputs will be disabled whenever $\overline{\text{OE}}$ goes HIGH. However, if this occurs (for a specified duration) while $\overline{\text{CAS}}$ is HIGH, the EDO operation will be suspended. Specifically, the data outputs will be disabled and will remain that way, regardless of subsequent transitions on $\overline{\text{OE}}$, until $\overline{\text{CAS}}$ goes LOW again for a READ cycle. This pulsed operation is beneficial in system implementations which include multiple banks of memory, and which may have rows activated in more than one bank simultaneously. Instead of supplying a separate $\overline{\text{OE}}$ signal for each bank, bank-specific $\overline{\text{CAS}}$ signals can be used in conjunction with a common $\overline{\text{OE}}$ signal to disable the data outputs for a given bank. Alternitively, $\overline{\text{WE}}$ going LOW at any time will suspend EDO operation; the outputs will be disabled and will remain disabled until $\overline{\text{CAS}}$ goes LOW for a READ cycle

Maximum page mode performance is achieved when executing strictly READ cycles ($\overline{\text{WE}}$ remains HIGH) or strictly WRITE cycles ($\overline{\text{WE}}$ remains LOW), as shown in the previous examples. Mixing READ and WRITE within a page is supported, but this usually requires additional clock cycles. For switching from a READ to a WRITE cycle, either $\overline{\text{OE}}$ or $\overline{\text{WE}}$ may be used to disable output data; depending on the individual device specification, one method may be faster than the other. In either case, $\overline{\text{WE}}$ must go LOW to execute the WRITE. More detailed information on $\overline{\text{OE}}$ and $\overline{\text{WE}}$ operation can be found in the individual device data sheets.

SUMMARY

EDO is a minor modification over conventional FPM memory components, with major implications in terms of system performance and/or simplifying system design complexity. A very simple physical change at the component level (data not being disabled by $\overline{\text{CAS}}$ going HIGH within a PAGE-MODE READ access) results in either a longer data valid window or a shorter PAGE MODE cycle time and often results in both. As with any component type, there are specific design factors to be considered but in general, the design complexity of an EDO-based system is equal to or less than that of an FPM-based system, resulting in a substantial performance increase with no added design cost. The performance increase is measured as an increase in peak memory bandwidth and on components which are widely available today, this increase can be up to 60 percent based on device specifications, and up to 100 percent once actual system clock timing is considered.

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TECHNICAL NOTE

VARIOUS METHODS OF DRAM REFRESH

INTRODUCTION

DRAM refresh is the topic most misunderstood by designers due to the many ways refresh can be accomplished. This article addresses the most often asked questions about refresh. The two basic means of performing refresh, distributed and burst, are explained first followed by the various ways to accomplish refresh: $\overline{\text{RAS}}$-ONLY REFRESH, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH and HIDDEN REFRESH.

STANDARD AND EXTENDED REFRESH

DRAMs are often referred to as either "standard refresh" or "extended refresh." Dividing the specified refresh time by the number of cycles required will determine if the DRAM is a standard refresh or an extended refresh device. If the result is 15.6µs it is a standard refresh device, while a result of 125µs indicates an extended refresh device.

Table 1 lists some of the standard DRAMs and their refresh specifications.

Table 1
STANDARD DRAMS AND REFRESH SPECIFICATIONS

DRAM	REFRESH TIME	NUMBER OF CYCLES	REFRESH RATE
4 Meg x 1	16 ms	1,024	15.6µs
256K x 16	8 ms	512	15.6µs
256K x 16 (L version)	64 ms	512	125µs
4 Meg x 4 (2K)	32 ms	2,046	15.6µs
4 Meg x 4 (4K)	64 ms	4,096	15.6µs

DISTRIBUTED REFRESH

Distributing the refresh cycles so that they are evenly spaced is known as distributed refresh. To perform distributed refresh on a standard DRAM, execute a refresh cycle every 15.6µs such that all rows are turned on before repeating the task. When not being refreshed, the DRAM can be read from or written to.

BURST REFRESH

Refresh may be achieved in a burst method by performing a series of refresh cycles, one right after the other until all rows have been accessed. During refresh other commands are not allowed. Below is a drawing representing burst and distributed refresh.

For example: a 4 Meg x 1 requires 1,024 consecutive refresh cycles, each of which will use 130ns (^{t}RC) for a 70ns device.

1,024 cycles x 130ns = 133,120ns = 0.133ms
16ms - 0.133ms = 15.867ms

Approximately 0.13ms would be spent performing refresh, and the remaining 15.87ms could be spent reading and writing; then burst refresh would occur again, and so on.

Distributed refresh is the more common of the two refresh categories. The DRAM controller is set up to perform a refresh cycle every 15.6µs. Usually, this means the controller allows the current cycle to be completed, and then holds off all instructions while a refresh is performed on the DRAM. The requested cycle is then allowed to resume.

REFRESH CYCLES

There are different cycles you can use to refresh DRAMs, all of which can be used in a distributed or burst method. There are three types listed in a standard data sheet:

- $\overline{\text{RAS}}$-ONLY REFRESH
- $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH
- HIDDEN REFRESH

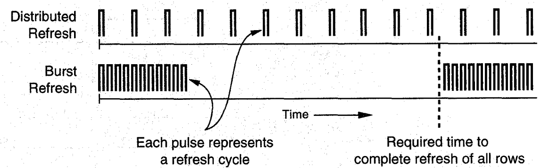

Figure 1
BURST AND DISTRIBUTED REFRESH

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RAS-ONLY REFRESH

To perform a RAS-ONLY REFRESH, a row address is put on the address lines and then RAS is dropped. When RAS falls, that row will be refreshed and, as long as CAS is held high, the DQs will remain open. (See Figure 2.)

It is the DRAM controller's function to provide the addresses to be refreshed and make sure that all rows are being refreshed in the appropriate amount of time. The row order of refreshing does not matter; what is important is that each row be refreshed in the specified amount of time.

CAS-BEFORE-RAS REFRESH

CAS-BEFORE-RAS REFRESH, also known as CBR REFRESH, is a frequently used method of refresh because it is easy to use and offers the advantage of a power savings. A CBR REFRESH cycle is performed by dropping CAS and then dropping RAS. One refresh cycle will be performed each time RAS falls. WE must be held high while RAS falls. The DQs will remain open during the cycle.

Here's how CBR REFRESH works. The die contains an internal counter which is initialized to a random count when the device is powered up. Each time a CBR REFRESH is performed, the device refreshes a row based on the counter, and then the counter is incremented. When CBR REFRESH is performed again, the next row is refreshed and the counter is incremented. The counter will automatically wrap and continue when it reaches the end of its count. There is no way to reset the counter. The user does not have to supply or keep track of row addresses. A drawing of one CBR REFRESH cycle is shown in Figure 3. CAS must be held low before and after RAS falls to meet ᵗCSR and ᵗCHR. Figure 4 shows three CBR REFRESH cycles. In this drawing, CAS stays low and only RAS toggles. Every time RAS falls a refresh cycle is performed. CAS may be toggled each time, but it's not necessary.

CBR POWER SAVINGS

Since CBR REFRESH uses the internal counter and not an external address, the address buffers are powered-down. For power sensitive applications, this can be a benefit, because there is no additional current used in switching address lines on a bus, nor will the DRAMs pull extra power if the address voltage is at an intermediate state.

CBR REFRESH IS EASY TO USE

Since CBR REFRESH uses its own internal counter, there is not a concern about the controller having to supply the refresh addresses. Virtually all DRAMs support CBR REFRESH and the 15.6µs refresh rate, so you can design for CBR REFRESH at the distributed rate of 15.6µs and plug in many different DRAMs without having to worry about refresh. For example, the 4 Meg x 4 comes in two versions:

- 2,048 cycles in 32ms
- 4,096 cycles in 64ms

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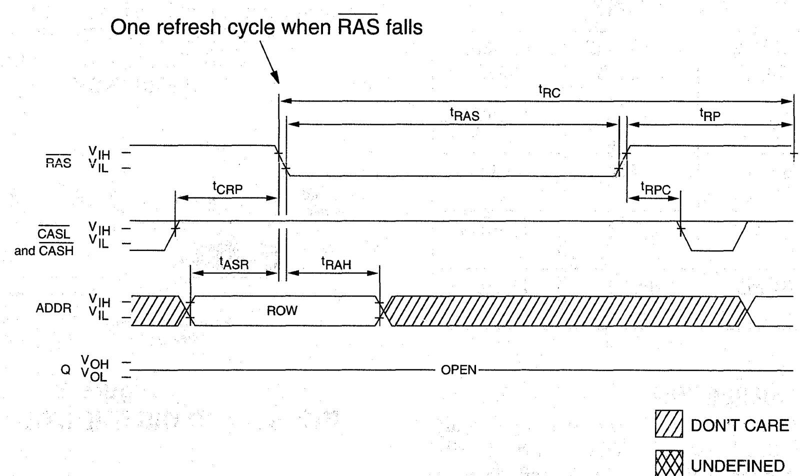

Figure 2
RAS-ONLY REFRESH

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If CBR REFRESH is used, simply maintain the standard 15.6µs refresh rate. If RAS-ONLY REFRESH is used, addresses must be supplied as follows:

- A0-A10 for the 2,048 cycle refresh
- A0-A11 for the 4,096 cycle refresh.

HIDDEN REFRESH

In HIDDEN REFRESH, the user does a READ or WRITE cycle and then, leaving CAS low, brings RAS high (for minimum of tRP) and then low. Since CAS was low before RAS went low, the part will execute a CBR REFRESH. In a READ cycle the output data will remain valid during the CBR REFRESH. The refresh is not "hidden" in the sense that you can hide the time it takes to refresh, instead it is hidden in the sense that data-out will stay on the lines while performing the function. READ and HIDDEN REFRESH cycles will take the same amount of time: tRC. The two cycles together take 2 x tRC. If we were to do a READ and

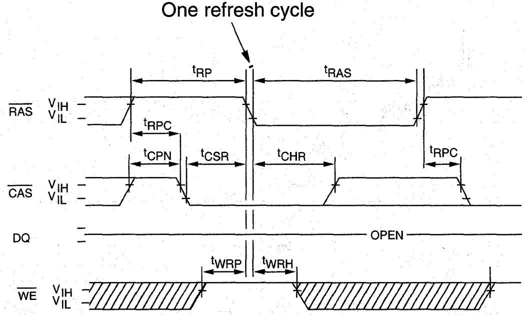

Figure 3
ONE CAS-BEFORE-RAS REFRESH CYCLE

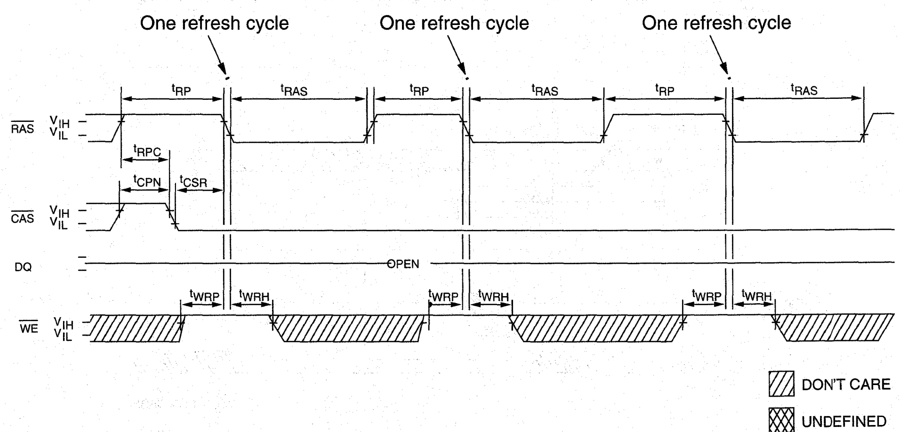

Figure 4
THREE CAS-BEFORE-RAS REFRESH CYCLES

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then follow it with a standard CBR REFRESH (instead of a HIDDEN REFRESH), this would take the same amount of time: 2 x ^tRC.

Figure 5 shows a READ followed by a HIDDEN REFRESH. Figure 6 shows a READ followed by a standard CBR REFRESH. The only difference between the two is that data-out is valid during the HIDDEN REFRESH.

SUMMARY

Three different cycles exist to perform refresh on a standard DRAM: $\overline{RAS}$-ONLY REFRESH, $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH, and HIDDEN REFRESH. Each cycle can be used in a burst or distributed method, whichever best fits the designer's needs. However, CBR REFRESH is the preferred choice because of its ease of use and power savings.

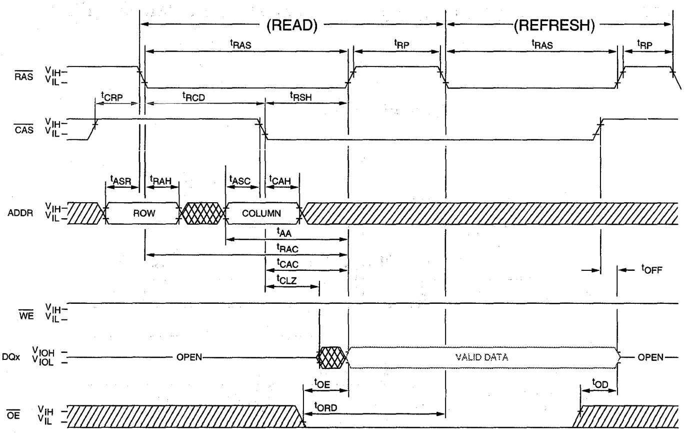

FIGURE 5
READ CYCLE FOLLOWED BY HIDDEN REFRESH

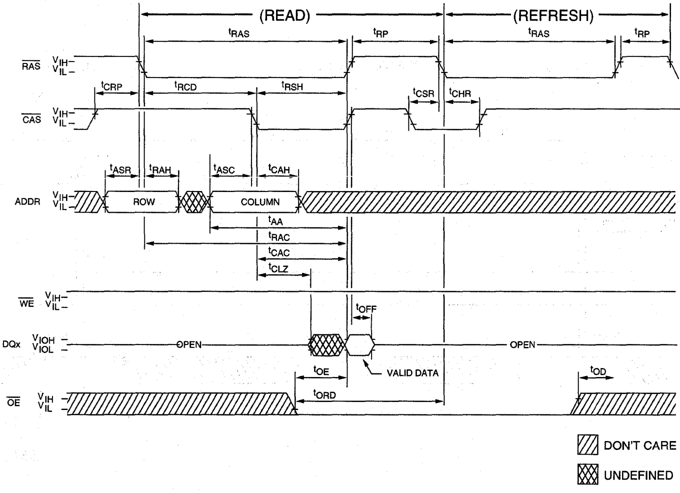

FIGURE 6
READ CYCLE FOLLOWED BY CBR REFRESH

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TECHNICAL NOTE

PCB LAYOUT FOR 4 MEG x 4 300 MIL OR 400 MIL SOJ

INTRODUCTION

The 4 Meg, the 16 Meg and the 64 Meg DRAMs are experiencing similar packaging trends, in which the first generation is produced in a larger package than later generations for a given density. A list of DRAM configurations for the various 4, 16 and 64 Meg DRAMs is provided in Table 1. For each device type, the initial offering (first generation) is listed along with the size reduction on later generations.

Table 1
PACKAGE TRENDS BY CONFIGURATION

Device	Initial Package		As Product Matures		
	Size	Pins	Size	Pins	Package
4 Meg x 1	350 mil	20/26	300 mil	20/26	SOJ
1 Meg x 4	350 mil	20/26	300 mil	20/26	SOJ
4 Meg x 4	400 mil	24/28	300 mil	24/26	SOJ/ TSOP
2 Meg x 8	400 mil	28	300 mil	28	TSOP
16 Meg x 4	500 mil	34	400 mil	32	SOJ
8 Meg x 8	500 mil	34	400 mil	32	SOJ

Although migrating from a larger to a smaller package has obvious long term benefits, it can make the memory designer's job more difficult when designing a printed circuit board (PCB) layout that can accommodate both sizes. This technical note demonstrates a PCB layout that can accommodate 300 mil or 400 mil 4 Meg x 4 SOJ DRAMs in a 2K refresh version, as well as help point out the need to layout for future trends. This note applies only to the 2K refresh version because it has symmetric addressing, so A10 and A3 can be used interchangeably. Because the 4K refresh has 2 address bits dedicated as row-only addresses, additional jumpers would be required.

Figure 1 shows the basic pad layout for either 4 Meg x 4 DRAM.

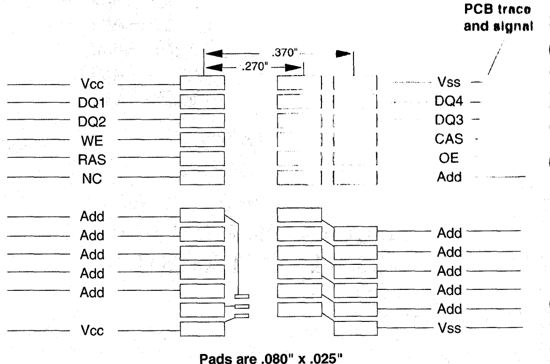

Figure 1
PCB LAYOUT FOR A 4 MEG x 4 SOJ

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In Figure 2, the shaded pads show the 24/28 pin 400 mil package in the layout. The shading represents a solder connection from the PCB pad to the package lead. The text within the shaded pad is the DRAM pin assignment, and the text outside the pads is the signal coming from the PCB. The small numbers reflect the DRAM pin numbers. The three small boxes provide the jumper connection to enable the 300 mil or 400 mil layout. A dotted line indicates where the jumper is used to make the correct electrical connection for the 400 mil package.

In Figure 3, the 24/26 300 mil package fit is shown. Notice that the inside pads are now shaded instead of the outside pads. The jumper has been placed in the alternate position to make the proper connection for the 300 mil package.

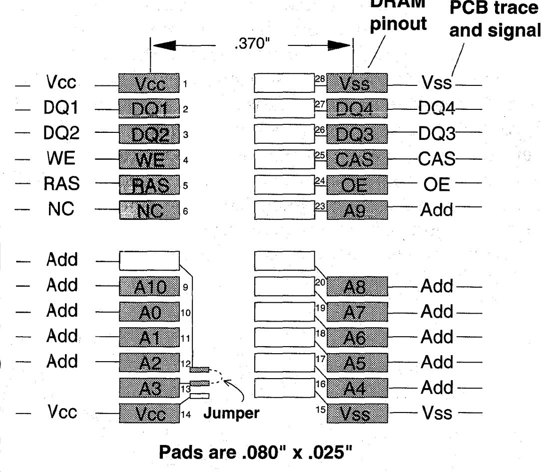

Figure 2
4 MEG x 4, 2K REFRESH
400 MIL SOJ LAYOUT

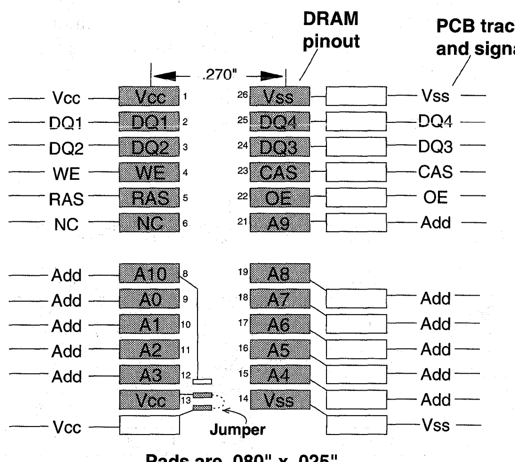

Figure 3
4 MEG x 4, 2K REFRESH
300 MIL SOJ LAYOUT

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TECHNICAL NOTE

REDUCE DRAM MEMORY COSTS WITH CACHE

INTRODUCTION

All PCs sold today (x486 and above) have cache memory, usually both internal to the processor (L1) and external to the processor (L2). The intended purpose of the cache memory is to minimize the number of wait-states the DRAM-based main memory imposes on the microprocessor. In other words, cache memory improves the speed of microprocessor accesses because it is significantly faster than DRAM-based main memory.

Today, the performance of the DRAM-based main memory is not nearly as important to the microprocessor accesses as it was before the use of cache memories; a side benefit of incorporating cache that is generally overlooked. Cache is used during most of the microprocessor accesses (80 to 96+ percent of the accesses). When cache memory is accessed, DRAM-based main memory is not accessed. This means DRAM-based main memory is accessed by the microprocessor a small percentage of the time. This is a dramatic shift from the previous generations of systems that did not incorporate cache memory.

Two performance factors of the DRAM which dramatically improve when the usage rate of the DRAM is reduced are speed and soft error rates (SER).

DRAM SPEED

Prior to the employment of cache memory, the DRAM speed had a significant effect on the microprocessor's performance and was generally considered to be the bottleneck in system performance. Figure 1 depicts the historical performance increases obtained as the DRAM speed has improved from 120ns to 80ns. The analysis assumes a 386 microprocessor (no L1 cache), no external cache and 10ns buffer/trace delay.

DRAM speed grade improvements generally provided significant microprocessor performance enhancements. This generated the demand for faster DRAMs and warranted the extra premium being charged for them.

With the introduction of primary (L1) and secondary (L2) cache memory, the number of microprocessor accesses to the DRAM main memory have been significantly reduced, as seen in Figure 2. A microprocessor with internal (L1) cache will generally require 15 to 20 percent of the memory accesses to go out of the microprocessor and access either an L2 cache memory or the DRAM main memory. With the addition of an L2 cache memory, just one to four percent of the memory accesses are required to go to the slower DRAM main memory.

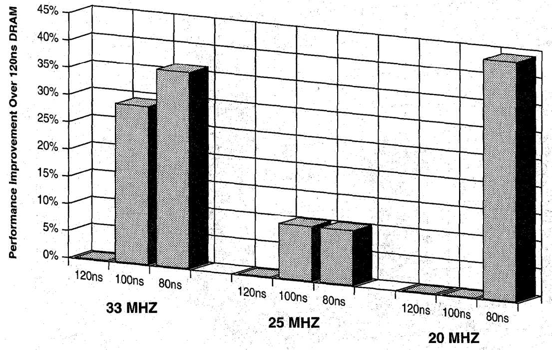

Figure 1
HISTORICAL DRAM MEMORY PERFORMANCE IN PCS

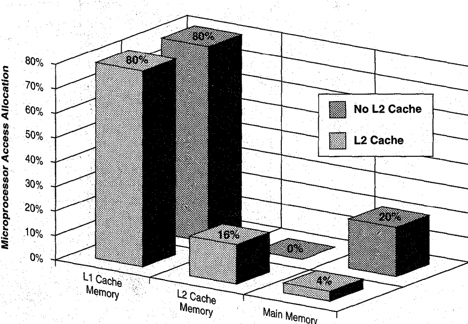

Figure 2
MICROPROCESSOR ACCESS ALLOCATION

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With only one to four percent of the memory accesses now going to DRAM main memory, microprocessor performance improvements obtained by using today's faster DRAMs are greatly minimized, as is seen in Figure 3. For example, utilizing 50ns DRAMs in a 486-based PC with an L2 cache and both L1 and L2 caches obtaining an 80 percent hit rate, the microprocessor's performance would be improved by less than one percent over the employment of 70ns DRAMs.

Excluding cache memory effects, a more in-depth look into the DRAM's speed performance reveals that the perceived advantages of faster DRAMs in PCs are, in part, diminished due to the nature of data being clocked. So, the faster DRAM speed does not affect the microprocessor's performance unless it can eliminate a wait-state, as demonstrated in Figure 4.

It should be noted that a faster ^{t}RAC (sufficiently fast enough to eliminate a wait state) only improves the microprocessor's burst performance by one clock at best. Whereas, a sufficiently faster ^{t}CAC improves the microprocessor's burst performance by three clocks. And thus, the impetus behind the growing demand for EDO DRAMs (see technical note TN-04-29, "Maximizing EDO Advantages at the System Level").

A prudent system designer can generally deliver the best price/performance ratio by using 70ns DRAMs rather than pay speed premiums for 50 and 60ns DRAMs. With today's computing architectures, one should not assume a faster DRAM equates to noticeable microprocessor performance improvement.

MULTIPLE-CLOCKED MICROPROCESSORS

It is worth noting that the previous analysis is based on non-multiple-clocked microprocessors. That is, microprocessors in which the data bus is clocking at the same rate as the microprocessor. The performance effects of the DRAM are more pronounced on multiple-clocked microprocessors.

Although the percentage of DRAM main memory accesses remain the same, the amount of time a DRAM access slows the microprocessor is no longer a one-to-one ratio due to the multiple microprocessor clocks. This ratio is different because each wait-state the external memory imposes on the microprocessor equates to several clocks for the microprocessor (e.g., three clocks for a triple-clocked microprocessor).

A typical PC system with an L1 cache (assume L1 and L2 each have 80 percent hit rate) will retain 80 percent of the memory accesses internal to the microprocessor (L1) and direct the remaining to external memory. Of this, 80 percent of the external memory accesses (16 percent of the total memory accesses) go to the secondary cache. The remaining memory accesses (4 percent of the total memory accesses) go to DRAM memory. For a multiple-clocked microprocessor based system, the L2 cache and DRAM memory accesses will require a higher percentage of execution time since each external clock translates to a multiple of the microprocessor's internal clocks.

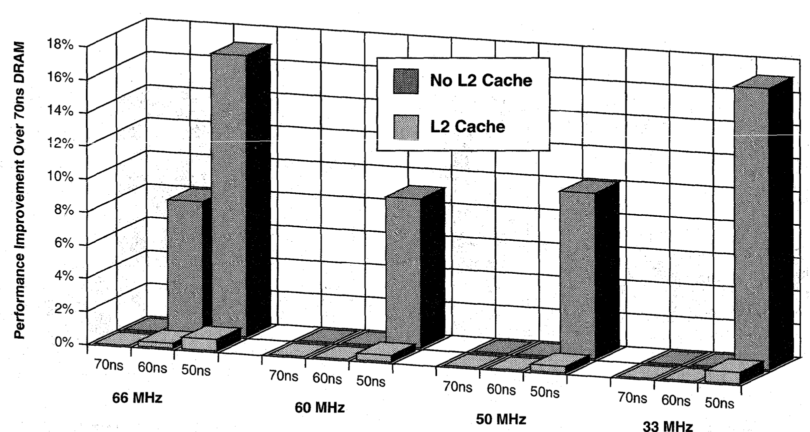

Figure 3
DRAM MEMORY PERFORMANCE IN PCs

NEW TECHNICAL NOTE

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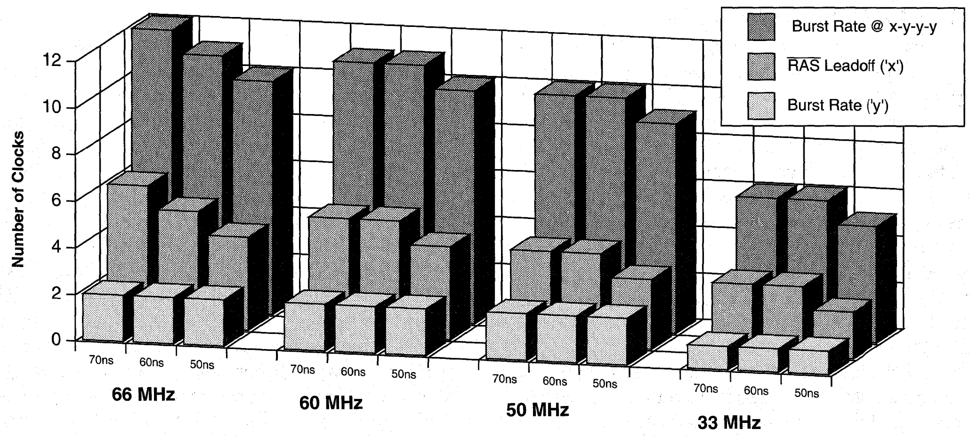

Figure 4
DRAM SPEED vs. CLOCKS IN PCs

The difference between a DX4-486 microprocessor (33 MHz external clock, 100 MHz internal clock) and a 33 MHz DX-486 when using 50ns and 70ns DRAMs is evaluated in Table 1.

This analysis shows that clocked-multiplied microprocessors put more demand on the external memories. For example, 70ns DRAMs require 8 percent of the memory accessing time with a typical 33 MHz-486DX but the clock-tripled 33 MHz-486DX4 requires 17 percent of the memory accessing time. Even with this additional demand on the DRAM memory performance, the performance improvement obtained from using a 50ns DRAM over a 70ns is negligible. The 50ns DRAM only improves the leadoff cycle (i.e., one clock and fails to improve the burst rate).

Table 1
EFFECTS OF MULTIPLE-CLOCKED MICROPROCESSORS

Memory Type	L1-Cache	L2-Cache	70ns DRAMs	50ns DRAMs
33 MHz-486DX				
Percent of accesses	80%	16%	4%	4%
Clocks per burst	5 (2-1-1-1)	5 (2-1-1-1)	11 (5-2-2-2)	10 (4-2-2-2)
Clocks seen by µP	5	5	11	10
Time allocation for burst	76.3%	15.3%	8.4%	n/a
Time allocation for burst	77%	15.3%	n/a	7.7%
100 MHz-486DX4				
Percent of accesses	80%	16%	4%	4%
Clocks per burst	5 (2-1-1-1)	5 (2-1-1-1)	11 (5-2-2-2)	10 (4-2-2-2)
Clocks seen by µP	5	15	33	30
Time allocation for burst	52%	31%	17%	n/a
Time allocation for burst	52.5%	31.5%	n/a	16%

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PERIPHERAL COMPONENTS

Besides microprocessor accesses, DRAM memory is accessed by peripheral components. Non-cached peripheral components access the DRAM main memory over either the ISA or the local bus. As previously discussed, even without cache memory, faster DRAMs do not necessarily equate to increased performance.

Figure 5 depicts the leadoff and Page-Mode cycles of today's faster DRAMs while being accessed by peripheral components over either the ISA or the local bus. As the DRAM speed improves, the burst rate does not improve since the speed improvement is not sufficient enough to reduce the number of clocks required. And in the bus speeds used the burst rate is already at one clock.

In most cases the leadoff cycle does not change between speed versions either. The only improvement in DRAM memory accesses by peripheral components is obtained when using 50ns DRAMs over slower DRAMs at 33 MHz. Additionally, main memory accesses by peripheral components are typically long streams of data (i.e., Page Mode) which minimizes the improved leadoff time obtained from the faster DRAMs. For example, assume a burst of 128 words. The 50ns DRAM-based main memory would only be 0.8 percent faster than using 70ns DRAMs in a 33 MHz local bus. Such a negligible performance increase makes it difficult to justify speed premiums associated with fast DRAMs.

DRAM SOFT ERRORS

There has been much discussion regarding DRAM soft error rate (SER) with the common question being asked "Do I need parity?" A previous technical note, TN-04-28, "DRAM Soft Error Rate Calculations," (1Q94), discussed the issue of parity in detail and provides a system designer with the information needed to answer this question. However, it is worth noting that when L1 and L2 cache memory is utilized, DRAM is accessed only one to four percent of the time. This leaves the DRAM main memory in the standby mode the remainder of the time. As mentioned in the same technical note, SER is highly dependent on the DRAM cycle rate. A DRAM is less susceptible to soft errors (by approximately a factor of 20x) when in standby mode (only refresh cycles) than when being accessed at a fast cycle rate.

Figure 6 depicts a typical 32-bit wide, 4MB, DRAM-based main memory's mean time between failures (MTBF) over various utilization rates (READ/WRITE accesses at 200ns). For example, a system with cache memories obtaining a 96 percent hit rate (80 percent L1 and 80 percent L2 Cache memory hit rates) can expect one DRAM soft error during 125 years of continuous use because it sees only a four percent utilization rate.

The same DRAM memory would expect one DRAM soft error every 25 years if only L1 cache (80 percent hit rate or 20 percent utilization rate) was employed. On the other extreme, the same DRAM memory in a non-cached (no L1 or L2 cache memory) system would see around a 50 percent to 70 percent utilization rate. These conditions would result in approximately one DRAM soft error every 10 years.

SUMMARY

The addition of cache memory not only achieves its objective of minimizing microprocessor wait states, but it also demands less of the DRAM main memory. With cache memory, the need for faster DRAMs and parity memory are all but eliminated in most designs. When improving main memory speed, focus on DRAM Page Mode speed (^{t}PC) rather than leadoff (^{t}RAC) speed.

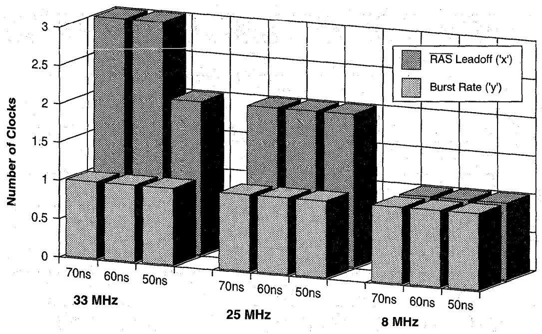

Figure 5
DRAM SPEED vs. LOCAL/ISA BUS ACCESSES

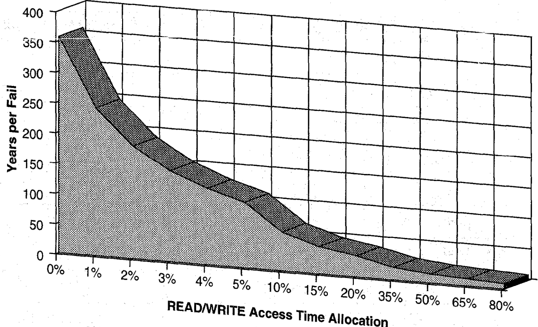

Figure 6
DRAM MTBF TO SOFT ERRORS vs. ACCESS RATE

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TECHNICAL NOTE

DECREMENT BURSTING WITH THE SGRAM

INTRODUCTION

Decrement bursting is a useful operation in many graphics applications, especially in a GUI environment. Any graphics memory device that facilitates this operation, such as the synchronous graphics RAM (SGRAM), provides system level benefits including reduced design complexity and increased performance.

There are several methods that can be used to achieve full-speed decrement bursting in synchronous DRAM (SDRAM)/SGRAM based graphics memory implementations. This note describes the various methods and the tradeoffs associated with each.

DECREMENT BURSTING

There are several instances in graphics applications where it is desired to access a series of pixels (in a line on the display) from right to left. This might occur when performing overlapping BITBLTs or when scrolling text horizontally within a window.

Pixels are typically mapped in memory such that moving from right to left in a section of a line on the screen means moving from a column location with a higher address in a row in memory to a column with a lower address. To perform the above operation requires the ability to burst sequentially from a starting column address to decreasing (or decrementing) column addresses within a row.

EXPLICIT COMMAND

One vendor of SDRAMs in a graphics configuration (256K x 16) has created an explicit command mode to accomplish decrement bursting, however this approach has several drawbacks. One drawback is that this command mode is additional to the defined command set for SDRAMs/SGRAMs. This means that both the controller and the memory devices must contain additional logic to support the new command mode. Another drawback is that the new command must be executed every time there is a change in direction (from incrementing to decrementing, and vice versa). This results in additional overhead, in the form of Mode Register accesses. In addition, this new command mode is not available from other vendors.

Alternatively, the methods described below can be achieved on any SDRAM/SGRAM with a pipelined architecture, which includes all SGRAMs and all SDRAMs tailored for graphics applications. In addition, these methods use the existing command sets defined for SDRAMs/SGRAMs and allow for operation at the maximum burst rate of the device.

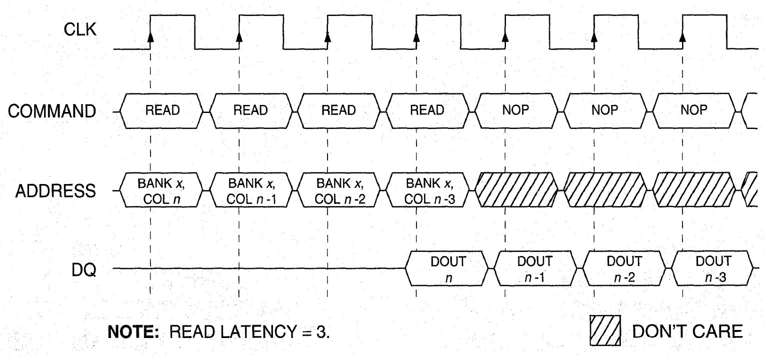

Figure 1
DECREMENT BURSTING - NEW COLUMN ADDRESS EVERY CYCLE

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RANDOM COLUMN ACCESS

SDRAMs/SGRAMs with a pipelined architecture can accept a new read or write command and column address on each cycle during a burst access within a page. This provides the capability to sequentially access incrementing or decrementing column addresses, as well as to randomly access column locations within a page at the maximum burst rate of the device.

Providing a new read or write command and column address on each clock cycle is the most flexible way to achieve decrement bursting because it can be used regardless of the programmed burst length and burst type. In addition, this method does not require any Mode Register accesses, thereby avoiding that additional overhead. An example is shown in Figure 1.

The only drawback of random column access is that the address and command busses are used during every clock cycle. However, this is no different from the way these operations are performed with conventional FPM DRAMs or EDO DRAMs and full-speed random access is a significant benefit.

SUCCESSIVE BURSTS OF TWO

The programmed burst length of two for SDRAMs/SGRAMs is inherently bidirectional. If the burst starts at the first location in the block of two; i.e., the least significant address bit is zero, then the address will increment for the next access; if the burst starts at the second location in the block of two; i.e., the least significant address bit is one, then the address will decrement for the next access. Longer incrementing bursts can be constructed by issuing successive read or write commands to incrementing even addresses every other clock cycle. Similarly, longer decrementing bursts can be constructed by issuing successive read or write commands to decrementing odd addresses on every other clock cycle.

In the case where a decrementing burst needs to start at an even address, the initial command issued for the even address simply needs to be followed immediately with the command to the previous (odd) address. After that, a command would be issued on every other cycle to the decrementing odd addresses. A similar procedure would be used to start an incrementing burst from an odd address.

After this initial orientation, if necessary, the address and command busses are available every other cycle for other commands. Examples are shown in Figures 2 and 3.

Additional overhead in the form of Mode Register accesses is only required if the burst of two is not the preferred mode of operation for other accesses.

CLK
COMMAND: WRITE, NOP, WRITE, NOP, WRITE, NOP
ADDRESS: BANK x, COL 61; BANK x, COL 59; BANK x, COL 57
DQ: DIN 61, DIN 60, DIN 59, DIN 58, DIN 57, DIN 56
DON'T CARE

Figure 2
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF TWO - STARTING AT AN ODD COLUMN ADDRESS

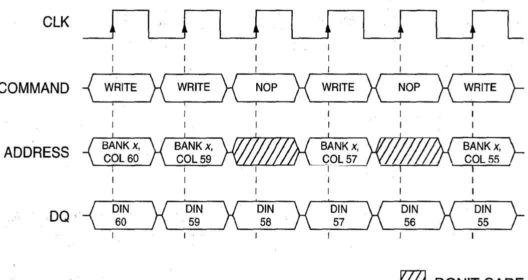

Figure 3
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF TWO - STARTING AT AN EVEN COLUMN ADDRESS

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SUCCESSIVE BURSTS OF FOUR OR EIGHT

A programmed burst length of four (eight) is bidirectional if starting at either the first or last location in the block and the burst type is "interleaved". If the burst starts at the first location in the block; i.e., the two (three) least significant address bits are all zeroes, then the address will increment for the next three (seven) accesses; if the burst starts at the last location in the block; i.e., the two (three) least significant address bits are all ones, then the address will decrement for the next three (seven) accesses. Longer incrementing bursts can be constructed by issuing successive read or write commands to every fourth (eighth) incrementing column address on every fourth (eighth) clock cycle, and similarly, longer decrementing bursts can be constructed by issuing successive read or write commands to every fourth (eighth) decrementing column address on every fourth (eighth) clock cycle.

In the case where a decrementing burst needs to start at a location other than the last in the block, individual commands must be issued on each clock until the lower boundary is reached. A command would then be issued on every fourth (eighth) cycle to every fourth (eighth) decrementing column address. A similar procedure would be used to start an incrementing burst from any address other than the first address in the block.

After this initial orientation, if necessary, the address and command busses are available three of four (seven of eight) clock cycles, for other commands. Examples are shown in Figures 4 and 5.

Additional overhead in the form of Mode Register accesses is only required if the interleaved burst of four (eight) is not the preferred mode of operation for other accesses.

SUMMARY

The SGRAM, with it's pipelined architecture, provides high speed burst access (66-100 MHz) while still offering the ability to change the column address for each access. This ability leads to full-speed random, incrementing, or decrementing burst accesses within a row in memory.

Decrement bursting in particular can be achieved using one of several different methods which rely only on existing command modes defined for SDRAM/SGRAMs. Each method represents a different combination of flexibility, complexity, overhead, and command and address bus utilization. Regardless of the method selected in a given system, full-speed decrementing accesses can be achieved without a dedicated and additional command mode.

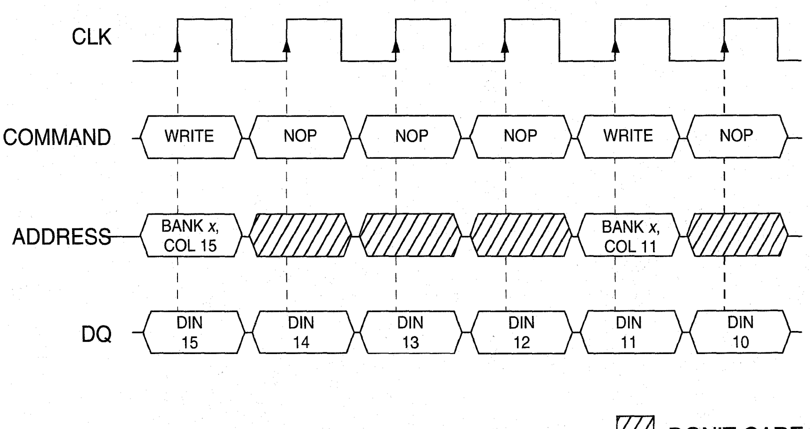

Figure 4
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF FOUR - STARTING AT THE LAST COLUMN ADDRESS IN THE BLOCK

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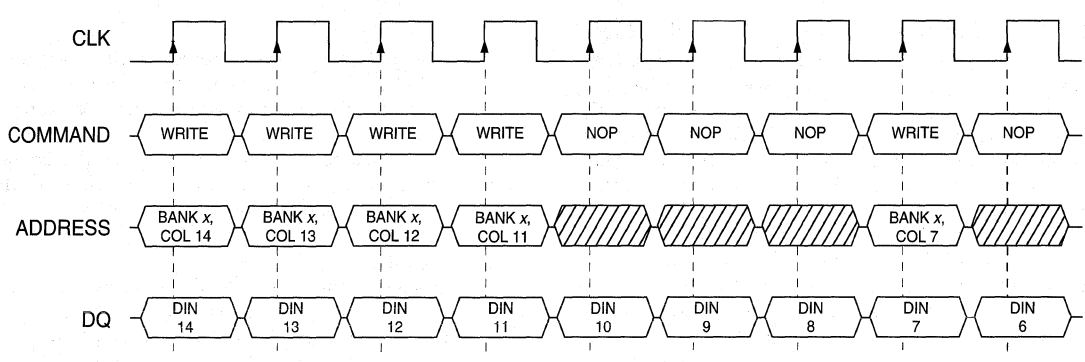

Figure 5
DECREMENT BURSTING WITH SUCCESSIVE BURSTS OF FOUR - STARTING AT THE SECOND COLUMN ADDRESS IN THE BLOCK

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TECHNICAL NOTE

88-PIN DRAM CARDS

INTRODUCTION

Just as SIMMs began a new period in memory placement and packaging in the 1980s, the 88-pin DRAM card promises to have an equal impact on the industry in the 1990s. The 88-pin DRAM card combines the architecture of a SIMM with an memory card form factor to create a high density, easy-to-use memory device. No longer do end-users have to disassemble their systems and risk ESD damage to add more SIMM modules or memory boards. Finally, a sensible approach to memory packaging has arrived.

For engineers, Micron's 88-pin DRAM cards offer a significant improvement in the way system designers manage main and add-in memory. DRAM memory cards require less system interface logic, they pack more memory into a given area than SIMM modules and they are better able to withstand more use and abuse than contemporary memory upgrade schemes. All this functionality is contained in a convenient, portable and standardized package.

Standards for the 88-pin DRAM card have been jointly ratified by the three major standard-setting bodies: PCMCIA, JEDIA and JEDEC. As a companion to the 68-pin memory card, or by itself, the 88-pin DRAM card will enhance your product design or offerings.

DRAM cards provide a rigid and durable enclosure for the printed circuit board and memory devices contained within. The card's physical dimensions are 2.126 ±0.004 inches wide by 3.37 ±0.004 inches long by 0.129 ±0.004 inches thick, which is about the same dimension as a credit card, though three times its thickness.

Once assembled, the strength of the DRAM card surpasses that of SIMM modules. Moreover, since the card's components are not subjected to direct physical contact by the user, it can withstand casual, even abusive, handling much better than a SIMM module. When a SIMM module is installed, removed or transported, there is a risk of inflicting damage due to ESD. The card is made with a conductive plastic that allows static charges to be safely dissipated to the ground pins via a High-Z path.

DRAM cards are designed to ease facilitation. Though the DRAM cards appear to function like 72-pin SIMM modules, significant differences favor the DRAM card. For example, the DRAM card provides its own buffering for its control lines, relieving the system board. Furthermore, buffering enhances system performance, both from noise reduction and reduced capacitive loading of the control lines.

The DRAM cards are preferable to SIMMs in small profile notebook and palmtop computers, because the cards offer a twofold improvement in board area usage. Proper choice of receptacle connector for the system board provides the ability for hot insertion or removal, which is impossible for a SIMM module. And the DRAM card's size and ruggedness make it ideal for mainframe or industrial applications.

Table 1
MEMORY ADDRESS RANGE

DRAM ADDRESS SPACE PER BANK	MEMORY ADDRESS RANGE					
	PRESENCE-DETECT BITS					TOTAL MEMORY SIZE
	PD1	PD2	PD3	PD4	PD5 = 0	PD5 = 1
no card installed	1	1	1	1	n/a	n/a
256K	0	0	0	0	1MB	2MB
512K	1	0	0	0	2MB	4MB
1 Meg	0	1	0	0	4MB	8MB
2 Meg	1	1	0	0	8MB	16MB
4 Meg	0	0	1	0	16MB	32MB
8 Meg	1	0	1	0	32MB	64MB
16 Meg	0	1	1	0	64MB	128MB

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PRESENCE-DETECT DEFINITIONS FOR THE 88-PIN DRAM CARD

It is necessary to clarify the presence-detect definitions for the 88-pin DRAM cards. The eight presence-detect pins are divided into four groups, consisting of memory size (four bits), number of DRAM banks (1 bit), DRAM access timing (two bits) and refresh control (1 bit). As shown in Table 1, presence-detect bits are defined as 0 = ground, 1 = open.

Presence-detect bits PD1, PD2, PD3 and PD4 relate to the byte size of the card or its memory address range. The PD5 presence-detect indicates the number of memory banks present on the card. The card will be provided with either one or two banks (32-bit version) or two or four banks (16-bit version).

For 32-bit applications, PD5's definition relates to whether one or two banks are present. Each bank is defined by two RAS lines. In other words, both RAS lines should be activated simultaneously for a 32-bit word access. When PD5 = 0, there is one bank present, activated by RAS0 and RAS2. When PD5 = 1, there are two banks present. Bank 1 is activated by RAS0 and RAS2 while Bank 2 is activated by RAS1 and RAS3.

For 16-bit applications, PD5's definition relates to whether two or four banks are present. Each bank is defined by a single RAS lines. When PD5 = 0, two banks are present, activated by RAS0 and RAS2. When PD5 = 1, two additional banks are present, activated by RAS1 and RAS3. A logical progression within the system's address space would be RAS0, RAS2, RAS1 and RAS3 in that order. For a 32-bit data bank interpreted as an 16-bit card, RAS relates to the data bus as shown in Table 2.

The PD6 and PD7 presence-detects indicate the access time of the card from RAS true to data-out. They are defined in Table 3.

The PD8 presence-detect is related to the refresh type of the card, either SELF REFRESH when PD8 = 0, or an extended refresh when PD8 = 1. Presently, all DRAM cards will leave PD8 open, indicating that the system should provide refreshing, preferably a CAS-BEFORE-RAS type of refresh. This allows an address-independent refresh, which allows interchangeability among different card types.

Table 2
RAS RELATION TO DATA BUS

RAS0	D0-D17	Bank 1
RAS1	D18-D31	Bank 2
RAS2	D0-D17	Bank 3
RAS3	D18-D31	Bank 4

Table 3
DATA-OUT ACCESS TIME

ACCESS TIME	PD7	PD6
100ns (or 50ns for future cards)	0	0
80ns	0	1
70ns	1	0
60ns	1	1

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Table 4
32-BIT PRODUCT OFFERINGS

PRODUCT NUMBER (32-BIT SERIES)	MEMORY SIZE (MB)	WORD LENGTH (BITS)	POWER SUPPLY	SPEED
MT8D88C132-xx	4	16, 32	5V	60-80ns
MT8D88C132V-xx	4	16, 32	3.3V	70-80ns
MT16D88C232-xx	8	16, 32	5V	60-80ns
MT16D88C232V-xx	8	16, 32	3.3V	70-80ns
MT8D88C432V-xx	16	16, 32	3.3V	60-80ns
MT16D88C832V-xx	32	16, 32	3.3V	60-80ns

PRODUCT OFFERING

DRAM cards are offered through Micron. The current product spectrum provides memory sizes from 4MB to 32MB with x16/x32 data path, and both 5V and 3.3V operation. Micron's product offering is shown in Table 4. The series is provided with speed grades from 80ns to 60ns. This is specified with a -8, -7 or -6 suffix to the part number where "xx" is shown. The cards use low-power, extended-refresh DRAMs. Cards using a 3.3V supply have their part number appended with a "V" option.

In addition, all versions of the standard DRAM card are available in a two-inch-long, bufferless version. Contact Micron for further details

SERVICES

Micron stands ready to help customers who wish to enter the IC DRAM card market with proprietary solutions. Our staff engineers are well-versed in the design of boards for the entire PCMCIA/JEDEC/JEIDA arena. If one of our standard products does not meet your current needs, we are ready and able to design a custom solution for you.

For customers desiring a standard product under private label, Micron can supply current products labeled and marked in virtually any manner the customer wishes. Simply supply us with the desired artwork and markings—Micron will do the rest.

Often overlooked by companies considering entrance into the DRAM card market are the mechanical considerations. Micron has invested considerable time and effort into developing superior card frames, covers and components. Our custom design services break down the significant entry barriers to this burgeoning market and will get your product to market on time and on budget. Design services include:

- Design from concept
- Schematic capture
- Board layout
- Enclosure design
- Thermal and signal noise analysis
- Custom marking
- Comprehensive testing
- Connector redesign
- ASIC solutions
- Packaging solutions

Applications engineering assistance is also available from 8 a.m. to 5 p.m. Mountain Time by calling 208-368-3900.

The DRAM card arena is very fast-paced. Product development and introduction will quickly outdate current information. When contemplating a design in this arena, please call us for the latest product datasheets and design guidelines.

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OVERVIEW

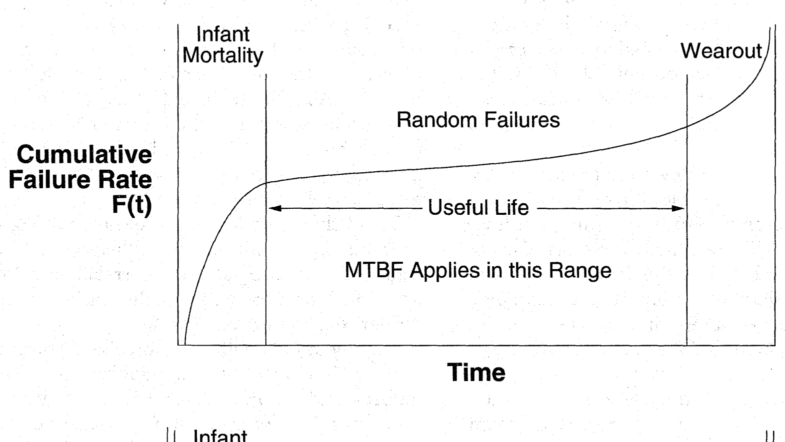
Product reliability is a product's ability to function within given performance limits, under specified operating conditions over time. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at $t_0 + 1$ in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failures and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX® intelligent burn-in/test system developed by Micron is described in the following section.



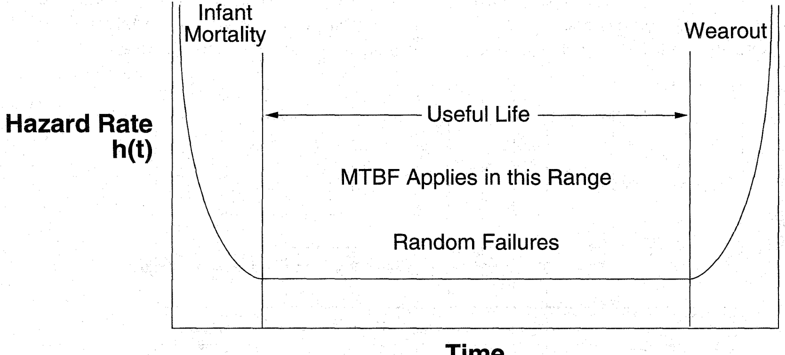


Figure 1
RELIABILITY CURVE

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MICRON'S AMBYX® INTELLIGENT BURN-IN AND TEST SYSTEM

Burn-in refers to the process of accelerating failures that occur during the infant mortality phase of component life to remove the inherently weaker devices. The process has been regarded as critical for ensuring product reliability since the beginning of the semiconductor industry. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, when we were unable to find a system that met our requirements, we introduced the concept of "intelligent" burn-in and developed the AMBYX intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings to our attention the slightest variation in a product's failure rate.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, Vcc voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot. These test results allow us to identify individual failures after each burn-in cycle.

There are two important reasons why Micron conducts the last two burn-in and test periods (or "quarters") at lower Vcc than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test used by IC manufacturers to compute random field failure rates. Second, we want to be sure we are not introducing new failure modes unrelated to normal wearout, such as VOS, by testing them at extremely elevated conditions.

Trend charts, such as the one shown in Figure 2, alert us to trends in lot failure rates. When we detect an upward trend in a failure rate, we correlate the lots that need additional burn-in with all the variables that might be influencing the increased rate.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

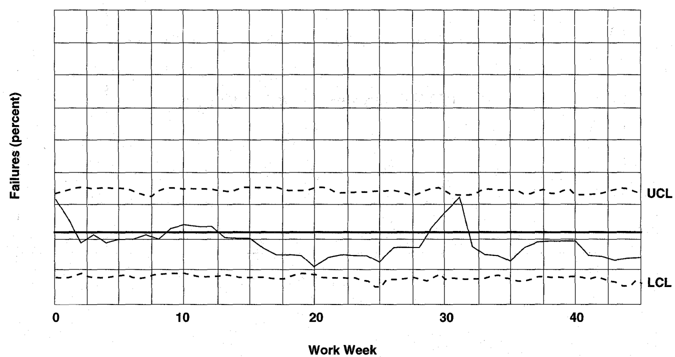

Figure 2
AMBYX FOURTH QUARTER FAILURES

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ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use. Table 1 shows the conditions for these tests, known as environmental stress tests. The EPM program described in Table 1 is for Micron's 3.3V 16 Meg DRAM.

Table 1
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 16 MEG DRAM

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 4.3V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	50 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% RH, 4V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% RH, 15 PSI, No Bias)	96 Hours	50 Devices
LOW TEMPERATURE LIFE (-25°C, 4.5V, Checkerboard/Checkerboard Complement Pattern)	1,008 Hours	15 Devices
TEMPERATURE CYCLE (-40°C for 15 min., +85°C for 15 min, air to air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C for 5 min., +125°C for 5 min., liquid to liquid)	700 Cycles	50 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015.7	40 Devices
V_{CC} LATCH-UP (MIN voltage, 25°C)	—	10 Devices
SYSTEM SOFT ERROR (3V, 0.3ms, Checkerboard/Checkerboard Complement Patterns)	168 Hours	1,020 Devices

NOTE: Samples used in the EPM program are taken from five different lots at finished goods. Before being subjected to environmental testing, all surface-mount products are run twice through an infrared (IR) reflow furnace, reaching a peak temperature of 240°C.

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FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as percent failures per thousand device hours or as FITs (failures in time, per billion device hours). Using Micron's 16 Meg DRAM as an example, the failure rate is calculated as follows:

$$\text{Failure Rate} = \frac{Pn}{\text{Device hours} \times AF}$$

where: Pn = Poisson Statistic (at a given confidence level). In our example given seven device failure, Pn = 0.916 at 60 percent confidence level.

Device hours = sample size multiplied by test time (in hours) In our example, device hours equal 1.125×10^6 in an accelerated environment. From the table below, device hours equal:

$(1{,}125 \times 168) + (1{,}125 \times 168) + (1{,}122 \times 168) + (1{,}115 \times 168) + (1{,}106 \times 168) + (1{,}105 \times 168) = 1{,}125{,}264$ or 1.125×10^6

AF = acceleration factor between the stress environment and typical use conditions. For the 16 Meg DRAM, the acceleration factor between 125°C, 4.3V (HTOL stress conditions) and 50°C, 3.3V (typical operating conditions) equals 56. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 16 Meg DRAM family is computed as follows:

$$\text{Failure Rate} = \frac{0.916}{(1.125 \times 10^6)(56)} = 1.454 \times 10^{-8}$$

where: total device hours at test conditions = 1.125×10^6. Equivalent device hours at typical use conditions (50°C, 3.3V Vcc) using an acceleration factor of 56 equals $56\ (1.125 \times 10^6) = 63 \times 10^6$.

To translate this failure rate into percent failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

Failure Rate = $(1.454 \times 10^{-8}) \times 10^5$ = 0.001454% or 0.0015% per 1K device hours

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

Failure Rate = $(1.454 \times 10^{-8}) \times 10^9$ = 1.454 or 15 FITs.

Table 2
HIGH TEMPERATURE OPERATING LIFE (HTOL)

Sample No.	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
1	0/0225	0/0225	0/0225	0/0225	0/0225	0/0225
2	0/0307	0/0307	0/0307	0/0306	0/0306	0/0306
3	0/0527	0/0527	0/0524	0/0522	0/0513	0/0513
4	0/0066	0/0066	0/0066	0/0062	0/0062	0/0061
Total	0/1125	1/1125	0/1122	0/1115	0/1106	0/1105

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ACCELERATION FACTOR CALCULATION

Again, using the 16 Meg DRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 4.3V) and typical operating conditions (50°C, 3.3V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\frac{E_a}{k}\left[\frac{1}{T_O} - \frac{1}{T_S}\right]}$$

where: k = Boltzmann's constant , which is equal to 8.617×10^{-5} eV/K.

T_O and T_S = typical operating and stress temperatures, respectively, in kelvins.

E = activation energy in eV. (For oxide defects, which is the most common failure mechanism for the 16 Meg DRAM used in our example. The activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.62.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_V = e^{\beta (V_S - V_O)}$$

where:

v_S and v_O = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 16 Meg DRAM used in our example, β equals 2).

Thus, the voltage acceleration factor for the 16 Meg DRAM between 4.3V (stress condition) and 3.3V (typical operating condition) is computed to be 7.39.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$AF_{overall} = AF_{temperature} \times AF_{voltage}$$
$$= 7.62 \times 7.39$$
$$= 56$$

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OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a sample from each production lot. These samples are subjected to visual and electrical testing to measure the acceptable quality level (AQL) of all outgoing product. Test flows for new products that have not met required production volume and ppm levels are more comprehensive than for mature products. Over a period of time, as a product matures, the objective is to eliminate those tests which devices never fail. AQL testing, although it is performed on only a small percentage of each product, is much more exhaustive. Conducted at spec conditions without guardband for every known timing, pattern and background, it is a sanity check on the production test flow. Its purpose is to detect subtle shifts in defect mechanisms which the production test flow may not catch.

Visual testing for mechanical defects consists of visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Testing is conducted at 0°C, or room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the devices are retested beginning at that point in the test flow. These are important steps to preserve the integrity of our test process.

AUTOMATED DATA CAPTURE AND ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 3 shows the various functional areas that provide the input to our VAX data bases.

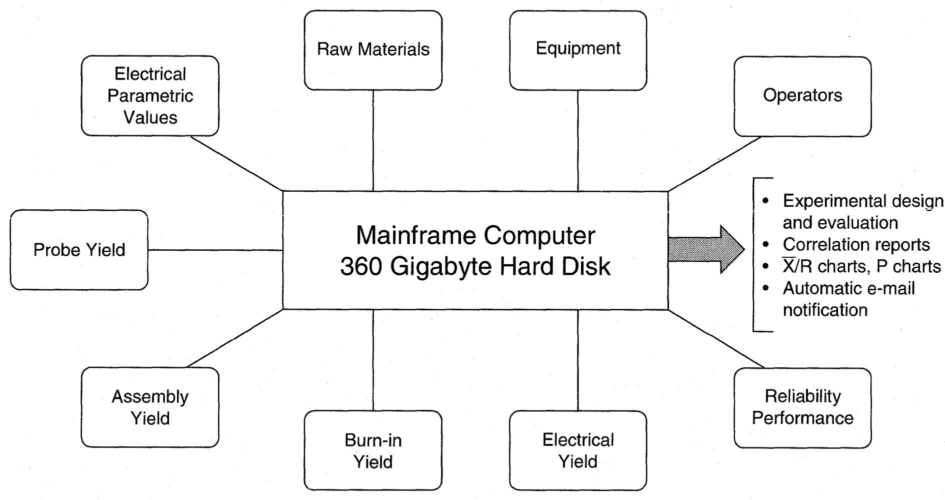

Figure 3
STATISTICAL CORRELATION

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DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors, such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL (SPC) CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE/MULREG

This analysis software is used for experimental design and evaluation of results. The statistical approach supported by this software (*t* tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble-shooting. It is also used to determine the relationships between process output, probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.

GAUGE CAPABILITY STUDIES

These studies are performed on both new and existing equipment. Gauge studies help us understand the cause of variation in a measurement process and determine the amount of variation in the system.

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FABRICATION*

INCOMING → PHOTOLITHOGRAPHY → ETCH → IMPLANT → DIFFUSION → METAL → PASSIVATION → PROBE → TO ASSEMBLY

Incoming
Verification that the starting material is clean, uniform and compliant with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping" and forms conductive regions on the wafer.

Diffusion
Silicon dioxide, nitrite and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases which either react with the silicon, causing it to oxidize and form an SiO_2 layer or react with each other, forming poly and nitrite deposits. These layers are patterned using photolithography and form the layers of the diodes, transistors and capacitors of the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many die. Each individual die on the wafer is taken through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map," storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good die are packaged.

Assembly (see next page)

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ASSEMBLY*

FABRICATION → WAFER MOUNT → WAFER SAW → DIE ATTACH → DIE ATTACH CURE → WIRE BOND → MOLD → LASER MARK/DEFLASH → POST-MOLD CURE → LEAD FINISH → TRIM/FORM → TO TEST

Fabrication
Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Mount
Fabricated wafers are automatically mounted on a carrying film.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Die Attach Cure
The die-attached leadframes are cured in an oven to fully polymerize the die attach adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire the diameter of a human hair. These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Mold
A heated mold with a hydraulic mechanism is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark/Deflash
A laser mark is scribed on the bottom and top sides of the package. This mark is a code used to identify the assembly manufacturing lot. Prior to lead-finish processing, the leadframes are run through chemical baths to clean lead surfaces. This process is known as deflash.

Post-Mold Cure
Molded leadframes are placed in an oven to complete the polymerization of the epoxy encapsulant.

Lead Finish
Each package is given a lead finish of tin/lead (electroplating) to ensure reliable application by the customer.

Trim/Form
A press with a tool set is used to cut and form leads of the lead frame into specified shapes. Some packages have leads formed for surface-mount applications. Other packages have leads for through-hole applications.

Test (see next page)

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TEST*

ASSEMBLY → HOT PREGRADE → BURN-IN → COLD TEST → HOT FINAL → COLD FINAL → MARKING → SCANNER → VISUAL INSPECTION → AQL → PACKAGING → FINISHED GOODS

Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Hot Pregrade
All testing (including speed sorting, parametric and functional testing) is conducted at 85°C; parts are tested for speed grade and functionality. Parametric tests are performed to detect opens, shorts, input/output leakage, input/output high and low levels and standby current. Functional tests include low and high Vcc margin, Vcc bump, speed sorting, dynamic and static refresh, long ^{t}RAS and ^{t}CAS lows, and a full range of algorithms and data backgrounds to verify AC parameters. Specific tests and temperatures are incorporated as applicable for specific products.

Burn-in
Micron uses its exclusive AMBYX® intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in, using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 5.7V Vcc for the first three intervals and 125°C, 4.3V Vcc for the final interval. Functional testing is performed at 85°C and back to 25°C AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 5.7V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Cold Test
Micron also uses its AMBYX test system to perform functional pattern tests at ambient, cold and hot temperatures. Low and high Vcc margin, dynamic (distibuted only) and static refresh, long ^{t}RAS and a full range of algorithms and data backgrounds are performed at temperatures ranging from -10°C to 90°C. To insure wire-bond integrity, testing is performed while temperature are ramped from 25°C to -10°C and back to 25°C.

Hot Final
All testing (including speed grade verification and parametric and functional testing) is conducted at 78°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether input/output high and low levels, and standby and operating currents are within specified limits. Functional tests include low and high Vcc margin, Vcc bump, speed verification, dynamic (distributed and disturbed) and static refresh, long ^{t}RAS and ^{t}CAS lows, and a full range of algorithms and data backgrounds to verify AC parameters.

Cold Final
Parametric and functional tests are conducted at -5°C. Parametric tests are performed to detect opens, shorts, and input/output leakage, and to determine whether input/output high and low levels and standby and operating currents are within specified limits. Functional tests include low and high Vcc margin, Vcc bump, speed verification, dynamic (distributed and disturbed) and static refresh, long ^{t}RAS and ^{t}CAS lows, and a full range of algorithms and data backgrounds to verify AC parameters.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay, coplanarity failures and tweeze failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices determined functional are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and repaired, if possible. Data on the type of defects found is carefully recorded and used for improving the manufacturing processes in both assembly and test.

AQL
A quality assurance monitoring program overseas the electrical and environmental performance of all production lots. New products which have not met required production volume and ppm levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron's requirements.

Packaging
Devices are prepared for shipping. They may remain in tubes or they may be mechanically placed in tape-and-reel packages, ready for application in automatic pick-and-place machines. Products will be either dry-packed in vacuum sealed bags, or placed in black antistatic bags.

Finished Goods
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on DRAM products.

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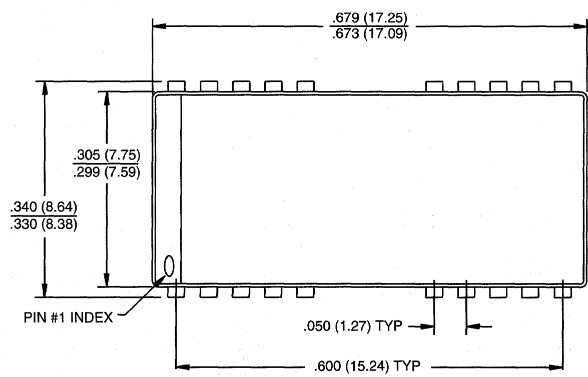
PACKAGE SELECTION GUIDE

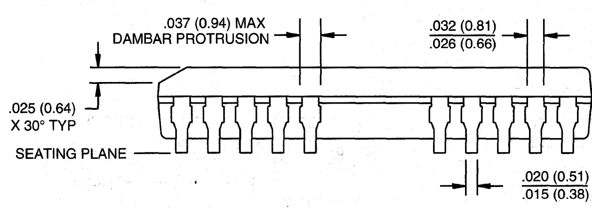
PACKAGE TYPE	REFERENCE CODE	PIN COUNT	WIDTH	PAGE
PLASTIC SOJ				
	DA-1	20/26	300 mil	9-1
	DA-2	24/26	300 mil	9-2
	DA-3	24/28	400 mil	9-3
	DA-4	28	300 mil	9-4
	DA-5	28	400 mil	9-5
	DA-6	34	500 mil	9-6
	DA-7	40	400 mil	9-7
	DA-8	42	400 mil	9-8
TSOP				
	DB-1	20/26	300 mil	9-9
	DB-2	24/26	300 mil	9-10
	DB-3	28	300 mil	9-11
	DB-4	40/44	400 mil	9-12
	DB-5	44/50	400 mil	9-13
TQFP				
	DC-1	100	14mm x 20mm	9-14

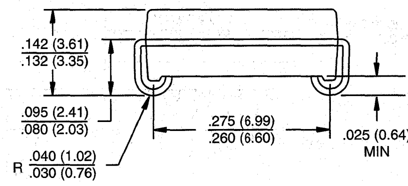
PACKAGE TYPE	REFERENCE CODE	PIN COUNT	HEIGHT	PAGE
MODULE SIMM				
	DD-1 to DD-2	30	0.5"	9-15
	DD-3 to DD-4	30	0.8"	9-16
	DD-5 to DD-10	72	1.0"	9-17
	DD-11 to DD-12	72	1.19"	9-20
	DD-13 to DD-18	72	1.0"	9-21
MODULE DIMM				
	DE-1 to DE-3	72	1.0"	9-25
	DE-4	72	1.25"	9-26
	DE-5	72	1.0"	9-27
	DE-6	72	1.25"	9-27
	DE-7 to DE-18	168	1.0"	9-28
DRAM CARD				
	DF-1	88	3.37"	9-38
	DF-2	88	2.0"	9-39
	DF-3	88	3.37"	9-40
	DF-4	88	2.0"	9-41

20/26-PIN PLASTIC SOJ (300 mil)

DA-1







NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

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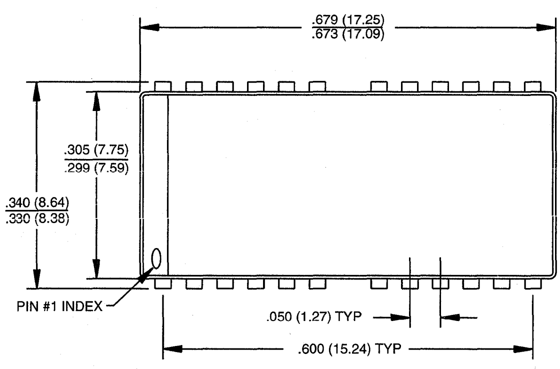
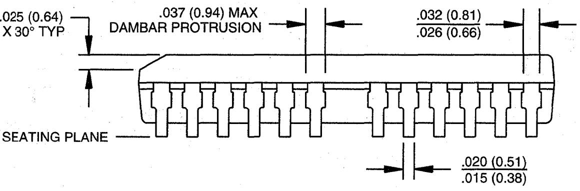
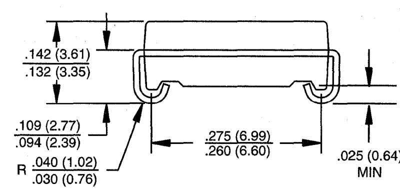
24/26-PIN PLASTIC SOJ (300 mil)

DA-2







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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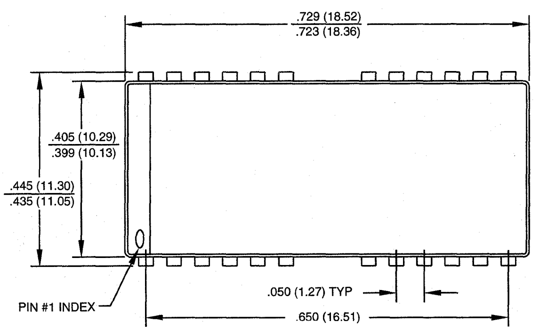
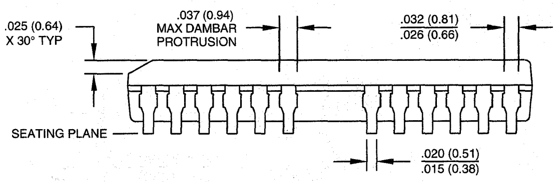
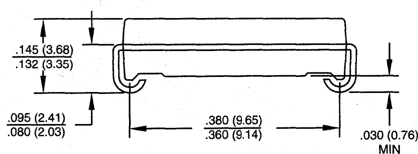
24/28-PIN PLASTIC SOJ (400 mil)

DA-3







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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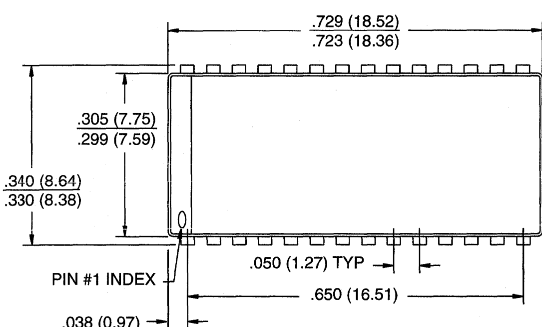
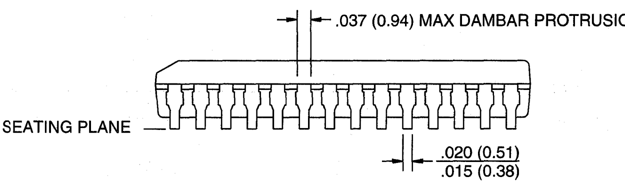
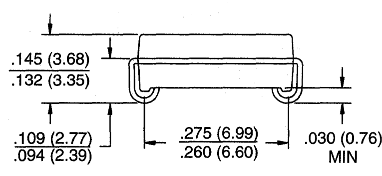
28-PIN PLASTIC SOJ (300 mil)

DA-4







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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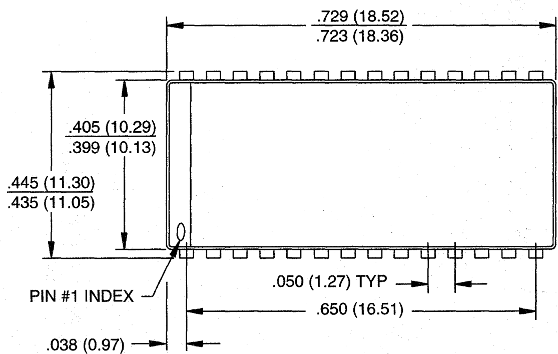
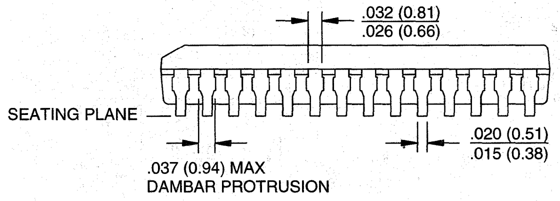
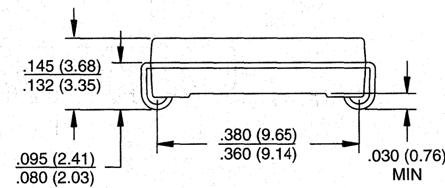
28-PIN PLASTIC SOJ (400 mil)

DA-5







NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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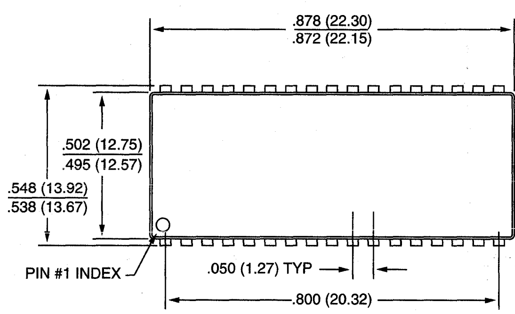
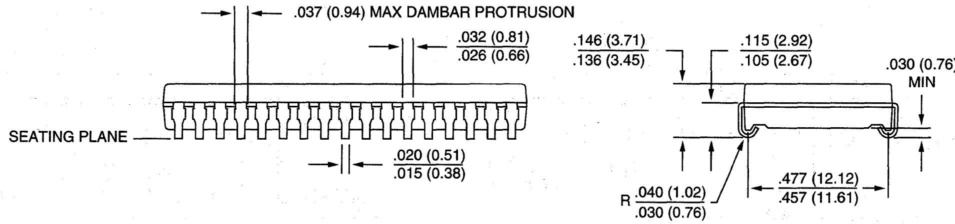
34-PIN PLASTIC SOJ (500 mil)

DA-6





PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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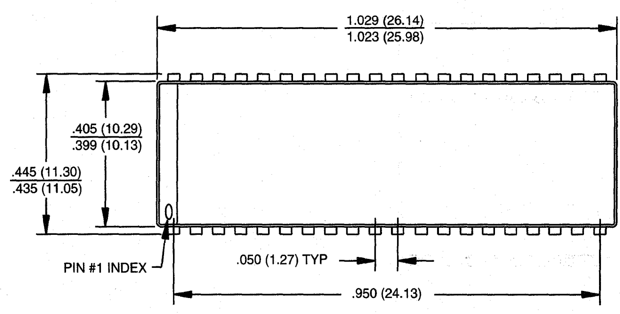
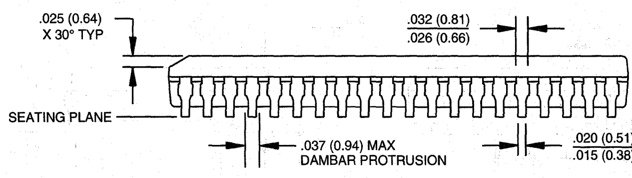
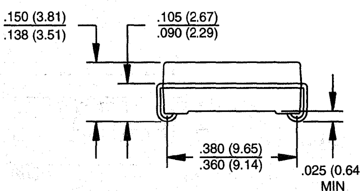
40-PIN PLASTIC SOJ (400 mil)

DA-7







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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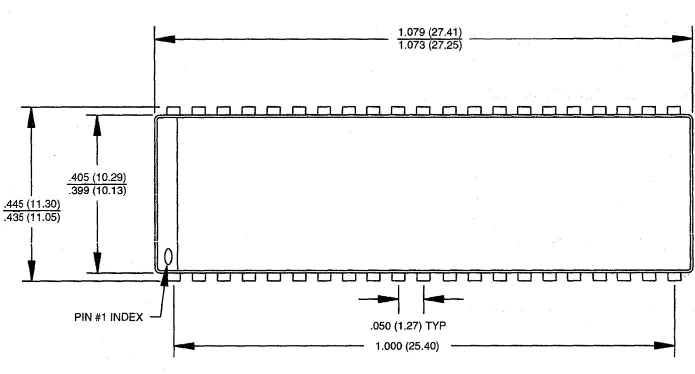
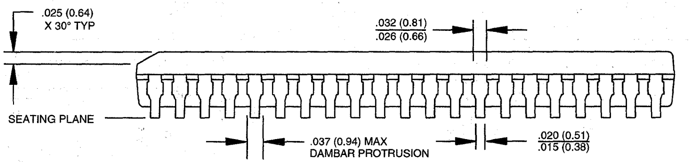
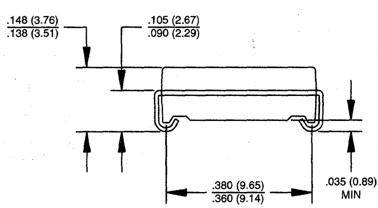
42-PIN PLASTIC SOJ (400 mil)

DA-8







PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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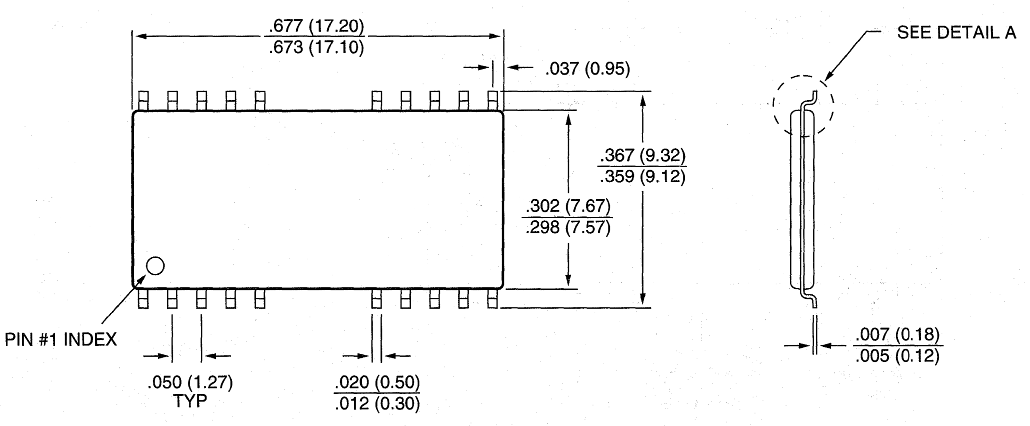
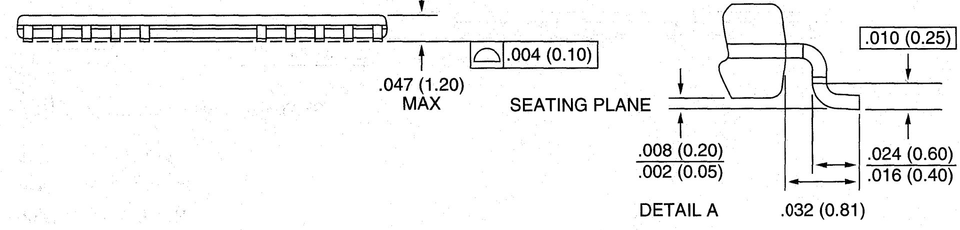
20/26-PIN PLASTIC TSOP (300 mil)

DB-1





NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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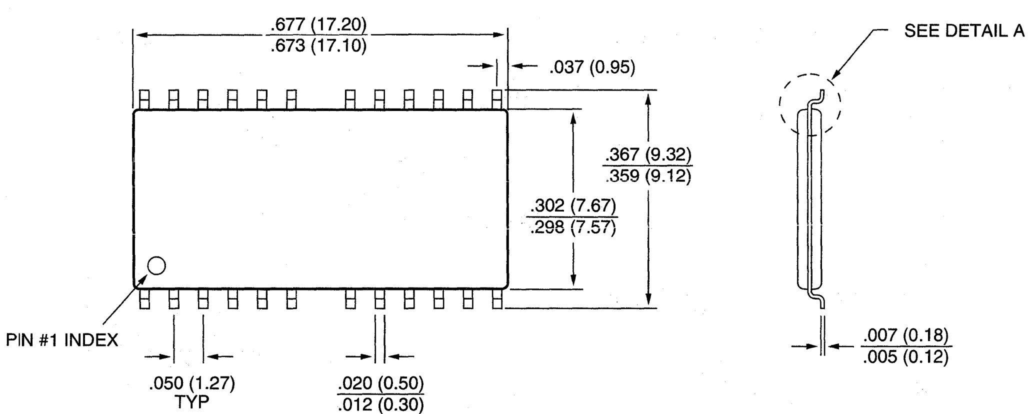
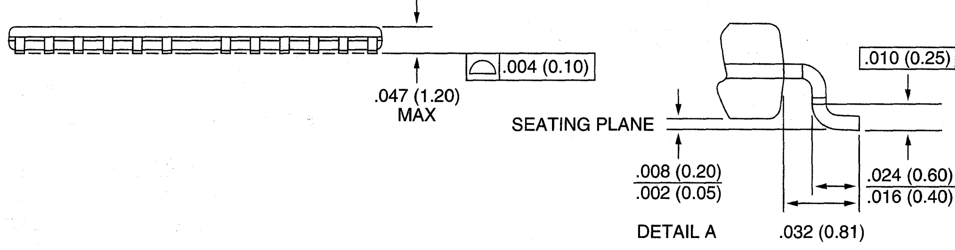
24/26-PIN PLASTIC TSOP (300 mil)

DB-2





NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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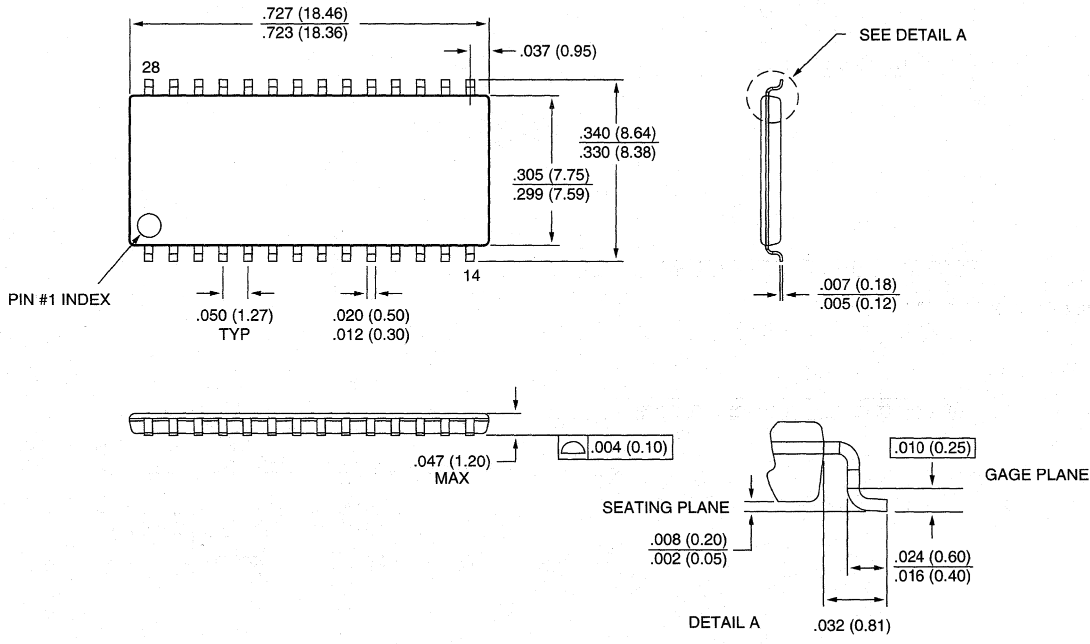
28-PIN PLASTIC TSOP (300 mil)

DB-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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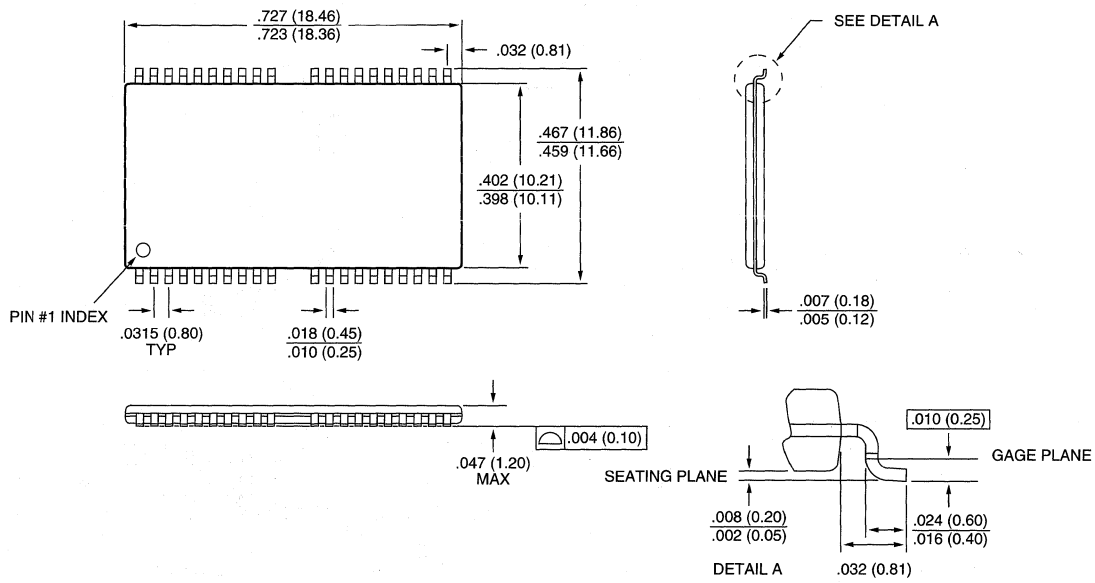
40/44-PIN PLASTIC TSOP (400 mil)

DB-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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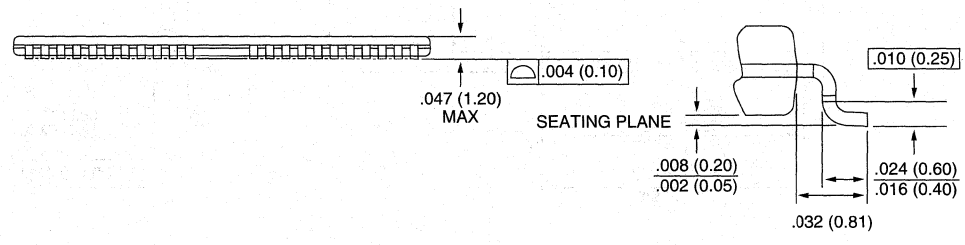
44/50-PIN PLASTIC TSOP (400 mil)

DB-5

.827 (21.01) / .823 (20.91)
.035 (0.88)
SEE DETAIL A
.467 (11.86) / .459 (11.66)
.402 (10.21) / .398 (10.11)
PIN #1 INDEX
.0315 (0.80) TYP
.018 (0.45) / .012 (0.30)
.007 (0.18) / .005 (0.12)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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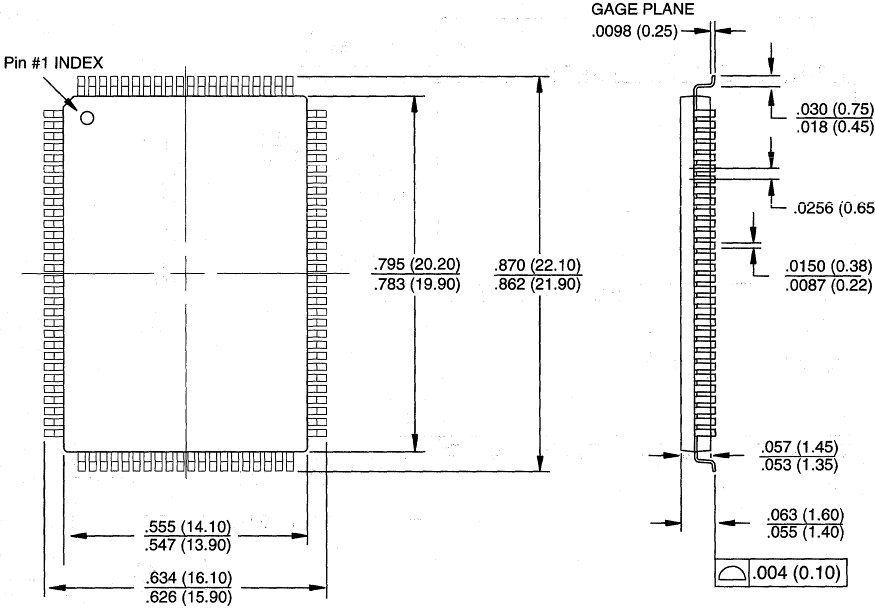
100-PIN PLASTIC TQFP

DC-1



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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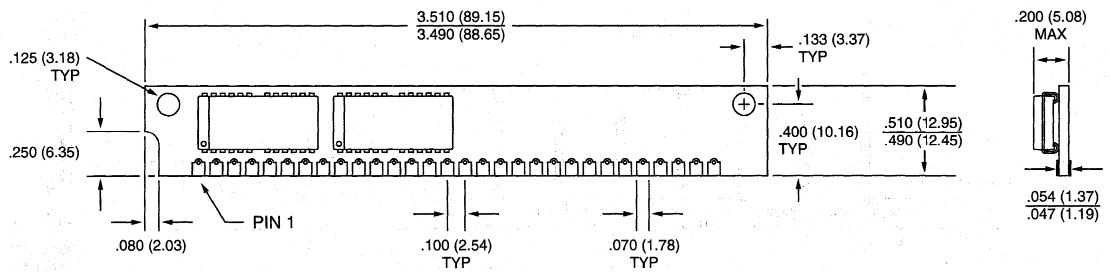
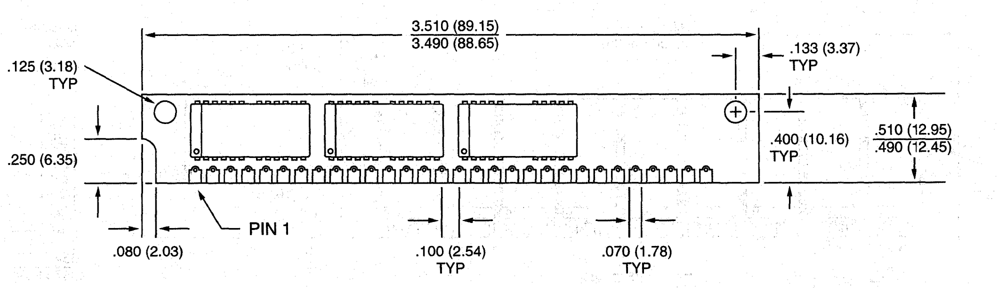
30-PIN SIMM

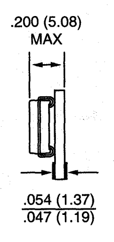
DD-1



30-PIN SIMM

DD-2





NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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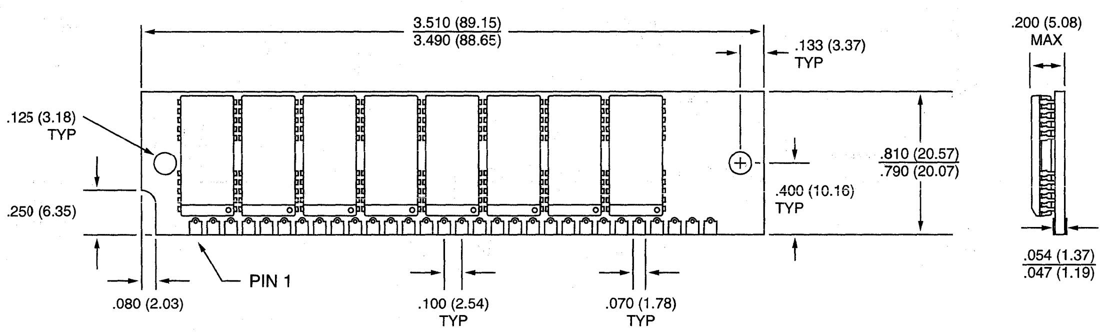
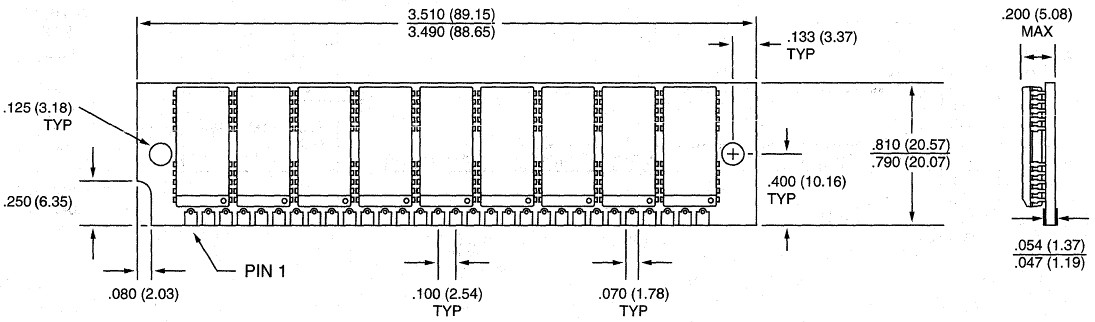
30-PIN SIMM
DD-3



30-PIN SIMM
DD-4



PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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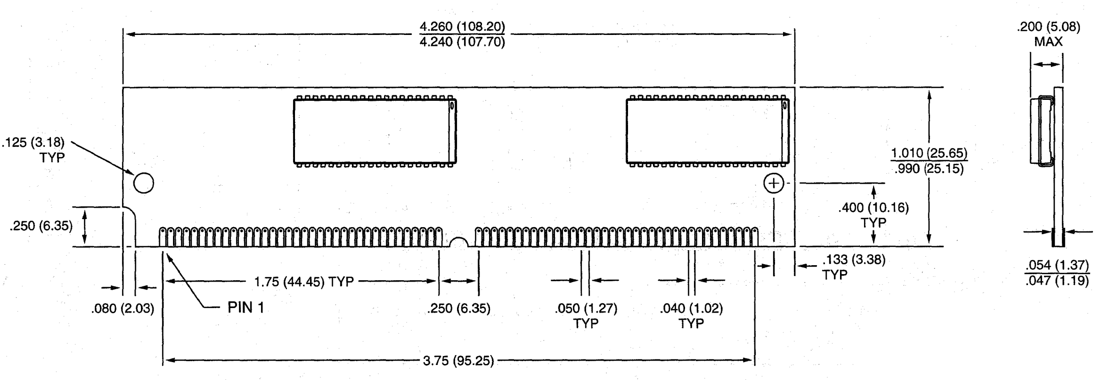
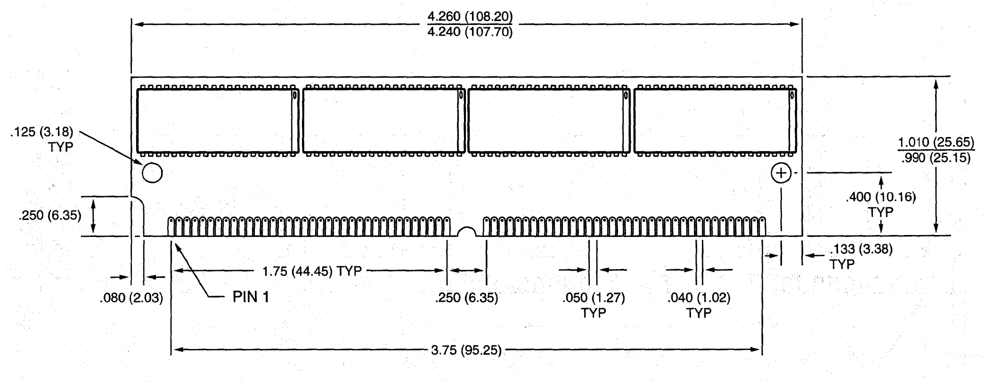
72-PIN SIMM

DD-5



72-PIN SIMM

DD-6



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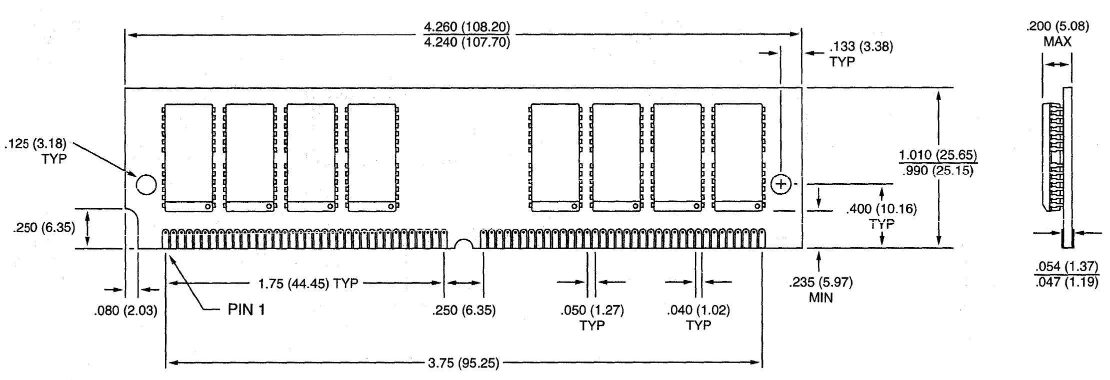
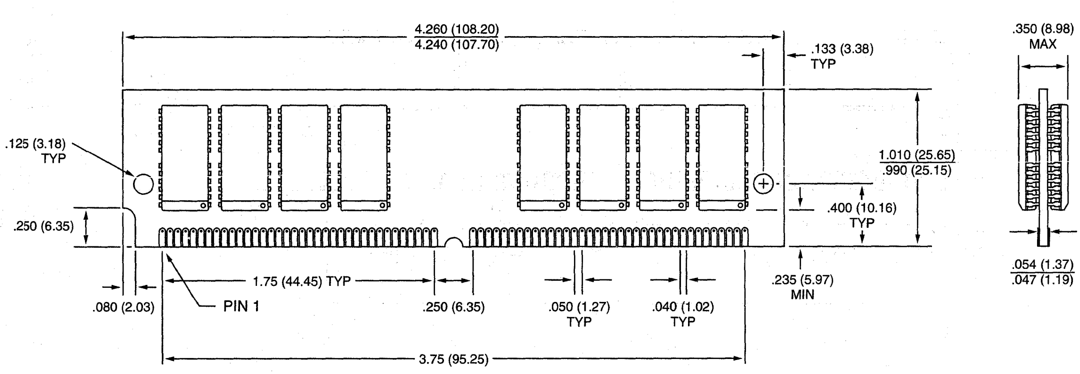
72-PIN SIMM
DD-7



72-PIN SIMM
DD-8



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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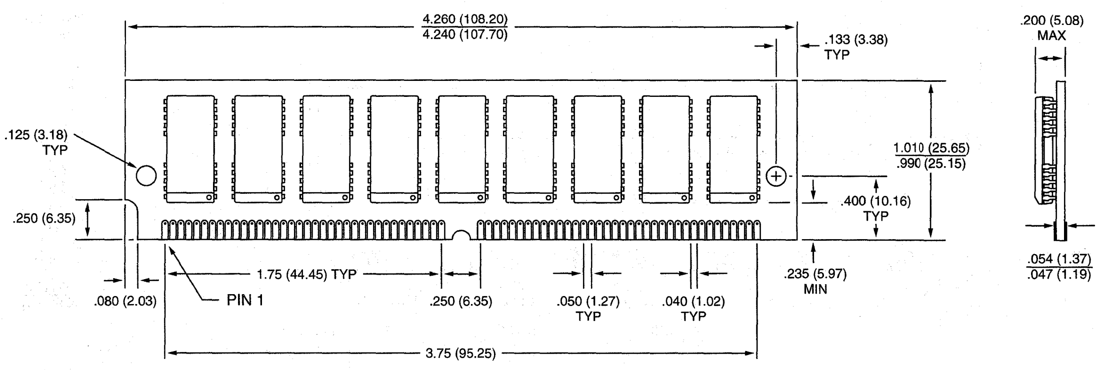
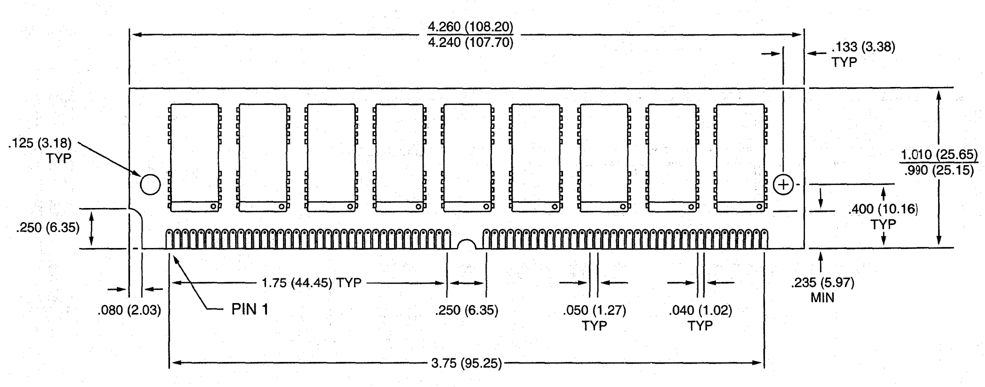
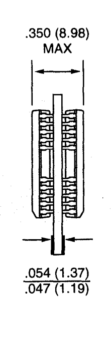
72-PIN SIMM
DD-9



72-PIN SIMM
DD-10





NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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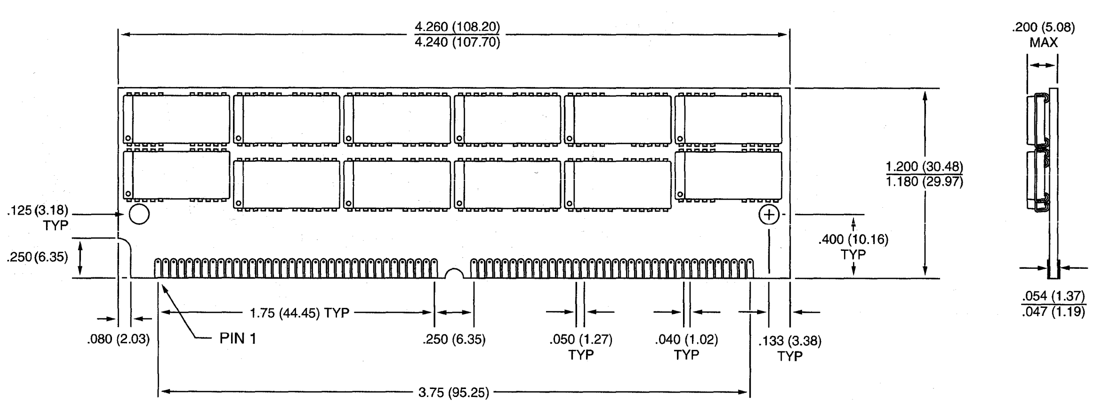
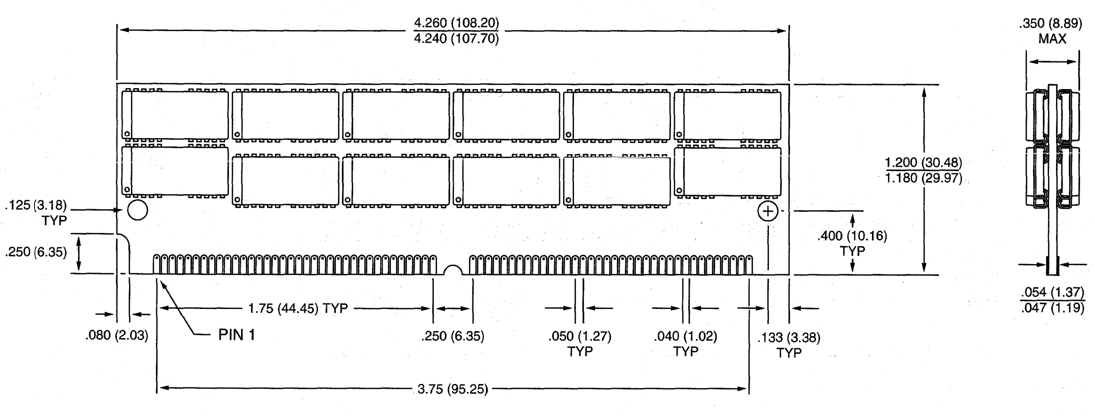
72-PIN SIMM
DD-11



72-PIN SIMM
DD-12



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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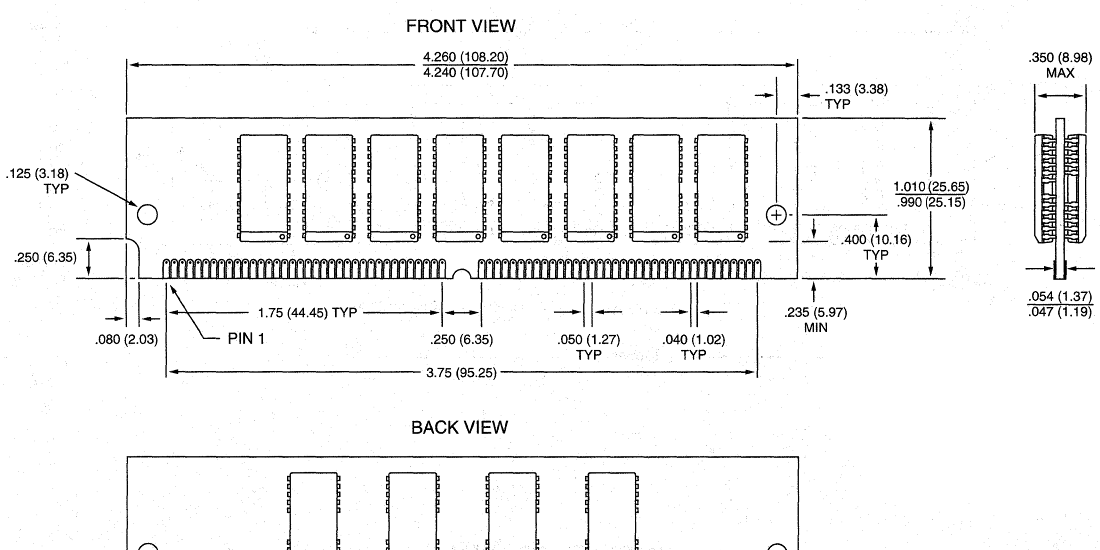
72-PIN SIMM
DD-13



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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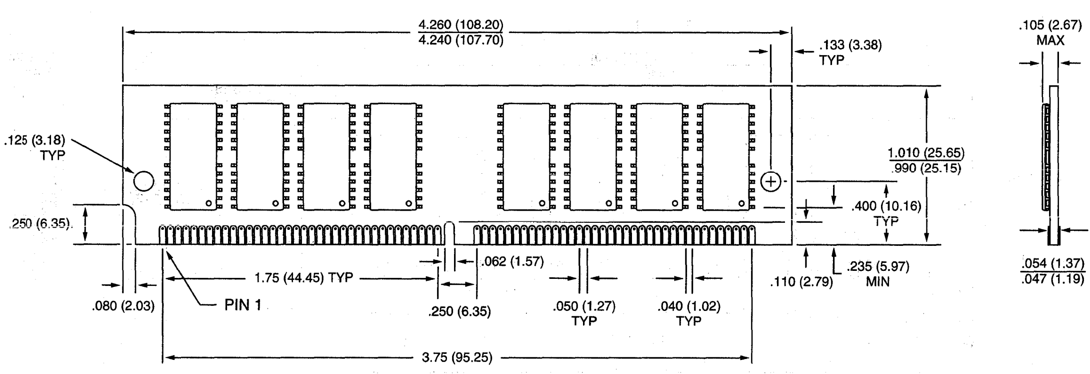
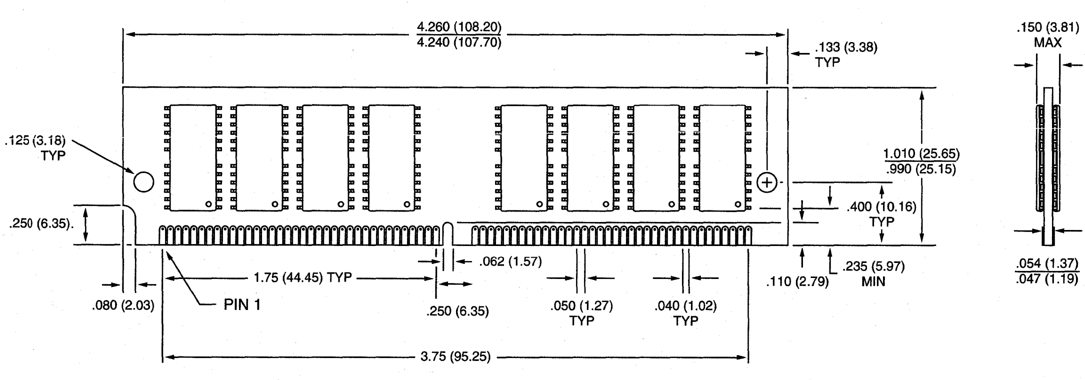
72-PIN TSOP SIMM
DD-14



72-PIN TSOP SIMM
DD-15



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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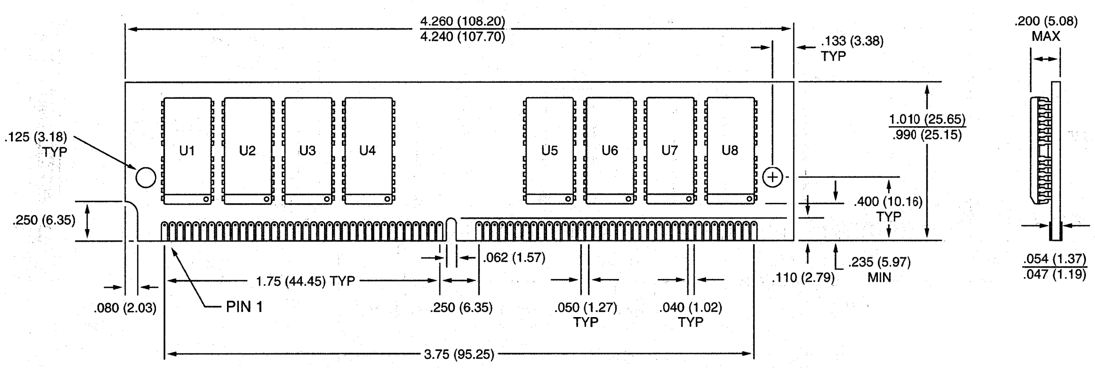
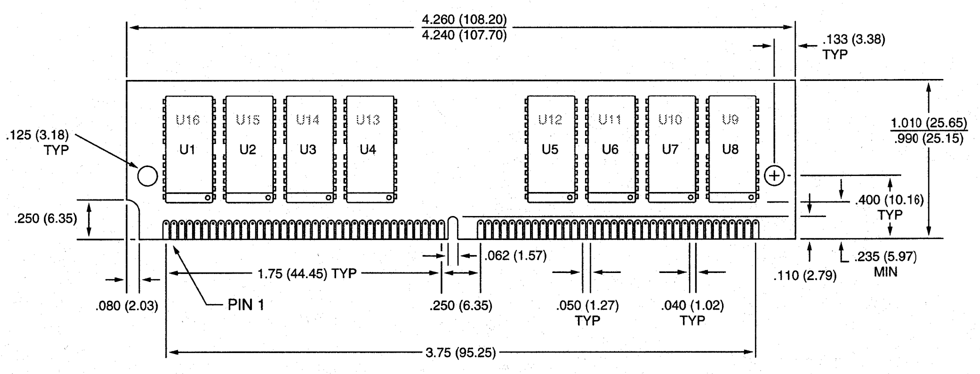
72-PIN SIMM
DD-16



72-PIN SIMM
DD-17



PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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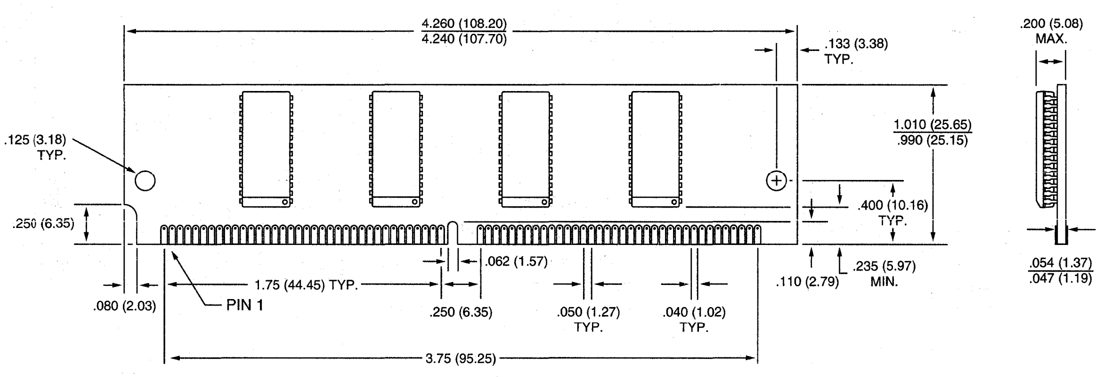
72-PIN SIMM
DD-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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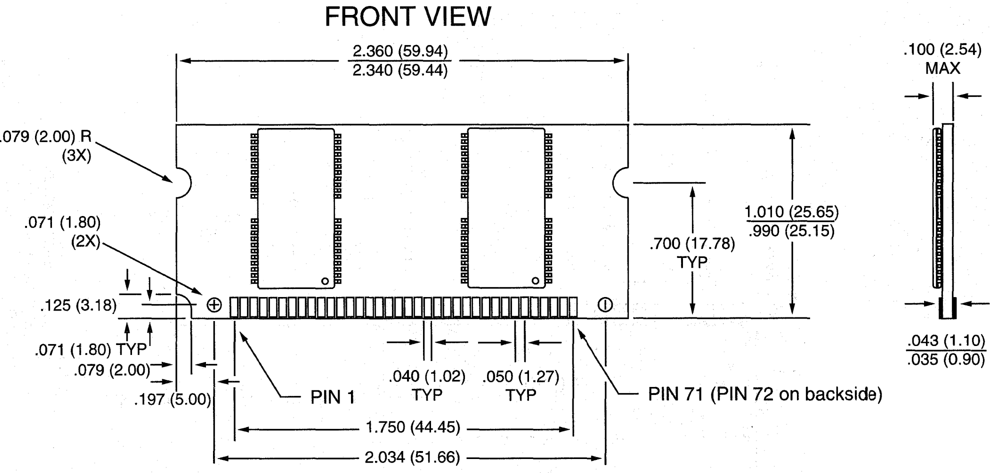
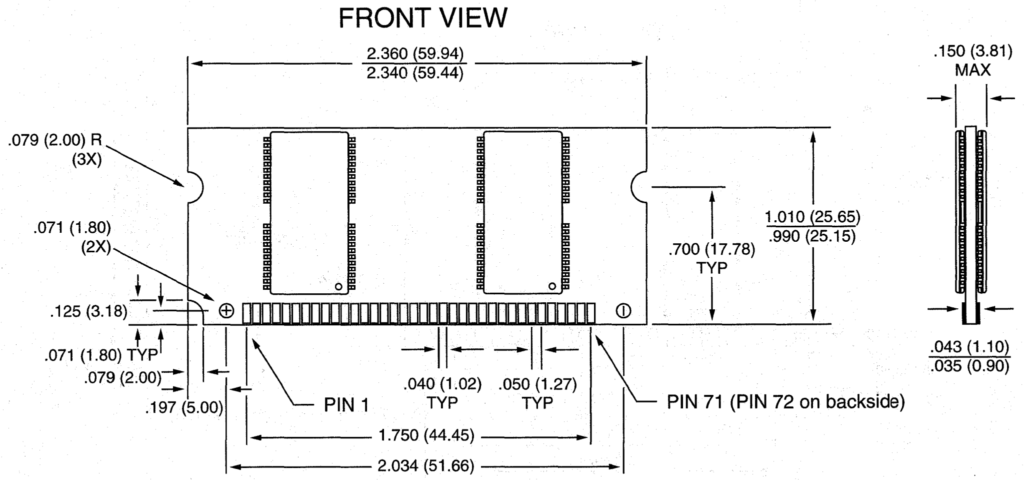
72-PIN TSOP DIMM
DE-1



72-PIN TSOP DIMM
DE-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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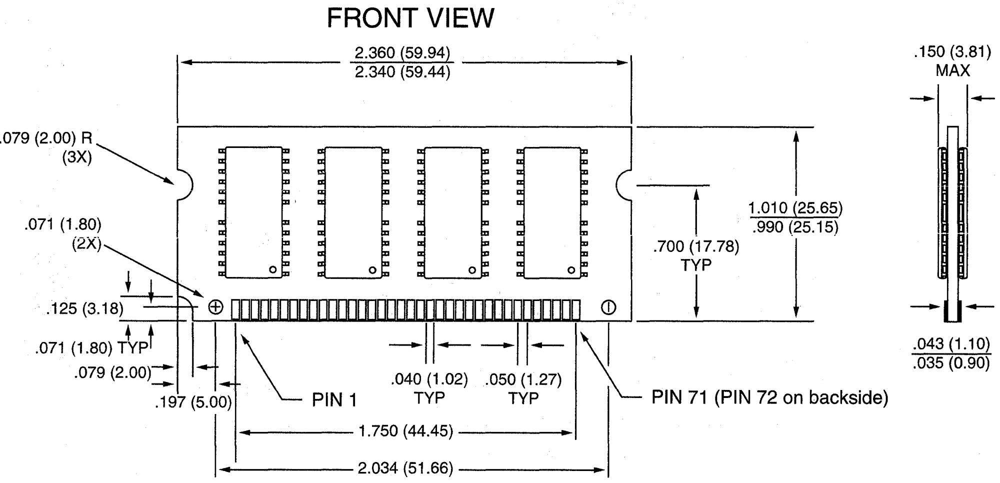
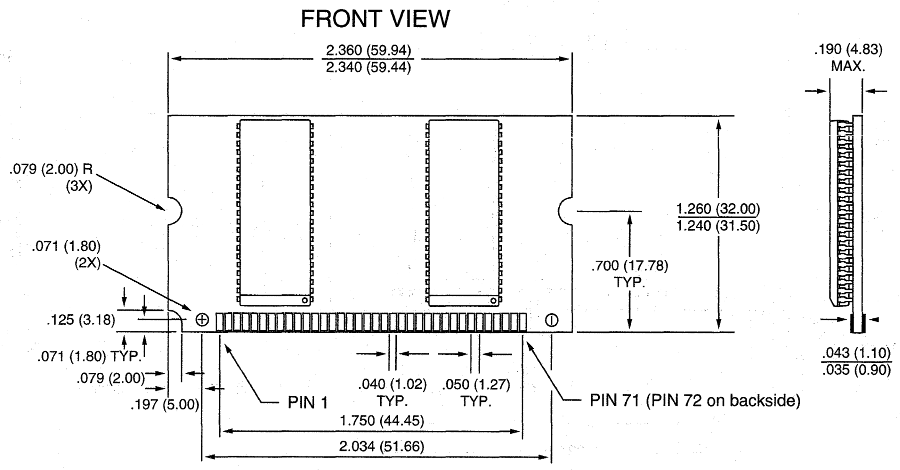
72-PIN TSOP DIMM

DE-3



72-PIN DIMM

DE-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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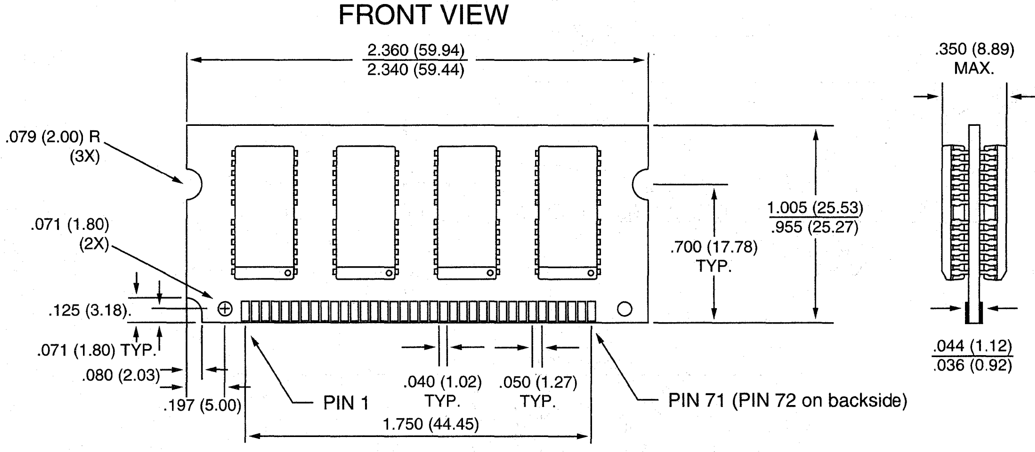
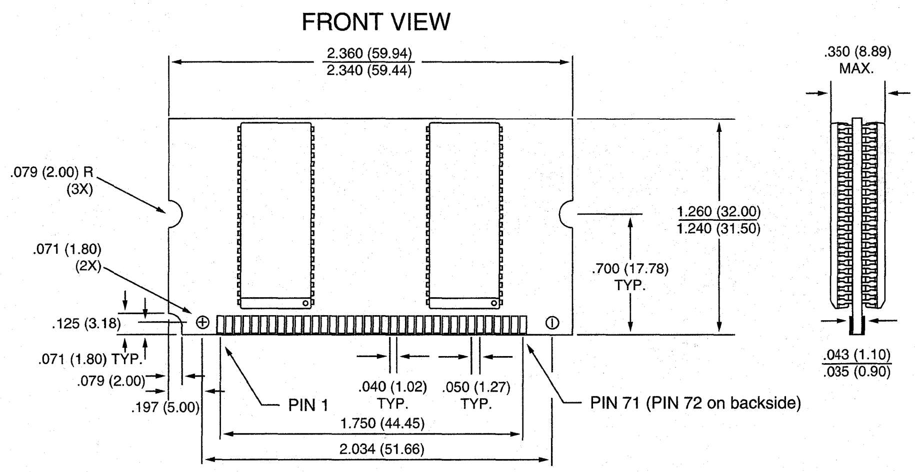
72-PIN DIMM
DE-5



72-PIN DIMM
DE-6



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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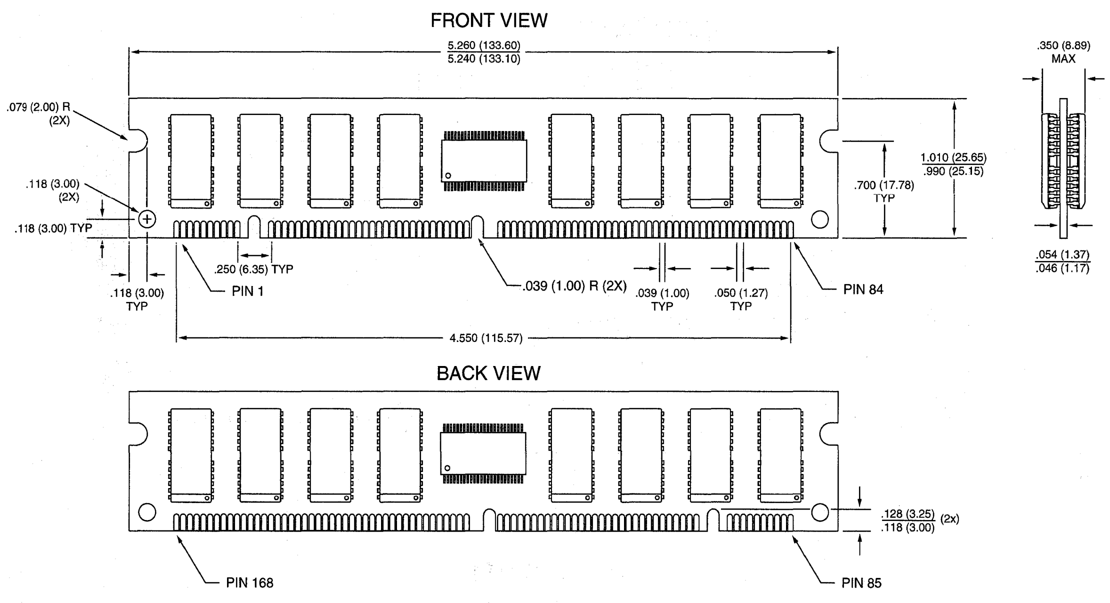
168-PIN DIMM

DE-7



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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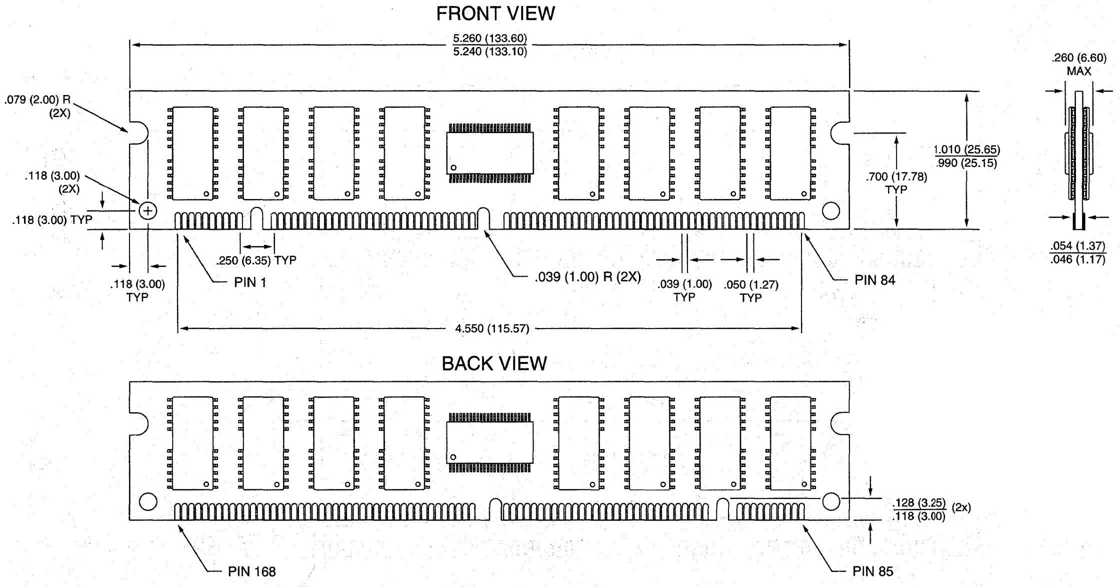
168-PIN TSOP DIMM

DE-8



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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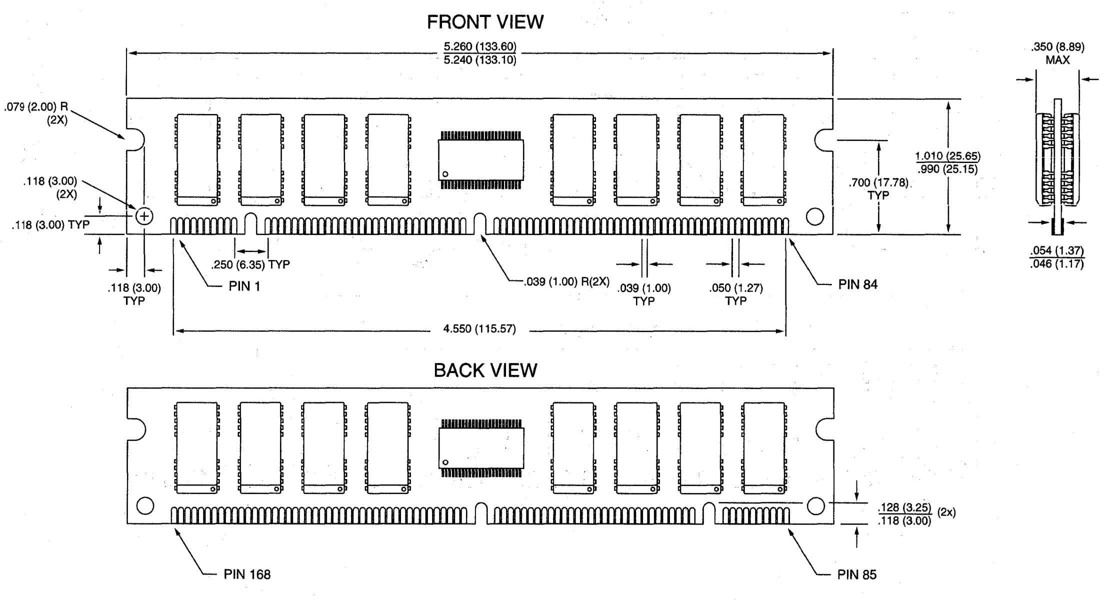
168-PIN DIMM

DE-9



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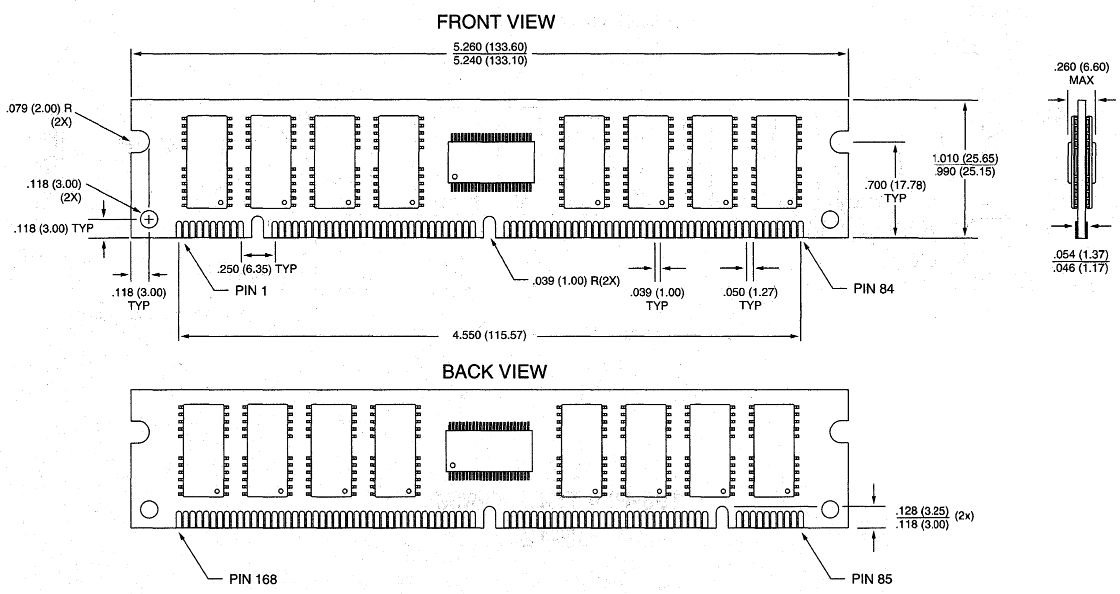
168-PIN TSOP DIMM
DE-10



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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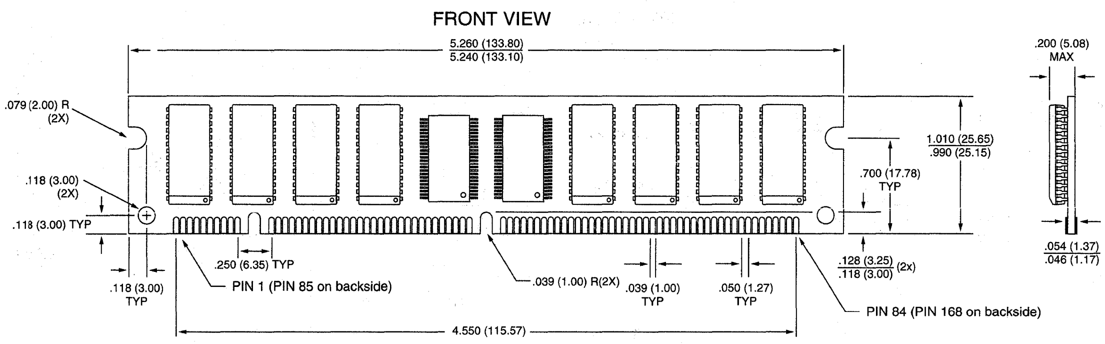
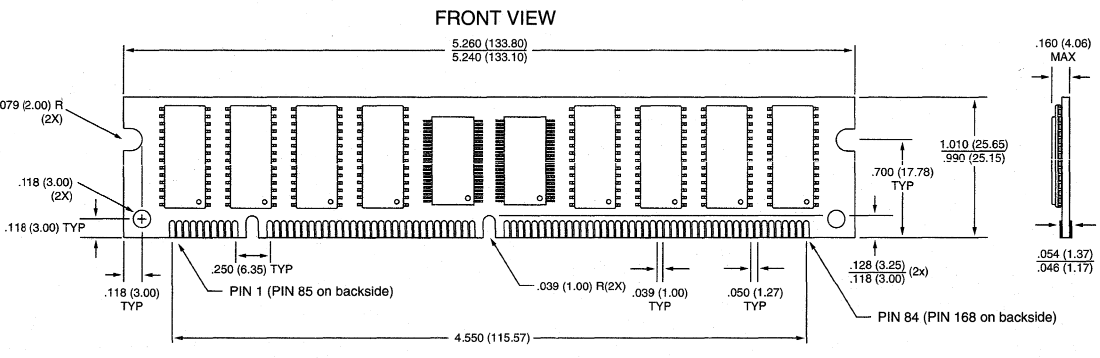
168-PIN DIMM
DE-11



168-PIN TSOP DIMM
DE-12



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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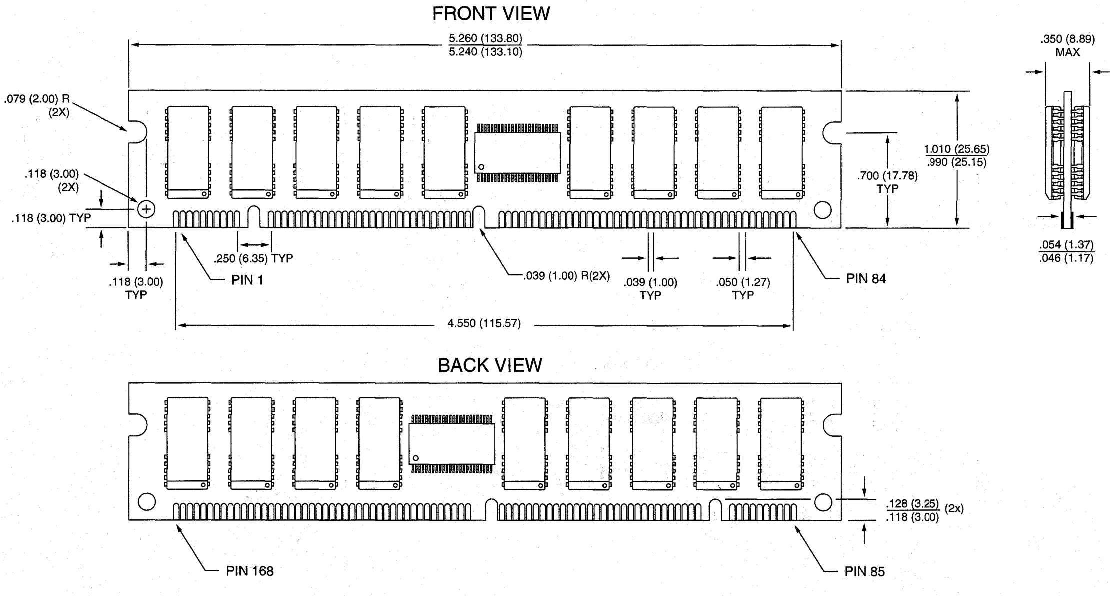
168-PIN DIMM

DE-13



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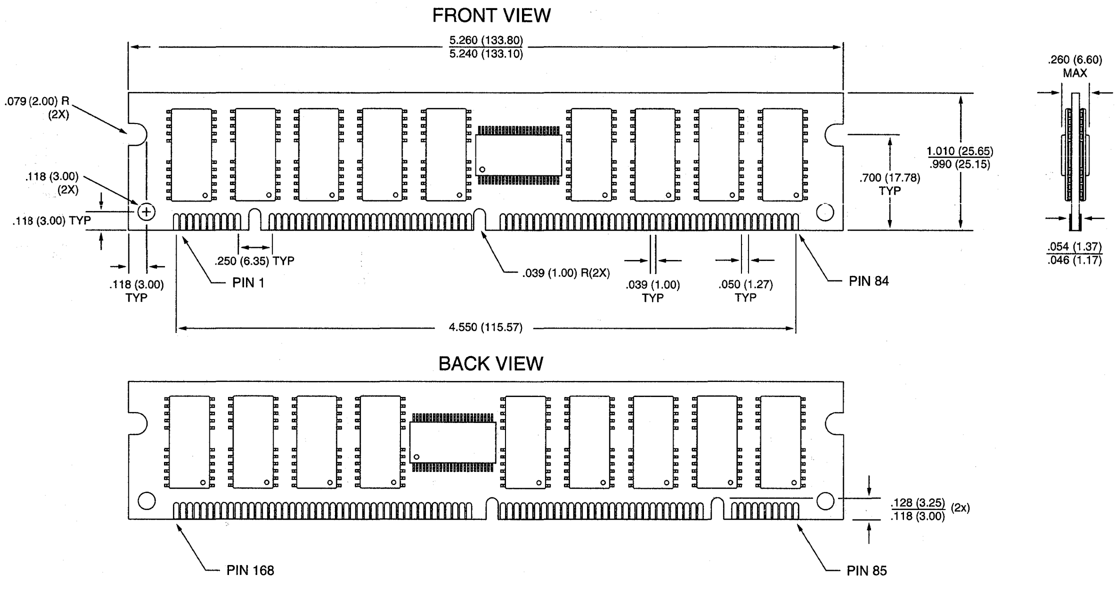
168-PIN TSOP DIMM

DE-14



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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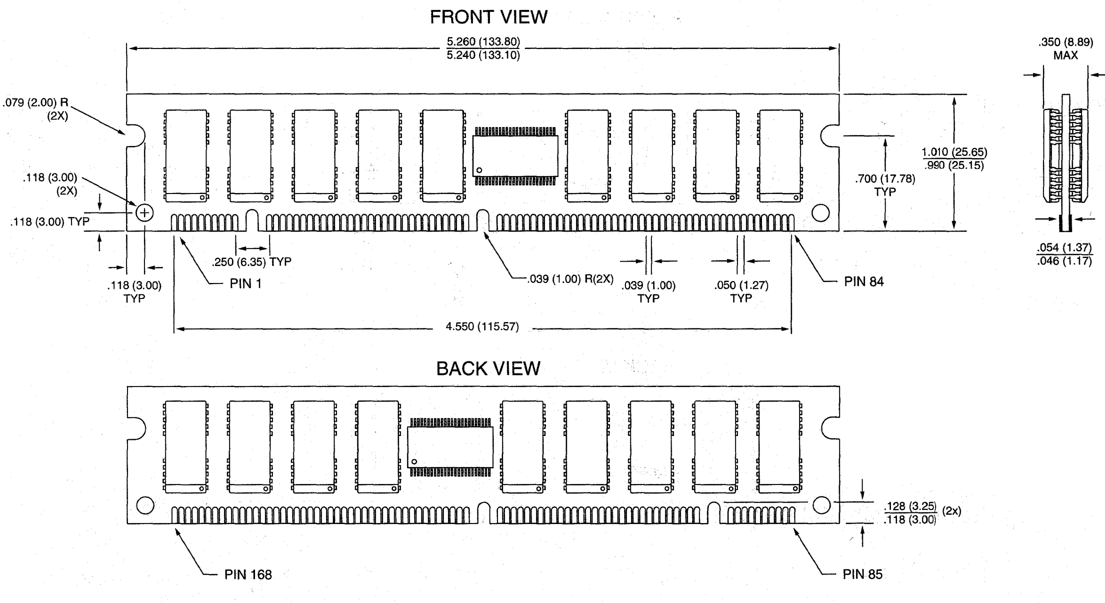
168-PIN DIMM

DE-15



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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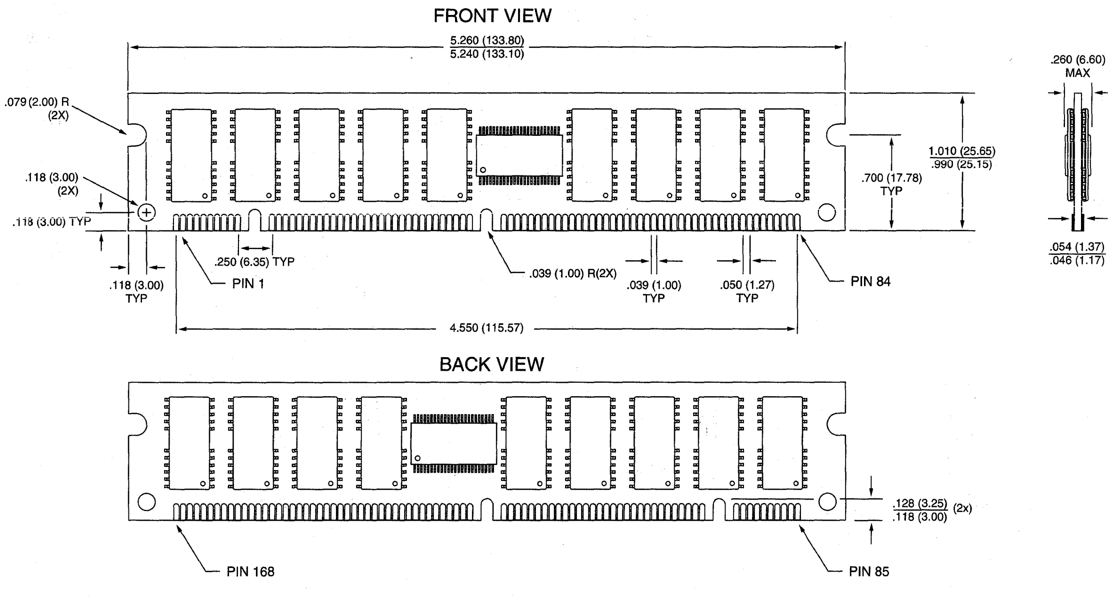
168-PIN TSOP DIMM

DE-16



PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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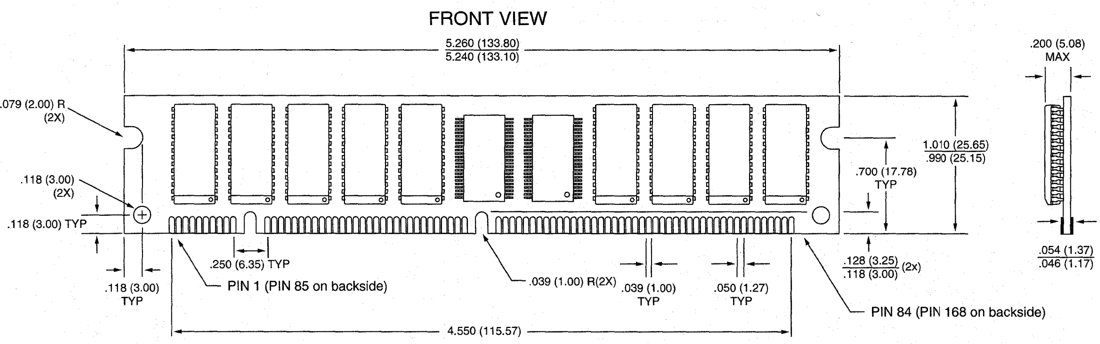
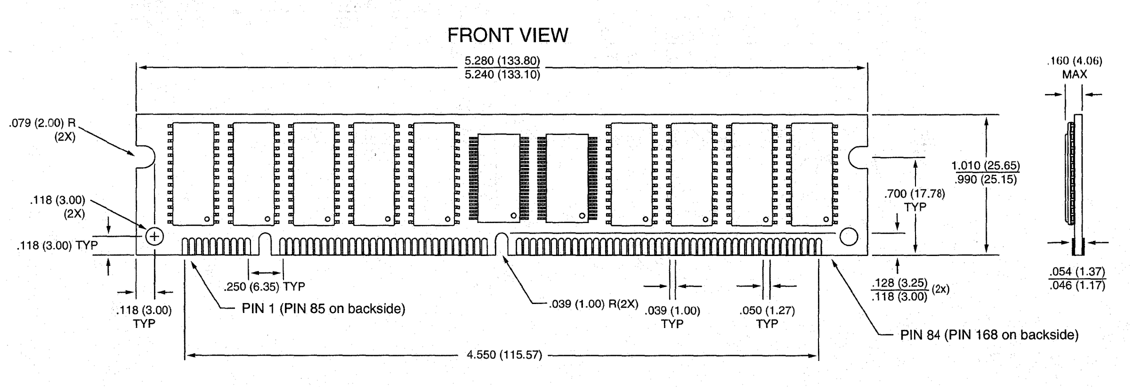
168-PIN DIMM

DE-17



168-PIN TSOP DIMM

DE-18



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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88-PIN DRAM CARD

DF-1

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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88-PIN REDUCED-LENGTH DRAM CARD

DF-2

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PACKAGE INFORMATION

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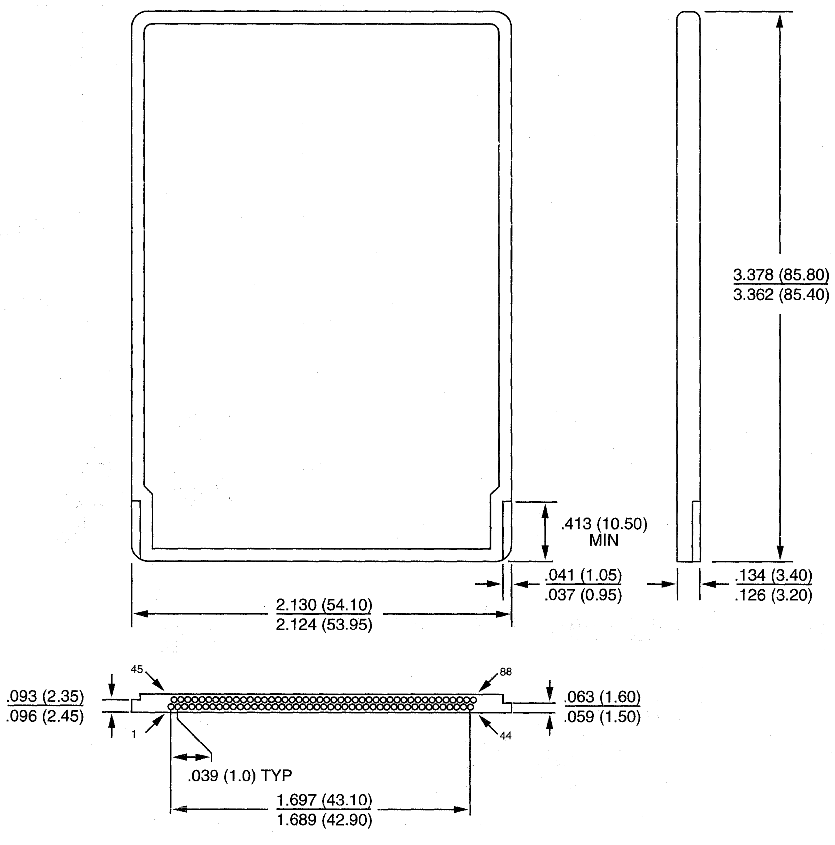
88-PIN DRAM CARD

DF-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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88-PIN REDUCED-LENGTH DRAM CARD

DF-4

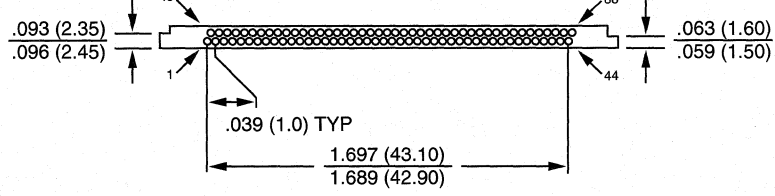
2.005 (50.93) / 1.995 (50.67)

.413 (10.50) MIN

.041 (1.05) / .037 (0.95)

2.130 (54.10) / 2.124 (53.95)

.134 (3.40) / .126 (3.20)



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MICRON TECHNOLOGY, INC.

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MICRON
TECHNOLOGY, INC.

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Micron Technology, Inc., has implemented standard bar code labels which accompany all shipments. These labels conform to EIA Standard 556.

The bar code labels allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar code label for master containers. Each individual box and/or container also has its own individual bar code label (see CSN-02).

BAR CODE INFORMATION

The information provided on the label is:

(4S) — Invoice/Packing Slip Number
(Q) — Quantity in master container
(Z) — Special: Reserved for individual customer requirements
(K) — Trans ID: Customer purchase order number
(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-To-Name: Customer's name and ship-to address
Ship-From-Name: Micron name and address
Master container package count
Package weight

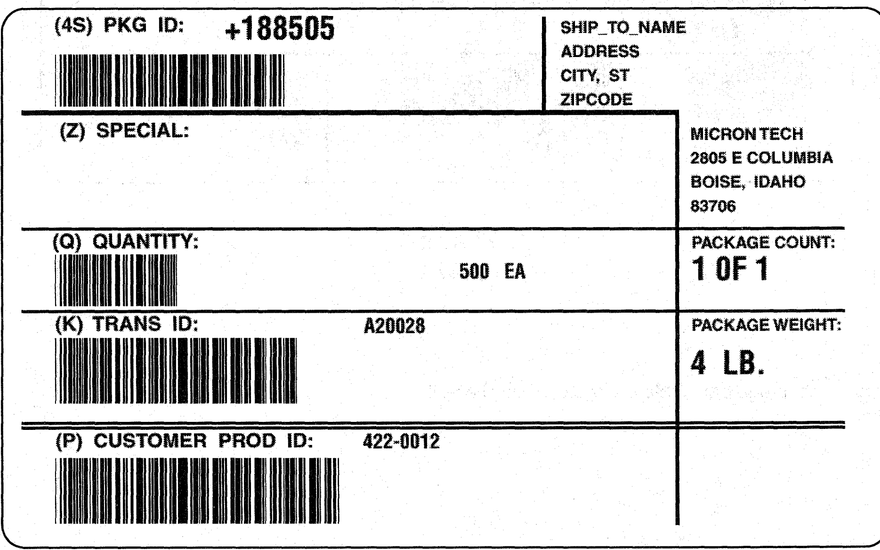

Figure 1
STANDARD BAR CODE LABEL

SALES AND SERVICE

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CUSTOMER SERVICE NOTE

INDIVIDUAL BOX AND CONTAINER BAR CODE LABELS

INTRODUCTION

Micron Technology, Inc., provides a standard bar code label on each individual box or container. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label used on individual boxes.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multibox shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*

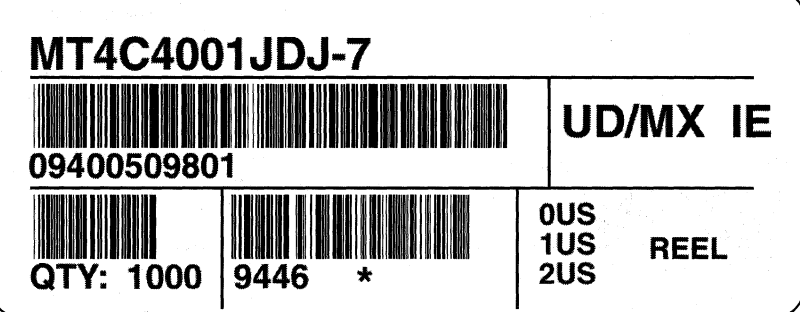

Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

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CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCT LABELING

INTRODUCTION

Micron Technology, Inc., provides a Humidity Indicator Card (HIC) with all surface-mount products.

Figure 1 shows an example of the standard HIC. Figure 2 shows approximate labeling of tape-and-reel packaged products.

HUMIDITY INDICATOR CARD (HIC)

The Humidity Indicator Card is hermetically sealed in drypack and provides an indication of the RH level of the contents.

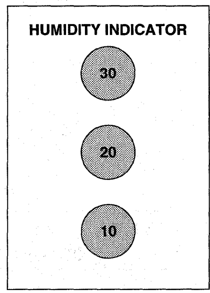

Figure 1
SURFACE-MOUNT PRODUCT HUMIDITY INDICATOR CARD

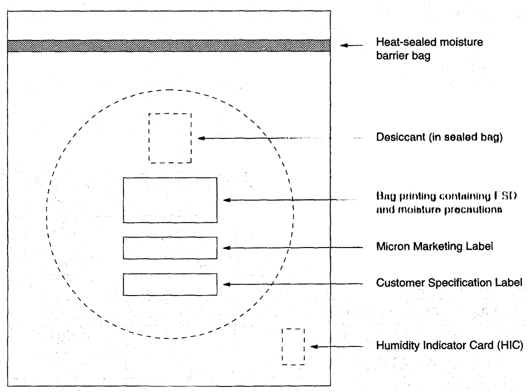

Figure 2
TAPE-AND-REEL PACKAGED PRODUCT LABEL

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CUSTOMER SERVICE NOTE

BOX AND TAPE-AND-REEL QUANTITY AND WEIGHT CHART

INTRODUCTION

Micron encourages customers to place orders in increments of standard box, tray and reel quantities whenever possible. The chart below will help determine order quantities.

ADDITIONAL SALES INFORMATION

Benefits to Micron's customers by ordering in standard quantities:

1. Cost Savings—it is less expensive to send a shipment containing full boxes.
2. Process Control—Micron's production tracking system automatically checks speeds, revs, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity—lot integrity is kept in tact when box quantities are not broken up.
4. Fewer returns—fewer errors equal fewer complaints and returns.

DRAM STANDARD BOX AND TAPE-AND-REEL CHART

PART TYPE	QUANTITY PER TRAY	QUANTITY PER BOX	LBS PER BOX	QUANTITY PER TUBE	TAPE-AND-REEL QUANTITY	LBS PER REEL	TAPE SIZE
DRAM - MEGS							
MT4C4M4B1-4LC4M4B1DJ	—	2000	—	25	500	—	—
MT4C1004JDJ-4C4001JDJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4C1004JTG-4C4001JTG	176	1000	8.0	—	1000	2.7	24mm x 12mm
MT4LC4001JDJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4LC4001JTG	176	1000	8.0	—	1000	2.7	24mm x 12mm
MT4C4004JDJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4C4007JDJ	—	4000	13.2	25	1000	4.1	24mm x 12mm
MT4LC4M4E8DJ	n/a	4000	13.2	25	1000	4.1	24mm x 12mm
MT4LC2M8B1DJ	n/a	4000	12.5	25	1000	3.9	24mm x 12mm
MT4LC2M8E7DJ	n/a	4000	12.5	25	1000	3.9	24mm x 12mm
MT4LC1M16C3TG	n/a	1000	10.0	n/a	500	3-4	44mm x 16mm
MT4LC1M16C3DJ	n/a	1500	12.0	15	500	4-5	44mm x 16mm
4 MEG SPECIALTY DRAMs							
MT4C16257DJ	—	1500	10.0	15	500	3.51	44mm x 16mm
MT4C16270DJ	—	1500	10.0	15	500	3.51	44mm x 16mm
MT4C16257TG	135	1000	9.0	—	500	2.5	44mm x 16mm

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MODULE STANDARD BOX AND TAPE-AND-REEL CHART

PART TYPE	TUBE QUANTITY	BOX QUANTITY	LBS PER BOX
DRAM MODULES			
MT2D18M/N	5	400	11
MT2D2568M	5	400	11
MT3D19M/N	5	400	10
MT3D2569M/N	5	400	12
MT8D132M/G	4	200	12
MT8D25632M/G	4	200	13
MT8D48M	5	400	17
MT8D48N	4	300	11
MT9D49M	5	400	18
MT9D49N	4	300	15
MT10D140M/G	4	200	15
MT12D136M/G	4	200	15
MT16D232M/G	4	200	15
MT16D51232M/G	4	200	15
MT18D236M/G	4	200	15
MT20D51240G	4	200	15
MT20D240G	4	200	15
MT24D236M/G	4	200	20
MT8D432M/G	4	200	15
MT12D436M/G	4	200	15
MT12D436DM/G	4	200	15
MT16D832M/G	4	200	15
MT24D836M/G	4	200	15
MT4D51232M/G	4	200	12
MT16D164G	3	150	16
MT2D48M	5	400	12
MT3D49M	5	400	12
MT9D136M/G	4	200	12
MT12D136DM/DG	4	200	15
MT2D25632M/G	4	200	10
MT16LD(T)164G	3	150	16
MT8LD(T)264G	3	150	16
MT16LD(T)464G	3	150	16
MT18LD(T)172G	3	150	16
MT9LD(T)272G	3	150	16
MT18LD(T)472G	3	150	16

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CUSTOMER SERVICE NOTE

ENVIRONMENTAL PROGRAMS

INTRODUCTION

Micron Technology, Inc., takes a proactive approach to environmental protection and worker safety. We believe that this is not only environmentally responsible, but gives the company a long-term competitive advantage. Environmental protection programs include educating the workforce about chemical hazards, reduction in toxic chemical usage and air pollutants, recycling, and treating waste water.

CHEMICAL AWARENESS AND MONITORING

Micron educates and involves its workforce in eliminating hazardous and polluting chemicals and conditions. Micron currently has several programs in place which enable the company to minimize hazardous chemical use while maintaining flexibility in processes and operations. Examples of these programs include:

ENVIRONMENTAL TASK FORCE

This internal task force meets weekly to review the effects of process changes, new construction, and new equipment on the environment and on worker safety. The group also reviews regulations and compliance issues, and anticipates possible impacts of potential regulation changes from legislation.

CHEMICAL APPROVAL SYSTEM

This approval and monitoring system insures that Micron remains in compliance with OSHA and EPA reporting requirements and tracks chemicals in use. Acting as a guidance and training resource, the Chemical Approval Team gives direction and alternatives, rather than policing, chemical use. This cooperative method of identifying hazardous chemicals, waste treatment needs and costs, and safety procedures has proven very effective.

TOXIC CHEMICAL REDUCTION PROGRAM

This is an active program for continuous reduction of EPA toxic chemicals and other chemicals determined to be of some risk to employees or the environment. Through this program, in 1992 Micron eliminated the use of hazardous ethylene-based glycol ethers in manufacturing and replaced anhydrous ammonia in storage tanks with a process that uses aqueous calcium hydroxide. Micron also eliminated ozone-depleting chemicals from the manufacturing process in 1992.

REDUCTION OF AIR POLLUTANTS

Micron has an ongoing program to reduce toxic air pollutant emissions and is evaluating several different types of pollution abatement methods for air emissions. Micron has successfully reduced toxic air pollutant emissions and fugitive volatile organic compound (VOC) emmisions by 90 percent. Reductions were made in the use of acetone, toluene, methanol, and isopropyl alcohol. Use of methyl ethyl ketone was completely eliminated.

The company successfully replaced its solvent-based cleanroom cleaner with a water-based solution. Because cleaning procedures were changed and existing wipes were replaced with more absorbent ones, the water-based cleaner proved to be more effective than the solvent-based cleaner and has greatly reduced fugitive VOC emissions.

In converting from "puddle primers" to vapor primer ovens in our photo process, Micron has reduced HMDS usage by 90 percent. Micron has also installed high-efficiency purge pumps which exceed EPA specifications on refrigeration units in order to eliminate the discharge of refrigerants into the atmosphere. In addition, portable refrigerant reclaim units are used to recover and recycle refrigerants during maintenance or when equipment is retired.

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WASTE WATER TREATMENT

Micron has completed the first phase of a three-phase industrial waste water treatment facility. The system was designed to remove fluoride from used process water and allow the water to be reclaimed. By 1997 Micron will reclaim all of its waste water and reduce ground water use by 80 percent. Micron recently won a Water Conservation Award from the Pacific Northwest Section of the American Water Works Association for this project.

RECYCLING AND ENERGY CONSERVATION

Several Micron teams have developed systems to recycle items for sale to outside customers or reuse within the manufacturing process. These items include sulfuric acid, gold, various solvents and alcohols, scrap metal, wire, aluminum and steel cans, buckets and barrels, pallets, plastic, and cardboard and paper products.

In 1987 Micron engineers developed an alternate cooling system, the Wet Side Economizer, which saves the company approximately $150,000 annually. The Wet Side Economizer uses cold air rather than refrigeration to cool the manufacturing complex. The system reduces kWh consumption by 15.1 million, which translates into a 11,174-ton reduction in CO_2 emissions, a 121-ton reduction in SO_2 emissions, and a 53-ton cut in NOx emissions. The system earned Micron a Certificate of Recognition for Energy Consciousness from the state of Idaho and an award for Energy Innovation from the U. S. Department of Energy in 1991.

Micron is continually working toward reducing emissions through recycling of solvents. We work with suppliers and internally to incorporate chemical recycling systems into processes. Micron is currently redistilling acetone and isopropyl alcohol on-site to repurify for reuse in the fab. We are also reviewing methods to recycle resist edge remover and organic strip.

COMMUNITY ASSISTANCE

Micron volunteers lab resources and provides consultation to local companies and community organizations, such as the Peregrine Fund, to help resolve industrial hygiene and environmental issues. Micron team members are active in local environmental and safety organizations and in the Community Emergency Planning Committee. Team members periodically host training classes (such as Hazardous Gas Bottle Handling and Disposal) for local professional organizations. Micron is also a member of the Idaho Association of Commerce and Industry (IACI) and is very active in the environmental committee.

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CUSTOMER SERVICE NOTE

ELECTRONIC DATA INTERCHANGE

INTRODUCTION

Electronic Data Interchange (EDI) has become an important data transmission element in today's marketplace. Micron is ready to serve your EDI needs and encourages customer participation.

STANDARDS SUPPORTED

X.12

Micron supports versions 002000 through 003040 for all implemented transaction sets. The addition of new versions is an automated process which drives off of the standard diskettes available through Data Interchange Standards Association.

EDIFACT

Micron supports EDIFACT under the 90.1 EDIFICE guidelines (for the Purchase Order [PO], PO Acknowledgment, PO Change and PO Change Acknowledgment messages) and EDIFACT version 92.1 for all implemented messages.

TRANSACTION SETS

Inbound	Outbound
850 - PO	855 - PO Acknowledgment
860 - PO Change	865 - PO Change Acknowledgment
840 - Request For Quote (RFQ)	843 - Response to RFQ
830 - Forecast	856 - Advanced Ship Notice
846 - Inventory Inquiry/ Advice	810 - Invoice
867 - Product Transfer & Resale	832 - Price/Sales Catalog
844 - Product Transfer Account Adjustment (PTAA)	849 - Response to PTAA
997 - Functional Acknowledgment	
ORDERS - PO Message	ORDRSP - PO Response Message
ORDCHG - PO Change Request Message	INVOIC - Invoice Message
DELFOR - Delivery Schedule Message	DESADV - Despatch Advice Message

VALUE ADDED NETWORKS

AT&T

AT&T allows our partners to transmit EDI documents via standard protocol or X.400 (e-mail protocol).

Advantis

Advantis is the result of a merger between the Sears and IBM networks.

TRANSMISSION TIMES

Transmission times are 2 a.m., 10 a.m., 1 p.m., 3 p.m. and 8 p.m. MST weekdays and 1 p.m. MST on weekends. Additional transmission times can be added easily as circumstances warrant.

MICRON EDI CONTACTS

EDI Project Leader	EDI Software Development
Becka Shirrod	Tony Holden
208-368-3338	208-368-3855

STEPS TO IMPLEMENTATION

The following are typical steps taken as Micron begins exchanging EDI data with a new trading partner:

- Micron receives an implementation guide from a trading partner
- Micron's EDI team contacts the trading partner's EDI coordinator to set up a trading partnership and coordinate the transmission and receipt of test documents
- Micron receives a test EDI document from the partner's VAN and responds with the necessary acknowledgments
- Once both parties agree everything is working properly, parallel testing with EDI and paper documents begins
- Micron insures an EDI agreement has been signed and returned to the trading partner
- Paper documents are replaced with EDI documents (full production).

LEAD TIMES FOR FULL PRODUCTION

X.12	EDIFACT
One Month	Two Months

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CUSTOMER SERVICE NOTE

RETURNED MATERIAL AUTHORIZATION (RMA) PROCEDURES

HOW TO RETURN PRODUCT TO MICRON

- Obtain an RMA number (see "How to Obtain an RMA" below).
- Package product taking all antistatic precautions.
- Write RMA number on outside of box for proper routing.
- Ship package prepaid to:
  Micron Technology, Inc.
  Attn.: RMA Area
  2805 East Columbia Road
  P.O. Box 6
  Boise, ID 83706-0006
- If RMA is being shipped from outside of the United States, please note that Boise, Idaho, is a customs port city; reference Port City Code 2907.

HOW TO OBTAIN AN RMA

NONFAILURE-RELATED RETURNS:

- If you buy direct, contact your Micron sales representative at 208-368-3900.
- If you buy through a Micron sales representative, contact that sales representative.
- If you buy through Distribution, contact the distributor.

Provide the following information:

- Micron part number, including speed and package
- Reason for return
- One of the following: PO number, invoice number, or sales order number
- Preferred reimbursement method: replacement parts, credit only, or refund.

FAILURE-RELATED RETURNS AND/OR APPLICATION PROBLEMS:

- Contact Micron Application Engineering Department at 208-368-3950.

Provide the following information:

- Micron part number, including speed and package
- Type of failure
- Name of engineer who witnessed failure or requested failure analysis report
- One of the following: PO number, invoice number, or sales order number
- Preferred reimbursement method: replacement parts, credit only, or refund.

FAILURE ANALYSIS STANDARDS FOR RETURNED MATERIAL AUTHORIZATIONS:

- Upon receipt of an RMA for failure analysis, Micron's Quality Assurance Department will provide an initial response within 48 hours.
- Micron's Quality Assurance Department will issue a completed failure analysis report within three weeks of receiving an RMA.

MICRON ACCOUNTING PROCEDURES FOR RETURNED MATERIAL AUTHORIZATIONS

- Replacements: Replacement parts are shipped after receipt of the RMA parts. The credit memo will be applied directly to the replacement invoice, unless a tax is involved, in which case a credit memo will be sent out along with an additional billing invoice. A new invoice will be sent when the replacement amount is greater than the returned amount. If this is not compatible with your accounts payable procedures, please advise your sales representative upon RMA request.
- Credit: A credit memo is sent out for the amount of the return upon arrival of the RMA parts. This credit memo number should be referenced when sending in payment information if intended to be used.
- Refund: A check request is submitted to Micron Accounts Payable upon receipt of RMA parts. A refund check is sent upon completion of the check request approval process.

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CUSTOMER SERVICE NOTE

ISO 9001 CERTIFICATION

INTRODUCTION

Micron Technology, Inc., was certified to ISO 9001 in the United States and Europe on February 1, 1994, by KEMA Registered Quality, Inc. The certification is also recognized by EQNET, the European Network for Quality System Assessment and Certification. Through this network, our KEMA certification is recognized by: AENOR Spain, AFAQ France, AIB-Vincotte Belgium, BSI QA United Kingdom, CISQItaly, DS Denmark, ELOT Greece, IPQ Portugal, NCS Norway, NSAI Ireland, OQS Austria, SFS Finland, SIS Sweden and SQS Switzerland.

ISO 9001 CERTIFICATION DEFINED

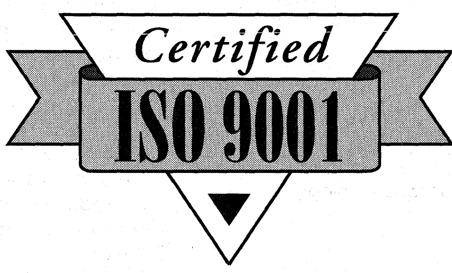
ISO 9001 is one of a series of three international standards dealing with quality systems that can be used for external quality assurance purposes. It is a model for quality assurance in design/development, manufacturing, testing, installation and servicing. It is the most comprehensive level of certification in the internationally recognized ISO 9000 family for quality assurance management systems.

ISO 9000 gives customers and suppliers a single set of guidelines that are accepted worldwide and that can be followed to achieve a definable level of quality. The certification implies that a company's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and should produce consistent results. A company seeking ISO certification must be certified as ISO 9001 if it has complete control over the design of its product with that control being a major factor in ensuring delivered quality.

A supplier's ability to conform to the ISO 9001 standard is assessed via the standard's Quality System Requirements—a set of twenty paragraphs each designed to address a specific portion of a quality system: management responsibility; quality system; contract review; design control; document control; purchasing; purchaser supplied product; product identification and traceability; process control; inspection and testing; inspection measuring and test equipment; inspection and test status; control of nonconforming product; corrective action; handling, storage, packaging and delivery; quality records; internal quality audits; training; servicing; and statistical techniques.

Micron's ISO 9001 certificate, number 93119, is valid until February 1, 1997, at which time Micron must again complete the audit cycle.

In February, 1995, a surveillence audit will be performed and Micron's certificate is expected to be renewed. At this point the certificate will reflect the company's name change (Micron Semiconductor, Inc. has become Micron Technology, Inc.).



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MEMBER OF THE EUROPEAN NETWORK FOR QUALITY SYSTEM ASSESSMENT AND CERTIFICATION "EQNET"

CERTIFICATE

Number: 93119

The quality system of:

MICRON SEMICONDUCTOR, INC.
BOISE, IDAHO

including the implementation meets the requirements of the standard:

ISO 9001

Scope:
Micron's semiconductor business, including the design, manufacturing, electrical and environmental testing and the marketing of semiconductor memory components.

Reports that form the basis of this certificate:
93119-KRQ-1 up to and including 93119-KRQ-3

This certificate is valid until: February 1, 1997

Issued for the first time: February 1, 1994

dr.ir. J.H. Blom
managing director

The method of operation for quality certification is defined in the KEMA Regulations for Quality System Certification.
Integral publication of this certificate and adjoining reports is allowed.

N.V. KEMA
Utrechtseweg 310, Arnhem, Postbus 9035, 6800 ET ARNHEM
Telephone +31 85 56 34 98 Telefax +31 85 45 88 25

ACCEPTED BY THE
DUTCH COUNCIL FOR
CERTIFICATION

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CUSTOMER SERVICE NOTE

MICRON DATAFAX

INTRODUCTION

Micron Technology, Inc., gives customers and potential customers instant access to technical and sales information via Micron DataFax[SM], a user-friendly, fax-on-demand system.

Micron DataFax allows callers to make automated requests for data sheets, product literature and other product information during and after regular business hours. Micron DataFax improves customer support by offering product information 24-hours-a-day, and shortens the sales and design-in cycle by offering engineers the most up-to-date product information.

HOW IT WORKS

Micron DataFax makes ordering product information quick and easy using the touchtone keypad on your fax machine. Here's how it works:

1. From your fax machine, call 208-368-5800.
2. Press 1 to order. When requested, enter document number(s).*
3. The documents you ordered will be sent to the fax machine you called from.

*An index of the documents available from Micron DataFax can be found in the last section of this book. This index is also available through the system itself and is updated periodically. Follow the voice instructions to receive the latest revision of the index.

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CUSTOMER SERVICE NOTE

CUSTOMER COMMENT LINE

INTRODUCTION

Micron Technology, Inc., is committed to achieving the highest standard in customer satisfaction, and we believe that giving our customers the opportunity to voice comments and complaints will help us discover ways to better serve them. To achieve continuous improvement, we need ongoing constructive customer feedback so we know exactly what our customers expect and need.

COMMENT LINE INFORMATION

Micron's Comment Line is answered by Customer Service personnel from 8:00 a.m. to 5:00 p.m. MST weekdays and is transferred to voice mail during off hours, weekends, and holidays. You may also fax your comments to us at any time. Whether you have experienced a recent transaction with Micron that requires immediate assistance, you want to provide feedback, or need information on local representatives in your area, please call or fax. Direct your inquiry to a customer satisfaction representative. We value your input!

STANDARDS

At Micron, we are dedicated to serving our customers and have set a 24-hour standard of returning all calls received on the Customer Comment Line. If we can't solve the matter at the time of your call, we will respond with an update to your question or concern within 24 hours.

Customer Comment Line:
U.S.A. 800-932-4992
Intl. 01-208-368-3410
Fax 208-368-3342

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CUSTOMER SERVICE NOTE

PART MARKING

INTRODUCTION

Micron Technology, Inc., utilizes a standard part marking on each product as shown in Figure 1 below. The only exceptions to this marking are for 32-lead and 52-lead EJ products on which the pin one designator is assigned a different location (see Figure 2).

PART MARKING INFORMATION

The part marking is right and left justified, and the character size is a minimum of .035/maximum of .045 inches high. Each part marking contains the following information: date code, revision letter (if relevant), country of origin (assembly), Micron logo, product family, process technology, device number, package type, pin one designator, speed and special test option (if relevant).

LASER SCRIBE IDENTIFICATION

Each part is also laser-scribed with a unique identification number. This identification number was previously located on the bottom side of the part only. We are currently adding the laser inscription to the top side as well.* The top-side inscription will allow for complete traceability of a component even after soldered onto a printed circuit board.

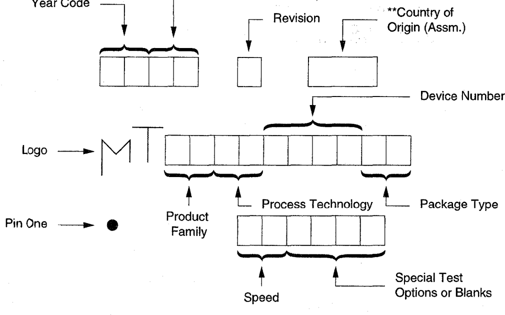

Figure 1
STANDARD PART MARKING

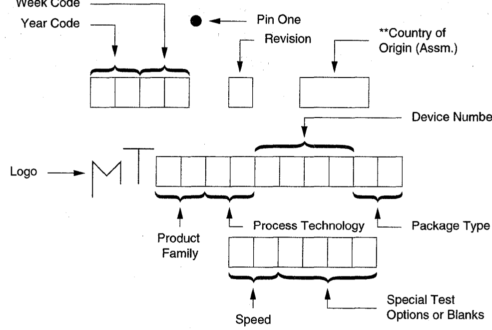

Figure 2
32-LEAD AND 52-LEAD EJ PRODUCTS PART MARKING

* Exceptions: A top-side laser inscription will not be added to the ZIP package. Off-shore assembled products will not be laser-scribed on the top side.

** May be blank if country of origin is printed on bottom of device.

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CUSTOMER SERVICE NOTE

PRODUCT CHANGE NOTIFICATION (PCN) SYSTEM

MICRON'S PCN SYSTEM

Micron's automated Product Change Notification (PCN) System provides notification to customers, per mutually agreed upon requirements, of Micron product or production changes affecting form, fit or function.

CHANGES REQUIRING NOTIFICATION

Product and production changes requiring customer notification include:

- bonding wire
- data sheet
- die coat
- die redesign
- die shrink
- geographic location
- internal connections
- lead frame
- mark change
- mark ink
- metalization
- mold compound
- package dimensions
- packaging
- passivation
- plating material
- plating process
- product obsolescence
- shipping tube
- wafer material

PCN LETTER DOCUMENTATION

PCN letters include the following information:

- PCN number
- a detailed description of the change
- a statement of the reason for the change
- supporting qualification data if appropriate
- a description of Micron product(s) affected by the change
- a list of each Micron part number (along with the corresponding customer number if available) purchased during the past 12 months or for which there is current backlog.

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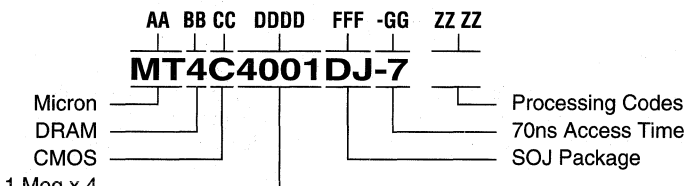
EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product .... MT

BB – PRODUCT FAMILY

DRAM 4
SRAM 5

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

DRAM .... Width, Density
TPDRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

JEDEC Test Mode (4 Meg DRAM) .... J
Errata on Base Part .... Q

FFF – PACKAGE CODES

PLASTIC

DIP .... Blank
DIP (Wide Body) .... W
ZIP .... Z
LCC .... EJ
SOP/SOIC .... SG
QFP .... LG
TSOP (Type I) .... VG
TSOP (Type I, Reversed) .... XG
TSOP (Type II) .... TG
TSOP (Reversed) .... RG
TSOP (Longer) .... TL
SOJ .... DJ
SOJ (Reversed) .... DR
SOJ (Longer) .... DL

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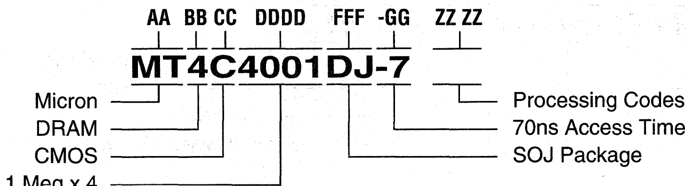
EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
EPI Wafer	E
Operating Temperature Range	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

*Used in device order codes; this code is not marked on device.

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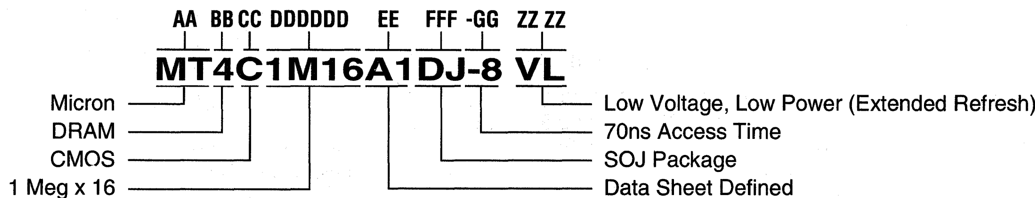
NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product .... MT

BB – PRODUCT FAMILY

Flash (Dual Supply) 28
DRAM 4
SGRAM 41
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS .... B
Low Voltage BiCMOS .... LB
Flash CMOS .... F
Low Voltage Flash CMOS .... LF
AP Flash CMOS .... AF

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits
Flash .... Density, Configuration

EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic
DIP .... Blank
DIP (Wide Body) .... W
ZIP .... Z
LCC .... EJ
SOP/SOIC .... SG
QFP .... LG
TSOP (Type II) .... TG
TSOP (Reversed) .... RG
TSOP (Longer) .... TL
SOJ .... DJ
SOJ (Wide) .... DW
SOJ (Reversed) .... DR
SOJ (Longer) .... DL

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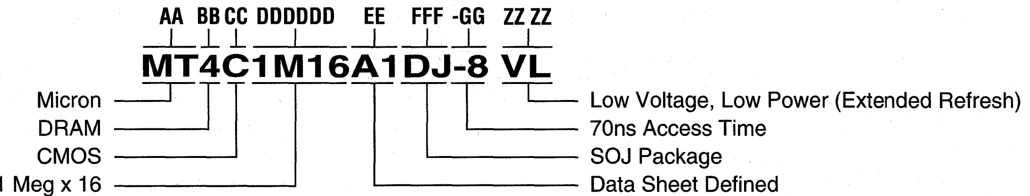
NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

Code	Access Time
-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

Description	Code
Interim	I
Low Voltage	V
DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
Flash	
3.3V Read (AP)	V
Bottom Boot Block	B
Top Boot Block	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

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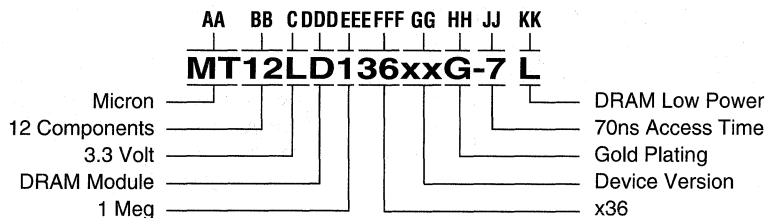
MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY
LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY
DRAM .... D
DRAM TSOP .... DT
SRAM .... S
SRAM TSOP .... ST
SYNCHRONOUS SRAM .... SY
SYNCHRONOUS SRAM TQFP .... SYT

EEE – DEPTH

FFF – WIDTH

GG – DEVICE VERSIONS
Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE
Gold Plated SIMM/DIMM .... G
ZIP .... Z
SIP .... N
SIMM/DIMM .... M
Small Outline DIMM .... H
Small Outline Gold DIMM .... HG
Double-Sided SIMM (1 or 4 Meg x 36 Only) .... DM
Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) .... DG

JJ – ACCESS TIME
-10 .... 10ns
-12 .... 12ns
-15 .... 15ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

KK – MODULE SPECIAL DESIGNATOR
SRAM
2V data retention L
Low Power .... P
Low Power, 2V data retention .... LP
DRAM
Low Power (Extended Refresh) L
ECC C
Extended Data Out X
Self Refresh .... S
16 Meg DRAM 4,096 Refresh .... A

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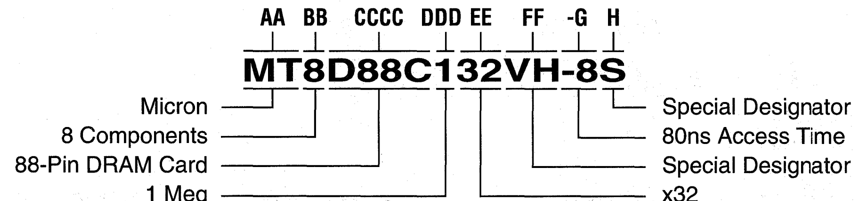
DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier
Micron Product .... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C

DDD – DEPTH

EE – WIDTH

FF – SPECIAL DESIGNATOR
3.3 Volts V
Reduced length (2") .... H

G – ACCESS TIME
-5 .... 50ns
-6 .... 60ns
-7 .... 70ns
-8 .... 80ns

H– SPECIAL DESIGNATOR
Self Refresh .... S

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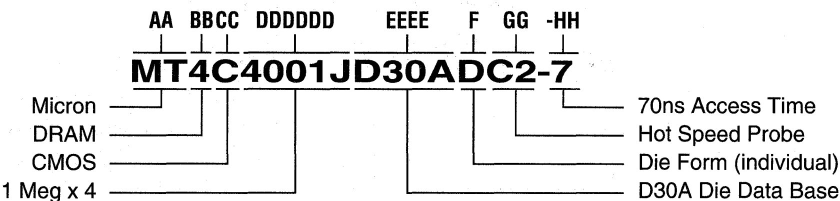
DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Component Product .... MT

BB – PRODUCT FAMILY
SRAM 5
DRAM 4
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY
CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER
When *no* alpha character appears as part of this section, the section is defined as:
DRAM .... Width, Density
SRAM .... Total Bits, Width
Synchronous SRAM .... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter .... Bits
K .... Kilobits
M .... Megabits
G .... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM
Die Form .... D
Wafer Form (6" Wafer) .... W

GG – TESTING LEVELS
Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3
KGD Plus® C7

HH – ACCESS TIME
(Applicable for C2 and C3 only)
-5 .... 5ns or 50ns
-6 .... 6ns or 60ns
-7 .... 7ns or 70ns
-8 .... 8ns or 80ns
-9 .... 9ns or 90ns
-10 .... 10ns or 100ns
-12 .... 12ns or 120ns
-15 .... 15ns or 150ns
-17 .... 17ns
-20 .... 20ns
-25 .... 25ns
-35 .... 35ns
-45 .... 45ns
-50 (SRAM only) 50ns
-SS (C2 only) .... speed sorted

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KGD Plus is a registered trademark of Micron Technology, Inc.

ORDER INFORMATION*

Each Micron component family is manufactured and quality controlled in the U.S.A. at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products meeting JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX intelligent burn-in and test system.

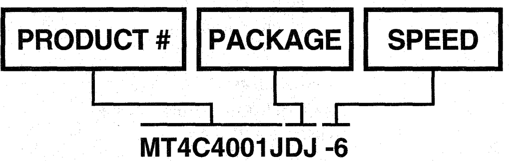
Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributor nearest you. Micron's policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

Telephone: 208-368-3900
Fax: 208-368-4431
Micron DataFax: 208-368-5802
Customer Comment Line:
U.S.A. 800-932-4992
Intl. 01-208-368-3410
Fax 208-368-3342

ORDER EXAMPLES

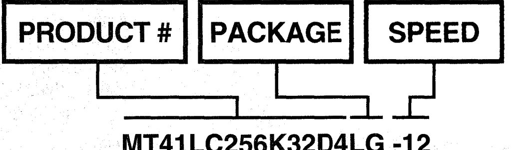
DRAM

1 Meg x 4, 60ns in Plastic SOJ



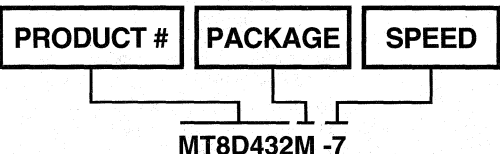
SGRAM

256K x 32, 12ns in Plastic QFP



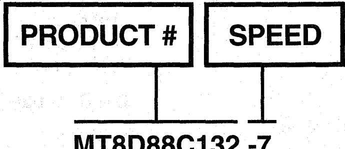
DRAM MODULE

4 Meg x 32, 70ns in SIMM Module



DRAM CARD

1 Meg x 32, 70ns DRAM Card



*For more detailed information, refer to the product numbering charts on pages 10-16 through 10-22.

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ALABAMA

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
Fax - 205-534-2384

Distributors

Anthem Electronics Incorporated
4920 H, Corporate Drive
Huntsville, AL 35805
Phone - 205-890-0302
Phone - 800-359-3531
Fax - 205-890-0130

Hamilton Hallmark
4890 University Square, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
Phone - 800-572-7236
Fax - 205-830-2565

Wyle Laboratories
Tower Building, 2nd Floor
7800 Governers Drive West
Huntsville, AL 35807
Phone - 205-830-1119
Fax - 205-830-1520

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARIZONA

Representative

Quatra Associates
4645 South Lakeshore Drive, Suite 1
Tempe, AZ 85282
Phone - 602-820-7050
Fax - 602-820-7054

Distributors

Anthem Electronics Incorporated
1555 10th Place, Suite 101
Tempe, AZ 85281
Phone - 602-966-6600
Fax - 602-966-4826

Hamilton Hallmark
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
Phone - 800-352-8489
Fax - 602-437-2348

Wyle Laboratories
4141 E. Raymond Street, Suite 1
Phoenix, AZ 85040
Phone - 602-437-2088
Fax - 602-437-2124

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARKANSAS

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-265-4600
Fax - 214-265-4668

Distributors

Anthem Electronics Incorporated
651 N. Plano Road, Suite 401
Richardson, TX 75081
Phone - 214-238-7100
Fax - 214-238-0237

Hamilton Hallmark
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214- 235-9953
Fax - 214-644-5064

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CALIFORNIA

Representatives (Northern California)

Bay Area Electronic Sales, Inc.
2001 Gateway Place, Suite 315 W
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Bay Area Electronic Sales, Inc.
9119 Eden Oak Circle
Loomis, CA 95650
Phone - 916-652-6777
Fax - 916-652-5678

Sales Offices (Southern California)

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Fax - 353-18-453625

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Fax - 81-3-3363-8486

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MICRON

DataFax℠

208-368-5800

Instructions for using Micron DataFax can be found in Customer Service Note, CSN-09, on page 10-12.

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EDO DRAMs

Part	Rev.	Organization	Description	Pages	Document Number
MT4C4007J	(Rev. 2/95)	1 Meg x 4	5V	15 pg	125
MT4C4007J S	(Rev. 2/95)	1 Meg x 4	5V, S	15 pg	125
MT4LC4007J	(Rev. 2/95)	1 Meg x 4	3.3V	17 pg	117
MT4LC4007J S	(Rev. 2/95)	1 Meg x 4	3.3V, S	17 pg	117
MT4LC4M4E8	(Rev. 2/95)	4 Meg x 4	3.3V, 2KR	18 pg	120
MT4LC4M4E8 S	(Rev. 2/95)	4 Meg x 4	3.3V, 2KR, S	18 pg	120
MT4LC16M4G3	(Rev. 2/95)	16 Meg x 4	3.3V, 8KR	16 pg	121
MT4LC16M4H9	(Rev. 2/95)	16 Meg x 4	3.3V, 4KR	16 pg	121
MT4LC2M8E7	(Rev. 2/95)	2 Meg x 8	3.3V, 2KR	16 pg	309
MT4LC2M8E7 S	(Rev. 2/95)	2 Meg x 8	3.3V, 2KR, S	16 pg	309
MT4LC8M8P4	(Rev. 2/95)	8 Meg x 8	3.3V, 8KR	15 pg	123
MT4LC8M8C2	(Rev. 2/95)	8 Meg x 8	3.3V, 4KR	15 pg	123
MT4C16270	(Rev. 2/95)	256K x 16	5V, DC	18 pg	305
MT4LC16270	(Rev. 2/95)	256K x 16	3.3V, DC	18 pg	310
MT4LC1M16E5	(Rev. 2/95)	1 Meg x 16	3.3V, DC, 1KR	21 pg	119
MT4LC1M16E5 S	(Rev. 2/95)	1 Meg x 16	3.3V, DC, 1KR, S	21 pg	119

DC .... Dual CAS
2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
5V .... 5 volt Vcc
1KR .... 1,024 Refresh
4KR .... 4,096 Refresh
S .... SELF REFRESH
3.3V .... 3.3 volt Vcc

FPM DRAMs

Part	Rev.	Organization	Description	Pages	Document Number
MT4C1004J	(Rev. 2/95)	4 Meg x 1	5V	16 pg	102
MT4C1004J S	(Rev. 2/95)	4 Meg x 1	5V, S	16 pg	102

DC .... Dual CAS
1KR .... 1,024 Refresh
4KR .... 4,096 Refresh
S .... SELF REFRESH
3.3V .... 3.3 volt Vcc
QC .... Quad CAS
2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
5V .... 5 volt Vcc

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FPM DRAMs (continued)

Part	Rev.	Organization	Features	Pages	DOCUMENT NUMBER
MT4C4001J	(Rev. 2/95)	1 Meg x 4	5V	16 pg	106
MT4C4001J S	(Rev. 2/95)	1 Meg x 4	5V, S	16 pg	106
MT4LC4001J	(Rev. 2/95)	1 Meg x 4	3.3V	14 pg	107
MT4LC4001J S	(Rev. 2/95)	1 Meg x 4	3.3V, S	14 pg	107
MT4C4004J	(Rev. 2/95)	1 Meg x 4	5V, QC	13 pg	118
MT4C4M4B1	(Rev. 2/95)	4 Meg x 4	5V, 2KR	14 pg	114
MT4LC4M4B1	(Rev. 2/95)	4 Meg x 4	3.3V, 2KR	16 pg	115
MT4LC4M4B1 S	(Rev. 2/95)	4 Meg x 4	3.3V, 2KR, S	16 pg	115
MT4LC16M4A7	(Rev. 2/95)	16 Meg x 4	3.3V, 8KR	13 pg	122
MT4LC16M4T8	(Rev. 2/95)	16 Meg x 4	3.3V, 4KR	13 pg	122
MT4LC2M8B1	(Rev. 2/95)	2 Meg x 8	3.3V, 2KR	16 pg	307
MT4LC2M8B1 S	(Rev. 2/95)	2 Meg x 8	3.3V, 2KR, S	16 pg	307
MT4LC8M8E1	(Rev. 2/95)	8 Meg x 8	3.3V, 8KR	13 pg	124
MT4LC8M8B6	(Rev. 2/95)	8 Meg x 8	3.3V, 4KR	13 pg	124
MT4C16257	(Rev. 2/95)	256K x 16	5V, DC	16 pg	302
MT4LC16257	(Rev. 2/95)	256K x 16	3.3V, DC	18 pg	311
MT4LC16257 S	(Rev. 2/95)	256K x 16	3.3V, DC, S	18 pg	311
MT4C1M16C3	(Rev. 2/95)	1 Meg x 16	5V, DC, 1KR	16 pg	312
MT4LC1M16C3	(Rev. 2/95)	1 Meg x 16	3.3V, DC, 1KR	17 pg	308
MT4LC1M16C3 S	(Rev. 2/95)	1 Meg x 16	3.3V, DC, 1KR, S	17 pg	308

DC .... Dual CAS
1KR .... 1,024 Refresh
4KR .... 4,096 Refresh
S .... SELF REFRESH
3.3V .... 3.3 volt Vcc
QC .... Quad CAS
2KR .... 2,048 Refresh
8KR .... 8,192 Refresh
5V .... 5 volt Vcc

SGRAM

Part	Rev.	Organization	Features	Pages	DOCUMENT NUMBER
MT41LC256K32D4	(Rev. 2/95)	256K x 32	3.3V	15 pg	2700*
MT41LC256K32D4 S	(Rev. 2/95)	256K x 32	3.3V, S	15 pg	2700*

S .... SELF REFRESH
3.3V .... 3.3 volt Vcc

DRAM DIE

Part	Rev.	Density	Features	Pages	DOCUMENT NUMBER
D22A	(Rev. 7/94)	4 Meg	x1, x4	4 pg	2401
D18A	(Rev. 9/94)	4 Meg	x8, x16	4 pg	2400
D21A	(Rev. 7/94)	16 Meg	x4	4 pg	2402
D24A	(Rev. 7/94)	16 Meg	x4, x8, x16	4 pg	2403

DRAM SIMMs

Part	Rev.	Organization	Features	Pages	DOCUMENT NUMBER
MT2D18	(Rev. 2/95)	1 Meg x 8	5V	11 pg	400
MT2D48	(Rev. 2/95)	4 Meg x 8	5V	11 pg	402
MT8D48	(Rev. 2/95)	4 Meg x 8	5V	11 pg	403
MT3D49	(Rev. 2/95)	4 Meg x 9	5V	11 pg	406
MT9D49	(Rev. 2/95)	4 Meg x 9	5V	11 pg	407
MT2D25632	(Rev. 2/95)	256K x 32	5V	13 pg	433
MT4D51232	(Rev. 2/95)	512K x 32	5V	13 pg	433
MT8D132	(Rev. 2/95)	1 Meg x 32	5V	16 pg	447
MT8D132 S	(Rev. 2/95)	1 Meg x 32	5V, S	16 pg	447

S .... SELF REFRESH
5V .... 5 volt Vcc
EDO .... Extended Data-Out
3.3V .... 3.3 volt Vcc

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DRAM SIMMs (continued)

Part	Rev.	Configuration	Description	Pages	DOCUMENT NUMBER
MT8LD(T)132	(Rev. 2/95)	1 Meg x 32	3.3V	24 pg	441
MT8LD(T)132 S	(Rev. 2/95)	1 Meg x 32	3.3V, S	24 pg	441
MT8LD(T)132 X	(Rev. 2/95)	1 Meg x 32	3.3V, EDO	24 pg	441
MT8LD(T)132 XS	(Rev. 2/95)	1 Meg x 32	3.3V, EDO, S	24 pg	441
MT16D232	(Rev. 2/95)	2 Meg x 32	5V	16 pg	447
MT16D232 S	(Rev. 2/95)	2 Meg x 32	5V, S	16 pg	447
MT16LD(T)232	(Rev. 2/95)	2 Meg x 32	3.3V	24 pg	441
MT16LD(T)232 S	(Rev. 2/95)	2 Meg x 32	3.3V, S	24 pg	441
MT16LD(T)232 X	(Rev. 2/95)	2 Meg x 32	3.3V, EDO	24 pg	441
MT16LD(T)232 XS	(Rev. 2/95)	2 Meg x 32	3.3V, EDO, S	24 pg	441
MT4LD232	(Rev. 2/95)	2 Meg x 32	3.3V	21 pg	442
MT4LD232 S	(Rev. 2/95)	2 Meg x 32	3.3V, S	21 pg	442
MT4LD232 X	(Rev. 2/95)	2 Meg x 32	3.3V, EDO	21 pg	442
MT4LD232 XS	(Rev. 2/95)	2 Meg x 32	3.3V, EDO, S	21 pg	442
MT8D432	(Rev. 2/95)	4 Meg x 32	5V	14 pg	412
MT8D432 S	(Rev. 2/95)	4 Meg x 32	5V, S	14 pg	412
MT8LD432	(Rev. 2/95)	4 Meg x 32	3.3V	22 pg	443
MT8LD432 S	(Rev. 2/95)	4 Meg x 32	3.3V, S	22 pg	443
MT8LD432 X	(Rev. 2/95)	4 Meg x 32	3.3V, EDO	22 pg	443
MT8LD432 XS	(Rev. 2/95)	4 Meg x 32	3.3V, EDO, S	22 pg	443
MT16D832	(Rev. 2/95)	8 Meg x 32	5V	14 pg	412
MT16D832 S	(Rev. 2/95)	8 Meg x 32	5V, S	14 pg	412
MT16LD832	(Rev. 2/95)	8 Meg x 32	3.3V	22 pg	443
MT16LD832 S	(Rev. 2/95)	8 Meg x 32	3.3V, S	22 pg	443
MT16LD832 X	(Rev. 2/95)	8 Meg x 32	3.3V, EDO	22 pg	443
MT16LD832 XS	(Rev. 2/95)	8 Meg x 32	3.3V, EDO, S	22 pg	443
MT9D136	(Rev. 2/95)	1 Meg x 36	5V	13 pg	449
MT18D236	(Rev. 2/95)	2 Meg x 36	5V	13 pg	449
MT12D436	(Rev. 2/95)	4 Meg x 36	5V	16 pg	417
MT12D436 S	(Rev. 2/95)	4 Meg x 36	5V, S	16 pg	417
MT24D836	(Rev. 2/95)	8 Meg x 36	5V	16 pg	417
MT24D836 S	(Rev. 2/95)	8 Meg x 36	5V, S	16 pg	417

S .... SELF REFRESH
5V .... 5 volt Vcc
EDO .... Extended Data-Out
3.3V .... 3.3 volt Vcc

DRAM DIMMs

Part	Rev.	Configuration	Description	Pages	DOCUMENT NUMBER
MT2LD(T)132H	(Rev. 2/95)	1 Meg x 32	3.3V	16 pg	446
MT2LD(T)132H S	(Rev. 2/95)	1 Meg x 32	3.3V, S	16 pg	446
MT4LD(T)232H	(Rev. 2/95)	2 Meg x 32	3.3V	16 pg	446
MT4LD(T)232H S	(Rev. 2/95)	2 Meg x 32	3.3V, S	16 pg	446
MT8LD(T)432H	(Rev. 2/95)	4 Meg x 32	3.3V	15 pg	440
MT8LD(T)432H S	(Rev. 2/95)	4 Meg x 32	3.3V, S	15 pg	440
MT16D(T)164	(Rev. 2/95)	1 Meg x 64	5V	19 pg	429
MT16D(T)164 S	(Rev. 2/95)	1 Meg x 64	5V, S	19 pg	429
MT16LD(T)164	(Rev. 2/95)	1 Meg x 64	3.3V	24 pg	435
MT16LD(T)164 S	(Rev. 2/95)	1 Meg x 64	3.3V, S	24 pg	435
MT8LD(T)264	(Rev. 2/95)	2 Meg x 64	3.3V	23 pg	437
MT8LD(T)264 S	(Rev. 2/95)	2 Meg x 64	3.3V, S	23 pg	437
MT8LD(T)264 X	(Rev. 2/95)	2 Meg x 64	3.3V, EDO	23 pg	437

S .... SELF REFRESH
5V .... 5 volt Vcc
EDO .... Extended Data-Out
3.3V .... 3.3 volt Vcc

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DRAM DIMMs (continued)

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MT16D(T)464	(Rev. 2/95)	4 Meg x 64	5V	19 pg	429
MT16LD(T)464	(Rev. 2/95)	4 Meg x 64	3.3V	24 pg	435
MT16LD(T)464 S	(Rev. 2/95)	4 Meg x 64	3.3V, S	24 pg	435
MT16LD(T)464 X	(Rev. 2/95)	4 Meg x 64	3.3V, EDO	24 pg	435
MT16LD(T)464 XS	(Rev. 2/95)	4 Meg x 64	3.3V, EDO, S	24 pg	435
MT18D(T)172	(Rev. 2/95)	1 Meg x 72	5V	19 pg	451
MT18D(T)172 S	(Rev. 2/95)	1 Meg x 72	5V, S	19 pg	451
MT18LD(T)172	(Rev. 2/95)	1 Meg x 72	3.3V	24 pg	438
MT18LD(T)172 S	(Rev. 2/95)	1 Meg x 72	3.3V, S	24 pg	438
MT9LD(T)272	(Rev. 2/95)	2 Meg x 72	3.3V	23 pg	439
MT9LD(T)272 S	(Rev. 2/95)	2 Meg x 72	3.3V, S	23 pg	439
MT9LD(T)272 X	(Rev. 2/95)	2 Meg x 72	3.3V, EDO	23 pg	439
MT9LD(T)272 XS	(Rev. 2/95)	2 Meg x 72	3.3V, EDO, S	23 pg	439
MT18D(T)472	(Rev. 2/95)	4 Meg x 72	5V	19 pg	451
MT18LD(T)472	(Rev. 2/95)	4 Meg x 72	3.3V	24 pg	438
MT18LD(T)472 S	(Rev. 2/95)	4 Meg x 72	3.3V, S	24 pg	438
MT18LD(T)472 X	(Rev. 2/95)	4 Meg x 72	3.3V, EDO	24 pg	438
MT18LD(T)472 XS	(Rev. 2/95)	4 Meg x 72	3.3V, EDO, S	24 pg	438

S .... SELF REFRESH   EDO .... Extended Data-Out
5V .... 5 volt Vcc   3.3V .... 3.3 volt Vcc

DRAM CARDS

Part	Rev.	Organization	Description	Pages	Document Number
MT8D88C132(S)	(Rev. 2/95)	1 Meg x 32	5V	17 pg	500
MT8D88C132H(S)	(Rev. 2/95)	1 Meg x 32	5V	17 pg	501
MT8D88C132V(S)	(Rev. 2/95)	1 Meg x 32	3.3V	17 pg	502
MT8D88C132VH(S)	(Rev. 2/95)	1 Meg x 32	3.3V	17 pg	503
MT16D88C232(S)	(Rev. 2/95)	2 Meg x 32	5V	17 pg	500
MT16D88C232H(S)	(Rev. 2/95)	2 Meg x 32	5V	17 pg	501
MT16D88C232V(S)	(Rev. 2/95)	2 Meg x 32	3.3V	17 pg	502
MT16D88C232VH(S)	(Rev. 2/95)	2 Meg x 32	3.3V	17 pg	503
MT8D88C432V(S)	(Rev. 2/95)	4 Meg x 32	3.3V	17 pg	502
MT8D88C432VH(S)	(Rev. 2/95)	4 Meg x 32	3.3V	17 pg	503
MT16D88C832V(S)	(Rev. 2/95)	8 Meg x 32	3.3V	17 pg	502
MT16D88C832VH(S)	(Rev. 2/95)	8 Meg x 32	3.3V	17 pg	503

5V .... 5 volt Vcc   3.3V .... 3.3 volt Vcc

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TN-00-02	Tape-and-Reel Procedures (Rev. 2/95)	5 pg	601
TN-00-03	Using Gel-Pak® Packaging With Micron Die (Rev. 2/95)	2 pg	624
TN-04-01	DRAM Power-Up and Refresh Constraints (Rev. 2/95)	1 pg	602
TN-04-06	$\overline{OE}$-Controlled/LATE WRITE Cycles (DRAM) (Rev. 2/95)	2 pg	603
TN-04-12	LPDRAM Extended Refresh Current vs. $\overline{RAS}$ Active Time (4 Meg) (Rev. 2/95)	1 pg	606
TN-04-15	DRAM Considerations for PC Memory Design (Rev. 2/95)	6 pg	608
TN-04-16	16 Meg DRAM—2K vs. 4K Refresh Comparison (Rev. 2/95)	2 pg	609
TN-04-19	Low-Power DRAMs vs. Slow SRAMs for Main Memory (Rev. 2/95)	2 pg	611
TN-04-20	SELF REFRESH DRAMs (Rev. 2/95)	2 pg	612
TN-04-21	Reduce DRAM Cycle Times with Extended Data-Out (Rev. 2/95)	8 pg	613

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TN-04-22	256K x 16 DRAM Typical Operating Curves (Rev. 2/95)	2 pg	614
TN-04-23	4 Meg DRAM Typical Operating Curves (Rev. 2/95)	6 pg	615
TN-04-24	4 Meg DRAM—Access Time vs. Capacitance (Rev. 2/95)	2 pg	616
TN-04-26	256K x 16—Access Time vs. Capacitance (Rev. 2/95)	1 pg	619
TN-04-28	DRAM Soft Error Rate Calculations (Rev. 2/95)	3 pg	621
TN-04-29	Maximizing EDO Advantages at the System Level (Rev. 2/95)	12 pg	622
TN-04-30	Various Methods of DRAM Refresh (Rev. 2/95)	4 pg	623
TN-04-31	PCB Layout for 4 Meg x 4 300 Mil or 400 Mil SOJ (Rev. 2/95)	2 pg	626
TN-04-32	Reduce DRAM Memory Cost with Cache (Rev. 2/95)	4 pg	627
TN-41-01	Decrement Bursting with the SGRAM (Rev. 2/95)	4 pg	625
TN-88-01	88-Pin DRAM Cards (Rev. 2/95)	3 pg	618

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5V SRAMs

MT5C2561	(Rev. 11/94)	256K x 1	CE only	11 pg	1202
MT5C2564	(Rev. 11/94)	64K x 4	CE only	11 pg	1208
MT5C2565	(Rev. 11/94)	64K x 4	CE & OE	12 pg	1209
MT5C256K4A1	(Rev. 11/94)	256K x 4	CE & OE, Revolutionary Pinout	10 pg	1211
MT5C2568	(Rev. 11/94)	32K x 8	CE & OE	12 pg	1215
MT5C128K8A1	(Rev. 11/94)	128K x 8	CE & OE, Revolutionary Pinout	10 pg	1217
MT5C64K16A1	(Rev. 11/94)	64K x 16	BE, CE & OE, Revolutionary Pinout	11 pg	1221

CE .... CHIP ENABLE
BE .... BYTE ENABLE
OE .... OUTPUT ENABLE
REVOLUTIONARY PINOUT .... CENTER PIN POWER AND GROUND

3.3V SRAMS

MT5LC2561	(Rev. 11/94A)	256K x 1	CE only with separate I/O	9 pg	1300
MT5LC1001	(Rev. 11/94)	1 Meg x 1	CE only with separate I/O	9 pg	1301
MT5LC2564	(Rev. 11/94A)	64K x 4	CE only	9 pg	1302
MT5LC2565	(Rev. 11/94A)	64K x 4	CE & OE	10 pg	1303
MT5LC1005	(Rev. 11/94)	256K x 4	CE & OE	10 pg	1304
MT5LC256K4D4	(Rev. 11/94)	256K x 4	CE, Revolutionary Pinout	10 pg	1305
MT5LC1M4D4	(Rev. 11/94)	1 Meg x 4	CE & OE, Revolutionary Pinout	9 pg	1306
MT5LC2568	(Rev. 11/94A)	32K x 8	CE & OE	10 pg	1307
MT5LC1008	(Rev. 11/94)	128K x 8	CE1, CE2 & OE	11 pg	1308
MT5LC128K8D4	(Rev. 11/94)	128K x 8	CE & OE, Revolutionary Pinout	10 pg	1309
MT5LC512K8D4	(Rev. 11/94)	512K x 8	CE & OE, Revolutionary Pinout	9 pg	1310
MT5LC64K16D4	(Rev. 11/94)	64K x 16	BE, CE & OE, Revolutionary Pinout	11 pg	1311
MT5LC256K16D4	(Rev. 11/94)	256K x 16	BE, CE & OE	13 pg	1312

CE .... CHIP ENABLE
BE .... BYTE ENABLE
OE .... OUTPUT ENABLE
REVOLUTIONARY PINOUT .... CENTER PIN POWER AND GROUND

SRAM DIE

S12D	(Rev. 1/94)	256K	x1, x4, x8	4 pg	2502
S12C	(Rev. 11/94)	256K	x1, x4, x8	5 pg	2506
S18A	(Rev. 1/94)	1 Meg	x1, x4, x8 (Available 8/94)	5 pg	2503
S13A	(Rev. 11/94)	1 Meg	x8, x16	4 pg	2504
S22B	(Rev. 9/94)	1 Meg	x18, x32, x36	5 pg	2507

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SYNCHRONOUS SRAMs

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MT58LC64K18M1	(Rev. 11/94)	64K x 18	SyncBurst, Linear	17 pg	1502
MT58LC32K32B2	(Rev. 11/94)	32K x 32	SyncBurst	17 pg	1512
MT58LC32K32C4	(Rev. 11/94)	32K x 32	SyncBurst, Interleaved, Pipelined	16 pg	1513
MT58LC32K36B2	(Rev. 11/94)	32K x 36	SyncBurst, Interleaved	14 pg	1508
MT58LC32K36C4	(Rev. 11/94)	32K x 36	SyncBurst, Interleaved, Pipelined	14 pg	1509
MT58LC64K36B2	(Rev. 12/94)	64K x 36		18 pg	1514

SRAM MODULES

Part	Revision	Configuration	Description	Pages	DOCUMENT NUMBER
MT8S6432	(Rev. 11/94)	64K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1901
MT8LS6432	(Rev. 11/94)	64K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1902
MT4S12832	(Rev. 11/94)	128K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1903
MT4LS12832	(Rev. 11/94)	128K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1904
MT4LS12832R	(Rev. 9/94)	128K x 32		9 pg	1909
MT8S25632	(Rev. 11/94)	256K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1905
MT8LS25632	(Rev. 11/94)	256K x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1906
MT8LS25632R	(Rev. 9/94)	256K x 32		9 pg	1908
MT8LS132	(Rev. 11/94)	1 Meg x 32	$\overline{CE}$ & $\overline{OE}$	9 pg	1907
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MT2LSYT3264T2	(Rev. 11/94)	32K x 64	SyncBurst, Interleaved	13 pg	3002
MT2LSYT3264T4	(Rev. 11/94)	32K x 64	SyncBurst, Interleaved, Pipelined	13 pg	3003
MT2LSYT3264T6	(Rev. 11/94)	32K x 64	SyncBurst, Linear, Pipelined	13 pg	3003
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MT2LSYT3264C4	(Rev. 11/94)	32K x 64	SyncBurst, Interleaved, Linear, Pipelined	7 pg	3001
MT2LSYT3272T1	(Rev. 11/94)	32K x 72	SyncBurst, Linear	14 pg	3006
MT2LSYT3272T2	(Rev. 11/94)	32K x 72	SyncBurst, Interleaved	14 pg	3006
MT2LSYT3272T4	(Rev. 11/94)	32K x 72	SyncBurst, Interleaved, Pipelined	14 pg	3007
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MT4LSY6472T6	(Rev. 11/94)	64K x 72	SyncBurst, Linear, Pipelined	14 pg	3007
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MT4LSYT6472C4	(Rev. 11/94)	64K x 72	SyncBurst, Interleaved, Linear, Pipelined	8 pg	3005

CE .... CHIP ENABLE   OE .... OUTPUT ENABLE

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TN-05-02	SRAM Bus Contention Design Considerations (Rev. 11/94)	4 pg	2000
TN-05-03	5V SRAM Capacitive Loading (Rev. 11/94)	1 pg	2001
TN-05-06	1 Meg Evolutionary Pinout SRAM Typical (5V) Operating Curves (Rev. 11/94)	2 pg	2002
TN-05-07	256K SRAM Typical (5V) Operating Curves (Rev. 11/94)	2 pg	2003
TN-05-13	1 Meg Low-Power SRAMs (Rev. 11/94)	3 pg	2005
TN-05-14	SRAM Thermal Design Considerations (Rev. 11/94)	5 pg	2006
TN-05-16	A Designer's Guide to 3.3V SRAMs (Rev. 11/94)	6 pg	2010
TN-05-17	Low-Power Memory Design Using Data Retention (Rev. 11/94)	3 pg	2011

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TN-05-21 .... High-Speed Memory Design Techniques (Rev. 11/94) .... 6 pg 2015
TN-05-22 .... 1 Meg Revolutionary Pinout SRAM Typical (5V) Operating Curves (Rev. 11/94) .... 3 pg 2017
TN-05-23 .... 256K SRAM Typical (3.3V) Operating Curves (Rev. 11/94) .... 2 pg 2018
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TN-58-02 .... Design Tips: 32K x 36 Synchronous SRAM (Rev. 11/94) .... 5 pg 2009
TN-58-03 .... SyncBurst™ SRAMs in Asynchronous Designs (Rev. 11/94) .... 5 pg 2012
TN-58-04 .... Design Tips: SyncBurst™ SRAM Standards (Rev. 11/94) .... 5 pg 2019

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MT28F200 .... (Rev. 7/94) ..... 128K x 16/256K x 8 — BB, AUTO .... 26 pg 2602
MT28F004 .... (Rev. 7/94) .... 512K x 8 — BB, AUTO .... 25 pg 2603
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BB .... Boot Block
SB .... Symmetric Block
AUTO .... Automated W/E Algorithm
DPD .... Deep Power Down

3.3/12 VOLT FLASH MEMORY

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MT28LF400 .... (Rev. 7/94) ..... 256K x 16/512K x 8 — BB, AUTO .... 26 pg 2903
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BB .... Boot Block
SB .... Symmetric Block
AUTO .... Automated W/E Algorithm
DPD .... Deep Power Down

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Design Line, February (Spring), 1993:
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