Data Book

CBT Bus Switches
Crossbar Technology

1995

TEXAS INSTRUMENTS

CBT Bus Switches
Crossbar Technology

Data Book

1995

Advanced System Logic Products

CBT Bus Switches
Crossbar Technology
Data Book

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Printed in U.S.A. by
Custom Printing Company
Owensville, Missouri

INTRODUCTION

Digital electronics are performing at ever higher speeds; therefore, every barrier to system performance must be removed. High-speed microprocessors, synchronous DRAMs, and new bus architectures require supporting logic that keeps data moving fast.

This edition of the Texas Instruments 1995 CBT Bus Switches Crossbar Technology Data Book includes the industry's most comprehensive line of integrated bus switches. With propagation delays of 250 ps, these high-speed bus switches bring greater system speed and reduced power consumption to today's advanced electronic equipment. These n-channel MOS transistors provide isolation (3-state) when the switch is open and near-zero propagation delay when the switch is closed. CBT switches also function as 5-V to 3.3-V level translators, helping designers mix low-cost DRAMs with high-performance 3-V processors.

The CBT family of bus switches consists of 4-, 8-, 10-, 16-, 18-, and 24-bit-wide switches, exchangers, and multiplexers. With pin-for-pin compatible devices, the migration from existing logic devices is easy. These products are offered in the industry's most extensive line of packaging including the world's smallest octal package and the distributed power and ground Widebus™ package.

Most of the products in this data book are available in production quantities. Please contact your local authorized distributor or Texas Instruments representative for details on any of these devices. Some of the devices in this data book are not yet available in production quantities; information on these devices is included as Advanced Information or Product Preview. For more information on these products including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments representative, authorized distributor, or call the Advanced System Logic hotline at (903) 868-5202.

We hope that you agree that Texas Instruments has the most complete line of bus-switch products in the industry. We also hope that these products meet your system and design needs.

PRODUCT STAGE STATEMENTS

Product stage statements are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

If all products specified in a data sheet are at the same development stage, the appropriate statement from the following list is placed in the lower left corner of the first page of the data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

If not all products specified in a data sheet are at the PRODUCTION DATA stage, then the first statement below is placed in the lower left corner of the first page of the data sheet. Subsequent pages of the data sheet containing PRODUCT PREVIEW information or ADVANCE INFORMATION are then marked in the lower left-hand corner with the appropriate statement given below:

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Contents

INTRODUCTION

Replacements are based on similarity of electrical and mechanical characteristics shown in currently published data. Interchangeability in particular applications is not ensured. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and the buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

CBT octal function cross-reference guide

TEXAS INSTRUMENTS	QUALITY	PERICOM
SN74CBT3125	QS3125	PI5C3125
SN74CBT3126†	—	PI5C3126
SN74CBT3244	QS3244	PI5C3244
SN74CBT3245	QS3245	PI5C3245
SN74CBT3251†	QS3251	PI5C3251
SN74CBT3253†	QS3253	PI5C3253
SN74CBT3257	QS3257	PI5C3257
SN74CBT3306	—	—
SN74CBT3345	—	—
SN74CBT3383	QS3383, QS3L383	PI5C3383
SN74CBT3384A	QS3384, QS3L384	PI5C3384
SN74CBT3386†	QS3386	—
SN74CBT3388†	QS3388	—
SN74CBT6800	QS3800	—

† Please contact the Advanced System Logic hotline at (903) 868-5202 to learn more about plans for these devices.

package cross-reference guide

TEXAS INSTRUMENTS	QUALITY	PERICOM
D	S1	W
DB	—	—
DW	SO	S
PW‡	—	L

‡ Smallest CBT package

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**

The internal capacitance at an input of the device

C_o **Output capacitance**

The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} **Supply current**

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V_O = 5.5 V

$I_{I(hold)}$ **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} **High-level input current**

The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**

The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V_{CC} = 0 V

I_{OH} **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, establish a high level at the output

I_{OL} **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, establish a low level at the output

*Current out of a terminal is given as a negative value.

I_{OZ} **Off-state (high-impedance-state) output current (of a 3-state output)**

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, establish the high-impedance state at the output

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs change only if they are responding to data that would cause the output to go low so, for them $t_{en} = t_{PHL}$.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to a high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to a high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to the defined low level

$t_{sk(o)}$ **Output skew**

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establish a high level at the output

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establish a low level at the output

V_{T+} **Positive-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}

V_{T-} **Negative-going threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}

In digital-system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the CBT family. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\Theta JA} \times P_T + T_A$$

Where:

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to ambient
P_T = total power dissipation of the device
T_A = free-air temperature

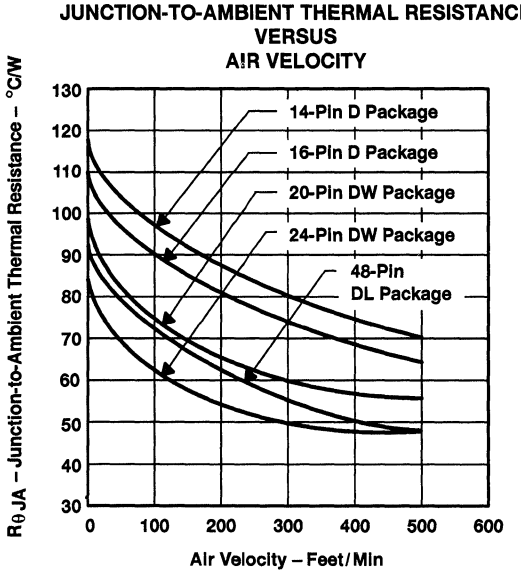


Figure 1

Figures 2 through 5 show power dissipation derating for the 8-, 16,- 20-, and 24-pin DB packages.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

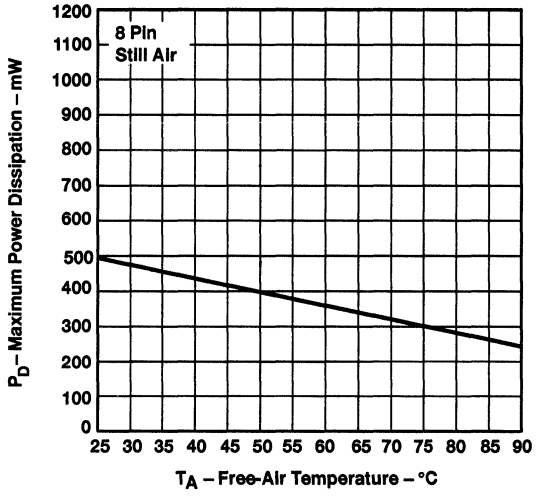


Figure 2

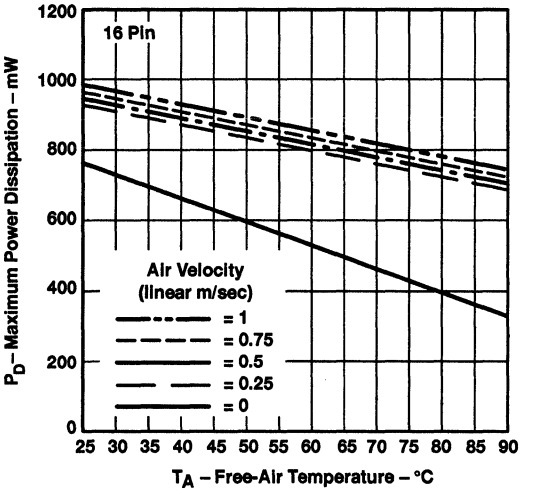


Figure 3

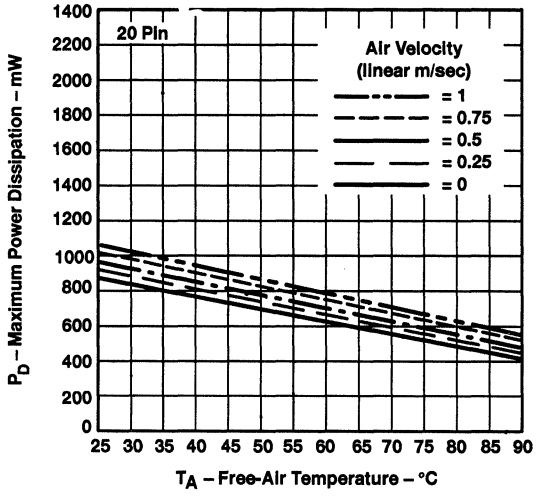


Figure 4

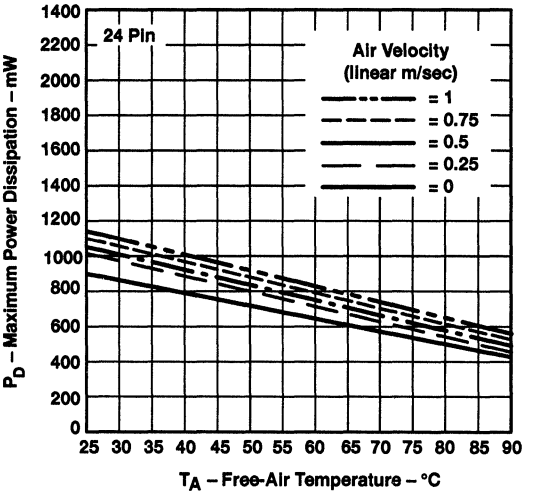
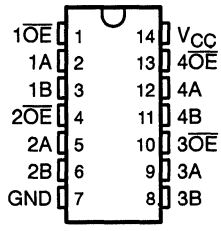


Figure 5

Contents

- **Standard '125-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3125 quadruple bus switch features independent line switches. Each switch is disabled when the associated output-enable ($\overline{OE}$) input is high.

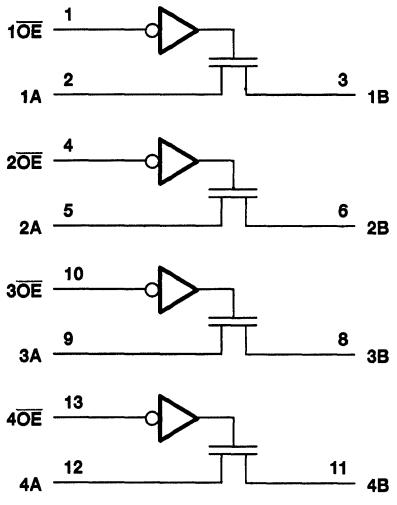
The SN74CBT3125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT $\overline{OE}$	INPUTS/ OUTPUTS
	A, B
L	A = B
H	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}¶		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		16	22	Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		10	15	Ω

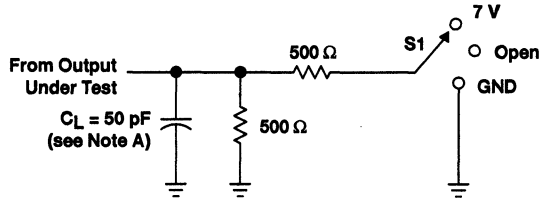
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.25		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.6	5.4		6	ns
t_{dis}	$\overline{OE}$	A or B	1	4.7		5.1	ns

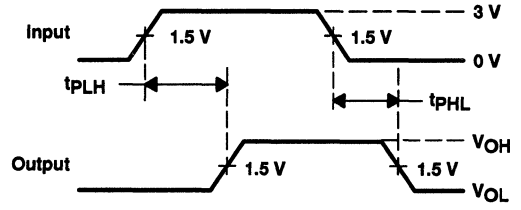
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

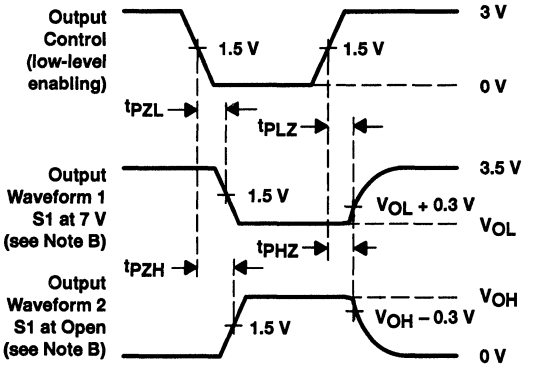


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



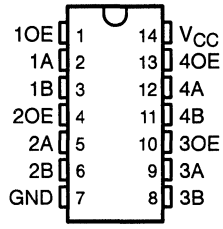
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Standard '126-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3126 quadruple bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

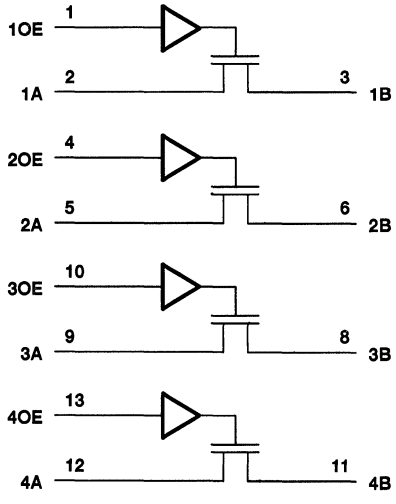
The SN74CBT3126 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT3126 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT OE	INPUTS/ OUTPUTS
	A, B
H	A = B
L	Z

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.25 W
DB package ..... 0.5 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	OE = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

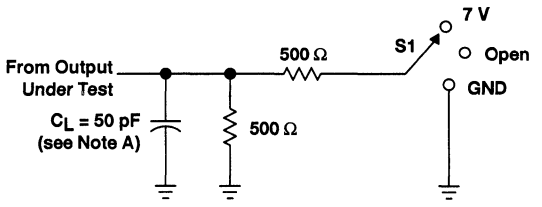
PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns

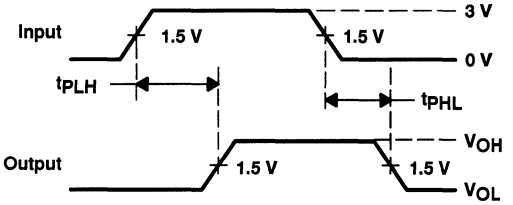
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

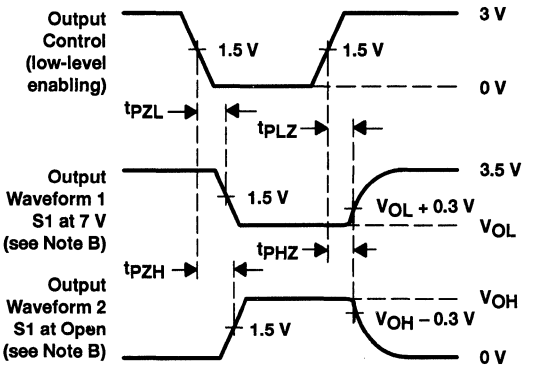


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

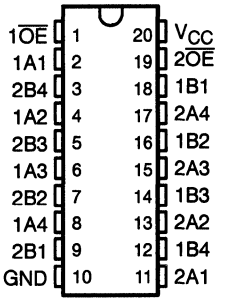
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

SCDS001C – NOVEMBER 1992 – REVISED MAY 1995

- **Functionally Equivalent to QS3244**
- **Standard '244-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

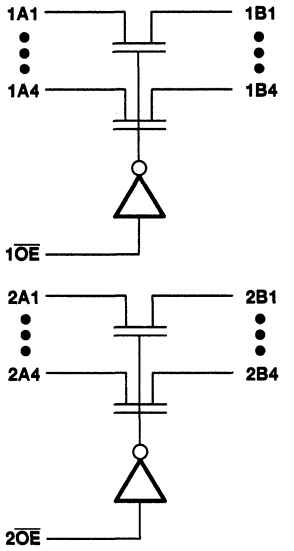
The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3244 is characterized for operation from 0°C to 70 °C.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$1\overline{OE}$	$2\overline{OE}$	1A, 1B	2A, 2B
L	L	1A= 1B	2A= 2B
L	H	1A= 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Continuous channel current ..... 128 mA
Clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

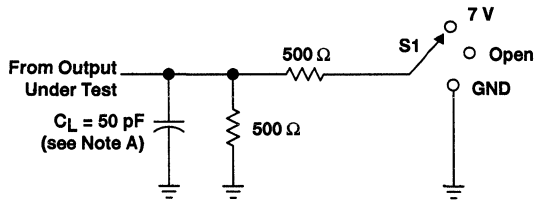
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.9	ns
t_{dis}	$\overline{OE}$	A or B	1	7.4	ns

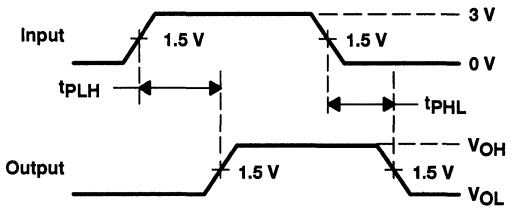
¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

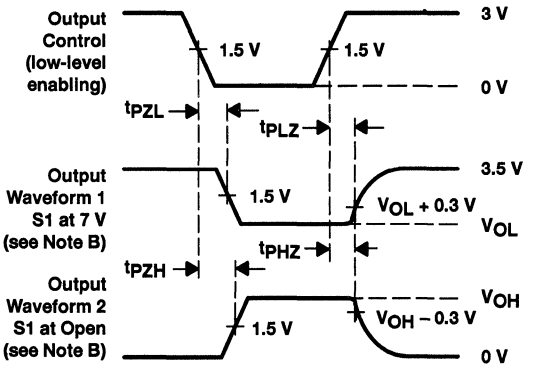


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

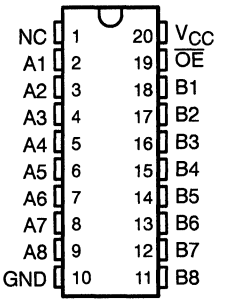
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} andt_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS002C – NOVEMBER 1992 – REVISED MAY 1995

- **Functionally Equivalent to QS3245**
- **Standard '245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

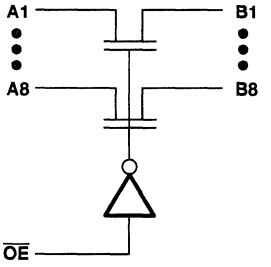
The device is organized as one 8-bit switch. When output enable ($\overline{OE}$) is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT $\overline{OE}$	INPUTS/ OUTPUTS A, B
L	A = B
H	Z

logic diagram



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

ADVANCE INFORMATION

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	μA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		10	15	Ω

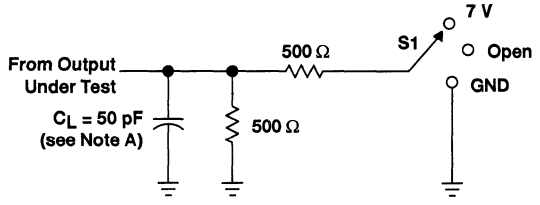
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B			ns
t_{dis}	$\overline{OE}$	A or B			ns

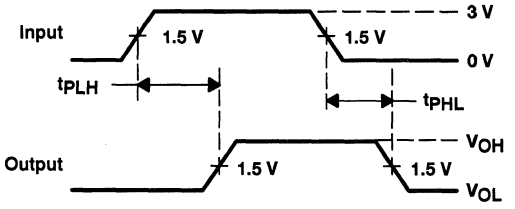
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

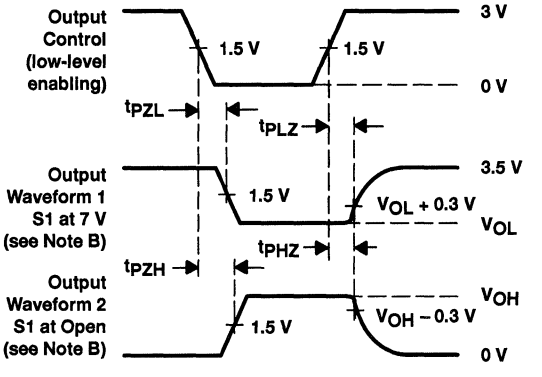


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

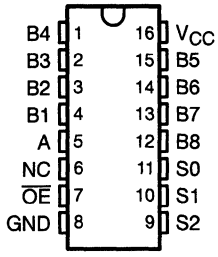
Figure 1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

SCDS019 – MAY 1995

- **Functionally Equivalent to QS3251**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3251 is an 8-bit to 1-bit high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When output enable ($\overline{OE}$) is low, the SN74CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

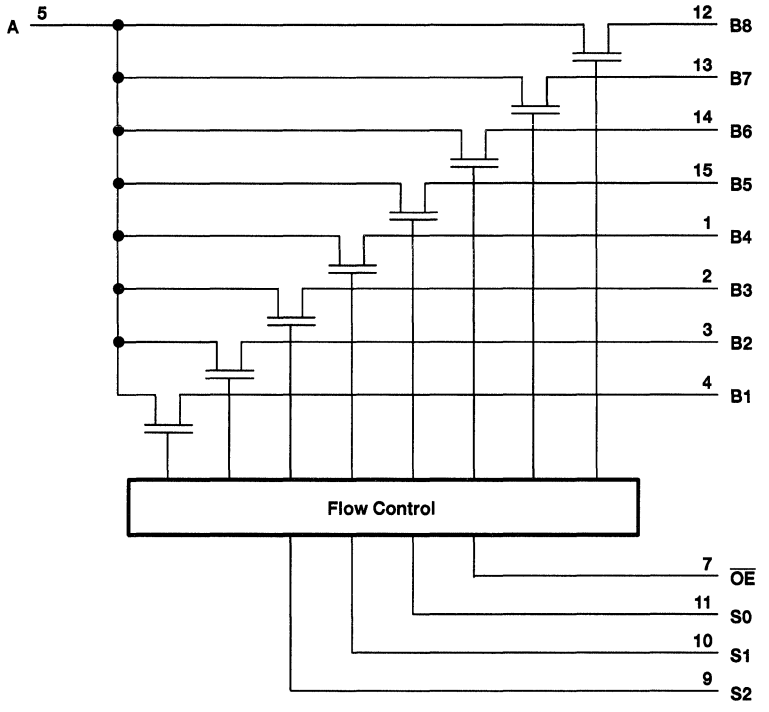
The SN74CBT3251 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	$\overline{OE}$	FUNCTION
X	X	X	H	Disconnect
L	L	L	L	A to B1
L	L	H	L	A to B2
L	H	L	L	A to B3
L	H	H	L	A to B4
H	L	L	L	A to B5
H	L	H	L	A to B6
H	H	L	L	A to B7
H	H	H	L	A to B8

PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

PRODUCT PREVIEW

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}					pF
	B port					6		
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA (optional)		5	7	
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

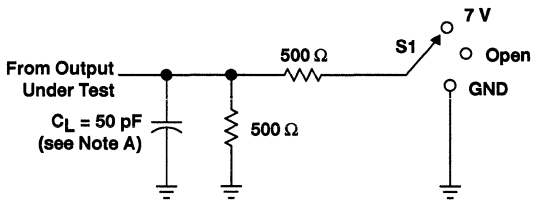
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

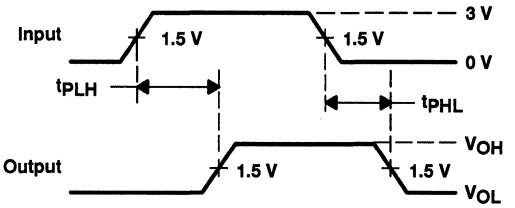
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

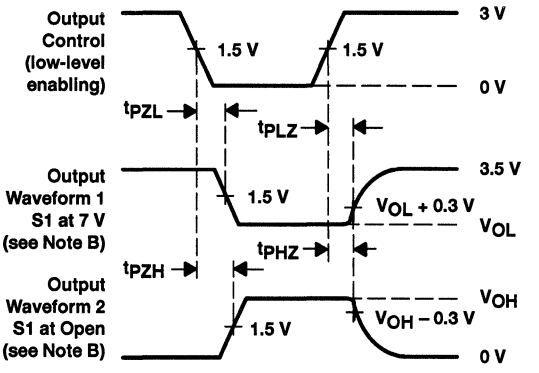


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

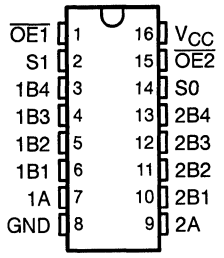
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS018 – MAY 1995

- **Functionally Equivalent to QS3253**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3253 is a dual 4-bit to 1-bit high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

$\overline{OE1}$, $\overline{OE2}$, S0, and S1 select the appropriate B output for the A-input data.

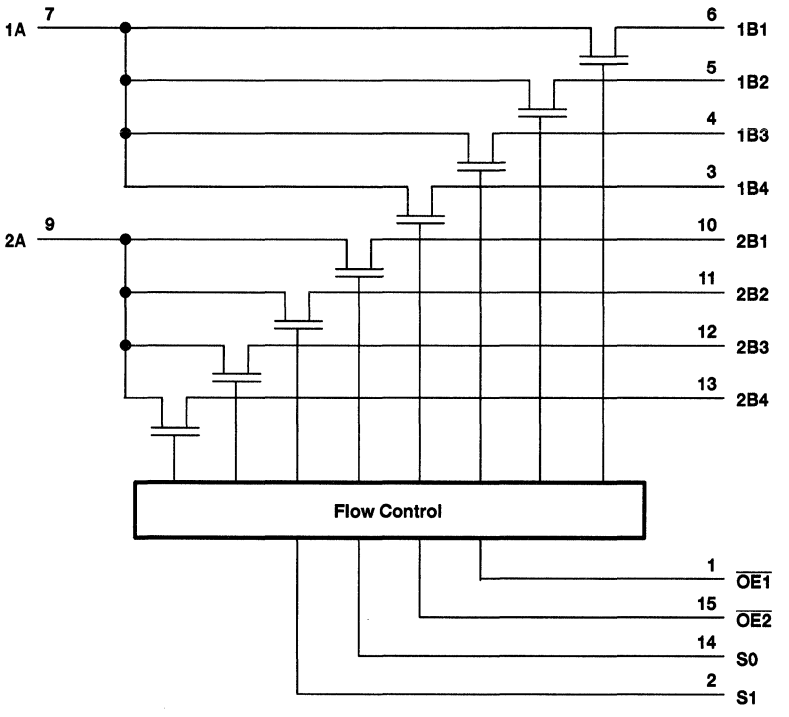
The SN74CBT3253 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S1	S0	$\overline{OE1}$	$\overline{OE2}$	FUNCTION
X	X	X	H	Disconnect 1A
X	X	H	X	Disconnect 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	H	L	L	1A to 1B2 and 2A to 2B2
H	L	L	L	1A to 1B3 and 2A to 2B3
H	H	L	L	1A to 1B4 and 2A to 2B4

PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

PRODUCT PREVIEW

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5 V,	V_I = 5.5 V to GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}					pF
	B port					6		
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA (optional)		5	7	
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

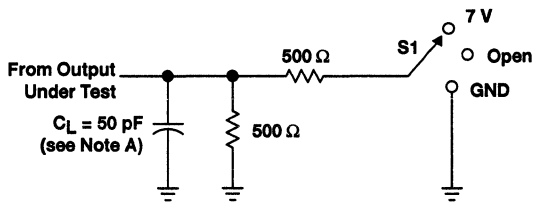
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

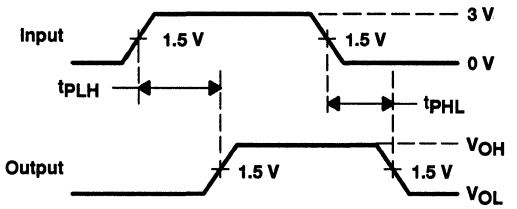
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

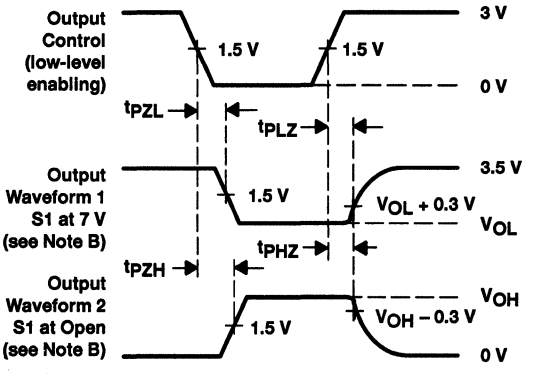


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

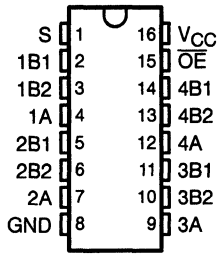
Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SCDS017 – MAY 1995

- **Functionally Equivalent to QS3257**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3257 is a quadruple 2-bit to 1-bit high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

$\overline{OE}$ and S select the appropriate B1 and B2 outputs for the A-input data.

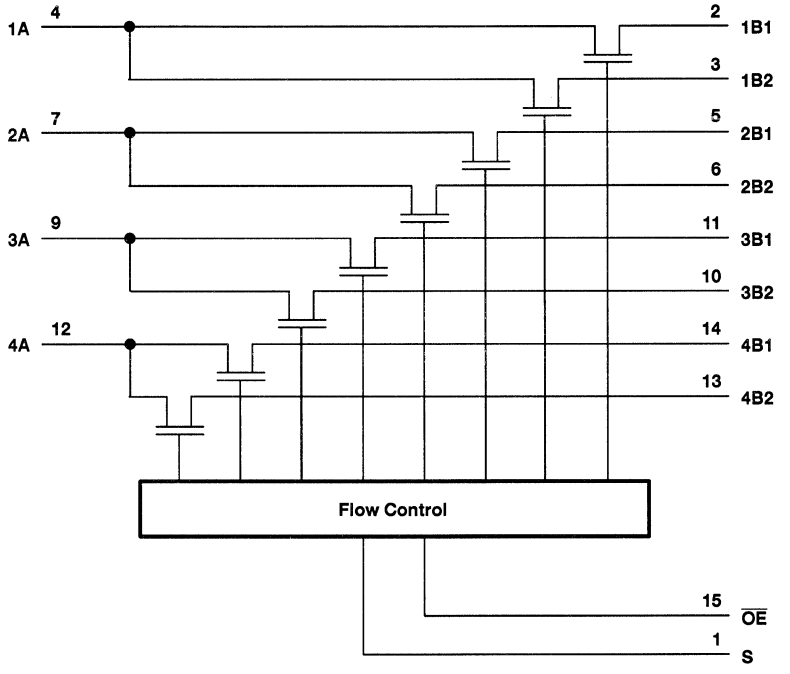
The SN74CBT3257 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	1A to 1B1, 2A to 2B1, 3A to 3B1 and 4B to 4B1
H	L	1A to 1B2, 2A to 2B2, 3A to 3B2 and 4A to 4B2

ADVANCE INFORMATION

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 1.3 W
DB package ..... 0.55 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

ADVANCE INFORMATION

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}					pF
	B port					6		
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA (optional)		5	7	
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

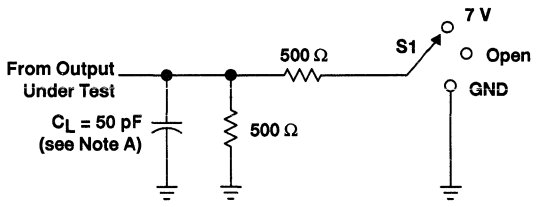
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	S	A or B			ns
t_{en}	$\overline{OE}$	A or B			ns
t_{dis}	$\overline{OE}$	A or B			ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

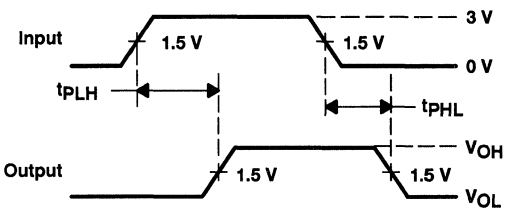
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

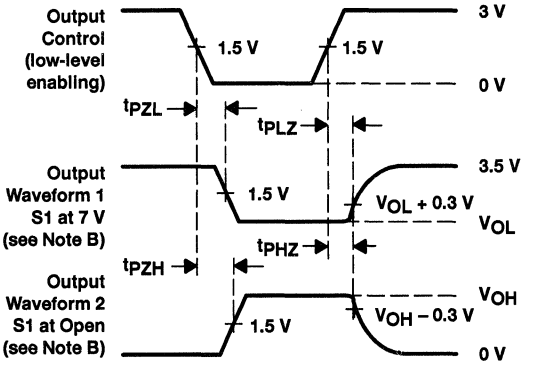


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

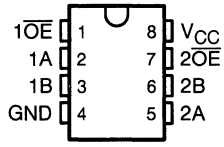
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages**

D OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3306 dual bus switch features independent line switches. Each switch is disabled when the associated output-enable ($\overline{OE}$) input is high.

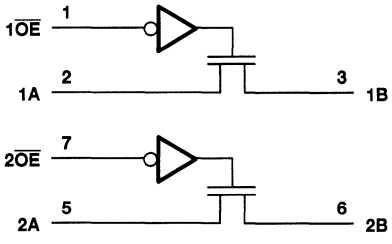
The SN74CBT3306 is available in TI's plastic small-outline package (D) and thin shrink small-outline package (PW).

The SN74CBT3306 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUT $\overline{OE}$	INPUTS/ OUTPUTS
	A, B
L	A = B
H	Z

logic diagram (positive logic)



ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_K ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package ..... 0.8 W
PW package ..... 0.5 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V to GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA (optional)		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 15 mA		10	15	Ω

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

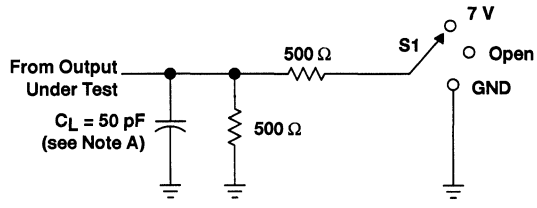
ADVANCE INFORMATION

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B			ns
t_{dis}	$\overline{OE}$	A or B			ns

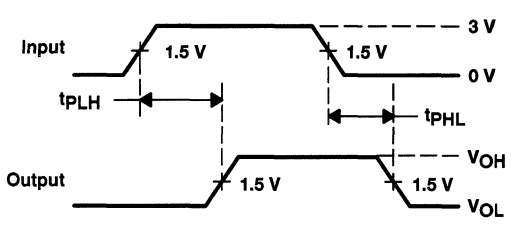
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

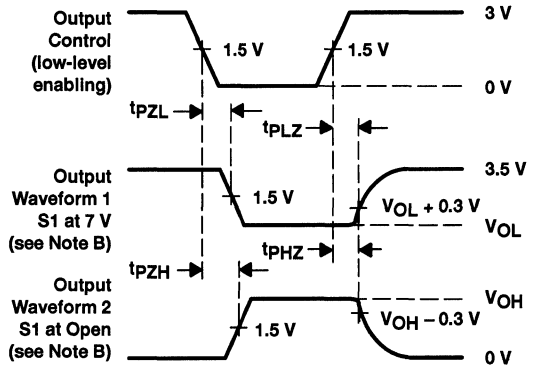


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

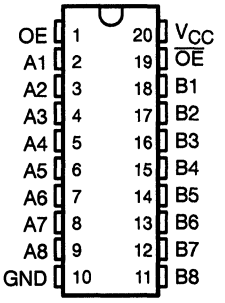
Figure 1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

SCDS027 – MAY 1995

- **Standard '245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Control Input Levels**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

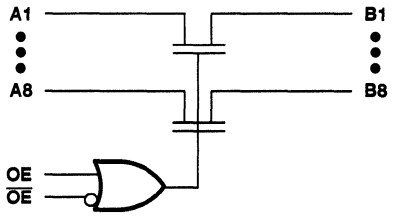
The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{OE}$) inputs. When $\overline{OE}$ is low or OE is high, the switch is on and port A is connected to port B. When $\overline{OE}$ is high and OE is low, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3345 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		INPUT/ OUTPUTS
OE	$\overline{OE}$	A, B
X	L	A = B
H	X	A = B
L	H	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	$V_I = V_{CC}$ or GND			50	μA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE} = V_{CC}$ or OE = GND			6		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

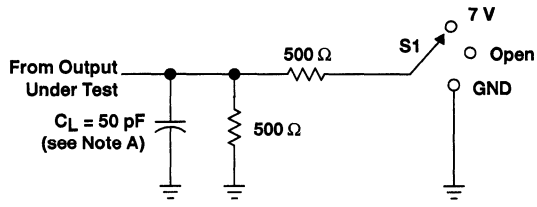
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$ or OE	A or B	1	9.1	ns
t_{dis}	$\overline{OE}$ or OE	A or B	1	8.7	ns

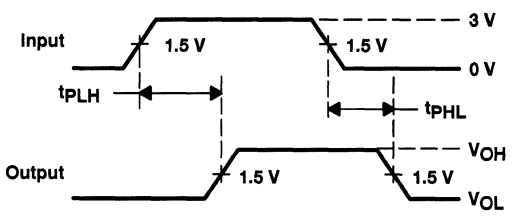
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

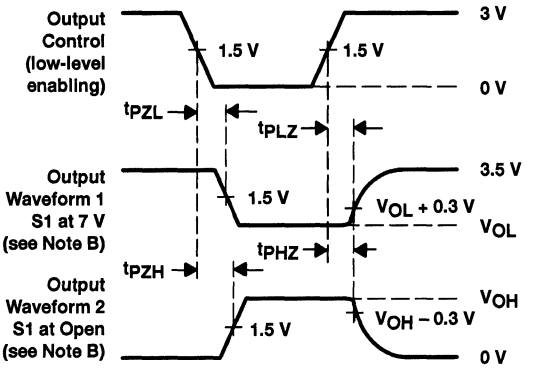


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

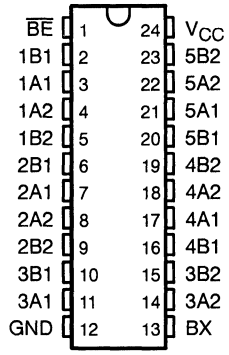
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS003C – NOVEMBER 1992 – REVISED MAY 1995

- **Functionally Equivalent to QS3383 and QS3L383**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), Thin Shrink Small-Outline (PW), Ceramic DIPs (JT), and Ceramic Flat (W) Packages**

SN54CBT3383 . . . JT OR W PACKAGE
SN74CBT3383 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The 'CBT3383 provide ten bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

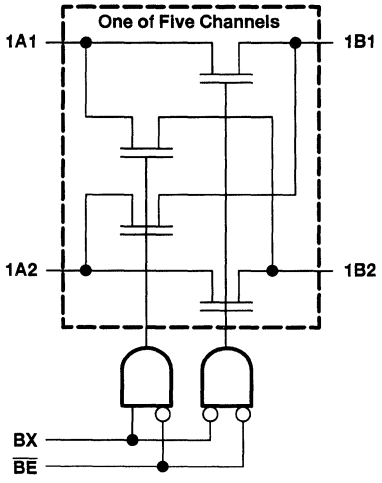
The devices operate as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when $\overline{BE}$ is low.

The SN54CBT3383 is charaterized for operation from –55°C to 125°C. The SN74CBT3383 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

$\overline{BE}$	BX	1A1–5A1	1A2–5A2
L	L	1B1–5B1	1B2–5B2
L	H	1B2–5B2	1B1–5B1
H	X	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 6 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		SN54CBT3383		SN74CBT3383		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54CBT3383			SN74CBT3383			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN§,	I_I = −18 mA				−1.2			−1.2	V
I_I		V_{CC} = MAX§,	V_I = V_{CC} MAX or GND				±5			±5	µA
I_{CC}		V_{CC} = MAX§, V_I = V_{CC} or GND	I_O = 0,				50			50	µA
ΔI_{CC}¶	Control pins	V_{CC} = MAX§, Other inputs at V_{CC} or GND	One input at 3.4 V,				2.5			2.5	mA
C_i	Control pins	V_I = 3 V or 0							3		pF
		V_I = 2.5 V					5				
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{BE}$ = V_{CC}						6		pF
		V_O = 2.5 V	$\overline{BE}$ = V_{CC}				6				
r_{on}#		V_{CC} = MIN§,	V_I = 0,	I_I = 64 mA		5	9.2		5	7	Ω
		V_{CC} = MIN§,	V_I = 0,	I_I = 30 mA					5	7	
		V_{CC} = MIN§,	V_I = 2.4 V,	I_I = 15 mA		10	17		10	15	

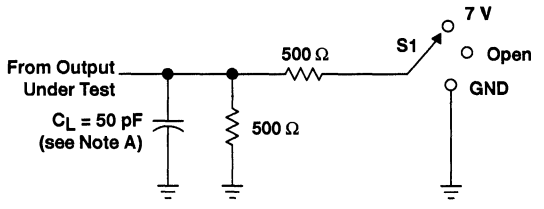
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ For conditions shown as MIN or MAX use the appropriate values under recommended operating conditions.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
# Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT3383		SN74CBT3383		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		1.5		0.25	ns
t_{en}	BX	A or B	1	10.2	1	9.2	ns
t_{en}	$\overline{BE}$	A or B	1	10.8	1	8.6	ns
t_{dis}	$\overline{BE}$	A or B	1	8.2	1	7.5	ns

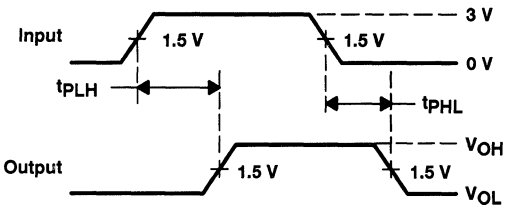
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

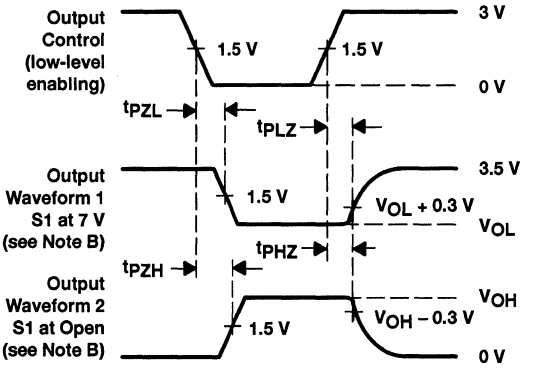


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

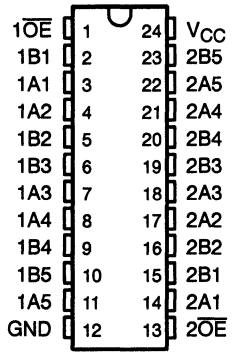
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS004C – NOVEMBER 1992 – REVISED JULY 1995

- **Functionally Equivalent to QS3384 and QS3L384**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3384A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

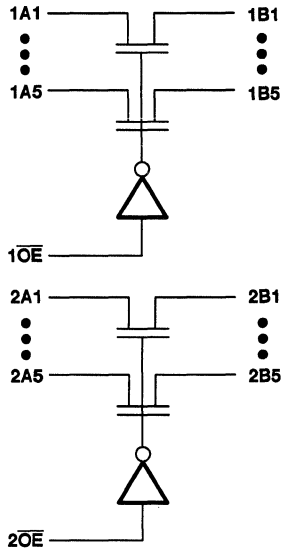
The device is organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBT3384A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$1\overline{OE}$	$2\overline{OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4.5		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

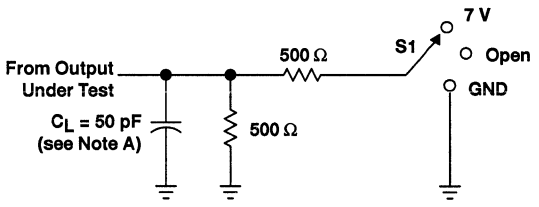
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.9	5.7		6.2	ns
t_{dis}	$\overline{OE}$	A or B	2.1	5.2		5.5	ns

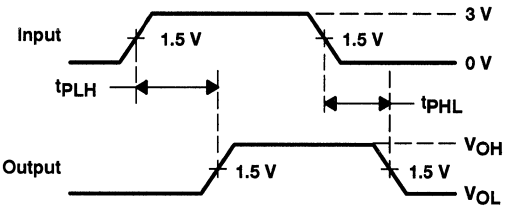
¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

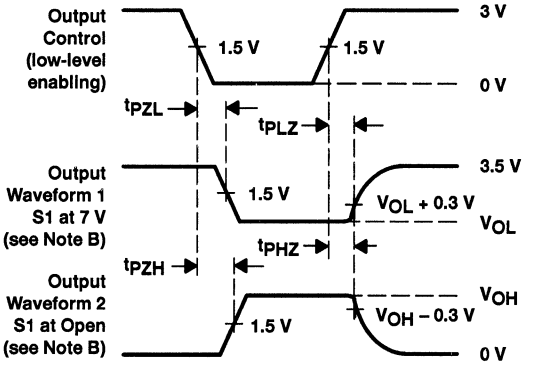


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



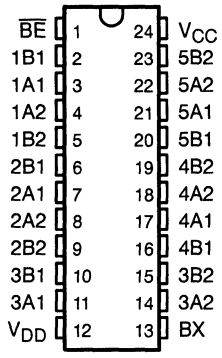
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Functionally Equivalent to QS3386**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (DB), Shrink Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**
- **Uses V_{CC} of 5 V and V_{DD} of –2 V**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3386 provides ten bits of high-speed TTL-compatible bus switching or exchanging. The input signals can range from –2 V to 5 V. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

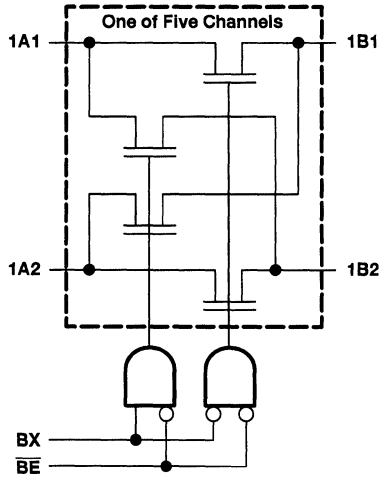
The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which allows swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are disconnected when $\overline{BE}$ is high.

The SN74CBT3386 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$\overline{BE}$	BX	1A1–5A1	1A2–5A2
L	L	1B1–5B1	1B2–5B2
L	H	1B2–5B2	1B1–5B1
H	X	Z	Z

logic diagram



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} to V_{DD} ..... −0.5 V to 7 V
Supply voltage range, V_{DD} ..... −2.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... V_{DD} − 0.5 V to V_{DD} + 7.5 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				V_{DD} −1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}§	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{BE}$ = V_{CC}			6		pF
r_{on}¶		V_{CC} = 4.75 V,	V_I = 0,	I_I = 64 mA (optional)		7	9	Ω
		V_{CC} = 4.75 V,	V_I = 0,	I_I = 30 mA		7	9	
		V_{CC} = 4.75 V,	V_I = 2.4 V,	I_I = 15 mA		12	17	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two terminals.

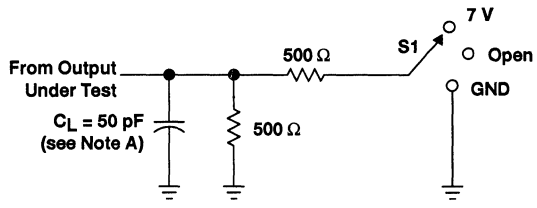
PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}†	A or B	B or A		0.25	ns
t_{en}	BX	A or B			ns
t_{en}	$\overline{BE}$	A or B			ns
t_{dis}	$\overline{BE}$	A or B			ns

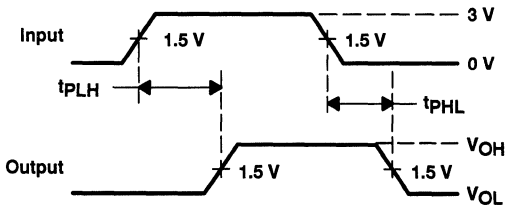
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

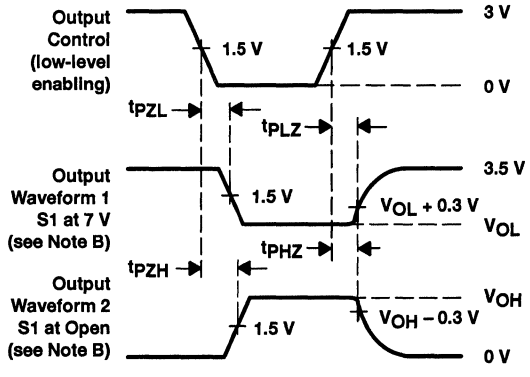


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

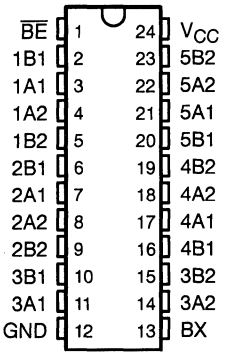
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Functionally Equivalent to QS3388**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Bus Hold on I/O Pins**
- **Package Options Include Plastic Small-Outline (DB), Shrink Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT3388 provides ten bits of high-speed TTL-compatible bus switching or exchanging with bus hold on all I/Os. The low on-state resistance of the switch allows connection to be made with minimal propagation delay. When the switch is turned off, the bus-hold circuit pulls all I/Os to V_{CC} or to GND, depending on the last-known state of the pin. The bus-hold feature holds unused buses in a known TTL state, away from threshold. The bus-hold circuit can hold the bus in the last-known state as long as its leakage does not exceed 100 μA. If the leakage on the bus exceeds this value, the bus hold switches states. The bus-hold feature is active only when the SN74CBT3388 I/Os are in the high-impedance state.

The device operates as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when $\overline{BE}$ is low. The switches are open when BX is high.

The SN74CBT3388 is characterized for operation from –40°C to 85°C.

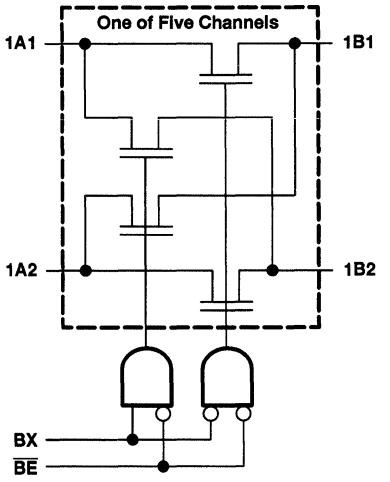
FUNCTION TABLE

$\overline{BE}$	BX	1A1–5A1	1A2–5A2
L	L	1B1–5B1	1B2–5B2
L	H	1B2–5B2	1B1–5B1
H	X	Z	Z

PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} to V_{DD} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
$I_{I(hold)}$		V_{CC} = 4.5 V,	V_I = 2 V or 0.8 V		100		500	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{BE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.5 V,	V_I = 0,	I_I = 64 mA		5	7	Ω
		V_{CC} = 4.5 V,	V_I = 0,	I_I = 30 mA		5	7	
		V_{CC} = 4.5 V,	V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two terminals.

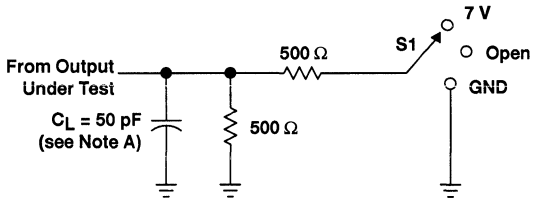
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

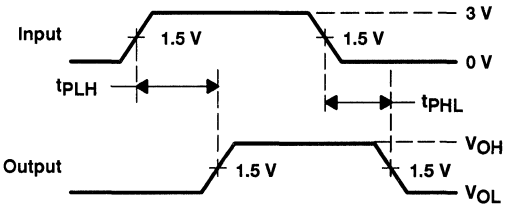
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

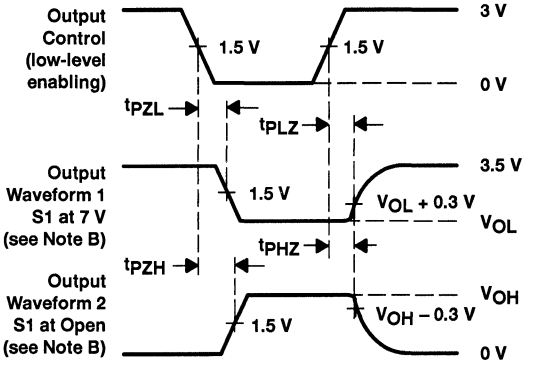


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



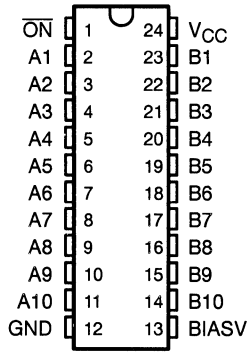
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **Near-Zero Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Package Options Include Plastic Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

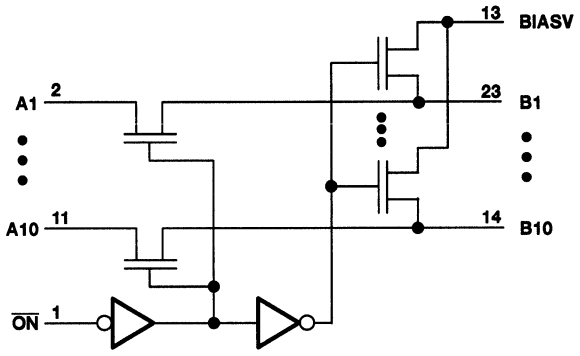
The SN74CBT6800 is organized as one 10-bit switch with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

The SN74CBT6800 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Bias voltage range, BIASV ..... −0.5 V 6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.7 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_O		V_{CC} = 4.5 V,	BIASV = 2.4 V,	V_O = 0	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	mA
ΔI_{CC}‡		V_{CC} = 3.6 V,	One input at 2.7 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3.5		pF
$C_{o(OFF)}$		V_O = 3 V or 0,	Switch off			4.5		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 30 mA		5	7	
			V_I = 0,	I_I = 64 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

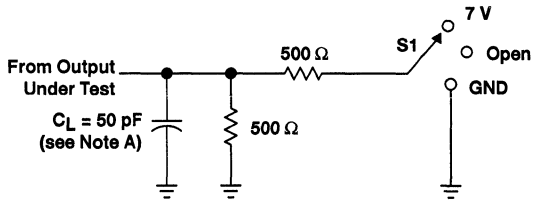
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{PZH}#	$\overline{ON}$	A or B	3.1	8.1		9.1	ns
t_{PZL}‖			3.6	8.6		9.6	
t_{PHZ}#	$\overline{ON}$	A or B	2.7	6.1		5.9	ns
t_{PLZ}‖			3	7.3		6.4	

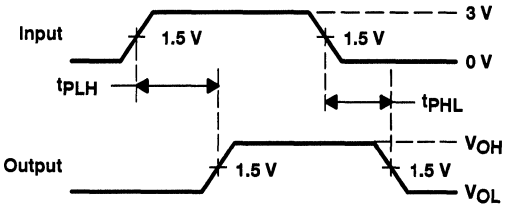
¶ This parameter is characterized but not tested. This propagation delay is due to the RC time constant of the on-state resistance of the switch and the load capacitance.
# BIASV = GND
‖ BIASV = 3 V

PARAMETER MEASUREMENT INFORMATION

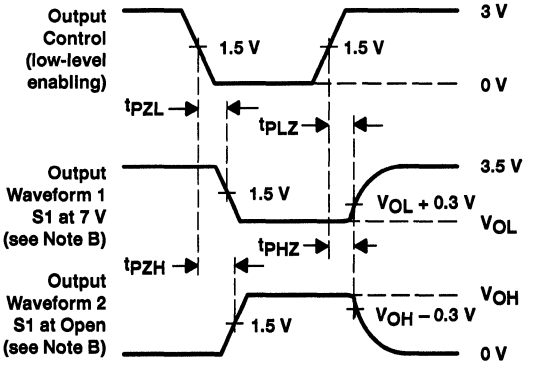


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

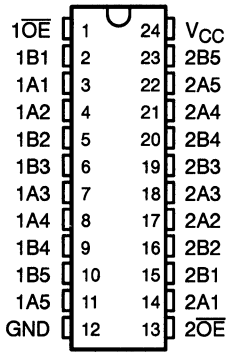
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

Contents

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Designed to Be Used in Level-Shifting Applications**
- **Package Options Include Plastic Small-Outline (DB), Shrink Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTD3384 provides ten bits of high-speed TTL-compatible bus switching with a diode to V_{CC}. The diode enables the bus switch to be used for level translation between a 5-V system and a 3.3-V system with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

The SN74CBTD3384 is characterized for operation from −40°C to 85°C.

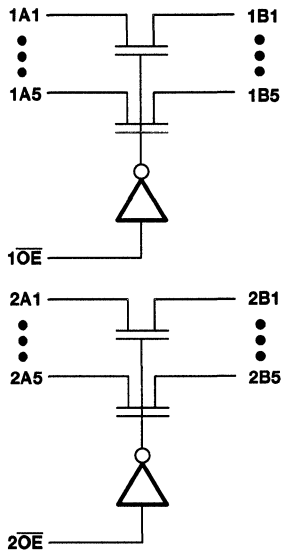
FUNCTION TABLE

$1\overline{OE}$	$2\overline{OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

ADVANCE INFORMATION

ADVANCE INFORMATION

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_I = V_{CC}					V
		V_{CC} = 5 V,	V_I = V_{CC}					
		V_{CC} = 5.5 V,	V_I = V_{CC}					
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V		250		mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

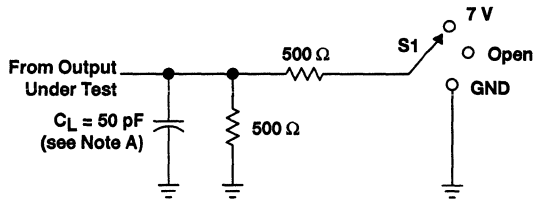
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B			ns
t_{dis}	$\overline{OE}$	A or B			ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

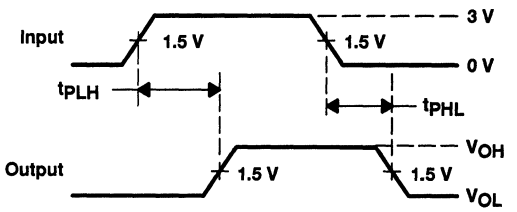
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

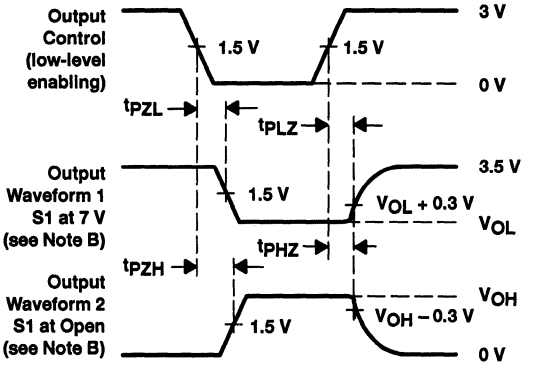


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



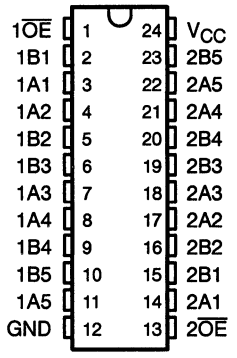
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Functionally Equivalent to QS3384**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Small-Outline (DB), Shrink Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTS3384 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoot. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit bus switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports.

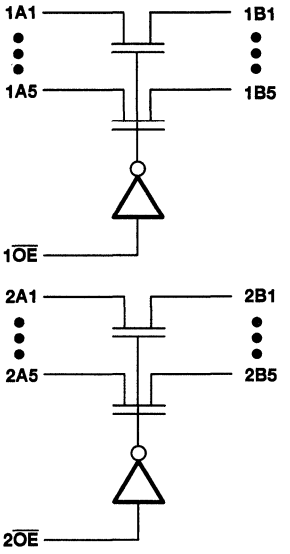
The SN74CBTS3384 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

$1\overline{OE}$	$2\overline{OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

ADVANCE INFORMATION

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.3 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package ..... 0.6 W
DW package ..... 1.6 W
PW package ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

ADVANCE INFORMATION

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA					V
I_I	I_{IL}	V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
	I_{IH}	V_{CC} = 5.5 V,	V_I = 5.5 V or GND					μA
I_{OS}		V_{CC} = 4.5 V,	$V_{I(A)}$ = 0,	$V_{I(B)}$ = 4.5 V		250		mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0						pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}					pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA (optional)		5	7	Ω
			V_I = 0,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

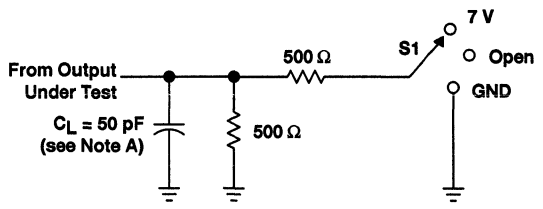
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B			ns
t_{dis}	$\overline{OE}$	A or B			ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

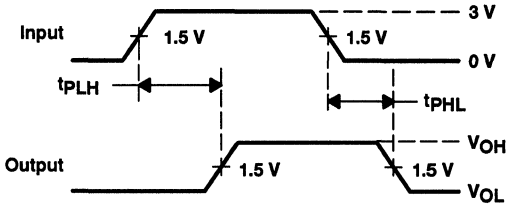
ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

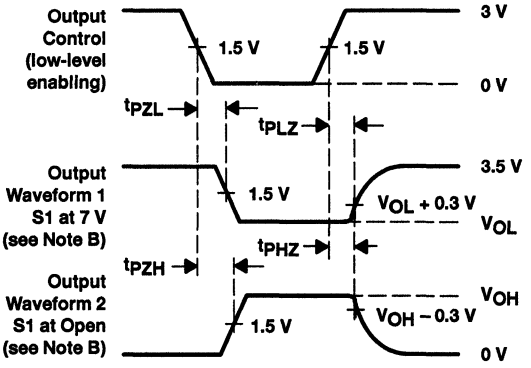


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

Contents

SCDS006D – NOVEMBER 1992 – REVISED MAY 1995

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG), 300-mil Shrink Small-Outline (DL), and 380-mil Fine-Pitch Ceramic Flat (WD) Packages**

description

The 'CBT16209 provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

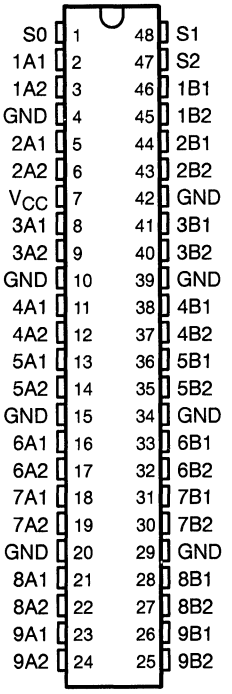
The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN54CBT16209 is characterized for operation form –55°C to 125°C. The SN74CBT16209 is characterized for operation from –40°C to 85°C.

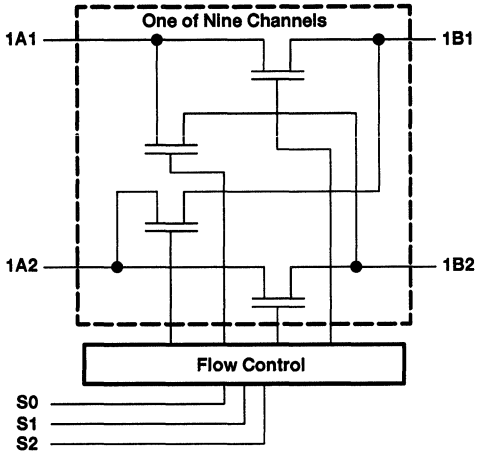
FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

SN54CBT16209 . . . WD PACKAGE
SN74CBT16209 . . . DGG OR DL PACKAGE
(TOP VIEW)



logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		SN54CBT16209		SN74CBT16209		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4	5.5	4	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, or S2 = V_{CC}			7.5		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	8	Ω
				I_I = 30 mA		4	8	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

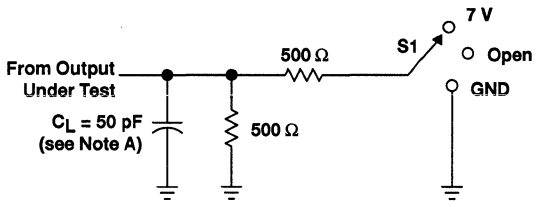
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16209				SN74CBT16209				UNIT
			V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.8				0.25		0.25	ns
t_{pd}	S		2	13.1		14	2.6	10.2		11.3	
t_{en}	S	A or B	1.7	15.3		16	2.7	10.6		11.5	ns
t_{dis}	S	A or B	1	13.2		14.5	1.2	11.3		12.1	ns

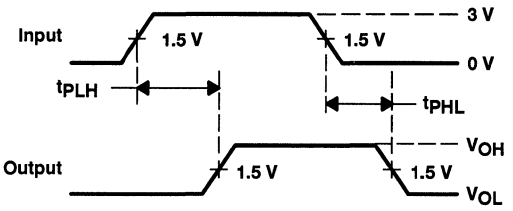
¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

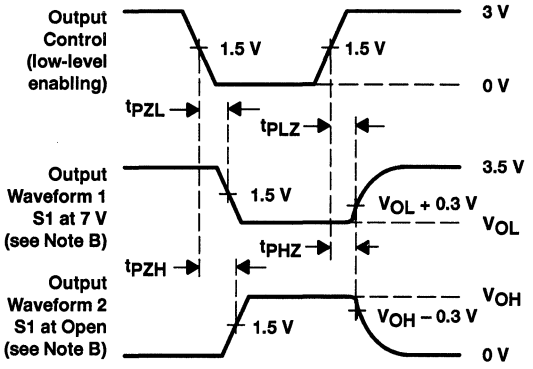


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS028 – JULY 1995

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Packaged in Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16211 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

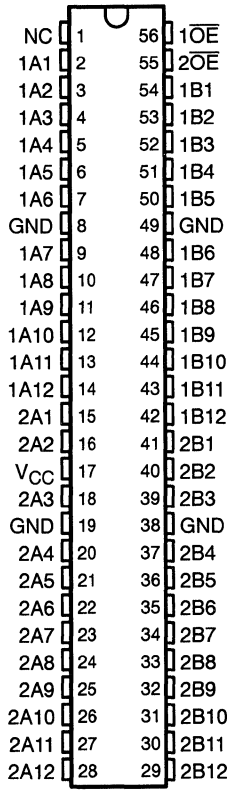
The device operates as a 12- or 24-bit bus exchange switch. When $1\overline{OE}$ is low, 1A is connected to 1B. When $2\overline{OE}$ is low, 2A is connected to 2B.

The SN74CBT16211 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

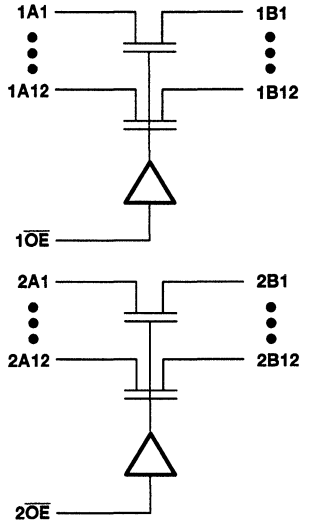
$1\overline{OE}$	$2\overline{OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0 V,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}‡		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			6		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		5	6	Ω
			V_I = 2.4 V,	I_I = 15 mA			12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

PRODUCT PREVIEW

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

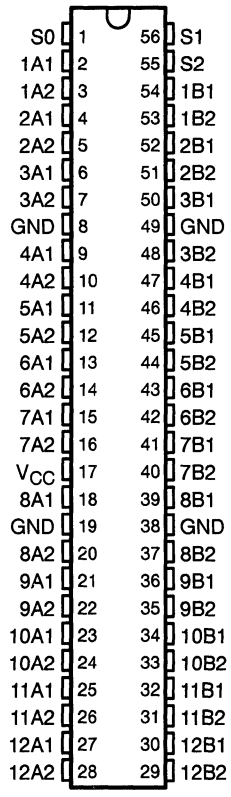
The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBT16212 is characterized for operation from –40°C to 85°C.

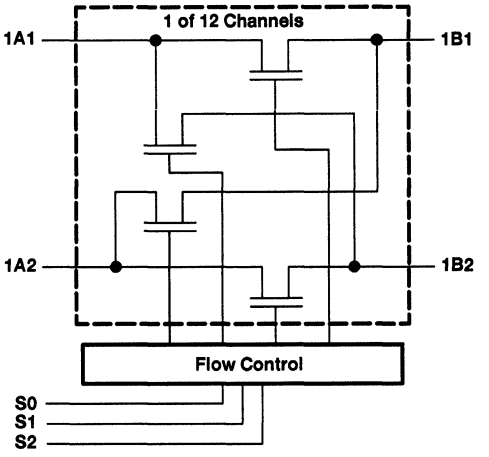
FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

DGG OR DL PACKAGE
(TOP VIEW)



logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	μA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, or S2 = V_{CC}			7.5		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	7	Ω
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

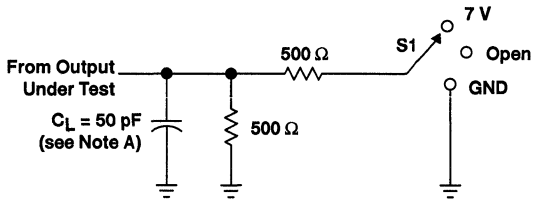
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{pd}	S		2.6	10.2		11.3	
t_{en}	S	A or B	2.7	10.6		11.5	ns
t_{dis}	S	A or B	1.2	11.3		12.1	ns

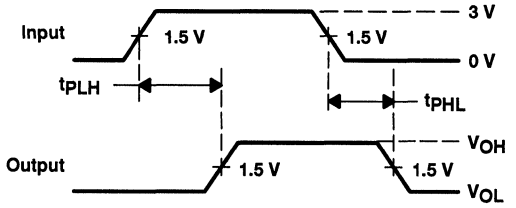
¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

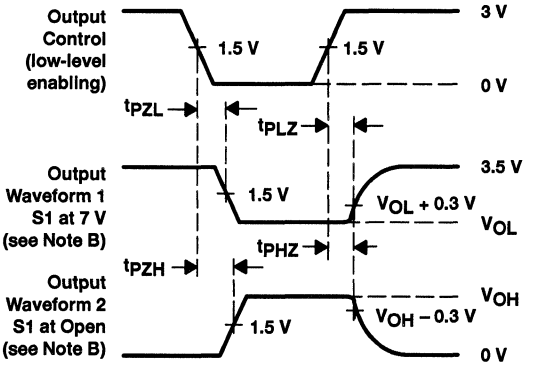


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16213 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

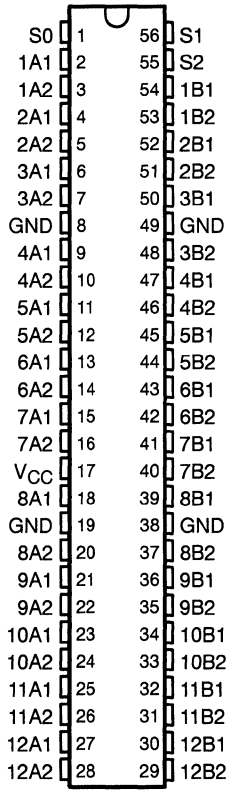
The device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The SN74CBT16213 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

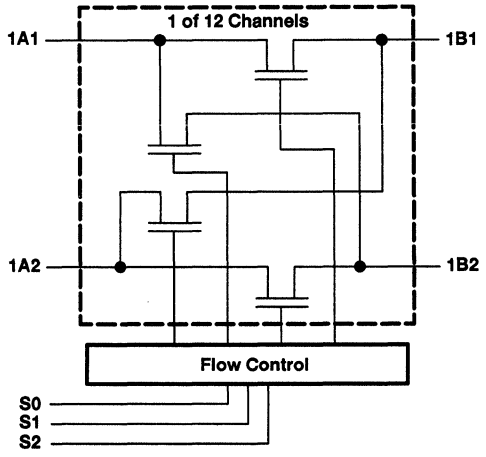
S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 to B1
L	H	L	B2	Z	A1 to B2
L	H	H	Z	B1	A2 to B1
H	L	L	Z	B2	A2 to B2
H	L	H	A2 and B2	Z	A1 to A2 and B2
H	H	L	B1	B2	A1 to B1, A2 to B2
H	H	H	B2	B1	A1 to B2, A2 to B1

DGG OR DL PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S0, S1, or S2 = V_{CC}			7.5		pF
r_{on}§	A to B	V_{CC} = 4 V	V_I = 0	I_I = 30 mA				Ω
				I_I = 64 mA				
			V_I = 2.4	I_I = 15 mA				
		V_{CC} = 4.5 V	V_I = 0	I_I = 30 mA		4	7	
				I_I = 64 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	
	A1 to A2	V_{CC} = 4 V	V_I = 0	I_I = 30 mA				Ω
				I_I = 64 mA				
			V_I = 2.4 V,	I_I = 15 mA				
		V_{CC} = 4.5 V	V_I = 0	I_I = 30 mA				
				I_I = 64 mA				
			V_I = 2.4 V,	I_I = 15 mA				

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

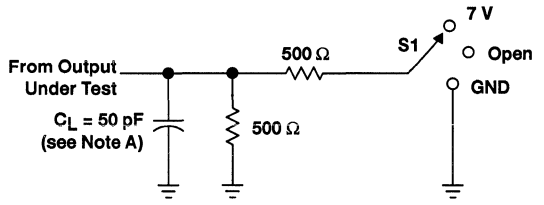
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t_{pd}¶	A or B	B or A		0.25	ns
t_{pd}	A1	A2			
	S	B or A			
t_{en}	S	A or B			ns
t_{dis}	S	A or B			ns

¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

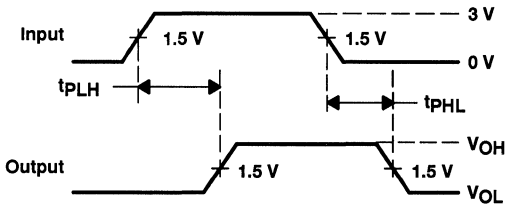
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

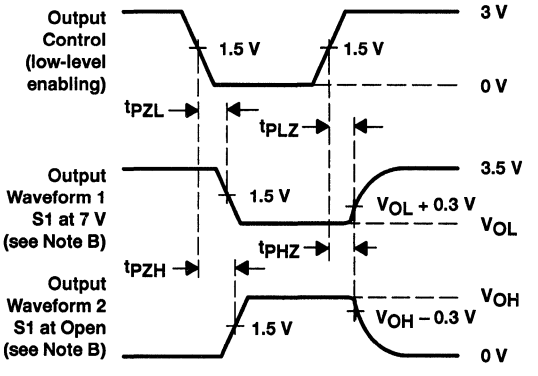


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

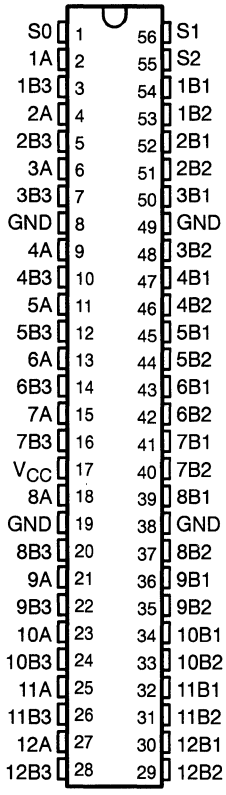
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74CBT16214 provides 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

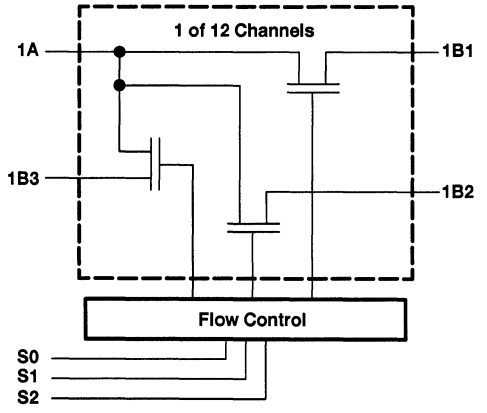
The SN74CBT16214 operates as a 12-bit bus-select switch via the data-select (S0–S2) terminals.

The SN74CBT16214 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S2	S1	S0	A	FUNCTION
L	L	L	Z	Disconnect
L	L	H	B1	A to B1
L	H	L	B2	A to B2
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A to B3
H	H	L	B1	A to B1
H	H	H	B2	A to B2

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}§		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control pins	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	A = Z			7.5		pF
r_{on}¶		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA		4	7	Ω
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

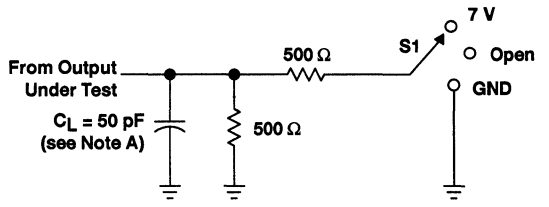
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.25		0.25	ns
t_{pd}	S		5.5	13.9		15.3	
t_{en}	S	A or B	5.1	14.5		16	ns
t_{dis}	S	A or B	3.6	11.7		12.1	ns

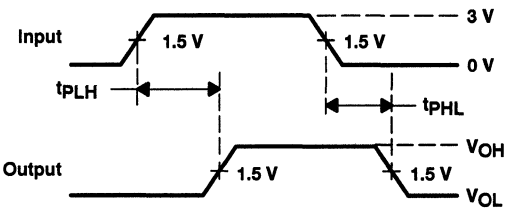
† This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

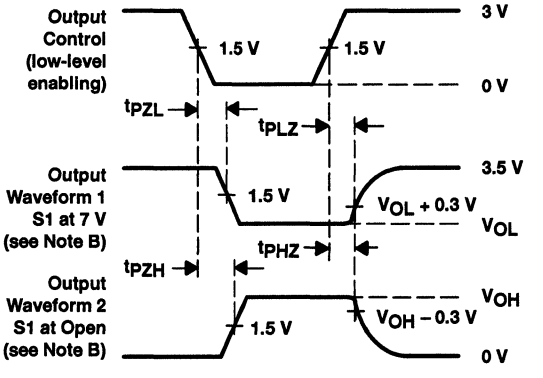


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS009 – MAY 1995

- **5-Ω Switch Connection Between Two Ports**
- **0.25-ns Maximum Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16232 is a 16-bit to 32-bit synchronous switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

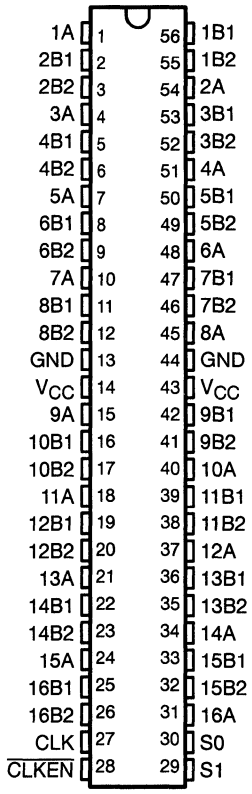
Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

The SN74CBT16232 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

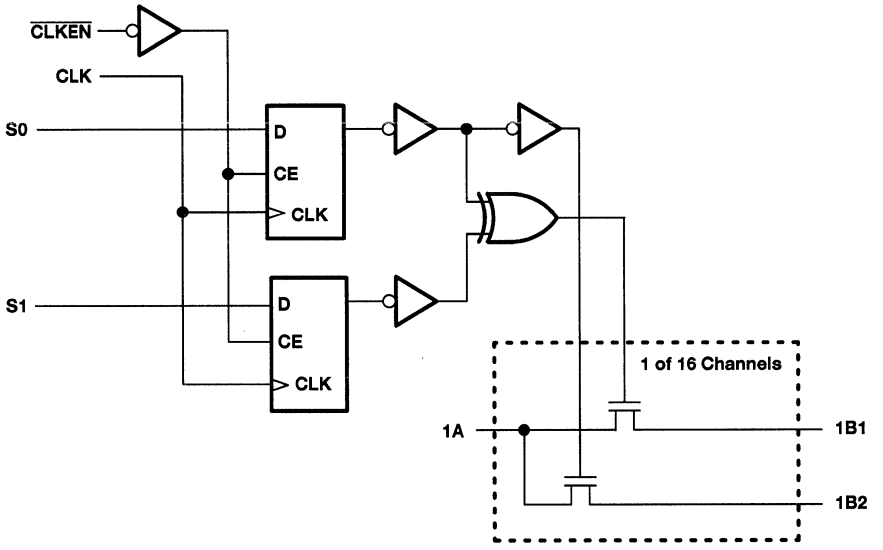
S1	S0	CLK	$\overline{\text{CLKEN}}$	FUNCTION
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A to B1 and A to B2
H	L	↑	L	A to B1 or B1 to A
H	H	↑	L	A to B2 or B2 to A

DGG OR DL PACKAGE
(TOP VIEW)



ADVANCE INFORMATION

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Maximum power package dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4		5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	– 40		85	°C

ADVANCE INFORMATION

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_I	Control pins	V_I = 3 V or 0				4.5		pF
C_{ioOFF}		V_O = 3 V or 0				4		pF
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA				Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA				
			V_I = 0,	I_I = 32 mA				
			V_I = 2.4 V,	I_I = 15 mA				

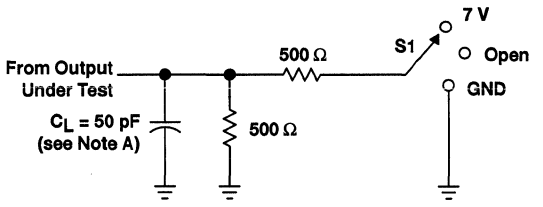
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{pd}¶	A or B	B or A			0.25	ns
t_{en}	CLK	B or A				ns
t_{dis}	CLK	B or A				ns

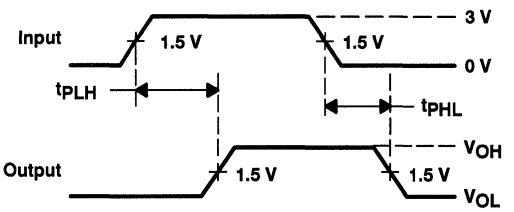
¶ This parameter is characterized but not tested. This propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF.

PARAMETER MEASUREMENT INFORMATION

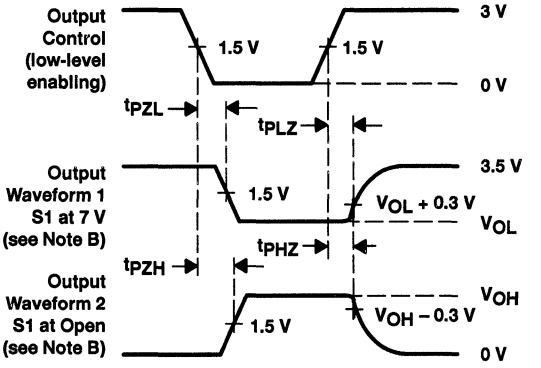


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

ADVANCE INFORMATION

- **5-Ω Switch Connection Between Two Ports**
- **0.25-ns Maximum Propagation Delay**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16233 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The SN74CBT16233 can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select inputs (SEL0 and SEL1) control the data flow. When the TEST inputs are asserted, the A port is connected to both the 1B and the 2B ports. SEL0, SEL1, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

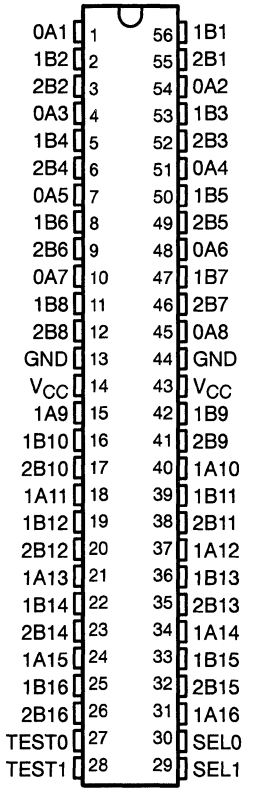
The SN74CBT16233 is specified by design not to have through current when switching directions.

The SN74CBT16233 is characterized for operation from 0°C to 70°C.

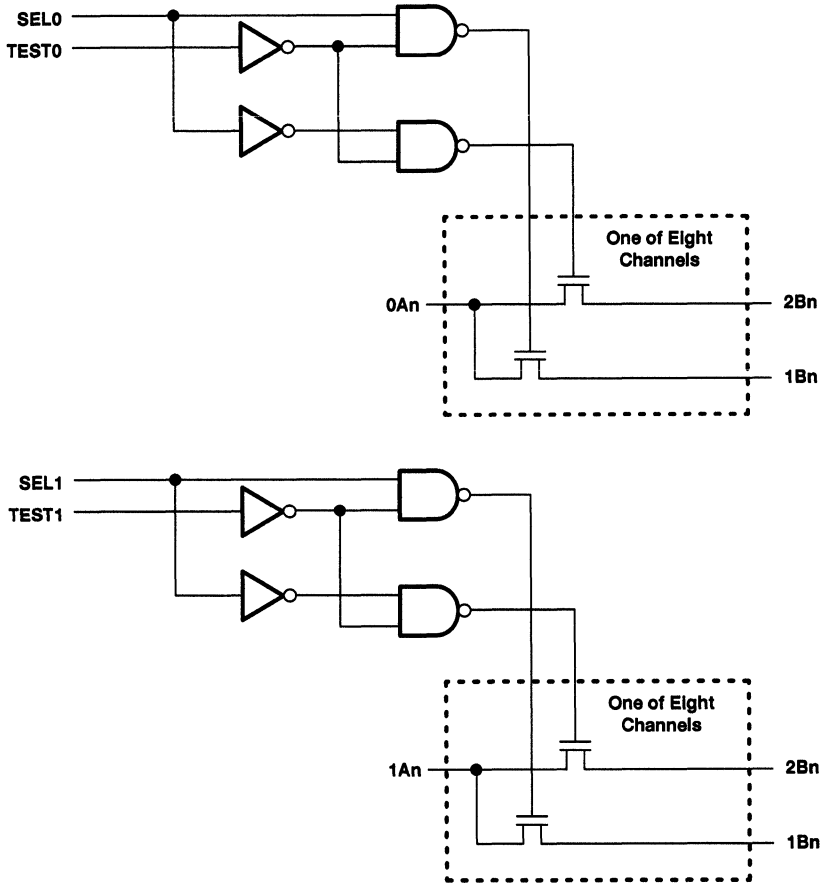
FUNCTION TABLE

SEL0,1	TEST 0,1	FUNCTION
L	L	A to 1B or 1B to A
H	L	A to 2B or 2B to A
X	H	A to 1B and A to 2B

DGG OR DL PACKAGE
(TOP VIEW)



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Continuous channel current ..... 128 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Maximum power package dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75		5.25	V
V_{IH}	High-level control input voltage	2			V
V_{IL}	Low-level control input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 0	V_I = 5.25 V				10	µA
		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±1	µA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡		V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_I	Control pins	V_I = 3 V or 0				4.5		pF
C_{OFF}		V_O = 3 V or 0				4		pF
r_{on}§		V_{CC} = 4.75 V,	V_I = 0,	I_I = 12 mA		5	7	Ω
		V_{CC} = 4.75 V,	V_I = 2.4 V,	I_I = 8 mA		10	15	Ω

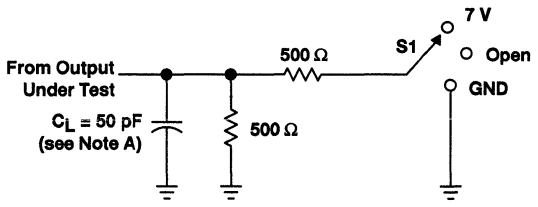
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A, B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 0°C to 70°C			UNIT
			MIN	TYP†	MAX	
t_{pd}¶	A or B	B or A			0.25	ns
t_{pd}	SEL0, SEL1	A	1.6	3.6	5.3	ns
t_{en}	TEST0, TEST1 OR SEL0, SEL1	B	1.3	3.6	5.2	ns
t_{dis}			0.5	3.9	5.3	

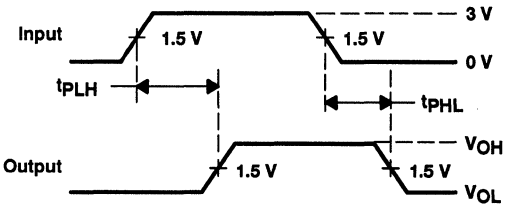
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ This parameter is characterized but not tested. This propagation delay is due to the RC time constant of the typical on-state resistance of the switch and a 50-pF load capacitance.

PARAMETER MEASUREMENT INFORMATION

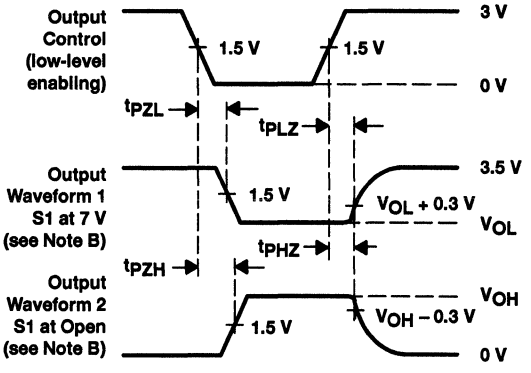


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

5 Application Note

Texas Instruments Crossbar Switches

Ramzi Ammar
Advanced System Logic – Semiconductor Group

SCDA001A

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Illustrations

What Are Texas Instruments Crossbar Switches?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an N-channel MOS transistor driven by a CMOS gate. When enabled, the N-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on-state resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈ 1 V less than the gate potential, regardless of the level at the input pin. This is one of the N-channel transistor characteristics (see Figures 1 and 2). Note the ≈ 1-V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

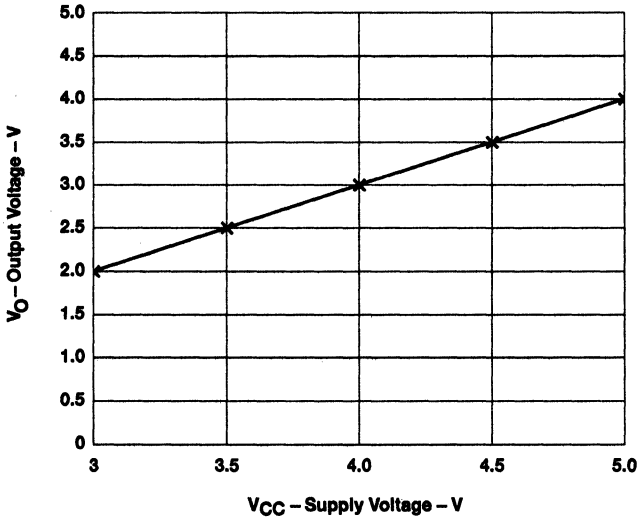


Figure 1. Output Voltage Versus Supply Voltage

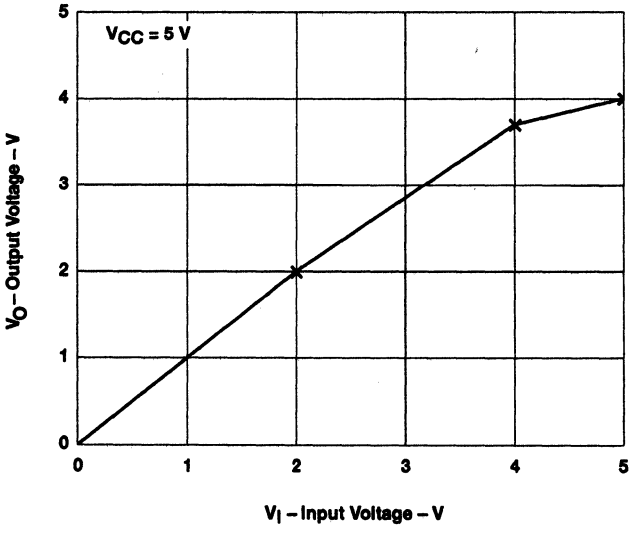


Figure 2. Output Voltage Versus Input Voltage

The on-state resistance (r_{on}) increases gradually with V_I until V_I approaches $V_{CC} - 1$ V, where r_{on} rapidly increases, clamping V_O at $V_{CC} - 1$ V (see Figure 3). Also, by the nature of the N-channel transistor design, the input and output terminals are fully isolated when the transistor is off. Leakage and capacitance are to ground and not between input and output, which minimizes feedthrough when the transistor is off.

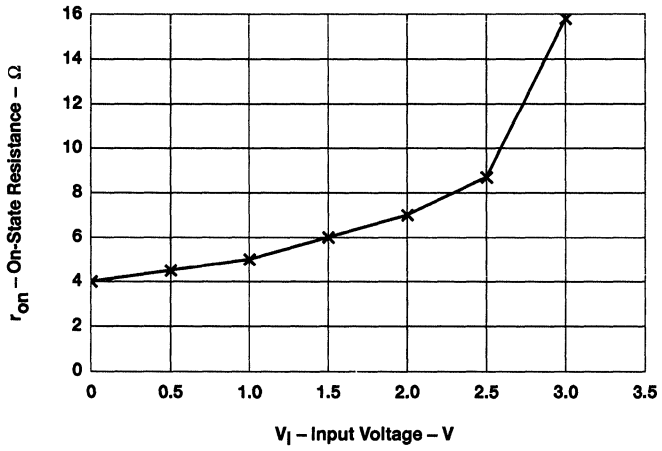


Figure 3. On-State Resistance Versus Input Voltage

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices also can provide bidirectional 5-V to 3-V translation with minimal propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes gate voltage of 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

These devices consume very little current (I_{CC} = 3 μA). This current is not satisfactory for the diode to operate. Using a resistor from the cathode of the diode to GND allows more current from the supply voltage, causing the diode to operate and to clamp at the specified 4.3 V (see Figure 4). The recommended value of the resistor is 1 KΩ or less.

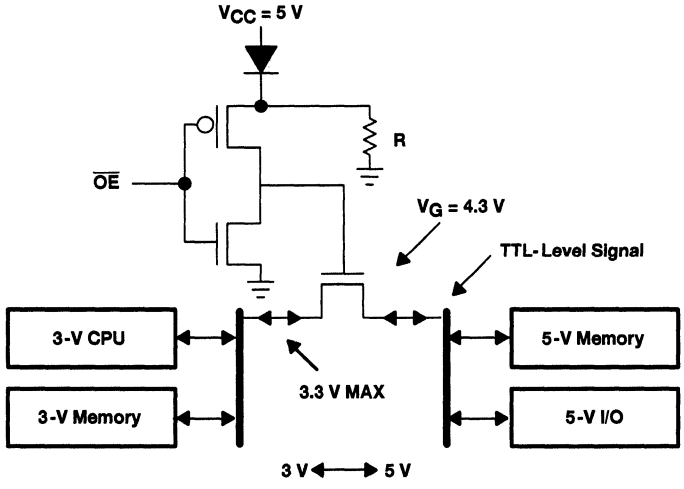


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems in which signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices also can replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on-state resistance and without relay-reliability problems.

Bus Switches Convert TTL Logic to Hot-Card Insertion Capability

This application is used mostly in systems that require hot-card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and cannot be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., which do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first, followed by the signal pins, then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance cannot be achieved using CMOS logic since it contains P-channel transistors that provide an inherent diode between the I/O pins and V_{CC}. The diode is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground, leaving the bus disturbed.

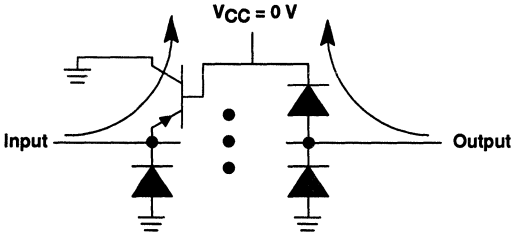


Figure 5. ACL Direction of Current Flow When V_{CC} = 0 V

Another issue to consider is that, when V_{CC} is ramping but still below the device-operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error does not occur.

There are two solutions to this problem; one is to use Texas Instruments BiCMOS technology (BCT) or advanced BiCMOS technology (ABT) families, since both ensure the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down.

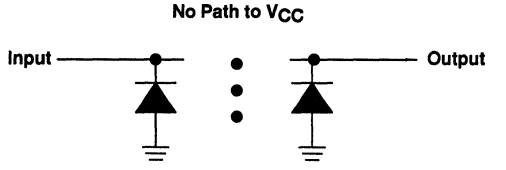


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments CBT family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot-card insertion. It has a built-in channel pullup tied to a bias voltage (BIASV) that is provided to ensure power up with the buses not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

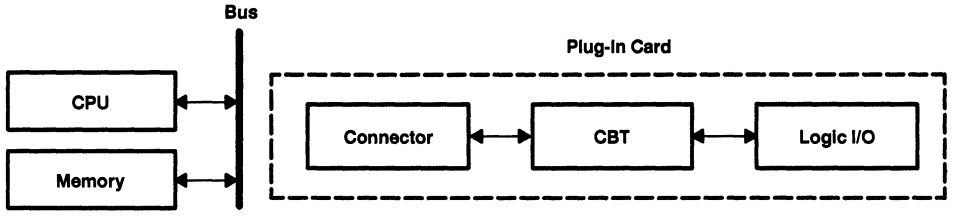
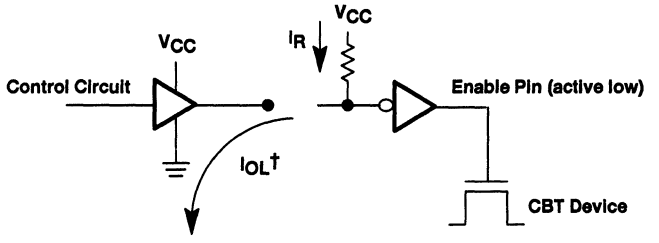


Figure 7. Hot-Card Insertion Application



† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple N-channel transistors, they are capable of providing several important bus functions, such as hot-card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

EXAMPLE: SN 74CBT3245 PW LE

Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN = Standard prefix
SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SIX TO TWELVE CHARACTERS

Examples: 74CBT3125
74CBT16233

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DB, DL = plastic shrink small-outline package
DGG, PW = plastic thin shrink small-outline package
JT = ceramic dual-in-line package
W, WD = ceramic flat package
(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

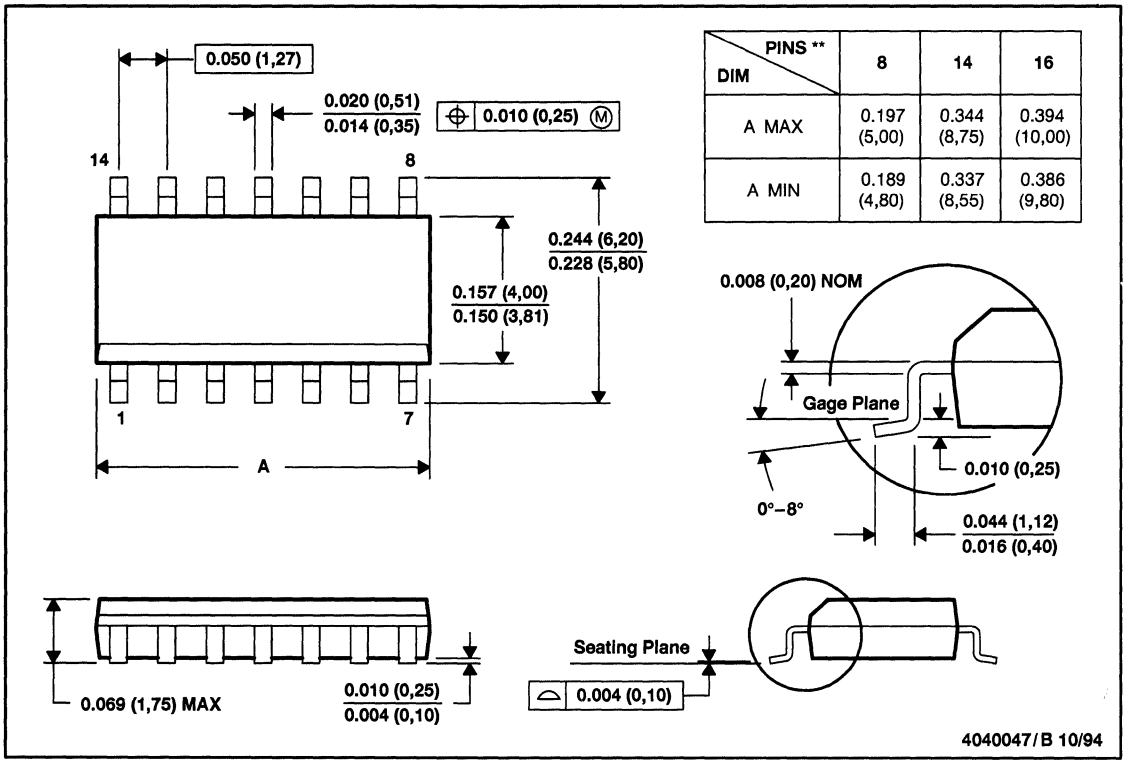
Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE TO TWO LETTERS

LE = Left-embossed tape and reel (required for DB and PW packages)
R = Standard tape and reel (required for DGG; optional for D, DW, and DL packages)

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

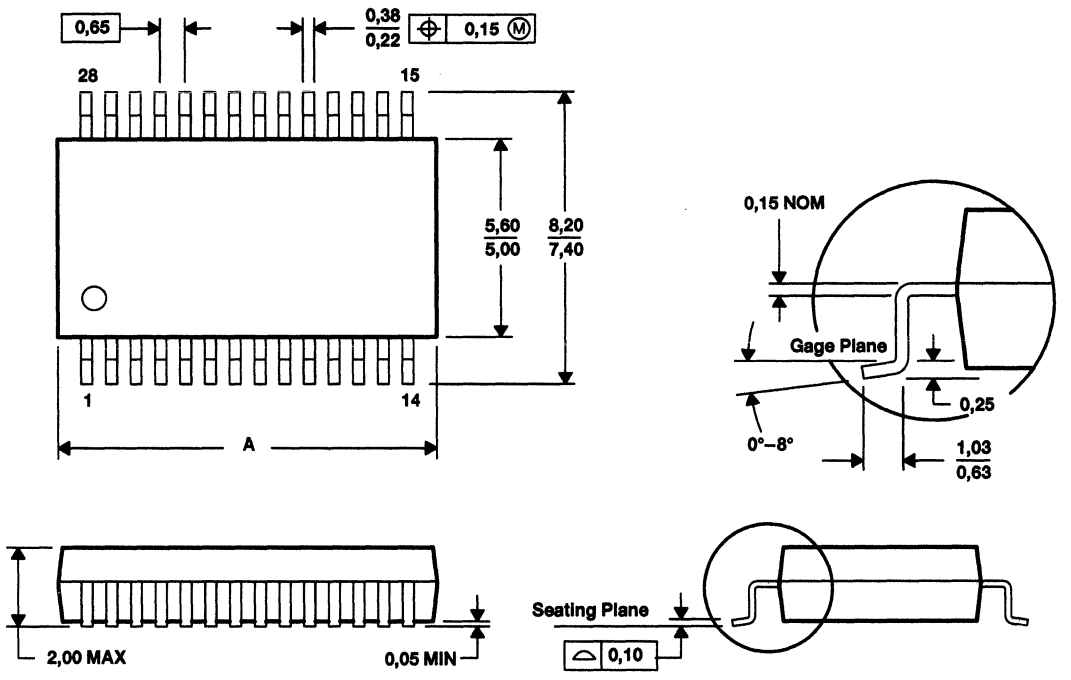


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



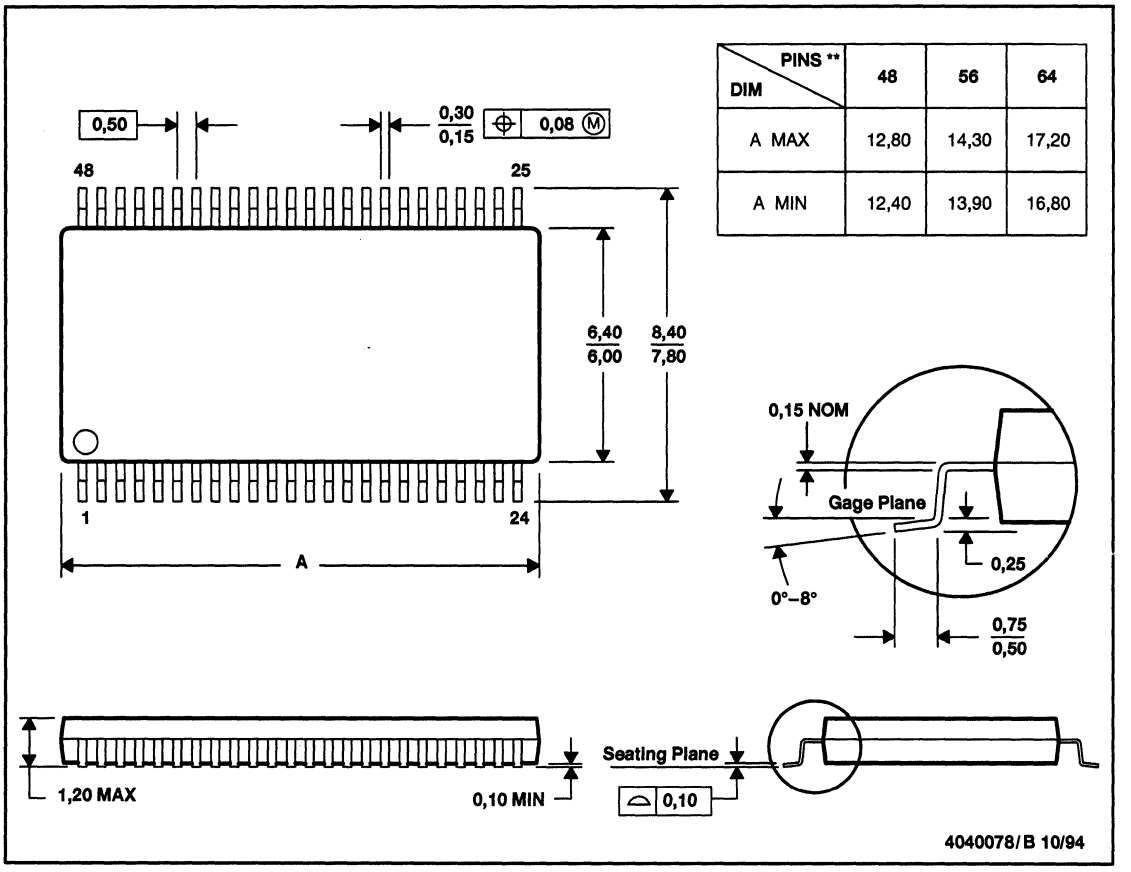
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

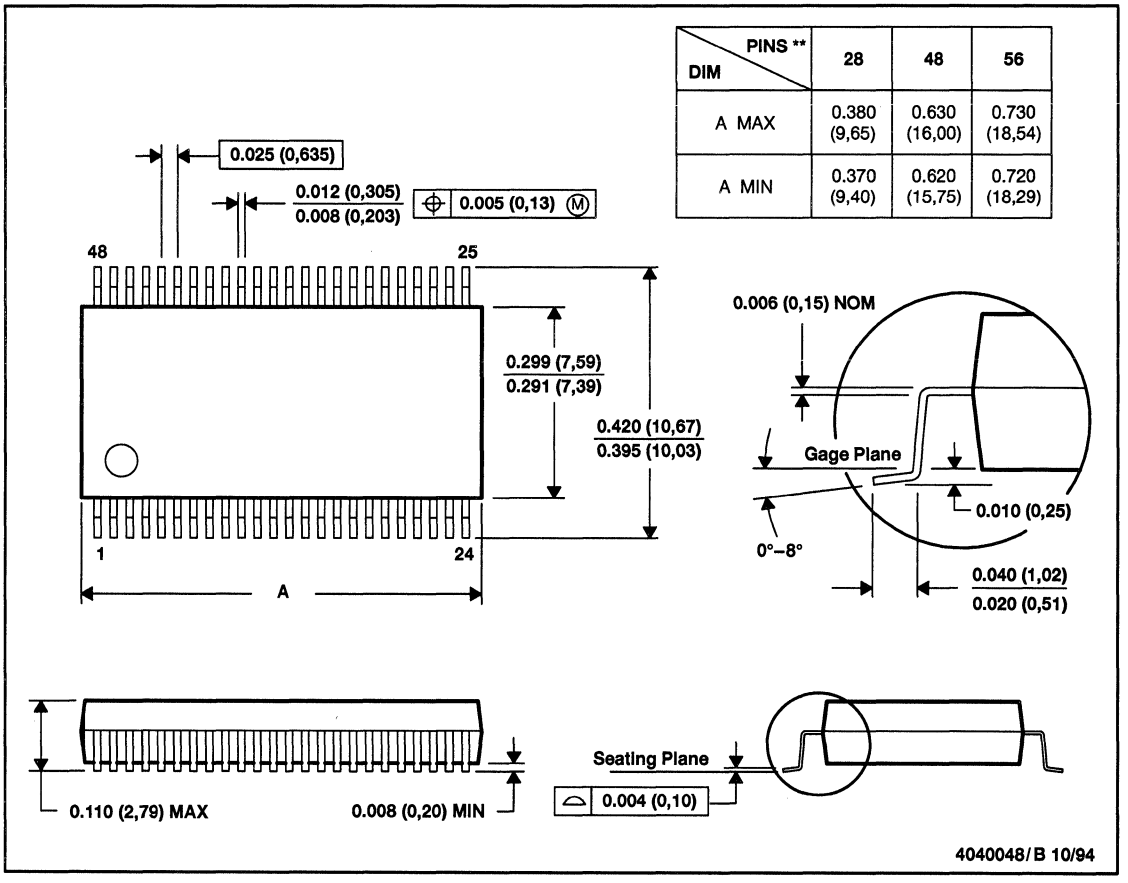


DIM \ PINS **	48	56	64
A MAX	12,80	14,30	17,20
A MIN	12,40	13,90	16,80

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

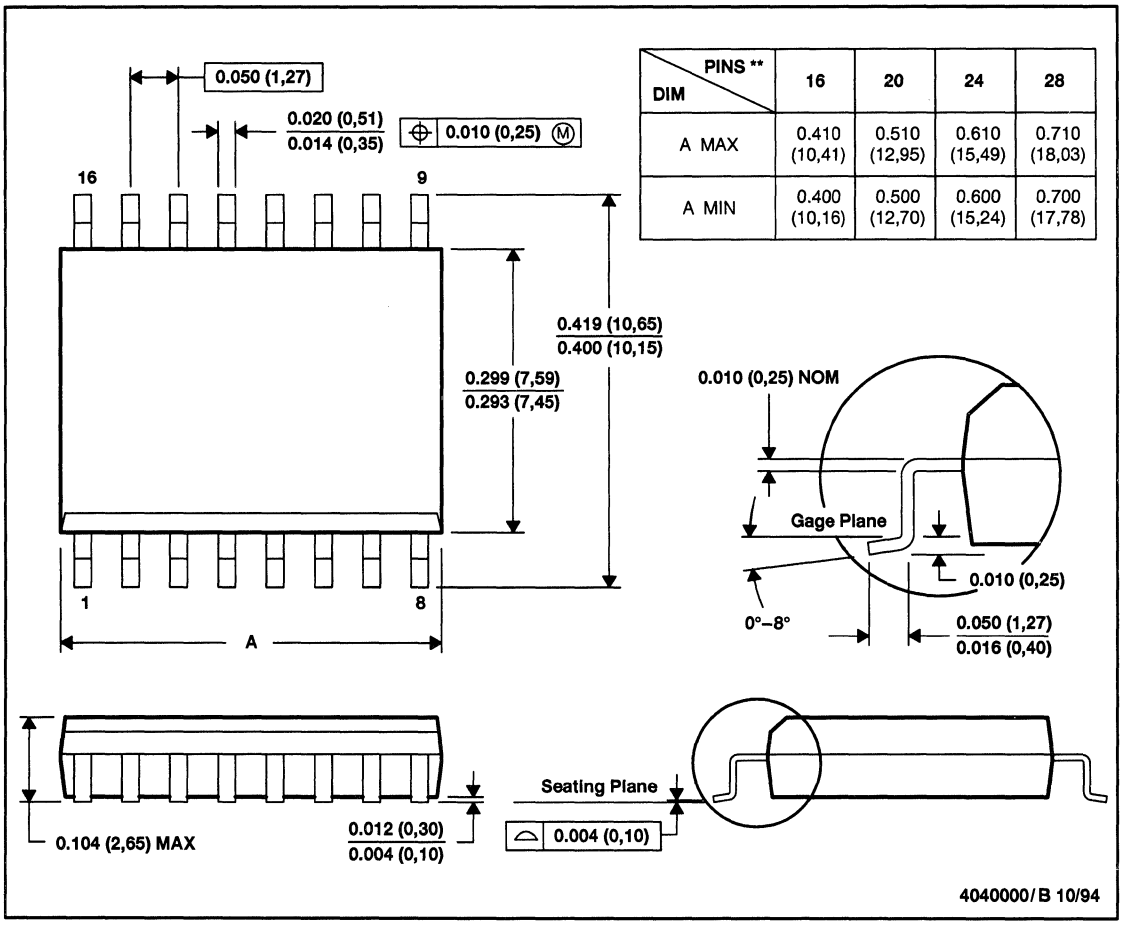
48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN

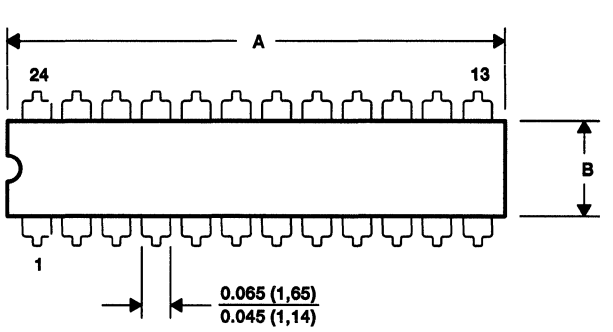


DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

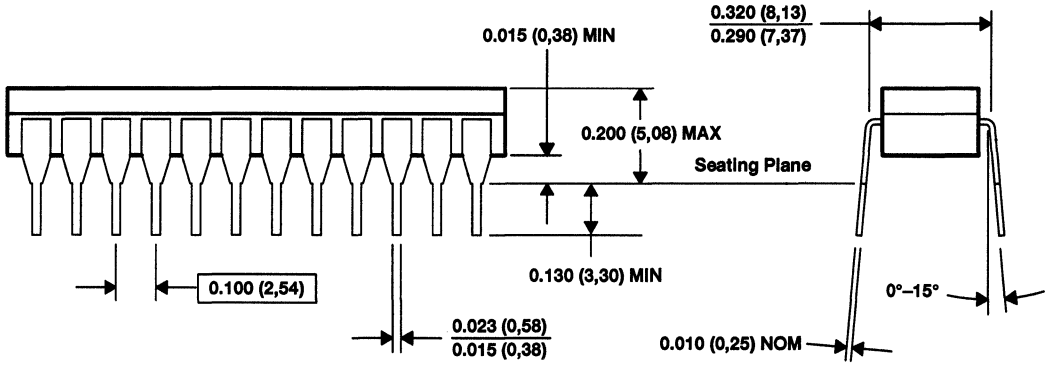
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS**	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

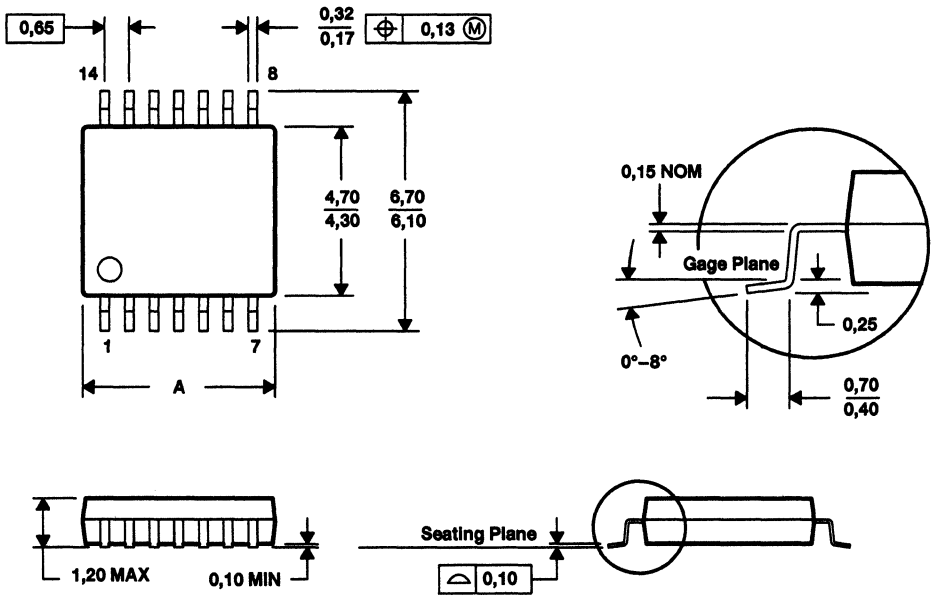


4040110/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

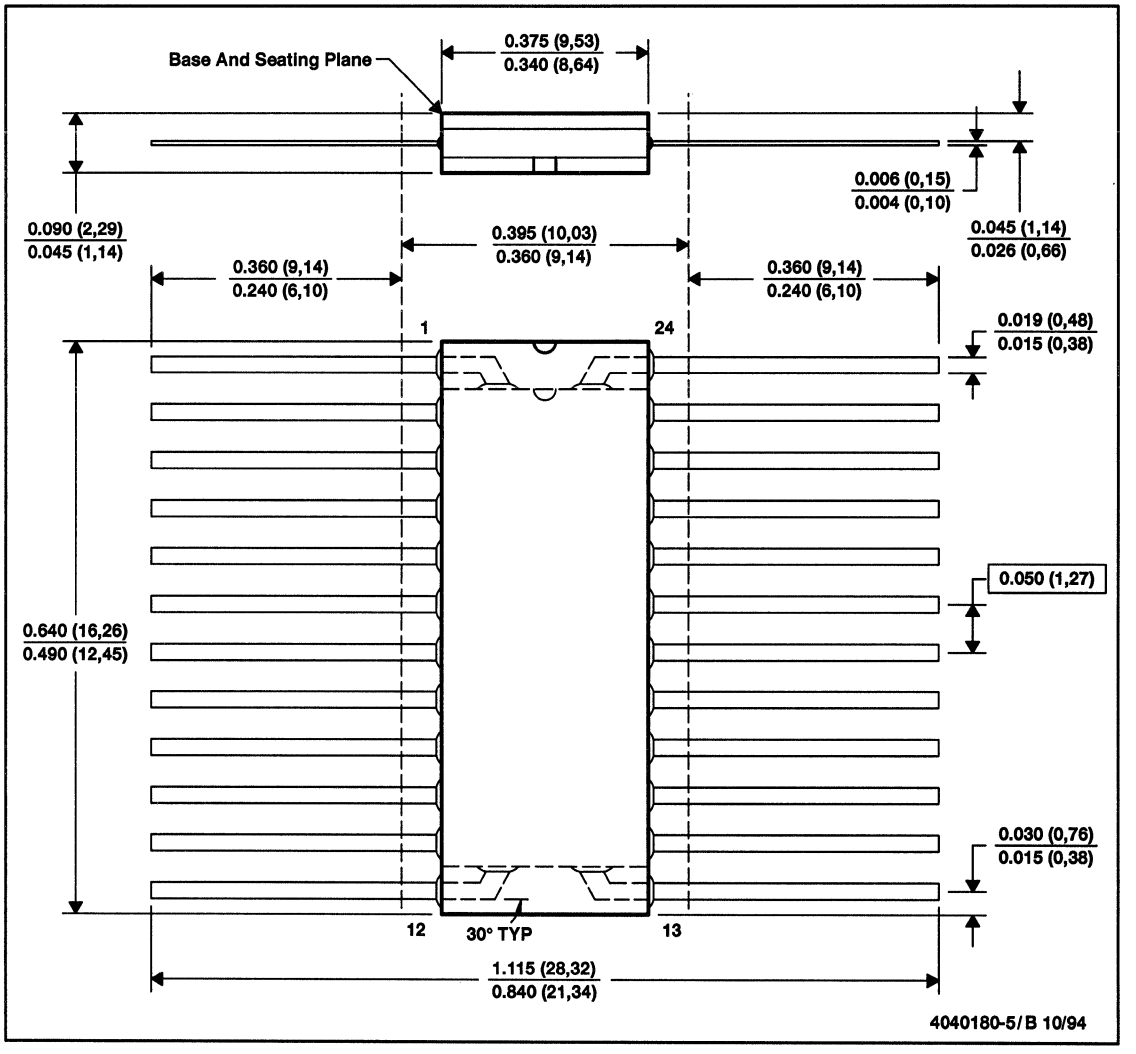


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

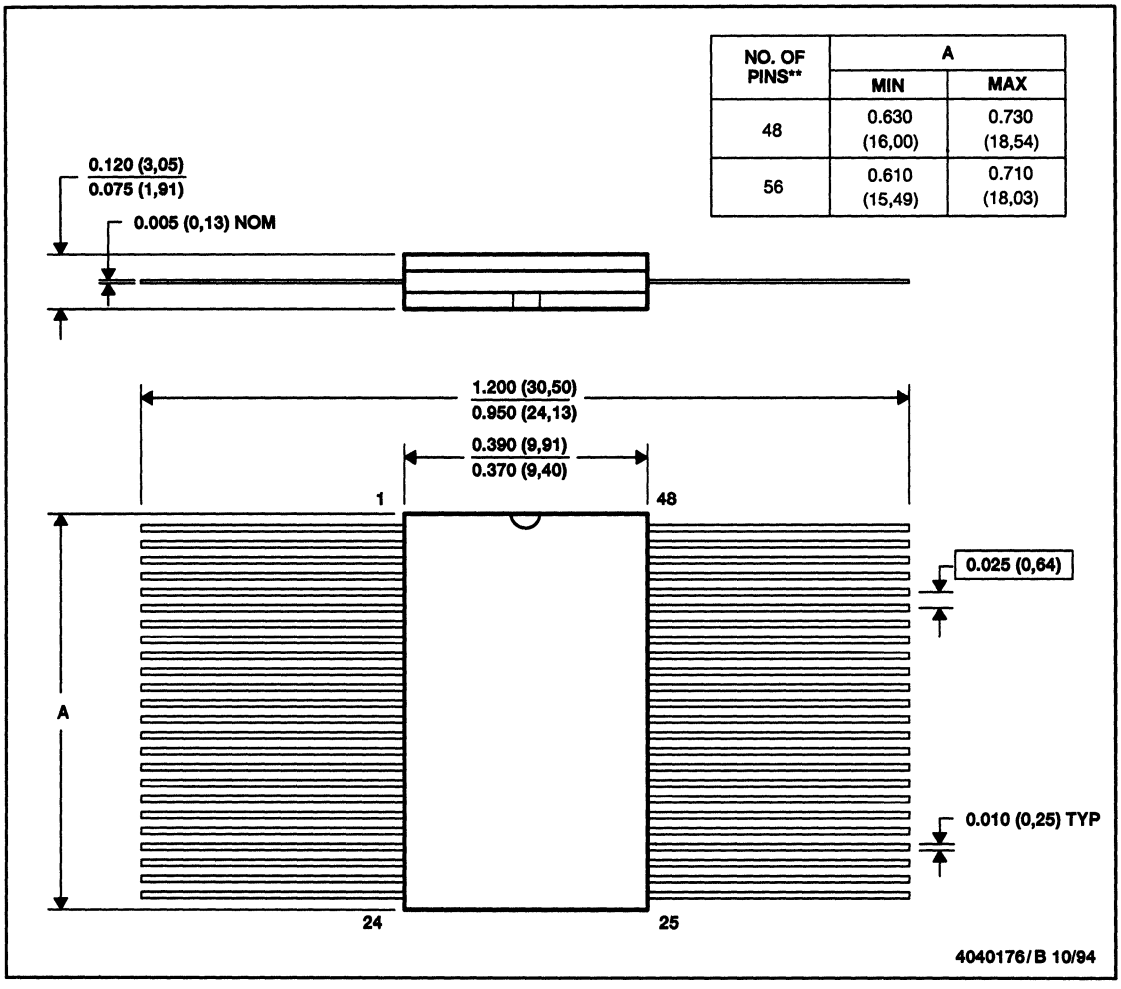
W (R-GDFP-F24) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
E. Index point is provided on cap for terminal identification only.

WD (R-GDFP-F)** **CERAMIC DUAL FLATPACK**

48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only.
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

NOTES

TI Worldwide Sales and Representative Offices

AUSTRALIA / NEW ZEALAND: Texas Instruments Australia Ltd.: Sydney [61] 2-910-3100, Fax 2-805-1186; **Melbourne** 3-696-1211, Fax 3-696-4446.
BELGIUM: Texas Instruments Belgium S.A./N.V.: Brussels [32] (02) 726-75-80, Fax (02) 726 72 76.
BRAZIL: Texas Instrumentos Electronicos do Brasil Ltda.: Sao Paulo [55] 11-535-5133.
CANADA: Texas Instruments Canada Ltd.: Montreal (514) 335-8392; **Ottawa** (613) 726-3201; **Toronto** (416) 884-9181.
DENMARK: Texas Instruments A/S: Ballerup [45] (44) 68 74 00.
FINLAND: Texas Instruments/OY: Espoo [358] (0) 43 54 20 33, Fax (0) 46 73 23.
FRANCE: Texas Instruments France: Velizy-Villacoublay Cedex [33] (1) 30 70 10 01, Fax (1) 30 70 10 54.
GERMANY: Texas Instruments Deutschland GmbH.: Freising [49] (08161) 80-0, Fax (08161) 80 45 16; **Hannover** (0511) 90 49 60, Fax (0511) 64 90 331; **Ostfildern** (0711) 34 03 0, Fax (0711) 34 032 57.
HONG KONG: Texas Instruments Hong Kong Ltd.: Kowloon [852] 2956-7288, Fax 2965-2200.
HUNGARY: Texas Instruments Representation: Budapest [36] (1) 269 8310, Fax (1) 267 1357.
IRELAND: Texas Instruments Ireland Ltd.: Dublin [353] (01) 475 52 33, Fax (01) 478 14 63.
ITALY: Texas Instruments Italia S.p.A.: Agrate Brianza [39] (039) 68 42.1, Fax (039) 68 42.912; **Rome** (06) 657 26 51.
JAPAN: Texas Instruments Japan Ltd.: Tokyo [81] 03-769-8700, Fax 03-3457-6777; **Osaka** 06-204-1881, Fax 06-204-1895; **Nagoya** 052-583-8691, Fax 052-583-8696; **Ishikawa** 0762-23-5471, Fax 0762-23-1583; **Nagano** 0263-33-1060, Fax 0263-35-1025; **Kanagawa** 045-338-1220, Fax 045-338-1255; **Kyoto** 075-341-7713, Fax 075-341-7724; **Saitama** 0485-22-2440, Fax 0425-23-5787; **Oita** 0977-73-1557, Fax 0977-73-1583.
KOREA: Texas Instruments Korea Ltd.: Seoul [82] 2-551-2800, Fax 2-551-2828.
MALAYSIA: Texas Instruments Malaysia Sdn Bhd: Kuala Lumpur [60] 3-208-6001, Fax 3-230-6605.
MEXICO: Texas Instruments de Mexico S.A. de C.V.: Colonia del Valle [52] 5-639-9740.
NORWAY: Texas Instruments Norge A/S: Oslo [47] (02) 264 75 70.
MAINLAND CHINA: Texas Instruments China Inc.: Beijing [86] 1-500-2255, Ext. 3750, Fax 1-500-2705.
PHILIPPINES: Texas Instruments Asia Ltd.: Metro Manila [63] 2-817-6031, Fax 2-817-6096.
PORTUGAL: Texas Instruments Equipamento Electronico (Portugal) LDA.: Maia [351] (2) 948 10 03, Fax (2) 948 19 29.
SINGAPORE (& INDIA, INDONESIA, THAILAND): Texas Instruments Singapore (PTE) Ltd.: Singapore [65] 390-7100, Fax 390-7062.
SPAIN: Texas Instruments España S.A.: Madrid [34] (1) 372 80 51, Fax (1) 372 82 66; **Barcelona** (3) 31 791 80.
SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen): Kista [46] (08) 752 58 00, Fax (08) 751 97 15.
SWITZERLAND: Texas Instruments Switzerland AG: Dietikon [41] 886-2-3771450.
TAIWAN: Texas Instruments Taiwan Limited: Taipei [886] (2) 378-6800, Fax 2-377-2718.
UNITED KINGDOM: Texas Instruments Ltd.: Northampton [44] (0234) 270 111, Fax (0234) 223 459.

UNITED STATES: Texas Instruments Incorporated: ALABAMA: Huntsville (205) 430-0114; **ARIZONA: Phoenix** (602) 224-7800; **CALIFORNIA: Irvine** (714) 660-1200; **San Diego** (619) 278-9600; **San Jose** (408) 894-9000; **Woodland Hills** (818) 704-8100; **COLORADO: Denver** (303) 488-9300; **CONNECTICUT: Wallingford** (203) 265-3807; **FLORIDA: Orlando** (407) 667-5300; **Fort Lauderdale** (305) 425-7820; **Tampa** (813) 882-0017; **GEORGIA: Atlanta** (404) 662-7967; **ILLINOIS: Arlington Heights** (708) 640-2925; **INDIANA: Indianapolis** (317) 573-6400; **KANSAS: Kansas City** (913) 451-4511; **MARYLAND: Columbia** (410) 312-7900; **MASSACHUSETTS: Boston** (617) 895-9100; **MICHIGAN: Detroit** (313) 553-1500; **MINNESOTA: Minneapolis** (612) 828-9300; **NEW JERSEY: Edison** (908) 906-0033; **NEW MEXICO: Albuquerque** (505) 345-2555; **NEW YORK: Poughkeepsie** (914) 897-2900; **Long Island** (516) 454-6601; **Rochester** (716) 385-6770; **NORTH CAROLINA: Charlotte** (704) 522-5487; **Raleigh** (919) 876-2725; **OHIO: Cleveland** (216) 765-7258; **Dayton** (513) 427-6200; **OREGON: Portland** (503) 643-6758; **PENNSYLVANIA: Philadelphia** (215) 825-9500; **PUERTO RICO: Hato Rey** (809) 753-8700; **TEXAS: Austin** (512) 250-6769; **Dallas** (214) 917-1264; **Houston** (713) 778-6592; **WISCONSIN: Milwaukee** (414) 798-1001.

North American Authorized Distributors

COMMERCIAL	
Almac / Arrow	800-426-1410 / 800-452-9185 Oregon only
Anthem Electronics	800-826-8436
Arrow / Schweber	800-777-2776
Future Electronics (Canada)	800-388-8731
Hamilton Hallmark	800-332-8638
Marshall Industries	800-522-0084 or www.marshall.com
Wyle	800-414-4144
OBSOLETE PRODUCTS	
Rochester Electronics	508-462-9332
MILITARY	
Alliance Electronics Inc	800-608-9494
Future Electronics (Canada)	800-388-8731
Hamilton Hallmark	800-332-8638
Zeus, An Arrow Company	800-524-4735
CATALOG	
Allied Electronics	800-433-5700
Arrow Advantage	800-777-2776
Newark Electonics	800-367-3573

For Distributors outside North America, contact your local Sales Office.

A040395

TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

Printed in U.S.A.
0795–CP

SCDD001