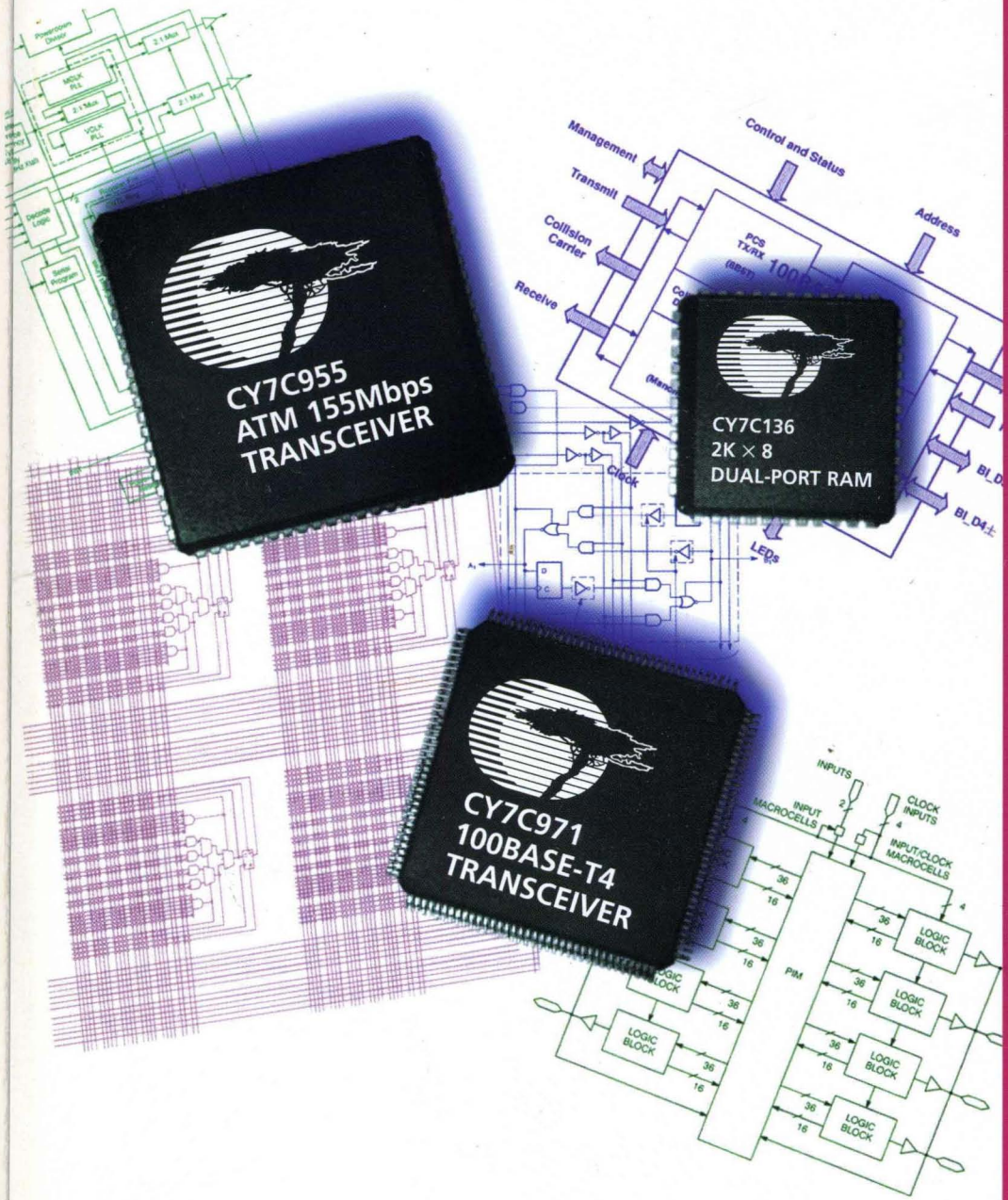
Data Communications DATA BOOK

ATM
Ethernet
Fibre Channel
FIFOs
Dual-Ports
Clocks

1996

CYPRESS



CYPRESS

Data Communications

DATA BOOK

Data Communications Data Book

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How To Use This Book

Overall Organization

This book has been organized by product type, beginning with Product Information. The products are next, starting with SRAMs, then Modules, Non-Volatile Memories, FIFOs, Dual-Ports, Data Communications, Bus Interface Products, FCT Logic, Timing Technology Products, and PC Chip Sets. A section containing military information is next, followed by Quality and Reliability aspects, then Thermal Data and Packages. Within each section, data sheets are arranged in order of part number.

Recommended Search Paths

To search by:	Use:
Product line	Table of Contents or flip through the book using the tabs on the right-hand pages.
Size	The Product Selector Guide in section 1.
Numeric part number	Numeric Device Index following the Table of Contents. The book is also arranged in order of part number.
Other manufacturer's part number	The Cross Reference Guide in section 1.
Military part number	The Military Selector Guide in section 12.

Key to Waveform Diagrams

 = Rising edge of signal will occur during this time.

 = Falling edge of signal will occur during this time.

 = Signal may transition during this time (don't care condition).

 = Signal changes from high-impedance state to valid logic level during this time.

 = Signal changes from valid logic level to high-impedance state during this time.

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General Information 1

General Information

Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and has been listed on the New York Stock Exchange since October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's offers products in four divisions: the Static Memory Division, the Programmable Products Division, the Computation Products Division, and the Data Communications Division.

Static Memories Division

Cypress is a market-leading supplier of SRAMs, providing a wide range of SRAM memories for leading companies worldwide. SRAMs are used in high-performance personal computers, workstations, telecommunications systems, industrial systems, instrumentation devices, and networking products. Cypress's lower production cost structure allows the company to compete effectively in the high-volume personal computer and workstation market for SRAMs, including providing cache RAMs to support today's high-performance microprocessors, such as Pentium™, and PowerPC™. This business, combined with upcoming low-voltage products for the cellular communications, portable instrument, and laptop/notebook PC markets, positions Cypress for future success in this key product area.

Multichip modules is a fast-growing market segment that consists of multiple semiconductor chips mounted in packages that can be inserted in a computer circuit board. Cache modules for personal computers are the mainstay of this product line, and Cypress has announced major design wins for these products in IBM's PS/ValuePoint™ line of PCs, and in Apple Computer's highest performing Power Macintosh™ products.

Programmable Products Division

With increasing pressure on system designers to bring products to market more quickly, programmable logic devices (PLDs) are becoming extremely popular. PLDs are logic control devices that can be easily programmed by engineers in the field, and later erased and reprogrammed. This allows the designers to make key changes to their systems very late in the development cycle to ensure competitive advantage. Used extensively in a wide range of applications, PLDs constitute a large and growing market. Cypress's UltraLogic™ product line addresses the high-density programmable logic market. UltraLogic includes the Ultra38000™ and pASIC380™ families of field-programmable gate arrays (FPGAs), the industry's fastest. It also includes high performance complex PLDs, the FLASH370™ family. Both of these product families are supported by Cypress's VHDL (Very high-speed integrated circuit Hardware Description Language) based *Warp* software design tools. Cypress pioneered the use of VHDL for PLD programming, and *Warp* software is a key factor in the company's overall success in the PLD market.

Cypress is a leading provider of the industry-standard 22V10 PLD with a wide range of products. Cypress is committed to competing in all ranges of the PLD market, with small devices, including the industry standard 16V8, the MAX340 EPLD line, and the UltraLogic products. To support these products, Cypress offers one of the industry's broadest range of programming tools and software for the programming of its PLDs.

Cypress provides one of the industry's broadest ranges of CMOS EPROMs and PROMs. Cypress owns a large share of the high-speed CMOS PROM market, and with its new cost structure, is effectively penetrating the mainstream EPROM market with a popular 256 Kbit EPROM, and the introduction of the world's fastest 512K and 1 Megabit EPROMs at 25 ns.

FCT Logic products are used in bus interface and data buffering applications in almost all digital systems. With the addition of the FCT logic product line, Cypress now offers over 46 standard logic and bus interface functions. The products are offered in the second generation FCT-T format, which is pin-compatible with the older FCT devices, but adds TTL (transistor-to-transistor logic) outputs for significantly lower ground bounce and improved system noise immunity. Cypress also offers the most popular devices with on-chip 25-ohm termination resistors (FCT2-T) to further lower ground bounce with no speed loss. Included in the new product family is the CYBUS3384, a bus switch that enables bidirectional data transfer between multiple bus systems or between 5 volt and 3.3 volt devices. Cypress also offers 16-bit versions of popular FCT products. This broad product offering is produced on Cypress's high-volume, CMOS manufacturing lines.

Data Communications Division

This is an especially significant area for Cypress since it represents a more market-driven orientation for the company in a fast-growing market segment. As part of the new company strategy, Cypress has dedicated this product line to serve the high-speed data communications market with a range of products from the physical connection layer to system-level solutions. HOTLink™, high-speed, point-to-point serial communications chips have been well received. HOTLink, along with the SONET/SDS Serial Transceiver (SST™), address the fast-growing market segments of Asynchronous Transfer Mode (ATM) and Fibre Channel communications. The company has also entered the Ethernet market with the 100BaseT-4 CY7C971 Fast Ethernet Transceiver and the CY7B8392 Coax Ethernet Transceiver. The data communications division encompasses related products including RoboClock, a programmable skew clock buffer that adjusts complex timing control signals for a broad range of systems. The division also offers a broad range of First-In, First-Out (FIFO) memories, used to communicate data between systems operating at different frequencies, and Dual-Port Memories, used to distribute data to two different systems simultaneously.

Computation Products Division

This division focuses on the high-volume, high-growth market surrounding the desktop computer. It is the second of Cypress's market-oriented divisions. The division includes timing technology products offered through Cypress's IC Designs Subsidiary in Kirkland, Washington. IC Designs products are used widely in personal computers and disk drives, and the product line provides Cypress with major inroads into these markets, helping move the company towards a more market-driven orientation. IC Designs clock oscillators control the intricate timing of all aspects of a computer system, including signals for the computer's central processing unit (CPU), keyboard, disk drives, system bus, serial port, and real-time clock. They replace all of the metal can oscillators used in the system. IC Designs recently announced a new product, QuiXTAL™, which is a programmable metal can oscillator, and replaces individual oscillators used to control timing signals in virtually every type of electronics equipment. QuiXTAL can be programmed to any frequency, providing users the ability to make last-minute frequency adjustments, speeding time to market. QuiXTAL takes frequency synthesis beyond the PC market, and addresses the broad market segments of electronic instrumentation, telecommunications equipment, and medical systems.

Also offered by this division are chipsets for personal computers. Cypress entered this market with the 1994 acquisition of Contaq Microsystems, and recently announced the hyperCache™ Chipset for Pentium™-class PCs. The hyperCache Chipset is the industry's most highly integrated. In addition to integrating keyboard and mouse control, real-time clock, and local-bus IDE control, it is the only chipset which offers integrated second-level cache.

Cypress Facilities

Cypress operates wafer fabrication facilities in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota. The company's fourth wafer fab, located adjacent to the Bloomington, Minnesota facility, went on-line in July 1995. There are additional Cypress Design Centers in Starkville, Mississippi, Colorado Springs, Colorado, and the United Kingdom, and a PLD software design group in Beaverton, Oregon. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.1 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

The company has also received ISO9000 registration, a standard model of quality assurance that is awarded to companies with exacting standards of quality management, production, and inspections.

Attention to assembly is equally critical. Cypress manufactures 100 percent of its wafers in the United States, at the front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, the company's largest fab, and Cypress Minnesota's fabs, are all Class 1 facilities.

To improve global competitiveness, Cypress chose to move most back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site—Cypress Bangkok.

The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet—a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres—sufficient room for expansion to a number of buildings in a campus-like setting. In order to meet growing demand for its products, Cypress has broken ground on a new assembly and test facility in the Philippines, which is scheduled for completion in 1996.

Cypress San Jose maintains complete management control of all assembly, test, mark, and ship operations worldwide, thus assuring complete continuity of back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to its package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

From Cypress's facility in Minnesota, a VME Bus Interface Products group has been in operation since the acquisition of VTC's fab in 1990. Cypress manufactures VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees . . . all striving to make the best products."

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Erasable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most advanced production processes in the world. The drive to maintain

leadership in process technology has not stopped with the 0.8-micron devices. Cypress introduced a 0.65-micron process in 1991. A 0.5-micron process is currently in production.

Although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2-, 0.8-, 0.65-, and 0.5-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching, and 100-percent stepper technology with the world's most advanced equipment.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

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DataCom Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. We have continued to serve this market using state-of-the-art process and circuit technology combined with architectural excellence. Our initial product thrusts included high-performance SRAMs, PLDs, FIFOs, Dual Port RAMs, and EPROMs.

In 1991, Cypress created a Data Communications division, with a focus on Physical Layer (PHY) devices to serve the ATM, SONET, Ethernet, ESCON, and Fibre Channel markets. Cypress's DataCom division has delivered a family of these PHY devices including the SST (SONET Serial Transceiver) Clock Recovery Device, the HOTLink 330 MHz point-to-point transmitter/receiver chip set, the CY7C971 10/100 Base-T4 Fast Ethernet Transceiver and the industry standard CY7B8392 10Base-2 Ethernet Coax Transceiver. In 1996 and 1997, Cypress will continue to deliver high performance solutions for the Physical Layer Datacom market covering 10 Base-FL, 100 Base-TX, and 155 MHz (OC-3) ATM/SONET Integration.

Our goal is to continue to provide PHY solutions for all segments of the DataCom market including Network Adapter Cards, Routers, Switches, Repeaters, Mass Storage, and Disk Farms. Our product evolution will continue through complete solutions for these growth markets.

In addition to PHY devices, the DataCom division includes a multitude of Specialty Memories including FIFOs (First-In-First-Out) and Dual Port RAMs which are frequently used in communications systems. Our current product count includes 44 Asynchronous and Synchronous FIFOs ranging from 64 x 9/18 through 32K x 9 at 100 MHz as well as 18 Dual Ports from 1K x 8 through 8K x 18 with 15 ns access times. We are confident that our wide variety of Specialty Memory products will suit many of your buffering requirements.

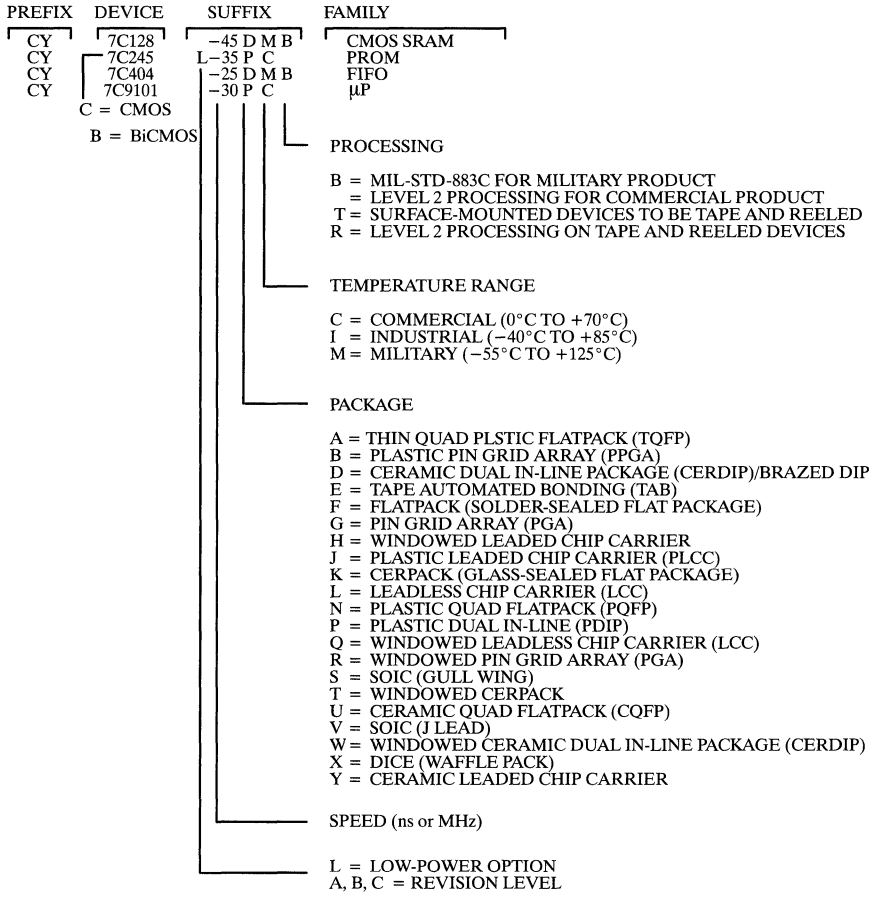
In addition to this DataCom Data Book, Cypress also offers technical documentation including a new Applications Handbook, HOTLink User's Guide, and a VME User's Guide.

We look forward to serving you. Please call with any requests for design, application, or additional product information.

Ordering Information

In general, the valid ordering codes for all products (except modules and VMEbus products) follow the format below; e.g., CY7C128–45DMB, PALC16R8L–35PC

RAM, PROM, FIFO, µP, ECL



Cypress FSCM #65786

Dual-Port RAMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ ns)	Packages
8K	1K x 8—Dual-Port Master	48	CY7C130	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Slave	48	CY7C140	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Master	52	CY7C131	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
8K	1K x 8—Dual-Port Slave	52	CY7C141	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual Port Master	48	CY7C132	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Slave	48	CY7C142	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Master	52	CY7C136	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual-Port Slave	52	CY7C146	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
32K	4K x 8—Dual-Port, No Arbitration	48	CY7B134	t_{AA} = 20, 25, 35, 55	240 @ 20	D, L, P
32K	4K x 8—Dual-Port, w/Semaph	52	CY7B1342	t_{AA} = 20, 25, 35, 55	240 @ 20	J
32K	2K x 16—Dual-Port Slave	68	CY7C143	t_{AA} = 15, 25, 35, 55	170 @25	J, A
32K	2K x 16—Dual-Port Master	68	CY7C133	t_{AA} = 15, 25, 35, 55	170 @ 25	J, A
32K	4K x 8—Dual-Port, w/ Semaph, Busy, Int	64, 68	CY7B138	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
32K	4K x 8—Dual-Port, No Arbitration	52	CY7B135	t_{AA} = 20, 25, 35, 55	240 @ 20	J, L
32K	4K x 9—Dual-Port, w/ Semaph, Busy, Int	68, 80	CY7B139	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	8K x 8—Dual-Port, w/ Semaph, Busy, Int	64, 68	CY7B144	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	8K x 9—Dual-Port, w/ Semaph, Busy, Int	68, 80	CY7B145	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	4K x 16—Dual-Port, w/ Semaph, Busy, Int	84, 100	CY7C024	t_{AA} = 15, 25, 35, 55	280 @ 15	J, A
64K	4K x 18—Dual-Port, w/ Semaph, Busy, Int	84, 100	CY7C0241	t_{AA} = 15, 25, 35, 55	280 @ 15	J, A
128K	8K x 16—Dual-Port w/ Semaph, Busy, Int	84, 100	CY7C025	t_{AA} = 15, 25, 35, 55	280 @ 15	J, A
128K	8K x 18—Dual-Port w/ Semaph, Busy, Int	84, 100	CY7C0251	t_{AA} = 15, 25, 35, 55	280 @ 15	J, A
128K	16K x 8—Dual-Port w/ Semaph, Busy, Int	64, 68	CY7C006	t_{AA} = 15, 25, 35, 55	260 @ 15	J, A
128K	16K x 9—Dual-Port w/ Semaph, Busy, Int	68, 80	CY7C016	t_{AA} = 15, 25, 35, 55	260 @ 15	J, A

Communication Products

Description	Pins	Part Number	Speed (MHz)	I_{CC} (mA)	Packages
HOTLink Transmitter	28	CY7B923	160–330	65	J, L, S
HOTLink Receiver	28	CY7B933	160–330	120	J, L, S
SONET/SDH Serial Transceiver	24	CY7B951	51 & 155	50	S
ATM SONET/SDH Transceiver		CY7B955			
10BASE 2/5 Ethernet Coax Transceiver	16, 20, 28	CY7B8392	10	25	J, P
Fast Ethernet 100BASE-T4 Transceiver	80	CY7C971	10 & 100	300	N
Fast Ethernet 100BASE-TX Transceiver	44	CY7C973	100	200	J
HOTLink Evaluation Card	N/A	CY9266	160–330	—N/A	C, F*, T

Note: Please contact a Cypress Representative for product availability.

FIFOs

Asynchronous

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ ns)	Packages
64x4	16	CY3341	1.2, 2 MHz	45	D, P
64x4	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P
64x4—w/$\overline{OE}$	16	CY7C403	10, 15, 25 MHz	75	D, L, P
64x5	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P
64x5—w/$\overline{OE}$	18	CY7C404	10, 15, 25 MHz	75	D, L, P
64x8—w/$\overline{OE}$ and Almost Flags	28S	CY7C408A	15, 25, 35 MHz	115 @ 15	D, L, P, V
64x9—w/Almost Flags	28S	CY7C409A	15, 25, 35 MHz	115 @ 15	D, L, P, V
256x9—w/Half Full Flag	28S, 32	CY7C419	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, L, P, V
512x9—w/Half Full Flag	28	CY7C420	20, 25, 30, 40, 65	35 @ 20	D, P
512x9—w/Half Full Flag	28S, 32	CY7C421	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
1Kx9—w/ Half Full Flag	28	CY7C424	20, 25, 30, 40, 65	35 @ 20	D, P
1Kx9—w/ Half Full Flag	28S, 32	CY7C425	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
2Kx9—w/ Half Full Flag	28	CY7C428	20, 25, 30, 40, 65	35 @ 20	D, P
2Kx9—w/ Half Full Flag	28S, 32	CY7C429	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
4Kx9—w/ Half Full Flag	28	CY7C432	25, 30, 40, 65	35 @ 20	D, P
4Kx9—w/Half Full Flag	28S, 32	CY7C433	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
8K x 9—w/ Half Full Flag	28	CY7C460	15, 25, 40, 65	105 @ 15	D, J, L, P
8K x 9—w/ Prog. Flags	28	CY7C470	15, 25, 40, 65	105 @ 15	D, J, L, P
16K x 9—w/ Half Full Flag	28	CY7C462	15, 25, 40, 65	105 @ 15	D, J, L, P
16K x 9—w/ Prog. Flags	28	CY7C472	15, 25, 40, 65	105 @ 15	D, J, L, P
32K x 9—w/ Half Full Flag	28	CY7C464	15, 25, 40, 65	105 @ 15	D, J, L, P
32K x 9—w/ Prog. Flags	28	CY7C474	15, 25, 40, 65	105 @ 15	D, J, L, P
2Kx9—Bidirectional	28S	CY7C439	25, 30, 40, 65	147@ 25	D, J, L, P

Clocked

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	Packages
512 x 9—Clocked	28S, 32	CY7C441	14, 20, 30*	70 @ 20	D, J, L, P, V
512 x 9—Clocked w/ Prog. Flags	32	CY7C451	14, 20, 30*	70 @ 20	D, J, L
2K x 9—Clocked	28S, 32	CY7C443	14, 20, 30*	70 @ 20	D, J, L, P, V
2K x 9—Clocked w/ Prog. Flags	32	CY7C453	14, 20, 30*	70 @ 20	D, J, L
512x18—Clocked w/Prog. Flags	52	CY7C455	14, 20, 30*	90 @ 20	J, L, N
1Kx18—Clocked w/Prog. Flags	52	CY7C456	14, 20, 30*	90 @ 20	J, L, N
2Kx18—Clocked w/Prog. Flags	52	CY7C457	14, 20, 30*	90 @ 20	J, L, N

Synchronous

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	Packages
64x9—Synchronous	32	CY7C4421	10, 15, 25, 35*	50 @ 20	A, J
256x9—Synchronous	32	CY7C4201	10, 15, 25, 35*	50 @ 20	A, J
512x9—Synchronous	32	CY7C4211	10, 15, 25, 35*	50 @ 20	A, J
1Kx9—Synchronous	32	CY7C4221	10, 15, 25, 35*	50 @ 20	A, J
2Kx9—Synchronous	32	CY7C4231	10, 15, 25, 35*	50 @ 20	A, J

Note: Please contact a Cypress Representative for product availability.

FIFOs (continued)

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	Packages
4Kx9—Synchronous	32	CY7C4241	10, 15, 25, 35*	50 @ 20	A, J
8Kx9—Synchronous	32	CY7C4251	10, 15, 25, 35*	50 @ 20	A, J
16Kx9—Synchronous	32	CY7C4261	10, 15, 25, 35*	50 @ 20	A, J
32Kx9—Synchronous	32	CY7C4271	10, 15, 15, 35*	50 @ 20	A, J
64x18—Synchronous	64, 68	CY7C4425	10, 15, 25, 35*	100 @ 20	A, J
256x18—Synchronous	64, 68	CY7C4205	10, 15, 25, 35*	100 @ 20	A, J
512x18—Synchronous	64, 68	CY7C4215	10, 15, 25, 35*	100 @ 20	A, J
1Kx18—Synchronous	64, 68	CY7C4225	10, 15, 25, 35*	100 @ 20	A, J
2Kx18—Synchronous	64, 68	CY7C4235	10, 15, 25, 35*	100 @ 20	A, J
4Kx18—Synchronous	64, 68	CY7C4245	10, 15, 25, 35*	100 @ 20	A, J
8Kx18—Synchronous	64, 68	CY7C4255	10, 15, 25, 35*	100 @ 20	A, J
16Kx18—Synchronous	64, 68	CY7C4265	10, 15, 25, 35*	100 @ 20	A, J

* Cycle Times

Timing Technology Products

Application	Part #	# of PLLs	# of Outputs	Features	Package
Industry Standard Motherboard Frequency Synthesizers	CY2250	1	14	Pentium/Pentium Pro servers: 12 skew controlled CPU clocks (250 ps pin-to-pin), 2 buffered reference clocks, 3.3V	28 SOIC
	CY2252	2	14	Pentium portables: 5 CPU/6 PCI clocks (2 "early" PCI for docking stations), 24 MHz, 2 buffered reference clocks, 3.3V	28 SSOP
	CY2254	2	14	Intel Triton chipset compatible: 4 CPU/6 PCI clocks, 12 MHz, 24 MHz, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2255	1	14	OPTi Viper chipset compatible: 6 CPU (1 "early")/6 PCI clocks, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2257	1	14	Ali Aladdin chipset compatible: 6 CPU/6 PCI clocks, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2260	2	14	Intel Natoma/Triton II chipset compatible: 4 CPU/6 PCI clocks, 48 MHz USB clock, 3 buffered reference clocks, 3.3V	28 SOIC 28 SSOP
General Purpose Programmable Products (486 Pentium/Pentium Pro motherboards, peripherals, cable TV, video games, MPEG decoders, etc.)	CY2071	1	3	Factory EPROM programmable single PLL, 0.5 – 100 MHz, 5V/3.3V	8 SOIC
	CY2081	3	3	Factory EPROM programmable triple PLL, 0.5 – 100 MHz, 5V/3.3V	8 SOIC
	CY2291	3	8	Factory EPROM progrmmable triple PLL, 0.2 – 100 MHz, 5V/3.3V	20 SOIC
	CY2292	3	6	Factory EPROM programmable triple PLL, 0.2 – 100 MHz, 5V/3.3V	16 SOIC
	ICD2051	2	5	User-programmable dual PLL, 0.3 – 120 MHz, 5V	16 SOIC
	ICD2053B	1	1	User-programmable single PLL, 0.4 – 100 MHz, 5V	8 SOIC
PC Graphics Frequency Synthesizers	ICD2061A	2	2	User-programmable PC video/memory clocks, 0.4 – 120 MHz, 5V	16 SOIC
	ICD2062B	2	6	User-programmable PECL video clock for workstations, 0.5 – 165 MHz, 5V	20 SOIC
	ICD2063	2	2	User-programmable PC video/memory clocks, 0.3 – 135 MHz, 5V/3.3V	16 SOIC
Programmable Skew Clock Buffer (TTL Output)	CY7B991	1	8	3 – 80 MHz, Programmable Skew (700 ps increments) 250 ps pin-to-pin skew	J, L
Programmable Skew Clock Buffer (CMOS Output)	CY7B992	1	8	3 – 80 MHz, Programmable Skew (700 ps increments) 250 ps pin-to-pin skew	J, L

Note: Please contact a Cypress Representative for product availability.

Timing Technology Products (continued)

Application	Part #	# of PLLs	# of Outputs	Features	Package
Low Skew Clock Buffer (TTL Output)	CY7B9910	1	8	15–80 MHz, t_{PD} = 500 ps 250 ps pin-to-pin skew	S
Low Skew Clock Buffer (CMOS Output)	CY7B9920	1	8	15–80 MHz, t_{PD} = 500 ps 250 ps pin-to-pin skew	S

Note: Please contact a Cypress Representative for product availability.

HOTLink Cross Reference

Cypress		TriQuint		AMCC		Raytheon	
Device	**Speed Range**	**Device**	**Speed Range**	**Device**	**Speed Range**	**Device**	**Speed Range**
CY7B923/33	160–330	GA9101/2/3*	200/265	S2032/33*	265/531/1062	RCC700*	200/265

SST Cross Reference

Cypress		Analog Devices		AMCC	
Device	**Requires 155-MHz Oscillator**	**Device**	**Requires 155-MHz Oscillator**	**Device**	**Requires 155-MHz Oscillator**
CY7B951	No	AD 802*	Yes	S3014*	Yes

* Not pin compatible; see product profile for Cypress advantages.

CY7C971 Fast Ethernet Transceiver (100BASE-T4) Cross Reference

Cypress		Broadcom		Seeq		AT&T	
Device	**Integrated Transmit Filter**	**Device**	**Integrated Transmit Filter**	**Device**	**Integrated Transmit Filter**	**Device**	**Integrated Transmit Filter**
CY7C971	Yes	BCM5000*	No	80C240*	Yes	*	No

* Not pin compatible; see product profile for Cypress advantages.

CY7B8392 10BASE–2 Ethernet Coax Transceiver Cross Reference

Cypress				National				Seeq			
Device	**I_{CC}**	**Auto AUI**	**Distance**	**Device**	**I_{CC}**	**Auto AUI**	**Distance**	**Device**	**I_{CC}**	**Auto AUI**	**Distance**
CY7B8392	35 mA	Yes	300M	8392	130 mA	No	185M	83C92	70 mA	No	185M

CY7B8392 10BASE–2 Ethernet Coax Transceiver Cross Reference

Phillips/Sig				SSI			
Device	**I_{CC}**	**Auto AUI**	**Distance**	**Device**	**I_{CC}**	**Auto AUI**	**Distance**
NE83Q92	35 mA	Yes	185M	78Q8392	130 mA	No	185M

* Not pin compatible; see product profile for Cypress advantages.
** Speed in MHz.

FIFO Cross Reference

Cypress, prefix CY		IDT, prefix IDT		AMD, prefix Am		Quality, prefix QS		TI, prefix SN74		Sharp, prefix LH	
Device	**Speed (ns)**	**Device**	**Speed (ns)**	**Device**	**Speed (ns)**	**Device**	**Speed (ns)**	**Device**	**Speed (ns)**	**Device**	**Speed (ns)**
7C401	5–25**	72401	10–45**	67C401	10–35* *			ALS236	10–45**		
7C402	5–25**	72402	10–45**	67C402	10–35* *						
7C403	5–25**	72403	10–45**	67C403	10–35* *			ALS234	10–45**		
7C404	5–25**	72404	10–45**	67C404	10–35* *						
7C408/9	15–35**									5481/91*	15–50
7C419	10–65	7200	15–65	7200	25–120			ACT7200	15–50	5495	15–80
7C420/1	10–65	7201	15–65	7201	25–120	7201	12–120	ACT7201	15–50	5496	15–80
7C424/5	10–65	7202	15–65	7202	15–80	7202	12–120	ACT7202	15–50	5497	15–80
7C428/9	10–65	7203	15–65	7203A	15–80	7203	10–120	ACT7203	20–50	5498	15–80
7C432/3	10–65	7204	15–65	7204A	15–80	7204	10–120	ACT7204	20–50	5499	20–50
7C441/451	14–30	72211*	15–50								
7C443/453	14–30	72231*	15–50							5492*	25–50
7C455	14–30	72215*	15–50							540215*	20–50
7C457	14–30	72235*	15–50								
7C460	15–40	7205	20–50	7205	15–50						
7C462	15–40	7206	20–50								
7C462	15–40	7207	15–50								
7C4421	10–35	72421	15–50								
7C4201	10–35	72201	15–50								
7C4211	10–35	72211	15–50			72211		ACT72211	15–50		
7C4221	10–35	72221	15–50			72221		ACT72221	15–50		
7C4231	10–35	72231	15–50			72231		ACT72231	15–50		
7C4241	10–35	72241	15–50			72241		ACT72241	15–50		
7C4251	10–35										
7C4261	10–35										
7C4271	10–35										
7C4425	10–35										
7C4205	10–35	72205	10–50								
7C4215	10–35	72215	10–50			72215					
7C4225	10–35	72225	10–50			72215					
7C4235	10–35	72235	10–50								
7C4245	10–35	72245	10–50								
7C4255	10–35										
7C4265	10–35										
Package	**Code**	**Package**	**Code**	**Package**	**Code**	**Package**	**Code**	**Package**	**Code**	**Package**	**Code**
PLCC	J	PLCC	J	PLCC	J	PLCC	JR	PLCC	RJ	PLCC	U
T/PQFP	N	T/PQFP	PF					T/PQFP	PN/PH		
PDIP	P	PDIP	TP	PDIP	R/P	PDIP	P/P6	PDIP	NP/NT	PDIP	D/Blank
CDIP	D	CDIP	D	CDIP	X	CDIP	D/D6	CDIP	NR/		
Temp. Range	**Code**	**Temp. Range**	**Code**	**Temp. Range**	**Code**	**Temp. Range**	**Code**	**Temp. Range**	**Code**	**Temp. Range**	**Code**
Com'l	C	Com'l	Blank	Com'l	C	Com'l	N/A	Com'l	SN	Com'l	
Industrial	I	Industrial		Industrial		Industrial		Industrial		Industrial	
Military	MB	Military	B	Military	B	Military	B	Military	SNJ	Military	Not offered

* Not pin compatible; see product profile for Cypress advantages.
** Speed in MHz.

Dual Port Cross Reference

Cypress, prefix CY		IDT, prefix IDT	
Device	**Speed (ns)**	**Device**	**Speed (ns)**
7C130/1 7B131	15–55	7130	20–100
7C132	25–55	7132	20–100
7C133	15–55	7133	25–90
7C136 7B136	15–55	71321	25–55
7C140/1 7B141	15–55	7140	20–100
7C142	25–55	7142	20–100
7C143	15–55	7143	25–90
7C146 7B146	15–55	71421	25–55
7B134 /5	15–35	7134	25–70
7B1342	15–35	71342	25–70
7B144	15–35	7005	25–70
7C024	15–55	7024	20–70
7C025	15–55	7025	20–70
7C006	15–55	7006	25–70
7C016	15–55	7016	15–70
7C0241	15–55		
7C0251	15–55		
7B145	15–55	7015	20–70
Package	**Code**	**Package**	**Code**
PLCC	J	PLCC	J
PDIP	P	PDIP	P
CDIP	D	CDIP	D
Temp. Range	**Code**	**Temp. Range**	**Code**
Com'l	C	Com'l	Blank
Industrial	I	Industrial	
Military	MB	Military	B

* Not pin compatible; see product profile for Cypress advantages.
** Speed in MHz.

Cypress Semiconductor Bulletin Board System (BBS) Announcement

Cypress Semiconductor supports a 24-hour electronic Bulletin Board System (BBS) that allows Cypress Applications to better serve our customers by allowing them to transfer files to and from the BBS.

The BBS is set up to serve in multiple ways. One of its purposes is to allow customers to receive the most recent versions of Cypress programming software. Another is to allow the customers to send PLD programming files that they are having trouble with to the BBS. Cypress Applications can then find the errors in the files, correct them, and place them back on the BBS for the customer to download. The customer may also ask questions in our open forum message area. The sysop (system operator) will forward these questions to the appropriate applications engineer for an answer. The answers then get posted back into the forum.

Communications Set-Up

The BBS uses USRobotics HST Dual Standard modems capable of 14.4-Kbaud rates without compression and rates upwards of 19.2-Kbaud with compression. It is compatible with CCITT V.32 bis, V.32, V.22 (2400-baud), Bell 212A (1200-baud), CCITT V.42, and CCITT V.42 bis. It also handles MNP levels 2, 3, 4, and 5.

To call the BBS, set your communication package parameters as follows:

Baud Rate: 1200 baud to 19.2 Kbaud. Max. is determined by your modem.
Data Bits: 8
Parity: None (N)
Stop Bits: 1

In the U.S. the phone number for the BBS is (408) 943−2954. In Japan the BBS number is 81−423−69−8220. In Europe the BBS number is 49−810−62−2675. These numbers are for transmitting data only.

If the line is busy, please retry at a later time. When you access the BBS, an initial screen with the following statement will appear:

```
Rybbs Bulletin Board
```

After you choose the graphics format you want to use, the system will ask for your first and last name. If you are a first-time user, you will be asked a few questions for the purposes of registration. Otherwise you will be asked for your password, and then you will be logged onto the BBS, which is completely menu driven.

Downloading Application Notes and Datasheets

A complete listing of files that may be downloaded is included on the BBS. Application notes are available for downloading in two formats, PCL and Postscript™. An "hp" in front of the file name indicates it is a PCL file and can be downloaded to Hewlett-Packard LaserJets™ and compatible printers. Files without the hp preceding them are in Postscript and can be downloaded to any Postscript printer.

If you have any problems or questions regarding the BBS, please contact Cypress Applications at (408) 943−2821 (voice).

Postscript is a trademark of Adobe Corporation.
LaserJet is a trademark of Hewlett Packard Corporation.

Ethernet 2

Ethernet

100BASE-T4/10BASE-T Fast Ethernet Transceiver (CAT 3)

Features

- **Complies with IEEE 802.3u draft standard**
- **Three operating modes:**
  - **— 100BASE-T4**
  - **— 10BASE-T Full Duplex**
  - **— 10BASE-T**
- **Media Independent Interface (MII)**
  - **— Three-state receive port**
  - **— Serial management port**
- **Auto-Negotiation**
- **On-chip transmit wave shaper**
- **Receive filter and adaptive equalization**
- **PMA Interface for repeater applications**
- **Jam function for hub applications**
- **LED status indicators: TX, RX, Link**
- **Loopback mode for PHY integrity testing**
- **Auto-polarity correction**
- **Low-power CMOS**
- **80-pin PQFP**

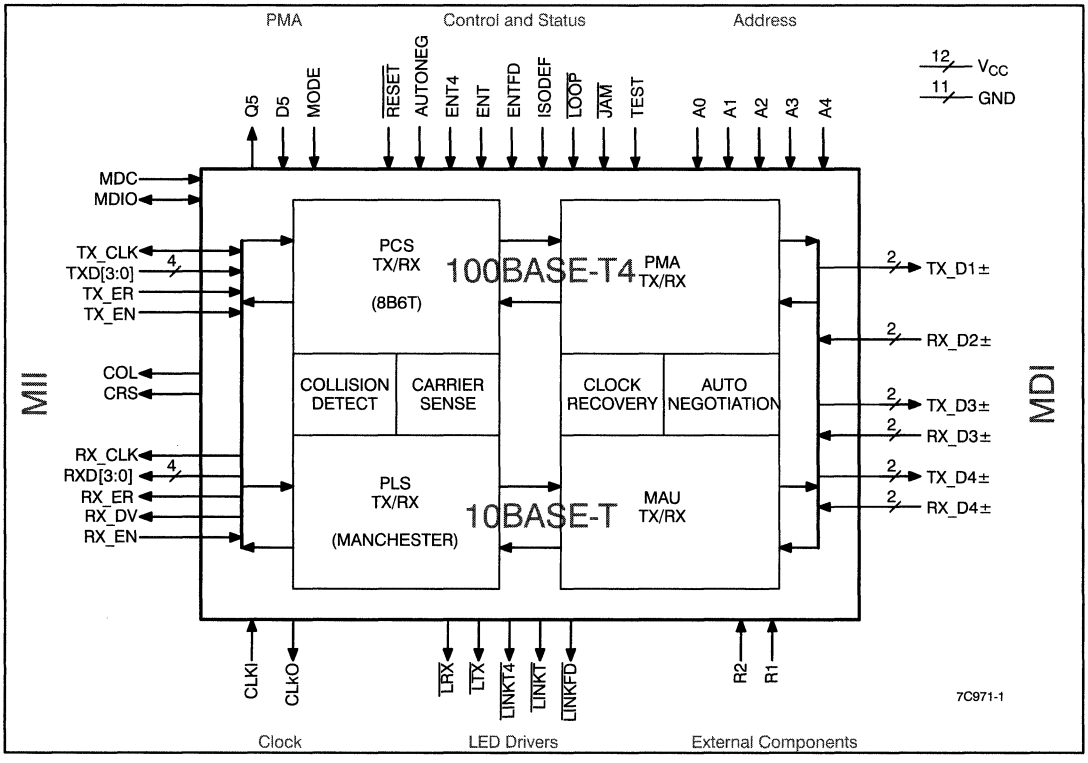
Functional Description

The CY7C971 is a full featured physical layer transceiver (PHY) device supporting both 100BASE-T4 (Fast Ethernet) and 10BASE-T Local Area Network (LAN) standards. The CY7C971 complies with IEEE 802.3 100BASE-T4, 10BASE-T, MII, and Auto-Negotiation standards for twisted pair interfaces.

The CY7C971 interfaces to category 3, 4, or 5 unshielded twisted-pair cable through its Media Dependent Interface (MDI). The Media Independent Interface (MII) attaches directly to Media Access Control (MAC) layer devices.

The CY7C971 performs the Physical Coding Sublayer (PCS), Physical Layer Signalling (PLS), Physical Media Attachment (PMA), and Media Attachment Unit (MAU) functions defined in the 802.3 standard. Ethernet frames are transferred from the MAC to the CY7C971 over the MII interface. The data is encoded in the PCS or PLS encoder (8B6T for 100BASE-T4 or Manchester for 10BASE-T) and then passed to the PMA or MAU where the encoded data is shifted bitwise on to the twisted-pair media. Collision and Carrier Sense signals are generated by the CY7C971 and passed to the MAC over the MII.

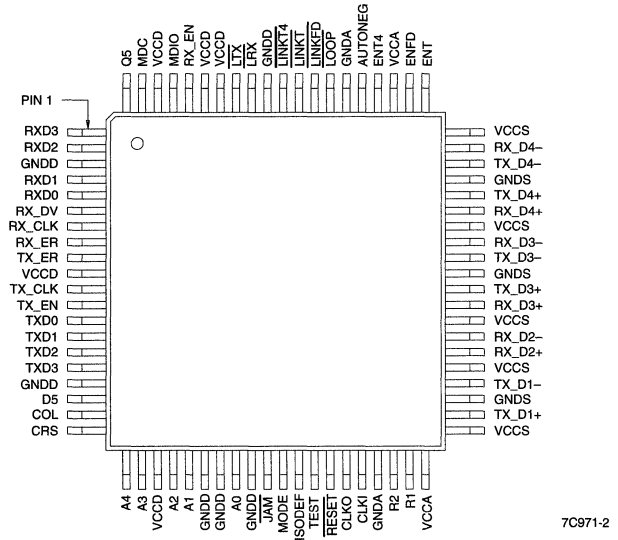
The CY7C971 PHY uses 802.3 standard Auto Negotiation to configure the link. The PHY includes a direct interface to the PMA layer for repeater applications.



Pin Configuration

80-Lead Plastic Quad Flatpack

(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Pin Descriptions

Media Independent Interface (MII)

Name	I/O	Description
TXD[3:0] (D[3:0])	Input (TTL)	Transmit Data. TXD[3:0] are the data signals that carry the Ethernet transmit frame data from the MAC to the PHY on a nibble basis. TXD[3:0] are sampled on the rising edge of TX_CLK when TX_EN is asserted HIGH. In PMA mode, these pins become the D[3:0] pins used for passing binary encoded 8B6T symbols to the PMA sublayer.
TX_EN	Input (TTL)	Transmit Enable. When asserted HIGH, TX_EN indicates that the MAC is presenting data to the TXD[3:0] inputs of the PHY. TX_EN should be asserted HIGH with the first nibble of the preamble and remain HIGH for the duration of the frame.TX_EN should be deasserted on the first cycle following the final nibble of the frame. In PMA mode, TX_EN is asserted HIGH in order to latch D[5:0] into the transmitter.
TX_CLK	Output (TTL, Three State)	Transmit Clock. In MII Mode (MODE = HIGH), TX_CLK is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TX_EN, and TX_ER from the MAC. The nominal frequency of TX_CLK is 25 MHz in 100-Mb/s mode and 2.5 MHz in 10-Mb/s mode.
TX_ER (D4)	Input (TTL)	Transmit Coding Error. When asserted HIGH while TX_EN is HIGH, the PHY will transmit an error code word . TX_ER is sampled on the rising edge of TX_CLK. In PMA mode, this pin becomes the D4 pin used for passing binary encoded 8B6T symbols to the PMA sublayer.
RXD[3:0] (Q[3:0])	Output (TTL, Three State)	Receive Data. RXD[3:0] are the data signals that carry the received Ethernet frame data from the PHY to the MAC on a nibble basis. RXD[3:0] are driven synchronous to RX_CLK. In PMA mode, these pins become the Q[3:0] pins used for transferring binary encoded 8B6T symbols from the PMA sublayer.
RX_DV	Output (TTL, Three State)	Receive Data Valid. When asserted HIGH, RX_DV indicates that the PHY is presenting recovered and decoded nibbles on the RXD[3:0] lines and that RX_CLK has been synchronized to the recovered data. RX_DV is first driven HIGH when RXD[3:0] contains the SFD and is held HIGH for the duration of the frame. RX_DV makes transitions synchronous to RX_CLK. In PMA Mode, RX_DV is driven high when Q2–3 contains the first data symbol.
RX_CLK	Output (TTL, Three State)	Receive Clock. RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER signals from the PHY to the MAC. When RX_DV is HIGH, RX_CLK is recovered from the received data. When RX_DV is LOW, RX_CLK is sourced from the PHY's nominal frequency. Transition between nominal frequency and recovered frequency is made while RX_DV is LOW. In 100-Mb/s mode, the nominal clock frequency is 25 MHz,and in 10-Mb/s the nominal frequency is 2.5 MHz.
RX_EN[1]	Input (TTL)	Receiver Output Enable. RX_EN enables the RXD[3:0], COL, Q5, RX_ER, and RX_DV signal drivers. RX_EN allows the receive data signals to bussed together for multiple PHY applications.
RX_ER	Output (TTL, Three State)	Receive Error. RX_ER is asserted HIGH to indicate to the MAC that a fault condition was detected during the frame presently being transferred from the PHY to the MAC. RX_ER is driven synchronously with RX_CLK.
COL (Q4)	Output (TTL, Three State)	Collision Detect. COL is asserted HIGH to indicate that a collision has occurred on the media. COL is asserted asynchronously and with minimum delay from the start of the collision. In PMA Mode, this pin becomes the Q4 pin used for transferring binary encoded 8B6T symbols from the PMA sublayer.
CRS	Output (TTL, Three State)	Carrier Sense. CRS is asserted HIGH by the PHY to indicate the detection of a non-idle condition on the media. CRS is asserted asynchronously and with minimum delay from the detection of the non-idle condition. CRS is asserted HIGH throughout the duration of a collision condition.
MDC	Input (TTL)	Management Data Clock. MDC is sourced from the station management entity (STA) to the PHY as a timing reference for the transfer of management information on the MDIO signal.
MDIO	Bidirectional (TTL, Three State)	Management Data Input/Output. MDIO is a bidirectional signal between the PHY and the station management entity (STA) used to transfer control and status information. Control information is driven from STA to the PHY synchronously with MDC and sampled on the rising edge of MDC. The PHY drives status information to the STA synchronously with MDC. The STA samples the data on the rising edge of MDC.

Note:
1. RX_EN is not specified in the 802.3 MII standard.

Pin Descriptions (continued)

Media Dependent Interface

Name	I/O	Description
TX_D1+ TX_D1−	Differential Output	Transmit Data. TX_D1± are differential line drivers for data transmission. In 10BASE-T mode TX_D1± transmit Manchester encoded data with a nominal period of 100 ns. In 100BASE-T4 mode TX_D1± transmit 8B6T ternary symbols with a nominal period of 40 ns. TX_D1± also participate in the Link Integrity function.
RX_D2+ RX_D2−	Differential Input	Receive Data. RX_D2± are differential line receivers for data reception. In 100-Mb/s mode, RX_D2± receives 8B6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D2± receives Manchester encoded bits with a nominal period of 100ns. RX_D2± also participates in the Link Integrity function.
TX_D3+ TX_D3−	Differential Output	Transmit Data. TX_D3± are differential line drivers for data transmission. In 100-Mb/s mode, TX_D3± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D3± are not used.
RX_D3+ RX_D3−	Differential Input	Receive Data. RX_D3± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D3± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D3± are not used.
TX_D4+ TX_D4−	Differential Output	Transmit Data. TX_D4± are differential line drivers used for data transmission. In 100-Mb/s mode, TX_D4± transmits 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, TX_D4± are not used.
RX_D4+ RX_D4−	Differential Input	Receive Data. RX_D4± are differential line receivers used for data reception. In 100-Mb/s mode, RX_D4± receives 6T ternary symbols with a nominal period of 40 ns. In 10-Mb/s mode, RX_D4± are not used.

Physical Media Attachment Interface

Name	I/O	Description
MODE	Input (TTL)	Mode. When MODE is tied HIGH, the transceiver is in normal mode. Received and tranmitted data will move through the PMA and the PCS sublayers. Asserting MODE LOW exposes the 100BASE-T4 PMA service interface and disables 10BASE-T. The PCS is bypassed and the binary coded 6T serial data is presented at the MII and PMA interface pins.
D5	Input (TTL)	PMA Input Data. D5 is an input signal to the PMA transmit sublayer when MODE is asserted LOW.
Q5	Output (TTL, Three State)	PMA Output Data. Q5 is an output signal from the PMA receive sublayer when MODE is asserted LOW. Q5 is high-impedence when RX_EN is HIGH.

Control and Status

Name	I/O	Description
$\overline{\text{RESET}}$	Input (TTL)	Reset. When $\overline{\text{RESET}}$ is asserted LOW, the PHY is placed in the reset state and the transmit and receive functions are disables. The MII registers are placed in their default states.
AUTONEG	Input (TTL)	Auto-Negotiation Enable. When asserted HIGH, Auto-Negotation capability is enabled by setting the Status Register bit 1.3. Auto-Negotation is controlled through the MII management registers. When asserted LOW, Auto-Negotation capability is disabled. AUTONEG is sampled on the rising edge of $\overline{\text{RESET}}$.
ENT4	Input (TTL)	Enable 100BASE-T4. ENT4 enables 100BASE-T4 operation by setting the Status Register bit 1.15. When ENT4 is HIGH, bit 1.15 is forced HIGH, enabling 100BASE-T4 operation. When ENT4 is LOW, bit 1.15 is forced LOW, disabling 100BASE-T4. ENT4 is latched on the rising edge of $\overline{\text{RESET}}$.
ENT	Input (TTL)	Enable 10BASE-T. ENT enables 10BASE-T operation by setting the Status Register bit 1.11. When ENT is HIGH, bit 1.11 is forced HIGH, enabling 10BASE-T operation. When ENT4 is LOW, bit 1.11 is forced LOW, disabling 10BASE-T. ENT is latched on the rising edge of $\overline{\text{RESET}}$.
ENTFD	Input (TTL)	Enable 10BASE-T Full Duplex. ENTFD enables 10BASE-T Full Duplex operation by setting the Status Register bit 1.12. When ENTFD is HIGH, bit 1.12 is forced HIGH, enabling 10BASE-T Full Duplex operation. When ENTFD is LOW, bit 1.12 is forced LOW, disabling 10BASE-T Full Duplex. ENTFD is latched on the rising edge of $\overline{\text{RESET}}$.
ISODEF	Input (TTL)	Isolate Default. ISODEF determines the default state of Isolate Bit 0.10 in the Control Register. When ISODEF is HIGH, the default value for 0.10 is 1. When ISODEF is LOW, the default value for 0.10 is 0. ISODEF is latched on the rising edge of $\overline{\text{RESET}}$.
$\overline{\text{LOOP}}$	Input (TTL)	Loopback Enable. When asserted LOW, the transmitter bit stream is looped back to the receiver for diagnostic testing. When $\overline{\text{LOOP}}$ is HIGH, the Loopback function is controlled by the Loopback bit in the control register.

Pin Descriptions (continued)

Control and Status (continued)

Name	I/O	Description
$\overline{JAM}$	Input (TTL)	100BASE-T4 Jam Generation. When $\overline{JAM}$ is LOW in 100BASE-T4 mode and a carrier is present, the PHY will enter the collision state and generate the Jam pattern. The jam condition will persist for a minimum of 512 bit times.
TEST	Input (TTL)	Test. This pin is used for factory testing and should be tied LOW for normal operation.

Address

Name	I/O	Description
A[4:0]	Input (TTL)	PHY Address. These pins assign the management address to the PHY. A0 is least significant bit and A4 is the most significant bit. A4 is the first address bit received by the PHY in the management frame. The address is latched on the rising edge of $\overline{RESET}$.

LED Drivers

Name	I/O	Description
$\overline{LRX}$	Output (Open Drain, Weak Pull-Up)	Receive LED Indicator. $\overline{LRX}$ is driven LOW when the transceiver is receiving. An internal 20KΩ resistor will pull $\overline{LRX}$ HIGH when the transceiver is not receiving.
$\overline{LTX}$	Output (Open Drain, Weak Pull-Up)	Transmit LED Indicator. $\overline{LTX}$ is driven LOW when the transceiver is transmitting. An internal 20KΩ resistor will pull $\overline{LTX}$ HIGH when the transceiver is not transmitting.
$\overline{LINKT4}$	Output (Open Drain, Weak Pull-Up)	100BASE-T4 Link Pass LED Indicator. $\overline{LINKT4}$ is driven LOW when the 100BASE-T4 transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINKT4}$ HIGH when the transceiver is not in the 100BASE-T4 Link Pass State.
$\overline{LINKT}$	Output (Open Drain, Weak Pull-Up)	10BASE-T Link Pass LED Indicator. $\overline{LINKT}$ is driven LOW when the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINKT}$ HIGH when the transceiver is not in the 100BASE-T Link Pass State.
$\overline{LINKFD}$	Output (Open Drain, Weak Pull-Up)	10BASE-T Full Duplex Link Pass LED Indicator. $\overline{LINKFD}$ is driven LOW when 10BASE-T Full Duplex has been negotiated or chosen as the operating mode and the 10BASE-T transceiver is in the Link Pass State. An internal 20KΩ resistor will pull $\overline{LINTFD}$ HIGH when the transceiver is not in the 100BASE-T Link Pass State.

Clock

Name	I/O	Description
CLKI	Input	Reference Clock Input. In MII Mode (MODE=HIGH), the 25-MHz signal is used as a timing reference for TX_CLK and analog circuits. This pin should be connected to either to a 25-MHz crystal or a crystal-controlled TTL-level clock source. In PMA mode (MODE = LOW), CLKI is an input and is used as a timing reference for the PMA interface and analog circuits.
CLKO	Output	Reference Clock Output. This pin connects to a 25 MHz crystal or is left open if a TTL clock is used with CLKI. In PMA mode, CLKO should be left open.

External Components

Name	I/O	Description
R1	Passive	10K ±1% External resistor.
R2	Passive	10K ±1% External resistor.

Power and Ground

Name	I/O	Description
V_{CCD}	Digital Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
V_{CCA}	Analog Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
V_{CCS}	Serial MDI Power	Positive Voltage Supply. V_{CC} requires a 5V±10% supply.
GNDD	Digital Ground	Ground.
GNDA	Analog Ground	Ground.
GNDS	Serial MDI Ground	Ground.

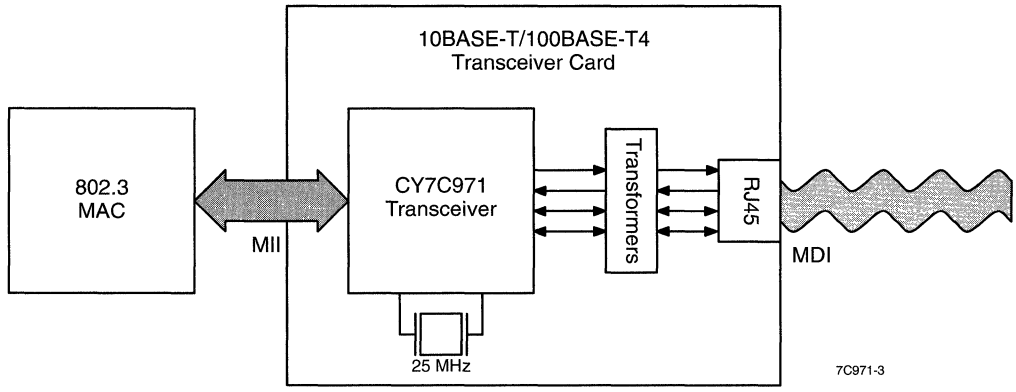


Figure 1. Transceiver Card Block Diagram

CY7C971 Description

100BASE-T4

The CY7C971 provides a physical layer interface (PHY) for dual speed IEEE 802.3 100BASE-T4 and 10BASE-T CSMA/CD local area networks. 100BASE-T4 offers increased performance over existing 10BASE-T networks while maintaining compatibility with the existing Ethernet Media Access Control (MAC) specification. The 100BASE-T4 PHY interfaces to 4 pairs of category 3, 4, or 5 cable. The 100BASE-T4 PHY is comprised of the Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Media Independent Interface (MII), and Media Dependent Interface (MDI). A typical 100BASE-T4 transceiver card application is shown in *Figure 1*.

Transmitter

The transmitter is comprised of the Physical Coding Sublayer (PCS) and the Physical Media Attachment (PMA). *Figure 2* shows a block diagram of the T4 transmitter.

Transmit Physical Coding Sublayer (PCS)

The PCS takes nibble-wide data from the MII and accumulates them into 8-bit octets in the TXD1 and TXD2 registers. The octets are then encoded using the 8B6T ternary code according to the 802.3 standard. The encoded 8B6T code groups are then loaded in binary form to the shift registers.

Three shift registers convert the parallel 8B6T code groups to serial form. When the transmitter is active, a shift register is loaded on every other TX_CLK cycle. The first 8B6T code group of the frame is loaded into TX_shift1. The second group is loaded into TX_shift2 and the third into TX_shift3. The 4th group will be loaded into TX_shift1. This sequence continues until all of the 8B6T code groups comprising the frame have been transmitted.

At the start of the transmit frame, TX_shift2 and TX_shift3 will be loaded with a pad sequence aligned with first 8B6T code group in TX_shift1. The pad sequence aides the receiver with clock recovery and pair alignment. The preamble is generated automatically and follows the pad sequence.

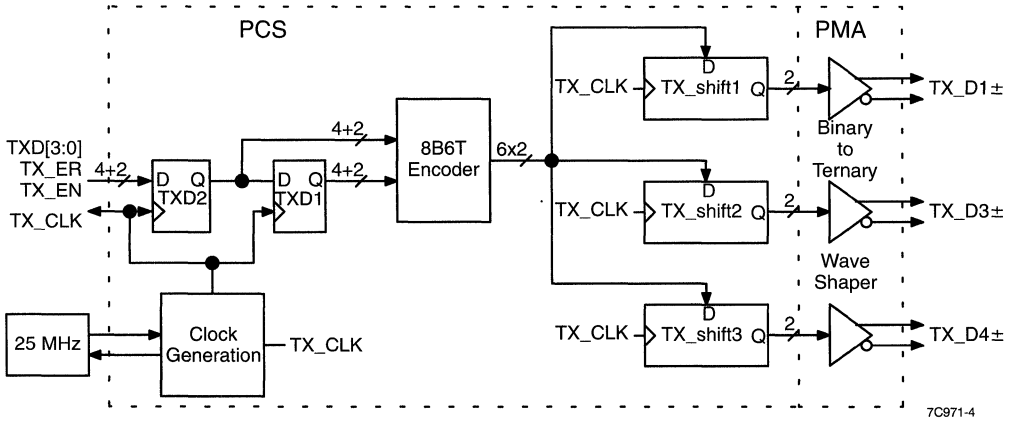


Figure 2. T4 Transmitter Block Diagram

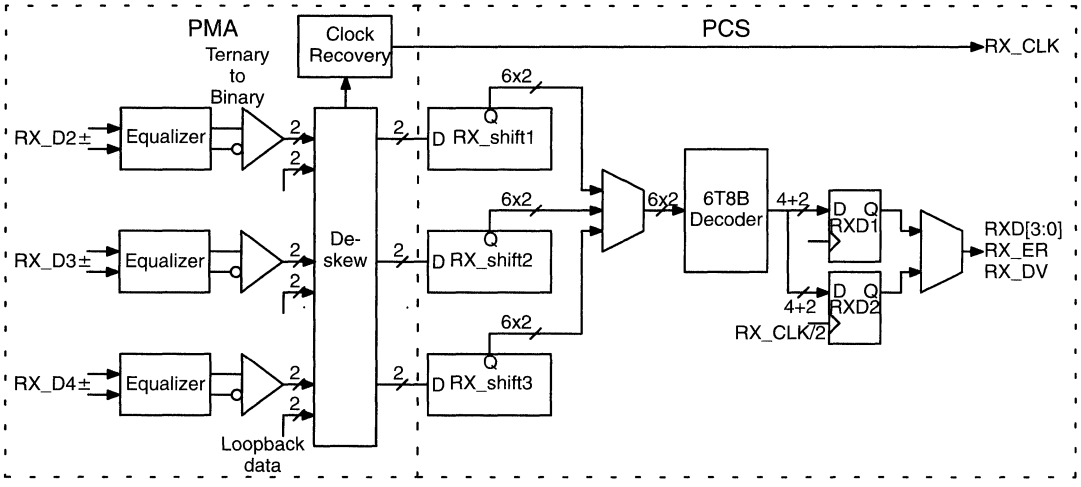


Figure 3. T4 Receiver Block Diagram

Transmit Physical Media Attachment (PMA)

The Transmit PMA converts the serial encoded 6T bits from the transmit PCS to their corresponding ternary waveforms. The waveshaper Digial to Analog Converter (DAC) generates high precision raised cosine waveforms on each transmission pair. The waveforms conform to the 100BASE-T4 output template specification. No external filters are required. The PMA output drivers interface to the media through external termination resistors and isolation transformers.

Receiver

The T4 receiver is comprised of the PCS and the PMA. *Figure 3* shows a block diagram of the receiver

Receive Physical Media Attachment (PMA)

The PMA receives serial 8B6T symbols from the twisted-pair interface and presents them to the PCS. The T4 receiver media interface features three adaptive equalizers. The equalizers compensate for the attentuation of high-frequency signals by up to 100 meters of category 3, 4, or 5 twisted-pair cable. The equalized waveforms are converted to binary form and passed to the clock recovery and data alignment blocks. The clock recovery circuit aligns the frequency and phase of RX_CLK with that of the received serial data. The data alignment block deskews the three receive channels.

Receive Physical Coding Sublayer (PCS)

The PCS accepts serial 8B6T symbols from the PMA, deserializes them, and then decodes the 8B6T code groups. Three shift registers convert the serial data back to parallel form. The first 8B6T code group is shifted into RX_shift1. The second 6T symbol group is shifted into RX_shift2 and the third into RX_shift3. The fourth code group is then shifted into RX_shift1. This process continues until the entire frame has been deserialized. The parallel 8B6T data are converted to 8-bit octets and latched into registers RXD1 and RXD2 on every other RX_CLK. The data is then presented at the MII interface in nibble form. RX_DV indicates that received data is present on the RXD[3:0] pins. RX_ER indicates that a receiver fault has occured.

Carrier Sense

The carrier sense function detects activity on the media using a smart squelch function similiar to 10BASE-T. The CRS signal is asserted HIGH when a valid carrier is detected on the pair RX_D2 according to the 10BASE-T4 draft standard. After detecting a valid carrier, an eop1 code group or seven consecutive zeros on RX_D2 must be detected before CRS is deasserted.

Collision Detection

A collision is detected when the transmitter is active simultaneously with the detection of a valid carrier by the carrier sense function. The MII COL signal will be asserted HIGH to signal the presence of a collision. When a collision is detected the TX_D2 and TX_D3 pair drivers turn off.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotation and normal operation.

10BASE-T

The CY7C971 provides a 10BASE-T physical layer interface for compatibility with existing 10-Mb/s Ethernet networks. 10BASE-T operation is automatically selected if Auto-Negotation established 10BASE-T as the highest common operating mode. The 10BASE-T transceiver can also be enabled manually by disabling Auto-Negotation and clearing the Speed Selection (0.13) bit in the MII Control Register. The $\overline{\text{LINKT}}$ pin indicates when 10BASE-T is the selected mode of operation and the 10BASE-T transceiver is in the link pass state. *Figure 4* shows a block diagram of the 10BASE-T transceiver.

During 10BASE-T operation, transmit and receive data are transfered over the MII interface in nibble wide groups. The TX_CLK and RX_CLK clocks are sourced from the PHY with a 2.5-MHz nominal clock rate. TX_EN qualifies incoming transmit data,and RX_DV qualifies receive data. In this mode, the MII complies with the IEEE MII specification for a 10-Mb/s interface.

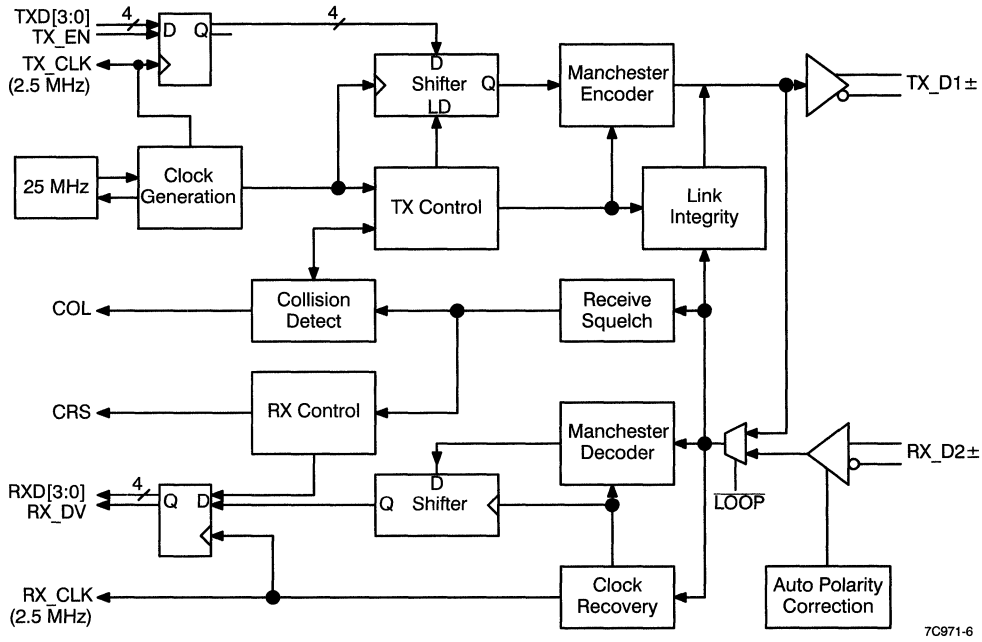


Figure 4. 10BASE-T Transmitter & Receiver Block Diagram

Full Duplex

The CY7C971 supports Full Duplex operation in 10BASE-T mode. 10BASE-T Full Duplex operation is automatically selected if Auto-Negotation established 10BASE-T Full Duplex as the highest common operating mode. The 10BASE-T Full Duplex operation can also be selected manually by disabling Auto-Negotation and clearing the Speed Selection (0.13) bit and setting the Duplex Mode Bit (0.8) in the MII Control Register. 10BASE-T Full Duplex mode cannot be enabled through Auto-Negotation or manually unless the the ENTFD pin is HIGH. The $\overline{\text{LINKFD}}$ pin indicates when 10BASE-T Full Duplex is the selected mode of operation and the 10BASE-T transceiver is in the Link Pass State. During full duplex operation, the collision pin (COL) is LOW.

Auto-Polarity Correction

The Auto-Polarity Correction function monitors the received signal polarity on RX_D2± and inverts the received signal internally if its polarity is inverted. Auto-Polarity Correction is active during Auto-Negotation and normal operation.

Media Independent Interface (MII)

The MII provides a connection between the PHY and the MAC and between the PHY and the station management (STA) entity. The MII is capable of supporting 100- and 10-Mb/s operation.

Data transfer is accomplished over nibble-wide dedicated transmit and receive channels. When TX_EN is asserted HIGH, data on TXD[3:0] channel is latched into the PHY on the rising edge of TX_CLK and passed to the PCS. If TX_ER is asserted HIGH, an 8B6T code violation word will be sent in place of the transmit data. TX_CLK provides a continuous clock that is sourced from the PHY.

When recovered data is available from the PCS, the RX_DV signal is asserted HIGH simultaneously with the first Start of Frame Delimiter (SFD) nibble on RXD[3:0]. The RX_DV signal remains HIGH continuously through the final recovered nibble of the frame. If an error is detected in the frame by the PHY, the RX_ER signal is driven HIGH synchronously with RX_CLK.

RX_CLK is a continuous clock that provides a timing reference for the transfer of RXD[3:0], RX_DV, and RX_ER from the PHY to the MAC. RX_CLK is sourced from the PHY. While RX_DV is deasserted, RX_CLK will run at the PHY's nominal frequency. When RX_DV is asserted, the frequency and phase of RX_CLK is recovered from the received data. During the transition from nominal to recovered frequency, the period of RX_CLK may extend by up to one cycle. RX_CLK stretching prevents logic failures from occuring in downstream logic while the clock makes it transition.

When a carrier is detected, the CRS signal is asserted HIGH. A collision is signaled by asserting COL HIGH. CRS is asserted throughout a collision condition.

Access to the management facilities are provided throught the MII with the MDC and MDIO pins. These pins provide a serial interface to the management control and status registers. The MDC signal is driven to the PHY from the management station (STA) as a timing reference for transfer of information on the MDIO signal. The MDIO signal is a bidirectional signal between the PHY and the STA. Control information is driven by the STA to the PHY. Status information is driven from the PHY to the STA.

Media Dependent Interface

The Media Interface is comprised of four communications channels. A dedicated transmit channel, TX_D1±, transmits 100BASE-T4 and 10BASE-T signals. RX_D2± is a dedicated receive channel for both 100BASE-T4 and 10BASE-T signals. The two bidirectional channels for 100BASE-T4 are formed from TX_D3±, RX_D3± and TX_D4±, RX_D4±.

The MDI pins interface to the medium through external resistors and isolation transformers. No external filters are required. The transmit drivers use class AB differential drivers to help reduce power consumption while providing ample drive capability. The drivers have a common mode control circuit to help reduce common mode emissions.

Management

The management facilities are used to control and indicate the status of the PHY resources. The management facilities and MII management interface is compliant with the IEEE 802.3 MII draft specification.

MII Management Interface

The management facilities are accessed through the MII management pins MDC and MDIO. The management facilities respond to register accesses that match the PHY address. The PHY address is assigned with the A[4:0] pins. The value of these pins are latched into the internal PHY address register on the rising edge of $\overline{\text{RESET}}$.

Register accesses are perfomed by transferring an opcode, address, and register number to the PHY management facility. If the address transferred matches the PHY address at the A0–A4 pins, the PHY responds to the access. During a read access, 16 bits of data from the selected register are transferred from the PHY to the STA on the MDIO pin. During a write, 16 bits of data are transferred from the STA to the PHY and written into the selected register.

Control and Status Registers

Control and status information are stored in two 16-bit registers. The Control register is assigned address 0 and the Status register is assigned address 1. *Table 1* shows a map of the Control register and *Table 2* shows the Status register.

Table 1. MII Control Register Definition[2]

Control Register (Register 0)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
0.15	Reset	1 = PHY Reset 0 = Normal Operation	R/W S/C	0	Resets the status and control registers to their default states. Reset is self clearing.
0.14	Loopback	1 = Loopback Mode 0 = Normal Operation	R/W	0	Loopback connects the transmit data path to the receive data path.
0.13	Speed Selection	1 = 100 Mb/s 0 = 10 Mb/s	R/W	1	When Auto-Negotiation is disabled, Speed Select determines the speed of the PHY.
0.12	Auto Negotiation Enable	1 = Enable Auto-Negotation 0 = Disable Auto-Negotiation	R/W	1	This bit enables the Auto-Negotiation function.
0.11	Power Down	1 = Power Down 0 = Normal operation	R/W	0	Power down shuts off the internal PLLs and core logic.
0.10	Isolate[3]	1 = Isolate PHY from MII 0 = Normal Operation	R/W	0, 1	Isolate places the receiver MII channel in high impedence, and the MII transmiter channel does not respond to MII activity.
0.9	RestartAuto-Negotiation	1 = Restart Auto-Negotiation 0 = Normal Operation	R/W S/C	0	Restart Auto-Negotiation breaks the link and restarts the Auto Negotiation process.
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	0	Duplex Mode selects between full and half duplex operation for 10BASE-T.
0.7	Collision Test	1 = Test COL Signal 0 = Normal Operation	R/W	0	Collision test causes the COL signal to be asserted when TX_EN is asserted.
0.6:0	Reserved			0	

Notes:
2. R/W = Read/Write
   SC = Self Cleaning
   RO = Read Only
   LH = Latched HIGH
3. Isolate default is set by the ISODEF pin.

Table 2. MII Status Register Definition

Status Register (Register 1)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
1.15[4]	100BASE-T4	1 = 100BASE-T4 Able 0 = 100BASE-T4 Able	RO	1,0	When set, this bit indicates that the PHY is 100BASE-T4 capable.
1.14	100BASE-TX Full Duplex	0 = 100BASE-TX Full Duplex Not Supported	RO	0	This bit is always set to zero.
1.13	100BASE-TX Half Duplex	0 = 100BASE-TX Half Duplex Not Supported	RO	0	This bit is always set to zero.
1.12[5]	10BASE-T Full Duplex	1 = 10BASE-T Full Duplex Able 0 = 10BASE-T Full Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T full duplex capable.
1.11[6]	10BASE-T Half Duplex	1 = 10BASE-T Half Duplex Able 0 = 10BASE-T Half Duplex Able	RO	1,0	When set, this bit indicates that the PHY is 10BASE-T half duplex capable.
1.10:6	Reserved	0 = Default	RO	0	
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation Complete 0 = Auto-Negotiation Incomplete	RO	0	This bit is set when NWAY has completed the auto negotiation process.
1.4	Remote Fault	1 = Remote Fault Condition 0 = No Remote Fault Condition	RO	0	This bit is set when Auto Negotiation detects a remote fault.
1.3[7]	Auto Negotiation Ability	1 = PHY is Able to Perform Auto Negotiation	RO	1,0	PHY supports Auto-Negotiation.
1.2	Link Status	1 = Link Is Up 0 = Link Is Down	RO	0	Link Status indicates that the PHY is in the Link Pass State.
1.1	Jabber Detect	1 = Jabber Condition Detected 0 = No Jabber Condition Detected	RO LH	0	Jabber Detect indicates that a jabber condition has been detected for 10BASE-T.
1.0	Extended Capabilities	1 = Extended Register Capable	RO	1	OUI and Auto-Negotiation Extended Registers 2–7 are present.

Vendor and Product ID Registers

Vendor and Product identification codes are stored in management ID registers 2 and 3. These registers contain the Cypress Semiconductor Corporation unique identifier and the CY7C971 product and revision number. *Table 3* explains the ID registers.

Auto-Negotation Registers

The Auto-Negotation process is managed through the Auto-Negotation registers. Register 4 is the Auto-Negotation Advertisement register. This register contains the 16-bit code word that is advertised to the remote link partner. Register 5 is the Auto-Negotation Link Partner Ability register for base and next pages. This register holds the 16-bit code word that the Auto-Negotation function receives from the remote link partner. Register 6 is the Auto-Negotation Expansion register and is used to monitor the negotiation process. Register 7 is the Auto-Negotation Next Page Transmit register. The function of the Auto-Negotation register bits are defined in *Tables 4* through *7*.

Auto-Negotation

The IEEE Auto-Negotation function provides remote capability detection and automatic speed selection. Auto-Negotation is fully compatible with existing 10BASE-T only devices.

Auto-Negotation advertises the capabilities of the PHY by transmitting a sequence of fast link pulses (FLPs) that form a standard 16-bit code word. The advertised code word is contained in the Auto-Negotation Advertisement register (Register 4). Auto-Negotation receives 16-bit code words and stores them in the Auto-Negotation Partner Ability register (Register 5). Once the code words have been sent and acknowledged, Auto-Negotation selects the highest common operating mode as the current mode of operation. The highest common mode of operation is determined by the Priority Resolution Table specified in the Auto-Negotation standard. When a mode of operation is selected, Auto-Negotation enables the transition to the selected mode's Link Pass state.

The Auto-Negotation process is controlled and monitored through the MII management registers. Auto-Negotation may be disabled in the MII control register or by asserting the AUTONEG pin HIGH.

The Auto-Negotation is capable of transmitting and receiving code word pages in addition to the base pages. The next page process is controlled through the MII registers.

Notes:

4. 100BASE-T4 Default is set by the ENT4 pin.
5. 10BASE-T FD Default is set by the ENTFD pin.
6. 10BASE-T HD Default is set by he ENT pin.
7. Auto-Negotiation Default is set by the AUTONEG pin.

Table 3. MII PHY ID Register Definition

PHY Identifier (Register 2 and 3)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
2.15:0	OUI PHY Identifier	16 Most Significant OUI Bits	RO	0028h	This field contains 16 bits of the Cypress Organizationally Unique Identifier (OUI).
3.15:10	OUI PHY Identifier	6 Least Significant OUI Bits	RO	02h	This field contains 6 bits of the Cypress Organizationally Unique Identifier (OUI).
3.9:4	Model Number	CY7C971 Model Number	RO	01h	This field contains a 6-bit model number.
3.3:0	Revision Number	CY7C971 Revision Number	RO	–	This field contains a 4-bit revision number.

Table 4. MII Auto-Negotation Advertisement Register Definition

Auto-Negotation Advertisement Register (Register 4)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
4.15	Next Page	1 = Next Page to be Transmitted 0 = No Next Page	R/W	0	When set, this bit will cause the PHY to advertise Next Page capability.
4.14	Reserved		RO	0	Reserved.
4.13	Remote Fault	1 = Fault Indication 0 = No Fault	R/W	0	When set, this bit will cause the PHY to advertise a Remote Fault has occured.
4.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
4.9[8]	Technology Ability Field 100BASE-T4	1 = Advertise 100BASE-T4 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 100BASE-T4 capability. This bit may only be set if 100BASE-T4 is enabled.
4.8	Technology Ability Field 100BASE-TX Full Duplex	0 = 100BASE-TX FD Not Supported	RO	0	This bit will always be zero. 100BASE–TX FD is not supported.
4.7	Technology Ability Field 100BASE-TX	0 = 100BASE-TX Not Supported	RO	0	This bit will always be zero. 100BASE–TX is not supported.
4.6[9]	Technology Ability Field 10BASE-T Full Duplex	1 = Advertise 10BASE-T FD 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T FD capability. This bit may only be set if 10BASE-T FD is enabled.
4.5[10]	Technology Ability Field 10BASE-T	1 = Advertise 10BASE-T 0 = Do Not Advertise	R/W	1,0	When set, this bit will cause the PHY to advertise 10BASE-T capability. This bit may only be set if 10BASE-T is enabled.
4.4:0	Selector Field	Indicates IEEE 802.3 LAN	RO	01h	This field is permanently set to 0001 to advertise IEEE 802.3 CSMA/CD LAN.

Notes:
8. 100BASE-T4 Advertised Ability default is set by the ENT4 pin.
9. 10BASE-T FD Advertised Ability default is set by the ENTFD pin.
10. 10BASE-T Advertised Ability default is set by the ENT pin.

Table 5. MII Auto-Negotation Link Partner Ability Register Definition

Auto-Negotation Link Partner Ability Register (Register 5)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
5.15	Remote Next Page	1 = Next Page to be Transmitted 0 = No Next Page	RO	0	When set, this bit indicates the remote PHY has a Next Page to send.
5.14	Remote Acknowledge	1 = Remote Acknowledge 0 = No Acknowledge	RO	0	When set, this bit indicates that the remote PHY has acknowledged receipt of a page.
5.13	Remote Fault	1 = Fault Indication 0 = No Fault	RO	0	When set, this bit indicates that a fault has ocurred in the remote PHY.
5.12	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.11	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.10	Technology Ability Field Reserved	Reserved	RO	0	Reserved.
5.9	Technology Ability Field 100BASE-T4	1 = 100BASE-T4 Able 0 = Not 100BASE-T4 Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-T4 capability.
5.8	Technology Ability Field 100BASE-TX Full Duplex	1 = 100BASE-TX FD Able 0 = Not 100BASE-TX FD Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX FD capability.
5.7	Technology Ability Field 100BASE-TX	1 = 100BASE-TX Able 0 = Not 00Base-TX Able	RO	0	When set, this bit indicates that the remote PHY has 100BASE-TX capability.
5.6	Technology Ability Field 10BASE-T Full Duplex	1 = 10BASE-T FD Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T FD capability.
5.5	Technology Ability Field 10BASE-T	1 = 10BASE-T Able 0 = Not 10BASE-T Able	RO	0	When set, this bit indicates that the remote PHY has 10BASE-T capability.
5.4:0	Selector Field	Indicates LAN Type	RO	00h	This field indicates the type of LANs being advertised by the remote PHY.

Table 6. MII Auto-Negotation Expansion Register Definition

Auto Negotiation Expansion Register (Register 6)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
6.15:5	Reserved	Reserved	RO	0	Reserved.
6.4	Parallel Detection Fault	1 = Parallel Detection Fault 0 = No Parallel Detection Fault	RO LH	0	When set, this bit indicates that local Auto-Negotation has detcted more than one valid link.
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is Not Next Page Able	RO	0	When set, this bit indicates that the remote PHY supports Next Page capability
6.2	Next Page Able	1 = Next Page Able	RO	1	This bit indicates that local Auto-Negotation supports Next Page capability.
6.1	Page Received	1 = 3 Identical Code Words Received 0 = 3 Identical Code Words Have Not Been Received	RO LH	0	When set, this bit indicates that local Auto-Negotation has received three consecutive and identical code words.
6.0	Link Partner Auto Negotiation Able	1 = Link Partner is Auto-Negotiation Able 0 = Link Partner is Not Auto-Negotiation Able	RO	0	When set, this bit indicates that the remote PHY has Auto-Negotation capability.

Table 7. MII Auto-Negotation Next Page Transmit Register Definition

Auto-Negotation Next Page Transmit Register (Register 7)					
Bit(s)	**Name**	**Setting**	**R/W**	**Default**	**Description**
7.15	Next page	1 = More Pages Follow 0 = Last Page	R/W	0	When set, this bit indicates that more pages follow. When clear, it indicates that the last page is being sent.
7.14	Reserved		RO	0	
7.13	Message Page	1 = Message Page 0 = Unformatted Page	R/W	0	When set, this bit indicates that the next page being sent is formatted as a message page.
7.12	Acknowledge 2	1 = Will Comply 0 = Cannot Comply	RO	1	When set, this bit indicates that the device can comply with the received message.
7.11	Toggle	1 = Previous Toggle Was Zero 0 = Previous Toggle Was One	RO	0	This bit is used to ensure synchronization with the link partner during next page exchange.
7.10:0	Message/Unformatted Code Field	Eleven-Bit Field	R/W	000h	This field contains the message/unformatted bits for the next page.

Loopback

In Loopback Mode, the transmit PMA circuits are isolated from the media and are connected to the receive PMA circuits. Transmit data flows from the MII through the PCS and into the PMA. The serial data is then looped back through the Receiver PMA and PCS to the MII interface. Loopback Mode is useful for checking the integrity of the PHY and MAC operations.

Loopback Mode is enabled by either setting the Loopback bit in the Management Control register to one or by asserting the $\overline{\text{LOOP}}$ pin LOW.

PMA Mode

When the MODE pin is LOW, the CY7C971 is in 100BASE-T4 PMA mode. This mode of operation is intended for use in repeater applications. In PMA mode, the PCS is bypassed exposing the PMA sublayer. Binary encoded 6T symbols are transfered directly over the PMA interface pins. This reduces the transmitter latency for use in class 1 and class 2 repeaters. A block diagram of the PMA interface is shown in *Figure 5*. 10BASE-T is disabled in the Status register.

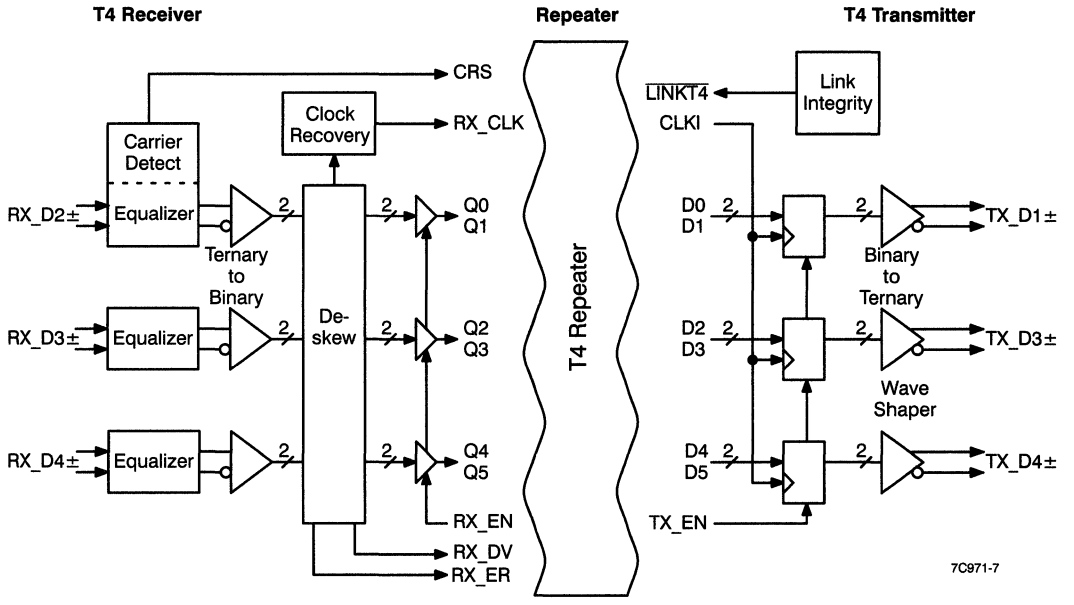


Figure 5. T4 Transmitter & Receiver PMA Interface and Block Diagram (MODE = LOW)

Serial 6T data from the three PMA circuits are transferred over the PMA interface pins in binary form. The Receiver aligns and converts the line signals to their 6T binary representation and drives them to the Q[5:0] pins. The transmitter latches the three 6T symbol streams on its D[5:0] input pins on the rising edge of TX_CLK. The 6T symbols are loaded into the waveshaper DAC and converted to their corresponding ternary waveforms. *Table 8* shows the mapping of binary PMA signals to ternary waveforms.

Table 8. PMA Binary to Ternary Map[11]

PMA Q1–0, Q3–2, Q5–4 D1–0, D3–2, D5–4	Transmitter	Receiver
00	CS0	CS0
10	CS1	CS1
01	CS–1	CS–1
11	CS0	–

Notes:
11. CS0 is a waveform which conveys the ternary symbol 0.
CS1 is a waveform which conveys the ternary symbol 1.
CS–1 is a waveform which conveys the ternary symbol –1.

The RX_DV signal indicates when the first data symbol after sosb is present on the Q0–5 PMA interface pins. RX_DV will remain HIGH throughout the transfer of data symbols across the PMA interface. RX_DV is LOW when there is no carrier present. RX_ER HIGH indicates a pair alignment error. The RX_EN input pin enables the Q0–5, RX_DV, and RX_ER drivers. RX_EN LOW places the drivers in the high-impedence state.

The transmit PMA interface is synchronous to the CLKI input clock signal. The TX_EN HIGH causes data on the PMA D0–5 pins to be loaded into the transmit PMA waveshaper on the rising edge of CLKI. When TX_EN is LOW, the output drivers transmit the CSO idle symbols.

Applications

The CY7C971 is a flexible physical-layer device that fits into any Ethernet application including network interface cards, transceiver cards, repeaters, hubs and switches. *Figure 6* shows a schematic of the CY7C971 configured for a transceiver card application with an exposed MII port.

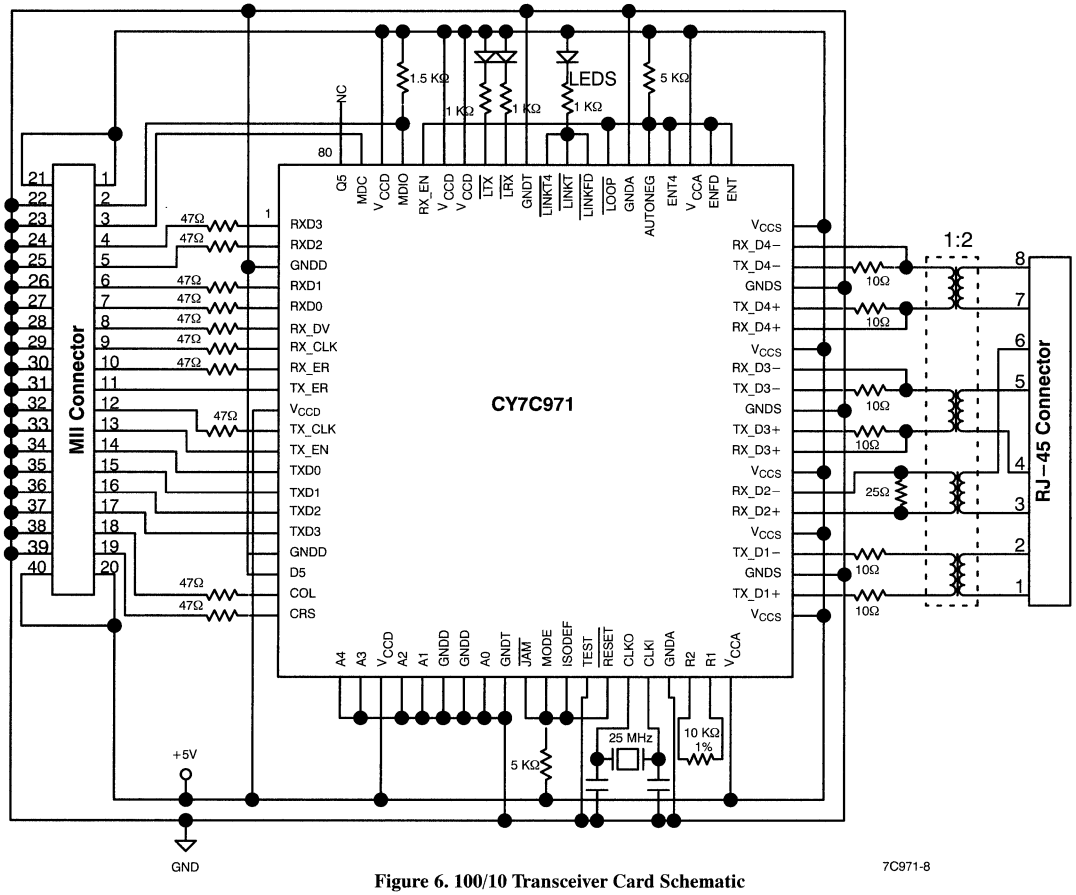


Figure 6. 100/10 Transceiver Card Schematic

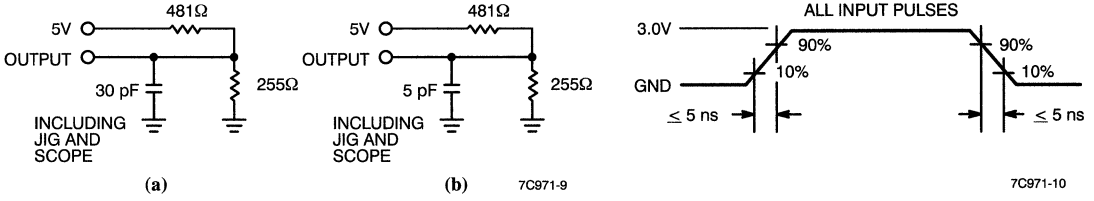
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
TTL Pins					
V_{OHT}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OLT}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IHT}	Input HIGH Voltage		2.0	6.0	V
V_{ILT}	Input LOW Voltage		−3.0	0.8	V
I_{IXT}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZT}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	μA
I_{OST}	Output Short Circuit Current[12]	V_{CC} = Max., V_{OUT} = GND		−350	mA
Open Drain LED Pins					
V_{OLD}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4	V
Miscellaneous					
I_{CC1}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, 100BASE-T4 transmitting		300	mA
I_{CC2}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, 100BASE-T4 not transmitting		100	mA
I_{SB}	Power-Down Current	Max. V_{CC}		TBD	mA

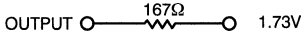
Capacitance[13]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:
12. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
13. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	Min.	Max.	Unit
MII Timing				
$t_{TCPWHT4}$	TX_CLK Pulse Width HIGH (T4)	14	26	ns
$t_{TCPWLT4}$	TX_CLK Pulse Width LOW (T4)	14	26	ns
t_{TCPWHT}	TX_CLK Pulse Width HIGH (T)	194	206	ns
t_{TCPWLT}	TX_CLK Pulse Width LOW (T)	194	206	ns
t_{TDS}	TXD Set Up	10		ns
t_{TDH}	TXD Hold	0		ns
t_{TMIIT4}	Transmit Latency (T4)		110	ns
t_{TMIIT}	Transmit Latency (T)		500	ns
$t_{TCRSHT4}$	Transmit Path CRS Assert (T4)		20	ns
t_{TCRSHT}	Transmit Path CRS Assert (T)		20	ns
$t_{TCRSLT4}$	Transmit Path CRS Deassert (T4)		320	ns
t_{TCRSLT}	Transmit Path CRS Deassert (T)		100	ns
$t_{RCPWHT4}$[15]	RX_CLK Pulse Width HIGH	14	26	ns
$t_{RCPWLT4}$[15]	RX_CLK Pulse Width LOW	14	26	ns
t_{RCPWHT}[15]	RX_CLK Pulse Width HIGH	194	206	ns
t_{RCPWLT}[15]	RX_CLK Pulse Width LOW	194	206	ns
t_{RDV}	RXD Valid from Clock		18	ns
t_{RDH}	RXD Hold from Clock	10		ns
t_{RXDVT4}	RXD Valid Latency (T4)		870	ns
t_{RXDVT}	RXD Valid Latency (T)		500	ns
$t_{RXDATAT4}$	RXD Latency (T4)		950	ns
$t_{RXDATAT}$	RXD Latency (T)		8700	ns
t_{RHZD}	RX_EN HIGH to Valid Data		15	ns
t_{RDHZ}	RX_EN LOW to High Impedance		20	ns
100BASE-T4 CRS and COL				
t_{CRSH}[16]	CRS Assert Latency for Preamble	110	140	ns
t_{CRSLC}[17]	CRS Deassert Latency for EOC		370	ns
t_{CRSLE}[18]	CRS Deassert Latency for EOP		370	ns
t_{COLH1}[19]	COL Assert Latency from TX_EN HIGH		20	ns
t_{COLL1}[20]	COL Deassert Latency from TX_EN LOW		20	ns
t_{COLH2}[21]	COL Assert Latency from Preamble		190	ns
t_{COLL2}[22]	COL Deassert Latency from EOC or EOP		370	ns

Notes:

14. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
15. During clock transition, clock max time could be as long as an entire cycle.
16. t_{CRSH} is measured from the rising edge of the latest arriving signal of the three pair that meets the 100BASE-T4 squelch criterion to the rising edge of CRS. The rising and falling edges of CRS are guarenteed to meet the fairness timing specification defined in the 100BASE-T4 standard.
17. t_{CRSLC} is measured from the end of the last data symbol on RX_D2 to the falling edge on CRS. Seven consecutive zeros must be received on RX_D2 in order for the PMA to recognize loss of carrier.
18. t_{CRSLE} is measured from the begining of the first symbol of EOP1 on any RX_Dx MDI pair accounting for skew to the falling edge on CRS. Detection of a properly framed EOP1 will cause the PCS to recognize loss of carrier.
19. t_{COLH1} is measured from the rising edge of TX_CLK while TX_EN is HIGH to the rising edge of COL.
20. t_{COLL1} is measured from the rising edge of TX_CLK while TX_EN is LOW to the falling edge of COL.
21. t_{COLH2} is measured from the rising edge of the signal on RX_D2 that meets the 100BASE-T4 unsquelch criterion to the rising edge of COL.
22. t_{COLL2} is measured from the first symbol of the EOP or EOC sequences to the falling edge of COL.

Switching Characteristics Over the Operating Range (continued)

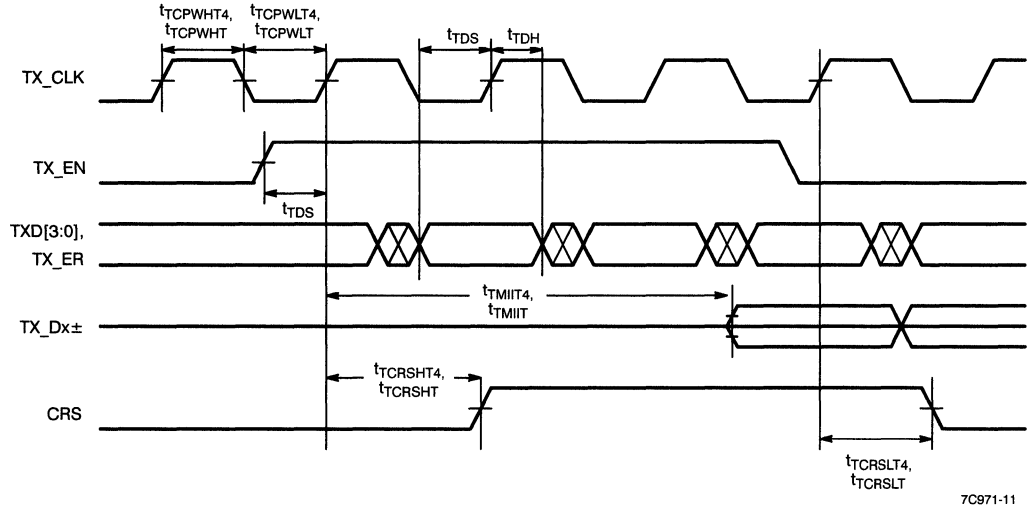
Parameter	Description	Min.	Max.	Unit
10BASE-T CRS and COL				
t_{CRSH3}[23]	CRS Assert Latency		500	ns
t_{CRSL3}[24]	CRS Deassert Latency		500	ns
Management Timing				
t_{MCPWH}	MDC Pulse Width HIGH	25		ns
t_{MCPWL}	MDC Pulse Width LOW	25		ns
f_M	MDC Frequency		12.5	MHz
t_{MDS}	MDIO Set-Up	10		ns
t_{MDH}	MDIO Hold	0		ns
t_{MDO}	MDIO Valid from Clock		40	ns
t_{MDOH}	MDIO Hold from Clock	0		ns
t_{MDHZ}	MDC to High Impedance		40	ns
t_{MDLZ}	MDC to Low Impedance	0	20	ns
Control and Status Timing				
t_{RL}	Reset Pulse Width LOW	5		µs
t_{RS}	Control Input Set-Up	100		ns
PMA Interface Timing				
t_{TPMA}	PMA Transmit Latency		40	ns
t_{TDS}	PMA Transmit Data Set Up	10		ns
t_{TDH}	PMA Transmit Data Hold	0		ns
$t_{PMACRSH}$	PMA CRS Assert Latency	110	140	ns
$t_{PMACRSL}$	PMA CRS Deassert Latency		650	ns
$t_{PMADATA}$	PMA Receiver Data Latency		800	ns
Clock Timing				
t_{CPWH}	Reference Clock Pulse Width HIGH	16	24	ns
t_{CPWL}	Reference Clock Pulse Width LOW	16	24	ns
f_C	Reference Clock Frequency	25 − 100 ppm	25 + 100 ppm	MHz

Notes:

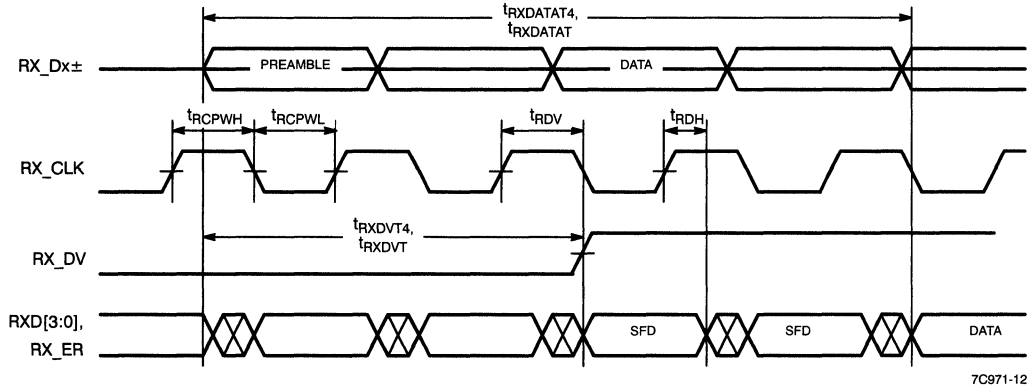
23. t_{CRSH3} is measured from the rising edge of the signal on RX_D2 that meets the 10BASE-T carrier criterion to the rising edge of $\overline{CRS}$.
24. t_{CRSL3} is measured from th eend of the last data symbol on RX_D2 to the falling edge of CRS.

Switching Waveforms

MII Transmit Port Data Timing[25]



MII Receive Port Data Timing[26, 27]

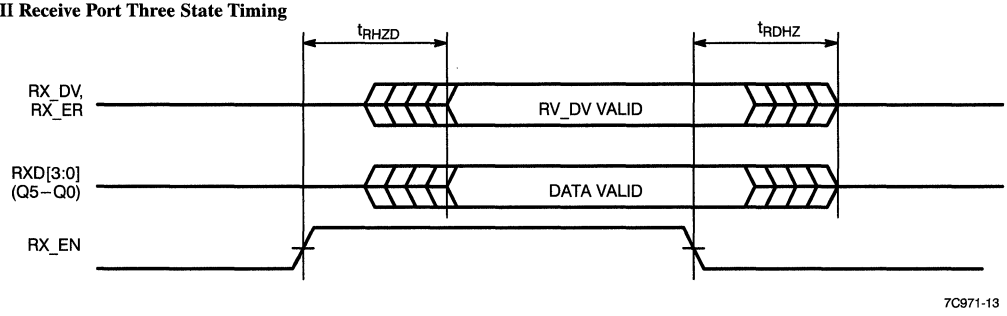


Notes:

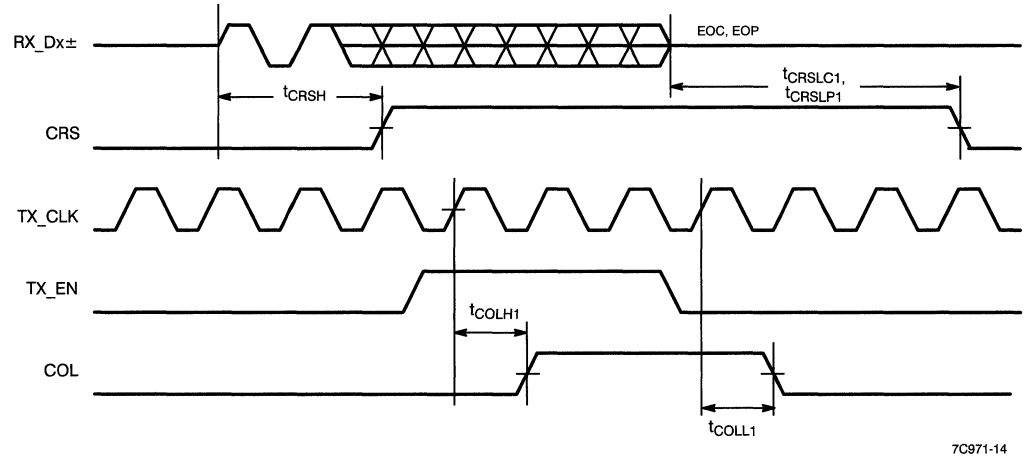
25. t_{MII} is measured from the rising edge of TX_CLK to the 50% point of the TX_Dx± outputs at the MDI pins.
26. t_{RXDV} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of RX_DV. This includes up to 64 bits of preamble and SFD plus the latency of the receive circuitry.
27. t_{RXDATA} is measured from the first rising edge of the preamble at the MDI input pins to the rising edge of valid data at the RXD pins. This includes up to 64 bits of preamble and SFD plus the first 8 bits of data and the latency of the receive circuitry.

Switching Waveforms (continued)

MII Receive Port Three State Timing

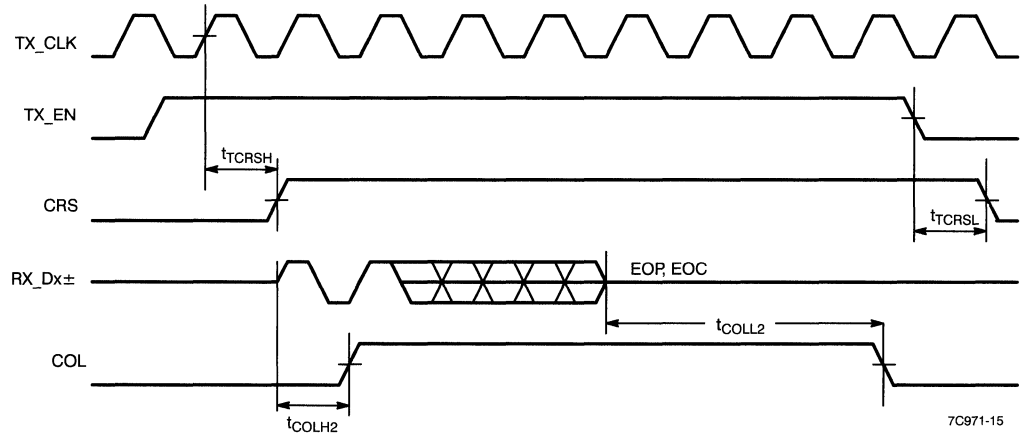


MII Carrier Sense and Collision (100BASE-T4)

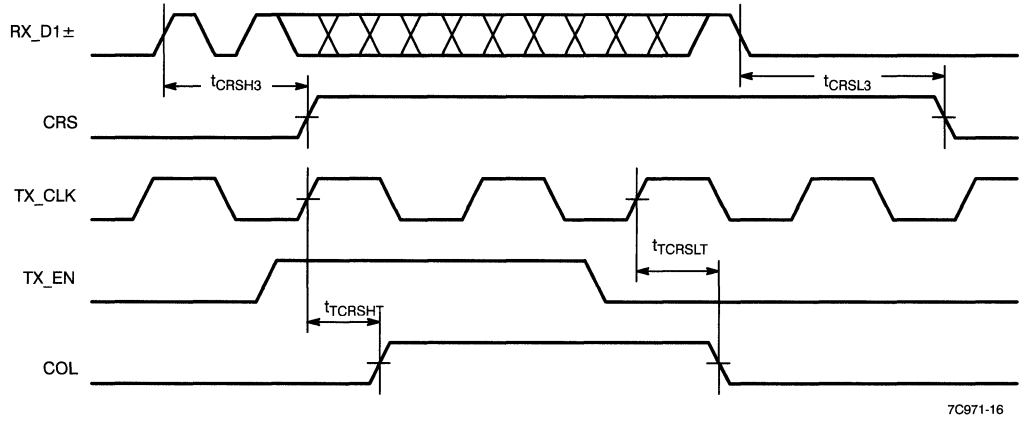


Switching Waveforms (continued)

MII Carrier Sense and Collision (100BASE-T4)



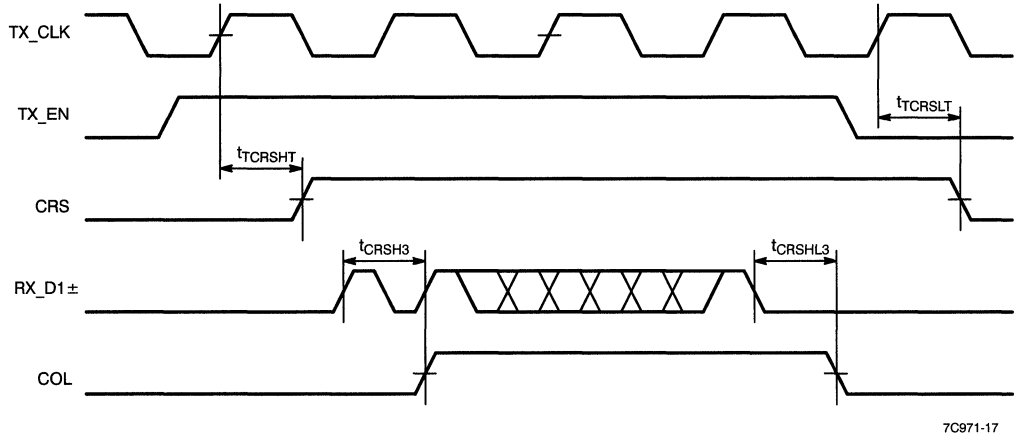
MII Carrier Sense and Collision (10BASE-T) [28]



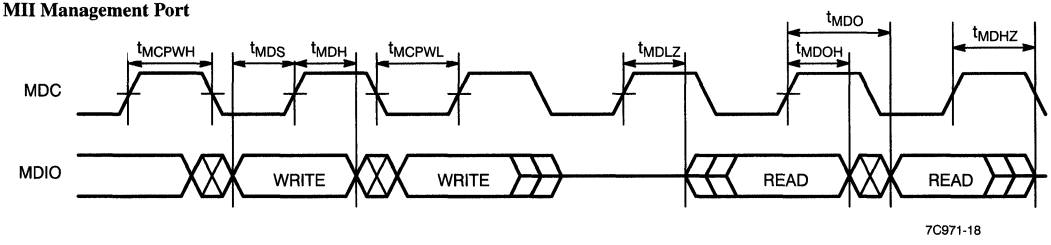
Notes:
28. Switching waveforms show CRS and COL timing for a colision that is started and terminated by the transmit path (TX_EN HIGH).

Switching Waveforms (continued)

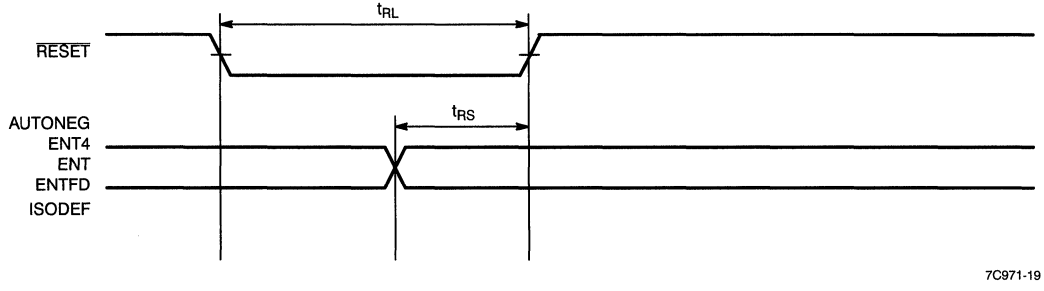
MII Carrier Sense and Collision (10BASE-T) [29]



MII Management Port



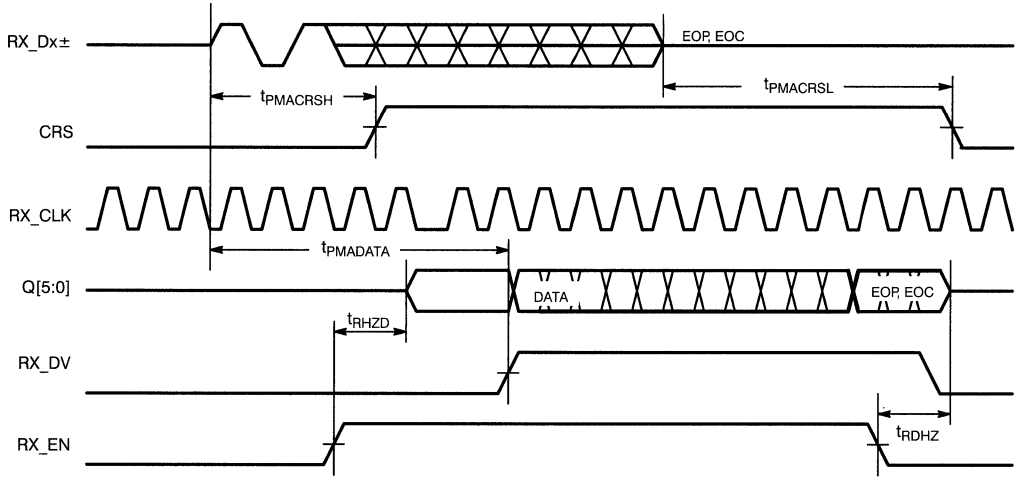
Control and Status Pins



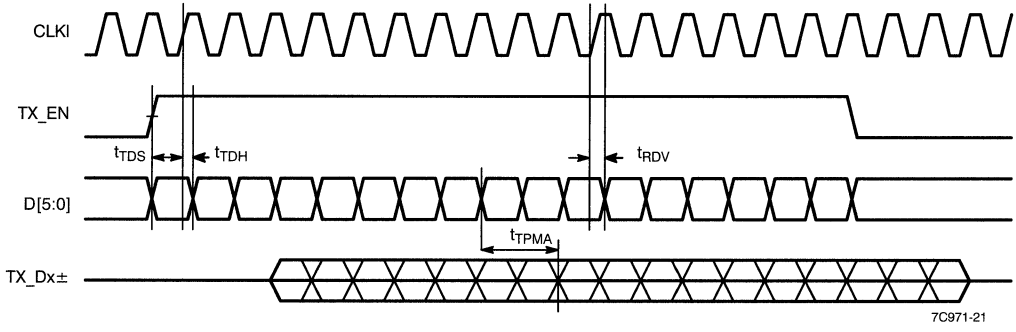
Notes:
29. Switching waveforms show CRS and COL timing for a collision that is started and terminiated by activity on the receive path.

Switching Waveforms (continued)

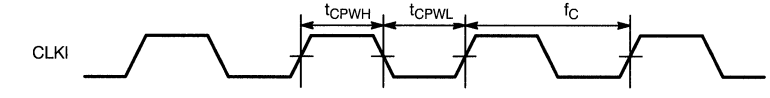
PMA Receiver Interface (MODE = LOW)



PMA Transmitter Interface (MODE = LOW)



Reference Clock Pins



Document #: 38−00415

Ethernet Coax Transceiver Interface

Features

- **Compliant with IEEE802.3 10BASE5 and 10BASE2**
- **Pin compatible with the popular 8392**
- **Internal squelch circuit to eliminate input noise**
- **Hybrid mode collision detect for extended distance**
- **Automatic AUI port isolation when coaxial connector is not present**
- **Low power BiCMOS design**
- **16-Pin DIP or 28-Pin PLCC)**

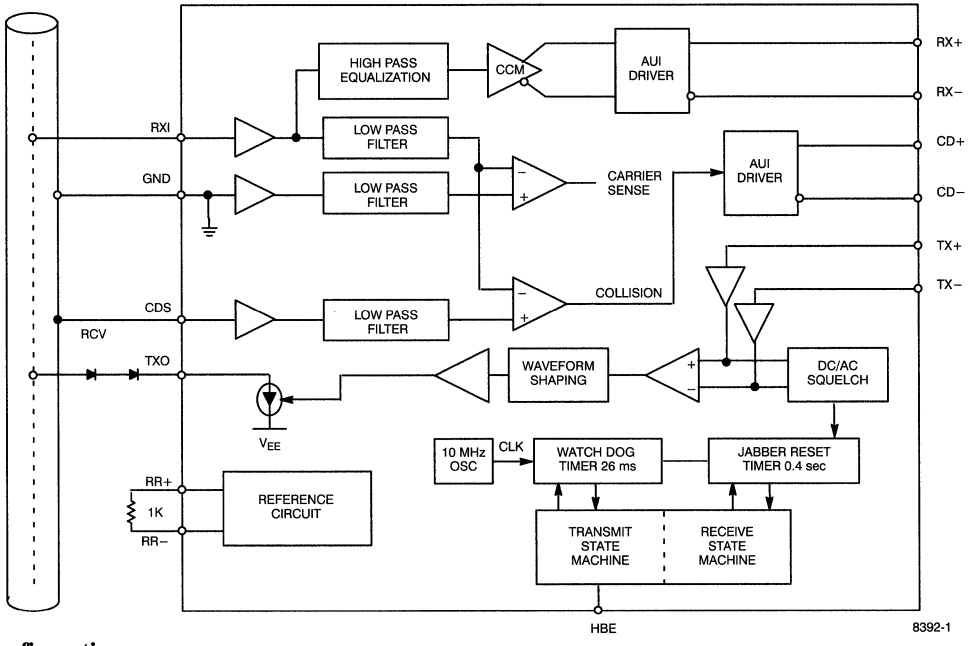
Functional Description

The CY7B8392 is a low power coaxial transceiver for Ethernet 10BASE5 and 10BASE2 applications. The device contains all the circuits required to perform transmit, receive, collision detection, heartbeat generation, jabber timer and attachment unit interface (AUI) functions. In addition, the CY7B8392 features an advanced hybrid collision detection.

The transmitter output is connected directly to a double terminated 50Ω cable.

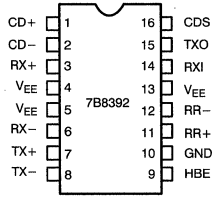
The CY7B8392 is fabricated with an advanced low power BiCMOS process. Typical standby current during idle is 25 mA.

Logic Block Diagram



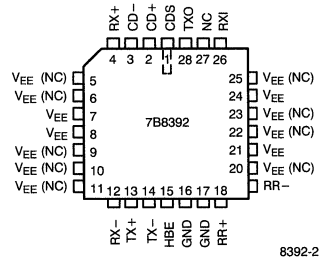
Pin Configurations

DIP
Top View



8392-3

PLCC
Top View



8392-2

Pin Description

Pin Number		Pin Name	Description
16-Pin DIP	28-Pin PLCC		
1 2	2 3	CD+ CD−	AUI Collision Output pins. Differential driver that transmit a 10-MHz signal during collision events, jabber and CD Heartbeat conditions. Also referred to as CI port.
3 6	4 12	RX+ RX−	AUI Receive Output pins. Differential driver that outputs the signal receive from the line. Also referred to as DI port.
7 8	13 14	TX+ TX−	AUI Transmit Input pins. Differential receiver that inputs the signal for transmission onto the cable.
9	15	HBE	Heartbeat Enable Pin. When this pin is grounded, the heartbeat is enabled. When the pin is connected to V_{EE}, the heartbeat is disabled.
11 12	18 19	RR+ RR−	External Resistor. A 1K 1% resistor should be connected between these pins to establish proper internal operation current.
14	26	RXI	Receive Input. This pin is connected directly to the coaxial cable.
15	28	TXO	Transmitter Output. This pin is connected directly (10BASE2 thin wire) or through a diode to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detect circuit. This pin should be connected separately to the shield to prevent ground drops from altering the receive mode collision detect threshold.
10	16,17	GND	Positive Power Supply Pin.
4,5,13	5−11, 20−25	V_{EE}	Negative Power Supply Pin.

CY7B8392 Description

Transmitter

The CY7B8392 transfers Manchester-encoded data from the AUI port of the DTE (TX+ and TX−) to the coaxial cable. The output waveform is wave shaped to meet IEEE 802.3 specifications. For Ethernet compatible applications (10BASE5), an external isolation diode should be added to further reduce the coax load capacitance.

The AUI squelch circuit prevents signals with less than 15 ns pulse width or smaller than 225 mV in amplitude from reaching the output driver. The squelch circuit also turns the transmitter off at the end of the packet if the amplitude remains less than 225 mV for more than 190 ns.

Receiver

The CY7B8392 receiver transfers the serial data from the coaxial cable to the DTE via the balanced differential output (RX+ and RX−). The received signal is amplified and equalized by the on chip equalizer.

The device also contains an internal squelch function that discriminates noise from valid data. A 4-pole Bessel filter is used to extract the DC level of the received signal. If the DC level of the received signal is lower than an internally set squelch threshold, the CY7B8392 receive function will not be activated.

Collision Detection

The collision detection circuit monitors the signal level on the coax cable. This signal voltage level is compared against the collision voltage threshold V_{CD}. When the measured signal level is more negative than V_{CD}, a collision condition is declared by the CY7B8392 by sending a 10-MHz signal over the CD+/CD− pair.

Long Cable Application

The IEEE 802.3 standard is designed for 500 meters of Ethernet cable and 185 meters of thin coax cable (RG58A/U). To extend the cable segment to 1000 meters and 300 meters of Ethernet cable and thin coaxial cable respectively, transmit collision detection mode is required. The disadvantage of ordinary transmit collision detection mode is that it will detect collision only when the station is transmitting; it will not be able to detect collision of two far-end stations when it is not transmitting. Transmit mode collision detection is not allowed in repeater applications.

The CY7B8392 utilizes a hybrid combination of receive and transmit collision detection. When the device is not transmitting, the unit automatically sets the collision threshold voltage to the smaller (less negative) receive level. This allows collision detection of two far end stations while the unit is not transmitting. If the unit enters the transmit mode, the collision detection threshold is automatically changed to the larger (more negative) transmit collision detection threshold. This feature eliminates the need for an external voltage divider at the input of CDS when using the 1000 meters and 300 meters of Ethernet and thin coaxial cable length, respectively.

Heartbeat Test Function

The Heartbeat Test Function is enabled when the HBE pin is tied to ground. When enabled, a 10-MHz collision signal is transmitted to the MAC over the CD+/CD− pair after the transmission of a packet for 10±5BT[1]. The Heartbeat function should be disabled by tying the HBE pin to V_{EE} for repeater applications.

Note:

1. BT = Bit Time = 100 ns.

Jabber Function

The on-chip watchdog timer prevents the DTE from locking up a network by transmitting continuously. When the transmission exceeds the jabber time limit, the Jabber function disables the transmitter and sends a 10-MHz signal over the CD± pair. Once the transmitter is in the jabber state, it must remain in the idle state for 500 ms before it will exit the jabber state.

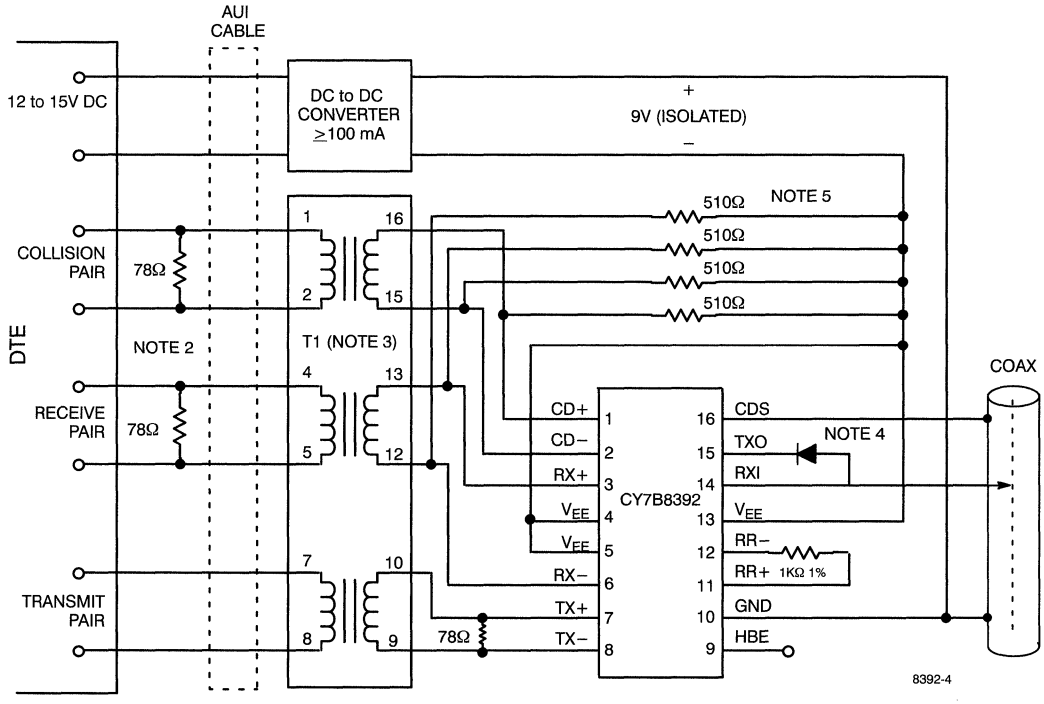
AUI Function

The CY7B8392 Auto AUI function will isolate the AUI port when coaxial cable is not present. Initially, during power-up, the CI and DI ports of the AUI are high impedance. The CY7B8392 monitors the average DC level at the RXI input and determines if a properly terminated coaxial segment is attached. While RXI is unterminated the AUI port will remain powered down. The AUI port will only be activated when RXI is connected to a terminated coaxial segment.

When the RXI input becomes unterminated (after power-up), a 10-MHz signal is transmitted over the CI circuit for 800 ms with the DI port disabled. After the transmission of the 10-MHz signal, the CI port is disabled.

This function allows multiple MAUs to be connected to a single AUI port without having to turn off the coaxial transceiver manually.

Connection Diagram for Standard CY7B8392 Applications



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage ..... −12V

Input Voltage ..... GND+0.3V to V_{EE}−0.3V

Operating Range

Range	Ambient Temperature	V_{EE}
Commercial	0°C to +70°C	−9V ± 5%

Notes:

2. 78Ω resistors not required if AUI cable not present.
3. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100 μH.
4. IN916 or equivalent.
5. Resistors may be as small as 510Ω; larger values may be used to reduce power dissipation.

Electrical Characteristics Over the Operating Range[6]

Parameter	Description	Min.	Typ.	Max.	Unit
V_{EE}	Supply Voltage	−8.55	−9.0	−9.45	V
I_{EE1}	(V_{EE} to GND) Non-transmitting[7]		−25	−35	mA
I_{EE2}	(V_{EE} to GND) Transmitting		−70	−80	mA
I_{MAU}	Input Bias Current (RXI and T_{XO} pin)	−2		25	μA
I_{TDC}	Transmitter Output DC Current	37	41	45	mA
I_{TAC}	Transmitter AC Current	±28			mA
V_{CD}	Collision Threshold (Receive Mode)	−1.45	−1.53	−1.62	V
V_{CS}	Carrier Sense Threshold	−0.42		−0.60	V
RX, CD	Differential Output Voltage	±475		±1500	mV
V_{OC}	Common Mode Voltage[8] (DI and CI ports)		−3.5		V
V_{TS}	Transmitter Squelch Threshold[9]	−175	−225	−300	mV
R_{RXI}	Shunt Resistance—Non-transmitting[10]	100			KΩ
R_{TXO}	Shunt Resistance—Transmitting[10]	10			KΩ

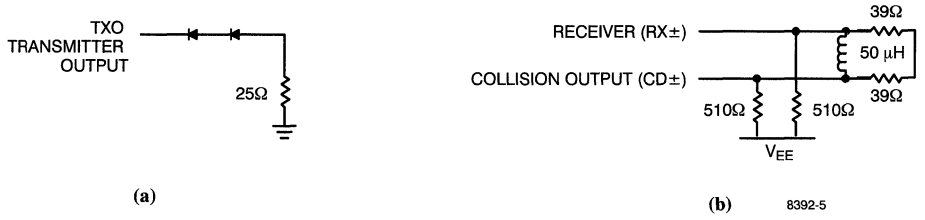
Capacitance

Parameter	Description	Test Conditions	Typ.	Unit
C_X	Input Capacitance	Guaranteed by Design	1.5	pF

Notes:
6. Testing is done under test load as defined in AC Test Loads and Waveforms.
7. Not including current through external pulldown resistors.
8. During idle, V_{OC} is reduced to minimize the power dissipation across the load resistors connected to RX± and CD±.
9. For a minimum pulse width of >40 ns.
10. To measure shunt resistance, the pin (RXI or TXO) is terminated to 0 volts and the current is measured, then the pin is forced to −2 volts and the current is measured. The resistance is found by:

$$R = \frac{\Delta V}{\Delta I} = \frac{2V}{I_{(0V)} - I_{(-2V)}}$$

AC Test Loads and Waveforms



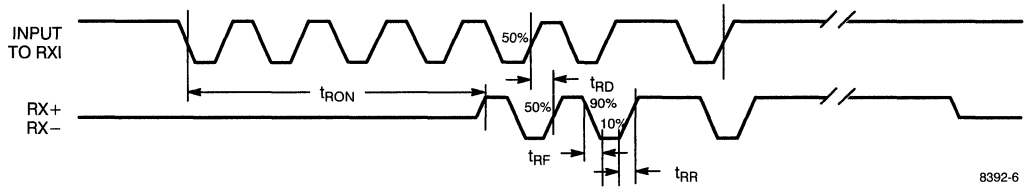
Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Typ.	Max.	Unit
t_{RON}	Receiver Start-Up Delay		2.5	5	bits
t_{RD}	Receiver Propagation Delay		25	50	ns
t_{RR}	Differential Output Rise Time (RX±, CD±)		4	7	ns
t_{RF}	Differential Output Fall Time (RX±, CD±)		4	7	ns
t_{RJ}	Receiver and Cable Total Jitter		±2		ns
t_{TST}	Transmitter Start-Up Delay		1	2	bits
t_{TD}	Transmitter Propagation Delay		25	50	ns
t_{TR}	Transmitter Output Rise Time (TXO)	20	25	30	ns
t_{TF}	Transmitter Fall Time (TXO)	20	25	30	ns
t_{TM}	t_{TR} and t_{TF} Mismatch		±0.5	±3	ns
t_{TS}	Transmit Skew (TXO)		±0.5	±2	ns
t_{TON}	Transmit Turn-On Pulse Width at V_{TS} (TX±)[11]	10	20	40	ns
t_{TOFF}	Transmit Turn-Off Delay	130	200	300	ns
t_{CON}	Collision Turn-On Delay		7	13	bits
t_{COFF}	Collision Turn-Off Delay			20	bits
f_{CD}	Collision Frequency	8.5	10	12.5	MHz
t_{CD}	Collision Pulse Width	40	50	60	ns
t_{HON}	CD Heartbeat Delay	0.6	1.1	1.6	µs
t_{HW}	CD Heartbeat Duration	0.5	1.0	1.5	µs
t_{JA}	Jabber Activation Delay	20	26	32	ms
t_{JR}	Jabber Reset Time Out	300	420	550	ms

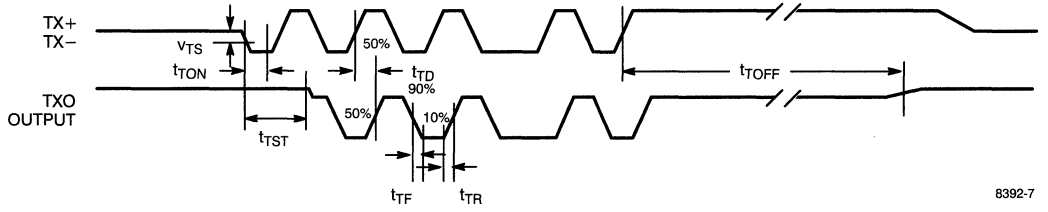
Note:
11. For a minimum pulse amplitude of >300 mV.

Switching Waveforms

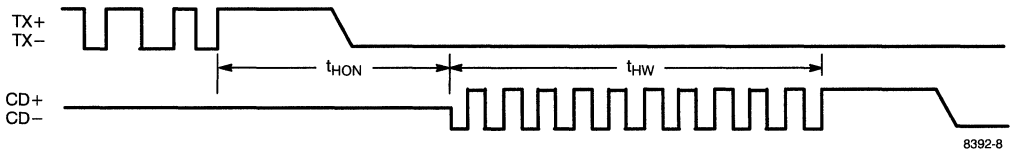
Receiver Timing



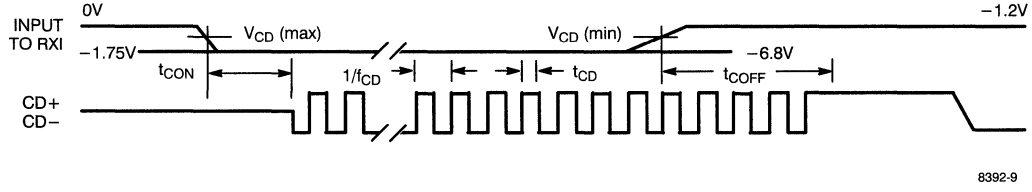
Transmit Timing



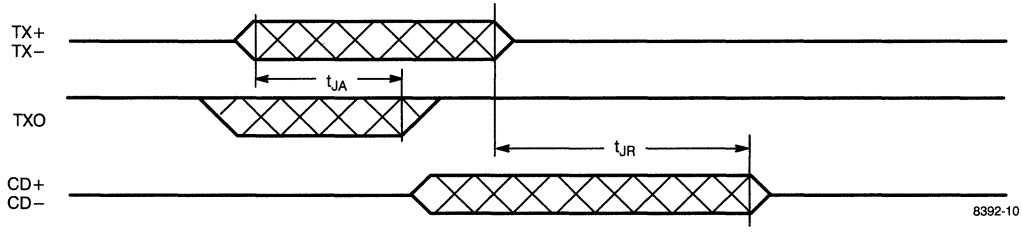
Heartbeat Timing



Collision Timing



Jabber Timing



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B8392–JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B8392–PC	P1	16-Lead (300-Mil) Molded DIP	

Document #: 38–00430–B

CY7B4663

Integrated 10BASE-FL Ethernet Transceiver

Features

- **Single chip Ethernet solution**
- **Complies with IEEE 802.3 10BASE-FL standard**
- **Pin compatible with the popular 4663**
- **110 mA LED current drive capability**
- **AUI interface allows both transformer and capacitive coupling**
- **Requires single 5 volt ±10% supply**
- **No external crystal or clock required**
- **Five network status LED pins**
- **28 pin PLCC package**
- **1 MHz idle signal, Jabber function, and SQE Test with enable/disable function integrated on chip**
- **Receive squelch function**
- **Integrated data quantizer**
- **Low power BiCMOS design**

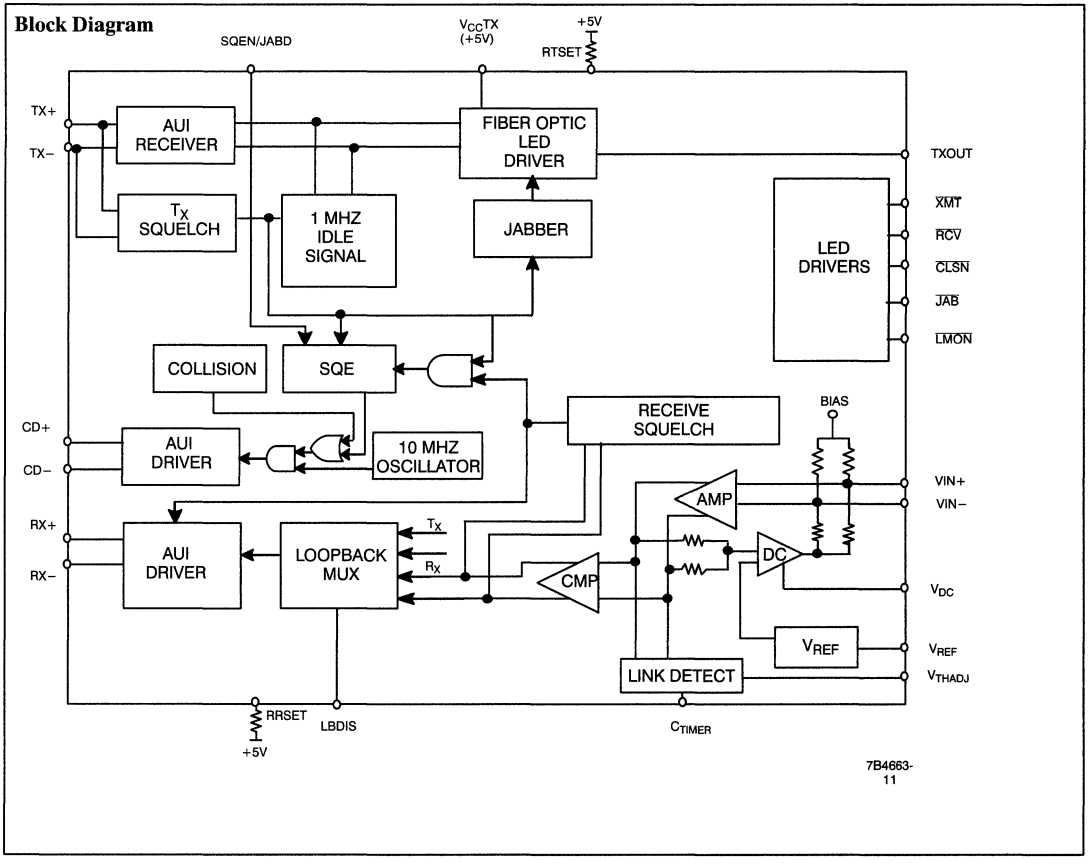
Functional Description

The CY7B4663 is a single chip solution low power fiber optic transceiver for 10BASE-FL applications. The CY7B4663 complies with IEEE 802.3 standards for fiber optic Ethernet.

The CY7B4663 has a current driven output which drives the fiber optic LED transmitter with a maximum current of 110 mA. The transmitter automatically inserts a 1 MHz signal during idle time. The 1 MHz idle signal, Jabber function, and SQE test are all internal functions of the chip. The receiver contains a data quantizer capable of accepting input signals as low as $2mV_{P-P}$ with a 55dB dynamic range.

The CY7B4663 is fabricated using an advanced, low power BiCMOS process. Typical standby current during idle is 35 mA.

Block Diagram



Pin Descriptions

CY7B4663

Pin Number	Name	Description
1	$\overline{CLSN}$	Active low LED driver which indicates that a collision is occurring. The collision event is extended with an internal timer for visibility.
2 3	CD+ CD−	AUI collision output pins. Differential driver that transmits a 10 MHz signal during collision events, jabber, and CD Heartbeat conditions. Also referred to as CI port.
4	C_{TIMER}	Tying a capacitor from this pin to V_{CC} determines the Link Monitor response time.
5	SQEN/JABD	SQE Test Enable, Jabber Disable. Tying this pin low disables the SQE test, tying high enables the SQE function. When tied between 1.5V and $V_{CC}-2.0V$ both the SQE test and Jabber are disabled.
6 7	RX+ RX−	AUI receive output pins. Differential driver that outputs the signal received from the fiber optic. Also referred to as the DI port.
8	LBDIS	Loopback Disable. Tying this pin to VCC disables the loopback function. The AUI transmit pair data is not looped back to the AUI receive pair and the collision function is disabled. Tying this pin to ground or leaving it floating enables the loopback and collision functions.
9	V_{CC}	+5 volt supply.
10 11	TX+ TX−	AUI Transmit Input pins. Differential receiver that inputs the signal for transmission onto the cable.
12	RTSET	Sets the current level driven by the transmitter
13	RRSET	A 1% 61.9 kΩ resistor tied to V_{CC} sets the proper internal operating currents
14	$\overline{LMON}$	Active low LED driver indicating the Link Monitor status. If there are transitions on RXIN± indicating an idle signal or a packet transmission this pin will be pulled low. The threshold for input sensing by the Link Monitor circuitry is set with the V_{THADJ} pin.
15	$\overline{XMT}$	Active low LED driver which indicates that a transmission is occurring. The event is extended with an internal timer for visibility.
16	$\overline{RCV}$	Active low LED driver that indicates the transceiver is receiving a frame from the optical receiver. The event is extended with an internal timer for visibility.
17	V_{CC}TX	+5 volt supply for LED driver.
18	TXOUT	Fiber optic LED driver output.
19 20	GND GND	Ground Reference
21	V_{DC}	Tying a capacitor from this pin to ground alters the DC feedback loop pole. The value of this capacitor should be at least ten times larger than the input coupling capacitors.
22	V_{REF}	A 2.5V reference.
23	V_{THADJ}	Input pin which sets the link monitor threshold.
24	GND	Ground Reference
25 26	VIN− VIN+	These pins are capacitively coupled to the fiber optic receiver.
27	V_{CC}	+5 Volt Supply
28	$\overline{JAB}$	Active low LED driver. When Jabber occurs this pin is low to indicate the Jabber status.

CY7B4663 Description

The CY7B4663 contains:

1. Transmitter which drives the fiber optic LED.

2. Receiver with integrated quantizer which takes data from the fiber optic receiver module and passes it to the AUI.

3. AUI (Attachment Unit Interface) which consists of three signal pairs: the transmit pair, receive pair, and the collision pair.

4. Fiber media link monitor function with link status LED.

5. Collision, Loopback, Signal Quality Error (SQE) , and Jabber functions.

6. Five chip/system status LED pins with 10 mA nominal drivers.

Transmitter

The CY7B4663 transfers Manchester−encoded data from the AUI port of the DTE (TX+ and TX−) to the fiber optic media. The output meets IEEE 802.3 specifications for fiber optic Ethernet.

The fiber transmitter detects data on the TX± input and passes this data to the fiber media. If TX+ is positive with respect to TX−, then TXOUT is high impedance and no current flows through the transmitter. When TX+ is negative with respect to TX− then TXOUT will sink up to 110 mA of current into the

CY7B4663 and the fiber LED transmitter will light up. When in the non−transmitting state the CY7B4663 will transmit a 1 MHz link signal over the fiber network to maintain link integrity.

In order for data to be transferred from the AUI TX± inputs to the fiber output it must meet the squelch requirements for the DO pair. The squelch circuit prevents noise from reaching the LED driver. The circuit rejects signals with pulse widths less than 15 ns or smaller than (typically) 225 mV. After TX unsquelches it looks for the start of idle signal before turning on the squelch again. If the TX± signal exceeds 225 mV for more than 190 ns the squelch circuitry is turned on and the transmitter disabled.

Receiver

The CY7B4663 receiver has an integrated data quantizer which takes data directly from the fiber optic receiver. This data is sent out on the AUI over the RX± pins.

The device also contains an internal squelch function that discriminates noise from signal. The receive squelch will reject frequencies lower than 2.5 MHz, or any signal if the link monitor function indicates a link loss. When in the unsquelched state the receive circuitry looks for the start of idle signal. Any signal which exceeds 160 ns without transition will send the receiver into squelched state and the start of idle signal will be sent over the RX± AUI driver.

The V_{THADJ} pin can be used to adjust the sensitivity of the receiver. For 10BASE−FL V_{THADJ} can be tied directly to V_{REF} and achieve a bit error ratio of less than 1.0×10^{-9}. If greater sensitivity is desired a voltage divider can be used to adjust V_{THADJ}. The relationship between V_{THADJ} and V_{TH} is:

$$V_{THADJ} = 408V_{TH}$$

AUI Function

The AUI consists of three pairs of signals: TX±, RX±, and CD±. Manchester encoded differential data is sent from the MAC to the TX±. In the case of an external Medium Attachment Unit (MAU) the data is AC coupled through either an isolation transformer or through isolation capacitors. If the transceiver is internal the part may be either AC or DC coupled. Valid data from the fiber optic media is sent from the RX± differential pair to the DTE. In the case of a collision or Jabber the CD± drivers will send a signal to the MAC.

The AUI drivers are capable of driving a full 50 meters of AUI cabling. They have a typical rise and fall time of 4 ns. The RX± and CD± differential output voltage is minimized during idle time to prevent standing current in the isolation transformer.

Link Monitor Function

The link monitor function monitors the input signal voltage level and determines if it falls below a preset level. If the input voltage falls below a preset level the CY7B4663 enters the Low Light state. In this state the transmitter sends out the 1MHz link signal, but all data received at TX± is ignored. In addition, the loopback function and the receiver are disabled and the $\overline{\text{LMON}}$ LED pin goes high. To switch back to the Link Pass state the link monitor threshold must be exceeded by 20%. Once the CY7B4663 returns to Link Pass it waits 250ms to 750ms and then checks if TX± is idle and no data is being received before re−enabling the transmitter, loopback, and receiver, and bringing the $\overline{\text{LMON}}$ pin low.

Collision

If the transceiver is both receiving data and transmitting at the same time the collision AUI outputs will be activated. The collision ports will not be activated when the loopback is disabled. The collision signal consists of a 10 MHz −15%/+25% signal with a worst case 45/55 or 55/45 duty cycle. The collision signal is also activated during Jabber and at the end of packet for the SQE test.

Loopback

The CY7B4663 loopback function sends the transmit data from the DTE back over the AUI receive pair, RX±. Loopback can be disabled by tying LBDIS to V_{CC}. This allows the chip to act as a full duplex transmitter and receiver with collision detection disabled.

Heartbeat Test Function (SQE Test)

The Signal Quality Error (SQE) / Heartbeat function is enabled by tying the SQEN pin to V_{CC}. When enabled, a 10 MHz collision signal is transmitted to the MAC over the CD± pair after the transmission of a packet. The transmission lasts 10±5 BT. The heartbeat function should be disabled by tying the HBE pin to ground for repeater applications.

Jabber Function

The on chip timer prevents the DTE from locking up a network by transmitting continuously. When the transmission exceeds the jabber time limit, the Jabber function disables the transmitter and sends a 10 MHz signal over the CD± pair. Once the transmitter is in the jabber state, it must remain idle for 500 ms before it will exit the jabber state. The 1 MHz idle signal will be transmitted during jabber regardless of the transmitter being disabled. The jabber function is enabled by tying the SQEN/JABD pin to either VCC or ground. The function can be disabled by tying the pin between 1.5V and V_{CC}−2V.

LED Drivers

The CY7B4663 provides five LED status drivers. The LED drivers are active low, and the LEDs are normally off except for the $\overline{\text{LMON}}$ pin, which remains on until link is lost. The pins are tied to V_{CC} through the LED and a series 500Ω resistor.

Because the transmit, receive, and collision events occur so rapidly, the $\overline{\text{XMT}}$, $\overline{\text{RCV}}$, and $\overline{\text{CLSN}}$ pins have event extenders on them. The extenders allow the event to be visible. Whenever a transmission, reception, or collision occurs the respective pin will be visible for a typical period of 16 ms. If the event is repeated before the 16 ms period expires, the timer is reset and the LED timing period is restarted. The $\overline{\text{JAB}}$ and $\overline{\text{LMON}}$ LEDs do not have event extenders because they occur for a long enough period to be visible to the user.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Supplied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current TXOUT ..... 110 mA

Input Current RRSET, RTSET, $\overline{\text{JAB}}$, $\overline{\text{CLSN}}$, $\overline{\text{XMT}}$, $\overline{\text{RCV}}$, $\overline{\text{LMON}}$ ... 60 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

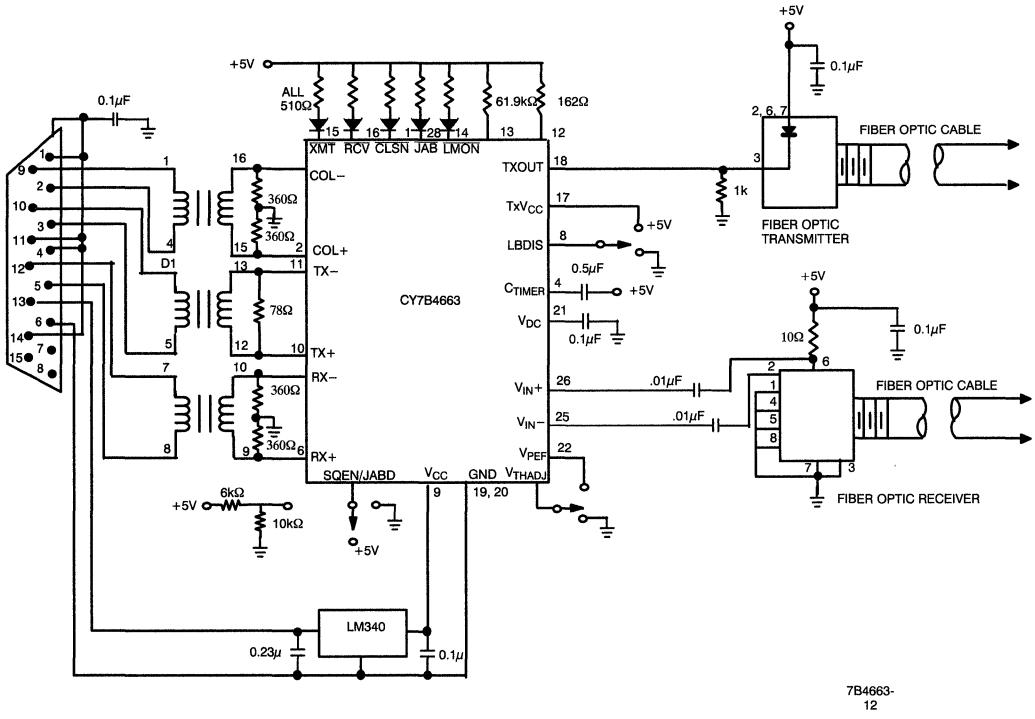


Figure 1. CY7B4663 Schematic Diagram

Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
I_{CC1}	Power Supply Current Non-Transmitting		35	50	mA
I_{CC2}	Power Supply Current Transmitting		80	100	mA
V_{OL}	LED Driver Low Voltage (I_{OL}=10mA)			0.8	V
I_{TXP}	Transmit Peak Output Current			110	mA
V_{TS}	Transmitter Squelch Voltage (TX±)	175	225	300	mV
V_{IC}	Common Mode Input Voltage (TX±, RXIN±)	2		V_{CC}-0.5	V
RX, CD	Differential Output Voltage	±500		±1200	V
V_{OC}	Common Mode Output Voltage (RX±, CD±)		2.5		V
V_{IMB}	Differential Output Voltage Imbalance			±40	mV
V_{SQED}	SQE Test Disable Voltage			0.3	V
V_{JD}	Jabber Disable Voltage	1.5		V_{CC}-2	V
V_{SQBE}	SQE/Jabber Both Enabled	V_{CC}-0.5			V
V_{LBD}	LBDIS Disable Threshold	V_{CC}-1			V
V_{LBE}	LBDIS Enable Threshold			1	V
V_{CTX}	Common Mode Voltage (TX±)		3.5		V
V_{CIN}	Common Mode Voltage (VIN+, VIN-)		1.65		V
V_{REF}	Reference Voltage	2.35	2.45	2.55	V
V_{RSC}	VREF Output Source Current			5	mA
G_{AMP}	Input Amplifier Gain		100		V/V
V_{ISR}	Fiber Input Signal Range	2		1600	mV_{P-P}
V_{SET}	External Voltage at V_{THADJ} to Set V_{TH}	0.5		2.7	V
V_{IOF}	Input Offset (V_{DC} = V_{REF})		3		mV
V_{IRN}	Input Referred Noise (50 MHz BW)		25		µV
R_{IN}	Input Resistance V_{IN}±	0.8	1.3	2.0	kΩ
I_{THADJ}	Input Bias Current of V_{THADJ}	-200	0	200	µA
V_{LPTV}	Threshold for Switching from Link Fail to Link Pass	5	6	7	mV_{P-P}
	Hysteresis of Link Fail to Link Pass		20		%

AC Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
t_{TXNPW}	Transmit Turn On Pulse Width	10	20	40	ns
t_{TXFPW}	Transmit Turn–Off Pulse Width (TX to idle transitions)	500		2000	ns
t_{TXLP}	Transmit Loopback Startup Delay			400	ns
t_{TXODY}	Transmit Turn–On Delay			100	ns
t_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle Duty Cycle	45		55	%
t_{TXSDY}	Transmit Steady State Propagation Delay		15	50	ns
t_{TXI}	Transmitter Jitter Into 31 Ω			±1.5	ns
t_{RXSFT}	Receive Squelch Frequency Threshold	2.5		4.5	MHz
t_{RXODY}	Receive Turn–On Delay			150	ns
t_{RXFX}	Last Bit Received To Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXI}	Receiver Jitter		±1.5		ns
t_{AR}	Differential Output Rise Time (RX±, CD±)		4	7	ns
t_{AF}	Differential Output Fall Time (RX±, CD±)		4	7	ns
t_{CPSQE}	Collision Turn–On Delay			300	ns
t_{SQEXR}	Collision Turn–Off Delay			650	ns
t_{CLF}	Collision Frequency	8.5		11.5	MHz
t_{CLPDC}	Collision Pulse Duty Cycle	45	50	55	%
t_{SQEDY}	SQE Test Turn–On Delay After Transmission	0.7	1.1	1.5	µs
t_{SQETD}	SQE Test Duration	0.6	1.0	1.4	µs
t_{JAD}	Jabber Activation Delay	20	26	32	ms
t_{JRT}	Jabber Reset Time Out	300	420	550	ms
t_{JSQE}	Delay From Outputs Disabled to Collision Oscillator On		100		ns
t_{LED}	$\overline{RCV}$, $\overline{CLSN}$, $\overline{XMIT}$ On Time	8	16	32	ms
t_{LLPH}	Low Light Present to $\overline{LMON}$ High	3	5	10	µs
t_{LLCL}	Low Light Clear to $\overline{LMON}$ Low	250		750	ms

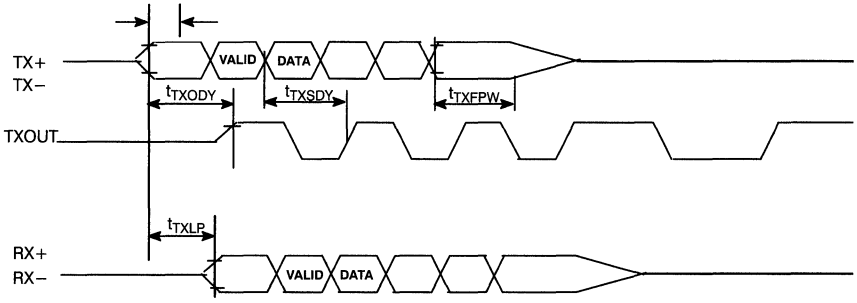


Figure 2. Transmit and Loopback Timing

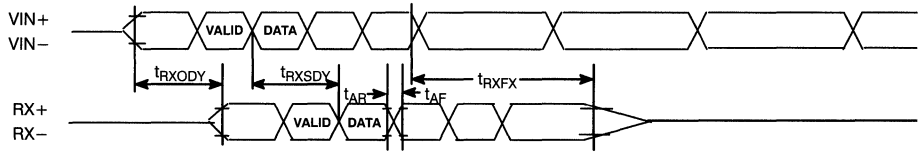


Figure 3. Receive Timing

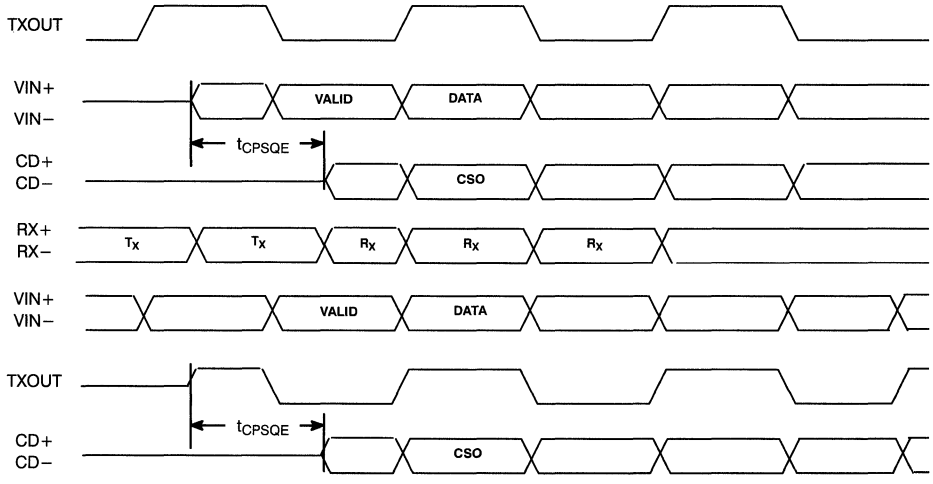


Figure 4. Collision Timing

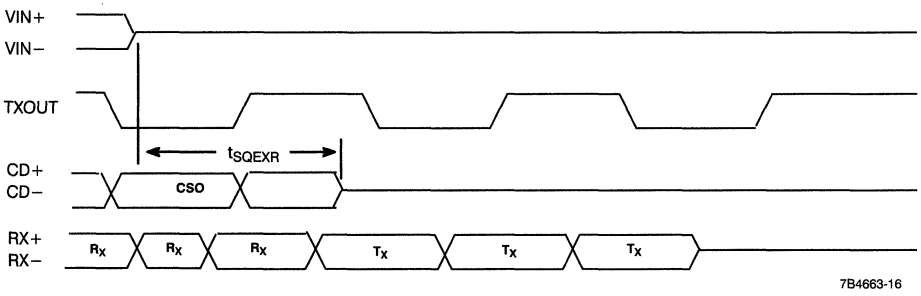


Figure 5. Collision Timing

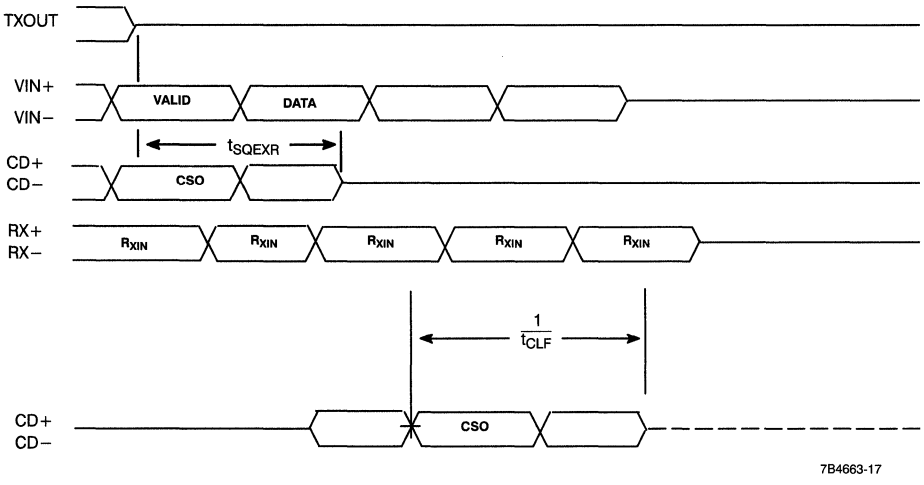


Figure 6. Collision Timing

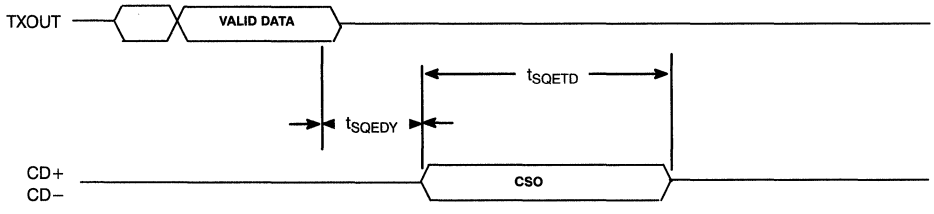


Figure 7. SQE Timing

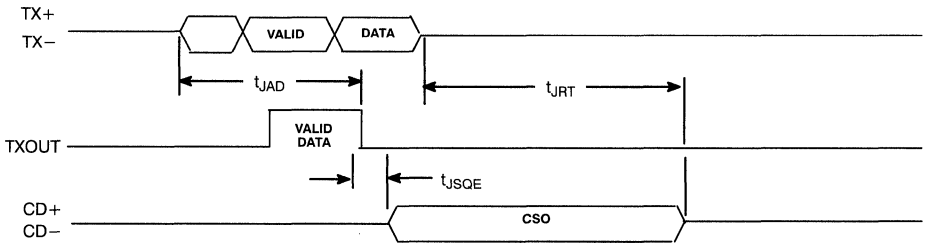


Figure 8. Jabber Timing

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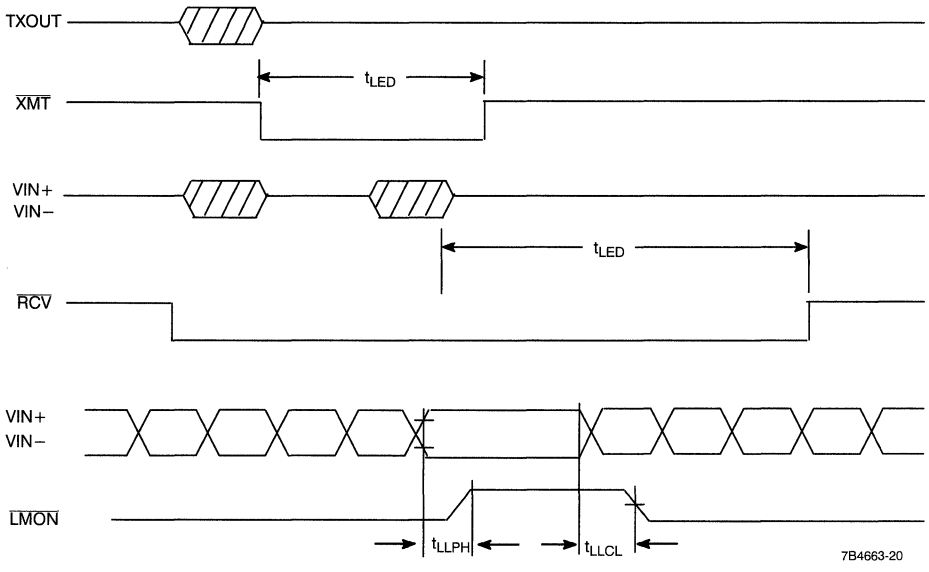


Figure 9. LED Timing

Document #: 38−00508

CY7B8392 Low Power Ethernet Coaxial Transceiver Application

This application note describes the differences between the 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) versions of the IEEE 802.3 standard, and provides guidelines for design with the CY7B8392.

Introduction

The CY7B8392 is a physical layer device used to transmit data over a shared coaxial medium. It functions as specified by the IEEE 802.3 standard.

Figure 1 shows a block diagram of a single network node. The MAC (Media Access Control) is responsible for framing data and controlling its transmission and reception on the network. When transmitting the MAC sends NRZ data to the Physical Signaling (PLS) Layer. The PLS processes the MAC sublayer data, setting the signaling rate and translating the NRZ data to Manchester Encoded Data, and sends it to the transceiver.

Figure 2 displays an example of Manchester encoding. Instead of straight binary encoding, each bit period is divided into two equal intervals. To send a one, the voltage is HIGH (ground) for the first half of the interval and LOW (−2.0 V by IEEE 802.3) for the second half of the interval. In the case of a binary zero the reverse is true, the first half of the bit period the signal is LOW and HIGH the second half.

Data is sent out over the network in packets. An Ethernet packet consists of the preamble, destination address, source address, length field, data, and a Cyclic Redundancy Check (CRC). Each packet can be viewed as a sequence of 8-bit bytes, with the least significant bit of each byte being transmitted first. A typical Ethernet packet is shown in *Figure 3*. The ***preamble*** contains 8 bytes of alternating ones and zeros, ending with two consecutive ones. The preamble allows the receiving PLS to synchronize its clock with the sender. The two consecutive ones at the end of the preamble signify the start of frame packet and are sometimes referred to as the Start of Frame Delimiter. The ***destination address*** is a 6-byte

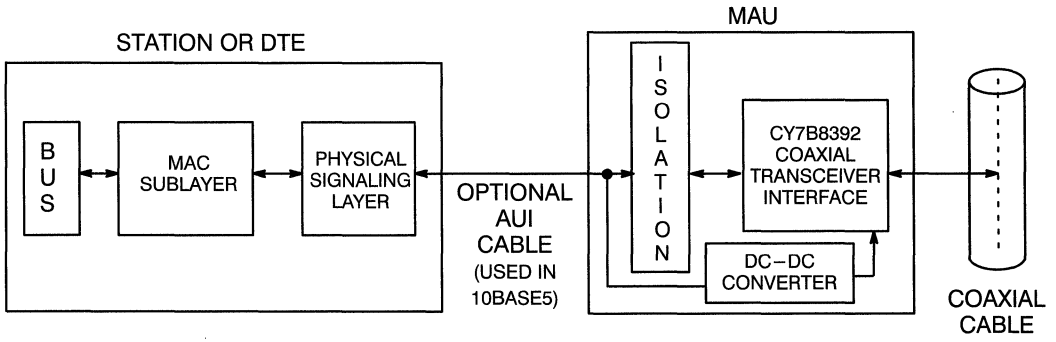


Figure 1. Block Diagram of Single Network Node

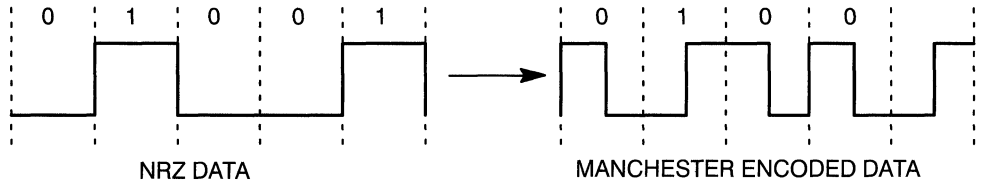


Figure 2. Manchester Encoding

field that specifies the station(s) to which the packet is being sent. Every station examines this field and determines whether it should accept the packet. The high-order bit of the destination address is a zero for ordinary addresses and one for group (multicast) addresses. Group addresses allow multiple stations to listen to one address. The ***source address*** is a 6 byte field that contains the unique address of the station that is transmitting the packet. The ***length*** field is used to determine how many bytes are in the data field. This is necessary because IEEE 802.3 dictates the data portion of a packet must be a minimum of 46 bytes. If the data portion of a packet is less than 46 bytes, it is padded with random bits until it is the legal size. The length field is used to notify the controller which part of the data field is valid. The ***data*** field contains an integral number of bytes ranging from 46 to 1500. The ***CRC*** field contains code that checks on the integrity of a packet.

10BASE5/10BASE2 Ethernet Network

IEEE 802.3 standard allows for two different versions of coaxial data transmission, 10BASE5 and 10BASE2. 10BASE5 (Ethernet) uses thick coaxial cable with transceivers directly attached to the cable network. Because of the inflexibility of the thick coaxial cable an AUI drop cable is needed to electrically connect the Ethernet transceiver to the Data Terminal Equipment (DTE). IEEE standard allows up to 500 meter lengths of RG−8 coaxial cable to be used in 10BASE5 applications. 10BASE2 (Cheapernet) uses a thin, flexible cable which can be directly attached to the DTE or a Medium Attachment Unit (MAU). A maximum of 185 meters of cable is allowed when using 10BASE2. *Figure 4* and *Table 1* show the differences between Ethernet and Cheapernet (sometimes referred to as Thinnet).

Table 1. Comparison of 10BASE5 and 10BASE2 Media

	10BASE5	10BASE2
Cable type	RG−8	RG−58 A/U
Maximum cable length	500 meters	185 meters
Maximum network length	2500 meters	925 meters
Attachments per segment	100	30
Attachment spacing	2.5 meters	0.5 meters
Topology	Linear bus	Linear bus

Due to the inflexibility of the thick coaxial cable it is difficult to bring the cable directly to the DTE. To solve this problem an AUI drop cable is used in 10BASE5 applications. The AUI cable consists of four individually shielded twisted pairs with an overall shield covering these pairs. The twisted pairs

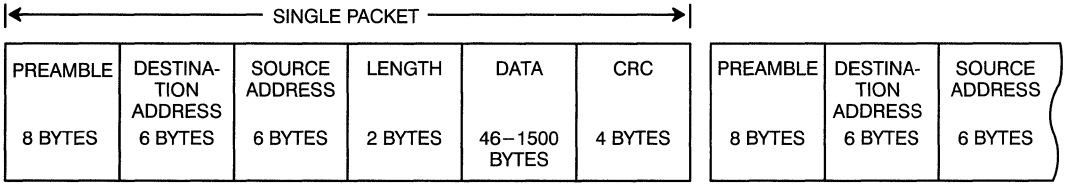


Figure 3. Typical Ethernet Packet

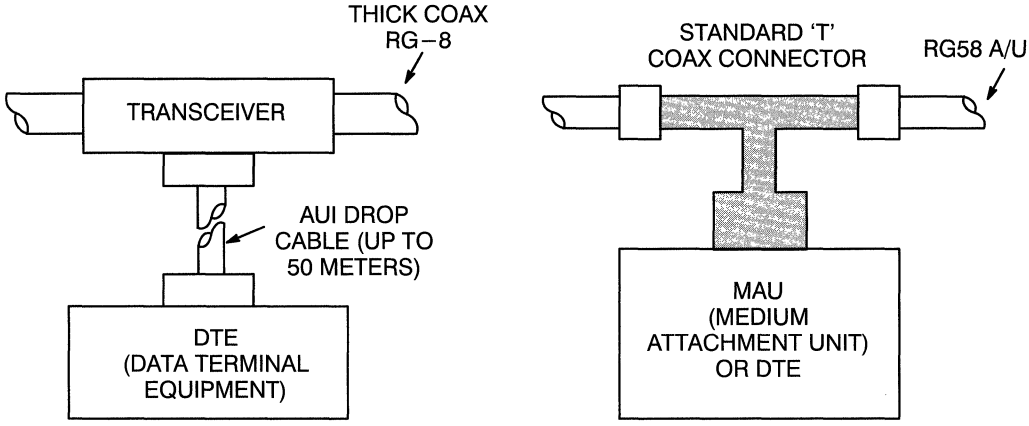


Figure 4. Ethernet vs. Cheapernet

have a characteristic impedance of 78 ±5Ω. The cable can be up to 50 meters in length. The individual shields should be connected to logic ground while the outer shield should be connected to chassis ground. The signal assignments for the AUI twisted pairs are shown in *Table* 2. AUI drop cable is typically not used in 10BASE2 applications because the thin coaxial cable is flexible enough to be directly attached to the DTE.

Table 2. AUI Interface Signal Assignments

Pins	Signal	Description
1	Control In circuit Shield	Shield for CD± twisted pair
2	Control In circuit A	CD+ signal
3	Data Out circuit A	TX+ signal
4	Data In circuit Shield	Shield for the RX± twisted pair
5	Data In circuit A	RX+ signal
6	Voltage Common	
7	No Connect	
8	No Connect	
9	Control in circuit B	CD– signal
10	Data Out circuit B	TX– signal
11	Data Out circuit Shield	Shield for the TX± twisted pair
12	Data In circuit B	RX– signal
13	Voltage Plus	Voltage supply from DTE
14	Voltage Shield	
15	No Connect	

It is possible, through the use of repeaters, to combine several networks together. These networks can be a single Physical layer, i.e., only 10BASE2 or only 10BASE5, or it can by a combination of many different Ethernet physical layers. The maximum length of a 10BASE5 network using repeaters is 2500 meters, while the maximum length of a 10BASE2 network with repeaters is 925 meters. *Figure 5* shows a combined network with both Ethernet and Cheapernet connected through repeaters.

CY7B8392 Signal Transmission/ Reception

During transmission, differential Manchester encoded data is sent to the CY7B8392 from the DTE. This data is shaped to meet IEEE signal requirements and sent out single-ended onto the coaxial cable. Conversely, when the transceiver is receiving data from the coaxial cable it takes single-ended Manchester encoded signal from the cable and sends differential data to the DTE.

In order to visualize the operation of a 10BASE system using the CY7B8392, we will follow a signal from transmission to reception. When the DTE decides to send a packet, the controller sends NRZ data to the SNI, which in turn sends differential Manchester encoded data through an isolation transformer to the CY7B8392. The transceiver and the coaxial network must be electrically isolated from all external signals. The isolation is required to be 500 V_{AC} for 10BASE2 and 2000 V_{AC} for 10BASE5. This isolation can be performed using three pulse transformers, which are available in 16-pin DIP and 16- or 12-pin surface mount packages available from several manufacturers (Pulse Engineering, Valor Electronics, Bel Fuse). After the differential signal passes through the transformer it is received at the TX± ports of the CY7B8392. This

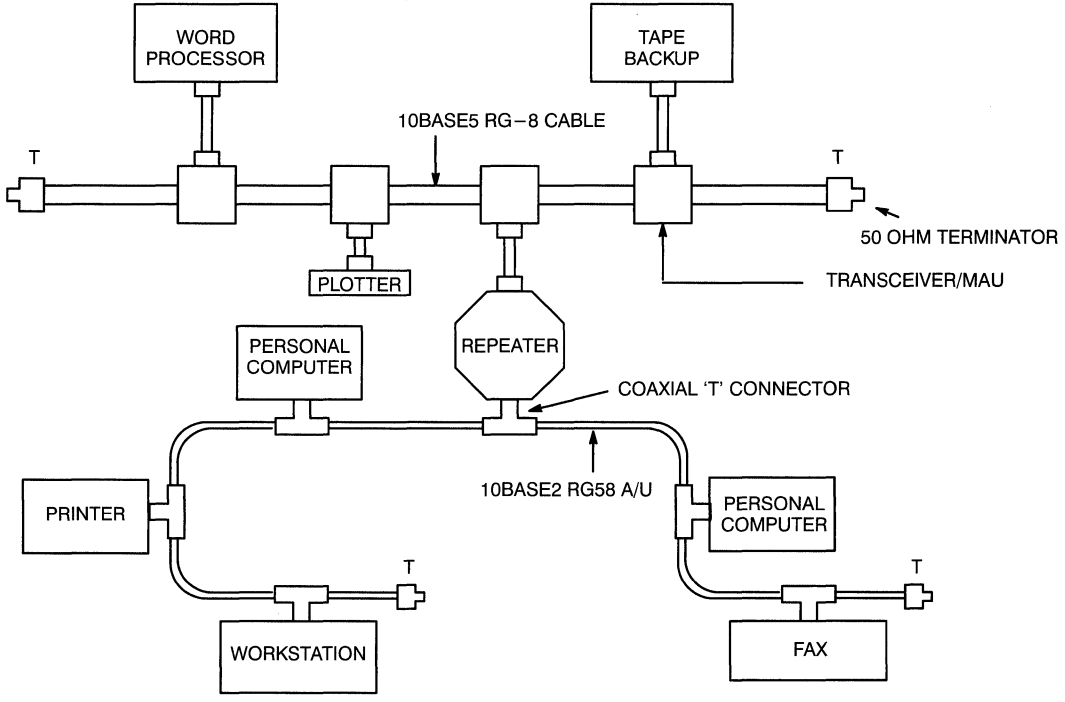


Figure 5. Combined Ethernet and Cheapernet Network

signal must have an AC signal amplitude greater than −225 mV and a pulse width of more than 15 ns. If these values are not met, the transmitter squelch circuitry will not allow the signal to reach the output driver. The differential signal is sent to a comparator with hysteresis. Every differential voltage crossing flips the output of the comparator which triggers the internal waveform shaping circuitry. The waveform shaping circuitry, feeds a current amplifier which sinks 10 mA (LOW) and 75 mA (HIGH) into the TXO port. Because the network appears as a 25Ω load (two 50Ω resistors in parallel), this translates to a single-ended voltage swing of –0.25V to –1.875V at TXO.

By IEEE 802.3 specifications, the DC offset of the output driver should be between −37 mA and −45 mA. The AC swing should be from ±28 mA up to the offset value. This current drive limit must be met even in the case of one other unit transmitting on the network. The 10−90% rise/fall times must be 25 ±5 ns at 10 Mb/s and they must match within 2 ns.

On the other end of the network data is received from the coaxial cable at the RXI port. The signal is the equalized and amplified before being sent out of the RX± ports. Due to the low pass characteristics of the coaxial cable, equalization of the signal is necessary before it can be amplified and sent to the DTE. The CY7B8392 receiver circuitry has a high pass filter which compensates for the cable characteristics and sends equalized differential Manchester encoded data to Physical Signaling Layer through the RX± ports. In addition to the equalizer, the receiver has a carrier sense feature which will reject signals with less than 467 mV DC content. *Figure 6* depicts CY7B8392 transmission and reception over the network.

JITTER

A characteristic of transmission over a coaxial network is system jitter. Jitter is defined as the short term variations of a digital signal from its ideal position in time. In other words, a clock may be expected to have a rising edge at time t=0, but instead the rising edge occurs slightly after or before t=0. Jitter can be caused by many parts of a network such as source clock imperfections, cable distortion, etc. If the length of the network is large then the low pass filter characteristics of the cable can induce a significant jitter by attenuating the higher frequencies more than the lower frequency signal content. The maximum system jitter allowed by IEEE 802.3 standards is ±7 ns. Minimizing jitter allows the MAC sublayer devices to accurately process data received from the CY7B8392. If the jitter is too great then the bit error rate may increase above acceptable levels.

Collision Detection

Because 10BASE2 and 10BASE5 transmit over a shared medium, it is necessary to detect instances where two or more stations are transmitting at the same time. This is known as collision detection.

There are two standard types of collision detection, receive and transmit. Both modes compare the average DC voltage on the coaxial cable with respect to ground and determine if a collision is occurring between two transmitting stations.

In ***receive mode collision detection,*** any collision between two separate transmitting nodes will be detected by the transceiver when the average DC cable voltage with two nodes transmitting is from −1.4V to −1.58V. The CY7B8392 and all competition devices have a set internal collision detection voltage that falls into this collision window. IEEE 802.3 standards require receive mode collision detection in applications where repeaters are used. This is done to limit the round trip signal delay to 50 µs, ensuring that all stations on the network will detect a collision before the end of a minimum length packet (57.6 µs). The allowable cable lengths using receive mode collision detection are 185 and 500 meters for 10BASE2 and 10BASE5, respectively.

In ***transmit mode collision detection*** a collision between two stations will be detected while the transceiver is actively transmitting (i.e., it is one of the two colliding stations). Competition 8392 parts require an external voltage divider at the CDS input in order to implement transmit collision detection mode. The voltage divider is used to give the CDS pin a DC offset of approximately −250 mV. Because collision is detected as the voltage difference between the RXI and CDS pins, this allows the coaxial cable to fall 250 mV lower than the receive mode threshold before collision is detected. The relaxed

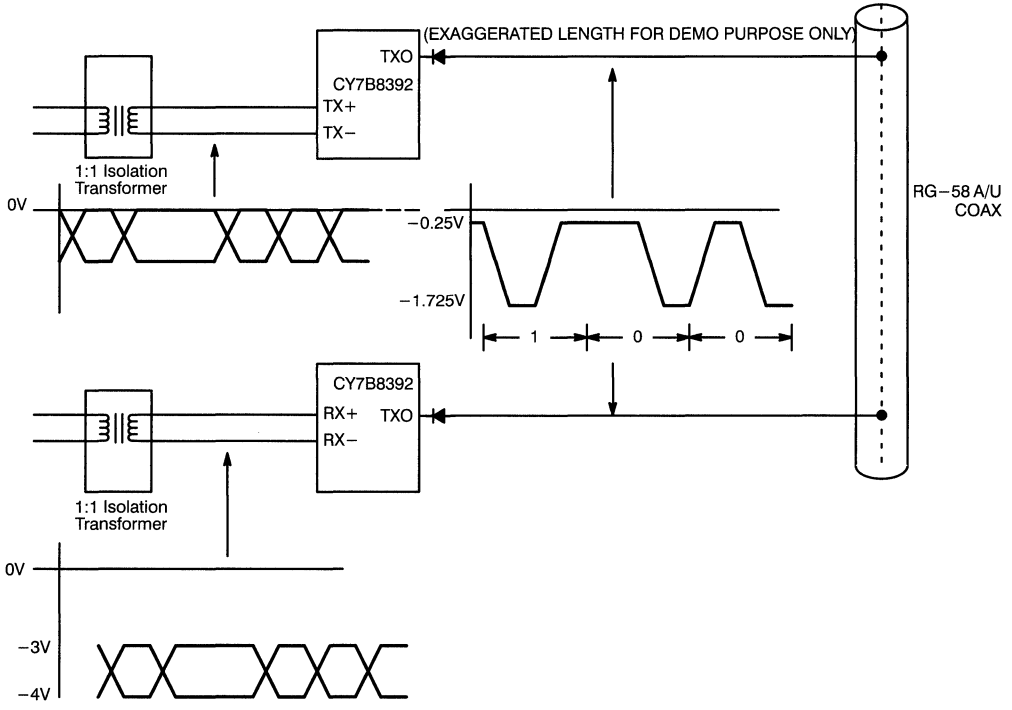


Figure 6. CY7B8392 Transmission and Reception over the Network

upper limit allows longer cable lengths to be used. Transmit mode collision detection allows 300 and 1000 meters of coaxial cable to be used with 10BASE2 and 10BASE5, respectively.

The collision detection offered only by the CY7B8392 is ***hybrid collision detection,*** a combination of receive and transmit mode collision detection. When the CY7B8392 is not transmitting, it automatically sets the collision threshold voltage to the smaller (less negative) receive level. If the unit enters the transmit mode, the collision detection threshold is automatically changed to the larger (more negative) transmit mode. Hybrid collision detection allows extended cable lengths to be used in non-repeater applications without an external voltage divider at the CDS pin. It can also be used in repeater applications with regular cable lengths without redoing the board design.

In the case of transceivers with receive collision detection, a separate board is required for repeater and long cable applications. Thus, the CY7B8392 Hybrid collision detection is a more flexible solution than the competition's collision detection techniques.

CY7B8392 Heartbeat Function

The CY7B8392 Heartbeat function is enabled when the HBE pin is tied to GND (OV). When enabled, a 10 MHz collision signal is transmitted to the MAC over the CD± pair after the transmission of a packet. For repeater applications the Heartbeat function can be disabled by tying the HBE pin to V_{EE} (−9V). Additionally, if the HBE pin is raised to approximately a TTL level above ground (1.0V nominal) the 8392 enters the test mode state. In the test mode state the Jabber timer, which controls datasheet parameters T_{JA} and T_{JR}, is accelerated by

2^{12}. This allows accelerated testing of these parameters in production.

Designing a 10BASE5 MAU with the CY7B8392

When designing an Ethernet board electrical isolation of both the signal and power supply is necessary. AUI signal isolation is easily achieved through the use of a pulse transformer at the AUI ports. Power isolation is achieved using an isolated DC–DC converter which is required to take the 12V–15V DTE supply as an input and provide a –9V nominal output. To step down the voltage, a transformer is used, which also supplies the required isolation characteristics. For a detailed DC–DC converter design see the section on power supply design in this application note.

Careful consideration should be taken when designing the MAU printed circuit board. According to IEEE 802.3, a total of 4 pF of capacitive loading is allowed for each transceiver attachment in 10BASE5 applications when measured by both a 25 ns rise time and 25 ns fall time waveform (typical coaxial media waveform). This allotment is split into 2 pF of shunt capacitance allowed for the MAU circuitry and 2 pF for the cable tap mechanism. To keep capacitance as low as possible, the traces from TXO and RXI to the connector should be kept as short as possible. The addition of a diode with the anode electrically connected to the TXO port and the cathode to the cable tap mechanism helps minimize tap capacitance by isolating the output capacitance of the export. The CY7B8392 should be directly soldered to the board without a socket to keep stray capacitance to a minimum. Finally, all metal traces, including ground and V_{EE}, should be kept as far from the RXI and TXO traces as possible to minimize stray capacitance. *Figure 7* displays the CY7B8392 layout considerations.

Because 10 BASE5 applications use an AUI drop cable, termination resistors are required on the differential transmit pair. The AUI cable has a characteristic impedance of 78Ω. Using two 39Ω and a 0.01 µF capacitor as the center grounding effectively terminates the line and also minimizes common mode signal, or a more simple 78Ω resistor will suffice.

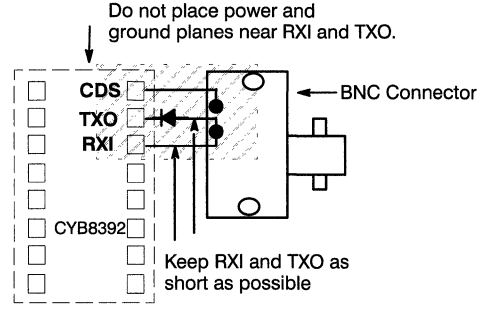


Figure 7. CY7B8392 Application (not to scale)

A controlled breakdown path is required that will shunt high-energy transients to an effective ground. This controlled breakdown is required to meet the isolation requirements outlined in the IEEE 802.3 standard. In addition, the standard also requires that all applications provide an adequate radio frequency ground return path. These requirements can be met by connecting a 1 MΩ 0.25W resistor and a 0.01 µF capacitor in parallel. The resistor provides the static discharge path while the capacitor ensures low susceptibility to magnetic interference. *Figure 8* shows a typical CY7B8392 10BASE5 application with heartbeat disabled.

Designing a 10BASE2 MAU with the CY7B8392

10BASE2 transceivers are designed using the same circuit as in 10BASE5. The one difference is that an AUI drop cable is not used in 10BASE2. Because an AUI drop cable is not used in Thinnet applications, the termination resistors are not necessary on the incoming TX± signal traces.

Driving Longer Cable with the CY7B8392

With the CY7B8392 it is possible to drive longer cable lengths. Because of the Hybrid collision detection which is available in the CY7B8392, up to 1000m (10 BASE5) or 300m (10 BASE2) of coaxial cable can be used. These extended cable lengths can be used in non-repeater applications only. In repeater applications the standard cable length maximums of 500 and 185 meters must be adhered to. This limit is enforced because the maximum end-to-end delay time for a signal on the network cannot ex-

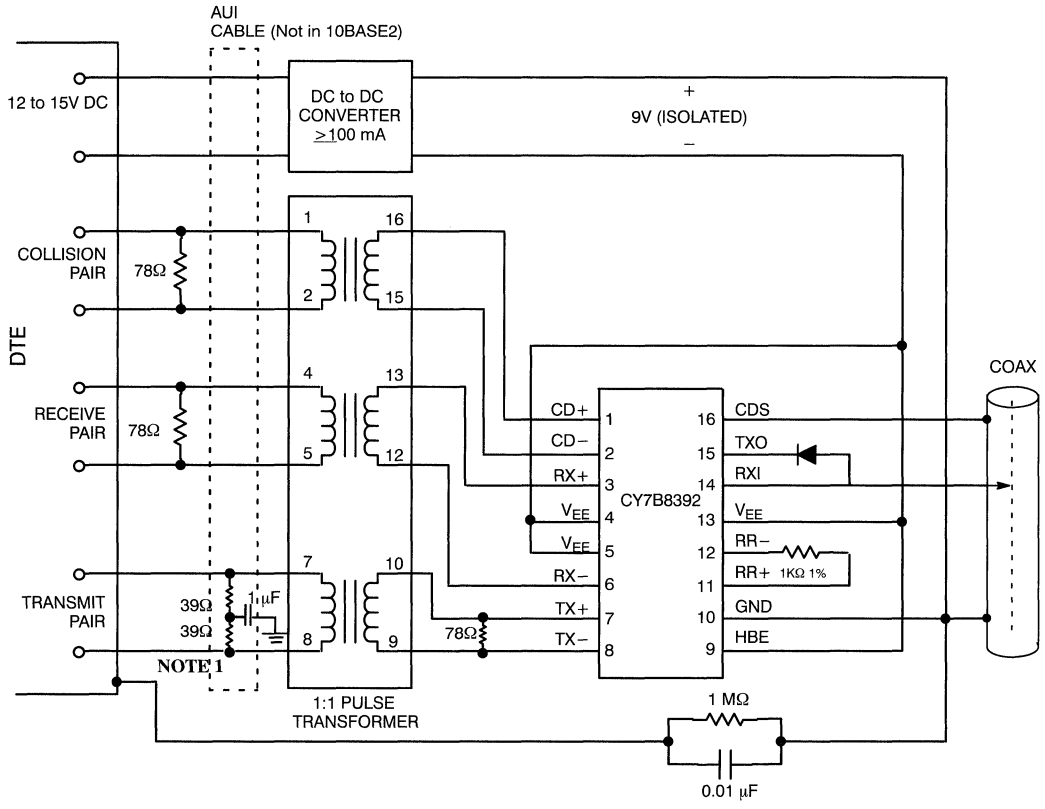


Figure 8. CY7B8392 MAU Application with Heartbeat Disabled[1]

ceed 25 µs by IEEE 802.3 standard. Thus, the total delay of the cable plus a maximum of four repeaters must be less than 25 µs.

Driving Non-Standard Cable with the CY7B8392

In many situations a network cabling system will already be installed, and some these networks used coaxial cable with different characteristic impedances. Because a significant portion of the cost for installing a LAN is the cost of the cable and the labor to install it, it is in the interest of the customer to use the existing cable plant if possible. This can be achieved either by using a BALUN (BALanced to UNbalanced) or modifying the transceiver board design to operate with the non-standard cable.

Modifying the transceiver board for non-standard cable applications involves attenuating the signal at the RXI and CDS pin. If this is not done then the voltage appearing at the RXI pin will not be within acceptable limits for the CY7B8392. In the case of 93Ω cable, the window for setting collision threshold is between −2637 mV and −2895 mV due to the altered resistance of the cable network. These voltages are calculated by taking the RG-58 A/U thresholds and multiplying by 1.86 (93/50). Because the CY7B8392 is designed to send a collision signal if the DC voltage on the line falls below −1530 mV, every transmission on 93Ω cable will be seen as a colli-

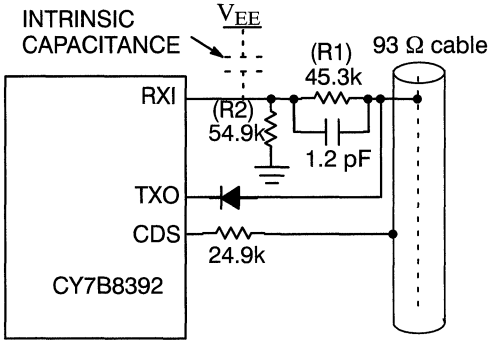


Figure 9. CY7B8392 application using 93Ω Cable

sion. Thus, a resistive divider is required to lower the receive voltage to an acceptable level for collision detection. Using standard resistor values, the voltages should be divided so that 1530 mV lies in the acceptable window of collision detection. Choosing a voltage divider with resistor values of 54.9 kΩ and 45.3 kΩ provides a satisfactory result. An example of an application using 93Ω cable is shown in *Figure 9*. The intrinsic capacitance of the RXI pin and trace capacitance (typically 1 pF combined) can create a low pass filter effect with the voltage divider in place. This can be offset by compensated by placing a capacitor (~ 1.2 pF) in parallel with the leading resistor of the voltage divider, as shown in *Figure 9*. A series 24. 9 kΩ (45.3k||54.9k) resistor is also required on the CDS pin to insure that biasing currents on CDS and RXI produce an equivalent voltage drop.

Any resistor combination that solves *Equation 1* will provide the necessary offset for non-standard cable applications. Larger resistor values are desirable to keep the shunt resistance of the transceiver node as high as possible.

$$(R2/R1+R2)\ *(Z_{COAX}/50\Omega)=1 \qquad \text{Eq.1}$$

(Z_{COAX}=Non-standard cable impedance)

When different resistor values are used at the voltage divider of RXI, the biasing resistor at CDS must also be changed to reflect the altered parallel resistance of R1 and R2.

Auto-AUI Function

The CY7B8392 Auto-AUI function allows a 10BASE designer the ability to easily design NICs (Network Interface Cards). The Auto-AUI function has the ability to switch between AUI, twisted pair, and coax connections (assuming both the twisted pair and coax transceivers have Auto-AUI function). This feature benefits both the board designer with a cost savings, and the user who no longer has to open the computer or program software to reconfigure the NIC.

A typical NIC is shown in *Figure 10*. If the user wishes to change from the AUI port to the 10BASE2 coaxial connection it is necessary to open the computer and flip switches, or in some cases reconfigure the NIC software through a tedious process. Both of these situations require the user to consult a manual for reference. If this manual is lost, changing the configuration becomes problematic for the user.

Figure 11 shows a NIC design using the CY7B8392 Auto-AUI function. This application eliminates the need for switches/jumpers or special software. The CY7B8392 automatically does the reconfiguration by either turning its AUI drivers on (properly terminated coaxial cable is attached), or placing them in a high-impedance state (no coaxial cable attached). Thus, simply attaching a coaxial cable to the 10BASE2 coaxial port and leaving the 10BASE−T and AUI ports unconnected automatically configures the NIC.

DC−DC Converter Design for CY7B8392 Applications

In MAU applications the CY7B8392 requires a −9V isolated power supply from a 12−15V power source. Both discrete and integrated DC−DC converters are available for this application. Integrated DC−DC converters are available through several vendors (Fil−Mag, Valor). A discrete design can be provided through a transformer, self-oscillating primary, and rectifying secondary. Because the 8392 consumes very little power when compared to competitive devices a discrete transformer allows the designer to minimize the DC−DC cost through the selection of low power components. A schematic of the circuit is shown in *Figure 12*.

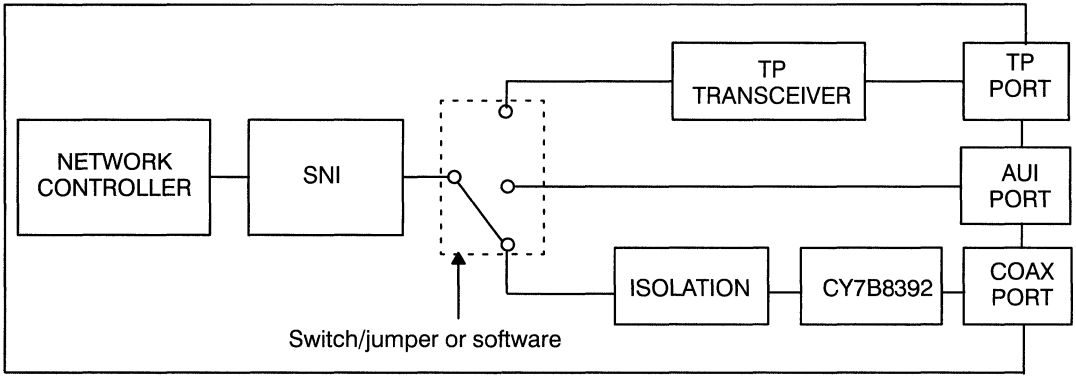


Figure 10. Typical Network Interface Card

The function of the circuit is as follows: Initially, 12V is applied across the input of the converter. This causes the voltage at (1) to rise until one of the transistors arbitrarily turns on. For this example we will assume that Q1 turns on. As Q1 starts conducting, current begins to flow through the transformer winding connected to the collector of Q1. This current change is opposed by the inductive characteristics of the transformer, which induces a voltage in the opposite direction. Because all the transformer windings are wound around a common core, every separate winding will induce a voltage. The direction of the induced voltages follow the transformer dot convention. Thus, with Q1 ramping, every winding appears as a voltage source with the positive terminal at the end of the winding (opposite the dot). This induced voltage will force the base voltage of Q1 higher, turning it on hard, and force the base voltage of Q2 low, ensuring that it remains off.

At the same time the current is ramping up in the primary, the voltage induced in the transformer is applied to the secondary rectification circuit. Again, following the dot convention, a positive voltage is applied at the cathode of D1 and a negative voltage at the cathode of D2. Current flows through D1 and charges the output capacitors, while D2 opposes current flow.

Eventually, as the current increases in Q1, it reaches a point where the 12V supply cannot continue to sustain di/dt. As this occurs, the induced voltage opposing the current flow in the transformer will disappear. Consequently, the voltage at the base of Q1 will be unable to sustain the collector current and

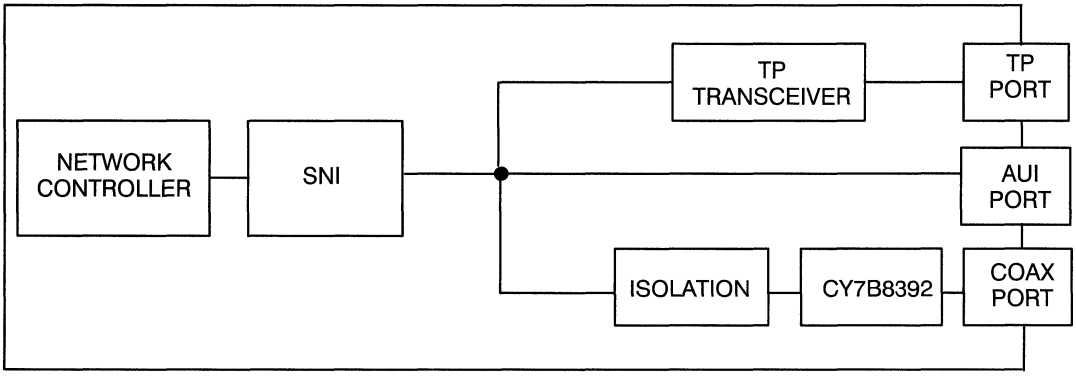


Figure 11. Advanced Network Interface Card with Auto-AUI Function

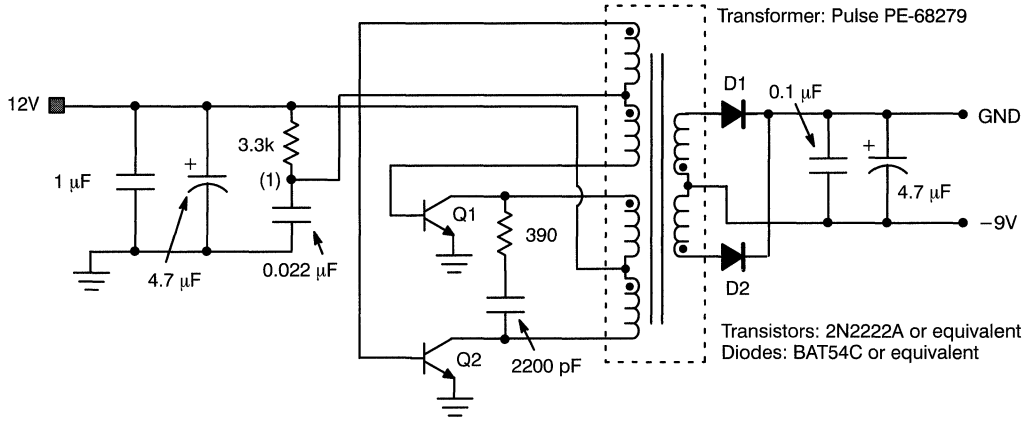


Figure 12. DC−DC Converter Design

Q1 will come out of saturation. In turn, the current flow in the winding will begin to decrease. Because the inductive nature of the transformer opposes the change in current, a voltage is induced which opposes this decrease in current. Following the dot convention, the positive terminal appears at the beginning of the winding (the end with the dot). The induced voltage forces the voltage at the base of Q2 high and turns the transistor on hard while Q1 is forced off. The current then flows through the transformer winding to the collector of Q2 and then to ground. In this manner the primary circuit oscillates and changes DC to AC.

Applying the induced voltage to the secondary rectification circuit, a positive voltage is applied to the cathode of D2, which allows current to charge the output capacitors. These capacitors minimize voltage ripple at the output and provide a constant DC supply to the CY7B8392.

If the CY7B8392 is being used in an adapter card application where 5V± 5% is available, then the discrete DC−DC converter shown in *Figure 12* can be easily redesigned to use this supply. Simply replace the 3.3 KΩ resistor on the input with a 270Ω resistor and change the transformer to a Pulse PE−68283.

CY7B8392 vs. The Competition

As shown in this application note and the CY7B8392 data sheet, the Cypress coaxial transceiver has features which set it apart from the competition. The low power characteristics of the CY7B8392 mean that the cost of the power supply is reduced, saving on the overall cost of the board design. Cypress hybrid collision detection, available only on the CY7B8392, allows larger diameter networks to be used without reconfiguring the transceiver board with a voltage divider at CDS. Pulldown resistors are no longer required on the RX± and CD± AUI ports, again minimizing board space and cost. These features make the CY7B8392 a standard to follow in coaxial Ethernet transceiver applications.

Notes:

1. The TX± 78Ω termination resistor may be exchanged with two 39Ω resistors and a 1-µF capacitor for common mode rejection. Only one configuration should be used, not both together.

100BASE-T4/10BASE-T Ethernet Transceiver Application

Introduction

This application note briefly describes a 100BASE-T4/10BASE-T transceiver application using the CY7C971 Fast Ethernet Transceiver. A schematic and a description of the board layout are included.

The transceiver's function is to provide an interface between the media (4 pair of CATegory 3, 4, or 5 Unshielded Twisted Pair for 100BASE-T4, or 2 pair of CAT3, 4, or 5 UTP for 10BASE-T) and the Media Independent Interface (or MII) as defined in the IEEE Fast Ethernet standard.

Transceiver Schematic

The schematic for the transceiver application is very simple due to the high level of integration designed into the CY7C971 (see the CY7C971 data sheet). The schematic is shown in *Figures 1 and 2*. The basic components are:

1. CY7C971 Fast Ethernet Transceiver
2. Quad 1:2 Transformer
3. 25MHz Crystal
4. Connectors (MII and RJ45)
5. LEDs
6. Resistors
7. Capacitors

The CY7C971 performs all of the functions necessary to implement the transceiver design. The quad transformer provides isolation from the twisted pair media and modifies the signal amplitude. The 25MHz crystal is used as a timing reference for the CY7C971. The connectors provide for an external interface to the twisted pair media, and the MII. LEDs are used to indicate the mode of operation (100BASE-T4, 10BASE-T, or 10BASE-T Full Duplex), as well as indicating transmit and receive status. Finally, the various resistors are used for terminations and current limiting, and the capacitors are used for decoupling.

Note, there is no external transmit or receive filter required. Without the bulky filter magnetics, the board layout becomes quite simple.

Transceiver Board Layout

Figure 3 is a Printed Circuit Board (PCB) design for the transceiver application shown in *Figures 1 & 2*. As noted above, due to the high level of integration within the CY7C971, the board layout is very simple. The board consists of two layers, one signal layer and one split power and ground plane.

The dominating components on the board are the CY7C971 (u1), the quad transformer (t1), the 25MHz crystal (x1), the MII connector (j2), and the RJ45 connector (j1). Other components are the LEDs, resistors, and capacitors.

Conclusion

The transceiver application breifly described in this application note is intended as an evaluation tool for the CY7C971 Fast Ethernet Transceiver. Transceiver boards, schematics, and Gerber files are available from Cypress Semiconductor by contacting a local Cypress sales office.

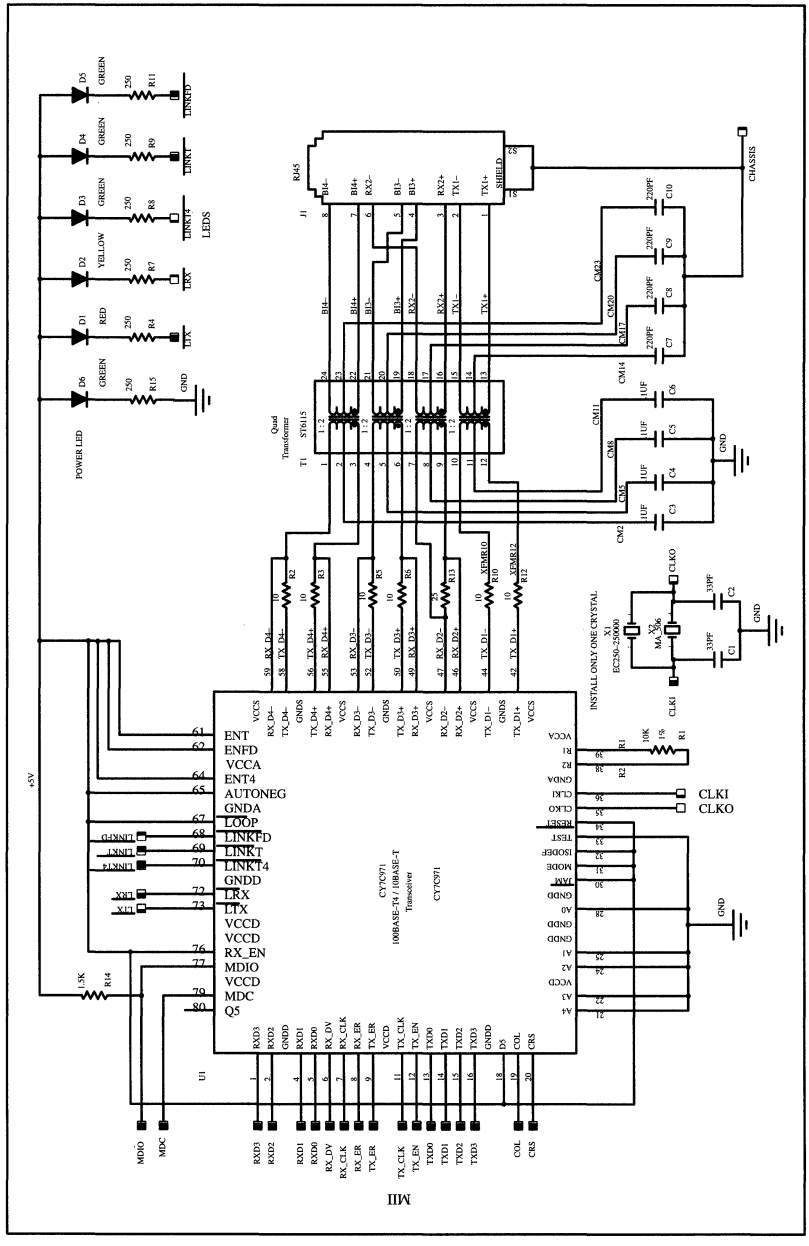


Figure 1. Transceiver Application Schematic Sheet 1

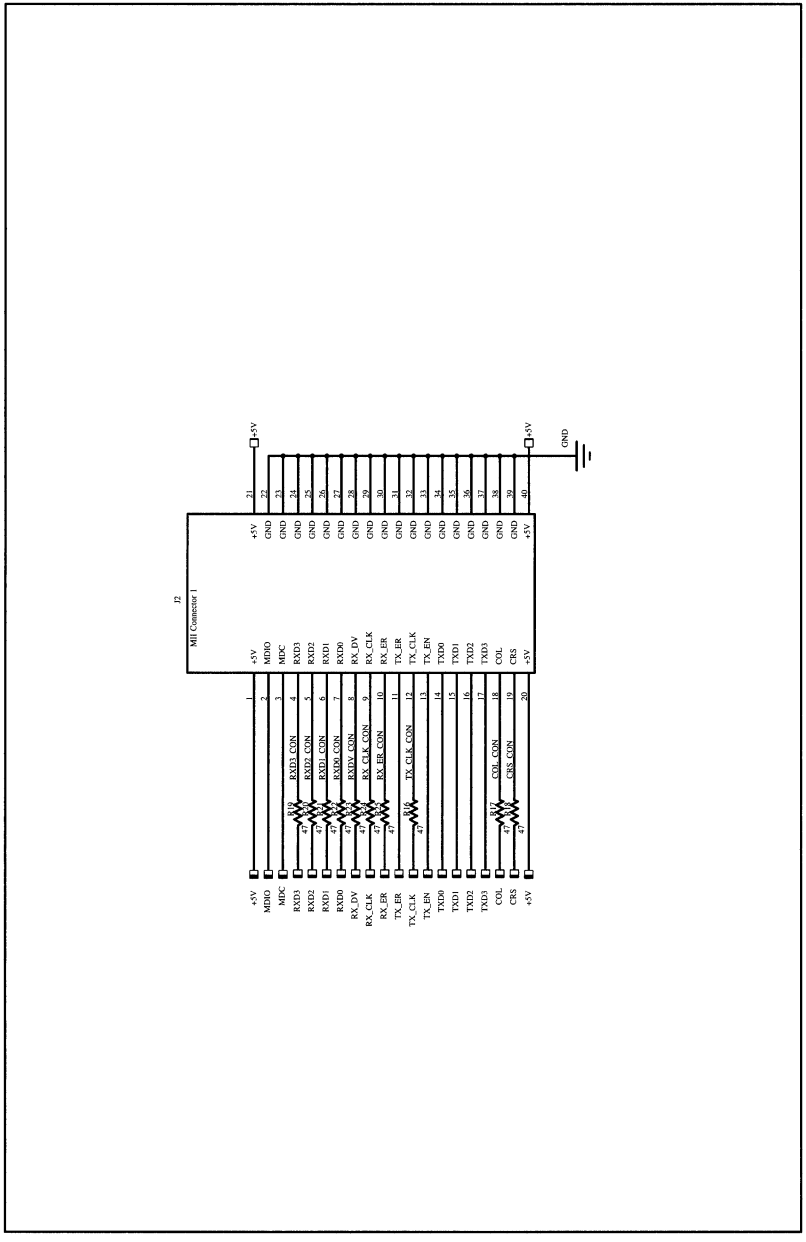


Figure 2. Transceiver Application Schematic Sheet 2

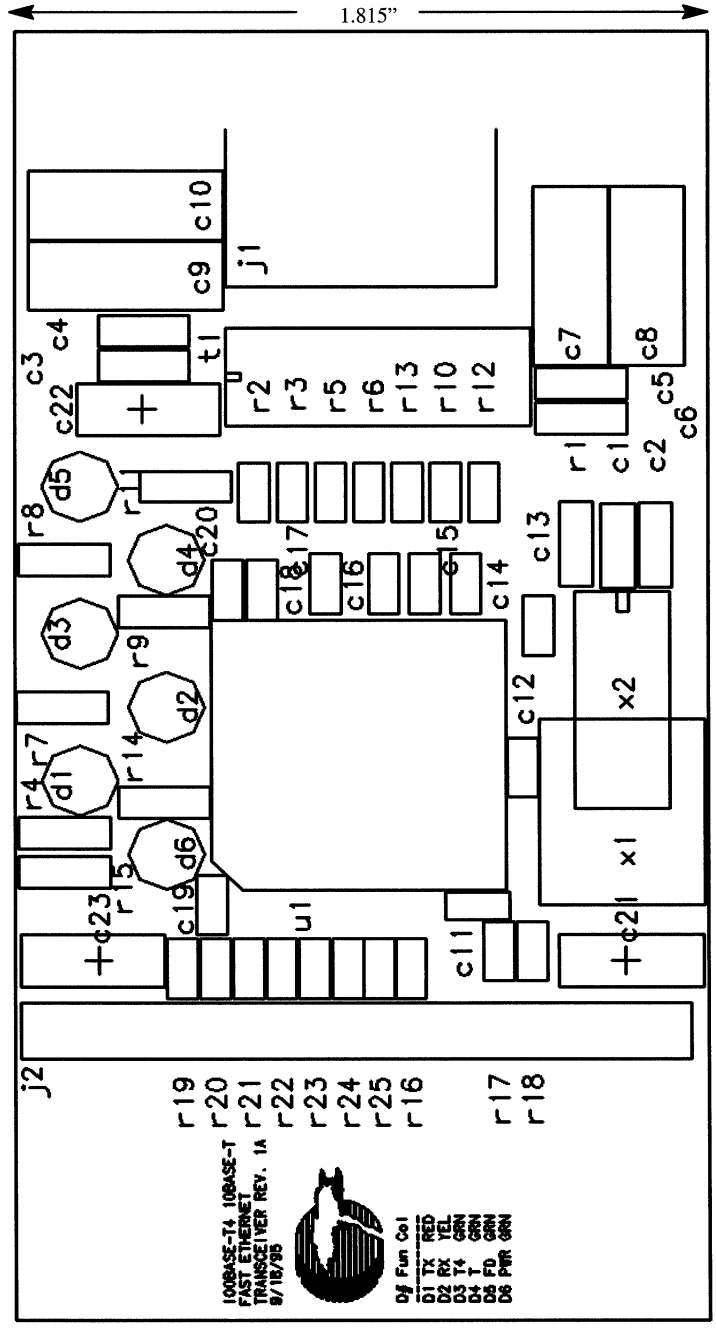


Figure 3. Transceiver Application PCB

100BASE-T4 / 10BASE-T Ethernet PCI Network Adapter

Background

This application note describes the design of a dual speed 100BASE-T4/10BASE-T Ethernet Network Adapter card for PCI systems using the Cypress CY7C971 PHY and the Digital Semiconductor 21140 MAC (Media Access Controller). The adapter card has the following features:

- Dual Speed 100BASE-T4/10BASE-T
- Full Duplex 10BASE-T
- IEEE Compliant Auto-Negotiation
- High Performance PCI Interface

The network adapter card's function is to interface the host computer to the network cabling. The adapter card plugs into the host computer's PCI bus. The twisted-pair network cable plugs into the end of the network adapter card via an 8-pin modular RJ−45 jack. *Figure 1* illustrates a PCI Network Adapter with a host motherboard.

The network interface card contains all of the circuitry for the Ethernet physical layer, MAC layer, and PCI interface. The Cypress CY7C971 contains all of the physical layer circuitry for 100BASE-T4, 10BASE-T, and Auto-Negotiation. The DEC 21140 contains all of the logic for Ethernet MAC and the PCI bus interface. The CY7C971 and the DEC

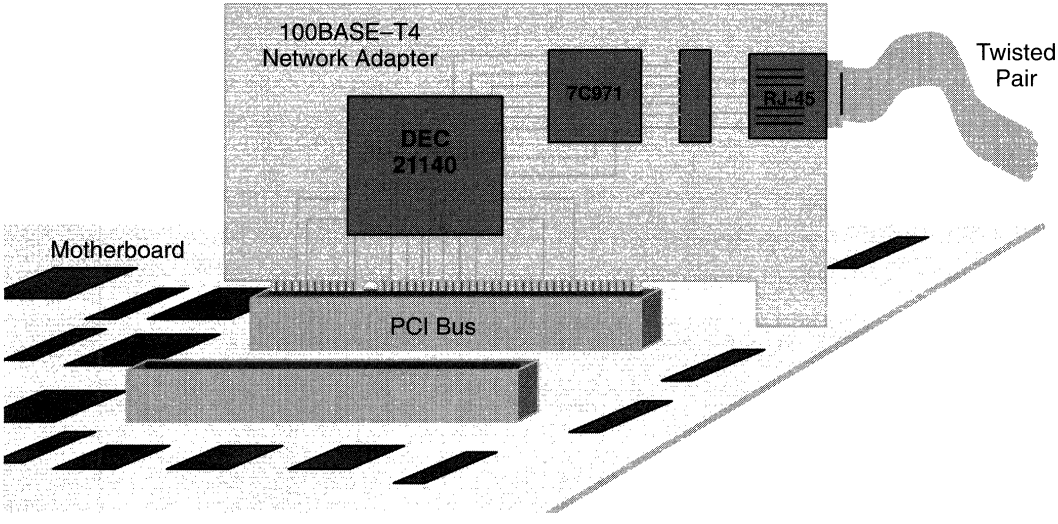


Figure 1. PCI Network Adapter Card

21140 interface to each other through the Media Independent Interface (MII). The MII is an IEEE standard interface between the Ethernet physical layer and the MAC layer.

CY7C971

Media Dependent Interface (MDI)

The CY7C971 provides a simple interface to the 8-pin modular RJ−45 jack. No expensive external filters or components are necessary because all transmit filtering and equalization are performed on-chip. All CY7C971 media interface pins are dual speed, allowing shared magnetics to be used. A quad 1:2 transformer for electrical isolation and termination resistors to match the cable impedance are all that is required.

The output buffer design uses a feedback voltage driver that minimizes power consumption and controls the common mode output voltage. The transformer provides sufficient common-mode rejection over the frequencies of interest so that an external common mode choke is not needed. *Figure 2* shows a schematic of the media interface with the CY7C971.

The characteristic impedance of the twisted pair medium is a nominal 100Ω The 1:2 transformer reduces (by the square of the turns ratio) medium load impedance to 25Ω on the primary (971) side. The termination resistors and the output buffer impedance together form a matching 25Ω load. The matching load insures that maximum signal is transferred to the medium and minimizes reflections due to impedance mismatch.

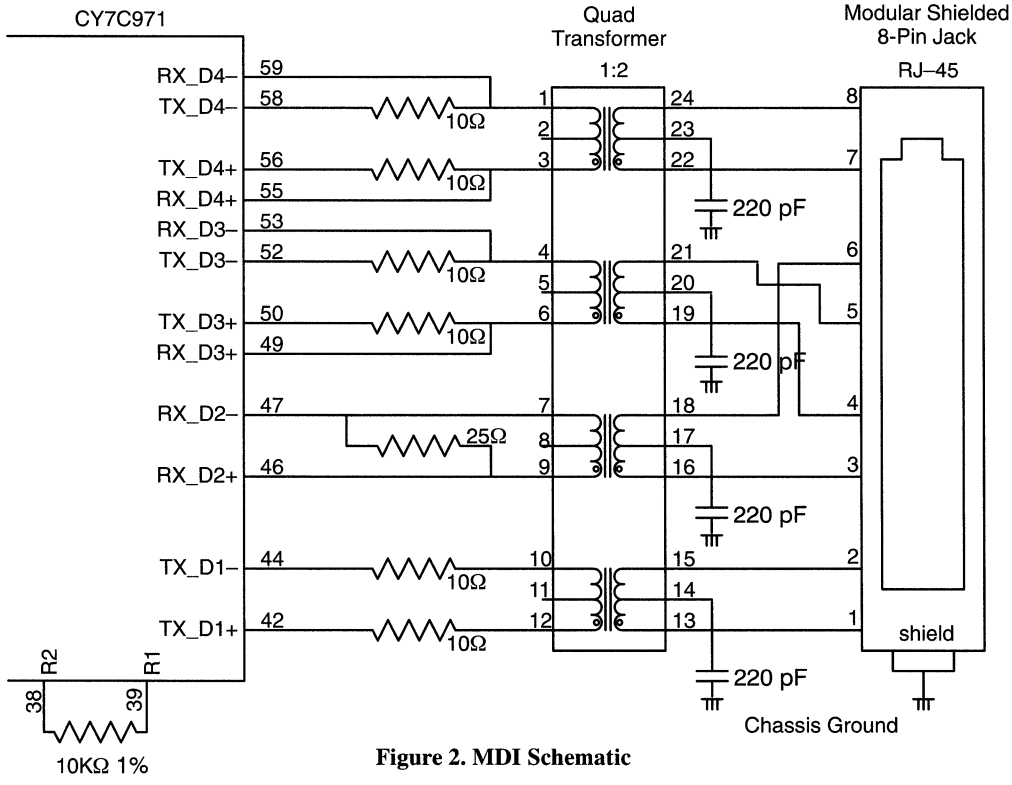


Figure 2. MDI Schematic

The center taps on the media side of the transformer are connected to the chassis ground through 220-pF (minimum) high-voltage (2 KV) capacitors. These capacitors help absorb common-mode noise that is picked up or generated on the twisted-pair medium. The capacitors must be capable of withstanding the isolation requirements specified in the 100BASE-T4 standard. High-voltage ceramic disc capacitors are economical and work well in this application.

The high precision currents needed for the transmit DAC and equalizer are derived from the external 10KΩ 1% resistor on pins R1 and R2. An internally generated band-gap voltage reference is used by the CY7C971 for all internal reference voltages.

Media Independent Interface (MII)

The Media Independent Interface (MII) is the IEEE Ethernet standard interface for communication between the MAC and PHY devices. The MII supports both 100 Mb/s and 10 Mb/s data transfer modes. In 100 Mb/s mode, the MII transfers nibble wide data groups at 25 MHz transfer rate yielding 100 Mb/s throughput. In 10 Mb/s mode, the transfer rate is reduced to 2.5 MHz for a 10 M/s throughput. During all transfers, the receive and transmit reference clock are continuously sourced from the CY7C971 PHY to the 21140 MAC. *Figure 3* shows the MII connections between the CY7C971 and the DEC 21140.

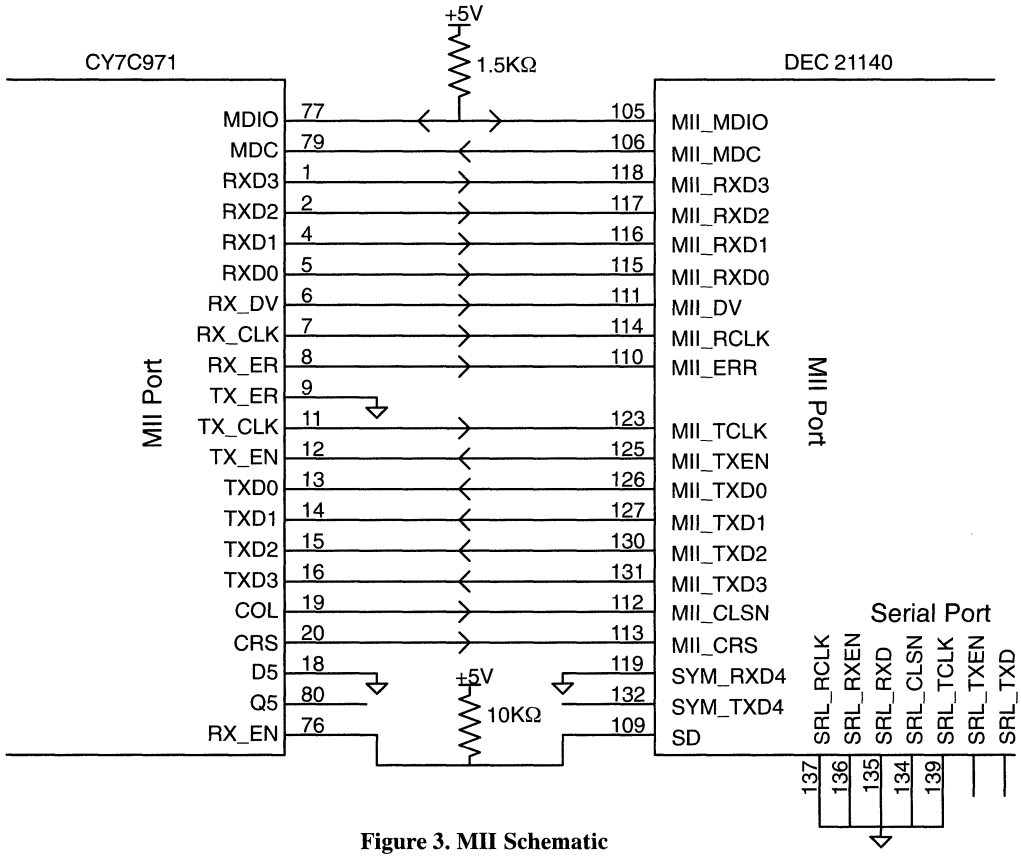


Figure 3. MII Schematic

All data transfers between the CY7C971 and the DEC 21140 are over the MII interface. The DEC 21140 has an additional 7-wire serial interface for an external 10 Mb/s transceiver. This port is not used in conjunction with the CY7C971 and these port pins are tied inactive as shown in the schematic (Appendix A).

The CY7C971 has a buffer enable input signal, RX_EN, that is not part of the MII standard. This pin is used to place the MII output buffers in high impedance. In this application, RX_EN should be tied HIGH to permanently enable the MII output buffers. The Q5 and D5 pins on the CY7C971 are not used in MII mode. D5 can be tied either HIGH or LOW. Since the DEC 21140 does not support explicit transmit error generation over the MII interface, the 971 TX_ER pin should be tied LOW to prevent inadvertent transmit error generation.

The MDC and MDIO pins form a simple two-wire serial management interface between the 7C971 and 21140. MDC is a clock signal sourced from the 21140. The MDIO line is a bidirectional data line used to transfer management data frames. The MDIO signal requires a 1.5 Kohm pull-up resistor to VCC. This interface is used to transfer standard management frames that control and monitor the behavior of the CY7C971. Management frames contain a PHY address, register number, op code, and a 16-bit data field.

Clock Pins

The CY7C971 generates all internal and external clock signals from its on-board oscillator circuit. The oscillator circuit requires an external 25 MHz parallel resonant crystal connected between the CLKO and CLKI pins. The external load capacitors (C_{load}) should be chosen so that the total load capacitance matches the parallel resonant capacitance of the crystal. The load capacitors form a series capacitance network. The required load capacitance is derived from the following equation:

$$C_{xtal} = (C_{pin} + C_{load} + C_{trace}) / 2$$

$$C_{load} = 2 \bullet C_{xtal} - C_{pin} - C_{trace}$$

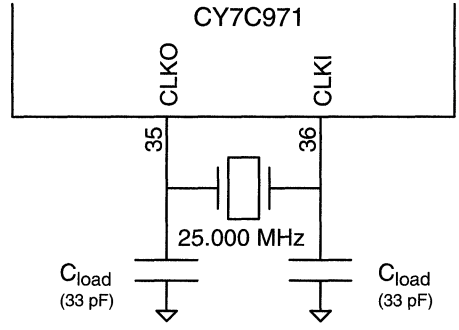


Figure 4. Clock Pins

The package pins contribute approximately 1.5 pF to the parallel load capacitance. Board trace and pads contribute between 1–2 pF of parasitic capacitance depending on trace length, width and dielectric thickness. According to this formula, an 18-pF parallel resonant crystal would require 33-pF load capacitors.

The crystal should have frequency stability of 100 ppm or less in order to comply with the Ethernet standards *Figure 4* shows the CY7C971 clock pin connections. The load capacitors are connected between the Clock pins and ground.

LED Pins

The CY7C971 can drive LEDs directly. The LED pins use an open drain output buffer that can sink up to 12 mA. The buffers have a weak internal pull-up resistor. *Figure 5* shows how the LED pins connect to the LEDs.

The $\overline{LTX}$ and $\overline{LRX}$ pins indicate when the CY7C971 is actively transmitting or receiving Ethernet frames. $\overline{LTX}$ indicates that the transmitter is active, and $\overline{LRX}$ indicates that the receiver is active. These signals are time stretched to at least 25 ms so that light pulses emitted from the LED can be detected by the human eye. These pins may be tied together in a wire-or fashion to form a generic activity indicator.

The $\overline{LINKT4}$, $\overline{LINKT}$, and $\overline{LINKFD}$ pins indicate when the CY7C971 is in the link pass state for

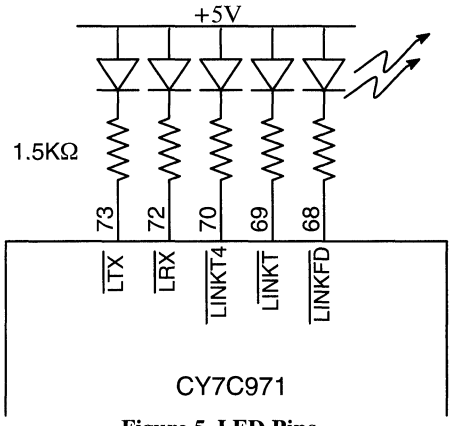


Figure 5. LED Pins

100BASE-T4, 10BASE-T, or 10BASE-T Full Duplex. The operating mode is determined either through the Auto-Negotiation process or by manual configuration with the control register (see section on MDC/MDIO Management Interface). The CY7C971 will enter a link pass state when an operating mode has been selected (either through Auto-Negotiation or manually) and properly formed technology dependent link integrity pulses are received from the medium. If only a single link indication is needed, the link indicator pins may be tied together in a wire-or fashion to form a generic link pass signal. These signals may also be individually connected to the 21140's General Purpose pins in order to quickly inform the MAC of any changes in the link status.

Configuration Pins

The configuration pins are wired for the adapter card application as shown in *Figure 6*. The ENT4, ENT, ENFD, AUTONEG are wired HIGH to enable all of the 7C971 operating modes. At power-up or during a hard reset, the logic values on these pins are loaded into their corresponding ability bits in the MII Status Register. The ability bits in the Status Register dictate whether an operating mode can be become active. After the power-up or reset cycle completes, the Auto-Negotiation process will advertise all operating modes that the Status Register reports as enabled. Management can alter the advertised abilities by changing the code word in the Auto-Negotiation Advertisement Register (Reg. 4).

The ISODEF (Isolate Default) pin is tied LOW in order to force the CY7C971 to power up with the MII ready for normal operation (not isolated). The Isolate Bit (0.10) will indicate normal operation as the default setting. The address pins (A0–A4) are wired for PHY address 01H. Address 00H is reserved for external transceivers and should not be used. The CY7C971 will respond to PHY management frames that use the assigned address. The values on the ISODEF and A0–A4 pins are latched into the 7C971 during a hard reset or power-on reset.

The MODE pin is tied HIGH to force the 7C971 into MII mode. MII mode enables the MII, PCS (Physical Coding Sublayer), and PLS (Physical Layer Signaling) logic. The PCS performs the 8B6T encoding/decoding and serial/parallel conversion for 100BASE-T4. The PLS performs Manchester encoding/decoding and serial/parallel conversion for 10BASE-T. When the MODE pin is LOW (PMA Mode), the MII, PCS, and PLS are disabled and the 100BASE-T4 PMA (Physical Medium Attachment) interface is exposed on the MII I/O pins. PMA Mode is used only in repeater applications.

The Test pin is tied LOW to permanently disable the CY7C971 test mode. Test mode is used for factory ATE testing only.

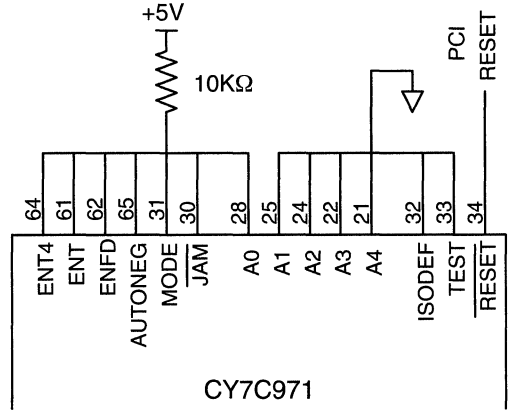


Figure 6. Configuration Pins

The $\overline{\text{RESET}}$ pin should be connected to the PCI reset pin on the card edge. Power-on reset is taken care of by an internally generated reset signal. During a hard or power-on reset, the values on the ENT4, ENT, ENFD, AUTONEG, ISODEF, and A0–A4 are loaded into the CY7C971 and all of the logic and analog circuits are forced to their default states. During a soft reset all of the logic and analog circuits are reset but the values on the configuration pins are ignored. The software drivers can issue a soft reset by setting the Reset Bit (0.15) in the Control Register. This bit is self clearing.

Layout Considerations

The adapter card design is simple enough to fit on a standard PCI short card (3.5" x 5") or smaller PCB. A 4 layer PCB construction with dedicated power and ground planes is recommended. The DEC 21140 requires a 3.3V power supply. The CY7C971 requires a 5V supply. Separate 5V and 3.3V power planes can be partitioned on a single power layer. *Figure 7* shows an example of partitioned power planes with component placement. The ground plane runs under both the 5V and 3.3V planes. There is a cutout in both the power and ground planes under the RJ–45 and transformer.

The media interface components can be neatly placed behind the RJ–45 connector. *Figure 8* illustrates the physical layout of the media interface with a 4-layer board. 0.027 µF decoupling capacitors are used on each of the CY7C971 power pins. These 0805 SMT capacitors are placed in a row as close to the pins as possible. The termination resistors fit neatly in a row behind the decoupling capacitors. Tantalum 10 µF capacitors are placed on opposite corners of the CY7C971. The CY7C971 media interface and power pins were placed in such a way to minimize the use of vias and simplify board layout.

Software Considerations

Software drivers are responsible for configuring registers within the DEC 21140 for proper operation with the CY7C971. The software drivers are also responsible for transferring Ethernet packets between the host computer's local memory and the

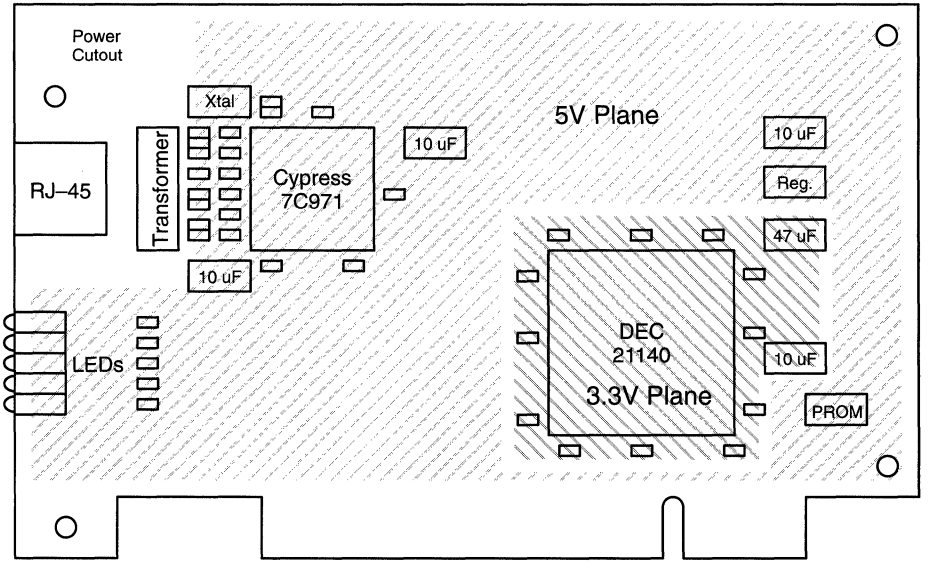


Figure 7. Power Plane and Component Placement

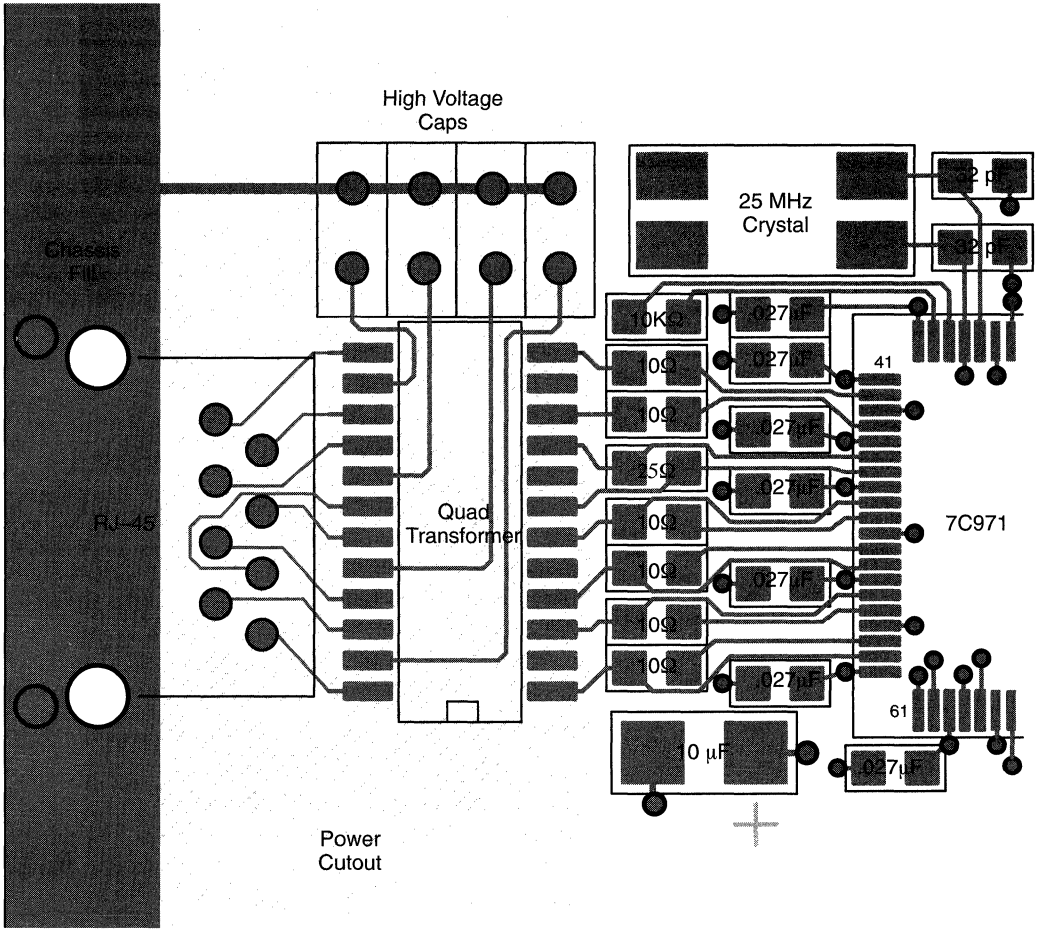


Figure 8. Media Interface Layout

21140's data buffers, and for managing the 21140 and CY7C971 resources during normal operation.

The CY7C971 contains an on-chip management facility that is accessed through its serial management port on the MII. The management facility consists of registers that report and control basic activities of the PHY such as Auto-Negotiation and link status.

The CY7C971 management facility acts as a slave device to management accesses from the MAC. Management data is transferred between CY7C971 and the DEC 21140 MAC with the MDC and MDIO pins on the MII. This connection is shown in *Figure 3*.

The DEC MAC emulates the management agent with its software drivers. During power-up, reset, or a down link, the drivers should poll the management registers to determine the result of Auto-Negotiation and the state of the link. While the link is up, the drivers should poll the CY7C971 Status Register on a timely basis to make sure the link is active. The CY7C971 was designed so that standard MII compliant software drivers can support the management facility.

DEC Register Set-Up

The 21140 Command and Status Registers (CSR) must be configured so that the 21140 communicates with the CY7C971 through the MII port. Register CSR6 in the 21140 controls the MAC-PHY interface configuration. The 21140 parallel MII port is enabled with the Port Select bit in CSR6 (CSR6, bit 18). When set, the MII port is enabled and the serial 10-Mb/s port is disabled.

The PCS Function and Scrambler Mode inside the 21140 must be disabled for proper operation with MII based transceivers such as the CY7C971. PCS and scrambler modes are used with 100BASE-X physical layer devices only. The PCS Function is disabled by clearing the PCS bit in CSR6 (CSR6, bit 23). The scrambler is disabled by clearing SCR bit in CSR6 (CRS6, bit 24).

The Transmit Threshold Mode (TTM) must be adjusted according to the operating speed of the link. This bit determines the number of bytes in a frame that must be stored in the transmit FIFO before the transmission process is initiated. In 10-Mb/s mode, the TTM bit (CSR6, bit 22) should be set. In 100-Mb/s mode, the TTM bit should be cleared. The link operating speed can be determined by polling the CY7C971 management Auto-Negotiation and Control registers or by monitoring the LED Link pins through the General Purpose Register.

MDC/MDIO Management Interface

The CY7C971 contains all of the standard and extended registers defined in the MII standard (Registers 0–7). There is also an additional CY7C971 specific register (Reg.16).The MAC can perform write and read operations to the CY7C971 management registers by transferring management frames over the MDIO serial interface. The MDC signal serves as the management data clock and is sourced from the MAC. The MDIO signal is bidirectional. The frame structure is shown in *Figure 9*.

The management frame is comprised of several fields. The start sequence 01 is used to identify the start of a frame. The op-code field determines whether a read, write, or no-op will be performed. The address field determines the target PHY. The CY7C971 will only respond to management frames whose address matches the address assigned to the CY7C971 by the address pins A0–4. In this application, the CY7C971 address has been permanently wired to 01H. All management accesses to the CY7C971 should use this address.

The register field determines the target register for the operation. The turn around field provides time to switch the direction of the bus during a read operation. The next 16 bits are the data field. During a read operation, the PHY will drive the MDIO line with the target register contents. During a write operation, 16 bits are transferred to the PHY from the MAC and written in the target register.

The CY7C971 can accept management frames that are not preceded by a 32-bit preamble. A sequence of 32 ones will force a reset on the CY7C971 management facility. It is recommended that the MAC issue this 32-bit sequence after power-up and periodically during normal operation.

The CY7C971 supports the standard and expanded MII register set. The Expanded Register set includes the OUI (Organizationally Unique Identifier) and Auto-Negotiation registers (registers 2–7). *Figure 10* shows the CY7C971 register map.

Control Register (Reg. 0)

The Control Register is used to manually set the operating modes and enable/disable certain features. Auto-Negotiation can be enabled/disabled through this register with bit 0.12. When Auto-Negotiation is enabled, the speed of the link is determined automatically, and the speed selection bit (0.13) has no effect. When Auto-Negotiation is disabled, the speed selection bit determines the speed of the link.

The loop back bit (0.14) is used to internally loop the transmit signal path to the receive signal path. Placing the CY7C971 in loopback mode will cause the

	Start	Op Code	PHY Address	Register Number	Turn Around	Data
Read	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD
Write	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD

Figure 9. Management Frame Structure

link to be broken and the transmit drivers will be forced to idle. The power-down bit (0.11) places the CY7C971 in low power stand-by mode. All of the analog circuits are placed in low power mode and the clock is stopped to all of the CMOS digital logic. Only the MDC/MDIO port is active. When power-down mode is exited, the CY7C971 will reset all of the registers to their default values. Any register setting other than the default value must be restored by the driver.

Status Register (Reg. 1)

The Status Register is a read-only register that reports the capabilities and status of the CY7C971. The status of the Auto-Negotiation process can be monitored through bit 1.5. This bit reports when Auto-Negotiation has completed. The Remote Fault bit (1.4) will indicate if Auto-Negotiation has detected a remote fault at the other end of the link. The Link Status bit indicates whenever any technology (i.e., the 10BASE-T or the 100BASE-T4 circuits of the CY7C971) has entered the Link Pass State. This means that the link is available for data transmission and reception.

OUI Registers (Reg. 2–3)

Registers 2 and 3 contain the Cypress Semiconductor Organizationally Unique Identifier and the CY7C971 part and revision number. The OUI is a 24-bit sequence that is uniquely assigned to organizations for identification purposes by the IEEE.

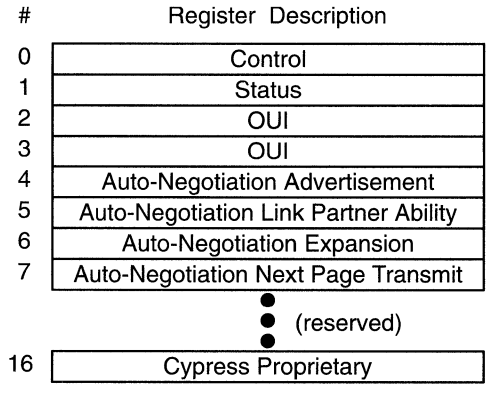


Figure 10. Register Map

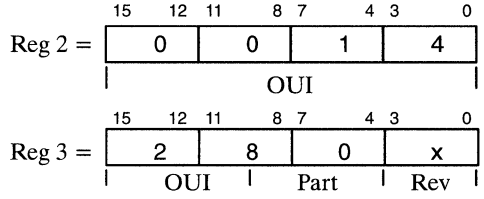


Figure 11. OUI Registers

The Cypress OUI is 00A050h. According to the Ethernet MII standard, twenty-two bits of the OUI are split between Registers 2 and 3. Register 2 contains 16 bits of the OUI and register 3 contains the other 6. Register 3 also contains 6 bits for the CY7C971 part number and 4 bits for the revision number. The register mapping and contents are shown in *Figure 11*.

Auto-Negotiation Registers (Reg. 4–7)

Registers 4 through 7 manage the Auto-Negotiation process. These registers only have meaning when Auto-Negotiation is enabled. Management intervention is not required during the normal Auto-Negotiation process. Management should only intervene with the Auto-Negotiation process in order to influence the outcome.

The Auto-Negotiation Advertisement Register (Reg. 4) holds the 16-bit code word that the CY7C971 advertises over the medium. This code word encodes the capabilities of the CY7C971, the LAN technology (CSMA/CD Ethernet), and fault indications. During power-up or reset, this register will set to the default conditions of the CY7C971 that are dictated by the enable pins. This causes Auto-Negotiation to only advertise the capabilities that are enabled. These enabled capabilities are reflected in the Status register. Management may intervene in the Auto-Negotiation process by writing to this register. Only the operating modes that are enabled in the Status Register will be advertised. Any attempt to advertise a disabled mode (disabled when ENx pin is LOW) by writing to the Advertisement Register will be ignored. Management should restart the Auto-Negotiation process by setting bit 0.9 (Restart Auto-Negotiation Bit) if the contents of the Advertisement Register are changed. *Figure 12* shows a block diagram of how the enable pins affect

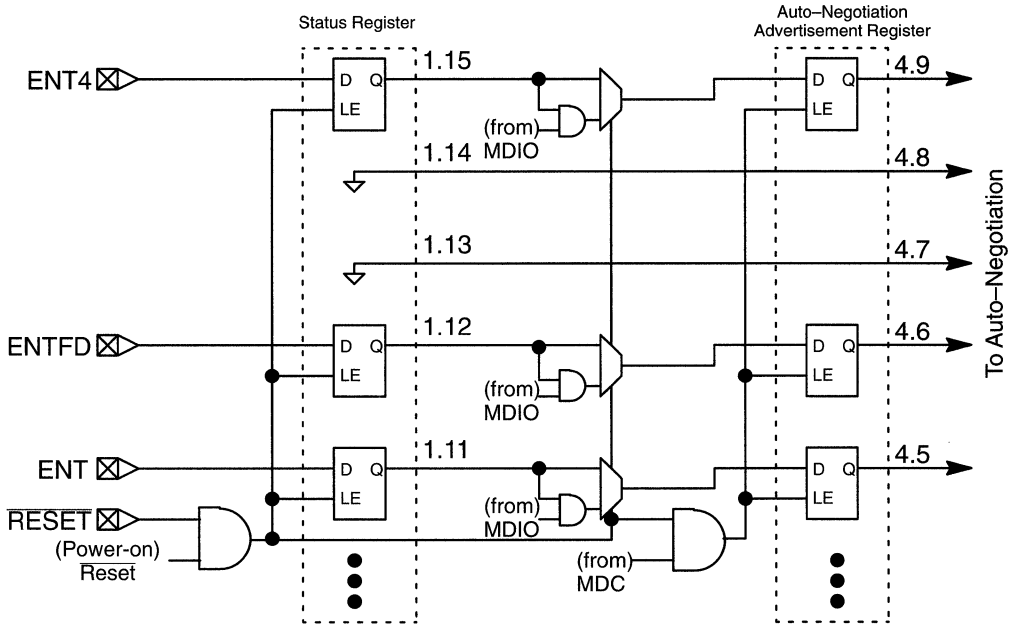


Figure 12. Register Block Diagram

Auto-Negotiation Advertisement and Status Registers.

The Auto-Negotiation Link Partner Ability Register (Reg. 5) contains the code word that has been consistently received from the PHY at other end of the medium. This register is valid when the Page Received bit (6.1) is set in Register 6. Auto-Negotiation uses the received code word to decide the operating mode of the link. The choice is based on the priority resolution table in the Auto-Negotiation standard. 100BASE-T4 has the highest priority. If Auto-Negotiation completes through parallel detection, the contents of this register are invalid. (Parallel Detection part of the Auto-Negotiation process. Its function is to detect the presence of Ethernet transceivers that do not support Auto-Negotiation.)

The Auto-Negotiation Expansion Register (Reg. 6) is a Read-Only register that reports the status of the Auto-Negotiation process. This register should be monitored during the Auto-Negotiation process in order to make sure that code words are being received and that there is not a Parallel Detection fault.

Register 7 is used to hold the Next Page code word that is to be transmitted during next page exchanges. Next Pages are code words that can be sent in addition to the base code word in the advertisement register. The Next Page facility is intended to be used as a simple scheme for passing messages between the PHYs on the medium before the link becomes active. The messages may contain information such as the presence of a fault, for example. The Next Page Transmit Register defaults to 2001H (Null Message) after power-up or a reset.

Cypress Proprietary Register (Reg. 16)

The Cypress Proprietary Register (Reg. 16) contains specific information about the CY7C971. Bit 15 indicates the polarity of the RX_D2± signal pair. When clear, this bit indicates that the polarity of RX_D2± is correct or undetermined. When set, this bit indicates that inverted polarity on RX_D2± was detected and has been corrected. Inverted po-

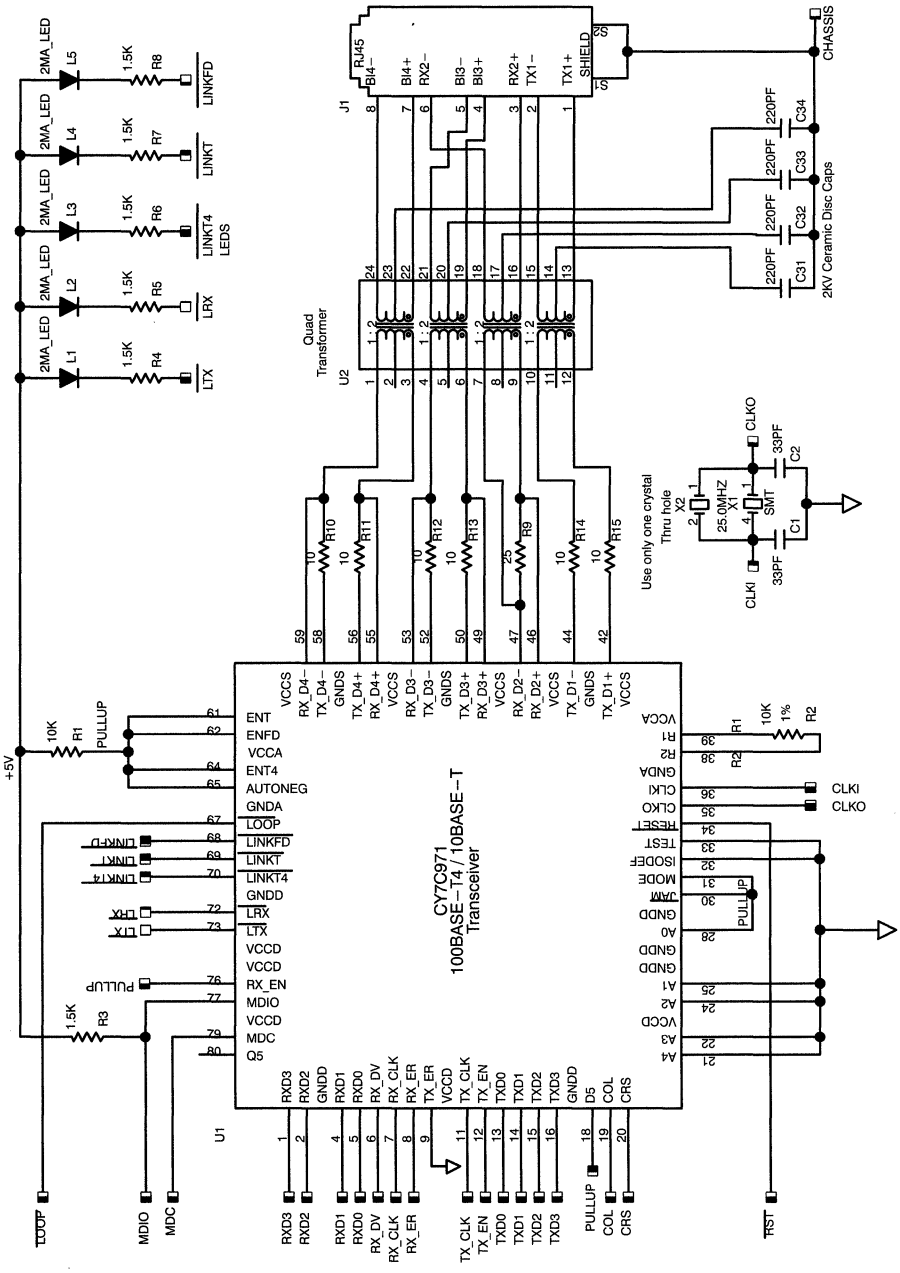
larity is most likely caused by inadvertently reversing the signal wires at the medium connector.

Conclusion

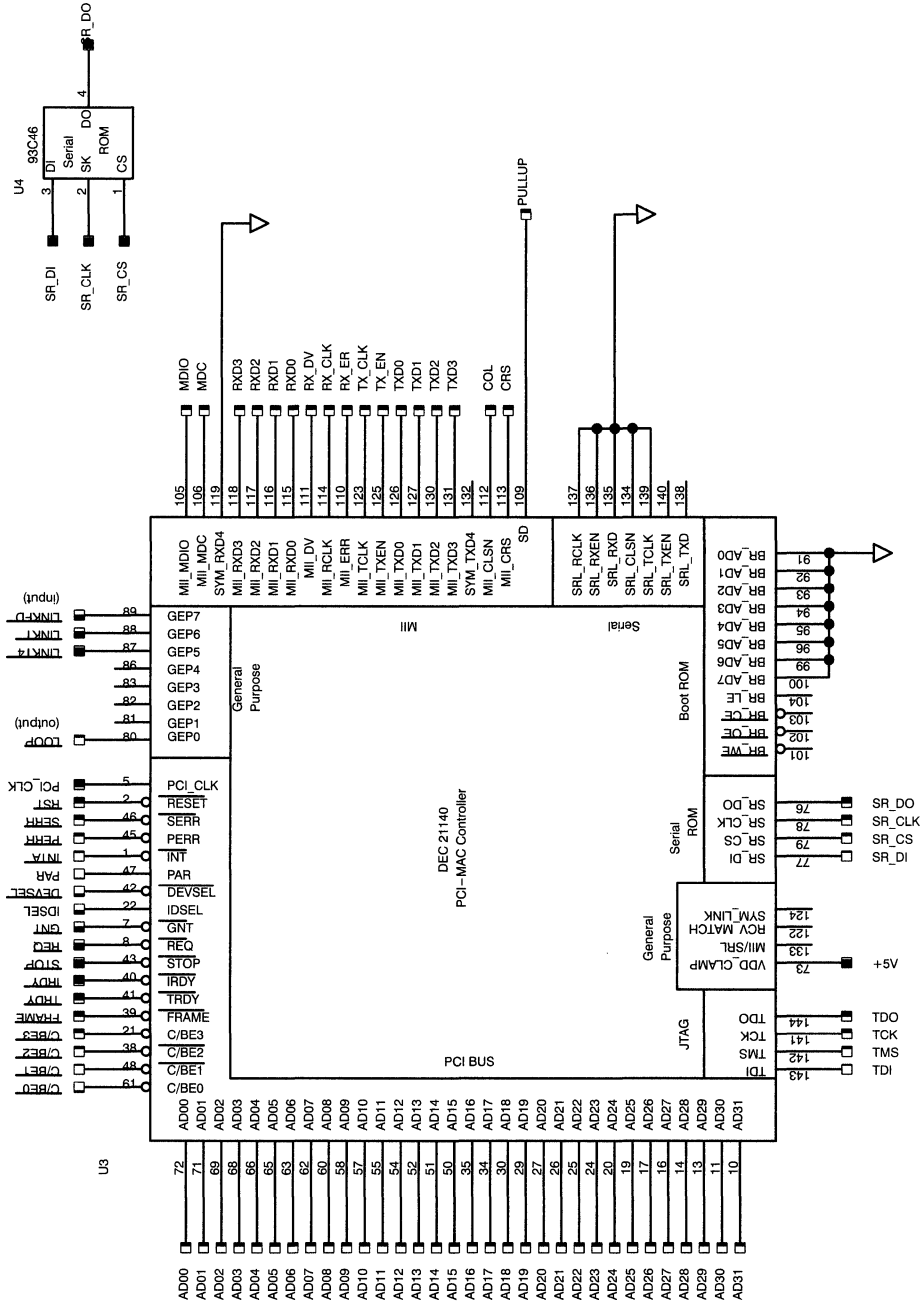
This application note covers the major issues for a dual speed Ethernet/PCI Bus adapter card design using the CY7C971 100BASE-T4/10BASE Transceiver and DEC21140 MAC. The high degree of integration in the CY7C971 keeps the number of external components to a minimum helping to reduce system cost and design effort.

The complete adapter card schematics and a bill of materials are included at the end of this application note (Appendix A and Appendix B, respectively). More information on the CY7C971 can be found in the data sheet. For more information on 100BASE-T4, MII and Auto-Negotiation standards, consult the IEEE 802.3u document: "MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100Mb/s Operation."

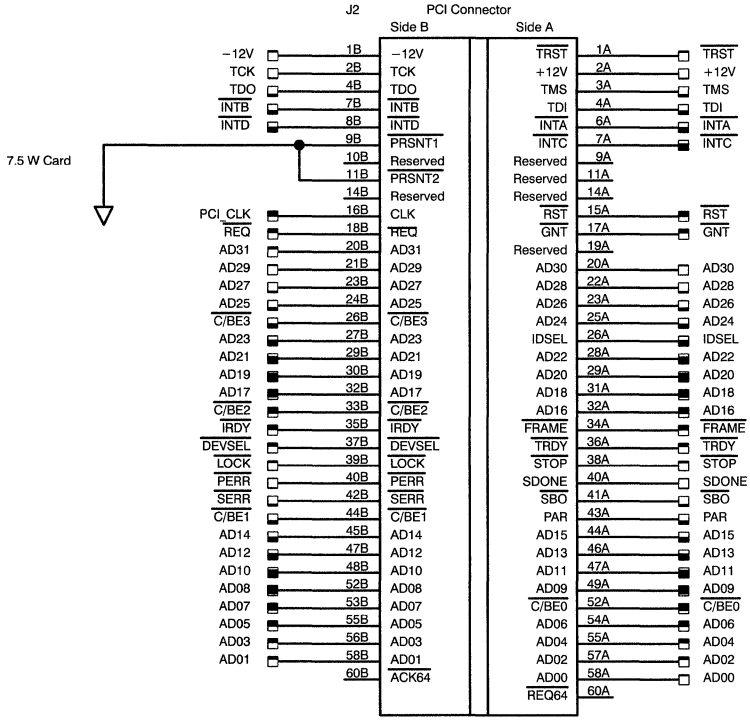
Appendix A. Schematics (Sheet 1 of 4)



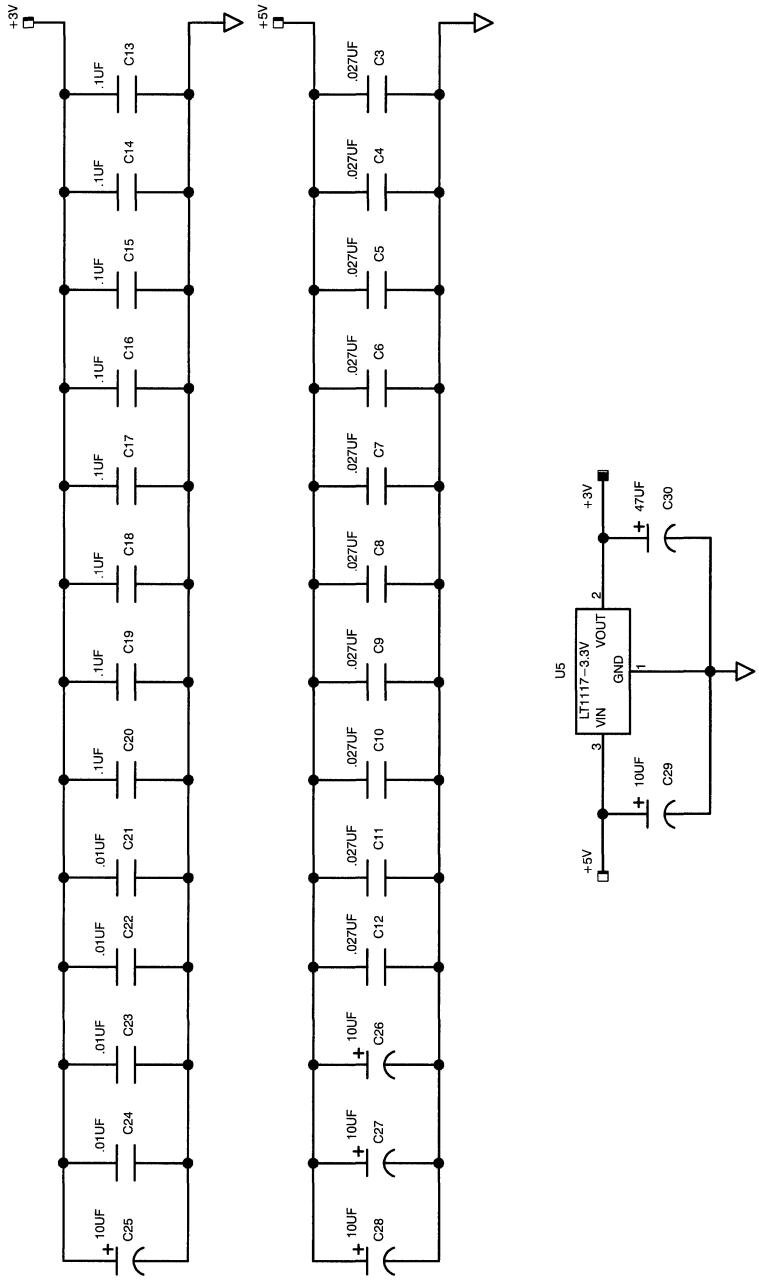
Appendix A. Schematics (Sheet 2 of 4)



Appendix A. Schematics (Sheet 3 of 4)



Appendix A. Schematics (Sheet 4 of 4)



Appendix B. Parts List

Description, Vendor, Part Number	Qty	Reference Designator
10 µF/16V Tantalum Capacitor (EIA Size C) Sprague Elec. 293D106X9016C2	6	C25, C26, C27, C28, C29, C31
47 µF/16V Tantalum Capacitor (EIA Size D) Sprague Elec. 293D476X9016D2	1	C30
.1 µF/50V Ceramic Capacitor (Size 1206) Panasonic ECU−V1H104KBW	8	C13, C14, C15, C16, C17, C18, C19, C20
.01 µF/50V Ceramic Capacitor (Size 1206) Panasonic ECU−V1H103KBM	4	C21, C22, C23, C24
.027 µF/50V Ceramic Capacitor (Size 0805) Panasonic ECU−V1H273KBX	10	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12
33 pF/50V Ceramic Capacitor (Size 0805) Panasonic ECU−V1H330JCG	2	C1, C2
220 pF/2KV Ceramic Disk Capacitor Murata/Erie DE0405B2212KV	4	C31, C32, C33, C34
10.0K ohm 5% 1/8W Resistor (Size 0805) Panasonic ERJ−6GEYJ10.0K	1	R1
10.0K ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF10.0K	1	R2
10.0 ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF10.0	6	R10, R11, R12, R13, R14, R15
24.9 ohm 1% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF24.9	1	R9
1.50K ohm 5% 1/10W Resistor (Size 0805) Panasonic ERJ−6ENF1.50K	6	R3, R4, R5, R6, R7, R8
2 mA Green LED, PC Board Side Mount IDI 5350T5LC	3	L3, L4, L5
2 mA Yellow LED, PC Board Side Mount IDI 5350T7LC	1	L2
2 mA Red LED, PC Board Side Mount IDI 5350T1LC	1	L1
25.0000 MHz SMT Crystal, Parallel Res 18 pF Epson Amer MA−506 25.000M−AD Epson Amer MA−406 25.000M−G	1	X1
25.0000 MHz HC−49/U Crystal, Parallel Res 18 pF Ecliptek EC250−25.0000	1	X2
Quad 2:1 Transformer, 330 µH Primary, 1500V Valor ST6115 Pulse PE−69001 Bel S553−1204−00	1	U2
CY7C971 100BASE-T4/10BASE-T Transceiver Cypress Sem. CY7C971−NC	1	U1

Appendix B. Parts List (continued)

Description, Vendor, Part Number	Qty	Reference Designator
LT1117 3.3V Regulator Linear Tech. LT1117CST−3.3	1	U5
RJ−45 Modular 8-Pin Shielded Jack Amp 555141−1	1	J1
DEC21140 Fast Ethernet PCI MAC Digital Sem. 21140−AA	1	U3
93C46 1K Serial EEPROM (8-Pin SOIC) National Sem. NM93C46M8	1	U4

Assembly Instructions

1. Assemble only 1 crystal (X1 or X2).

100BASE-T4 Ethernet Repeater

Background

This application note describes the design of a 100BASE-T4 Ethernet Network Repeater using the Cypress CY7C971 PHY and CY7C388P for the core logic. The repeater has the following features:

- 100-Mb/s Shared Bandwidth over Cat. 3 UTP
- 8 Unmanaged Ports
- Integrated Transmit Filters
- Compact Layout
- Low Latency

The function of the repeater is to create a logically shared communication channel between the end stations in the network. The end stations (computer, printer, etc.) communicate with the repeater over dedicated twisted pair links. The repeater listens to the signal being received on one port and "repeats" the restored signal to the other ports. *Figure 1* illustrates the function of the repeater in a 100BASE-T4 Ethernet Network. The repeater in this application note has eight communication ports.

The functional requirements of the 100BASE-T4 repeater are defined in the IEEE 802.3u Standard "MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100 Mb/s Operation," Clause 27. The repeater functional requirements are summarized below:

- Detect port activity and receive Ethernet packets
- Restore the shape, amplitude, and timing of the received signals prior to retransmission

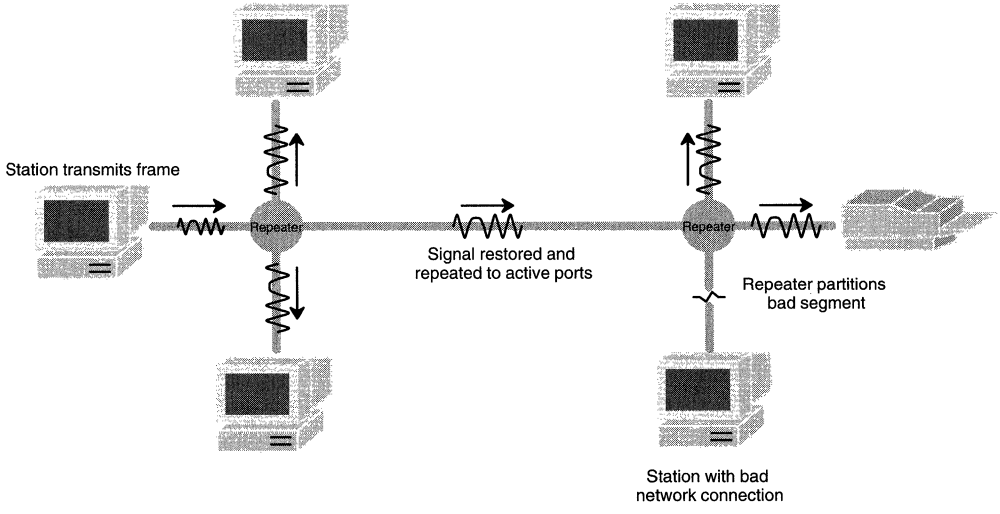


Figure 1. Ethernet Network Built with Repeaters

- Regenerate preamble sequence and prepend it to the received frame
- Forward the Ethernet frame to each of the ports
- Detect collisions between ports and generate jam sequence to all ports
- Protect network from long carrier events (jabber) and repeated collisions (partition)
- Allow installation (removal) of station without network disruption
- Provide basic port control (enable/disable)

Repeater Block Diagram

A block diagram of the 8-port repeater is shown in *Figure 2*. The CY7C971 functions as the physical layer device that interfaces the digital core logic to the twisted-pair medium. Each CY7C971 requires a quad 1:2 transformer for electrical isolation from the medium. The core logic is implemented with a CY7C388A FPGA. This device takes care of the basic repeater functions such as data retiming, sequence generation, and port control.

CY7C971

The CY7C971 (see *Figure 3*) has a special low latency repeater mode that is enabled when the MODE pin is LOW. In this mode, the MII (Media Independent Interface), PCS (Physical Coding Sublayer), and 10BASE-T are disabled. Only the 100BASE-T4 PMA (Physical Medium Attachment) circuits are active. These circuits perform the analog functions required to interface to the twisted-pair media such as transmit filtering, adaptive equalization, and clock recovery. A block diagram of the PMA interface is shown in *Figure 4*.

Media Dependent Interface (MDI)

The CY7C971 provides a simple interface to the 8-pin modular RJ−45 jack. No expensive external filters or components are necessary because all transmit filtering and equalization are performed on-chip. A quad 2:1 transformer for electrical isolation and termination resistors to match the cable impedance are all that is required.

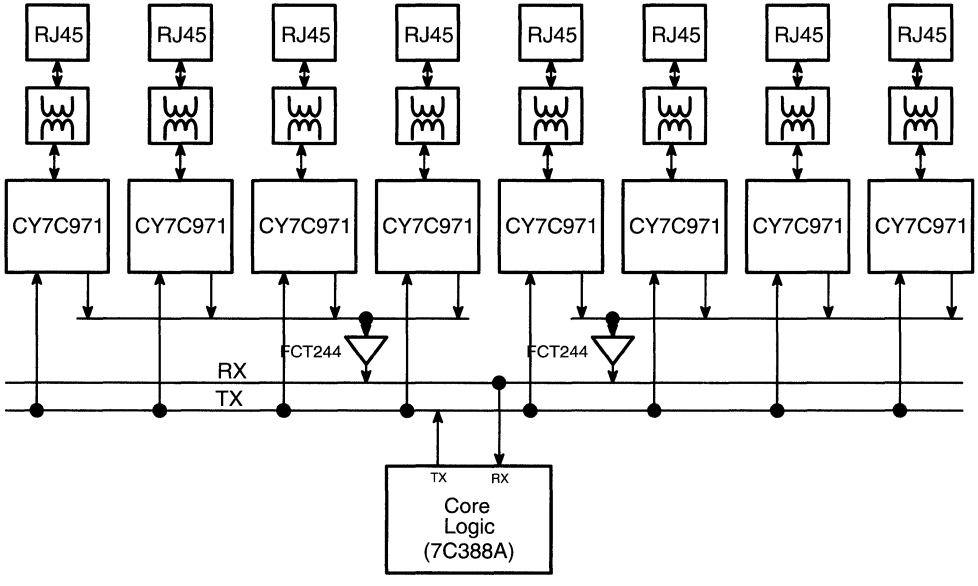


Figure 2. Repeater Block Diagram

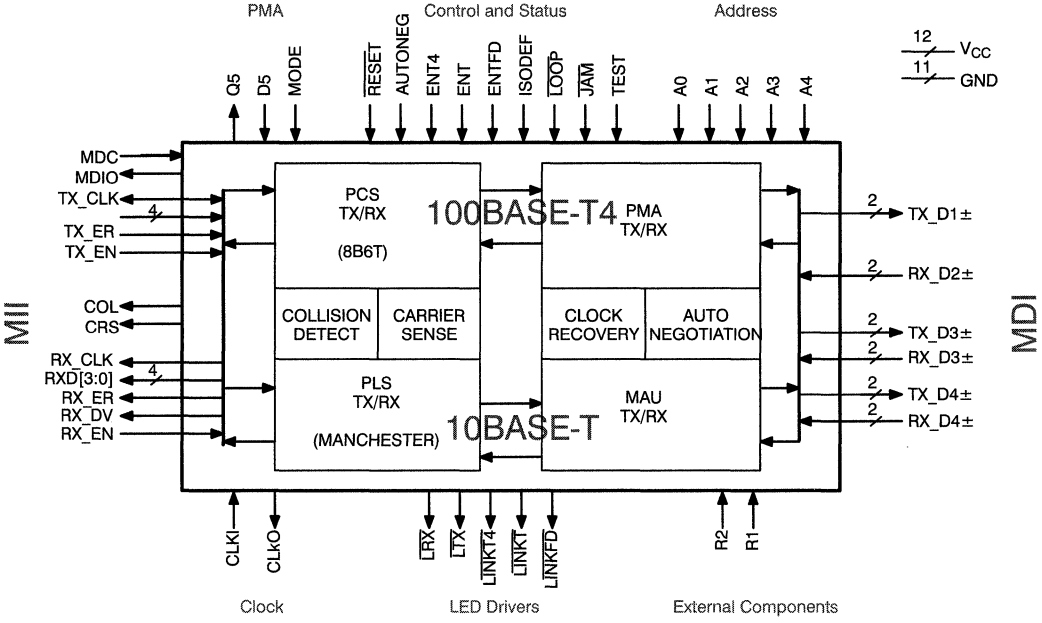


Figure 3. CY7C971 Block Diagram

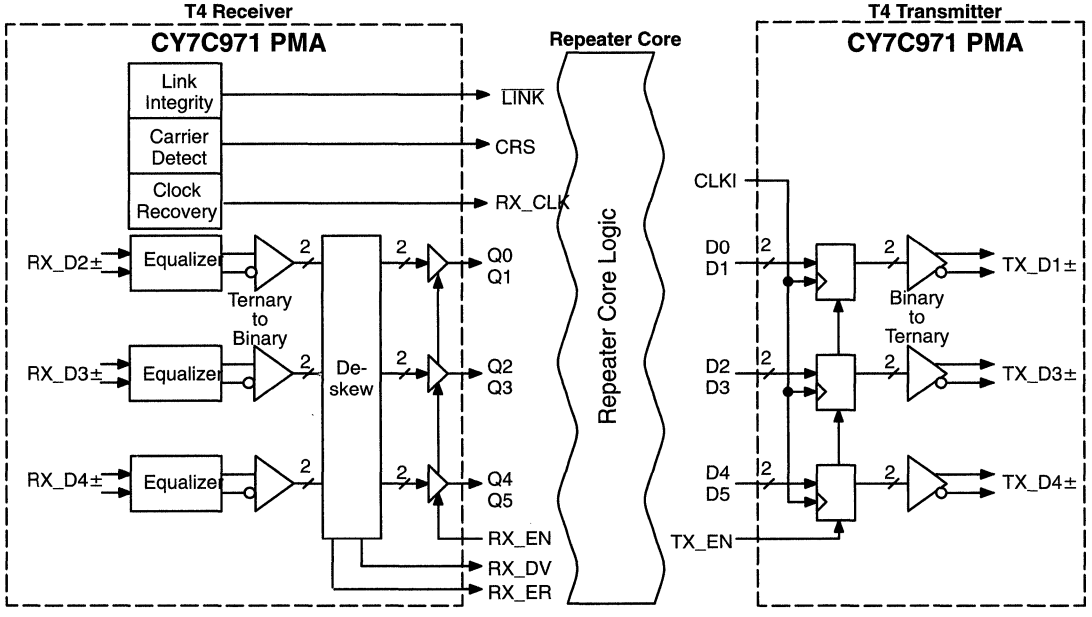


Figure 4. CY7C971 PMA Interface

The output buffer design uses a feedback voltage driver that minimizes power consumption and controls the common-mode output voltage. The transformer provides sufficient common mode rejection over the frequencies of interest so that an external common mode choke is not needed. *Figure 5* shows a schematic of the media interface with the CY7C971.

The characteristic impedance of the twisted pair medium is a nominal 100Ω The 1:2 transformer reduces (by the square of the turns ratio) medium load impedance to 25Ω on the primary (971) side. The termination resistors and the output buffer impedance together form a matching 25-ohm load. The matching load insures that maximum signal is transferred to the medium and minimizes reflections due to impedance mismatch.

The center taps on the media side of the transformer are connected to the chassis ground through 220-pF (minimum) high-voltage (2 KV) capacitors. These capacitors help absorb common mode noise that is picked up or generated on the twisted pair medium. The capacitors must be capable of withstanding the isolation requirements specified in the 100BASE-T4 standard. High voltage ceramic disc capacitors are economical and work well in this application.

The high precision currents needed for the transmit DAC and equalizer are derived from the external 10KΩ 1% resistor on pins R1 and R2. An internally generated band-gap voltage reference is used by the CY7C971 for all internal reference voltages.

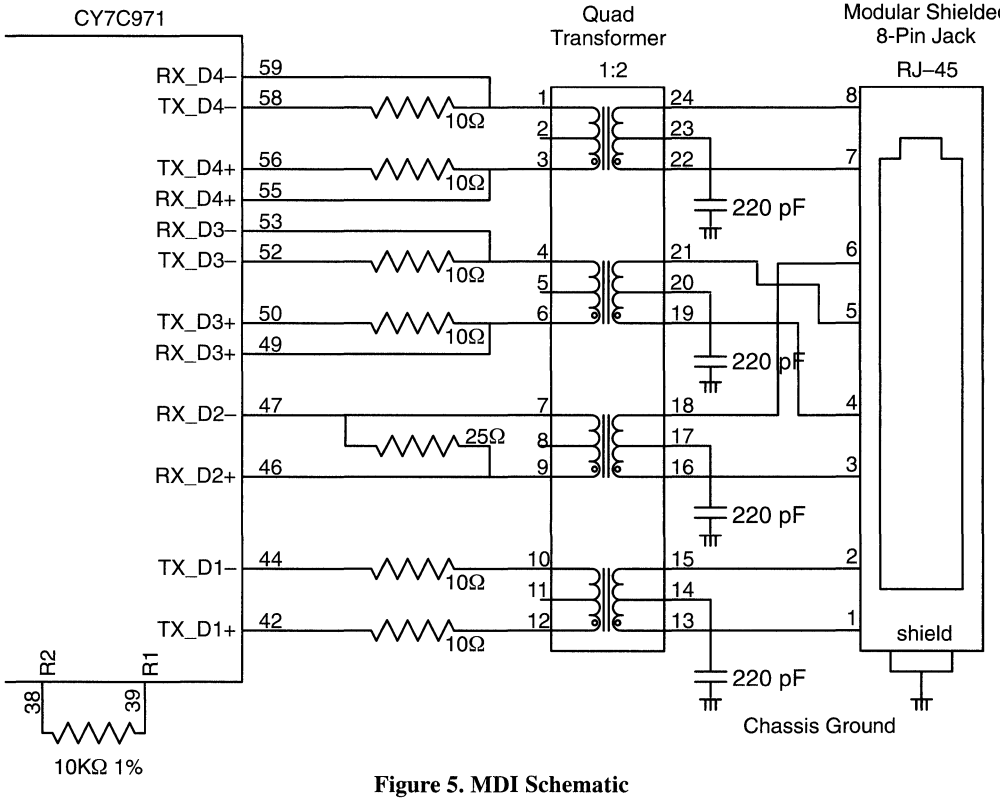


Figure 5. MDI Schematic

LED Pins

Figure 6 shows how the LED pins connect to the LEDs. The $\overline{\text{LINKT4}}$ pin indicates when the CY7C971 is in the link pass state for 100BASE-T4. The CY7C971 will enter a link pass state when properly formed technology dependent link integrity pulses are received from the medium. The $\overline{\text{LINKT}}$ and $\overline{\text{LINKFD}}$ signals remain inactive.

Configuration Pins

The configuration pins are wired for the repeater application as shown in *Figure 7*. The MODE pin is tied LOW to force the CY7C971 into 100BASE-T4 PMA mode. PMA mode disables the MII, PCS (Physical Coding Sublayer), and 10BASE-T. The 100BASE-T4 PMA performs all of the analog functions required to interface to 4 pair Cat. 3 UTP.

The ENT4 pin is wired HIGH to enable 10BASE-T4. The ENT and ENFD pins are wired LOW to disable 10BASE-T and Full Duplex operation. The AUTONEG pin is wired to a header block and pull-up. When a jumper is installed in the header block, Auto-Negotiation is disabled. When the jumper is absent, Auto-Negotiation is enabled.

The ISODEF (Isolate Default) pin is tied LOW in order to force the CY7C971 to power up with the MII ready for normal operation (not isolated). This

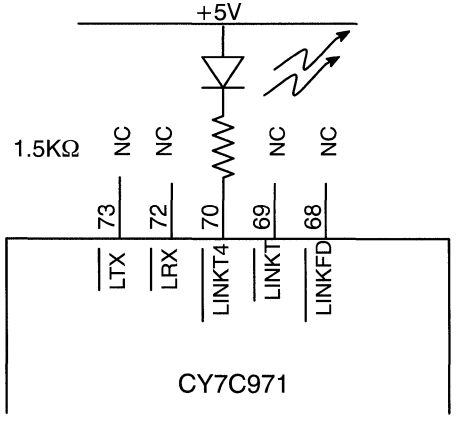


Figure 6. LED Pins

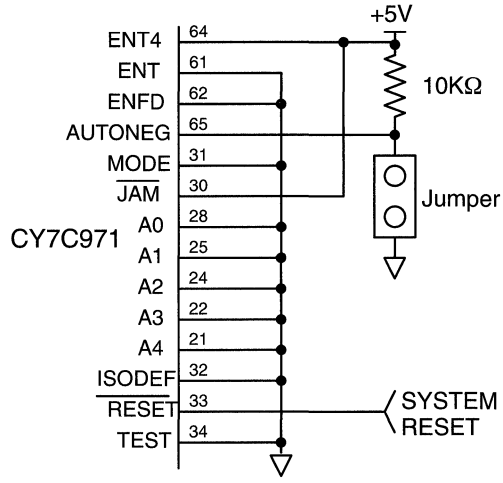


Figure 7. Configuration Pins

repeater application does not use the management port. The address pins can be assigned any address configuration.

The Test pin is tied LOW to permanently disable the 971 test mode. Test mode is used for factory ATE testing only.

The $\overline{\text{RESET}}$ pin should be connected to the system reset pin from the core logic. A system reset is issued at power-up or when the reset button is pushed. If a port is disabled by the core logic, the reset to the port will be active.

Layout Considerations

The repeater design is simple enough to fit on a small 7.75 in x 6.0 board using top-side-only placement. A four-layer PCB construction with dedicated power and ground planes is recommended. The CY7C971 requires a 5V supply. *Figure 8* shows an example of component placement.

The media interface components can be neatly placed in-line with the CY7C971. 0.027 µF decoupling capacitors are used on the CY7C971 power pins. These 0805 SMT capacitors are placed in a row as close to the pins as possible. The termination resistors fit neatly in a row behind the decoupling capacitors. The CY7C971 media interface and power

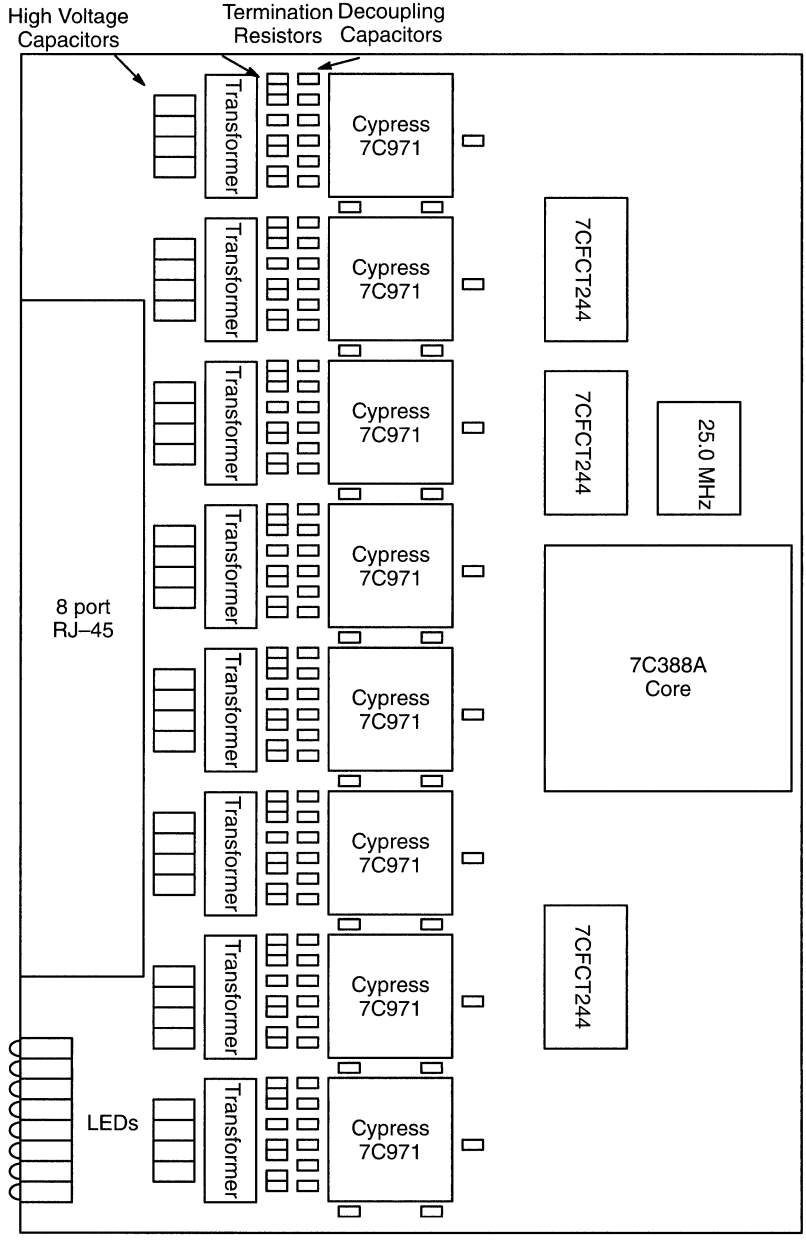


Figure 8. Component Placement

pins are placed in such a way to minimize the use of vias and simplify board layout.

Core Logic

Figure 9 shows a block diagram of the repeater core logic. The blocks perform functions as follows:

- **Port N.** Synchronizes signals and provides control signals to each port, along with detecting jabber and partition conditions.
- **Selection and Clock MUX.** Selects the receive clock from the incoming port and provides a common receive clock for use in retiming the incoming data.
- **RX FIFO.** Used for temporary storage and to retime the incoming data to TX_CLK.
- **Bad Symbol, Jam, Idle, Preamble Generator.** Provides the special characters that are transmitted during different conditions.
- **Output Register.** Provides temporary storage of outgoing data along with retiming to the TX_CLK.
- **Repeater State Machines and Logic.** Controls port selection during data reception. Also, provides collision detection and handling. Included in this block is the control of two expansion ports for use in the design of a stackable repeater.

The core logic is written in Verilog and fills 7K gates of a Cypress CY7C388P 8K pASIC.

Conclusion

This application note covers the major issues for a 8-port 100BASE-T4 Repeater design using the CY7C971 100BASE-T4/10BASE-T Transceiver and CY7C388P 8K FPGA. The high degree of integration in the CY7C971 keeps the number of external components to a minimum, helping to reduce system cost and design effort.

The complete repeater schematics and a bill of materials are available from Cypress Semiconductor. More information on the CY7C971 can be found in the data sheet. For more information on 100BASE-T4, MII, and Auto-Negotiation standards, consult the IEEE 802.3u document: "MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100Mb/s Operation."

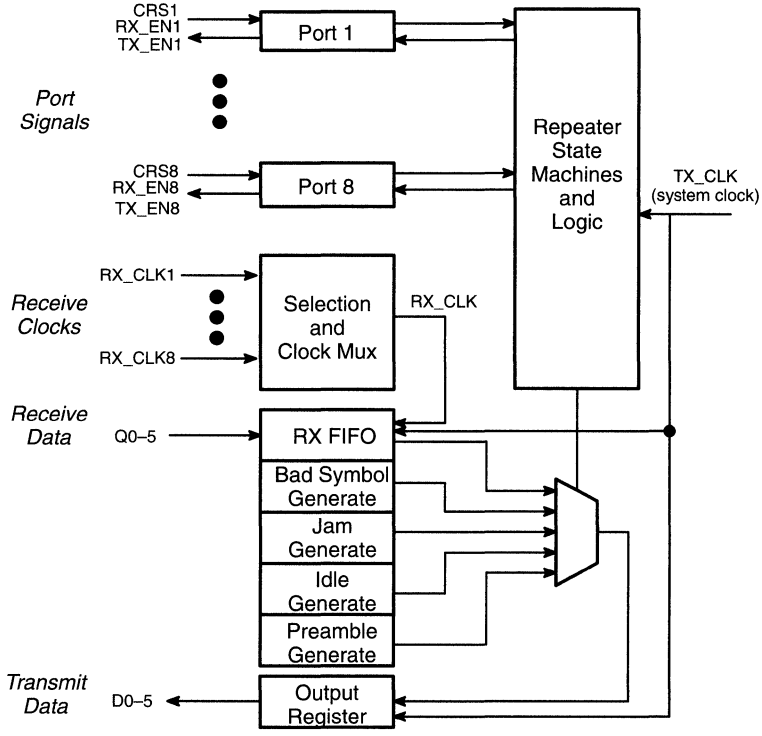


Figure 9. Core Logic

Asynchronous Transfer Mode (ATM) 3

ATMs

CY7B951

Local Area Network ATM Transceiver

Features

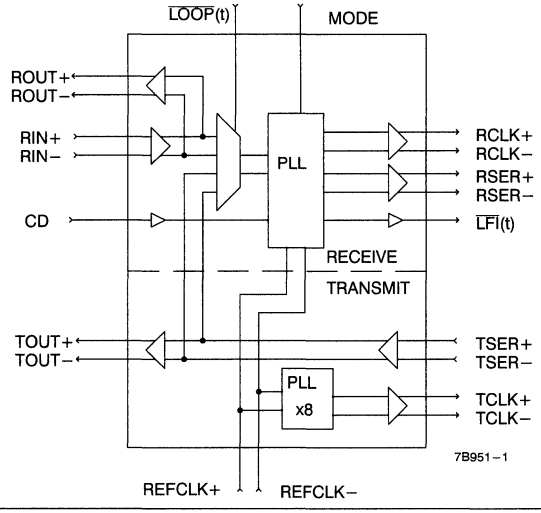
- SONET/SDH and ATM Compatible
- Compatible with PMC–Sierra PM5345 SUNI™
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- 100K ECL compatible I/O
- No output clock "drift" without data transitions
- Link Status Indication
- Loop-back testing
- Single +5V supply
- 24-pin SOIC
- Compatible with fiber-optic modules, coaxial cable, and twisted pair media
- No external PLL components
- Power-down options to minimize power or crosstalk
- Low operating current: <65 mA
- 0.8μ BiCMOS

Functional Description

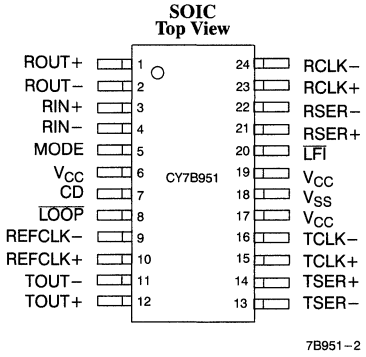
The Local Area Network ATM Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

3

Logic Block Diagram



Pin Configuration



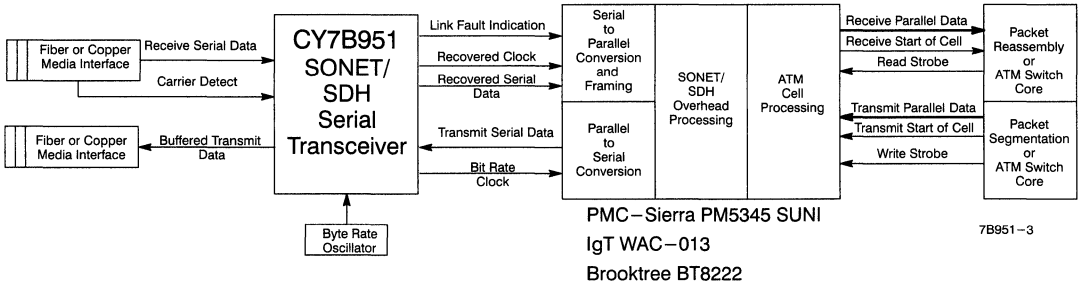


Figure 1. SONET/SDH and ATM Interface

SUNI is a trademark of PMC-Sierra, Incorporated.

Pin Descriptions

Name	I/O	Description
RIN±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embeded clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signaling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN− to V_{SS}.
ROUT±	ECL Out	Receive Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data dependent jitter. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
RSER±	ECL Out	Recovered Serial Data. These ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	Recovered Clock. These ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK×8 frequency. Also, the Link Fault Indicator ($\overline{LFI}$) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
$\overline{LFI}$	TTL Out	Link Fault Indicator. This output indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the $\overline{LFI}$ output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the $\overline{LFI}$ output will be LOW. If CD is at a TTL LOW then the $\overline{LFI}$ output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the $\overline{LOOP}$ pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect TSER+ to V_{CC} and TSER− to V_{SS}.
TOUT±	ECL Out	Transmit Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.
REFCLK±	Diff/TTL In	Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK− is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	Transmit Clock. These ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
$\overline{LOOP}$	TTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the $\overline{LOOP}$ input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When $\overline{LOOP}$ is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

Pin Descriptions (continued)

Name	I/O	Description
MODE	3-Level In	Frequency Mode Select. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS−3 (STM−1) line rate of 155.52 MHz. When this input is held LOW the two PLLs operate at the SONET STS−1 line rate of 51.84 MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE input is left floating or held at $V_{CC}/2$ the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
V_{CC}		Power.
V_{SS}		Ground.

Description

The CY7B951 Local Area Network ATM Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system (see *Figure 1*).

Operating Frequency

The CY7B951 operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. The MODE input has three different functional selections. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test mode.

Transmit Functions

The transmit section of the CY7B951 contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK×8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The CY7B951 Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter as shown in *Figure 1*.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK− are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK− or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the CY7B951 yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the receiver is to recover clock (RCLK±) and data (RSER±) from the incoming differential PECL data stream (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2.5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK×8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin as explained earlier. To insure accurate data and clock recovery, REFCLK×8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK×8 frequency accuracy be within 20−100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW (≤2.5V Max.), the $\overline{\text{LFI}}$ output will transition LOW and the Receiver PLL will align itself with the REFCLK×8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the CY7B951 has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The CY7B951 will detect a quiet link by counting

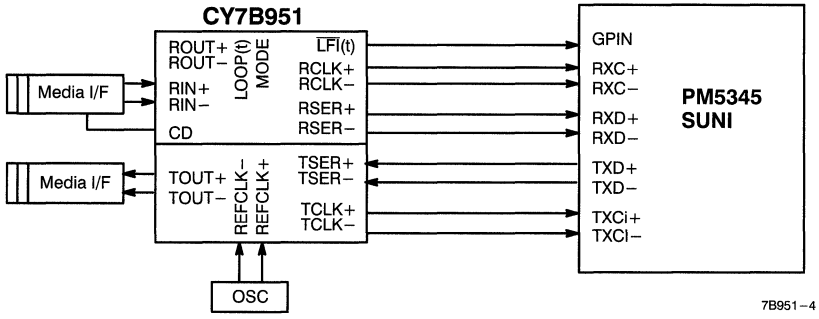


Figure 2. CY7B951 to PMC−Sierra PM5345 SUNI Connection Diagram

the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, $\overline{\text{LFI}}$ will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{\text{LFI}}$ will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW ($\leq$0.8V). When CD is pulled to a TTL LOW the $\overline{\text{LFI}}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLKX8 frequency. $\overline{\text{LFI}}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loop Back Testing

The TTL level $\overline{\text{LOOP}}$ pin is used to perform loop-back testing. When $\overline{\text{LOOP}}$ is asserted (held LOW) the Transmitter serial input (TSER±) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{\text{LOOP}}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{\text{LOOP}}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{\text{LOOP}}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power Down Modes

There are several power-down features on the CY7B951. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator ($\overline{\text{LFI}}$) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

The CY7B951 can be used in Local Area Network ATM applications. The operating frequency of the CY7B951 is centered around the SONET/SDH STS−1 rate of 51.84 MHz and the SONET/SDH STS−3/STM−1 rate of 155.52 MHz. This device can also be used in data mover and Local Area Network (LAN) applications that operate at these frequencies.

The CY7B951 can provide clock and data recovery as well as output buffering for physical layer protocol engines such as the SONET/SDH and ATM processing application shown in *Figures 1* and *2*

Figure 1 shows the CY7B951 in an ATM system that uses the PMC−Sierra PM5345 SUNI, or the IgT WAC−013, or the Brooktree BT8222 device. Assuming that PM5345 SUNI is used, the CY7B951 will recover clock and data from the input serial data stream and pass it to the PM5345 SUNI. The SUNI device will perform serial to parallel conversion, SONET/SDH overhead processing and ATM cell processing and then pass ATM cells to an ATM packet reassembly engine. On the Transmit side, a segmentation engine will divide long packets of data such as Ethernet packets into 53 byte cells and pass them to the SUNI. The SUNI device will then perform ATM cell processing, such as header generation, SONET/SDH overhead processing and parallel to serial conversion. This serial data will then be passed to the CY7B951 which will buffer this data stream and pass it along to the transmission media.

The CY7B951 provides the necessary clock and data recovery function to the PM5345. These differential PECL clock and data signals interface directly with the RXD± and RXC± inputs of the SUNI device as show in *Figure 2*. In addition, the CY7B951 provides transmit data output buffering for direct drive of cable transmission media. Lastly, the CY7B951 provides a bit rate reference clock to the SUNI transmitter by multiplying a local clock by eight allowing an inexpensive crystal oscillator to be used for the local reference.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL Outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Notes:
1. T_A is the "instant on" case temperature.

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

3

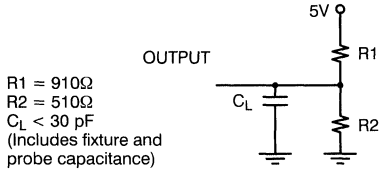
Electrical Characteristics Over the Operating Range

Parameter	Description		Test Condition	Min.	Max.	Unit
TTL Compatible Input Pins (LOOP, REFCLK+, REFCLK−)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			−0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK	$V_{IN}=V_{CC}$	+0.5	+200	µA
		LOOP	$V_{IN}=V_{CC}$	−10	+10	µA
I_{ILT}	Input LOW Current	REFCLK	$V_{IN}=0.0V$	−50	+50	µA
		LOOP	$V_{IN}=0.0V$	−500		µA
TTL Compatible Output Pins ($\overline{LFI}$)						
V_{OHT}	Output HIGH Voltage		$I_{OH}=-2$ mA	2.4		V
V_{OLT}	Output LOW Voltage		$I_{OL}=4$ mA		0.45	V
I_{OST}	Output Short Circuit Current		$V_{OUT}=0V$[2]	−15	−90	mA
ECL Compatible Input Pins (REFCLK ± CD, TSER±, RIN±)						
I_{IHE}	ECL Input HIGH Current	REFCLK/CD	$V_{IN}=V_{IHE(MAX)}$		+250	µA
		TSER/RIN	$V_{IN}=V_{IHE(MAX)}$		+750	µA
I_{ILE}[3]	ECL Input LOW Current	REFCLK/CD	$V_{IN}=V_{ILE(MIN)}$	+0.5		µA
		TSER/RIN	$V_{IN}=V_{ILE(MIN)}$	−200		µA
V_{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V_{IHE}	Input High Voltage	TSER/RIN			V_{CC}	V
		REFCLK		3.0	V_{CC}	V
		CD		$V_{CC}-1.165$	V_{CC}	V
V_{ILE}	Input LOW Voltage	TSER/RIN		2.0		V
		REFCLK		2.5		V
		CD (ECL)		2.5	$V_{CC}-1.475$	V
		CD (Disable)		−0.5	0.8	V
ECL Compatible Output Pins (ROUT±,RCLK ±,RSER±,TOUT±,TCLK±)						
V_{OHE}	ECL Output HIGH Voltage		Commercial	$V_{CC}-1.03$	$V_{CC}-0.83$	V
			Industrial[4]	$V_{CC}-1.08$	$V_{CC}-0.83$	
V_{OLE}	ECL Output LOW Voltage		T > 0°C	$V_{CC}-1.86$	$V_{CC}-1.62$	V
V_{ODIFF}	Output Differential Voltage			0.6		V
Three-Level Input Pins (MODE)						
V_{IHH}	Three-Level Input HIGH			$V_{CC}-0.75$	V_{CC}	V
V_{IMM}	Three-Level Input MID			$V_{CC}/2-0.5$	$V_{CC}/2+0.5$	V
V_{ILL}	Three-Level Input LOW			0.0	0.75	V
Operating Current[5]						
I_{CCS}	Static Operating Current				30	mA
I_{CCR}	Receiver Operating Current				50	mA
I_{CCT}	Transmitter Operating Current				13	mA
I_{CCE}	ECL Pair Operating Current				7.0	mA
I_{CC5}	Additional Current at 51.84 MHz				7.0	mA
I_{CCO}	Additional Current $\overline{LFI}$=LOW				3	mA

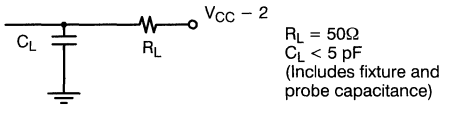
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 5.0V$	10	pF

AC Test Loads and Waveforms

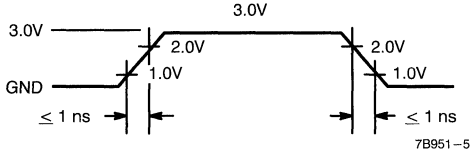


(a) TTL AC Test Load[7]



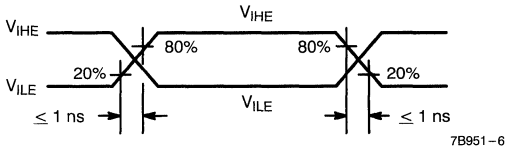
(b) ECL AC Test Load[7]

7B951–7



7B951–5

(c) TTL Input Test Waveform



7B951–6

(d) ECL Input Test Waveform

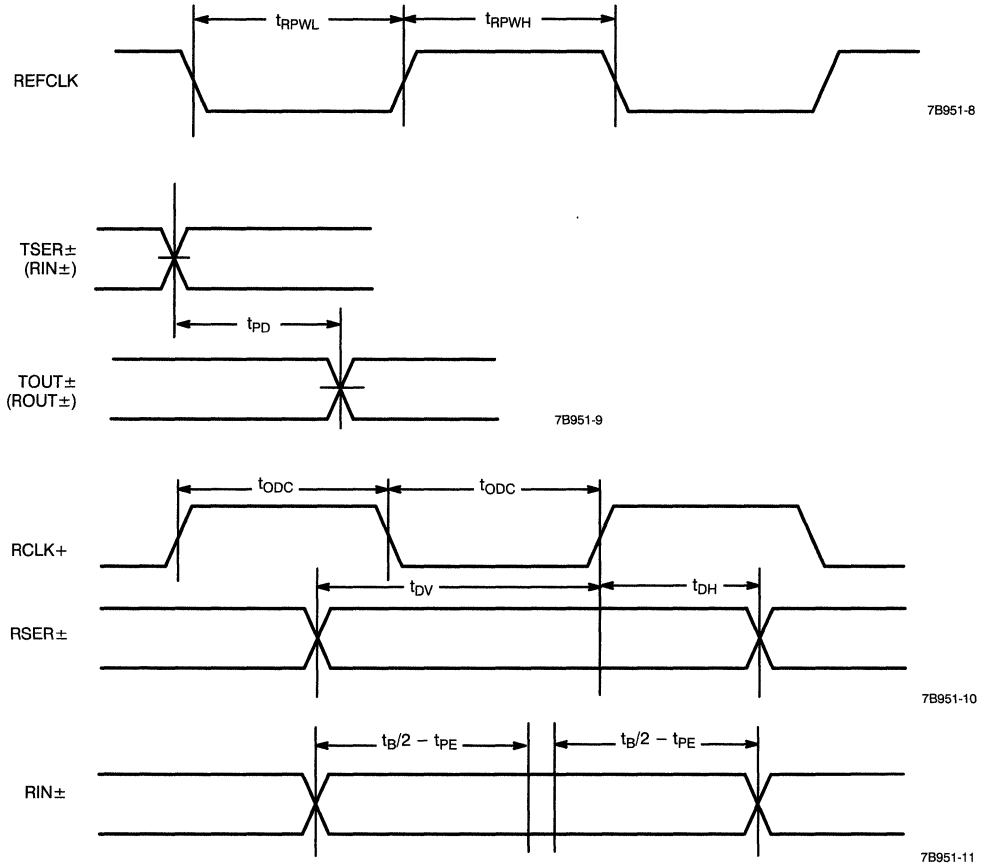
Switching Characteristics Over the Operating Range

Parameter	Description		Min.	Max.	Unit
f_{REF}	Reference Frequency	MODE=LOW	6.41	6.55	MHz
		MODE=HIGH	19.24	19.64	MHz
f_B	Bit Time[8]	MODE=LOW	19.5	19.1	ns
		MODE=HIGH	6.50	6.40	ns
t_{PE}	Receiver Static Phase Error[6]	MODE=LOW		100	ps
		MODE=HIGH		200	ps
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±)[6]		48	52	%
t_{RF}	Output Rise/Fall Time[6]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%)[9			100	µs
t_{RPWH}	REFCLK Pulse Width HIGH		10		ns
t_{RPWL}	REFCLK Pulse Width LOW		10		ns
t_{DV}	Data Valid		3		ns
t_{DH}	Data Hold		1		ns
t_{PD}	Propagation Delay (RIN to ROUT, TSER to TOUT)[10]			10	ns

Notes:

2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Input currents are always positive at all voltages above $V_{CC}/2$.
4. Specified only for temperatures below 0°C.
5. Total Receiver operating current (assuming that the Transmitter is not activated) can be found by adding $I_{CCS} + I_{CCR} + x * I_{CCE}$; where x is 2 if the ROUT± outputs are not activated and 3 if they are activated.
   Total Transmitter operating current (assuming that the Receiver is not activated) can be found by adding $I_{CCS} + I_{CCT} + x * I_{CCE}$; where x is 1 if the TOUT± outputs are not activated and 2 if they are activated.
   Total device power (assuming that the Transmitter and the Receiver are activated) can be found by adding $I_{CCS} + I_{CCR} + I_{CCT} + x * I_{CCE}$; where x represents the number of ECL output pairs activated.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
8. f_B is calculated as $1/(f_{REF}X8)$.
9. t_{LOCK} is the time needed for transitioning from lock to REFCLK X8 to lock to data.
10. The ECL switching threshold is the differential zero crossing (i.e., the place where + and − signals cross).

Switching Waveforms for the CY7B951 SONET/SDH Serial Transceiver



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B951–SC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY7B951–SI	S13	24-Lead (300-Mil) Molded SOIC	Industrial

Document #: 38–00358–D

SST™ SONET/SDH Serial Transceiver

Features

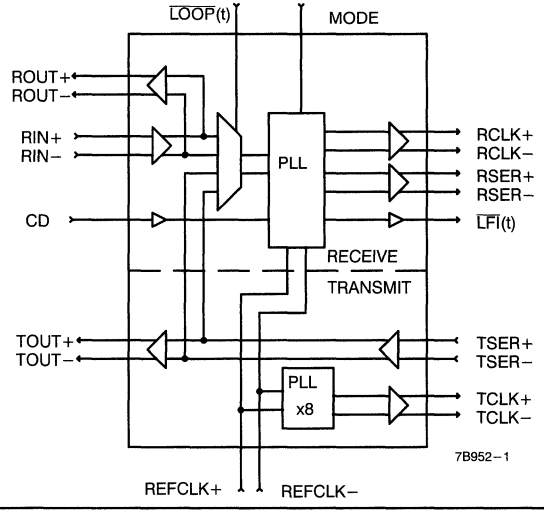
- Fully compliant with Bellcore and CCITT (ITU) specifications on:
  - Jitter Generation (<0.01 UI)
  - Jitter Transfer (<130 kHz)
  - Jitter Tolerance
- SONET/SDH and ATM Compliant
- Compatible with PMC-Sierra PM5343
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- 100K ECL compatible I/O
- No output clock "drift" without data transitions
- Link Status Indication
- Loop-back testing
- Single +5V supply
- 24-pin SOIC
- Compatible with fiber-optic modules, coaxial cable, and twisted pair media
- No external PLL components
- Power-down options to minimize power or crosstalk
- Low operating current: <65 mA
- 0.8μ BiCMOS

Functional Description

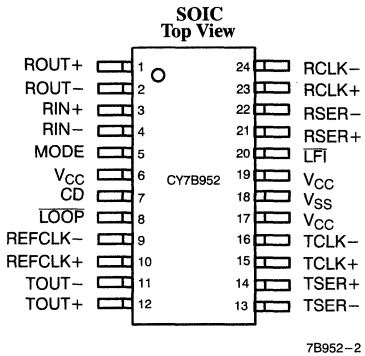
The SONET/SDH Serial Transceiver (SST) is used in Wide Area Network (WAN) SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

3

Logic Block Diagram



Pin Configuration



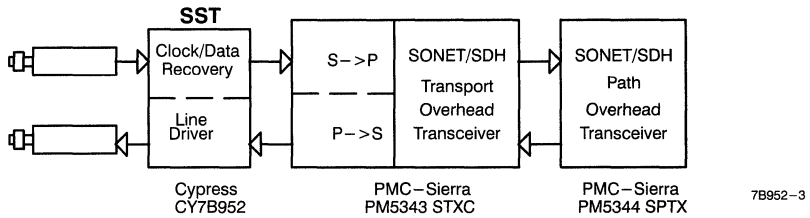


Figure 1. SONET/SDH Overhead Processing Application

SST is a trademark of Cypress Semiconductor Corporation
SUNI is a trademark of PMC-Sierra, Incorporated

Pin Descriptions

Name	I/O	Description
RIN±	Differential In	Receive Input. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedd clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN− to V_{SS}.
ROUT±	ECL Out	Receive Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data dependent jitter. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
RSER±	ECL Out	Recovered Serial Data. These ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	Recovered Clock. These ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK×8 frequency. Also, the Link Fault Indicator ($\overline{LFI}$) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
$\overline{LFI}$	TTL Out	Link Fault Indicator. This output indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the $\overline{LFI}$ output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the $\overline{LFI}$ output will be LOW. If CD is at a TTL LOW then the $\overline{LFI}$ output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	Transmit Serial Data. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the $\overline{LOOP}$ pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect TSER+ to V_{CC} and TSER− to V_{SS}.
TOUT±	ECL Out	Transmit Output. These ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.
REFCLK±	Diff/TTL In	Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK− is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	Transmit Clock. These ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
$\overline{LOOP}$	TTL In	Loop Back Select. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the $\overline{LOOP}$ input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When $\overline{LOOP}$ is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

Pin Descriptions (continued)

Name	I/O	Description
MODE	3-Level In	Frequency Mode Select. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS−3 (STM−1) line rate of 155.52 MHz. When this input is held LOW the two PLLs operate at the SONET STS−1 line rate of 51.84 MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE input is left floating or held at $V_{CC}/2$ the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
V_{CC}		Power.
V_{SS}		Ground.

Description

The CY7B952 Serial SONET/SDH Transceiver (SST) is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system. This device is fully compliant with all relevant SONET/SDH specifications including Bellcore TR−NWT−00253, ANSI T1X1.6/91−022, and CCITT G958.

Operating Frequency

The SST operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. The MODE input has three different functional selections. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test mode.

Transmit Functions

The transmit section of the SST contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK×8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The SST Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK− are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK− or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SST yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the receiver is to recover clock (RCLK±) and data (RSER±) from the incoming differential PECL data stream (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2.5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK×8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin as explained earlier. To insure accurate data and clock recovery, REFCLK×8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK×8 frequency accuracy be within 20−100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

The Receive PLL is fully compliant with the Bellcore jitter generation, jitter transfer, and jitter tolerance specifications.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW (≤2.5V Max.), the $\overline{\text{LFI}}$ output will transition LOW and the Receiver PLL will align itself with the REFCLK×8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the SST has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive me-

dia coupling. The SST will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, $\overline{LFI}$ will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{LFI}$ will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW (≤0.8V). When CD is pulled to a TTL LOW the $\overline{LFI}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLK×8 frequency. $\overline{LFI}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loop Back Testing

The TTL level $\overline{LOOP}$ pin is used to perform loop-back testing. When $\overline{LOOP}$ is asserted (held LOW) the Transmitter serial input (TSER±) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{LOOP}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{LOOP}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{LOOP}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator ($\overline{LFI}$) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

The SST can provide clock and data recovery as well as output buffering for physical layer protocol engines such as those used in WAN SONET/SDH and ATM applications. The operating frequency of the 7B952 is centered around the SONET/SDH STS−1 rate of 51.84 MHz and the SONET/SDH STS−3/STM−1 rate of 155.52 MHz. This device can also be used in data mover, Local Area Network (LAN) applications that operate at these frequencies.

In an ATM system, the SST is used to recover clock and data from an input SONET/SDH serial data stream for subsequent chips to do serial to parallel conversion, SONET/SDH overhead processing, ATM cell processing, and switching. On the Transmit side, ATM cells coming out of a switching matrix goes through ATM cell processing, SONET/SDH overhead processing and parallel to serial conversion before passing to the SST which buffers the data stream and drive the transmission media.

In a more generic telecommunications system (*Figure 1)*, the SST is used to provide clock and data recovery for a pure SONET/SDH system such as a SONET/SDH switch. The SST provides the recovered clock and data to a serial to parallel converter and SONET/SDH Transport Overhead Processor such as the PMC−Sierra PM5343 STXC. The parallel data is then passed to a SONET/SDH Path Overhead Processor such as the PMC−Sierra PM5344 SPTX.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL Outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Notes:

1. T_A is the "instant on" case temperature.

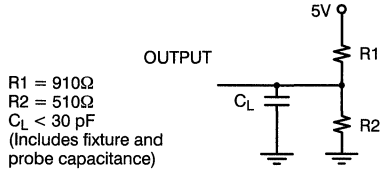
Electrical Characteristics Over the Operating Range

Parameter	Description		Test Condition	Min.	Max.	Unit
TTL Compatible Input Pins (LOOP, REFCLK+, REFCLK−)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			−0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK	$V_{IN}=V_{CC}$	+0.5	+200	µA
		LOOP	$V_{IN}=V_{CC}$	−10	+10	µA
I_{ILT}	Input LOW Current	REFCLK	$V_{IN}=0.0V$	−50	+50	µA
		LOOP	$V_{IN}=0.0V$	−500		µA
TTL Compatible Output Pins ($\overline{LFI}$)						
V_{OHT}	Output HIGH Voltage		$I_{OH}=-2$ mA	2.4		V
V_{OLT}	Output LOW Voltage		$I_{OL}=4$ mA		0.45	V
I_{OST}	Output Short Circuit Current		$V_{OUT}=0V$[2]	−15	−90	mA
ECL Compatible Input Pins (REFCLK±, CD, TSER±, RIN±)						
I_{IHE}	ECL Input HIGH Current	REFCLK/CD	$V_{IN}=V_{IHE(MAX)}$		+250	µA
		TSER/RIN	$V_{IN}=V_{IHE(MAX)}$		+750	µA
I_{ILE}[3]	ECL Input LOW Current	REFCLK/CD	$V_{IN}=V_{ILE(MIN)}$	+0.5		µA
		TSER/RIN	$V_{IN}=V_{ILE(MIN)}$	−200		µA
V_{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V_{IHE}	Input High Voltage	TSER/RIN			V_{CC}	V
		REFCLK		3.0	V_{CC}	V
		CD		$V_{CC}-1.165$	V_{CC}	V
V_{ILE}	Input LOW Voltage	TSER/RIN		2.0		V
		REFCLK		2.5		V
		CD (ECL)		2.5	$V_{CC}-1.475$	V
		CD (Disable)		−0.5	0.8	V
ECL Compatible Output Pins (ROUT±, RCLK±, RSER±, TOUT±, TCLK±)						
V_{OHE}	ECL Output HIGH Voltage		Commercial	$V_{CC}-1.03$	$V_{CC}-0.83$	V
			Industrial[4]	$V_{CC}-1.08$	$V_{CC}-0.83$	
V_{OLE}	ECL Output LOW Voltage		T > 0°C	$V_{CC}-1.86$	$V_{CC}-1.62$	V
V_{ODIFF}	Output Differential Voltage			0.6		V
Three-Level Input Pins (MODE)						
V_{IHH}	Three-Level Input HIGH			$V_{CC}-0.75$	V_{CC}	V
V_{IMM}	Three-Level Input MID			$V_{CC}/2-0.5$	$V_{CC}/2+0.5$	V
V_{ILL}	Three-Level Input LOW			0.0	0.75	V
Operating Current[5]						
I_{CCS}	Static Operating Current				30	mA
I_{CCR}	Receiver Operating Current				50	mA
I_{CCT}	Transmitter Operating Current				13	mA
I_{CCE}	ECL Pair Operating Current				7.0	mA
I_{CC5}	Additional Current at 51.84 MHz				7.0	mA
I_{CCO}	Additional Current $\overline{LFI}$=LOW				3	mA

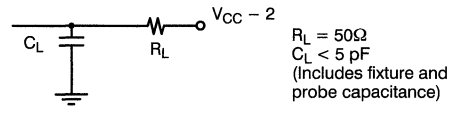
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 5.0V$	10	pF

AC Test Loads and Waveforms

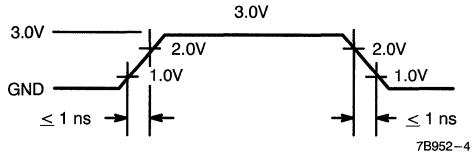


(a) TTL AC Test Load[7]



(b) ECL AC Test Load[7]

7B952–6



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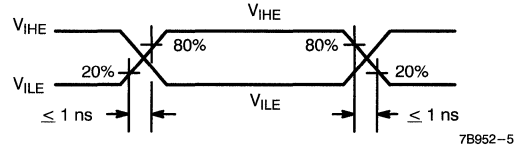
(c) TTL Input Test Waveform



7B952–5

(d) ECL Input Test Waveform

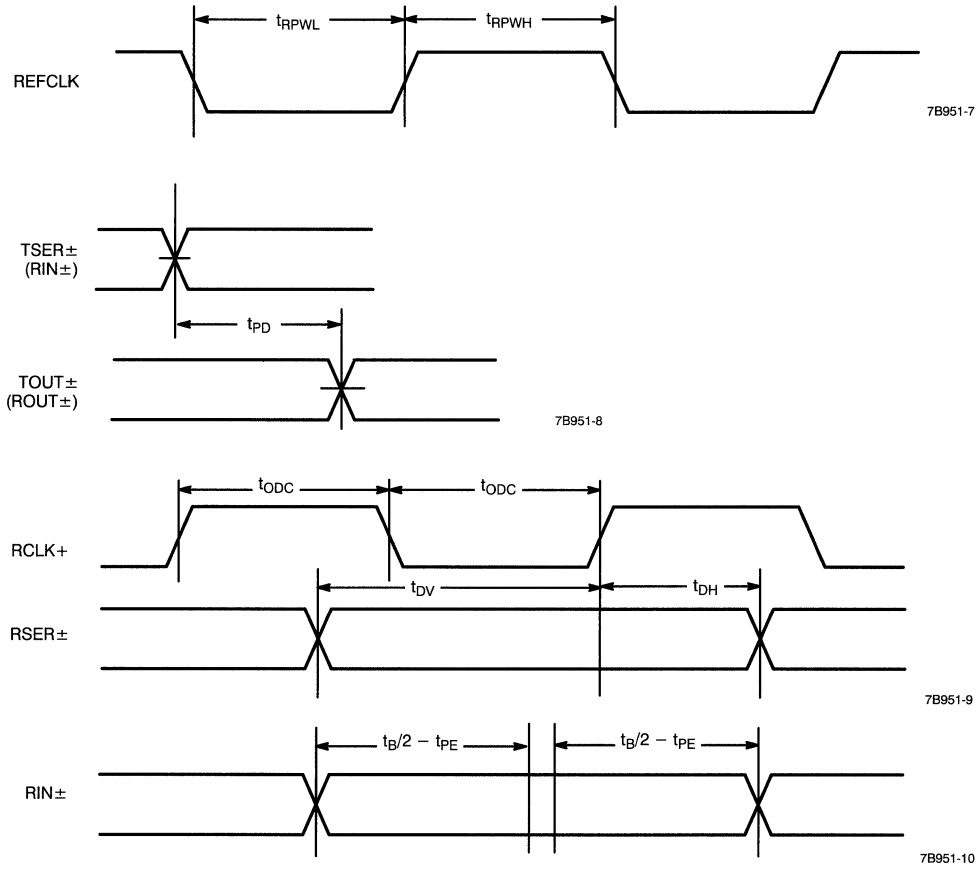
Switching Characteristics Over the Operating Range

Parameter	Description		Min.	Max.	Unit
f_{REF}	Reference Frequency	MODE=LOW	6.41	6.55	MHz
		MODE=HIGH	19.24	19.64	MHz
f_B	Bit Time[8]	MODE=LOW	19.5	19.1	ns
		MODE=HIGH	6.50	6.40	ns
t_{PE}	Receiver Static Phase Error[6]	MODE=LOW		100	ps
		MODE=HIGH		200	ps
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±)[6]		48	52	%
t_{RF}	Output Rise/Fall Time[6]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%)			0.5	ms
t_{RPWH}	REFCLK Pulse Width HIGH		10		ns
t_{RPWL}	REFCLK Pulse Width LOW		10		ns
t_{DV}	Data Valid		3		ns
t_{DH}	Data Hold		1		ns
t_{PD}	Propagation Delay (RIN to ROUT, TSER to TOUT)[9]			10	ns
Jitter Generation	Jitter Generation of RX PLL			0.01	UIrms
f_{-3dB}	–3 dB Gain Bandwidth of RX PLL (Jitter Transfer Bandwidth)	@ 155 MHz		130	kHz
		@ 52 MHz		45	kHz
Gpeak	Maximum Peaking of RX PLL			0.1	dB

Notes:

2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Input currents are always positive at all voltages above $V_{CC}/2$.
4. Specified only for temperatures below 0°C.
5. Total Receiver operating current (assuming that the Transmitter is not activated) can be found by adding $I_{CCS} + I_{CCR} + x * I_{CCE}$; where x is 2 if the ROUT± outputs are not activated and 3 if they are activated. Total Transmitter operating current (assuming that the Receiver is not activated) can be found by adding $I_{CCS} + I_{CCT} + x * I_{CCE}$; where x is 1 if the TOUT± outputs are not activated and 2 if they are activated. Total device power (assuming that the Transmitter and the Receiver are activated) can be found by adding $I_{CCS} + I_{CCR} + I_{CCT} + x * I_{CCE}$; where x represents the number of ECL output pairs activated.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
8. f_B is calculated a $1/(f_{REF \times 8})$.
9. The ECL switching threshold is the differential zero crossing (i.e., the place where + and – signals cross).

Switching Waveforms for the CY7B952 SONET/SDH Serial Transceiver



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B952–SC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY7B952–SI	S13	24-Lead (300-Mil) Molded SOIC	Industrial

Document #: 38–00502

This is an abbreviated version of this data-sheet. For the complete version, please contact your Cypress Marketing Representative.

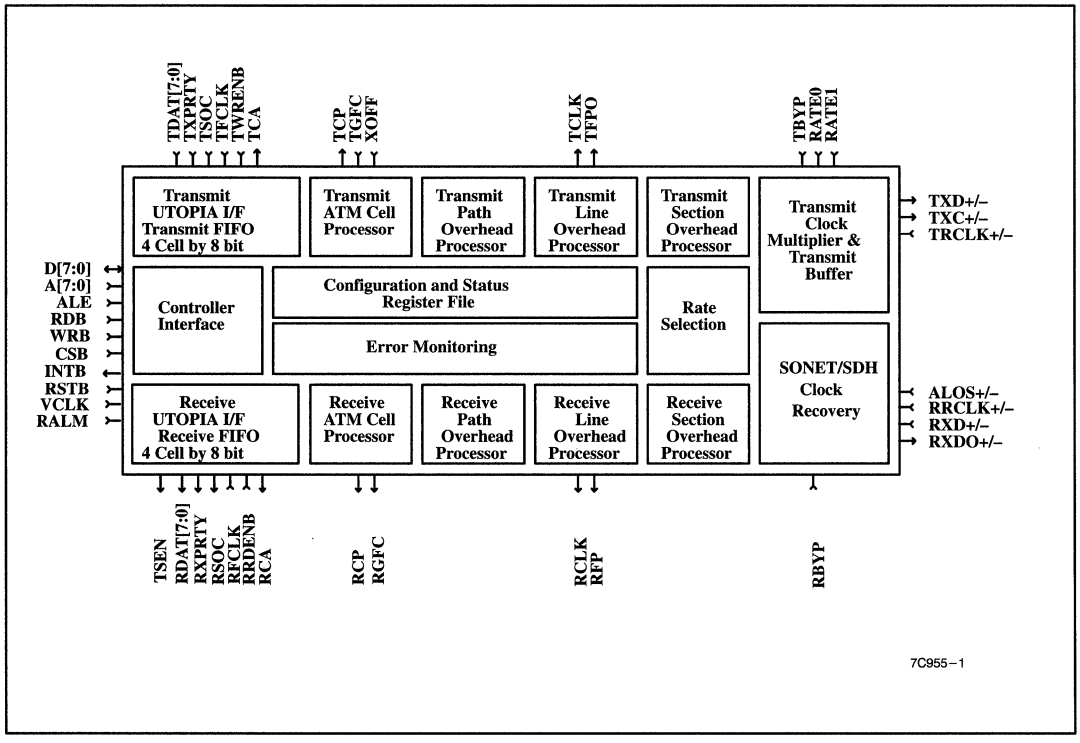
ADVANCED INFORMATION

CY7C955

ATM-SONET/SDH Transceiver

Features

- WAN and LAN ATM physical layer device
- Provides complete physical layer transport of ATM cells at
  - —STS-3c/ STM-1 rate of 155.52MHz
  - —STS−1 rate of 51.84MHz
- Compliant with ATM Forum User Network Interface 3.1 specification
- UTOPIA ATM interface
- ATM cell processing including
  - —HEC generation/verification
  - —Cell scrambling/descrambling
  - —Rate adaption/idle cell filtering
  - —Local Flow Control
  - —Cell alignment
- SONET frame processing including
  - —Compliant with, Bellcore GR−253, TI.105 I.432, and G.709
  - —Frame generation/recovery
  - —SONET scrambling/descrambling
  - —Frequency justification/pointer processing
- Complete line interface
  - —Clock and data recovery
  - —Transmit timing derived from receiver or byte−rate source
  - —No external PLL components
  - —SONET compliant PLL
  - —100K ECL compatible I/O
- Alarm indications including
  - —Loss Of Signal
  - —Out Of Frame, Loss Of Frame
  - —Line Far End Receive Failure
  - —Line Alarm Indication Signal
  - —B1 Parity Error
  - —Loss Of Cell Alignment
  - —Loss Of Receive Data
- Controller interface for internal interrupt and configuration registers
  - —Error monitoring
  - —Status indication
  - —Device configuration
- 0.65μ low-power CMOS



Document #: 38−00417

Interfacing with the SST™

This application note describes how to interface the CY7B951 SONET/SDH Serial Transceiver (SST™) with other physical-layer devices. The SST performs clock and data recovery from a SONET/SDH (Synchronous Optical NETwork/Synchronous Digital Hierarchy) 51.84 Mb/s or 155.52 Mb/s interface and can be used in a variety of SONET and ATM applications. The application note will begin with a brief introduction to the SST. Next, interface examples will be given that illustrate how to connect the SST to three different ATM controller devices; the first from PMC-Sierra called the PM5345 SUNI, the second, also from PMC-Sierra, called the S/UNI-LITE, and the third from Integrated Telecom Technologies (IgT) called the WAC-013.

Introduction

The CY7B951 SST is used in SONET/SDH applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit Clock, from a byte-rate source through the use of a frequency multiplier Phase-Locked Loop (PLL), and differential data buffering for the Transmit side of the system (see *Figure 1*). The pinout is shown in *Figure 2.*

Operating Frequency

The SST operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. When MODE is connected to V_{CC}, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the transmit PLL will multiply this rate by 8 to provide an output clock that operates at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the

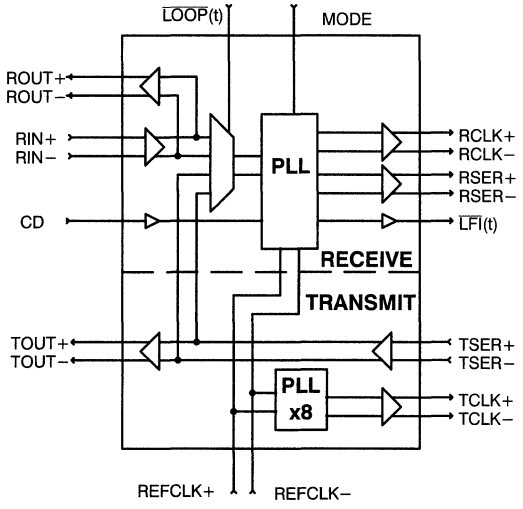


Figure 1. SST Block Diagram

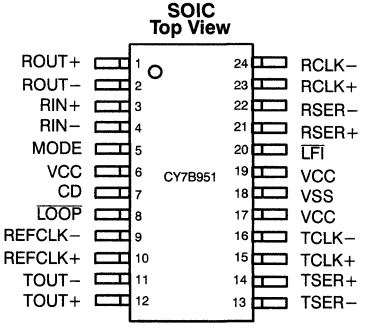


Figure 2. SST Pinout

device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the transmit PLL will multiply this rate by 8 to provide an output clock that operates at 51.84 MHz ±1%. In addition, when the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test Mode.

Transmit Functions

The Transmit section of the SST contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK*8) to produce a PECL (Pseudo ECL or Positive ECL) differential output clock (TCLK±). The Transmitter has two operating ranges that are selectable with the three-level MODE pin, as explained above. The SST Transmit frequency multiplier PLL allows low-cost byte-rate clock sources to be used to time the upstream serial data transmitter.

The REFCLK± inputs can be configured in three different ways. When both REFCLK+ and REFCLK− are connected to a differential 100K compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK− or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SST yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical fiber drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the Receiver is to generate recovered clock (RCLK±) and data (RSER±) signals from the incoming differential PECL data stream (RIN±). These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2−5V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media (such as coaxial cable or twisted pair).

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK*8) and is used as a bit-rate reference in comparison to the recovered clock to improve PLL lock time, and to provide a center frequency for operation in the absence of input data stream transitions. The Receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin, as explained earlier. To ensure accurate data and clock recovery, REFCLK*8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK*8 frequency accuracy be within 20−100 ppm.

The differential input serial data (RIN±) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT±. This output pair can be used as part of the transmission line interface circuit for base-line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the Receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect (CD) input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper-based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL-compatible signal that should be held HIGH when the incoming data

stream is valid. When CD is pulled to a PECL LOW, the $\overline{LFI}$ output will transition LOW, the Receiver PLL will align itself with the REFCLK*8 frequency, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data stream inputs (RIN).

In addition, the SST has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transitions can be caused by a break in the transmission media, a problem at the transmitter end of the media, or a problem with the transmit or receive media coupling hardware. The SST will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, $\overline{LFI}$ will transition LOW. The Receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK*8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. $\overline{LFI}$ will be driven HIGH again and the Receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW ($\leq$0.8V). When CD is pulled to a TTL LOW, the $\overline{LFI}$ will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLK*8 frequency. $\overline{LFI}$ LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When $\overline{LFI}$ is left unconnected, an internal pull-down resistor will pull this input to ground.

Loop Back Testing

The TTL level $\overline{LOOP}$ pin is used to perform loopback testing. When $\overline{LOOP}$ is asserted (held LOW) the Transmitter serial inputs (TSER±) are used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{LOOP}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{LOOP}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{LOOP}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

Power-Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC} the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the ($\overline{LFI}$ will still reflect the state of the CD input. This feature can be used for aggressive power management.

Interfacing with the PM5345 (SUNI)

The PM5345 is used in ATM applications for SONET frame processing, ATM cell processing, and error monitoring. The PMC-Sierra SUNI device requires Receive serial data aligned with a bit-rate clock. These signals need to be supplied through the RXD± and RXC± inputs respectively. A 155.52-MHz PECL Transmit clock (TXC±) is required to provide PM5345 transmit side clocking. For copper-based systems, the TXD± outputs must be buffered in order to drive transmission lines with low impedances. Lastly, a LOS detection is required from the clock and data recovery engine to

aid in the determination of the LOS, LOF, and OOF error conditions reported by the SUNI device. This signal is brought in through the SUNI GPIN (General Purpose Input). Before the introduction of the SST, clock and data recovery devices were interfaced to the PMC-SUNI as shown in *Figure 3.*

Figure 4 shows the SST signal connections with the PMC-Sierra PM5345 SUNI. The SST, together with the PM5345, provides a complete Physical layer interface. The Receive section of the SST provides serial SONET/SDH data at 155.52 Mb/s to the receive section of the PM5345 (RXC± and RXD±). The Transmit section of the SST provides the transmit side 155.52-MHz clock that is used by the PM5345 TXCI± input by multiplying a 19.44-MHz oscillator by eight. This function eliminates the need for an expensive 155.52-MHz oscillator to be used in the system. The SST buffers the TXD± output signals from the SUNI device for driving copper-based systems or for improved operation in fiber-based systems.

The $\overline{\text{LFI}}$ output is used to drive the GPIN input. This $\overline{\text{LFI}}$ output will transition LOW when any of the following occur: the CD (Carrier Detect) input transitions LOW, the frequency of the incoming data is outside of the lock range of the Receive PLL,

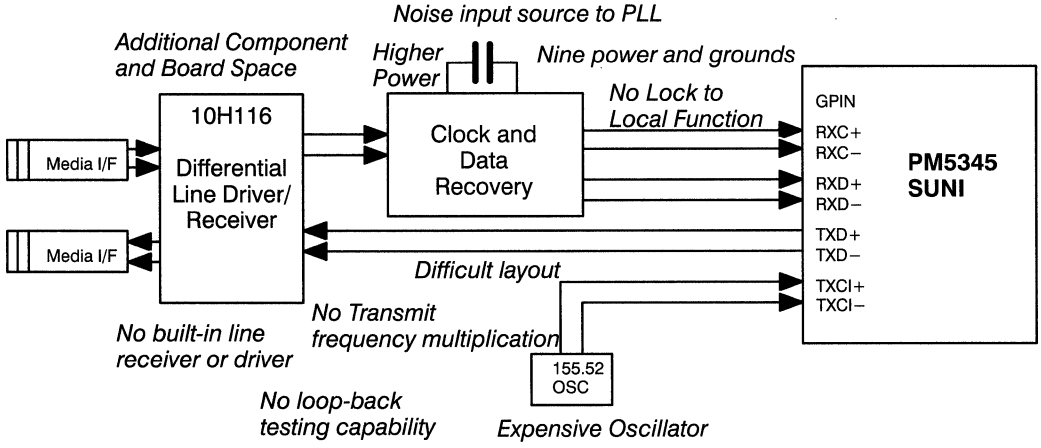


Figure 3. Typical SUNI interface without the Use of the SST

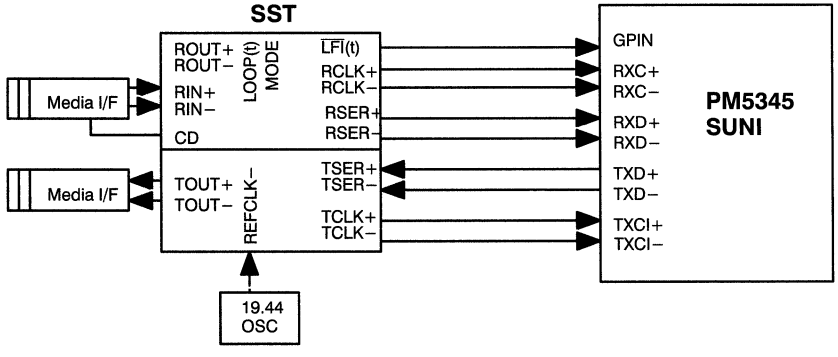


Figure 4. SST to PMC-Sierra PM5345 SUNI Connection Diagram

or there have been no transitions in the incoming data stream for the last 512 bit times. Additionally, when the CD input is forced LOW by an output from a source such as the signal detect of an optical module or an external transition detection circuitry for copper-based systems, the SST will force the RSER± outputs LOW. This will aid the SUNI device in the determination of the LOS state and minimize the length of time needed to determine an error condition.

Figure 5 shows an electrical interface of the SST to the PMC-SUNI device. Each SST PECL output is AC coupled into the SUNI inputs with a .01-µF capacitor, and is loaded with an 80Ω pull-up resistor and a 130Ω pull-down resistor. This scheme allows the SUNI device to self-bias (since the SUNI has a bias circuit built into each PECL input) its inputs and also provides the SST outputs with 50Ω terminations to approximately V_{CC} – 2V. The termination resistors are bypassed with .01-µF capacitors to provide high-speed switching current. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 160Ω and a pull-down resistor of 260Ω. Terminations for the SST outputs (TCLK, RCLK, RSER) should be placed as close to the SUNI as possible.

The TXD± outputs require different termination resistors values. The ideal biasing voltage for TXD± is 4.2V. This bias is achieved by connecting a 62Ω pull up to TAVD and a 330Ω pull down to GND at the end of the termination line connecting

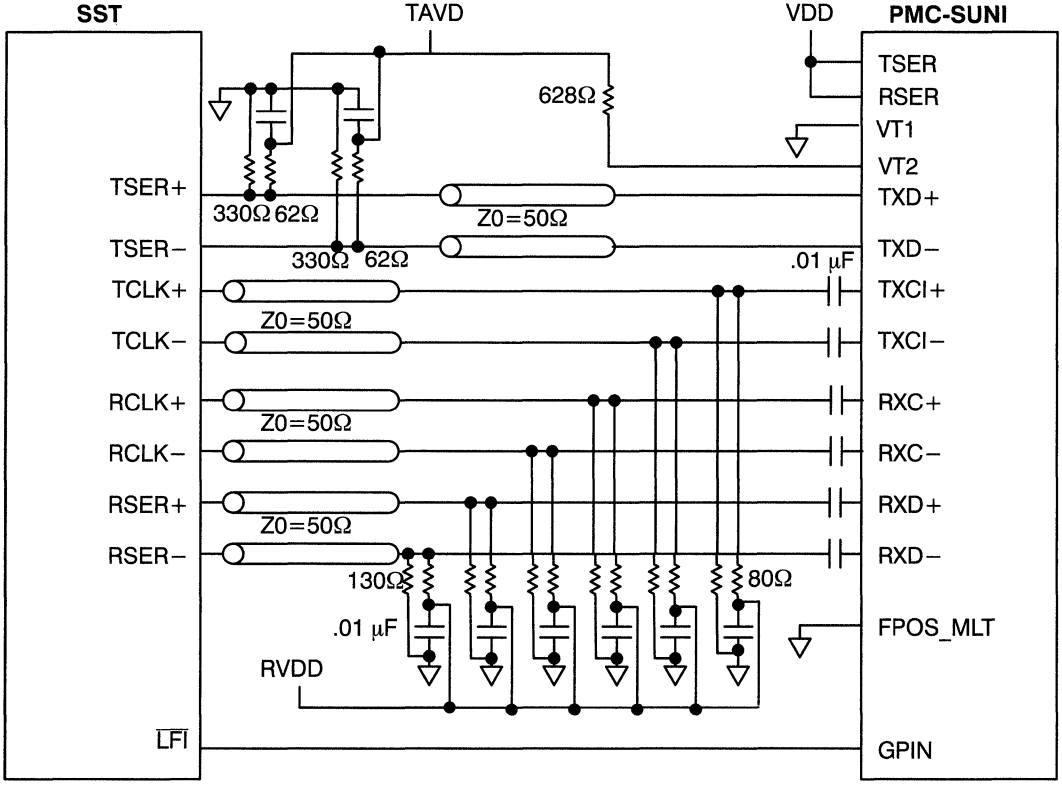


Figure 5. High Performance SST to PMC SUNI Interface

TXD± and TSER±. These resistor values are calculated based on $Z_0 = 50\Omega$. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 120Ω and a pull-down resistor of 636Ω. In addition, the VT2 resistor should also be scaled from 628Ω to 1260Ω when using 100Ω trace impedances. In general, $R_{VT2} = 12.564 * Z_0$.

Interfacing with the PM5346 (S/UNI-LITE)

The PM5346 is another PMC-Sierra product used in ATM systems for clock and data recovery, SONET frame processing, ATM cell processing, and error monitoring. Its small package size makes it more desirable than the PM5345 in cases where not all of the SONET frame processing functions of the PM5345 are needed. For performance reasons, the PLL of S/UNI-LITE can be bypassed and the SST can be used to perform clock and data recovery functions for the S/UNI-LITE.

Figure 6 shows how to interface the SST to the S/UNI-LITE. When RBYP is tied HIGH, the internal PLL of the S/UNI-LITE is disabled and RRCLK± is used to sample RXD±. In this configuration, the SST is used to supply the bit-aligned RRCLK. This is achieved by connecting RCLK± to RRCLK± and RSER± to RXD± using four equal-length traces. Each of these traces has an 80Ω pull-up to RVDD and a 130Ω pull-down to GND. These termination resistors are bypassed with .01-µF capacitors to satisfy the high-speed switching current

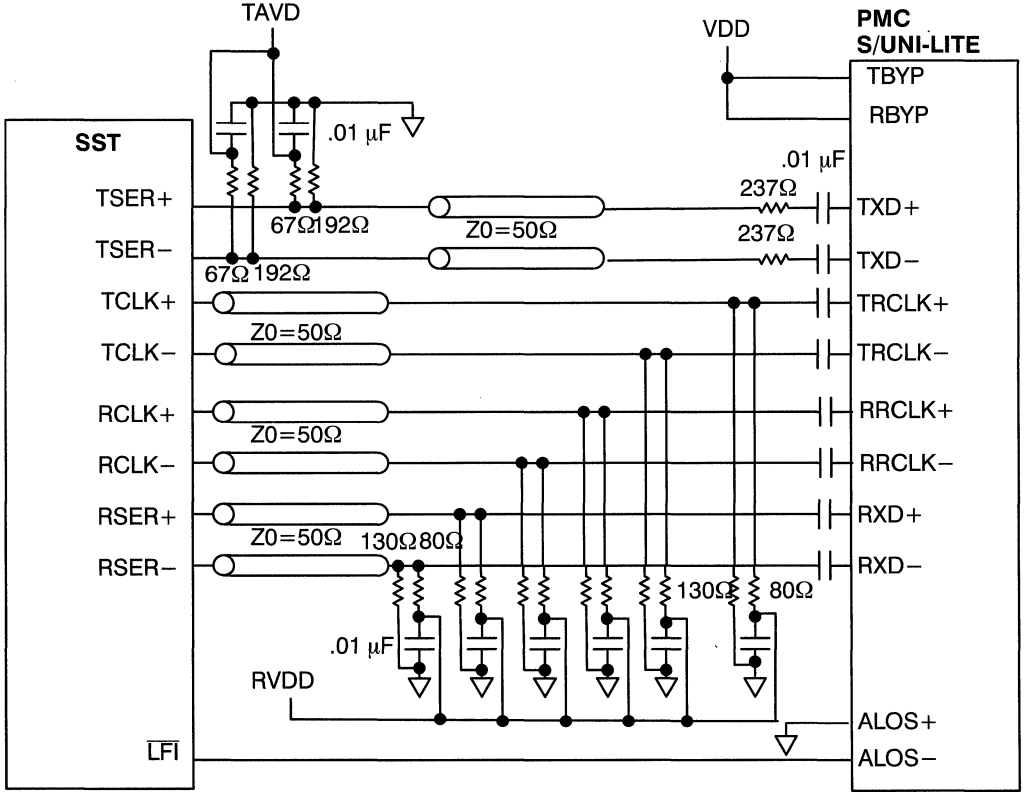


Figure 6. High Performance SST to PMC S/UNI-LITE Interface

requirements. A .01-μF DC-blocking capacitor is used in series with the transmission line to allow the S/UNI-LITE to self-bias its inputs (since the S/UNI-LITE, like the SUNI, also has bias circuits built into each PECL input). All these passive components are placed close to the S/UNI-LITE.

In the same way, the transmit side PLL of the S/UNI-LITE can also be disabled. When TBYP is tied HIGH, the clock multiplication function of the S/UNI-LITE is disabled and the 155.52-MHz or 51.84-MHz clock received from either RRCLK± or TRCLK± is used for clocking the transmit portion of the S/UNI-LITE. If the LOOPT bit of the Master Control register of the S/UNI-LITE is 1, RRCLK will be used and when the LOOPT bit is 0, TRCLK± will be used. TRCLK± is supplied by TCLK± of the SST. The termination/biasing circuit used for this TRCLK connection is the same as that used in the RXD± and RRCLK± connections described previously. These termination/biasing circuits should also be placed as close to the S/UNI-LITE as possible.

For the TXD± to TSER± connections, a 237Ω source resistor in series with a .01-μF capacitor placed closed to the S/UNI-LITE side is used with a 67Ω pull-up to TAVD and a 192Ω pull-down to GND placed close to the SST side to provide the necessary termination and biasing.

Interfacing with the IgT WAC-013.

The Integrated Telecom Technology (IgT) WAC-013 provides SONET frame processing, ATM cell processing, and error monitoring. The IgT device requires differential PECL Receive data (RS_SER_DATA) aligned with a differential PECL bit-rate clock (RS_SER_CLK). These signals represent the recovered clock and data from a SONET/SDH STS-3/STM-1 data stream of 155.52 Mb/s or a SONET STS-1 data stream of 51.84 Mb/s. The WAC-013 also requires a bit-rate transmit-clock (TS_SER_CLK) for Transmit Side clocking. The transmit data (TS_SER_DATA) should also be buffered for driving low-impedance transmission lines or copper transmission media. Prior to the introduction of the SST, clock and data recovery devices were connected to the WAC-013 as shown in *Figure 7.*

Figure 8 shows the SST signal connections with the IgT WAC-013. The SST, together with the WAC-013, provides a complete physical-layer interface. The Receive section of the SST provides serial SONET/SDH data at 155.52 Mb/s or 51.84 Mb/s (depending on the state of the SST MODE pin) to the Receive section of the IgT RS_SER_DATA and RS_SER_CLK inputs. The Transmit section of the SST provides the bit-rate clock (TS_SER_CLK) and Transmit buffering of the TS_SER_DATA outputs. The SST multiples a 19.44-MHz reference

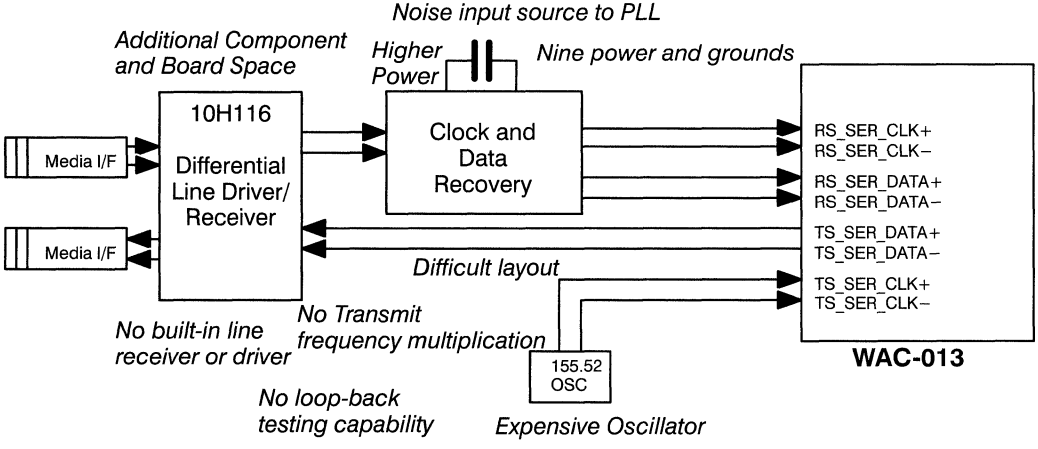


Figure 7. Typical WAC-013 interface without the Use of the SST

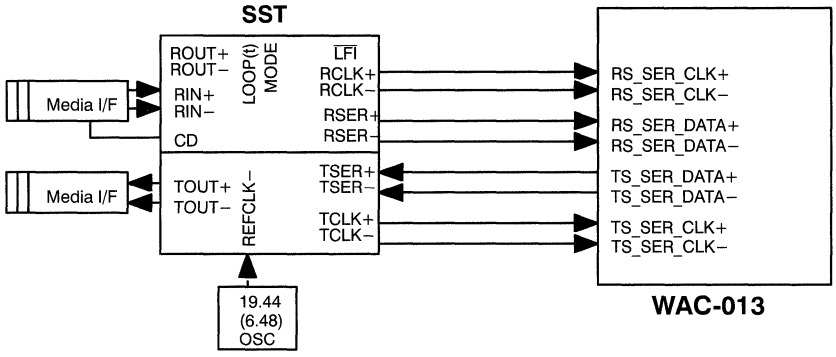


Figure 8. SST to IgT WAC-013 Connection Diagram

clock (6.48-MHz for STS-1 applications) by eight to produce the 155.52-MHz (51.84-MHz) transmit clock. This frequency multiplication function eliminates the need for an expensive 155.52-MHz crystal oscillator.

Figure 9 shows the electrical interface of the SST to the WAC-013. The outputs are loaded and terminated with 80Ω pull-up resistors and 130Ω pull-down resistors at the load. This provides a 50Ω termination to $V_{CC}-2V$. These resistors are also bypassed with a .01-µF capacitor to provide high-speed switching current. For PCB trace impedances higher than 50Ω, the terminating resistors should be scaled accordingly. For example, a 100Ω transmission line would require a pull-up resistor of 160Ω and a pull-down resistor of 260Ω.

Conclusion

The interface examples shown in this note demonstrate how to connect the SST to the PMC-Sierra PM5345 SUNI, the PMC-Sierra PM5346 S/UNI-LITE, and the IgT WAC-013. Together these devices provide a complete physical-layer solution for ATM applications over SONET/SDH at 155.52 Mb/s and 51.84 Mb/s. The SST greatly simplifies the physical-layer implementation with its ability to generate a Loss of Signal indication, its capability to lock to the local reference clock during error conditions, and its capacity to buffer the transmit data stream for driving low-impedance transmission lines. The SST also reduces the cost of physical-layer implementations by eliminating the need for a 155.52-MHz crystal oscillator with its ability to multiply a byte-rate clock to provide the bit-rate transmit source. Cypress's expertise in PLL-based clock and data recovery as well as the added features of the SST provide designers with the capacity to create simple, low cost, and robust ATM physical-layer designs.

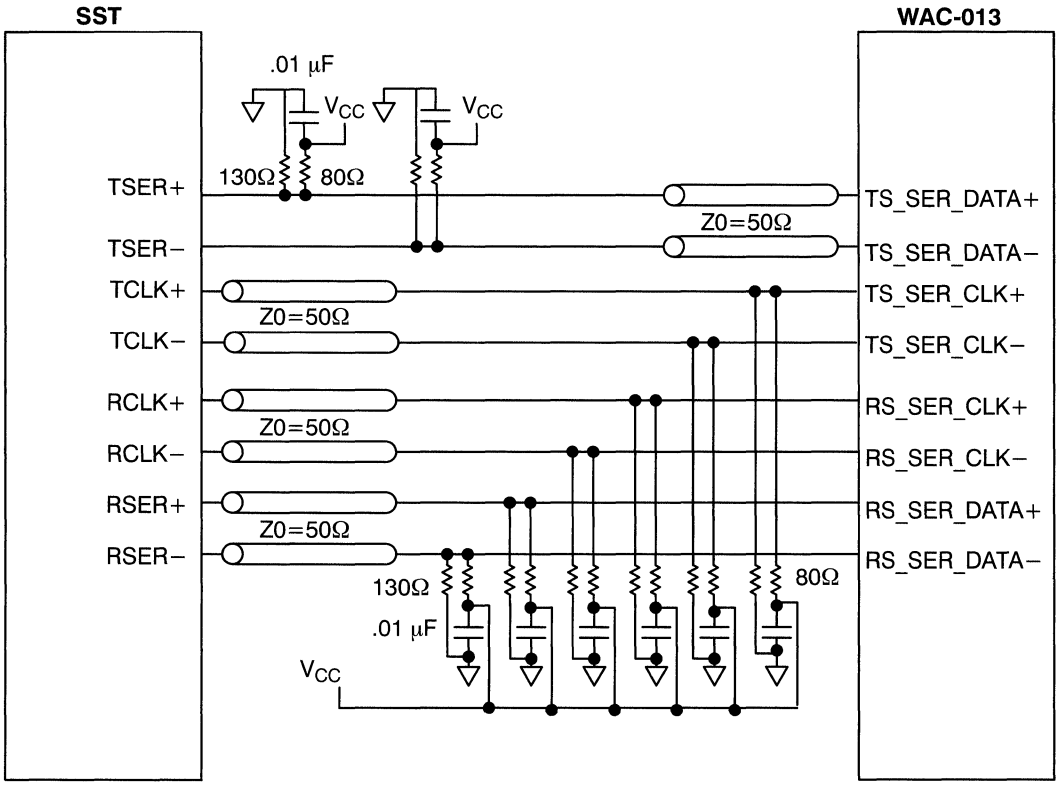


Figure 9. High Performance SST to WAC-013 Interface

SST is a trademark of Cypress Semiconductor Corporation.

High-Speed Serial/Fibre Channel/ESCON™ 4

4

Fibre Channel/ESCON™

CY7B923
CY7B933

HOTLink™ Transmitter/Receiver

Features

- **Fibre Channel compliant**
- **IBM ESCON® compliant**
- **ATM compliant**
- **8B/10B-coded or 10-bit unencoded**
- **160- to 330-Mbps data rate**
- **TTL synchronous I/O**
- **No external PLL components**
- **Triple PECL 100K serial outputs**
- **Dual PECL 100K serial inputs**
- **Low power: 350 mW (Tx), 650 mW (Rx)**
- **Compatible with fiber optic modules, coaxial cable, and twisted pair media**
- **Built-In Self-Test**
- **Single +5V supply**
- **28-pin SOIC/PLCC/LCC**
- **0.8μ BiCMOS**

Functional Description

The CY7B923 HOTLink™ Transmitter and CY7B933 HOTLink Receiver are point-to-point communications building blocks that transfer data over high-speed serial links (fiber, coax, and twisted pair) at 160 to 330 Mbits/second. *Figure 1* illustrates typical connections to host systems or controllers.

Eight bits of user data or protocol information are loaded into the HOTLink transmitter and are encoded. Serial data is shifted out of the three differential positive ECL (PECL) serial ports at the bit rate (which is 10 times the byte rate).

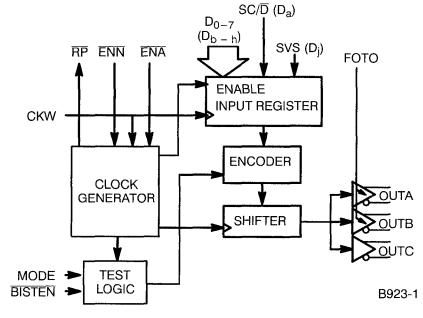
The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. The bit stream is deserialized, decoded, and checked for transmission errors. Recovered bytes are presented in parallel to the receiving host along with a byte rate clock.

The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. I/O signals are available to create a seamless interface with both asynchronous FIFOs (i.e., CY7C42X) and clocked FIFOs (i.e., CY7C44X). A Built-In Self-Test pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

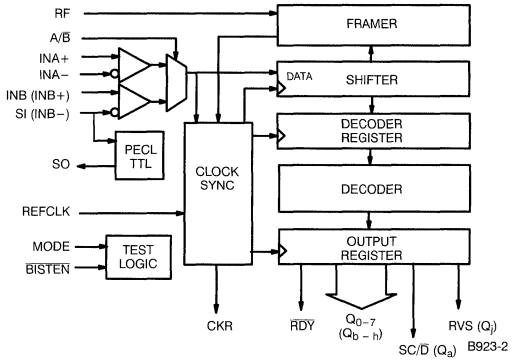
HOTLink devices are ideal for a variety of applications where a parallel interface can be replaced with a high-speed point-to-point serial link. Applications include interconnecting workstations, servers, mass storage, and video transmission equipment.

4

CY7B923 Transmitter Logic Block Diagram



CY7B933 Receiver Logic Block Diagram



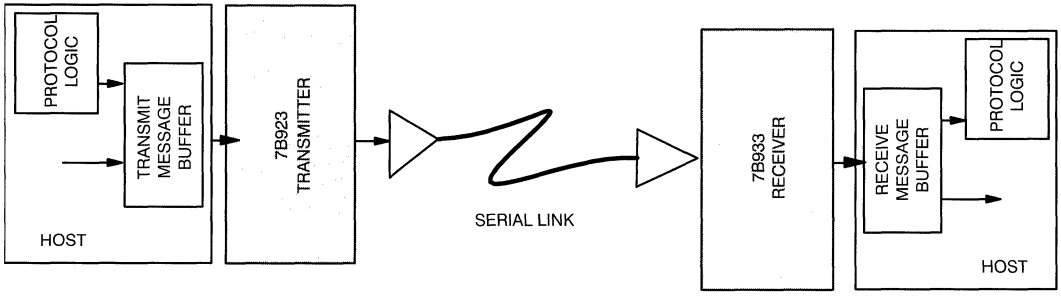
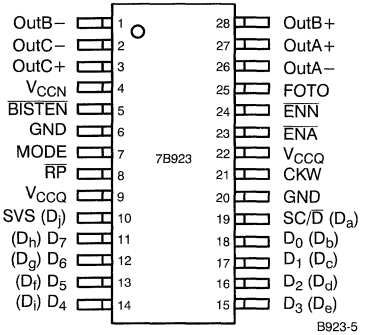


Figure 1. HOTLink System Connections

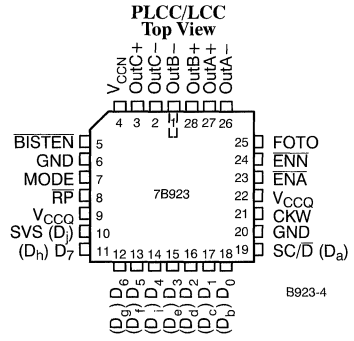
HOTLink is a trademark of Cypress Semiconductor Corporation.
ESCON is a registered trademark of IBM.

CY7B923 Transmitter Pin Configurations

SOIC
Top View

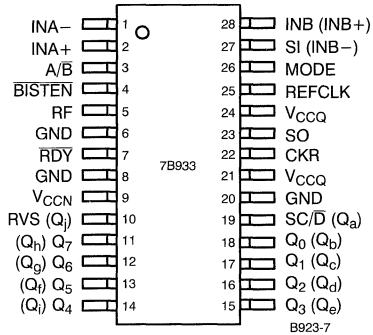


PLCC/LCC
Top View

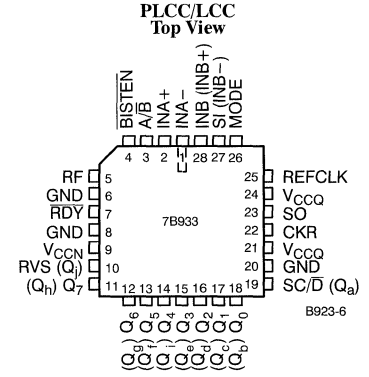


CY7B933 Receiver Pin Configurations

SOIC
Top View



PLCC/LCC
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into PECL outputs (HIGH) ..... −50 mA

Static Discharge Voltage ..... >4001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C Case Temperature	5V ± 10%

Pin Descriptions

CY7B923 HOTLink Transmitter

Name	I/O	Description
D_{0-7} (D_{b-h})	TTL In	Parallel Data Input. Data is clocked into the Transmitter on the rising edge of CKW if $\overline{ENA}$ is LOW (or on the next rising CKW with $\overline{ENN}$ LOW). If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, a Null character (K28.5) is sent. When MODE is HIGH, $D_{0,1,...7}$ become $D_{b,c,...h}$ respectively.
SC/$\overline{D}$ (D_a)	TTL In	Special Character/Data Select. A HIGH on SC/$\overline{D}$ when CKW rises causes the transmitter to encode the pattern on D_{0-7} as a control code (Special Character), while a LOW causes the data to be coded using the 8B/10B data alphabet. When MODE is HIGH, SC/$\overline{D}$ (D_a) acts as D_a input. SC/$\overline{D}$ has the same timing as D_{0-7}.
SVS (D_j)	TTL In	Send Violation Symbol. If SVS is HIGH when CKW rises, a Violation symbol is encoded and sent while the data on the parallel inputs is ignored. If SVS is LOW, the state of D_{0-7} and SC/$\overline{D}$ determines the code sent. In normal or test mode, this pin overrides the BIST generator and forces the transmission of a Violation code. When MODE is HIGH (placing the transmitter in unencoded mode), SVS (D_j) acts as the D_j input. SVS has the same timing as D_{0-7}.
$\overline{ENA}$	TTL In	Enable Parallel Data. If $\overline{ENA}$ is LOW on the rising edge of CKW, the data is loaded, encoded, and sent. If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the data inputs are ignored and the Transmitter will insert a Null character (K28.5) to fill the space between user data. $\overline{ENA}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte to be sent. If $\overline{ENA}$ is being used for data control, $\overline{ENN}$ will normally be strapped HIGH, but can be used for BIST function control.
$\overline{ENN}$	TTL In	Enable Next Parallel Data. If $\overline{ENN}$ is LOW, the data appearing on D_{0-7} at the next rising edge of CKW is loaded, encoded, and sent. If $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the data appearing on D_{0-7} at the next rising edge of CKW will be ignored and the Transmitter will insert a Null character to fill the space between user data. $\overline{ENN}$ may be held HIGH/LOW continuously or it may be pulsed with each data byte sent. If $\overline{ENN}$ is being used for data control, $\overline{ENA}$ will normally be strapped HIGH, but can be used for BIST function control.
CKW	TTL In	Clock Write. CKW is both the clock frequency reference for the multiplying PLL that generates the high-speed transmit clock, and the byte rate write signal that synchronizes the parallel data input. CKW must be connected to a crystal controlled time base that runs within the specified frequency range of the Transmitter and Receiver.
FOTO	TTL In	Fiber Optic Transmitter Off. FOTO determines the function of two of the three PECL transmitter output pairs. If FOTO is LOW, the data encoded by the Transmitter will appear at the outputs continuously. If FOTO is HIGH, OUTA± and OUTB± are forced to their "logic zero" state (OUT+ = LOW and OUT− = HIGH), causing a fiber optic transmit module to extinguish its light output. OUTC is unaffected by the level on FOTO, and can be used as a loop-back signal source for board-level diagnostic testing.
OUT A± OUT B± OUT C±	PECL Out	Differential Serial Data Outputs. These PECL 100K outputs (+5V referenced) are capable of driving terminated transmission lines or commercial fiber optic transmitter modules. Unused pairs of outputs can be wired to V_{CC} to reduce power if the output is not required. OUTA± and OUTB± are controlled by the level on FOTO, and will remain at their "logical zero" states when FOTO is asserted. OUTC± is unaffected by the level on FOTO. (OUTA+ and OUTB+ are used as a differential test clock input while in Test mode, i.e., MODE=UNCONNECTED or forced to $V_{CC}/2$.)
MODE	3-Level In	Encoder Mode Select. The level on MODE determines the encoding method to be used. When wired to GND, MODE selects 8B/10B encoding. When wired to V_{CC}, data inputs bypass the encoder and the bit pattern on D_{a-j} goes directly to the shifter. When left floating (internal resistors hold the input at $V_{CC}/2$) the internal bit-clock generator is disabled and OUTA+/OUTB+ become the differential bit clock to be used for factory test. In typical applications MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW and $\overline{ENA}$ and $\overline{ENN}$ are HIGH, the transmitter sends an alternating 1−0 pattern (D10.2 or D21.5). When either $\overline{ENA}$ or $\overline{ENN}$ is set LOW and $\overline{BISTEN}$ is LOW, the transmitter begins a repeating test sequence that allows the Transmitter and Receiver to work together to test the function of the entire link. In normal use this input is held HIGH or wired to V_{CC}. The BIST generator is a free-running pattern generator that need not be initialized, but if required, the BIST sequence can be initialized by momentarily asserting SVS while $\overline{BISTEN}$ is LOW. $\overline{BISTEN}$ has the same timing as D_{0-7}.
$\overline{RP}$	TTL Out	Read Pulse. $\overline{RP}$ is a 60% LOW duty-cycle byte-rate pulse train suitable for the read pulse in CY7C42X FIFOs. The frequency on $\overline{RP}$ is the same as CKW when enabled by $\overline{ENA}$, and duty cycle is independent of the CKW duty cycle. Pulse widths are set by logic internal to the transmitter. In BIST mode, $\overline{RP}$ will remain HIGH for all but the last byte of a test loop. $\overline{RP}$ will pulse LOW one byte time per BIST loop.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B933 HOTLink Receiver

Name	I/O	Description
Q_{0-7} (Q_{b-h})	TTL Out	Q_{0-7} Parallel Data Output. Q_{0-7} contain the most recently received data. These outputs change synchronously with CKR. When MODE is HIGH, $Q_{0,1,...7}$ become $Q_{b,c,...h}$ respectively.
SC/$\overline{D}$ (Q_a)	TTL Out	Special Character/Data Select. SC/$\overline{D}$ indicates the context of received data. HIGH indicates a Control (Special Character) code, LOW indicates a Data character. When MODE is HIGH (placing the receiver in Unencoded mode), SC/$\overline{D}$ acts as the Q_a output. SC/$\overline{D}$ has the same timing as Q_{0-7}.
RVS (Q_j)	TTL Out	Received Violation Symbol. A HIGH on RVS indicates that a code rule violation has been detected in the received data stream. A LOW shows that no error has been detected. In BIST mode, a LOW on RVS indicates correct operation of the Transmitter, Receiver, and link on a byte-by-byte basis. When MODE is HIGH (placing the receiver in Unedcoded mode), RVS acts as the Q_j output. RVS has the same timing as Q_{0-7}.
$\overline{RDY}$	TTL Out	Data Output Ready. A LOW pulse on $\overline{RDY}$ indicates that new data has been received and is ready to be delivered. A missing pulse on $\overline{RDY}$ shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In BIST mode $\overline{RDY}$ will remain LOW for all but the last byte of a test loop and will pulse HIGH one byte time per BIST loop.
CKR	TTL Out	Clock Read. This byte rate clock output is phase and frequency aligned to the incoming serial data stream. $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
A/$\overline{B}$	PECL in	Serial Data Input Select. This PECL 100K (+5V referenced) input selects INA or INB as the active data input. If A/$\overline{B}$ is HIGH, INA is connected to the shifter and signals connected to INA will be decoded. If A/$\overline{B}$ is LOW INB is selected.
INA±	Diff In	Serial Data Input A. The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of A/$\overline{B}$.
INB (INB+)	PECL in (Diff In)	Serial Data Input B. This pin is either a single-ended PECL data receiver (INB) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, INB becomes a single-ended PECL 100K (+5V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB−)	PECL in (Diff In)	Status Input. This pin is either a single-ended PECL status monitor input (SI) or half of the INB of the differential pair. If SO is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If SO is normally connected and loaded, SI becomes a single-ended PECL 100K (+5V referenced) status monitor input, which is translated into a TTL-level signal at the SO pin.
SO	TTL Out	Status Out. SO is the TTL-translated output of SI. It is typically used to translate the Carrier Detect output from a fiber-optic receiver connected to SI. When this pin is normally connected and loaded (without any external pull-up resistor), SO will assume the same logical level as SI and INB will become a single-ended PECL serial data input. If the status monitor translation is not desired, then SO may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
RF	TTL In	Reframe Enable. RF controls the Framer logic in the Receiver. When RF is held HIGH, each SYNC (K28.5) symbol detected in the shifter will frame the data that follows. If is HIGH for 2,048 consecutive bytes, the internal framer switches to double-byte mode. When RF is held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.
REFCLK	TTL In	Reference Clock. REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK must be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency must be the same as the transmitter CKW frequency (within CKW ±0.1%)
MODE	3-Level In	Decoder Mode Select. The level on the MODE pin determines the decoding method to be used. When wired to GND, MODE selects 8B/10B decoding. When wired to V_{CC}, registered shifter contents bypass the decoder and are sent to Q_{a-j} directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.
$\overline{BISTEN}$	TTL In	Built-In Self-Test Enable. When $\overline{BISTEN}$ is LOW the Receiver awaits a D0.0 (sent once per BIST loop) character and begins a continuous test sequence that tests the functionality of the Transmitter, the Receiver, and the link connecting them. In BIST mode the status of the test can be monitored with $\overline{RDY}$ and RVS outputs. In normal use $\overline{BISTEN}$ is held HIGH or wired to V_{CC}. $\overline{BISTEN}$ has the same timing as Q_{0-7}.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground.

CY7B923 HOTLink Transmitter Block Diagram Description

Input Register

The Input register holds the data to be processed by the HOTLink transmitter and allows the input timing to be made consistent with standard FIFOs. The Input register is clocked by CKW and loaded with information on the D_{0-7}, SC/$\overline{D}$, and SVS pins. Two enable inputs ($\overline{ENA}$ and $\overline{ENN}$) allow the user to choose when data is loaded in the register. Asserting $\overline{ENA}$ (Enable, active LOW) causes the inputs to be loaded in the register on the rising edge of CKW. If $\overline{ENN}$ (Enable Next, active LOW) is asserted when CKW rises, the data present on the inputs on the next rising edge of CKW will be loaded into the Input register. If neither $\overline{ENA}$ nor $\overline{ENN}$ are asserted LOW on the rising edge of CKW, then a SYNC (K28.5) character is sent. These two inputs allow proper timing and function for compatibility with either asynchronous FIFOs or clocked FIFOs without external logic, as shown in *Figure 5.*

In BIST mode, the Input register becomes the signature pattern generator by logically converting the parallel Input register into a Linear Feedback Shift Register (LFSR). When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Receiver.

Encoder

The Encoder transforms the input data held by the Input register into a form more suitable for transmission on a serial interface link. The code used is specified by ANSI X3.230 (Fibre Channel) and the IBM ESCON channel (code tables are at the end of this datasheet). The eight D_{0-7} data inputs are converted to either a Data symbol or a Special Character, depending upon the state of the SC/$\overline{D}$ input. If SC/$\overline{D}$ is HIGH, the data inputs represent a control code and are encoded using the Special Character code table. If SC/$\overline{D}$ is LOW, the data inputs are converted using the Data code table. If a byte time passes with the inputs disabled, the Encoder will output a Special Character Comma K28.5 (or SYNC) that will maintain link synchronization. SVS input forces the transmission of a specified Violation symbol to allow the user to check error handling system logic in the controller or for proprietary applications.

The 8B/10B coding function of the Encoder can be bypassed for systems that include an external coder or scrambler function as part of the controller. This bypass is controlled by setting the MODE select pin HIGH. When in bypass mode, D_{a-j} (note that bit order is specified in the Fibre Channel 8B/10B code) become the ten inputs to the Shifter, with D_a being the first bit to be shifted out.

Shifter

The Shifter accepts parallel data from the Encoder once each byte time and shifts it to the serial interface output buffers using a PLL multiplied bit clock that runs at ten (10) times the byte clock rate. Timing for the parallel transfer is controlled by the counter included in the Clock Generator and is not affected by signal levels or timing at the input pins.

OutA, OutB, OutC

The serial interface PECL output buffers (ECL100K referenced to +5v) are the drivers for the serial media. They are all connected to the Shifter and contain the same serial data. Two of the output pairs (OUTA± and OUTB±) are controllable by the FOTO input and can be disabled by the system controller to force a logical zero (i.e., "light off") at the outputs. The third output pair (OUTC±) is not affected by FOTO and will supply a continuous data stream suitable for loop-back testing of the subsystem.

OUTA± and OUTB± will respond to FOTO input changes within a few bit times. However, since FOTO is not synchronized with the transmitter data stream, the outputs will be forced off or turned on at arbitrary points in a transmitted byte. This function is intended to augment an external laser safety controller and as an aid for Receiver PLL testing.

In wire-based systems, control of the outputs may not be required, and FOTO can be strapped LOW. The three outputs are intended to add system and architectural flexibility by offering identical serial bit streams with separate interfaces for redundant connections or for multiple destinations. Unneeded outputs can be wired to V_{CC} to disable and power down the unused output circuitry.

Clock Generator

The clock generator is an embedded phase-locked loop (PLL) that takes a byte-rate reference clock (CKW) and multiplies it by ten (10) to create a bit rate clock for driving the serial shifter. The byte rate reference comes from CKW, the rising edge of which clocks data into the Input register. This clock must be a crystal referenced pulse stream that has a frequency between the minimum and maximum specified for the HOTLink Transmitter/Receiver pair. Signals controlled by this block form the bit clock and the timing signals that control internal data transfers between the Input register and the Shifter.

The read pulse ($\overline{RP}$) is derived from the feedback counter used in the PLL multiplier. It is a byte-rate pulse stream with the proper phase and pulse widths to allow transfer of data from an asynchronous FIFO. Pulse width is independent of CKW duty cycle, since proper phase and duty cycle is maintained by the PLL. The $\overline{RP}$ pulse stream will insure correct data transfers between asynchronous FIFOs and the transmitter input latch with no external logic.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic to properly select the data encoding. Test logic is discussed in more detail in the CY7B923 HOTLink Transmitter Operating Mode Description.

CY7B933 HOTLink Receiver Block Diagram Description

Serial Data Inputs

Two pairs of differential line receivers are the inputs for the serial data stream. INA± or INB± can be selected with the A/$\overline{B}$ input. INA± is selected with A/$\overline{B}$ HIGH and INB± is selected with A/$\overline{B}$ LOW. The threshold of A/$\overline{B}$ is compatible with the ECL 100K signals from PECL fiber optic interface modules. TTL logic elements can be used to select the A or B inputs by adding a resistor pull-up to the TTL driver connected to A/$\overline{B}$. The differential threshold of INA± and INB± will accommodate wire interconnect with filtering losses or transmission line attenuation greater than 20 db ($V_{DIF} \geq 50mv$) or can be directly connected to fiber optic interface modules (any ECL logic family, not limited to ECL 100K). The common mode tolerance will accommodate a wide range of signal termination voltages. The highest HIGH input that can be tolerated is $V_{IN} = V_{CC}$, and the lowest LOW input that can be interpreted correctly is V_{IN} = GND+2.0V.

PECL-TTL Translator

The function of the INB(INB+) input and the SI(INB−) input is defined by the connections on the SO output pin. If the PECL/TTL translator function is not required, the SO output is wired to

V_{CC}. A sensor circuit will detect this connection and cause the inputs to become INB± (a differential line-receiver serial-data input). If the PECL/TTL translator function is required, the SO output is connected to its normal TTL load (typically one or more TTL inputs, but no pull-up resistor) and the INB+ input becomes INB (single-ended ECL 100K, serial data input) and the INB− input becomes SI (single-ended, ECL 100K status input).

This positive-referenced PECL-to-TTL translator is provided to eliminate external logic between an PECL fiber-optic interface module "carrier detect" output and the TTL input in the control logic. The input threshold is compatible with ECL 100K levels (+5V referenced). It can also be used as part of the link status indication logic for wire connected systems.

Clock Synchronization

The Clock Synchronization function is performed by an embedded phase-locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of its internal bit rate clock to the serial data transitions. This block contains the logic to transfer the data from the Shifter to the Decode register once every byte. The counter that controls this transfer is initialized by the Framer logic. CKR is a buffered output derived from the bit counter used to control the Decode register and the output register transfers.

Clock output logic is designed so that when reframing causes the counter sequence to be interrupted, the period and pulse width of CKR will never be less than normal. Reframing may stretch the period of CKR by up to 90%, and either CKR Pulse Width HIGH or Pulse Width LOW may be stretched, depending on when reframe occurs.

The REFCLK input provides a byte-rate reference frequency to improve PLL acquisition time and limit unlocked frequency excursions of the CKR when no data is present at the serial inputs. The frequency of REFCLK is required to be within ±0.1% of the frequency of the clock that drives the transmitter CKW pin.

Framer

Framer logic checks the incoming bit stream for the pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as a Special Character Comma (K28.5). When it is found, the free-running bit counter in the Clock Synchronization block is synchronously reset to its initial state, thus framing the data correctly on the correct byte boundaries.

Random errors that occur in the serial data can corrupt some data patterns into a bit pattern identical to a K28.5, and thus cause an erroneous data-framing error. The RF input prevents this by inhibiting reframing during times when normal message data is present. When RF is held LOW, the HOTLink receiver will deserialize the incoming data without trying to reframe the data to incoming patterns. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, after which $\overline{RDY}$ will resume its normal function. While RF is HIGH, it is possible that an error could cause misframing, after which all data will be corrupted. Likewise, a K28.7 followed by D11.x, D20.x, or an SVS (C0.7) followed by D11.x will create alias K28.5 characters and cause erroneous framing. These sequences must be avoided while RF is HIGH.

If RF remains HIGH for greater than 2048 bytes, the framer converts to double-byte framing, requiring two K28.5 characters aligned on the same byte boundary within 5 bytes in order to reframe. Double-byte framing greatly reduces the possibility of erroneously reframing to an aliased K28.5 character.

Shifter

The Shifter accepts serial inputs from the Serial Data inputs one bit at a time, as clocked by the Clock Synchronization logic. Data is transferred to the Framer on each bit, and to the Decode register once per byte.

Decode Register

The Decode register accepts data from the Shifter once per byte as determined by the logic in the Clock Synchronization block. It is presented to the Decoder and held until it is transferred to the output latch.

Decoder

Parallel data is transformed from ANSI-specified X3.230 8B/10B codes back to "raw data" in the Decoder. This block uses the standard decoder patterns shown in the Valid Data Characters and Valid Special Character Codes and Sequences sections of this datasheet. Data patterns are signaled by a LOW on the SC/$\overline{D}$ output and Special Character patterns are signaled by a HIGH on the SC/$\overline{D}$ output. Unused patterns or disparity errors are signaled as errors by a HIGH on the RVS output and by specific Special Character codes.

Output Register

The Output register holds the recovered data (Q_{0-7}, SC/$\overline{D}$, and RVS) and aligns it with the recovered byte clock (CKR). This synchronization insures proper timing to match a FIFO interface or other logic that requires glitch free and specified output behavior. Outputs change synchronously with the rising edge of CKR.

In BIST mode, this register becomes the signature pattern generator and checker by logically converting itself into a Linear Feedback Shift Register (LFSR) pattern generator. When enabled, this LFSR will generate a 511-byte sequence that includes all Data and Special Character codes, including the explicit violation symbols. This pattern provides a predictable but pseudo-random sequence that can be matched to an identical LFSR in the Transmitter. When synchronized, it checks each byte in the Decoder with each byte generated by the LFSR and shows errors at RVS. Patterns generated by the LFSR are compared after being buffered to the output pins and then fed back to the comparators, allowing test of the entire receive function.

In BIST mode, the LFSR is initialized by the first occurrence of the transmitter BIST loop start code D0.0 (D0.0 is sent only once per BIST loop). Once the BIST loop has been started, RVS will be HIGH for pattern mismatches between the received sequence and the internally generated sequence. Code rule violations or running disparity errors that occur as part of the BIST loop will not cause an error indication. $\overline{RDY}$ will pulse HIGH once per BIST loop and can be used to check test pattern progress. The receiver BIST generator can be reinitialized by leaving and re-entering BIST mode.

Test Logic

Test logic includes the initialization and control for the Built-In Self-Test (BIST) generator, the multiplexer for Test mode clock distribution, and control logic for the decoder. Test logic is discussed in more detail in the CY7B933 HOTLink Receiver Operating Mode Description.

CY7B923/CY7B933 Electrical Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions		Min.	Max.	Unit
TTL OUTs, CY7B923: $\overline{RP}$; CY7B933: Q_{0-7}, SC/$\overline{D}$, RVS, $\overline{RDY}$, CKR, SO						
V_{OHT}	Output HIGH Voltage	I_{OH} = − 2 mA		2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA			0.45	V
I_{OST}	Output Short Circuit Current	V_{OUT} =0V[2]		−15	− 90	mA
TTL INs, CY7B923: D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, CKW, FOTO, BISTEN; CY7B933: RF, REFCLK, $\overline{BISTEN}$						
V_{IHT}	Input HIGH Voltage		Com'l & Mil	2.0	V_{CC}	V
			Mil (CKW and FOTO, only)	2.2	V_{CC}	V
V_{ILT}	Input LOW Voltage			− 0.5	0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{CC}		− 10	+10	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0V			− 500	µA
Transmitter PECL-Compatible Output Pins: OUTA+, OUTA−, OUTB+, OUTB−, OUTC+, OUTC−						
V_{OHE}	Output HIGH Voltage (V_{CC} referenced)	Load = 50 Ω to V_{CC} − 2V	Com'l	V_{CC}−1.03	V_{CC}−0.83	V
			Mil	V_{CC}−1.05	V_{CC}−0.83	V
V_{OLE}	Output LOW Voltage (V_{CC} referenced)	Load = 50 Ω to V_{CC} − 2V	Com'l	V_{CC}−1.86	V_{CC}−1.62	V
			Mil	V_{CC}−1.96	V_{CC}−1.62	V
V_{ODIF}	Output Differential Voltage |(OUT+) − (OUT−)|	Load = 50 ohms to V_{CC} − 2V		0.6		V
Receiver PECL-Compatible Input Pins: A/$\overline{B}$, SI, INB						
V_{IHE}	Input HIGH Voltage		Com'l	V_{CC}−1.165	V_{CC}	V
			Mil	V_{CC}−1.14	V_{CC}	V
V_{ILE}	Input LOW Voltage		Com'l	2.0	V_{CC}−1.475	V
			Mil	2.0	V_{CC}−1.50	V
I_{IHE}[3]	Input HIGH Current	V_{IN} = V_{IHE} Max.			+500	µA
I_{ILE}[3]	Input LOW Current	V_{IN} = V_{ILE} Min.		+0.5		µA
Differential Line Receiver Input Pins: INA+, INA−, INB+, INB−						
V_{DIFF}	Input Differential Voltage |(IN+) − (IN−)|			50		mV
V_{IHH}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILL}	Lowest Input LOW Voltage			2.0		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.			750	µA
I_{ILL}[4]	Input LOW Current	V_{IN} = V_{ILL} Min.		−200		µA
Miscellaneous				**Typ.**	**Max.**	
I_{CCT}[5]	Transmitter Power Supply Current	Freq. = Max.	Com'l	65	85	mA
			Mil	75	95	mA
I_{CCR}[6]	Receiver Power Supply Current	Freq. = Max.	Com'l	120	155	mA
			Mil	135	160	mA

Notes:

1. See the last page of this specification for Group A subgroup testing information.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
3. Applies to A/$\overline{B}$ only.
4. Input currents are always positive at all voltages above V_{CC}/2.
5. Maximum I_{CCT} is measured with V_{CC} = Max., one PECL output pair loaded with 50 ohms to V_{CC} − 2.0V, and other PECL outputs tied to V_{CC}. Typical I_{CCT} is measured with V_{CC} = 5.0V, T_A = 25°C, one output pair loaded with 50 ohms to V_{CC} − 2.0V, others tied to V_{CC}, $\overline{BISTEN}$ = LOW. I_{CCT} includes current into V_{CCQ} (pin 9 and pin 22) only. Current into V_{CCN} is determined by PECL load currents, typically 30 mA with 50 ohms to V_{CC} − 2.0V. Each additional enabled PECL pair adds 5 mA to I_{CCT} and an additional load current to V_{CCN} as described. When calculating the contribution of PECL load currents to chip power dissipation, the output load current should be multiplied by 1V instead of V_{CC}.
6. Maximum I_{CCR} is measured with V_{CC} = Max., RF = LOW, and outputs unloaded. Typical I_{CCR} is measured with V_{CC} = 5.0V, T_A = 25°C, RF = LOW, $\overline{BISTEN}$ = LOW, and outputs unloaded. I_{CCR} includes current into V_{CCQ} (pins 21 and 24). Current into V_{CCN} (pin 9) is determined by the total TTL output buffer quiescent current plus the sum of all the load currents for each output pin. The total buffer quiescent current is 10mA max., and max. TTL load current for each output pin can be calculated as follows:

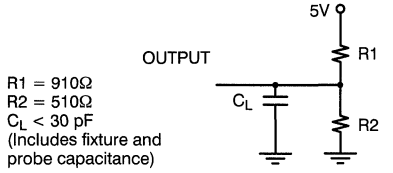
$$\frac{I_{CCN}}{TTLPin} = \left[\frac{0.95 + (V_{CCN} - 5) * 0.3}{R_L} + C_L * \left(\frac{V_{CCN}}{2} + 1.5\right) * F_{pin}\right] * 1.1$$

Where R_L=equivalent load resistance, C_L=capacitive load, and F_{pin}=frequency in MHz of data on pin. A derating factor of 1.1 has been included to account for worst process corner and temperature condition.

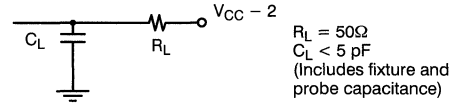
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f_0 = 1$ MHz, $V_{CC} = 5.0V$	10	pF

AC Test Loads and Waveforms

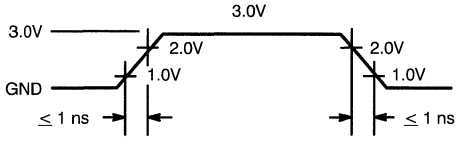


(a) TTL AC Test Load[8]



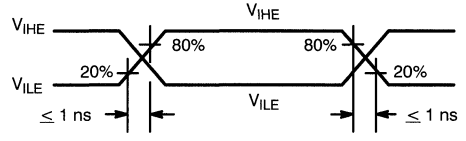
(b) PECL AC Test Load[8]

B923-8



(c) TTL Input Test Waveform

B923-9



(d) PECL Input Test Waveform

B923-10

Transmitter Switching Characteristics Over the Operating Range[1]

Parameter	Description	7B923		Unit
		Min.	Max.	
t_{CKW}	Write Clock Cycle	30.3	62.5	ns
t_B	Bit Time[9]	3.03	6.25	ns
t_{CPWH}	CKW Pulse Width HIGH	6.5		ns
t_{CPWL}	CKW Pulse Width LOW	6.5		ns
t_{SD}	Data Set-Up Time[10]	5		ns
t_{HD}	Data Hold Time[10]	0		ns
t_{SENP}	Enable Set-Up Time (to insure correct $\overline{RP}$)[11]	$6t_B + 8$		ns
t_{HENP}	Enable Hold Time (to insure correct $\overline{RP}$)[11]	0		ns
t_{PDR}	Read Pulse Rise Alignment[12]	−4	2	ns
t_{PPWH}	Read Pulse HIGH[12]	$4t_B-3$		ns
t_{PDF}	Read Pulse Fall Alignment[12]	$6t_B-3$		ns
t_{RISE}	PECL Output Rise Time 20−80% (PECL Test Load)[7]		1.2	ns
t_{FALL}	PECL Output Fall Time 80−20% (PECL Test Load)[7]		1.2	ns
t_{DJ}	Deterministic Jitter (peak-peak)[7, 13]		35	ps
t_{RJ}	Random Jitter (peak-peak)[7, 14]		175	ps
	Random Jitter (σ)[7, 14]		20	ps

Notes:

7. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
8. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
9. Transmitter t_B is calculated as $t_{CKW}/10$. The byte rate is one tenth of the bit rate.
10. Data includes D_{0-7}, SC/$\overline{D}$, SVS, $\overline{ENA}$, $\overline{ENN}$, and $\overline{BISTEN}$. t_{SD} and t_{HD} minimum timing assures correct data load on rising edge of CKW, but not $\overline{RP}$ function or timing.
11. t_{SENP} and t_{HENP} timing insures correct $\overline{RP}$ function and correct data load on the rising edge of CKW.
12. Loading on $\overline{RP}$ is the standard TTL test load shown in part (a) of AC Test Loads and Waveforms except $C_L = 15$ pF.
13. While sending continuous K28.5s, $\overline{Rp}$ unloaded, outputs loaded to 50Ω to $V_{CC}-2.0V$, over the operating range.
14. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to CKW input, over the operating range.

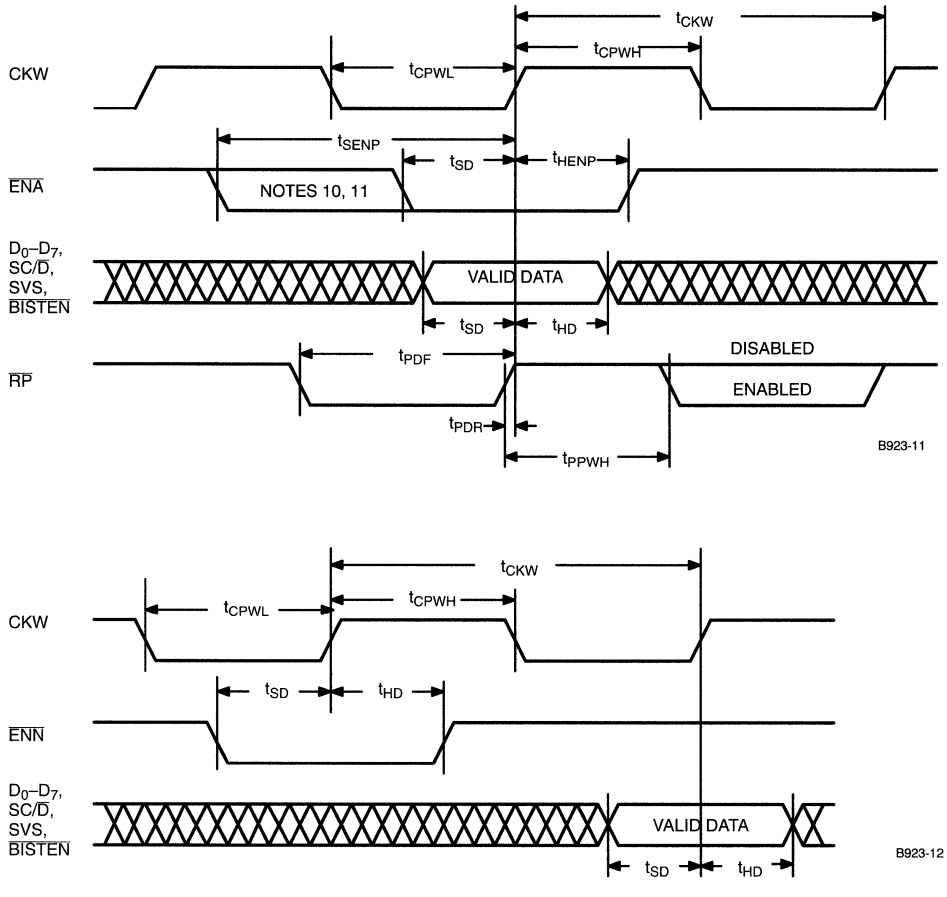
Receiver Switching Characteristics Over the Operating Range[1]

Parameter	Description	7B933		Unit
		Min.	Max.	
t_{CKR}	Read Clock Period (No Serial Data Input), REFCLK as Reference[15]	−1	+1	%
t_B	Bit Time[16]	3.03	6.25	ns
t_{CPRH}	Read Clock Pulse HIGH	$5t_B-3$		ns
t_{CPRL}	Read Clock Pulse LOW	$5t_B-3$		ns
t_{RH}	$\overline{RDY}$ Hold Time	t_B-3		ns
t_{PRF}	$\overline{RDY}$ Pulse Fall to CKR Rise	$5t_B-3$		ns
t_{PRH}	$\overline{RDY}$ Pulse Width HIGH	$4t_B-3$		ns
t_A	Data Access Time[17, 18]	$2t_B-2$	$2t_B+4$	ns
t_{ROH}	Data Hold Time[17, 18]	t_B-3		ns
t_H	Data Hold Time from CKR Rise [17, 18]	$2t_B-3$		ns
t_{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter[19]	−0.1	+0.1	%
t_{CPXH}	REFCLK Clock Pulse HIGH	6.5		ns
t_{CPXL}	REFCLK Clock Pulse LOW	6.5		ns
t_{DS}	Propagation Delay SI to SO (note PECL and TTL thresholds)[20]		20	ns
t_{SA}	Static Alignment[7, 21]		100	ps
t_{EFW}	Error Free Window[7, 22]	$0.9t_B$		

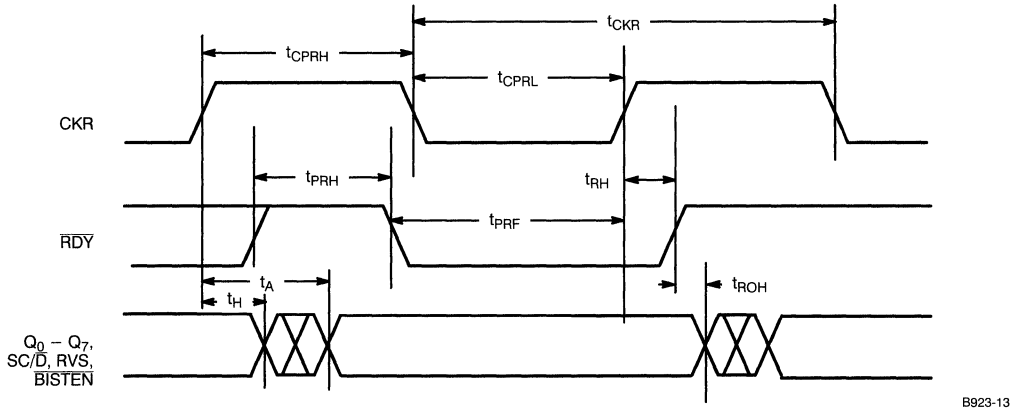
Notes:

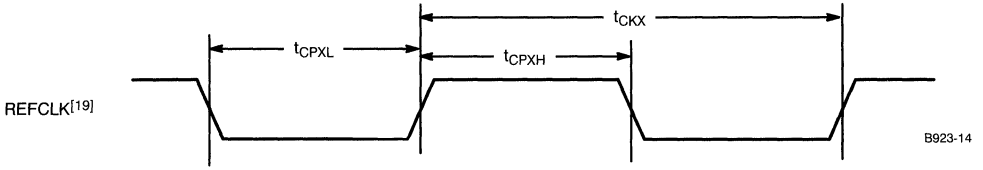
15. The period of t_{CKR} will match the period of the transmitter CKW when the receiver is receiving serial data. When data is interrupted, CKR may drift to one of the range limits above.
16. Receiver t_B is calculated as $t_{CKR}/10$ if no data is being received, or $t_{CKW}/10$ if data is being received. See note 9.
17. Data includes Q_{0-7}, SC/$\overline{D}$, and RVS.
18. t_A, t_{ROH}, and t_H specifications are only valid if all outputs (CKR, $\overline{RDY}$, Q_{0-7}, SC/$\overline{D}$, and RVS) are loaded with similar DC and AC loads.
19. REFCLK has no phase or frequency relationship with CKR and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within 0.1% of the transmitter CKW frequency, necessitating a ±500-PPM crystal.
20. The PECL switching threshold is the midpoint between the PECL–V_{OH}, and V_{OL} specification (approximately V_{CC} − 1.35V). The TTL switching threshold is 1.5V.
21. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a byte error occurs.
22. Error Free Window is a measure of the time window between bit centers where a transition may occur without causing a bit sampling error. EFW is measured over the operating range, input jitter < 50% Dj.

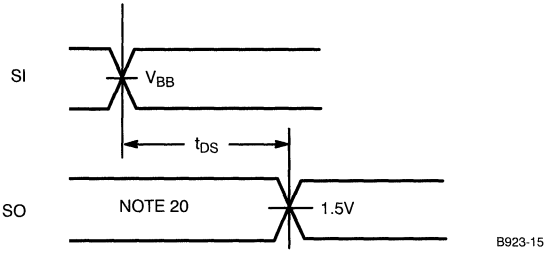
Switching Waveforms for the CY7B923 HOTLink Transmitter



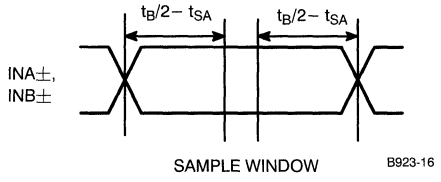
Switching Waveforms for the CY7B933 HOTLink Receiver



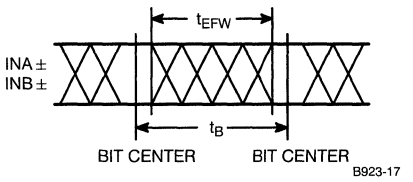




Static Alignment



Error-Free Window



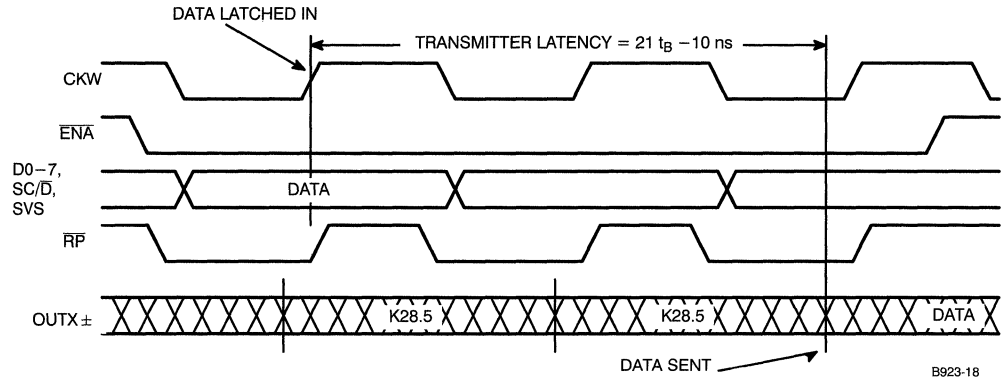


Figure 2. CY7B923 Transmitter Data Pipeline

HOTLink CY7B923 Transmitter and CY7B933 Receiver Operation

The CY7B923 Transmitter operating with the CY7B933 Receiver form a general purpose data communications subsystem capable of transporting user data at up to 33Mbytes per second over several types of serial interface media. *Figure 2* illustrates the flow of data through the HOTLink CY7B923 transmitter pipeline. Data is latched into the transmitter on the rising edge of CKW when enabled by $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$. $\overline{\text{RP}}$ is asserted LOW with a 60% LOW/40% HIGH duty cycle when $\overline{\text{ENA}}$ is LOW. $\overline{\text{RP}}$ may be used as a read strobe for accessing data stored in a FIFO. The parallel data flows through the encoder and is then shifted out of the OUTx± PECL drivers. The bit-rate clock is generated internally from a multiply-by-ten PLL clock generator. The latency through the transmitter is approximately $21t_B$ − 10 ns over the operating range. A more complete description is found in the section *CY7B923 HOTLink Transmitter Operating Mode Description*.

Figure 3 illustrates the data flow through the HOTLink CY7B933 receiver pipeline. Serial data is sampled by the receiver on the INx± inputs. The receiver PLL locks onto the serial bit stream and generates an internal bit rate clock. The bit stream is deserialized, decoded and then presented at the parallel output pins. A byte rate clock (bit clock ÷ 10) sycnchronous with the parallel data is presented at the CKR pin. The $\overline{\text{RDY}}$ pin will be asserted to LOW to indicate that data or control characters are present on the outputs. $\overline{\text{RDY}}$ will not be asserted LOW in a field of K28.5s except for any single K28.5 or the last one in a continuous series of K28.5's. The latency through the receiver is approximately $24t_B$ + 10 ns over the operating range. A more complete description of the receiver is in the section *CY7B933 HOTLink Receiver Operating Mode Description*.

The HOTLink Receiver has a built−in byte framer that synchronizes the Receiver pipeline with incomming SYNC (K28.5) characters. *Figure 4* illustrates the HOTLink CY7B933 Receiver framing operation. The Framer is enabled when the RF pin is asserted HIGH. RF is latched into the receiver on the falling edge of CKR. The framer looks for K28.5 characters embedded in the serial data stream. When a K28.5 is found, the framer sets the parallel byte boundary for subsequent data to the the K28.5 boundary. While the framer is enabled, the $\overline{\text{RDY}}$ pin indicates the status of the framing operation.

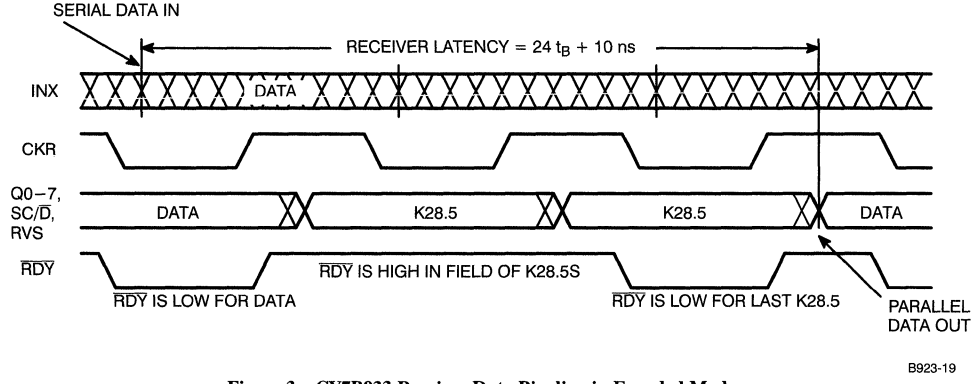


Figure 3. CY7B933 Receiver Data Pipeline in Encoded Mode

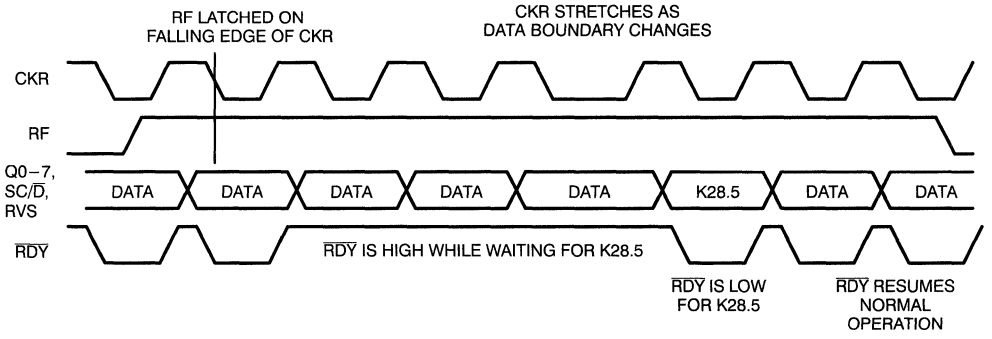


Figure 4. CY7B933 Framing Operation in Encoded Mode

When the RF pin is asserted HIGH, $\overline{RDY}$ leaves it normal mode of operation and is asserted HIGH while the framer searches the data stream for a K28.5 character. After the framer has synchronized to a K28.5 character, the Receiver will assert the $\overline{RDY}$ pin LOW when the K28.5 character is present at the parallel output. The $\overline{RDY}$ pin will then resume its normal operation as dictated by the $\overline{MODE}$ and $\overline{BISTEN}$ pins.

The normal operation of the $\overline{RDY}$ pin in encoded mode is to signal when parallel data is present at the output pins by pulsing LOW with a 60% LOW/40% HIGH duty cycle. $\overline{RDY}$ does not pulse LOW in a field of K28.5 characters; however, $\overline{RDY}$ does pulse LOW for the last K28.5 character in the field or for any single K28.5. In unencoded mode, the normal operation of the $\overline{RDY}$ pin is to signal when any K28.5 is at the parallel output pins.

The Transmitter and Receiver parallel interface timing and functionality can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by appropriately connecting signals (See *Figure 5*). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

The HOTLink Transmitter and Receiver serial interface provides a seamless interface to various types of media. A minimal number of external components are needed to properly terminate transmission lines and provide PECL loads. For proper power supply decoupling, a single 0.01 µF for each device is all that is required to bypass the V_{CC} and GND pins. *Figure 6* illustrates a HOTLink Transmitter and Receiver interface to fiber optic and copper media. More information on interfacing HOTLink to various media can be found in the *HOTLink Design Considerations* application note.

CY7B923 HOTLink Transmitter Operating Mode Description

In normal operation, the Transmitter can operate in either of two modes. The Encoded mode allows a user to send and receive eight (8) bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed in an external protocol controller.

In either mode, data is loaded into the Input register of the Transmitter on the rising edge of CKW. The input timing and functional response of the Transmitter input can be made to match the timing and functionality of either an asynchronous FIFO or a clocked FIFO by an appropriate connection of input signals (See *Figure 5*). Proper operation of the FIFO interface depends upon various FIFO-specific access and response specifications.

Encoded Mode Operation

In Encoded mode the input data is interpreted as eight bits of data (D_0 – D_7), a context control bit (SC/$\overline{D}$), and a system diagnostic input bit (SVS). If the context of the data is to be normal message data, the SC/$\overline{D}$ input should be LOW, and the data should be encoded using the valid data character set described in the Valid Data Characters section of this datasheet. If the context of the data is to be control or protocol information, the SC/$\overline{D}$ input will be HIGH, and the data will be encoded using the valid special character set described in the Valid Special Character Codes and Sequences section. Special characters include all protocol characters necessary to encode packets for Fibre Channel, ESCON, proprietary systems, and diagnostic purposes.

The diagnostic characters and sequences available as Special Characters include those for Fibre Channel link testing, as well as codes to be used for testing system response to link errors and timing. A Violation symbol can be explicitly sent as part of a user data packet (i.e., send C0.7; D_{7-0} = 111 00000 and SC/$\overline{D}$ = 1), or it can be sent in response to an external system using the SVS input. This will allow system diagnostic logic to evaluate the errors in an unambiguous manner, and will not require any modification to the transmission interface to force transmission errors for testing purposes.

Bypass Mode Operation

In Bypass mode the input data is interpreted as ten (10) bits (D_{b-h}), SC/$\overline{D}$ (D_a), and SVS (D_j) of pre-encoded transmission data to be serialized and sent over the link. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte), and that it be compatible with the transmission media.

Data loaded into the Input register on the rising edge of CKW will be loaded into the Shifter on the subsequent rising edges of CKW. It will then be shifted to the outputs one bit at a time using the internal clock generated by the clock generator. The first bit of the transmission character (D_a) will appear at the output (OUTA±, OUTB±, and OUTC±) after the next CKW edge.

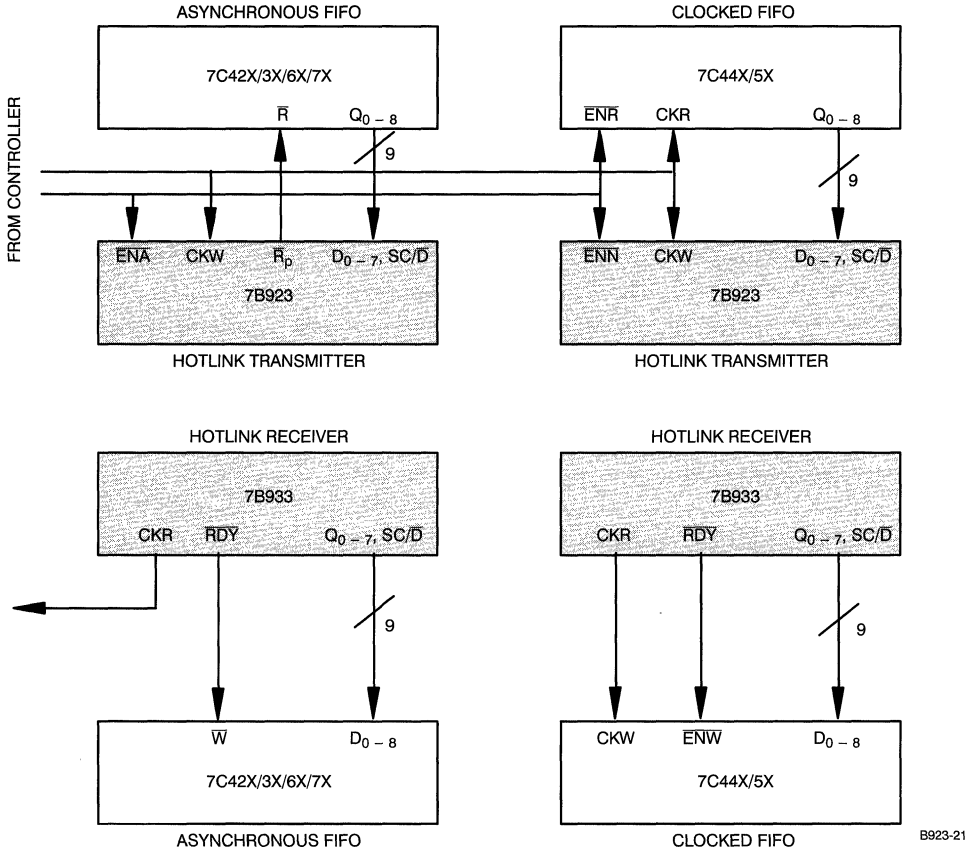


Figure 5. Seamless FIFO Interface

While in either the Encoded mode or Bypass mode, if a CKW edge arrives when the inputs are not enabled ($\overline{ENA}$ and $\overline{ENN}$ both HIGH), the Encoder will insert a pad character K28.5 (e.g., C5.0) to maintain proper link synchronization (in Bypass mode the proper sense of running disparity cannot be guaranteed for the first pad character, but is correct for all pad characters that follow). This automatic insertion of pad characters can be inhibited by insuring that the Transmitter is always enabled (i.e., $\overline{ENA}$ or $\overline{ENN}$ is hardwired LOW).

PECL Output Functional and Connection Options

The three pairs of PECL outputs all contain the same information and are intended for use in systems with multiple connections. Each output pair may be connected to a different serial media, each of which may be a different length, link type, or interface technology. For systems that do not require all three output pairs, the unused pairs should be wired to V_{CC} to minimize the power dissipated by the output circuit, and to minimize unwanted noise generation. An internal voltage comparator detects when an output differential pair is wired to V_{CC}, causing the current source for that pair to be disabled. This results in a power savings of around 5 mA for each unused pair.

In systems that require the outputs to be shut off during some periods when link transmission is prohibited (e.g., for laser safety functions), the FOTO input can be asserted. While it is possible to insure that the output state of the PECL drivers is LOW (i.e., light is off) by sending all 0's in Bypass mode, it is often inconvenient to insert this level of control into the data transmission channel, and it is impossible in Encoded mode. FOTO is provided to simplify and augment this control function (typically found in laser-based transmission systems). FOTO will force OUTA+ and OUTB+ to go LOW, OUTA− and OUTB− to go HIGH, while allowing OUTC± to continue to function normally (OUTC is typically used as a diagnostic feedback and cannot be disabled). This separation of function allows various system configurations without undue load on the control function or data channel logic.

Transmitter Serial Data Characteristics

The CY7B923 HOTLink Transmitter serial output conforms to the requirements of the Fibre Channel specification. The serial data output is controlled by an internal Phase-Locked Loop that multiplies the frequency of CKW by ten (10) to maintain the proper bit clock frequency. The jitter characteristics (including both PLL and logic components) are shown below:

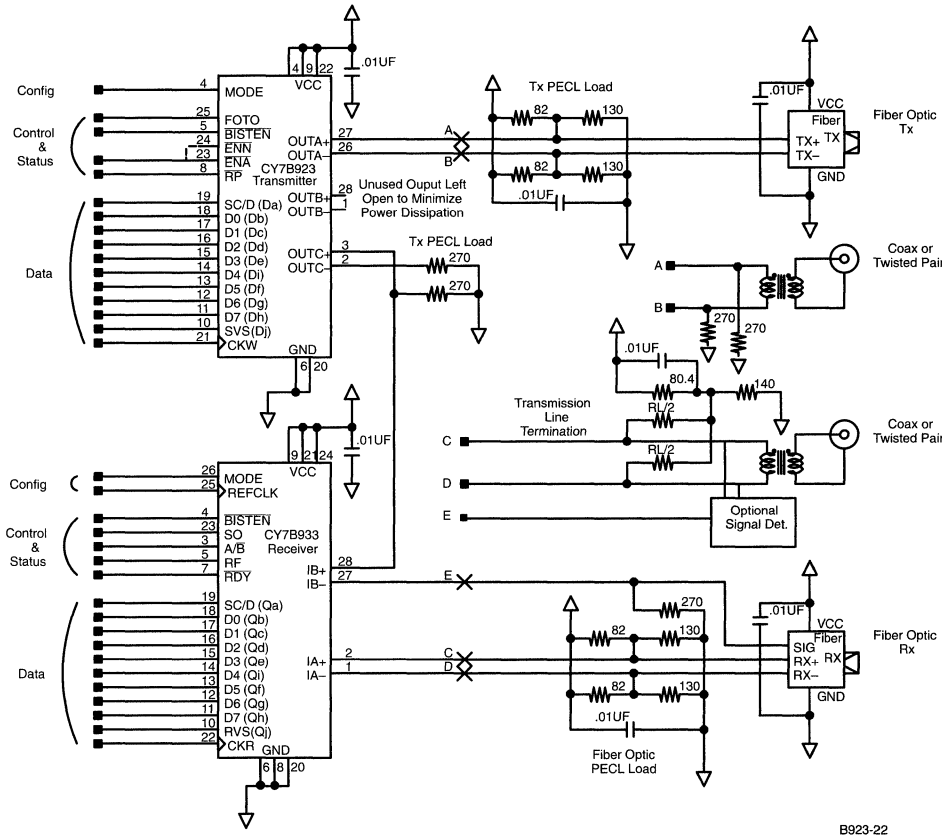


Figure 6. HOTLink Connection Diagram

Deterministic Jitter (D_j) < 35 ps (peak-peak). Typically measured while sending a continuous K28.5 (C5.0).

Random Jitter (R_j) < 175 ps (peak-peak). Typically measured while sending a continuous K28.7 (C7.0).

Transmitter Test Mode Description

The CY7B923 Transmitter offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver, and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 7*.

BIST Mode

BIST mode functions as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to begin test pattern generation. Transmitter begins sending bit rate ...1010...
2. Set either $\overline{\text{ENA}}$ or $\overline{\text{ENN}}$ LOW to begin pattern sequence generation (use of the Enable pin not being used for normal FIFO or system interface can minimize logic delays between the controller and transmitter).
3. Allow the Transmitter to run through several BIST loops or until the Receiver test is complete. $\overline{\text{RP}}$ will pulse LOW once per BIST loop, and can be used by an external counter to monitor the number of test pattern loops.
4. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and $\overline{\text{ENA}}$ and $\overline{\text{ENN}}$ HIGH and resume normal function.

Note: It may be advisable to send violation characters to test the RVS output in the Receiver. This can be done by explicitly sending a violation with the SVS input, or allowing the transmitter BIST loop to run while the Receiver runs in normal mode. The BIST loop includes deliberate violation symbols and will adequately test the RVS function.

BIST mode is intended to check the entire function of the Transmitter (except the Transmitter input pins and the bypass function in the Encoder), the serial link, and the Receiver. It augments normal factory ATE testing and provides the designer with a rigorous test mechanism to check the link transmission system without requiring any significant system overhead.

While in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{\text{BISTEN}}$ = LOW causes the Transmitter to switch to Encoded mode and begin sending the BIST pattern, as if MODE = LOW. When $\overline{\text{BISTEN}}$ returns

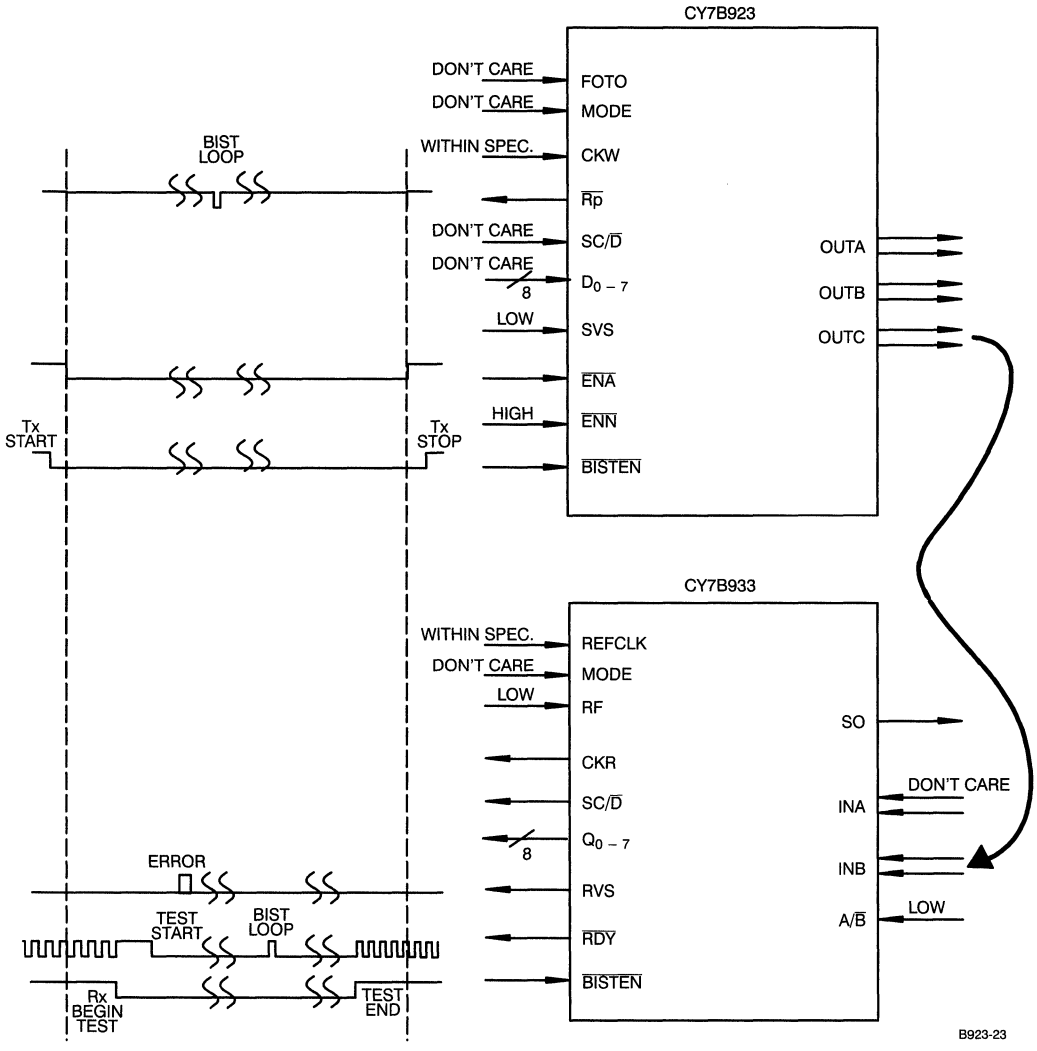


Figure 7. Built-In Self-Test Illustration

to HIGH, the Transmitter resumes normal Bypass operation. In Test mode the BIST function works as in the Normal mode. For more information on BIST, consult the "HOTLink Built-In Self-Test" Application Note.

Test Mode

The MODE input pin selects between three transmitter functional modes. When wired to V_{CC}, the $D_{(a-j)}$ inputs bypass the Encoder and load directly from the Input register into the Shifter. When wired to GND, the inputs D_{0-7}, SVS, and SC/$\overline{D}$ are encoded using the Fibre Channel 8B/10B codes and sequences (shown at the end of this datasheet). Since the Transmitter is usually hard wired to Encoded or Bypass mode and not switched between them, a third function is provided for the MODE pin. Test mode is selected by floating the MODE pin (internal resistors hold the MODE pin at $V_{CC}/2$). Test mode is used for factory or incoming device test.

Test mode causes the Transmitter to function in its Encoded mode, but with OutA+/OutB+ (used as a differential test clock input) as the bit rate clock input instead of the internal PLL-generated bit clock. In this mode, inputs are clocked by CKW and transfers between the Input register and Shifter are timed by the internal counters. The bit-clock and CKW must maintain a fixed phase and divide-by-ten ratio. The phase and pulse width of $\overline{RP}$ are controlled by phases of the bit counter (PLL feedback counter) as in Normal mode. Input and output patterns can be synchronized with internal logic by observing the state of $\overline{RP}$ or the device can be

initialized to match an ATE test pattern using the following technique:

1. With the MODE pin either HIGH or LOW, stop CKW and bit-clock.
2. Force the MODE pin to MID (open or $V_{CC}/2$) while the clocks are stopped.
3. Start the bit-clock and let it run for at least 2 cycles.
4. Start the CKW clock at the bit-clock/10 rate.

Test mode is intended to allow logical, DC, and AC testing of the Transmitter without requiring that the tester check output data patterns at the bit rate, or accommodate the PLL lock, tracking, and frequency range characteristics that are required when the HOTLink part operates in its normal mode. To use OutA+/OutB+ as the test clock input, the FOTO input is held HIGH while in Test mode. This forces the two outputs to go to an "PECL LOW," which can be ignored while the test system creates a differential input signal at some higher voltage.

CY7B933 HOTLink Receiver Operating Mode Description

In normal user operation, the Receiver can operate in either of two modes. The Encoded mode allows a user system to send and receive 8-bit data and control information without first converting it to transmission characters. The Bypass mode is used for systems in which the encoding and decoding is performed by an external protocol controller.

In either mode, serial data is received at one of the differential line receiver inputs and routed to the Shifter and the Clock Synchronization. The PLL in the Clock Synchronizer aligns the internally generated bit rate clock with the incoming data stream and clocks the data into the shifter. At the end of a byte time (ten bit times), the data accumulated in the shifter is transferred to the Decode register.

To properly align the incoming bit stream to the intended byte boundaries, the bit counter in the Clock Synchronizer must be initialized. The Framer logic block checks the incoming bit stream for the unique pattern that defines the byte boundaries. This combinatorial logic filter looks for the X3.230 symbol defined as "Special Character Comma" (K28.5). Once K28.5 is found, the free running bit counter in the Clock Synchronizer block is synchronously reset to its initial state, thus "framing" the data to the correct byte boundaries.

Since noise-induced errors can cause the incoming data to be corrupted, and since many combinations of error and legal data can create an alias K28.5, an option is included to disable resynchronization of the bit counter. The Framer will be inhibited when the RF input is held LOW. When RF rises, $\overline{RDY}$ will be inhibited until a K28.5 has been detected, and $\overline{RDY}$ will resume its normal function. Data will continue to flow through the Receiver while $\overline{RDY}$ is inhibited.

Encoded Mode Operation

In Encoded mode the serial input data is decoded into eight bits of data ($Q_0 - Q_7$), a context control bit ($SC/\overline{D}$), and a system diagnostic output bit (RVS). If the pattern in the Decode register is found in the Valid Data Characters table, the context of the data is decoded as normal message data and the $SC/\overline{D}$ output will be LOW. If the incoming bit pattern is found in the Valid Special Character Codes and Sequences table, it is interpreted as "control" or "protocol information," and the $SC/\overline{D}$ output will be HIGH. Special characters include all protocol characters defined for use in packets for Fibre Channel, ESCON, and other proprietary and diagnostic purposes.

The Violation symbol that can be explicitly sent as part of a user data packet (i.e., Transmitter sending C0.7; D_{7-0} = 111 00000 and $SC/\overline{D}$ = 1; or SVS = 1) will be decoded and indicated in exactly the same way as a noise-induced error in the transmission link. This function will allow system diagnostics to evaluate the error in an unambiguous manner, and will not require any modification to the receiver data interface for error-testing purposes.

Bypass Mode Operation

In Bypass mode the serial input data is not decoded, and is transferred directly from the Decode register to the Output register's 10 bits ($Q_{(a-j)}$). It is assumed that the data has been pre-encoded prior to transmission, and will be decoded in subsequent logic external to HOTLink. This data can use any encoding method suitable to the designer. The only restrictions upon the data encoding method is that it contain suitable transition density for the Receiver PLL data synchronizer (one per 10 bit byte) and that it be compatible with the transmission media.

The framer function in Bypass mode is identical to Encoded mode, so a K28.5 pattern can still be used to re-frame the serial bit stream.

Parallel Output Function

The 10 outputs (Q_{0-7}, $SC/\overline{D}$, and RVS) all transition simultaneously, and are aligned with $\overline{RDY}$ and CKR with timing allowances to interface directly with either an asynchronous FIFO or a clocked FIFO. Typical FIFO connections are shown in *Figure 5*.

Data outputs can be clocked into the system using either the rising or falling edge of CKR, or the rising or falling edge of $\overline{RDY}$. If CKR is used, $\overline{RDY}$ can be used as an enable for the receiving logic. A LOW pulse on $\overline{RDY}$ shows that new data has been received and is ready to be delivered. The signal on $\overline{RDY}$ is a 60%–LOW duty cycle byte-rate pulse train suitable for the write pulse in asynchronous FIFOs such as the CY7C42X, or the enable write input on Clocked FIFOs such as the CY7C44X. HIGH on $\overline{RDY}$ shows that the received data appearing at the outputs is the null character (normally inserted by the transmitter as a pad between data inputs) and should be ignored.

When the Transmitter is disabled it will continuously send pad characters (K28.5). To assure that the receive FIFO will not be overfilled with these dummy bytes, the $\overline{RDY}$ pulse output is inhibited during fill strings. Data at the Q_{0-7} outputs will reflect the correct received data, but will not appear to change, since a string of K28.5s all are decoded as Q_{7-0} =000 00101 and $SC/\overline{D}$ = 1 (C5.0). When new data appears (not K28.5), the $\overline{RDY}$ output will resume normal function. The "last" K28.5 will be accompanied by a normal $\overline{RDY}$ pulse.

Fill characters are defined as any K28.5 followed by another K28.5. All fill characters will not cause $\overline{RDY}$ to pulse. Any K28.5 followed by any other character (including violation or illegal characters) will be interpreted as usable data and will cause $\overline{RDY}$ to pulse.

As noted above, $\overline{RDY}$ can also be used as an indication of correct framing of received data. While the Receiver is awaiting receipt of a K28.5 with RF HIGH, the $\overline{RDY}$ outputs will be inhibited. When $\overline{RDY}$ resumes, the received data will be properly framed and will be decoded correctly. In Bypass mode with RF HIGH, $\overline{RDY}$ will pulse once for each K28.5 received. For more information on the $\overline{RDY}$ pin, consult the "HOTLink CY7B933 $\overline{RDY}$ Pin Description" application note.

Code rule violations and reception errors will be indicated as follows:

	RVS	SC/$\overline{D}$	Qouts	Name
1. Good Data code received with good Running Disparity (RD)	0	0	00–FF	D0.0–31.7
2. Good Special Character code received with good RD	0	1	00–0B	C0.0–11.0
3. K28.7 immediately following K28.1 (ESCON Connect_SOF)	0	1	27	C7.1
4. K28.7 immediately following K28.5 (ESCON Passive_SOF)	0	1	47	C7.2
5. Unassigned code received	1	1	E0	C0.7
6. –K28.5+ received when RD was +	1	1	E1	C1.7
7. +K28.5– received when RD was –	1	1	E2	C2.7
8. Good code received with wrong RD	1	1	E4	C4.7

Receiver Serial Data Requirements

The CY7B933 HOTLink Receiver serial input capability conforms to the requirements of the Fibre Channel specification. The serial data input is tracked by an internal Phase-Locked Loop that is used to recover the clock phase and to extract the data from the serial bit stream. Jitter tolerance characteristics (including both PLL and logic component requirements) are shown below:

Deterministic Jitter tolerance (D_j) >40% of t_B. Typically measured while receiving data carried by a bandwidth-limited channel (e.g., a coaxial transmission line) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Random Jitter tolerance (R_j) > 90% of t_B. Typically measured while receiving data carried by a random-noise-limited channel (e.g., a fiber-optic transmission system with low light levels) while maintaining a Bit Error Rate (BER) $<10^{-12}$.

Total Jitter tolerance >90% of t_B. Total of $D_j + R_j$.

PLL-Acquisition time <500-bit times from worst-case phase or frequency change in the serial input data stream, to receiving data within BER objective of 10^{-12}. Stable power supplies within specifications, stable REFCLK input frequency and normal data framing protocols are assumed. Note: Acquisition time is measured from worst-case phase or frequency change to zero phase and frequency error. As a result of the receiver's wide jitter tolerance, valid data will appear at the receiver's outputs a few byte times after a worst-case phase change.

Receiver Test Mode Description

The CY7B933 Receiver offers two types of test mode operation, BIST mode and Test mode. In a normal system application, the Built-In Self-Test (BIST) mode can be used to check the functionality of the Transmitter, the Receiver and the link connecting them. This mode is available with minimal impact on user system logic, and can be used as part of the normal system diagnostics. Typical connections and timing are shown in *Figure 7.*

BIST Mode

BIST Mode function is as follows:

1. Set $\overline{\text{BISTEN}}$ LOW to enable self-test generation and await $\overline{\text{RDY}}$ LOW indicating that the initialization code has been received.
2. Monitor RVS and check for any byte time with the pin HIGH to detect pattern mismatches. $\overline{\text{RDY}}$ will pulse HIGH once per BIST loop, and can be used by an external counter to monitor test pattern progress. Q_{0-7} and SC/$\overline{D}$ will show the expected pattern and may be useful for debug purposes.
3. When testing is completed, set $\overline{\text{BISTEN}}$ HIGH and resume normal function.

Note: A specific test of the RVS output may be required to assure an adequate test. To perform this test, it is only necessary to have the Transmitter send violation (SVS = HIGH) for a few bytes before beginning the BIST test sequence. Alternatively, the Receiver could enter BIST mode after the Transmitter has begun sending BIST loop data, or be removed before the Transmitter finishes sending BIST loops, each of which contain several deliberate violations and should cause RVS to pulse HIGH.

BIST mode is intended to check the entire function of the Transmitter, serial link, and Receiver. It augments normal factory ATE testing and provides the user system with a rigorous test mechanism to check the link transmission system, without requiring any significant system overhead.

When in Bypass mode, the BIST logic will function in the same way as in the Encoded mode. MODE = HIGH and $\overline{\text{BISTEN}}$ = LOW causes the Receiver to switch to Encoded mode and begin checking the decoded received data of the BIST pattern, as if MODE = LOW. When $\overline{\text{BISTEN}}$ returns to HIGH, the Receiver resumes normal Bypass operation. In Test mode the BIST function works as in the normal mode.

Test Mode

The MODE input pin selects between three receiver functional modes. When wired to V_{CC}, the Shifter contents bypass the Decoder and go directly from the Decoder latch to the Q_{a-j} inputs of the Output latch. When wired to GND, the outputs are decoded using the 8B/10B codes shown at the end of this datasheet and become Q_{0-7}, RVS, and SC/$\overline{D}$. The third function is Test mode, used for factory or incoming device test. This mode can be selected by leaving the MODE pin open (internal circuitry forces the open pin to $V_{CC}/2$).

Test mode causes the Receiver to function in its Encoded mode, but with INB (INB+) as the bit rate Test clock instead of the Internal PLL generated bit clock. In this mode, transfers between the Shifter, Decoder register and Output register are controlled by their normal logic, but with an external bit rate clock instead of the PLL (the recovered bit clock). Internal logic and test pattern inputs can be synchronized by sending a SYNC pattern and allowing the Framer to align the logic to the bit stream. The flow is as follows:

1. Assert Test mode for several test clock cycles to establish normal counter sequence.
2. Assert RF to enable reframing.
3. Input a repeating sequence of bits representing K28.5 (Sync).
4. $\overline{\text{RDY}}$ falling shows the byte boundary established by the K28.5 input pattern.
5. Proceed with pattern, voltage and timing tests as is convenient for the test program and tester to be used.

(While in Test mode and in BIST mode with RF HIGH, the Q_{0-7}, RVS, and SC/$\overline{D}$ outputs reflect various internal logic states and not the received data.)

Test mode is intended to allow logical, DC, and AC testing of the Receiver without requiring that the tester generate input data at the bit rate or accommodate the PLL lock, tracking and frequency

range characteristics that are required when the part operates in its normal mode.

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data (Data Characters) are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary rationale for use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard consist of a distinct and easily recognizable bit pattern (the Special Character Comma) that assists a Receiver in achieving word alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character (using 8B/10B Transmission Code notation)

```
FC-2  45
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation (note carefully that the order of bits is reversed):

```
Data Byte Name   D5.2
                 Bits: ABCDE FGH
                       10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
Bits: abcdei  fghj
      101001  0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and the SC/$\overline{D}$ pin is LOW) or a Special Character (c is set to K, and the SC/$\overline{D}$ pin is HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

Note: This definition of the 10-bit Transmission Code is based on (and is in basic agreement with) the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code" *IBM Journal of Research and Development*, 27, No. 5: 440–451 (September, 1983).

U.S. Patent 4,488,739. Peter A. Franaszek and Albert X. Widmer. "Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code" (December 4, 1984).

Fibre Channel Physical and Signaling Interface (dpANS X3.230–199X ANSI FC–PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22–7202).

8B/10B Transmission Code

The following information describes how the tables shall be used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within the higher-level constructs specified by the standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit "a" shall be transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order. (Note that bit i shall be transmitted between bit e and bit f, rather than in alphabetical order.)

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two (not necessarily different) Transmission Characters. The two columns correspond to the current value of the running disparity ("Current RD–" or "Current RD+"). Running disparity is a binary parameter with either the value negative (–) or the value positive (+).

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter shall calculate a new value for its running disparity based on the contents of the transmitted character. Special Character codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver shall decide whether the Transmission Character is valid or invalid according to the following rules and tables and shall calculate a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity shall be used to calculate the new running-disparity value for Transmission Characters that have been transmitted (Transmitter's running disparity) and that have been received (Receiver's running disparity).

Running disparity for a Transmission Character shall be calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks shall be calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in the table shall be found for the Valid Data byte or the Special Character byte for which a Transmission Character is to be generated (encoded). The current value of the Transmitter's running disparity shall be used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity shall be calculated. This new value shall be used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 1* shows naming notations and examples of valid transmission characters.

Table 1. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	000101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity shall be searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character shall be used to calculate a new value of running disparity. The new value shall be used as the Receiver's current running disparity for the next received Transmission Character.

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 2* shows an example of this behavior.

Table 2. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Valid Data Characters (SC/$\overline{D}$ = LOW)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.2	010	11111	101011	0101	010100	0101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.4	100	00110	011001	1101	011001	0010
D7.4	100	00111	111000	1101	000111	0010
D8.4	100	01000	111001	0010	000110	1101
D9.4	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010
D18.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010

Valid Data Characters (SC/$\overline{D}$ = LOW) (continued)

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110

Data Byte Name	Bits		Current RD−		Current RD+	
	HGF	EDCBA	abcdei	fghj	abcdei	fghj
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

Valid Special Character Codes and Sequences (SC/$\overline{D}$ = HIGH)[23, 24]

S.C. Byte Name	S.C. Code Name		Bits HGF	Bits EDCBA	Current RD− abcdei	Current RD− fghj	Current RD+ abcdei	Current RD+ fghj
K28.0	C0.0	(C00)	000	00000	001111	0100	110000	1011
K28.1	C1.0	(C01)	000	00001	001111	1001	110000	0110
K28.2	C2.0	(C02)	000	00010	001111	0101	110000	1010
K28.3	C3.0	(C03)	000	00011	001111	0011	110000	1100
K28.4	C4.0	(C04)	000	00100	001111	0010	110000	1101
K28.5	C5.0	(C05)	000	00101	001111	1010	110000	0101
K28.6	C6.0	(C06)	000	00110	001111	0110	110000	1001
K28.7	C7.0	(C07)	000	00111	001111	1000	110000	0111
K23.7	C8.0	(C08)	000	01000	111010	1000	000101	0111
K27.7	C9.0	(C09)	000	01001	110110	1000	001001	0111
K29.7	C10.0	(C0A)	000	01010	101110	1000	010001	0111
K30.7	C11.0	(C0B)	000	01011	011110	1000	100001	0111
Idle	C0.1	(C20)	001	00000	−K28.5+, D21.4, D21.5, D21.5, repeat[25]			
R_RDY	C1.1	(C21)	001	00001	−K28.5+, D21.4, D10.2, D10.2, repeat[26]			
EOFxx	C2.1	(C22)	001	00010	−K28.5, Dn.xxx0[27]		+K28.5, Dn.xxx1[27]	
	Follows K28.1 for ESCON Connect-SOF (Rx indication only)							
C-SOF	C7.1	(C27)	001	00111	001111	1000	110000	0111
	Follows K28.5 for ESCON Passive-SOF (Rx indication only)							
P-SOF	C7.2	(C47)	010	00111	001111	1000	110000	0111
					Code Rule Violation and SVS Tx Pattern			
Exception	C0.7	(CE0)	111	00000	100111	1000[28]	011000	0111[28]
−K28.5	C1.7	(CE1)	111	00001	001111	1010[29]	001111	1010[29]
+K28.5	C2.7	(CE2)	111	00010	110000	0101[30]	110000	0101[30]
					Running Disparity Violation Pattern			
Exception	C4.7	(CE4)	111	00100	110111	0101[31]	001000	1010[31]

Notes:

23. All codes not shown are reserved.
24. Notation for Special Character Byte Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn=the specified value between 00 and FF).
25. C0.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D21.5, D21.5, (repeat all four bytes)... defined in X3.230 as the primitive signal "Idle word." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

Notes (continued):

26. C1.1 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD when input is held for only one byte time. If held longer, transmitter begins sending the repeating transmit sequence −K28.5+, D21.4, D10.2, D10.2,(repeat all four bytes)... defined in X3.230 as the primitive signal "Receiver_Ready (R_RDY)." This Special Character input must be held for four (4) byte times or multiples of four bytes or it will be truncated by the new data.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7 and the subsequent bytes are decoded as data.

27. C2.1 = Transmit either −K28.5+ or +K28.5− as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (−) the LSB becomes 1. This modification allows construction of X3.230 "EOF" frame delimiters wherein the second data byte is determined by the Current RD.

    For example, to send "EOFdt" the controller could issue the sequence C2.1−D21.4− D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D21.4−D21.4−D21.4 or K28.5−D21.5−D21.4−D21.4 based on Current RD. Likewise to send "EOFdti" the controller could issue the sequence C2.1−D10.4−D21.4−D21.4, and the HOTLink Transmitter will send either K28.5−D10.4−D21.4−D21.4 or K28.5−D10.5−D21.4− D21.4 based on Current RD.

    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.

28. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. Transmission of this Special Character has the same effect as asserting SVS = HIGH.

    The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.

29. C1.7 = Transmit Negative K28.5 (−K28.5+) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if −K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.

30. C2.7 = Transmit Positive K28.5 (+K28.5−) disregarding Current RD.

    The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD−, otherwise K28.5 is decoded as C5.0 or C1.7.

31. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation.

    The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B923−JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B923−SC	S21	28-Lead (300-Mil) SOIC	
CY7B923−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B923−LMB	L64	28-Square Leadless Chip Carrier	Military

Ordering Code	Package Name	Package Type	Operating Range
CY7B933−JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B933−SC	S21	28-Lead (300-Mil) SOIC	
CY7B933−JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
CY7B933−LMB	L64	28-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroup
V_{OHT}	1, 2, 3
V_{OLT}	1, 2, 3
V_{OHE}	1, 2
V_{OLE}	1, 2, 3
V_{ODIF}	1, 2, 3
I_{OST}	1, 2, 3
V_{IHT}	1, 2, 3
V_{ILT}	1, 2, 3
V_{IHE}	1, 2, 3
V_{ILE}	1, 2, 3
I_{IHT}	1, 2, 3
I_{ILT}	1, 2, 3
I_{IHE}	1, 2, 3
I_{ILE}	1, 2, 3
I_{CC}	1, 2, 3
V_{DIFF}	1, 2, 3
V_{IHH}	1, 2, 3
V_{ILL}	1, 2, 3

Switching Characteristics

Parameter	Subgroup
t_{CKW}	9, 10, 11
t_{B}	9, 10, 11
t_{CPWH}	9, 10, 11
t_{CPWL}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SENP}	9, 10, 11
t_{HENP}	9, 10, 11
t_{PDR}	9, 10, 11
t_{PPWH}	9, 10, 11
t_{PDF}	9, 10, 11
t_{RISE}	9, 10, 11
t_{FALL}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CPRH}	9, 10, 11
t_{CPRL}	9, 10, 11
t_{RH}	9, 10, 11
t_{PRF}	9, 10, 11
t_{PRH}	9, 10, 11
t_{A}	9, 10, 11
t_{ROH}	9, 10, 11
t_{CKX}	9, 10, 11
t_{CPXH}	9, 10, 11
t_{CPXL}	9, 10, 11
t_{DS}	9, 10, 11

Document #: 38−00189−F

CY101E383

ECL/TTL/ECL Translator and High-Speed Bus Driver

Features

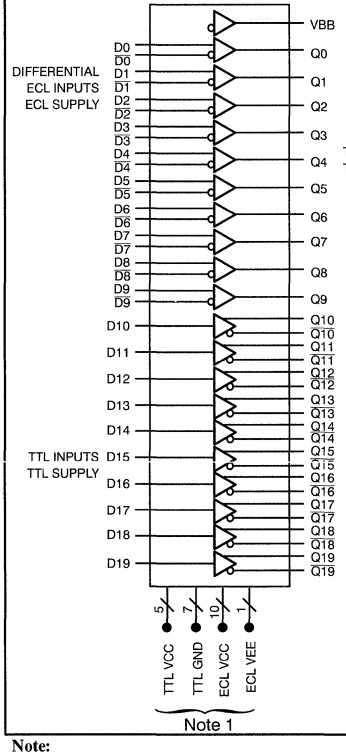
- **BiCMOS for optimum speed/power**
- **High speed (max.)**
  - **—2.5 ns t_{PD} TTL-to-ECL**
  - **—3 ns t_{PD} ECL-to-TTL**
- **Low skew < ± 1 ns**
- **Can operate on single +5V supply**
- **Full-duplex ECL/TTL data transmission**
- **Internal 2 kΩ ECL pull-down resistors on each ECL output**
- **80-pin PQFP package**
- **Surface-mount PLCC/CLCC package**
- **V_{BB} ECL reference voltage output**
- **Single- or dual-supply operation**
- **Capable of greater than 2001V ESD**
- **ECL cable/twisted pair driver**

Functional Description

The CY101E383 is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains ten independent TTL-to-ECL and ten independent ECL-to-TTL translators for high-speed full-duplex data transmission, mixed logic, and bus applications. The CY101E383 is especially suited to drive ECL backplanes between TTL boards. The CY101E383 is implemented with differential ECL I/O to provide balanced low noise operation over controlled impedance buses between TTL and/or ECL subsystems. In addition, the device has internal output 2 kΩ pull-down resistors tied to V_{EE} to decrease the number of external components. For system testing purposes or for driving light loads, the 2 kΩ is used as the only termination thereby eliminating up to 20 external resistors. The part meets standard 100K logic levels with the internal pull-down while driving 50Ω to −2V.

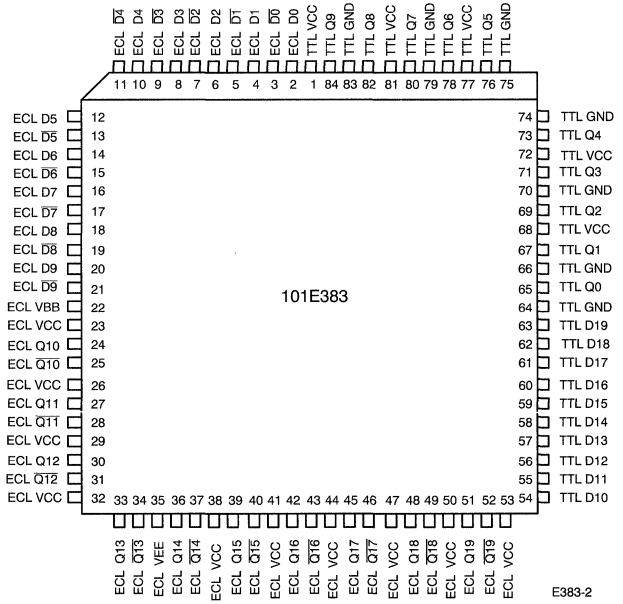
The device is designed with ample ground pins to reduce bounce, and has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The parts can operate in single- or dual-supply configurations while maintaining absolute and 100K level swings. The translators are offered in a standard 100K ECL-compatible version with −5.2V or −4.5V power supply. The TTL I/O is fully TTL compatible. The CY101E383 is packaged in 84-pin surface-mountable PLCCs and CLCCs. To save board space, an 80-pin PQFP package with 25-mil-lead pitch is available.

Logic Block Diagram



Pin Configurations

PLCC/CLCC
Top View

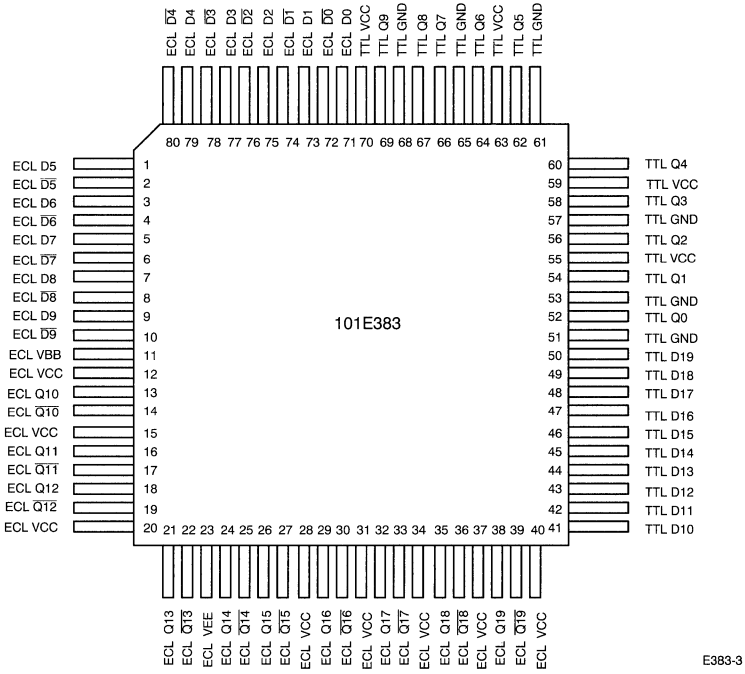


Note:

1. The PQFP package has one less each TTL V_{CC} and TTL GND pin and two less ECL V_{CC} pins.

Pin Configurations (continued)

PQFP
Top View



E383-3

Selection Guide

	101E383–2	101E383–3
Maximum Propagation Delay Time (ns) (TTL to ECL)	2.5	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	3	4
Maximum Operating Current (mA) Sum of I_{EE} and I_{CC}	270	270

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

TTL Supply Voltage to Ground Potential ... −0.5V to +7.0V

TTL DC Input Voltage ..... −3.0V to +7.0V

ECL Supply Voltage V_{EE} to ECL V_{CC} ..... −7.0V to +0.5V

ECL Input Voltage ..... V_{EE} to +0.5V

ECL Output Current ..... −50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V_{EE}	TTL V_{CC}
Commercial	100K	101E	0°C to +85°C	−4.2V to −5.46V	5V ± 5%

ECL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	Temperature[3]	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	101E, R_L = 50Ω to −2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	101E, R_L = 50Ω to −2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C	−1810	−1620	mV
V_{IH}	Input HIGH Voltage	101E	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	101E	T_A = 0°C to 85°C	−1810	−1475	mV
V_{BB}	Output Reference Voltage	101E[4]	T_A = 0°C to 85°C	−1.40	−1.23	V
V_{CM}[5]	Common Mode Voltage	±V_{CM} with respect to V_{BB}			1.0	V
V_{DIFF}	Input Voltage Differential	Required for Full Output Swing		150		mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.		−0.5	170	µA
R_{PD}	Pull-Down Resistor	Connected from All ECL Outputs to V_{EE}	T_A = 0°C to 85°C	1.6	2.6	kΩ
I_{EE}	Supply Current (All inputs and outputs open)				−180	mA

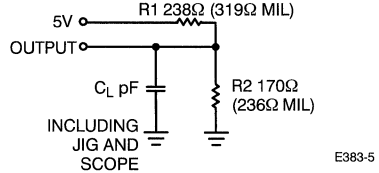
TTL Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions	101E383 Min.	101E383 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Max., I_{OL} = 16.0 mA		0.5	V
V_{IH}	Input HIGH Voltage[6]		2.0		V
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{CD}	Input Clamp Diode Voltage	I_{IN} = −10 mA	−1.5		V
I_{OS}[7]	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[8]	−180	−40	mA
I_{IX}	Input Load Current[9]	GND ≤ V_I ≤ V_{CC}	−250	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		90	mA

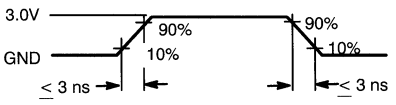
Capacitance[7]

Parameter	Description	Max.	Unit
C_{IN}[7]	Input Capacitance	4	pF
C_{OUT}[7]	Output Capacitance	5	pF

TTL AC Test Load and Waveform[10]

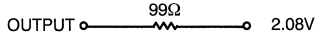


E383-5

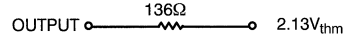


E383-4

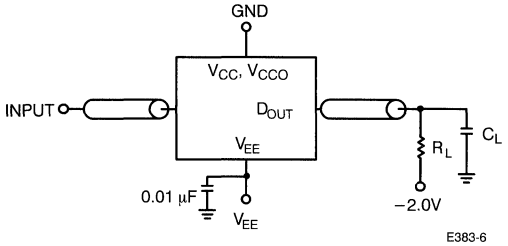
Equivalent to: THÉVENIN EQUIVALENT (Commercial)



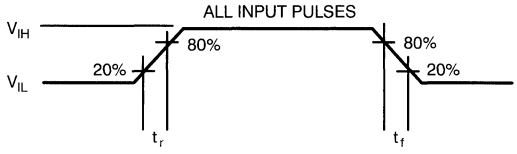
THÉVENIN EQUIVALENT (Military)



ECL AC Test Load and Waveform[11, 12, 13, 14, 15]



E383-6



E383-7

ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	101E383−2		101E383−3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns
t_{PHL}	Propagation Delay Time	D_n, $\overline{D}_n$ to Q_n	1	3	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	101E383−2		101E383−3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_{PHL}	Propagation Delay Time	D_n to Q_n, $\overline{Q}_n$	1	2.5	1	3	ns
t_R[7]	Output Rise Time	20% to 80%	0.35	1.7	0.35	1.7	ns
t_R[7]	Output Fall Time	20% to 80%	0.35	1.7	0.35	1.7	ns

Skew Time Switching Characteristics[7] (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

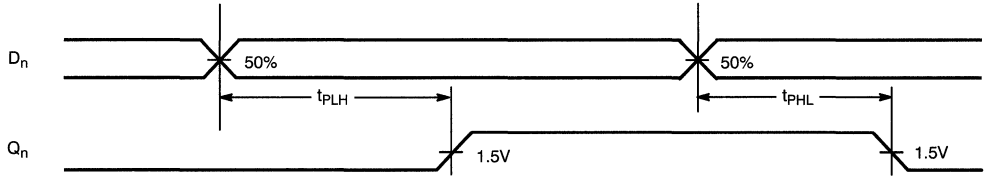
Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
t_{SKT}[7]	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		1	ns
t_{SKE}[7]	Data Skew Time TTL-to-ECL	$ECLQ_n$, $\overline{Q}_n$ to $ECLQ_{n+m}$, $\overline{Q}_{n+m}$		1	ns

Notes:

2. See AC Test Load and Waveform for test conditions.
3. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
4. Max. $I_{BB} = -1$ mA.
5. The internal gain of the CY101E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
6. These are absolute values with respect to device ground.
7. Characterized initially and after any design or process changes that may affect these parameters.
8. Not more than one output should be tested at a time. Duration of the short should not be more than one second.
9. I/O pin leakage is the worst case of I_{IX} (where X = H or L).
10. TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
11. $V_{IL} = -1.7$V, $V_{IH} = -0.9$V.
12. ECL $R_L = 50\Omega$, $C_L < 5$ pF (includes fixture and stray capacitance).
13. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
14. $t_r = t_f = 0.7$ ns
15. All timing measurements are made from the 50% point of all waveforms.

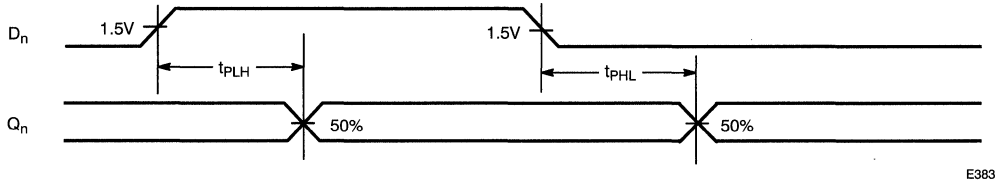
Switching Waveforms

ECL-to-TTL Timing



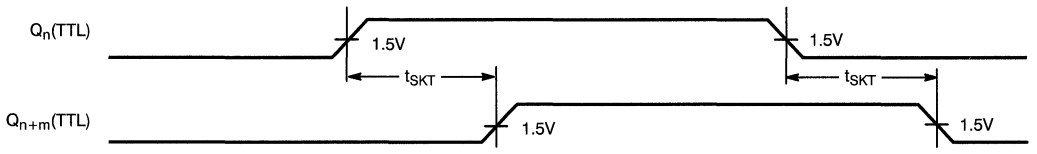
E383-8

TTL-to-ECL Timing



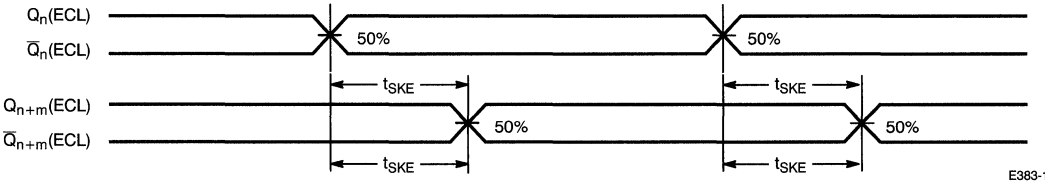
E383-9

Skew Test (t_{SKT})
TTL_{Qn}-to-TTL_{Qn+m}



E383-10

Skew Test (t_{SKE})
ECL_{Qn}, $\overline{Q}_n$-to-ECL_{Qn+m}, $\overline{Q}_{n+m}$



E383-11

ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL $\overline{D}_n$	TTL Q_n
Open[16]	Open[16]	L
L	H	L
H	L	H

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL $\overline{Q}_n$
L	L	H
H	H	L

Nominal Voltages

The CY101E383 can be used in dual ±5V or single +5V supply systems. The supply pins should be connected as shown in *Tables 1* and *2*. This connection technique involves shifting up all ECL supply pins by 5V. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding 5V. For example, if the termination is 50 ohms to −2V in a dual-supply system, the single +5V system should have 50 ohms to +3V. If the termination is a thévenin type, then the resistor tied to ground is now at +5V and the resistor tied to −5V is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL +5V supply lines will help to reduce the noise.

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−4.5V

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	+5.0V	+5.0V
TTL GND	0.0V	0.0V
ECL V_{CC}	+5.0V	0.0V
ECL V_{EE}	0.0V	−5.2V

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY101E383−2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383−2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY101E383−3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383−3NC	N80	80-Lead Plastic Quad Flatpack	

Note:
16. The ECL inputs will pull to a known logic level if left open.

Document #: 38−A−00023−F

PRELIMINARY

HOTLink™ Evaluation Board

Features

- 160 to 330 Mbps point-to-point serial data link
- Parallel-to-serial and serial-to-parallel I/O
- 10-bit-wide 8B/10B encode, decode or unencoded
- Full system diagnostics with Built-In-Self-Test (BIST)
- Compliant with ESCON®, Fiber Channel and ATM standards
- Compatible with Fiber Channel FC–0 specification (CY9266–C/T):
  - —25–TV–EL–S
  - —25–MI–EL–S
  - —25–TP–EL–S
- Compatible with Fiber Channel FC–0 specification (CY9266–F):
  - —25–M6–LE–I
- Development tool for proprietary networks
- Two-digit error display for BER analysis
- Multiple host interface:
  - —48-pin connector (IBM OLC–266™ compatible)
  - —60-pin edge connector
  - —60-pin two-row right-angle connector
- Easy to use for applications development

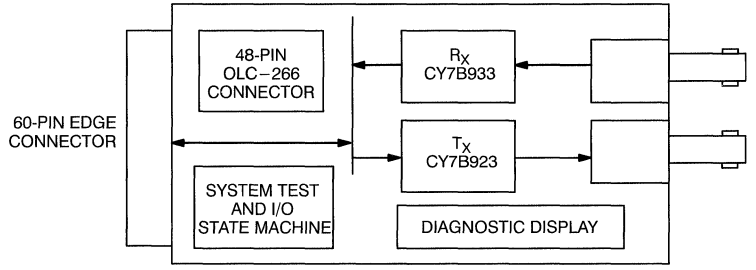


Figure 1. Copper Media Interface Evaluation Board CY9266–C

9266–1

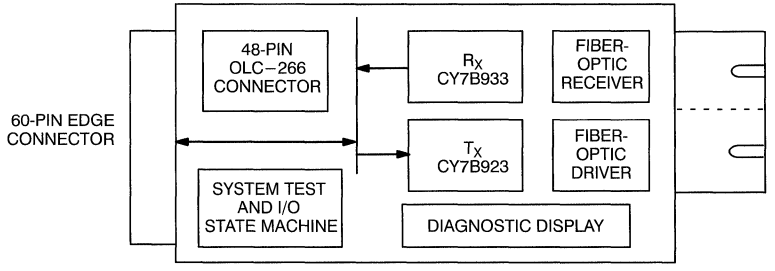


Figure 2. Fiber-Optic Interface Evaluation Board CY9266–F

9266–2

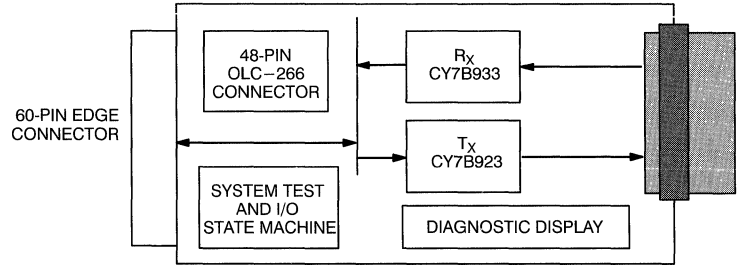


Figure 3. Twisted-Pair Interface Evaluation Board CY9266–T

9266–3

Functional Description

The HOTLink™ Evaluation Board (CY9266) is a system development tool that facilitates the design and evaluation of the Cypress HOTLink transmitter (CY7B923) and receiver (CY7B933) devices. The CY9266 Evaluation Board is offered with three serial media interface options: CY9266–C (copper), CY9266–F (fiber), and CY9266–T (twisted pair). The CY9266–C offers a low cost 1/4" coaxial connection, the CY9266–F interfaces with a longwave (1300 nm) LED optical transceiver and SC fiberoptics connector, and the CY9266–T is configured to support shielded twisted pair or twin axial cable that attaches through a 9-pin D-sub connector.

The CY9266 accepts data and control commands from the host via the parallel interface ports (available in three connectors). The 48-pin header connector allows interoperability with the IBM OLC–266 interface. The two 60-pin connectors are functionally equivalent. The vertical pin connector is used for probing and monitoring the appropriate signals, while the edge connector can be connected to a flat ribbon cable as a direct host communication interface.

In a typical point-to-point link, the host downloads parallel data to the CY9266 Evaluation Board. Parallel data can be formatted as pre-encoded 10-bit patterns or 8-bit data/special characters to be encoded by the HOTLink transmitter. The data is then encoded (optionally) and serialized by CY7B923 HOTLink Transmitter. Serial data is then transmitted via coax, twisted pair, or fiber.

In the receive operation, serial data is sent from a remote source (via copper/fiber/twisted pair) and transferred to the CY7B933 HOTLink receiver. The serialized data is converted to parallel and then optionally decoded. Parallel data is transferred to the host system along with various status and synchronizing signals. All I/O operations are performed between the host and the Evaluation Board using simple handshakes.

The CY9266 Evaluation Board can also operate in self-diagnostic mode and indicate errors in the serial transmission stream using a built-in two-digit, seven-segment LED display.

Typical Applications for the Evaluation Board include:

- HOTLink system development
- Telecommunication
- Remote data acquisition
- Processor-to-disk/peripheral communication
- Backplane extender
- Point-to-point video/image communications
- Point-to-point CPU/server communications
- High-speed data switching (TI Multiplier, etc.)
- Similar in function to IBM OLC-266 (single channel) and HP HOLC-0266™

Specification

Board Dimensions	3.0" x 4.0" (approx., plus media connector)
Two media types:	
CY9266–C	Coax connectors—BNC for transmit, TNC for receive
CY9266–F	Fiber optic module, single row or 4 row modules
CY9266–T	Twisted pair connector, 9-pin D-sub
Power Supply	+5V ± 5%
Maximum Clock Rate	33 MHz
Maximum Data Rate	330 Mbps
Parallel I/O	TTL
Serial I/O	Coax or twisted pair (CY9266–C/T) or Fiber optic with SC connector (CY9266–F)

Ordering Information

Ordering Code	Media Type
CY9266–C	Copper
CY9266–F	Fiber
CY9266–T	Twisted Pair
CY9266–FX	Fiber w/o optic module

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ESCON is a registered trademark of International Business Machines.
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HP HOLC–0266 is a trademark of Hewlett-Packard Corporation.

Frequently Asked Questions about HOTLink™

The following questions are frequently asked by customers who are evaluating HOTLink™ products. These cursory answers will serve as an introduction for each topic. Separate application notes cover these topics in more complete detail.

1. How far can HOTLink communicate over various media?

HOTLink has no intrinsic distance limit. The two issues that determine the distances over which data can be sent using HOTLink are: (1) the choice of interconnect media (fiber-optic cable, coaxial cable, twisted-pair cable, etc.); and (2) the jitter that accumulates or is injected while the data is in transit over the selected media.

HOTLink can drive all standard fiber-optic interface modules that support standard PECL interface signals. These electro-optical modules are suitable for communicating over distances from a few meters to several kilometers. Fiber-optic interconnect offers the longest distances and the lowest interference potential of all transmission media.

For lower-cost applications, HOTLink can directly drive wire transmission lines. The main distance determining factors when using wire links are related to the characteristics of the cable. Wire transmission lines have significant frequency-dependent attenuation that causes jitter as a direct function of the data rate and the media length. Uncompensated transmission line lengths are limited much more by jitter (and the jitter tolerance of the receiver) than by actual signal attenuation. The detrimental effect of jitter can be lessened with the addition of a suitable attenuation compensation filter that matches the attenuation characteristics of the cable. This filter trades receiver differential voltage amplitude for jitter reduction and increases the possible transmission distance. When using wire transmission lines, other issues beyond transmission distance often determine transmission line suitability. These issues include both radiated emissions and susceptibility to external disturbance that must be examined prior to selection of a link media type.

Some typical wire types and uncompensated transmission distances over which HOTLink can communicate are shown in *Table 1*. A simple compensation filter, built from passive components, can increase reliable transmission distance to more than twice these distances.

For more information see the application note "HOTLink Copper Interconnect—Maximum Length vs. Frequency."

Table 1. Coaxial Cable Types

Coaxial Cable	50Ω	75Ω	75Ω	93Ω
160 Mbaud	RG–58 A/U – 350 ft	RG–6 A/U – 900 ft	RG–59 A/U – 525 ft	RG–62 A/U – 675 ft
266 Mbaud	RG–58 A/U – 225 ft	RG–6 A/U – 600 ft	RG–59 A/U – 350 ft	RG–62 A/U – 400 ft
330 Mbaud	RG–58 A/U – 115 ft	RG–6 A/U – 500 ft	RG–59 A/U – 250 ft	RG–62 A/U – 325 ft

Table 2. Twisted Pair Cable Types

Shielded Twisted Pair	150Ω
160 Mbaud	IBM®–Type 1 – 550 ft
266 Mbaud	IBM–Type 1 – 350 ft
330 Mbaud	IBM–Type 1 – 275 ft

Unshielded Twisted Pair	UTP3	UTP5
160 Mbaud	140 ft	280 ft
266 Mbaud	80 ft	180 ft
330 Mbaud	60 ft	130 ft

2. Can the PECL inputs and outputs of HOTLink products be connected to ECL (–5.2V) products?

The +5.0V PECL inputs and outputs are directly compatible with true ECL (10K, 10KH, 100K, etc.) running on +5V power supplies. Connections between the HOTLink PECL I/O and ECL running on –5.2V is easily accomplished by capacitor-coupling the serial data lines. Details on this coupling technique are included in the Cypress application note "HOTLink Design Considerations."

3. What happens when the ECL inputs of the HOTLink Receiver are left open?

All of the ECL inputs on the HOTLink Receiver have internal pull-down resistors to assure that ECL-emitter follower outputs will see a positive input current (approximately 250 µA into the pin) at all normal ECL voltages. Thus, all single-ended ECL inputs (i.e., A/$\overline{B}$, SI, INB) will float to a logical LOW level. (These pull-downs will not sink enough current to act as the normal ECL output termination. They are only intended to prevent the emitter-follower oscillations caused by negative input-impedance that are possible in some less robust designs.) Open inputs will be interpreted as follows: A/$\overline{B}$ = LOW will cause the Receiver to accept data from the INB serial inputs; SI = LOW will cause the SO output to assume a LOW output state; INB = LOW will be interpreted as an input with no data (assuming A/$\overline{B}$ is also LOW). No data is interpreted as an error (RVS=HIGH & C0.7 in Encoded mode, and Qa–j outputs LOW in Bypass mode) and will cause the internal clock-synchronizer phase-locked loop (PLL) to track the REFCLK input frequency.

The internal resistor network used to pull the differential serial data inputs (i.e., INA± and INB±) will cause unconnected inputs to rest at approximately 2.0V. This resting voltage is a byproduct of the internal resistive attenuator used to enhance input-common mode range. If both inputs of a differential pair are left unconnected, the inputs will be in an undefined state and HOTLink receiver behavior will be unpredictable. Stray, non-differential noise that appears on these unconnected inputs will be amplified and interpreted as serial data. This will cause random parallel-data output changes, and may cause the PLL to wander or drift away from the REFCLK frequency. One input of an intentionally unused differential-pair should be terminated to V_{CC} through a 1–5 KΩ resistor to assure that no data transitions are accidentally created.

4. What special power-supply bypassing is required for HOTLink products?

HOTLink requires no special considerations for power-supply bypassing beyond that normally associated with high speed logic. This typically includes the use of a ground plane, a split V_{CC} plane, and multiple chip bypassing using RF quality capacitors. Each of the ground pins of a HOTLink IC should connect directly to the ground plane using short (<.25") traces and vias. All of the V_{CC} pins should connect to a V_{CC} pad under the HOTLink and then connect to the board V_{CC} through a single via. Connect one 22-nF capacitor for each V_{CC} pin directly from the pin to GND. For more information see the "Using Decoupling Capacitors" application note.

5. If the HOTLink Receiver is switched from INA to INB, how long will it take for the PLL to re-lock?

Assuming that the data on both INA and INB are within the ±0.1% frequency offset described in the HOTLink datasheet, the phase-locked loop (PLL) will acquire and lock to the new data stream within a few byte times. The exact time required involves statistical probabilities related to phase, frequency, and jitter, and cannot be exactly predicted. Empirical testing using normal data patterns shows that the time required to achieve absolute minimum phase error with the new data stream will vary from zero to about ten bytes.

An operational serial link will produce valid parallel data much earlier than the amount of time required to achieve minimum phase error, since instantaneous phase error is accommodated as jitter. The wide jitter tolerance offered by the HOTLink Receiver will minimize the time that data is incorrectly interpreted during phase acquisition. The larger problem facing a system protocol that allows switching of serial data streams, is byte synchronization (byte-framing). After the data-stream has been switched, it must be reframed. This requires that a K28.5 (or two K28.5s within five bytes if multibyte framing is enabled) must be received. The time that elapses before this happens depends on the system protocol and the timing of the data input switch. Correct data might not come out of the HOTLink Receiver for hundreds of byte times due to reframing regardless of speed of phase acquisition.

For more information, refer to the Receiver Data-Phase Acquisition Time section of the "HOTLink Jitter Characteristics" application note.

6. If the connection between the HOTLink Transmitter and Receiver is briefly interrupted, how long will it take for the PLL to re-lock?

The exact behavior of the HOTLink Receiver depends on the length and cause of the interruption. If the interruption is synchronous with the data (i.e., data bits disappear without any significant disturbance to the placement of the final few data transitions), and lasts for less than a few dozen bytes, it is probable that the PLL will relock on the very first bit. If the interruption is asynchronous (i.e., the timing of the final few transitions is disturbed) or if the synchronous interruption lasts longer than a few dozen bytes, the PLL will relock within the first one or two bytes after resumption of the data stream. If a long interruption occurs that is not synchronous to byte boundaries, the receiver may lose byte synchronization when the PLL relocks. In this case, the data will need to be reframed.

If the interruption is asynchronous, and the link interface allows noise to be injected into the serial inputs of the HOTLink Receiver, the time to relock the PLL becomes much harder to predict. If the noise that is being injected causes the PLL to track within its frequency offset limits (approximately ±0.25% of the REFCLK frequency) the PLL will reacquire in a few bytes (typically less than ten) after a good data stream reappears. If the PLL frequency has been moved to its offset limits by the input noise, it may take more than 60–70 bytes before the PLL locks to the good data. When the PLL hits the frequency offset limit, it will recenter itself at the REFCLK frequency and then attempt to lock to the data. While the PLL is out of lock (after experiencing a data stream interruption) the frequency of CKR will not wander beyond the offset limits.

For more information, refer to the Receiver Data-Phase Acquisition Time section of the "HOTLink Jitter Characteristics" application note.

7. If the connection between HOTLink Transmitter and Receiver is broken, what will come out of the receiver?

The exact behavior of HOTLink Receiver is difficult to predict when the serial data link is broken, since there are so many ways that the link itself can behave. The following behaviors are most common;

Bypass Mode–Reframe–OFF (RF = LOW) Clean link break with no extraneous noise input into serial inputs:

- CKR runs at REFCLK frequency.
- $\overline{RDY}$ is always HIGH.
- Qa–j all go LOW or HIGH depending on exact offsets built into transmission line termination. If the terminations are exactly matched, then Qa–j may be indeterminate.

Bypass Mode–Reframe–OFF Noise injection into serial inputs:

- CKR runs at REFCLK frequency $\pm$<1.0% (typically <$\pm$0.25%) and may wander between its range limits and the center frequency, randomly controlled by the injected noise.
- $\overline{RDY}$ may rest HIGH or may pulse randomly as false K28.5s are decoded from the noise.
- Qa–j will be indeterminate and may switch randomly.

Encoded Mode–Reframe–OFF Clean break with no extraneous noise input into serial inputs:

- CKR runs at REFCLK frequency.
- $\overline{RDY}$ pulses once per byte.
- Q_{0-7} indicate C0.7, SC/$\overline{D}$ is always HIGH, RVS is always HIGH if there are any offsets built into transmission line termination. If the terminations are exactly matched, then Q_{0-7}, SC/$\overline{D}$ and RVS may be indeterminate.

Encoded Mode–Reframe–OFF Noise injection into serial inputs:

- CKR runs at REFCLK frequency $\pm$<1.0% (typically <$\pm$0.25%) and may wander between its range limits and the center frequency randomly controlled by the injected noise.
- $\overline{RDY}$ may pulse randomly or once per byte.
- Q_{0-7}, SC/$\overline{D}$ and RVS may be indeterminate and may switch randomly.

Either Mode–Reframe–ON Noise injection into serial inputs:

- CKR runs at REFCLK frequency $\pm$<1.0% (typically <$\pm$0.25%) and may wander between its range limits and the center frequency randomly controlled by the injected noise. If RF has been HIGH for less than 2048 bytes, CKR will stretch randomly as false K28.5s are decoded from the noise. If RF has been HIGH for more than 2048 byte-times, CKR will only stretch when a multiple K28.5 string is decoded from the noise.
- $\overline{RDY}$ may pulse randomly or once per byte.
- Q_{0-7}, SC/$\overline{D}$ and RVS may be indeterminate and may switch randomly.

8. What is the correct operation of the RF input on the receiver? What is the minimum number of K28.5 characters required to insure proper framing? How can I tell if the receiver is framed properly?

Recovery of information from a serial data stream requires recovery of the bit clock (accomplished by the receiver PLL) and byte synchronization (accomplished by the receiver framer). The HOTLink framer is enabled or disabled by the RF input. In well behaved, standardized point-to-point protocols that are seldom switched, the control of the byte framer is managed as a service in the protocol controller. This service monitors when some error criteria have been exceeded, and goes to a framing subroutine. This framer service sets RF=HIGH while framing and LOW during normal message transactions.

In less well behaved systems, or systems that switch data sources often, it may be necessary to leave RF=HIGH for long periods (or permanently). Leaving RF HIGH opens the system to the problem of data corruption in the serial link caused by data patterns that happen to match the SYNC character. Since this Alias SYNC is unlikely to be aligned to the normal byte boundaries, it will cause the framer to align the parallel data to the wrong byte boundary resulting in long running data corruption. When RF is set HIGH, the receiver searches the received data stream for the bit pattern matching K28.5 (001111 1010 or 110000 0101). When it is found, the internal bit counter that controls byte translation is reset and the byte boundaries are aligned to the SYNC character.

HOTLink minimizes the alias SYNC problem by incorporating a multi-byte framer into the receiver. If RF has been HIGH for less than 2048 bytes, as would be typical in protocol driven framing control, a single K28.5 will align the byte boundaries. If RF has been HIGH for more than 2048 bytes, as would be typical in packet switched systems, the multi-byte framer is enabled and a single K28.5 is no longer sufficient to align the byte boundaries. To minimize the risk of alias SYNC, reframing is only allowed when two K28.5s are detected. These two K28.5s can be adjacent, or separated by exactly one, two, or three transmission characters. Any other spacing (i.e., non-integral character separation, or too far between K28.5) is assumed to be caused by transmission errors and will be ignored for framing purposes.

In addition to the upper level protocol error detection mechanisms common in communication links, the HOTLink Receiver offers several indications that a link is misframed. For example, in Bypass mode the $\overline{RDY}$ output pulses once per K28.5 detected. If RF is LOW, the only K28.5 that can be detected is one that is properly framed, and all others will just pass through as part of the received data. If the protocol in use has a maximum packet size or a minimum number of K28.5s, a simple retriggerable-one-shot can be used to detect when framing has been lost. In this example, if the one-shot is retriggered by the properly spaced K28.5s, then the data is properly framed. If the one-shot times-out, indicating that too much time had elapsed between SYNC characters, the data would automatically be reframed by raising RF till the next K28.5 indication.

Another example of HOTLink's indication of a misframed link occurs during Encoded mode. In Encoded mode, the RVS output serves a similar if not quite as obvious function. Normal data being sent over typical data links will have a very low error rate (e.g., bit-error-rates of $1x10^{-12}$ are quite common. BER=$1x10^{-12}$ $\approx$ one error per hour at 266 MHz). Therefore, if RVS is asserted often it can be assumed that the cause is misframing. Another retriggerable-one-shot could be used to detect this condition, or it could be detected by a simple synchronous state machine constructed in a PLD.

For more information, refer to the "HOTLink CY7B933 $\overline{RDY}$ Pin Description" application note.

9. What happens to the receiver's clock and parallel outputs when it reframes?

When a byte boundary realignment occurs, the external timing of the HOTLink Receiver changes to match the new byte alignment. Logic internal to the receiver guarantees that the clock outputs (CKR and $\overline{RDY}$) never glitch. They will stretch to the new byte alignment by adding to the HIGH or LOW time of the output pulse. The exact width of the high or low times of these clock outputs will depend on the exact timing of the realignment, but neither will ever be less than that of a nominal, normally running output (i.e., five bit times, each, minimum).

The data outputs (Q_{0-7}, SC/$\overline{D}$, and RVS) all change at a time determined by internal bit-rate counters, and are timed to assure maximum set-up and hold times to down-stream logic. Since realignment will reset the cycle of the internal counter, it is possible that the outputs will change, and then change again between clock edges when byte realignment happens. Since the clock-cycle stretches, this glitch on the data output remains outside the specified data-access and hold times.

For more information, refer to the "HOTLink CY7B933 $\overline{RDY}$ Pin Description" application note.

10. What does BIST do? How can I add BIST to my system without redoing all calculations for my critical interface timing? What functionality does the BIST test and guarantee?

The HOTLink built-in self-test allows a clear and unambiguous check of the HOTLink Transmitter and Receiver, and the serial link connecting them. As part of an offline diagnostic, this feature allows the user to insure that the interconnect link is fully operational and that any other diagnostic failure indications are caused by system blocks above the physical layer. BIST allows the HOTLink adapter card manufacturer to do a quick link quality test (or node quality test with the use of the loop-back functionality of HOTLink) without the necessity of bringing up a fully functional system to do link testing.

BIST is controlled by unused HOTLink data-enable inputs. Only a few connections and minimal external logic are necessary to add BIST to an otherwise complete system. (See the Cypress application note "HOTLink Built-In Self-Test.") BIST status indications appear on the $\overline{RP}$, RVS(Qj) and $\overline{RDY}$ outputs which are easily monitored by logic internal or external to the data flow controller.

In BIST mode, the HOTLink Transmitter generates a 2^9-1 (511 byte) pseudo-random pattern using its Input register configured as a Linear Feedback Shift register. The HOTLink Receiver compares the serial BIST data stream with identical BIST patterns generated in its Output register. All of the logic in the transmitter (except the input pins) and all of the logic in the receiver (including the output pins and their attached loads) are checked by BIST. All of the serial link interconnect components are exercised with normal data patterns, which are checked byte-by-byte in real time.

11. What fiber-optic components are compatible with HOTLink products?

All standard fiber-optic interface components are compatible with HOTLink products. The following table is a representative but not comprehensive list of optical interface manufacturers. A more complete list of vendors and products is included in the "HOTLink Design Considerations" application note.

AMP/Lytel Division
61 Chubb Way
P.O. Box 1300
Somerville, NJ 08876
(908) 685-2000

CTS Corp
1201 Cumberland Ave
West Lafayette, IN 47906–1388
(317) 463-2565

Hewlett-Packard
Components Division
370 West Trimble Road
San Jose, CA 95131
(800) 535-7449 or (408) 435-6342

Siemens Fiber Optic Components
20F Commerce Way
Totowa, NJ 07512
(201) 890-1606

Sumitomo Electric
Fiber Optics Corporation
777 Old Sawmill River Road
Tarrytown, NY 10591-6725
(914) 347-3770

12. What is the significance of the HOTLink claim of "no external PLL components"?

HOTLink Transmitter and Receiver have completely integrated the PLL clock multiplier and data separator functions. These functions are implemented with high-performance phase-locked loops (PLLs) that have been tuned for maximum performance and minimum system noise sensitivity. In competitive products that purport to offer similar functions, these PLLs are often implemented with external filter and frequency setting components with the goal of achieving maximum performance. But these very same external components are the largest cause of end-user complaints and random system failures because they expose the most critical analog signals in the circuit to the external noises that abound in normal systems. External components require critical, costly and time consuming printed circuit board layout as well as high-speed analog and digital design techniques that are unfamiliar to many system integrators. HOTLink products are designed and built using fully differential analog and digital circuits to give the lowest possible output jitter and highest possible jitter tolerance. There are no external components to compromise system performance in unexpected and unpredictable ways. For more information, refer to the HOTLink Transmitter Jitter section of the "HOTLink Jitter Characteristics" application note.

13. What is the intrinsic bit-error-rate of HOTLink Transmitter and Receiver?

HOTLink BER = Zero. HOTLink Transmitter and Receiver have no intrinsic failure modes. If their power is maintained and if the interface to the link connecting them has reasonable design margin, the total error rate will be exactly that of the interconnect media. Link error rates of $<<1x10^{-15}$ are common and easily achieved. Even with worst-case design derating and end-of-life derating, BER $<<1x10^{-12}$ presents no significant challenge.

The real question being asked is, "What will be my link BER when using HOTLink?" The answer to this question involves the design of the serial transmission link and the margins designed into it. HOTLink will not significantly degrade the BER of the link. For more information, refer to the "Understanding Bit-Error-Rate with HOTLink" application note.

14. How much jitter is created by the transmitter? How much jitter is created by the receiver? What is the significance of the HOTLink Transmitter requirement for a crystal-stable clock source?

The phase-locked loops (PLLs) in the HOTLink Transmitter and Receiver act like low-pass filters to jitter that is embedded in the data or clock signal source. For the transmitter, the signal source is the CKW input. Any jitter that appears at CKW will be passed unattenuated if it has frequency components below the natural frequency of the PLL filter (approximately 500 kHz). Frequency components above the natural frequency will be attenuated at about 6 dB/octave. Frequency components that fall very near the natural frequency of the filter will be slightly amplified (approximately 0.5 dB). These are the normal characteristics of a Type-2, second-order PLL filter. When the transmitter is fed by a low jitter clock source, typical output jitter will be less than 20 ps RMS and 200 ps peak-to-peak. It is possible to measure significantly more jitter than that which is actually present if the complete system is not well understood. A few hundred millivolts of V_{CC} noise, while insignificant to the logic of a normal system board, will add imaginary jitter to the measured output. This imaginary jitter appears because a single ended oscilloscope sees the waveform as if it were measured against a fixed threshold, while the differential serial interface sees V_{CC} noise as a common mode signal to be ignored (e.g., 100 mV of V_{CC} noise could create 100–200 ps of imaginary jitter). Likewise, the normal method of measuring peak-to-peak jitter, an infinite persistence scope trace, will show larger jitter than that contributed by the HOTLink Transmitter. Low frequency jitter (wander) in the oscillator, scope trigger, temperature, and voltage related delay variations will all contribute to the width of the stored scope trace. Delay variations include TTL threshold variations that cause apparent delay variation (e.g., 100 mV of TTL threshold change can cause 100–200 ps of apparent jitter).

The signal source for the receiver is the serial data stream and, like the transmitter, it passes the frequency components of received jitter that fall below the natural frequency of its filter (approximately 300 kHz to 1000 kHz depending on actual data transition density being received). Frequency components above the natural frequency will be attenuated and there is minor jitter peaking at about the natural frequency of the PLL. Since the characteristics of the input jitter will determine the jitter content on the receiver CKR output (the only place to directly measure Rx-PLL jitter) it is somewhat difficult to predict the output jitter. Maximum CKR output jitter is less than 200 ps (peak-to-peak) when the receiver is tracking normal data (BIST data is typical) that exhibits maximum tolerable peak-to-peak jitter. Jitter from normal data is wide-bandwidth, has a significantly high-frequency content, and can have peak-to-peak amplitude of up to about 90% of a bit time. If the serial data contains a significant low frequency jitter component (typical of crystal oscillators and some pulse generators) the output jitter measured on the CKR pin could be much higher. Jitter measurements at the receiver output can be more misleading than those associated with the transmitter serial outputs, since all measurements are made on TTL outputs.

The jitter characteristics mentioned above affect system performance in the following ways. Any low-frequency jitter (below the bandwidth of either transmitter or receiver PLL) will be treated as wander.

For purposes of the PLLs, wander (usually caused by low frequency power supply variations or temperature fluctuations within the timing ICs) will not reduce the system timing margins and will not contribute to bit-error-rate. Wander can affect system timing at interfaces where the transmitter clock source is used to clock information received from a receiver tracking data from another clock source. The variation in clock frequencies may violate set-up and hold times, the exact problems usually solved by FIFO memories in typical communication systems.

High-frequency jitter (at or above the natural frequency of the PLL filters) may contribute to BER. High-frequency jitter can be caused by the clock source, media transfer characteristics, or external noise. The recovered internal bit-rate clock will not track high-frequency jitter above the PLL natural frequency. High-frequency jitter, therefore, may cause a bit edge to move into the receiver sampling window causing the bit to be erroneously sampled (a bit error).

A suitable clock source should be selected with the above effects in mind. The only clock source guaranteed to offer the required stability and high-frequency specifications is a crystal oscillator. High-frequency jitter is minimal, and low-frequency wander is usually small and very low frequency. Frequency accuracy is easily guaranteed by mechanical means, and high accuracy devices are relatively low cost. Free-running resistor-capacitor (RC) oscillators, logic gate ring oscillators or inductor-capacitor (LC) oscillators include too much high-frequency jitter, experience wide frequency variation as a function of process and environmental conditions and thus are unsuitable for this application. See the "HOTLink Jitter Characteristics" application note for more information.

15. Can I use HOTLink for anything other than Fibre Channel/ESCON™ interconnect?

HOTLink has been designed to implement the required performance and specifications of Fibre Channel and ESCON, but has additional user features that encourage use beyond these specifications. The specific timing of the parallel I/O and clock signals allow efficient interconnect with typical generic controllers and FIFO memories. The built-in self-test and the included 8B/10B encoder functions allow users to implement custom protocols that are suitable to any data-movement application. HOTLink is compatible with all common link interconnect media and interfaces. It is a low-cost, low-power, high-performance tool that enables otherwise impractical system innovation. If there is data to move, HOTLink can carry it.

16. Is HOTLink compatible with ATM?

HOTLink is compatible with the 194.40 Mbaud (155.52 MBit/second), 8B/10B interface defined by the ATM Forum. It offers all of the data, special characters and framing behaviors described in the ATM Forum User-Network Interface (UNI) Specification. In particular HOTLink serves as the physical layer interface for the physical layer for 155 Mbps Interface (and its copper variant). When operating in this capacity, HOTLink runs at 194.40 Mbaud and uses the built-in 8B/10B encoder. All required data and special codes and responses are included in HOTLink.

17. Is HOTLink compatible with SONET?

HOTLink is not directly compatible with SONET for at least the following reasons:

- There are no standard SONET frequencies within its operating range of 160−330 Mbaud.
- HOTLink has a 10-bit unencoded interface, and SONET systems use an 8-bit interface.
- SONET requires a much slower rate-of-change of frequency during loss of signal than HOTLink can achieve.

The HOTLink Receiver can tolerate the long strings of zeros contained in SONET serial streams, and future designs will directly accommodate SONET specifications.

18. What is the latency through a HOTLink Transmitter and Receiver?

The input data is stored in the Transmitter Input register on the rising edge of CKW, so this becomes time-zero. Approximately 21 bit-times (i.e., 21 times the period of CKW ÷ 10) minus the t_{PD} of a TTL output buffer (approximately 10 ns) later, the first bit of that data will emerge from the OUTA±, B±, and C± pins. After the transit time of the serial link, which can be significant, that bit will appear at the receiver. Transit times for typical serial links include the propagation delay of the optical modules (typically 5–10 ns for the pair), if any, and the propagation rate in the link media (i.e., approximately 1 ns/ft in copper, and 2 ns/ft in multi-mode optical cable). Approximately 24 bit-times plus the t_{PD} of a TTL output buffer (approximately 10 ns) after the first data bit is received at the input of the receiver, it appears at the Q_{0-7} outputs. Eight bit-times later CKR rises and the data transfer is complete. The total latency of a HOTLink Tx/Rx pair is approximately link delay plus 45 bit-times.

19. Is there a VERILOG or VHDL model of HOTLink?

Logic Modeling offers full function logic models of both the HOTLink Transmitter (CY7B923) and the HOTLink Receiver (CY7B933). These models perform all of the normal chip functions including BIST, Encoded, and Bypass modes of operation. The models accurately model the "real" parts and have been validated by having them run the actual-chip design-simulation vectors and the outgoing-test vectors. Logic Modeling offers a wide variety of standard product logic models that run on various simulations platforms. They can be reached at:

Logic Modeling
19500 N.W. Gibbs Drive
P.O Box 310
Beaverton, OR 97006
Telephone (503) 690–6900
Fax (503) 690–6906

20. I need to estimate the reliability of HOTLink in my design. How many components does it contain?

Table 3. HOTLink Reliability Data

	CY7B923	CY7B933
Number of components	4285	7988
Number of transistors	3813	6855
Number of gates	2072	2960
Percent digital by gate count	85	90
Percent analog by die area	30	20
Die size	96 x 116 mils	126 x 131 mils

Built on Cypress Standard 0.8-micron BiCMOS. Designed for reliable operation at temperatures $-55^{\circ}C < T_j < 155^{\circ}C$. All pins characterized to withstand ESD >4400V (HBM). Wafer Fab Capability in San Jose, CA; Round Rock, TX.

HOTLink is a trademark of Cypress Semiconductor.
IBM is a registered trademark of International Business Machines Corporations.
ESCON is a trademark of International Business Machines Corporations.

Frequently Asked Questions about HOTLink™ Evaluation Boards

The following questions are frequently asked by customers who are using HOTLink™ Evaluation Boards. These cursory answers will serve as an introduction for each topic. Separate application notes cover these topics in more complete detail.

1. **How can I convert a CY9266–C (75Ω) Evaluation Board to use 50Ω cables? How can I convert a CY9266–C (75Ω) board to use 93Ω coax? How can I convert a CY9266–T (150Ω) STP (shielded twisted-pair) board to use 100Ω STP cables?**

   Conversions of the CY9266–C and CY9266–T boards to use transmission lines other than those shipped in the standard configurations is as simple as changing the transmission line termination resistors (R40 and R41) on the back side of the board. Carefully remove the ones currently on the board (presently 37.4Ω on a –C) and replace them with resistors with a value equal to half the transmission line characteristic impedance (i.e., 25Ω for a 50Ω cable). See *Table 1* for the values used for some common cable impedances. Extreme care must be used to avoid delamination of the board and damage to the traces by excessive heat during desoldering and resoldering.

   The change from higher to lower impedance transmission lines (e.g., 75Ω to 50Ω coax or 150Ω to 100Ω STP) may also require that the user change the transformer at T1. Changes from lower to higher impedance transmission lines usually do not require transformer changes. Alternatively, it may be desirable to add resistors at R54 and R55. (If these resistors are added, cut the built-in wire-traces that currently short the previously unused solder pads.) The higher currents involved in driving lower impedance transmission lines require either a higher inductance transformer or series current limiting resistors.

   As the impedance of the external cable changes, the drive level must vary to compensate. Part of the drive circuit, R61 & R62, needs to change to in order to vary the drive current available. See *Table 1* for the values required for various cable impedances. Changes in drive current will change the spectral characteristics of the souce signal and therefore the usable distance with a specific media type.

Table 1. Cable Impedance vs. R Values

Cable Impedance	R40 & R41	R61 & R62
150Ω	75Ω	392Ω
100Ω	50Ω	261Ω
93Ω	46.4Ω	243Ω
75Ω	37.4Ω	196Ω
50Ω	24.9Ω	130Ω

2. How can I convert a CY9266–C (75Ω) Evaluation Board to use 150Ω STP cables (like CY9266–T)? How can I convert a CY9266–T (150Ω) STP board to use 75Ω cables (like CY9266–C)?

Conversion of the CY9266–C and CY9266–T boards to use transmission lines other than those shipped in the standard configurations is as simple as changing the transmission line connectors and the transmission line termination resistors (see the answer to question 1).

For the CY9266–C: Carefully desolder and remove the BNC and TNC connectors installed at at J1 and J2. Replace them with the connector of choice using the mounting and solder terminal holes provided. WARNING: the CY9266–C board grounds the shield of the coax, and therefore one side of the transformer secondaries. Cut the traces leading to J1 and J2 on the solder side of the board (Under P1) to convert to balanced operation.

For the CY9266–T: Carefully desolder and remove the Sub-D installed at at P1. Replace it with the connector of choice using the mounting and solder terminal holes provided. The three traces running on the solder side from P1 to J1 and J2 were cut to unground the cable and allow balanced operation. Reconnect these wires for unbalanced cable connections.

Changing connectors often also involves changing the impedance of the cable used. See question 1 above about changing the resistor values for different values of cable impedance.

3. What types of Optical Modules are compatible with the CY9266–FX Evaluation Board?

We have tested and are shipping the CY9266–F Evaluation Board with Siemens, HP, and AT&T Optical Modules.

Table 2. Vendors for Optical Modules

Vendor	Part Number	Markings
CTS (formerly AT&T)	1408N	1408N ODL XCVR
HP	HFBR-5302	HFBR–5302
Siemens	V23806-A7-C2	Optical Data Link FC266 Transceiver
HP (formerly BT&D)	DLT1040-ST-2 DLR1040-ST-2	Separate TX & RX modules uses ST Fiber cabling
AMP/Lytel	269063–1	AMP SC Duplex Transceiver 270 Mb/s 269063-1

These modules may be purchased from the following vendors. Although this is not a complete list of Optical Module vendors, it will serve as a starting point for finding a module that may suit your needs:

AMP/Lytel Division
61 Chubb Way
P.O. Box 1300
Somerville, NJ 08876
(908) 685-2000

CTS Corp
1201 Cumberland Ave
West Lafayette, IN 47906–1388
(317) 463-2565

Hewlett-Packard
Components Division
370 West Trimble Road
San Jose, CA 95131
(800) 535-7449 or (408) 435-6342

Siemens Fiber Optic Components
20F Commerce Way
Totowa, NJ 07512
(201) 890-1606

Sumitomo Electric
Fiber Optics Corporation
777 Old Sawmill River Road
Tarrytown, NY 10591-6725
(914) 347-3770

4. Is this board compatible with (i.e., how do I use it with ...) the IBM/HP OLC card?

The HOTLink Evaluation Board is intended to allow easy evaluation of Cypress HOTLink parts and is not intended to replace the IBM® OLC card as a system interface (although it is capable of performing

this function). The OLC compatibility offered with these boards allows a familiar interface for those systems already compatible with the IBM cards.

OLC system interface signals in JP4 have the same timing and logical levels as the OLC card. Drive and loading are similar, but not identical. The function of the CY9266 Byte-Sync output differs from that of the OLC card when Sync-Enable is LOW. The OLC card will hold Byte-Sync LOW if Sync-Enable is LOW, while the CY9266 will set Byte-Sync HIGH for each byte containing a K28.5. When Sync-Enable is HIGH both boards will behave as the CY9266 does. The CY9266 behavior is convenient for implementing a simple "out of lock" indicator using timers that detect the interval between K28.5s (when Sync-Enable is LOW, a misframed K28.5 does not cause a Byte-Sync indication).

The CY9266 serial interface is incompatible with the IBM OLC card serial interface. The IBM OLC interface uses an 850-nm short wave laser and detector. The HOTLink Evaluation board uses off-the-shelf 1300-nm LED transmitters and detectors or copper transmission line interfaces. These various types are not compatible. For an operational link, use two compatible serial interfaces (i.e., two CY9266 boards of the same type, either −C, −T, or −F) for the two ends of the transmission link.

Note: The active signal level of the LOOPBACK signal, as implemented on the CY9266, is opposite that of an actual OLC-266 card. If this signal is under software control, it should be programmed to allow signal loopback when the signal is active LOW. For hardware controlled systems an external signal inversion is necessary, or the signal may be jumpered at JP1 for operation from the S1-7 DIP switch.

The physical size of the HOTLink Evaluation Board was chosen to be compatible with the two-channel version of the IBM OLC card. The X−Y dimensions are identical to those of the IBM product, but the thickness and the protrusion of the serial interface hardware is different from the IBM product.

The IBM OLC card includes plastic card guides and attachment clips that facilitate its use in production systems. The HOTLink Evaluation Board has none of these components since it is not intended for the same function.

5. Where can I get additional fiber-optic cables and accessories? Where can I get additional coaxial cables or STP cables?

We have located the following vendors of fiber-optic cables and accessories. You may contact them to receive further information about their offerings. The lists below represent only some of the available sources.

Fiber Instrument Sales Inc. 315-736-2206 315-736-2285 FAX	Nu-Power Optics 619-471-7131	FIBERTRON Tel: 714-871-3344 Fax: 714-871-5616	Belden Wire and Cable 800-BELDEN-1 order 317-983-5200

Additional coaxial and STP cables and other accessories may be found through:

Pasternack Enterprises 714-261-1920	First Source 408-371-1470	Newark 312-784-5100	Digi-Key Tel: 800-DIGI-KEY

6. How do I use this board to do bit-error-rate (BER) tests?

- Connect the board(s) with a suitable length of transmission line or fiber from the TX port of one board to the RX Port on another (or itself).
- Place the receiving board's Receiver in BIST mode by setting the RCV_BISTEN signal LOW. Ground the external pin marked RCV_BISTEN or set switch S1-5 to ON.

- Place the transmitting board's Transmitter in BIST Transmit mode by setting the XMIT_BISTEN signal LOW. Ground the external pin marked XMIT_BISTEN or set switch S1-1 to ON.
- Press the white reset button on the receiving board. The display should initially show a **.0.** . As the receiver finds an error in the data stream, it will show this with an increasing count. As the count exceeds 100, the overflow indicator will light up.
- The BER may be approximated by: 1 error/hour $\approx$ a BER of 1.1×10^{-12} using the 25.0-MHz oscillator shipped with the board.

7. How do I use this board to do transmitter jitter tests?

To achieve the best possible and most accurate transmit jitter measurements, the external environment of the HOTLink chips needs to have the lowest possible jitter to start. Common oscilloscopes and sources have so much jitter as to obscure the contribution of the transmitter. Additional sources of jitter on this board include:

- For the −C and −T versions: the transformer's frequency characteristics. For the −F version: the optical module.
- Layout of these boards has not been optimized for this testing, and does not have specific test connections built in.

With these items understood, a set-up to do an adequate test requires a quiet clock source and a digital oscilloscope such as the Tek 11801 or the HP 54720. The −F version without an optical module has the most convenient connections. Making connections to the −F board at location U4, all differential PECL signals, will allow the best measurements possible. (See the "HOTLink Jitter Characteristics" application note for information on how to measure jitter.)

Note: Transmit Jitter measured out of a −C or −T board includes significant crosstalk from the receive channel, coupled through the transformer. Ideally, measure Transmit Jitter with a quiet receive channel.

8. How do I use this board to do receiver jitter tolerance tests?

The ultimate performance of any serial link is determined by the performance of the receiver. The function of the receiver is to recover data from a (seemingly arbitrary) serial data stream. This data stream is translated several times, coupled to and though several non-linear devices and subjected to all manner of distortion. The receiver must accept this serial pulse train and recover a high-speed bit-synchronous clock, de-jitter it, and then separate the DATA from the CLOCK. Jitter tolerance is the typical term for the ability of the receiver to correctly recover the DATA and CLOCK in the presence of these many distortions. HOTLink Receiver jitter tolerance can be measured by connecting a suitable transmission media between the transmitter and receiver, and inserting a jitter generation source similar to that shown in the "HOTLink Jitter Characteristics" application note. By inserting measured jitter amplitudes and watching the RVS output of the receiver, jitter tolerance can be measured. Further details on the fabrication of the jitter generator and the measurement techniques required for accurate measurement of this injected jitter is beyond the scope of this note, but are covered in detail in the "HOTLink Jitter Characteristics" and "HOTLink Built-In Self-Test (BIST)" application notes.

9. How do I use this board to do HOTLink power supply noise immunity tests?

The layout and design of this board makes it difficult to test the power supply immunity of these parts. Power supply noise immunity testing requires injecting a signal into the power supply pins and observing the effect of this injected signal on the link. This requires a different layout to allow access to the power supply pins of the HOTLink chips without affecting the operation of the other parts on the board.

10. How do I use this board to do transmission-line tests?

To check for the maximum transmission-line length over which the HOTLink Evaluation Board can communicate, it is only necessary to connect the selected transmission line between the TX and RX ports of the HOTLink Evaluation Board. Using one board with the cable returning to its own RX port or two boards and cables for simultaneous testing in both/either directions of the transmission line will work quite well. The HOTLink Transmitter and Receiver BIST function serves the purpose of generating and testing the data so the user can check for an acceptable error rate without extra test equipment. Transmission lines can be extended or modified until the BIST error count indicates an unacceptable error rate. An error rate of approximately 1 error/hour $\approx$ a BER of 1.1×10^{-12} using the 25.0-MHz oscillator shipped with the board.

11. How do I use this board to do receiver-PLL acquisition-time tests?

Two kinds of receiver acquisition are measurable using this board. One kind shows how fast the receiver can recover from a phase hop, and the other shows how fast the receiver can acquire a datastream once the device is powered up with a stable REFCLK.

To measure the receiver recovery from a phase hop, connect a loopback cable with a delay just large enough to delay the data by almost one half a bit time ($\approx$2 ns for the shipped oscillator) with respect to the OUTC+ line that goes between the CY7B923 and the CY7B933. Then arrange a delayed synchronous switch signal into the A/$\overline{B}$ Select input of the receiver. Trigger this delay from $\overline{RP}$ and delay this pulse to a point in the data stream where the data stays HIGH for several bit times. By switching between the delayed and fast signal path, a phase hop can be created at the input to the receiver. Increase the delay until the receiver shows an RVS pulse during BIST testing. The receiver will properly recover data with a phase hop as large as $\pm 170°$. Invert the A/$\overline{B}$ select signal to get the other polarity of phase hop.

To observe the receiver recovery from a "lost" data stream, arrange the evaluation board to have an external REFCLOCK 0.1% faster or slower than the on-board oscillator. Configure the transmitter to only send K28.5s by either deasserting both the $\overline{ENN}$ and $\overline{ENA}$ signals, or constantly transmitting a C5.0 character in Encoded mode. With a clean pulse, switch the A/$\overline{B}$ select line to the B input. This will cause the receiver to see a lost and then found data stream. Using a delayed trigger, watch the CKR output with respect to the transmit clock. The two clocks will match frequency and stabilize in phase difference in less than 60 µs.

12. How do I use this board to do min/max frequency tests?

- Arrange the jumpers on the board so that the CKW and REFCLK use the same external clock input. Do this by removing the jumpers across pins IX–IY and GY–HY, then jumpering pins GX–GY and HX–IX. Apply an external reference clock to the XMITCLOCK pin on any of the interface connectors. Loopback the board either externally or by closing S1-7, which loops the board back on itself.
- Now enable the both the XMIT and RCVR BIST functions and the transmitter. The LED display should now show a stable number. Clear the count by pressing the RESET button S2.
- With the board set up as above, vary the frequency of the external reference clock from a nominal 20 MHz downward. As you approach the limits of operation, the board will start to indicate errors on the display. Clear the errors after setting a new frequency by pressing S2 again. The point in frequency where you do not see any BIST errors marks the edge of the frequency range. Change your frequency source upward toward 33 MHz and again clear the error indications until you achieve stable operation just below the high frequency limit.

Typical boards will operate as high as 40 MHz and as low as 12.5 MHz.

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Serializing High Speed Parallel Buses to Extend Their Operational Length

Introduction

Parallel buses are used in many designs for the purpose of moving data from one point to another. VME, ISA, EISA, VESA, PCI, SBus, and NuBus are some of the more familiar bus architectures. These buses are usually configured with a single bus master and multiple users, all communicating over a shared set of address and data lines. Some bus architectures, however, involve only two nodes on the bus, creating a point-to-point data link. Regardless of the architecture, the trend in bus design is for higher bandwidth achieved by increasing the width and transfer rate of the bus. When wide, high-speed, parallel buses are operated over distances of more than a couple of feet, problems can result. The source of these problems relates to the high-frequency signals interfering with each other over the long parallel conductors of the bus. This application note uses the UTOPIA bus as an example of how to serialize a high speed parallel point-to-point bus in order to allow the bus to operate over any distance.

The topics covered in this application note are as follows:

1. The UTOPIA Bus
2. UTOPIA Applications
3. Problems with Parallel Buses
4. The Serial Solution
5. Serial Links and HOTLink™
6. Serializing the UTOPIA Bus
7. Round Trip Latency
8. The UTOPIA Extender
9. Conclusions

The UTOPIA Bus

A good example of a high speed point-to-point parallel bus is the Universal Test and Operations Physical Interface for ATM (or UTOPIA). UTOPIA is used in ATM (or Asynchronous Transfer Mode) applications. ATM is a network protocol that has grown out of the need for a worldwide standard to allow interoperability of information, regardless of the "end-system" or type of information. With ATM, the goal is one international standard.

ATM is a method of communication which can be used as the basis for both LAN and WAN technologies. When information needs to be communicated, the sender negotiates a "requested path" with the network for a connection to the destination. When setting up this connection, the sender specifies the type, speed, and other attributes of the call, which determine the quality of service. Thus ATM is a switch-based technology (see *Figure 1*). By providing connectivity through a switch (instead of a shared bus) ATM delivers several benefits including dedicated bandwidth per connection, higher aggregate bandwidth, well-defined connection procedures, and flexible access speeds.

Using ATM, information to be sent is segmented into a fixed-length cell, transported to and reassembled at the destination. The ATM cell has a fixed length of 53 bytes. Being fixed-length allows different traffic types on the same network. The cell itself is broken into two main sections, the header and the payload. The payload (48 bytes) is the portion that

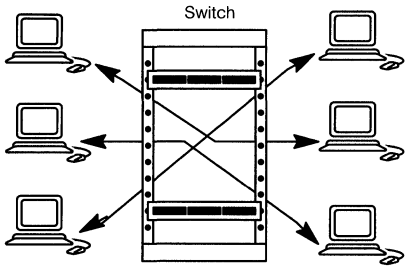


Figure 1. ATM Connections Through Switch

carries the actual information—either voice, data, or video. The Header (5 bytes) is the addressing mechanism (see *Figure 2*).

ATM closely follows the International Standards Organization's (ISO) Open Systems Interconnection (OSI) model for communication. This model breaks down any communication process into several sub processes arranged in a stack (see *Figure 3*).

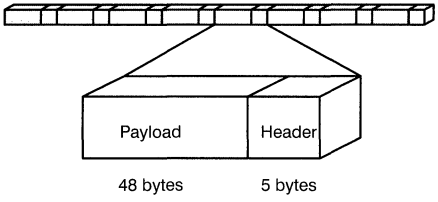


Figure 2. ATM Cell Format

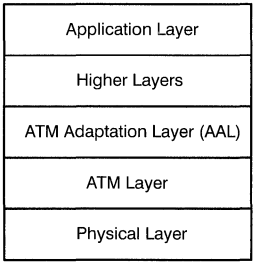


Figure 3. ATM Protocol Stack

Each layer of the "protocol stack" provides services to the layer above that allow the top most processes to communicate. The idea is that two different devices, using hardware and software from different vendors, but still conforming to the model, can communicate over an ATM network. The layers of the protocol stack can be thought of as modules in software code. Each layer performs a specific function and must provide data to other layers according to a specified interface. However, how that layer accomplishes its task is immaterial. Thus, layers in the stack can be updated without affecting the communication model.

The UTOPIA bus is a standard defined by the ATM forum for moving data between the physical (or PHY) and Asynchronous Transfer Mode (or ATM) layers in the ATM protocol stack. The PHY layer interfaces directly to the network media (i.e., fiber, twisted pair, etc.) and also handles "transmission convergence" (that is, extracting the ATM cells from the transport coding scheme). The ATM layer processes the cell headers and directs routing. The signals used by the UTOPIA bus are shown in *Figure 4* and described in *Table 1*.

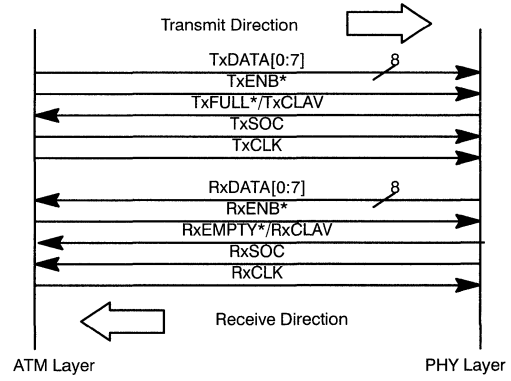


Figure 4. UTOPIA Signals

Table 1. UTOPIA Signals

Signal Name	Description
TxDATA[0:7]	Data lines for transmit (from ATM to PHY layer)
TxENB*	Indicates data on this cycle is valid
TxFULL*	Indicates Tx FIFO on PHY layer can only accept 4 more bytes (used only in Octet Level Handshaking)
TxCLAV	Indicates Tx FIFO on PHY layer is capable of storing an entire cell
TxSOC	Indicates data on this clock cycle is the start of a cell
TxCLK	Clock for Tx signals and data
RxDATA[0:7]	Data lines for receive (from PHY to ATM layer)
RxENB*	Indicates data on this cycle is valid
RxEMPTY*	Indicates Rx FIFO on PHY layer is empty (used only in Octet Level Handshaking)
RxCLAV	Indicates Rx FIFO on PHY layer is currently storing an entire cell
RxSOC	Indicates data on this clock cycle is the start of a cell
RxCLK	Clock for Rx signals and data

UTOPIA Applications

The UTOPIA bus is present in any ATM system that makes use of the ATM and PHY layers. Typical applications utilizing UTOPIA include Network Interface Cards and ATM switches. The ATM switch application for UTOPIA is of particular interest. Many switches are built using a rack mounted architecture as shown in *Figure 5*.

In this type of switch, individual shelves of the rack are dedicated to PHY layer circuits, and others to ATM layer circuits. Thus the UTOPIA bus is used to move the data between the different shelves of the switch. Usually, the interconnect between the

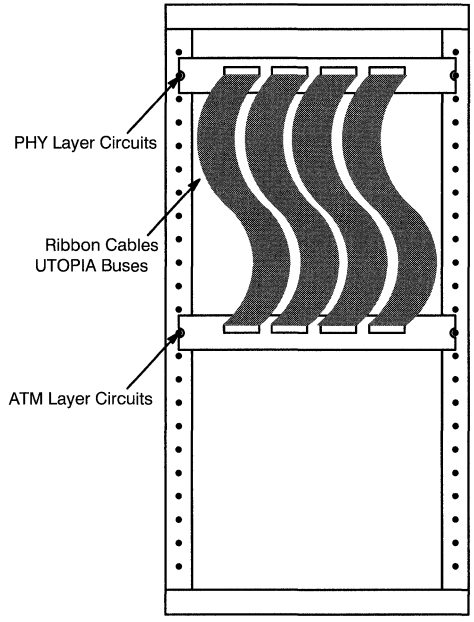


Figure 5. UTOPIA in a Rack Mount Switch

shelves is a simple multi-conductor ribbon cable. Since the shelves can be fairly far apart, the ribbon cable required to connect the shelves can be anywhere from 1 to 6 feet in length.

Problems with Parallel Buses

The difficulty with the use of ribbon cable for the UTOPIA switch application is related to the width and bandwidth requirements of the bus, combined with the uncontrolled impedance of the ribbon cable. These three characteristics can lead to skew across the signals of the UTOPIA bus as shown in *Figure 6*.

Note the skew shown in *Figure 6* has violated the set-up and/or hold times of the UTOPIA bus at the load end. Therefore, data communication over the bus will be corrupted. This effect is typical when high-speed parallel buses are driven over long distances. One possible solution is to drive each line of the bus differentially, but this also has the disadvantage of increasing the already bulky ribbon cable, and it is not guaranteed to solve the skew problem (skew can

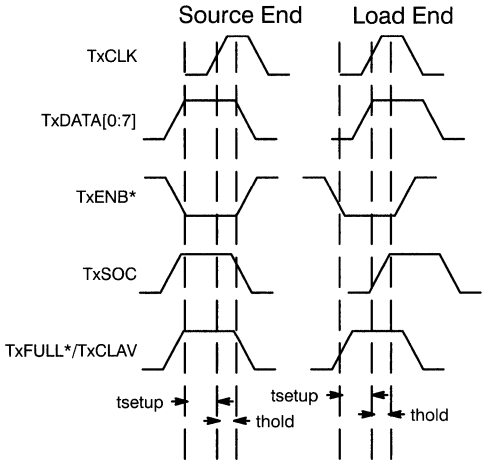


Figure 6. Effect of Skew on UTOPIA Bus

still result from differences in propagation delays for each signal through its respective differential driver/cable/receiver).

The Serial Solution

A good solution to the skew problems described above is to transmit the parallel bus data as a serial data stream. Transmitting the data serially requires a parallel-to-serial conversion of the UTOPIA data at the source end and a corresponding serial-to-parallel conversion at the load end. With such a scheme, the skew problems associated with operating a high-speed parallel bus over long distances are eliminated. In addition, the cable size is reduced from a multi-conductor ribbon cable to a two-conductor serial cable (such as coaxial cable).

The method by which a serial data transfer eliminates the skew problems associated with parallel buses is related to how serial links operate. Although some "serial" communication systems utilize more than one conductor (e.g., RS232), more serial links provide for transmission of only one signal. Note that to transmit one signal over copper media requires two conductors. This transmission can be either single-ended (requiring one conductor for the signal and one reference or ground) or differential (requiring two conductors for one signal). Both clock and data information must be included in this single signal. To accomplish this clock and data multiplexing function, serial links make use of special encoding schemes and use clock recovery circuits. The clock recovery circuits rely on the special characteristics of the data encoding scheme in order to recover or generate a clock of the same frequency and phase (with respect to the serial data) as the clock used to shift the data onto the serial link. The serial-to-parallel converter then uses this recovered clock to resample or retime the serial data before placing this data into a parallel word register. When this register is full, the serial-to-parallel converter presents the data in the register (in a parallel format) along with a parallel word clock (generated by dividing down the recovered serial clock). Thus, there is no skew between the clock and parallel data.

The main advantages of a serial link over a parallel bus are: (1) the clock is embedded with data, thus there is no skew between clock and data signals, (2) the distance over which the serial link is operated can be changed and the link will remain operational, (3) the transfer rate of the serial link can be scaled up and the link will remain operational, and (4) the cables required are smaller in size.

Serial Links and HOTLink™

The Cypress HOTLink™ chipset performs all of the functions shown in the simplified block diagram in *Figure 7*. The CY7B923 HOTLink Transmitter serves as the serializer while the CY7B933 HOTLink Receiver operates as a deserializer. In the HOTLink chipset, clock multiplication and clock recovery are accomplished using Phase Locked Loops (or PLLs). PLLs are closed loop control systems which align an output waveform in phase and frequency with an input waveform. Block diagrams of PLLs performing clock multiplication and clock recovery are shown in *Figure 8*.

PLLs operate by constantly comparing their output waveform with their input (or reference) waveform. Deviations in phase or frequency are then corrected at a rate governed by the Low Pass Filter (LPF). A wide bandwidth LPF allows a PLL to track high-frequency phase deviations between the reference and the output waveforms. A narrow bandwidth LPF dictates that the PLL rejects high-frequency phase

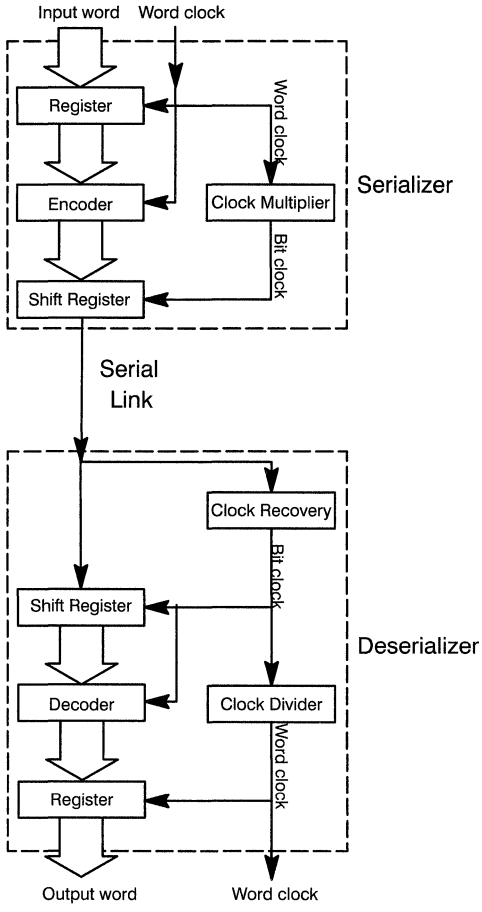


Figure 7. Architecture of a Serial Link

deviations between the reference and output waveform. Ideally, an input waveform would have a transition at a regular periodic rate, thus allowing the PLL to check its alignment constantly. However, such a signal would contain no information (essentially the link would be composed of one baseband frequency and its harmonics) and is not useful for data communication. Actual serial streams do not have data transitions at strictly periodic intervals. Instead, there are often "runs" of consecutive ones or zeros, which result in short periods where the serial stream has no transitions. The lack of transitions in the serial stream can cause the clock recovery PLL to fall out of phase lock, and eventually out

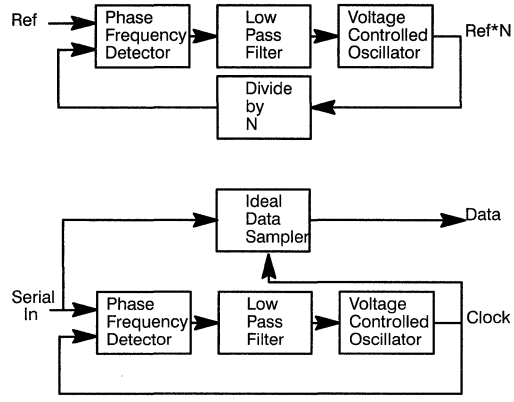


Figure 8. Multiplication and Clock/Data Recovery PLLs

of frequency lock. In order to reliably perform clock recovery with PLLs, the serial data needs to be encoded in such a way as to ensure there are frequent transitions (either from HIGH to LOW or LOW to HIGH) in the serial stream. These transitions cannot be ensured when sending unencoded data, since a user is free to send any data pattern. Some serial patterns like 00000000 contain no transitions and therefore could be transmited indefinitely resulting in a serial link without any transitions.

The HOTLink chipset utilizes an encoding scheme known as 8B/10B. This code takes in a 8-bit data word and converts it into a 10-bit transmission character. The transmission characters are chosen such that their run length is limited to 5 consecutive ones or zeros. With this encoding scheme, the HOTLink Receiver's clock recovery circuit can maintain lock and recover the clock from the serial data stream.

Serializing the UTOPIA Bus

Operating the UTOPIA bus over a serial link is accomplished using the architecture shown in *Figure 9*.

The basic block functions are as follows: On the ATM side, the serializer converts the parallel UTOPIA transmit data into a serial stream, embedding the UTOPIA transmit clock with the data. The deserializer converts the serial receive stream (from the PHY layer) back into parallel data and a receive clock. The First In First Out (FIFO) memory works

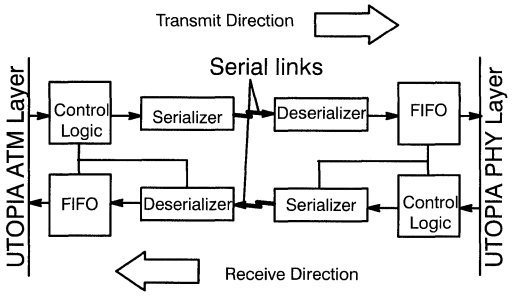


Figure 9. UTOPIA Serializer Block Diagram

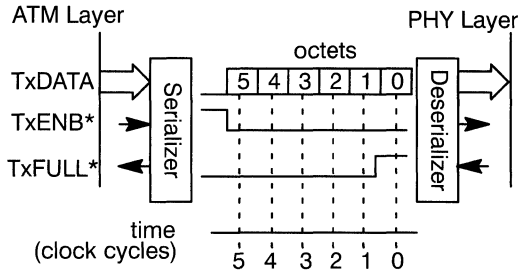


Figure 10. Round Trip Latency Example

as an elastic buffer, queuing the parallel receive data until the ATM layer parallel interface is ready to accept the data. The control logic provides control for all of the blocks. On the PHY side, the blocks perform similar functions. The serializer converts the parallel receive data into a serial stream, embedding the UTOPIA receive clock into the data. The deserializer converts the serial transmit stream (from the ATM layer) back into parallel data and a transmit clock. The FIFO provides buffering for the transmit interface, and the control logic manages all of the blocks.

Round Trip Latency

The purpose of the FIFO in the serialized UTOPIA architecture is to account for latency in the system. To understand the importance of the FIFO, consider a design which implemented a serialized UTOPIA bus. For UTOPIA transmits, there are two handshaking signals TX_FULL* (sourced at the PHY layer) and TX_ENB* (sourced at the ATM load). A transfer is initiated when TX_FULL* goes HIGH, followed by TX_ENB* going LOW and the UTOPIA data placed onto the bus. If TX_FULL* should go LOW at any time, the transfer must stop (according to the UTOPIA specification) within four write cycles. However, since TX_FULL* is sourced at the PHY layer and sampled at the ATM layer, there is a time delay for any change of state of TX_FULL* at the PHY layer to be recognized at the ATM layer. *Figure 10* shows an example of the timing relationships of the critical UTOPIA signals. This time delay is the latency through the serializer, serial media, and deserializer. There is a similar latency with respect to the TX_ENB* and TX_DATA from the ATM layer to the PHY layer. A problem arises if a transfer is in progress and TX_FULL* goes LOW. The figure shows that the transfer began successfully and several octets were placed onto the serial link. However, at clock cycle 1, the TX_FULL* signal on the PHY side went LOW, indicating that the PHY layer is full. According to the UTOPIA specification, the transfer must stop (TX_ENB* must go HIGH) within four byte times of TX_FULL* going LOW. In order for TX_ENB* to go HIGH, the ATM layer must recognize the change in state of TX_FULL*, but there is a delay from the PHY layer to the ATM layer. During this delay, the ATM layer may have already sent out too many bytes (in *Figure 10* five bytes are shown as being transmitted before TX_FULL* is recognized at the ATM layer). Since it is possible to not recognize the change in state of TX_FULL* within the four byte specification, there is the potential for data loss at the PHY layer.

Note that the latency in the link that is the source of the problem in the above example is *not* entirely due to the serializer and deserializer. If the serial link itself is long enough, the mere time delay required for the electrical pulses to travel down the link may be enough to cause the problems described above.

The latency issue is solved by buffering the data coming out of the deserializer. A FIFO is an adequate buffer for this application. With the FIFO buffer, the effects of the link latency are corrected. When the PHY layer UTOPIA interface indicates it has no more room for data, the FIFO can store the octets that are sent by the ATM layer before it receives the TX_FULL* signal. The data can then be

read out of the FIFO when the PHY layer UTOPIA interface is ready.

The UTOPIA Extender

Following the block diagram shown in *Figure 9*, and the hierarchical schematics shown in Appendix A, a serialized UTOPIA bus can be implemented. With the bus serialized, it can essentially be extended to any length, thus the design results in a "UTOPIA extender." The major components required to implement such a design are shown in *Table 2*.

Table 2. Cypress UTOPIA Extender Components

Generic Part	Cypress Part
Serializer	CY7B923 HOTLink Tx
Deserializer	CY7B933 HOTLink Rx
FIFO	CY7B451 512x9 clocked FIFO
Control Logic	CY7C371 32-macrocell Flash PLD

The "Top Level" hierarchical schematic shows a generic breakdown of the entire design. The "ATM Layer UTOPIA Extender" block implements all of the functions at the ATM layer interface necessary to serialize the UTOPIA bus. Likewise, the "PHY Layer UTOPIA Extender" block implements all of the functions at the PHY layer interface. Between these two blocks are two serial links over which the serialized UTOPIA bus operates. A system level application of the UTOPIA Extender is shown in *Figure 11*.

Both the "ATM" and "PHY Layer UTOPIA Extender" blocks have additional hierarchical schematics associated with them. Within these lower-level hierarchical schematics are additional blocks that show more detail than the previous levels. Each block performs a specific function necessary for the operation of the entire design. Some functions are common to both the "ATM" and "PHY Layer UTOPIA Extender" blocks, such as the "Media Interface" block. The "Media Interface" block performs the function of interfacing the transmit and receive electrical signals (comprising the serial links carrying the serialized UTOPIA bus) to the specific media interface used in the design (in this case to coaxial cable). The "Media Interface" schematic contains termination networks and transformers used to interface the transmit and receive serial signals to the coaxial cable.

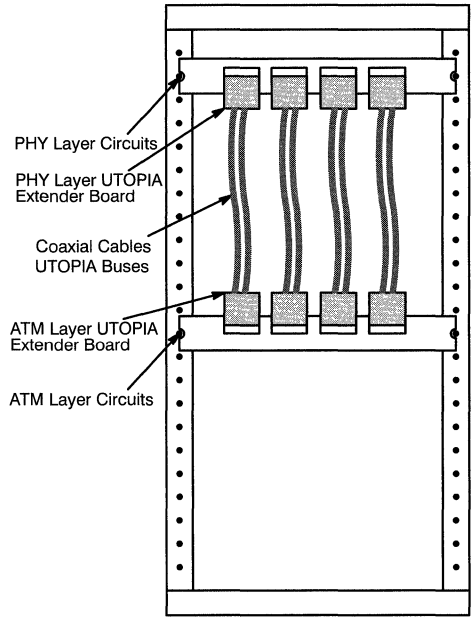


Figure 11. UTOPIA Extender in a Rack Mount Switch

The "ATM" and "PHY UTOPIA Logic" blocks contain all of the circuits used to serialize the UTOPIA bus. These blocks contain the serializers, deserializers, FIFOs, and PLDs used to implement the logic for the UTOPIA extender.

The operation of the UTOPIA extender, implemented in the "ATM" and "PHY UTOPIA Logic" blocks, can be broken down into two modes. The first mode, or Steady State mode, moves the UTOPIA transmit and receive data between the ATM and PHY layers, and handles generation of the necessary control signals. The second mode, or FIFO State Update mode, handles the control of the buffering FIFOs assuring that no data is lost due to overfilling of these buffers. This mode also handles the case of the CLAV signals going inactive, indicating the UTOPIA interface cannot accept more

data. Regardless of the mode of operation, the basic link operation revolves around the Cell Level Handshaking (or CLH) protocol.

The main characteristic of CLH is that once a cell transmission begins, all 53 octets of the cell are sent in succession on consecutive clocks. In this mode, back to back cell transmissions are also possible. For this design, however, back to back cell transmissions will not be allowed (this is accomplished through special considerations in the UTOPIA control logic). A gap will be forced between all cells. This gap serves two purposes. The first is to allow for the communication of the CLAV control codes from the PHY layer to the ATM layer and also to update the status of the buffering FIFOs. The second reason for the gap is to allow for easy generation of the SOC signal at the load end of the serial link.

The Steady State mode of operation for the UTOPIA extender is defined as the condition when neither buffer FIFO is overfilled. When in this mode, there is a minimal amount of control logic necessary to implement the extender. As an example, consider a UTOPIA transmit (defined as data movement from the ATM to the PHY layer). When a 53-octet cell becomes available on the ATM layer side, it is immediately placed into the HOTLink transmitter and sent over to the PHY side. Following the first octet, the remaining 52 octets of the cell are sent consecutively. Following transmission of the 53rd byte, the link pauses to implement the forced cell gap. During this pause, the HOTLink Transmitter is disabled and sends idle characters (called K28.5 or "Commas") across the link. If there is another cell available from the ATM layer, it is sent across after the cell gap. If no data is available, the link remains disabled. The flow of data under the steady state mode is shown in *Figure 12*.

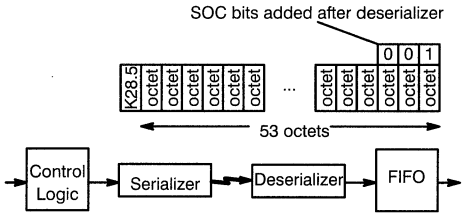


Figure 12. Transmission Data Flow

Upon receiving the octets from the ATM layer, the output of the HOTLink Receiver is immediately placed into the buffering FIFO. In addition, when the first octet out of the receiver is sensed (by taking advantage of the forced gap between cells), an additional bit, serving as the TX_SOC signal, is placed into the FIFO coincident with the first octet. The remaining 52 octets are also placed into the FIFO, but without the TX_SOC bit set. The TX_ENB* signal to the UTOPIA interface is then generated from the TX_CLAV signal and the FIFO status signals. The PHY UTOPIA interface directly reads the output of the buffering FIFO. Data movement in the UTOPIA receive direction is similar.

The other mode of operation is FIFO State Updating. This mode basically serves to handle the case when the CLAV signals change state. That is, if the TX_CLAV is deasserted, no data will be read out of the PHY side buffering FIFO. Eventually, this FIFO will fill beyond a check point and a code will be sent back to the ATM layer side indicating no more data should be sent until the FIFO is read beyond a certain level. The operation of this mode requires some additional control logic. Again, consider the case of UTOPIA transmission. A FIFO state update begins when the control logic on the PHY layer side detects that the buffering FIFO has filled beyond a predefined level. The control logic then waits for a pause in the data stream going back to the ATM layer side (remember a gap is forced between successive cells). During this pause, the control logic inserts a "FIFO Full" control code into the HOTLink transmitter in place of one of the comma characters (see *Figure 13*). This FIFO Full code travels across the link back to the ATM layer side. The ATM layer control logic then interprets the FIFO Full code and deasserts the TX_CLAV signal at the ATM layer UTOPIA interface, thus stopping transmission on the next cell boundary.

Eventually, the PHY layer FIFO will empty past another predefined level, thus indicating data transmission can begin again. The control logic on the PHY layer side then waits for a pause in the data stream back to the ATM layer side, and inserts a "FIFO Not Full" code in place of one of the comma characters (see *Figure 14*). This code travels down the link back to the ATM layer side where it is inter-

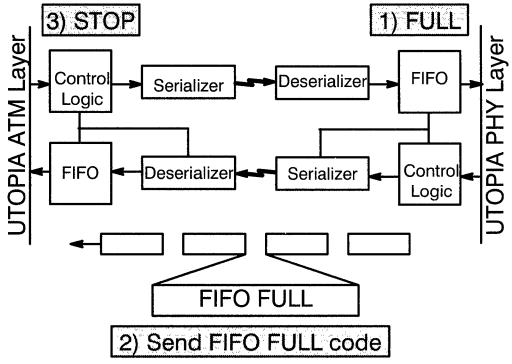


Figure 13. FIFO State Updating, FIFO Full

preted by the ATM layer control logic. The control logic then asserts the TX_CLAV signal to the ATM layer UTOPIA interface allowing data transmission to resume. Operation then reverts back to the Steady State mode.

The remaining blocks in the UTOPIA Extender ("ATM UTOPIA and Processor Interface," "PHY UTOPIA and Processor Interface," and "Framer Processor Interface") are used to interface the "ATM" and "PHY UTOPIA Logic" blocks to the UTOPIA bus of the ATM and PHY Layer Circuits as shown in *Figure 11*. In general, these remaining blocks contain connectors with pinouts specific to the particular ATM/PHY layer circuits used in the system. In addition, some ATM and/or PHY layer circuits require additional circuits to configure and/or monitor their operation. Thus the actual design of the "ATM UTOPIA and Processor Interface," "PHY UTOPIA and Processor Interface," and "Framer Processor Interface" blocks differs depending on the unique ATM and PHY layer circuits used in the system.

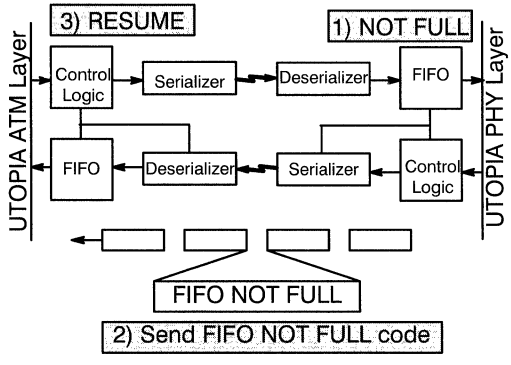


Figure 14. FIFO State Updating, FIFO Not Full

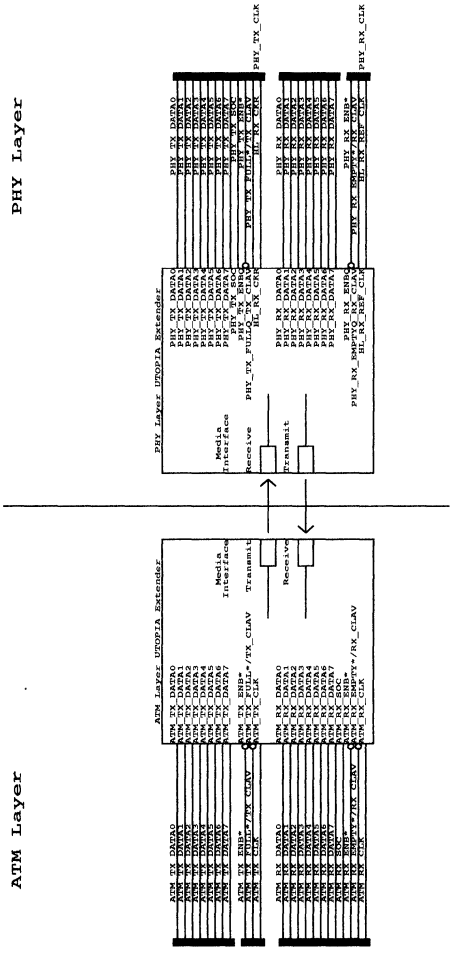
To exemplify a system using the UTOPIA Extender, a complete design of the PHY Layer is shown in the schematics (that is, only the "PHY Layer UTOPIA Extender" is shown fully implemented). The PHY Layer Circuit used was a Duke Communications DC-202® SONET/ATM UNI Transceiver Module. Thus the "PHY UTOPIA and Processor Interface" block was tailored to interface to the DC-202. In addition, the "Framer and Processor Interface" block was required to configure the DC-202 for proper operation. VHDL code for the "Framer and Processor Interface Block" is included in Appendix B. Also included in Appendix B is VHDL code implementing the algorithms for the "PHY UTOPIA Logic" PLD.

Conclusions

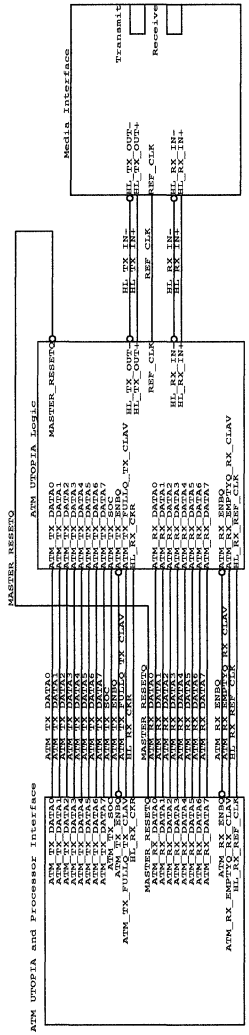
This application note has shown that signal skew across a ribbon cable can limit the operational distance of high-speed parallel buses such as UTOPIA. Serial links can operate over longer distances since they are not susceptible to the skew effects that limit parallel buses. This application note describes the design of a serialized parallel bus called the "UTOPIA Extender." Implementation of the UTOPIA Extender requires only a minimal amount of logic, with most of the work being performed by a high-speed serial-link chipset such as the Cypress HOTLink chipset.

HOTLink is a trademark of Cypress Semiconductor.
DC-202 is a registered trademark of Duke Communications.

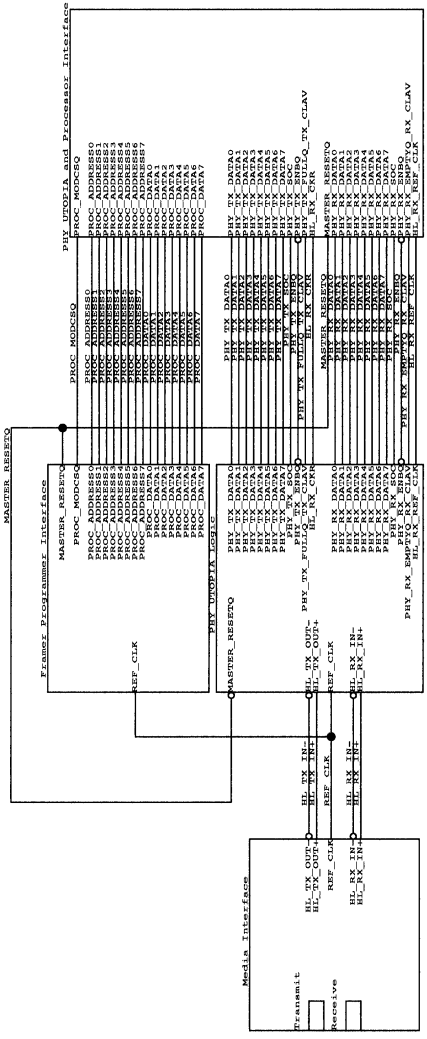
Appendix A. Hierarchical Schematics
Sheet 1 of 7: Top Level



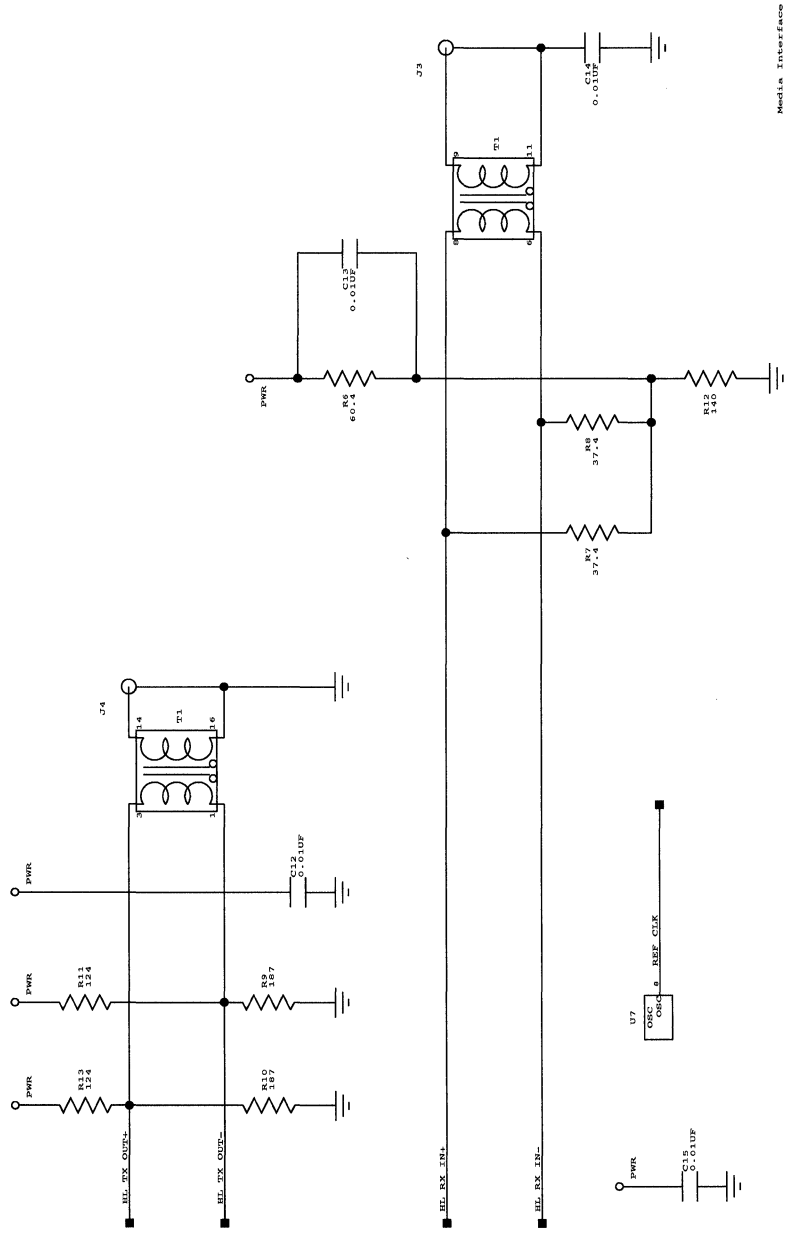
Appendix A. Hierarchical Schematics
Sheet 2 of 7: ATM Layer UTOPIA Extender



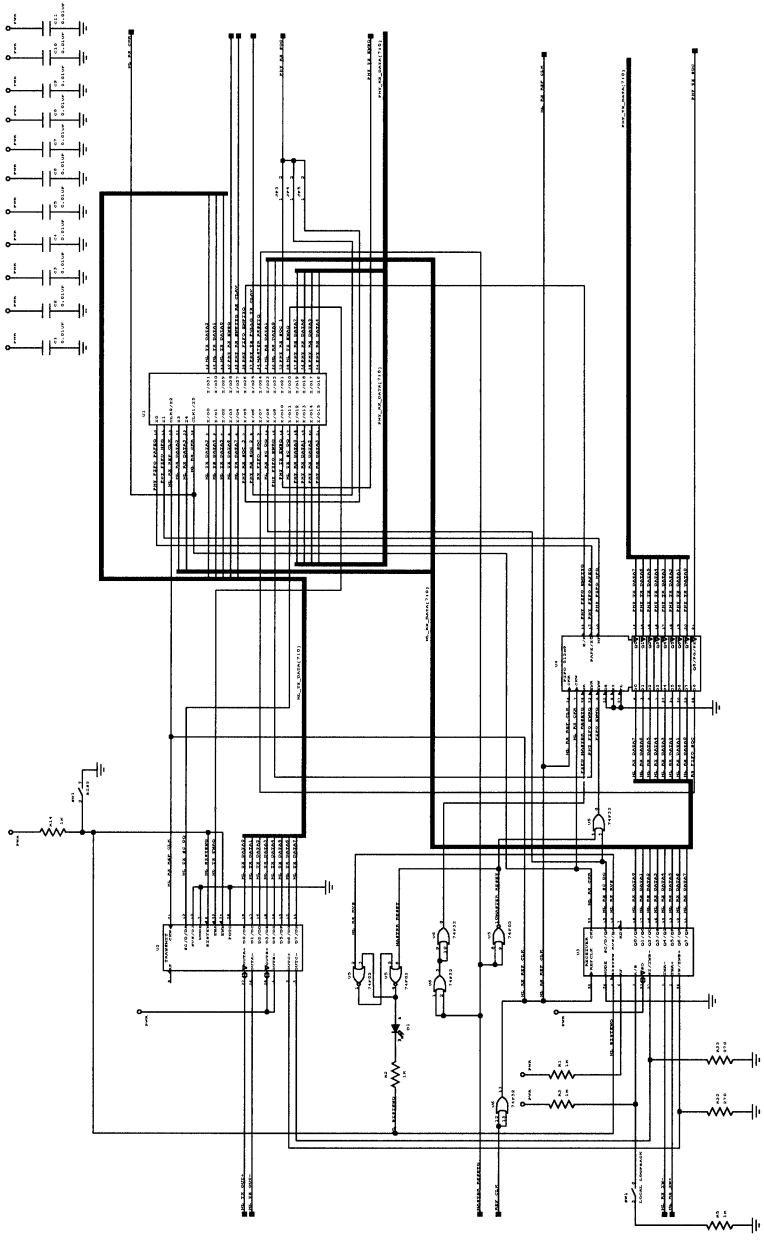
Appendix A. Hierarchical Schematics
Sheet 3 of 7: PHY Layer UTOPIA Extender



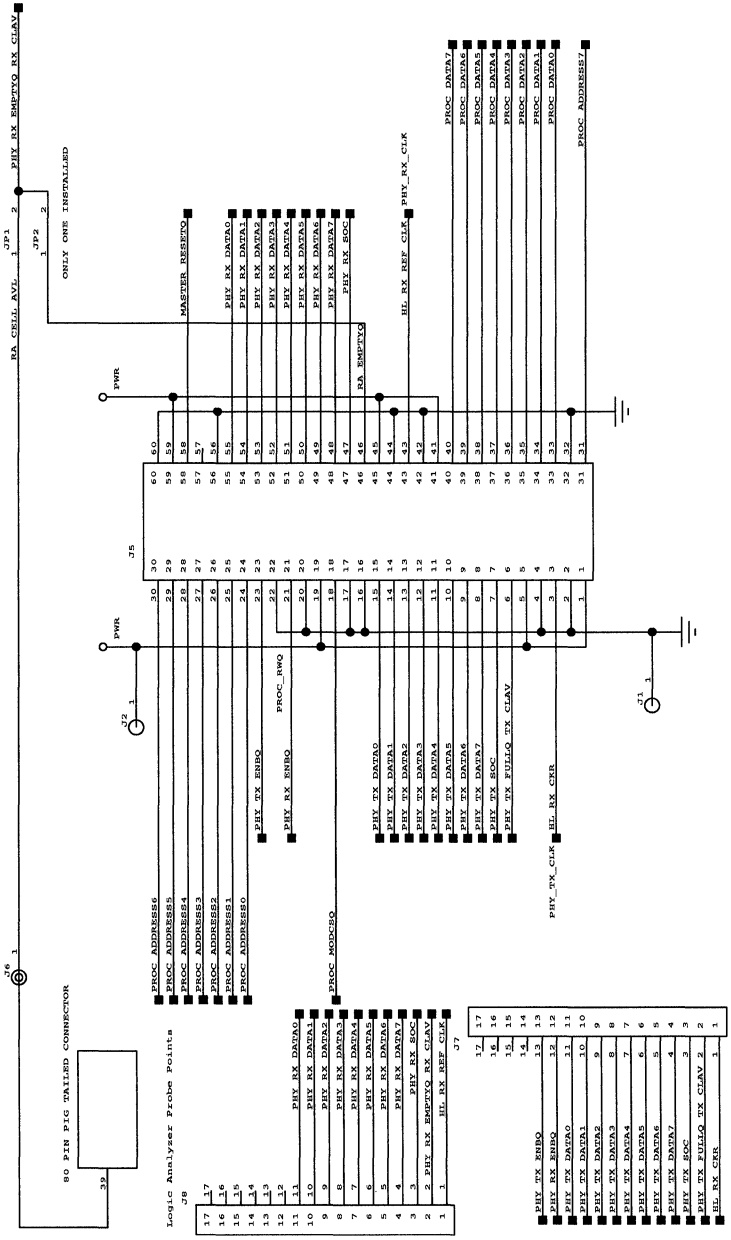
Appendix A. Hierarchical Schematics
Sheet 4 of 7: Media Interface



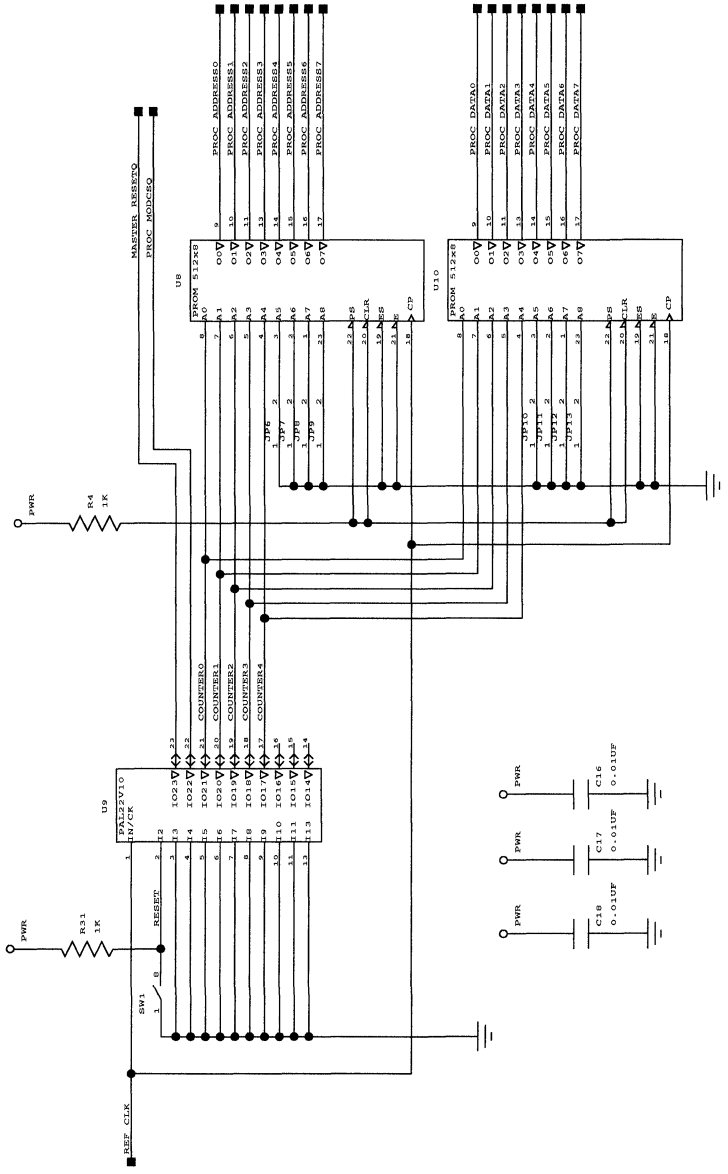
Appendix A. Hierarchical Schematics
Sheet 5 of 7: PHY UTOPIA Logic



Appendix A. Hierarchical Schematics
Sheet 6 of 7: PHY UTOPIA Processor Interface



Appendix A. Hierarchical Schematics
Sheet 7 of 7: Framer Programmer Interface



Appendix B: VHDL Code
UTOPIA Extender, PHY Layer

```
-- UTOPIA extender, PHY layer
--
--

USE WORK.phy_utopia_transmitter_package.ALL;
USE WORK.phy_utopia_receiver_package.ALL;

ENTITY phy_utopia IS
        PORT(   hl_rx_ckr, hl_rx_sc_d,
                master_reset,
                phy_tx_full_tx_clav,
                phy_fifo_hf, phy_fifo_pafe,
                phy_fifo_empty                  : IN BIT;
                hl_rx_data                      : IN BIT_VECTOR(0 to 3);
                rx_fifo_soc,
                phy_tx_enb, phy_fifo_enr        : INOUT BIT;

                phy_rx_clk,
                phy_rx_empty_rx_clav            : IN BIT;
                phy_rx_data                     : IN BIT_VECTOR(0 to 7);
                hl_tx_sc_d, hl_tx_ena,
                phy_rx_enb                      : INOUT BIT;
                hl_tx_data                      : INOUT BIT_VECTOR(0 to 7));

        ATTRIBUTE pin_numbers OF phy_utopia:ENTITY IS
                "hl_tx_data(3):2 " &
                "hl_tx_data(4):3 " &
                "hl_tx_data(5):4 " &
                "hl_tx_data(6):5 " &
                "hl_tx_data(7):6 " &
                "rx_fifo_soc:9 " &
                "phy_fifo_pafe:10 " &
                "phy_fifo_hf:11 " &
                "phy_rx_clk:13 " &
                "hl_rx_sc_d:14 " &
                "phy_fifo_enr:15 " &
                "phy_tx_enb:16 " &
                "hl_tx_sc_d:17 " &
                "phy_rx_data(0):18 " &
                "phy_rx_data(1):19 " &
                "phy_rx_data(2):20 " &
                "phy_rx_data(3):21 " &
                "phy_rx_data(4):24 " &
                "phy_rx_data(5):25 " &
                "phy_rx_data(6):26 " &
                "phy_rx_data(7):27 " &
                "hl_tx_ena:28 " &
                "hl_rx_data(0):30 " &
                "hl_rx_data(1):31 " &
                "hl_rx_data(2):32 " &
                "hl_rx_data(3):33 " &
                "hl_rx_ckr:35 " &
                "master_reset:36 " &
                "phy_tx_full_tx_clav:37 " &
                "phy_fifo_empty:38 " &
                "phy_rx_empty_rx_clav:39 " &
                "phy_rx_enb:40 " &
                "hl_tx_data(0):41 " &
                "hl_tx_data(1):42 " &
                "hl_tx_data(2):43 ";

END phy_utopia;

ARCHITECTURE netlist OF phy_utopia IS

        SIGNAL atm_fifo_hf_code                 : BIT;
        SIGNAL atm_fifo_not_hf_code             : BIT;
       SIGNAL phy_fifo_hf_state             : BIT;
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer (continued)

```
BEGIN
        U1: phy_utopia_transmitter
                PORT MAP (hl_rx_ckr, hl_rx_sc_d, master_reset,
                                phy_tx_full_tx_clav, phy_fifo_hf,
                              phy_fifo_pafe, phy_fifo_empty, hl_rx_data,
                                phy_fifo_hf_state, rx_fifo_soc,
                              atm_fifo_hf_code, atm_fifo_not_hf_code,
                              phy_tx_enb, phy_fifo_enr);

        U2: phy_utopia_receiver
                PORT MAP (phy_rx_clk, phy_rx_empty_rx_clav, master_reset,
                              atm_fifo_hf_code, atm_fifo_not_hf_code,
                              phy_fifo_hf_state, phy_rx_data, hl_tx_sc_d,
                                hl_tx_ena, phy_rx_enb, hl_tx_data);
END netlist;
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Transmitter Interface (PHY to ATM)

```
-- UTOPIA extender, PHY layer transmitter interface (PHY to ATM).
--

PACKAGE phy_utopia_transmitter_package IS

COMPONENT phy_utopia_transmitter

                -- Note, hl_rx_ckr = phy_tx_clk.

        PORT(   hl_rx_ckr, hl_rx_sc_d,
                master_reset,
                phy_tx_full_tx_clav,
               phy_fifo_hf, phy_fifo_pafe,
                phy_fifo_empty                  : IN BIT;
                hl_rx_data                      : IN BIT_VECTOR(0 to 3);
                phy_fifo_hf_state,
               rx_fifo_soc, atm_fifo_hf_code,
                atm_fifo_not_hf_code,
                phy_tx_enb, phy_fifo_enr        : INOUT BIT);

END COMPONENT;
END phy_utopia_transmitter_package;

ENTITY phy_utopia_transmitter IS
        PORT(   hl_rx_ckr, hl_rx_sc_d,
                master_reset,
                phy_tx_full_tx_clav,
               phy_fifo_hf, phy_fifo_pafe,
                phy_fifo_empty                  : IN BIT;
                hl_rx_data                      : IN BIT_VECTOR(0 to 3);
                phy_fifo_hf_state,
               rx_fifo_soc, atm_fifo_hf_code,
                atm_fifo_not_hf_code,
                phy_tx_enb, phy_fifo_enr        : INOUT BIT);

END phy_utopia_transmitter;

ARCHITECTURE behavior OF phy_utopia_transmitter IS

        -- Codes received from ATM side pertaining to the state
        --      of the ATM side FIFO.  Note, the 'fifo_hf_code'
        --      is a HOTLink K28.0 code, while the 'fifo_not_hf_code'
        --      is a HOTLink K28.2 code.

        CONSTANT fifo_hf_code : BIT_VECTOR := X"2";
        CONSTANT fifo_not_hf_code : BIT_VECTOR := X"0";

        SIGNAL phy_tx_enb_wait                  : BIT;

BEGIN

        -- Generate the FIFO read enable signal using the invert of
        -- phy_tx_full_tx_clav.  Also, want to disable when resetting.

        phy_fifo_enr <= NOT(phy_tx_full_tx_clav) OR NOT(master_reset);

        -- Note that data out of the FIFO is valid on the rising edge
        -- AFTER the data is read out.  So, want to delay the phy_tx_enb
        -- one clock from the FIFO read enable.

        PROCESS
        BEGIN
                WAIT UNTIL hl_rx_ckr = '1';
                phy_tx_enb_wait <= phy_fifo_empty AND phy_tx_full_tx_clav;

        END PROCESS;

        phy_tx_enb <= NOT(phy_tx_enb_wait) OR NOT(master_reset);

        -- Essentially, rx_fifo_soc is a one clock delay (w.r.t.
        -- hl_rx_ckr) of the hl_rx_sc_d pin.  This is then used to
        -- generate the input bit to the FIFO for the phy_tx_soc signal.
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Transmitter Interface (PHY to ATM) (continued)

```
        PROCESS
        BEGIN

              WAIT UNTIL hl_rx_ckr = '1';
              rx_fifo_soc <= hl_rx_sc_d;

        END PROCESS;

      PROCESS
      BEGIN

              WAIT UNTIL hl_rx_ckr = '1';

              IF ((hl_rx_data = fifo_hf_code) AND (hl_rx_sc_d = '1')) THEN
                      atm_fifo_hf_code <= '1';
              ELSIF ((hl_rx_data = fifo_not_hf_code) AND (hl_rx_sc_d = '1'))
                      THEN
                      atm_fifo_not_hf_code <= '1';
              ELSE
                      atm_fifo_hf_code <= '0';
                      atm_fifo_not_hf_code <= '0';
              END IF;
      END PROCESS;

        PROCESS (master_reset, phy_fifo_pafe, phy_fifo_hf)

        -- Hysterisis is added to the PHY FIFO half-full flag via the
        --      input 'phy_fifo_hf_state'.  Thus, the half-full state
        --      is set to TRUE (1) when 'phy_fifo_hf' = 0.  The half-full state
        --      is set to FALSE (0) when 'phy_fifo_pafe' = 0.

        BEGIN

        phy_fifo_hf_state <= (NOT(phy_fifo_hf) OR (phy_fifo_pafe AND
                              phy_fifo_hf_state)) AND (master_reset);

        END PROCESS;
END behavior;
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Receiver Interface (PHY to ATM)

```
-- UTOPIA extender, PHY layer receiver interface (PHY to ATM).
--
--

PACKAGE phy_utopia_receiver_package IS

COMPONENT phy_utopia_receiver
        PORT(   phy_rx_clk, phy_rx_empty_rx_clav,
               master_reset, atm_fifo_hf_code,
                atm_fifo_not_hf_code,
               phy_fifo_hf_state             : IN BIT;
                phy_rx_data                     : IN BIT_VECTOR(0 to 7);
                hl_tx_sc_d, hl_tx_ena,
                phy_rx_enb                      : INOUT BIT;
                hl_tx_data                      : INOUT BIT_VECTOR(0 to 7));

END COMPONENT;
END phy_utopia_receiver_package;

ENTITY phy_utopia_receiver IS

        PORT(   phy_rx_clk, phy_rx_empty_rx_clav,
                master_reset, atm_fifo_hf_code,
                atm_fifo_not_hf_code,
               phy_fifo_hf_state             : IN BIT;
                phy_rx_data                     : IN BIT_VECTOR(0 to 7);
                hl_tx_sc_d, hl_tx_ena,
                phy_rx_enb                      : INOUT BIT;
                hl_tx_data                      : INOUT BIT_VECTOR(0 to 7));


END phy_utopia_receiver;

ARCHITECTURE behavior OF phy_utopia_receiver IS

        -- Codes received from ATM side pertaining to the state
        --      of the PHY side FIFO.  Note, the 'fifo_hf_code'
        --      is a HOTLink K28.0 code, while the 'fifo_not_hf_code'
        --      is a HOTLink K28.2 code.
        -- 'packet_size' is the number of bytes in a packet (i.e. 53 bytes)
        -- 'packet_gap' is the minimum number clocks allowed between
        --      packets.
        -- 'packet_start_delay' is the number of clocks from when 'phy_rx_enb'
        --      is valid to when data appears at the PHY UTOPIA receiver
        --      interface.  Currently, this is defined by the UTOPIA spec.
        --      as 1 clock.

        CONSTANT fifo_hf_code                   : BIT_VECTOR := X"02";
        CONSTANT fifo_not_hf_code               : BIT_VECTOR := X"00";
        CONSTANT packet_size                    : INTEGER := 53;
        CONSTANT packet_gap                     : INTEGER := 1;
        CONSTANT packet_start_delay             : INTEGER := 0;

        -- State of ATM side FIFO maintained on PHY side as 'atm_fifo_hf'.
        -- State of PHY side FIFO as known on ATM side is
        --      'phy_fifo_hf_on_atm'.

        SIGNAL atm_fifo_hf                      : BIT:='0';
        SIGNAL phy_fifo_hf_on_atm               : BIT:='0';

        -- The 'counter' signal is used to establish the length of
        --      the packet from the PHY UTOPIA receiver interface.  It
        --      is also used to assure that there are a sufficient number
        --      of clocks in between packets as defined by 'packet_gap'.
       --      The 'hotlink_idle' signal is used to indicate no data
       --      is being transmitted by the HOTLink Tx and thus the
       --      Tx could be used to send FIFO update codes.

        SIGNAL counter                          : INTEGER(0 to packet_size):=0;
       SIGNAL hotlink_idle                     : BIT:='0';
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Receiver Interface (PHY to ATM) (continued)

```
        TYPE    state_type IS (wait_here, start_delay, count, cell_gap);
        SIGNAL  present_state, next_state     : state_type := wait_here;

BEGIN

        PROCESS (master_reset, atm_fifo_hf_code, atm_fifo_not_hf_code)
        BEGIN

                IF (master_reset = '0' OR atm_fifo_not_hf_code = '1') THEN
                        atm_fifo_hf <= '0';
                ELSIF (atm_fifo_hf_code = '1') THEN
                        atm_fifo_hf <= '1';

                        -- Set 'atm_fifo_hf' to 1 when receive
                        --      'atm_fifo_hf_code' and clear when receive
                        --      'atm_fifo_not_hf_code'.

                END IF;
        END PROCESS;

        PROCESS
        BEGIN

                WAIT UNTIL phy_rx_clk = '1';

                IF (present_state /= next_state)
                THEN
                        counter <= 1;
                ELSE
                        counter <= counter +1;
                END IF;

        END PROCESS;

        PROCESS(present_state, counter, phy_rx_empty_rx_clav, atm_fifo_hf,
                master_reset)

                -- 'phy_rx_empty_rx_clav' is 1 when the PHY side has
                --      a full cell (53 bytes).  So, if the ATM side
                --      FIFO is not half-full, then set 'phy_rx_enb'
                --      to 0 and start transmitting cells back to the
                --      ATM side.  Stop (i.e. set 'phy_rx_enb' to 1)
                --      after 53 bytes to prevent back to back cell
                --      transfers from the PHY UTOPIA receiver interface.
                --      Wait an additional 'packet_gap' number of clocks
                --      before reenabling the receiver via 'phy_rx_enb'.
                --      We must assure that there are at least packet_gap
                --      bytes between packets in order to recreate the
                --      rx_soc signal on the ATM side.  This gap will
                --      also be used to send PHY FIFO state codes to
                --      the ATM side.
        BEGIN

                CASE present_state IS

                WHEN wait_here =>

                        phy_rx_enb <= '1';
                        hotlink_idle <= '1';
                        IF (phy_rx_empty_rx_clav = '1' AND atm_fifo_hf = '0'
                                AND master_reset = '1')
                        THEN
                                IF (counter < packet_start_delay)
                                THEN
                                        next_state <= start_delay;
                                ELSE
                                        next_state <= count;
                                END IF;
                        ELSE
                                next_state <= wait_here;
                        END IF;
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Receiver Interface (PHY to ATM) (continued)

```
        WHEN start_delay =>
                phy_rx_enb <= '0';
                hotlink_idle <= '1';
                IF ((counter < packet_start_delay)
                        AND master_reset = '1')
                THEN
                        next_state <= start_delay;
                ELSIF (master_reset = '0')
                THEN
                        next_state <= wait_here;
                ELSE
                        next_state <= count;
                END IF;
        WHEN count =>
                  phy_rx_enb <= '0';
                hotlink_idle <= '0';
                IF ((counter < packet_size)
                        AND master_reset = '1')
                THEN
                        next_state <= count;
                ELSIF (master_reset = '0')
                THEN
                        next_state <= wait_here;
                ELSE
                        next_state <= cell_gap;
                END IF;
        WHEN cell_gap =>
                  phy_rx_enb <= '1';
                hotlink_idle <= '1';
                IF (counter < packet_gap)
                THEN
                        next_state <= cell_gap;
                ELSIF (phy_rx_empty_rx_clav = '1'
                        AND atm_fifo_hf = '0' AND master_reset = '1')
                THEN
                        IF (packet_start_delay < packet_gap)
                        THEN
                                next_state <= count;
                        ELSE
                                next_state <= start_delay;
                        END IF;
                ELSE
                        next_state <= wait_here;
                END IF;
        END CASE;
END PROCESS;

 PROCESS
 BEGIN
        WAIT UNTIL phy_rx_clk = '1';
        present_state <= next_state;
END PROCESS;

PROCESS (phy_fifo_hf_state, phy_fifo_hf_on_atm, hotlink_idle,
                phy_rx_clk)
BEGIN
        -- If hotlink_idle = '0' send data.
        IF (hotlink_idle = '0')
        THEN
                hl_tx_ena <= '0';
                hl_tx_sc_d <= '0';
                hl_tx_data <= phy_rx_data;
```

Appendix B: VHDL Code
UTOPIA Extender, PHY Layer Receiver Interface (PHY to ATM) (continued)

```
                -- If the HOTLink is idle (no data being sent) and
                --      the FIFO state needs updating, send the code.

                ELSE
                        hl_tx_sc_d <= '1';
                        IF (phy_fifo_hf_state /= phy_fifo_hf_on_atm)
                        THEN
                                hl_tx_ena <= '0';
                                IF (phy_fifo_hf_state = '1') THEN
                                        hl_tx_data <= fifo_hf_code;
                                ELSE
                                        hl_tx_data <= fifo_not_hf_code;
                                END IF;
                        ELSE
                                hl_tx_ena <= '1';
                        END IF;
                END IF;
        END PROCESS;

        PROCESS
        BEGIN

                WAIT UNTIL phy_rx_clk = '1';

                IF hotlink_idle = '1'
                THEN
                        phy_fifo_hf_on_atm <= phy_fifo_hf_state;
                END IF;
        END PROCESS;
END behavior;
```

Appendix B: VHDL Code
UTOPIA Extender, Duke PHY Board Programmer

```
-- UTOPIA extender, Duke PHY board programmer
--

PACKAGE duke_programmer_package IS

COMPONENT duke_programmer
        PORT(   ref_clk, reset                          : IN BIT;
                proc_modcs, master_reset        : INOUT BIT;
                counter                                 : INOUT INTEGER(0 to 24));

END COMPONENT;
END duke_programmer_package;

ENTITY duke_programmer IS
        PORT(   ref_clk, reset                          : IN BIT;
                proc_modcs, master_reset        : INOUT BIT;
                counter                                 : INOUT INTEGER(0 to 24));

       ATTRIBUTE pin_numbers OF duke_programmer:ENTITY IS
                "reset:2 " &
                "ref_clk:1 " &
                "counter(0):21 " &
                "counter(1):20 " &
                "counter(2):19 " &
                "counter(3):18 " &
                "counter(4):17 " &
                "proc_modcs:22 " &
                "master_reset:23 ";

END duke_programmer;

ARCHITECTURE behavior OF duke_programmer IS

       CONSTANT num_values                      : INTEGER :=24;

       TYPE state_type IS (wait_here, do_reset, count1, count2, count3);

       TYPE addrdata IS ARRAY(0 to num_values - 1) OF BIT_VECTOR(0 to 7);

       CONSTANT addresses : addrdata :=
       (       X"81",
               X"81",
               X"8D",
               X"8D",
               X"20",
               X"80",
               X"82",
               X"83",
               X"84",
               X"85",
               X"86",
               X"87",
               X"88",
               X"89",
               X"8A",
               X"8B",
               X"8C",
               X"8E",
               X"8F",
               X"90",
               X"91",
               X"92",
               X"9E",
               X"9F");
```

Appendix B: VHDL Code
UTOPIA Extender, Duke PHY Board Programmer (continued)

```
        CONSTANT data : addrdata :=
        (       X"01",
                X"00",
                X"01",
                X"00",
                X"0A",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00",
                X"00");

        SIGNAL  present_state, next_state     : state_type := wait_here;

BEGIN

        PROCESS(present_state, reset, ref_clk)
        BEGIN

                CASE present_state IS

                WHEN wait_here =>

                        master_reset <= '1';
                        proc_modcs <= '1';
                        IF (reset = '0')
                        THEN
                                next_state <= do_reset;
                        ELSE
                                next_state <= wait_here;
                        END IF;

                WHEN do_reset =>

                        master_reset <= '0';
                        proc_modcs <= '1';
                        next_state <= count1;

                WHEN count1 =>

                        master_reset <= '1';
                        proc_modcs <= '1';
                        next_state <= count2;

                WHEN count2 =>

                        master_reset <= '1';
                        proc_modcs <= '0';
                        next_state <= count3;
```

Appendix B: VHDL Code
UTOPIA Extender, Duke PHY Board Programmer (continued)

```
            WHEN count3 =>

                    master_reset <= '1';
                    proc_modcs <= '1';
                    next_state <= count2;
                    IF (counter < num_values - 1)
                    THEN
                            next_state <= count1;
                    ELSE
                            next_state <= wait_here;
                    END IF;

            END CASE;
    END PROCESS;

    PROCESS
    BEGIN

            WAIT UNTIL ref_clk = '1';

            present_state <= next_state;
    END PROCESS;

    PROCESS
    BEGIN

            WAIT UNTIL ref_clk = '1';

            IF (present_state = count3)
            THEN
                    counter <= counter + 1;
            END IF;
    END PROCESS;

END behavior;
```

Drive ESCON™ With HOTLink™

Introduction

The IBM® ESCON™ (Enterprise System CONnection) interface is presently experiencing rapid growth. Originally designed as a replacement for the older block-mux channel, it is also finding use as a high-performance system interface. This once IBM-proprietary interface is presently being processed to become an ANSI standard interface (known as SBCON) for computer to peripheral interconnect.

This application note contains an overview of ESCON operation and a design example of an ESCON physical interface, including a number of the low-level ESCON state machines (including the VHDL source code), implemented using HOTLink™ and a pASIC™ field programmable gate array.

Channels

The term *channel*, when referring to mainframes, carries a specific meaning. Rather than representing the connection between pieces of equipment, here it also represents a significant piece of equipment as well. The channel is, in effect, a sophisticated and intelligent DMA engine whose purpose is to move information between I/O devices and main storage. This channel function removes the burden of handling I/O activities from the main CPU.

Block-Multiplexer Channel

The original block-multiplexer channel dates back to the System 360/370 family of IBM mainframe CPUs. It uses a pair of parallel-bus copper cables (referred to as Bus and Tag cables) to move data between the host CPU and the I/O and storage peripherals as shown in *Figure 1*. These bus and tag cables were daisy-chained from the host channel adapter through multiple storage and I/O directors.

While quite powerful in its day, the block-mux channel shows both its heritage and its age. The bus and tag cables are quite bulky (around 1.5″ in diameter), heavy, *and* costly. The maximum length of the link between the host CPU channel adapter and the cable terminator is 400 feet, and operates at a maximum transfer rate of 4.5 MBytes/second. While originally designed to simultaneously support a larger number of peripherals, its is now possible to saturate the full I/O bandwidth capability of a block-mux channel with a single disk drive.

ESCON Channel

The ESCON channel was introduced in 1990 along with the ESA390 series of mainframe computers. It uses high-speed serial, point-to-point fiber-optic links to replace the daisy-chained parallel-bus copper cables of a block-mux channel. By maintaining the same host CPU software structures used with the block-mux channel, it was possible to dramatically change the architecture (and performance) of the I/O subsystem without effecting the major I/O routines present in the host CPU and channel microcode.

This new interconnect media was also merged with a dynamic switched connection scheme to improve both availability and access to the I/O peripherals. The use of switches (known as *directors*) allows many more paths to each peripheral, with multiple paths being active through each director at the same time. This new interconnect structure is shown in *Figure 2*. This switched I/O structure is now finding popular use in many other data communications in-

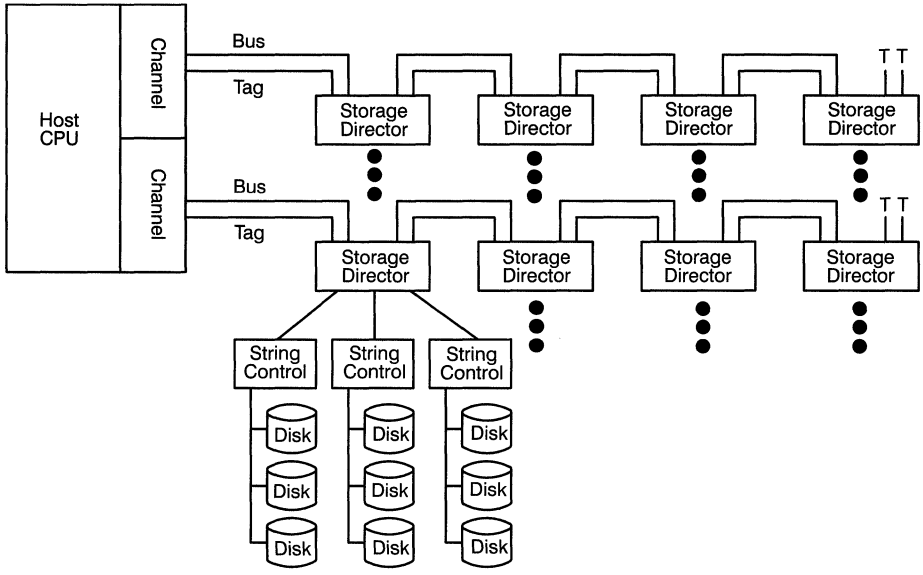


Figure 1. Block-Multiplexer Channel Subsystem

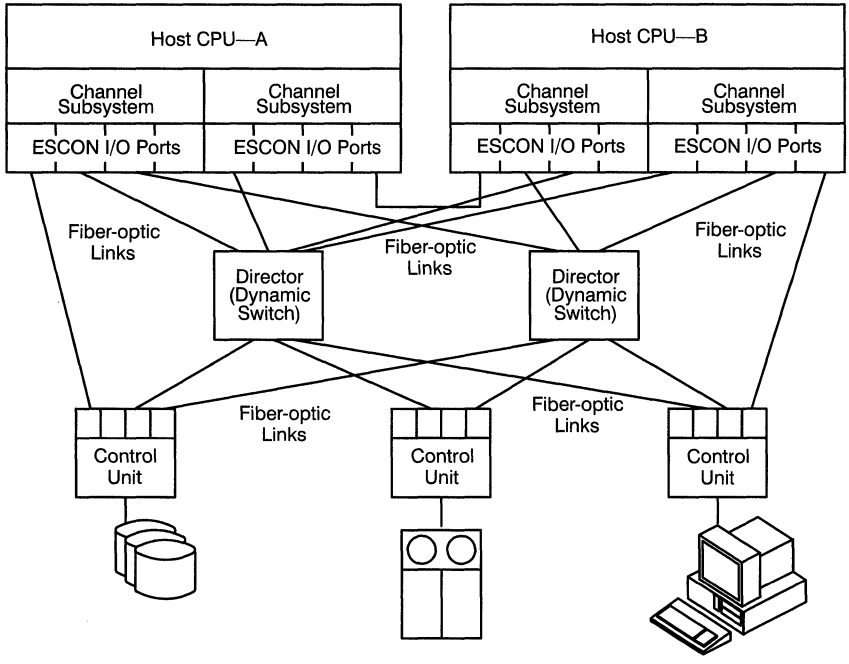


Figure 2. ESCON Channel Subsystem

terfaces like switched Ethernet, ATM, and Fibre Channel.

The ESCON interface provides numerous improvements over the older block-mux channel. A few of these are

- Improved transfer rate to 20 MBytes/second
- Longer distances—up to 3 km for each link and up to three links (two switches) between Channel and Control Unit
- Immunity from EMI/EMC concerns
- Improved access, redundancy, and availability through use of dynamic switches

ESCON Physical

The physical-level interconnections of ESCON are all made with 1300-nm LED-based optical links. These links operate through either 62.5 μm or 50 μm core multi-mode optical fibers at a fixed bit rate of 200 Mbits/second. This bit rate represents the encoded bit rate for the data being sent.

The data sent across ESCON links is encoded using the 8B/10B code built into HOTLink. (See the CY7B923/933 datasheet for a detailed description of the 8B/10B code.) This code converts normal 8-bit bytes into 10-bit transmission characters. While this encoding does have a 25% overhead, the benefits of using it far outweigh the data-rate penalty.

Part of the reason for the two extra bits in each character is to guarantee a minimum transition density for the receive PLL. Since no clock is present in the serial data, the HOTLink receiver PLL is used to extract a bit-rate clock from the data steam

Another benefit from this code is its DC-balance characteristic. This means that, over time, the net difference of all 1-bits versus 0-bits sent is at or near zero. This DC-balance characteristic allows the optical receiver circuits to be much simpler and lower in cost by reducing the complexity of the AGC (automatic gain control) in the receiver preamplifier.

With a transmission character being ten bits in length, there are actually 1024 possible transmission characters. Of these possible codes, only a fraction of them meet all the run length and DC-balance coding rules. The remainder are illegal codes and are detected as errors at the receive end of the link. Most of the valid codes are used to represent the 256 possible data bytes, with a few remaining legal transmission characters used for synchronization and in-band signaling.

The term *in-band* means that all delimiters, protocol, clocking, etc., are handled through the same serial interface as the data; i.e., there are no other control lines or interfaces used for this information. The 8B/10B code provides twelve transmission characters for these in-band functions. Of these twelve characters (referred to as special characters), only six are defined for use by ESCON.

Synchronization

With any serial interface some form of synchronization is necessary at the receiver-end of a link. The function of synchronization is to line up the receiver bit and byte clocks with the serial data stream.

Bit Synchronization

Bit synchronization is performed (for the most part) automatically by the receiver PLL. As transitions are detected, the phase detector in the receiver uses the position of the transition (relative to its internal bit-clock) to adjust the phase and frequency of the local bit-clock. This local bit-clock is optimally adjusted to allow the serial data stream to be sampled at the center of each bit. However, bit synchronization alone is not sufficient to recover and decode the transmitted information. This requires knowledge of which bit in the serial stream is the start of a character.

Framing

Proper detection of character boundaries is referred to as framing. Unlike bit synchronization, which occurs primarily in the analog domain, framing is a full-digital operation.

Framing is performed by examining the serial bit stream for a specific pattern (called a comma). This

test occurs on every bit-clock until an exact match is found. At this point the receiver byte-clock is reset to line up with the character boundary. Following this, all characters output from the receiver should remain properly synchronized, until some external event causes a significant disruption in the data stream.

The comma in the 8B/10B code is the seven bit pattern 0011111 (or its alternate 1100000). This bit pattern is part of the K28.5 special character. It cannot appear in any other location in any 8B/10B encoded character, and cannot be generated across the boundaries of any pair of characters.

While the detection of individual bits is controlled automatically by the PLL, the detection of framing for ESCON must be under the control of a separate state machine. This machine determines under what conditions the receiver is allowed to perform its framing function.

ESCON Synchronization

An ESCON interface is normally considered to be in one of two states regarding synchronization; either Synchronization_Acquired or Loss_Of_Synchronization (LOS). The transitions between these two primary states actually involve a number of substates that track error conditions and special characters on the interface. This state machine is shown in *Figure 3*.

In addition to its five states (four Sync Acquired and one Loss Of Sync), it operates with a 4-bit counter to track both valid characters and K28.5 characters. Since in any specific state of the machine only one thing is being counted (valid characters or K28.5 characters), only a single counter is needed.

Loss Of Synchronization

The ESCON interface automatically enters the LOS state following power-on. In this state (if a valid signal is present) the serial data receiver is enabled not only to received data, but also to frame on any received K28.5 character (RF=1).

While the receiver will frame on the first K28.5 received, this is not sufficient to leave the LOS state.

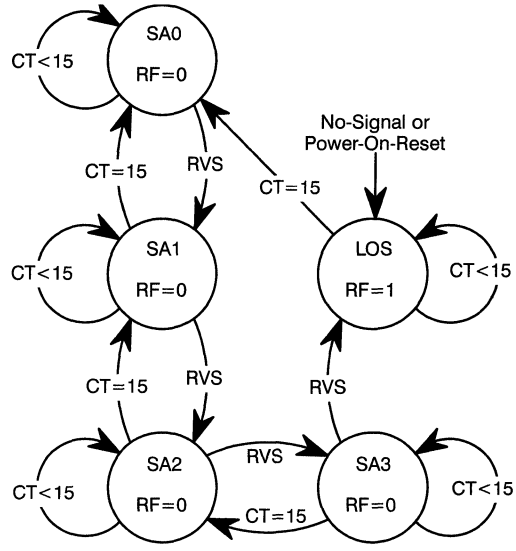


Figure 3. Synchronization State Machine

This requires reception of a minimum of fifteen K28.5 characters with no intervening code violations between any of the received characters. These K28.5 characters may be directly adjacent or more likely will have other characters interspersed. Once this string of K28.5 characters has been received, the receiver enters the Synchronization_Acquired state.

Synchronization Acquired

Exit from the LOS state also removes the reframe signal from the receiver (RF=0). In this condition the receiver will ignore (for framing purposes) all K28.5 characters embedded in the data stream. These characters are still properly received and decoded for use as part of the link protocol.

In the Sync Acquired state the state machine now tracks any code violations (RVS). If a code violation occurs the state machine changes from the basic Sync Acquired state (SA0) to SA1. In this state the machine has now detected a single error. It then enables the separate 4-bit counter to check for consecutive valid characters. If the following fifteen characters are received without error, the machine reverts back to the basic Sync_Acquired state.

If, however, additional character errors are detected, the state machine will advance through the SA1, SA2, and SA3 states—one change for each character received in error. At each of these states the machine will again check for valid characters and will revert to the previous state if fifteen are received without any errors. This would allow an interface receiving exactly one error every sixteen characters to remain in the SA0 and SA1 states, while a similar interface receiving one error every fifteen characters would quickly move to the LOS state and remain there.

Link-Level Operations

The actual functionality of an ESCON link is defined in terms of various ordered sets of special characters and data bytes. These ordered sets are used to define frame boundaries, control dynamic connections, and control synchronization between the transmitter and receiver circuits. All valid ESCON ordered sets are listed in *Table 1.*

Table 1. ESCON Ordered Sets

Ordered Set	Characters
Idle function	K28.5
Connect-start-of-frame delimiter	K28.1 K28.7
Passive-start-of-frame delimiter	K28.5 K28.7
Abort delimiter	K28.6 K28.4 K28.4
Disconnect-end-of-frame delimiter	K28.6 K28.1 K28.1
Passive-end-of-frame delimiter	K28.6, K28.2 K28.5
Not-operational	K28.5 D0.2
Unconditional-disconnect sequence	K28.5 D15.2
Unconditional-disconnect-response sequence	K28.5 D16.2
Off-line Sequence	K28.5 D24.2

Idle Function

The K28.5 character in ESCON is used for multiple purposes. It is

- the first character of many ordered sets
- used to provide byte framing of the serial data stream
- used as a fill or *Idle* character between frames and sequences

Because the K28.5 character is contained in many of the other ordered sets, a single K28.5 cannot be conferred to be an Idle function until the following character is detected. If the following character is also an K28.5, then the previous K28.5 is part of an Idle Function. If the following character is anything else, then the K28.5 character is part of a delimiter or sequence (or an error).

Delimiters

Delimiters are used to mark the start and end of frames. Frames are the real workhorse of the interface because they carry data. All frames have a start-of-frame delimiter (SOF) and an end-of-frame delimiter (EOF). (An Abort delimiter is considered to be a type of EOF.) These delimiters are only sent once per frame. Each frame must be separated by a minimum of four Idle characters.

Sequences

Sequences are used to indicate specific equipment conditions or states that cannot be identified through the use of frames. Unlike a delimiter, the ordered set defined for a specific sequence is sent repeatedly until the machine state changes or a specific response is received. At the receiver, a sequence is only detected as being valid if the defined ordered set is received a specific minimum number of times in succession.

Frames

Frames are used to carry information between the channel, switches, and the peripherals. Two generic types of frames exist; Link-Control and Device Level.

All frames follow the same three-field format:

- a 7-byte fixed-length link header
- a variable-length information field (may have a length of zero for some Link-Control frames)

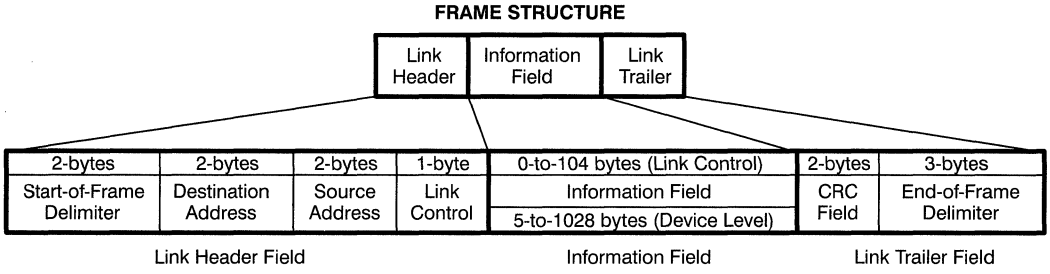


Figure 4. ESCON Frame Format

- and a 5-byte fixed-length link-trailer field

The structure of an ESCON frame is shown in *Figure 4*. The low-order bit of the Link Control field in the Link Header identifies the type of frame. When set to a one, the frame is a Link Control frame. When set to a zero, the frame is Device Level frame.

Link-Control frames are use to manage, configure, and maintain the link itself, and range in length from 12 to 116 bytes. Device Level frames carry data between the channel and the peripheral and range in size from 17 to 1040 bytes.

Frame Validation

Before a frame can be processed, it must be validated as a properly received frame. This involves making sure that there are no special characters or idles in the middle of the frame, no decoding errors are detected in the serial stream, and that the CRC Field (Cyclic Redundancy Check) shows no errors.

Cyclic Redundancy Check Field

The CRC field contains a 16-bit redundancy check code, used to insure that the received frame contents are the same as those sent. This field is generated at the transmitting end of a link and sent as the first two bytes of the Link Trailer field. It is calculated on all bytes between the start-of-frame delimiter and the Link Trailer field.

At the receiving end of the link the CRC is again generated using the received data stream. Now the CRC is generated on all bytes between the start-of-frame delimiter and the end-of-frame delimiter.

The CRC code used with ESCON is that defined by the ITU V.41 standard (previously known as CCITT). The polynomial for this CRC is listed in *Equation 1*.

$$x^{16} + x^{12} + x^5 + 1 \qquad \text{Eq. 1}$$

Normally with a code of this type the CRC remainder register is preset to an all 1s condition prior to the first bit of information being clocked through the polynomial. This is done to ensure that the polynomial will change state no matter what the data stream contains. At the end of the generation, the two bytes comprising the CRC remainder are sent as part of the data stream. At the receiving end the same process occurs, but the two CRC bytes are also clocked into the CRC register. If no errors exist in the serial stream then the contents of the CRC check register should be zero.

To increase the level of protection, the CRC is handled slightly differently in an ESCON interface. Here the CRC remainder generated at the transmitter is inverted prior to sending it across the link. When it is received (correctly) the CRC check register is no longer cleared, but must be set to exactly 1D0F (hexadecimal). Any other value indicates a transmission or reception error.

ESCON Design Example

The following design was originally done to replace an existing ESCON protocol component that was no longer available. All VHDL source code listed here has been both simulated and tested in a functioning ESCON system.

This design example covers

- an ESCON-compatible optical media interface
- ESCON-certified HOTLink serializer/deserializer components
- a pASIC383 protocol chip containing
  - — transmit and receive CRC circuits
  - — parity check and generate circuits
  - — synchronization state machine
  - — command code translation capability
  - — input/output pipeline registers
  - — miscellaneous flip-flops, muxes, and gates

The design is partitioned into transmit and receive data paths, and is implemented in four active devices:

- a pASIC383 containing both transmit and receive protocol functions
- a CY7B923 HOTLink transmitter for serialization and 8B/10B encode
- a CY7B933 HOTLink receiver for deserialization and 10B/8B decode
- a Siemens V23806–A1–M16 ESCON fiber-optic transceiver

The structure of how these components connect and major data paths are shown in *Figure 5*, with a complete schematic shown in *Figure 6*.

Fiber-optic Transceiver

The fiber-optic transceiver is an optoelectric device that both converts electrical signals to light (transmitter) and light into electrical signals (receiver).

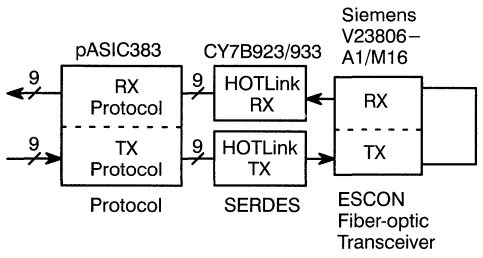


Figure 5. Design Example Structure

To operate with the ESCON interface the transceiver must meet a number of specific characteristics:

- operate at 200 Mbaud
- operate at 1300 nm wavelength
- use 62.5-µm or 50-µm core optical fiber
- meet the 0.7″ ferrule spacing and other dimensions of an ESCON optical connector

In addition to these criteria, compliant transceivers must meet numerous power level, receive sensitivity, and electrical interface criteria to properly operate in an ESCON environment. Manufacturers of ESCON compatible fiber-optic transceivers include Siemens, AMP, IBM, and others.

SERDES

The next section in an ESCON link is the serializer/deserializer block, also known as the SERDES. This section converts parallel bytes of information into an 8B/10B encoded serial data stream for transmission, and also converts a received 8B/10B encoded serial data stream back into parallel data bytes.

The Cypress CY7B923/933 HOTLink components are designed to perform this SERDES function. These components are specifically optimized to support the ESCON interface, as well as Fibre Channel, ATM (Asynchronous Transfer Mode), and proprietary communications links.

These HOTLink parts are especially well suited to the ESCON market because of their built-in 8B/10B encoders and decoders. This encode/decode function is required for ESCON operation. By building the encode/decode into the SERDES block, the complexity of this part of the interface design is removed from the design process. Its presence in the SERDES block also means that hardware resources are not required elsewhere to implement the encode/decode function.

The 8B/10B code used in the HOTLink components is licensed by Cypress Semiconductor from IBM. Any user of these parts is fully licensed to use the 8B/10B encoders and decoders contained in them at no cost and no royalties. For those applications that already have 8B/10B encoder/decoder circuits pres-

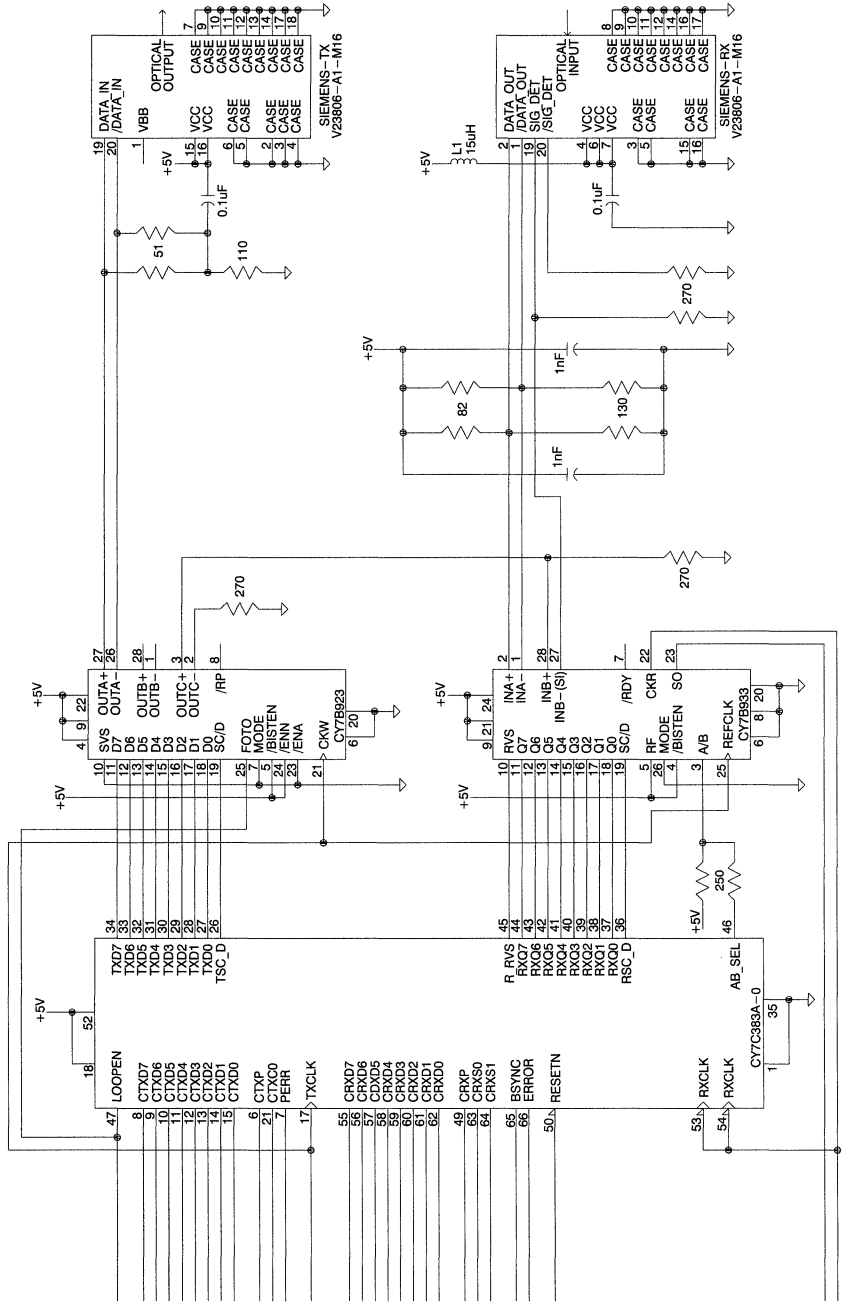


Figure 6. ESCON Physical I/O Interface Schematic

ent in their system, the encoder/decoder present in HOTLink can be bypassed through use of the MODE pin on each part.

An in-depth explanation of the operation and usage of the HOTLink components may be found in the CY7B923/933 datasheet and the *HOTLink User's Guide*.

Serial I/O Electrical Interface

The interface between the fiber-optic transceiver and the HOTLink SERDES operates at 200 Mbits/second. This interface is implemented with ECL (Emitter-Coupled-Logic) signaling to provide a low-noise, high-speed connection. Unlike standard ECL, which is normally operated below ground, both the fiber-optic transceiver and the HOTLink SERDES components are operated above ground. This allows the ECL portion of the design to use the same +5V supply as the surrounding logic. When ECL is operated from a positive supply it is referred to as Positive-ECL or PECL.

The source for the serial data stream is the CY7B923 HOTLink transmitter shown in *Figure 6*. A simplified schematic showing just the interconnect for the serial transmit path is shown in *Figure 7*.

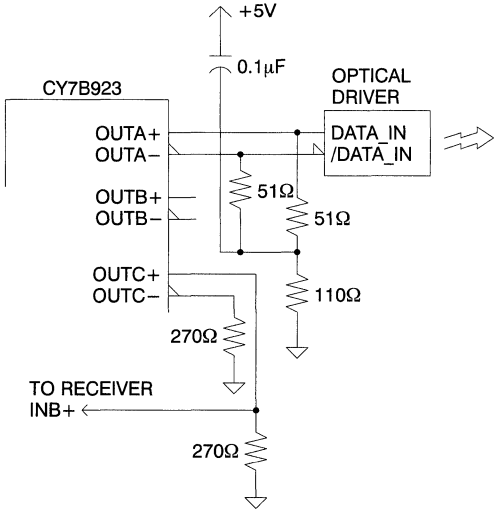


Figure 7. HOTLink Transmitter-to-Optical Serial Interface

The serial data is connected to the fiber-optic transmitter using a differential connection from the OUTA± differential output of the HOTLink transmitter. Because these are ECL/PECL signals, they require a pull-down bias to allow the outputs to switch.

With a transmission rate of 200 Mbits/second, the interconnect used for these signals should (in most cases) be constructed as a controlled-impedance transmission line. The bias network used on the OUTA± signals is referred to as a Y-bias network. It is designed to provide an equivalent transmission line termination impedance of 50Ω while providing a bias level of $V_{CC}-2V$.

The received serial data stream is output from the fiber-optic receiver as a differential signal, as shown in *Figure 6*, and is sent to the CY7B933 HOTLink receiver INA± inputs. A simplified schematic showing just the interconnect of the serial receive path is shown in *Figure 8*. Because this is also a PECL signal, it should be treated in a manner similar to the transmit serial path. This means controlled impedance transmission lines and a proper bias/termination network.

While the receive-path bias/termination network may be implemented using the same Y-bias network used with the transmit serial path, a Thévenin network is shown here. These two bias networks, when used with differential signals, are effectively interchangeable. For single-ended signals requiring the

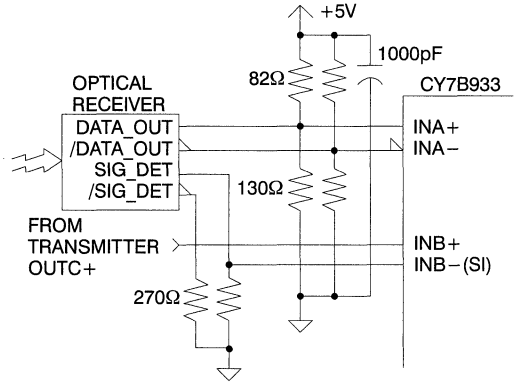


Figure 8. Optical-to-HOTLink Receiver Serial Interface

same electrical characteristics, the Thévenin network must be used. For additional information on terminating and biasing PECL signals, please see the application note "HOTLink Design Considerations" in the *HOTlink User's Guide*.

Serial I/O Support Interface

In addition to the transmit and receive serial data streams, two other PECL signals are normally present in an ESCON interface: signal-detect and local-loopback. The signal-detect function is performed by the fiber-optic receiver. It outputs a PECL logic signal to inform the upstream hardware if a valid signal is present or not. This signal is monitored to determine the synchronization state of the interface.

Because this is a PECL-level signal, it is necessary to convert it to a TTL-level signal for use by upstream logic. While there are components available that explicitly perform this level translation, they are not necessary for this application. Instead it is possible to use one of the design features of the HOTLink receiver INB± inputs to perform this signal-level conversion.

The INB± input can be configured as either a differential PECL receiver (like INA±), or as a single-ended serial PECL receiver and a PECL-to-TTL converter. To use INB± as a differential receiver it is necessary to pull the SO (Status Out) pin to V_{CC}. This disables the PECL-to-TTL converter and maintains both inputs as a differential pair.

To use INB± as two separate inputs requires that the SO pin be loaded as a normal TTL-level output. When configured this way the INB− pin is the input for the PECL-to-TTL converter, with SO being the TTL output. This is the configuration used in *Figures 6* and *8*.

Most ESCON interfaces are also equipped with numerous self-diagnostic capabilities. At the physical interface the most common is a selectable loopback of the serial data stream. This allows all components (with the exception of the fiber-optic transceiver) of the interface to be tested by transmitting data and verifying that it can be properly received. This loopback function is normally implemented using the OUTC+ output of the HOTLink transmitter and the INB+ input on the HOTLink receiver in a single-ended PECL connection, as shown in *Figures 6, 7,* and *8*.

While the best PECL connection is always a differential connection (like that used on INA±), the usage of INB+ in a single-ended mode is fine under these conditions. Because the HOTLink transmitter and receiver are close together in the system and operate from a common power supply, the normal noise-margin concerns of single-ended connections do not apply.

This local loopback functionality is selected through the LOOPBACK signal on the pASIC FPGA. When active (HIGH), this signal drives the HOTLink receiver A/$\overline{B}$ select input LOW to selected the INB+ input for the deserializer, and drives the FOTO input to the HOTLink transmitter HIGH. This FOTO pin is used to disable the OUTA± and OUTB± outputs of the transmitter. This is normally done during loopback diagnostics to prevent the diagnostic data from being interpreted at the other end of the fiber-optic link.

ESCON Protocol Controller

The control of the serial data stream is performed using a pASIC383 FPGA. This part has been programmed to manage both the transmit and receive serial data streams. The programming and verification were done using VHDL (VHSIC Hardware Description Language) using Cypress's *Warp3*™ logic synthesis and simulation tools. Complete source code of the design VHDL modules is listed in Appendixes A through H of this application note, and is available for download from the Cypress Bulletin Board system.

The design shown in this application note is effectively a logic replacement for a Triquint GA9104 ESCON protocol chip. Due to the flexibility of the pASIC family of parts, it is possible to add, replace, or remove logic that is not optimal for a specific application. In this design, the 8B/10B encoders present in the normal GA9104 were not implemented in the pASIC383 because they are already present in the HOTLink CY7B923/933. This allowed the entire functionality to be duplicated in a 2K-equivalent gate FPGA. The functions present in this design are

- Transmit Path
  - — input and output pipeline registers
  - — parity checker and status bit
  - — CRC generator and control state machine
  - — Command/data mux
  - — Command translator
- Receive Path
  - — input and output pipeline registers
  - — CRC checker, control state machine, and status bit
  - — parity generator
  - — Command/data mux
  - — Command translator
- Byte-Sync State Machine

Transmit Path

A block diagram of the transmit path is shown in *Figure 9*. Data is captured into a 10-bit register on each rising edge of the transmit clock (CKW). The data consists of an 8-bit data byte, a single control line (CTXC0), and a parity bit. The CTXC0 line is used to identify whether the data on the inputs is a command code (HIGH) or a data byte (LOW). If the latched character is a data byte, the data is simultaneously presented to the CRC register, the parity checker, and the output multiplexers. At the next rising edge of the transmit clock, this data byte is clocked into the CRC register, checked for proper parity, and loaded into the output register along with TSC_D set LOW.

The detection of a parity error is only a reported event, and occurs one cycle after the data (or command) is latched into the input register. Recovery from detected parity errors would normally require abnormal termination of the current frame using the Abort delimiter.

The CRC/MUX Control block is the heart of the transmit path logic. It monitors the CTXC0 line to determine when to

- preset the CRC register
- accumulate a CRC
- output the CRC bytes
- translate/send command codes

This block is implemented as a simple shift register that tracks the current and previous three states of CTXC0. These sixteen possible combinations (with don't care states removed) and their resulting outputs are listed in *Table 2*. The VHDL source code for this block is listed in Appendix C.

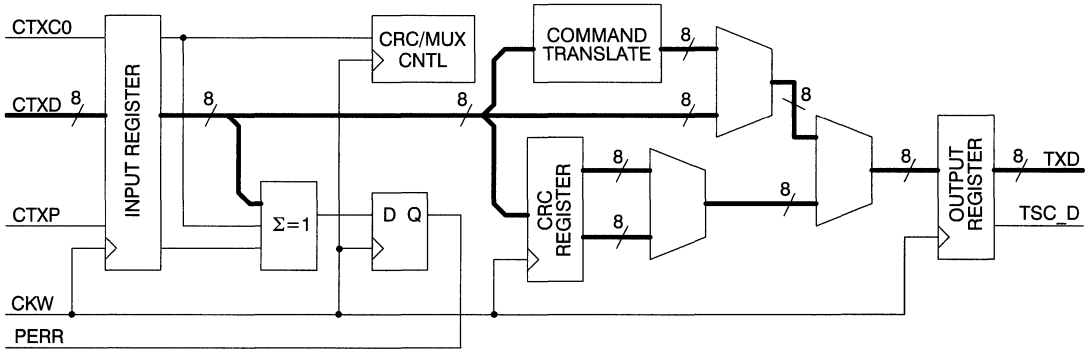


Figure 9. pASIC Transmit Path Block Diagram

Table 2. Transmit Path Control

CTXC0				Mux Select/ CRC Control
t+3	t+2	t+1	t+0	
X	X	X	0	Data
X	0	0	1	CRC High Byte
0	0	1	1	CRC Low Byte
X	X	1	1	Preset CRC
X	1	0	1	Command
1	0	1	1	Command

The CRC block implements the CRC-16 function in a byte-parallel fashion. This allows a full byte to be accumulated in a single clock cycle. While this does require a much larger number of XOR gates to implement than a serial CRC function, it allows the design to be constructed from much slower logic. Here the main CRC register is clocked at 20 MHz, rather than having to operate at a 200-MHz bit-clock rate. The VHDL source code for this function is listed in Appendix B.

The command-translate block is not normally needed for new designs. For this specific design it was necessary to translate an existing set of command codes to the native HOTLink command set. This translation is quite simple with the logic reduction performed manually for the transmit path. Here an 8-bit input command is decoded into a 4-bit command field (with the upper four bits of the byte set to zero).

The translation block actually implements circuitry to translate all twelve command codes in the 8B/10B character set. For ESCON implementations this logic could be simplified because only half of these (six) are actually allowed for use in ESCON ordered sets. The VHDL source code for this function is listed in Appendix D.

The last section in the transmit path is the output pipeline register. This block receives the multiplexed output of either the input pipeline register, the high-CRC byte, the low-CRC byte, or the translated command. It serves to keep the data presented to the HOTLink transmitter synchronous with the transmit clock.

Receive Path

A block diagram of the receive path is shown in *Figure 10.* Data is captured from the HOTLink receiver into the input register on each falling edge of the HOTLink recovered receive clock (CKR). Note that this could also be implemented using a rising edge clock, but that a falling edge clock was used for compatibility with the implementation being replaced.

All received data characters are clocked into the CRC register. Like the transmit path, this function is implemented in a byte-parallel form. The CRC register is synchronously preset if any command code is present in the input register. For all data codes it accumulates the CRC remainder.

The CRC register is constantly compared for the x'1D0F' pattern. The output of this compare is clocked into the output register. It is forced to a LOW for all clocks except the first command character received following a data character. This CRC status remains valid for only one clock cycle. The

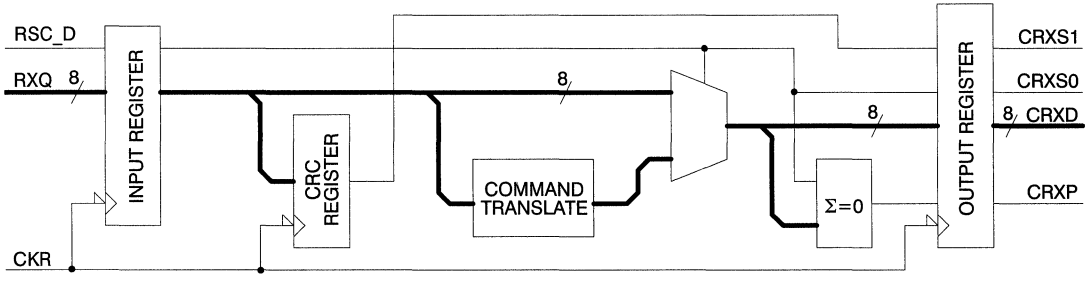


Figure 10. pASIC Receive Path Block Diagram

VHDL source code for this function is listed in Appendix E.

Just as in the transmit path, a command translation block is present in the design. This command translate block is not normally needed for new designs. For this specific design it was necessary to translate an existing set of command codes from the native HOTLink command set to a different set of command codes embedded in upstream logic. This block allows the HOTLink command codes to be translated to any host command set.

The translation block actually implements circuitry to translate all twelve command codes in the 8B/10B character set. For ESCON implementations this logic could be simplified because only half of these (six) are actually allowed for use in ESCON ordered sets. The VHDL source code for this function is listed in Appendix D.

Odd parity is generated on the output data byte and the CRXS0 status bit. This allows upstream logic to validate that the byte received is the same as that generated by the pASIC FPGA.

The last block in the receive section is the output pipeline register. This block receives the multiplexed output of either the input pipeline register or the translated command. It serves to keep the data presented to the upstream logic synchronous with the receive clock.

Byte-Sync State Machine

A block diagram of the byte-sync state machine is shown in *Figure 11*. The two primary structures in the machine are a 4-bit counter and a controlling state machine. The controlling state machine is programmed to follow the state diagram shown in *Figure 11*. It tracks the state of the RVS signal from the receiver and a decode from the input register of all C5.0 command codes (Idle characters). The four-bit counter is used to alternately count either valid characters (the absence of RVS) or valid Idle characters, based on the state of the machine.

The present form of this state machine was designed to duplicate the functionality of a previous implementation. Because of this it does not take into account the the additional condition of Signal Detected that is generated by the fiber-optic receiver. Sufficient I/O and logic resources are still available in the FPGA to add this into the state machine equations.

Design Summary

The small size of the FPGA design is made possible by the enhanced functionality present in the HOTLink transmitter and receiver. This removes the need to design and implement the 8B/10B encoders and decoders, and provides full received character validation. The embedded PECL-to-TTL converter also allows a small footprint by removing the need for an external conversion circuit.

The VHDL design both auto-routes and auto-places into a pASIC383 FPGA. Because of the high-speed operation of the pASIC cells and interconnect, this design meets or exceeds all design performance parameters, over worst case temperature and voltage, using the slow −0 speed bin of the pASIC383.

The 100% routability of the pASIC family allows the circuit board signal routing to be improved by selecting pins that best match the system interconnect. The pinouts listed in the top-level VHDL file were selected to allow straight-through routing (no crossovers) of the signals between the FPGA and the HOTLink transmitter and receiver. In addition, the

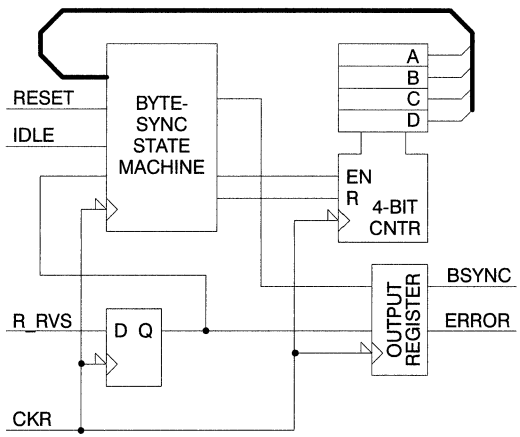


Figure 11. Byte-Sync State Machine Block Diagram

placement of the HOTLink transmitter and receiver were selected to line up with the transmit and receive halves of the fiber-optic transceiver. This pinout selection and interconnect are shown in *Figure 12*.

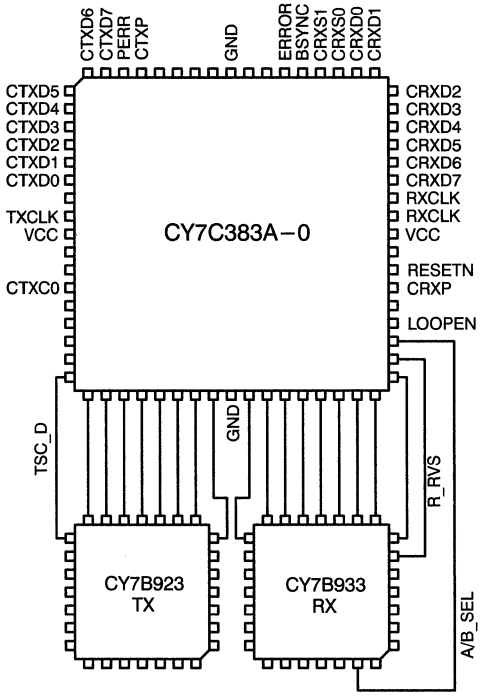


Figure 12. HOTLink/pASIC Pinout and Interconnect

Conclusions

The ESCON interface is both an elegant and powerful replacement for the older block-mux channels. The use of the HOTLink serializer/deserializer components to implement an ESCON interface guarantees both compliance with the 8B/10B coding rules and all jitter and timing specifications of the ESCON interface.

Due to the high-speed operation of the ESCON interface, the byte-level control is best implemented in hardware. The flexibility of the VHDL language and the unlimited routing of the Cypress pASIC family of FPGAs make them a perfect choice for building the control state machines. While only the lower level of the ESCON protocol is controlled in the design documented here, much of the higher level control may also be implemented through the use of either larger or additional FPGA components.

References

1. *ESCON I/O Interface*, IBM, 1990, 1991
2. *HOTLink User's Guide,* Cypress Semiconductor, 1995
3. *GA9104 Datasheet,* Triquint Semiconductor, Inc, 1992

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IBM is a registered trademark of International Business Machines, Inc.

Appendix A. Top-Level pASIC Code

```
-- ESC_TOP.VHD
--
-- ESCON Interface Control PLD
-- Equivalent to the Triquint GA9104 but designed for operation
-- with the Cypress Semiconductor HOTLink chipset
ENTITY esc_top IS PORT (
  txclk: IN BIT;                    -- transmit path byte clock
  rxclkA: IN BIT;                   -- receiver path byte clock
  rxclkB: IN BIT;                   -- receiver path byte clock
  resetn: IN BIT;                   -- active low reset
  rxq: INOUT X01Z_VECTOR(0 TO 7);   -- HOTLink receiver data in
  rsc_d: INOUT X01Z;                -- HOTLink receiver SC/D
  r_rvs: INOUT X01Z;                -- HOTLink receiver RVS
  txd: INOUT X01Z_VECTOR(0 TO 7);   -- HOTLink transmitter data out
  tsc_d: INOUT X01Z;                -- HOTLink transmitter SC/D
  crxd: INOUT X01Z_VECTOR(0 TO 7); -- receive path data output
  ctxd: INOUT X01Z_VECTOR(0 TO 7); -- transmit path data input
  crxs0: INOUT X01Z;                -- receive status 0 (command/data)
  crxs1: INOUT X01Z;                -- receive status 1 (CRC)
  ctxc0: INOUT X01Z;                -- transmit control 0 (command/data)
  bsync: INOUT X01Z;                -- byte sync acquired
  error: INOUT X01Z;                -- receive bad character error
  perr: INOUT X01Z;                 -- transmit-in parity error
  crxp: INOUT X01Z;                 -- odd parity output
  ctxp: INOUT X01Z;                 -- odd parity input
  loopen: INOUT X01Z;               -- local loopback enable
  ab_sel: INOUT X01Z);              -- receiver A/B select

ATTRIBUTE part_name OF esc_top:ENTITY IS "C383A";
ATTRIBUTE pin_numbers OF esc_top:ENTITY IS
    "txclk:17 rxclkA:53 rxclkB:54 resetn:50 rxq(7):44 rxq(6):43 "
  & "rxq(5):42 rxq(4):41 rxq(3):40 rxq(2):39 rxq(1):38 rxq(0):37 "
  & "rsc_d:36 r_rvs:45 txd(7):34 txd(6):33 txd(5):32 txd(4):31 "
  & "txd(3):30 txd(2):29 txd(1):28 txd(0):27 tsc_d:26 crxd(0):62 "
  & "crxd(1):61 crxd(2):60 crxd(3):59 crxd(4):58 crxd(5):57 "
  & "crxd(6):56 crxd(7):55 ctxd(0):15 ctxd(1):14 ctxd(2):13 "
  & "ctxd(3):12 ctxd(4):11 ctxd(5):10 ctxd(6):9 ctxd(7):8 "
  & "crxs0:63 crxs1:64 ctxc0:21 bsync:65 error:66 perr:7 "
  & "crxp:49 ctxp:6 loopen:47 ab_sel:46";

END esc_top;

USE work.cypress.all;
USE work.rtlpkg.all;
USE work.memorypkg.all;
USE work.ttlpkg.all;
USE work.registerpkg.all;
```

Appendix A. Top-Level pASIC Code (continued)

```
USE work.iopkg.all;
USE work.mcpartspkg.all;
USE work.gatespkg.all;
USE work.resolutionpkg.all;     -- used to double-buffer
USE work.bv_math.all;           -- allow use of INV function
USE work.crc_t.all;             -- add in CRC transmit function
USE work.crc_r.all;             -- add in CRC receive function
USE work.crc_ctl.all;           -- add in transmit CRC control machine
USE work.sync_det.all;          -- add in SYNC detect state machine
USE work.trig_code.all;         -- add in command decoder section
USE work.iopluspkg.all;         -- add in enhanced I/O buffers

ARCHITECTURE escon_top OF esc_top IS
-- add internal signal equivalents of signals after I/O pads
SIGNAL tclk : BIT;                  -- transmit clock
SIGNAL rclk : BIT;                  -- negative edge receiver clock
SIGNAL reset : BIT;                 -- reset controller
SIGNAL HL_rx : BIT_VECTOR(0 to 7); -- HOTLink receiver data bus
SIGNAL HL_rsc_d : BIT;              -- HOTLink receiver SC/D
SIGNAL HL_r_rvs : BIT;              -- HOTlink receiver RVS
SIGNAL HL_tx : BIT_VECTOR(0 to 7); -- HOTLink transmitter data bus
SIGNAL HL_tsc_d : BIT;              -- HOTLink transmitter SC/D
SIGNAL HL_tsc_q : BIT;              -- clocked HOTLink transmitter SC/D
SIGNAL sync_r : BIT;                -- receiver byte sync
SIGNAL c_rxd : BIT_VECTOR(0 to 7); -- controller receive path data out
SIGNAL c_txd : BIT_VECTOR(0 to 7); -- controller transmit path dataout
SIGNAL c_rxs0 : BIT;                -- receive status 0 (command/data)
SIGNAL c_rxs1 : BIT;                -- receive status 1 (CRC)
SIGNAL c_txc0 : BIT;                -- transmit control 0 (command/data)
SIGNAL b_sync : BIT;                -- byte sync acquired
SIGNAL r_error : BIT;               -- receive bad character error
SIGNAL p_err : BIT;                 -- parity error
SIGNAL c_rxp : BIT;                 -- odd parity output
SIGNAL c_txp : BIT;                 -- odd parity input
SIGNAL b_loopen : BIT;              -- buffered loop enable

-- transmit internal signals
SIGNAL t_data : BIT_VECTOR(0 TO 7);   -- transmit data bus
SIGNAL t_mux : BIT_VECTOR(0 TO 7);    -- muxed transmit data path
SIGNAL t_comm : BIT_VECTOR(0 TO 7);   -- re-encoded transmit commands
SIGNAL tp_odd : BIT;                  -- transmit data parity input
SIGNAL t_parity : BIT;                -- transmit parity checker output
```

Appendix A. Top-Level pASIC Code (continued)

```
SIGNAL t_CRC : BIT_VECTOR(0 TO 7);    -- transmit CRC vector
SIGNAL c_txc_0 : BIT;                 -- transmit command/data
SIGNAL mux_hi : BIT;                  -- enable HI/LOW transmit CRC byte
SIGNAL mux_low : BIT;                 -- enable LOW transmit CRC byte
sIGNAL ctxc3 : BIT;                   -- 3x registered c_txc_0
SIGNAL t_CRC_reset : BIT;             -- preset transmit CRC register
-- receive internal signals
SIGNAL r_data : BIT_VECTOR(0 TO 7);   -- registered receiver data bus
SIGNAL r_mux : BIT_VECTOR(0 TO 7);    -- muxed data and translated commands
SIGNAL rp_odd : BIT;                  -- receive data parity output
SIGNAL rcom_data : BIT;               -- registered SC/D pin
SIGNAL r_com_data: multi_buffer BIT;  -- double buffered registerd SC/D pin
SIGNAL r_crc_err : BIT;               -- un-registered CRC status
SIGNAL r_CRC_d : BIT;                 -- CRC check D-input
SIGNAL rvs : BIT;                     -- registered RVS signal
SIGNAL sync : BIT;                    -- decoded K28.5 signal
SIGNAL t_code : BIT_VECTOR(0 to 7);   -- Triquint pattern for K-codes

-------------------------------------------------------------------------
-------------------------------------------------------------------------
BEGIN
-- instantiate pASIC buffers/drivers on I/O signals
-- clocks
p1: CKPAD PORT MAP (txclk, tclk);       -- transmit path clock
p2: HDI2PAD PORT MAP (rxclkA, rxclkB, rclk); -- receive path clock on
                                             -- on negative edge
-- high drive pads
p3: HDIPAD PORT MAP (resetn ,reset);    -- active HIGH system reset
-- data buses
-- HOTLink receiver data bus (input)
p4:  INPAD PORT MAP (rxq(0), HL_rx(0));
p5:  INPAD PORT MAP (rxq(1), HL_rx(1));
p6:  INPAD PORT MAP (rxq(2), HL_rx(2));
p7:  INPAD PORT MAP (rxq(3), HL_rx(3));
p8:  INPAD PORT MAP (rxq(4), HL_rx(4));
p9:  INPAD PORT MAP (rxq(5), HL_rx(5));
p10: INPAD PORT MAP (rxq(6), HL_rx(6));
p11: INPAD PORT MAP (rxq(7), HL_rx(7));
p12: INPAD PORT MAP (rsc_d,  HL_rsc_d);       -- receive SC/D
p13: INPAD PORT MAP (r_rvs,  HL_r_rvs);       -- RVS
-- HOTLink transmitter data bus (output)
p14: OUTPAD PORT MAP (HL_tx(0), txd(0));
p15: OUTPAD PORT MAP (HL_tx(1), txd(1));
p16: OUTPAD PORT MAP (HL_tx(2), txd(2));
p17: OUTPAD PORT MAP (HL_tx(3), txd(3));
p18: OUTPAD PORT MAP (HL_tx(4), txd(4));
p19: OUTPAD PORT MAP (HL_tx(5), txd(5));
```

Appendix A. Top-Level pASIC Code (continued)

```
p20: OUTPAD PORT MAP (HL_tx(6), txd(6));
p21: OUTPAD PORT MAP (HL_tx(7), txd(7));
p22: OUTPAD PORT MAP (HL_tsc_q, tsc_d);
-- controller transmit data bus (input)
p24: INPAD PORT MAP (ctxd(0), c_txd(0));
p25: INPAD PORT MAP (ctxd(1), c_txd(1));
p26: INPAD PORT MAP (ctxd(2), c_txd(2));
p27: INPAD PORT MAP (ctxd(3), c_txd(3));
p28: INPAD PORT MAP (ctxd(4), c_txd(4));
p29: INPAD PORT MAP (ctxd(5), c_txd(5));
p30: INPAD PORT MAP (ctxd(6), c_txd(6));
p31: INPAD PORT MAP (ctxd(7), c_txd(7));
-- controller receiver data bus (output)
p34: OUTPAD PORT MAP (c_rxd(0), crxd(0));
p35: OUTPAD PORT MAP (c_rxd(1), crxd(1));
p36: OUTPAD PORT MAP (c_rxd(2), crxd(2));
p37: OUTPAD PORT MAP (c_rxd(3), crxd(3));
p38: OUTPAD PORT MAP (c_rxd(4), crxd(4));
p39: OUTPAD PORT MAP (c_rxd(5), crxd(5));
p40: OUTPAD PORT MAP (c_rxd(6), crxd(6));
p41: OUTPAD PORT MAP (c_rxd(7), crxd(7));
-- misc input pads
p44: INPAD PORT MAP (loopen, b_loopen); -- loopback enable
p45: INPAD PORT MAP (ctxc0, c_txc0);    -- transmit control 0
p49: INPAD PORT MAP (ctxp, c_txp);      -- odd parity input
-- misc output pads
p50: OUTPAD PORT MAP (c_rxs0, crxs0);   -- receiver status 0 output
p51: OUTPAD PORT MAP (c_rxs1, crxs1);   -- receiver status 1 output
p53: OUTPAD PORT MAP (b_sync, bsync);   -- byte sync acquired
p54: OUTPAD PORT MAP (r_error, error);  -- received bad character
p55: OUTPAD PORT MAP (p_err, perr);     -- parity error
p56: OUTPAD PORT MAP (c_rxp, crxp);     -- odd parity output
p57: OUTPAD PORT MAP (INV(b_loopen),ab_sel); -- HOTLink receiver A/B select
-------------------------------------------------------------------------
-------------- TRANSMIT PATH --------------------------------------------
-------------------------------------------------------------------------
-- add in transmit path input data pipeline register
t1a: DFF PORT MAP (c_txd(0), tclk, t_data(0));
t1b: DFF PORT MAP (c_txd(1), tclk, t_data(1));
t1c: DFF PORT MAP (c_txd(2), tclk, t_data(2));
t1d: DFF PORT MAP (c_txd(3), tclk, t_data(3));
t1e: DFF PORT MAP (c_txd(4), tclk, t_data(4));
t1f: DFF PORT MAP (c_txd(5), tclk, t_data(5));
t1g: DFF PORT MAP (c_txd(6), tclk, t_data(6));
t1h: DFF PORT MAP (c_txd(7), tclk, t_data(7));
```

Appendix A. Top-Level pASIC Code (continued)

```
-- add parity and control bits
t1j: DFF PORT MAP (c_txp, tclk, tp_odd);
t1k: DFF PORT MAP (c_txc0, tclk, c_txc_0);
-------------------------------------------------------------------------
-- add transmit data parity checker (10 bit parity tree)
t_parity <= NOT(t_data(0) XOR t_data(1) XOR t_data(2) XOR t_data(3)
  XOR t_data(4) XOR t_data(5) XOR t_data(6) XOR t_data(7)
  XOR tp_odd XOR c_txc_0);
-------------------------------------------------------------------------
-- add parity check F-F
t2: DFF PORT MAP (
  t_parity,                          -- parity of inputs
  tclk,                              -- transmit clock
  p_err);                            -- output parity status
-------------------------------------------------------------------------
-- add transmitter CRC generator
t3: crc_tx PORT MAP (
  tclk,                          -- transmit clock
  t_CRC_reset,                   -- from tx CRC control state machine
  c_txc_0,                       -- from tx input register
  mux_hi,                        -- enable low byte onto bus
  t_data,                        -- transmit data bus
  t_CRC);                        -- 8-bit transmit CRC output vector
t_CRC_reset <= '0' WHEN (c_txc_0 = '0' OR mux_hi = '0') ELSE '1';
-------------------------------------------------------------------------
-- add transmit output register
t5a: DFF PORT MAP (t_mux(0), tclk, HL_tx(0));
t5b: DFF PORT MAP (t_mux(1), tclk, HL_tx(1));
t5c: DFF PORT MAP (t_mux(2), tclk, HL_tx(2));
t5d: DFF PORT MAP (t_mux(3), tclk, HL_tx(3));
t5e: DFF PORT MAP (t_mux(4), tclk, HL_tx(4));
t5f: DFF PORT MAP (t_mux(5), tclk, HL_tx(5));
t5g: DFF PORT MAP (t_mux(6), tclk, HL_tx(6));
t5h: DFF PORT MAP (t_mux(7), tclk, HL_tx(7));
HL_tsc_d <= (mux_low AND c_txc_0) OR
            (c_txc_0 AND mux_hi AND ctxc3);
-- add in SC/D output bit
t5j: DFF PORT MAP (HL_tsc_d, tclk, HL_tsc_q);

-------------------------------------------------------------------------
-- add in transmit CRC supervisor machine
-- contains the double pipelined C/D bit
t6: tx_ctl_crc PORT MAP (
  tclk,                    -- transmit clock
  c_txc_0,                 -- registerd command/data control bit
  mux_hi,                  -- registered c_txc_0
  mux_low);                -- 2x registered c_txc_0
```

Appendix A. Top-Level pASIC Code (continued)

```
-------------------------------------------------------------------------
-- transmit path data/command/CRC mux
t8: PROCESS (c_txc_0, mux_low, mux_hi)
BEGIN
  IF (c_txc_0 = '0') THEN
    t_mux <= t_data;
  ELSIF (c_txc_0 = '1' AND ((mux_low = '0' AND mux_hi='0') OR
        (ctxc3 = '0' AND mux_low = '0' AND mux_hi = '1'))) THEN
    -- output CRC bytes
    t_mux <= t_CRC;
  ELSE
    -- output re-encoded command codes
    t_mux <= t_comm;
  END IF;
END PROCESS t8;

-- Add in transmit command decoder
t9: t_decode PORT MAP (t_data, t_comm); -- translate to HOTLink commands

-------------------------------------------------------------------------
-------------- RECEIVE PATH -------------------------------------------
-------------------------------------------------------------------------
-- add in receive path input data pipeline register
r1a: DFF PORT MAP (HL_rx(0), rclk, r_data(0));
r1b: DFF PORT MAP (HL_rx(1), rclk, r_data(1));
r1c: DFF PORT MAP (HL_rx(2), rclk, r_data(2));
r1d: DFF PORT MAP (HL_rx(3), rclk, r_data(3));
r1e: DFF PORT MAP (HL_rx(4), rclk, r_data(4));
r1f: DFF PORT MAP (HL_rx(5), rclk, r_data(5));
r1g: DFF PORT MAP (HL_rx(6), rclk, r_data(6));
r1h: DFF PORT MAP (HL_rx(7), rclk, r_data(7)); -- add SC/D bit and RVS
r1j: DFF PORT MAP (HL_rsc_d, rclk, rcom_data); -- registerd SC/D
r1k: DFF PORT MAP (HL_r_rvs, rclk, rvs);        -- registered RVS signal
-- create double buffered signals
db1: BUF PORT MAP (rcom_data, r_com_data);
db2: BUF PORT MAP (rcom_data, r_com_data);
-------------------------------------------------------------------------
-- receive path output register
r2a: DFF PORT MAP (r_mux(0), rclk, c_rxd(0));
r2b: DFF PORT MAP (r_mux(1), rclk, c_rxd(1));
r2c: DFF PORT MAP (r_mux(2), rclk, c_rxd(2));
r2d: DFF PORT MAP (r_mux(3), rclk, c_rxd(3));
r2e: DFF PORT MAP (r_mux(4), rclk, c_rxd(4));
r2f: DFF PORT MAP (r_mux(5), rclk, c_rxd(5));
r2g: DFF PORT MAP (r_mux(6), rclk, c_rxd(6));
r2h: DFF PORT MAP (r_mux(7), rclk, c_rxd(7));-- command/data bit and rvs
r2j: DFF PORT MAP (r_com_data, rclk, c_rxs0);
r2k: DFF PORT MAP (rvs, rclk, r_error);
```

Appendix A. Top-Level pASIC Code (continued)

```
-------------------------------------------------------------------------------
-- add receive parity generate
r3: TTL180 PORT MAP (
  r_mux(0), r_mux(1), r_mux(2), r_mux(3), r_mux(4), r_mux(5),
  r_mux(6), r_mux(7), INV(r_com_data), r_com_data, rp_odd, open);

r3a: DFF PORT MAP (rp_odd, rclk, c_rxp);
-------------------------------------------------------------------------------
-- add in receive CRC block
r4: crc_rx PORT MAP (
  rclk,                    -- receive path clock
  r_com_data,              -- enable only for data bytes
  r_data,                  -- receiver data bus
  r_crc_err);              -- receive path crc status
-------------------------------------------------------------------------------
-- add CRC check register
r5: DFF PORT MAP (r_CRC_d, rclk, c_rxs1);
r_CRC_d <= r_crc_err AND r_com_data AND (NOT(c_rxs0));
-------------------------------------------------------------------------------
-- add in byte-sync state machine
r6: byte_syn PORT MAP (
  rclk,                    -- receiver clock
  reset,                   -- system reset
  rvs,                     -- receiver RVS signal
  sync,                    -- decoded k28.5
  b_sync);                 -- byte sync acquired

sync <= '1' WHEN (r_com_data='1' AND r_data(0 TO 3)="1010") ELSE '0';
-------------------------------------------------------------------------------
-- add command transposition logic and mux
r7: PROCESS (r_com_data, r_data(0), r_data(1), r_data(2), r_data(3))
BEGIN
  IF (r_com_data='0') THEN
    r_mux <= r_data;
  ELSE
    r_mux <= t_code;         -- add in command decoder
  END IF;
END PROCESS r7;
-------------------------------------------------------------------------------
-- add receiver path command encoder
-- t_code is output vector
r8: t_encode PORT MAP (
  r_data,                  -- HOTLink data bus
  t_code);                 -- decoded Triquint commands

END escon_top;
```

Appendix B. Transmit Path CRC Generator

```
-- CRC_T.VHD
--
-- transmit 16-bit CCITT CRC for use in data mover
--
-- When sequencing bytes out, the qt(15)-qt(8) byte must be sent out first.
-- Per the ESCON spec, the CRC is the 1's compliment (inversion) of the
-- qt[15:0] bus.
--
PACKAGE crc_T IS
  COMPONENT crc_tx PORT (
  clk,                        -- system clock
  preset: IN      BIT;        -- synchronous preset, set to all 1s
  enable: IN      BIT;        -- enable when not a command byte
  mux_hi: IN      BIT;        -- enable high-byte onto bus
  dt:     IN      BIT_VECTOR (0 TO 7); -- Input data byte
  q_out:  OUT     BIT_VECTOR (0 TO 7)  -- CRC register
  );
  END COMPONENT;
END crc_T;

use work.rtlpkg.all;
use work.cypress.all;

ENTITY crc_tx IS PORT (
  clk,                        -- system clock
  preset: IN      BIT;        -- synchronous reset, set to all 1s
  enable: IN      BIT;        -- enable when not a command byte
  mux_hi: IN      BIT;        -- enable high CRC byte out
  dt:     IN      BIT_VECTOR (0 TO 7); -- Input data byte
  q_out:  OUT     BIT_VECTOR (0 TO 7)  -- CRC register
  );
END crc_tx;

ARCHITECTURE ccitt_tx OF crc_tx IS
SIGNAL qt: BIT_VECTOR (0 TO 15); -- CRC register
BEGIN
proc1: PROCESS BEGIN
  WAIT UNTIL (clk='1');
    IF (preset='1') THEN
      qt <= x"FFFF";      -- Preset to 1's for reset
    ELSIF (enable='1') THEN
      qt <= qt;           -- keep same value
    ELSE
      qt(0) <= qt(8) XOR qt(12) XOR dt(3) XOR dt(7);
      qt(1) <= qt(9) XOR qt(13) XOR dt(2) XOR dt(6);
      qt(2) <= qt(10) XOR qt(14) XOR dt(1) XOR dt(5);
      qt(3) <= qt(11) XOR qt(15) XOR dt(0) XOR dt(4);
```

Appendix B. Transmit Path CRC Generator (continued)

```
      qt(4) <= qt(12) XOR dt(3);
      qt(5) <= qt(13) XOR qt(12) XOR qt(8) XOR dt(7) XOR dt(3) XOR dt(2);
      qt(6) <= qt(14) XOR qt(13) XOR qt(9) XOR dt(1)XOR dt(2) XOR dt(6);
      qt(7) <= qt(15) XOR qt(14) XOR qt(10) XOR dt(0) XOR dt(1) XOR dt(5);
      qt(8) <= qt(15) XOR qt(11) XOR qt(0) XOR dt(0) XOR dt(4);
      qt(9) <= qt(12) XOR qt(1) XOR dt(3);
      qt(10) <= qt(13) XOR qt(2) XOR dt(2);
      qt(11) <= qt(14) XOR qt(3) XOR dt(1);
      qt(12) <= qt(15) XOR qt(12) XOR qt(8) XOR qt(4)
                XOR dt(0) XOR dt(3) XOR dt(7);
      qt(13) <= qt(13) XOR qt(9) XOR qt(5) XOR dt(2) XOR dt(6);
      qt(14) <= qt(14) XOR qt(10) XOR qt(6) XOR dt(1) XOR dt(5);
      qt(15) <= qt(15) XOR qt(11) XOR qt(7) XOR dt(0) XOR dt(4);
    END IF;
END PROCESS;

-- mux and Invert CRC and swap bits
m1: PROCESS (mux_hi)
BEGIN
-- Mux out high and low bytes and transpose bit order
IF mux_hi = '0' THEN
  q_out(7) <= not qt(8);
  q_out(6) <= not qt(9);
  q_out(5) <= not qt(10);
  q_out(4) <= not qt(11);
  q_out(3) <= not qt(12);
  q_out(2) <= not qt(13);
  q_out(1) <= not qt(14);
  q_out(0) <= not qt(15);
ELSE
  q_out(7) <= not qt(0);
  q_out(6) <= not qt(1);
  q_out(5) <= not qt(2);
  q_out(4) <= not qt(3);
  q_out(3) <= not qt(4);
  q_out(2) <= not qt(5);
  q_out(1) <= not qt(6);
  q_out(0) <= not qt(7);
END IF;
END PROCESS m1;

END ccitt_tx;
```

Appendix C. Transmit Path CRC Controler

```
-- CTL_CRCT.VHD
--
-- Control transmit CRC function
--
--
-- All actions are based on the CTXC0 input.  This input is active
-- at the end of every data sequence and is a 1 (HIGH) for all
-- non-data bytes.
--

PACKAGE crc_ctl IS
  COMPONENT tx_ctl_crc PORT (
  clk,                      -- transmit clock
  ctxc0: IN BIT;            -- command/data control bit
  ctxc1,                    -- registered ctxc0
  ctxc2,                    -- 2x registered ctxc0
  ctxc3: OUT BIT);          -- 3x registered ctxc0
  END COMPONENT;
END crc_ctl;

ENTITY tx_ctl_crc IS PORT (
  clk,                      -- transmit clock
  ctxc0: IN BIT;            -- command/data control bit
  ctxc1,                    -- registered ctxc0
  ctxc2,                    -- 2x registered ctxc0
  ctxc3: OUT BIT);          -- 3x registered ctxc0
END tx_ctl_crc;

USE work.cypress.all;
USE work.rtlpkg.all;

ARCHITECTURE ctl_1 OF tx_ctl_crc IS

SIGNAL cq1: BIT;                -- single registered c/d
SIGNAL cq2: BIT;                -- double registered c/d

BEGIN

-- Instantiate DFF to track status of ctxc0 bit
d1: DFF PORT MAP (ctxc0, clk, cq1);
d2: DFF PORT MAP (cq1, clk, cq2);
d3: DFF PORT MAP (cq2, clk, ctxc3);

-- assign outputs
ctxc1 <= cq1;
ctxc2 <= cq2;

END ctl_1;
```

Appendix D. Command Mapper

```
-- TRI_CODE.VHD
--
-- Command decode/translate between the Triquint GA9104 and HOTLink
-- K-code command sets

--------------------------------------------------------------------------
-- Triquint/Cypress Command mapping
--          GA9104          HOTLink HEX
--          HEX BIN         TX RX        BIN
-- k28.0*   1C 00011100     00           00000000
-- k28.1    3C 00111100     01           00000001
-- k28.2    5C 01011100     02           00000010
-- k28.3*   7C 01111100     03           00000011
-- k28.4    9C 10011100     04           00000100
-- k28.5    BC 10111100     05,E1,E2     00000101
-- k28.6    DC 11011100     06           00000110
-- k28.7    FC 11111100     07,27,47     00000111
-- k23.7*   F7 11110111     08           00001000
-- k27.7*   FB 11111011     09           00001001
-- k29.7*   FD 11111101     0A           00001010
-- k30.7*   FE 11111110     0B           00001011
-- * - Illegal for use in ESCON operations

PACKAGE triq_code IS
  COMPONENT t_encode PORT (
  c_code : IN BIT_VECTOR(0 TO 7); -- Cypress HOTLink C-codes
  t_code : OUT BIT_VECTOR(0 TO 7) -- Triquint K-codes
  );
  END COMPONENT;

  COMPONENT t_decode PORT (
  t_data : IN BIT_VECTOR(0 TO 7); -- Triquint K-codes
  t_comm : OUT BIT_VECTOR(0 TO 7) -- Cypress HOTLink C-codes
  );
  END COMPONENT;
END triq_code;

USE work.cypress.all;
USE work.table_bv.all;          -- use for command encoder

ENTITY t_encode IS PORT (
  c_code : IN BIT_VECTOR(0 TO 7); -- Cypress HOTLink C-codes
  t_code : OUT BIT_VECTOR(0 TO 7) -- Triquint K-codes
  );
END t_encode;
```

Appendix D. Command Mapper (continued)

```
ARCHITECTURE t_encoder OF t_encode IS
-- use TTF function to translate from one command set to the other
-- Command constants
-- T-codes (output vectors)
CONSTANT K28_0: x01_VECTOR(0 TO 7) := "00111000";
CONSTANT K28_1: x01_VECTOR(0 TO 7) := "00111100";
CONSTANT K28_2: x01_VECTOR(0 TO 7) := "00111010";
CONSTANT K28_3: x01_VECTOR(0 TO 7) := "00111110";
CONSTANT K28_4: x01_VECTOR(0 TO 7) := "00111001";
CONSTANT K28_5: x01_VECTOR(0 TO 7) := "00111101";
CONSTANT K28_6: x01_VECTOR(0 TO 7) := "00111011";
CONSTANT K28_7: x01_VECTOR(0 TO 7) := "00111111";
CONSTANT K23_7: x01_VECTOR(0 TO 7) := "11101111";
CONSTANT K27_7: x01_VECTOR(0 TO 7) := "11011111";
CONSTANT K29_7: x01_VECTOR(0 TO 7) := "10111111";
CONSTANT K30_7: x01_VECTOR(0 TO 7) := "01111111";
-- C-codes (input vectors)
CONSTANT C00_0: x01_VECTOR(0 TO 7) := "0000xxxx";
CONSTANT C01_0: x01_VECTOR(0 TO 7) := "1000xxx0";
CONSTANT C02_0: x01_VECTOR(0 TO 7) := "0100xxx0";
CONSTANT C03_0: x01_VECTOR(0 TO 7) := "1100xxxx";
CONSTANT C04_0: x01_VECTOR(0 TO 7) := "0010xxxx";
CONSTANT C05_0: x01_VECTOR(0 TO 7) := "1010xxxx";
CONSTANT C06_0: x01_VECTOR(0 TO 7) := "0110xxxx";
CONSTANT C07_0: x01_VECTOR(0 TO 7) := "1110xxxx";
CONSTANT C08_0: x01_VECTOR(0 TO 7) := "0001xxxx";
CONSTANT C09_0: x01_VECTOR(0 TO 7) := "1001xxxx";
CONSTANT C10_0: x01_VECTOR(0 TO 7) := "0101xxxx";
CONSTANT C11_0: x01_VECTOR(0 TO 7) := "1101xxxx";
CONSTANT C12_0: x01_VECTOR(0 TO 7) := "0011xxxx";
-- errors and special mappings
CONSTANT C01_7: x01_VECTOR(0 TO 7) := "1000xxx1";
CONSTANT C02_7: x01_VECTOR(0 TO 7) := "0100xxx1";

CONSTANT table: x01_TABLE(0 TO 13, 0 TO 15) := (   -- command mappings
--          Command
--       Input   Output
--       -----   ------
         C00_0 & K28_0,
         C01_0 & K28_1,
         C02_0 & K28_2,
         C03_0 & K28_3,
         C04_0 & K28_4,
         C05_0 & K28_5,
         C06_0 & K28_6,
         C07_0 & K28_7,
```

Appendix D. Command Mapper (continued)

```
        C08_0 & K23_7,
        C09_0 & K27_7,
        C10_0 & K29_7,
        C11_0 & K30_7,
        C01_7 & K28_5,
        C02_7 & K28_5);

BEGIN
p1: PROCESS (c_code)
  BEGIN
    t_code <= ttf(table,(c_code));
  END PROCESS p1;
END t_encoder;

USE work.cypress.all;

ENTITY t_decode IS PORT (
  t_data : IN BIT_VECTOR(0 TO 7); -- Triquint K-codes
  t_comm : OUT BIT_VECTOR(0 TO 7) -- Cypress HOTLink C-codes
  );
END t_decode;

ARCHITECTURE t_decoder OF t_decode IS

BEGIN

t_comm(7) <= '0';
t_comm(6) <= '0';
t_comm(5) <= '0';
t_comm(4) <= '0';
t_comm(3) <= '0' WHEN (t_data(0 TO 1) = "00") ELSE '1';
t_comm(2) <= '1' WHEN ((t_data(7) = '1')
             AND (t_data(0 TO 1) = "00")) ELSE '0';

t1: PROCESS (t_data(0), t_data(1), t_data(6),
          t_data(5), t_data(3), t_data(2))
  BEGIN
    IF (t_data(0 TO 1) = "00") THEN
      t_comm(1) <= t_data(6);
      t_comm(0) <= t_data(5);
    ELSE
      t_comm(1) <= t_data(3) AND t_data(2);
      t_comm(0) <= t_data(2) AND t_data(0);
    END IF;
  END PROCESS t1;

END t_decoder;
```

Appendix E. Receive Path CRC Checker

```
-- CRC_R.VHD
--
-- receiver 16-bit CCITT CRC for use in data mover
PACKAGE crc_r IS
  COMPONENT crc_rx PORT (
  clk,                    -- system clock
  preset: IN      BIT;    -- synchronous reset, set to all 1s
  dr:      IN      BIT_VECTOR (0 TO 7); -- Input data byte
  crc_err:  OUT   BIT     -- error detected
  );
  END COMPONENT;
END crc_r;

use work.rtlpkg.all;
use work.cypress.all;

ENTITY crc_rx IS PORT (
  clk,                    -- system clock
  preset:  IN BIT;        -- synchronous preset, set to all 1s
  dr:      IN      BIT_VECTOR (0 TO 7); -- Input data byte
  crc_err:  OUT   BIT     -- error detected
  );
END crc_rx;

ARCHITECTURE ccitt_rx OF crc_rx IS
-- declare CRC register
SIGNAL qr: BIT_VECTOR (0 TO 15);    -- CRC register
ATTRIBUTE POLARITY OF qr:SIGNAL IS PL_KEEP;  -- maintain polarity f
BEGIN
proc1: PROCESS BEGIN
  WAIT UNTIL (clk='1');
    IF (preset='1') THEN
      qr <= x"FFFF";     -- Preset to 1's for reset
    ELSE
      qr(0) <= qr(8) XOR qr(12) XOR dr(3) XOR dr(7);
      qr(1) <= qr(9) XOR qr(13) XOR dr(2) XOR dr(6);
      qr(2) <= qr(10) XOR qr(14) XOR dr(1) XOR dr(5);
      qr(3) <= qr(11) XOR qr(15) XOR dr(0) XOR dr(4);
      qr(4) <= qr(12) XOR dr(3);
      qr(5) <= qr(13) XOR qr(12) XOR qr(8) XOR dr(7) XOR dr(3) XOR dr(2);
      qr(6) <= qr(14) XOR qr(13) XOR qr(9) XOR dr(1) XOR dr(2) XOR dr(6);
      qr(7) <= qr(15) XOR qr(14) XOR qr(10) XOR dr(0) XOR dr(1) XOR dr(5);
      qr(8) <= qr(15) XOR qr(11) XOR qr(0) XOR dr(0) XOR dr(4);
      qr(9) <= qr(12) XOR qr(1) XOR dr(3);
      qr(10) <= qr(13) XOR qr(2) XOR dr(2);
      qr(11) <= qr(14) XOR qr(3) XOR dr(1);
```

Appendix E. Receive Path CRC Checker (continued)

```
      qr(12) <= qr(15) XOR qr(12) XOR qr(8) XOR qr(4)
                XOR dr(0) XOR dr(3) XOR dr(7);
      qr(13) <= qr(13) XOR qr(9) XOR qr(5) XOR dr(2) XOR dr(6);
      qr(14) <= qr(14) XOR qr(10) XOR qr(6) XOR dr(1) XOR dr(5);
      qr(15) <= qr(15) XOR qr(11) XOR qr(7) XOR dr(0) XOR dr(4);
    END IF;
END PROCESS;

-- Need to look for a 1D0F at the receiver
-- output is LOW when 1D0F present
crc_err <= NOT(qr(0)) OR NOT(qr(1)) OR NOT(qr(2)) OR NOT(qr(3))
      OR qr(4) OR qr(5) OR qr(6) OR qr(7)
      OR NOT(qr(8)) OR qr(9) OR NOT(qr(10)) OR NOT(qr(11))
      OR NOT(qr(12)) OR qr(13) OR qr(14) OR qr(15);

END ccitt_rx;
```

Appendix F. Byte Sync Controller

```
-- B_SYNC.VHD - byte synchronization state machine
--
-- This machne has a five state supervisor machine that tracks
-- the number of errors detected within a specific period of time.
-- It also tracks valid characters and SYNC codes.

PACKAGE sync_det IS
  COMPONENT byte_syn PORT (
  clk,                    -- Receiver clock
  reset,                  -- system reset
  error,                  -- bad character
  sync: IN BIT;           -- valid k28.5
  bsync: OUT BIT);        -- byte-sync acquired
  END COMPONENT;
END sync_det;

USE work.cypress.all;
USE work.rtlpkg.all;
USE work.counterpkg.all;

ENTITY byte_syn IS PORT (
  clk,                    -- Receiver clock
  reset,                  -- system reset
  error,                  -- bad character
  sync: IN BIT;           -- valid k28.5
  bsync: OUT BIT);        -- byte-sync acquired
END byte_syn;

ARCHITECTURE arch1 OF byte_syn IS
-- declare internal signals
SIGNAL ctr_en: BIT;             -- counter enable
SIGNAL ctr_reset: BIT;          -- counter reset
SIGNAL bbsync: BIT;             -- interface in sync
SIGNAL cnt: BIT_VECTOR(0 TO 3); -- 4-bit counter vector
-- declare state machine
TYPE sync_state IS (
        state0,                 -- reset or errors, waiting for SYNC codes
        state1,                 -- no errors, in sync
        state2,                 -- 1 error, in sync
        state3,                 -- 2 errors, in sync
        state4);                -- 3 errors, in sync

-- declare state machine encoding, state variable, and initial state
SIGNAL s_state : sync_state := state0;
```

Appendix F. Byte Sync Controller (continued)

```
BEGIN
proc1: PROCESS BEGIN
  WAIT UNTIL (clk='1');
  IF (reset='1') THEN
    s_state <= state0;       -- don't even look yet
  ELSE
    CASE s_state IS
      WHEN state0 =>
        IF ((cnt="1111") AND (error='0')) THEN
          s_state <= state1;
        ELSE
          s_state <= state0;
        END IF;
      WHEN state1 =>
        IF (error='1') THEN
          s_state <= state2;
        ELSE
          s_state <= state1;
        END IF;
      WHEN state2 =>
        IF (error='1') THEN
          s_state <= state3;
        ELSIF (cnt="1111") THEN
          s_state <= state1;
        ELSE
          s_state <= state2;
        END IF;
      WHEN state3 =>
        IF (error='1') THEN
          s_state <= state4;
        ELSIF (cnt="1111") THEN
          s_state <= state2;
        ELSE
          s_state <= state3;
        END IF;
      WHEN state4 =>
        IF (error='1') THEN
          s_state <= state0;
        ELSIF  (cnt="1111") THEN
          s_state <= state3;
        ELSE
          s_state <= state4;
        END IF;
      WHEN others =>
        s_state <= state0;
    END CASE;
  END IF;
END PROCESS proc1;
```

Appendix F. Byte Sync Controller (continued)

```
-- build 4-bit counter with enable and reset
ctr_en <=  '1' WHEN ((s_state=state0 AND reset='0' AND sync='1')
        OR (s_state=state2)
        OR (s_state=state3)
        OR (s_state=state4))
        ELSE '0';

ctr_reset <= '1' WHEN ((reset='1') OR (error='1')) ELSE '0';

-- add standard counter module
ctr1: cntr4 PORT MAP (                    -- contains the 4 bits of ctr1
  one,                              -- set carry in always active
  open,                             -- carry out unused
  ctr_en,                           -- counter enable
  zero,                             -- never load this counter
  zero, zero, zero, zero,           -- load inputs are not used
  clk,                              -- counter clock
  ctr_reset,                        -- will need to expand this signal
  cnt(3), cnt(2),                   --  counter holding register inputs
  cnt(1), cnt(0)
  );

-- assign output
bbsync <= '0' WHEN (s_state=state0) ELSE '1';
d1: DFF PORT MAP (bbsync, clk, bsync);

END arch1;
```

Appendix G. I/O Support

```
-- IOPLUS.VHD

-- Create enhanced I/O buffer that is not part of the io.vhd
-- package for the pASIC 380 family

PACKAGE iopluspkg IS
  COMPONENT HDI2PAD PORT (
    p0 : IN BIT;
    p1 : IN BIT;
    qn : OUT BIT);
  END COMPONENT;
END iopluspkg;

USE work.cypress.all;
USE work.rtlpkg.all;
USE work.iopkg.all;
USE work.resolutionpkg.all;

ENTITY HDI2PAD IS PORT (
  p0 : IN BIT;
  p1 : IN BIT;
  qn : OUT BIT);
END HDI2PAD;

ARCHITECTURE archHDI2PAD OF HDI2PAD IS

SIGNAL o : multi_buffer BIT;

BEGIN

u0: PAINCELL PORT MAP ( ip => p0, ini => o, iz => OPEN);
u1: PAINCELL PORT MAP ( ip => p1, ini => o, iz => OPEN);
qn <= o;

END archHDI2PAD;
```

Replace Your TAXI™ −125 and TAXI−175

This application note will explain how to replace TAXIchip™ devices with the HOTLink™ devices from Cypress Semiconductor. This note begins with an introduction to HOTLink and then gives advantages and replacement suggestions for the TAXI−125 and TAXI−175 devices.

HOTLink Introduction

The HOTLink family of devices transfers data from point to point over high-speed serial links at 160 to 330 Mbits/second (*Figure 1*). The CY7B923 Transmitter (*Figure 2*) takes an 8-bit parallel data stream and encodes it using the Fibre Channel compliant and ESCON™-compliant 8B/10B code. This code maps all 8-bit data characters into a 10-bit transmission code that insures the transmission signal contains suitable transitions for recovery by the receiving device. The transmitter takes this 10-bit data word and converts it to a serial bit-stream and transmits it at 10 times the byte rate over a serial transmission link.

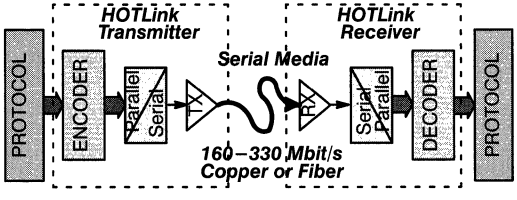

Figure 1. CY7B923 Transmitter Logic Diagram

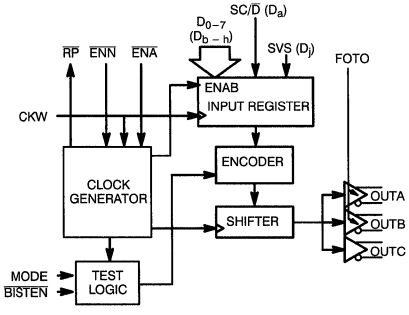

Figure 2. CY7B923 Transmitter Logic Diagram

The CY7B933 HOTLink Receiver (*Figure 3*) lies on the other end of a transmission link that may consist of anything from a few inches of printed circuit-board trace to several kilometers of fiberoptic cable. The receiver decodes the incoming bit stream and reconstructs the original parallel data character, which is presented at the outputs aligned with the recovered clock. The receiver, in addition to these tasks, checks the incoming data stream for errors that may have occurred in the serial transmission.

The SC/$\overline{D}$ (Special Character/$\overline{Data}$) pin provides the ability to transmit command codes in addition to sending data characters. These codes are mapped

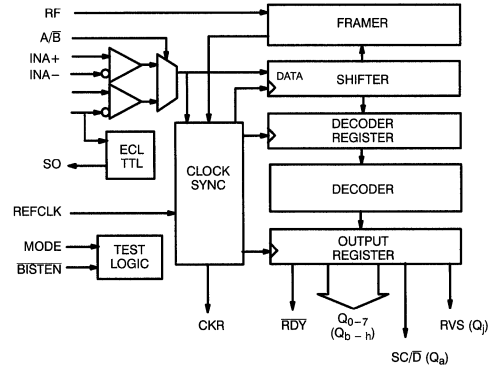

Figure 3. CY7B933 Receiver Logic Diagram

to 10-bit transmission characters defined in the 8B/10B codes of the Fibre Channel standard. This provides the ability to send commands as part of the transmission stream signaling events such as Idle, Start-of-frame, End-of-frame, etc.

Other features include Built-In Self-Test for in-system diagnostic testing, unencoded mode for sending 10-bit data in systems that use a different encoding method, and a seamless parallel interface for connection with both asynchronous and clocked FIFOs. A brief description of the various features of HOTLink is given below with a more detailed discussion found in the CY7B923/CY7B933 HOTLink Transmitter/Receiver datasheet. The PLCC pinouts for these devices are shown in *Figure 4*.

Replacement of TAXI−1 Devices

The following section shows how to upgrade a system using the TAXI−1 (Am7968/Am7969−125 or the Am7968/Am7969−175) with HOTLink. This section begins with a brief explanation of the TAXI−1 devices. It then shows how HOTLink simplifies systems that either use, or plan to use, these devices. It ends with a discussion on how to modify systems that use some of the features of these TAXI devices that are different from HOTLink.

Brief Description of TAXI−1

The Am7968/AM7969 provide a method of connecting systems over a serial link. These devices accept 8-, 9-, or 10-bit parallel data words on the transmitting side of the link (*Figure 5*) and convert the data to a serial bit stream using 4B/5B and 5B/6B NRZI (Non Return to Zero, Invert on 1s) codes. These codes convert 4 input bits into 5 transmission bits in the case of the 4B/5B code, or 5 input bits into 6 transmission bits in the case of the 5B/6B code. These codes insure that enough signal transitions occur on the link for the receiving device to recover the data. On the receiving end of the system (*Figure 6*), the serial data is decoded and presented to the outputs along with the recovered transmitted clock. The pinouts of the Am7968 TAXI Transmitter and Am7969 TAXI Receiver are shown in *Figure 7*.

Simplifying Your System with HOTLink

HOTLink offers an extensive feature list that provides a host of benefits when designing systems that perform point-to-point serial communication.

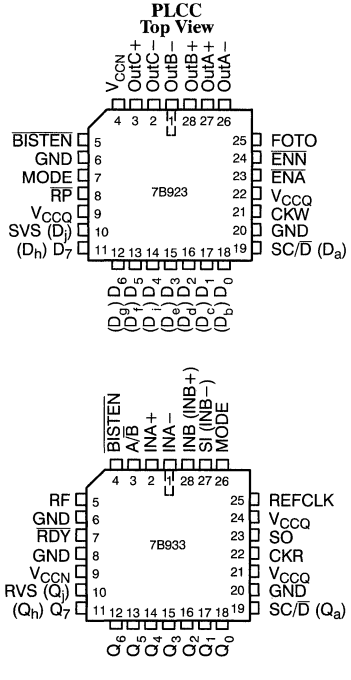

Figure 4. CY7B923 and CY7B933 Pin Configurations

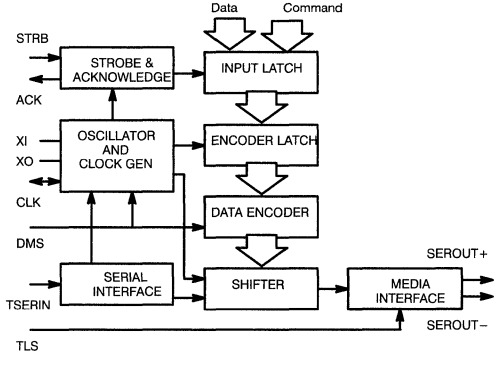

Figure 5. Am7968 Logic Diagram

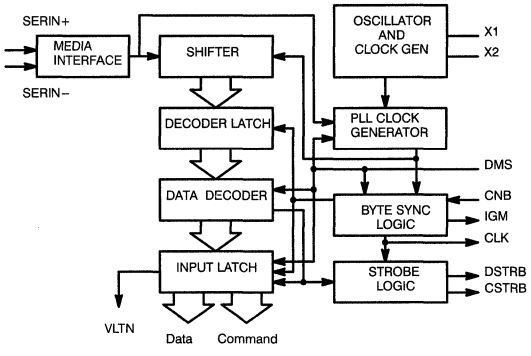

Figure 6. Am7969 Logic Diagram

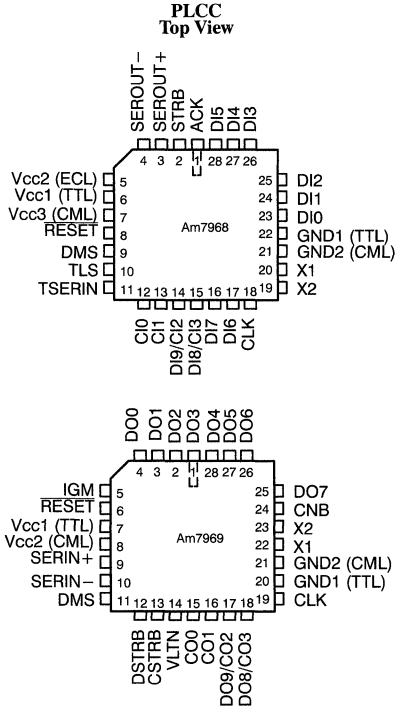

Figure 7. Am7968 and Am7969 Pin Configurations

While many of these features are offered in the TAXI−1 devices, they are difficult to use. These features include multiplexed command and data, multiple inputs and outputs, self-test operation, and many others. Below is a list of HOTLink features and advantage offered to the system designer when compared with the TAXI−1 devices.

Multiplexed Command and Data

One of the major differences between the HOTLink and the TAXI devices is the parallel data interface. The TAXI devices have separate inputs for command and data, while the HOTLink devices have an integrated command and data path. An external controller connected to the command inputs determines what command or data is to be sent. HOTLink determines if a Special Character (Command) should be sent by the status on SC/$\overline{D}$ pin (Special Character/$\overline{Data}$).

The integrated command and data paths of HOTLink allow a simpler, more conventional controller architecture. Instead of creating a separate command path, command codes can be integrated within the data stream and a ninth bit (the SC/$\overline{D}$ bit) can be added to indicate the status of the associated 8 bits of information.

More Serial Outputs

TAXI has one pair of differential ECL outputs. The HOTLink transmitter has three identical differential Pseudo ECL (PECL) serial output ports, any number of which can be disabled to conserve power. Additionally, two of these outputs may be switched off with the use of the FOTO (Fiberoptic Transmitter Off) pin. The AMD™ devices, on the other hand, have only one differential PECL output pair.

The additional HOTLink outputs can be used in a system to provide redundant data paths, for loopback testing, or for building complete networks where a single transmitter is received by multiple receivers.

More Serial Inputs

The TAXI Receiver has a single pair of differential inputs (SERIN±). The HOTLink Receiver has multiple interfaces to the serial transmission medium (INA± and INB±). As in the case of the

HOTLink Transmitter, the additional media inputs of the HOTLink Receiver can be used to provide loop-back testing, redundant transmission paths, or more complex network configurations. The TAXI SERIN− is used to control Test Mode function of the part. In addition to limiting the "in-circuit" test ability of TAXI, this limits the common mode range of the TAXI receiver.

Loop-back testing is easily accomplished with the multiple media interface features of the HOTLink devices. In a typical network-style configuration, both a transmitter and a receiver will exist for each node. By connecting one of the three output pairs of the transmitter to the the second input pair of the receiver as shown in *Figure 8*, the system gains the ability to perform a complete self-check upon system initialization or when an excessive amount of errors are received over the transmission link. HOTLink provides the ability to check the transmitting and receiving devices as well as the associated serial transmission link.

Neither complete system diagnostics nor integrated loop-back testing can be accomplished with the TAXI−1 devices. Many TAXI−1 based systems attempt this feature with single-ended ECL multi-

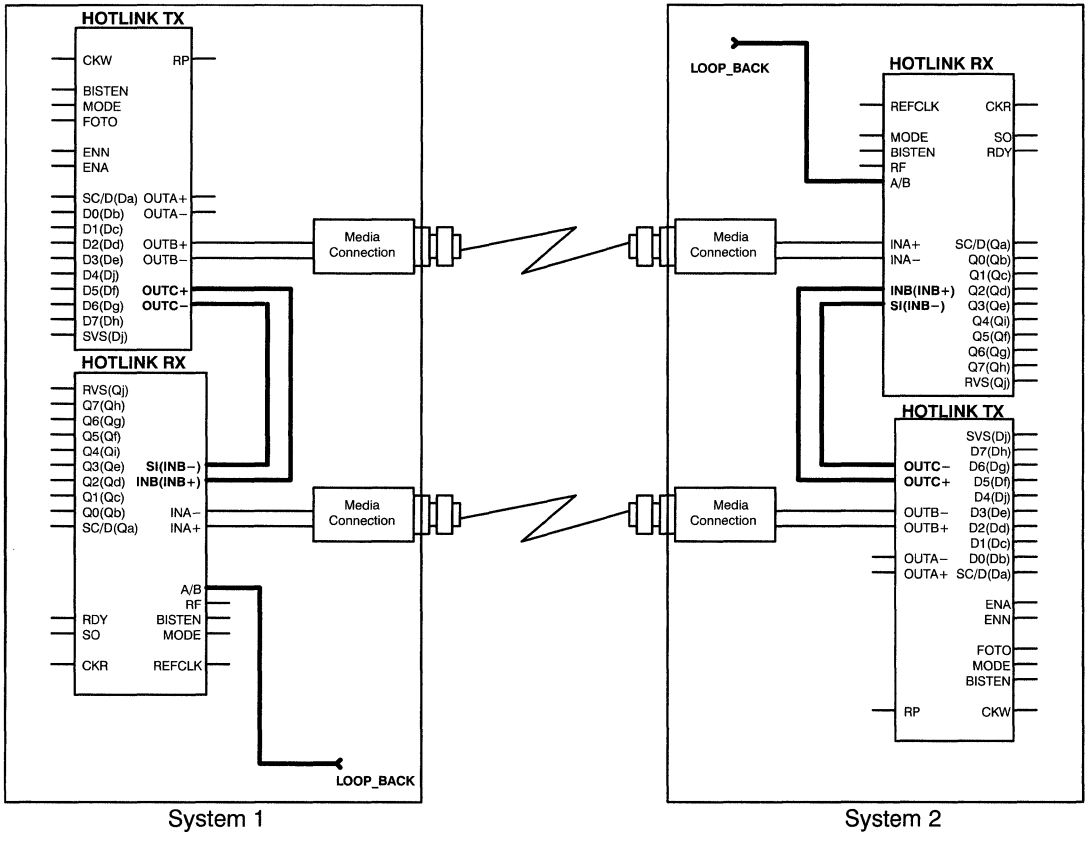

Figure 8. Example HOTLink Loop-Back System Connection

plexers, as shown in *Figure 9*. This solution compromises system reliability and performance.

Superior Data Encoding

Both the HOTLink and TAXI devices map the 8 bits of incoming transmission data into 10-bit transmission characters. The TAXI−1 devices accomplish this task by changing each pair of 4-bit nibbles of data into a pair of 5-bit transmission symbols according to the ANSI X3T9.5 (FDDI) standard. HOTLink, on the other hand, converts each 8 bits of data into a 10-bit transmission symbol according to the ANSI X3T9.3 Fibre Channel and ESCON (Enterprise System CONnection) specifications.

The primary purpose of converting the 8 data bits to 10 transmission bits is to include clock information in the data stream. A code is selected that maps each user character to a transmission character. This mapping insures that the data stream contains enough signal transitions to insure that the receiver PLL stays frequency and phase locked with the incoming data. By including the clock along with the data, the receiver is able to sample the incoming stream of data at the correct rate and position. For example, without this embedded clock information there would be no way of knowing if 1000, 999, or 1001 1s were sent in a row.

While the 4B/5B code used in TAXI−1 merely insures that the transition density of the serial bit stream is maintained, the 8B/10B code used in HOTLink also maintains the DC balance of the signal on the transmission line. This code maintains DC balance by insuring that, on the average, the number of 1s sent is equal to the number of 0s. This improves system performance by reducing the low-frequency "base-line" wander that causes jitter.

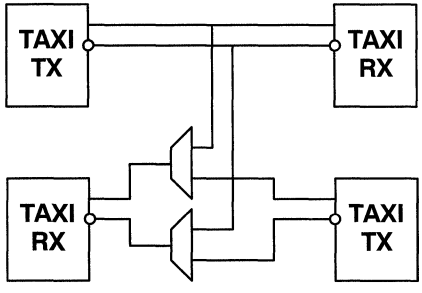

Figure 9. Loop-Back Testing with Multiplexers

More Robust Reframing Capabilities

To reassemble the incoming data stream into parallel data words, the receiver must know which bit location is the beginning of each byte. The transmitter must send SYNC characters to let the receiver know the location of byte boundaries. The TAXI−1 Transmitter sends a SYNC character when neither Data or Command is strobed into the part. At the receiver, this character is decoded as a command and the command strobe is pulsed.

The HOTLink Transmitter also sends a SYNC character when neither data nor command information is latched into the device. And again, at the receiver this character is decoded and the SC/$\overline{D}$ is held HIGH. HOTLink, however, differs in some very important ways from TAXI−1 devices.

TAXI−1 does not have a method for sending a SYNC character as part of the user character stream. HOTLink has a dedicated code that forces a SYNC character to be sent. This is important for controllers that wish to send a SYNC character at the beginning of each packet to insure that previous framing errors do not affect the current packet of data. This simplifies the controller and parallel data interface since the code can be embedded in a stream of other data.

Both TAXI−1 and HOTLink pad the spaces between data packets with SYNC characters. When the "No STRB" condition exists with TAXI−1 or the "No Enable" condition exists with HOTLink, the transmitter fills the unused bandwidth with JK (TAXI−1) or K28.5 (HOTLink). This pad string must be identified at the receiver so that the receiving system is not forced to process this information.

TAXI−1 has no method for ignoring multiple SYNC characters and preventing them from being passed to the receiving system. This is important in systems that have bursty data transmission or transmit data slower than the maximum TAXI−1 data operating frequency. If multiple SYNCs are passed to the outputs of the receiver, the receive FIFO will overflow with useless SYNC characters and this will

require external decoder logic to discard the extraneous information. HOTLink eliminates this problem by only presenting the last SYNC character in a string of SYNC characters (the first SYNC character of a new packet of information) to the outputs of the receiver. This prevents redundant information from being passed to the receive system, yet maintains packet boundaries for easy packet identification.

Occasionally transmission links will experience noise that transforms part of the information stream into a SYNC character (an alias SYNC). This may cause the receiver to incorrectly identify the byte boundary and cause all of the following information to be misframed. This will continue to occur until the transmitter sends an intentional SYNC symbol. The TAXI−1 devices have no method to prevent this unintended reframing. HOTLink can prevent this in two ways.

The first way HOTLink prevents misalignment is provided by its ability to disengage reframing under user control with the RF (reframe) pin. In systems that need reframing only between packets, or only during supervisory functions, the reframe option can be selectively activated or deactivated depending on the system needs.

The second way HOTLink prevents misalignment is provided by its multi-byte framing capability. After the initial start-up phase, approximately 2K bytes after reframe (RF=HIGH) has been activated, the receiver will no longer frame on just one SYNC character, but instead requires at least two SYNC characters separated by exactly 0, 10, 20, or 30 bits of valid data as shown in *Figure 10*.

The multi-byte reframe option is useful in systems that wish to keep the Reframe option activated continuously, but do not want to suffer the data corruption consequences of erroneous misalignment. Systems that stay connected for long communication sessions (e.g., point-to-point data recovery) rarely need to be Reframed since the receiver will rarely lose byte alignment. In these systems, the protocol, or an external timer, can control reframing and only enable framing when it is required. On the HOTLink Receiver this will save 50 mW of power.

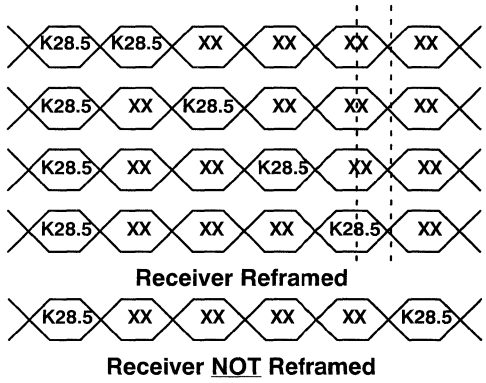

Figure 10. Double-Byte Reframing

For systems that are reconnected often (switched systems) the need to quickly reacquire byte synchronization requires that Reframe be continuously enabled. Multibyte framing available with HOTLink protects these systems from alias SYNC characters.

Higher Operating Frequency

HOTLink provides the biggest improvement in a system upgrade by allowing operation at nearly twice the rate of the TAXI−175 devices and nearly 2.5 times the rate of the TAXI−125s. The range of the TAXI−1 devices is 40 to 175 MBaud whereas HOTLink operates from 160 to 330 MBaud. This increased operating frequency range provides the ability to transfer data at over twice the rate of an equivalent TAXI system.

Built-In Self-Test Capabilities

BIST (Built-In Self-Test) can be used to test the transmitter, receiver, and the serial data link connecting them. During BIST (See *Figure 11*), the transmitter repeats a pattern representing all possible data and command characters, decodes them into transmission symbols and passes them to its outputs. The receiver, while in BIST, waits for the symbol that represents the beginning of the BIST pattern. It then decodes this symbol and every following symbol and compares it with an internally generated pattern that matches those produced by the transmitter's pattern generator. Error signals are indicated with pulses on the RVS (Received

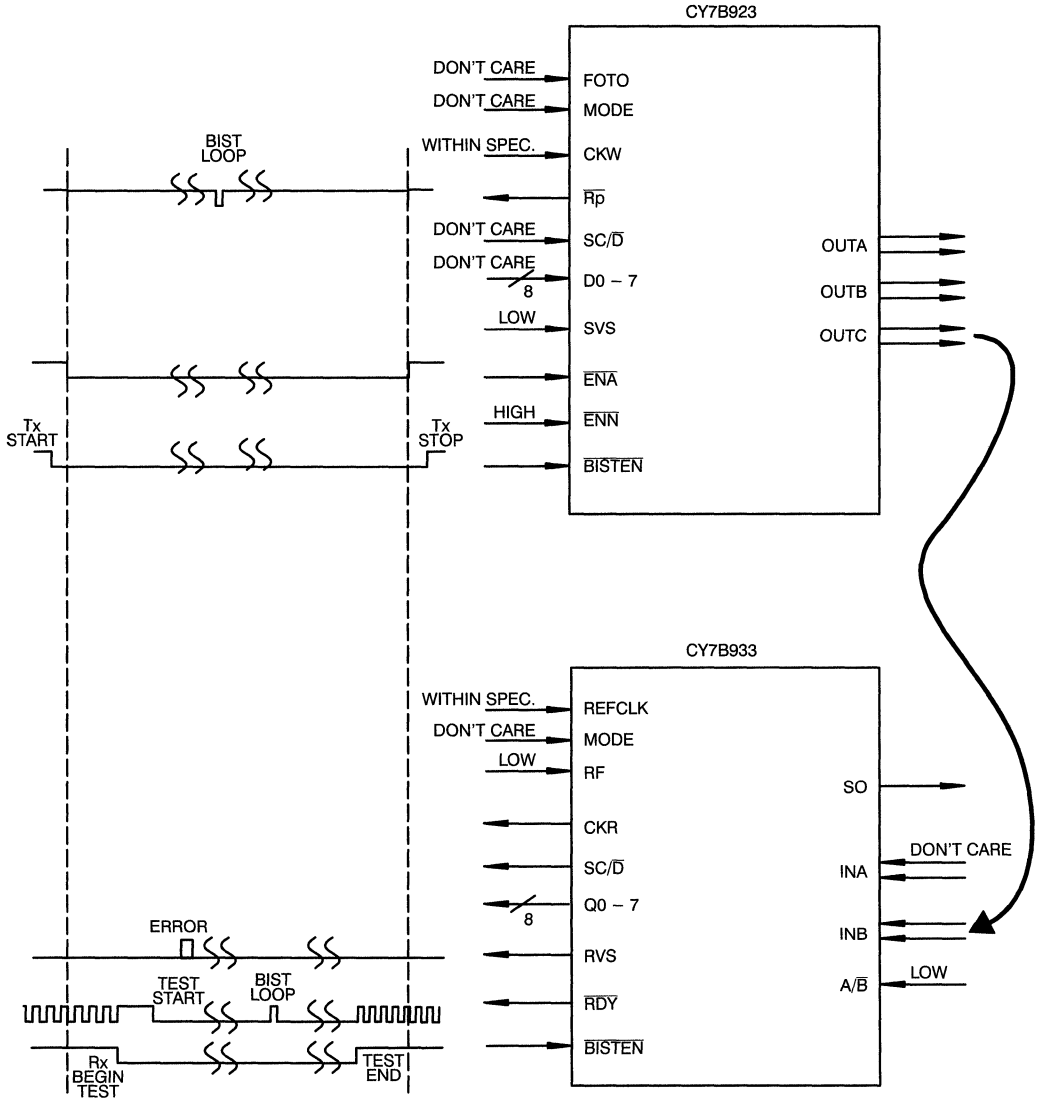

Figure 11. Built-In Self-Test

Violation Symbol) while completed BIST loops are indicated with pulses on the $\overline{RDY}$ line. The BIST function, therefore, checks the entire function of the transmitter (except the transmitter input pins and the bypass function in the Encoder), the serial link, and the receiver.

These functions can not be implemented with the TAXI devices. A substantial amount of additional circuitry would need to be added to a TAXI system to imitate this function. This type of testing is necessary for many types of diagnostics including device functionality and link integrity.

Simplified Synchronous Interface

The TAXI−1 devices have two methods of strobing data into the devices, synchronous and asynchronous. In the asynchronous mode of operation, a strobe line is used in conjunction with an acknowledge line to present data to the device. In this mode of operation the maximum byte-rate frequency for the TAXI−175 devices under the most ideal conditions is no faster than 14 MB/sec. The synchronous strobing feature of the TAXI−1 devices is also cumbersome. This method involves connecting the strobe to the clock line.

HOTLink has a very simple interface that allows seamless connection to both asynchronous and clocked FIFOs. On the transmitter, two enable inputs control when data is to be transmitted. When the $\overline{ENA}$ input is asserted, data on the data lines is serialized and transmitted. When the $\overline{ENN}$ line is asserted, data that is presented on the data lines during the next rising edge of the CLK input is transmitted. This allows efficient, synchronous state machines to control the flow of data over the serial link. In addition, the $\overline{RP}$ (read pulse) output can be connected to the $\overline{R}$ (read) input of asynchronous FIFOs, as shown in *Figure 12*, to provide a seamless asynchronous interface. The $\overline{RP}$ signal has timing that matches the timing required by asynchronous FIFOs. For clocked FIFO designs like that shown in *Figure 13*, the $\overline{ENN}$ input is used to read data from a Clocked FIFO like the Cypress CY7C453 as well as latch data into the transmitter on the next rising edge of CKW.

The receiver has an $\overline{RDY}$ output that pulses LOW each time new data has been received. The $\overline{RDY}$ output has timing that allows the receiver to be seamlessly interfaced with both asynchronous and clocked FIFOs as shown in *Figures 12* and *13*. The TAXI devices require a significant amount of additional circuitry to allow interfacing with FIFOs.

Better DC Specifications

The maximum current specifications of the TAXI−1 Transmitter operating at 17.5 MB/sec is 265 mA. The maximum current specification of the HOTLink Transmitter, on the other hand is 80 mA even when operating at 33 MB/sec.

The TAXI−1 Receiver requires a maximum of 350 mA to operate at 17.5 MB/sec whereas the HOTLink Receiver requires only 150 mA when operating at 33 MB/sec.

The TAXI−1 devices require 300 mV of differential input voltage at the receiver to accurately recover the clock and data from the input serial data stream. The HOTLink Receiver requires only 50 mV of differential input voltage. This translates into lower error rates, increased noise margins, higher jitter tolerance, and longer transmission distances when compared with the TAXI−1 devices.

Loop-Back Testing Capabilities

TAXI−1 has no loop-back testing capabilities. As mentioned previously, the redundant inputs and outputs on the HOTLink devices allow in-system loop-back testing to be performed. An additional output from the transmitter can be connected to an unused input of the receiver. The transmitter/receiver pair of an individual port can be tested together by simply switching the receiver from the link input to the Loop-back input as shown in *Figure 8*.

Ability to Send Violations

The TAXI−1 Transmitter has no method of sending violations. The TAXI Receiver has no unambiguous violation indication. Many, but not all, errors will be indicated as C0 (SYNC) while others will be indicated as other commands. In many systems it is important to explicitly send violations. In normal system operation, a violation can be caused by either a received symbol having no corresponding decode

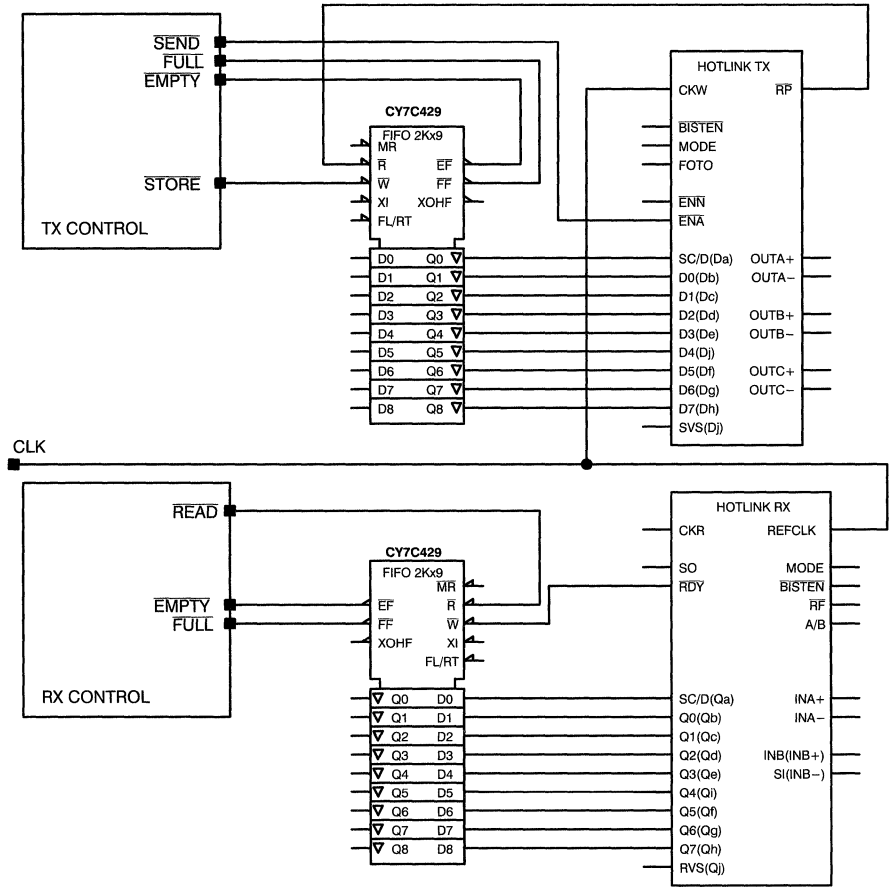

Figure 12. Asynchronous FIFO Interface

value in the receiver, or a valid code received with the wrong running disparity. Sending a violation code on purpose is useful for testing, signaling, and interrupting the receiving system.

The HOTLink Transmitter, on the other hand, provides two mechanisms to allow a system to send a pattern that will translate into a Code Rule Violation at the receiver. Various codes are included in the Special Character (SC) codes to send code rule and Running Disparity (RD) violations as part of the normal data stream. The SVS (Send Violation Symbol) pin allows an external supervisory system to force errors on an otherwise undisturbed data stream. Received errors are unambiguously indicated in the received data stream. All errors also generate an indication on the RVS (Received Violation Symbol) pin to be used by external supervisory logic.

Ability to Turn-Off Serial Output Stream

There is no method of turning off the serial output of the TAXI−1 devices. The FOTO (Fiberoptic Transmitter Off) is an input found on the HOTLink Transmitter that allows the OUTA and OUTB differential outputs to be logically turned off. Laser

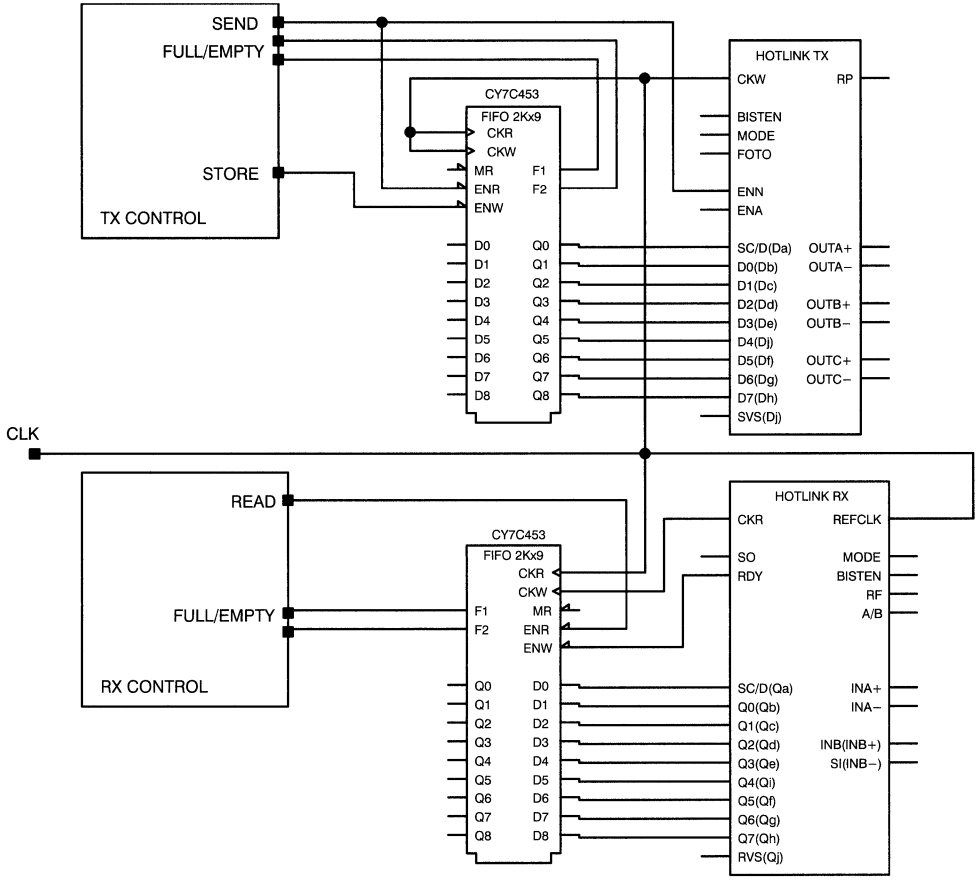

Figure 13. Clocked FIFO Interface

safety systems can use this input to shut off the lasers in the case of a fiber disconnect.

ECL to TTL Translator

The TAXI devices have no ECL to TTL translator. The HOTLink devices have a built-in ECL to TTL translator. The SI input takes the single-ended ECL 100K (+5V referenced) input and the translated TTL signal is presented at the SO output. The system can utilize this translator to convert a carrier-detect signal into its TTL equivalent for use by a controller.

Modifying the System for HOTLink

Listed below are some simple system modifications that can be performed in lieu of modifying the entire system architecture for designers who currently use the TAXI−1 devices and wish to easily upgrade to the HOTLink devices in order to take advantage of its performance and architectural improvements.

Multiplexed Command and Data

Most systems have, at some level, an integrated command and data path, much like that used in HOTLink. These systems explicitly demultiplex these paths to make themselves compatible with the TAXI architecture. These systems can easily take

advantage of the HOTLink architecture by removing the unnecessary multiplexing circuitry and allowing the demultiplexer control line and the data/command lines to drive HOTLink directly.

Some systems, however, send command codes out-of-band with respect to the data stream. These systems can be easily modified by adding a simple multiplexer external to HOTLink or external to the FIFO that drives HOTLink. The MUX select can be driven by the AND of the command lines.

Data Words Longer than 8 Bits

Most data words that need to be encoded are 8 bits in length. In a few cases, however, the data that needs to be encoded is 9, or even 10, bits in length. In these cases, an external multiplexer can be used external to a FIFO that would put each half of the 9- or 10-bit data word into the FIFO separately. At the receiving end, the same operation would be performed in reverse. This is possible due to the extended operating frequency of HOTLink.

Asynchronous Strobing

HOTLink provides a very user-friendly synchronous interface. For asynchronous operation, a FIFO can be used to interface the two asynchronous entities.

Mapping Command Codes

In 8-bit mode, TAXI-1 has 15 different command codes (see *Table 1*), while HOTLink can transmit and receive 12 specific codes (see *Table 2*). Several of these TAXI command codes have restrictions on their usage. HOTLink has no restrictions on the use of any codes. If the system must use more than 12 codes, an easy way to expand the command set is by utilizing a specific code that indicates that the next data word is also a command code. Using this method, or a simple extension of this method, allows nearly an infinite command code set to be transmitted and received.

Operating Frequency

The operating frequency of HOTLink is much faster than the TAXI devices. No design issues need to be considered in systems that wish to operate their parallel side at the same rate and take advantage of the increased system flexibility and functionality that HOTLink offers. When the system has no data to send over the transmission link, HOTLink simply sends strings of SYNC characters automatically. These SYNC characters are ignored on the receiving end. So, whenever the transmitting side of the link does not present data to the transmitter, a SYNC character will be sent. These characters, although used to keep the receiver in lock with the transmission stream, will not be presented as a character to the outputs.

Conclusion

The HOTLink Transmitter and Receiver have many advantages over the AMD Am7968 Transmitter and the Am7969 Receiver (TAXI−1). These advantages include those listed below.

- Multiplexed command and data
- More serial outputs
- More serial inputs
- Superior data encoding
- More robust reframing
- Higher operating frequency
- Built-in self-test
- Simplified synchronous interface
- Reduced power consumption
- Loop-back testing capabilities
- Ability to send violations
- Ability to turn off serial output stream
- ECL-to-TTL translator

Table 1. TAXIchip Command Symbols

Am7968 Transmitter				Am7969 Receiver	
Command Input				Command Output	
HEX	Binary	Encoded Symbol	Mnemonic	HEX	Binary
8-Bit Mode					
0	0000	XXXXX XXXXX	Data	No Change	No Change
No STRB	No STRB	11000 10001	JK (8-bit Sync)	0	0000
1	0001	11111 11111	II	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	IH	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8[1]	1000	00100 00100	HH	8	1000
9	1001	00100 11111	HI	9	1001
A[1]	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D[1]	1101	00000 00100	QH	D	1101
E[1]	1110	00000 11111	QI	E	1110
F[1]	1111	00000 00000	QQ	F	1111

Note

1. While these Commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

Table 2. HOTLink Valid Special Character Codes and Sequences (SC/$\overline{D}$ = HIGH)

HOTLink Special Code Byte Name	Special Code Code Name	Bits HGF	Bits EDCBA	Current RD− abcdei	Current RD− fghj	Current RD+ abcdei	Current RD+ fghj	Receiver Output Code Name
K28.0	C0.0 (C00)	000	00000	001111	0100	110000	1011	C0.0
K28.1	C1.0 (C01)	000	00001	001111	1001	110000	0110	C1.0
K28.2	C2.0 (C02)	000	00010	001111	0101	110000	1010	C2.0
K28.3	C3.0 (C03)	000	00011	001111	0011	110000	1100	C3.0
K28.4	C4.0 (C04)	000	00100	001111	0010	110000	1101	C4.0
K28.5	C5.0 (C05)	000	00101	001111	1010	110000	0101	C5.0
K28.6	C6.0 (C06)	000	00110	001111	0110	110000	1001	C6.0
K28.7	C7.0 (C07)	000	00111	001111	1000	110000	0111	C7.0
K23.7	C8.0 (C08)	000	01000	111010	1000	000101	0111	C8.0
K27.7	C9.0 (C09)	000	01001	110110	1000	001001	0111	C9.0
K29.7	C10.0 (C0A)	000	01010	101110	1000	010001	0111	C10.0
K30.7	C11.0 (C0B)	000	01011	011110	1000	100001	0111	C11.0
Sequences								
Idle	C0.1 (C20)	001	00000	-K28.5+,D21.4,D21.5,D21.5, repeat				C5.0, D21.4, D21.5, D21.5
R_RDY	C1.1 (C21)	001	00001	-K28.5+,D21.4,D10.2,D10.2, repeat				C5.0, D21.4, D10.2, D10.2
EOFxx	C2.1 (C22)	001	00010	-K28.5,Dn.xxx0		+K28.5,Dn.xxx1		C5.0,Dn.xxx0 or C5.0,Dn.xxx1
Follows K28.1 for ESCON Connect-SOF (Rx indication only)								
C-SOF	C7.1 (C27)	001	00111	001111	1000	110000	0111	C7.1
Follows K28.5 for ESCON Passive-SOF (Rx indication only)								
P-SOF	C7.2 (C47)	010	00111	001111	1000	110000	0111	C7.2
Code Rule Violation and SVS Tx Pattern								
Exception	C0.7 (CE0)	111	00000	100111	1000	011000	0111	C0.7
-K28.5	C1.7 (CE1)	111	00001	001111	1010	001111	1010	C5.0 or C1.7
+K28.5	C2.7 (CE2)	111	00010	110000	0101	110000	0101	C5.0 or C2.7
Running Disparity Violation Pattern								
Exception	C4.7 (CE4)	111	00100	110111	0101	001000	1010	C4.7

References

1. Cypress Semiconductor, *CY7B923/CY7B933 HOTLink Transmitter/Receiver Preliminary Datasheet*, Cypress Semiconductor High Performance Data Book, August 1, 1993.
2. Cypress Semiconductor, *HOTLink Design Considerations Application Note*, October 1993.
3. Advanced Micro Devices, TAXIchip Integrated Circuits Transparent Asynchronous Transmitter/Receiver Interface Am7968/Am7969−125 Am7968/Am7969−175 Data Sheet and Technical Manual, 1992
4. Advanced Micro Devices, Am79168/Am79169−275 TAXI−275 Integrated Circuits Technical Manual, Rev. 1.0, 1993.
5. Advanced Micro Devices, Am79168/Am79169−275 TAXI−275 Transmitter/Receiver Transparent Asynchronous Transmitter/Receiver Interface Preliminary Data Sheet, March 1993 Rev B.

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FIFOs 5

FIFOs

CY7C408A
CY7C409A

64 x 8 Cascadable FIFO
64 x 9 Cascadable FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35-MHz shift in and shift out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual-port RAM architecture**
- **Fast (50-ns) bubble-through**
- **Independent asynchronous inputs and outputs**
- **Output enable (CY7C408A)**
- **Expandable in word width and FIFO depth**
- **5V ±10% supply**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge voltage**
- **300-mil, 28-pin DIP**

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry-standard handshaking signals, almost full/almost empty (AFE) and half full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an output enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI_0 – DI_8) under the control of the shift in (SI) input when the input ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO_0 – DO_8 output pins under the control of the shift out (SO) input when the output ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

The IR and OR signals are also used to connect the FIFOs in parallel to make a wider word or in series to make a deeper buffer, or both.

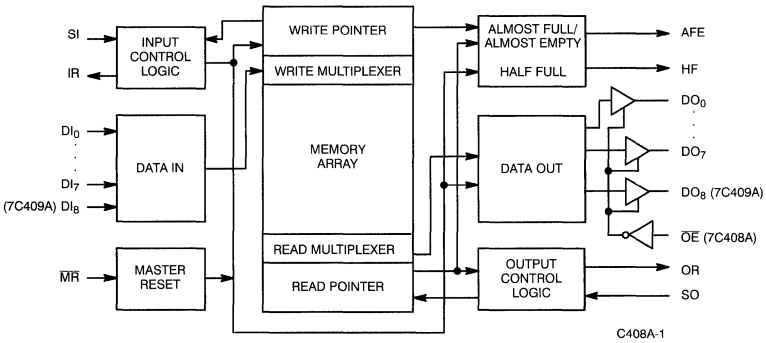
Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together (*Figure 5*). The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO (*Figure 4*). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

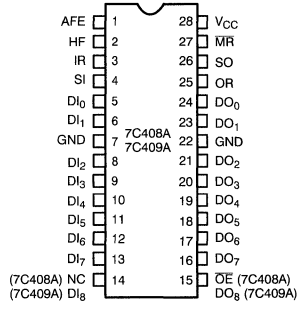
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift in and shift out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual-port RAM architecture, make them ideal for high-speed communications and controllers.

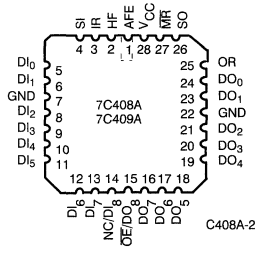
5

Logic Block Diagram



Pin Configurations





Flag Definitions

HF	AFE	Words Stored
L	H	0 – 8
L	L	9 – 31
H	L	32 – 55
H	H	56 – 64

Selection Guide

		7C408A–15 7C409A–15	7C408A–25 7C409A–25	7C408A–35 7C409A–35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)[1]	Commercial	115	125	135
	Military	140	150	N/A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State (7C408A) ..... −0.5V to +7.0V
DC Input Voltage ..... −3.0V to +7.0V
Power Dissipation 1.0W
Output Current, into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	mA
I_{CC}	Power Supply Current	$I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$				

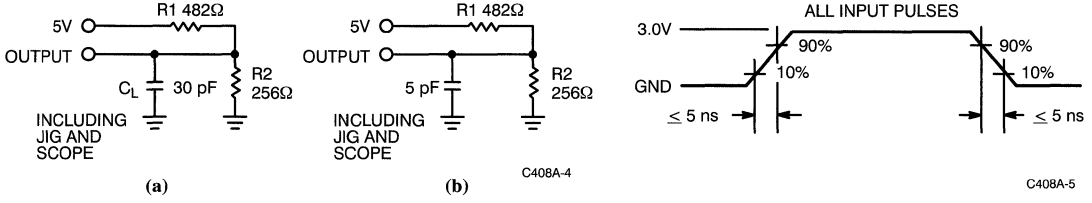
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

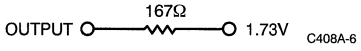
Notes:

1. $I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

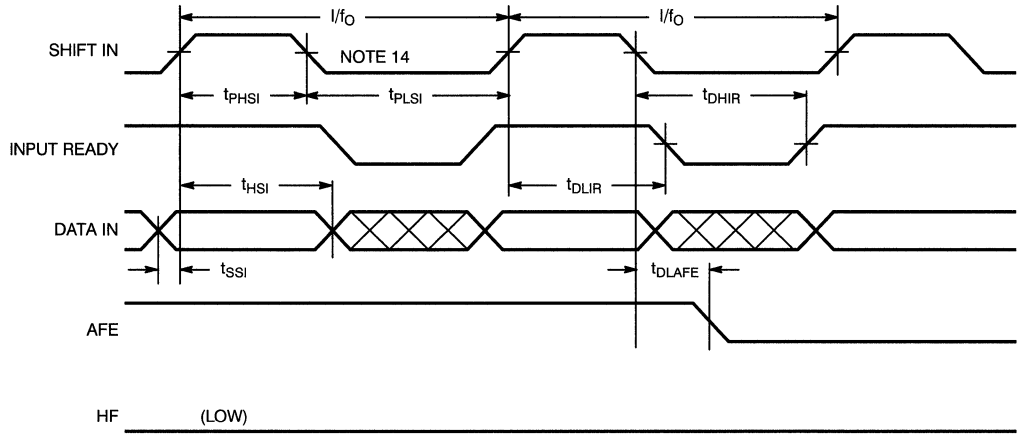
Parameter	Description	Test Conditions	7C408A–15 7C409A–15		7C408A–25 7C409A–25		7C408A–35 7C409A–35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		15		25		35	MHz
t_{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t_{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t_{SSI}	Data Set-Up to SI	Note 8	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t_{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Fall-through, Bubble-back Time		10	65	10	60	10	50	ns
t_{SIR}	Data Set-Up to IR	Note 9	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t_{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t_{DLZOE}	OE LOW to LOW Z (7C408A)	Note 12		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408A)	Note 7		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 13		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns
t_{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

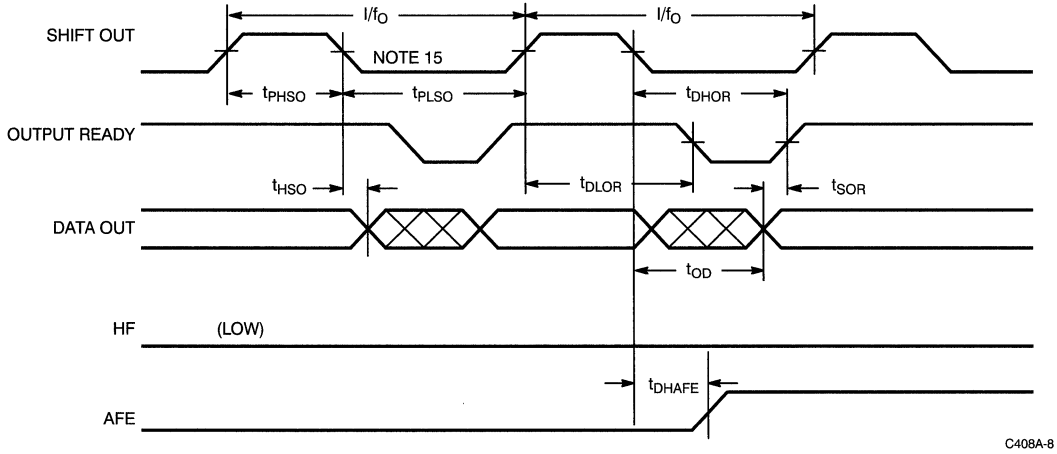
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in parts (a) and (b) of AC Test Loads and Waveforms.
7. $1/f_O \geq (t_{PHSI} + t_{PLSI})$, $1/f_O \geq (t_{PHSO} + t_{PLSO})$.
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
10. At any given operating condition $t_{PIR} \geq (t_{PHSO}$ required).
11. At any given operating condition $t_{POR} \geq (t_{PHSI}$ required).
12. t_{DHZOE} and t_{DLZOE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. t_{DHZOE} transition is measured ±500 mV from steady-state voltage. t_{DLZOE} transition is measured ±100 mV from steady-state voltage. These parameters are guaranteed and not 100% tested.
13. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

Switching Waveforms

Data In Timing Diagram



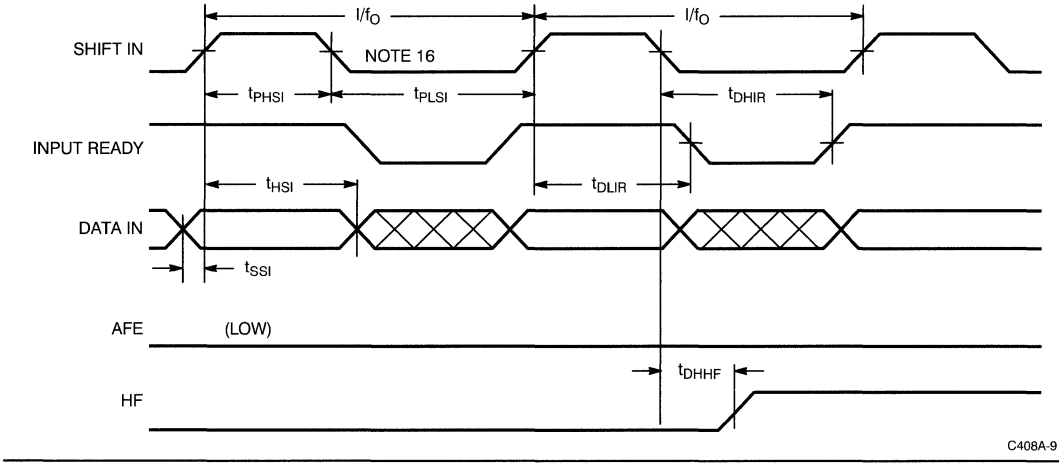
Data Out Timing Diagram



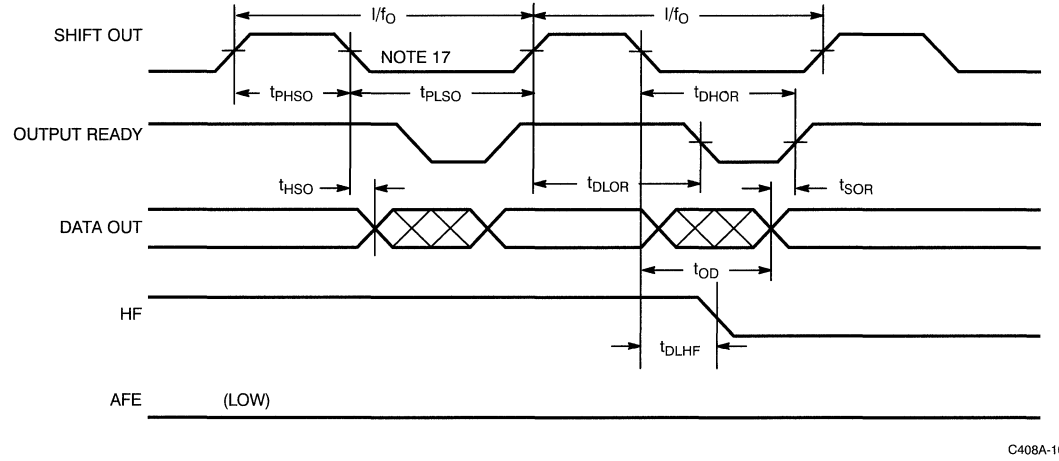
Notes:
14. FIFO contains 8 words.
15. FIFO contains 9 words.

Switching Waveforms (continued)

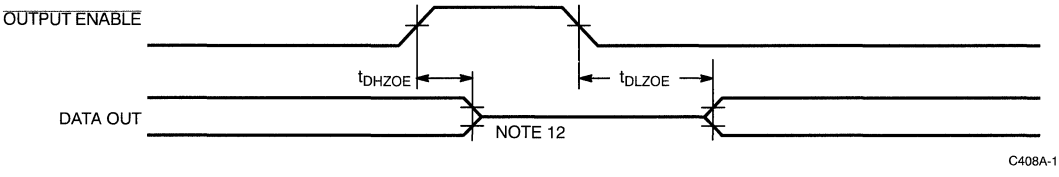
Data In Timing Diagram



Data Out Timing Diagram



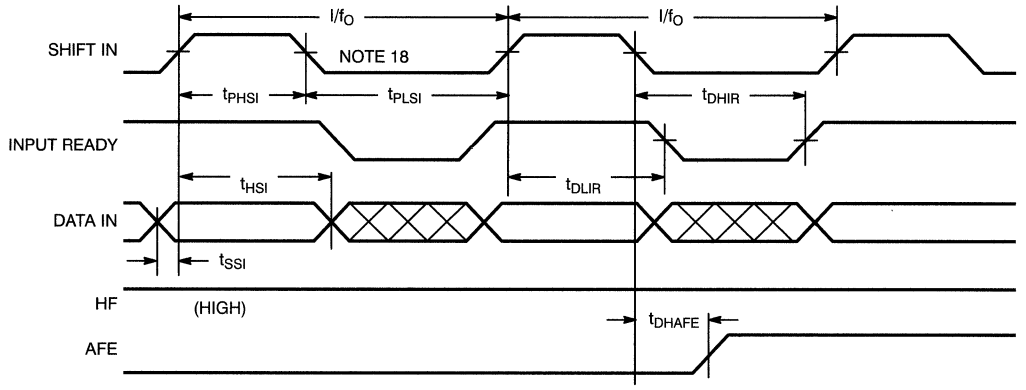
Output Enable (CY7C408A only)



Notes:
16. FIFO contains 31 words.
17. FIFO contains 32 words.

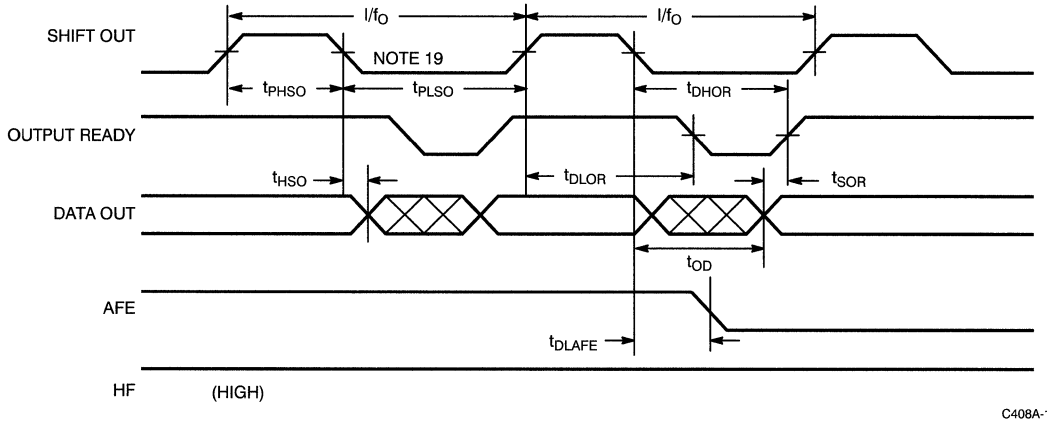
Switching Waveforms (continued)

Data In Timing Diagram



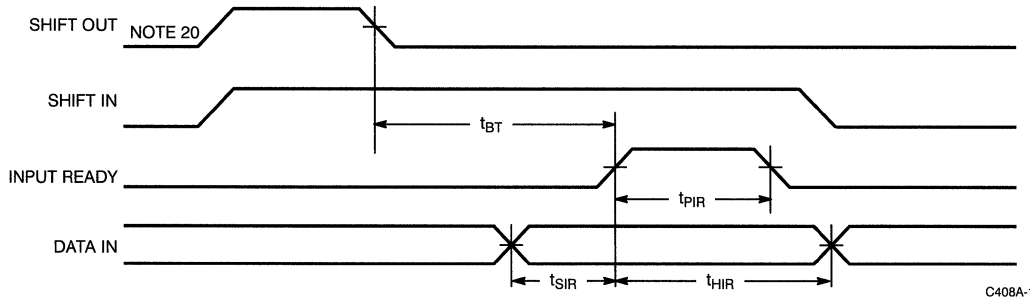
C408A-12

Data Out Timing Diagram



C408A-13

Bubble-Back, Data Out To Data In Diagram

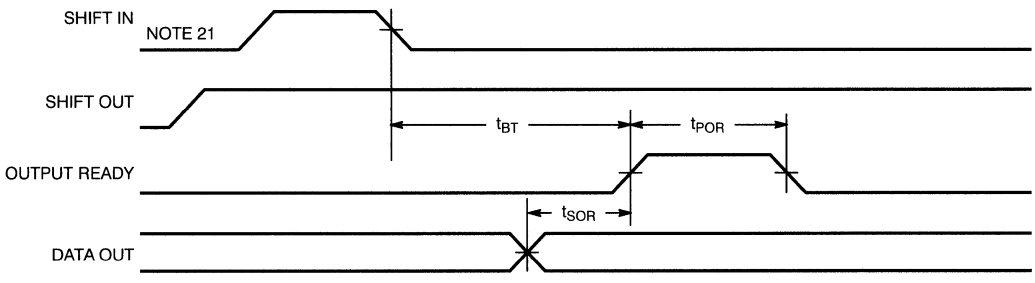


C408A-14

Notes:
18. FIFO contains 55 words.
19. FIFO contains 56 words.
20. FIFO contains 64 words.

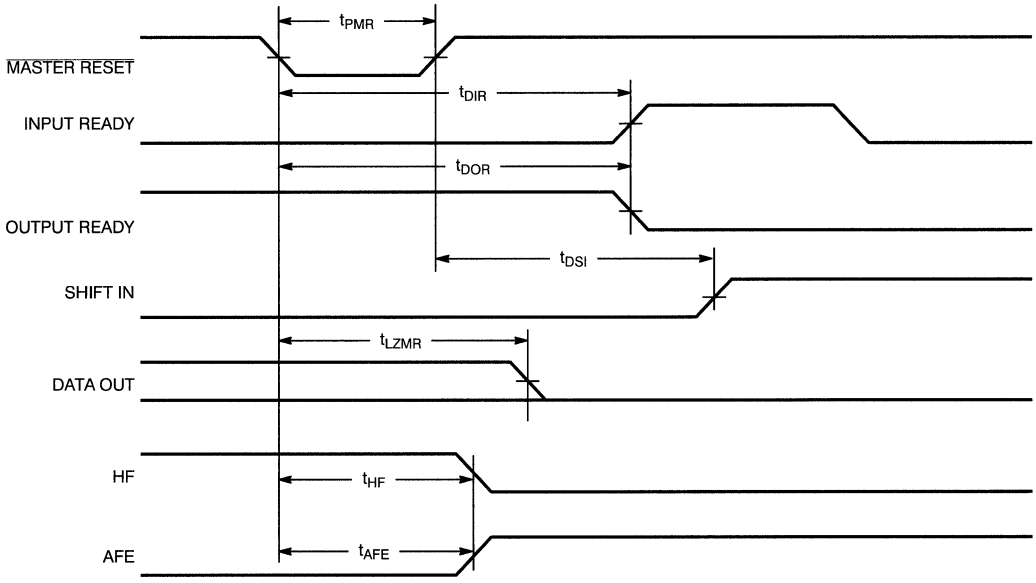
Switching Waveforms (continued)

Fall-Through, Data In to Data Out Diagram



C408A-15

Master Reset Timing Diagram



C408A-16

Note:
21. FIFO is empty.

Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8 or 9 bits each (which are implemented using a dual-port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the almost full/almost empty (AFE) and half full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which it would have to do if the memory were implemented using the conventional register array architecture.

Fall-Through and Bubble-Back

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the fall-through time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the bubble-back time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or near empty) and by the bubble-back time when it is full (or near full).

The conventional definitions of fall-through and bubble-back do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst-case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 – DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the input ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the shift in (SI) pin will clock the data on the DI_0 – DI_8 inputs into the FIFO. Data propagates through the device at the falling edge of SI.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.

Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the output ready (OR) signal. After the FIFO is reset all data outputs (DO_0 – DO_8) will be in the LOW state. As long as the FIFO remains empty, the OR signal will be LOW and all SO pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

AFE and HF Flags

Two flags, almost full/almost empty (AFE) and half full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are 8 or fewer or 56 or more words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (*Figures 1* and *2*).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay (t_{DHAFE}, t_{DLAFE}, t_{DHHF} or t_{DLHF}). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

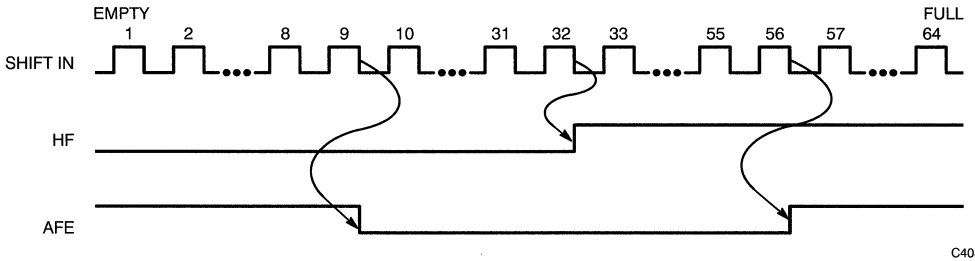


Figure 1. Shifting Words In

Cascading the 7C408/9A–35 Above 25 MHz

First, the capacity of N cascaded FIFOs is decreased from N × 64 to (N × 63) + 1.

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin (*Figure 3*). Two things should be noted when this configuration is implemented.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data shifted in faster than it is shifted out, and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.[28]

When data packets[29] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 (=2 × 63 + 1) words may be shifted in at up to 35 MHz and then the entire packet may be shifted out at up to 35 MHz.

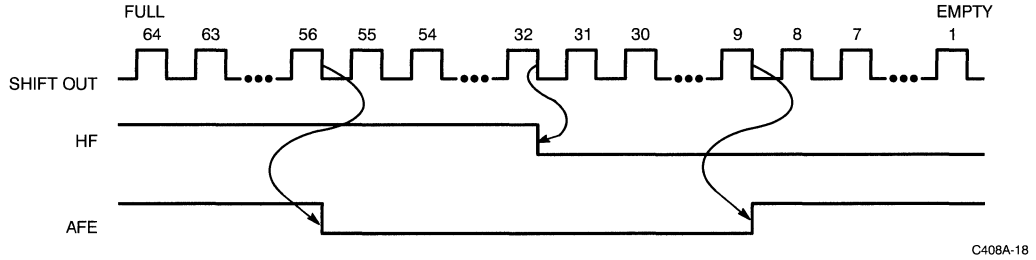


Figure 2. Shifting Words Out

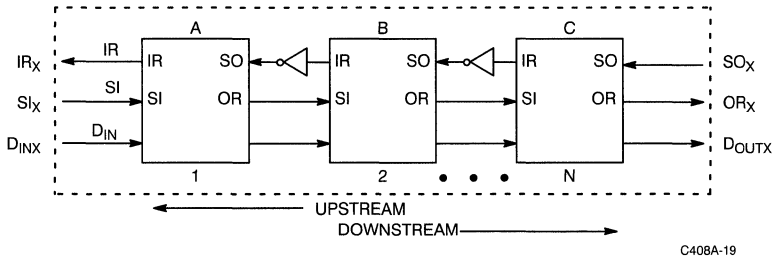


Figure 3. Cascaded Configuration Above 25 MHz

128 x 9 Configuration

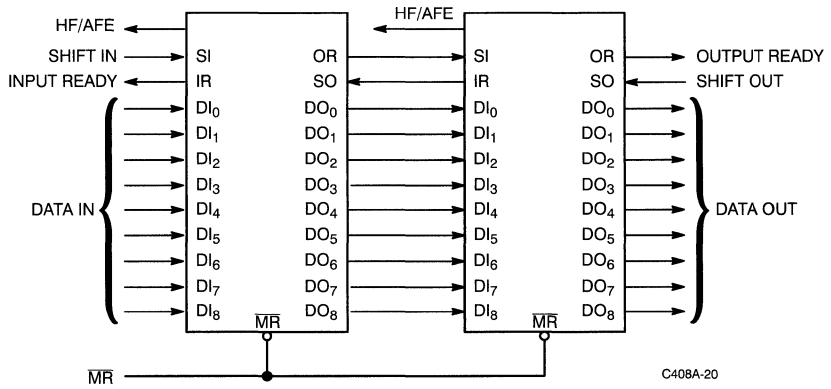


Figure 4. Cascaded Configuration at or below 25 MHz[22, 23, 24, 25, 26]

192 x 27 Configuration

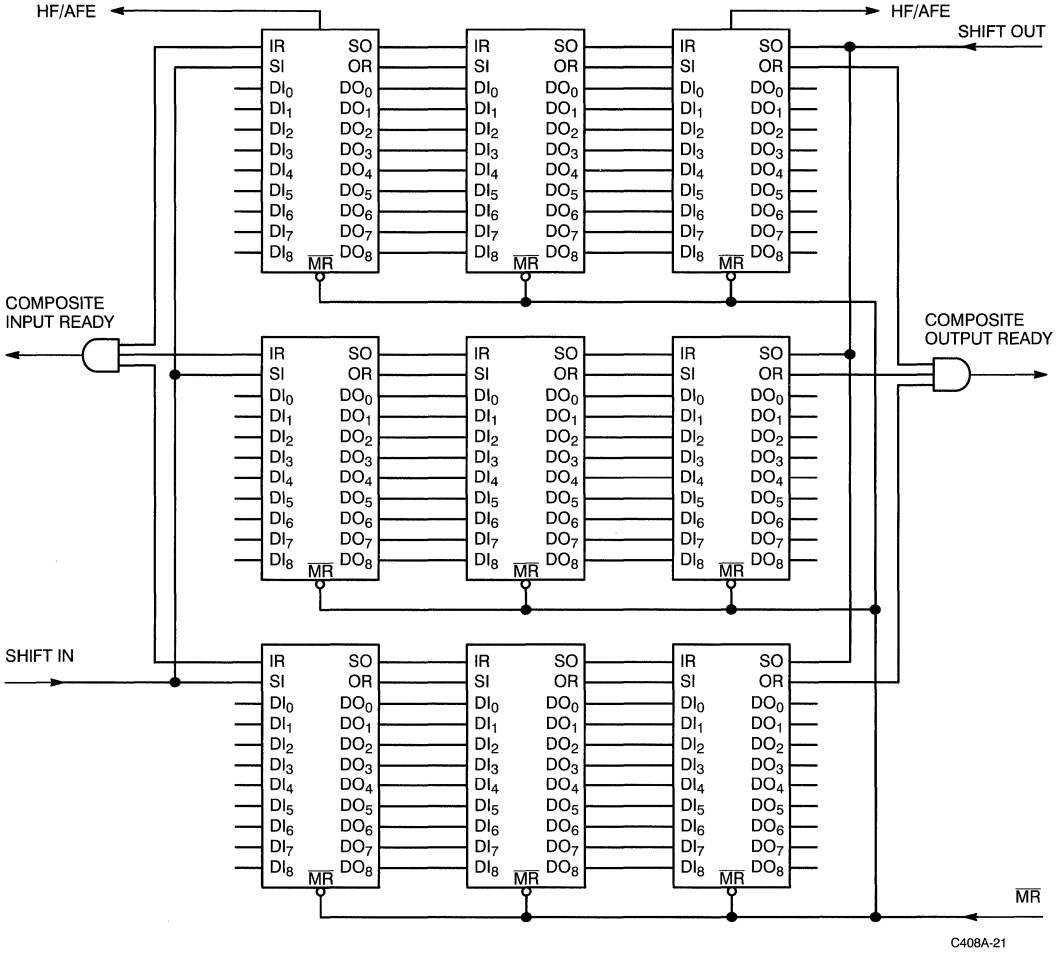


Figure 5. Depth and Width Expansion[23, 24, 25, 26, 27]

Notes:

22. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
23. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
24. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
25. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
26. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH, and OR goes LOW.
27. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite input ready and output ready flags. This need is due to the variation of delays of the FIFOs.

If data is to be shifted out simultaneously with the data being shifted in, the concept of "virtual capacity" is introduced. Virtual capacity is simply how large a packet of data can be shifted in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted out at any given frequency. *Figure 6* is a graph of packet size[30] vs. shift out frequency (f_{SOx}) for two different values of shift in frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high shift out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep.[31] If data is shifted in simultaneously, *Figure 6* applies with f_{SIx} and f_{SOx} interchanged.

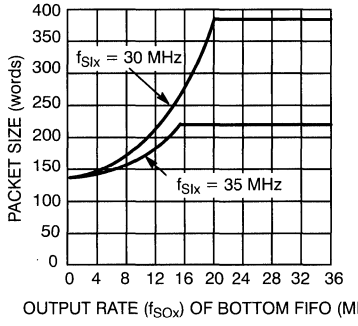


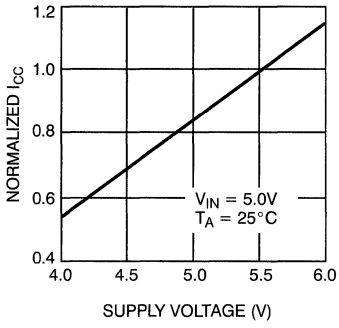
Figure 6. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter

Notes:

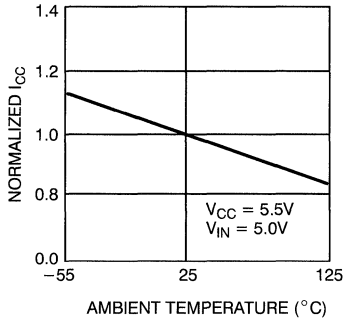
28. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
29. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is shifted in without simultaneous shift out clock occurring. The complement of this holds when data is shifted out as a packet.
30. These are typical packet sizes using an inverter whose delay is 4 ns.
31. Only devices with the same speed grade are specified to cascade together.

Typical DC and AC Characteristics

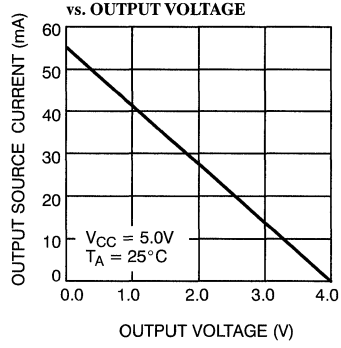
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



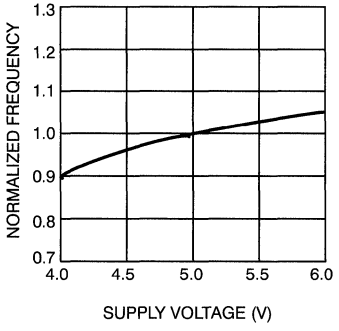
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



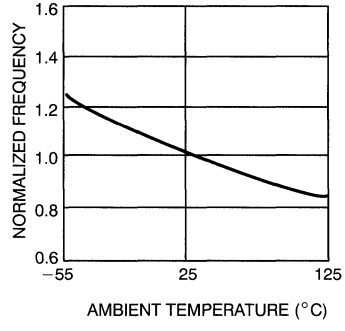
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



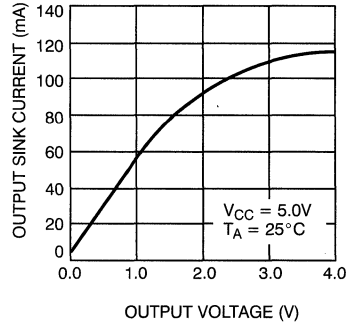
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



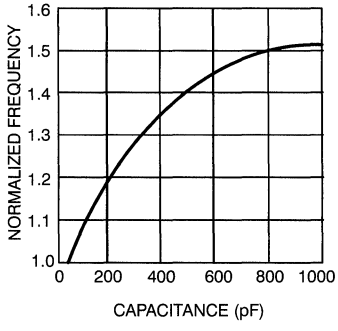
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



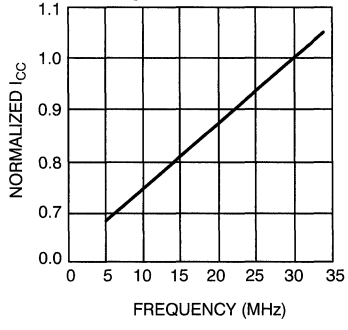
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



C408A-23

Ordering Information

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C408A–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C408A–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C408A–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C409A–15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C409A–25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A–25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C409A–35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A–35VC	V21	28-Lead (300-Mil) Molded SOJ	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CCQ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{SIIR}	7, 8, 9, 10, 11
t_{SOOR}	7, 8, 9, 10, 11
t_{DLZOE}	7, 8, 9, 10, 11
t_{DHZOE}	7, 8, 9, 10, 11
t_{DHHF}	7, 8, 9, 10, 11
t_{DLHF}	7, 8, 9, 10, 11
t_{DLAFE}	7, 8, 9, 10, 11
t_{DHAFE}	7, 8, 9, 10, 11
t_B	7, 8, 9, 10, 11
t_{OD}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{AFE}	7, 8, 9, 10, 11
t_{HF}	7, 8, 9, 10, 11

Document #: 38-00059-G

256 x 9, 512 x 9, 1K x 9, 2K x 9, 4K x 9 Cascadable FIFO

Features

- **256 x 9, 512 x 9, 1,024 x 9, 2048 x 9, and 4096 x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 50.0-MHz read/write independent of depth/width**
- **Low operating power**
  — I_{CC1} = 35 mA
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil DIP packaging**
- **7x7 TQFP**
- **300-mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7200, IDT7201, IDT7202, IDT7203, and IDT7204**

Functional Description

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, and CY7C432/3 are first-in first-out (FIFO) memories offered in 600-mil wide and 300-mil wide packages. They are, respectively, 256, 512, 1,024, 2,048, and 4,096 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

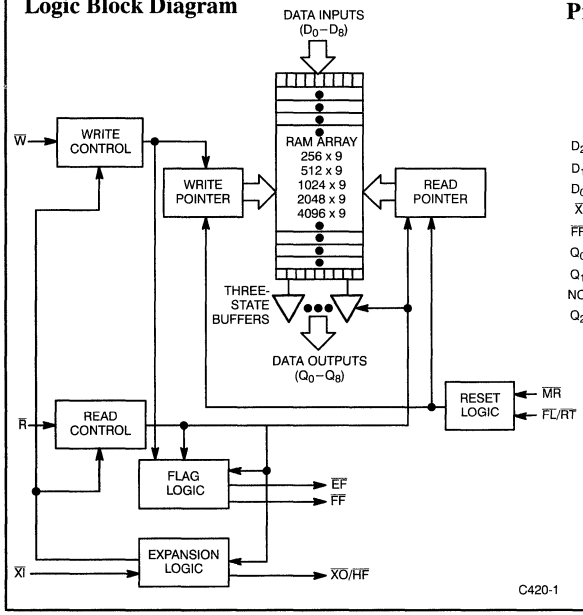
The read and write operations may be asynchronous; each can occur at a rate of 50.0 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

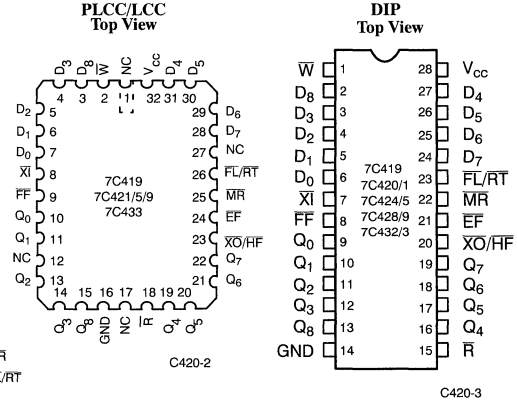
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

The CY7C419, CY7C420, CY7C421, CY7C424, CY7C425, CY7C428, CY7C429, CY7C432, and CY7C433 are fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout and guard rings.

Logic Block Diagram



Pin Configurations

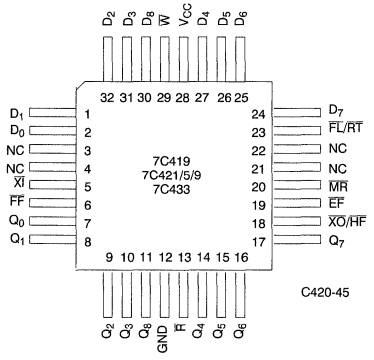


Selection Guide

256 x 9	**7C419–10**	**7C419–15**	**7C419–20**	**7C419–25**	**7C419–30**	**7C419–40**	**7C419–65**
512 x 9 (600-mil only)			**7C420–20**	**7C420–25**	**7C420–30**	**7C420–40**	**7C420–65**
512 x 9	**7C421–10**	**7C421–15**	**7C421–20**	**7C421–25**	**7C421–30**	**7C421–40**	**7C421–65**
1K x 9 (600-mil only)			**7C424–20**	**7C424–25**	**7C424–30**	**7C424–40**	**7C424–65**
1K x 9	**7C425–10**	**7C425–15**	**7C425–20**	**7C425–25**	**7C425–30**	**7C425–40**	**7C425–65**
2K x 9 (600-mil only)			**7C428–20**	**7C428–25**	**7C428–30**	**7C428–40**	**7C428–65**
2K x 9	**7C429–10**	**7C429–15**	**7C429–20**	**7C429–25**	**7C429–30**	**7C429–40**	**7C429–65**
4K x 9 (600-mil only)				**7C432–25**	**7C432–30**	**7C432–40**	**7C432–65**
4K x 9	**7C433–10**	**7C433–15**	**7C433–20**	**7C433–25**	**7C433–30**	**7C433–40**	**7C433–65**
Frequency (MHz)	50	40	33.3	28.5	25	20	12.5
Maximum Access Time (ns)	10	15	20	25	30	40	65
I_{CC1} (mA)	35	35	35	35	35	35	35

Pin Configurations (continued)

TQFP
Top View



Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C419–10, 15, 20, 25, 30, 40, 65 7C420/1–10, 15, 20, 25, 30, 40, 65 7C424/5–10, 15, 20, 25, 30, 40, 65 7C428/9–10, 15, 20, 25, 30, 40, 65 7C432/3–10, 15, 20, 25, 30, 40, 65 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	
V_{IL}	Input LOW Voltage			Note 3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−90	mA

Electrical Characteristics Over the Operating Range[2] (continued)

Parameter	Description	Test Conditions		7C419–10 7C421–10 7C425–10 7C429–10 7C433–10		7C419–15 7C421–15 7C425–15 7C429–15 7C433–15		7C419–20 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20		7C419–25 7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25 7C432–25 7C433–25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Com'l		85		65		55		50	mA
			Mil/Ind				100		90		80	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		10		10		10		10	mA
			Mil/Ind				15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		5		5		5		5	mA
			Mil/Ind				8		8		8	

Electrical Characteristics Over the Operating Range[2] (continued)

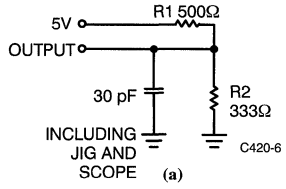
Parameter	Description	Test Conditions		7C419–30 7C420–30 7C421–30 7C424–30 7C425–30 7C428–30 7C429–30 7C432–30 7C433–30		7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C428–40 7C429–40 7C432–40 7C433–40		7C419–65 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C432–65 7C433–65		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA f = f_{MAX}	Com'l		40		35		35	mA
			Mil/Ind		75		70		65	
I_{CC1}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA F = 20 MHz	Com'l		35		35		35	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		10		10		10	mA
			Mil		15		15		15	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		5		5		5	mA
			Mil		8		8		8	

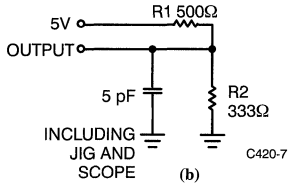
Capacitance[5]

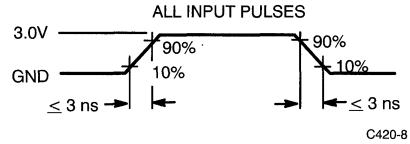
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	6	pF
C_{OUT}	Output Capacitance		6	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (Min.) = −2.0V for pulse durations of less than 20 ns.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

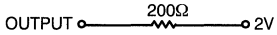
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[6, 7]

Parameter	Description	7C419–10 7C421–10 7C425–10 7C429–10 7C433–10		7C419–15 7C421–15 7C425–15 7C429–15 7C433–15		7C419–20 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20		7C419–25 7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25 7C432–25 7C433–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	20		25		30		35		ns
t_A	Access Time		10		15		20		25	ns
t_{RR}	Read Recovery Time	10		10		10		10		ns
t_{PR}	Read Pulse Width	10		15		20		25		ns
t_{LZR}[5,8]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8,9]	Data Valid After Read HIGH	5		5		5		5		ns
t_{HZR}[5,8,9]	Read HIGH to High Z		15		15		15		18	ns
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{PW}	Write Pulse Width	10		15		20		25		ns
t_{HWZ}[5,8]	Write HIGH to Low Z	5		5		5		5		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-Up Time	6		8		12		15		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	20		25		30		35		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		20		25		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		20		25		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		20		25		ns
t_{RTC}	Retransmit Cycle Time	20		25		30		35		ns
t_{PRT}	Retransmit Pulse Width	10		15		20		25		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
7. See the last page of this specification for Group A subgroup testing information.
8. t_{HZR} transition is measured at +200 mV from V_{OL} and −200 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
9. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load and Waveforms.

Switching Characteristics Over the Operating Range[6, 7] (continued)

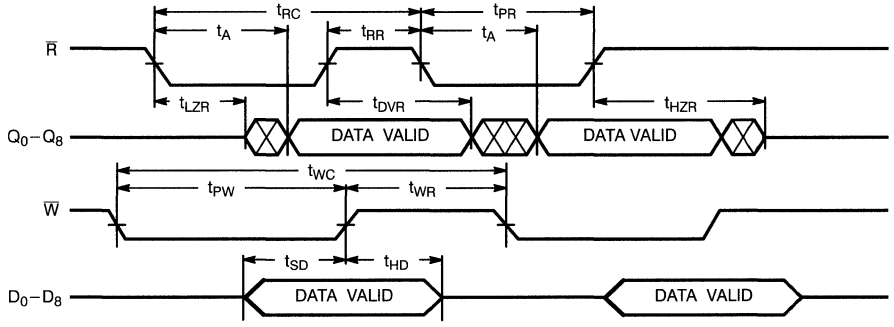
Parameter	Description	7C419–10 7C421–10 7C425–10 7C429–10 7C433–10		7C419–15 7C421–15 7C425–15 7C429–15 7C433–15		7C419–20 7C420–20 7C421–20 7C424–20 7C425–20 7C428–20 7C429–20 7C433–20		7C419–25 7C420–25 7C421–25 7C424–25 7C425–25 7C428–25 7C429–25 7C432–25 7C433–25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		20		25		30		35	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		20		25		30		35	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		20		25		30		35	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15		20		25	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15		20		25	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15		20		25	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15		20		25	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15		20		25	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15		20		25	ns
t_{RAE}	Effective Read from Write HIGH		10		15		20		25	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	10		15		20		25		ns
t_{WAF}	Effective Write from Read HIGH		10		15		20		25	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	10		15		20		25		ns
t_{XOL}	Expansion Out LOW Delay from Clock		10		15		20		25	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		10		15		20		25	ns

Switching Characteristics Over the Operating Range[6, 7] (continued)

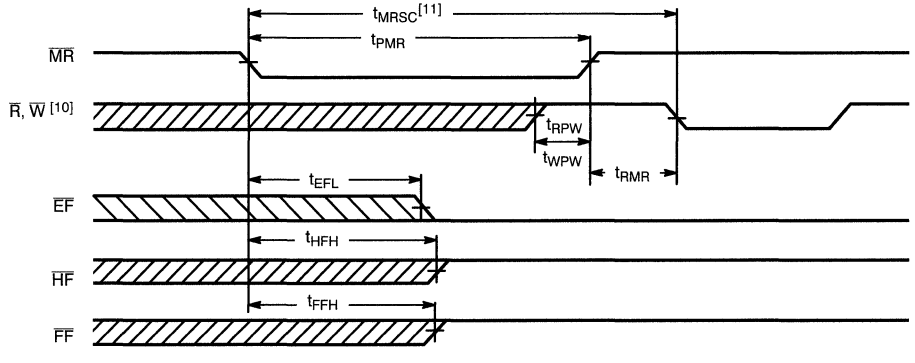
Parameter	Description	7C419–30 7C420–30 7C421–30 7C424–30 7C425–30 7C428–30 7C429–30 7C432–30 7C433–30		7C419–40 7C420–40 7C421–40 7C424–40 7C425–40 7C428–40 7C429–40 7C432–40 7C433–40		7C419–65 7C420–65 7C421–65 7C424–65 7C425–65 7C428–65 7C429–65 7C432–65 7C433–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_A	Access Time		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}[5,8]	Read LOW to Low Z	3		3		3		ns
t_{DVR}[8,9]	Data Valid After Read HIGH	5		5		5		ns
t_{HZR}[5,8,9]	Read HIGH to High Z		20		20		20	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{HWZ}[5,8]	Write HIGH to Low Z	5		5		5		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	30		40		65		ns
t_{RTC}	Retransmit Cycle Time	40		50		80		ns
t_{PRT}	Retransmit Pulse Width	30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		30		35		60	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		30		35		60	ns
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		30		35		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		40		65	ns

Switching Waveforms

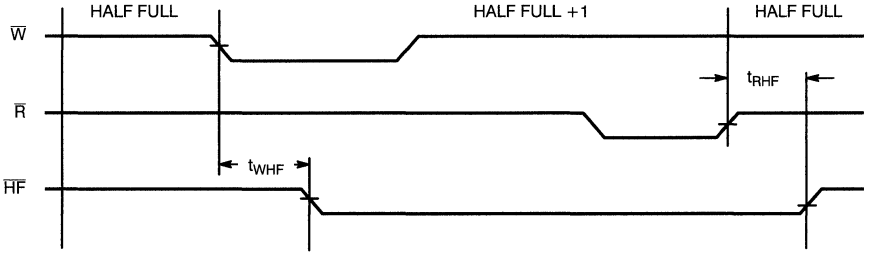
Asynchronous Read and Write



Master Reset



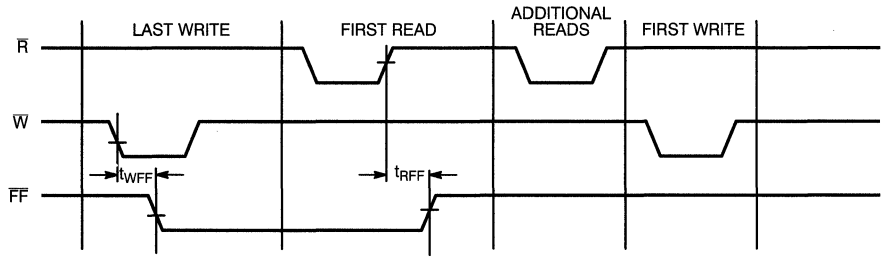
Half-Full Flag



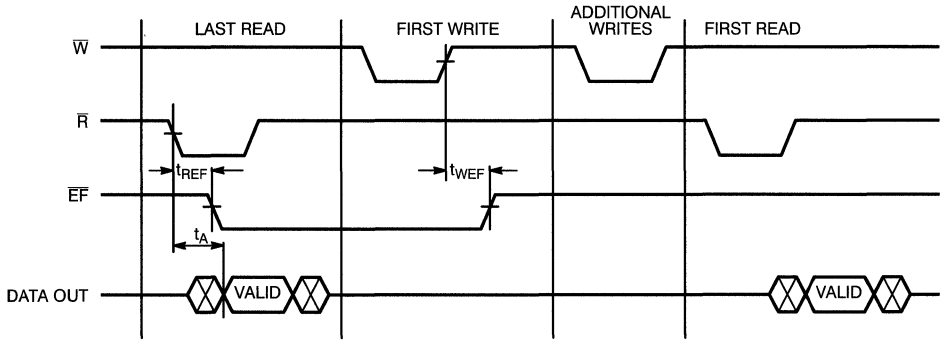
Notes:
10. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)

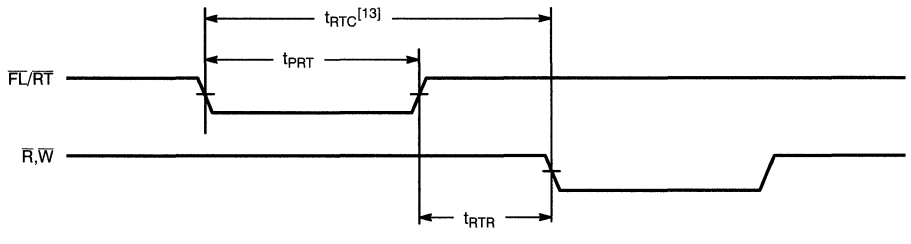
Last Write to First Read Full Flag



Last Read to First Write Empty Flag



Retransmit[12]

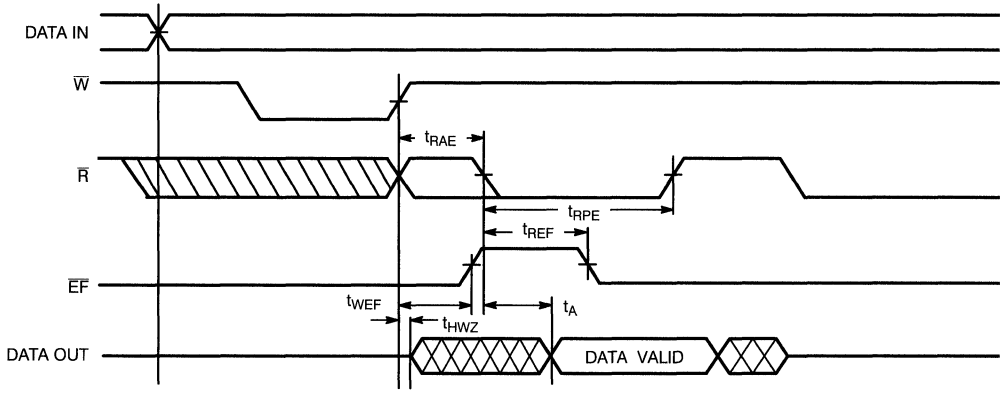


Notes:

12. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
13. $t_{RTC} = t_{PRT} + t_{RTR}$.

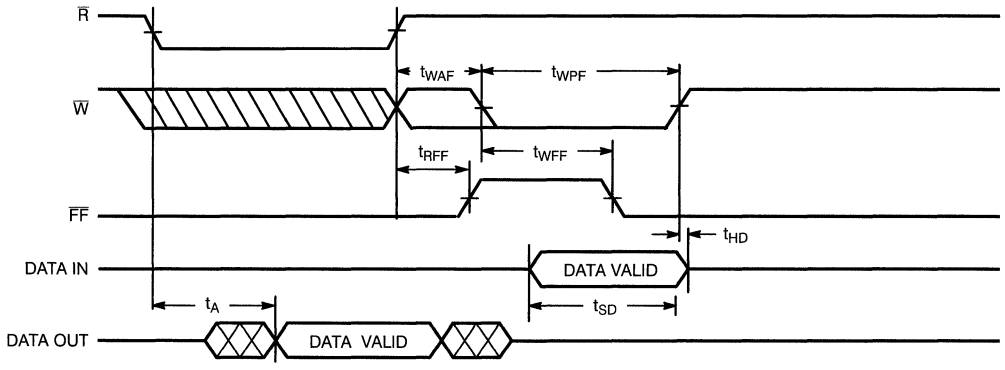
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



C420-15

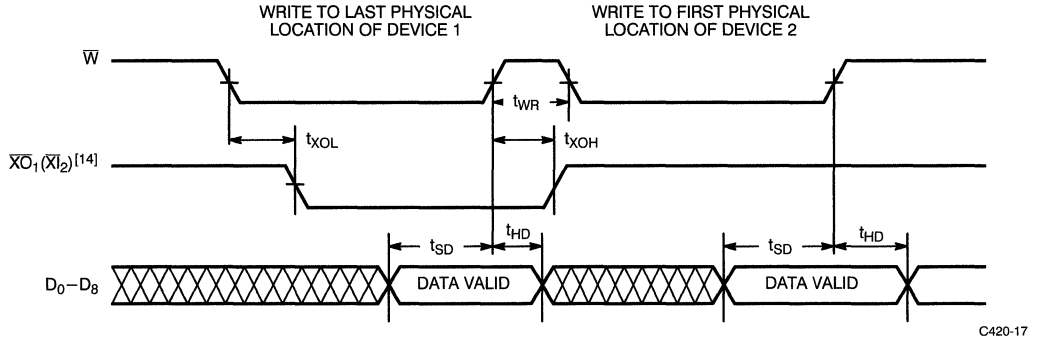
Full Flag and Write Data Flow-Through Mode

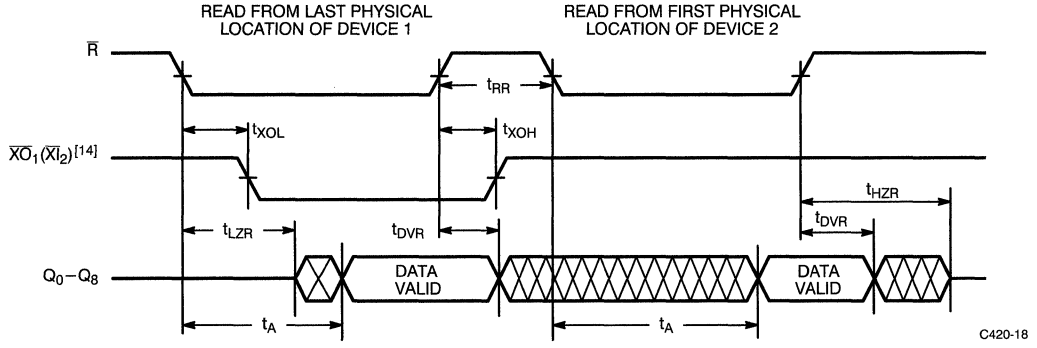


C420-16

Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
14. Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

Architecture

The CY7C419, CY7C420/1, CY7C424/5, CY7C428/9, CY7C432/3 FIFOs consist of an array of 256, 512, 1024, 2048, 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0-Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. The rising edge of $\overline{R}$ causes the data outputs to go to the high-impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data as well as not previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

Up to the full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

Use of the Empty and Full Flags

In order to achieve the maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read of write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement; some competitors' FIFOs do not.

The reason why the flags are required to be valid by the next cycle is fairly complex. It has to do with the "effective pulse width violation" phenomenon, which can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that it cannot be determined what the effective pulse width of the read signal is, because the state machine does not look at the read signal until it goes to the empty+1 state. In a similar manner, the minimum write pulse width may be violated by attempting to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but in order to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

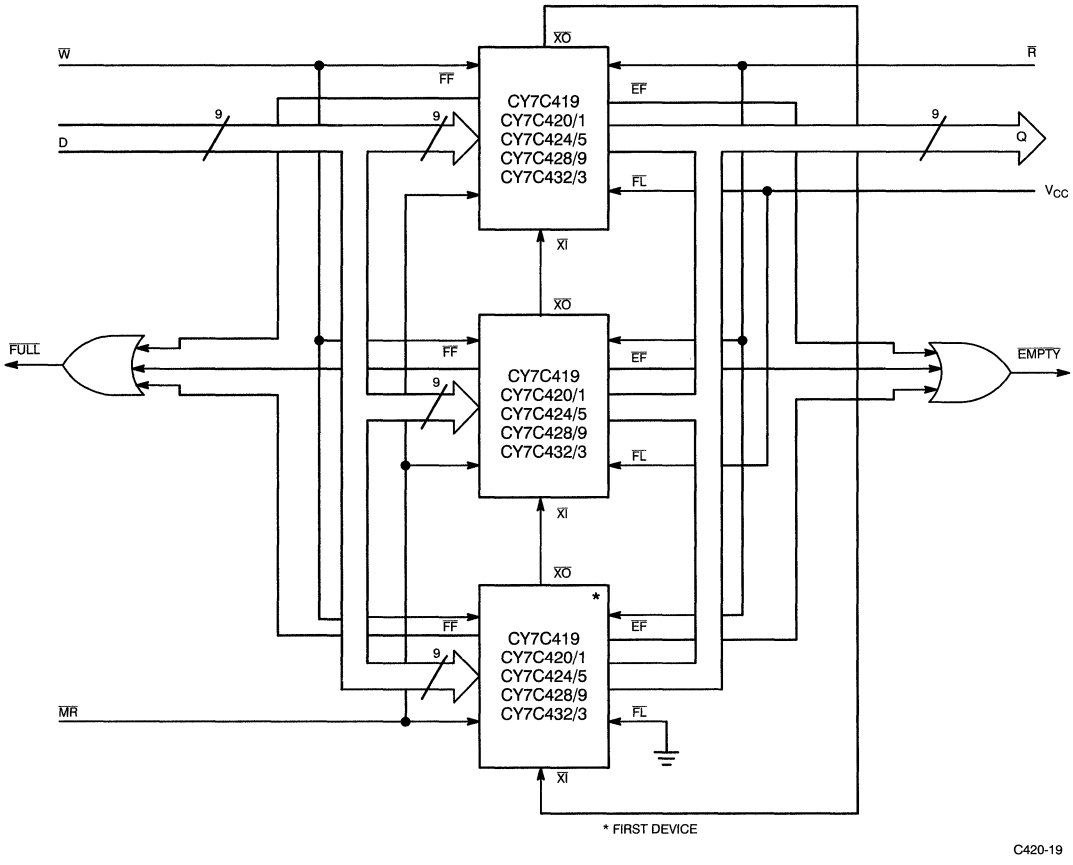


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C419–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C419–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C419–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C419–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C419–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C419–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–40VC	V21	28-Lead (300-Mil) Molded SOJ	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
	CY7C419–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C419–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C419–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C419–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C419–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C419–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C419–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C419–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C420–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C420–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C420–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C420–30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C420–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C420–40PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C420–40PI	P15	28-Lead (600-Mil) Molded DIP	Industry
	CY7C420–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C420–65PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C420–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C420–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C421–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C421–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C421–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C421–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C421–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C421–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C421–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C421–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C421–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C421–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C421–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C421–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C421–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C424–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C424–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C424–30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C424–40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C424–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C424–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C424–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C425–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C425–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C425–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C425–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C425–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C425–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C425–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C425–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C425–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C425–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C425–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C425–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C425–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CY7C428–20PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
25	CY7C428–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–25PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–25DMB	D16	28-Lead (600-Mil) CerDIP	Military
30	CY7C428–30PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C428–40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C428–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C428–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C428–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7C429–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C429–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C429–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C429–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C429–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C429–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40VC	V21	28-Lead (300-Mil) Molded SOJ	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
40	CY7C429–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C429–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C429–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C429–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C429–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C429–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C429–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C429–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C432–25PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
30	CY7C432–30PC	P15	28-Lead (600-Mil) Molded DIP	Commerical
	CY7C432–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C432–40PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C432–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C432–65PC	P15	28-Lead (600-Mil) Molded DIP	Commercial
	CY7C432–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C433–10AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–10PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–10VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C433–15AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–15PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–15VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–15LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C433–20AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–20PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–20VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C433–25AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–25PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C433–30AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C433–40AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C433–65AC	A32	32-Pin Thin Plastic Quad Flatpack	Commercial
	CY7C433–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VI	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{CC1}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38-00079-L

CY7C4421/4201/4211/4221
CY7C4231/4241/4251

64/256/512/1K/2K/4K/8K x 9 Synchronous FIFOs

Features

- **64 x 9 (CY7C4421)**
- **256 x 9 (CY7C4201)**
- **512 x 9 (CY7C4211)**
- **1K x 9 (CY7C4221)**
- **2K x 9 (CY7C4231)**
- **4K x 9 (CY7C4241)**
- **8K x 9 (CY7C4251)**
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin compatible and functionally equivalent to IDT72421, 72201, 72211, 72221, 72231, 72241**
- **Fully asynchronous and simultaneous read and write operation**
- **Four status flags: Empty, Full, and programmable Almost Empty/Almost Full**
- **Expandable in width**
- **Low operating power**
  I_{CC2} = 50 mA
- **Output Enable ($\overline{OE}$) pin**
- **32-pin PLCC/TQFP**

Functional Description

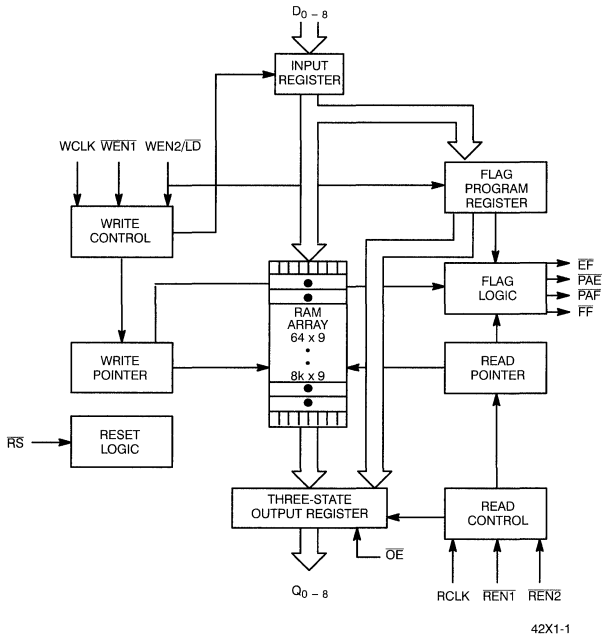
The CY7C42X1 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 9 bits wide. The CY7C42X1 are pin-compatible to IDT722X1. The CY7C42X1 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1 has an output enable pin ($\overline{OE}$). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

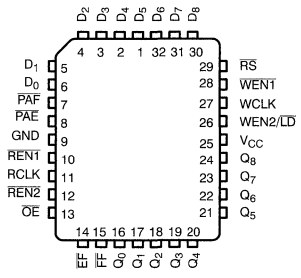
Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram

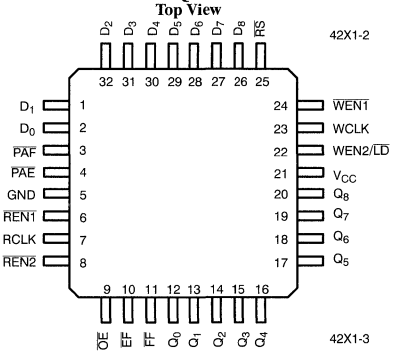


Pin Configuration

PLCC
Top View



TQFP
Top View



42X1-2

42X1-3

5

Functional Description (continued)

The CY7C42X1 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty-7 and Full-7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 4001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C42X1–10	7C42X1–15	7C42X1–25	7C42X1–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Operating Current (I_{CC5}) (mA)	Commercial	50	50	50	50
	Industrial	70	70	70	70

	CY7C4421	CY7C4201	CY7C4211	CY7C4221	CY7C4231	CY7C4241	CY7C4251
Density	64 x 9	256 x 9	512 x 9	1K x 9	2K x 9	4K x 9	8K x 9

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	Data Inputs for 9-bit bus
Q_{0-8}	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or lead the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	Enables the device for Read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

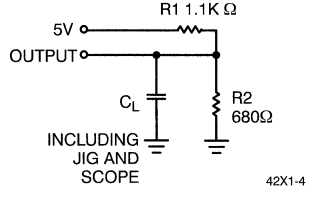
Electrical Characteristics Over the Operating Range[2]

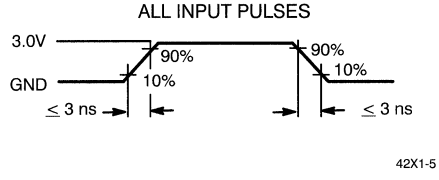
Parameter	Description	Test Conditions		7C42X1–10 Min.	7C42X1–10 Max.	7C42X1–15 Min.	7C42X1–15 Max.	7C42X1–25 Min.	7C42X1–25 Max.	7C42X1– 35 Min.	7C42X1– 35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{CC1}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		150		130		75		60	mA
			Ind		170		150		95		80	mA
I_{CC2}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		50		50		50		50	mA
			Ind		70		70		70		70	mA
I_{SB}[6]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		28		25		22	mA
			Ind		40		38		35		35	mA

Capacitance[7]

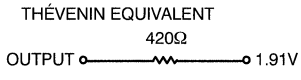
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[8, 9]





Equivalent to: THÉVENIN EQUIVALENT



Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time for not more than one second.
4. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
5. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
6. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
7. Tested initially and after any design or process changes that may affect these parameters.
8. C_L = 30 pF for all AC parameters except for t_{OHZ}.
9. C_L = 5 pF for t_{OHZ}.

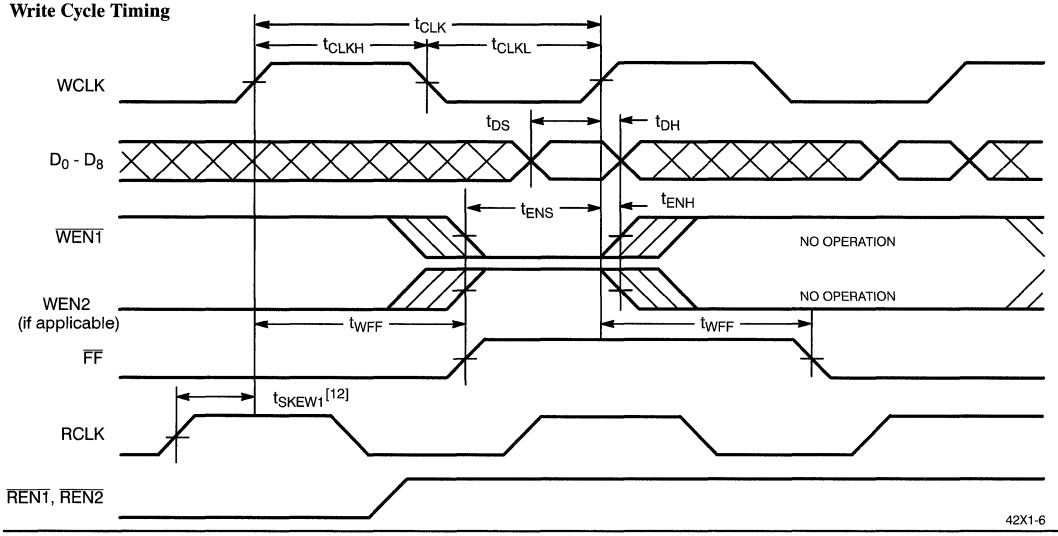
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1–10		7C42X1–15		7C42X1–25		7C42X1–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	ns
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[10]	10		15		25		35		ns
t_{RSS}	Reset Set-Up Time	8		10		15		20		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{OLZ}	Output Enable to Output in Low Z[11]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[11]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	10		15		18		20		ns

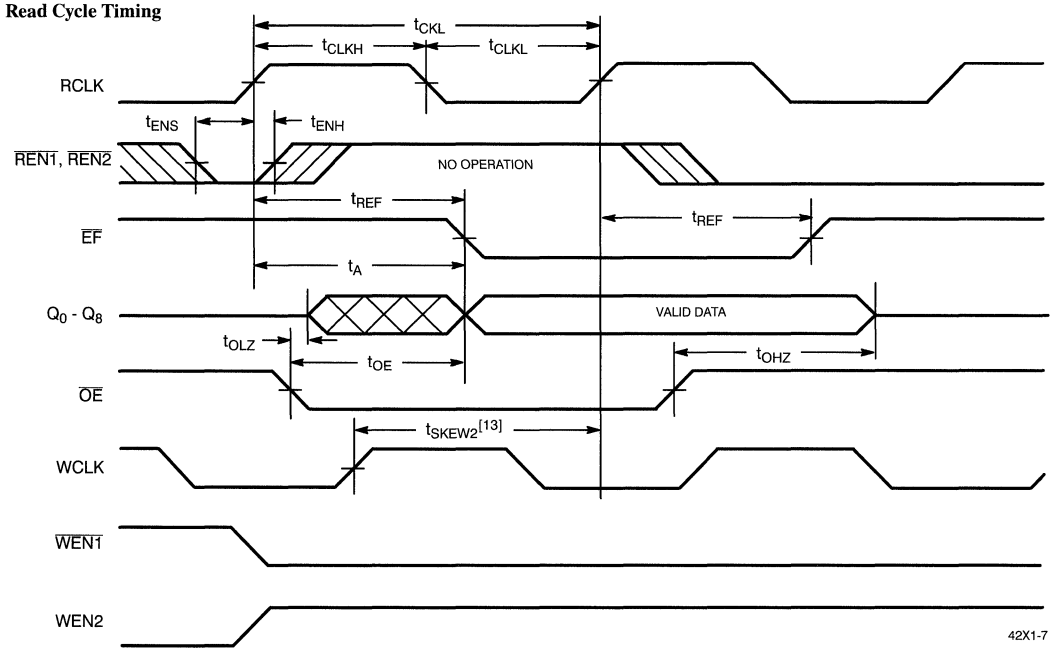
Notes:
10. Pulse widths less than minimum values are not allowed.
11. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

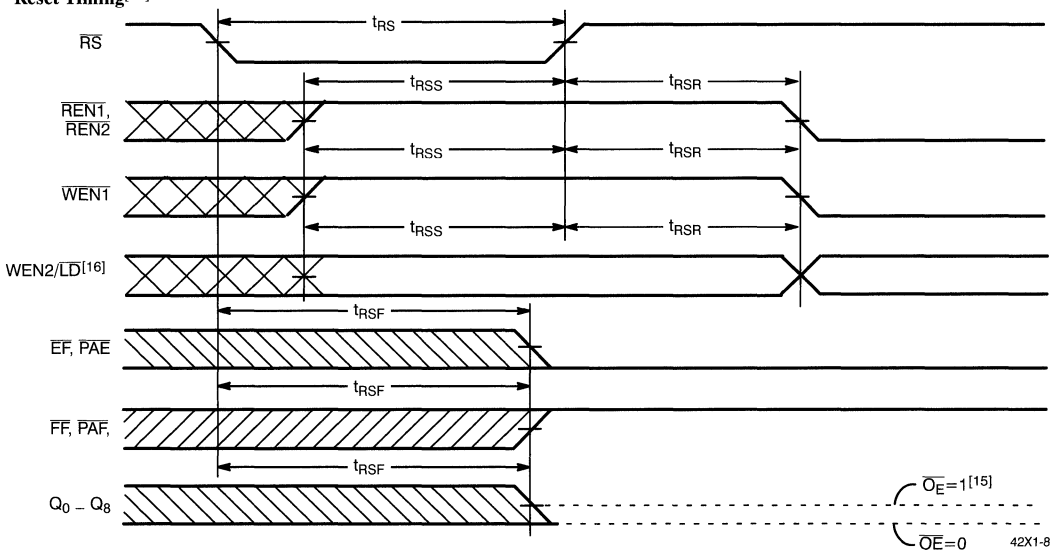


Notes:

12. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.
13. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Switching Waveforms (continued)

Reset Timing[14]

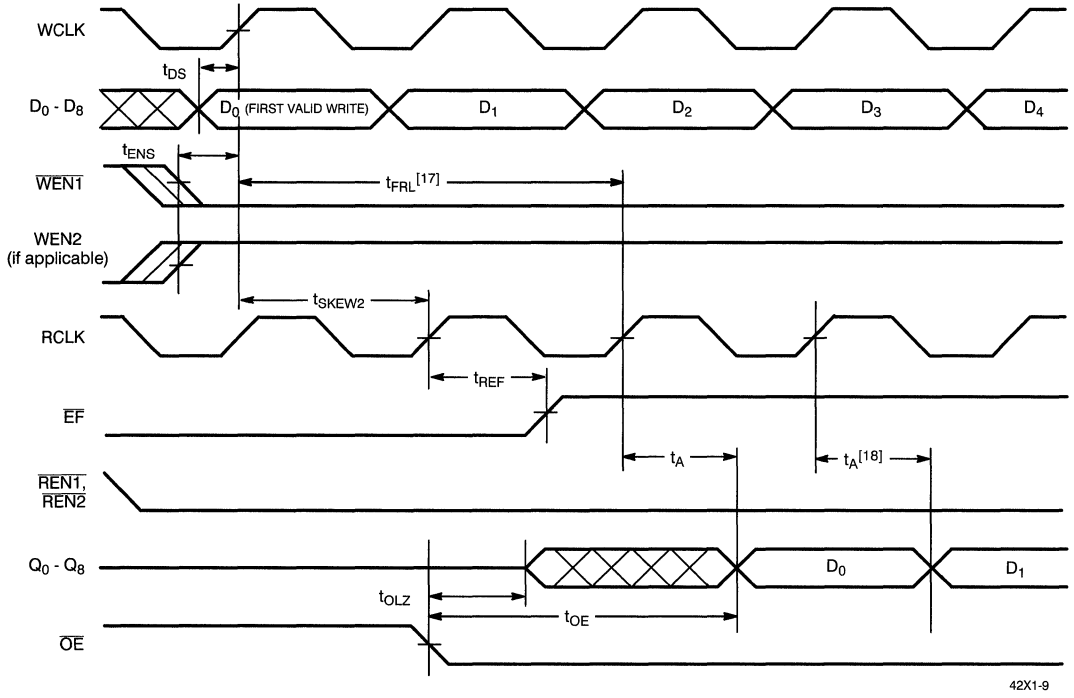


Notes:

14. The clocks (RCLK, WCLK) can be free-running during reset.
15. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
16. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)

First Data Word Latency after Reset with Simultaneous Read and Write

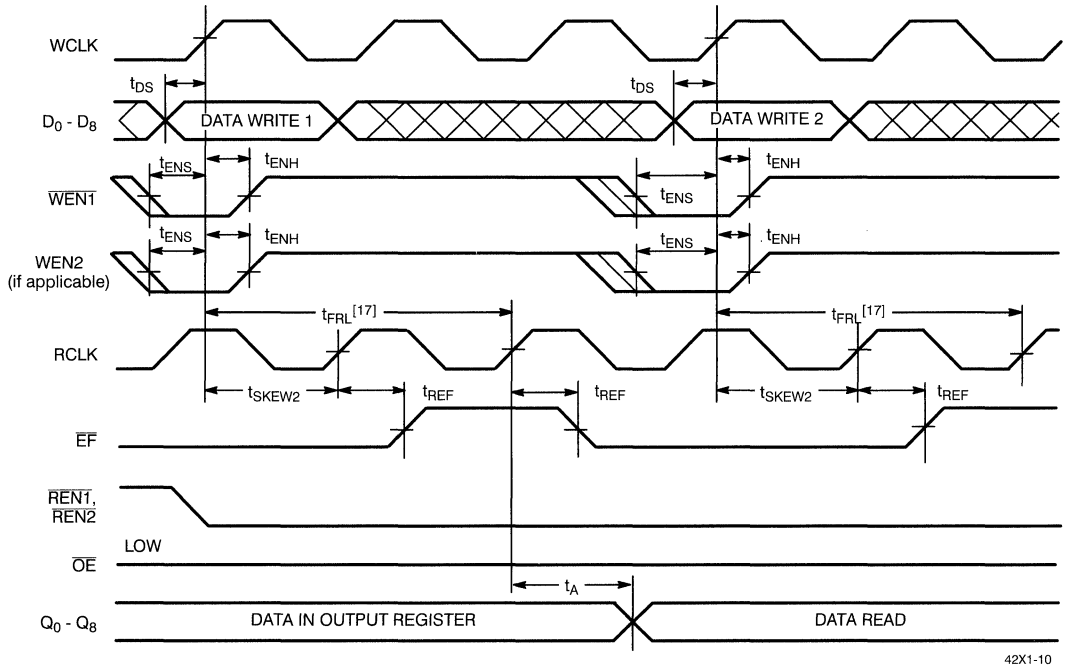


Notes:

17. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
18. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

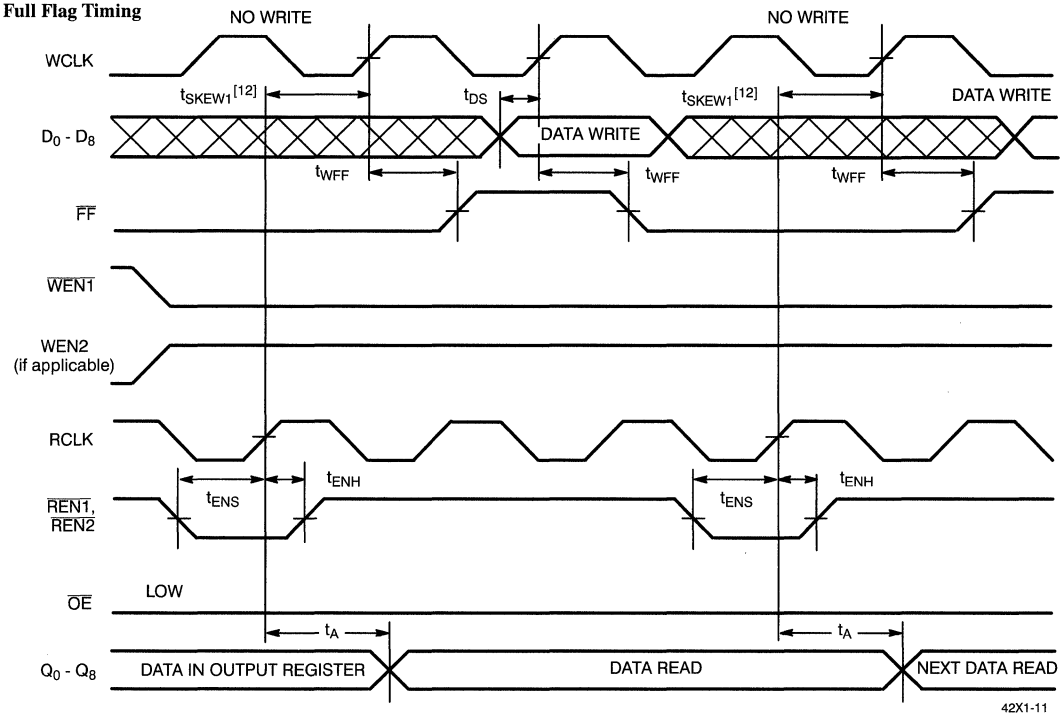
Switching Waveforms (continued)

Empty Flag Timing



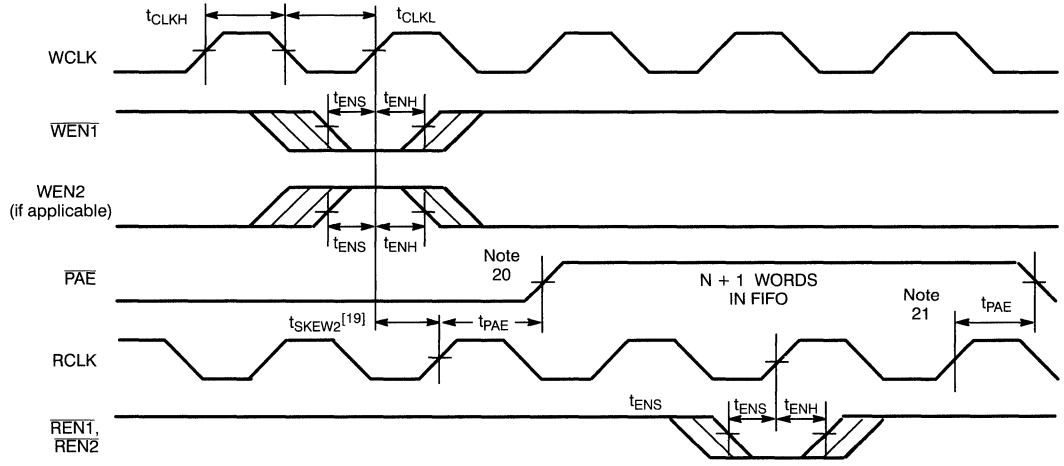
Switching Waveforms (continued)

Full Flag Timing

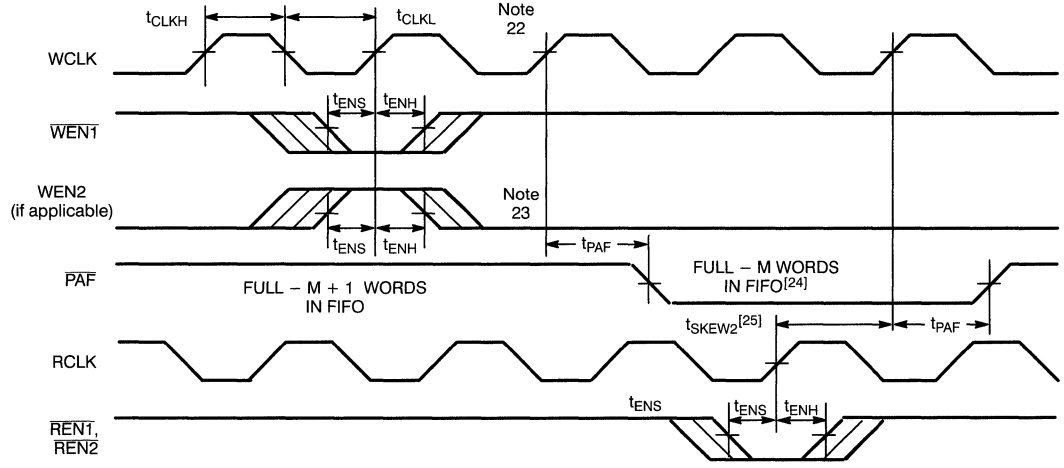


Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Full Flag Timing

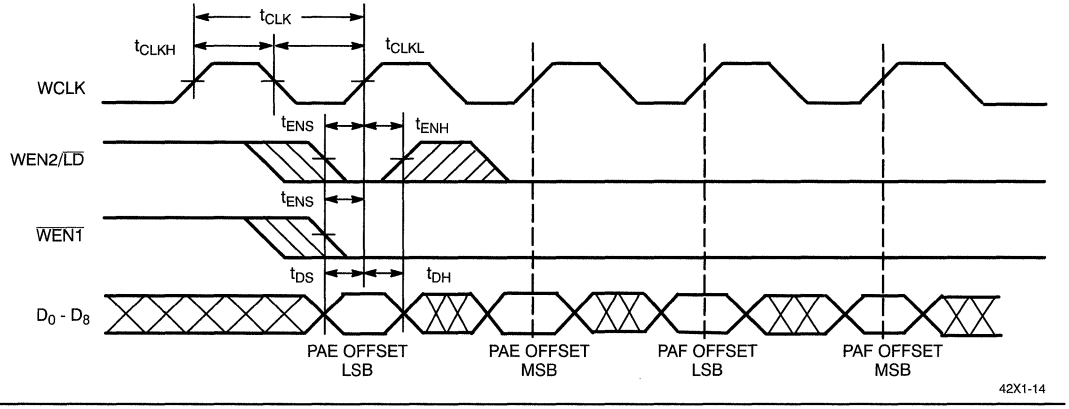


Notes:

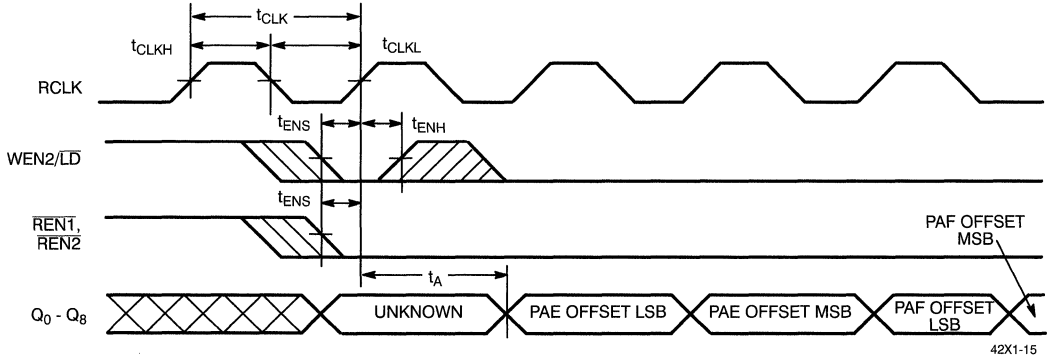
19. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
20. PAE offset – n.
21. If a read is preformed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
22. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
23. PAF offset = m.
24. 64–m words for CY7C4421, 256–m words in FIFO for CY7C4201, 512–m words for CY7C4211, 1024–m words for CY7C4221, 2048–m words for CY7C4231, 4096–m words for CY7C4241, 8192–m words for CY7C4251.
25. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising.

Switching Waveforms (continued)

Write Programmable Registers



Read Programmable Registers



Architecture

The CY7C42X1 consists of an array of 64 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$) – If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data

is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$) – This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

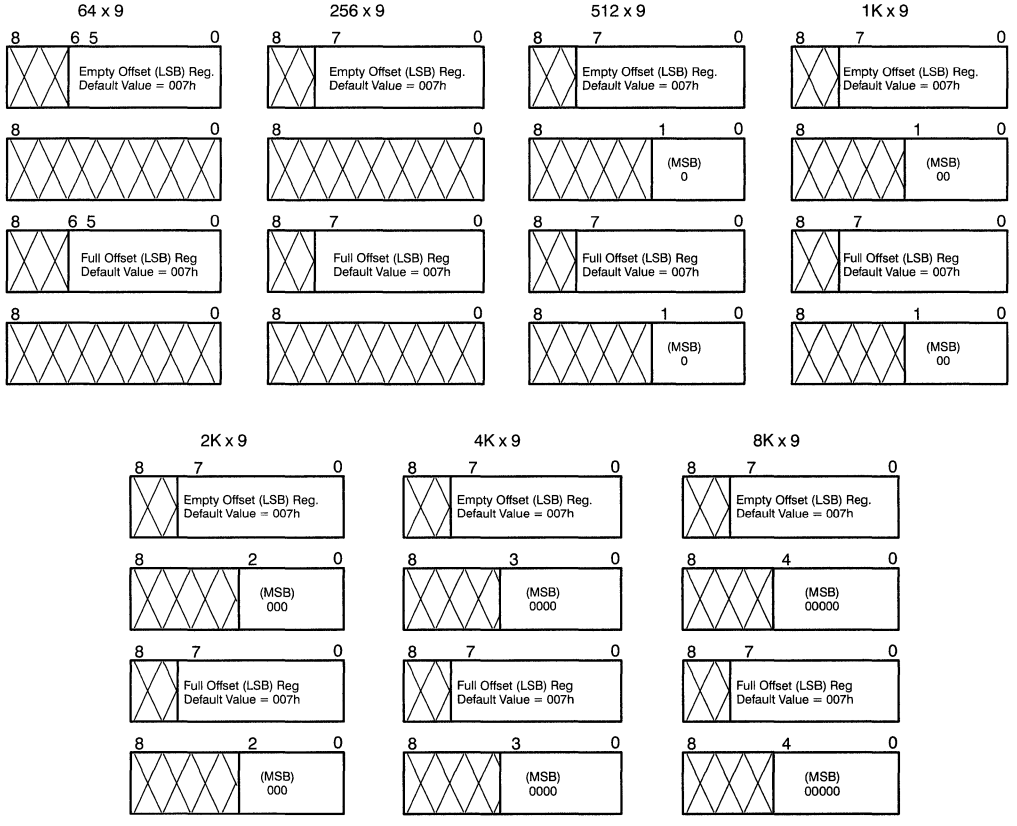


Figure 1. Offset Register Location and Default Values

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

$\overline{LD}$	$\overline{WEN}$	WCLK[26]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4421. (64−m), CY7C4201 (256−m), CY7C4211 (512−m), CY7C4221 (1K−m), CY7C4231 (2K−m), CY7C4241 (4K−m), and CY7C4251 (8K−m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO						
CY7C4421	CY7C4201	CY7C4211	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[27]	1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H
33 to (64−(m+1))	129 to (256−(m+1))	257 to (512−(m+1))	H	H	H	H
(64−m)[28] to 63	(256−m)[28] to 255	(512−m)[28] to 511	H	L	H	H
64	256	512	L	L	H	H

Number of Words in FIFO							
CY7C4221	CY7C4231	CY7C4241	CY7C4251	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	H	H	L	L
1 to n[27]	1 to n[27]	1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	(n+1) to 4096	H	H	H	H
513 to (1024 −(m+1))	1025 to (2048 −(m+1))	2049 to (4096 −(m+1))	4097 to (8182 −(m+1))	H	H	H	H
(1024−m)[28] to 1023	(2048−m)[28] to 2047	(4096−m)[28] to 4095	(8182−m)[28] to 8181	H	L	H	H
1024	2048	4096	8182	L	L	H	H

Notes:

26. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.
27. n = Empty Offset (n=7 default value).
28. m = Full Offset (m=7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

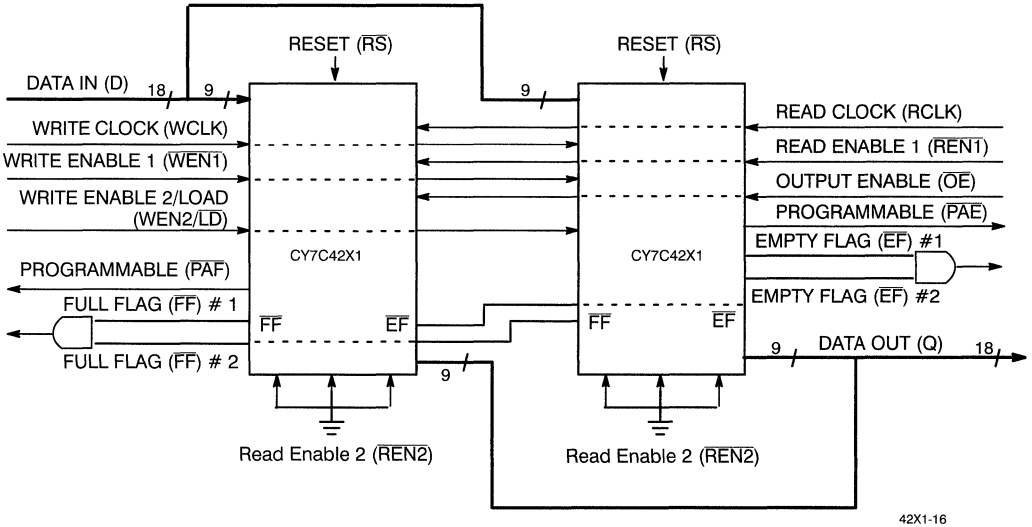
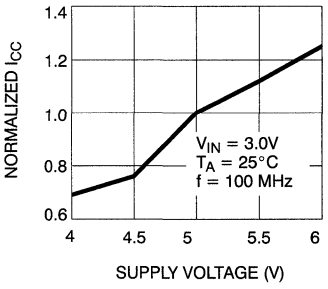


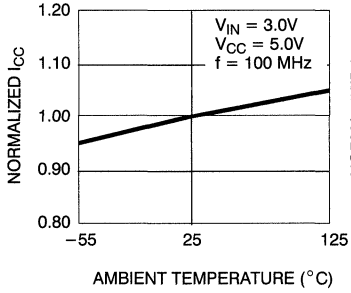
Figure 2. Block Diagram of 64 x 9,256 x 9,512 x 9,1024 x 9,2048 x 9,4096 x 9,8192 x 9 Synchronous FIFO Memory Used in a Width Expansion Configuration

Typical AC and DC Characteristics

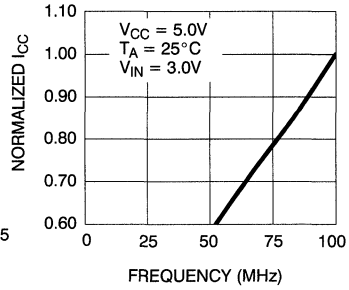
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



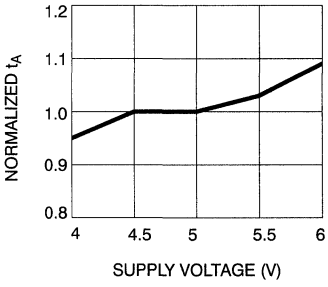
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



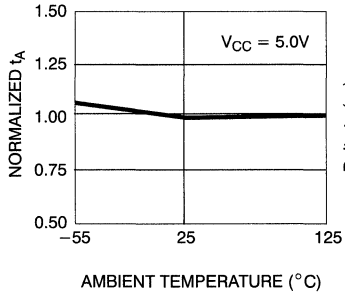
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



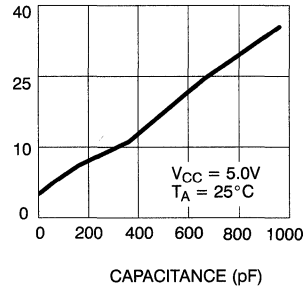
NORMALIZED t_A vs. SUPPLY VOLTAGE



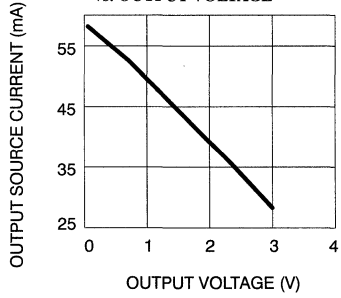
NORMALIZED t_A vs. AMBIENT TEMPERATURE



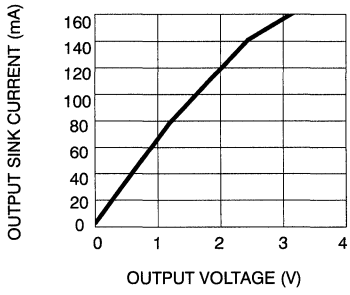
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4421-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4421-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4421-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4421-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4421-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4421-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4421-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4201-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4201-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4201-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4201-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4201-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4201-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4201-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4211–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4211–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4211–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4211–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4211–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4211–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4211–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4221–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4221–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4221–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4221–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4221–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4221–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4221–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4231–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4231–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4231–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4231–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4231–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4231–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4231–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4241–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4241–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4241–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4241–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4241–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4241–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4241–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4251–10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4251–15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4251–25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4251–35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4251–35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4251–35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4251–35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Document #: 38–00419

CY7C4425/4205/4215
CY7C4225/4235/4245

64, 256, 512, 1K, 2K, 4K x 18 Synchronous FIFOs

Features

- **64 x 18 (CY7C4425)**
- **256 x 18 (CY7C4205)**
- **512 x 18 (CY7C4215)**
- **1K x 18 (CY7C4225)**
- **2K x 18 (CY7C4235)**
- **4K x 18 (CY7C4245)**
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin compatible and functional equivalent to IDT72425, 72205, 72215, 72225, 72235, 72245**
- **Additional features**
  - **— Retransmit**
  - **— Synchronous Almost Empty/Full flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Five status flags: Empty, Full, Half Full, and programmable Almost Empty/Almost Full**
- **Low operating power**
  - **— I_{CC1} = 100 mA**
- **Output Enable ($\overline{OE}$) pin**
- **68-pin PLCC and 64-pin TQFP**

Functional Description

The CY7C42X5 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin/functionally compatible to IDT722x5. The CY7C42X5 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

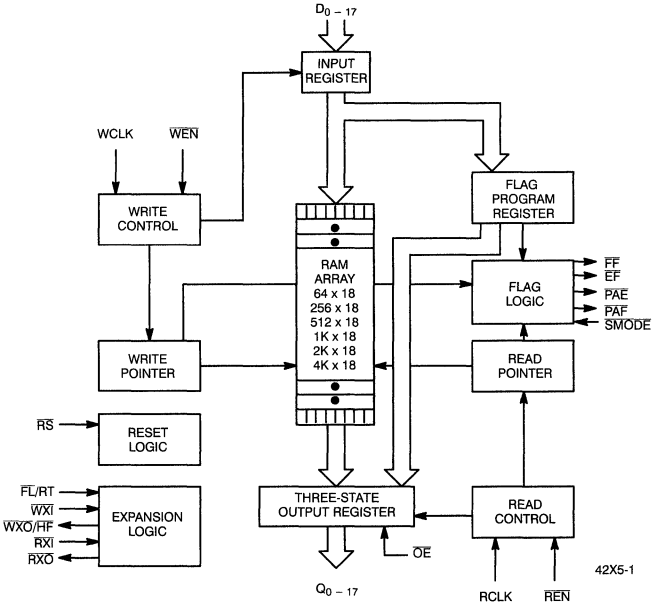
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin ($\overline{WEN}$).

When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin ($\overline{REN}$). In addition, the CY7C42X5 have an output enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

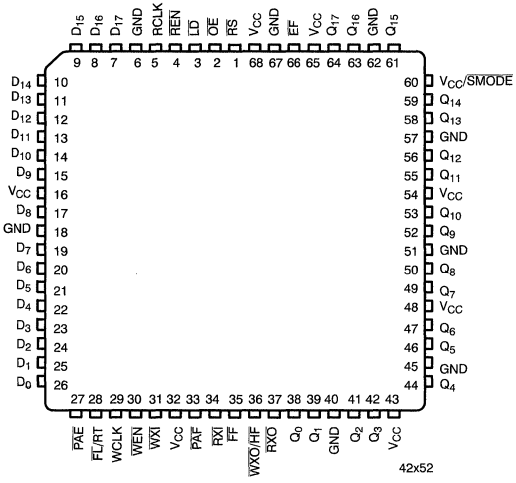
Depth expansion is possible using the cascade input ($\overline{WXI}$, $\overline{RXI}$), cascade output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

Logic Block Diagram



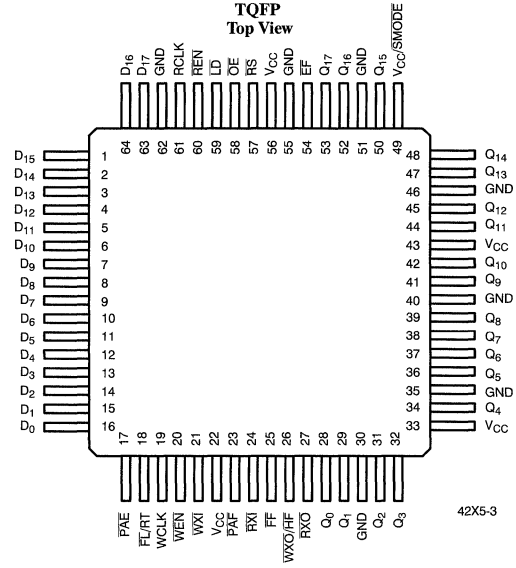
Pin Configurations

PLCC
Top View



42x52

TQFP
Top View



42X5-3

Functional Description (continued)

The CY7C42X5 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 4*). The Half Full flag shares the $\overline{WXO}$ pin. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{WXO}$) information that is used to signal the next FIFO when it will be activated.

The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. As mentioned previously, the Almost Empty/Almost Full flags become synchronous if the $V_{CC}/\overline{SMODE}$ is tied to V_{SS}. All configurations are fabricated using an advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C42X5–10	7C42X5–15	7C42X5–25	7C42X5–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Active Power Supply Current (I_{CC1}) (mA)	Commercial	100	100	100	100
	Industrial	120	120	120	120

	CY7C4425	CY7C4205	CY7C4215	CY7C4225	CY7C4235	CY7C4245
Density	64 x 18	256 x 18	512 x 18	1K x 18	2K x 18	4K x 18

Pin Definitions

Signal Name	Description	I/O	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus
$\overline{WEN}$	Write Enable	I	Enables the WCLK input
$\overline{REN}$	Read Enable	I	Enables the RCLK input
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion – Half Full status flag. Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (Q_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}/RT$	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded – The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standalone mode or width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS}. Retransmit function is also available in standalone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin Asynchronous Almost Empty/Almost Full flags – tied to V_{CC}. Synchronous Almost Empty/Almost Full flags – tied to V_{SS}. (Almost Empty synchonized to RCLK, Almost Full synchronized to WCLK.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

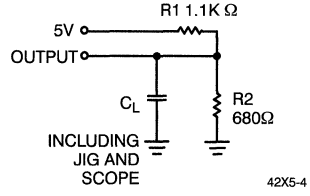
Electrical Characteristics Over the Operating Range[2]

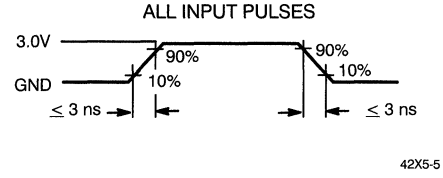
Parameter	Description	Test Conditions		7C42X5–10 Min.	7C42X5–10 Max.	7C42X5–15 Min.	7C42X5–15 Max.	7C42X5–25 Min.	7C42X5–25 Max.	7C42X5– 35 Min.	7C42X5– 35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[3]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC1}[5]	Active Power Supply Current		Com'l		100		100		100		100	mA
			Ind		120		120		120		120	mA
I_{CC2}[6]	Average Standby Current		Com'l		30		28		25		25	mA
			Ind		40		38		35		35	mA
I_{CCfmax}[7]	Operating Current at Maximum Frequency		Com'l		230		200		115		90	mA
			Ind		250		220		135		110	mA

Capacitance[8]

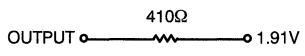
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[9, 10]





Equivalent to: THÉVENIN EQUIVALENT



Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
4. Test no more than one output at a time for not more than one second.
5. Tested at frequency = 20 MHz with outputs open.
6. All input = V_{CC} − 0.2V, except RCLK and WCLK, which are switching at maximum frequency, and $\overline{FL}/RT$ = V_{SS}.
7. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
8. Tested initially and after any design or process changes that may affect these parameters.
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.

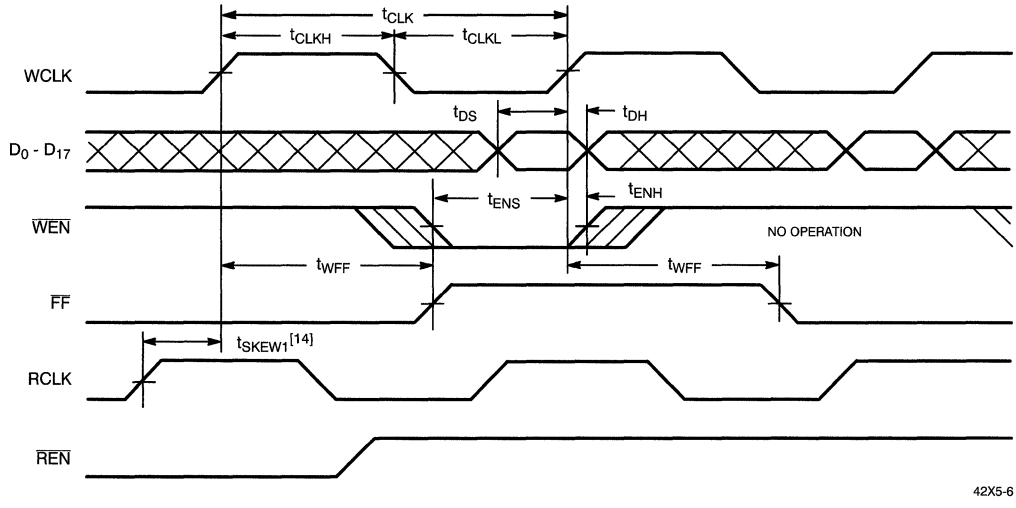
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X5–10		7C42X5–15		7C42X5–25		7C42X5–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[11]	10		15		25		35		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{PRT}	Retransmit Pulse Width	12		15		25		35		ns
t_{RTR}	Retransmit Recovery Time	12		15		25		35		ns
t_{OLZ}	Output Enable to Output in Low Z[12]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[12]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
t_{HF}	Clock to Half-Full Flag		12		16		20		25	ns
t_{XO}	Clock to Expansion Out		6		10		15		20	ns
t_{XI}	Expansion in Pulse Width	4.5		6.5		10		14		ns
t_{XIS}	Expansion in Set-Up Time	4		5		10		15		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5		6		10		12		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags (Synchronous Mode only).	10		15		18		20		ns

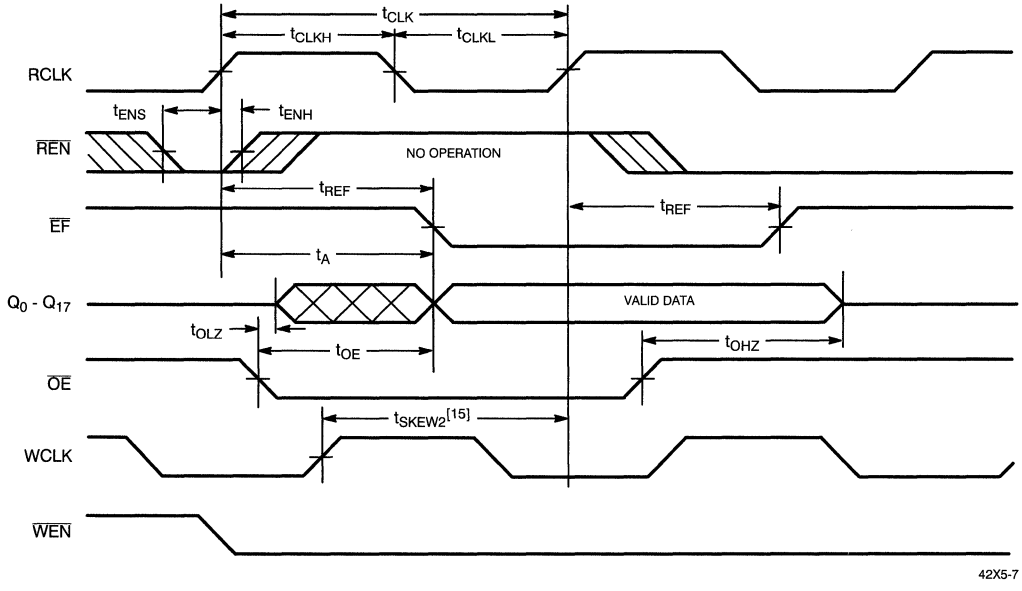
Notes:
11. Pulse widths less than minimum values are not allowed.
12. Values guaranteed by design, not currently tested.
13. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

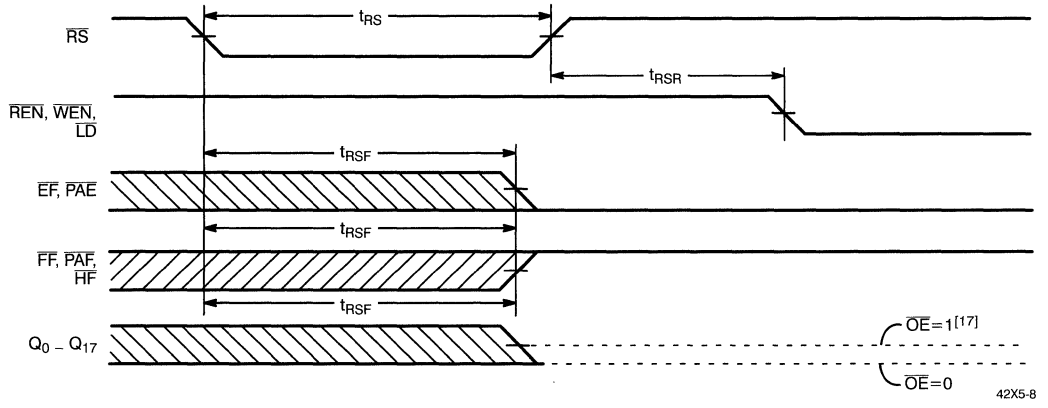


Notes:

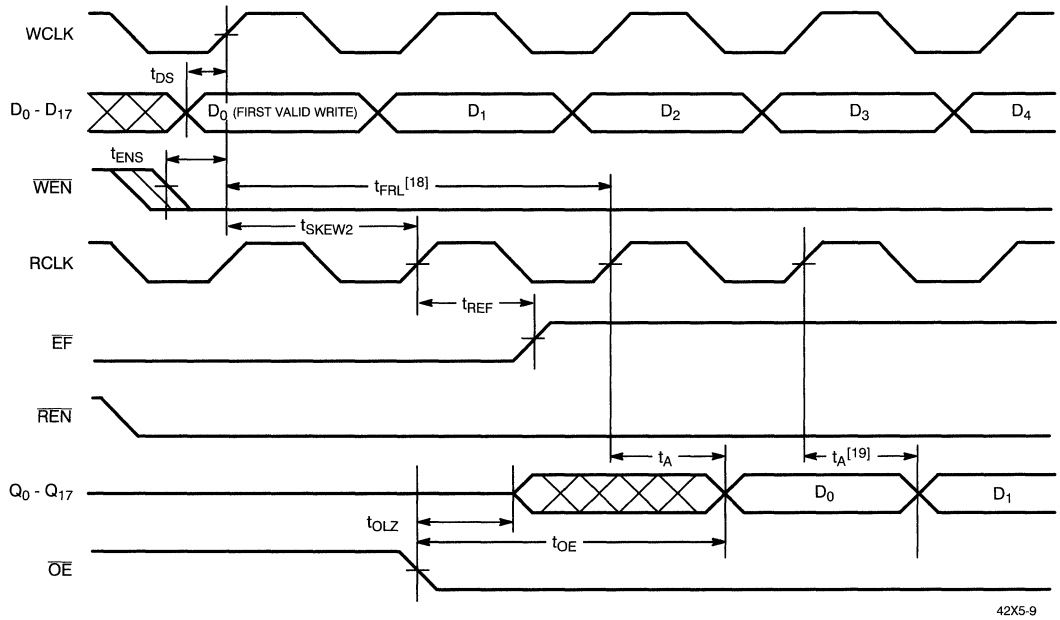
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
15. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing[16]



First Data Word Latency after Reset with Simultaneous Read and Write

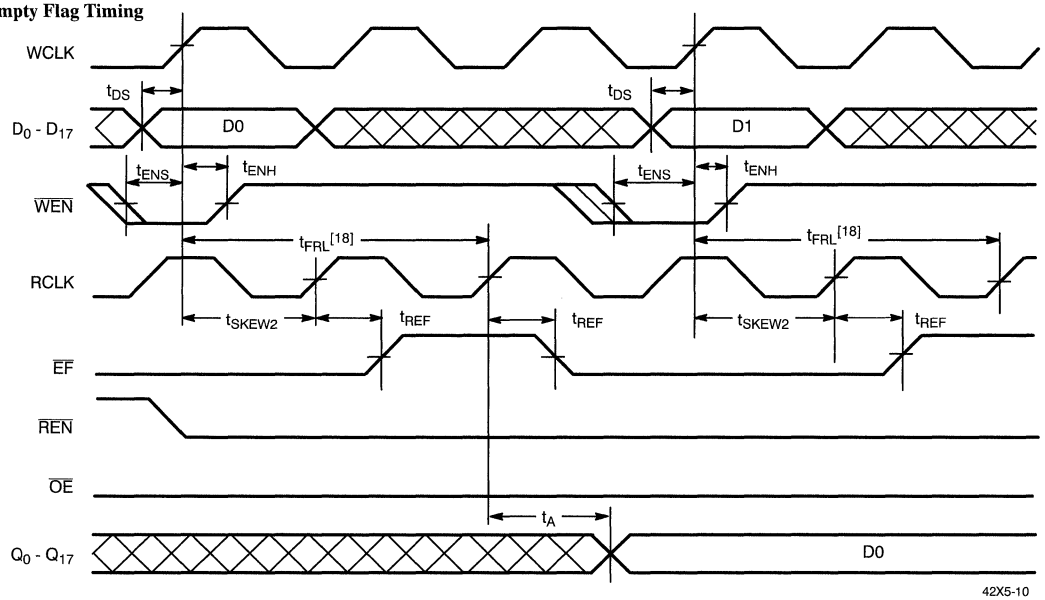


Notes:

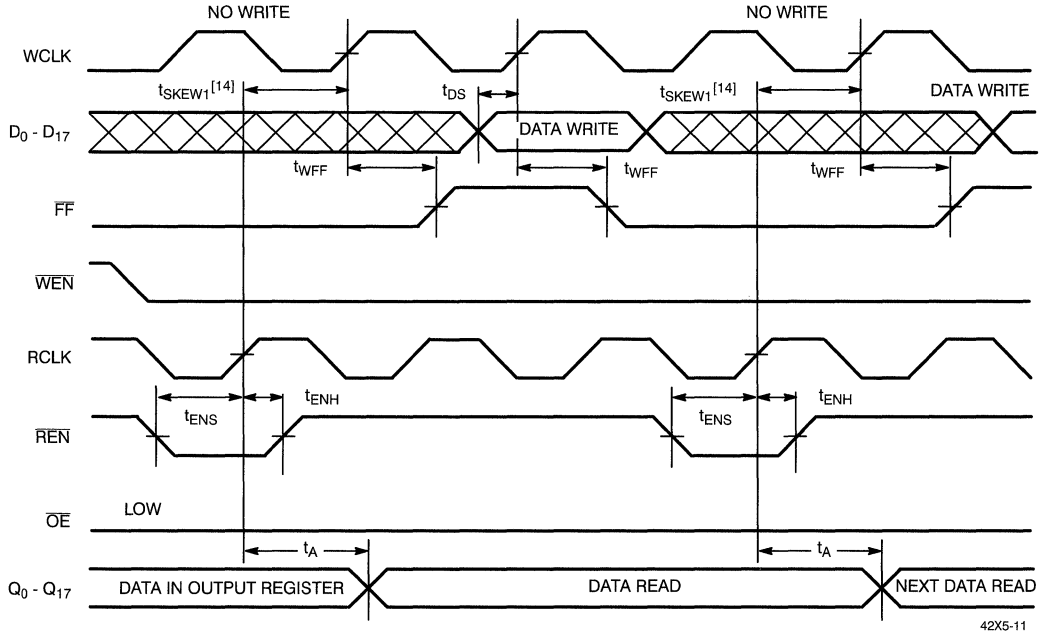
16. The clocks (RCLK, WCLK) can be free-running during reset.
17. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
18. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
19. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Switching Waveforms (continued)

Empty Flag Timing

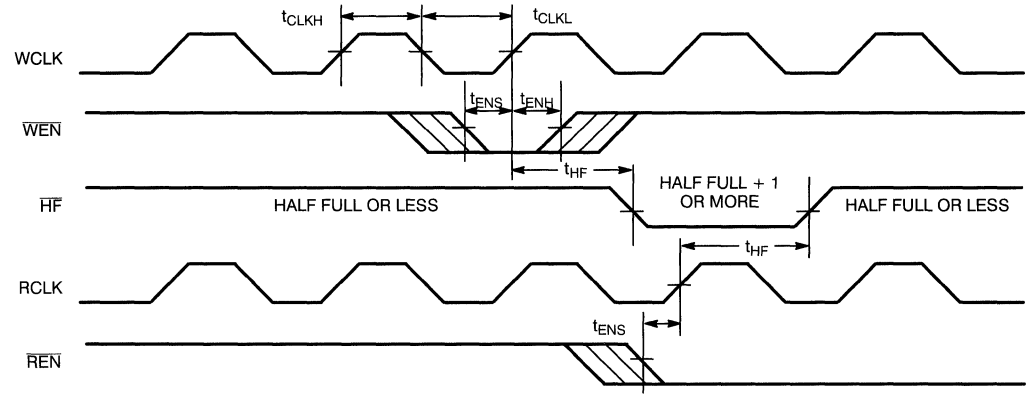


Full Flag Timing

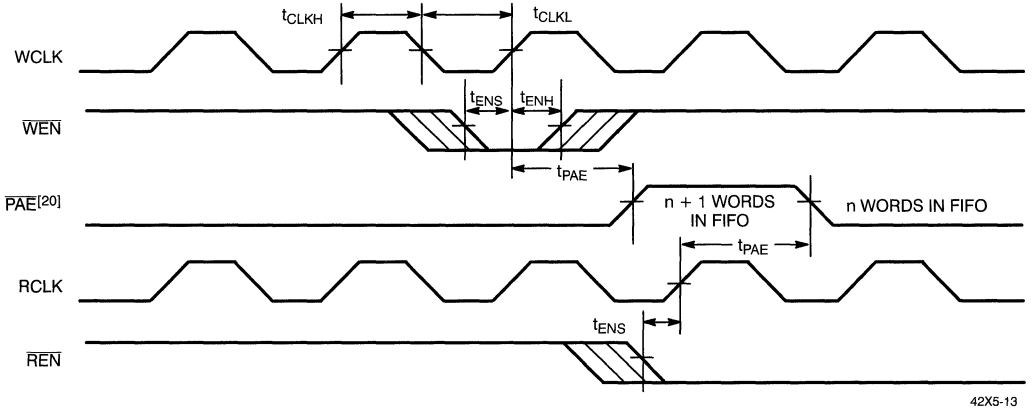


Switching Waveforms (continued)

Half-Full Flag Timing



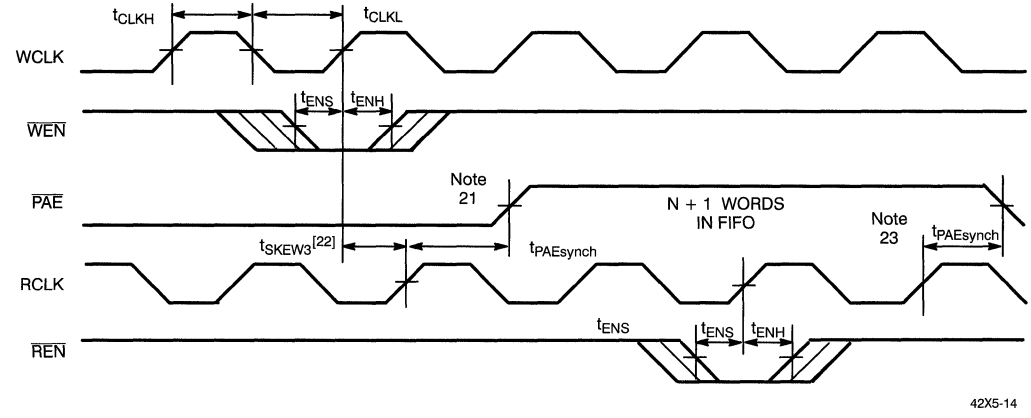
Programmable Almost Empty Flag Timing



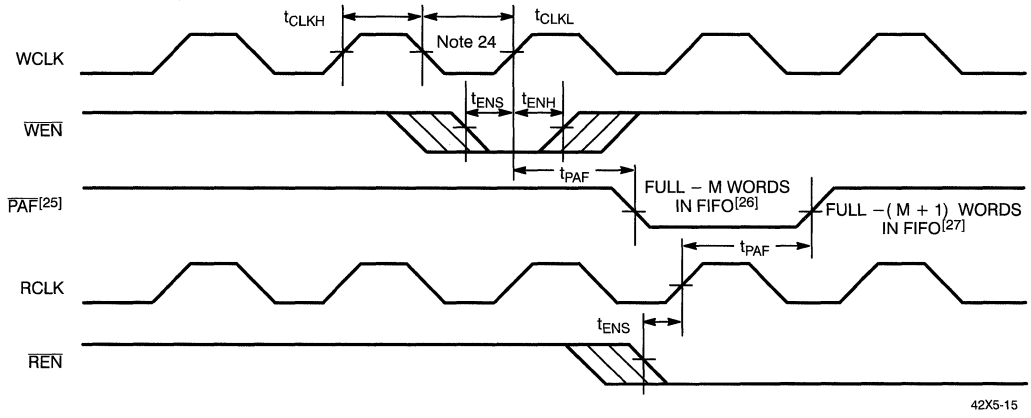
Note:
20. $\overline{PAE}$ is offset = n. Number of data words into FIFO already = n.

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing (applies only in $\overline{\text{SMODE}}$ ($\overline{\text{SMODE}}$ is LOW))



Programmable Almost Full Flag Timing

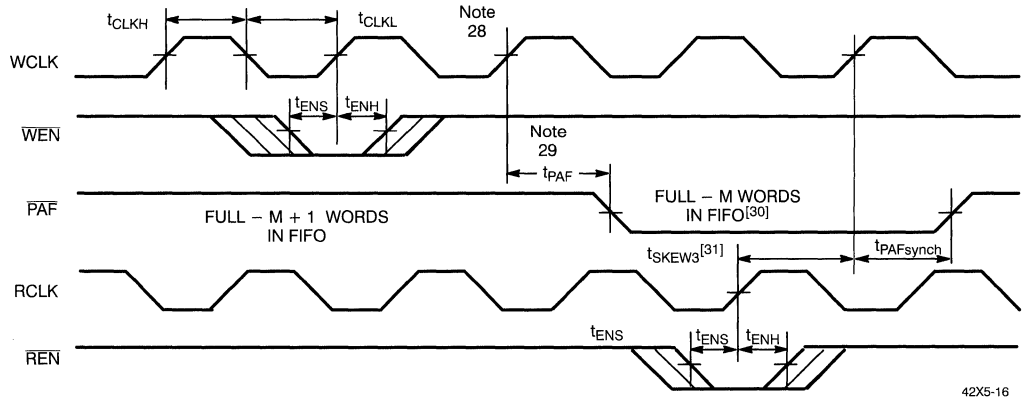


Notes:

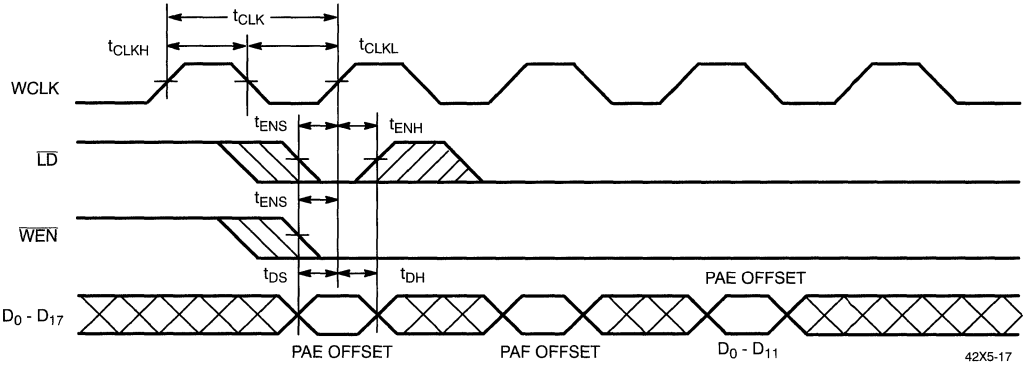
21. PAE offset – n.
22. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{\text{PAE}}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then $\overline{\text{PAE}}$ may not change state until the next RCLK.
23. If a read is preformed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{\text{PAE}}$ goes LOW.
24. PAF offset = m. Number of data words written into FIFO already = 64 – (m + 1) for the CY7C4425, 256 – (m + 1) for the CY7C4205, 512 – (m + 1) for the CY7C4215. 1024 – (m + 1) for the CY7C4225, 2048 – (m + 1) for the CY7C4235, and 4096 – (m + 1) for the CY7C4245.
25. PAF is offset = m.
26. 64 – m words in CY7C4425, 256 – m words inCY7C4205, 512 – m words in CY7C4215. 1024 – m words in CY7C4225, 2048 – m words in CY7C4235, and 4096 – m words in CY7C4245.
27. 64 – (m + 1) words in CY7C4425, 256 – (m + 1) words in CY7C4205, 512 – (m + 1) words in CY7C4215. 1024 – (m + 1) CY7C4225, 2048 – (m + 1) words in CY7C4235, and 4096 – (m + 1) words inCY7C4245.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))



Write Programmable Registers

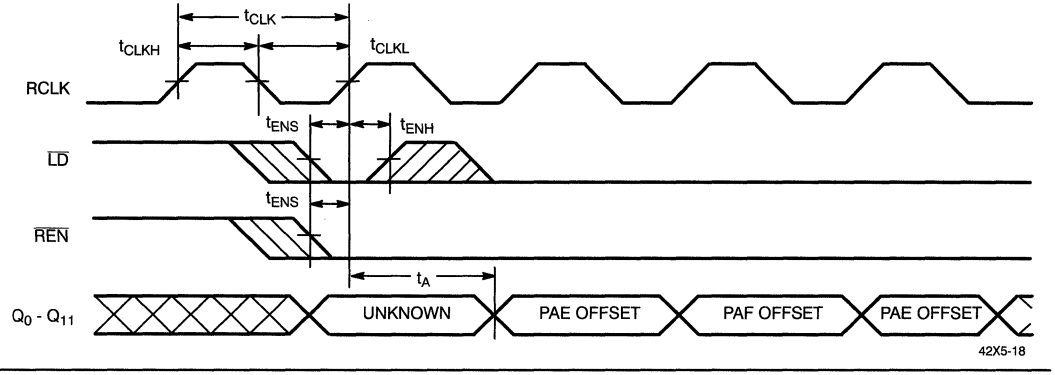


Notes:

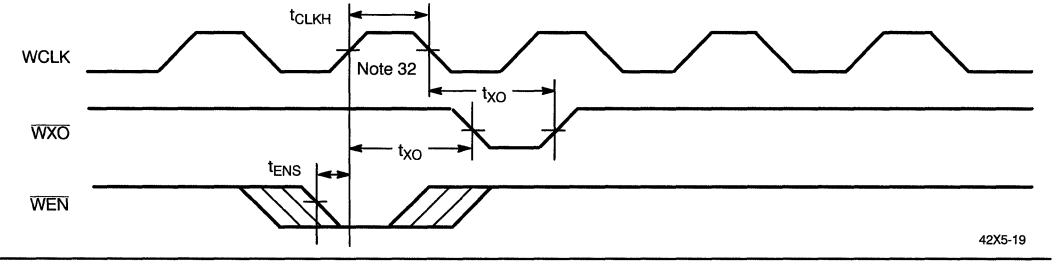
28. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words in the FIFO when $\overline{PAF}$ goes LOW.
29. PAF offset = m.
30. 64 – m words in CY7C4425 , 256 – m words in FIFO for CY7C4205, 512 – m words in CY7C4215. 1024 – m words in CY7C4225, 2048 – m words in CY7C4235, and 4096 – m words in CY7C4245.
31. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{PAF}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

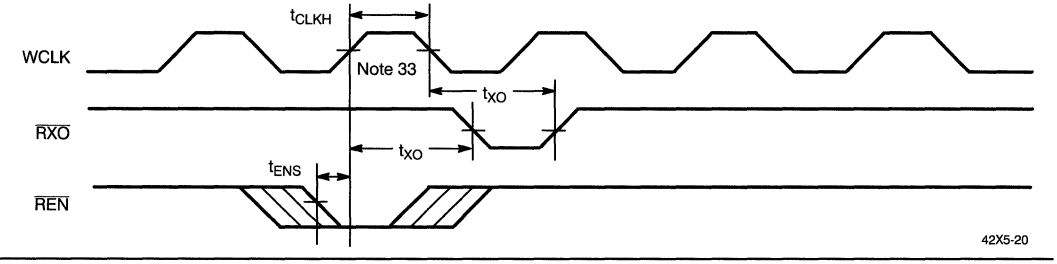
Read Programmable Registers



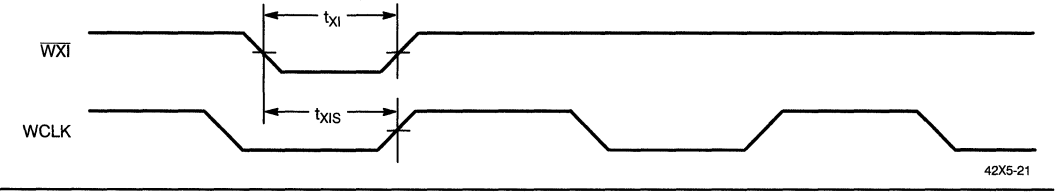
Write Expansion Out Timing



Read Expansion Out Timing



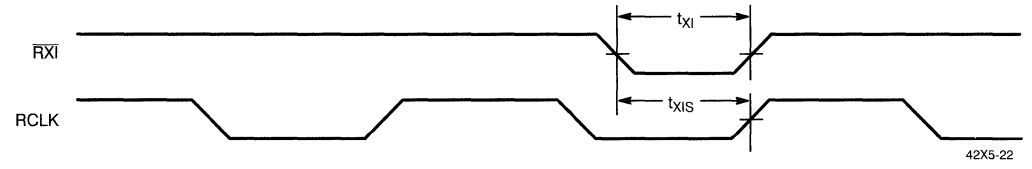
Write Expansion In Timing



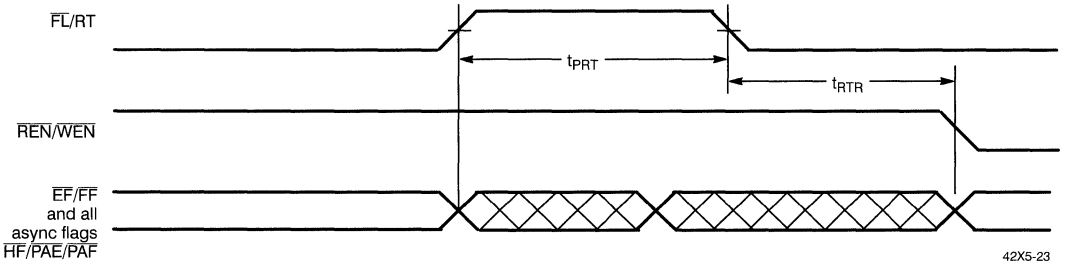
Notes:
32. Write to Last Physical Location.
33. Read from Last Physical Location.

Switching Waveforms (continued)

Read Expansion In Timing



Retransmit Timing[34, 35, 36]



Architecture

The CY7C42X5 consists of an array of 64 to 4K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, $\overline{FF}$). The CY7C42X5 also includes the control signals $\overline{WXI}$, $\overline{RXI}$, $\overline{WXO}$, $\overline{RXO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is deasserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C42X5 devices contain two 12-bit offset registers. Data present on D_{0-11} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see *Table 4*). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D_{0-11} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see *Table 3*). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written, when WCLK transitions from LOW to HIGH.

The contents of the offset registers can be read on the output pins when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Notes:

34. Clocks are free running in this case.
35. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
36. For the synchronous $\overline{PAE}$ and $\overline{PAF}$ flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Table 3. Write Offset Register

$\overline{LD}$	$\overline{WEN}$	WCLK[37]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C42X5 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C42X5 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 4* for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 4. Flag Truth Table

Number of Words in FIFO							
7C4425 – 64 x 18	7C4205 – 256 x 18	7C4215 – 512 x 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	H	L	L
1 to n[38]	1 to n[38]	1 to n[38]	H	H	H	L	H
(n+1) to 32	(n+1) to 128	(n+1) to 256	H	H	H	H	H
33 to (64−(m+1))	129 to (256−(m+1))	257 to (512−(m+1))	H	H	L	H	H
(64−m)[39] to 63	(256−m)[39] to 255	(512−m)[39] to 511	H	L	L	H	H
64	256	512	L	L	L	H	H

Number of Words in FIFO							
7C4225 – 1K x 18	7C4235 – 2K x 18	7C4245 – 4K x 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	H	L	L
1 to n[38]	1 to n[38]	1 to n[38]	H	H	H	L	H
(n+1) to 512	(n+1) to 1024	(n+1) to 2048	H	H	H	H	H
513 to (1024 −(m+1))	1025 to (2048 −(m+1))	2049 to (4096 −(m+1))	H	H	L	H	H
(1024−m)[39] to 1023	(2048−m)[39] to 2047	(4096−m)[39] to 4095	H	L	L	H	H
1024	2048	4096	L	L	L	H	H

Notes:

37. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.
38. n = Empty Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).
39. m = Full Offset (Default Values: CY7C4425 n = 7, CY7C4205 n = 31, CY7C4215 n = 63, CY7C4225/7C4235/7C4245 n = 127).

Width Expansion Configuration

The CY7C42X5 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO. This technique will avoid ready data from the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. *Figure1* demonstrates a 36-word width by using two CY7C42X5.

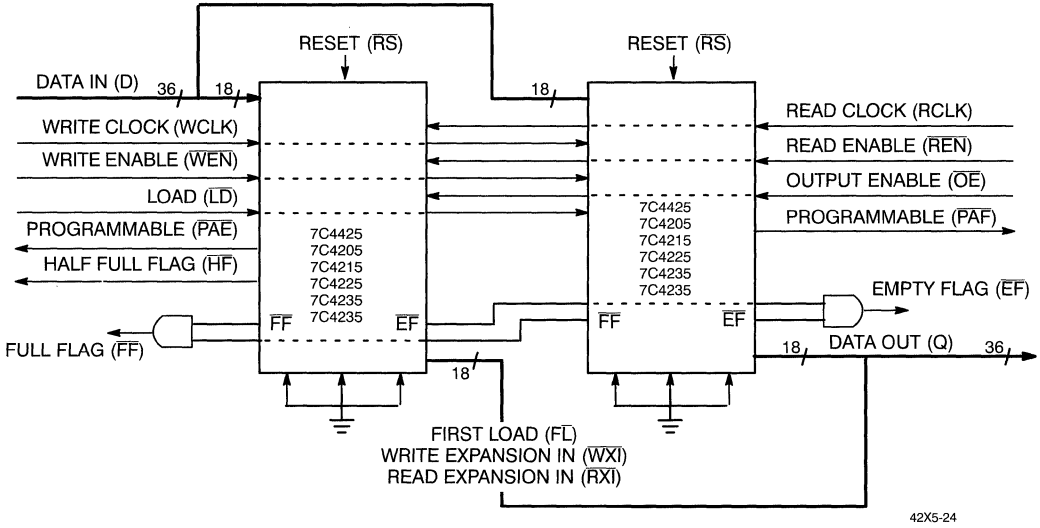


Figure 1. Block Diagram of 64 x 36/256 x 36/512 x 36/1024 x 36/2048 x 36/4096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

The CY7C42X5 can easily be adapted to applications requiring more than 64/256/512/1024/2048/4096 words of buffering. *Figure 2* shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

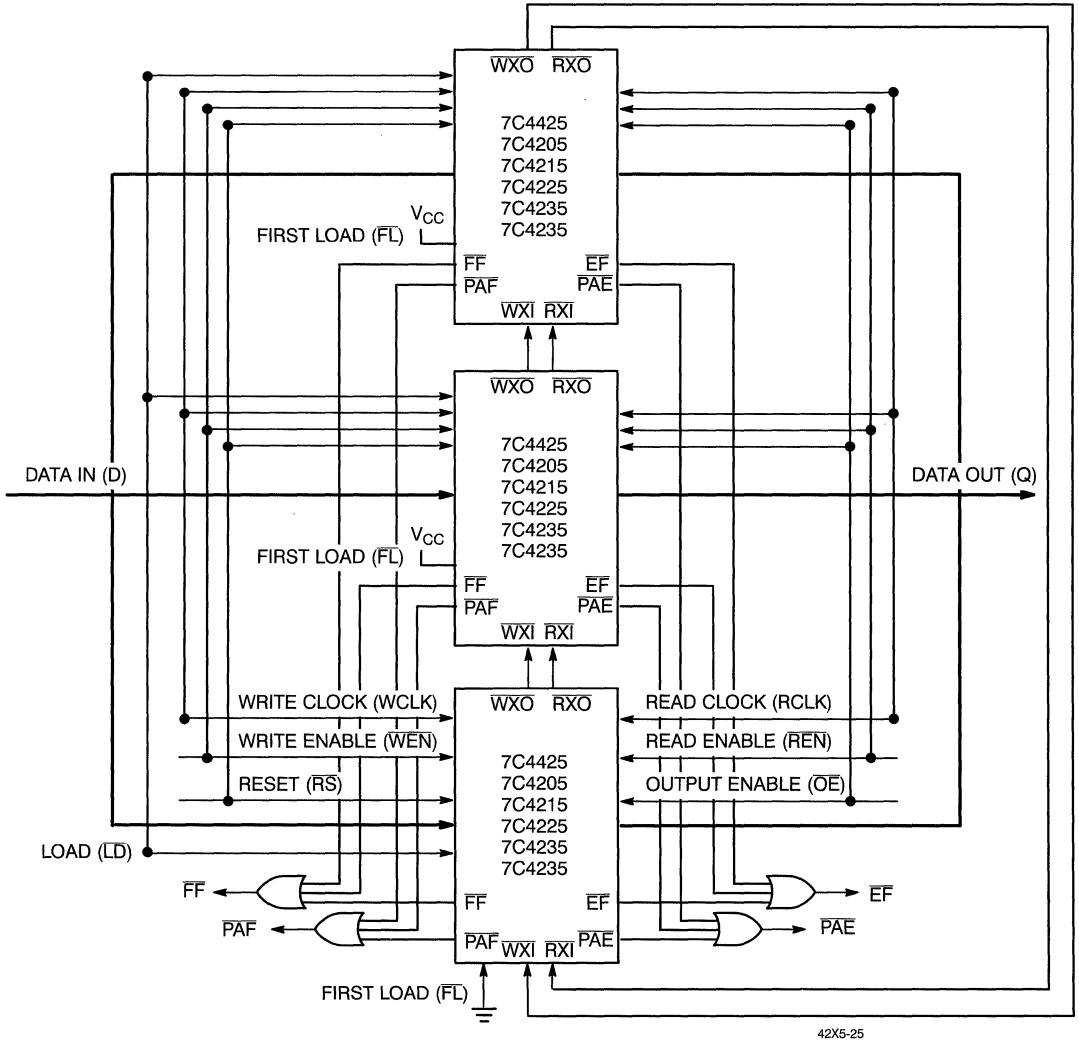
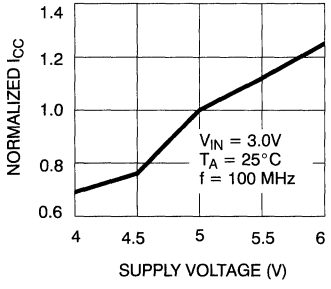
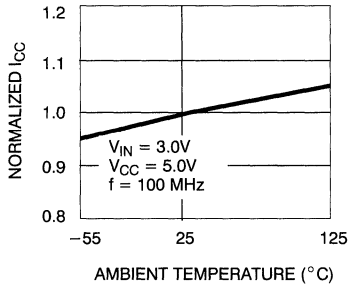


Figure 2. Block Diagram of 192 x 18/768 x 18/1536 x 18/3072 x 18/12288 x 18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

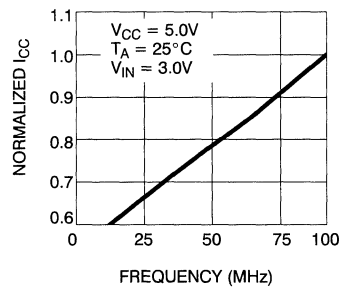
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



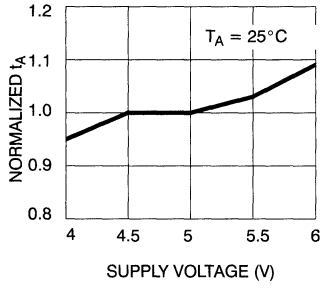
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



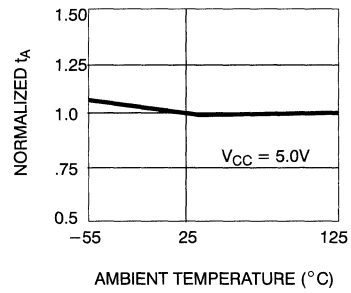
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



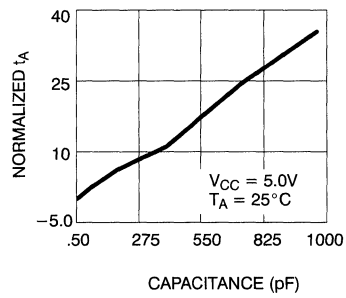
NORMALIZED t_A vs. SUPPLY VOLTAGE



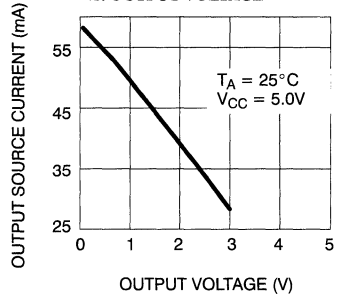
NORMALIZED t_A vs. AMBIENT TEMPERATURE



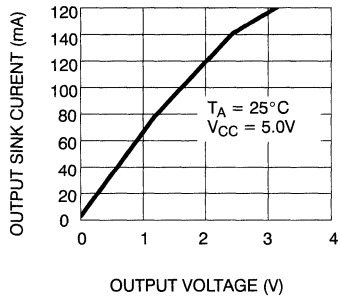
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

64 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4425–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4425–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4425–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4425–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4425–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4425–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4425–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

256 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4205–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4205–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4205–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4205–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4205–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4205–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4205–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

512 x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4215–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4215–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4215–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4215–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4215–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4215–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4215–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

1K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4225–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4225–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4225–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4225–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4225–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4225–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4225–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

2K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4235–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4235–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4235–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4235–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4235–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4235–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4235–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

4K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4245–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4245–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4245–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4245–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4245–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4245–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4245–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Document #: 38–00420–A

CY7C4255
CY7C4265

8K/16K x 18 Synchronous FIFOs

Features

- **8K x 18 (CY7C4255)**
- **16K x 18 (CY7C4265)**
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin-compatible density upgrade to CY7C42X5 family**
- **Pin-compatible density upgrade to IDT72205/15/25/35/45**
- **Additional features**
  - **— Retransmit**
  - **— Synchronous Almost Empty/Full flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Five status flags: Empty, Full, Half Full, and programmable Almost Empty/Almost Full**
- **Low operating power**
  - **— I_{CC1} = 100 mA**
- **Output Enable ($\overline{OE}$) pin**
- **68-pin PLCC and 64-pin TQFP**

Functional Description

The CY7C4255/65 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin/functionally compatible to the CY7C42X5 Synchronous FIFO family. The CY7C4255/65 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

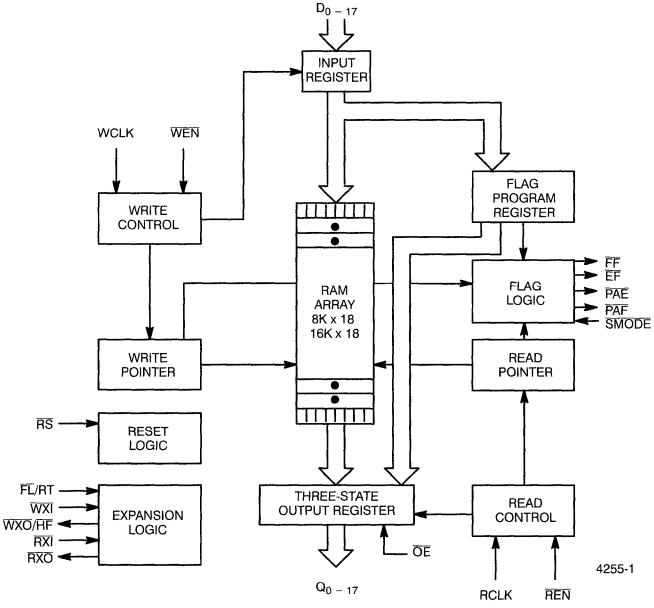
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin ($\overline{WEN}$).

When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin ($\overline{REN}$). In addition, the CY7C42X5 have an output enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

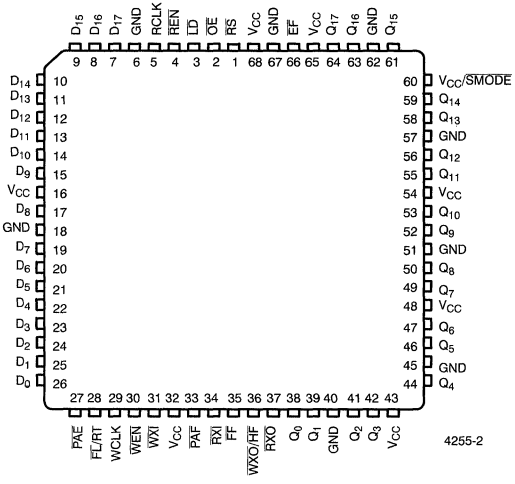
Depth expansion is possible using the cascade input ($\overline{WXI}$, $\overline{RXI}$), cascade output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

Logic Block Diagram

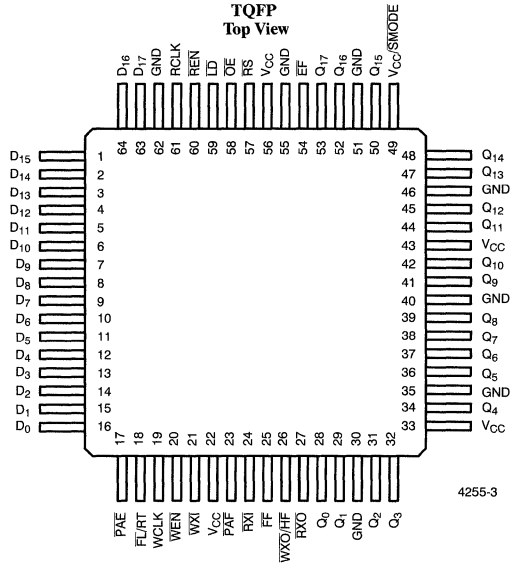


Pin Configurations

PLCC
Top View



TQFP
Top View



Functional Description (continued)

The CY7C4255/65 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 6*). The Half Full flag shares the $\overline{WXO}$ pin. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{WXO}$) information that is used to signal the next FIFO when it will be activated.

The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. As mentioned previously, the Almost Empty/Almost Full flags become synchronous if the $V_{CC}/\overline{SMODE}$ is tied to V_{SS}. All configurations are fabricated using an advanced 0.65µ N-Well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C4255/65–10	7C4255/65–15	7C4255/65–25	7C4255/65–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Active Power Supply Current (I_{CC1}) (mA)	Commercial	100	100	100	100
	Industrial	120	120	120	120

	CY7C4255	CY7C4265
Density	8K x 18	16K x 18

Pin Definitions

Signal Name	Description	I/O	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus
$\overline{WEN}$	Write Enable	I	Enables the WCLK input
$\overline{REN}$	Read Enable	I	Enables the RCLK input
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion – Half Full status flag. Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (O_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}/RT$	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded – The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standard mode of width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS}. Retransmit function is also available in standalone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin Asynchronous Almost Empty/Almost Full flags – tied to V_{CC}. Synchronous Almost Empty/Almost Full flags – tied to V_{SS}. (Almost Empty synchonized to RCLK, Almost Full synchronized to WCLK.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

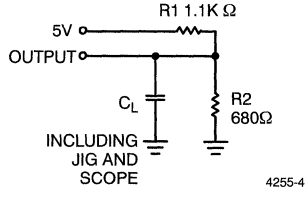
Electrical Characteristics Over the Operating Range[2]

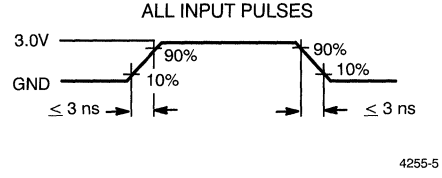
Parameter	Description	Test Conditions		7C42X5–10 Min.	7C42X5–10 Max.	7C42X5–15 Min.	7C42X5–15 Max.	7C42X5–25 Min.	7C42X5–25 Max.	7C42X5– 35 Min.	7C42X5– 35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[3]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}[4]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{CC1}[5]	Active Power Supply Current		Com'l		100		100		100		100	mA
			Ind		120		120		120		120	mA
I_{CCfMAX}.[6]	Operating Current at Maximum Frequency		Com'l		230		200		115		90	mA
			Ind		250		220		135		110	mA
I_{CC2}[7]	Average Standby Current		Com'l		30		28		25		25	mA
			Ind		40		38		35		35	mA

Capacitance[8]

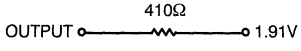
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[9, 10]





Equivalent to: THÉVENIN EQUIVALENT



Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
4. Test no more than one output at a time for not more than one second.
5. Tested at freqeumcy = 20 MHz with outputs open.
6. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
7. All inputs = V_{CC} − 0.2V, except RCLK and WCLK (which are switching at frequency = 100 MHz). All outputs are unloaded.
8. Tested initially and after any design or process changes that may affect these parameters.
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.

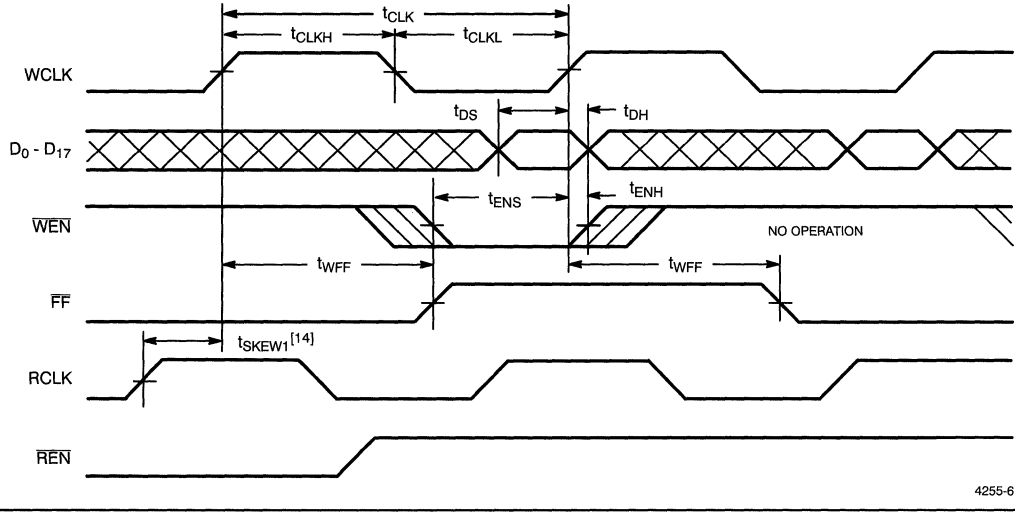
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X5–10		7C42X5–15		7C42X5–25		7C42X5–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[11]	10		15		25		35		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{PRT}	Retransmit Pulse Width	40		60		60		60		ns
t_{RTR}	Retransmit Recovery Time	90		90		90		90		ns
t_{OLZ}	Output Enable to Output in Low Z[12]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[12]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[13] (Asynchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchonous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
t_{HF}	Clock to Half-Full Flag		12		16		20		25	ns
t_{XO}	Clock to Expansion Out		7.5		10		15		20	ns
t_{XI}	Expansion in Pulse Width	4.5		6.5		10		14		ns
t_{XIS}	Expansion in Set-Up Time	2.5		5		10		15		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5		6		10		12		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags (Synchronous Mode only)	10		15		18		20		ns

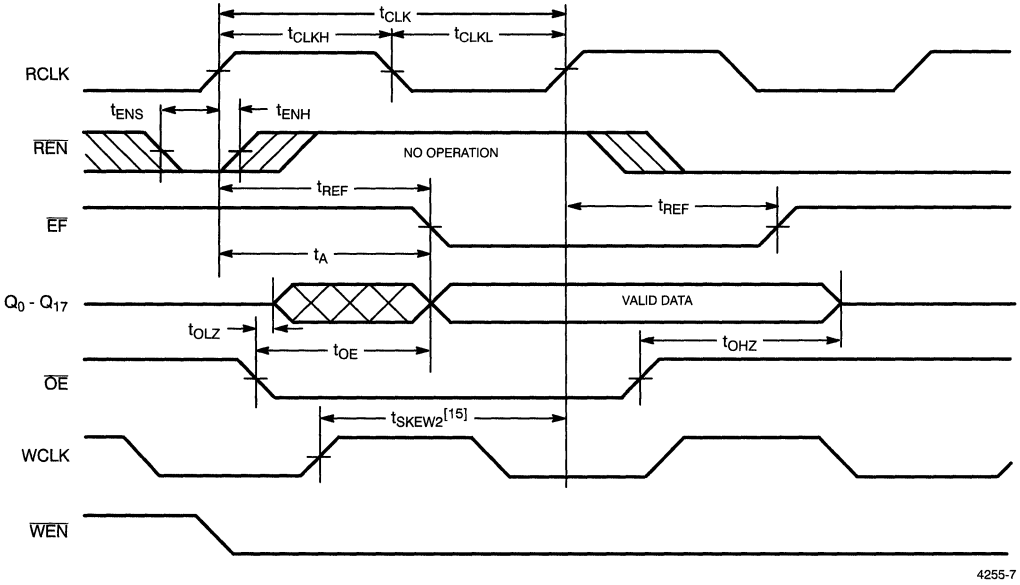
Notes:
11. Pulse widths less than minimum values are not allowed.
12. Values guaranteed by design, not currently tested.
13. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

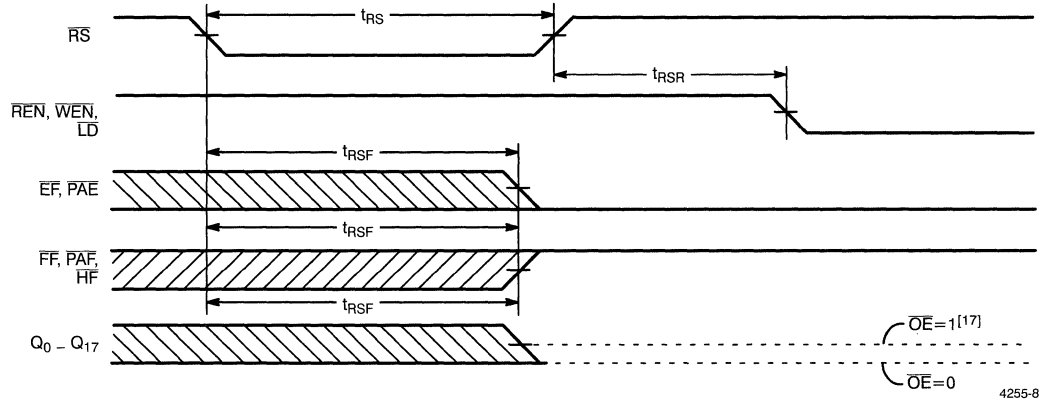


Notes:

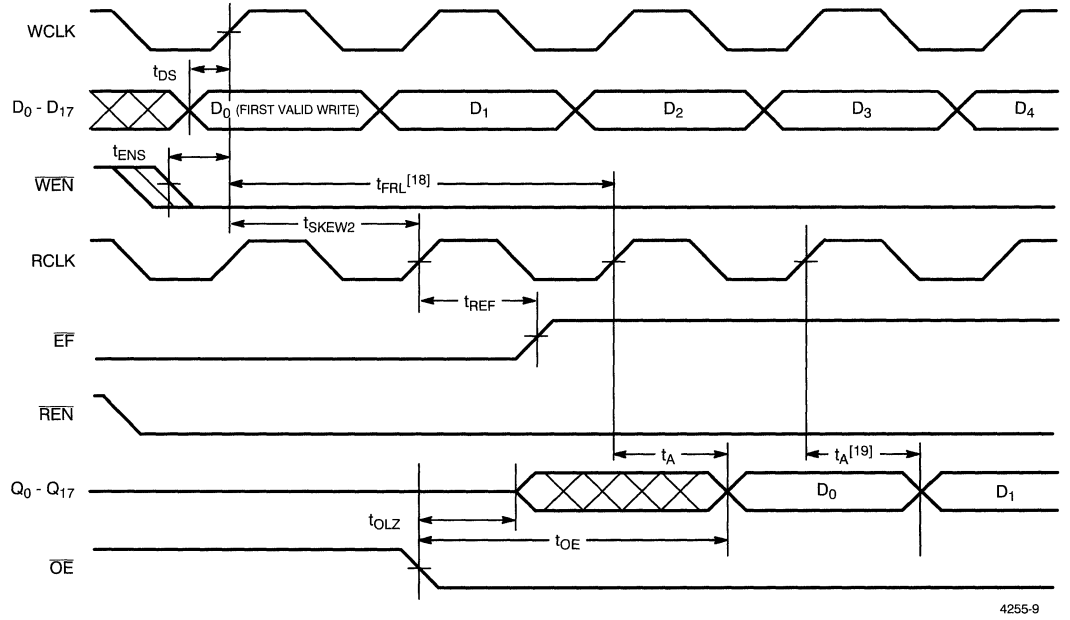
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
15. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing[16]



First Data Word Latency after Reset with Simultaneous Read and Write

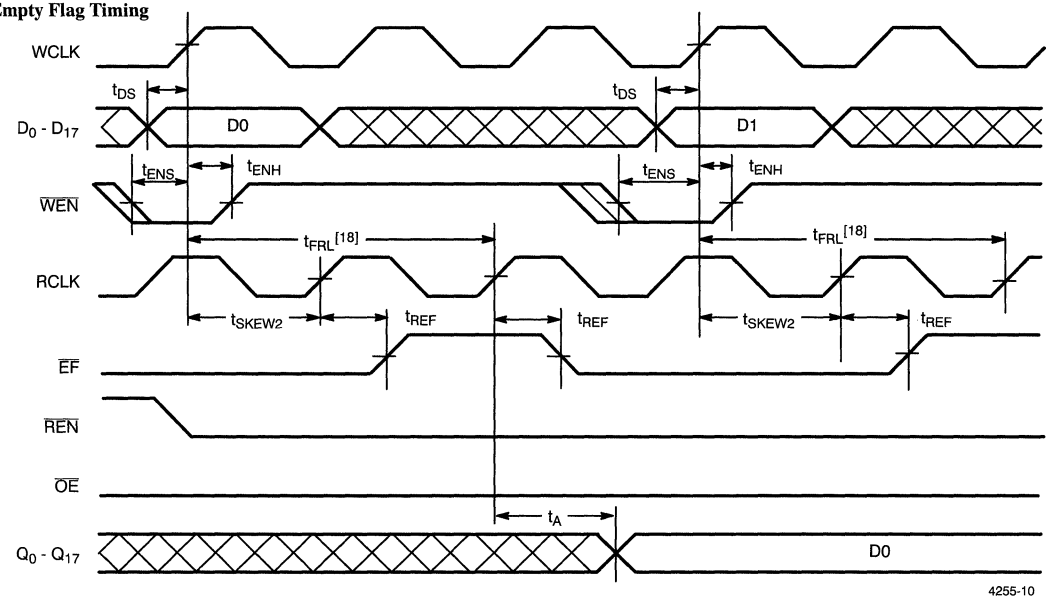


Notes:

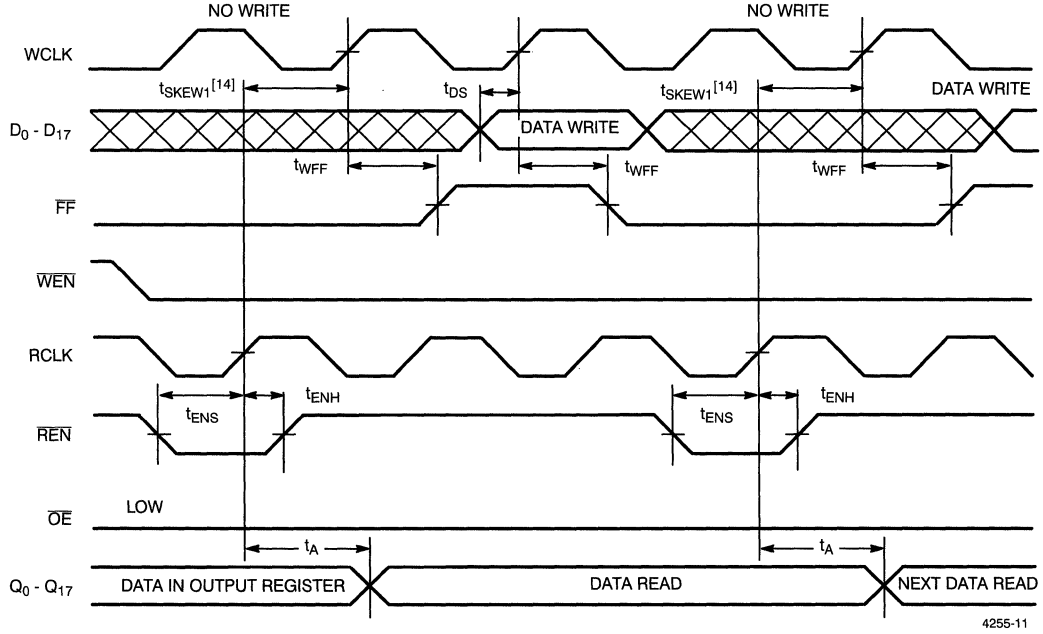
16. The clocks (RCLK, WCLK) can be free-running during reset.
17. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
18. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
19. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Switching Waveforms (continued)

Empty Flag Timing

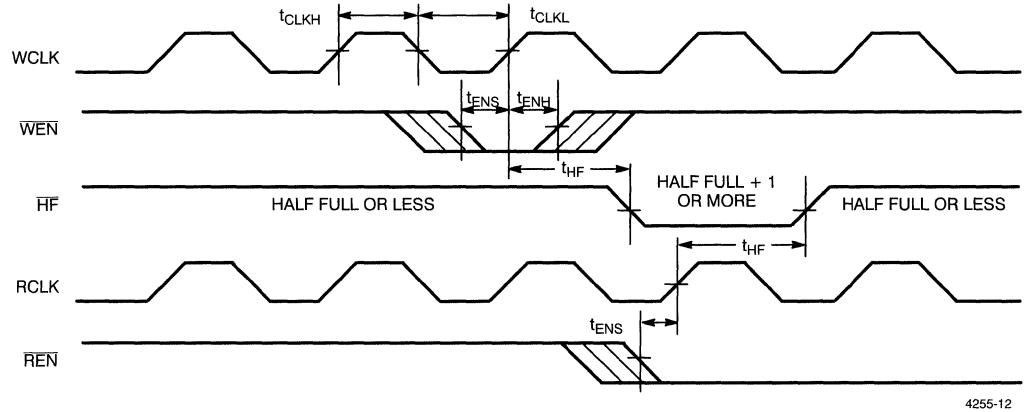


Full Flag Timing

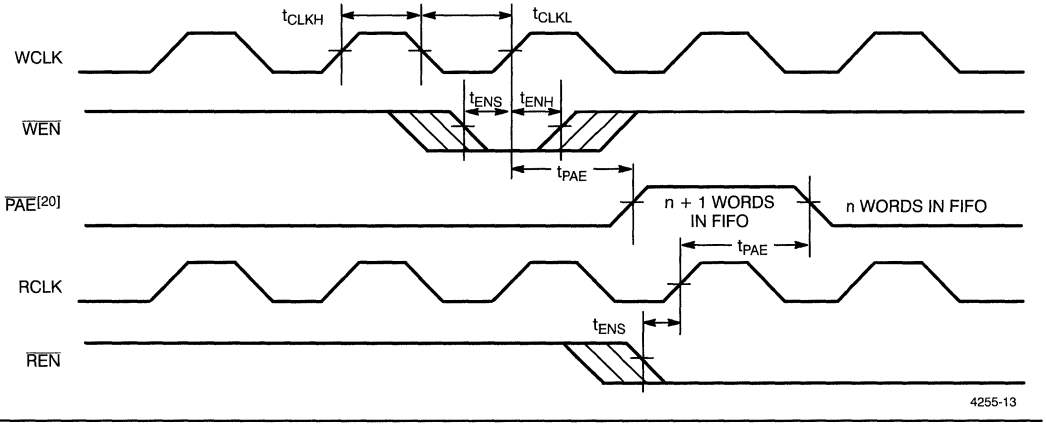


Switching Waveforms (continued)

Half-Full Flag Timing



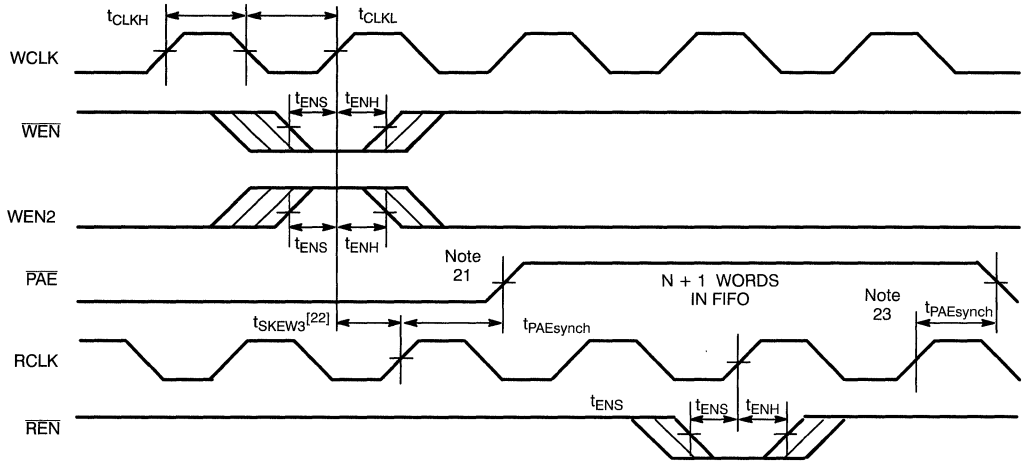
Programmable Almost Empty Flag Timing



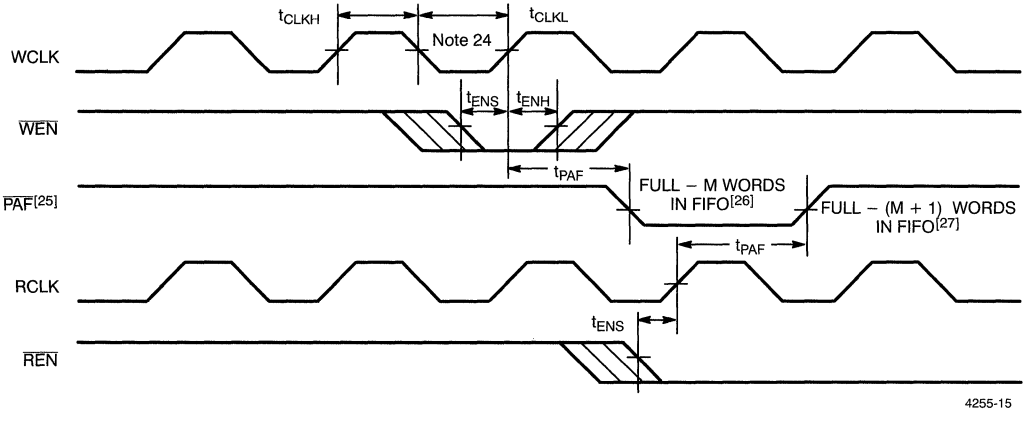
Note:
20. $\overline{PAE}$ is offset = n. Number of data words into FIFO already = n.

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))



Programmable Almost Full Flag Timing

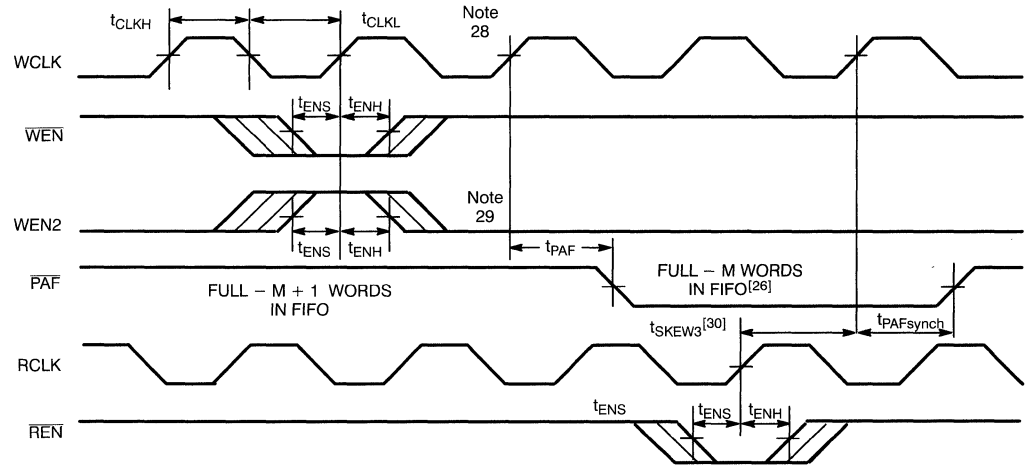


Notes:

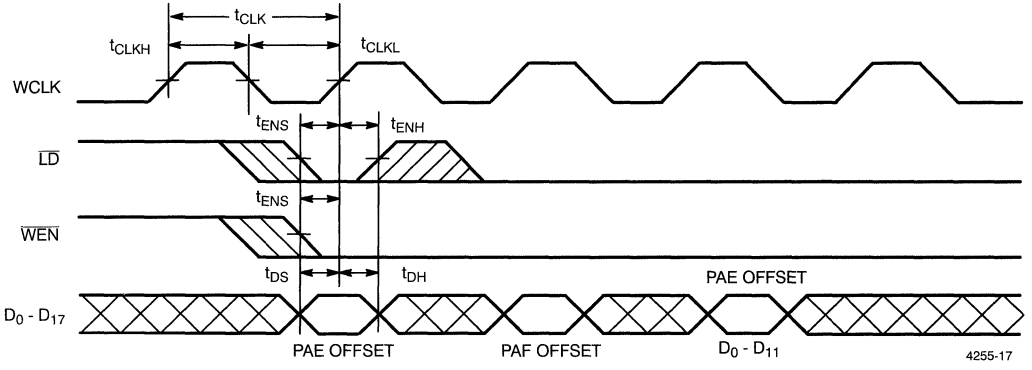
21. PAE offset – n.
22. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then $\overline{PAE}$ may not change state until the next RCLK.
23. If a read is preformed on this rising edge of the read clock, there will be Empty + (n−1) words in the FIFO when $\overline{PAE}$ goes LOW.
24. PAF offset = m. Number of data words written into FIFO already = 8192 – (m + 1) for the CY7C4255 and 16384 – (m + 1) for the CY7C4265.
25. PAF is offset = m.
26. 8192 – m words in CY7C4255 and 16384 – m words in CY7C4265.
27. 8192 – (m + 1) words in CY7C4255 and 16384 – (m + 1) CY7C4265.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))



Write Programmable Registers

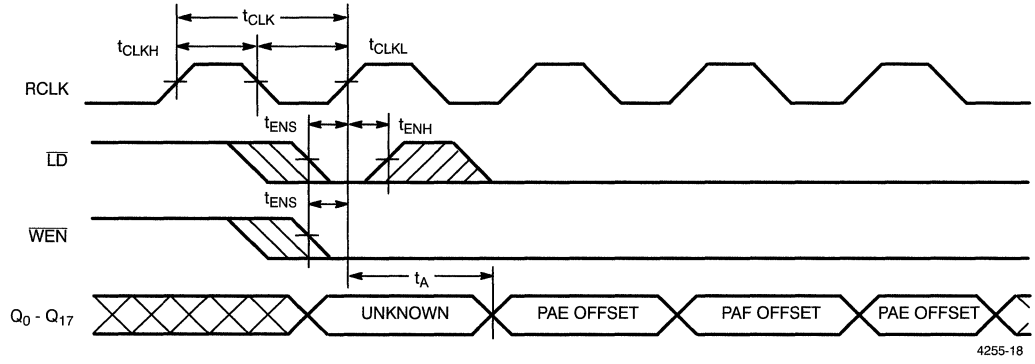


Notes:

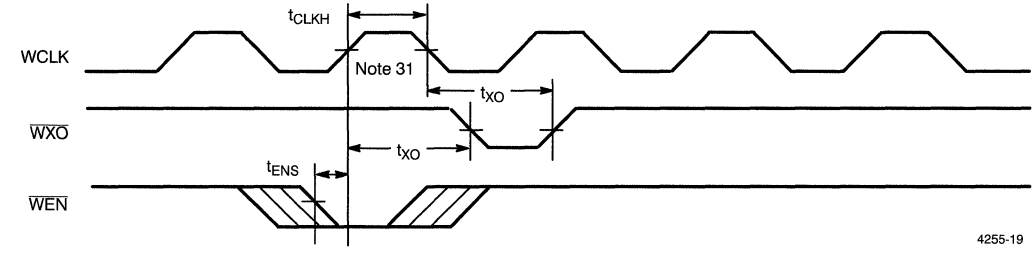
28. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
29. PAF offset = m.
30. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{PAF}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.

Switching Waveforms (continued)

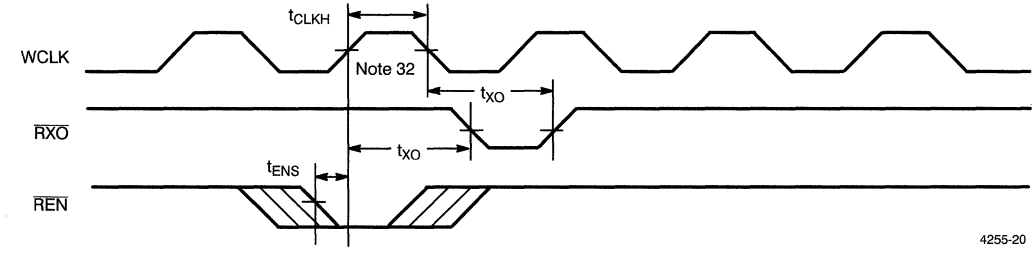
Read Programmable Registers



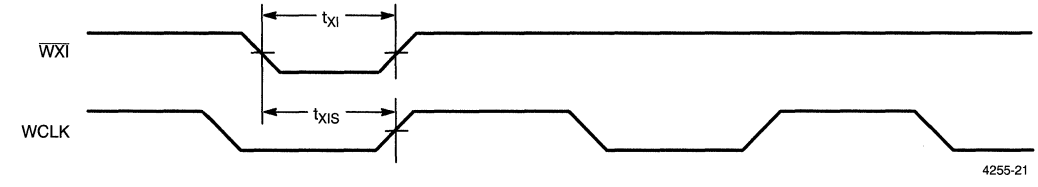
Write Expansion Out Timing



Read Expansion Out Timing



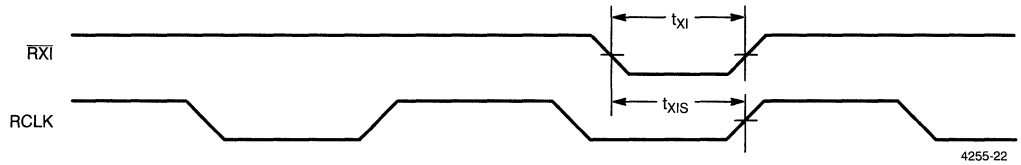
Write Expansion In Timing



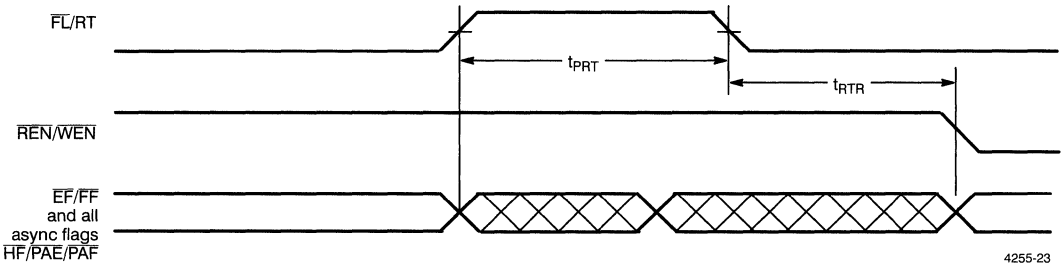
Notes:
31. Write to Last Physical Location.
32. Read from Last Physical Location.

Switching Waveforms (continued)

Read Expansion In Timing



Retransmit Timing[33, 34, 35]



Architecture

The CY7C4256/65 consists of an array of 8K/16K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, $\overline{FF}$). The CY7C4255/65 also includes the control signals $\overline{WXI}$, $\overline{RXI}$, $\overline{WXO}$, $\overline{RXO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is deasserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C4255/65 devices contain two 14-bit offset registers. Data present on D_{0-13} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see *Table 6*). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D_{0-13} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see *Table 5*). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Notes:

33. Clocks are free running in this case.
34. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
35. For the synchronous $\overline{PAE}$ and $\overline{PAF}$ flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Table 5. Write Offset Register

$\overline{LD}$	$\overline{WEN}$	WCLK[36]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C4255/65 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C4255/65 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 6* for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 6. Flag Truth Table

Number of Words in FIFO						
7C4255 – 8K x 18	7C4265 – 16K x 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to n[37]	1 to n[37]	H	H	H	L	H
(n+1) to 4096	(n+1) to 8192	H	H	H	H	H
4097 to (8192–(m+1))	8193 to (16384 –(m+1))	H	H	L	H	H
(8192–m)[38] to 8191	(16384–m)[38] to 16383	H	L	L	H	H
8192	16384	L	L	L	H	H

Notes:

36. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.
37. n = Empty Offset (Default Values: CY7C4255/CY7C4265 n = 127).
38. m = Full Offset (Default Values: CY7C4255/CY7C4265 n = 127).

Width Expansion Configuration

The CY7C4255/65 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO. This technique will avoid ready data from the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. *Figure 1* demonstrates a 36-word width by using two CY7C4255/65s.

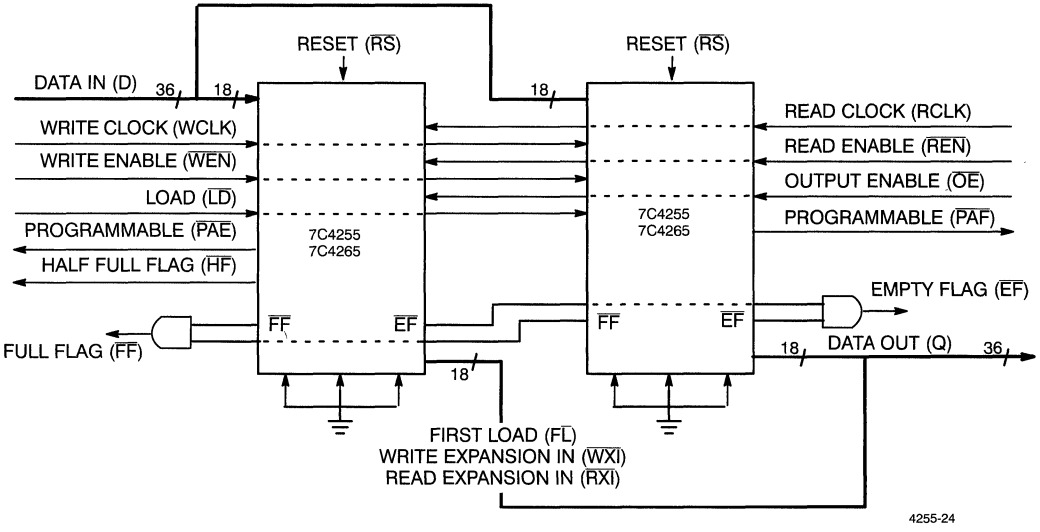


Figure 1. Block Diagram of 8K x 36/16K x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

The CY7C4255/65 can easily be adapted to applications requiring more than 8192/16384 words of buffering. *Figure 2* shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

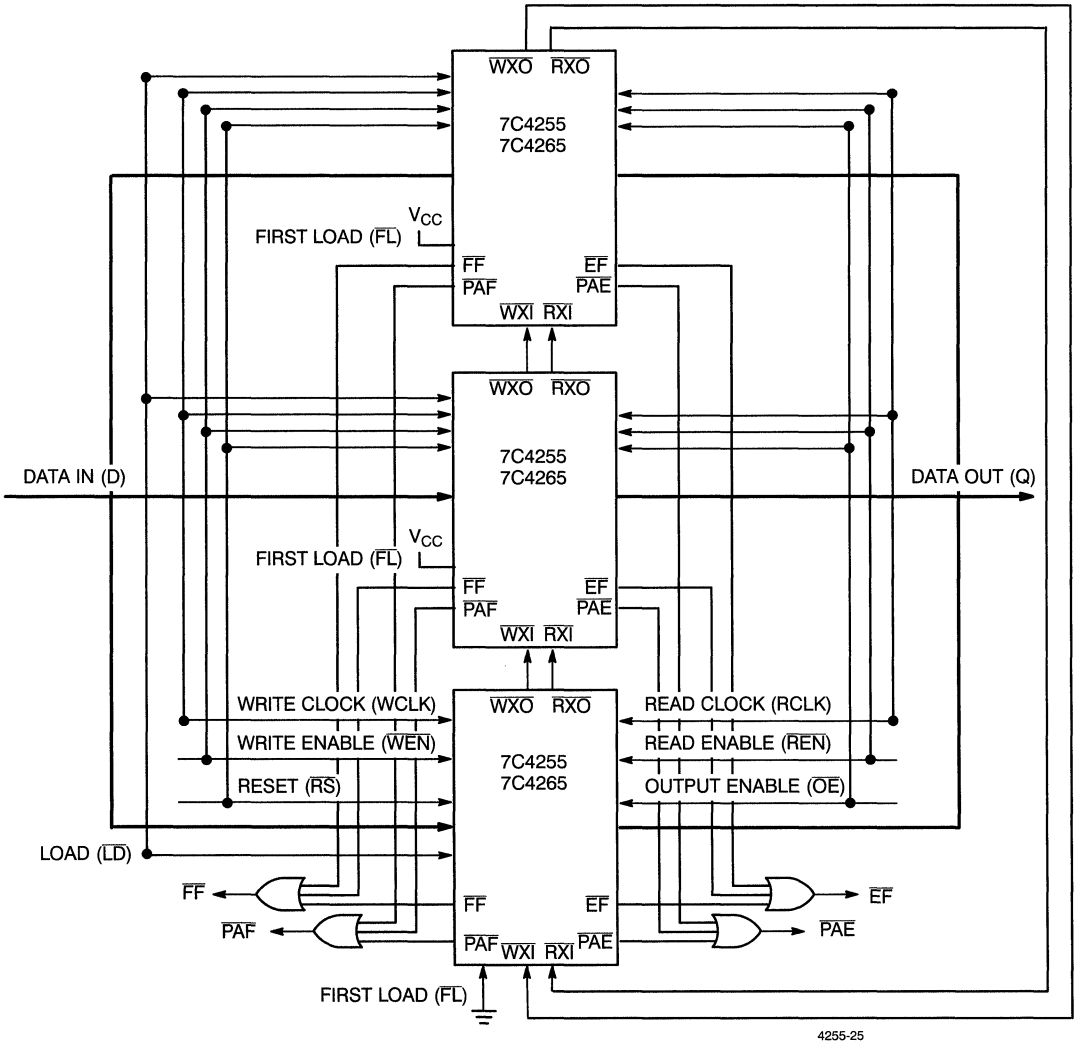


Figure 2. Block Diagram of 24576 x 18/49152 x 18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

Ordering Information

8K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4255–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4255–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4255–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4255–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

16K x 18

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4265–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4265–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4265–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4265–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Document #: 38–00468

PRELIMINARY

CY7C4261
CY7C4271

16K/32K x 9 Synchronous FIFOs

Features

- **16K x 9 (CY7C4261)**
- **32K x 9 (CY7C4271)**
- **High-speed 100-MHz operation (10 ns read/write cycle time)**
- **Pin-compatible density upgrade to CY7C42X1 family**
- **Pin-compatible density upgrade to IDT72201/11/21/31/41/51**
- **Fully asynchronous and simultaneous read and write operation**
- **Four status flags: Empty, Full, and programmable Almost Empty/Almost Full**
- **Expandable in width**
- **Low operating power**
  I_{CC1} = 100 mA
- **Output Enable ($\overline{OE}$) pin**
- **32-pin PLCC/TQFP**

Functional Description

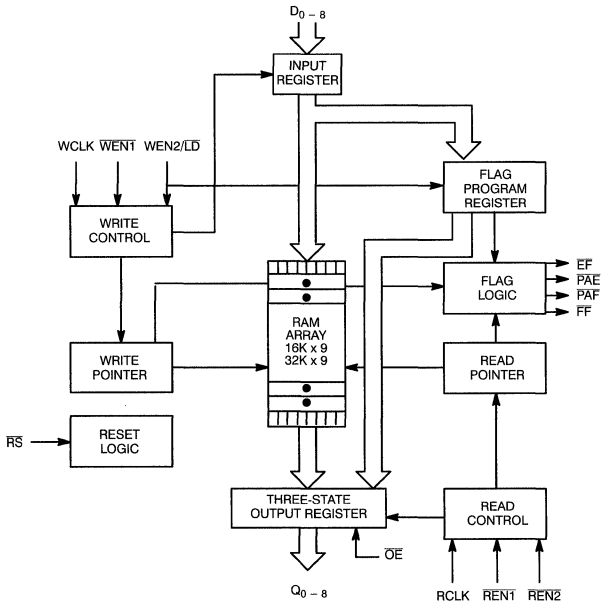
The CY7C4261/71 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 9 bits wide. The CY7C4261/71 are pin-compatible to the CY7C42X1 Synchronous FIFO family. The CY7C4261/71 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

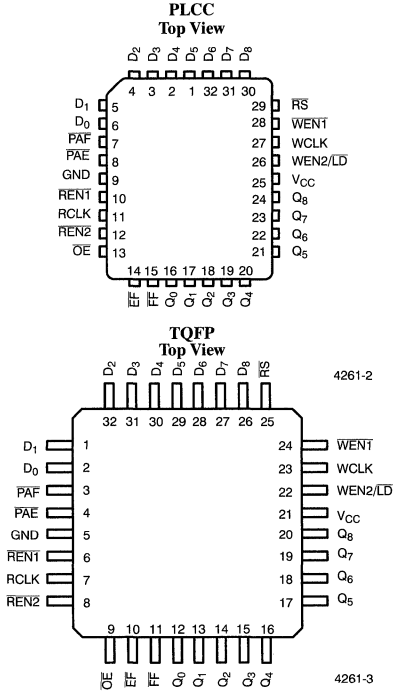
When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$, WEN2/$\overline{LD}$ is held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C42X1 has an output enable pin ($\overline{OE}$). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pin Configuration



Functional Description (continued)

The CY7C4261/71 provides four status pins: Empty, Full, Almost Empty, Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty-7 and Full-7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.65μ N-Well CMOS technology. Input ESD protection is greater than 4001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C4261/71–10	7C4261/71–15	7C4261/71–25	7C4261/71–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Active Power Supply Current (I_{CC1}) (mA)	Commercial	50	50	50	50
	Industrial	70	70	70	70

	CY7C4261	CY7C4271
Density	16K x 9	32K x 9

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	Data Inputs for 9-bit bus
Q_{0-8}	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or lead the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	Enables the device for Read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

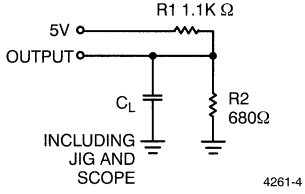
Electrical Characteristics Over the Operating Range[2]

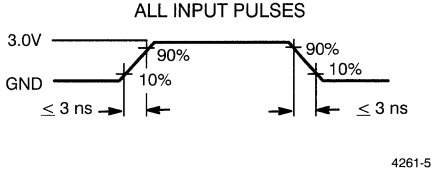
Parameter	Description	Test Conditions		7C42X1–10 Min.	7C42X1–10 Max.	7C42X1–15 Min.	7C42X1–15 Max.	7C42X1–25 Min.	7C42X1–25 Max.	7C42X1–35 Min.	7C42X1–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC1}[4]	Active Power Supply Current		Com'l		50		50		50		50	mA
			Ind		70		70		70		70	mA
I_{CCfMAX}[5]	Operating Current at Maximum Frequency		Com'l		150		130		75		60	mA
			Ind		170		150		95		80	mA
I_{CC2}[6]	Average Standby Current		Com'l		30		28		25		22	mA
			Ind		40		38		35		35	mA

Capacitance[7]

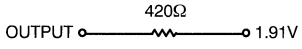
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms[8, 9]





Equivalent to: THÉVENIN EQUIVALENT



Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time for not more than one second.
4. Outputs open. Tested at frequency = 20 MHz.
5. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
6. All inputs = V_{CC} − 0.2V, except WCLK and RCLK (which are switching at frequency = 100 MHz). All outputs are unloaded.
7. Tested initially and after any design or process changes that may affect these parameters.
8. C_L = 30 pF for all AC parameters except for t_{OHZ}.
9. C_L = 5 pF for t_{OHZ}.

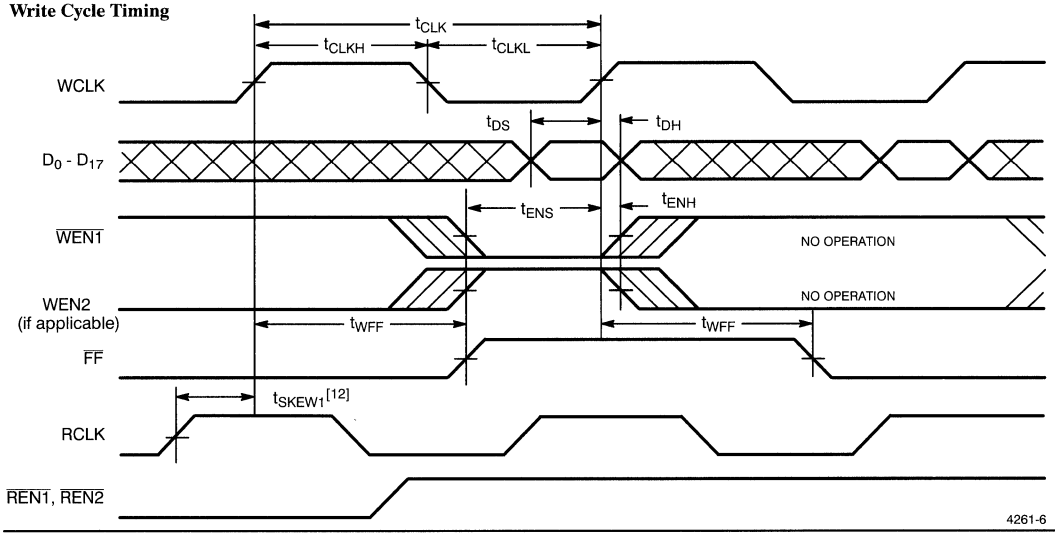
Switching Characteristics Over the Operating Range

Parameter	Description	7C42X1–10		7C42X1–15		7C42X1–25		7C42X1–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[10]	10		15		25		35		ns
t_{RSS}	Reset Set-Up Time	8		10		15		20		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{OLZ}	Output Enable to Output in Low Z[11]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[11]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15		20	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	10		15		18		20		ns

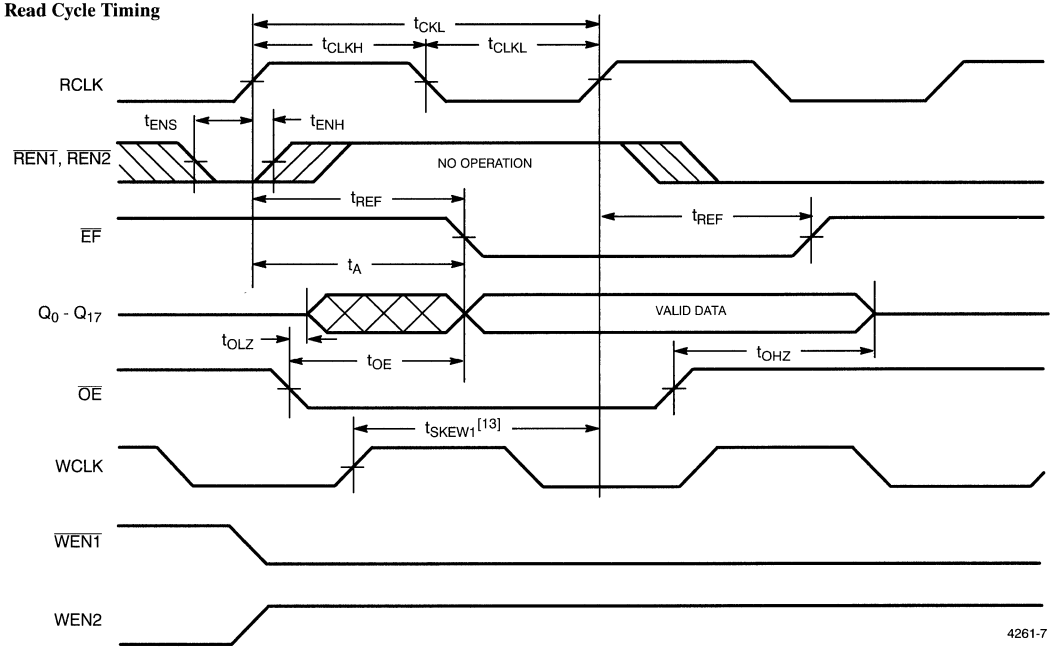
Notes:
10. Pulse widths less than minimum values are not allowed.
11. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

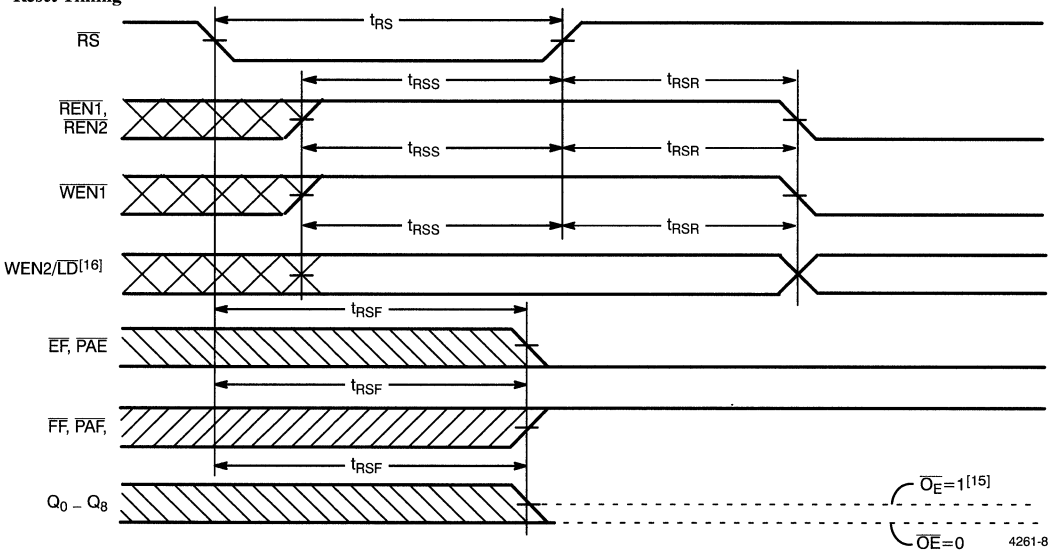


Notes:

12. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
13. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing[14]

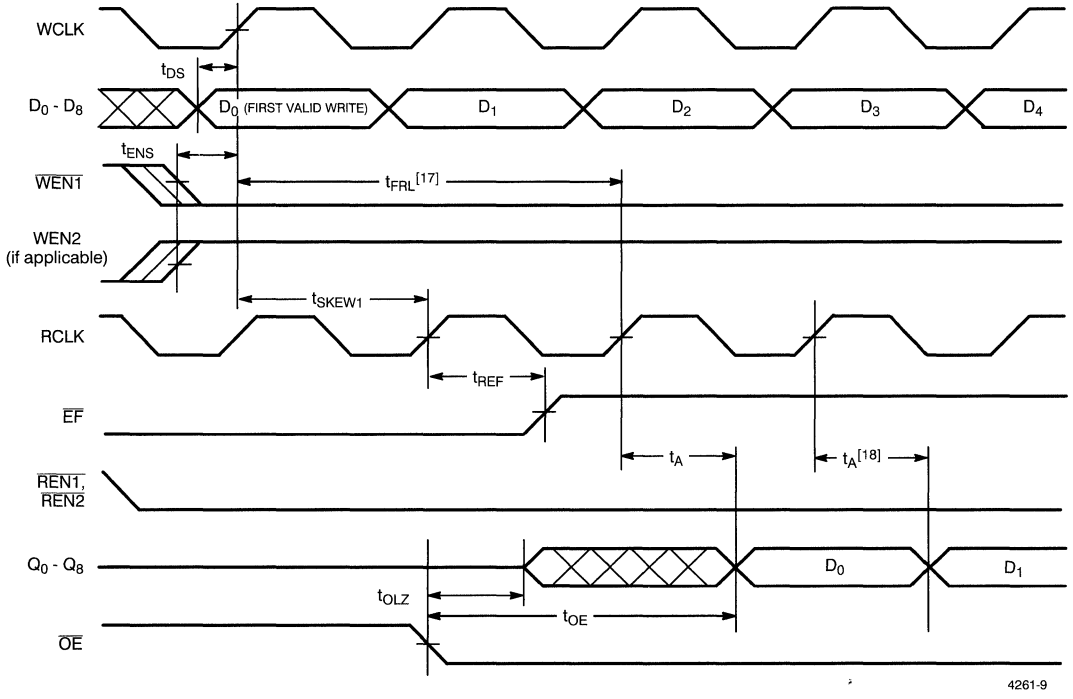


Notes:

14. The clocks (RCLK, WCLK) can be free-running during reset.
15. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
16. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)

First Data Word Latency after Reset with Simultaneous Read and Write

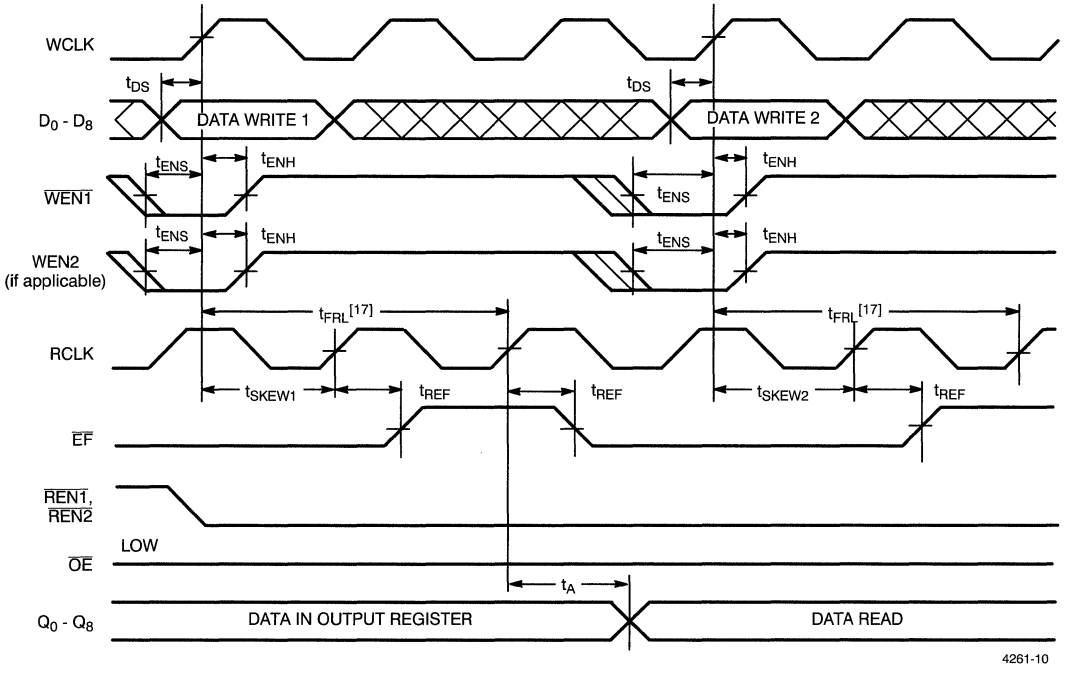


Notes:

17. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
18. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

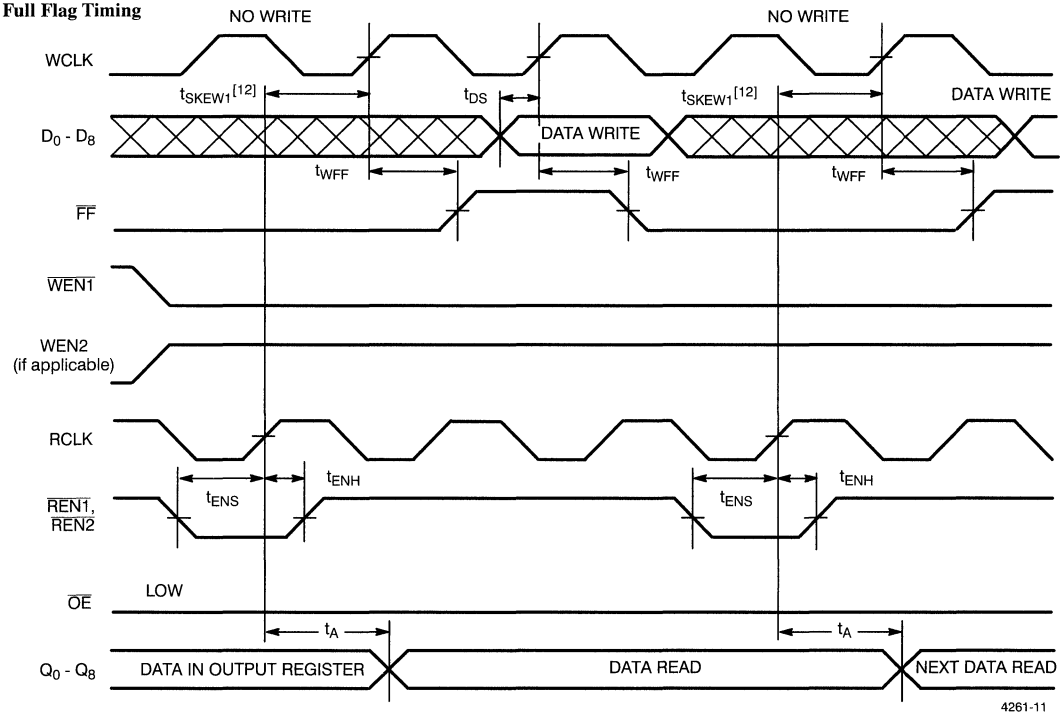
Switching Waveforms (continued)

Empty Flag Timing



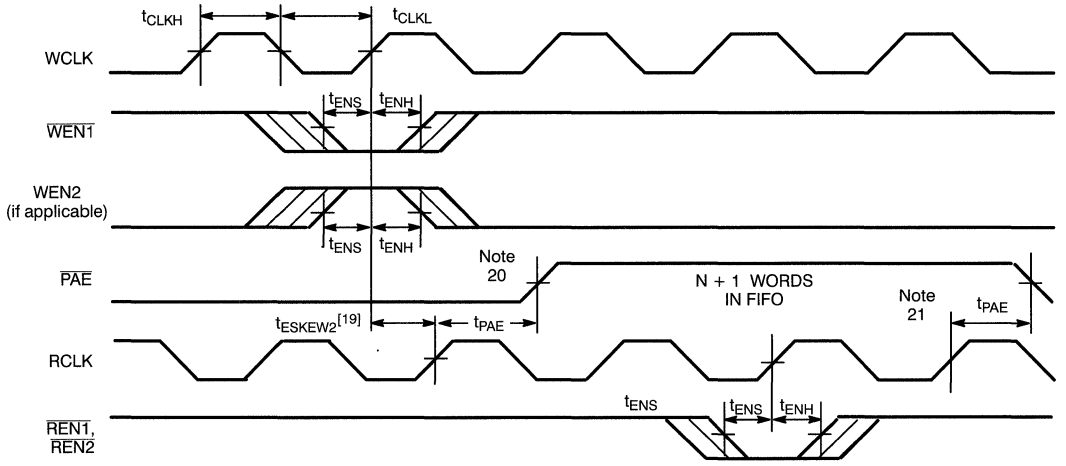
Switching Waveforms (continued)

Full Flag Timing

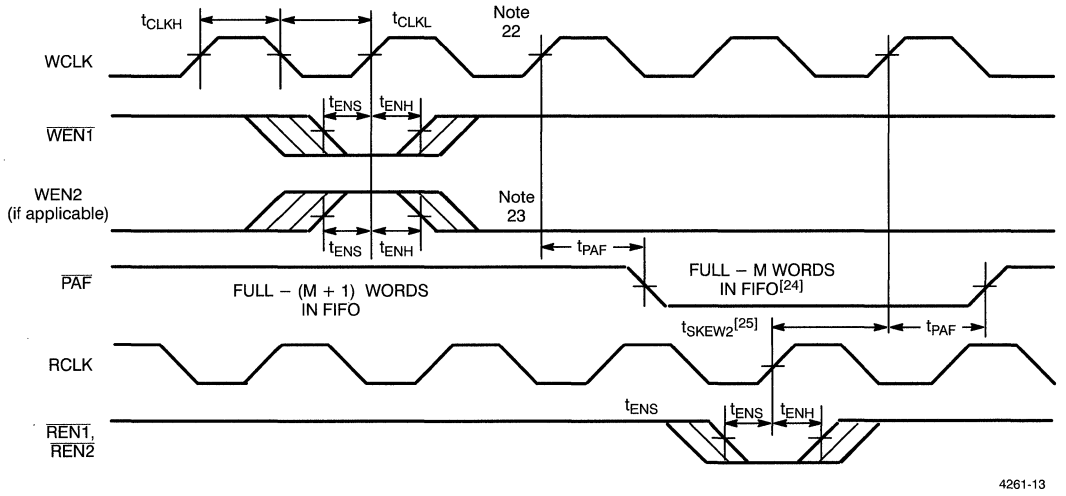


Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Full Flag Timing

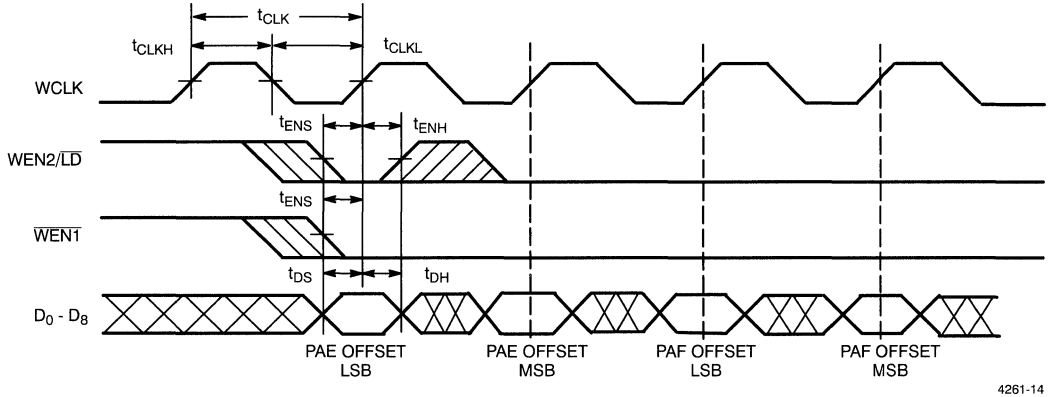


Notes:

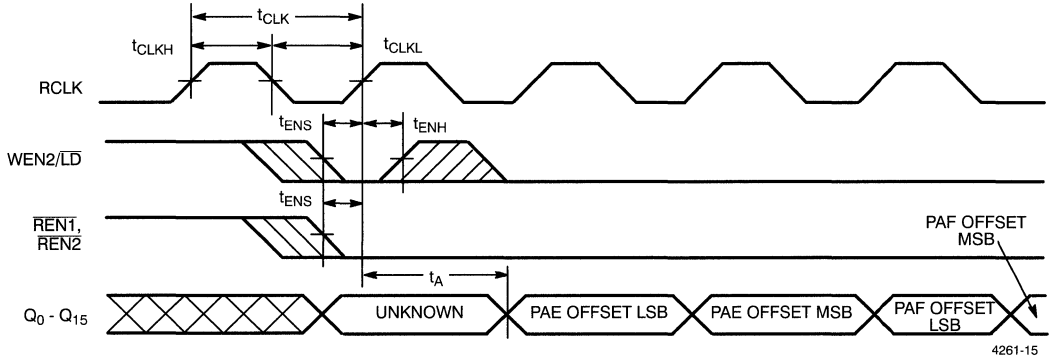
19. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
20. PAE offset – n.
21. If a read is preformed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
22. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
23. PAF offset = m.
24. 16,384 – m words for CY7C4261, 32,768 – m words for CY4271.
25. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

Write Programmable Registers



Read Programmable Registers



Architecture

The CY7C4261/71 consists of an array of 64 to 8K words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs (Q_{0-8}) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW and WEN2 is active HIGH, data present on the D_{0-8} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-8} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$) – If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data

is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$) – This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 8-bit offset registers contained in the CY7C42X1 for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

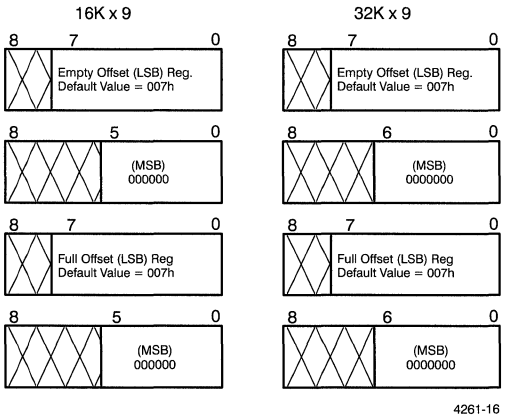


Figure 1. Offset Register Location and Default Values

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be preformed simultaneously on the offset registers.

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

Table 1. Writing the Offset Registers

$\overline{LD}$	$\overline{WEN}$	WCLK[26]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

The number formed by the empty offset least significant bit register and empty offset most significant register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4261 (16K–m) and CY7C4271 (32K–m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Note:
26. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK.

Table 2. Status Flags

Number of Words in FIFO					
CY7C4261	CY7C4271	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	L	L
1 to n[27]	1 to n[27]	H	H	L	H
(n+1) to 8192	(n+1) to 16384	H	H	H	H
8193 to (16384 – (m+1))	16385 to (32768 – (m+1))	H	H	H	H
(16384 – m)[28] to 16383	(32768 – m)[28] to 32767	H	L	H	H
16384	32768	L	L	H	H

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42X1s. Any word width can be attained by adding additional CY7C42X1s.

When the CY7C42X1 is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load ($\overline{WEN2/LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C4261/71 devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and $WEN2/\overline{LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

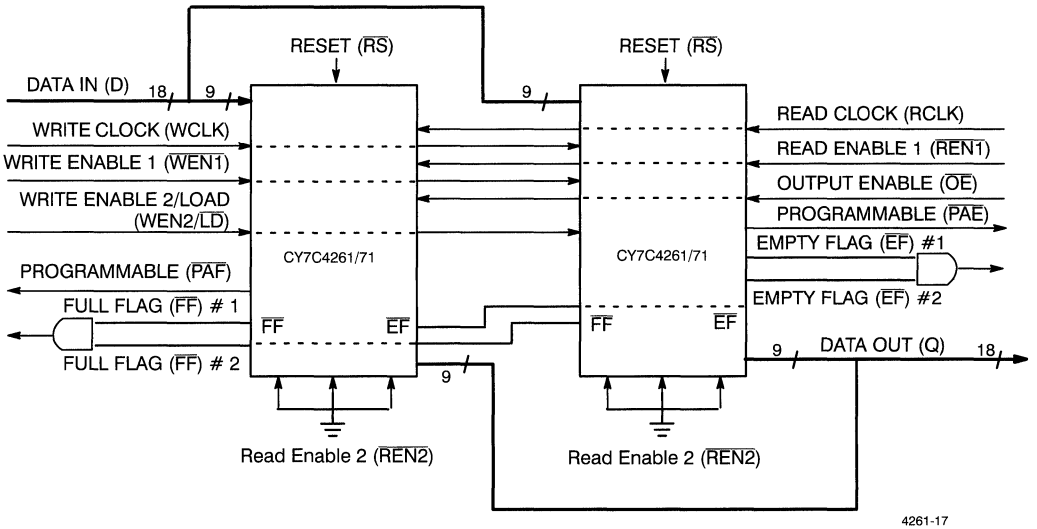


Figure 2. Block Diagram of 16K x 18/32K x 18 Synchronous FIFO Memory Used in a Width Expansion Configuration

Notes:
27. n = Empty Offset (n=7 default value).
28. m = Full Offset (m=7 default value).

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4261-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4261-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4261-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4261-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4261-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4261-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4261-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4261-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4261-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4261-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4261-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4261-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4261-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4261-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4261-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4261-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4271-10AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4271-10JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4271-10AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4271-10JI	J65	32-Lead Plastic Leaded Chip Carrier	
15	CY7C4271-15AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4271-15JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4271-15AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4271-15JI	J65	32-Lead Plastic Leaded Chip Carrier	
25	CY7C4271-25AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4271-25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4271-25AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4271-25JI	J65	32-Lead Plastic Leaded Chip Carrier	
35	CY7C4271-35AC	A32	32-Lead Thin Quad Flatpack	Commercial
	CY7C4271-35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C4271-35AI	A32	32-Lead Thin Quad Flatpack	Industrial
	CY7C4271-35JI	J65	32-Lead Plastic Leaded Chip Carrier	

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CY7C439

Bidirectional 2K x 9 FIFO

Features

- **2048 x 9 FIFO buffer memory**
- **Bidirectional operation**
- **High-speed 28.5-MHz asynchronous reads and writes**
- **Simple control interface**
- **Registered and transparent bypass modes**
- **Flags indicate Empty, Full, and Half Full conditions**
- **5V ± 10% supply**
- **Available in 300-mil DIP, PLCC, LCC, and SOJ packages**
- **TTL compatible**

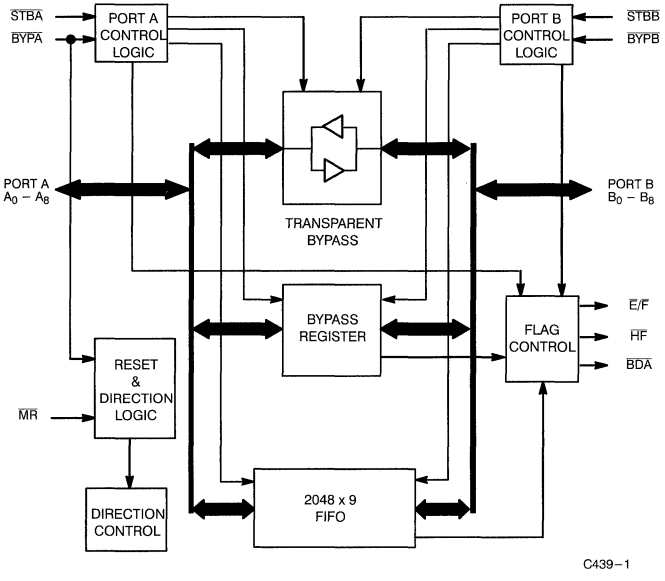
Functional Description

The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block—$\overline{E}/\overline{F}$ (Empty/Full) and $\overline{HF}$ (Half Full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin ($\overline{MR}$) and the bypass/direction pin ($\overline{BYPA}$). There are no control or status registers on the CY7C439, making the part simple to use while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 28.5 MHz. The port designated as the write port drives its strobe pin ($\overline{STBX}$, X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin ($\overline{BYPX}$, X = A or B) to remain HIGH.

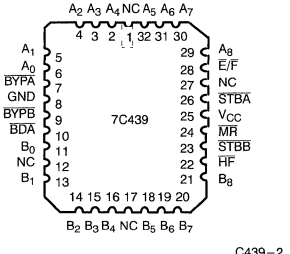
In addition to the FIFO, two other data paths are provided; registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The

Logic Block Diagram

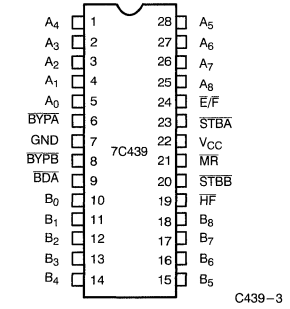


Pin Configurations

PLCC/LCC
Top View



DIP
Top View



Selection Guide

		7C439–25	7C439–30	7C439–40	7C439–65
Frequency (MHz)		28.5	25	20	12.5
Maximum Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	147	140	130	115
	Military		170	160	145

Functional Description (continued)

bypass register provides a means of sending a 9-bit status or control word to the FIFO-write port. The bypass data available pin ($\overline{BDA}$) indicates whether the bypass register is full or empty. The direction of the bypass register is always opposite to that of the main FIFO.

The port designated to write to the bypass register drives its bypass control pin ($\overline{BYPX}$) LOW. The other port detects the presence of data by monitoring $\overline{BDA}$ and reads the data by driving its bypass control pin ($\overline{BYPX}$) LOW. Registered bypass operations require that the associated FIFO strobe pin ($\overline{STBX}$) remains HIGH. Registered bypass operations do not affect data residing in the FIFO, or FIFO operations at the other port.

Transparent bypass provides a means of transferring a single word (9 bits) of data immediately in either direction. This feature allows the device to act as a simple 9-bit bidirectional buffer. This is useful for allowing the controlling circuitry to access a dumb peripheral for control/programming information.

For transparent bypass, the port wishing to send immediate data to the other side drives both its bypass and its strobe pins LOW simultaneously. This causes the buffered data to be driven out of the other port. On-chip circuitry detects conflicting use of the control pins and causes both data ports to enter a high-impedance state until the conflict is resolved.

Additionally, a Test mode is offered on the CY7C439. This mode allows the user to load data into the FIFO and then read it back out of the same port. Built-In Self Test (BIST) and diagnostic functions can take advantage of these features.

The CY7C439 is fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPA}$ and $\overline{STBA}$
$B_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPB}$ and $\overline{STBB}$
$\overline{BYPA}$	I	Registered Bypass Mode Select for A Side
$\overline{BYPB}$	I	Registered Bypass Mode Select for B Side
$\overline{BDA}$	O	Bypass Data Available Flag
$\overline{STBA}$	I	Data Strobe for A Side
$\overline{STBB}$	I	Data Strobe for B Side
$\overline{E}/\overline{F}$	O	Encoded Empty/Full Flag
$\overline{HF}$	O	Half Full Flag
$\overline{MR}$	I	Master Reset

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C439–25 Min.	7C439–25 Max.	7C439–30 Min.	7C439–30 Max.	7C439–40 Min.	7C439–40 Max.	7C439–65 Min.	7C439–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
			Mil			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{STBX}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		147		140		130		115	mA
			Mil[4]				170		160		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		40		40		40		40	mA
			Mil				45		45		45	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20		20		20		20	mA
			Mil				25		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90		−90	mA

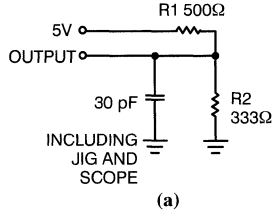
Capacitance[6]

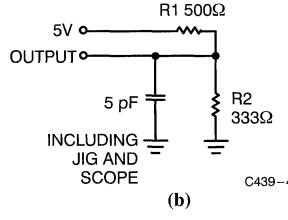
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

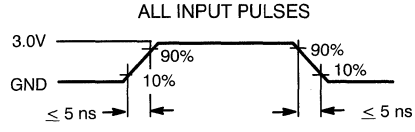
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 115 mA + [($\bar{f}$ − 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 145 mA + [($\bar{f}$ − 12.5) · 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveform



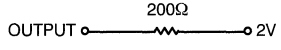


C439–4



C439–5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 7]

Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_A	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[8, 9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8, 9]	Data Valid from Read HIGH	3		3		3		3		ns
t_{HZR}[8, 9]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[8, 9]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPS}	$\overline{STBX}$ HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RPBS}	$\overline{BYPA}$ to $\overline{MR}$ HIGH	10		10		15		20		ns
t_{RPBH}	$\overline{BYPA}$ Hold after $\overline{MR}$ HIGH	0		0		0		0		ns
t_{BDH}	$\overline{MR}$ LOW to $\overline{BDA}$ HIGH		35		40		50		80	ns
t_{BSR}	$\overline{STBX}$ HIGH to $\overline{BYPA}$ LOW	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{BRS}	$\overline{BYPX}$ HIGH to $\overline{STBX}$ LOW	10		10		10		15		ns
t_{REF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Read)		25		30		35		60	ns
t_{RFF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Read)		25		30		35		60	ns
t_{WEF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Write)		25		30		35		60	ns
t_{WFF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Write)		25		30		35		60	ns
t_{BDA}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ LOW (Write)		25		30		35		60	ns
t_{BDB}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ HIGH (Read)		25		30		35		60	ns
t_{BA}	$\overline{BYPX}$ LOW to Data Valid (Read)		30		30		40		60	ns
t_{BHZ}[8, 9]	$\overline{BYPX}$ HIGH to High Z (Read)		18		20		25		30	ns
t_{TSB}	$\overline{STBX}$ HIGH to $\overline{BYPX}$ LOW Set-Up	10		10		10		15		ns
t_{TBS}	$\overline{STBX}$ LOW after $\overline{BYPX}$ LOW	0	10	0	10	0	10	0	10	ns
t_{TSN}	$\overline{STBX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TSD}[8, 9]	$\overline{STBX}$ HIGH to Data High Z		18		20		25		30	ns
t_{TBN}	$\overline{BYPX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TBD}	$\overline{BYPX}$ HIGH to Data High Z		18		20		25		30	ns

Switching Characteristics Over the Operating Range[2, 7] (continued)

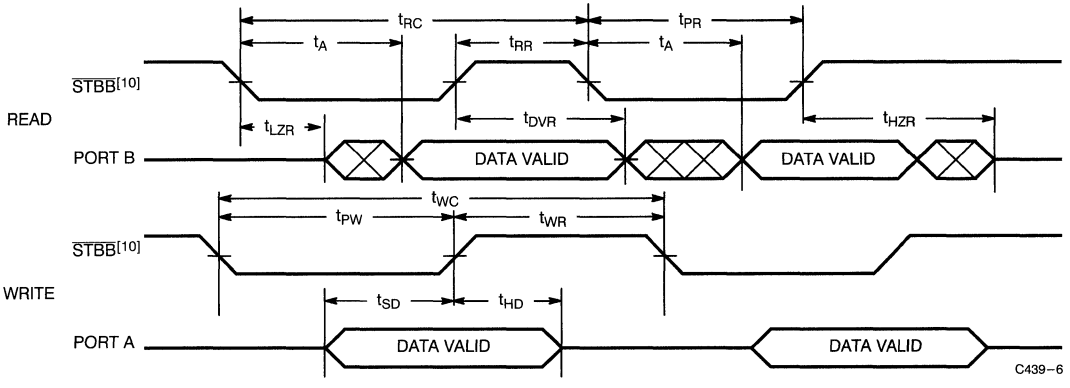
Parameter	Description	7C439–25		7C439–30		7C439–40		7C439–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{TPD}[8, 9]	$\overline{STBX}$ LOW to Data Valid		20		20		30		55	ns
t_{DL}	Transparent Propagation Delay		20		20		25		30	ns
t_{ESD}[8, 9]	$\overline{STBX}$ LOW to High Z		18		20		25		30	ns
t_{EBD}[8, 9]	$\overline{BYPX}$ LOW to High Z		18		20		25		30	ns
t_{EDS}	$\overline{STBX}$ HIGH to Low Z		18		20		25		30	ns
t_{EDB}	$\overline{BYPX}$ HIGH to Low Z		18		20		25		30	ns
t_{BPW}	$\overline{BYPX}$ Pulse Width (Trans.)	25		30		40		65		ns
t_{TSP}	$\overline{STBX}$ Pulse Width (Trans.)	20		20		30		55		ns
t_{BLZ}[8, 9]	$\overline{BYPX}$ LOW to Low Z (Read)	10		10		10		10		ns
t_{BDV}	$\overline{BYPX}$ HIGH to Data Invalid (Read)	3		3		3		3		ns
t_{WHF}	$\overline{STBX}$ LOW to $\overline{HF}$ LOW (Write)		35		40		50		80	ns
t_{RHF}	$\overline{STBX}$ HIGH to $\overline{HF}$ HIGH (Read)		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	15		18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		0		10		ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance as in part (a) of AC Test Loads, unless otherwise specified.
8. t_{DVR}, t_{BDV}, t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, t_{TSD}, t_{LZR}, t_{HWZ}, and t_{BLZ} use capacitance loading as in part (b) of AC Test Loads.
9. t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, and t_{TSD} transition is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}. t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR}, t_{HWZ}, and t_{BLZ} transition is measured at ±100 mV from the steady state.

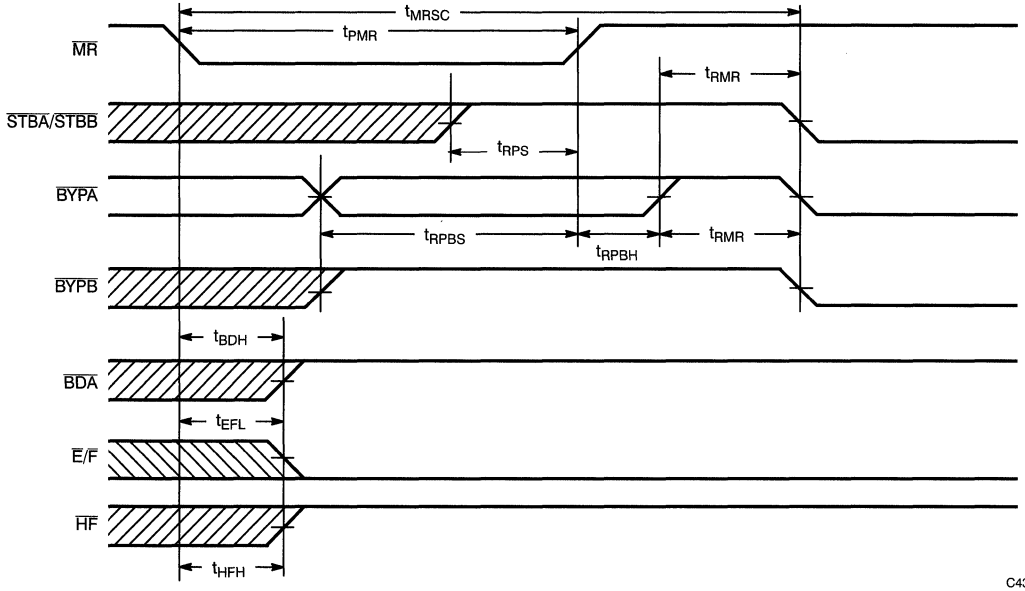
Switching Waveforms

Asynchronous Read and Write Timing Diagram

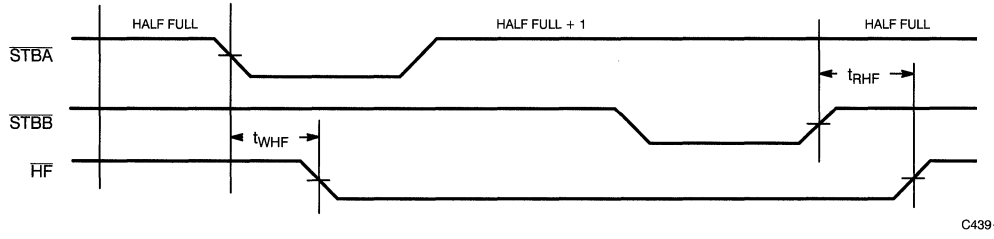


Switching Waveforms (continued)

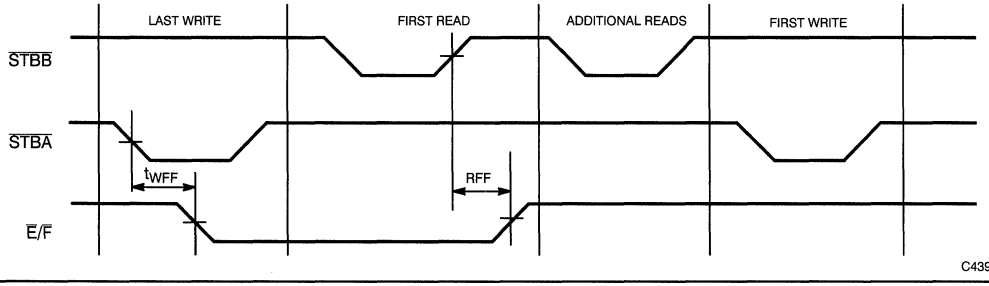
Master Reset Timing Diagram



Half-Full Flag Timing Diagram[11]



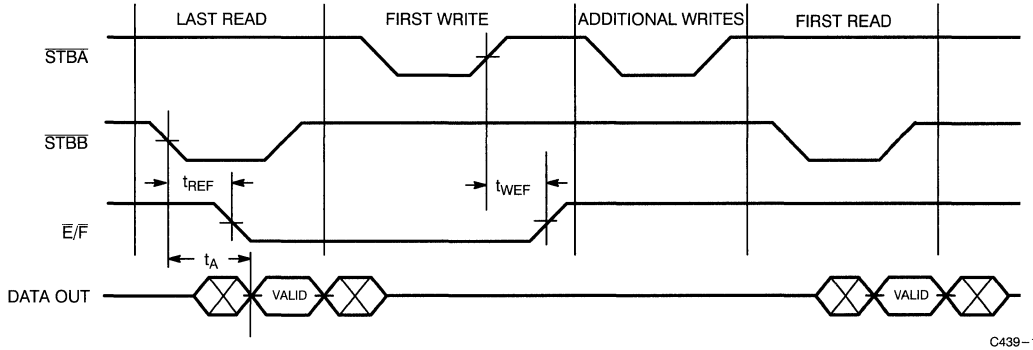
Last Write to First Read Empty/Full Flag Timing Diagram[11]



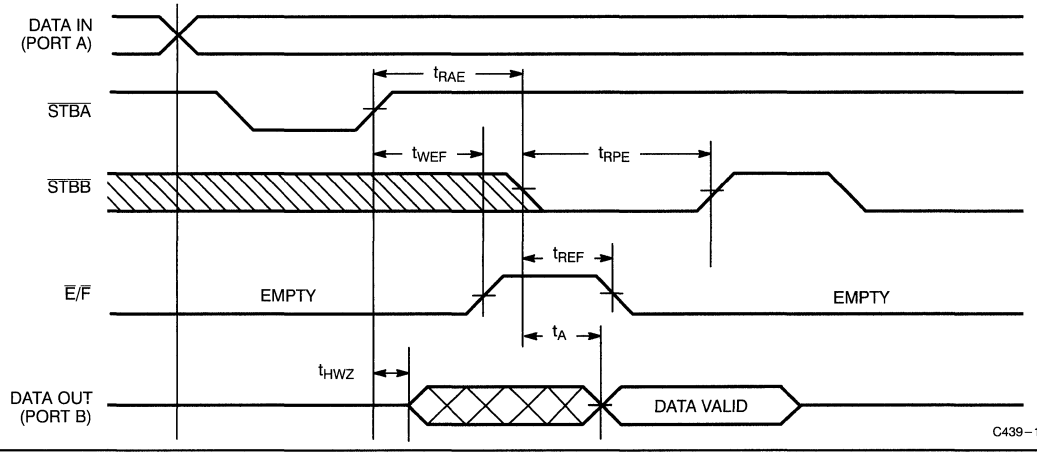
Notes:
10. Direction selected Port A to Port B.
11. Direction selected as A to B.

Switching Waveforms (continued)

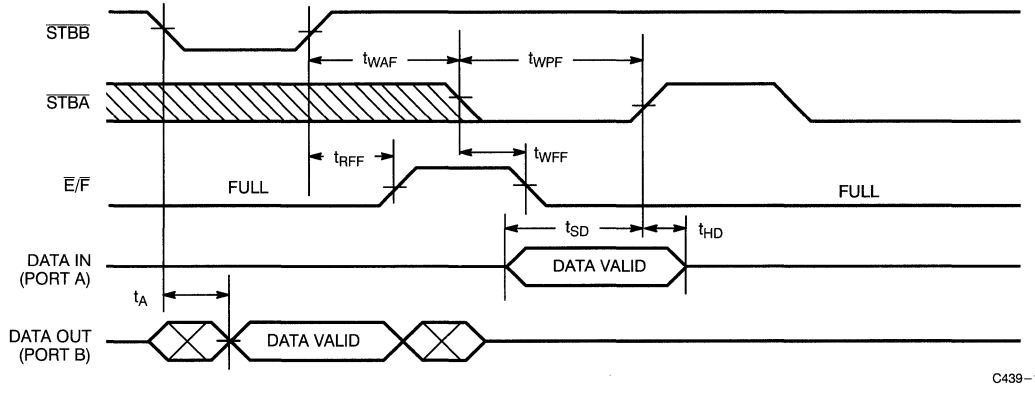
Last Read to First Write Empty/Full Flag Timing Diagram[11]



Empty/Full Flag and Read Bubble-Through Mode Timing Diagram[11]

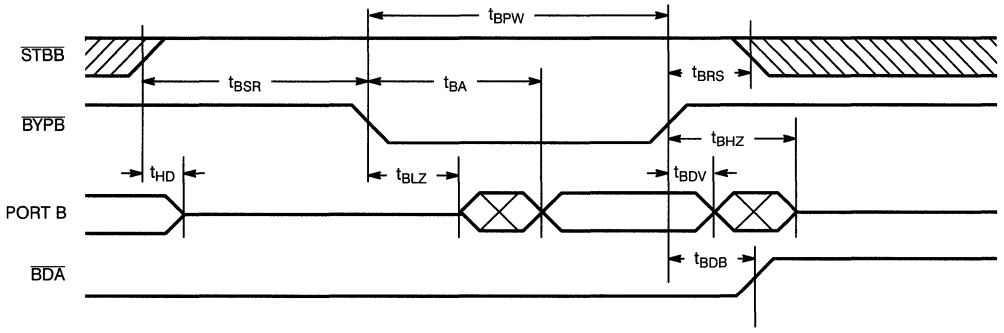


Empty/Full Flag and Write Bubble-Through Mode Timing Diagram[11]



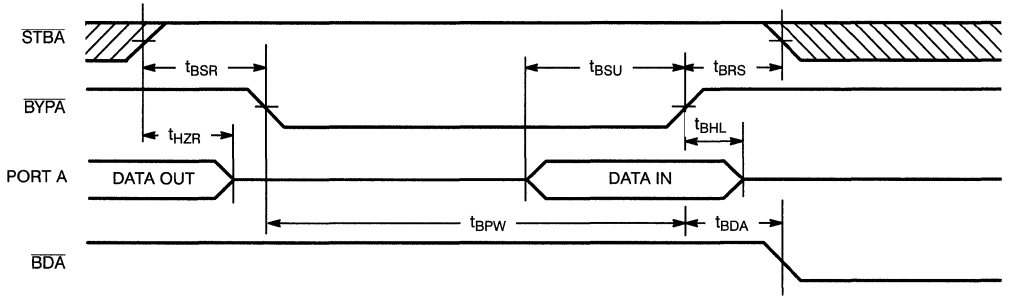
Switching Waveforms (continued)

Registered Bypass Read Timing Diagram[12]



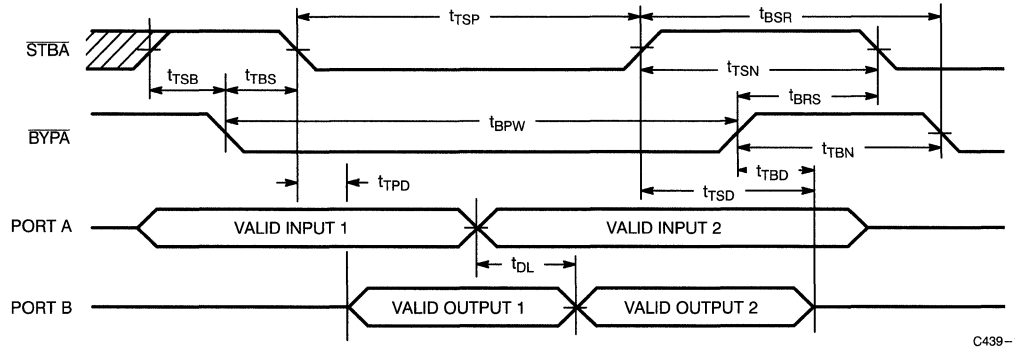
C439–13

Registered Bypass Write Timing Diagram[13]



C439–14

Transparent Bypass Read Timing Diagram[14]



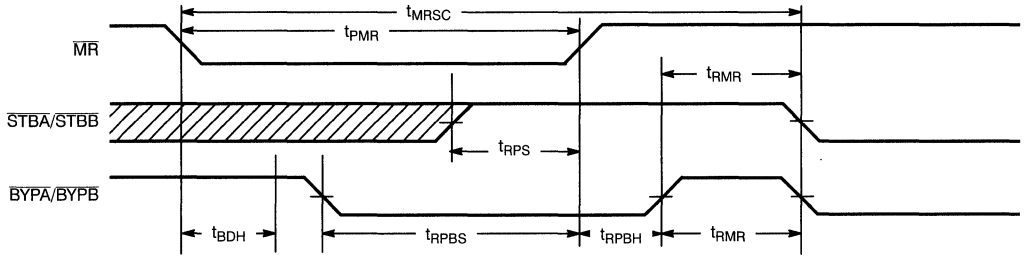
C439–15

Notes:

12. Port B selected to read bypass register (FIFO direction Port B to Port A).
13. Port A selected to write bypass register (FIFO direction Port B to Port A.
14. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

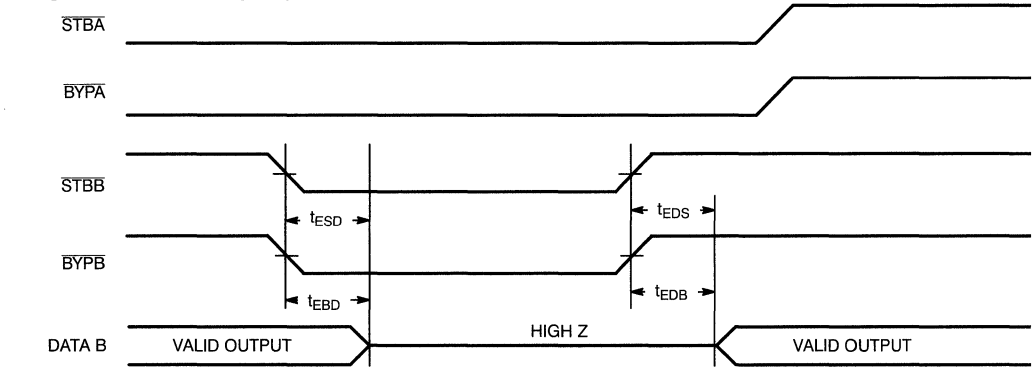
Switching Waveforms (continued)

Test Mode Timing Diagram



C439-16

Exception Condition Timing Diagram[14]



C439-17

Architecture

The CY7C439 consists of a 2048 by 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals ($\overline{STBA}$, $\overline{STBB}$, $\overline{BYPA}$, $\overline{BYPB}$, $\overline{MR}$), and flags ($\overline{E}/\overline{F}$, $\overline{HF}$, $\overline{BDA}$).

Operation at Power-On

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. During an $\overline{MR}$ cycle, the user can initialize the device by choosing the direction of FIFO operation (see *Table 1*). There is a minimum LOW period for $\overline{MR}$, but no maximum time. The state of $\overline{BYPA}$ is latched internally by the rising edge of $\overline{MR}$ and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the reset condition (see *Table 1*), the FIFO three-states the data ports, sets $\overline{BDA}$ and $\overline{HF}$ HIGH, $\overline{E}/\overline{F}$ LOW, and ignores the state of $\overline{BYPA}/\overline{B}$ and $\overline{STBA}/\overline{B}$. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving $\overline{BYPA}$ HIGH or LOW, and $\overline{BYPB}$, $\overline{STBA}$, and $\overline{STBB}$ HIGH. If $\overline{BYPA}$ is LOW (selecting direction B>A), the FIFO will then remain in a reset condition until the user terminates the reset operation by driving $\overline{BYPA}$ HIGH. If $\overline{BYPA}$ is HIGH (selecting direction A>B), the reset condition terminates after the rising edge of $\overline{MR}$. The entire reset phase can be accomplished in one cycle time of t_{RC}.

FIFO Operation

The operation of the FIFO requires only one control pin per port ($\overline{STBX}$). The user determines the direction of the FIFO data flow by initiating an $\overline{MR}$ cycle (see *Table 1*), which clears the FIFO and bypass register and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another $\overline{MR}$ cycle. Data is written into the FIFO on the rising edge of the input, $\overline{STBX}$, and read from the FIFO by a low level at the output, $\overline{STBX}$. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a bubble-through read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter if the read strobe ($\overline{STBX}$) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at which time the bubble-through write is performed if the write strobe ($\overline{STBX}$) is still LOW.

Registered Bypass Operation

The registered bypass feature provides a means of transferring one 9-bit word of data in the opposite direction to normal data flow without affecting either the FIFO contents or the FIFO write operations at the other port. The bypass register is configured during reset to provide a data path in the opposite direction to that of the FIFO (see *Table 1*). For example, if port A is writing data to the FIFO (hence port B is reading data from the FIFO) then $\overline{BYPB}$ is used to write to the bypass register at port B, and $\overline{BYPA}$ is used to read a single word from the bypass register at port A. The bypass data available flag ($\overline{BDA}$) is generated to notify port A that bypass data is available. $\overline{BDA}$ goes true on the trailing edge of the $\overline{BYPX}$ write operation and false upon the trailing edge of the $\overline{BYPX}$ read operation.

Data is written on the rising edge of $\overline{BYPX}$ into the bypass register for later retrieval by the other port, regardless of the state of $\overline{BDA}$. The bypass register is read by a low level at $\overline{BYPX}$, regardless of the state of $\overline{BDA}$.

Transparent Bypass Operation

The transparent bypass feature provides a means of sending immediate data "around" the FIFO in either direction. The FIFO contents are not affected by the use of transparent bypass, but the control signals for transparent bypass are shared with those of the normal FIFO operation. Hence there are limitations on the use of transparent bypass to ensure that data integrity and ease of use are preserved. The port wishing to send immediate data must ensure that the other port will not attempt a FIFO read or write during the transparent bypass cycle. If this is not possible, registered bypass or external circuitry should be used.

Transparent bypass mode is initiated by bringing both $\overline{BYPA}$ and $\overline{STBA}$ LOW together. Care should be taken to observe the following constraints on the timing relationships. Since $\overline{STBA}$ is used for normal FIFO operations, it must follow $\overline{BYPA}$ falling edge by t_{TBS} to prevent erroneous FIFO read or write operations. Since $\overline{BYPA}$ is used alone to initiate registered bypass read and write, it is internally delayed before initiating registered bypass. If $\overline{STBA}$ falls during this time, delay registered bypass is averted, and transparent bypass is initiated. Identical arguments apply to $\overline{BYPB}$ and $\overline{STBB}$.

If a transparent bypass sequence is successfully accomplished, data presented to the initiating port (port A in the above discussion) will be buffered to the other (port B) after t_{DL}. Either port can initiate a transparent bypass operation at any time, but if the control signals ($\overline{STBA}$/B, $\overline{BYPA}$/B) are in conflict (exception condition), internal circuitry will switch both ports to high-impedance until the conflict is resolved.

Test Mode Operation

The Test mode feature provides a means of reading the FIFO contents from the same port that the data was written to the FIFO. This feature is useful for Built-In Self Test (BIST) and diagnostic functions. To utilize this capability, initialize FIFO direction A to B and load data into the FIFO using normal write timing. In order to read data back out of the same port (port A), initiate a $\overline{MR}$ cycle with both $\overline{BYPA}$ and $\overline{BYPB}$ LOW (see Test Mode Timing diagram). After completing the cycle, the data can be read out of port A in FIFO order. Data will be inverted when read out of the device. Also, flags are not valid when reading data.

Flag Operation

There are two flags, Empty/Full ($\overline{E}/\overline{F}$) and Half Full ($\overline{HF}$), which are used to decode four FIFO states (see *Table 4*). The states are empty, 1–1024 locations full, 1025–2047 locations full, and full. Note that two conditions cause the $\overline{E}/\overline{F}$ pin to go LOW, Empty and Full, hence both flag pins must be used to resolve the two conditions.

Table 1. FIFO Direction Select Truth Table

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal Operation
⌐¬	1	1	1	1	FIFO Direction A to B, Registered Bypass Direction B to A
⌐¬	0	1	1	1	FIFO Direction B to A, Registered Bypass Direction A to B
0	X	X	X	X	Reset Condition

Table 2. Bypass Operation Truth Table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A⇾B	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at A, Read at B
A⇾B	1	⌐¬	⌐¬	1	Normal FIFO Read at B, Bypass Register Read at A
A⇾B	⌐¬	1	1	⌐¬	Normal FIFO Write at A, Bypass Register Write at B
B⇾A	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at B, Read at A
B⇾A	1	⌐¬	⌐¬	1	Normal FIFO Write at B, Bypass Register Write at A
B⇾A	⌐¬	1	1	⌐¬	Normal FIFO Read at A, Bypass Register Read at B
X	0	0	1	1	No FIFO Operations, Transparent Data A to B
X	1	1	0	0	No FIFO Operations, Transparent Data B to A

Table 3. Exception Conditions: Operation Not Defined

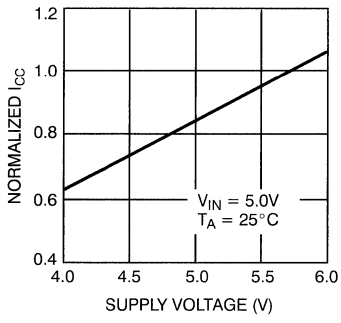
Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYBP}$	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

Table 4. Flag Truth Table

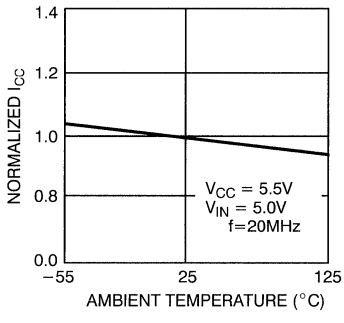
$\overline{E}/\overline{F}$	$\overline{HF}$	State
0	1	Empty
1	1	1–1024 Locations Full
1	0	1025–2047 Locations Full
0	0	Full

Typical DC and AC Characteristics

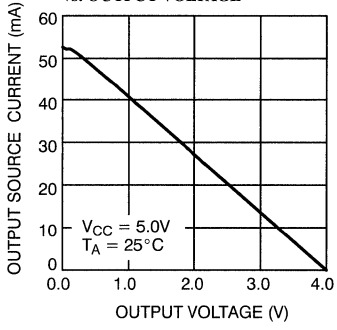
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



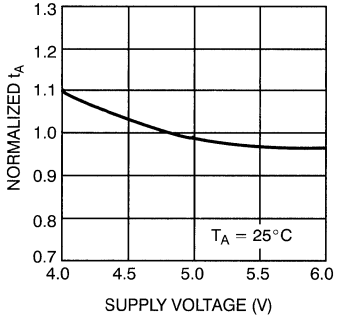
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



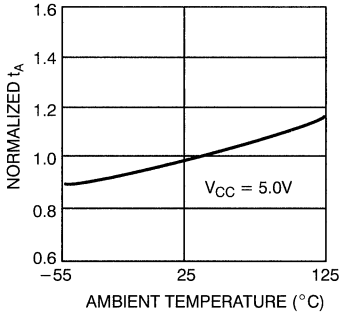
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



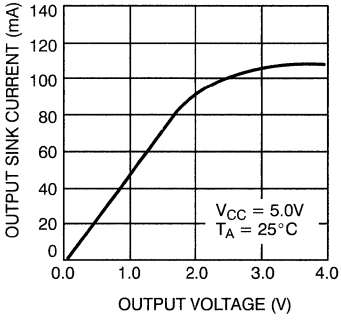
NORMALIZED t_A vs. SUPPLY VOLTAGE



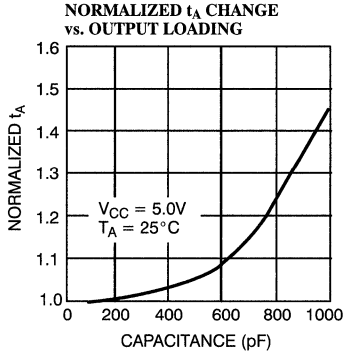
NORMALIZED t_A vs. AMBIENT TEMPERATURE

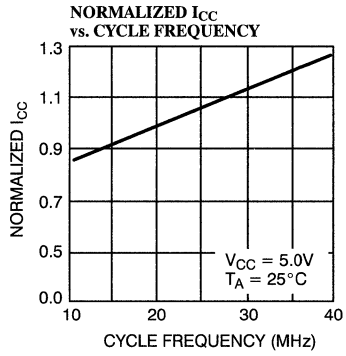


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)





Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C439–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–25PC	P21	28-Lead (300-Mil) Molded DIP	
30	CY7C439–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C439–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C439–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPS}	9, 10, 11
t_{RPBS}	9, 10, 11
t_{RPBH}	9, 10, 11
t_{BDH}	9, 10, 11
t_{BSR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{BRS}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{BSU}	9, 10, 11
t_{BHL}	9, 10, 11
t_{BDA}	9, 10, 11
t_{BDB}	9, 10, 11
t_{BA}	9, 10, 11
t_{BHZ}	9, 10, 11
t_{TSB}	9, 10, 11
t_{TBS}	9, 10, 11
t_{TSN}	9, 10, 11
t_{TSD}	9, 10, 11
t_{TBN}	9, 10, 11
t_{TBD}	9, 10, 11
t_{TPD}	9, 10, 11
t_{DL}	9, 10, 11
t_{ESD}	9, 10, 11
t_{EBD}	9, 10, 11
t_{EDS}	9, 10, 11
t_{EDB}	9, 10, 11
t_{BPW}	9, 10, 11
t_{TSP}	9, 10, 11
t_{BLZ}	9, 10, 11
t_{BDV}	9, 10, 11

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CY7C441
CY7C443

Clocked 512 x 9, 2K x 9 FIFOs

Features

- **512 x 9 (CY7C441) and 2,048 x 9 (CY7C443) FIFO buffer memory**
- **High-speed 70-MHz operation**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, and Almost Full status flags**
- **Fully asynchronous and simultaneous read and write operation**
- **Width expandable**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 28-pin DIP, PLCC, LCC, and SOJ packages**
- **Proprietary 0.8µ CMOS technology**
- **TTL compatible**
- **Low power – I_{CC}=70 mA**

Functional Description

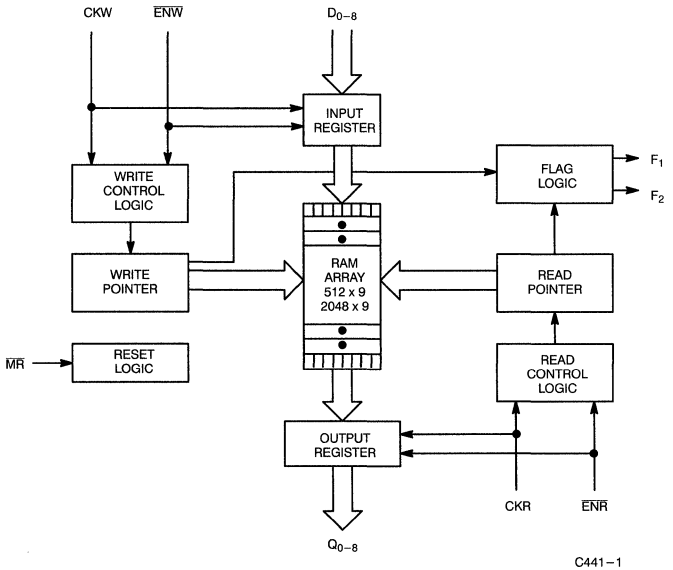
The CY7C441 and CY7C443 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C441 has a 512 word by 9 bit memory array, while the CY7C443 has a 2048 word by 9 bit memory array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable.

The CY7C441 and CY7C443 clocked FIFOs provide two status flag pins (F1 and F2). These flags are decoded to determine one of four states: Empty, Almost Empty, Intermediate, and Almost Full (*Table 1*). The flags are synchronous; i.e., change state relative to either the read clock (CKR) or the write clock (CKW). The Empty and Almost Empty states are updated exclusively by the CKR while Almost Full is updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C441 and the CY7C443 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8µ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

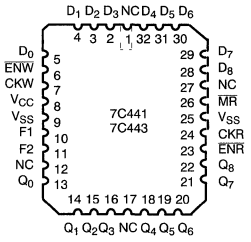
Logic Block Diagram



C441–1

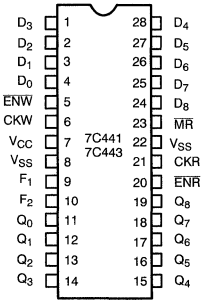
Pin Configurations

PLCC/LCC
Top View



C441–2

DIP/SOJ
Top View



C441–3

Selection Guide

		7C441–14 7C443–14	7C441–20 7C443–20	7C441–30 7C443–30
Maximum Frequency (MHz)		71.4	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: when the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_0 – D_8) into the FIFO's memory
Q_{0-8}	O	Data Outputs: when the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_0 – Q_8) out of the FIFO's memory
$\overline{ENW}$	I	Enable Write: enables the CKW input
$\overline{ENR}$	I	Enable Read: enables the CKR input
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW and updates the Almost Full flag state
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW and updates the Almost Empty and Empty flag states
F1	O	Flag 1: is used in conjunction with Flag 2 to decode which state the FIFO is in (see *Table 1*)
F2	O	Flag 2: is used in conjunction with Flag 1 to decode which state the FIFO is in (see *Table 1*)
$\overline{MR}$	I	Master Reset: resets the device to an empty condition

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

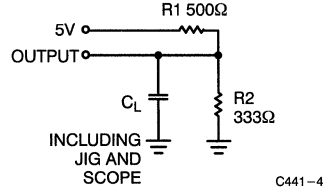
Parameter	Description	Test Conditions		7C441–14 7C443–14 Min.	7C441–14 7C443–14 Max.	7C441–20 7C443–20 Min.	7C441–20 7C443–20 Max.	7C441–30 7C443–30 Min.	7C441–30 7C443–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	– 10	+10	μA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		– 90		– 90		– 90		mA
I_{CC1}[4]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[5]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[6]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

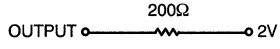
Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. Test no more than one output at a time and do not test any output for more than one second.
4. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
5. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
6. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
7. Tested initially and after any design or process changes that may affect these parameters.

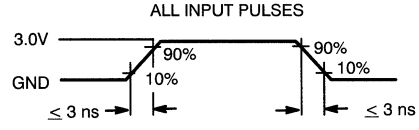
AC Test Loads and Waveform[8,9]



C441–4

Equivalent to: THÉVENIN EQUIVALENT





C441–5

Switching Characteristics Over the Operating Range[2,10]

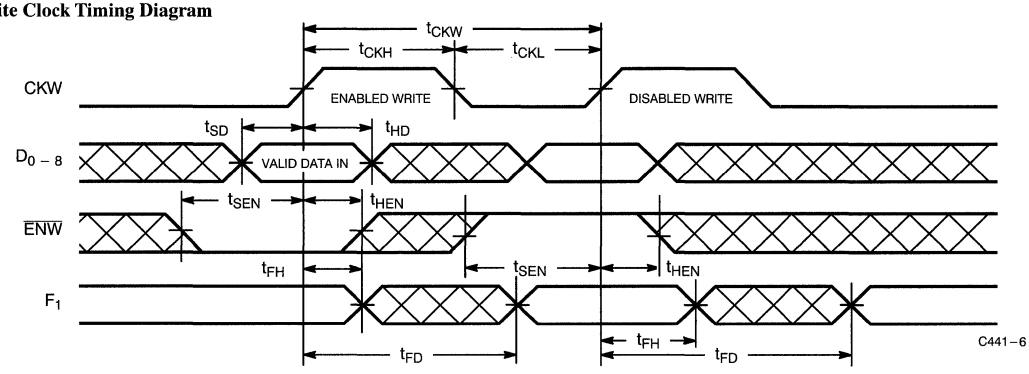
Parameter	Description	7C441–14 7C443–14		7C441–20 7C443–20		7C441–30 7C443–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[11]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[12]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[13]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns

Notes:

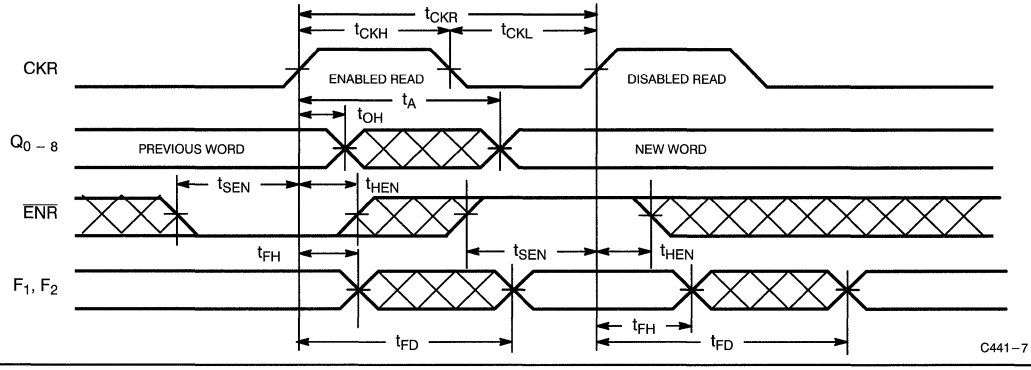
8. C_L = 30 pF for all AC parameters.
9. All AC measurements are referenced to 1.5V.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in the AC Test Loads and Waveforms and capacitance as in note NO TAG, unless otherwise specified.
11. Access time includes all data outputs switching simultaneously.
12. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full flag. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Almost Full flag, CKR is the clock for Empty and Almost Empty flags.
13. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is abritrary. See Note NO TAG for definition of clock and opposite clock.

Switching Waveforms

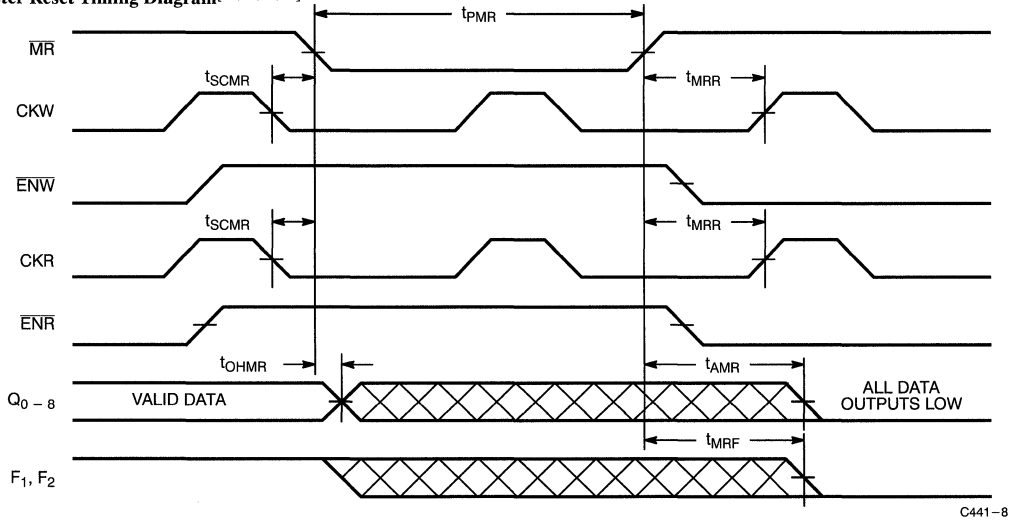
Write Clock Timing Diagram



Read Clock Timing Diagram

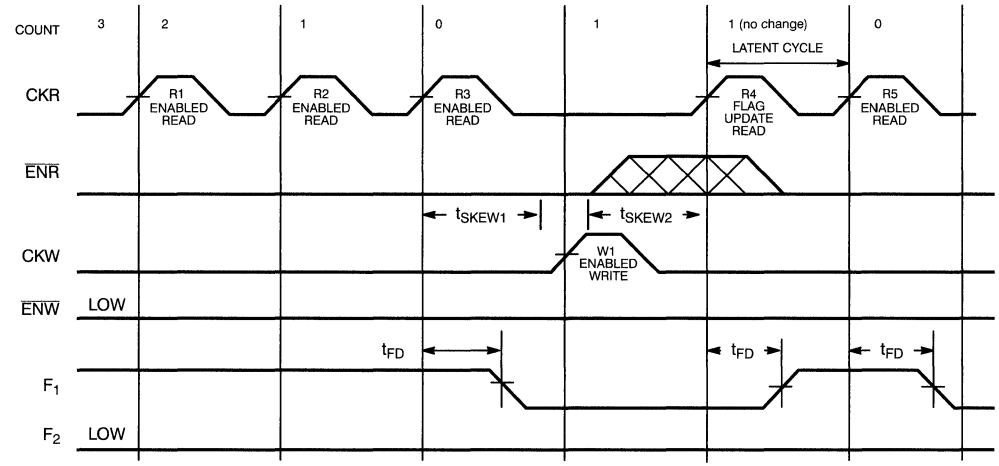


Master Reset Timing Diagram[14,15,16,17]



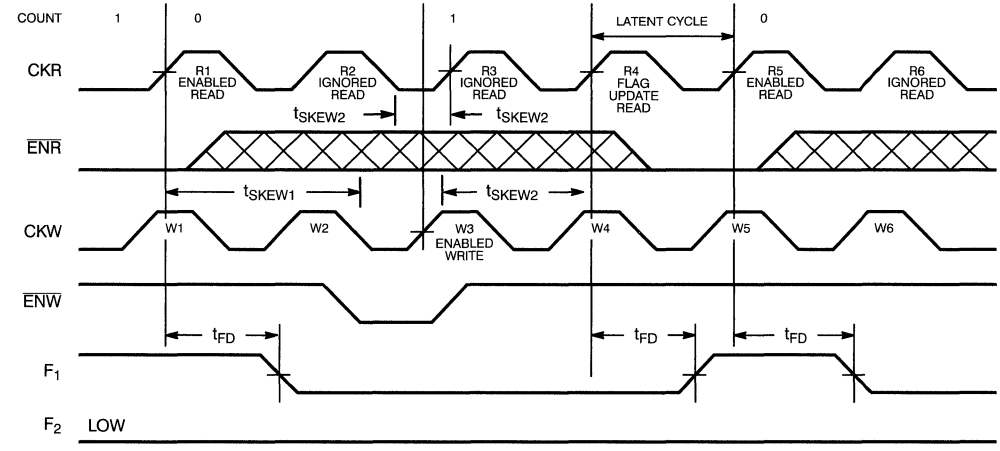
Switching Waveforms (continued)

Read to Empty Timing Diagram[18,19,20]



C441–10

Read to Empty Timing Diagram with Free-Running Clocks[18,19,21]



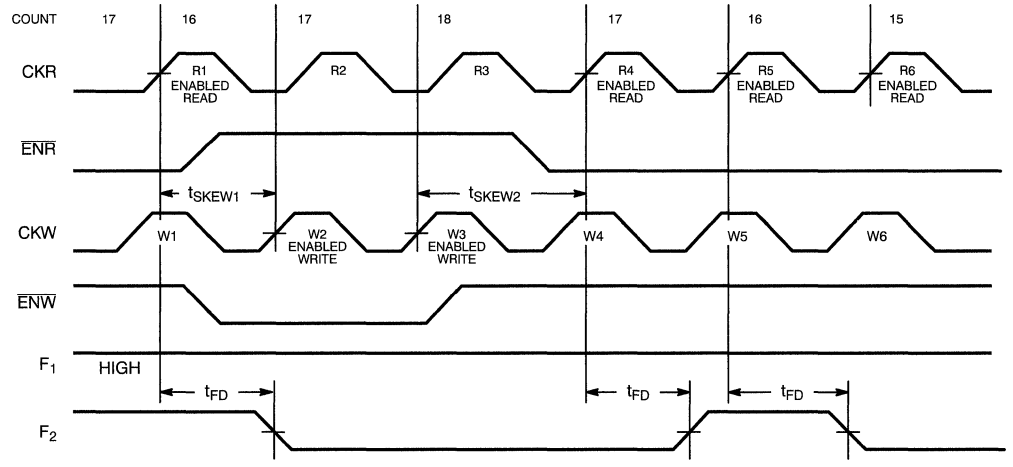
C441–9

Notes:

14. $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
15. $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
16. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$.
17. In this example, Q_{0-8} will remain valid until t_{OHMR} if the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.
18. "Count" is the number of words in the FIFO.
19. CKR is clock and CKW is opposite clock.
20. R3 updates the flags to the Empty state by bringing F1 LOW. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and therefore updates the FIFO to the Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status, regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.
21. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.

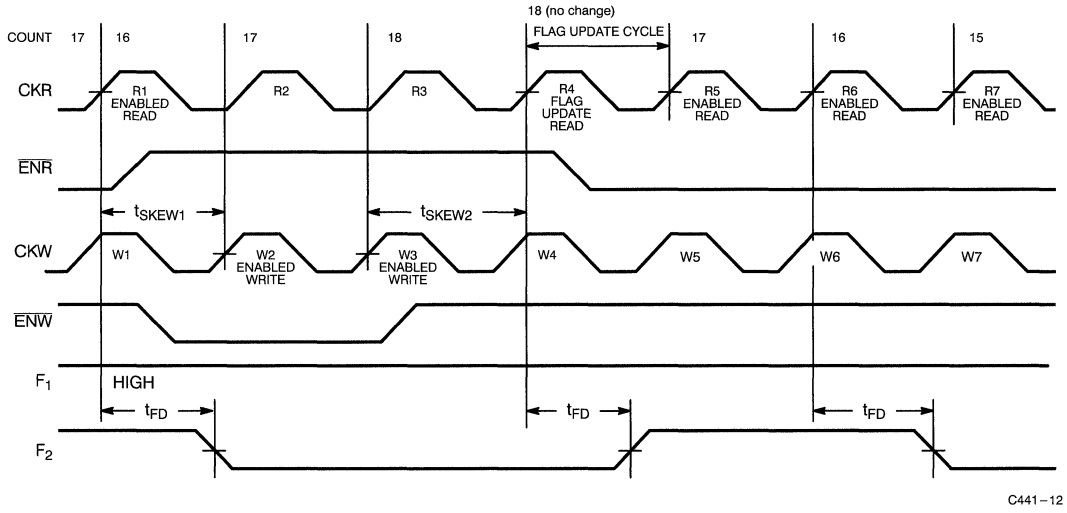
Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[18,19]



C441-11

Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[18,19,22,23]



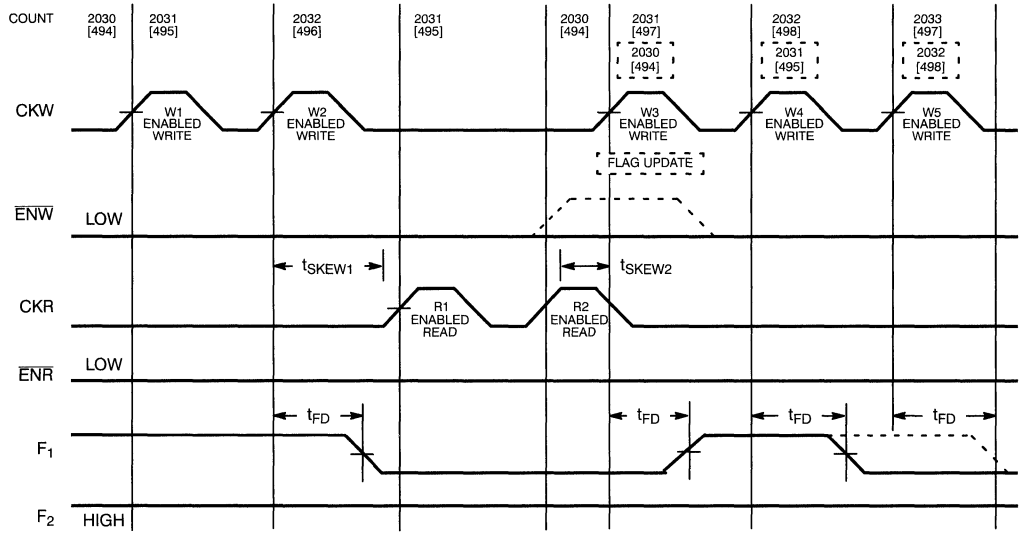
C441-12

Notes:

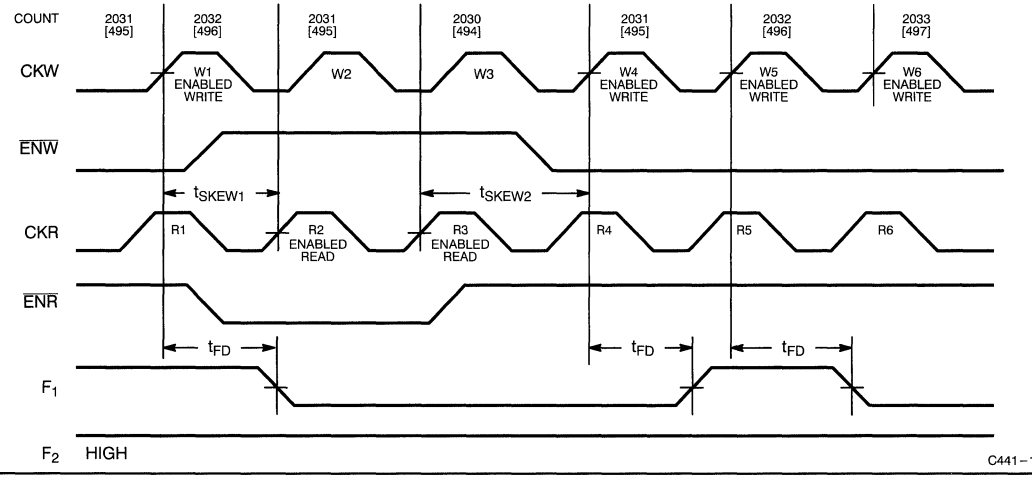
22. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
23. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧ 18; two enabled writes: W2, W3) before a read (R4) can update flags to the Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram[18,24,25,26,27]



Write to Almost Full Timing Diagram with Free-Running Clocks[18,24,25]

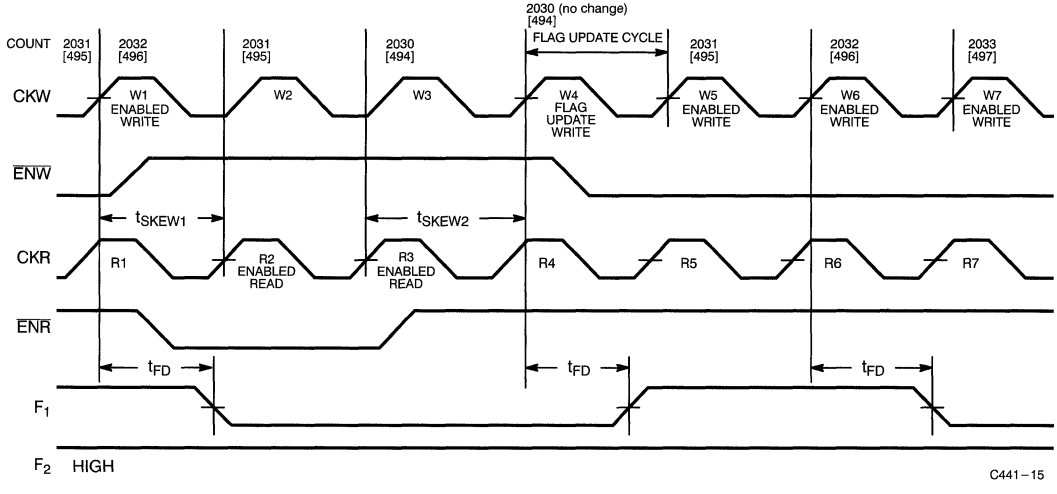


Notes:

24. CKW is clock and CKR is opposite clock.
25. Count = 2032 indicates Almost Full for CY7C443 and count = 496 indicates Almost Full for CY7C441. Values for the CY7C441 count are shown in brackets.
26. The dashed lines show W3 as flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.
27. W2 updates the flags to the Almost Full state by bringing F1 LOW. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
28. When making the transition from Almost Full to Intermediate, the count must decrease by two (2032 ♦ 2030; two enabled reads: R2, R3) before a write (W4) can update flags to Intermediate state.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clock[18,24,25,28]



Architecture

The CY7C441/443 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$), and flags (F1, F2).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by both flags F1 and F2 being LOW. All data outputs (Q_{0-8}) go LOW at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. F_1 and F_2 are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read duration. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Flag Operation

The CY7C441/3 provide two flags, F1 and F2, which are used to decode four FIFO states (see *Table 1*). All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate; see *Figure 1*). The synchronous architecture guarantees some minimum valid time for the flags.

The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the F1 and F2 pins to output a state signifying the Empty condition. The Almost Full flag is updated exclusively by the write clock (CKW). For example, if the CY7C443 FIFO contains 2031 words (2032 words or greater indicates Almost Full in the CY7C443), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the F1 and F2 pins to output the Almost Full state.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the Almost Full flag is only updated by the CKW, careful attention must be given to the flag operation. The user must be aware that if a flag boundary (Empty, Almost Empty, and Almost Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e.,CKR does not effect Almost Full), a flag update is necessary to represent the FIFO's new state. This signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for the Almost Full flag).

Table 1. Flag Truth Table

F1	F2	State	CY7C441 Number of Words in FIFO	CY7C443 Number of Words in FIFO
0	0	Empty	0	0
1	0	Almost Empty	1 – 16	1 – 16
1	1	Intermediate Range	17 – 495	17 – 2031
0	1	Almost Full or Full	496 – 512	2032 – 2048

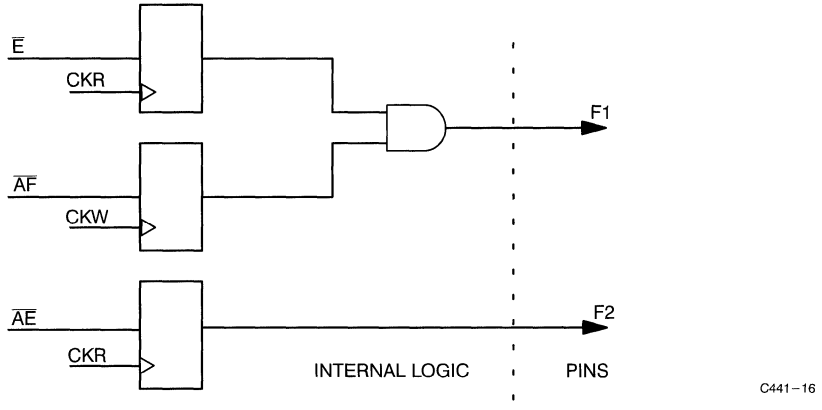


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Until the flag update cycle is executed, the synchronous flags do not show the true state of the FIFO. For example, if 2,040 writes are performed to an empty CY7C443 without a single read, F1 and F2 will still exhibit an Empty flag. This is because F2 is exclusively updated by the CKR, therefore, a single read (flag update cycle) is necessary to update flags to Almost Full state. It should be noted that this flag update read does not require $\overline{ENR}$ = LOW, so a free-running read clock will initiate the flag update cycle.

When updating the flags, the CY7C441/443 decide whether or not the opposite clock was recognized when a clock updates the flag. For example, if a write occurs at least t_{SKEW1} after a read when updating the Empty flag, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates the flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Almost Full) is different from that used to update the boundary flag (Empty). Both operations are described below.

Boundary Flag (Empty)

The Empty flag is synchronized to the CKR signal. The Empty flag can only be updated by a clock pulse on the CKR pin. An empty FIFO that is written to will be described with an Empty flag state until a clock pulse is presented on the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Intermediate or Empty to Almost Full), a clock cycle on the CKR is necessary to update the flags to the current state. Such a state (flags displaying empty even though data has been written to the FIFO) would require two read cycles to read data out of FIFO. The first read serves only to update the flags to the Almost Empty, Intermediate, or Almost Full state, and the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flags are updated regardless of the $\overline{ENR}$ state. Therefore the update occurs even when $\overline{ENR}$ is deasserted (HIGH) so that a valid read is not necessary to update the flags to correctly describe the FIFO. With a free-running clock connected to CKR, the flag updates with each cycle. *Figure 1* shows sample operations that update the Empty flag.

Although a Full flag is not supplied externally on the CY7C441/CY7C443, a Full flag exists internally. The operation of the FIFO at the Full boundary is analogous to its operation at the Empty boundary. See the text section "Boundary Flags (Full)" in the CY7C451/CY7C453 datasheet.

Non-Boundary Flags (Almost Empty, Almost Full)

The flag status pins, F_1 and F_2, exhibit the Almost Empty status when both the CY7C441 and the CY7C443 contain 16 words or less. The Almost Full Flag becomes active when the FIFO contains 16 or less empty locations. The CY7C441 becomes Almost Full when it contains 496 words. The CY7C443 becomes Almost Full when it contains 2032 words. The Almost Empty flag (like the Empty flag) is synchronous to the CKR signal, whereas the Almost Full flag is synchronous to the CKW signal. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO state. For example, if the FIFO just reaches the Almost Empty state (16 words) and then two words are written, a read clock (CKR) will be required to update the flags to the Intermediate state. However, unlike the boundary (Empty) flag's update cycle, the state of the enable pin ($\overline{ENR}$ in this case) affects the operation. Therefore, ENR set-up (t_{SEN}) and hold (t_{HEN}) times must be met. If $\overline{ENR}$ is asserted ($\overline{ENR}$=LOW) during the latent cycle, the count and data update in addition to F1 and F2. If $\overline{ENR}$ is not active ($\overline{ENR}$=1) during the flag update cycle, only the flag is updated.

The same principles apply for updating the flags when a transition from the Almost Full to the Intermediate state occurs. If the CY7C443 just reaches the Almost Full state (2032 words) and then two words are read, a write clock (CKW) will be required to update the flag to the Intermediate state. If $\overline{ENW}$ is LOW during the flag update cycle, the count and data update in addition to the flags. If $\overline{ENW}$ is HIGH, only the flag is updated. Therefore, $\overline{ENW}$ set-up (t_{SEN}) and hold (t_{HEN}) times must be met. *Tables 3* and *4* show examples for a sequence of operations that affect the Almost Empty and Almost Full flags, respectively.

Width Expansion

The CY7C441/3 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode, all control inputs are common. When the FIFO is being read near

the Empty boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty condition on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width expanded devices (A and B), device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored).The first write occurs because a read within t_{SKEW2} of the first write is only guaranteed to be either recognized or ignored, but which of the two is not guaranteed. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to outpout "staggered" data assuming more data has been written to the FIFOs.

In the width expansion configuration, any of the devices' flags may be monitored for the composite Almost Full status.

Table 2. Empty Flag Operation Example [29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Write ($\overline{ENW}$ = LOW)	Empty	0	0	2	Write
Empty	0	0	2	Read ($\overline{ENR}$ = HIGH)	AE	1	0	2	Flag Update
AE	1	0	2	Read ($\overline{ENR}$ = LOW)	AE	1	0	1	Read
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition for Almost Empty to Empty)
Empty	0	0	0	Write ($\overline{ENW}$ = LOW)	Empty	0	0	1	Write
Empty	0	0	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	Flag Update
AE	1	0	1	Read ($\overline{ENR}$ = LOW)	Empty	0	0	0	Read (Transition from Almost Empty to Empty)

Table 3. Almost Empty Flag Operation Example[29]

Status Before Operation						Status After Operation			
Current State of FIFO	F1	F2	Number of Words in FIFO	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO	Comments
AE	1	0	16	Write ($\overline{ENW}$ = LOW)	AE	1	0	17	Write
AE	1	0	17	Write ($\overline{ENW}$ = LOW)	AE	1	0	18	Write
AE	1	0	18	Read ($\overline{ENR}$ = LOW)	Intermediate	1	1	17	Flag Update and Read
Intermediate	1	1	17	Read ($\overline{ENR}$ = LOW)	AE	1	0	16	Read (Transition from Intermediate to Almost Empty)
AE	1	0	16	Read ($\overline{ENR}$ = HIGH)	AE	1	0	16	Ignored Read

Table 4. Almost Full Flag Operation Example[30,31]

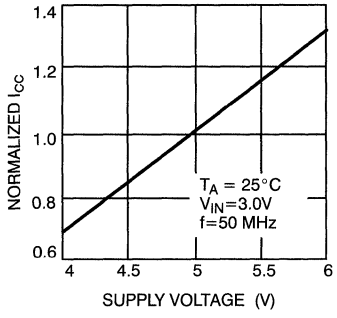
Status Before Operation							Status After Operation				
Current State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Operation	Next State of FIFO	F1	F2	Number of Words in FIFO CY7C441	Number of Words in FIFO CY7C443	Comments
AF	0	1	496	2032	Read ($\overline{ENR}$=LOW)	AF	0	1	495	2031	Read
AF	0	1	495	2031	Read ($\overline{ENR}$=LOW)	AF	0	1	494	2030	Read
AF	0	1	494	2030	Write ($\overline{ENW}$=HIGH)	Intermediate	1	1	494	2030	Flag Update
Intermediate	1	1	494	2030	Write ($\overline{ENW}$=LOW)	Intermediate	1	1	495	2031	Write
Intermediate	1	1	495	2031	Write ($\overline{ENW}$=LOW)	AF	0	1	496	2032	Write (Transition from Intermediate to Almost Full)

Notes:
29. Applies to both the CY7C441 and CY7C443 operations.
30. The CY7C441 Almost Full state is represented by 496 or more words.
31. The CY7C443 Almost Full state is represented by 2032 or more words.

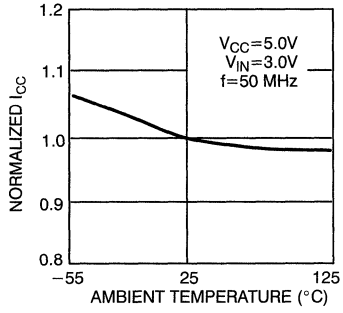
5

Typical DC and AC Characteristics

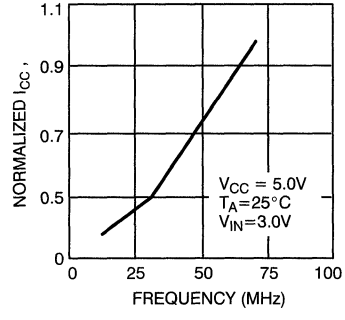
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



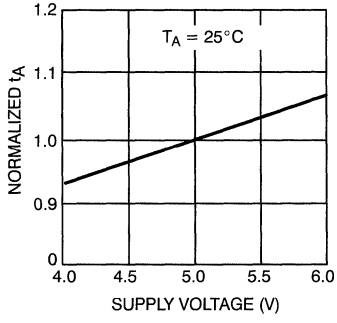
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



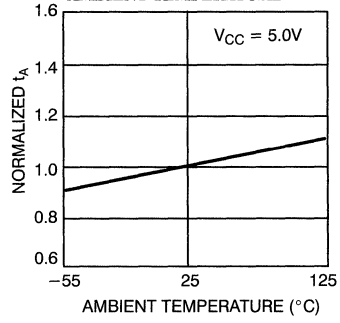
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



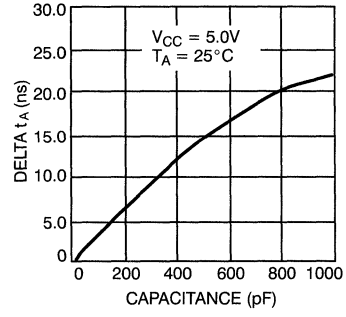
NORMALIZED t_A vs. SUPPLY VOLTAGE



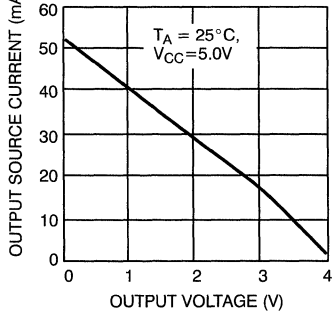
NORMALIZED t_A vs. AMBIENT TEMPERATURE



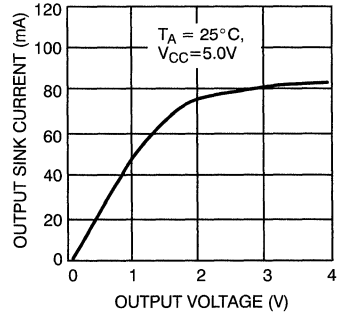
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C441–14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C441–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C441–30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C441–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C441–30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C441–30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C441–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C441–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C443–14PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–14VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–14PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–14JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–14DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C443–20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–20PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–20JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C443–30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C443–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C443–30PI	P21	28-Lead (300-Mil) Molded DIP	Industrial
	CY7C443–30JI	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C443–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C443–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKR}	9, 10, 11
t_{CKW}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{HENR}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11

Document #: 38−00124−F

CY7C451
CY7C453

512 x 9 Cascadable Clocked and 2K x 9 Cascadable Clocked FIFOs with Programmable Flags

Features

- **512 x 9 (CY7C451) and 2,048 x 9 (CY7C453) FIFO buffer memory**
- **Expandable in width and depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable Almost Full/Empty flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$)**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Available in 300-mil 32-pin DIP, PLCC, and LCC packages**
- **Proprietary 0.8µ CMOS technology**
- **Low power**
  —I_{CC}=70 mA

Functional Description

The CY7C451 and CY7C453 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. Both FIFOs are 9 bits wide. The CY7C451 has a 512-word by 9-bit memory array, while the CY7C453 has a 2048-word by 9-bit memory array. Devices can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

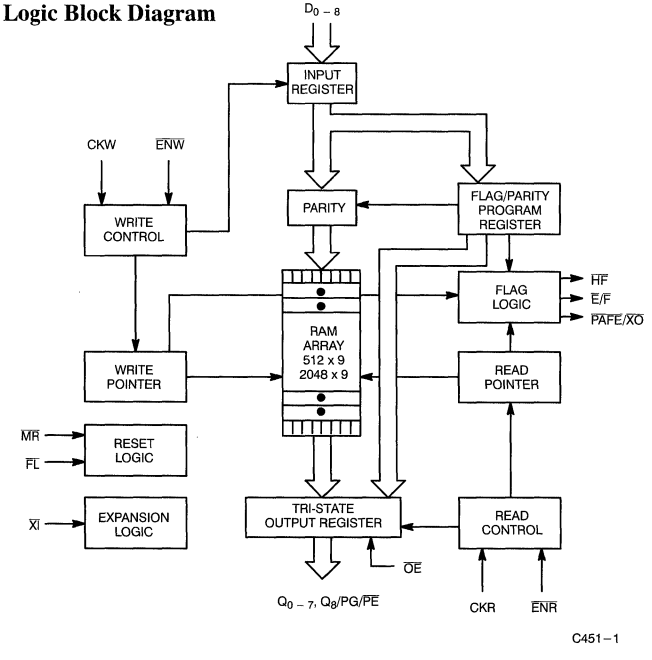
Both FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle.

The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are acceptable in the standalone configuration, and up to 50 MHz is acceptable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input ($\overline{XI}$) and cascade output ($\overline{XO}$). The $\overline{XO}$ signal is connected to the $\overline{XI}$ of the next device, and the $\overline{XO}$ of the last device should be connected to the $\overline{XI}$ of the first device. In standalone mode, the input ($\overline{XI}$) pin is simply tied to V_{SS}.

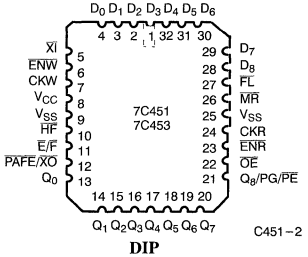
The CY7C451 and CY7C453 provide three status pins to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{PAFE}$) and $\overline{XO}$ functions share the same pin. The Almost Empty/Full flag is

Logic Block Diagram

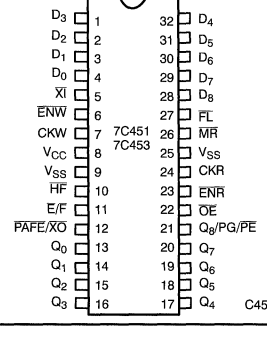


Pin Configurations

PLCC/LCC
Top View



DIP
Top View



Functional Description (continued)

valid in the standalone and width expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{XO}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time.

The CY7C451 and the CY7C453 use center power and ground for reduced noise. Both configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

Selection Guide

		7C451–14 7C453–14	7C451–20 7C453–20	7C451–30 7C453–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadable Frequency		N/A[2]	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		7	9	12
Minimum Data or Enable Hold (ns)		0	0	0
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	140	120	100
	Military/Industrial	150	130	110

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Notes:

1. 71.4-MHz operation is available only in the standalone configuration.
2. The −14 device cannot be cascaded.
3. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
D_{0-8}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-8}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW then data is written into the FIFO's programming register. D_8 is ignored if the device is configured for parity generation.
Q_{0-7}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR then data is read from the programming register.
$Q_8/PG/\overline{PE}$	O	Function varies according to mode: Parity disabled – same function as Q_{0-7} Parity enabled, generation – parity generation bit (PG) Parity enabled, check – Parity Error Flag ($\overline{PE}$)
$\overline{ENW}$	I	Enable Write: enables the CKW input (for both non-program and program modes)
$\overline{ENR}$	I	Enable Read: enables the CKR input (for both non-program and program modes)
CKW	I	Write Clock: the rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: the rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag – synchronized to CKW.
$\overline{E}/\overline{F}$	O	Empty or Full Flag – $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW
$\overline{PAFE}/\overline{XO}$	O	Dual-Mode Pin: Not Cascaded – Programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR Cascaded – Expansion Out signal, connected to $\overline{XI}$ of next device
$\overline{XI}$	I	Not Cascaded – $\overline{XI}$ is tied to V_{SS} Cascaded – Expansion Input, connected to $\overline{XO}$ of previous device
$\overline{FL}$	I	First Load Pin: Cascaded – the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure2*) Not Cascaded – tied to V_{CC}
$\overline{MR}$	I	Master Reset: resets device to empty condition. Non-Programming Mode: program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of CKW. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7} and $Q_8/PG/\overline{PE}$ pins

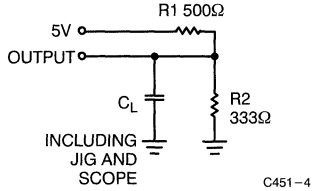
Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C451–14 7C453–14 Min.	7C451–14 7C453–14 Max.	7C451–20 7C453–20 Min.	7C451–20 7C453–20 Max.	7C451–30 7C453–30 Min.	7C451–30 7C453–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[5]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[5]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	µA
I_{OS}[6]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+ 10	µA
I_{CC1}[7]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		140		120		100	mA
			Mil/Ind		150		130		110	mA
I_{CC2}[8]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		70	mA
			Mil/Ind		80		80		80	mA
I_{SB}[9]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		30		30		30	mA
			Mil/Ind		30		30		30	mA

Capacitance[10]

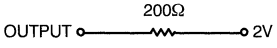
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

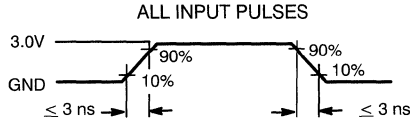
AC Test Loads and Waveforms[11, 12, 13, 14, 15]



C451–4

Equivalent to: THÉVENIN EQUIVALENT





C451–5

Notes:

4. See the last page of this specification for Group A subgroup testing information.
5. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
6. Test no more than one output at a time for not more than one second.
7. Input signals switch from 0V to 3V with a rise/fall time of 3 ns or less, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
8. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
9. All inputs signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
10. Tested initially and after any design or process changes that may affect these parameters.
11. C_L = 30 pF for all AC parameters except for t_{OHZ}.
12. C_L = 5 pF for t_{OHZ}.
13. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
14. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
15. t_{OHZ} is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[4, 16]

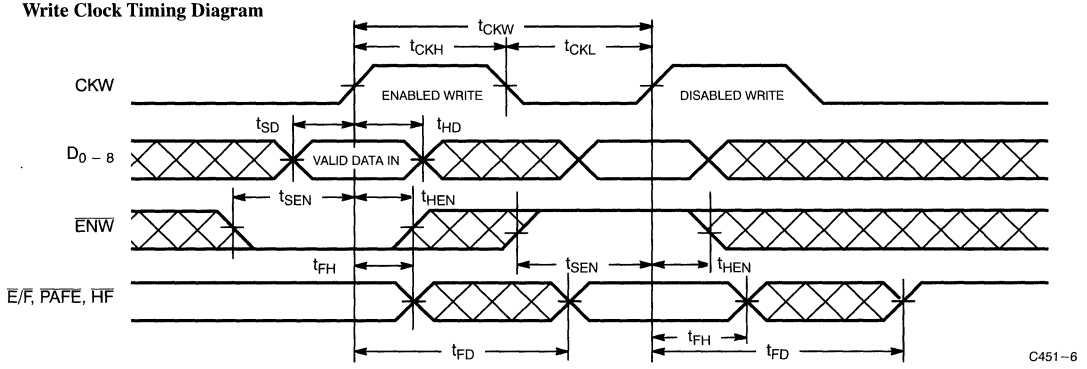
Parameter	Description	7C451–14 7C453–14		7C451–20 7C453–20		7C451–30 7C453–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A[17]	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	7		9		12		ns
t_{HD}	Data Hold	0		0		0		ns
t_{SEN}	Enable Set-Up	7		9		12		ns
t_{HEN}	Enable Hold	0		0		0		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[10, 18]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[10, 18]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[19]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[20]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		25		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

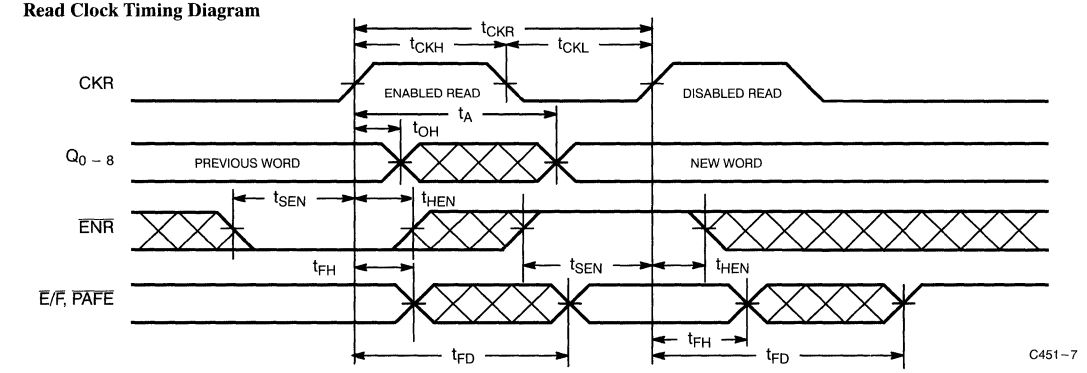
16. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 11 and 12, unless otherwise specified.
17. Access time includes all data outputs switching simultaneously.
18. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
19. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.
20. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 19 for definition of clock and opposite clock.

Switching Waveforms

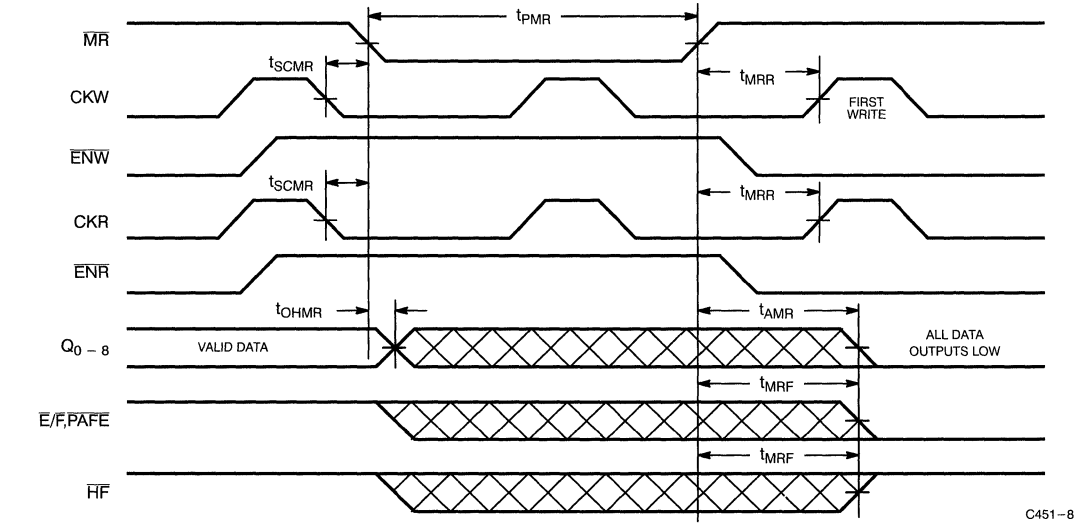
Write Clock Timing Diagram



Read Clock Timing Diagram

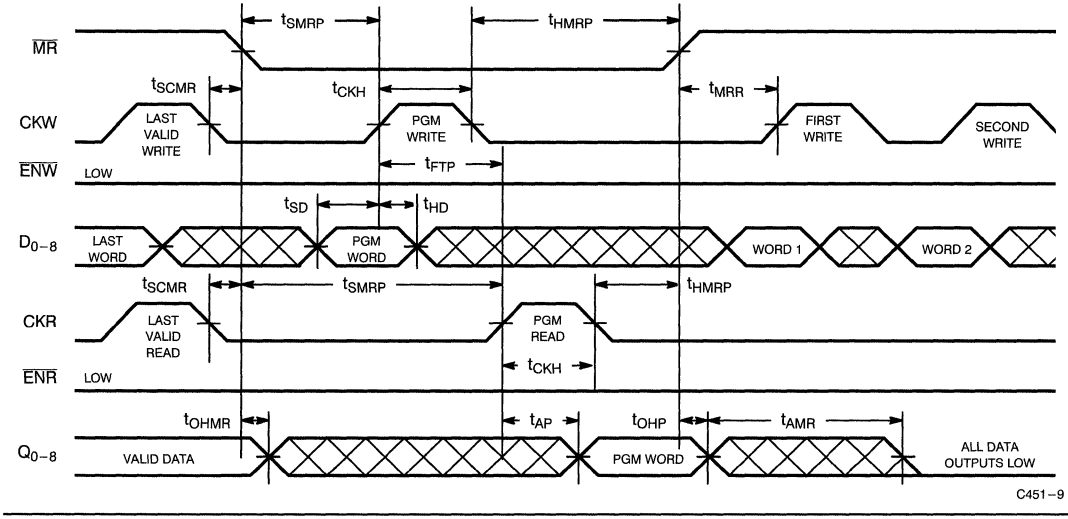


Master Reset (Default with Free-Running Clocks) Timing Diagram[21, 22, 23, 24]

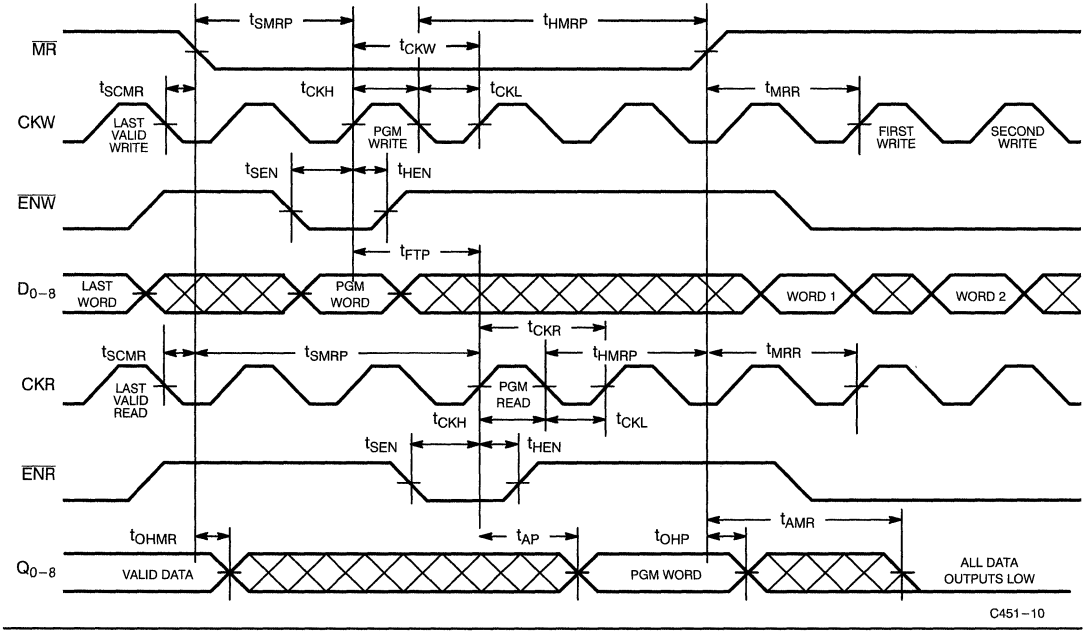


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[23, 24]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[23, 24]

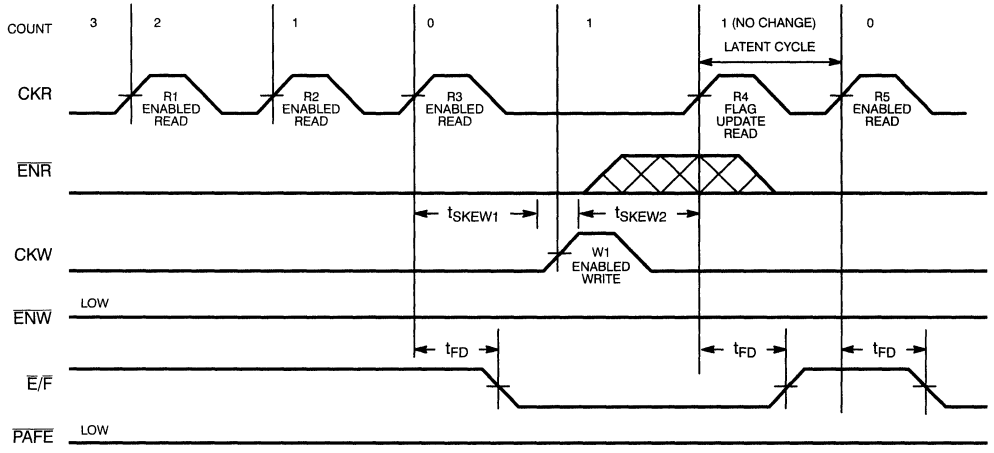


Notes:

21. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
22. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
23. All data outputs (Q_{0-8}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
24. In this example, Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

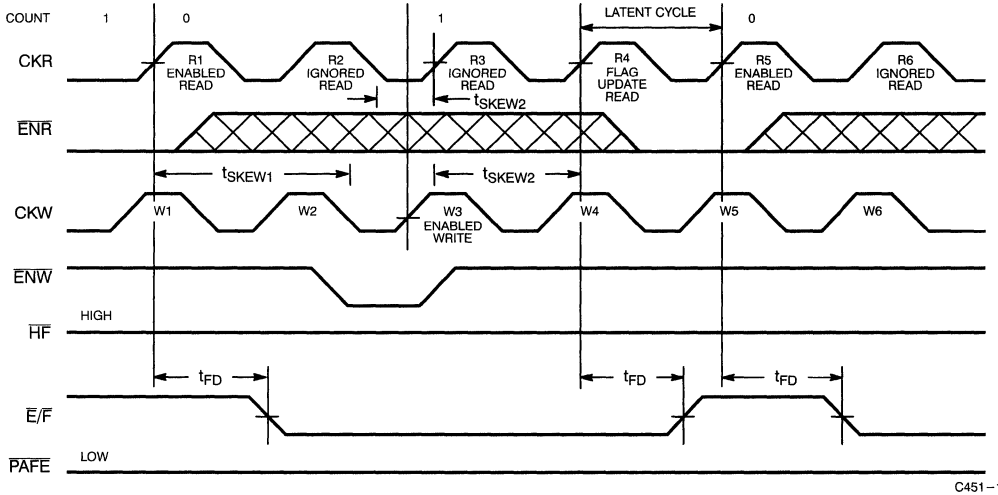
Switching Waveforms (continued)

Read to Empty Timing Diagram[25, 28, 29]



C451–12

Read to Empty Timing Diagram with Free-Running Clocks[25, 26, 27, 28]



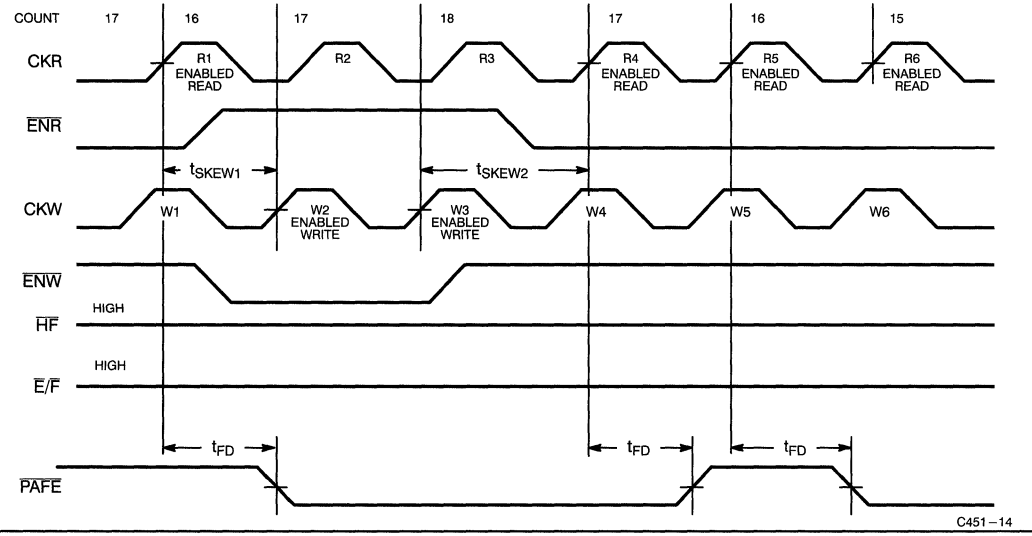
C451–11

Notes:

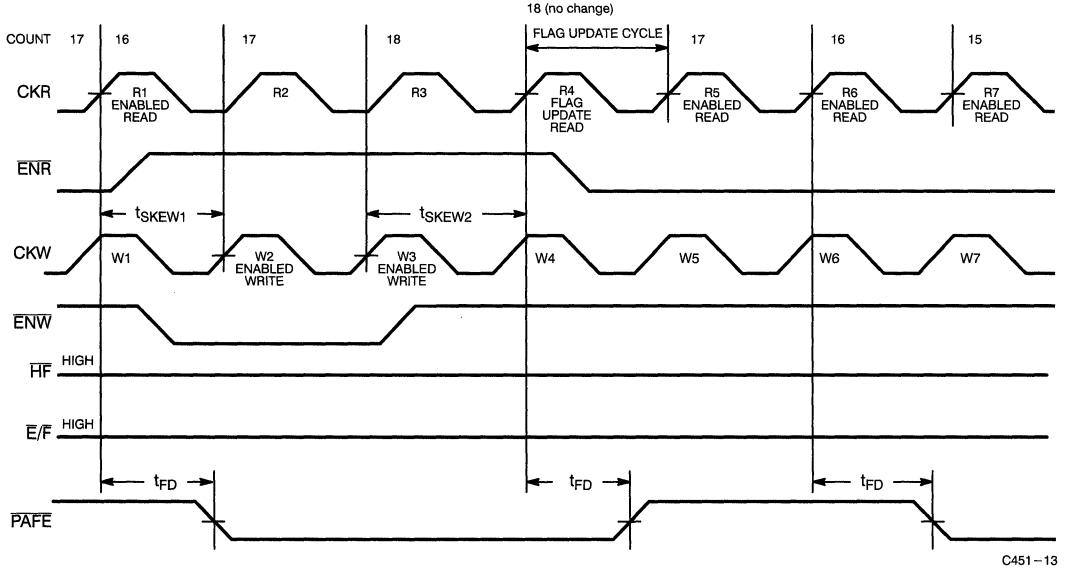
25. "Count" is the number of words in the FIFO.
26. The FIFO is assumed to be programmed with P>0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
27. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
28. CKR is clock; CKW is opposite clock.
29. R3 updates the flag to the Empty state by asserting $\overline{E/F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[25, 28, 30]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle and Free-Running Clocks[25, 28, 30, 31, 32]

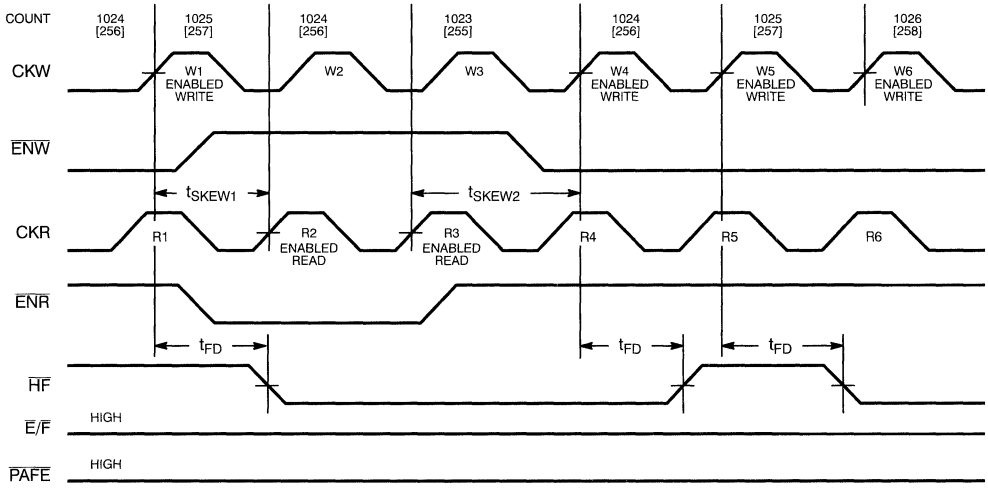


Notes:

30. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
31. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
32. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

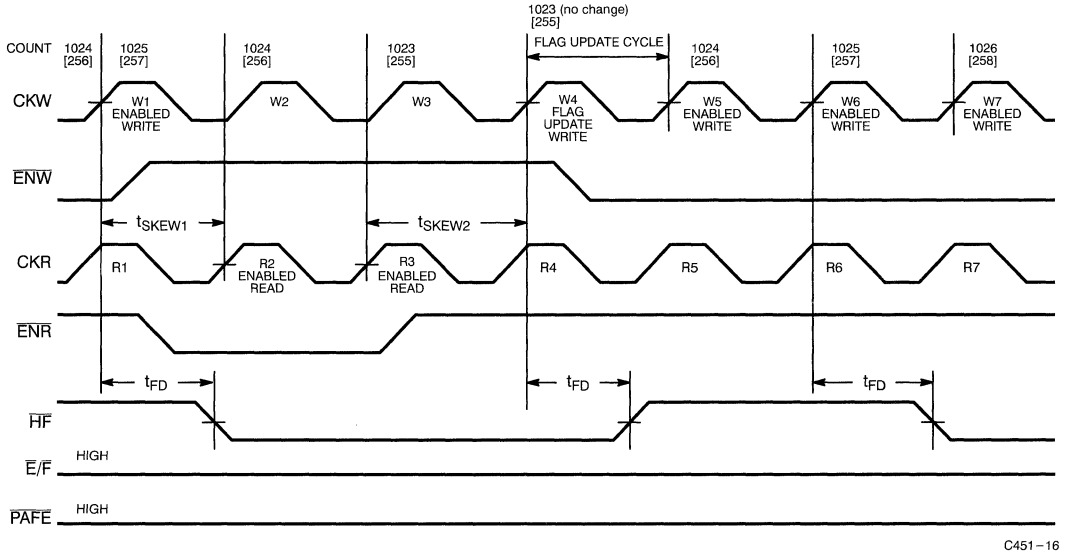
Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[25, 33, 34, 35]



C451–15

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[25, 33, 34, 35, 36, 37]



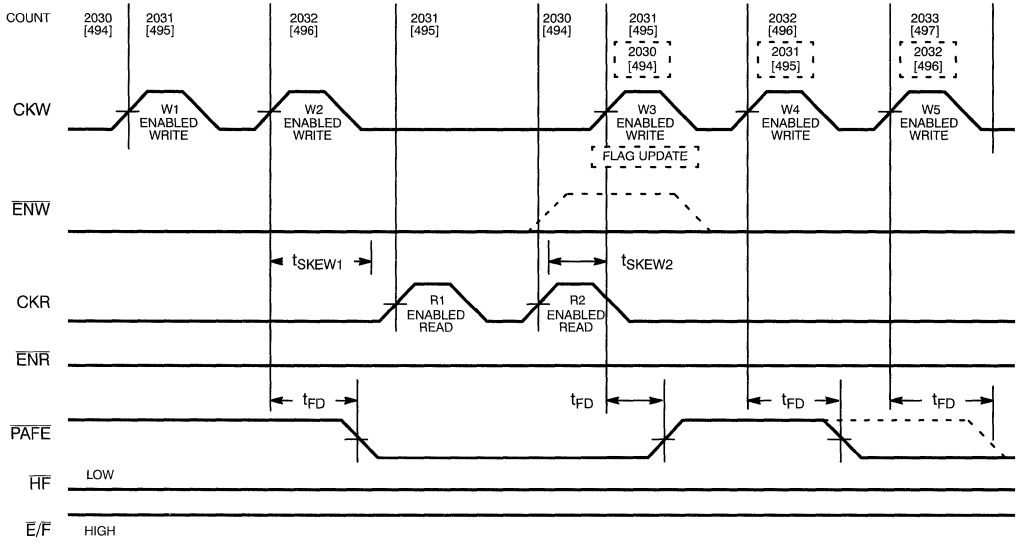
C451–16

Notes:

33. CKW is clock and CKR is opposite clock.
34. Count = 1,025 indicates Half Full for the CY7C453 and count = 257 indicates Half Full for the CY7C451. Values for CY7C451 count are shown in brackets.
35. When the FIFO contains 1,024 [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
36. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
37. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (1,025 ➧ 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

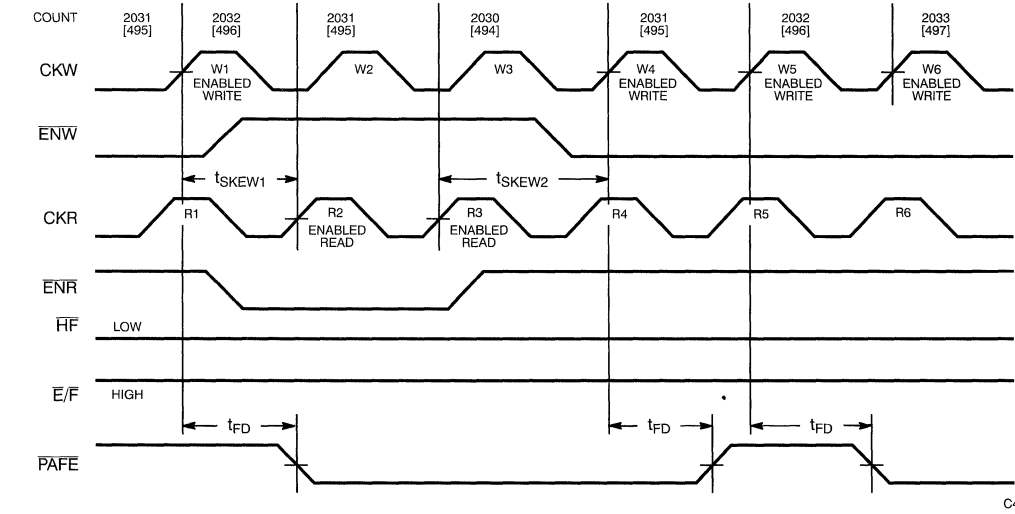
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[25, 30, 33, 38, 39]



C451–18

Write to Almost Full Timing Diagram with Free-Running Clocks[25, 30, 33]



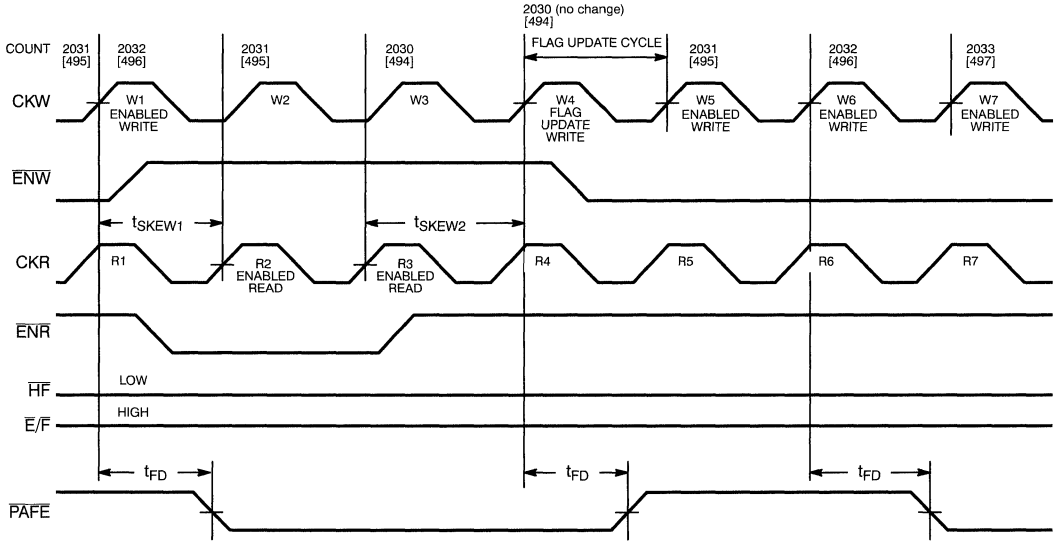
C451–17

Notes:

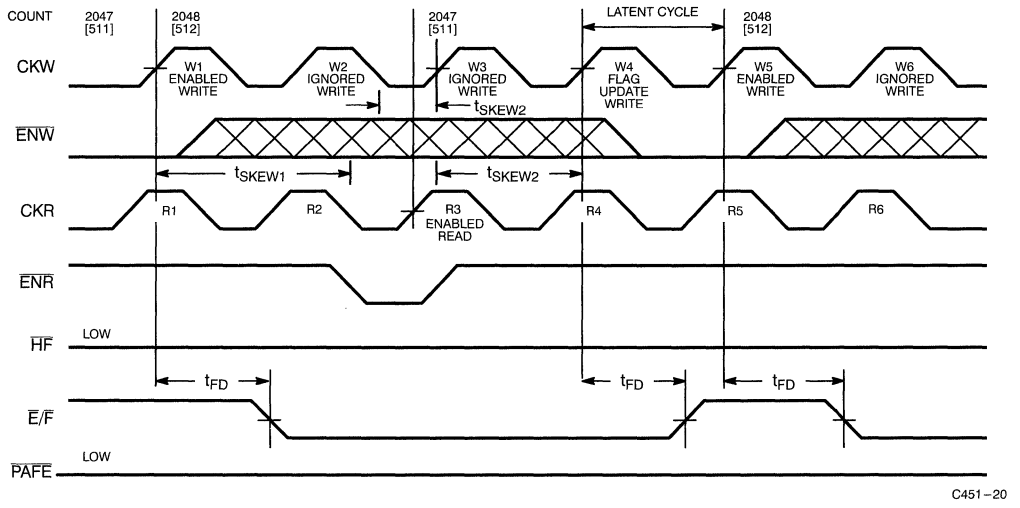
38. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
39. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[25, 30, 33]



Write to Full Flag Timing Diagram with Free-Running Clocks[25, 26, 33, 40]

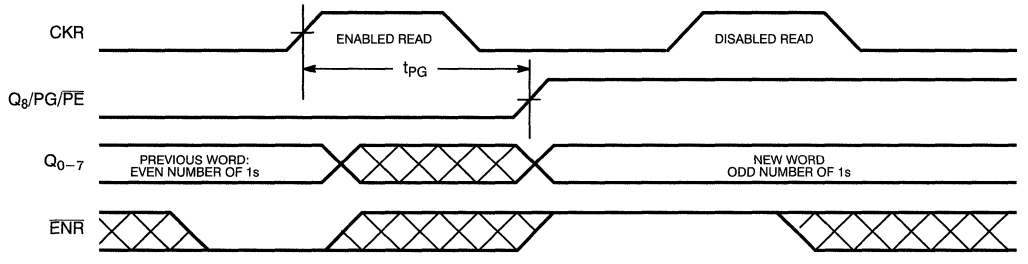


Notes:

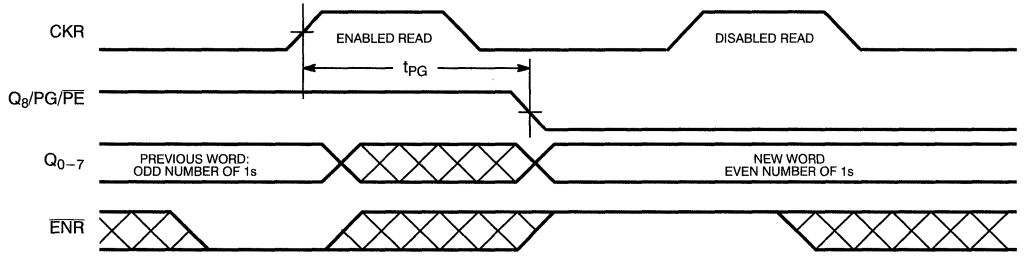
40. W2 is ignored because the FIFO is full (count = 2,048 [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram[41, 42]



Even Parity Generation Timing Diagram[41, 43]

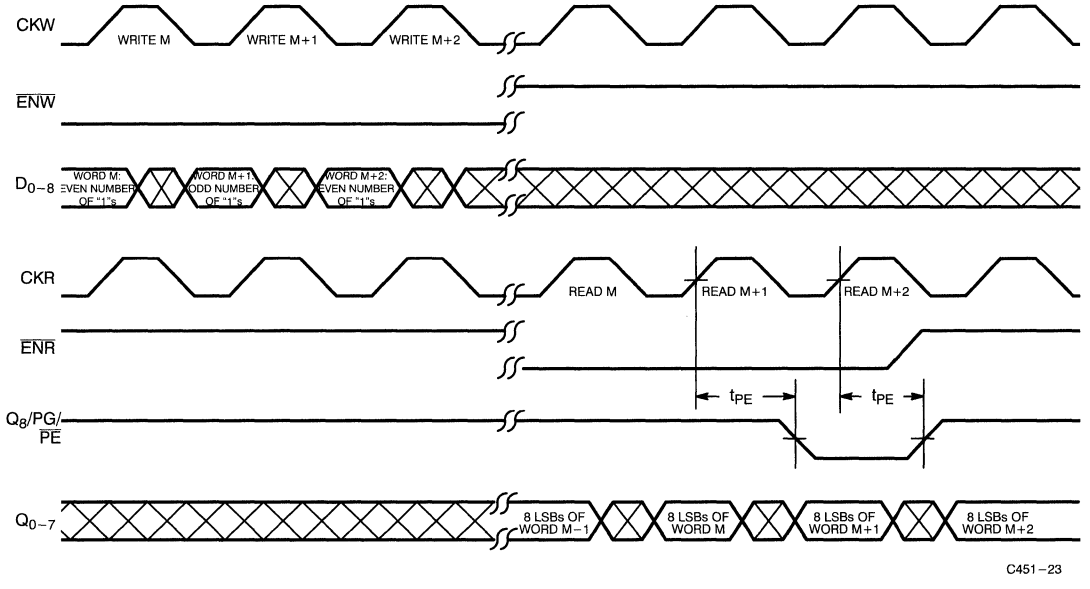


Notes:

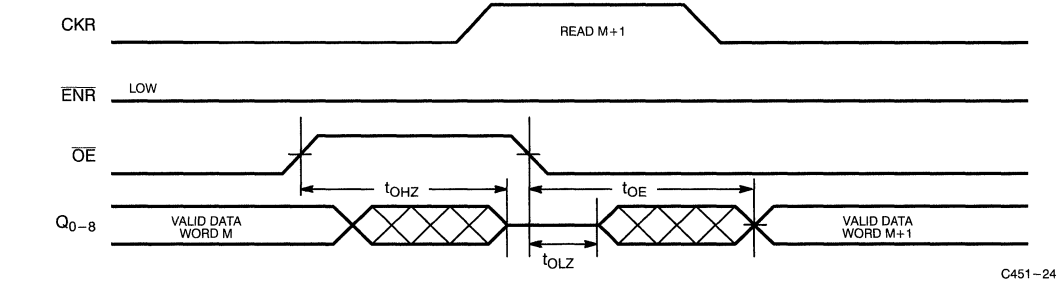
41. In this example, the FIFO is assumed to be programmed to generate even parity.
42. If Q_{0-7} "new word" also has an even number of 1s, then PG stays LOW.
43. If Q_{0-7} "new word" also has an odd number of 1s, then PG stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[44]



Output Enable Timing[45, 46]



Notes:

44. In this example, the FIFO is assumed to be programmed to check for even parity.
45. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$.
46. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C451 and CY7C453 consist of an array of 512/2048 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{CKR}$, $\overline{CKW}$, $\overline{ENR}$, $\overline{ENW}$, $\overline{MR}$, $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, $\overline{XO}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-8}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the Master Reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-8} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-8} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to tri-state the Q_{0-8} outputs when $\overline{OE}$ is not asserted. When $\overline{OE}$ is enabled, data in the output register will be available to Q_{0-8} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-8} outputs even after additional reads occur.

Programming

The CY7C451 and CY7C453 are programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write D_{0-8} inputs into the programming register. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-5} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in 1 refers to the decimal equivalent of the binary number represented by D_{0-5}. Programming options for the CY7C451 and CY7C453 are listed in *Table 5*. Programming resolution is 16 words for either device.

The programmable $\overline{PAFE}$ function is only valid when the CY7C451/453 are not cascaded. If the user elects not to program the FIFO's flags, the default (P=1) is as follows: Almost Empty condition (Almost Full condition) is activated when the CY7C451/453 contain 16 or less words (empty locations).

Parity is programmed with the D_{6-8} bits. See *Table 6* for a summary of the various parity programming options. Data present on D_{6-8} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-8} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C451/453 provide three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when FIFOs are cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate. See *Figure 1.*). The synchronous architecture guarantees some minimum valid time for the flags. The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock (CKW). For example, if the CY7C453 FIFO contains 2047 words (2048 words indicate Full for the CY7C453), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Table 1. Flag Truth Table[47]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	CY7C451 512 x 9 Number of Words in FIFO	CY7C453 2K x 9 Number of Words in FIFO
0	0	1	Empty	0	0
1	0	1	Almost Empty	1 ➧ (16 • P)	1 ➧ (16 • P)
1	1	1	Less than or Equal to Half Full	(16 • P)+1 ➧ 256	(16 • P)+1 ➧ 1024
1	1	0	Greater than Half Full	257 ➧ 511 − (16 • P)	1025 ➧ 2047 − 16 • P
1	0	0	Almost Full	512 − (16 • P) ➧ 511	2048 − (16 • P) ➧ 2047
0	0	0	Full	512	2048

Note:

47. P is the decimal value of the binary number represented by D_{0-5}. When programming the CY7C451/53, P can have values from 0 to 15 for the CY7C451 and values from 0 to 63 for the CY7C453. See *Table 5* for D_{0-5} representation. P = 0 signifies Almost Empty state = Empty state.

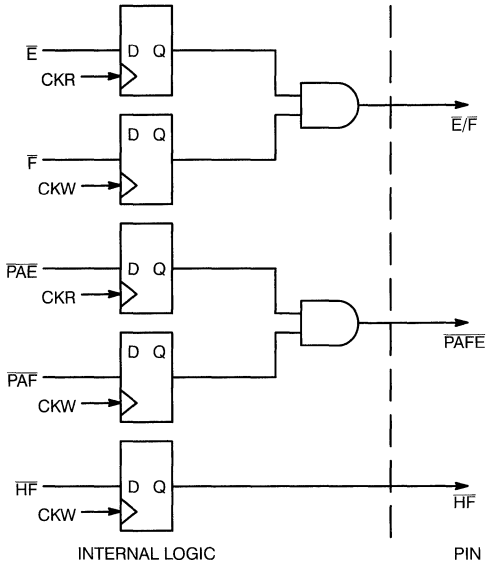


Figure 1. Flag Logic Diagram

Flag Operation (continued)

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the CY7C451/453 must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1}/t_{SKEW2} after or before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on the CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read cycles are required to read data out of FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is unasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on the CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C451/453 feature programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at a distance of up to 1008 words/locations for the CY7C453 (240 words/locations for the CY7C451) from the Empty/Full boundary. The programming resolution is 16 words/locations. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

The default distance (CY7C451/453 not programmed) from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Tables 3* and *4* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

Programmable Parity

The CY7C451/453 also features even or odd parity checking and generation. D_{6-8} are used during a program write to describe the parity option desired. *Table 6* gives a summary of programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on one multimode output pin (Q8/PG/$\overline{PE}$). The three possible modes are described in the following paragraphs. Regardless of the mode selected, the $\overline{OE}$ pin retains tri-state control of all 9 Q_{0-8} bits.

Parity Disabled (Q8 mode)

When parity is disabled (or user does not program parity option) the CY7C451/453 stores all 9 bits present on D_{0-8} inputs internally and will output all 9 bits on Q_{0-8}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7}. D_8 input is ignored. The parity bit is stored internally as D_8 and during a subsequent read will be available on the PG pin along with the data word from which the parity was generated (Q_{0-7}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the CY7C451/453 is programmed for parity checking, the FIFO will compare the parity of D_{0-8} with the program register. If the expected parity is present, D_8 will be set HIGH internally. When this word is later read, $\overline{PE}$ will be HIGH. If a parity error occurs, D_8 will be set LOW internally. When this word is later read, $\overline{PE}$ will be LOW. For example, if parity check is set to odd and D_{0-8} have an even number of 1s, a parity error occurs. When that word is later read, $\overline{PE}$ will be asserted (LOW).

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. The CY7C451/453 can be expanded in width to provide word width greater than 9 in increments of 9. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C451/453 can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with

$\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-8}, Q_{0-8}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-8} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-8} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-8} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C451/453 are cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-8} during a program read. Q_{0-8} of all other devices will remain in a high-impedance state to avoid bus contention.

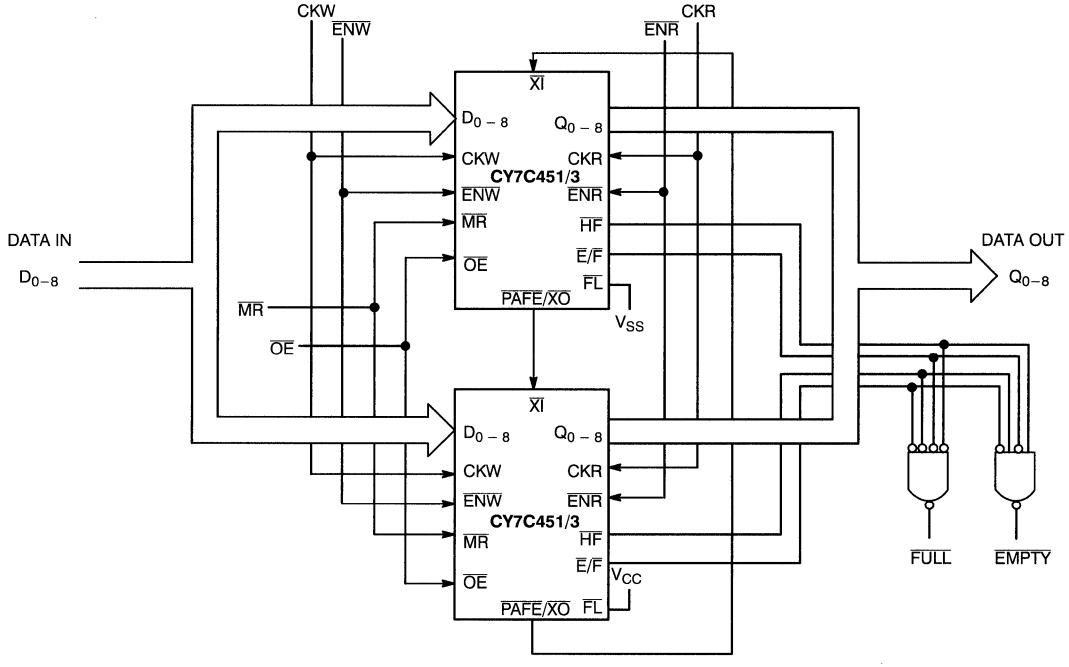


Figure 2. Depth Expansion with CY7C451/3

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[48]

Status Before Operation					Operation	Status After Operation					Comments
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO		Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (Transition from <HF to AE)

Table 4. Almost Full Flag Operation Example[49]

Status Before Operation						Operation	Status After Operation						Comments
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453		Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of Words in FIFO CY7C451	Number of Words in FIFO CY7C453	
AF	1	0	0	496	2032	Read ($\overline{ENR}$ = 0)	AF	1	0	0	495	2031	Read
AF	1	0	0	495	2031	Read ($\overline{ENR}$ = 0)	AF	1	0	0	494	2030	Read
AF	1	0	0	494	2030	Write ($\overline{ENW}$ = 1)	>HF	1	1	0	494	2030	Flag Update
>HF	1	1	0	494	2030	Write ($\overline{ENW}$ = 0)	>HF	1	1	0	495	2031	Write
>HF	1	1	0	495	2031	Write ($\overline{ENW}$ = 0)	AF	1	0	0	496	2032	Write (Transition from >HF to AF)

Notes:

48. Applies to both CY7C451 and CY7C453 operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.
49. Programmed so that Almost Full becomes active when the FIFO contains 16 or less empty locations.

Table 5. Programmable Almost Full/Almost Empty Options – CY7C451/CY7C453[50]

D5	D4	D3	D2	D1	D0	PAFE Active when CY7C451/453 is:	P[51]
0	0	0	0	0	0	Completely Full and Empty.	0
0	0	0	0	0	1	16 or less locations from Empty/Full (default)	1
0	0	0	0	1	0	32 or less locations from Empty/Full	2
0	0	0	0	1	1	48 or less locations from Empty/Full	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	1	1	1	0	224 or less locations from Empty/Full	14
0	0	1	1	1	1	240 or less locations from Empty/Full	15
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	992 or less locations from Empty/Full	62
1	1	1	1	1	1	1008 or less locations from Empty/Full	63

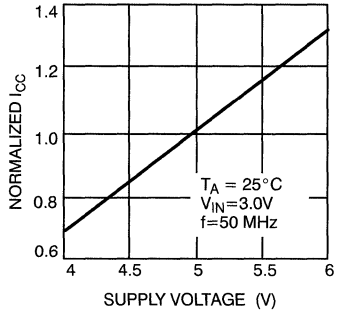
Table 6. Programmable Parity Options

D8	D7	D6	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

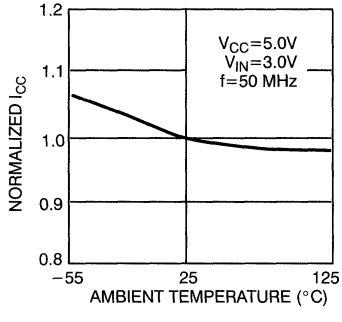
Notes:
50. D4 and D5 are don't care for CY7C451.
51. Referenced in *Table 1*.

Typical DC and AC Characteristics

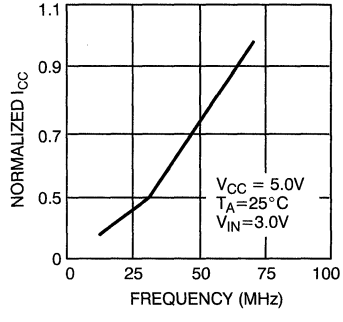
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



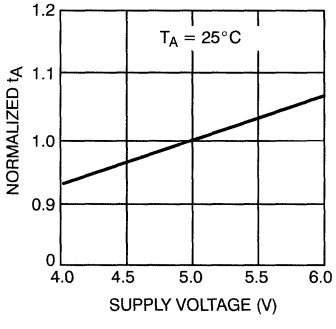
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



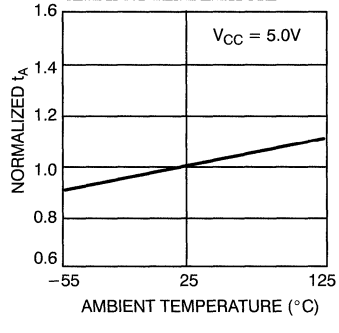
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



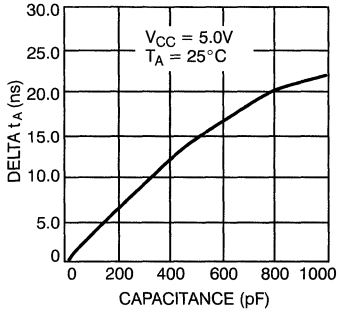
NORMALIZED t_A vs. SUPPLY VOLTAGE



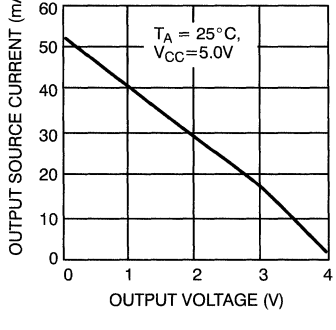
NORMALIZED t_A vs. AMBIENT TEMPERATURE



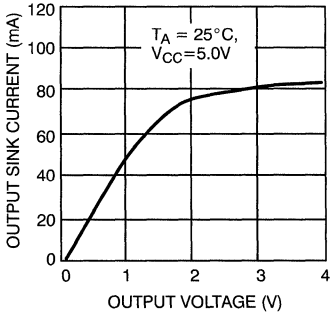
TYPICAL t_A CHANGE vs. OUTPUT LOADING



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C451–14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–14JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C451–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C451–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C451–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C451–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C451–30JI	D32	32-Lead (300-Mil) CerDIP	Industrial
	CY7C451–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C451–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

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14	CY7C453–14DC	D32	32-Lead (300-Mil) CerDIP	Commercial
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	CY7C453–14JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–14DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–14LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
20	CY7C453–20DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–20JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–20JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–20DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
30	CY7C453–30DC	D32	32-Lead (300-Mil) CerDIP	Commercial
	CY7C453–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C453–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C453–30DMB	D32	32-Lead (300-Mil) CerDIP	Military
	CY7C453–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{SB}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CKW}	9, 10, 11
t_{CKR}	9, 10, 11
t_{CKH}	9, 10, 11
t_{CKL}	9, 10, 11
t_{A}	9, 10, 11
t_{OH}	9, 10, 11
t_{FH}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{SEN}	9, 10, 11
t_{HEN}	9, 10, 11
t_{OE}	9, 10, 11
t_{PG}	9, 10, 11
t_{PE}	9, 10, 11
t_{FD}	9, 10, 11
t_{SKEW1}	9, 10, 11
t_{SKEW2}	9, 10, 11
t_{PMR}	9, 10, 11
t_{SCMR}	9, 10, 11
t_{OHMR}	9, 10, 11
t_{MRR}	9, 10, 11
t_{MRF}	9, 10, 11
t_{AMR}	9, 10, 11
t_{SMRP}	9, 10, 11
t_{HMRP}	9, 10, 11
t_{FTP}	9, 10, 11
t_{AP}	9, 10, 11
t_{OHP}	9, 10, 11

Document #: 38−00125−E

CY7C455
CY7C456
CY7C457

512 x 18, 1K x 18, and 2K x 18 Cascadable Clocked FIFOs with Programmable Flags

Features

- **512 x 18 (CY7C455), 1,024 x 18 (CY7C456), 2,048 x 18 (CY7C457) FIFO buffer memory**
- **Expandable in width**
- **Expandable in depth**
- **High-speed 70-MHz standalone; 50-MHz cascaded**
- **Supports free-running 50% duty cycle clock inputs**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **Parity generation/checking**
- **Fully asynchronous and simultaneous read and write operation**
- **Output Enable ($\overline{OE}$) pin**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **52-pin PLCC and 52-pin PQFP**
- **Proprietary 0.8µ CMOS technology**
- **TTL compatible**

Functional Description

The CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C455 has a 512-word memory array, the CY7C456 has a 1,024-word memory array, and the CY7C457 has a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

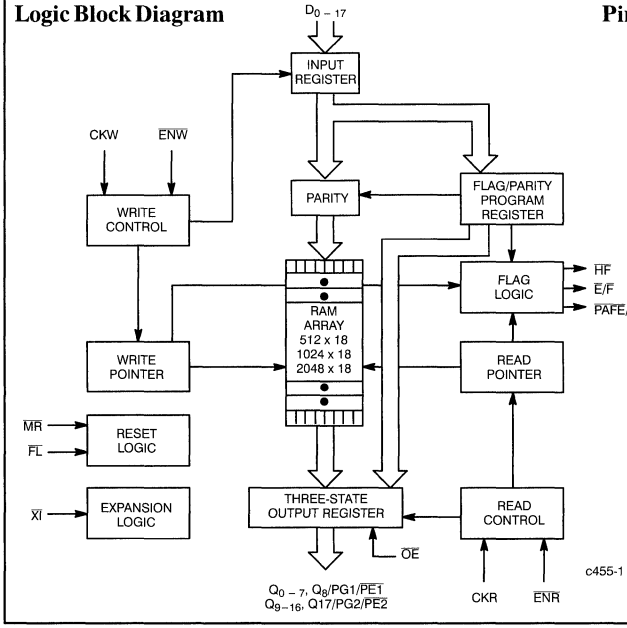
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin ($\overline{ENW}$).

When $\overline{ENW}$ is asserted, data is written into the FIFO on the rising edge of the CKW signal. While $\overline{ENW}$ is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin ($\overline{ENR}$). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin ($\overline{OE}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are achievable in the standalone configuration, and up to 50 MHz is achievable when FIFOs are cascaded for depth expansion.

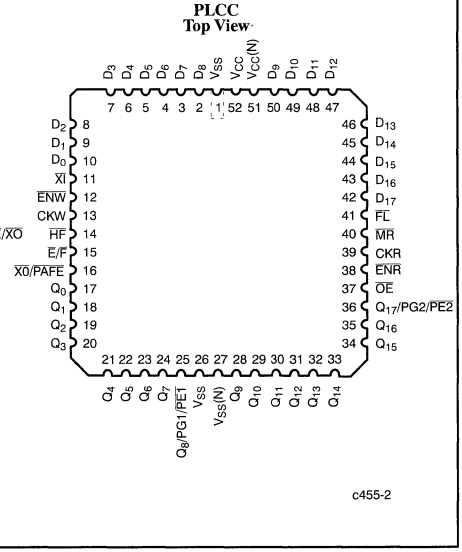
Depth expansion is possible using the cascade input ($\overline{XI}$), cascade output ($\overline{XO}$), and First Load ($\overline{FL}$) pins. The $\overline{XO}$ pin is connected to the $\overline{XI}$ pin of the next device, and the $\overline{XO}$ pin of the last device should be connected to the $\overline{XI}$ pin of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS}.

5

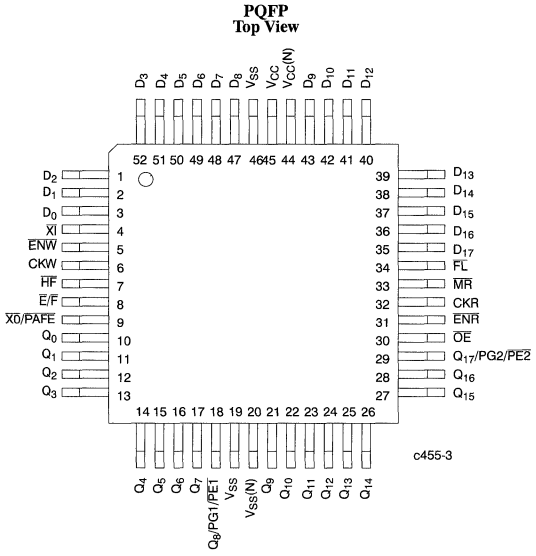
Logic Block Diagram



Pin Configuration



Pin Configurations (continued)



Functional Description (continued)

The CY7C455, CY7C456, and CY7C457 provide three status pins. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag ($\overline{\text{PAFE}}$) shares the $\overline{\text{XO}}$ pin on the CY7C455, CY7C456, and CY7C457. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{\text{XO}}$) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time. This time is typically equal to approximately one cycle time.

The CY7C45X uses center power and ground for reduced noise. All configurations are fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings and a substrate bias generator.

Selection Guide

		7C45X–14	7C45X–20	7C45X–30
Maximum Frequency (MHz)		71.4[1]	50	33.3
Maximum Cascadable Frequency		N/A	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		5	7	9
Minimum Data or Enable Hold (ns)		1	1	1
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	160	140	120
	Industrial	180	160	140

	CY7C455	CY7C456	CY7C457
Density	512 x 18	1,024 x 18	2,048 x 18
$\overline{\text{OE}}$, Depth Cascadable	Yes	Yes	Yes
Package	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP

Note:
1. 71.4-MHz operation is available only in the standalone configuration.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%

Pin Definitions

Signal Name	I/O	Description
D_{0-17}	I	Data Inputs: When the FIFO is not full and $\overline{ENW}$ is active, CKW (rising edge) writes data (D_{0-17}) into the FIFO's memory. If $\overline{MR}$ is asserted at the rising edge of CKW, data is written into the FIFO's programming register. $D_{8,17}$ are ignored if the device is configured for parity generation.
Q_{0-7} Q_{9-16}	O	Data Outputs: When the FIFO is not empty and $\overline{ENR}$ is active, CKR (rising edge) reads data (Q_{0-7}, Q_{9-16}) out of the FIFO's memory. If $\overline{MR}$ is active at the rising edge of CKR, data is read from the programming register.
Q_8/PG1/$\overline{PE1}$ Q_{17}/PG2/$\overline{PE2}$	O	Function varies according to mode: Parity disabled − same function as Q_{0-7} and Q_{9-16} Parity enabled, generation − parity generation bit (PG_x) Parity enabled, check − Parity Error Flag ($\overline{PE_x}$)
$\overline{ENW}$	I	Enable Write: Enables the CKW input (for both non-program and program modes).
$\overline{ENR}$	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when $\overline{ENW}$ is LOW; updates Half Full, Almost Full, and Full flag states. When $\overline{MR}$ is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when $\overline{ENR}$ is LOW; updates the Empty and Almost Empty flag states. When $\overline{MR}$ is asserted, CKR reads data out of the program register.
$\overline{HF}$	O	Half Full Flag: Synchronized to CKW.
$\overline{E}/\overline{F}$	O	Empty or Full Flag: $\overline{E}$ is synchronized to CKR; $\overline{F}$ is synchronized to CKW.
$\overline{PAFE}/\overline{XO}$	O	Dual-Mode Pin: Not Cascaded − programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded − expansion out signal, connected to $\overline{XI}$ of next device.
$\overline{XI}$	I	Expansion-In Pin: Not Cascaded − $\overline{XI}$ is tied to V_{SS}. Cascaded − expansion Input, connected to $\overline{XO}$ of previous device.
$\overline{FL}$	I	First Load Pin: Cascaded − the first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC} (*Figure 1*). Not Cascaded − tied to V_{CC}.
$\overline{MR}$	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and $\overline{PAFE}$ active at 16 or less locations from Full/Empty. Programming Mode: Data present on D_{0-8} is written into the programmable register on the rising edge of CKW. Program register contents appear on Q_{0-8} after the rising edge of CKR.
$\overline{OE}$	I	Output Enable for Q_{0-7}, Q_{9-16}, Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$ pins.

Note:
2. T_A is the "instant on" case temperature.

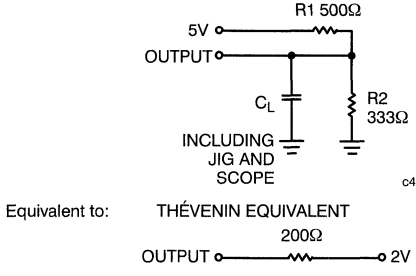
Electrical Characteristics Over the Operating Range[3]

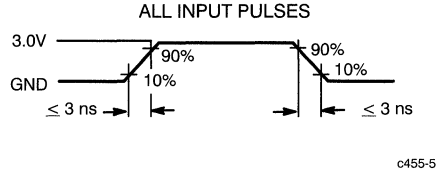
Parameter	Description	Test Conditions		7C45X–14 Min.	7C45X–14 Max.	7C45X–20 Min.	7C45X–20 Max.	7C45X–30 Min.	7C45X–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}[4]	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}[4]	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		−10	+10	−10	+10	−10	+10	μA
I_{OS}[5]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−90		−90		−90		mA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		−10	+10	−10	+10	−10	+10	μA
I_{CC1}[6]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		160		140		120	mA
			Ind		180		160		140	mA
I_{CC2}[7]	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		90		90	mA
			Ind		100		100		100	mA
I_{SB}[8]	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		40		40		40	mA
			Ind		40		40		40	mA

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms[10, 11, 12, 13, 14]





Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.
5. Test no more than one output at a time for not more than one second.
6. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$. Outputs are unloaded.
7. Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
8. All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
9. Tested initially and after any design or process changes that may affect these parameters.
10. C_L = 30 pF for all AC parameters except for t_{OHZ}.
11. C_L = 5 pF for t_{OHZ}.
12. All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
13. t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
14. t_{OHZ} is measured at +500 mV from V_{OL} and − 500 mV from V_{OH}.

Switching Characteristics Over the Operating Range[3, 15]

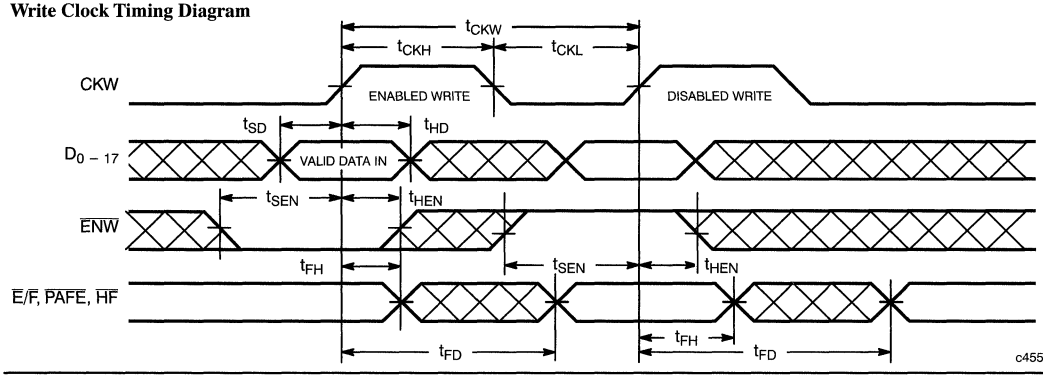
Parameter	Description	7C45X–14		7C45X–20		7C45X–30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CKW}	Write Clock Cycle	14		20		30		ns
t_{CKR}	Read Clock Cycle	14		20		30		ns
t_{CKH}	Clock HIGH	6.5		9		12		ns
t_{CKL}	Clock LOW	6.5		9		12		ns
t_A	Data Access Time		10		15		20	ns
t_{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t_{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t_{SD}	Data Set-Up	5		7		9		ns
t_{HD}	Data Hold	1		1		1		ns
t_{SEN}	Enable Set-Up	5		7		9		ns
t_{HEN}	Enable Hold	1		1		1		ns
t_{OE}	$\overline{OE}$ LOW to Output Data Valid		10		15		20	ns
t_{OLZ}[9, 16]	$\overline{OE}$ LOW to Output Data in Low Z	0		0		0		ns
t_{OHZ}[9, 16]	$\overline{OE}$ HIGH to Output Data in High Z		10		15		20	ns
t_{PG}	Read HIGH to Parity Generation		10		15		20	ns
t_{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t_{FD}	Flag Delay		10		15		20	ns
t_{SKEW1}[17]	Opposite Clock After Clock	0		0		0		ns
t_{SKEW2}[18]	Opposite Clock Before Clock	14		20		30		ns
t_{PMR}	Master Reset Pulse Width ($\overline{MR}$ LOW)	14		20		30		ns
t_{SCMR}	Last Valid Clock LOW Set-Up to $\overline{MR}$ LOW	0		0		0		ns
t_{OHMR}	Data Hold From $\overline{MR}$ LOW	0		0		0		ns
t_{MRR}	Master Reset Recovery ($\overline{MR}$ HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t_{MRF}	$\overline{MR}$ HIGH to Flags Valid		14		20		30	ns
t_{AMR}	$\overline{MR}$ HIGH to Data Outputs LOW		14		20		30	ns
t_{SMRP}	Program Mode—$\overline{MR}$ LOW Set-Up	14		20		30		ns
t_{HMRP}	Program Mode—$\overline{MR}$ LOW Hold	10		15		20		ns
t_{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t_{AP}	Program Mode—Data Access Time		14		20		30	ns
t_{OHP}	Program Mode—Data Hold Time from $\overline{MR}$ HIGH	0		0		0		ns

Notes:

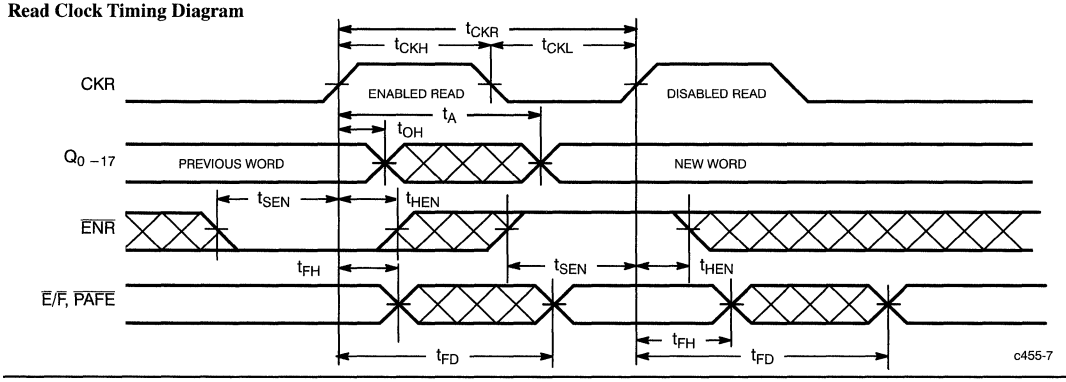
15. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 10 and 11, unless otherwise specified.
16. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
17. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. *Note*: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, and CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, and CKR is the clock for Empty and Almost Empty flags.
18. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 17 for definition of clock and opposite clock.

Switching Waveforms

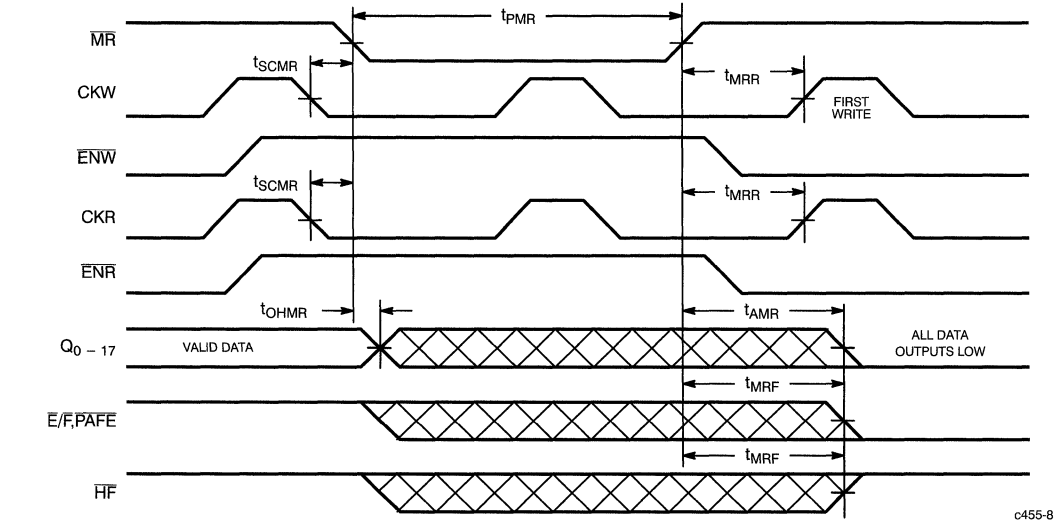
Write Clock Timing Diagram



Read Clock Timing Diagram

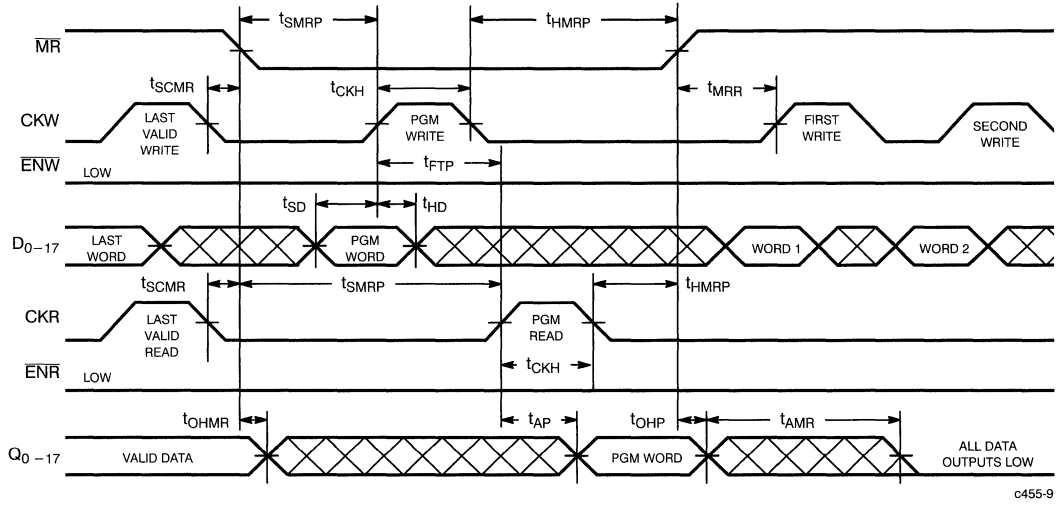


Master Reset (Default with Free-Running Clocks) Timing Diagram[19, 20, 21, 22]

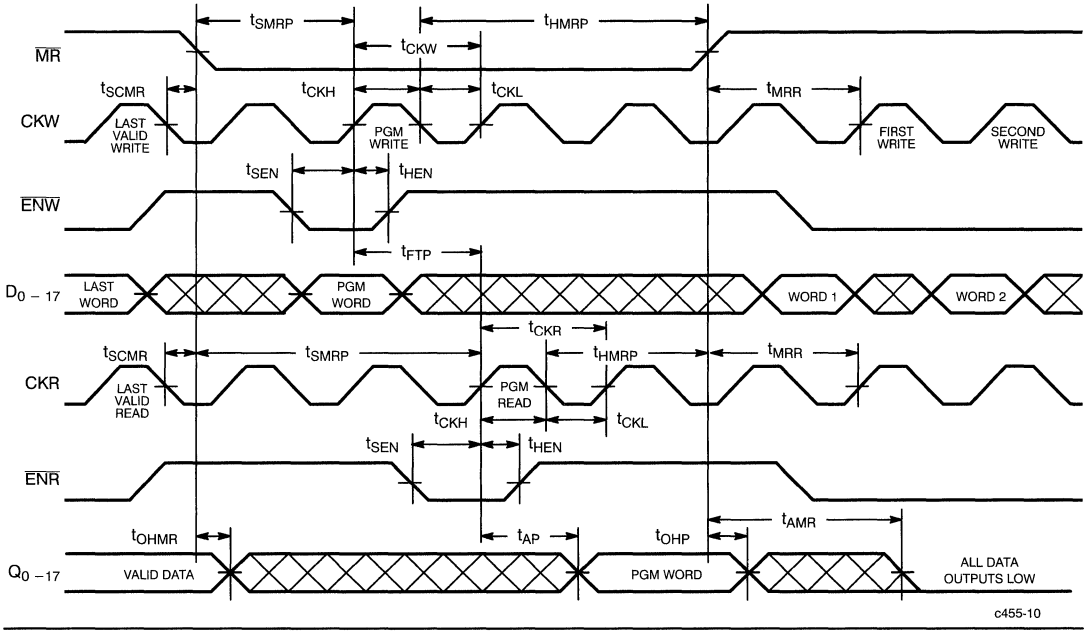


Switching Waveforms (continued)

Master Reset (Programming Mode) Timing Diagram[21, 22]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram[21, 22]

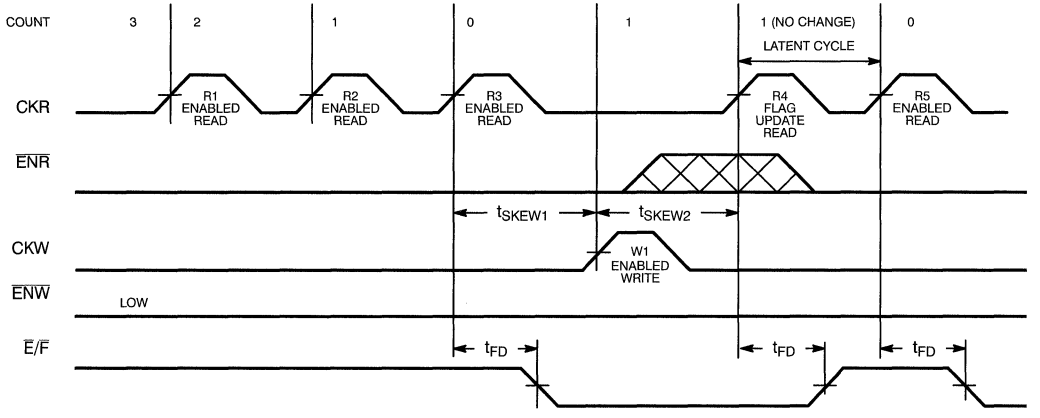


Notes:

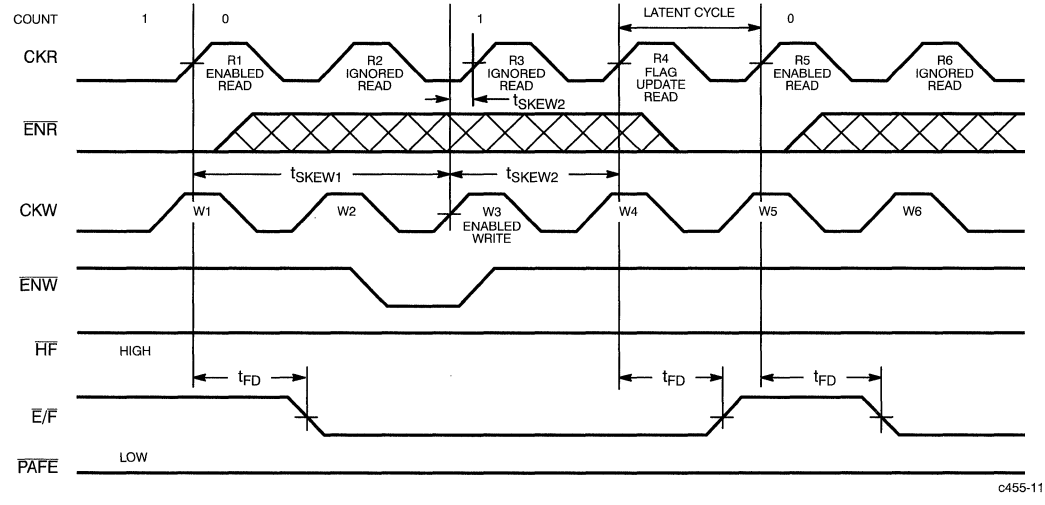
19. To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is LOW.
20. To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is LOW.
21. All data outputs (Q_{0-17}) go LOW as a result of the rising edge of $\overline{MR}$ after t_{AMR}.
22. In this example, Q_{0-17} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

Switching Waveforms (continued)

Read to Empty Timing Diagram[23, 26, 27]



Read to Empty Timing Diagram with Free-Running Clocks[23, 24, 25, 26]

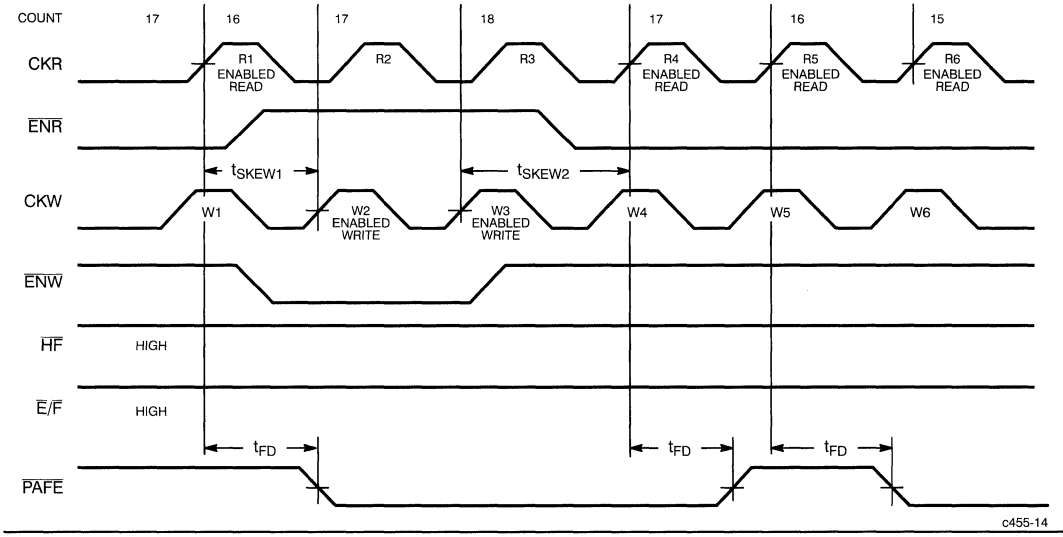


Notes:

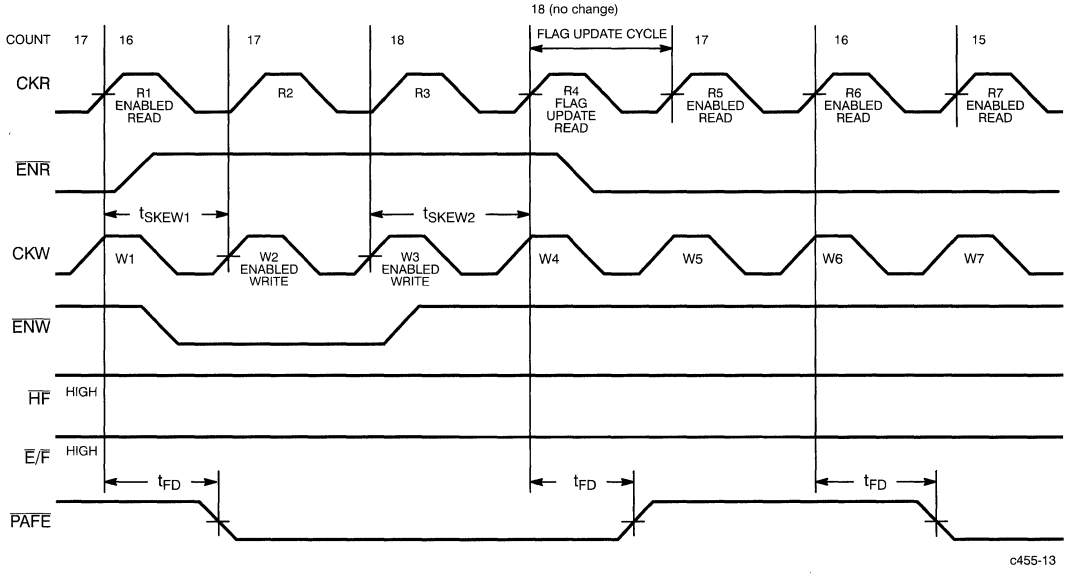
23. "Count" is the number of words in the FIFO.
24. The FIFO is assumed to be programmed with P > 0 (i.e., $\overline{PAFE}$ does not transition at Empty or Full).
25. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
26. CKR is clock and CKW is opposite clock.
27. R3 updates the flag to the Empty state by asserting $\overline{E}/\overline{F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks[23, 26, 28]



Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks[23, 26, 28, 29, 30]

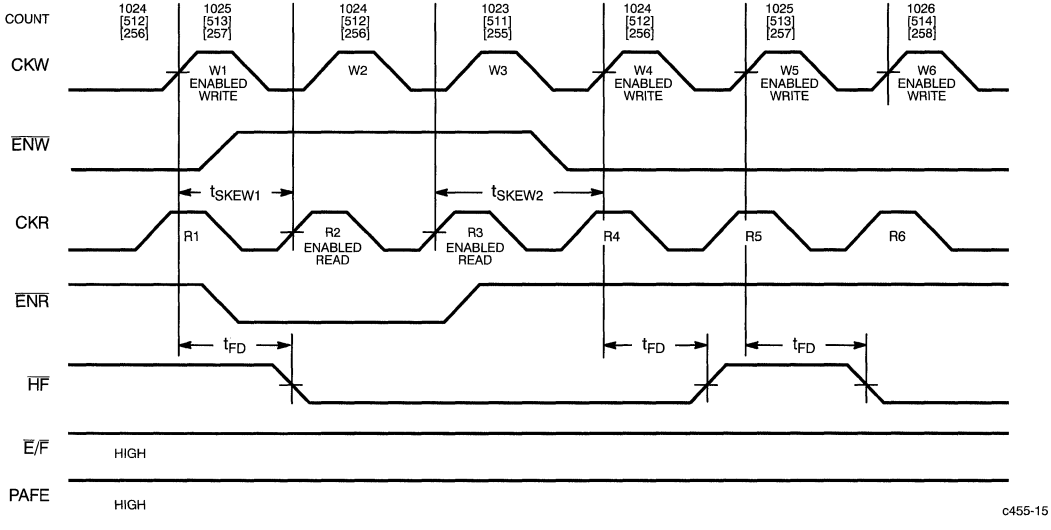


Notes:

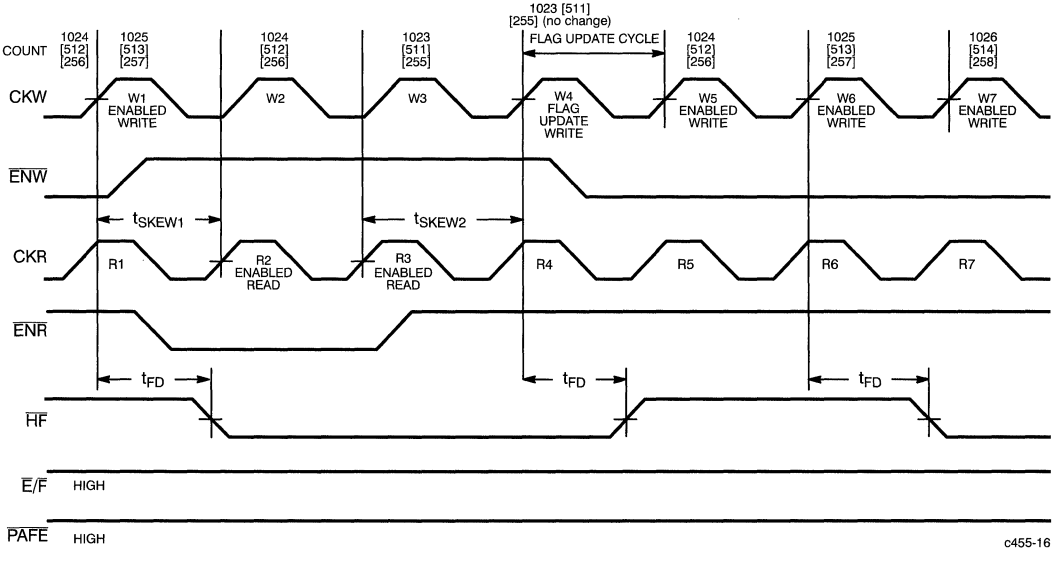
28. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
29. R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is HIGH.
30. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 ➧18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks[23, 31, 32, 33]



Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks[23, 31, 32, 33, 34, 35]

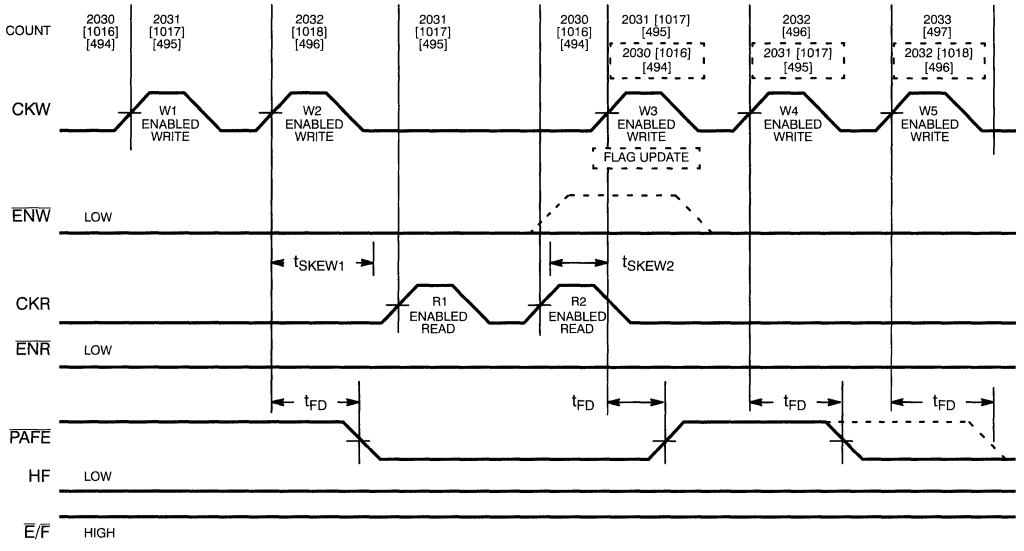


Notes:

31. CKW is clock and CKR is opposite clock.
32. Count = 1,025 indicates Half Full for the CY7C446 and CY7C456. Count = 513 indicates Half Full for the CY7C447 and CY7C457. Count = 257 indicates Half Full for the CY7C448 and CY7C458.
33. When the FIFO contains 1,024 [512] [256] words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (LOW).
34. The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is HIGH. It only updates $\overline{HF}$ to HIGH.
35. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (i.e., 1,025 ➧1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.

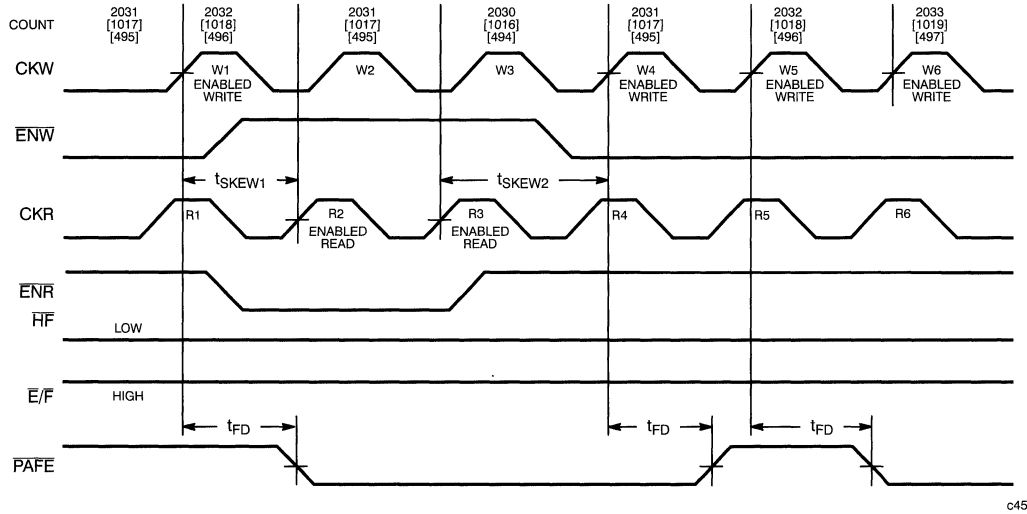
Switching Waveforms (continued)

Write to Almost Full Timing Diagram[23, 28, 31, 36, 37]



c455-18

Write to Almost Full Timing Diagram with Free-Running Clocks[23, 28, 31]



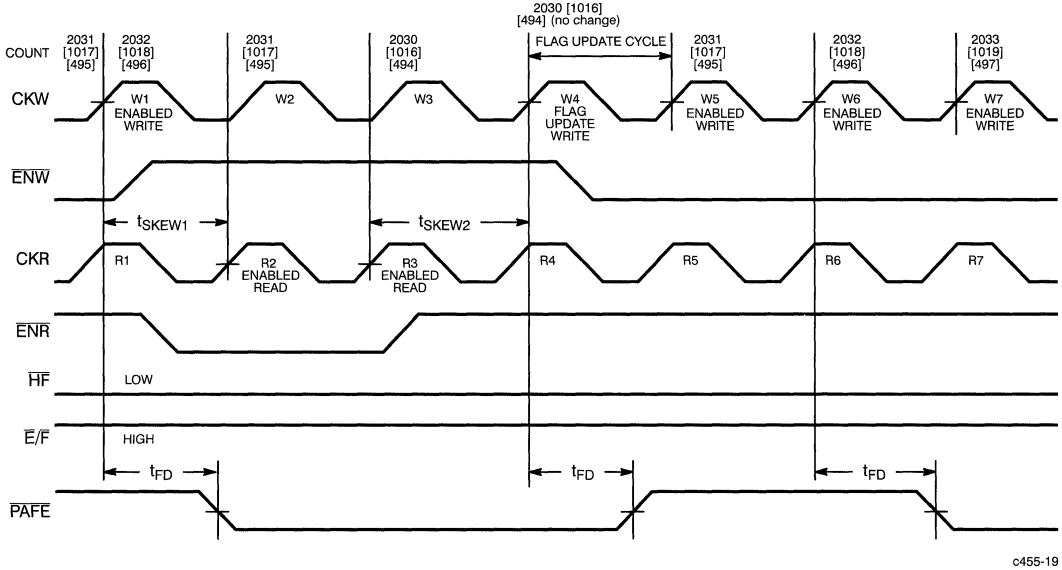
c455-17

Notes:

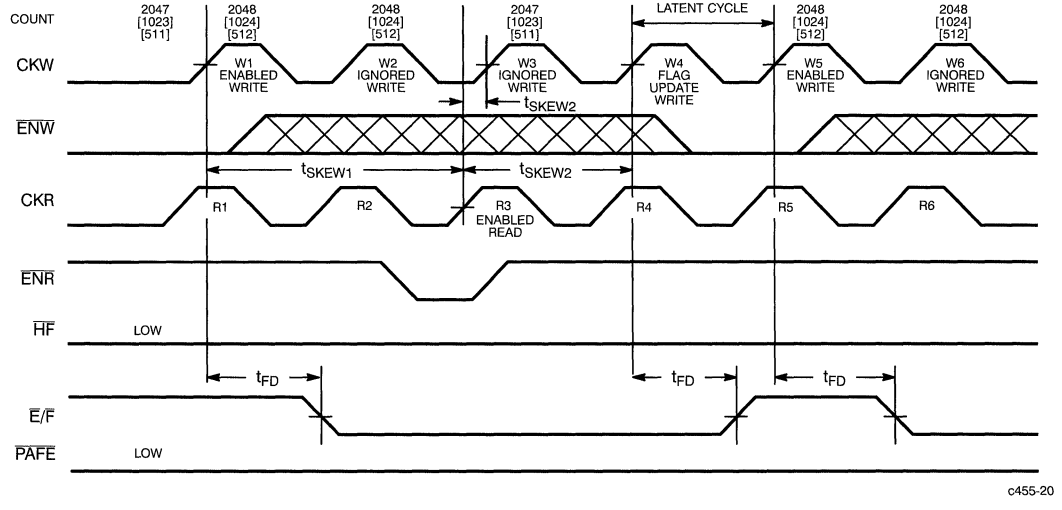
36. W2 updates the flag to the Almost Full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.
37. The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is HIGH.

Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks[23, 28, 31]



Write to Full Flag Timing Diagram with Free-Running Clocks[23, 31, 38]

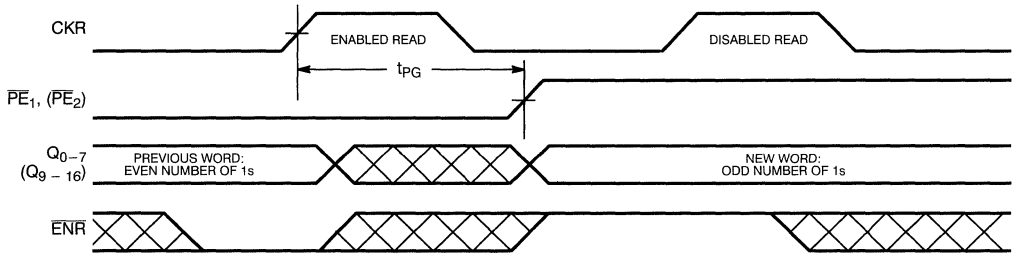


Note:

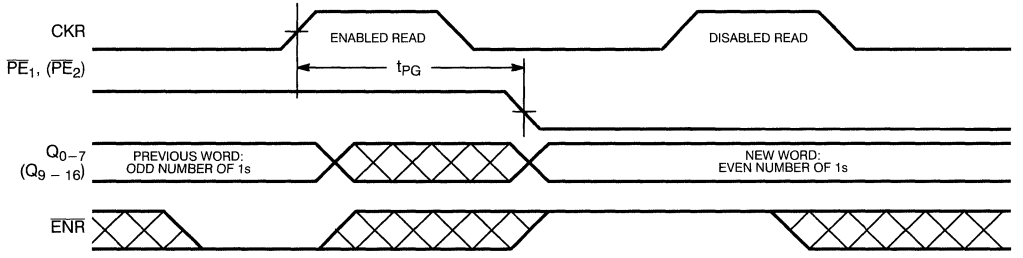
38. W2 is ignored because the FIFO is full (count = 2,048 [1,024] [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

Switching Waveforms (continued)

Even Parity Generation Timing Diagram[39, 40]



Even Parity Generation Timing Diagram[39, 41]

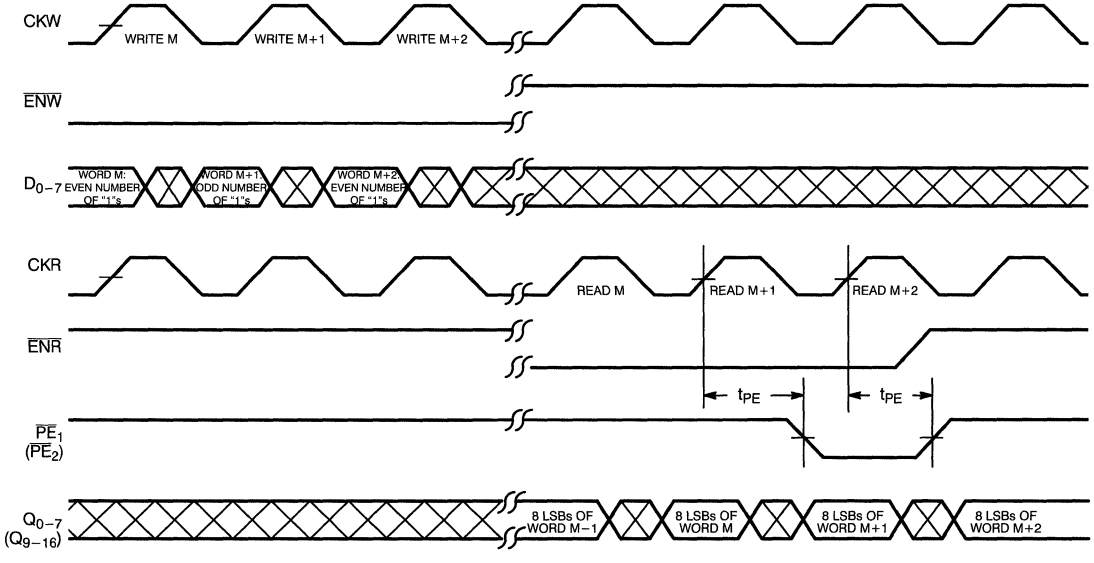


Notes:

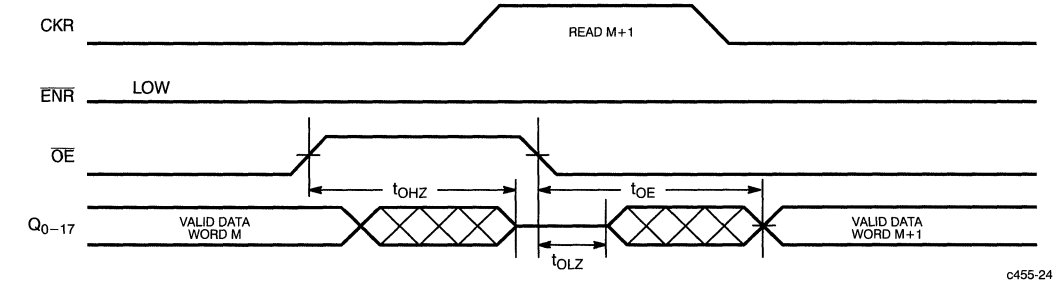
39. In this example, the FIFO is assumed to be programmed to generate even parity. The Q_{0-7} word is shown. The example is similar for the Q_{9-16} word.
40. If Q_{0-7} "new word" also has an even number of 1s, then PG1 stays LOW.
41. If Q_{0-7} "new word" also has odd number of 1s, then PG1 stays HIGH.

Switching Waveforms (continued)

Even Parity Checking[42]



Output Enable Timing[43, 44]



Notes:

42. In this example, the FIFO is assumed to be programmed to check for even parity. The Q_{0-7} word is shown.
43. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$. The Q_{0-7} word is shown.
44. If $\overline{ENR}$ was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.

Architecture

The CY7C45X consists of an array of 512, 1,024, or 2,048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, $\overline{ENR}$, $\overline{ENW}$, and $\overline{MR}$), and flags ($\overline{HF}$, $\overline{E/F}$, $\overline{PAFE}$). The CY7C45X also includes the control signals $\overline{OE}$, $\overline{FL}$, $\overline{XI}$, and $\overline{XO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{E/F}$ and $\overline{PAFE}$ being LOW and $\overline{HF}$ being HIGH. All data outputs (Q_{0-17}) go low at the rising edge of $\overline{MR}$. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{MR}$ and the user must not read or write while $\overline{MR}$ is LOW (unless $\overline{ENR}$ and/or $\overline{ENW}$ are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after $\overline{MR}$ is deasserted. All flags are guaranteed to be valid t_{MRF} after $\overline{MR}$ is taken HIGH.

FIFO Operation

When the $\overline{ENW}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the $\overline{ENR}$ signal is active, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of CKR while $\overline{ENR}$ is active. $\overline{ENR}$ must set up t_{SEN} before CKR for it to be a valid read function. $\overline{ENW}$ must occur t_{SEN} before CKW for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (low), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C45X is programmed during a master reset cycle. If $\overline{MR}$ and $\overline{ENW}$ are LOW, a rising edge on CKW will write the $D_{0-9,10 \text{ or } 11}$ inputs into the programming register[45]. $\overline{MR}$ must be set up a minimum of t_{SMRP} before the program write rising edge and held t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when $\overline{MR}$ and $\overline{ENR}$ are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after $\overline{MR}$ is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for $\overline{ENW}$ and $\overline{ENR}$.

Data present on D_{0-9} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See *Table 1* for a description of the six possible FIFO states. P in *Table 1* refers to the decimal equivalent of the binary number represented by $D_{0-7,8 \text{ or } 9}$. Programming options for the CY7C45X are listed in *Table 4*.

The programmable $\overline{PAFE}$ function on the CY7C45X is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the D_{15-17} bits. See *Table 4* for a summary of the various parity programming options. Data present on D_{15-17} during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D_{0-7} and D_{9-16} thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C45X provides three status pins when not cascaded. The three pins, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, allow decoding of six FIFO states (*Table 1*). $\overline{PAFE}$ is not available when the CY7C45X is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).[46] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock ($\overline{CKR}$). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while $\overline{ENR}$=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock

Table 1. Flag Truth Table[47]

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State	7C455 Words in FIFO	7C456 Words in FIFO	7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 ➧ P	1 ➧ P	1 ➧ P
1	1	1	Less than or Equal to Half Full	P + 1 ➧ 256	P + 1 ➧ 512	P + 1 ➧ 1024
1	1	0	Greater than Half Full	257 ➧ 511 − P	513 ➧ 1023 − P	1025 ➧ 2047 − P
1	0	0	Almost Full	512 − P ➧ 511	1024 − P ➧ 1023	2048 − P ➧ 2047
0	0	0	Full	512	1024	2048

Notes:

45. CKW will write D_{0-9} into the programming register. CKR will read D_{0-9} during a programming register read.
46. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.
47. P is the decimal value of the binary number represented by D_{0-7} for the CY7C455, D_{0-8} for the CY7C456, and D_{0-9} for the CY7C457. P = 0 signifies that the Almost Empty state = Empty state.

Flag Operation (continued)

(CKW). For example, if the CY7C457 contains 2,047 words (2,048 words indicate Full for the CY7C457), the next write (rising edge of CKW while $\overline{ENW}$=LOW) causes the flag pins to output a state that is decoded as Full.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the FIFO must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1} after or t_{SKEW2} before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read clock cycles are required to read data out of the FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the $\overline{ENR}$ state. Therefore, the update occurs even when $\overline{ENR}$ is deasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. *Table 2* shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full to Almost Full (or Full to Greater Than Half Full), a clock cycle on CKW is necessary to update the flags to the current state. In such a state (flags showing Full even through data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the $\overline{ENW}$ state. Therefore, the update occurs even when $\overline{ENW}$ is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in *Table 2*.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C45X features programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at any distance from the Empty/Full boundary. When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAFE}$ flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the $\overline{PAFE}$ will also be asserted signifying that the FIFO is Almost Full. The $\overline{HF}$ flag is decoded to distinguish the states.

The default distance from where $\overline{PAFE}$ becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin ($\overline{ENW}$ in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to $\overline{PAFE}$ and $\overline{HF}$. If the enable pin is not asserted during the flag update cycle, only the flags are updated. *Tables 3* show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

The CY7C45X also features even or odd parity checking and generation. D_{15-17} are used during a program write to describe the parity option desired. *Table 4* summarizes programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on two multi-mode output pins (Q_8/PG1/$\overline{PE1}$ and Q_{17}/PG2/$\overline{PE2}$). The three possible modes are described in the following paragraphs.

Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E}/\overline{F}$	$\overline{AFE}$	$\overline{HF}$	Number of words in FIFO	Comments
Empty	0	0	1	0	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write ($\overline{ENW}$ = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read ($\overline{ENR}$ = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read ($\overline{ENR}$ = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write ($\overline{ENR}$ = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read ($\overline{ENR}$ = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read ($\overline{ENR}$ = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Programmable Parity

Parity Disabled (Q_8/Q_{17} mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on D_{0-17} inputs internally and will output all 18 bits on Q_{0-17}.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D_{0-7} and D_{9-16}. D_8 and D_{17} inputs are ignored. The parity bits are stored internally as D_8 and D_{17}, and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated (Q_{0-7} and Q_{9-16}). For example, if parity generate is set to ODD and the D_{0-7} inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check ($\overline{PE}$ mode)

If the FIFO is programmed for parity checking, it will compare the parity of D_{0-8} and D_{9-17} with the program register. For example, D_8 and D_{17} will be set according to the result of the parity check on each word. When these words are later read, $\overline{PE}_1$ and $\overline{PE}_2$ will reflect the result of the parity check. If a parity error occurs in D_{0-8}, D_8 will be set LOW internally. When this word is later read, $\overline{PE1}$ will be LOW.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKEW2} after the first write to two width-expanded devices, A and B, device A may go Almost Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKEW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C45X can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out ($\overline{XO}$) of the first device to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. The first device has its first load pin ($\overline{FL}$) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, $\overline{ENW}$, $\overline{ENR}$, D_{0-17}, Q_{0-17}, and $\overline{MR}$ pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting $\overline{XO}$ when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q_{0-17} outputs of the first device into a high-impedance state. This occurs regardless of the state of $\overline{ENR}$ or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q_{0-17} bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q_{0-17} bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C45X is cascaded. Only the "first device" (FIFO with $\overline{FL}$=LOW) will output its program register contents on Q_{0-17} during a program read. Q_{0-17} of all other devices will remain in a high-impedance state to avoid bus contention.

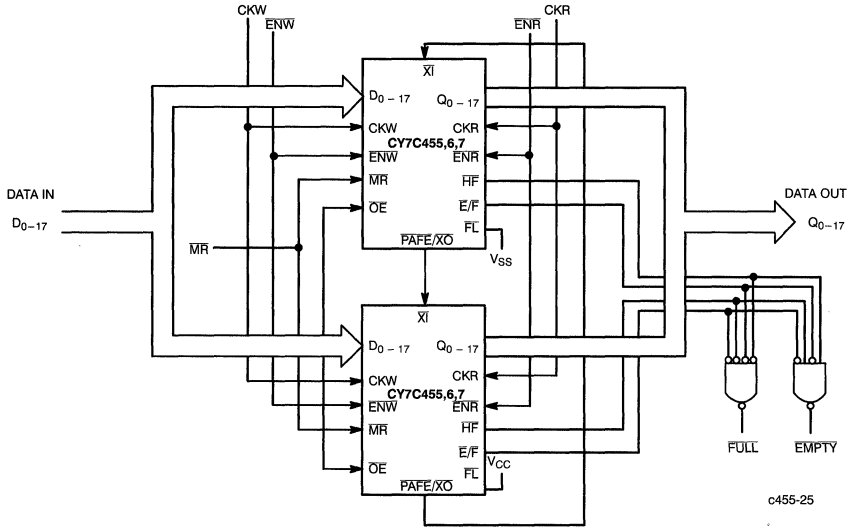


Figure 1. Depth Expansion with CY7C45X

Table 3. Almost Empty Flag (Non-Boundary Flag) Operation Example[48]

Status Before Operation						Status After Operation					
Current State of FIFO	$\overline{E/F}$	$\overline{AFE}$	$\overline{HF}$	Number of Words in FIFO	Operation	Next State of FIFO	$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	Number of words in FIFO	Comments
AE	1	0	1	32	Write ($\overline{ENW}$ = 0)	AE	1	0	1	33	Write
AE	1	0	1	33	Write ($\overline{ENW}$ = 0)	AE	1	0	1	34	Write
AE	1	0	1	34	Read ($\overline{ENR}$ = 0)	<HF	1	1	1	33	Flag Update and Read
<HF	1	1	1	33	Read ($\overline{ENR}$ = 1)	<HF	1	1	1	33	Ignored Read ($\overline{ENR}$ = 1)
<HF	1	1	1	33	Read ($\overline{ENR}$ = 0)	AE	1	0	1	32	Read (transition from <HF to AE)

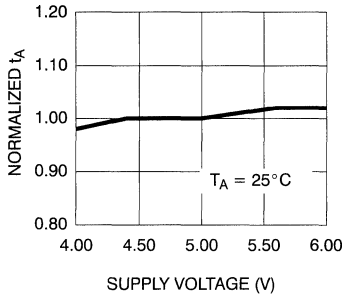
Table 4. Programmable Parity Options

D17	D16	D15	Condition
0	X	X	Parity disabled.
1	0	0	Generate even parity on PG output pin.
1	0	1	Generate odd parity on PG output pin.
1	1	0	Check for even parity. Indicate error on $\overline{PE}$ output pin.
1	1	1	Check for odd parity. Indicate error on $\overline{PE}$ output pin.

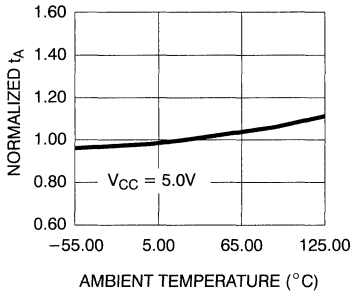
Note:
48. Applies to CY7C45X operations when devices are programmed so that Almost Empty becomes active when the FIFO contains 32 or fewer words.

Typical AC and DC Characteristics

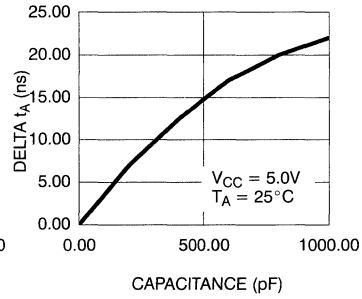
NORMALIZED t_A vs. SUPPLY VOLTAGE



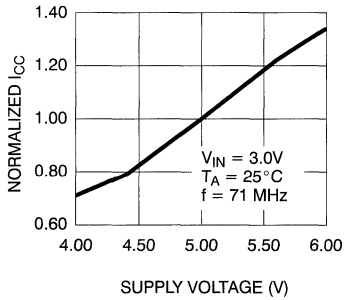
NORMALIZED t_A vs. AMBIENT TEMPERATURE



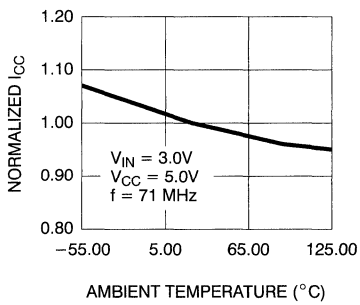
TYPICAL t_A CHANGE vs. OUTPUT LOADING



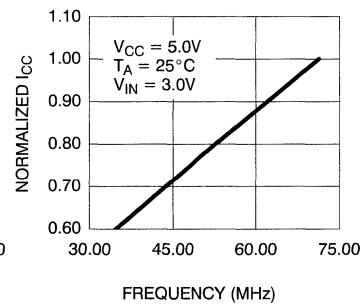
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



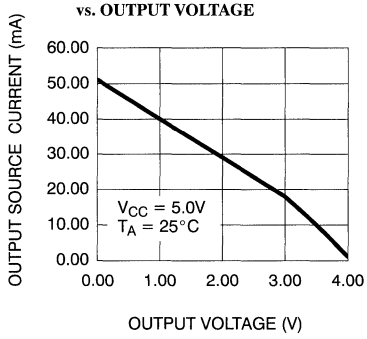
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



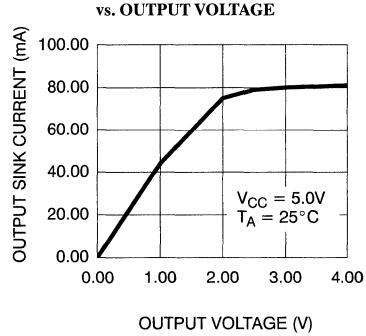
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C455–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C455–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C455–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C456–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C456–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C456–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C457–14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C457–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
30	CY7C457–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Document #: 38–00211–C

CY7C460
CY7C462
CY7C464

Cascadable 8K x 9 FIFO
Cascadable 16K x 9 FIFO
Cascadable 32K x 9 FIFO

Features

- **8K x 9 FIFO (CY7C460)**
- **16K x 9 FIFO (CY76C462)**
- **32K x 9 FIFO (CY7C464)**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  — I_{CC} = 70 mA (max.)
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **5V ± 10% supply**
- **PLCC, LCC, and 600-mil DIP packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functionally equivalent to IDT7205, IDT7206**

Functional Description

The CY7C460, CY7C462, and CY7C464 are respectively, 8K, 16K, and 32K words by 9-bit wide first-in-first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

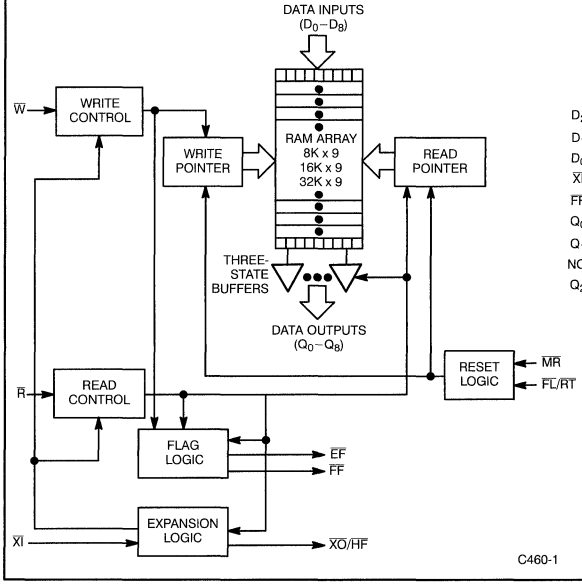
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

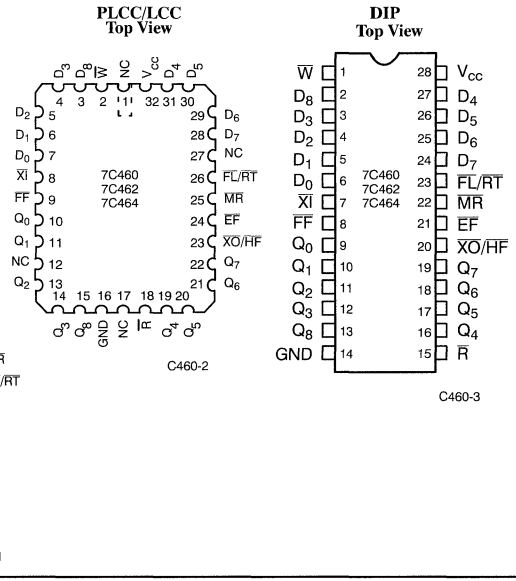
In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C460, CY7C462, and CY7C464 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C460–15 7C462–15 7C464–15	7C460–20 7C462–20 7C464–20	7C460–25 7C462–25 7C464–25	7C460–40 7C462–40 7C464–40	7C460–65 7C462–65 7C464–65
Frequency (MHz)		33.3	33.3	28.5	20	12.5
Maximum Access Time (ns)		15	20	25	40	65
Maximum Operating Current (mA)	Commercial	105		90	70	70
	Military		110	95	75	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C460–15 7C462–15 7C464–15		7C460–20 7C462–20 7C464–20		7C460–25 7C462–25 7C464–25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2				2.2		V
			Mil/Ind			2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		105				90	mA
			Mil/Ind				110		95	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20				20	mA
			Mil/Ind				25		25	
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.

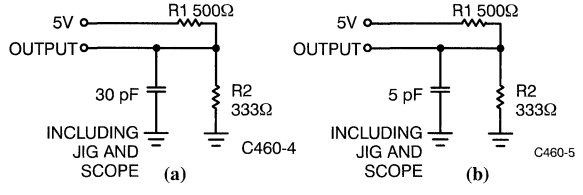
Electrical Characteristics Over the Operating Range (continued)[2]

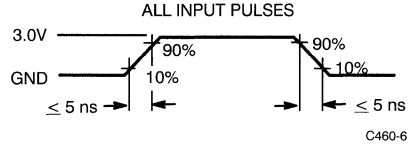
Parameter	Description	Test Conditions		7C460–40 7C462–40 7C464–40 Min.	7C460–40 7C462–40 7C464–40 Max.	7C460–65 7C462–65 7C464–65 Min.	7C460–65 7C462–65 7C464–65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2		2.2		V
			Mil/Ind	2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70	mA
			Mil/Ind		75			
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind		30		30	
I_{SB2}	Power-Down Current	All Inputs V_{CC} − 0.2V	Com'l		20		20	mA
			Mil/Ind		25		25	
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA

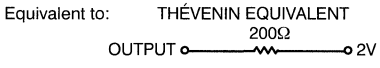
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms







Notes:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 5]

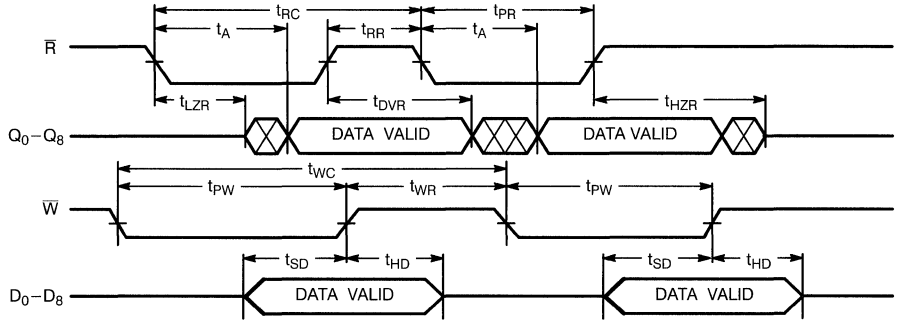
Parameter	Description	7C460–15 7C462–15 7C464–15		7C460–20 7C462–20 7C464–20		7C460–25 7C462–25 7C464–25		7C460–40 7C462–40 7C464–40		7C460–65 7C462–65 7C464–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		30		35		50		80		ns
t_A	Access Time		15		20		25		40		65	ns
t_{RR}	Read Recovery Time	15		10		10		10		15		ns
t_{PR}	Read Pulse Width	15		20		25		40		65		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		3		ns
t_{DVR}[6]	Data Valid After Read HIGH	3		3		3		3		3		ns
t_{HZR}[6]	Read HIGH to High Z		15		15		18		25		25	ns
t_{WC}	Write Cycle Time	30		30		35		50		80		ns
t_{PW}	Write Pulse Width	15		20		25		40		65		ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		5		ns
t_{WR}	Write Recovery Time	15		10		10		10		15		ns
t_{SD}	Data Set-Up Time	11		12		15		20		30		ns
t_{HD}	Data Hold Time	0		0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		30		35		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	15		20		25		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	15		10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	15		20		25		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	15		20		25		40		65		ns
t_{RTC}	Retransmit Cycle Time	30		30		35		50		80		ns
t_{PRT}	Retransmit Pulse Width	15		20		25		40		65		ns
t_{RTR}	Retransmit Recovery Time	15		10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		25		30		35		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		25		30		35		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		25		30		35		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		15		20		25		40		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		15		20		25		40		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		15		20		25		40		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		15		20		25		40		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		25		30		35		50		60	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		25		30		35		50		60	ns
t_{RAE}	Effective Read from Write HIGH		15		20		25		40		60	ns
t_{RPE}	Effective Read Pulse Width After $\overline{EF}$ HIGH	15		20		25		40		65		ns
t_{WAF}	Effective Write from Read HIGH		15		20		25		40		60	ns
t_{WPF}	Effective Write Pulse Width After $\overline{FF}$ HIGH	15		20		25		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		15		20		25		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		30		35		35		50		65	ns

Notes:

5. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load, unless otherwise specified.
6. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Load.

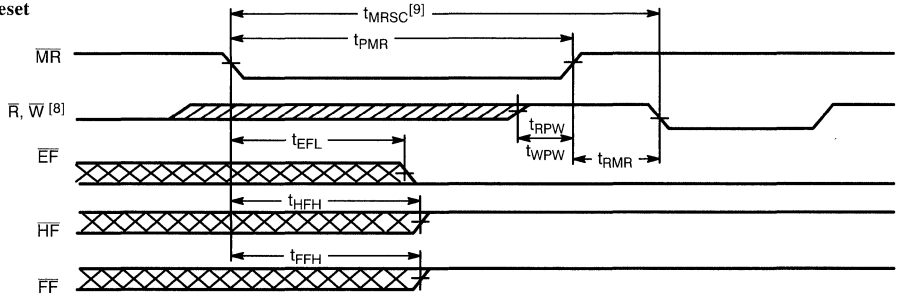
Switching Waveforms[7]

Asynchronous Read and Write



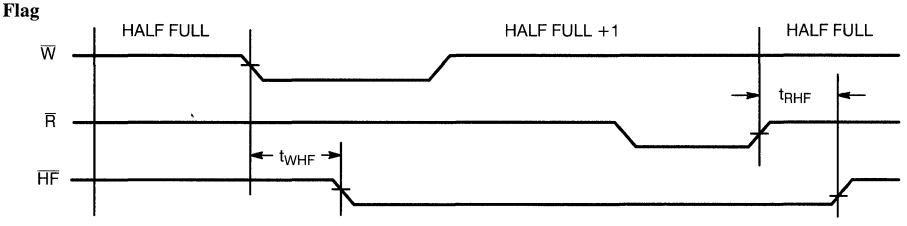
C460-7

Master Reset



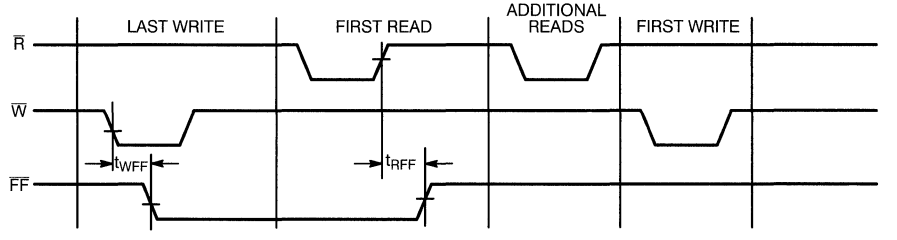
C460-8

Half Full Flag



C460-9

Last Write to First Read Full Flag



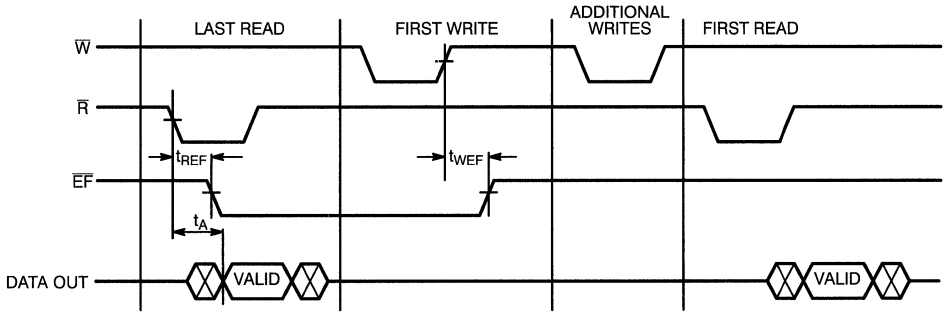
C460-10

Notes:

7. A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a LOW-to-HIGH strobe transition causes a LOW-to-HIGH flag transition.
8. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

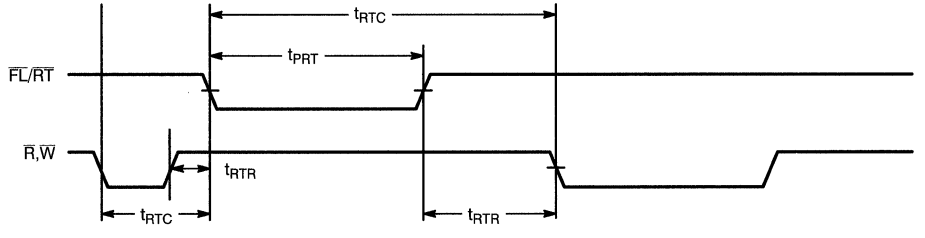
Switching Waveforms

Last READ to First WRITE Empty Flag



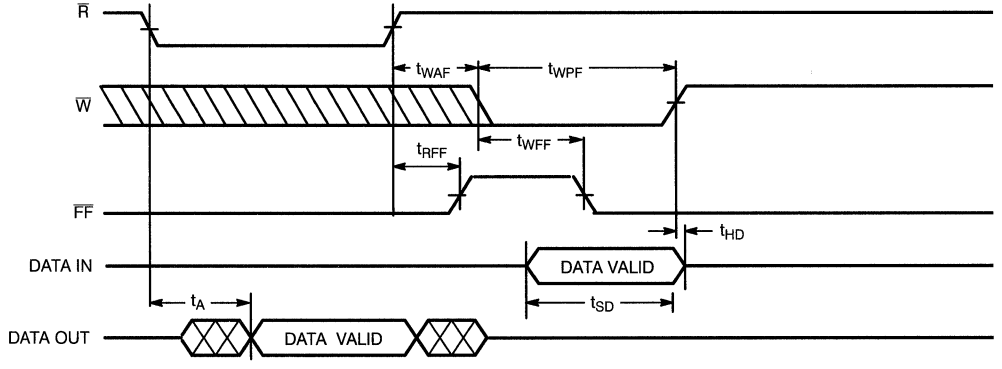
C460-11

Retransmit[10, 11]



C460-12

Full Flag and Write Data Flow-Through Mode



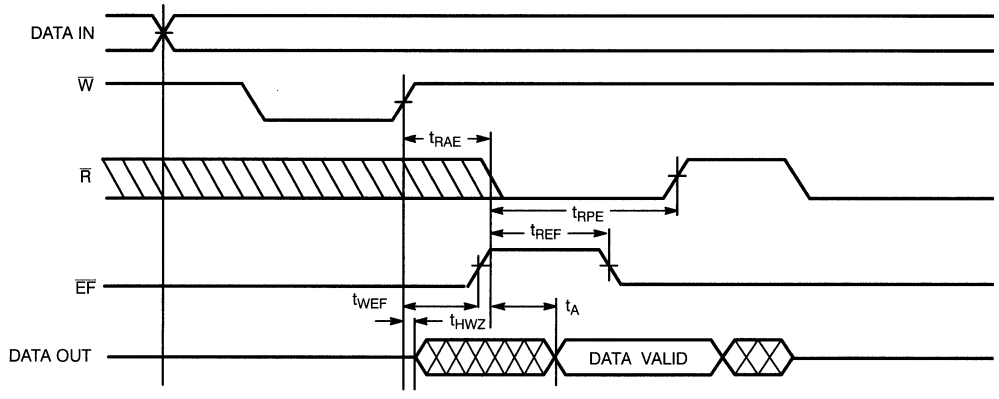
C460-13

Notes:

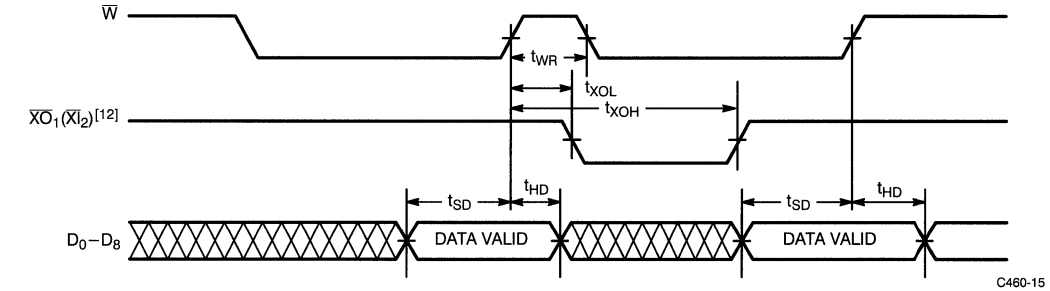
10. $t_{RTC} = t_{PRT} + t_{RTR}$.
11. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}, except for the CY7C46x–20 (Military), whose flags will be valid after t_{RTC} + 10 ns.

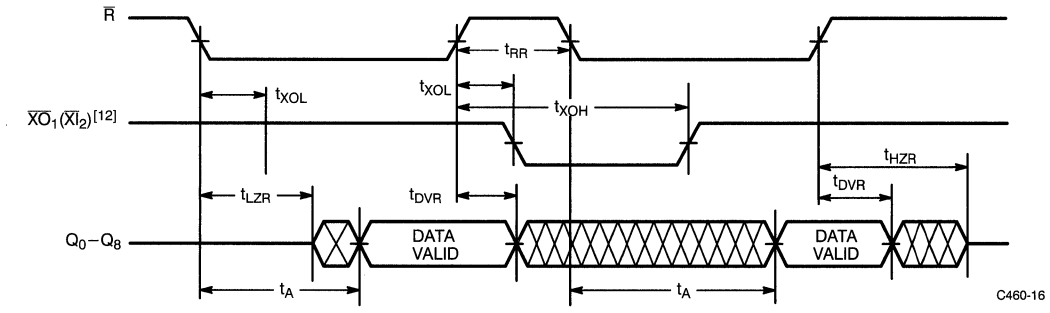
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



Expansion Timing Diagrams





Note:
12. Expansion out of device 1 ($\overline{XO_1}$) is connected to expansion in of device 2 ($\overline{XI_2}$).

CYPRESS

Architecture

Resetting the FIFO

Upon power up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$), and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs ($D_0 - D_8$) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being half full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{RFF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs ($Q_0 - Q_8$) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal-to-or-less-than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer incremented until equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding expansion in ($\overline{XI}$) and tying first load ($\overline{FL}$) to V_{CC} prior to a $\overline{MR}$ cycle. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (*see Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode, the first load ($\overline{FL}$) input, when grounded, indicates that this is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created with word widths in increments of nine. When expanding in depth, a composite $\overline{FF}$ is created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

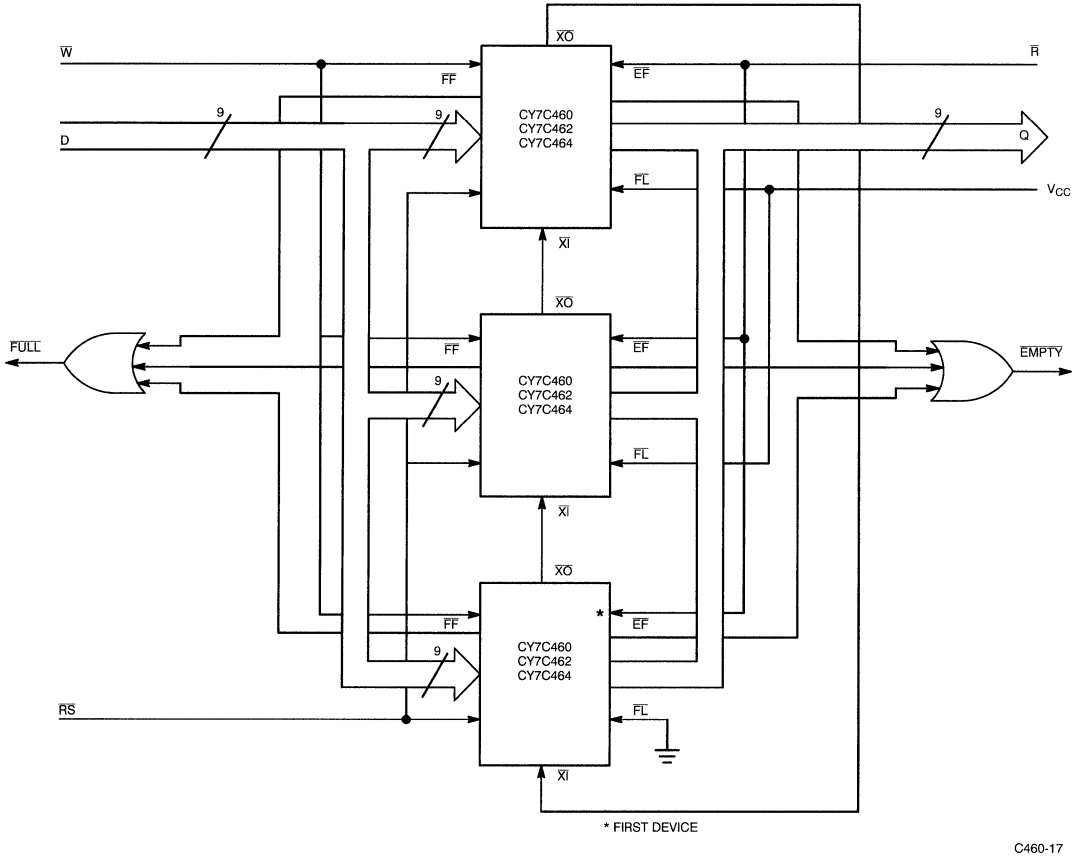
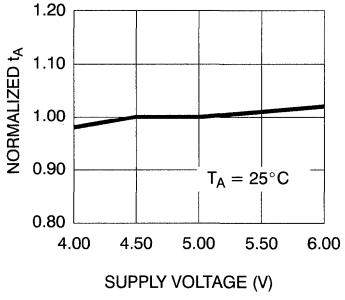


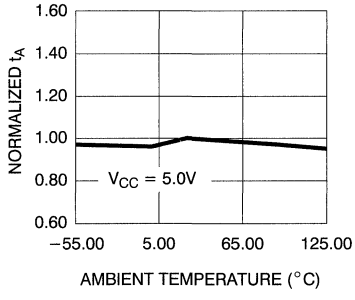
Figure 1. Depth Expansion

Typical AC and DC Characteristics

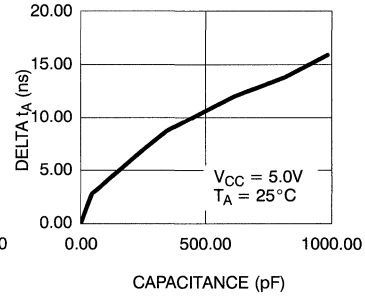
NORMALIZED t_A vs. SUPPLY VOLTAGE



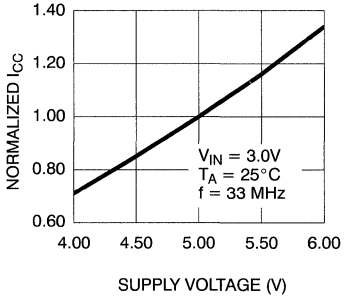
NORMALIZED t_A vs. AMBIENT TEMPERATURE



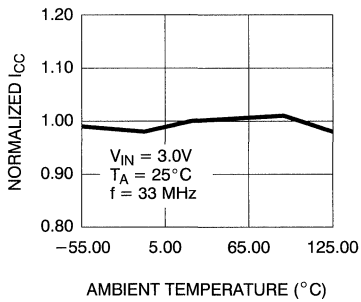
TYPICAL t_A CHANGE vs. OUTPUT LOADING



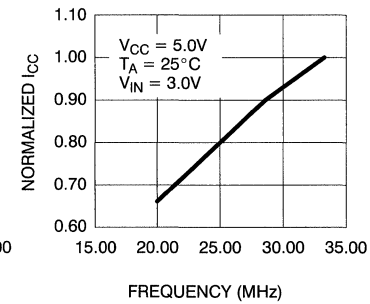
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



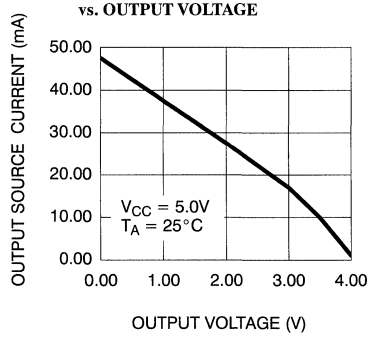
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



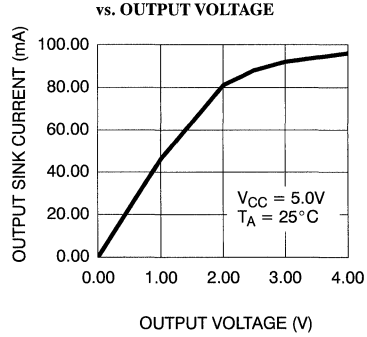
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



CYPRESS

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C460–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C460–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C460–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C460–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C460–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C460–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C460–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C460–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C460–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C462–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C462–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C462–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C462–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C462–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C462–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C462–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C462–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C462–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

CYPRESS

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C464–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C464–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C464–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C464–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C464–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C464–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C464–65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C464–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C464–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38-00141-G

CY7C470
CY7C472
CY7C474

8K x 9 FIFO, 16K x 9 FIFO, 32K x 9 FIFO with Programmable Flags

Features

- **8K x 9, 16K x 9, and 32K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 33.3-MHz read/write independent of depth/width**
- **Low operating power**
  — I_{CC} (max.) = 70 mA
- **Programmable Almost Full/Empty flag**
- **Empty, Almost Empty, Half Full, Almost Full, and Full status flags**
- **Programmable retransmit**
- **Expandable in width**
- **5V ± 10% supply**
- **TTL compatible**
- **Three-state outputs**
- **Proprietary 0.8-micron CMOS technology**

Functional Description

The CYC47X FIFO series consists of high-speed, low-power, first-in first-out (FIFO) memories with programmable flags and retransmit mark. The CY7C470, CY7C472, and CY7C474 are 8K, 16K, and 32K words by 9 bits wide, respectively. They are offered in 600-mil DIP, PLCC, and LCC packages. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Three status pins—Empty/Full ($\overline{E}/\overline{F}$), Programmable Almost Full/Empty ($\overline{PAFE}$), and Half Full ($\overline{HF}$)—are provided to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than Half Full, Greater than Half Full, Almost Full, and Full.

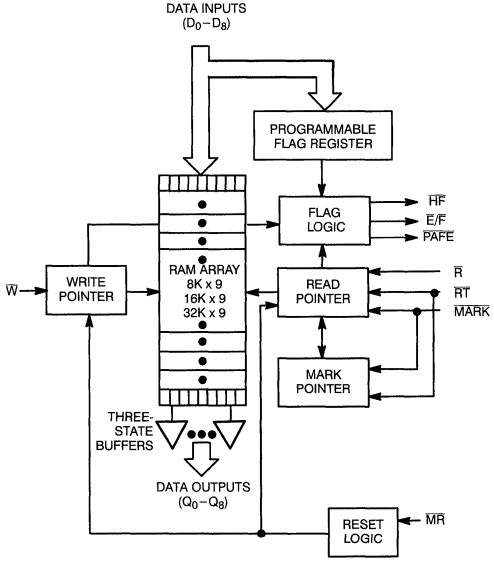
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write ($\overline{W}$) signal goes LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go into a high-impedance state when $\overline{R}$ is HIGH.

The user can store the value of the read pointer for retransmit by using the $\overline{MARK}$ pin. A LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend data by resetting the read pointer to the value stored in the mark pointer.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFO to resend the data. With the mark feature, retransmit can start from any word in the FIFO.

The CYC47X series is fabricated using a proprietary 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2001V and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.

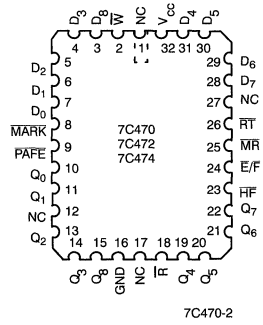
Logic Block Diagram



7C470-1

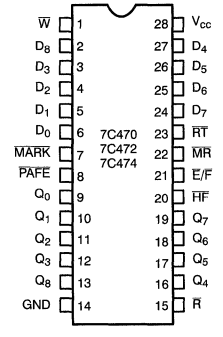
Pin Configurations

PLCC/LCC
Top View



7C470-2

DIP
Top View



7C470-3

CYPRESS

Selection Guide

		7C470–15 7C472–15 7C474–15	7C470–20 7C472–20 7C474–20	7C470–25 7C472–25 7C474–25	7C470–40 7C472–40 7C474–40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	105		90	70
	Military/Industrial		110	95	75

Maximum Ratings

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C470–15 7C472–15 7C474–15 Min.	Max.	7C470–20 7C472–20 7C474–20 Min.	Max.	7C470–25 7C472–25 7C474–25 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2				2.2		V
			Mil/Ind			2.2		2.2		
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		105				90	mA
			Mil/Ind				110		95	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25				25	mA
			Mil/Ind				30		30	
I_{SB2}	Power-Down Current	All Inputs = V_{CC} − 0.2V	Com'l		20				20	mA
			Mil/Ind				25		25	
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90	mA

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.

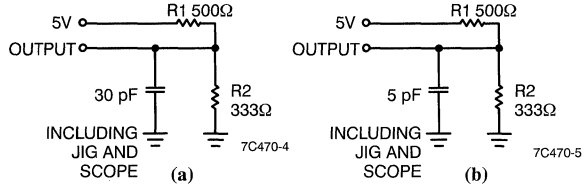
Electrical Characteristics Over the Operating Range[2] (continued)

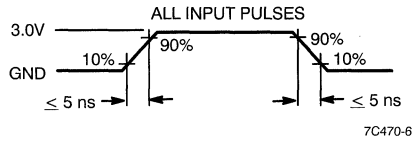
Parameter	Description	Test Conditions		7C470–40 7C472–40 7C474–40 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2		V
			Mil/Ind	2.2		
V_{IL}	Input LOW Voltage				0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R} \ge V_{IH}$, $GND \le V_O \le V_{CC}$		−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70	mA
			Mil/Ind		75	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25	mA
			Mil/Ind		30	
I_{SB2}	Power-Down Current	All Inputs = V_{CC} − 0.2V	Com'l		20	mA
			Mil/Ind		25	
I_{OS}[3]	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			−90	mA

Capacitance[4]

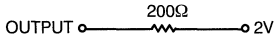
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	10	pF
C_{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5, 6]

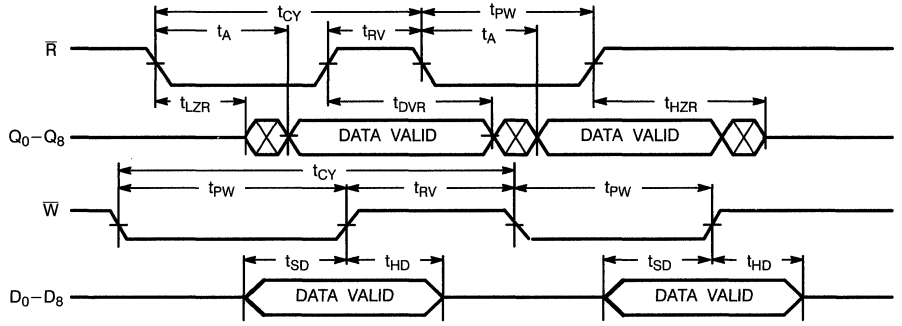
Parameter	Description	7C470–15 7C472–15 7C474–15		7C470–20 7C472–20 7C474–20		7C470–25 7C472–25 7C474–25		7C470–40 7C472–40 7C474–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	30		30		35		50		ns
t_A	Access Time		15		20		25		40	ns
t_{RV}	Recovery Time	15		10		10		10		ns
t_{PW}	Pulse Width	15		20		25		40		ns
t_{LZR}	Read LOW to Low Z	3		3		3		3		ns
t_{DV}[7]	Valid Data from Read HIGH	3		3		3		3		ns
t_{HZ}[7]	Read HIGH to High Z		15		15		18		25	ns
t_{HWZ}	Write HIGH to Low Z	5		5		5		5		ns
t_{SD}	Data Set-Up Time	11		12		15		20		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{EFD}	$\overline{E}/\overline{F}$ Delay		15		20		25		40	ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		25		30		35		50	ns
t_{HFD}	$\overline{HF}$ Delay		25		30		35		50	ns
t_{AFED}	$\overline{PAFE}$ Delay		25		30		35		50	ns
t_{RAE}	Effective Read from Write HIGH	15		20		25		40		ns
t_{WAF}	Effective Write from Read HIGH	15		20		25		40		ns

Notes:

5. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.

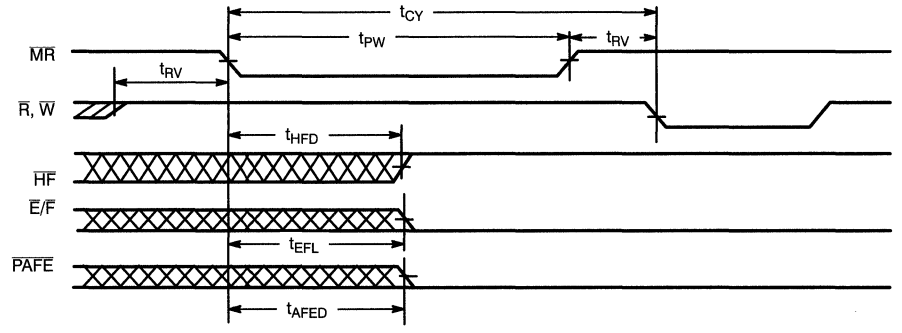
Switching Waveforms

Asynchronous Read and Write



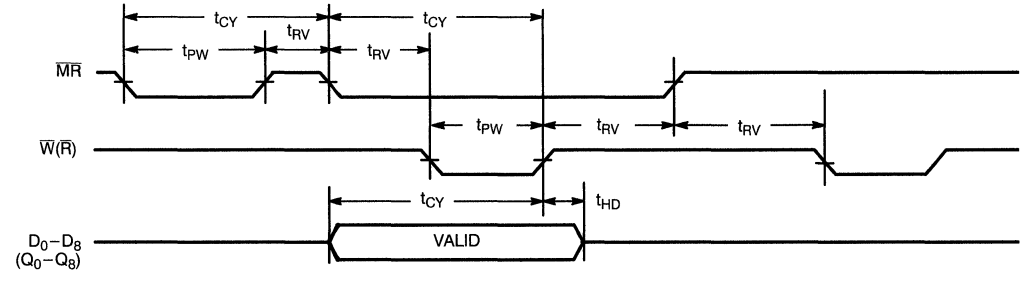
7C470-7

Master Reset (No Write to Programmable Flag Register)



7C470-8

Master Reset (Write to Programmable Flag Register)[8, 9]

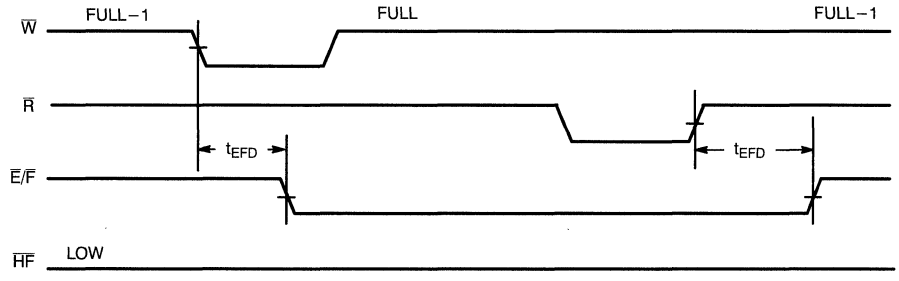


7C470-9

Note:
8. Waveform labels in parentheses pertain to writing the programmable flag register from the output port ($Q_0 - Q_8$).
9. Master Reset ($\overline{MR}$) must be pulsed LOW once prior to programming.

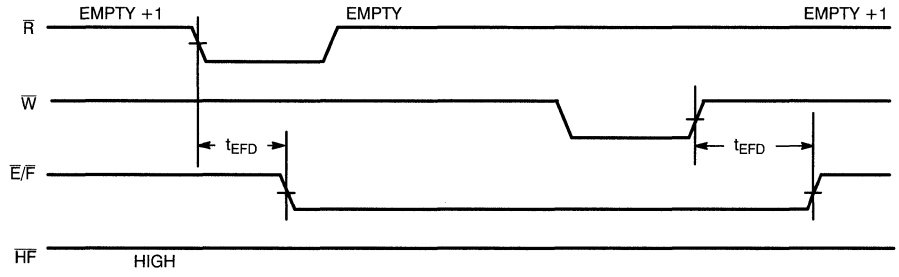
Switching Waveforms (continued)

$\overline{E}/\overline{F}$ Flag (Last Write to First Read Full Flag)



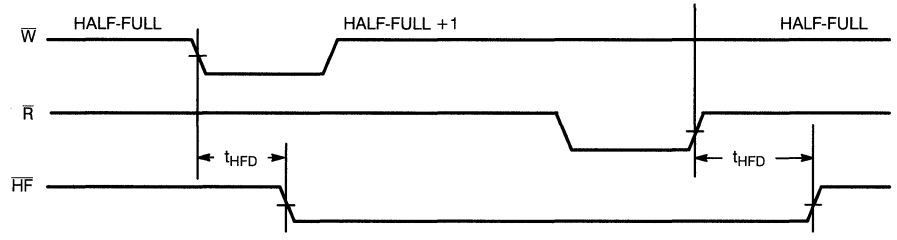
7C470-10

$\overline{E}/\overline{F}$ Flag (Last Read to First Write Empty Flag)



7C470-11

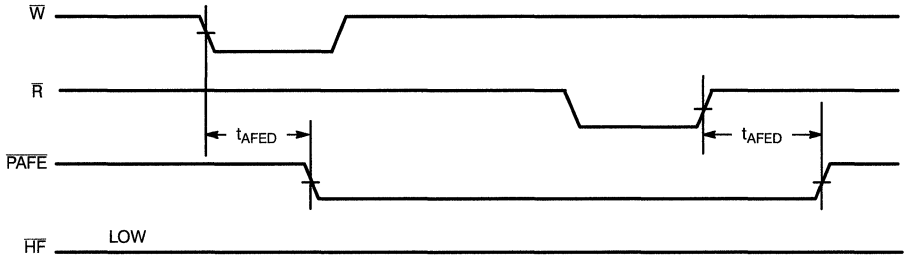
Half Full Flag



7C470-12

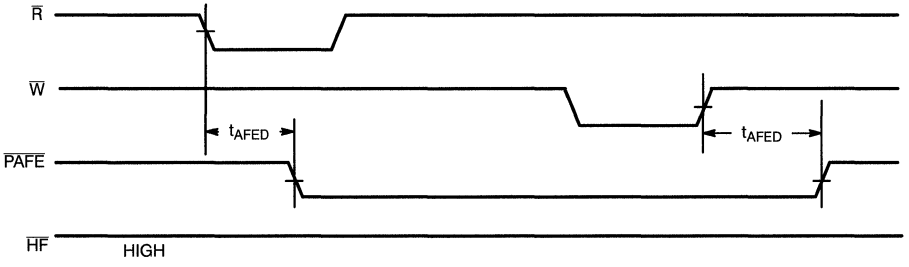
Switching Waveforms (continued)

$\overline{\text{PAFE}}$ Flag (Almost Full)



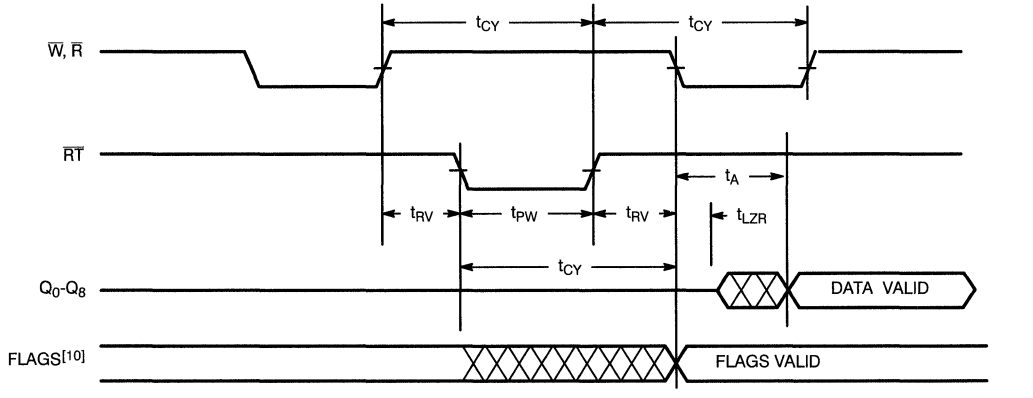
7C470-13

$\overline{\text{PAFE}}$ Flag (Almost Empty)



7C470-14

Retransmit[10]



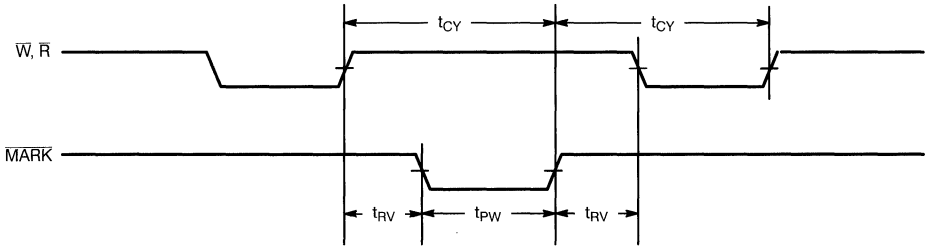
7C470-15

Notes:

10. The flags may change state during retransmit, but they will be valid a t_{CY} later, except for the CY7C47X–20 (Military), whose flags will be valid after t_{CY} + 10 ns.

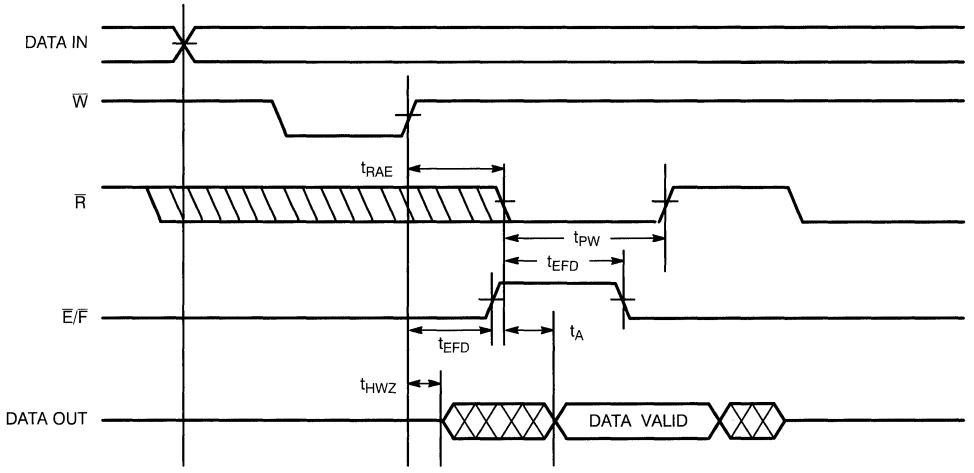
Switching Waveforms (continued)

Mark



7C470-16

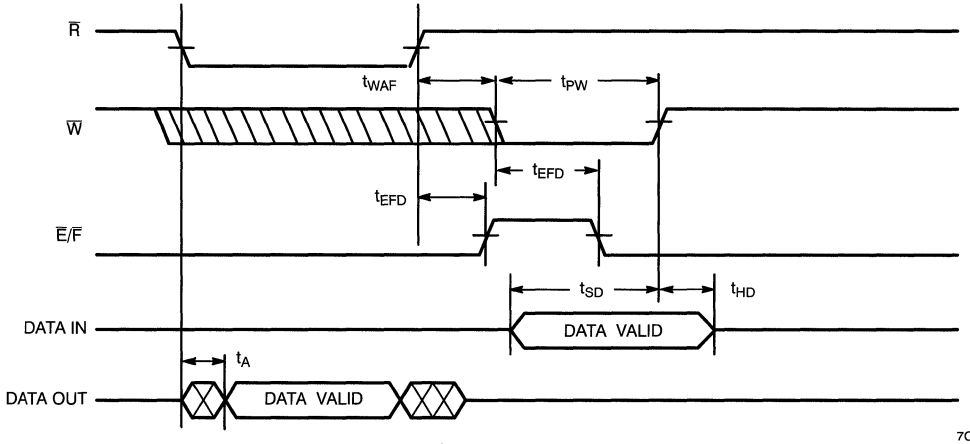
Empty Flag and Read Data Flow-Through Mode



7C470-17

Switching Waveforms (continued)

Full Flag and Write Data Flow-Through Mode



Architecture

The CY7C470, CY7C472, and CY7C474 FIFOs consist of an array of 8,192, 16,384, and 32,768 words of 9 bits each, respectively. The control consists of a read pointer, a write pointer, a retransmit pointer, control signals (i.e., write, read, mark, retransmit, and master reset), and flags (i.e., Empty/Full, Half Full, and Programmable Almost Full/Empty).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{E}/\overline{F}$) and Almost Full/Empty flag ($\overline{PAFE}$) being LOW, and Half Full flag ($\overline{HF}$) being HIGH. The read pointer, write pointer, and retransmit pointer are reset to zero. For a valid reset, Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before the falling edge and t_{RMR} after the rising edge of $\overline{MR}$.

Writing Data to the FIFO

Data can be written to the FIFO when it is not FULL[11]. A falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

Reading Data from the FIFO

Data can be read from the FIFO when it is not empty[12]. A falling edge of $\overline{R}$ initiates a read cycle. Data outputs (Q_0-Q_8) are in a high-impedance condition when the FIFO is empty and between read operations ($\overline{R}$ HIGH). The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a high-to-low transition of $\overline{E}/\overline{F}$, prohibiting any further read operations until t_{RFF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and resent if necessary. Retransmission can start from anywhere in the FIFO and be repeated without limitation.

The retransmit methodology is as follows: mark the current value of the read pointer, after an error in subsequent read operations return to that location and resume reading. This effectively resends all of the data from the mark point. When $\overline{MARK}$ is LOW, the current value of the read pointer is stored. This operation marks the beginning of the packet to be resent. When $\overline{RT}$ is LOW, the read pointer is updated with the mark location. During each subsequent read cycle, data is read and the read pointer incremented.

Care must be taken when using the retransmit feature. Use the mark function such that the write pointer does not pass the mark pointer, because further write operations will overwrite data.

Programmable Almost Full/Empty Flag

The CY7C470/2/4 offer a variable offset for the Almost Empty and the Almost Full condition. The offset is loaded into the programmable flag register (PFR) during a master reset cycle. While $\overline{MR}$ is LOW, the PFR can be loaded from Q_8-Q_0 by pulsing $\overline{R}$ LOW or from D_8-D_0 by pulsing $\overline{W}$ LOW. The offset options are listed in *Table 2*. See *Table 1* for a description of the six FIFO states. If the PFR is not loaded during master reset ($\overline{R}$ and $\overline{W}$ HIGH) the default offset will be 256 words from Full and Empty.

Notes:

11. When the FIFO is less than half full, the flags make a LOW-to-HIGH transition on the rising edge of $\overline{W}$ and make the HIGH-to-LOW transition on the falling edge of $\overline{R}$. If the FIFO is more than half full, the flags make the LOW-to-HIGH transition on the rising edge of $\overline{R}$ and HIGH-to-LOW transition on the falling edge of $\overline{W}$.
12. Full and empty states can be decoded from the Half-Full ($\overline{HF}$) and Empty/Full ($\overline{E}/\overline{F}$) flags.

Table 1. Flag Truth Table[13]

$\overline{HF}$	$\overline{E}/\overline{F}$	$\overline{PAFE}$	State	CY77C470 (8K x 9) Number of Words in FIFO	CY77C472 (16K x 9) Number of Words in FIFO	CY77C474 (32K x 9) Number of Words in FIFO
1	0	0	Empty	0	0	0
1	1	0	Almost Empty	1 ➧ (P − 1)	1 ➧ (P − 1)	1 ➧ (P − 1)
1	1	1	Less than Half Full	P ➧ 4096	P ➧ 8192	P ➧ 16384
0	1	1	Greater than Half Full	4097 ➧ (8192 − P)	8193 ➧ (16384 − P)	16385 ➧ (32768 − P)
0	1	0	Almost Full	(8192 − P+1) ➧ 8191	(16384 − P+1) ➧ 16383	(32768 − P+1) ➧ 32767
0	0	0	Full	8192	16384	32768

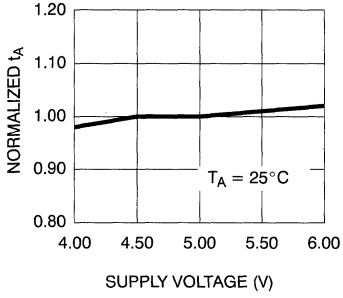
Table 2. Programmable Almost Full/Empty Options[14]

D3	D2	D1	D0	PAFE Active when:	P
0	0	0	0	256 or less locations from Empty/Full (default)	256
0	0	0	1	16 or less locations from Empty/Full	16
0	0	1	0	32 or less locations from Empty/Full	32
0	0	1	1	64 or less locations from Empty/Full	64
0	1	0	0	128 or less locations from Empty/Full	128
0	1	0	1	256 or less locations from Empty/Full (default)	256
0	1	1	0	512 or less locations from Empty/Full	512
0	1	1	1	1024 or less locations from Empty/Full	1024
1	0	0	0	2048 or less locations from Empty/Full	2048
1	0	0	1	4098 or less locations from Empty/Full[15]	4098
1	0	1	0	8192 or less locations from Empty/Full[16]	8192

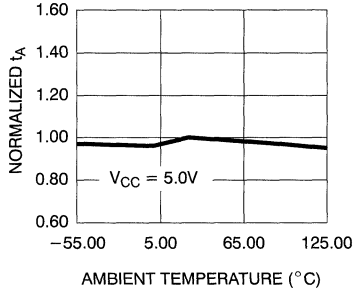
Notes:
13. See *Table 2* for P values.
14. Almost flags default to 256 locations from Empty/Full.
15. Only for CY7C472 and CY7C474.
16. Only for CY7C470.

Typical AC and DC Characteristics

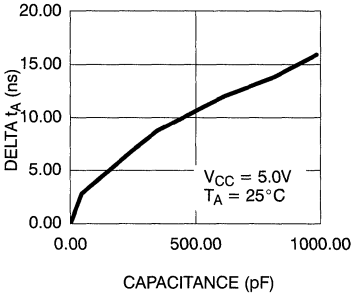
NORMALIZED t_A vs. SUPPLY VOLTAGE



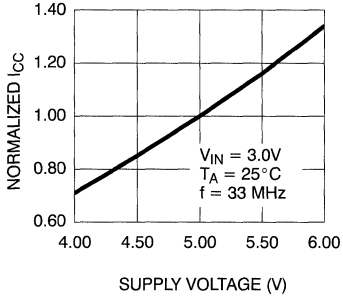
NORMALIZED t_A vs. AMBIENT TEMPERATURE



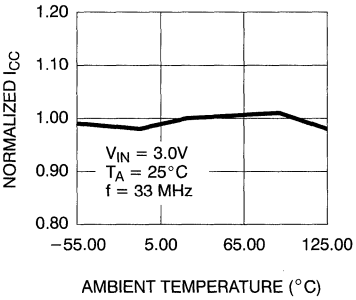
TYPICAL t_A CHANGE vs. OUTPUT LOADING



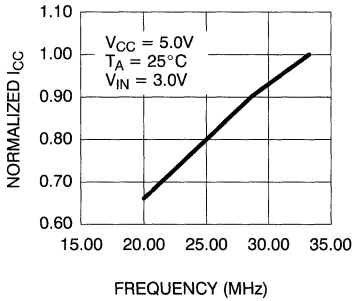
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



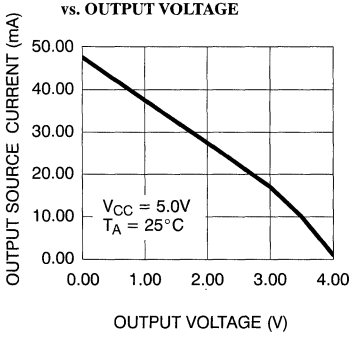
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



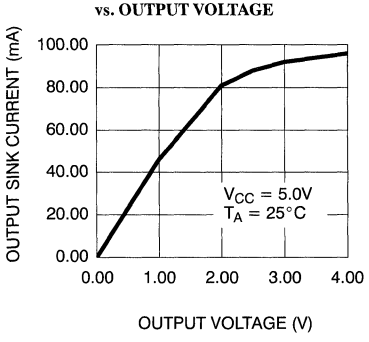
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C470–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C470–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C470–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C470–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C470–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C472–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C472–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C472–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C472–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C472–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C474–15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C474–20DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C474–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474–25DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C474–40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474–40DMB	D43	28-Lead (600-Mil) Sidebraze CerDIP	Military
	CY7C474–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{CY}	9, 10, 11
t_{A}	9, 10, 11
t_{RV}	9, 10, 11
t_{PW}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{EFD}	9, 10, 11
t_{HFD}	9, 10, 11
t_{AFED}	9, 10, 11
t_{RAE}	9, 10, 11
t_{WAF}	9, 10, 11

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Dual Ports 6

Dual Ports

CY7C130/CY7C131
CY7C140/CY7C141

1K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141**
- **$\overline{BUSY}$ output flag on CY7C130/CY7C131; $\overline{BUSY}$ input on CY7C140/CY7C141**
- **$\overline{INT}$ flag for port-to-port communication**
- **Pin compatible and functionally equivalent to IDT7130 and IDT7140**

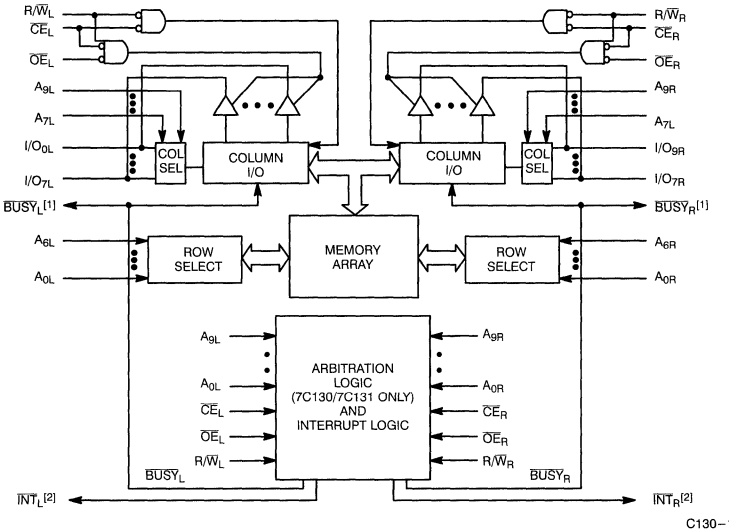
Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in 52-pin LCC, PLCC, and PQFP.

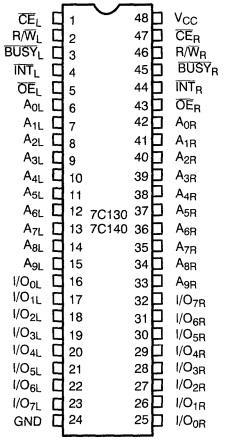
Logic Block Diagram



C130–1

Pin Configurations

DIP
Top View



C130–2

Notes:

1. CY7C130/CY7C131 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs: pull-up resistor required.

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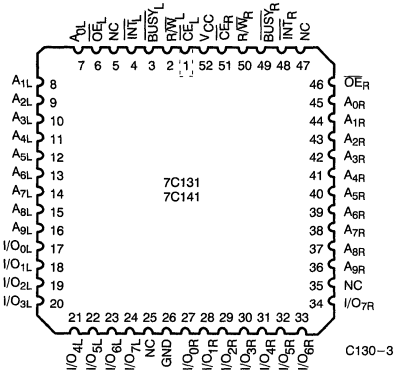
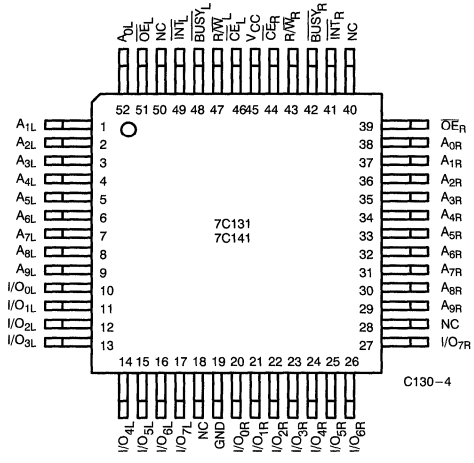
Pin Configurations (continued)

LCC/PLCC
Top View



PQFP
Top View



Selection Guide

		7C130–25[3] 7C131–25 7C140–25 7C141–25	7C130–30 7C131–30 7C140–30 7C141–30	7C130–35 7C131–35 7C140–35 7C141–35	7C130–45 7C131–45 7C140–45 7C141–45	7C130–55 7C131–55 7C140–55 7C141–55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available only in PLCC/PQFP packages.

4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C130–25, 30[3] 7C131–25, 30 7C140–25, 30 7C141–25, 30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45, 55 7C131–45, 55 7C140–45, 55 7C141–45, 55		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[7, 8]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[9]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[9]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[9]	Com'l		105		85		70	mA
			Mil				105		85	

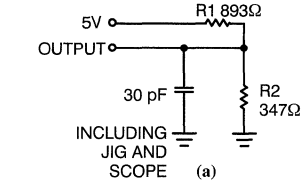
Capacitance[8]

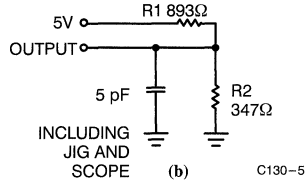
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

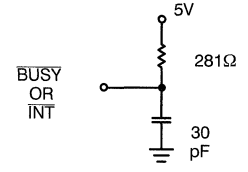
5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters.
9. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms



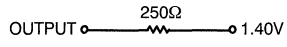


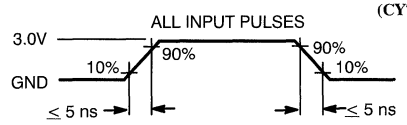
C130–5



BUSY Output Load (CY7C130/CY7C131 ONLY)

Equivalent to: THÉVENIN EQUIVALENT





C130–6

Switching Characteristics Over the Operating Range[5, 10]

Parameter	Description	7C130–25[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12, 13]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12, 13]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[13]		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[13]	0		0		0		0		0		ns

Switching Characteristics Over the Operating Range[5, 10] (continued)

Parameter	Description	7C130–25[3] 7C131–25 7C140–25 7C141–25		7C130–30 7C131–30 7C140–30 7C141–30		7C130–35 7C131–35 7C140–35 7C141–35		7C130–45 7C131–45 7C140–45 7C141–45		7C130–55 7C131–55 7C140–55 7C141–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

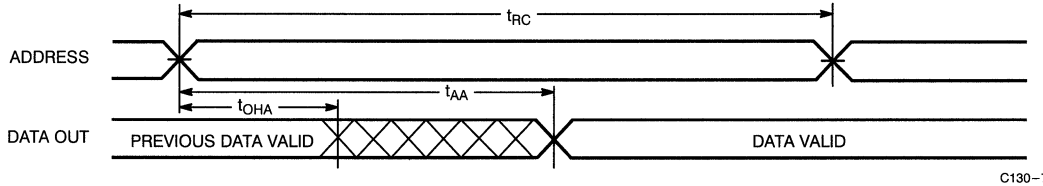
Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C140/CY7C141 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address is toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. R/$\overline{W}$ is HIGH for read cycle.
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
21. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
22. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms

Read Cycle No. 1[18, 19]

Either Port Address Access



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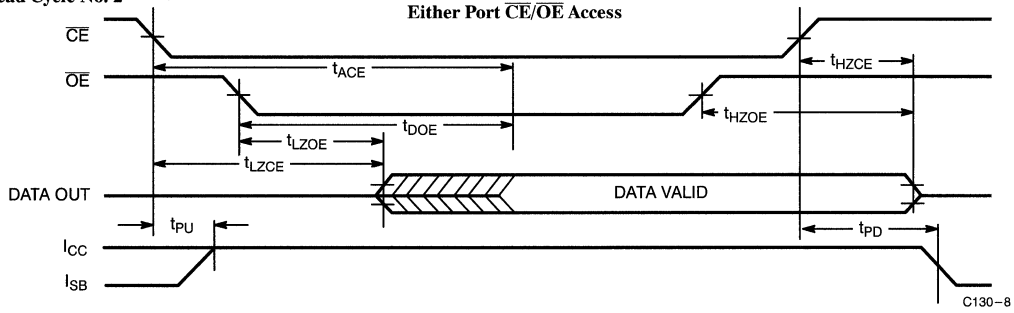
Switching Waveforms (continued)

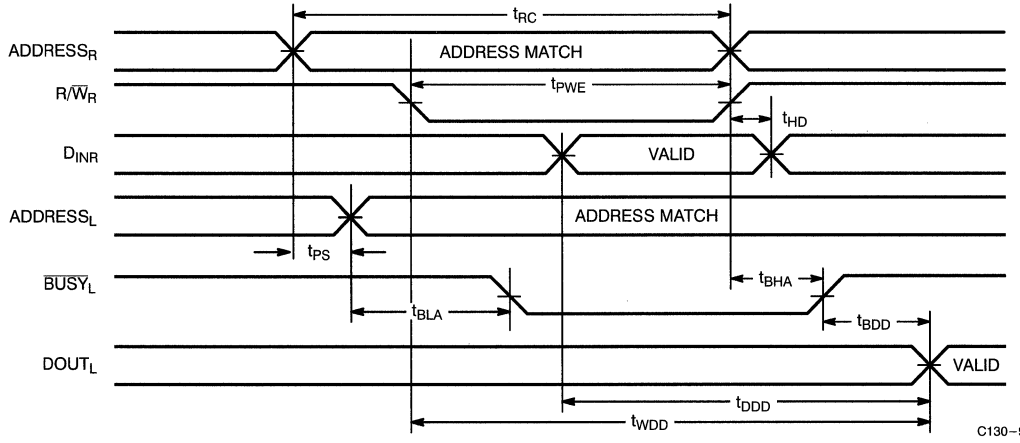
Read Cycle No. 2[18, 20]

Either Port $\overline{CE}/\overline{OE}$ Access



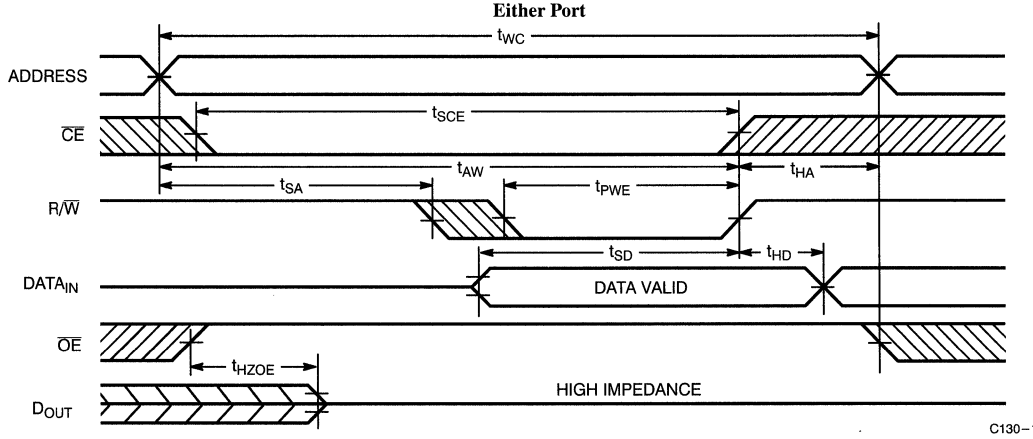
Read Cycle No. 3[19]

Read with $\overline{BUSY}$, Master: CY7C130 and CY7C131



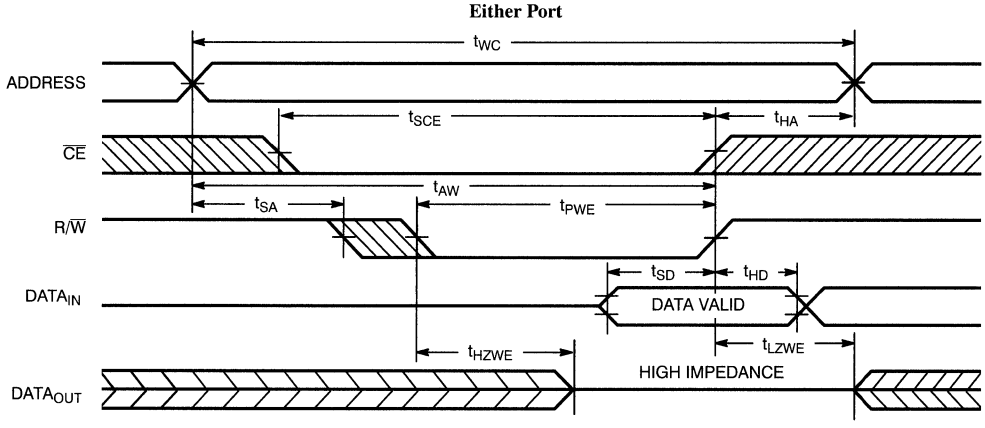
Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port)[14, 21]

Either Port



Switching Waveforms (continued)

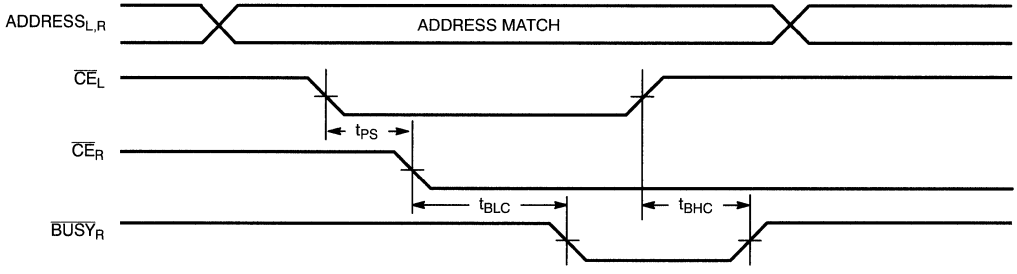
Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[15, 22]



C130–11

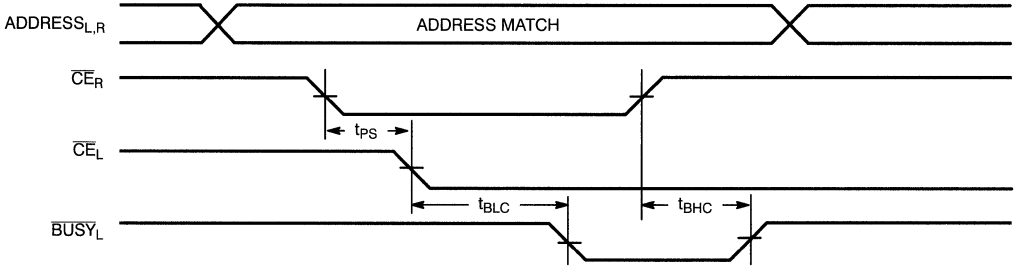
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



C130–12

$\overline{CE}_R$ Valid First:

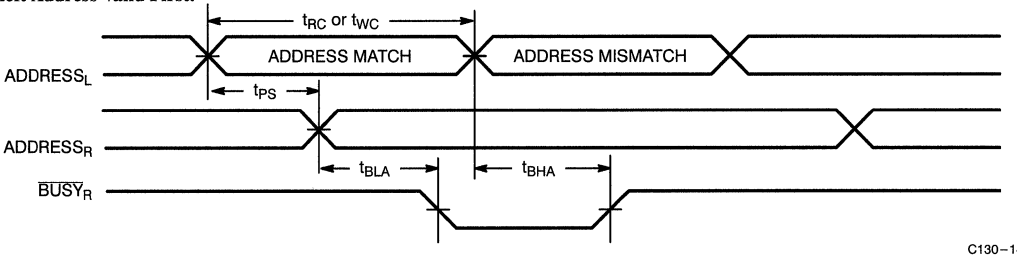


C130–13

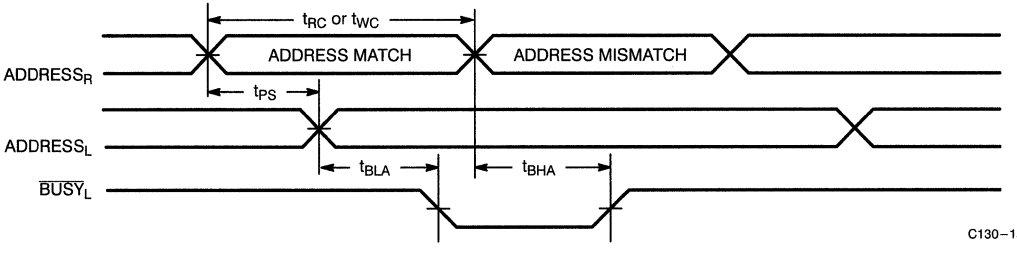
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

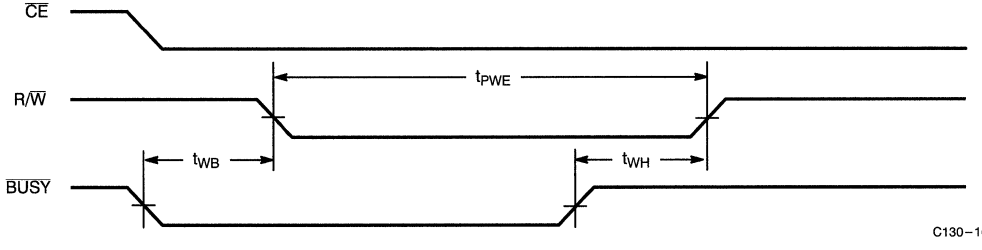


Right Address Valid First:



Busy Timing Diagram No. 3

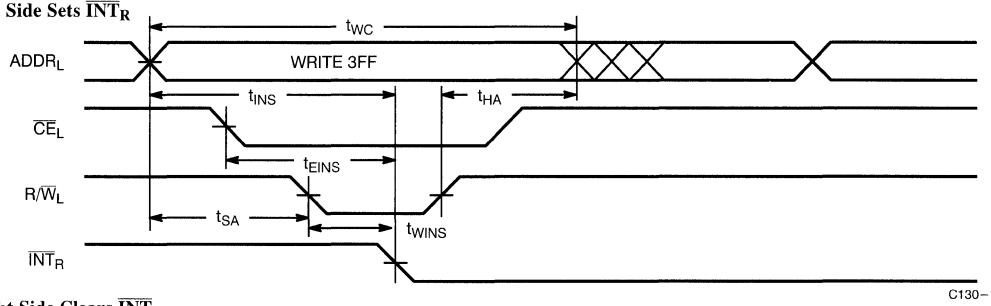
Write with $\overline{BUSY}$ (Slave: CY7C140/CY7C141)



Switching Waveforms (continued)

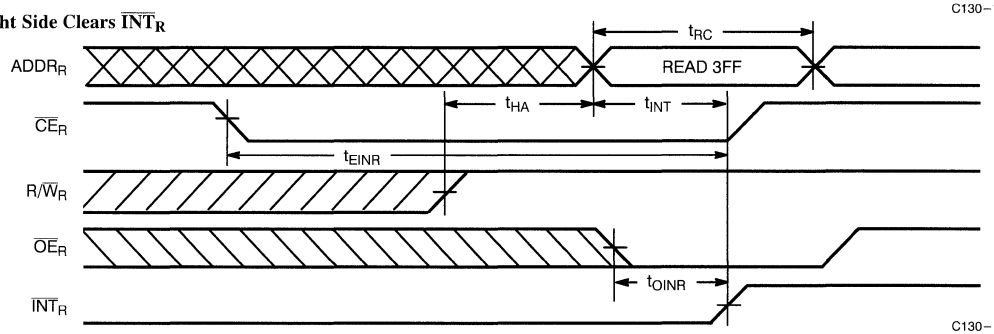
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$



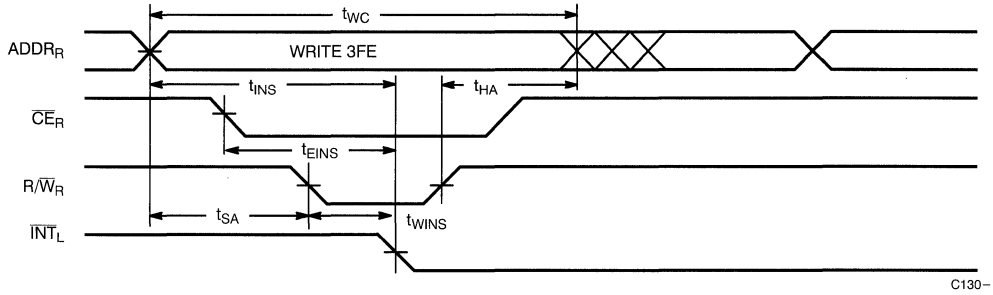
C130-17

Right Side Clears $\overline{INT}_R$



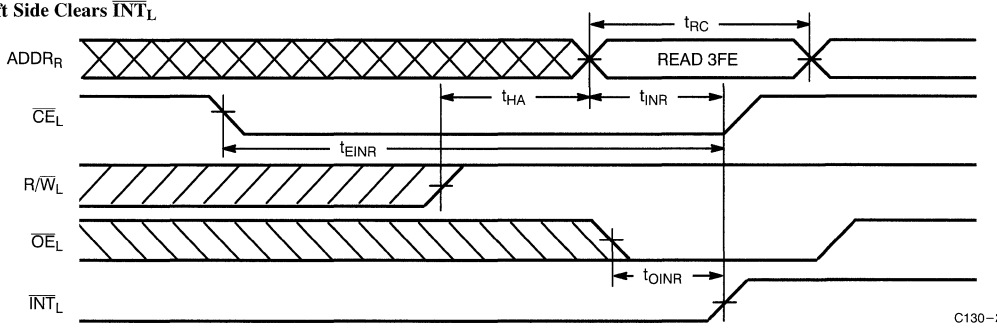
C130-18

Right Side Sets $\overline{INT}_L$



C130-19

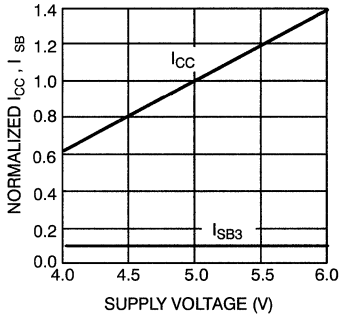
Left Side Clears $\overline{INT}_L$



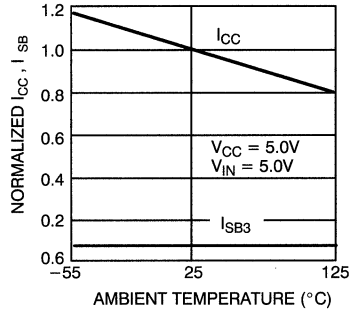
C130-20

Typical DC and AC Characteristics

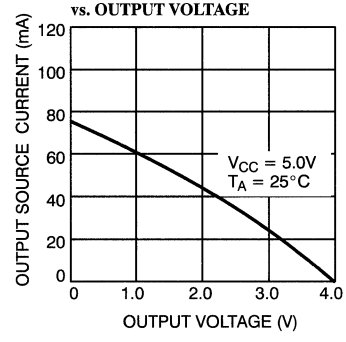
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



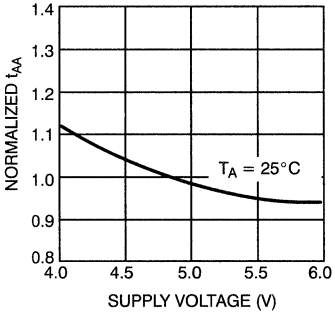
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



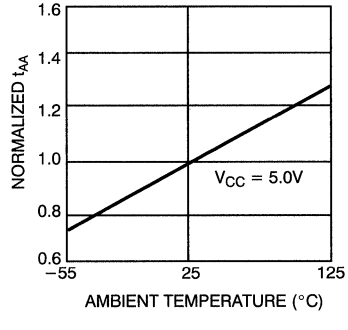
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



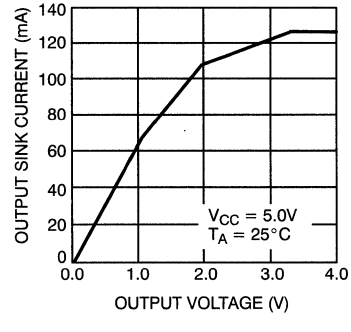
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



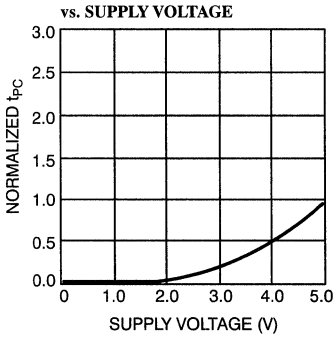
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



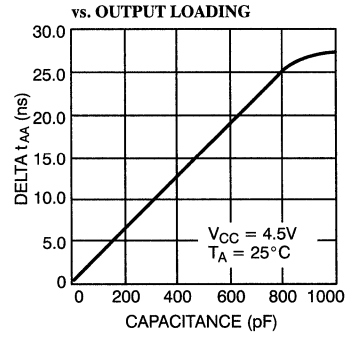
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



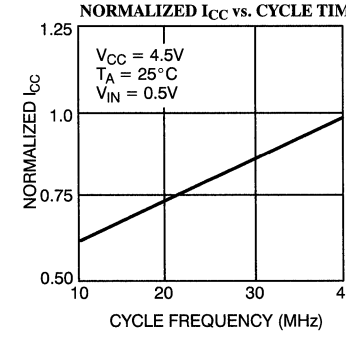
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C130–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C130–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C130–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C130–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C130–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C130–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C131–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C131–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C131–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C131–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C131–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C131–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C131–55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C131–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C140–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C140–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C140–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C140–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C140–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C140–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C141–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–25NI	N52	52-Pin Plastic Quad Flatpack	
30	CY7C141–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C141–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–35NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C141–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–45NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C141–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C141–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C141–55NI	N52	52-Pin Plastic Quad Flatpack	
	CY7C141–55LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[23]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
23. CY7C140/CY7C141 only.

Document #: 38−00027−K

CY7B131
CY7B141

1K x 8 Dual-Port Static RAM

Features

- **0.8-micron BiCMOS for high performance**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7B131 easily expands data bus width to 16 or more bits using slave CY7B141**
- **$\overline{BUSY}$ output flag on CY7B131; $\overline{BUSY}$ input on CY7B141**
- **$\overline{INT}$ flag for port-to-port communication**

Functional Description

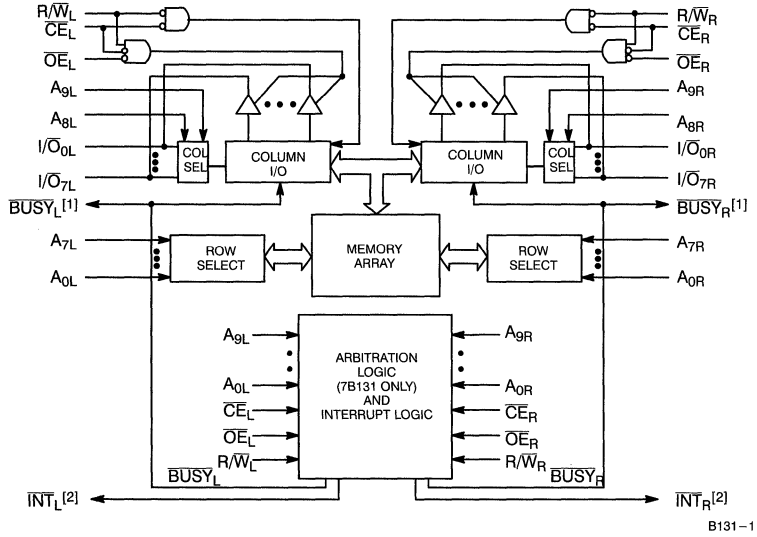
The CY7B131 and CY7B141 are high-speed BiCMOS 1K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7B131 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7B141 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ flags are provided on each port. In addition, an interrupt flag ($\overline{INT}$) is provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (3FF for the right port and 3FE for the left port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7B131/CY7B141 are available in 52-lead PLCC.

Logic Block Diagram

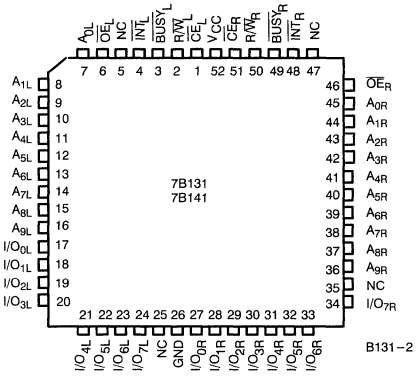


Notes:

1. CY7B131 (Master): $\overline{BUSY}$ is an open drain output and requires a pull-up resistor. CY7B141 (Slave): $\overline{BUSY}$ is an input.
2. Open drain outputs; pull-up resistor required.

Pin Configuration

52-Lead PLCC
Top View



Selection Guide

		7B131–15 7B141–15	7B131–20 7B141–20
Maximum Access Time (ns)		15	20
Maximum Operating Current (mA)	Com'l/Ind	260	240/300
Maximum Standby Current (mA)	Com'l/Ind	110	100/105

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 52 to Pin 26) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B131–15 7B141–15 Min.	7B131–15 7B141–15 Max.	7B131–20 7B141–20 Min.	7B131–20 7B141–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4	V
		I_{OL} = 16.0 mA[4]			0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[5]	Com'l		260		240	mA
			Ind				300	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		110		100	mA
			Ind				105	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		165		155	mA
			Ind				180	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15	mA
			Ind				30	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		160		150	mA
			Ind				170	

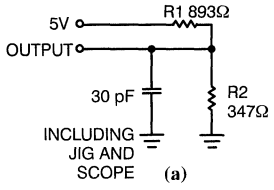
Capacitance[6]

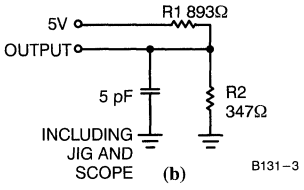
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

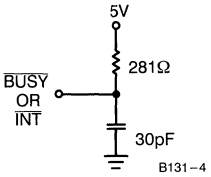
Notes:

3. See the last page of this specification for Group A subgroup testing information.
4. $\overline{BUSY}$ and $\overline{INT}$ pins only.
5. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
6. Tested initially and after any design or process changes that may affect these parameters.

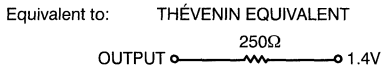
AC Test Loads and Waveforms

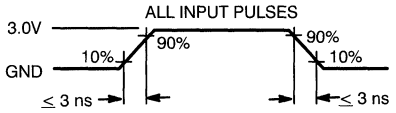






BUSY Output Load (CY7B131 ONLY)





Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B131–15 7B141–15 Min.	7B131–15 7B141–15 Max.	7B131–20 7B141–20 Min.	7B131–20 7B141–20 Max.	Unit
READ CYCLE						
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address to Data Valid[8]		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		10		13	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		10		13	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		10		13	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20	ns
WRITE CYCLE[11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		ns
t_{AW}	Address Set-Up to Write End	12		15		ns
t_{HA}	Address Hold from Write End	2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		ns
t_{SD}	Data Set-Up to Write End	10		13		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		10		13	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	3		3		ns

Notes:

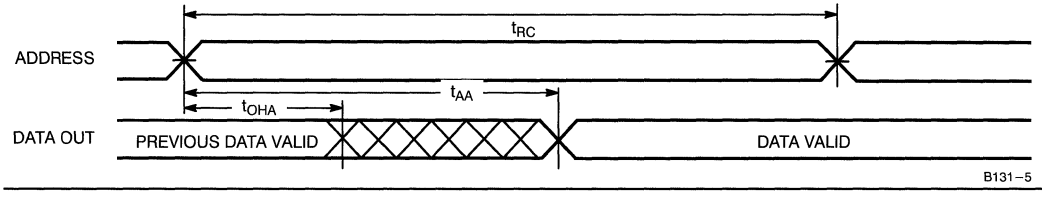
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3, 7] (continued)

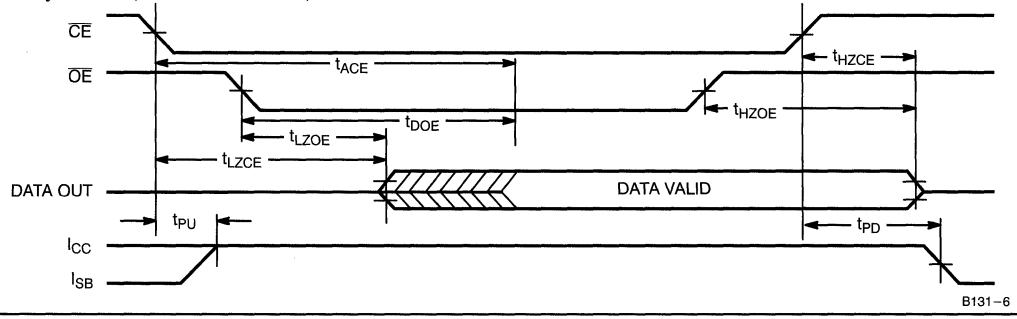
Parameter	Description	7B131–15 7B141–15 Min.	7B131–15 7B141–15 Max.	7B131–20 7B141–20 Min.	7B131–20 7B141–20 Max.	Unit
BUSY/INTERRUPT TIMING						
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[12]		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[12]		15		20	ns
t_{PS}	Port Set Up for Priority	5		5		ns
t_{WB}[13]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		15		20	ns
t_{DDD}	Write Data Valid to Read Data Valid[14]		25		30	ns
t_{WDD}	Write Pulse to Data Delay[14]		30		40	ns
INTERRUPT TIMING						
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns

Switching Waveforms

Read Cycle No. 1 (Either Port–Address Access[15, 16]



Read Cycle No. 2 (Either Port–$\overline{CE}$/$\overline{OE}$)[15, 17]

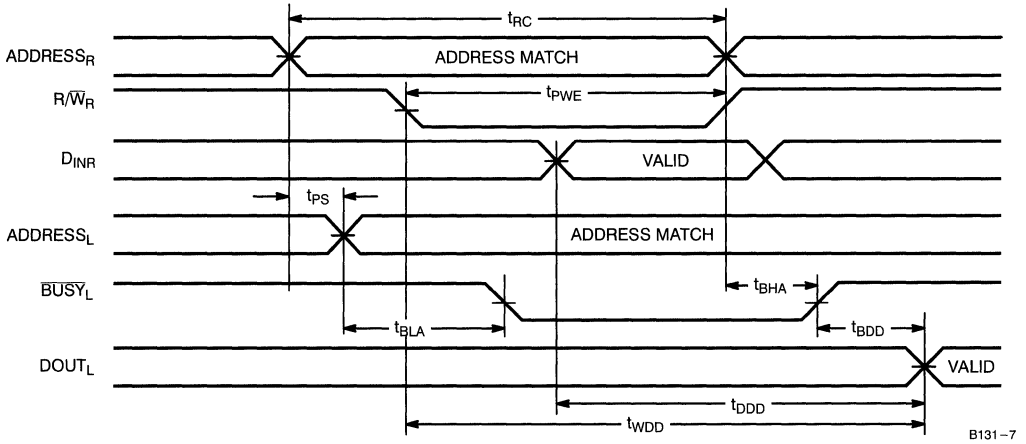


Notes:

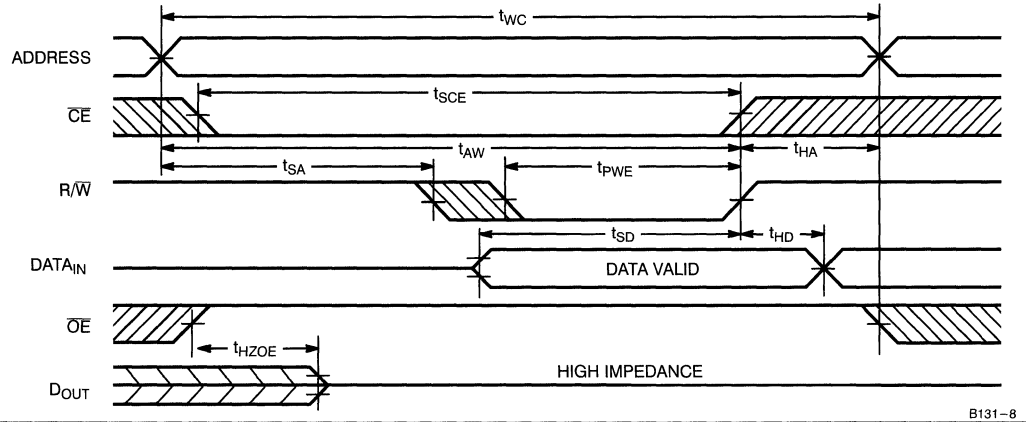
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7B141 only.
14. For information on port-to-port delay through RAM cells, from writing port to reading port, refer to the Read Timing with Port-to-Port Delay timing diagram.
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Read Cycle No. 3 (Read with $\overline{BUSY}$ Master: CY7B131)



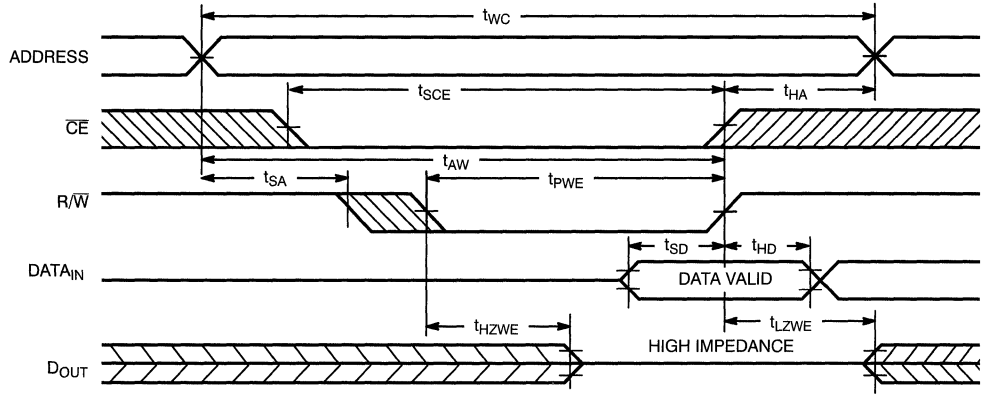
Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port) [11, 18]



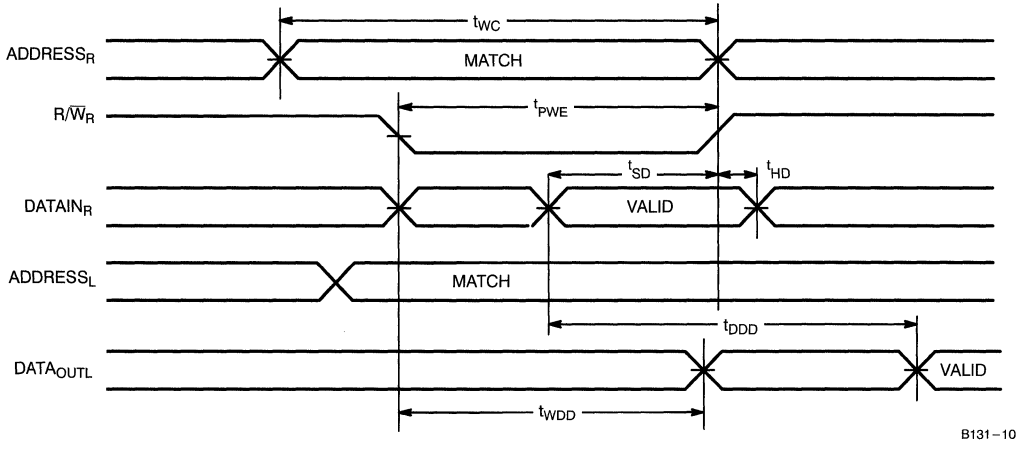
Note:
18. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[11, 19]



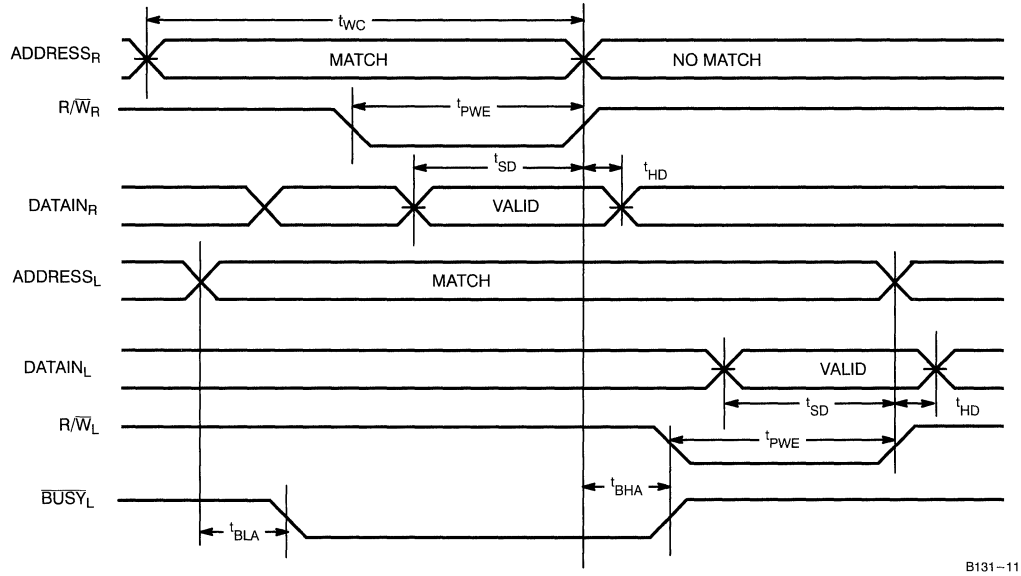
Read Timing with Port-to-Port Delay ($\overline{CE}_L = \overline{CE}_R$ = LOW, $\overline{BUSY}$ = HIGH for the Writing Port)



Note:
19. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms (continued)

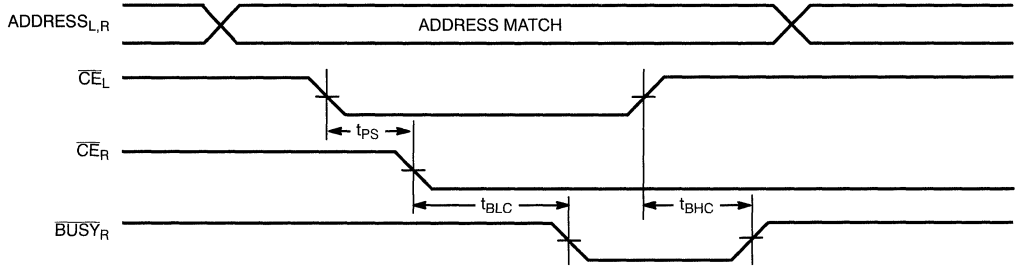
Write Timing with Port-to-Port Delay ($\overline{CE}_L$ = $\overline{CE}_R$ = LOW)



B131–11

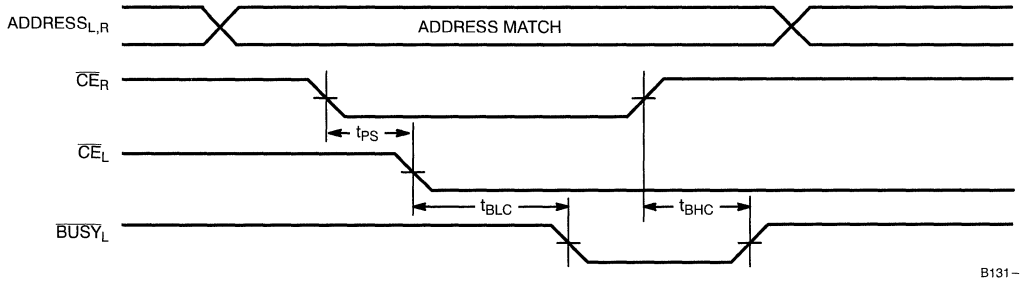
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



B131–12

$\overline{CE}_R$ Valid First:

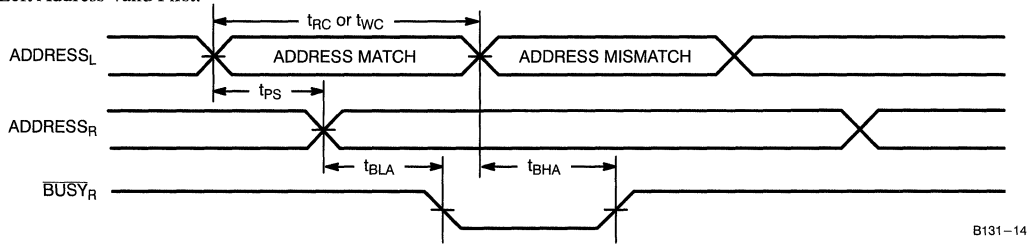


B131–13

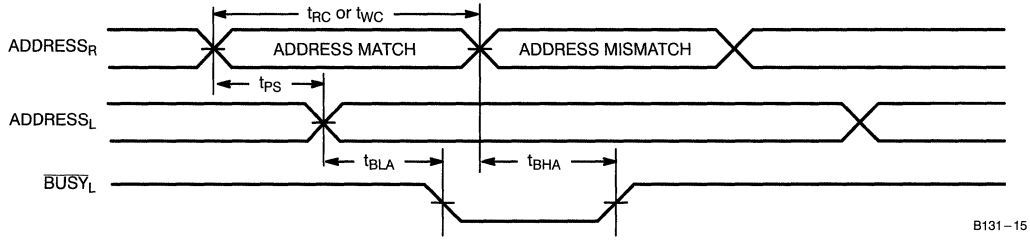
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

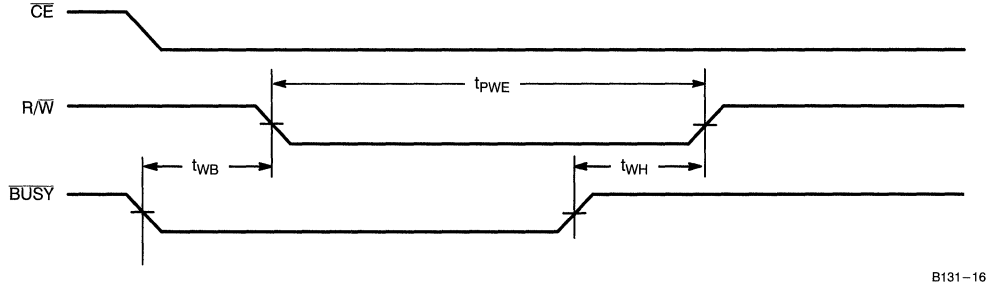
Left Address Valid First:



Right Address Valid First:

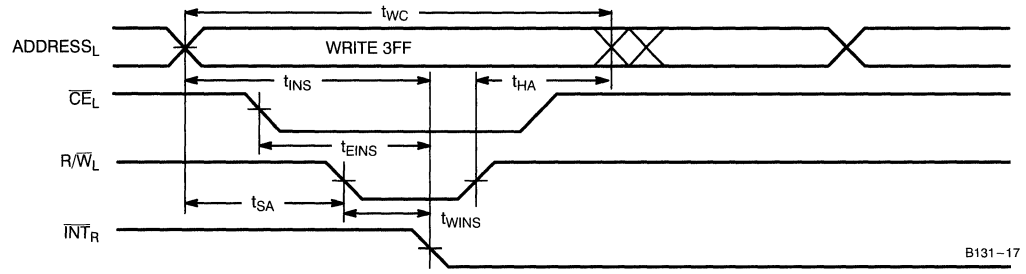


Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7B141)

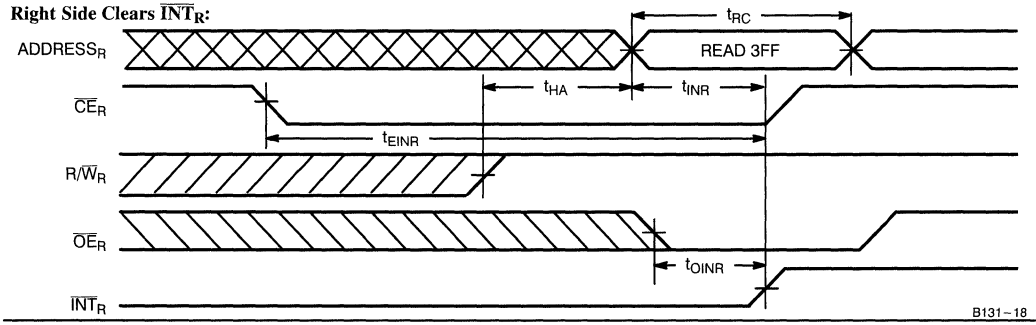


Interrupt Timing Diagrams

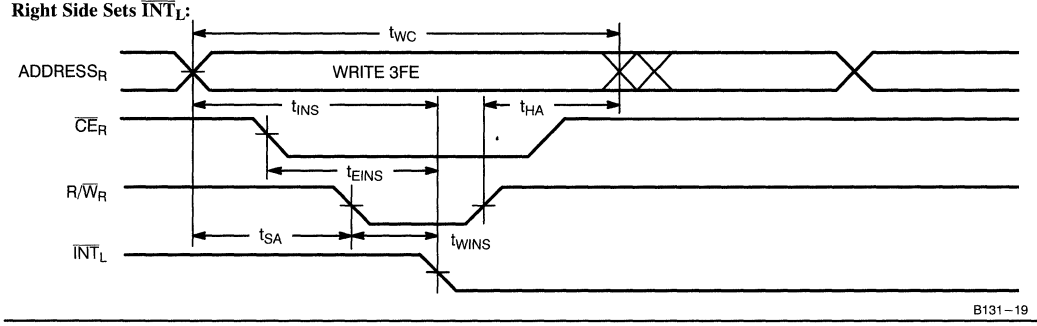
Left Side Sets $\overline{INT}_R$:



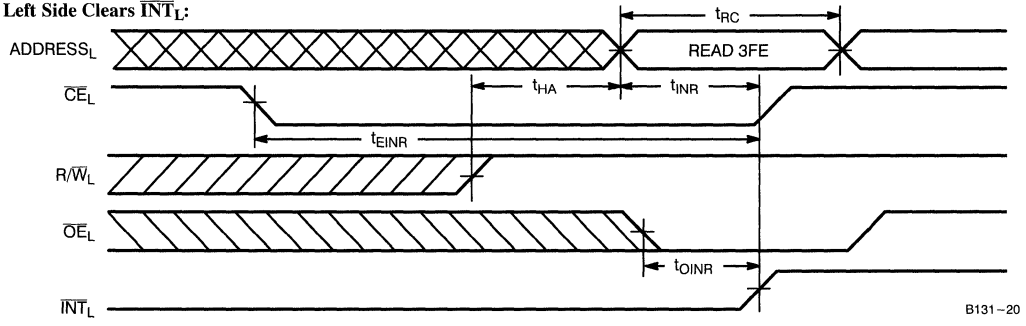
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Architecture

The CY7B131 (master) and CY7B141 (slave) are 1024-byte deep dual-port RAMs, with two independent sets of address signals, common I/O data signals, and control signals. By convention, the two ports are called the left port and the right port. The subscript R or L on the signal name identifies the port.

The upper two memory locations (3FF, 3FE) are special locations and may be used as "mailboxes" for passing messages between the ports. Location 3FF is the mailbox for the right port and location 3FE is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner of the mailbox. When the owner reads the mailbox, the interrupt is reset.

The address and control signals provide independent, asynchronous, random access to any location in the memory. It is possible that both ports may attempt to access the same memory location at the same time. If this contention occurs, a circuit in the master called an arbiter decides which port temporarily "owns" the memory location. The losing port receives a BUSY signal, which notifies it that the memory location is owned by the other port and that the operation it attempted to perform may not be successful.

The two BUSY signals are outputs from the master and inputs to the slave.

Contention, Arbitration and Resolution— The Significance of BUSY

When contention occurs, the arbiter decides which port wins (owns) the memory location and which port loses. The decision is on a "first-come-first-served" basis. In order for contention to occur, both ports must address the same memory location and have their respective chip enables active. If one port precedes the other by an amount of time greater than or equal to t_{PS} (port set-up for priority;equal to five nanoseconds) it is guaranteed to win the arbitration. If contention occurs within the t_{PS} interval, it is not possible to predict which port will win, but one will win and the other will lose.

There are two ports and each may be either reading or writing, and each may win or lose, so there are eight combinations. They are listed in *Table 1* and identified as cases one through eight. In cases one and two, both ports are reading, the losing port receives a BUSY, the read is allowed to occur, and the data read by both ports is valid. In case three, the left port wins and reads valid data, and the write attempted by the right port is inhibited. In cases four and five, when the winning port is writing, the write is completed, but the data read by the losing port may be invalid. Case six is similar to case three; the right port successfully reads and the write attempt by the left port is inhibited. In cases seven and eight the winning port successfully writes and the attempted write by the losing port is inhibited.

In cases four and five, where the losing port is reading, if the port signals are asynchronous to each other, the data read may be the old data, the new data, or some random combination of the two sets of data. In cases seven and eight the losing port is prevented from writing. The commonality between these four cases is that the losing port receives a busy signal, which tells it that either (1) the operation it attempted was not successful, or (2) that the data it read may not be valid. In either situation, the operation should be repeated after the busy signal becomes inactive.

Flow-Through Operation

The CY7B131/141 have a flow-through architecture that facilitates repeating (actually extending) an operation when a BUSY is received by a losing port. The BUSY signal should be interpreted as a NOT READY. If a BUSY to a port is active, the port should wait for BUSY to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Read Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either t_{WDD} after the falling edge of the write strobe of the left port, or t_{DDD} after the data being written becomes stable.

The timing diagram titled, "Write Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port wants to write to the same address. If the left port extends its write strobe for a minimum time of t_{PWE} after the BUSY signal to it goes inactive, its write will be successful; it writes over the data just written by the right port.

Data Bus Width Expansion Using Slaves

One master and as many slaves as necessary may be connected in parallel to expand the data bus width in byte increments.

Two masters must not be connected in parallel because, if the time interval between which they address the same location is less than t_{PS}, both could end up waiting for the other to release the BUSY to it.

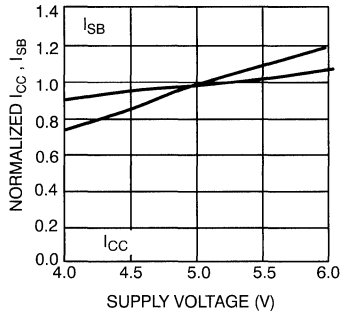
Therefore, only one master must arbitrate, and it can drive as many slaves as required. The write strobe to the slaves must be delayed an amount of time equal to at least t_{BLA}. This insures that the slave is not inadvertently written to before the outcome of the arbitration is determined.

Table 1. Operation

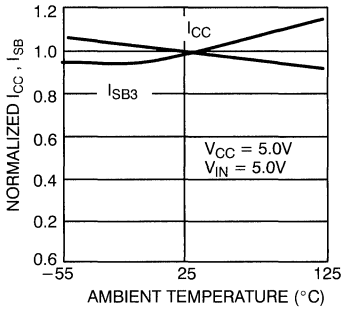
Case	Operation Port		Winning Port	Result
	L	R		
1	R	R	L	Both Read
2	R	R	R	Both Read
3	R	W	L	L Reads OK, R Write Inhibited
4	R	W	R	R Writes OK L Data May Be Invalid
5	W	R	L	L writes OK R Data May Be Invalid
6	W	R	R	R Reads OK L Write Inhibited
7	W	W	L	L Writes OK R Write Inhibited
8	W	W	R	R Writes OK L Write Inhibited

Typical DC and AC Characteristics

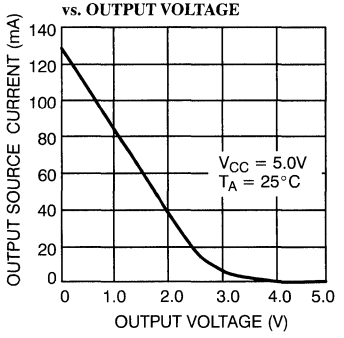
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



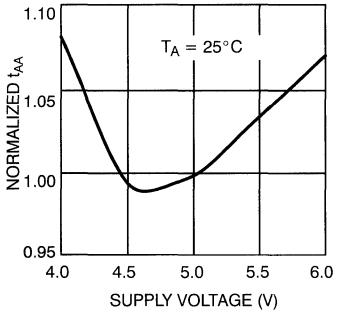
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



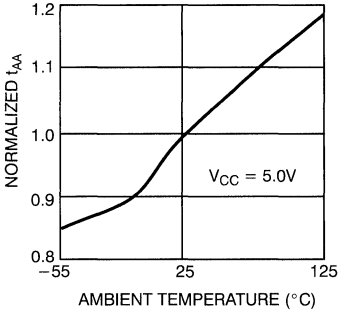
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



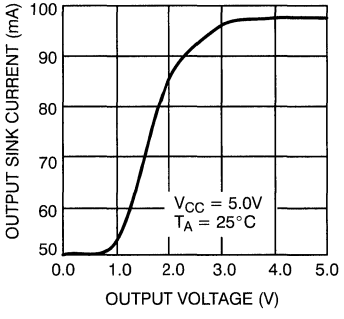
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



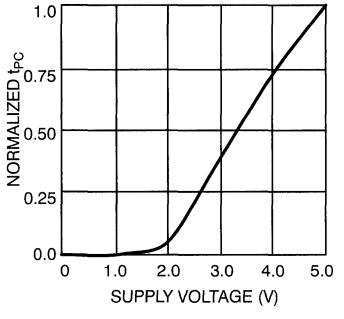
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



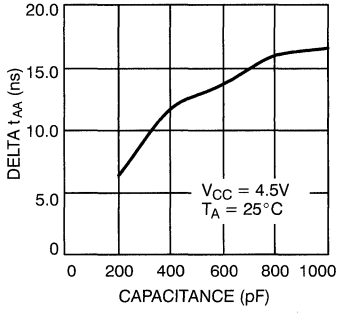
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



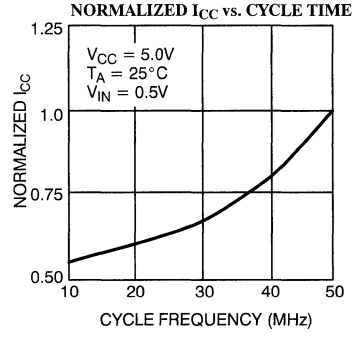
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



6

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B131–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B131–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B131–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B141–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B141–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B141–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Document #: 38–00466

CY7C132/CY7C136
CY7C142/CY7C146

2K x 8 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146**
- **$\overline{BUSY}$ output flag on CY7C132/CY7C136; $\overline{BUSY}$ input on CY7C142/CY7C146**
- **$\overline{INT}$ flag for port-to-port communication (52-pin LCC/PLCC/PQFP versions)**

Functional Description

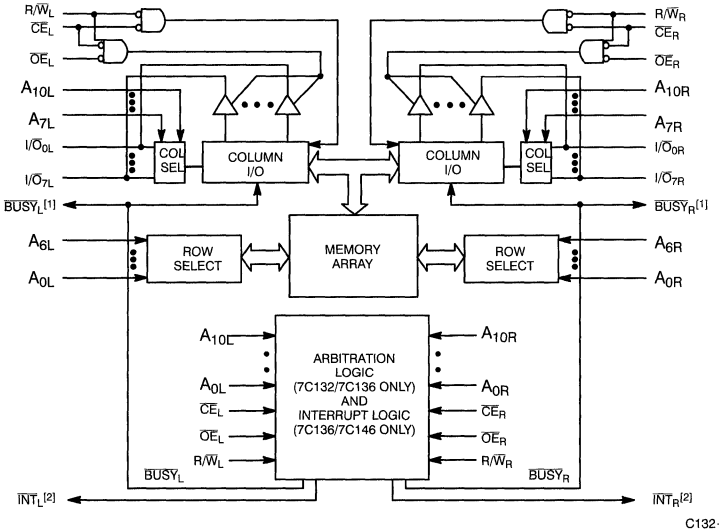
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7C132/CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ flags are provided on each port. In addition, an interrupt flag ($\overline{INT}$) is provided on each port of the 52-pin LCC and PLCC versions. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, $\overline{INT}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in 52-pin LCC, PLCC, and PQFP.

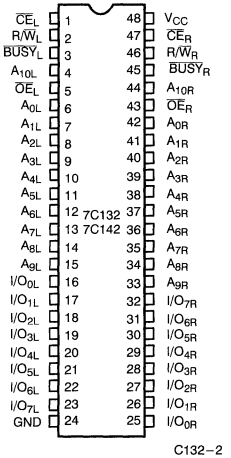
Logic Block Diagram



C132–1

Pin Configuration

DIP
Top View



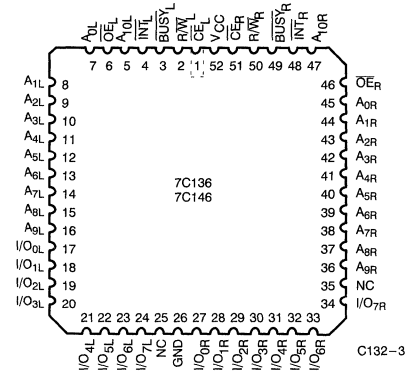
C132–2

Notes:

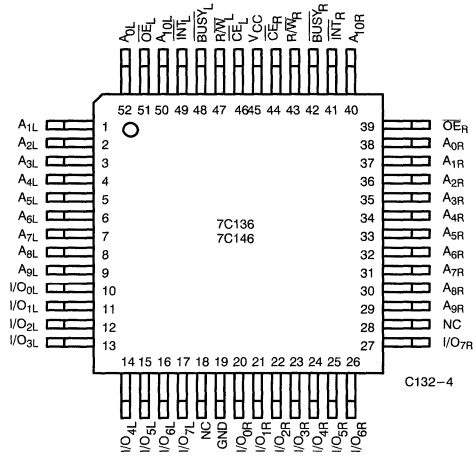
1. CY7C132/CY7C136 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): $\overline{BUSY}$ is input.
2. Open drain outputs; pull-up resistor required.

Pin Configurations (continued)

LCC/PLCC
Top View



PQFP
Top View



Selection Guide

		7C132-25[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[4]	−55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in PQFP and PLCC packages only.
4. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C132–25, 30[3] 7C136–25, 30 7C142–25, 30 7C146–25, 30 Min.	Max.	7C132–35 7C136–35 7C142–35 7C146–35 Min.	Max.	7C132–45, 55 7C136–45, 55 7C142–45, 55 7C146–45, 55 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[6]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		170		120		90	mA
			Mil				170		120	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		65		45		35	mA
			Mil				65		45	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		115		90		75	mA
			Mil				115		90	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		105		85		70	mA
			Mil				105		85	

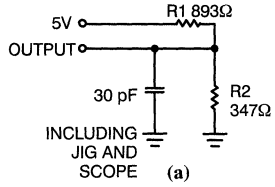
Capacitance[9]

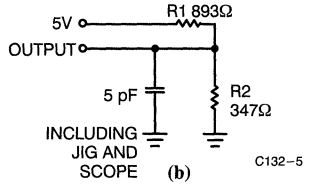
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

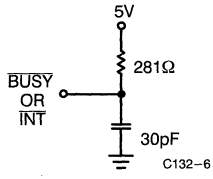
Notes:

5. See the last page of this specification for Group A subgroup testing information.
6. $\overline{BUSY}$ and $\overline{INT}$ pins only.
7. Duration of the short circuit should not exceed 30 seconds.
8. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
11. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
12. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
13. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
14. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

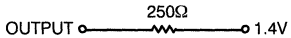


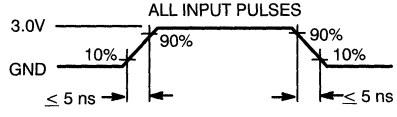




BUSY Output Load (CY7C132/CY7C136 ONLY)

Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[5, 10]

Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid[11]		25		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[11]		25		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[11]		15		20		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[12]	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[12]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[12, 13]		15		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE[14]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	15		25		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		15		15		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		0		ns

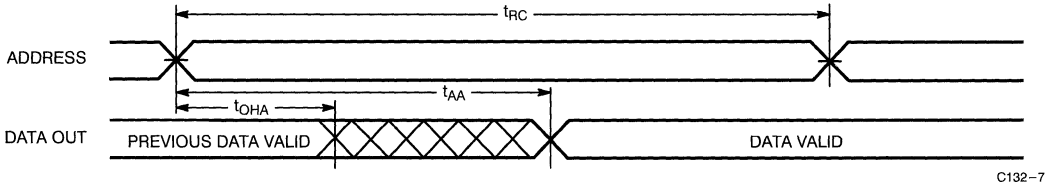
Switching Characteristics Over the Operating Range[5, 10] (continued)

Parameter	Description	7C132–25[3] 7C136–25 7C142–25 7C146–25		7C132–30 7C136–30 7C142–30 7C146–30		7C132–35 7C136–35 7C142–35 7C146–35		7C132–45 7C136–45 7C142–45 7C146–45		7C132–55 7C136–55 7C142–55 7C146–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[15]		20		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[15]		20		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t_{WB}[16]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	20		30		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		30		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t_{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING[18]												
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[15]		25		25		25		35		45	ns

Notes:
15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
16. CY7C142/CY7C146 only.
17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. R/$\overline{W}$ for Port B is toggled during valid read.
18. 52-pin LCC/PLCC versions only.
19. R/$\overline{W}$ is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms

Read Cycle No. 1 (Either Port–Address Access[19, 20]



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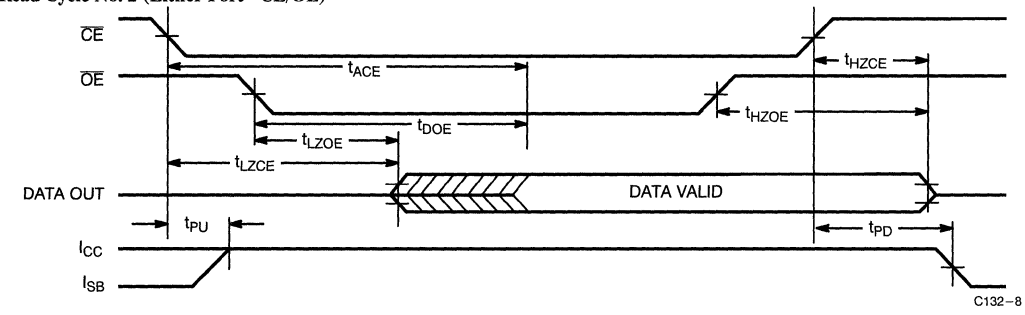
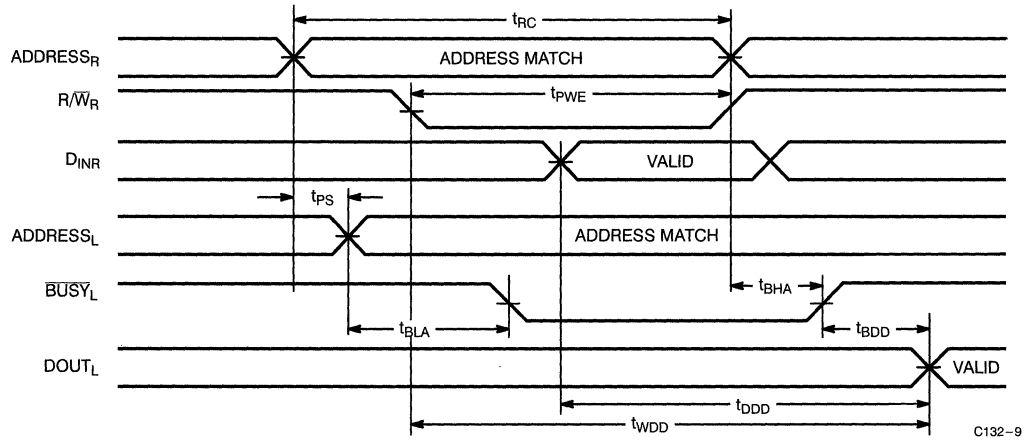
Switching Waveforms (continued)

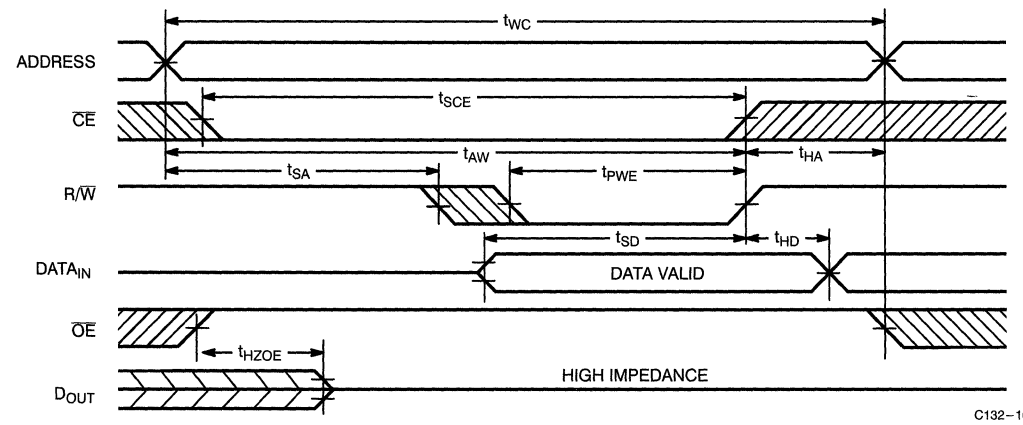
Read Cycle No. 2 (Either Port–$\overline{CE}/\overline{OE}$)[19, 21]



Read Cycle No. 3 (Read with $\overline{BUSY}$ Master: CY7C132 and CY7C136)

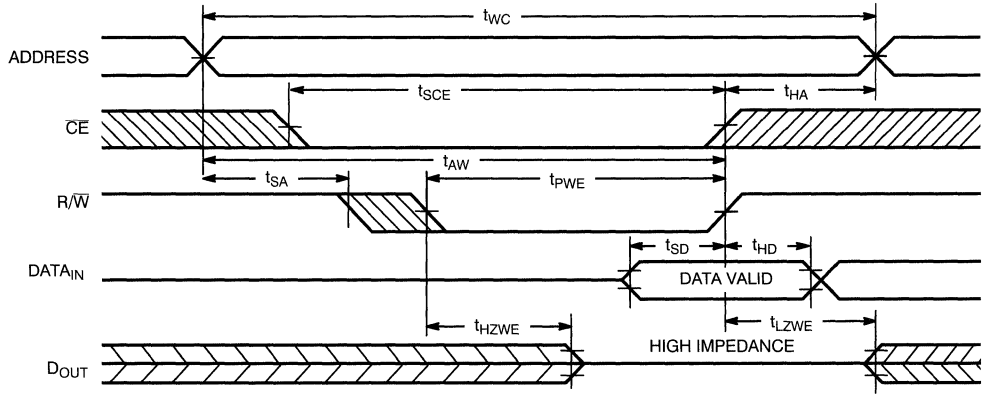


Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port) [14, 22]



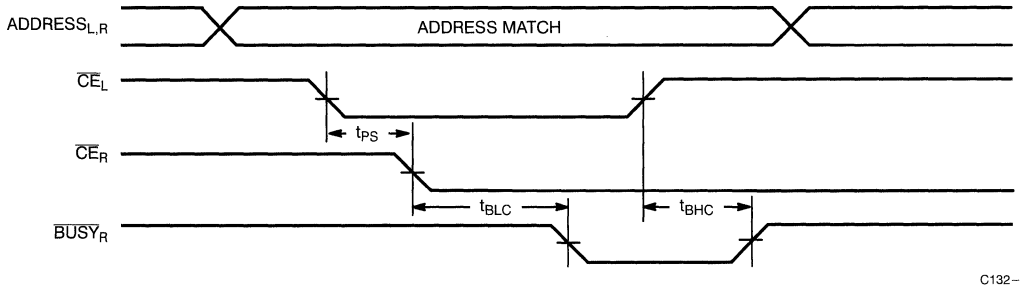
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[14, 23]

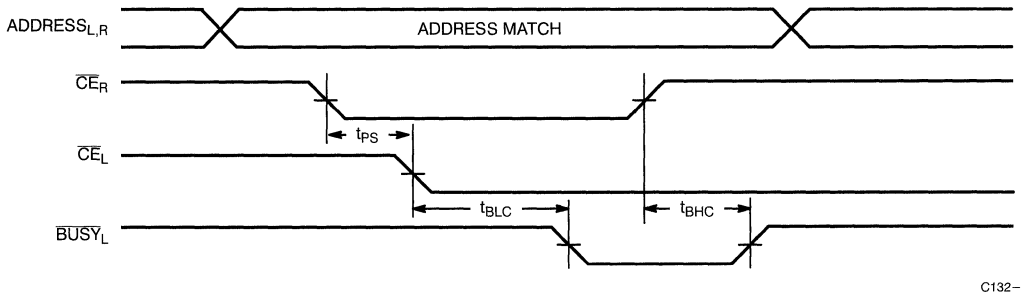


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



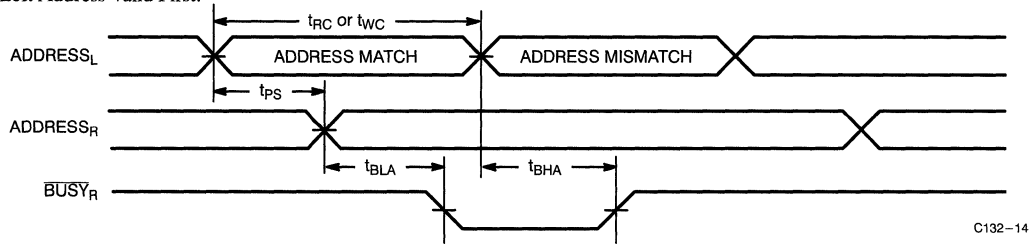
$\overline{CE}_R$ Valid First:



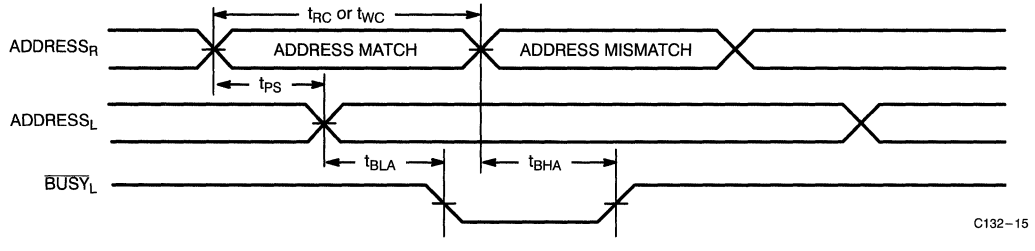
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

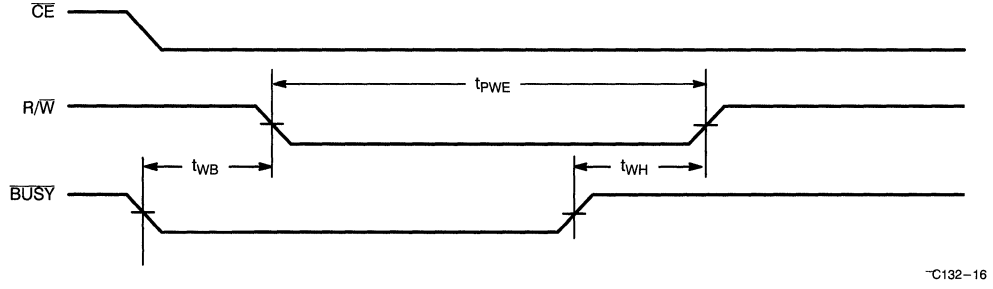
Left Address Valid First:



Right Address Valid First:

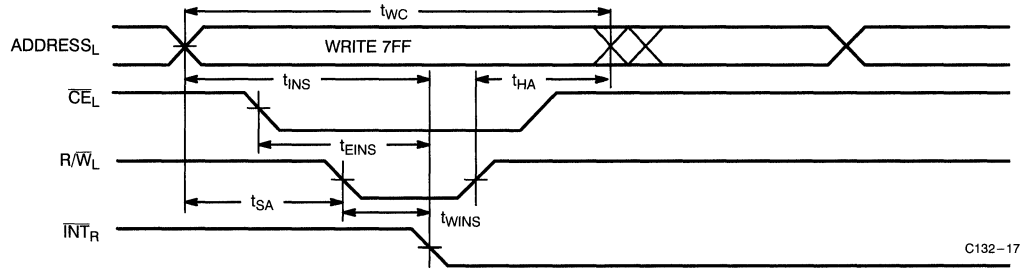


Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7C142/CY7C146)

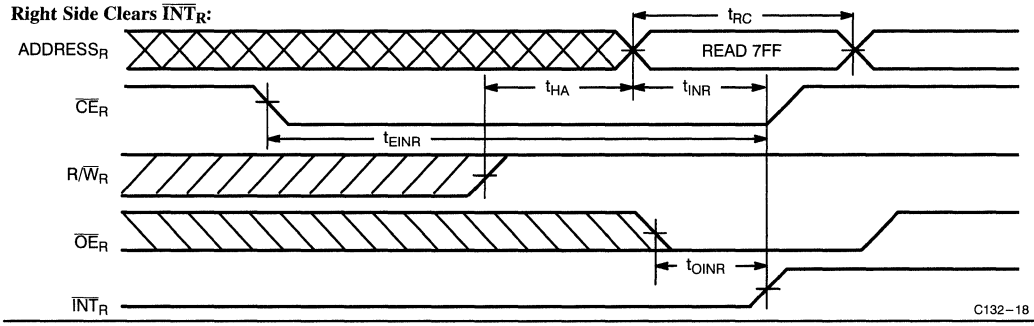


Interrupt Timing Diagrams[18]

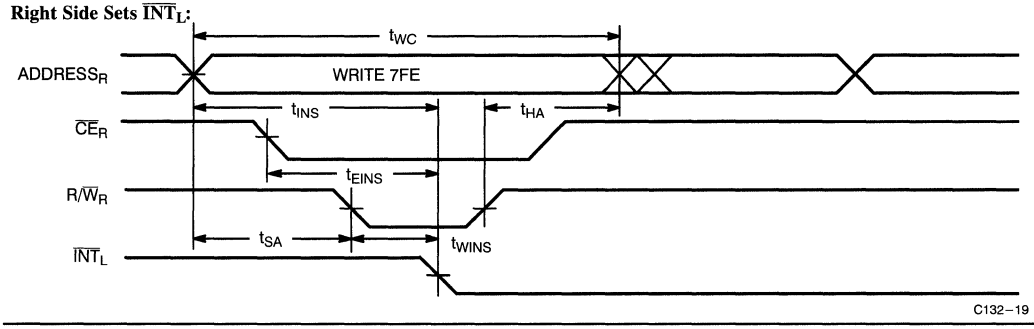
Left Side Sets $\overline{INT}_R$:



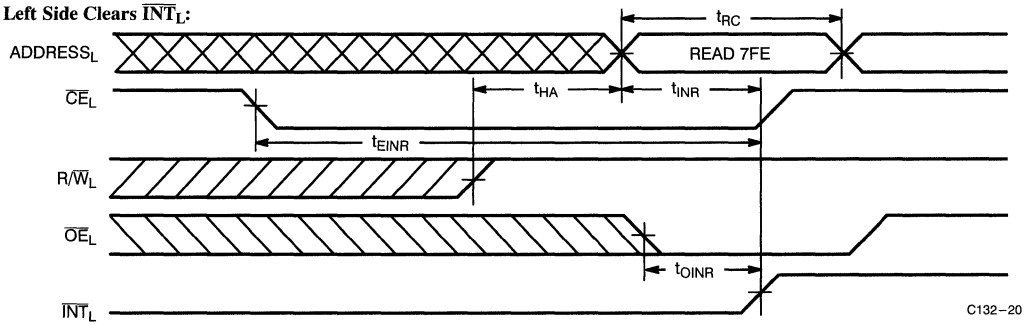
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



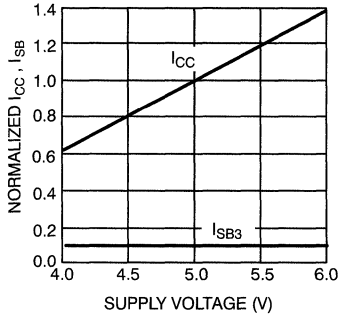
Left Side Clears $\overline{INT}_L$:



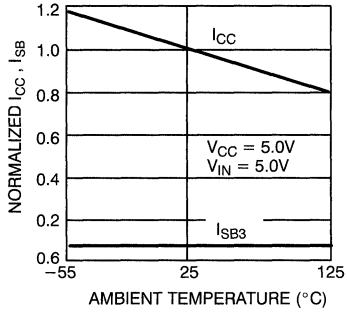
6

Typical DC and AC Characteristics

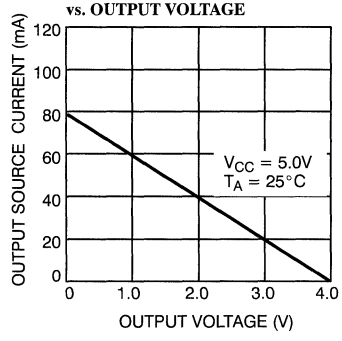
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



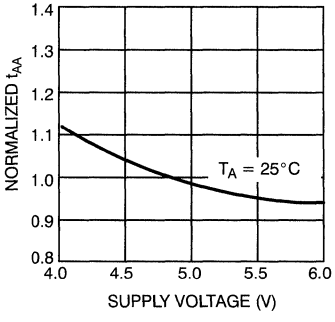
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



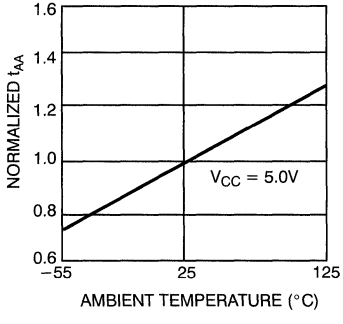
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



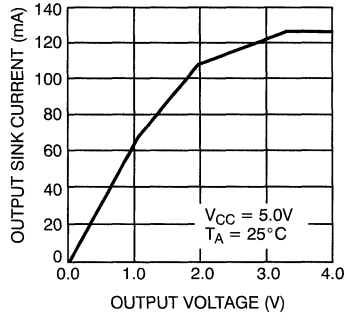
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



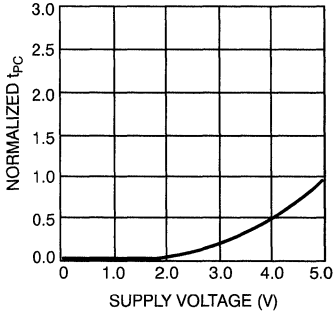
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



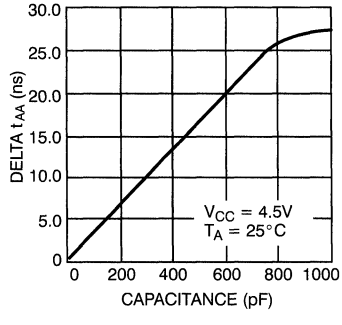
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



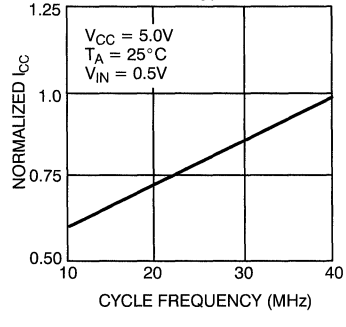
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C132–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C132–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C136–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136–55LMB	L69	52-Square Leadless Chip Carrier	Military

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142–30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
45	CY7C142–45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–45DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7C142–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142–55DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C146–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C146–30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146–45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146–55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146–55LMB	L69	52-Square Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[24]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
24. CY7C142/CY7C146 only.

Document #: 38-00061-J

CY7C133
CY7C143

2K x 16 Dual-Port Static RAM

Features

- **0.8-micron CMOS for optimum speed/power**
- **High speed access: 25 ns**
- **Low operating power: I_{CC} = 170 mA (typ.)**
- **Automatic power-down**
- **TTL compatible**
- **Fully asynchronous operation**
- **Master CY7C133 easily expands data bus width to 32 or more bits using slave CY7C143**
- **$\overline{BUSY}$ output flag on CY7C133; $\overline{BUSY}$ input on CY7C143**
- **Available in 68-pin PLCC**
- **Pin compatible and functionally equivalent to IDT7133 and IDT7143**

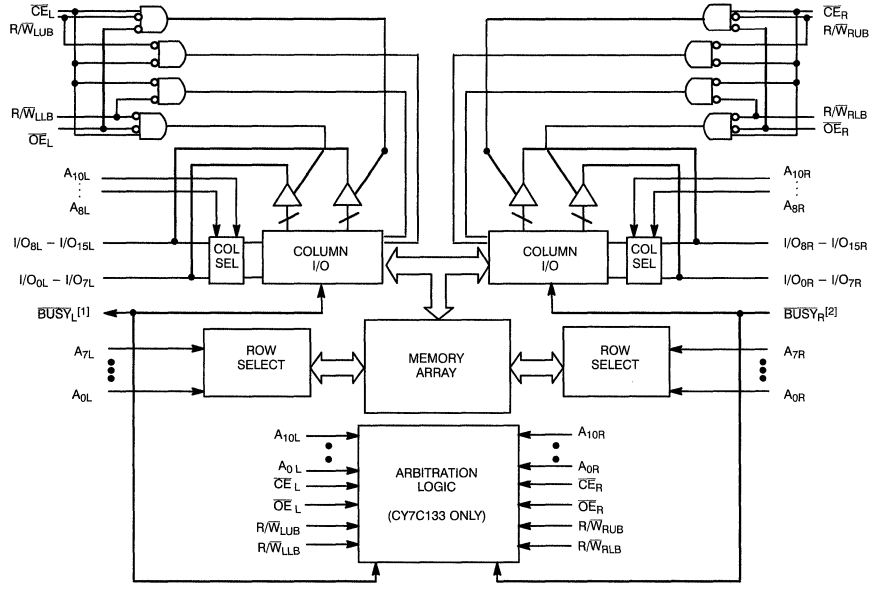
Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a standalone 16-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C143 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($R/\overline{W}_{UB}$, $R/\overline{W}_{LB}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C133 and CY7C143 are available in 68-pin PLCC.

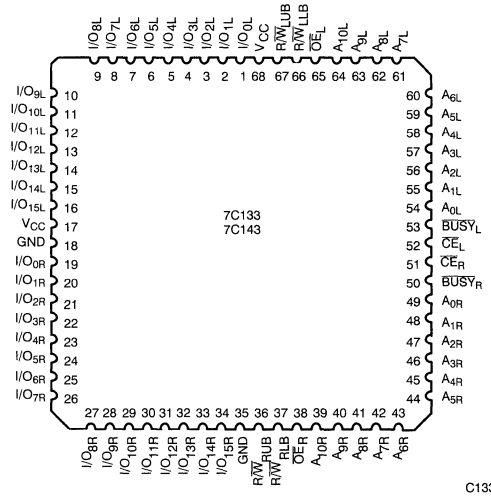
Logic Block Diagram



Notes:
1. CY7C133 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C143 (Slave): $\overline{BUSY}$ is input.

Pin Configuration

68-Pin LCC/PLCC
Top View



C133–2

Selection Guide

	7C133–25 7C143–25	7C133–35 7C143–35	7C133–55 7C143–55
Maximum Access Time (ns)	25	35	55
Typical Operating Current I_{CC} (mA)	170	160	150
Typical Standby Current for I_{SB1} (mA)	40	30	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

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Electrical Characteristics Over the Operating Range[2]

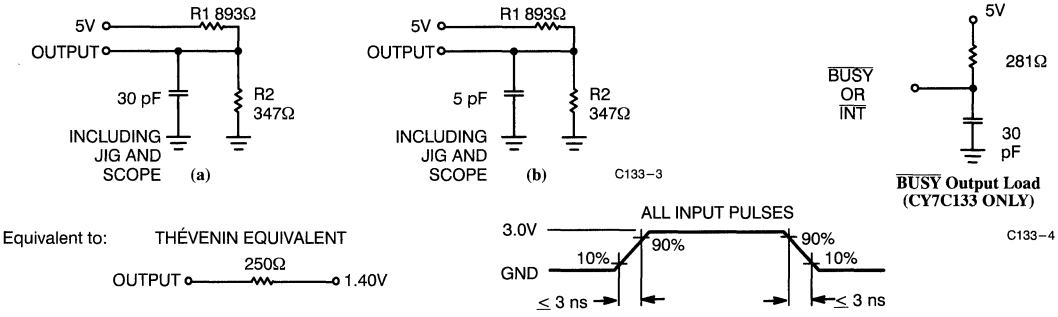
Parameter	Description	Test Conditions		7C133–25 7C143–25 Min.	Typ.	Max.	7C133–35 7C143–35 Min.	Typ.	Max.	7C133–55 7C143–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA				0.4			0.4			0.4	V
		I_{OL} = 16.0 mA[3]				0.5			0.5			0.5	
V_{IH}	Input HIGH Voltage			2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−5		+5	−5		+5	−5		+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5		+5	−5		+5	−5		−5	μA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = GND				−200			−200			−200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[6]	Com'l		170	250		160	230		150	220	mA
			Ind		170	290		160	260		150	250	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		40	60		30	50		20	40	mA
			Ind		40	75		30	65		20	55	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		100	140		85	125		75	110	mA
			Ind		100	160		85	140		75	125	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15		3	15		3	15	mA
			Ind		3	15		3	15		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[6]	Com'l		90	120		80	105		70	90	mA
			Ind		90	140		80	120		70	105	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
2. See the last page of this specification for Group A subgroup testing information.
3. $\overline{BUSY}$ pin only.
4. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C133–25 7C143–25		7C133–35 7C143–35		7C133–55 7C143–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		55		ns
t_{AA}	Address to Data Valid[8]		25		35		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9, 10]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9, 10]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		25	ns
WRITE CYCLE[11]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		40		ns
t_{AW}	Address Set-Up to Write End	20		25		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[10]		15		20		20	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[10]	0		0		0		ns

Notes:

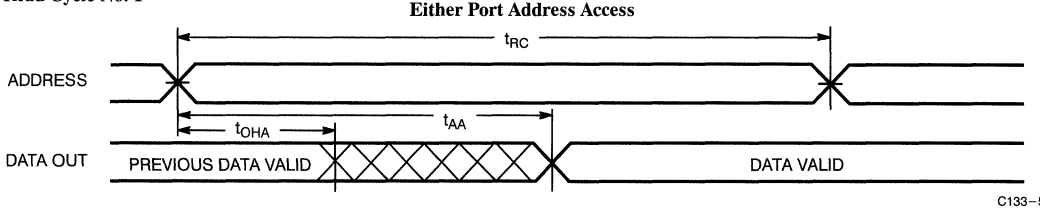
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{LZCE} is less than t_{HZCE} and t_{LZOE} is less than t_{HZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[2,7] (continued)

Parameter	Description	7C133–25 7C143–25		7C133–35 7C143–35		7C133–55 7C143–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING (For Master CY7C133)								
t_{BLA}	$\overline{BUSY}$ Low from Address Match		25		35		50	ns
t_{BHA}	$\overline{BUSY}$ High from Address Mismatch		20		30		40	ns
t_{BLC}	$\overline{BUSY}$ Low from $\overline{CE}$ Low		20		25		35	ns
t_{BHC}	$\overline{BUSY}$ High from $\overline{CE}$ High		20		20		30	ns
t_{WDD}	Write Pulse to Data Delay[12]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[12]		35		45		55	ns
t_{BDD}	$\overline{BUSY}$ High to Valid Data[13]		Note 13		Note 13		Note 13	ns
t_{PS}	Arbitration Priority Set Up Time[14]	5		5		5		ns
BUSY TIMING (For Slave CY7C143)								
t_{WB}	Write to $\overline{BUSY}$[15]	0		0		0		ns
t_{WH}	Write Hold After $\overline{BUSY}$[16]	20		25		30		ns
t_{WDD}	Write Pulse to Data Delay[17]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[17]		35		45		55	ns

Switching Waveforms

Read Cycle No. 1[18, 19]



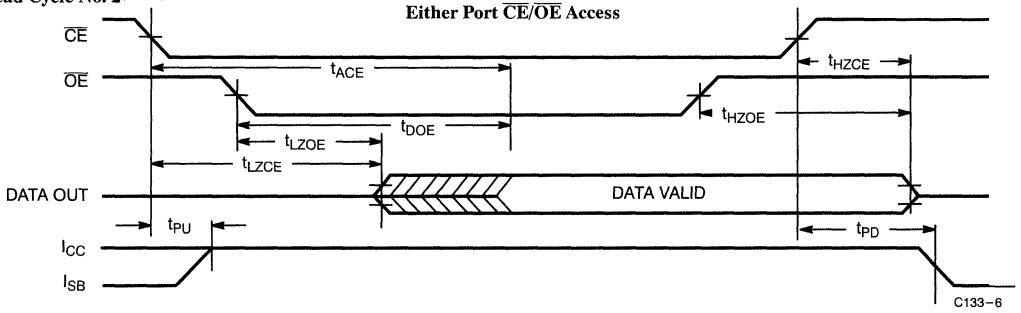
Notes:

12. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with $\overline{BUSY}$, Master: CY7C133."
13. t_{BDD} is calculated parameter and is greater of 0,$t_{WDD}-t_{WP}$ (actual) or $t_{DDD}-t_{DW}$ (actual).
14. To ensure that the earlier of the two ports wins.
15. To ensure that write cycle is inhibited during contention.
16. To ensure that a write cycle is completed after contention.
17. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with Port-to-port Delay."
18. R/$\overline{W}$ is HIGH for read cycle
19. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.

Switching Waveforms (continued)

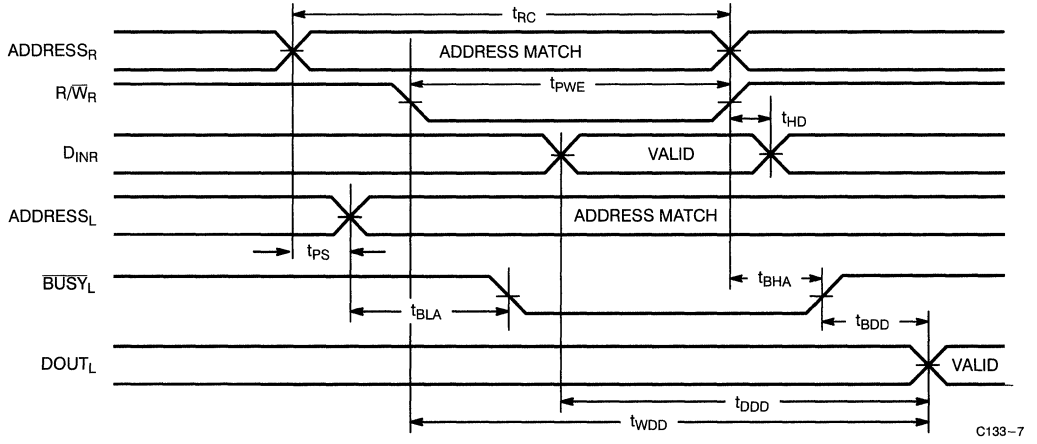
Read Cycle No. 2[18,20]

Either Port $\overline{CE}/\overline{OE}$ Access



Read Cycle No. 3[19]

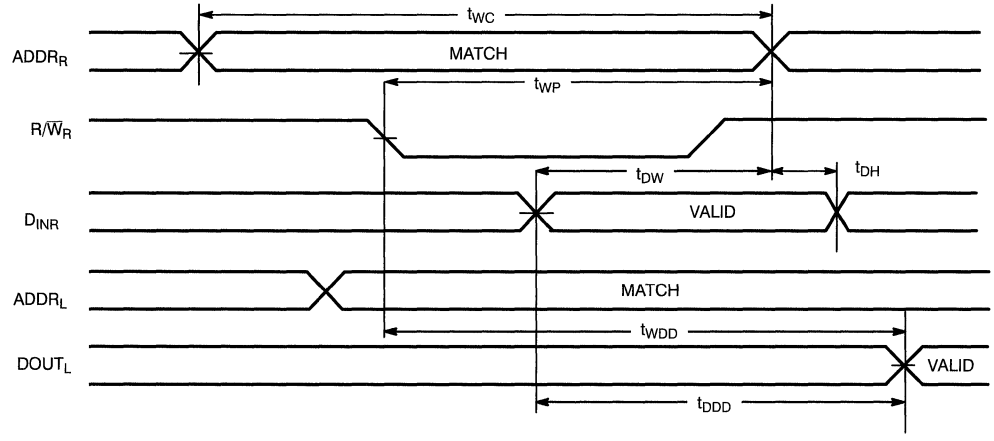
Read with $\overline{BUSY}$, Master: CY7C133



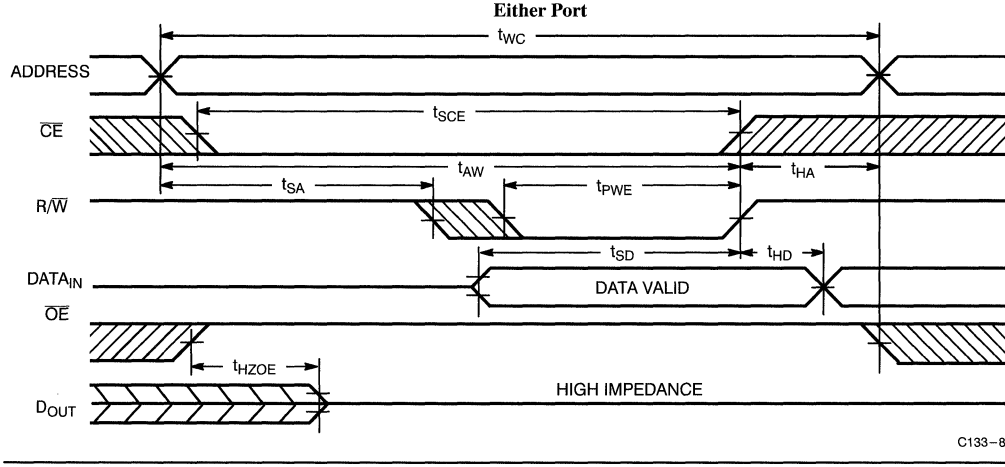
Notes:
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Timing Waveform of Read with Port-to-port Delay No. 4 (For Slave CY7C143)[21,22,23]



Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port)[14,24]

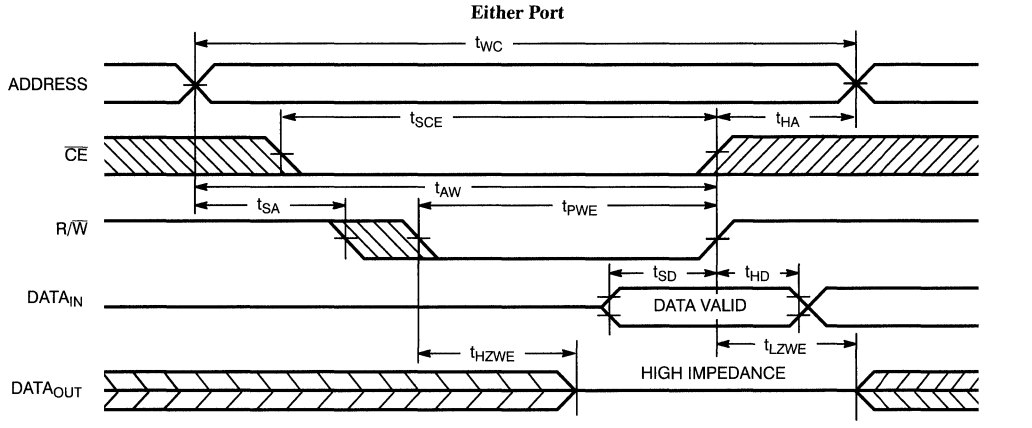


Notes:

21. Assume $\overline{BUSY}$ input at V_{IH} for the writing port and at V_{IL} for the reading port.
22. Write cycle parameters should be adhered to inorder to ensure proper writing.
23. Device is continuously enabled for both ports.
24. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

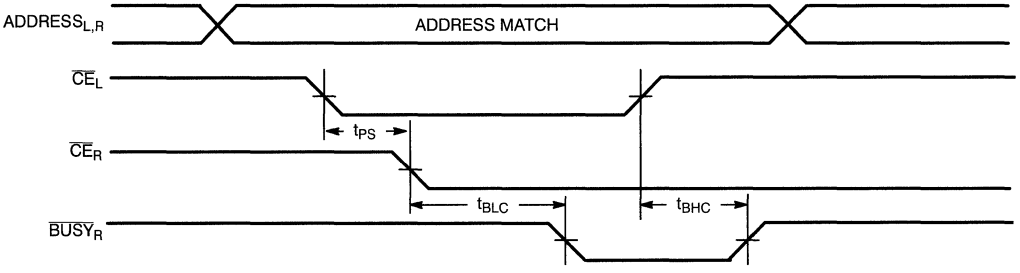
Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[20,25]

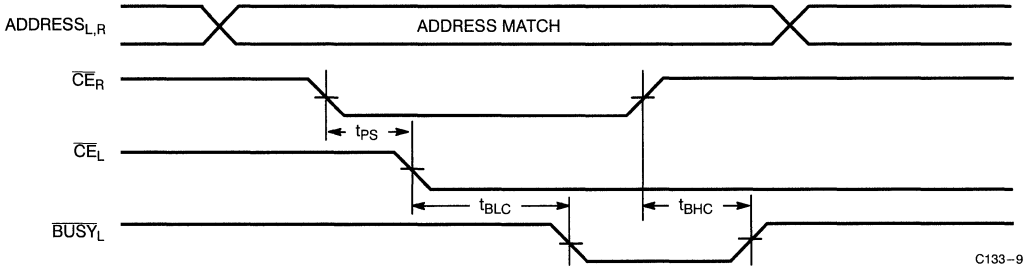


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

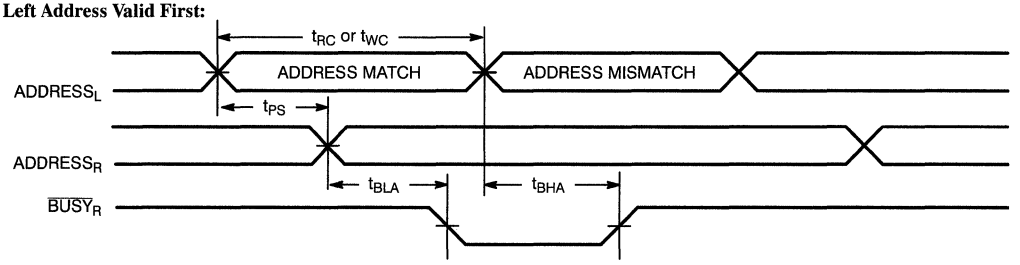


Note:
25. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

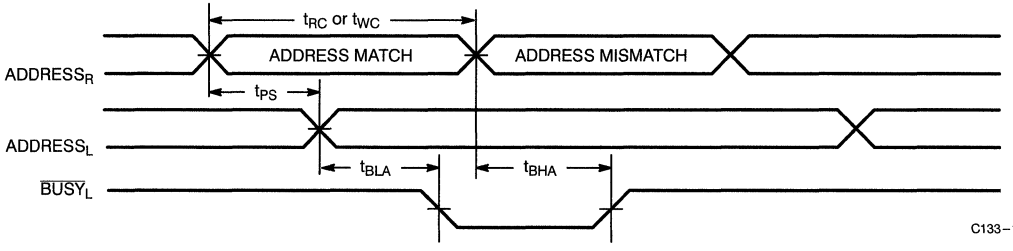
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



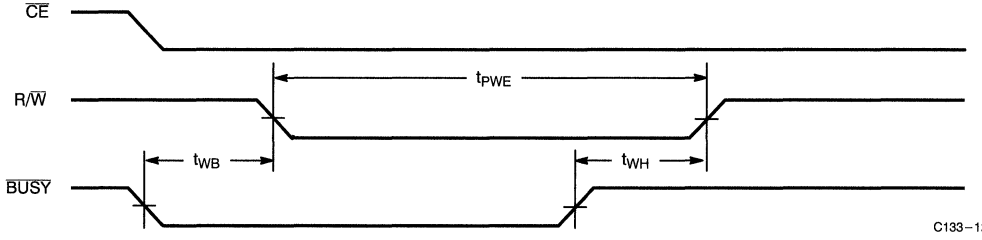
Right Address Valid First:



C133–11

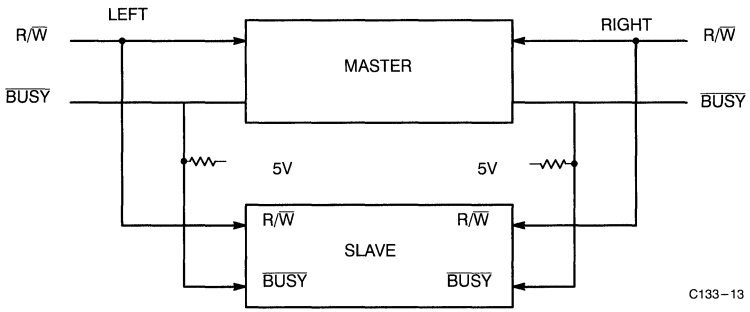
Busy Timing Diagram No. 3

Write with $\overline{BUSY}$ (Slave: CY7C143)



C133–12

32-Bit Master/Slave Dual-Port Memory Systems



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C133-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C133-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C133-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C143-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C143-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C143-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C143-55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[26]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

Note:
23. CY7C143 only.

Document #: 38-00414

CY7B134
CY7B135
CY7B1342

4K x 8 Dual-Port Static RAMs and 4K x 8 Dual-Port Static RAM with Semaphores

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **7B1342 includes semaphores**
- **7B134 available in 48-pin DIP**
- **7B135/7B1342 available in 52-pin LCC/PLCC**

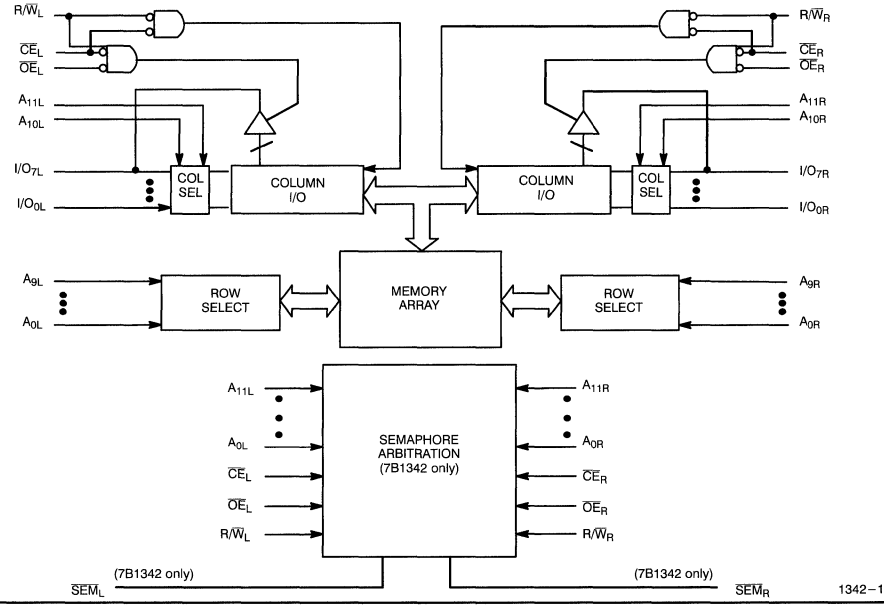
Functional Description

The CY7B134, CY7B135, and CY7B1342 are high-speed BiCMOS 4K x 8 dual-port static RAMs. The CY7B1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). The CY7B134/135 are suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7B1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7B1342 only).

The CY7B134 is available in 48-pin DIP. The CY7B135 and CY7B1342 are available in 52-pin LCC/PLCC.

Logic Block Diagram

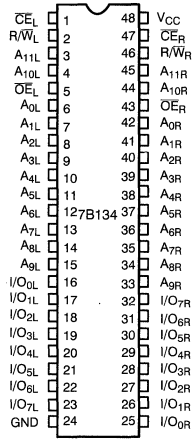


Selection Guide

		7B135–15 7B1342–15	7B134–20 7B135–20 7B1342–20	7B134–25 7B135–25 7B1342–25	7B134–35 7B135–35 7B1342–35	7B134–55 7B135–55 7B1342–55
Maximum Access Time (ns)		15	20	25	35	55
Maximum Operating Current (mA)	Commercial	260	240	220	210	210
	Military			260	250	250
Maximum Standby Current (mA)	Commercial	110	100	95	90	90
	Military			100	95	95

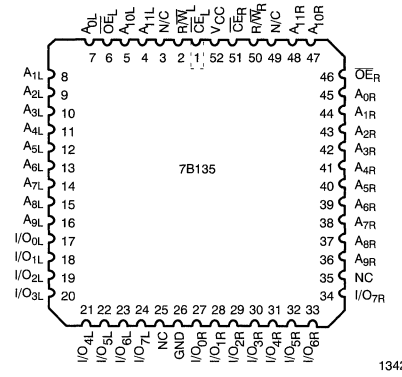
Pin Configurations

DIP
Top View



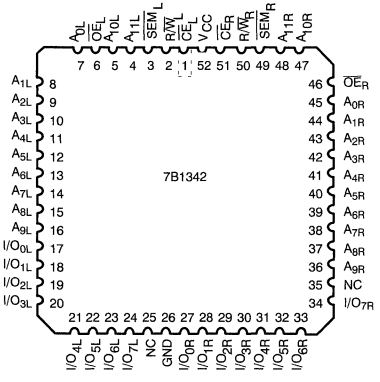
1342–2

LCC/PLCC
Top View



1342–3

LCC/PLCC
Top View



1342–4

Pin Definitions

Left Port	Right Port	Description
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7B1342 only)	$\overline{SEM}_R$ (CY7B1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −3.0V to +7.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B135−15 7B1342−15 Min.	7B135−15 7B1342−15 Max.	7B134−20 7B135−20 7B1342−20 Min.	7B134−20 7B135−20 7B1342−20 Max.	7B134−25 7B135−25 7B1342−25 Min.	7B134−25 7B135−25 7B1342−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		260		240		220	mA
			Mil/Ind.						260	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		110		100		95	mA
			Mil/Ind.						100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		165		155		145	mA
			Mil/Ind.						170	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		15		15		15	mA
			Mil/Ind.						30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		160		150		140	mA
			Mil/Ind.						160	

Notes:

1. Pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 meas no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

6

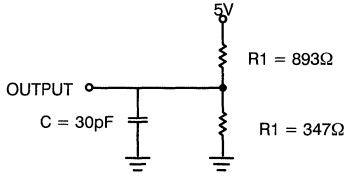
Electrical Characteristics Over the Operating Range[3](continued)

Parameter	Description	Test Conditions		7B134–35 7B135–35 7B1342–35 Min.	7B134–35 7B135–35 7B1342–35 Max.	7B134–55 7B135–55 7B1342–55 Min.	7B134–55 7B135–55 7B1342–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		210		210	mA
			Mil/Ind.		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		90		90	mA
			Mil/Ind.		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		135		135	mA
			Mil/Ind.		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		15		15	mA
			Mil/Ind.		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		130		130	mA
			Mil/Ind.		140		140	

Capacitance[5]

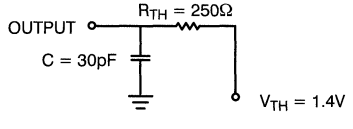
Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



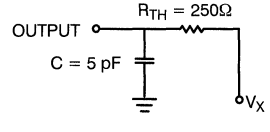
(a) Normal Load (Load 1)

1342–5



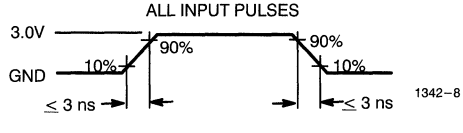
(b) Thévenin Equivalent (Load 1)

1342–6



(c) Three-State Delay (Load 3)

1342–7



1342–8

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. For all packages except DIP and cerDIP (D26, P25), which have maximums of C_{IN} = 15 pF, C_{OUT} = 15 pF.

Switching Characteristics Over the Operating Range[7, 8]

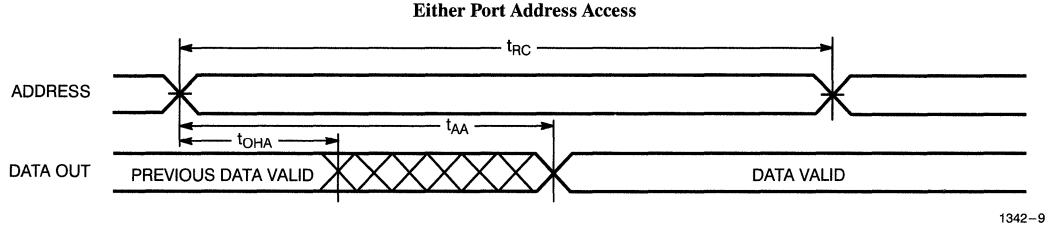
Parameter	Description	7B135–15 7B1342–15		7B134–20 7B135–20 7B1342–20		7B134–25 7B135–25 7B1342–25		7B134–35 7B135–35 7B1342–35		7B134–55 7B135–55 7B1342–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		55		ns
t_{AA}	Address to Data Valid		15		20		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		15		20		25	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		3		3		ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z		10		13		15		20		25	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z		10		13		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		25		35		55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15		20		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		30		50		ns
t_{AW}	Address Set-Up to Write End	12		15		20		30		50		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		15		20		25		50		ns
t_{SD}	Data Set-Up to Write End	10		13		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		10		13		15		20		25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		3		ns
t_{WDD}[11]	Write Pulse to Data Delay		30		40		50		60		70	ns
t_{DDD}[11]	Write Data Valid to Read Data Valid		25		30		30		35		40	ns
SEMAPHORE TIMING[12]												
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		15		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		5		ns

Notes:

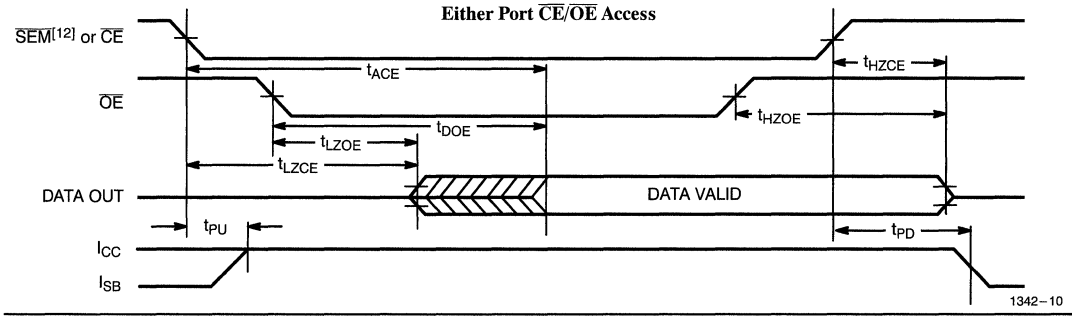
7. See the last page of this specification for Group A subgroup testing information.
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
12. Semaphore timing applies only to CY7B1342.

Switching Waveforms

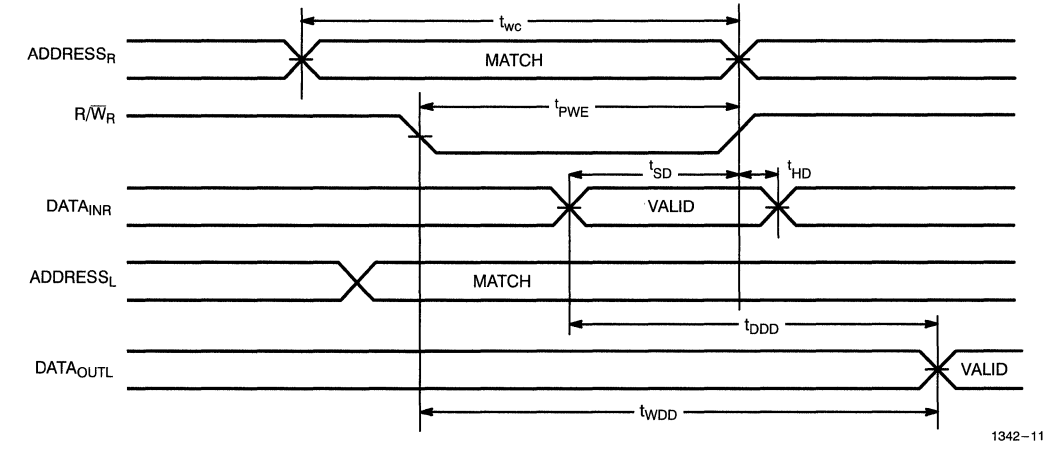
Read Cycle No. 1[13, 14]



Read Cycle No. 2[13, 15]



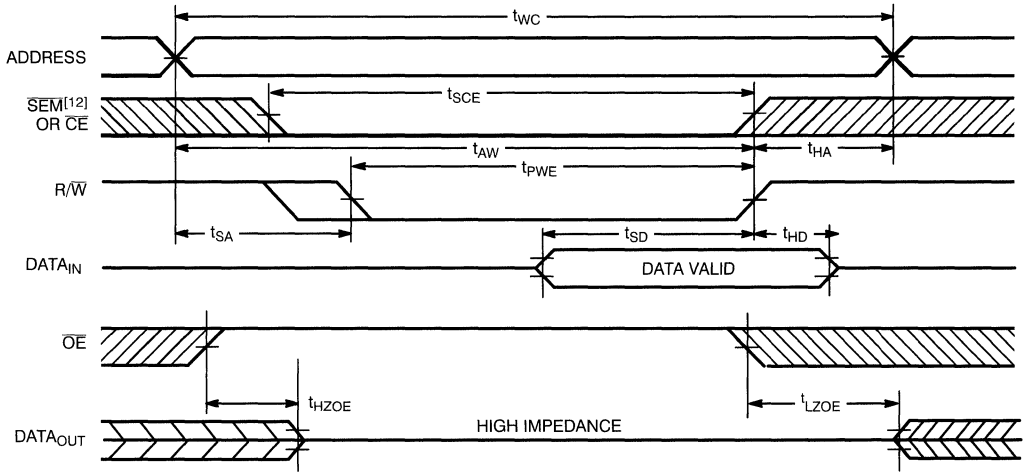
Read Timing with Port-to-Port Delay[16]



Notes:
13. R/$\overline{W}$ is HIGH for read cycle.
14. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. $\overline{CE}_L$ = $\overline{CE}_R$ =LOW; R/$\overline{W}_L$ = HIGH

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[17, 18, 19]



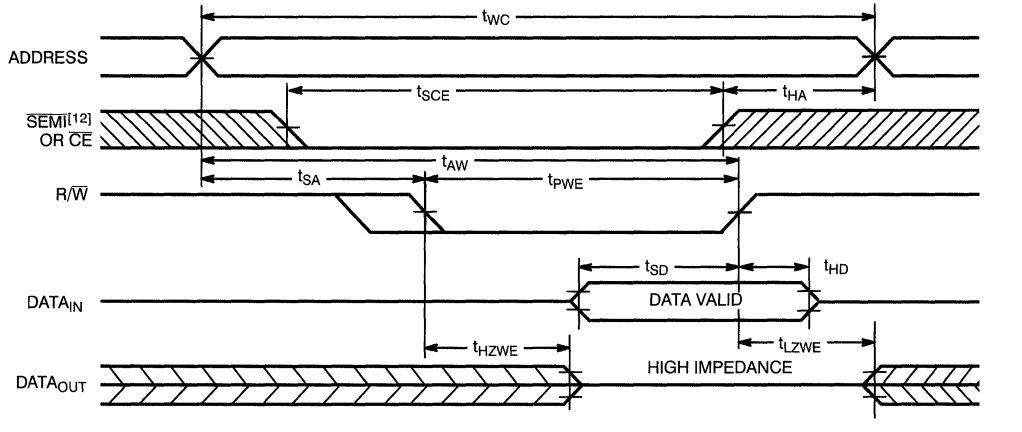
Notes:

17. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. R/$\overline{W}$ must be HIGH during all address transactions.
19. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.

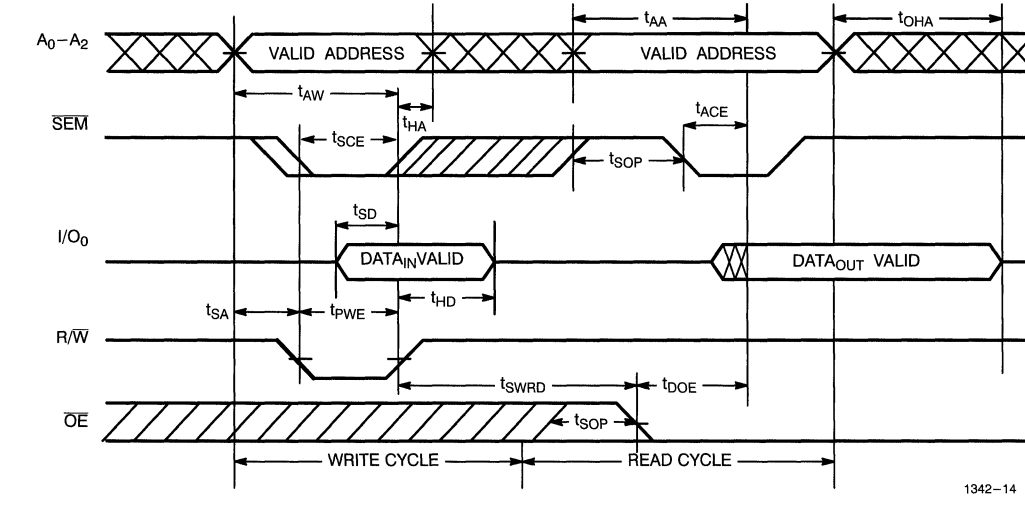
6

Switching Waveforms (continued)

Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[18, 20]



Semaphore Read After Write Timing, Either Side (CY7B1342 only)[21]

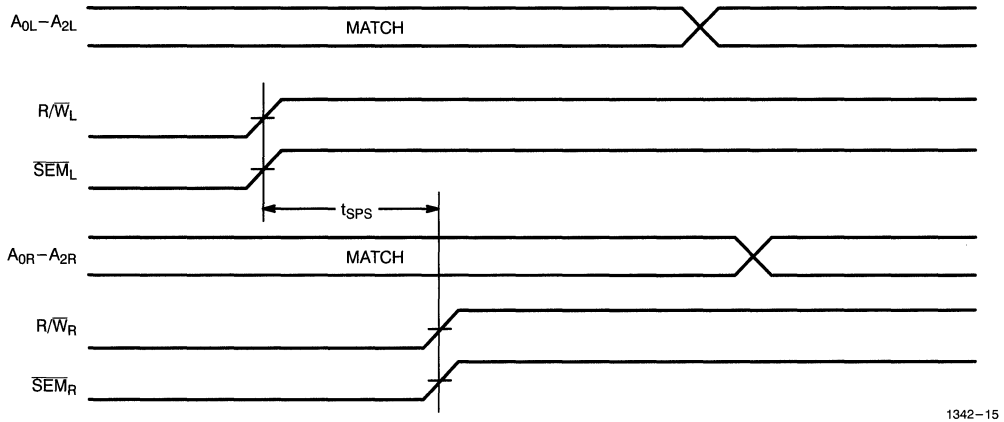


Notes:

20. Data I/O pins enter high-impedance when $\overline{OE}$ is held LOW during write.
21. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued)

Timing Diagram of Semaphore Contention (CY7B1342 only)[22, 23, 24]



Notes:
22. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
23. Semaphores are reset (available to both ports) at cycle start.
24. If t_{SPS} is violated, it is guaranteed that only one side will gain access to the semaphore.

Architecture

The CY7B134 and CY7B135 consist of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/W). Two semaphore control pins exist for the CY7B1342 ($\overline{SEM}_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. Since there is no on-chip arbitration, the user must be sure that a specific location will not be accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 timing diagram) or the R/$\overline{W}$ pin (see Write Cycle No. 2 timing diagram). Data can be written t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for write operations are summarized in *Table 1.*

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B1342 wishes to access a semaphore, the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin. Required inputs for read operations are summarized in *Table 1.*

Semaphore Operation

The CY7B1342 provides eight semaphore latches which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches. $\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. *Table 2* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side will gain access to the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

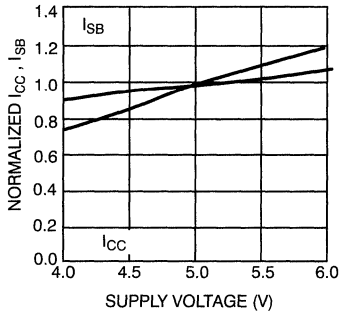
Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read $Data_{IN}$ Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Semaphore Operation Example

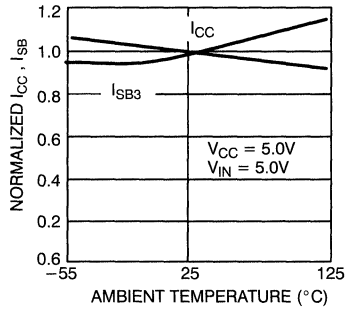
Function	I/O_0 Left	I/O_0 Right	Status
No Action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to Semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

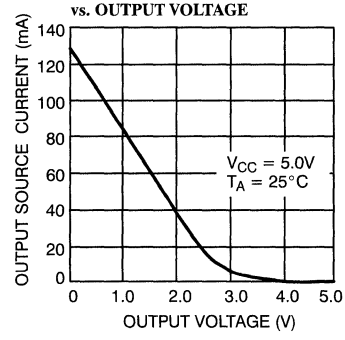
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



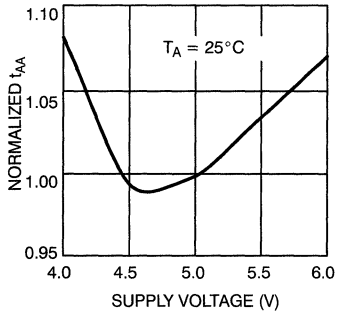
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



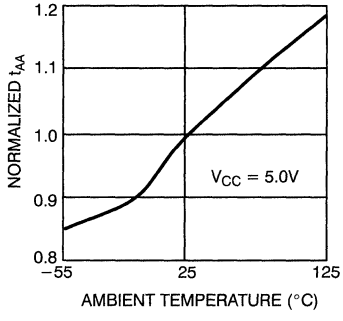
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



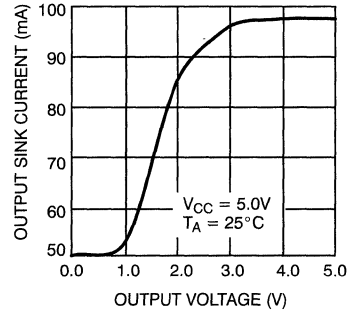
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



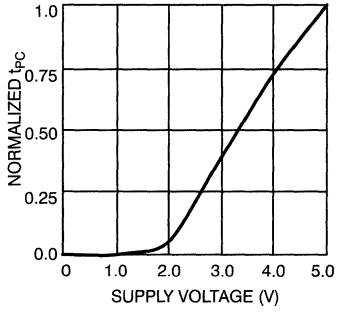
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



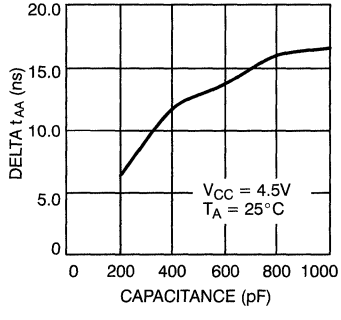
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



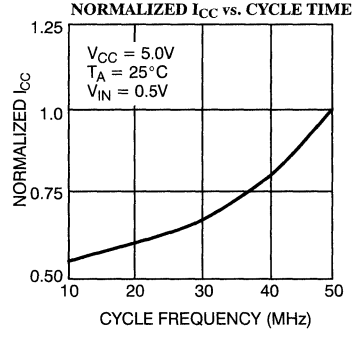
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7B134–20PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
25	CY7B134–25PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–25PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–25DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
35	CY7B134–35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134–35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7B134–55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134–55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B135–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B135–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B135–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B135–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135–35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B135–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7B1342–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B1342–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B1342–25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342–25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B1342–35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342–35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B1342–55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342–55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
SEMAPHORE CYCLE	
t_{SOD}	7, 8, 9, 10, 11
t_{SWRD}	7, 8, 9, 10, 11
t_{SPS}	7, 8, 9, 10, 11

Document #: 38-00161-D

CY7B136
CY7B146

2K x 8 Dual-Port Static RAM

Features

- **0.8-micron BiCMOS for high performance**
- **Automatic power-down**
- **TTL compatible**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Fully asynchronous operation**
- **Master CY7B136 easily expands data bus width to 16 or more bits using slave CY7B146**
- **$\overline{\text{BUSY}}$ output flag on CY7B136; $\overline{\text{BUSY}}$ input on CY7B146**
- **$\overline{\text{INT}}$ flag for port-to-port communication**

Functional Description

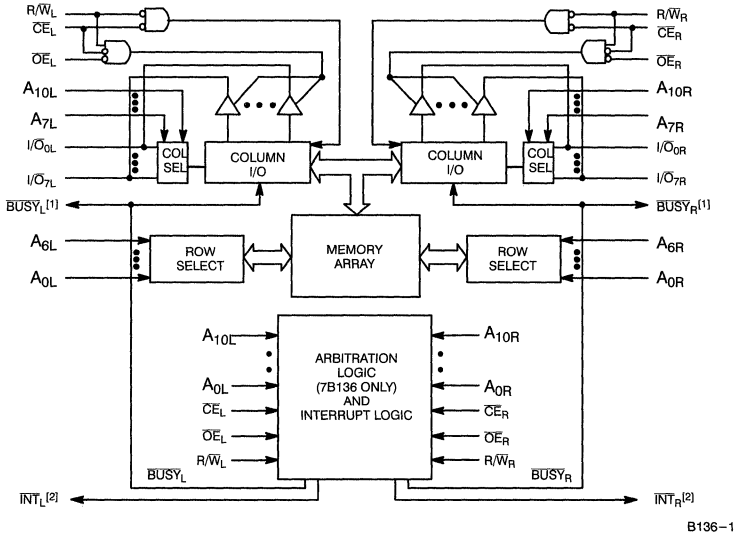
The CY7B136 and CY7B146 are high-speed BiCMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7B136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7B146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{\text{CE}}$), write enable (R/$\overline{\text{W}}$), and output enable ($\overline{\text{OE}}$). $\overline{\text{BUSY}}$ flags are provided on each port. In addition, an interrupt flag ($\overline{\text{INT}}$) is provided on each port. $\overline{\text{BUSY}}$ signals that the port is trying to access the same location currently being accessed by the other port. The $\overline{\text{INT}}$ is an interrupt flag indicating that data has been placed in a unique location (7FF for the right port and 7FE for the left port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{\text{CE}}$) pins.

The CY7B136/CY7B146 are available in 52-lead PLCC.

Logic Block Diagram

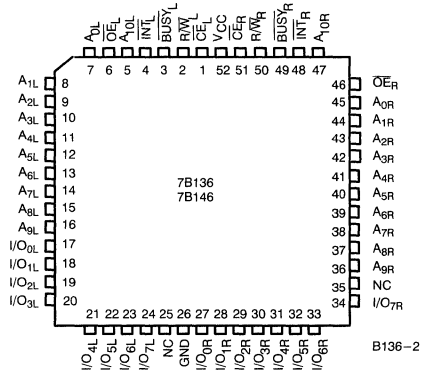


Notes:

1. CY7B136 (Master): $\overline{\text{BUSY}}$ is an open drain output and requires a pull-up resistor.
   CY7B146 (Slave): $\overline{\text{BUSY}}$ is an input.
2. Open drain outputs; pull-up resistor required.

Pin Configuration

52-Lead PLCC
Top View



Selection Guide

		7B136–15 7B146–15	7B136–20 7B146–20
Maximum Access Time (ns)		15	20
Maximum Operating Current (mA)	Com'l/Ind	260	240
Maximum Standby Current (mA)	Com'l/Ind	110	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 52 to Pin 26) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

6

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B136–15 7B146–15 Min.	7B136–15 7B146–15 Max.	7B136–20 7B146–20 Min.	7B136–20 7B146–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4	V
		I_{OL} = 16.0 mA[4]			0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[5]	Com'l		260		240	mA
			Ind				300	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		110		100	mA
			Ind				105	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		165		155	mA
			Ind				180	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15	mA
			Ind				30	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		160		150	mA
			Ind				170	

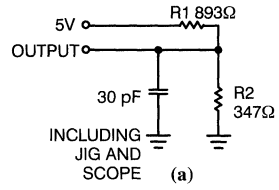
Capacitance[6]

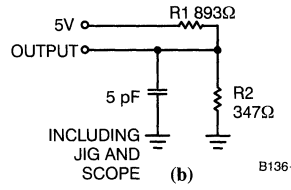
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

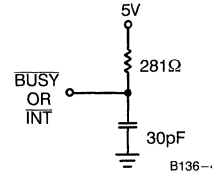
3. See the last page of this specification for Group A subgroup testing information.
4. $\overline{BUSY}$ and $\overline{INT}$ pins only.
5. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



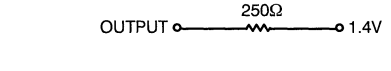


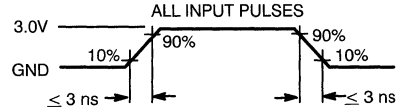
B136-3



B136-4

BUSY Output Load (CY7B136 ONLY)





Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B136–15 7B146–15 Min.	7B136–15 7B146–15 Max.	7B136–20 7B146–20 Min.	7B136–20 7B146–20 Max.	Unit
READ CYCLE						
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address to Data Valid[8]		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		10		13	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		10		13	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		10		13	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20	ns
WRITE CYCLE[11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		ns
t_{AW}	Address Set-Up to Write End	12		15		ns
t_{HA}	Address Hold from Write End	2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		ns
t_{SD}	Data Set-Up to Write End	10		13		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		10		13	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	3		3		ns

Notes:

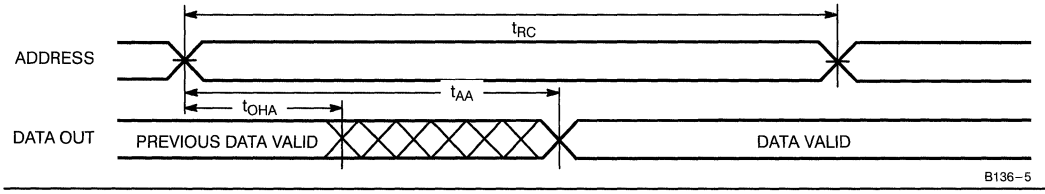
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3, 7] (continued)

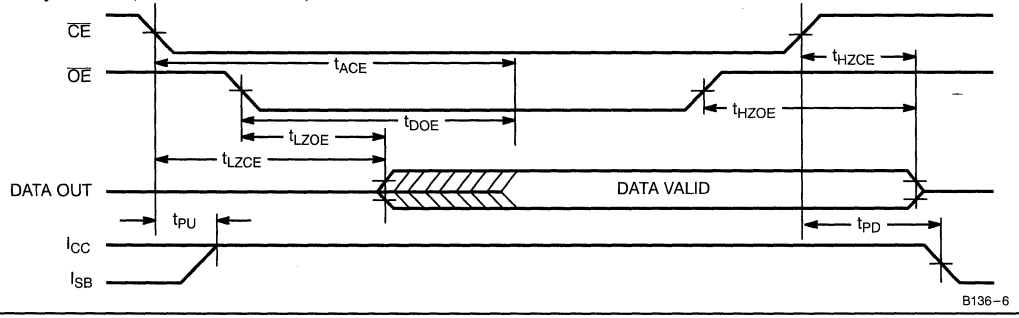
Parameter	Description	7B136–15 7B146–15		7B136–20 7B146–20		Unit
		Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING						
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[12]		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[12]		15		20	ns
t_{PS}	Port Set Up for Priority	5		5		ns
t_{WB}[13]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		15		20	ns
t_{DDD}	Write Data Valid to Read Data Valid[14]		25		30	ns
t_{WDD}	Write Pulse to Data Delay[14]		30		40	ns
INTERRUPT TIMING						
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns

Switching Waveforms

Read Cycle No. 1 (Either Port–Address Access[15, 16]



Read Cycle No. 2 (Either Port–$\overline{CE}$/$\overline{OE}$)[15, 17]

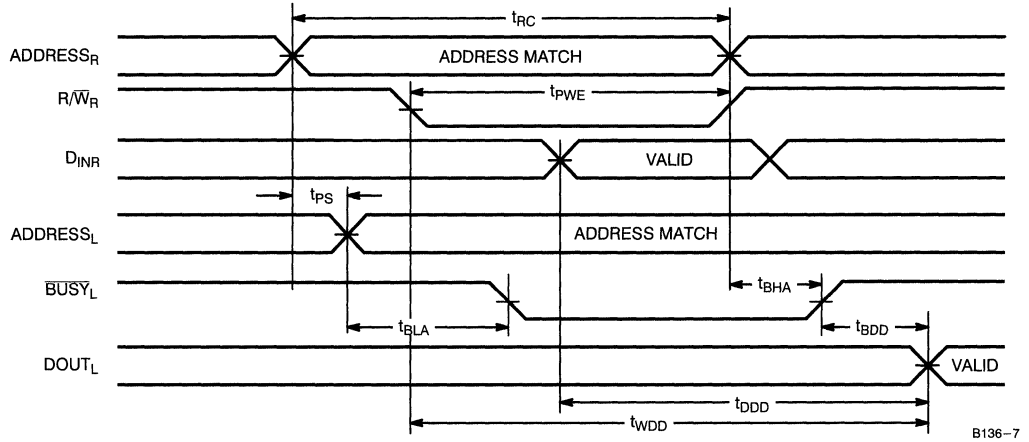


Notes:

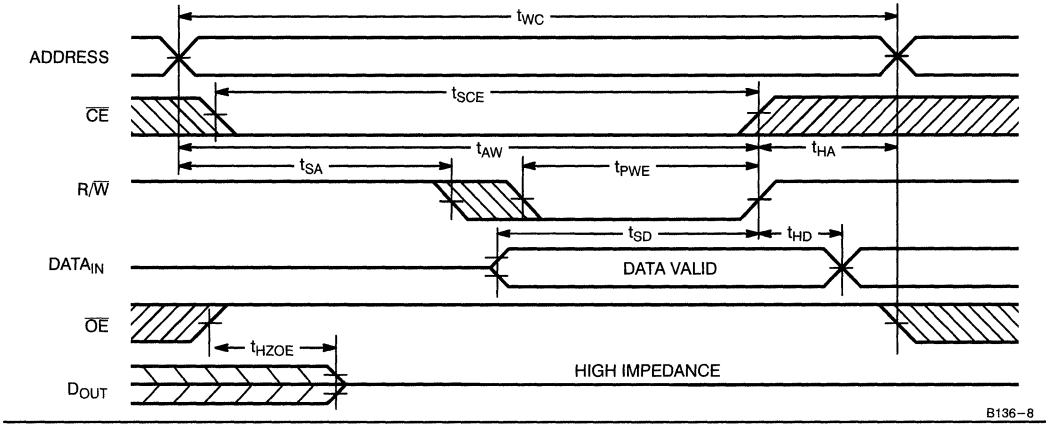
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7B146 only.
14. For information on port-to-port delay through RAM cells, from writing port to reading port, refer to the Read Timing with Port-to-Port Delay timing diagram.
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Read Cycle No. 3 (Read with $\overline{BUSY}$ Master: CY7B136)



Write Cycle No.1 ($\overline{OE}$ Three-States Data I/Os – Either Port) [11, 18]

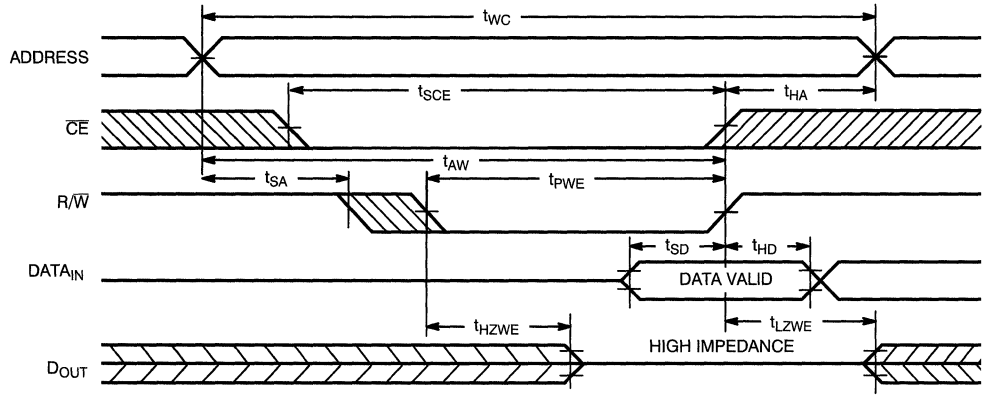


Note:

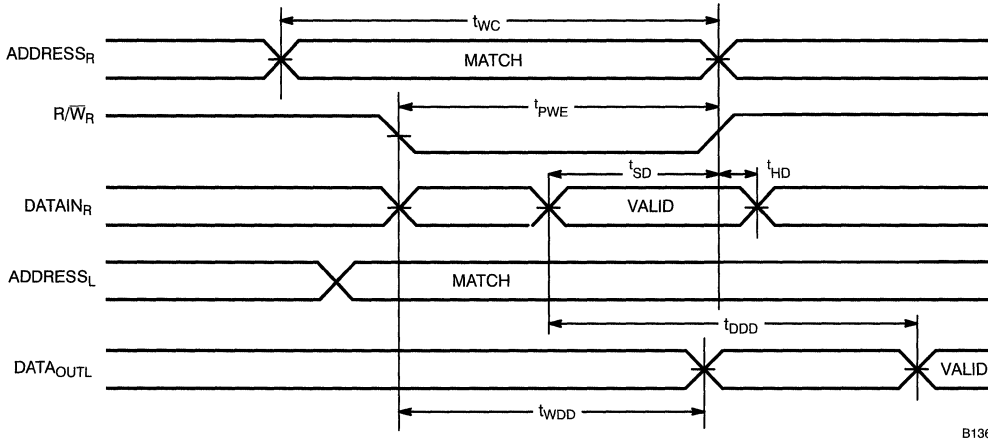
18. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

Switching Waveforms (continued)

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os – Either Port)[11, 19]



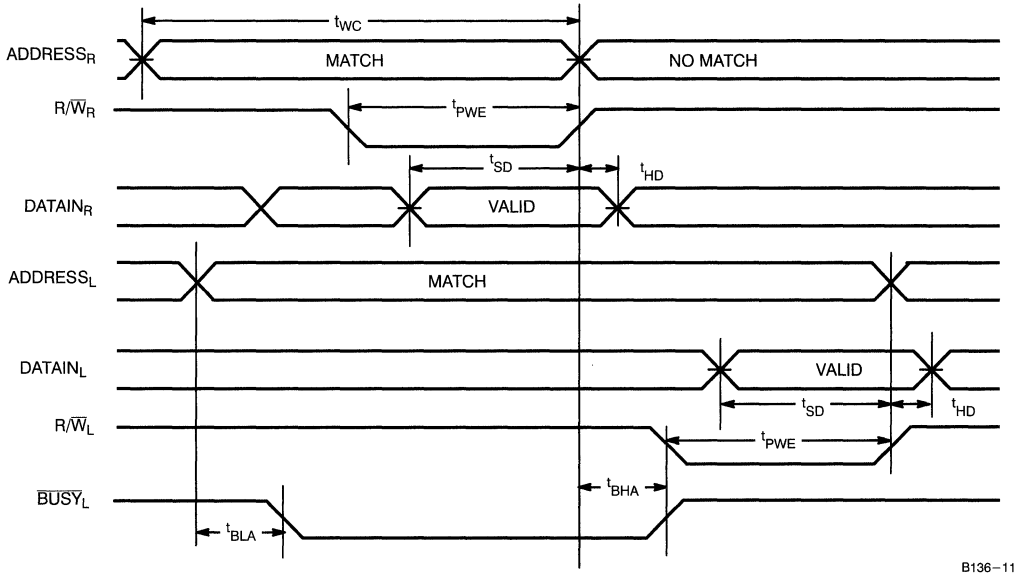
Read Timing with Port-to-Port Delay ($\overline{CE}_L = \overline{CE}_R$ = LOW, $\overline{BUSY}$ = HIGH for the Writing Port)



Note:
19. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

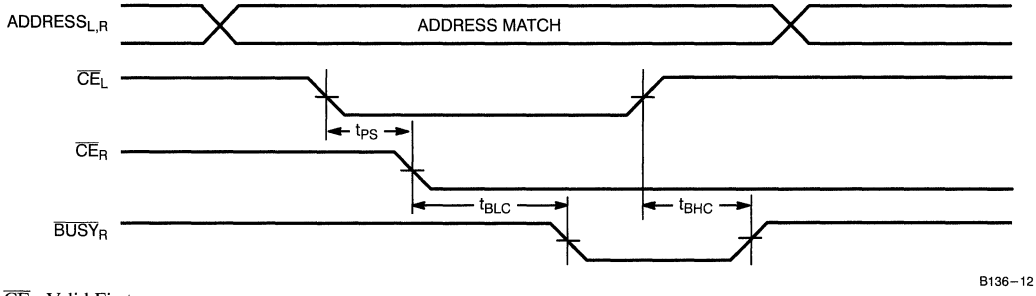
Switching Waveforms (continued)

Write Timing with Port-to-Port Delay ($\overline{CE}_L$ = $\overline{CE}_R$ = LOW)

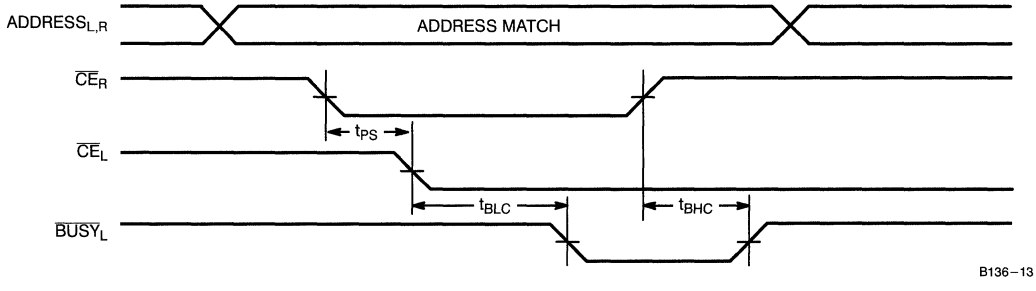


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



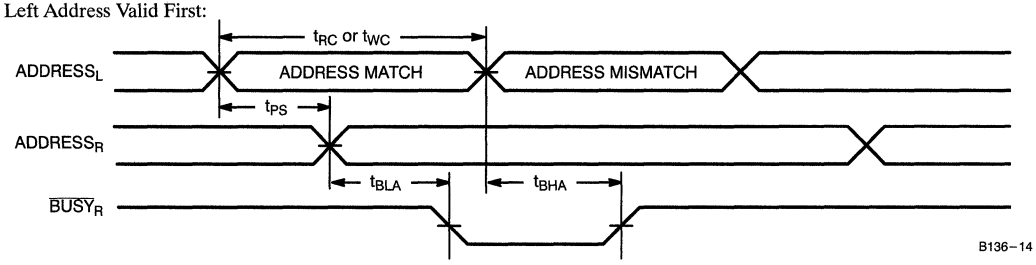
$\overline{CE}_R$ Valid First:



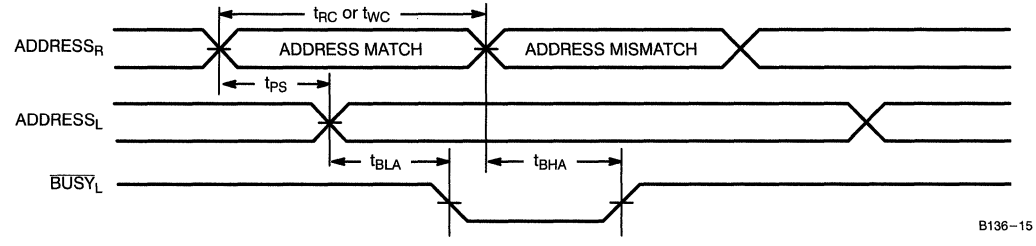
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

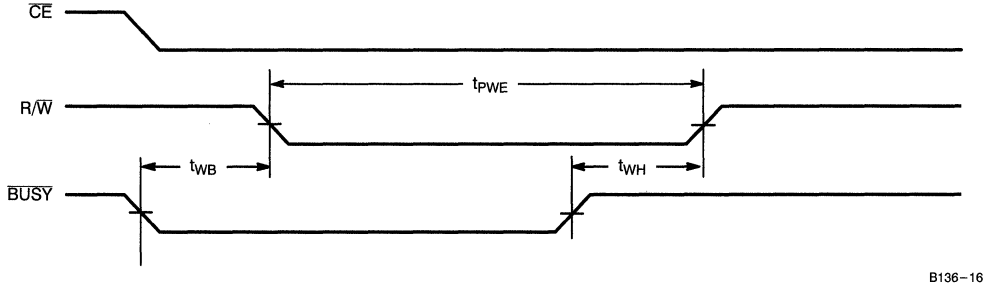
Left Address Valid First:



Right Address Valid First:

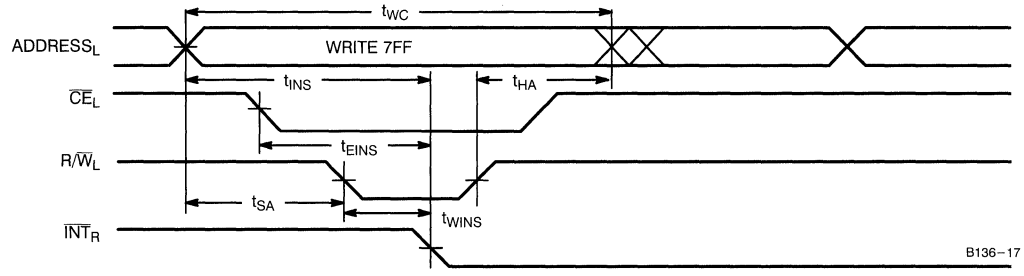


Busy Timing Diagram No. 3 (Write with $\overline{BUSY}$, Slave: CY7B146)



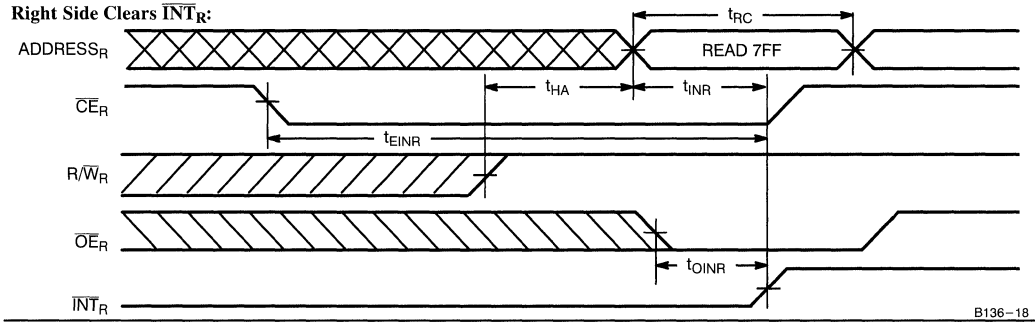
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$:



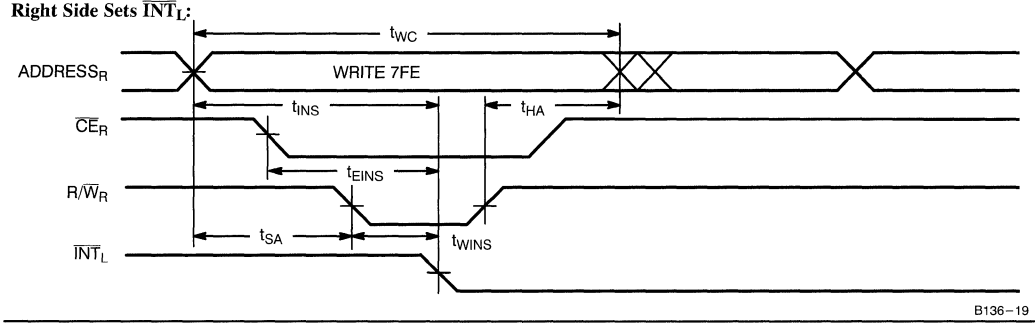
B136-17

Right Side Clears $\overline{INT}_R$:



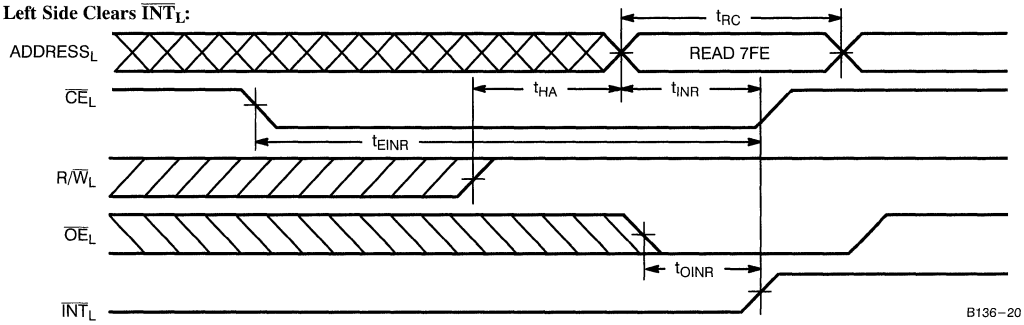
B136-18

Right Side Sets $\overline{INT}_L$:



B136-19

Left Side Clears $\overline{INT}_L$:



B136-20

Architecture

The CY7B136 (master) and CY7B146 (slave) are 2048-byte deep dual-port RAMs, with two independent sets of address signals, common I/O data signals, and control signals. By convention, the two ports are called the left port and the right port. The subscript R or L on the signal name identifies the port.

The upper two memory locations (7FF, 7FE) are special locations and may be used as "mailboxes" for passing messages between the ports. Location 7FF is the mailbox for the right port and location 7FE is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner of the mailbox. When the owner reads the mailbox, the interrupt is reset.

The address and control signals provide independent, asynchronous, random access to any location in the memory. It is possible that both ports may attempt to access the same memory location at the same time. If this contention occurs, a circuit in the master called an arbiter decides which port temporarily "owns" the memory location. The losing port receives a BUSY signal, which notifies it that the memory location is owned by the other port and that the operation it attempted to perform may not be successful.

The two BUSY signals are outputs from the master and inputs to the slave.

Contention, Arbitration and Resolution—The Significance of BUSY

When contention occurs, the arbiter decides which port wins (owns) the memory location and which port loses. The decision is on a "first-come-first-served" basis. In order for contention to occur, both ports must address the same memory location and have their respective chip enables active. If one port precedes the other by an amount of time greater than or equal to t_{PS} (port set-up for priority;equal to five nanoseconds) it is guaranteed to win the arbitration. If contention occurs within the t_{PS} interval, it is not possible to predict which port will win, but one will win and the other will lose.

There are two ports and each may be either reading or writing, and each may win or lose, so there are eight combinations. They are listed in *Table 1* and identified as cases one through eight. In cases one and two, both ports are reading, the losing port receives a BUSY, the read is allowed to occur, and the data read by both ports is valid. In case three, the left port wins and reads valid data, and the write attempted by the right port is inhibited. In cases four and five, when the winning port is writing, the write is completed, but the data read by the losing port may be invalid. Case six is similar to case three; the right port successfully reads and the write attempt by the left port is inhibited. In cases seven and eight the winning port successfully writes and the attempted write by the losing port is inhibited.

In cases four and five, where the losing port is reading, if the port signals are asynchronous to each other, the data read may be the old data, the new data, or some random combination of the two sets of data. In cases seven and eight the losing port is prevented from writing. The commonality between these four cases is that the losing port receives a busy signal, which tells it that either (1) the operation it attempted was not successful, or (2) that the data it read may not be valid. In either situation, the operation should be repeated after the busy signal becomes inactive.

Flow-Through Operation

The CY7B136/146 have a flow-through architecture that facilitates repeating (actually extending) an operation when a BUSY is received by a losing port. The BUSY signal should be interpreted as a NOT READY. If a BUSY to a port is active, the port should wait for BUSY to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Read Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either t_{WDD} after the falling edge of the write strobe of the left port, or t_{DDD} after the data being written becomes stable.

The timing diagram titled, "Write Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port wants to write to the same address. If the left port extends its write strobe for a minimum time of t_{PWE} after the BUSY signal to it goes inactive, its write will be successful; it writes over the data just written by the right port.

Data Bus Width Expansion Using Slaves

One master and as many slaves as necessary may be connected in parallel to expand the data bus width in byte increments.

Two masters must not be connected in parallel because, if the time interval between which they address the same location is less than t_{PS}, both could end up waiting for the other to release the BUSY to it.

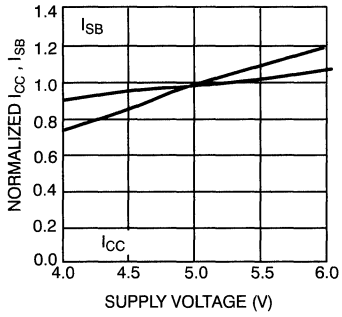
Therefore, only one master must arbitrate, and it can drive as many slaves as required. The write strobe to the slaves must be delayed an amount of time equal to at least t_{BLA}. This insures that the slave is not inadvertently written to before the outcome of the arbitration is determined.

Table 1. Operation

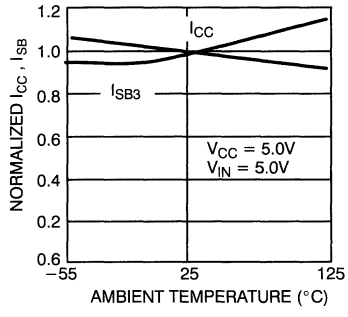
Case	Operation Port		Winning Port	Result
	L	R		
1	R	R	L	Both Read
2	R	R	R	Both Read
3	R	W	L	L Reads OK, R Write Inhibited
4	R	W	R	R Writes OK L Data May Be Invalid
5	W	R	L	L writes OK R Data May Be Invalid
6	W	R	R	R Reads OK L Write Inhibited
7	W	W	L	L Writes OK R Write Inhibited
8	W	W	R	R Writes OK L Write Inhibited

Typical DC and AC Characteristics

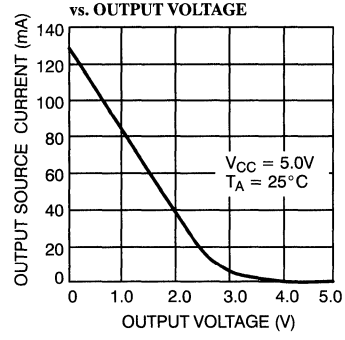
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



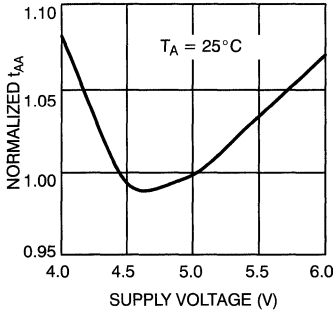
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



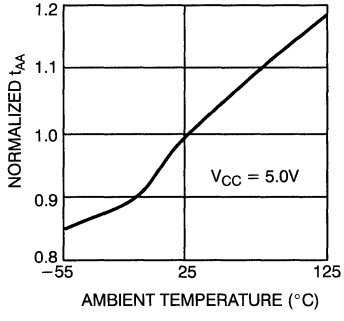
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



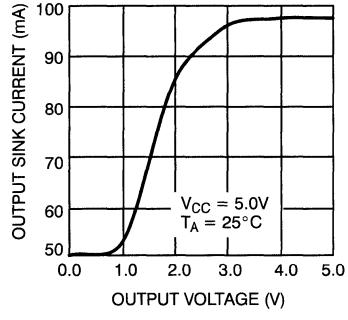
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



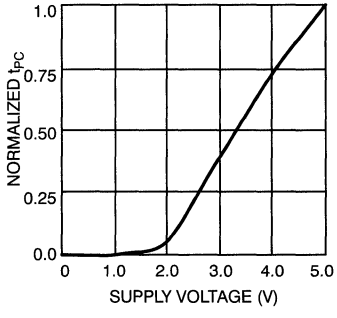
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



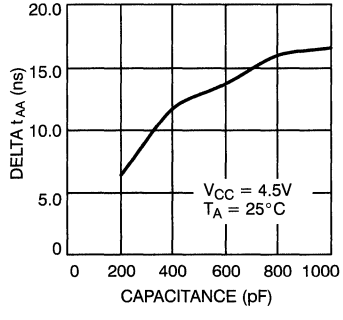
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



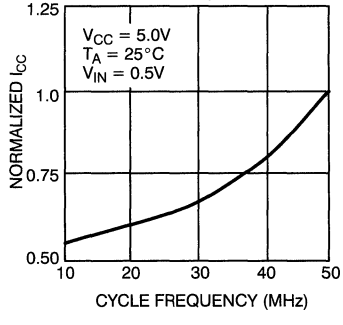
TYPICAL POWER–ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



6

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B136–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B136–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B136–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B146–15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B146–20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B146–20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Document #: 38–00464

CY7B138
CY7B139

4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (com'l)**
  - **— 25 ns (mil)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master /Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC/PGA**
- **TTL compatible**

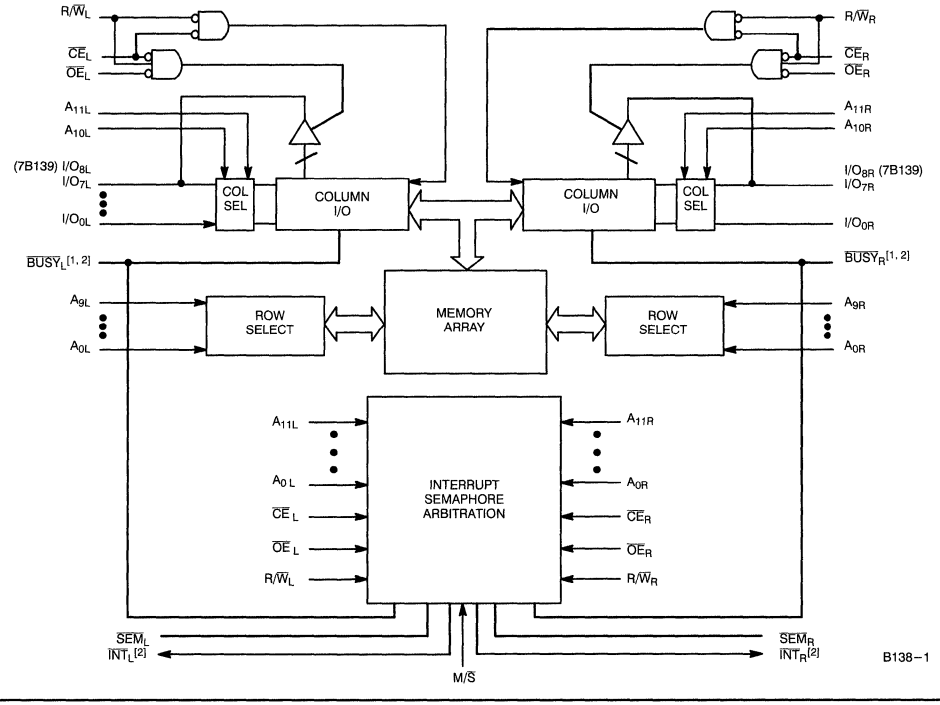
Functional Description

The CY7B138 and CY7B139 are high-speed BiCMOS 4K x 8 and 4K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B138/9 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B138/9 can be utilized as a stand-alone 32-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B138 and CY7B139 are available in 68-pin LCCs, and PLCCs.

Logic Block Diagram

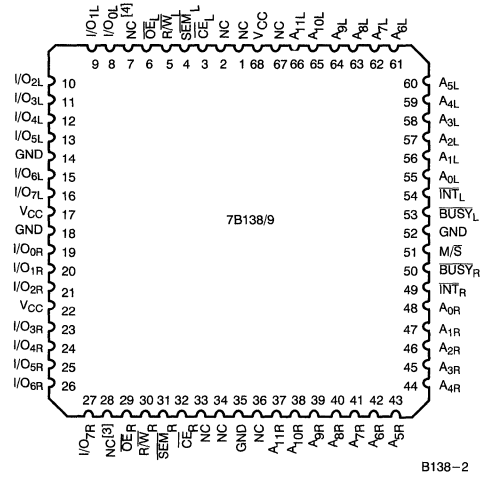


Notes:

1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

Pin Configurations

68-Pin LCC/PLCC
Top View



B138–2

Notes:
3. I/O_{8R} on the CY7B139.
4. I/O_{SL} on the CY7B139.

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location FFE and is cleared when left port reads location FFE. $\overline{INT}_R$ is set when left port writes location FFF and is cleared when right port reads location FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B138–15 7B139–15	7B138–25 7B139–25	7B138–35 7B139–35	7B138–55 7B139–55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military/Industrial		280	250	250
Maximum Standby Current for I_{SB1}(mA)	Commercial	110	95	90	90
	Military/Industrial		100	95	95

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[5] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[6]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B138−15 7B139−15 Min.	7B138−15 7B139−15 Max.	7B138−25 7B139−25 Min.	7B138−25 7B139−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		260		220	mA
			Mil/Ind				280	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		110		95	mA
			Mil/Ind				100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		165		145	mA
			Mil/Ind				180	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		160		140	mA
			Mil/Ind				160	

Notes:

5. Pulse width < 20 ns.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.
8. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

6

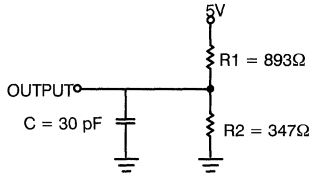
Electrical Characteristics Over the Operating Range[7] (continued)

Parameter	Description	Test Conditions		7B138–35 7B139–35 Min.	7B138–35 7B139–35 Max.	7B138–55 7B139–55 Min.	7B138–55 7B139–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		130		130	mA
			Mil/Ind		140		140	

Capacitance[9]

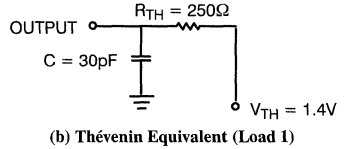
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms



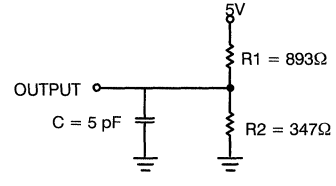
(a) Normal Load (Load 1)

B138–3



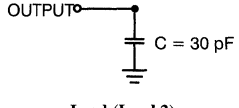
(b) Thévenin Equivalent (Load 1)

B138–4



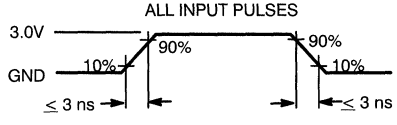
(c) Three-State Delay (Load 3)

B138–5



Load (Load 2)

B138–6



B138–7

Note:
9. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[7, 10]

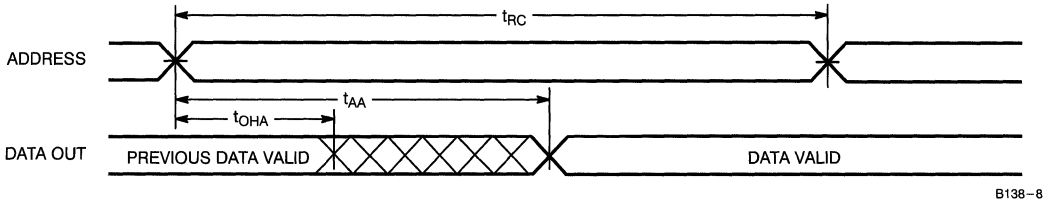
Parameter	Description	7B138–15 7B139–15		7B138–25 7B139–25		7B138–35 7B139–35		7B138–55 7B139–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[11, 12]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[11, 12]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[11, 12]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[11, 12]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		40		ns
t_{AW}	Address Set-Up to Write End	12		20		30		40		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		15		20		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[12]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[12]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[13]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid		25		30		35		40	ns
BUSY TIMING[14]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		40	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		40	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		35	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		40		ns
t_{BDD}[15]	$\overline{BUSY}$ HIGH to Data Valid		Note 15		Note 15		Note 15		Note 15	ns
INTERRUPT TIMING[14]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Notes:

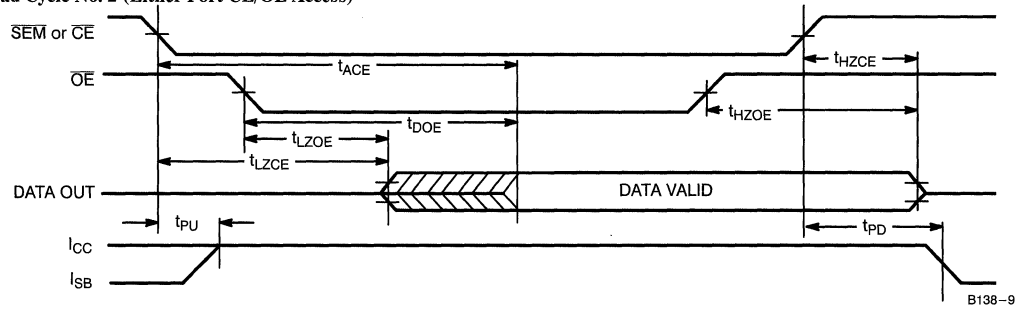
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 3.
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.

Switching Waveforms

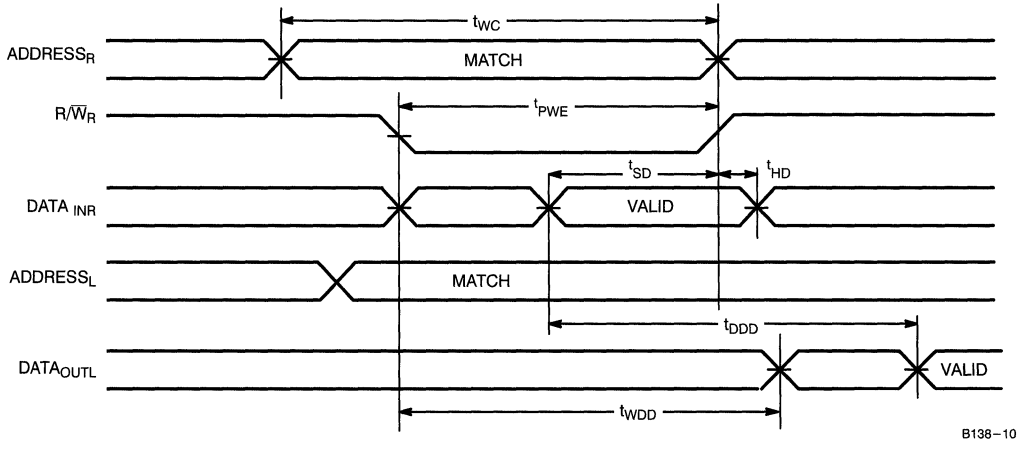
Read Cycle No. 1 (Either Port Address Access)[16, 17]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [16, 18, 19]



Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[20, 21]

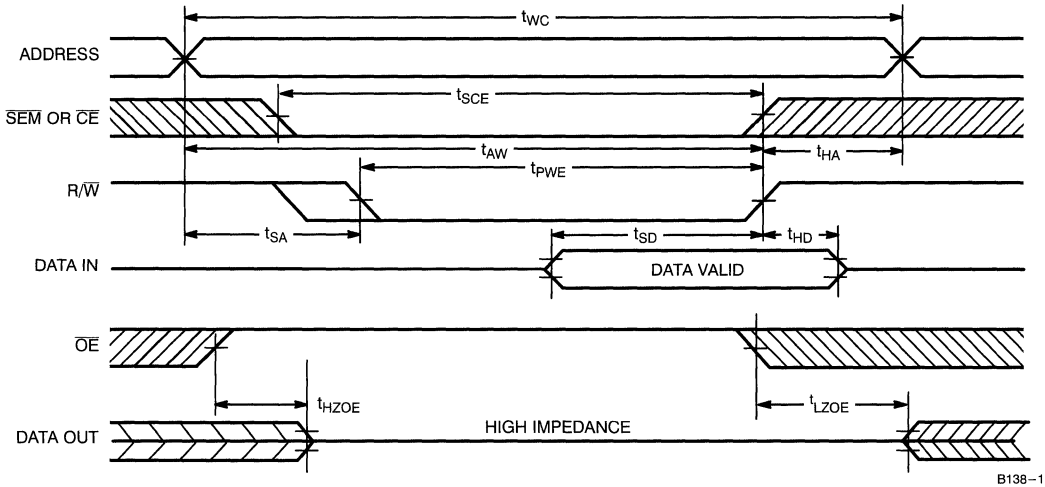


Notes:

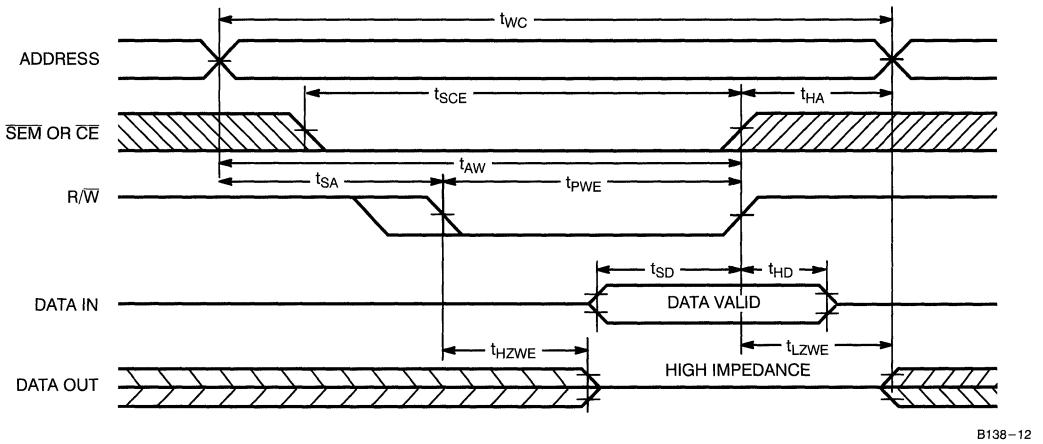
15. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).
16. R/$\overline{W}$ is HIGH for read cycle.
17. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
20. $\overline{BUSY}$ = HIGH for the writing port.
21. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[22, 23, 24]



Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[22, 24, 25]

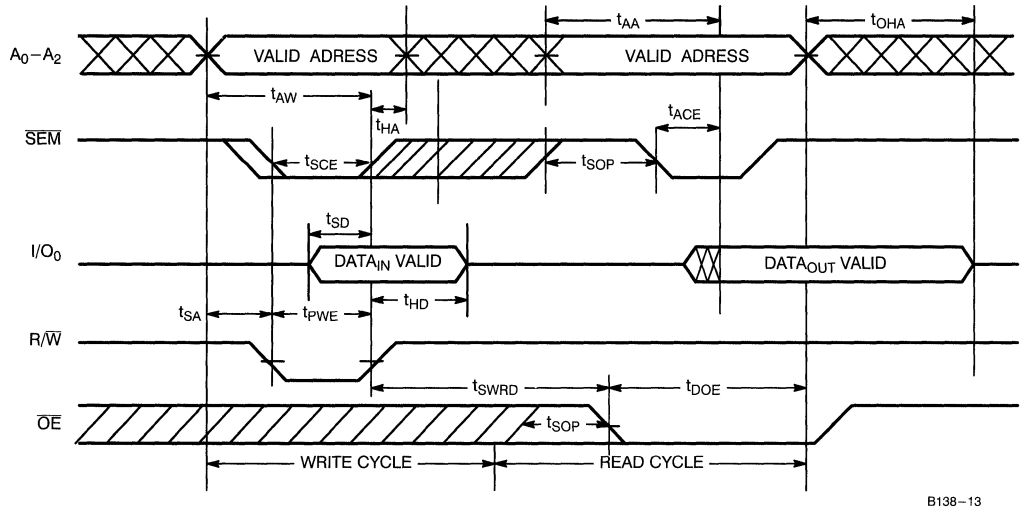


Notes:

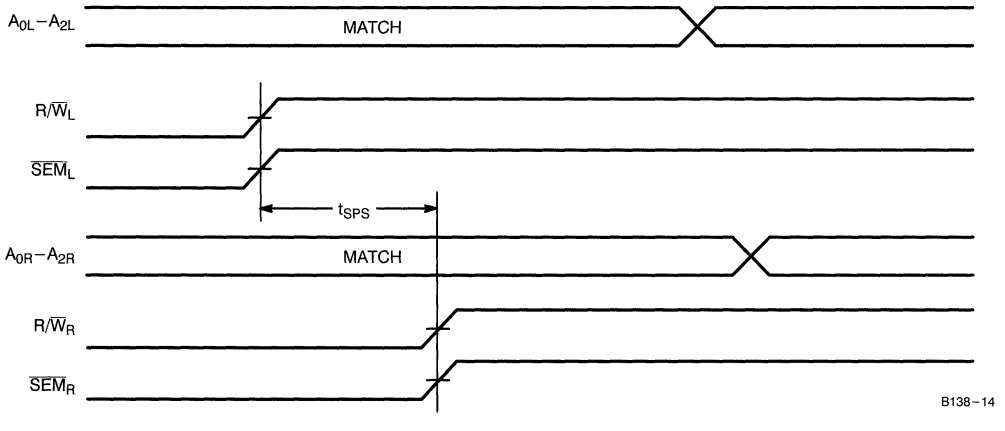
22. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
24. R/$\overline{W}$ must be HIGH during all address transitions.
25. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[26]



Timing Diagram of Semaphore Contention[27, 28, 29]

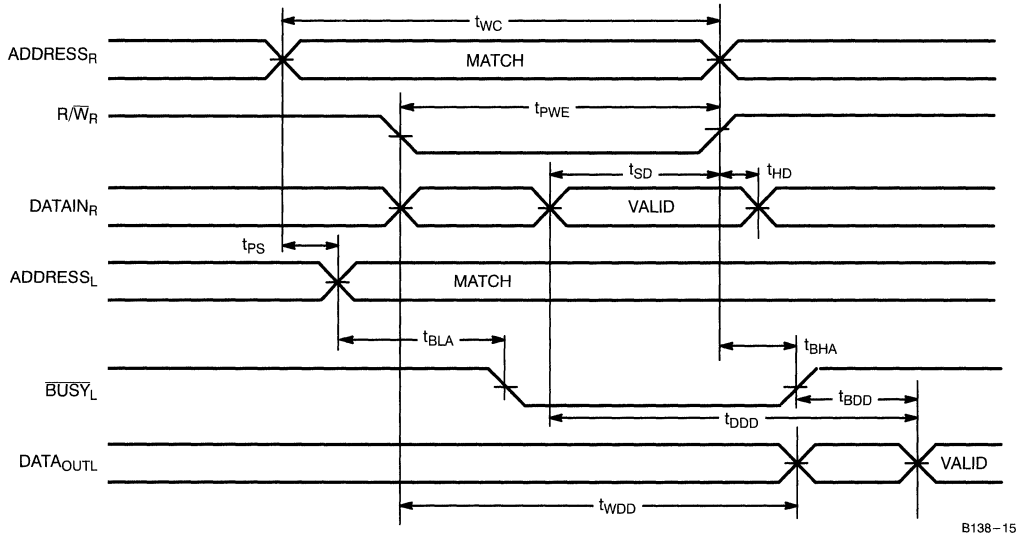


Notes:

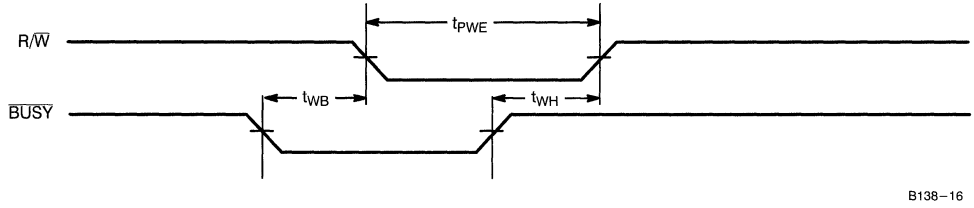
26. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
27. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
28. Semaphores are reset (available to both ports) at cycle start.
29. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[21]



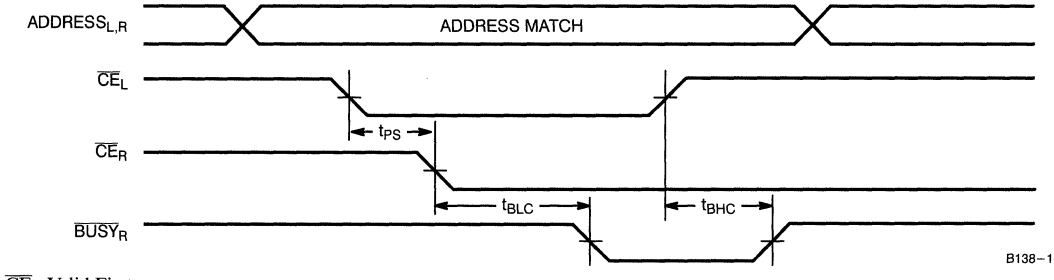
Write Timing with Busy Input (M/$\overline{S}$=LOW)



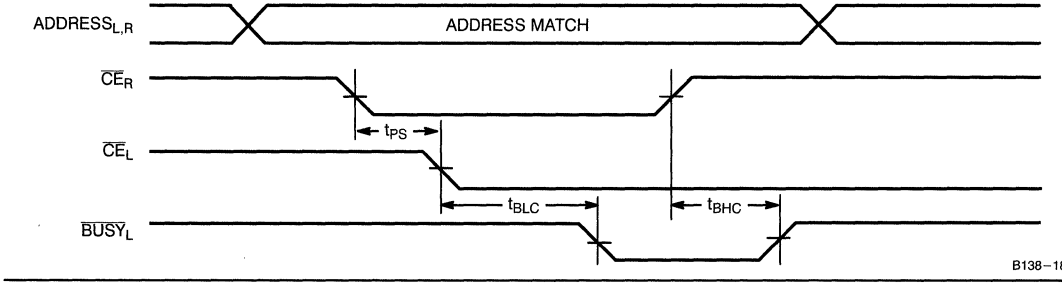
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[30]

$\overline{CE}_L$ Valid First:

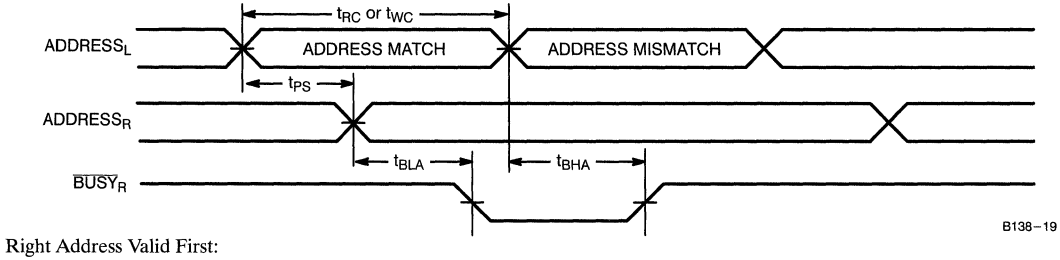


$\overline{CE}_R$ Valid First:

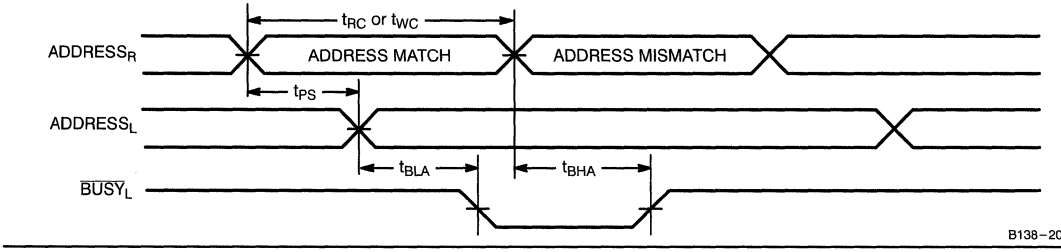


Busy Timing Diagram No. 2 (Address Arbitration)[30]

Left Address Valid First:



Right Address Valid First:

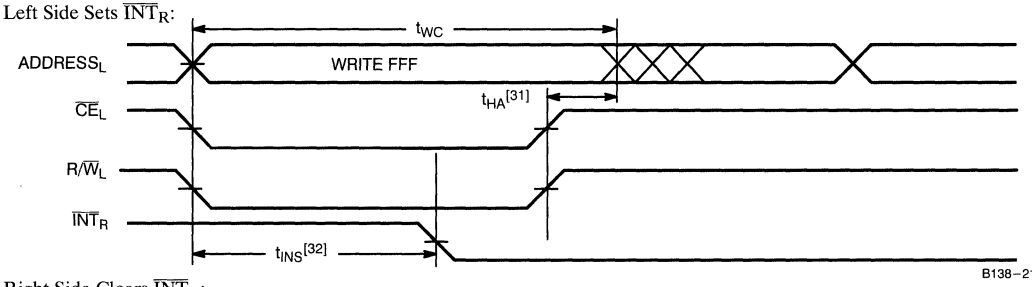


Note:
30. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

Switching Waveforms (continued)

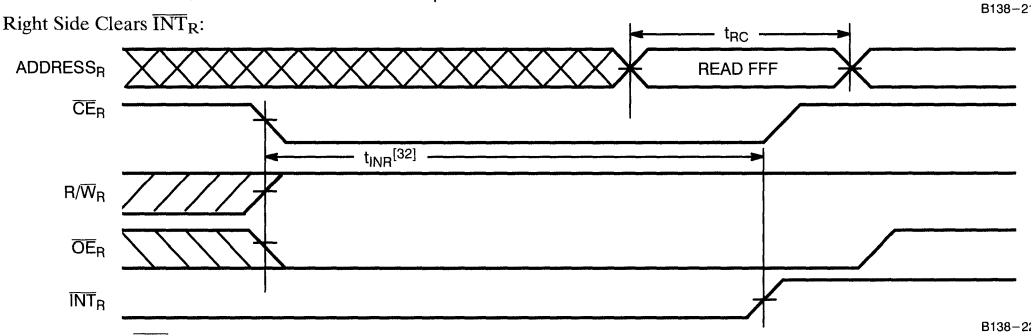
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$:



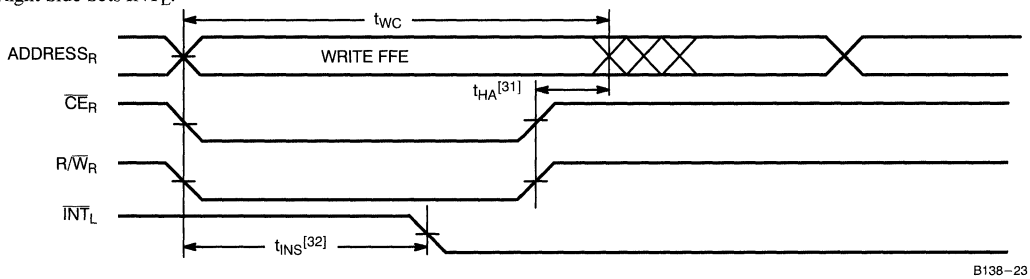
B138-21

Right Side Clears $\overline{INT}_R$:



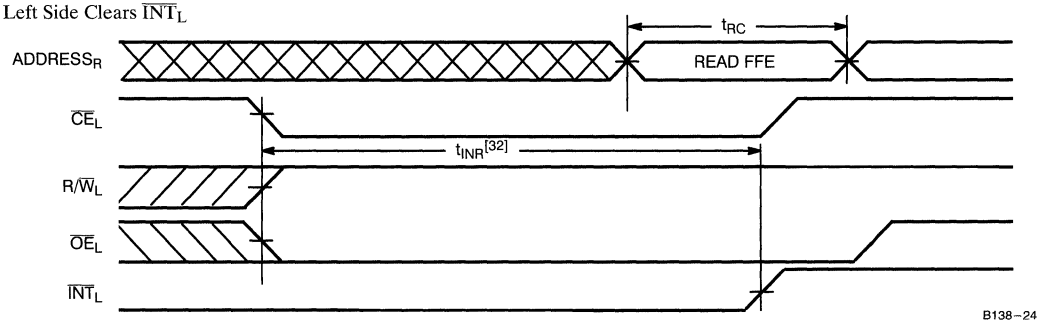
B138-22

Right Side Sets $\overline{INT}_L$:



B138-23

Left Side Clears $\overline{INT}_L$



B138-24

Notes:

31. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
32. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

Architecture

The CY7B138/9 consists of an array of 4K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B138/9 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B138/9 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7B138/9 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location FFF, the right port's interrupt flag ($\overline{INT}_R$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT}_L$) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT}_R$ and $\overline{INT}_L$ are push-pull outputs and do not require pull-up resistors to operate. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B138/9 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B138/9 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the a semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into themn at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

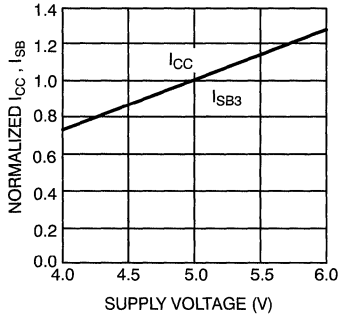
	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	FFE	X
Reset Left $\overline{INT}$	X	L	L	FFE	H	X	X	X	X	X
Set Right $\overline{INT}$	L	L	X	FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	FFF	H

Table 3. Semaphore Operation Example

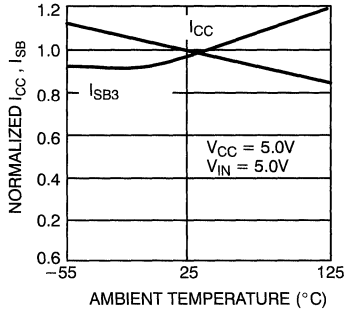
Function	I/O 0 Left	I/O 0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

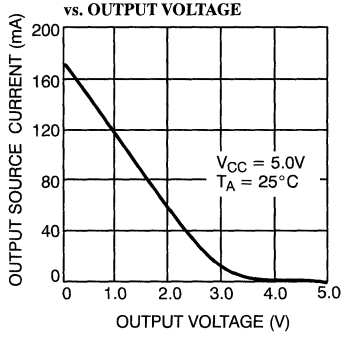
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



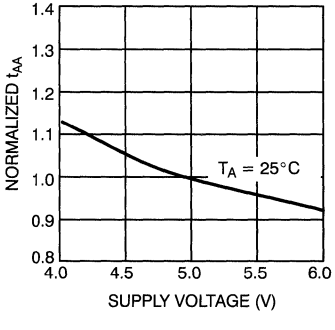
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



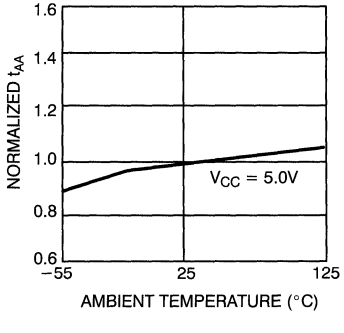
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



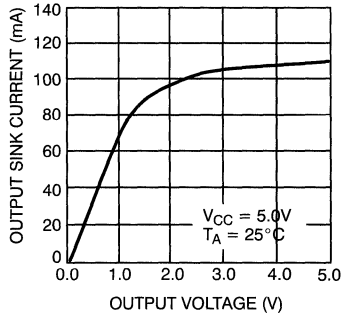
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



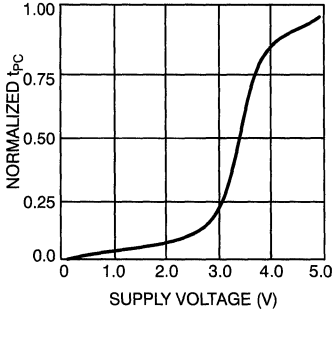
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



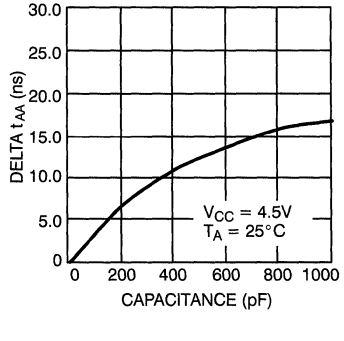
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



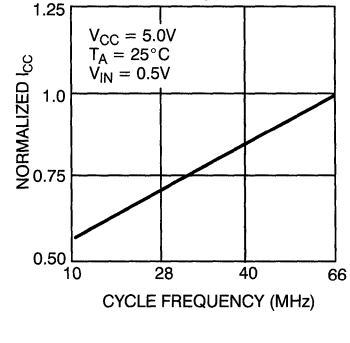
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B138–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B138–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B138–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B138–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B138–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B138–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7B139–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B139–25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B139–35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B139–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B139–55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B139–55JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

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CY7B144
CY7B145

8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC, 64-pin and 80-pin TQFP**
- **TTL compatible**
- **Pin compatible and functionally equivalent to IDT7005 and IDT7015**

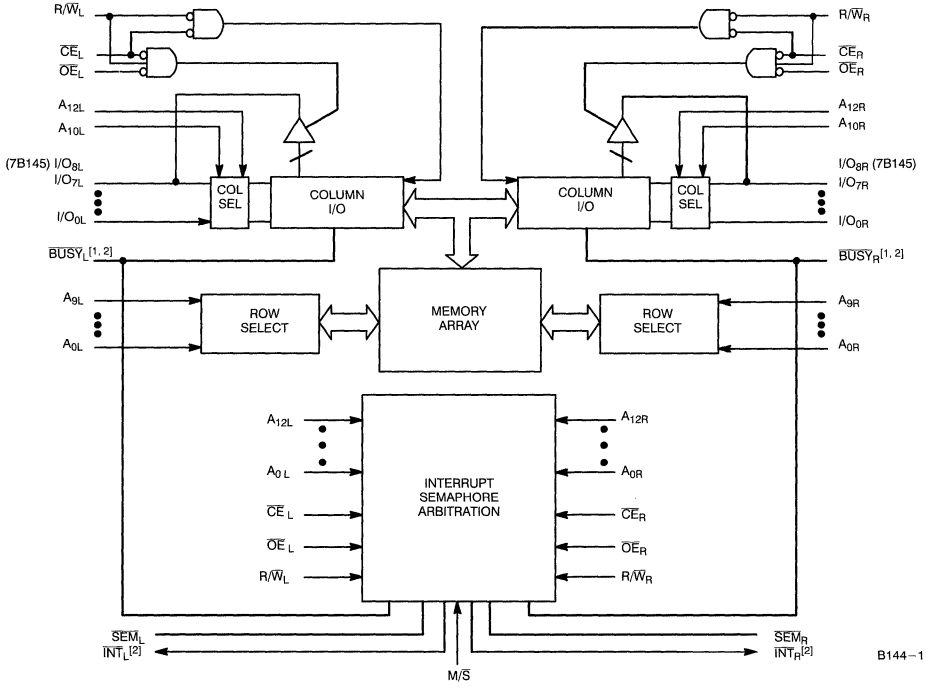
Functional Description

The CY7B144 and CY7B145 are high-speed BiCMOS 8K x 8 and 8K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B144/5 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B144/5 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B144 and CY7B145 are available in 68-pin LCCs, PLCCs, 64-pin (CY7B144) and 80-pin TQFP (CY7B145).

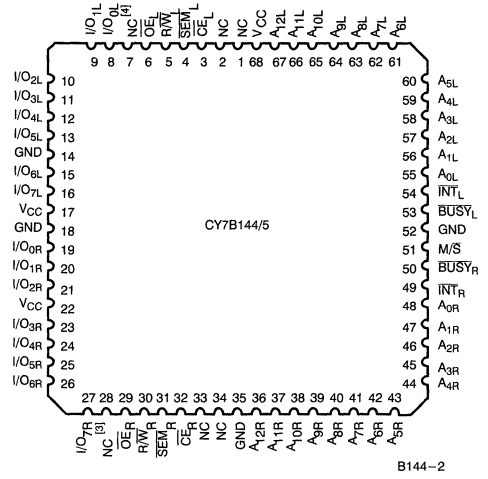
Logic Block Diagram



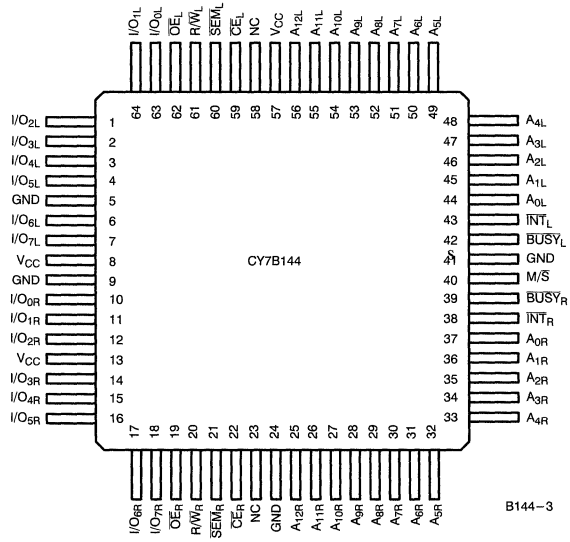
Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

Pin Configurations

68-Pin LCC/PLCC
Top View



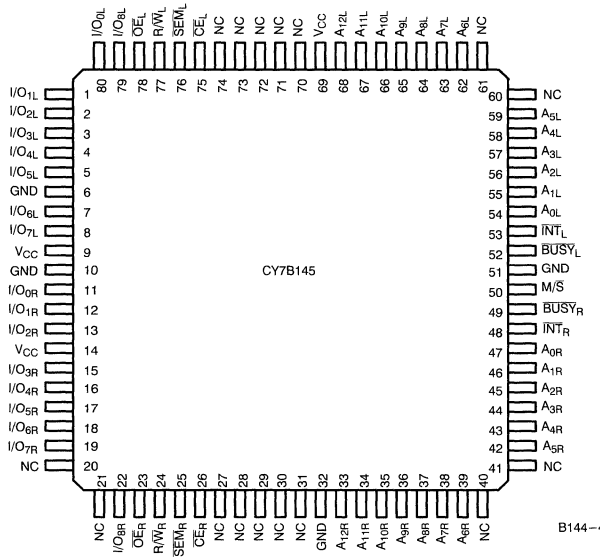
64-Pin TQFP
Top View



Notes:
3. I/O_{8R} on the CY7B145.
4. I/O_{8L} on the CY7B145.

Pin Configurations (continued)

80-Pin TQFP
Top View



Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data bus Input/Output
A_{0L-12L}	A_{0R-12R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B144–15 7B145–15	7B144–25 7B145–25	7B144–35 7B145–35	7B144–55 7B145–55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military		280	250	
Maximum Standby Current for I_{SB1} (mA)	Commercial	110	95	90	90
	Military		100	95	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[5] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[6]	−55°C to +125°C	5V ± 10%

Notes:

5. Pulse width < 20 ns.

6. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		260		220	mA
			Mil/Ind				280	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		110		95	mA
			Mil/Ind				100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		165		145	mA
			Mil/Ind				180	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		160		140	mA
			Mil/Ind				160	

Parameter	Description	Test Conditions		7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		130		130	mA
			Mil/Ind		140		140	

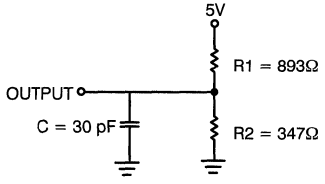
Notes:

7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance[9]

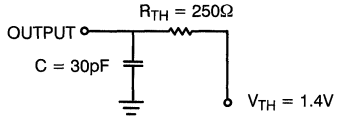
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms



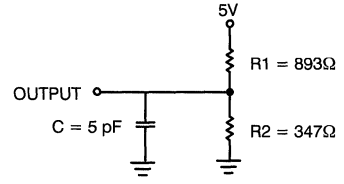
(a) Normal Load (Load 1)

B144–5



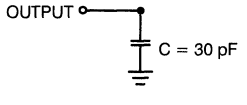
(b) Thévenin Equivalent (Load 1)

B144–6



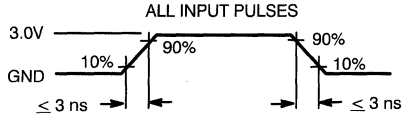
(c) Three-State Delay (Load 3)

B144–7



Load (Load 2)

B144–8



B144–9

Switching Characteristics Over the Operating Range[7, 10]

Parameter	Description	7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[11, 12]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[11, 12]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[11, 12]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[11, 12]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns

Notes:

9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 3.

Switching Characteristics Over the Operating Range[7, 10] (continued)

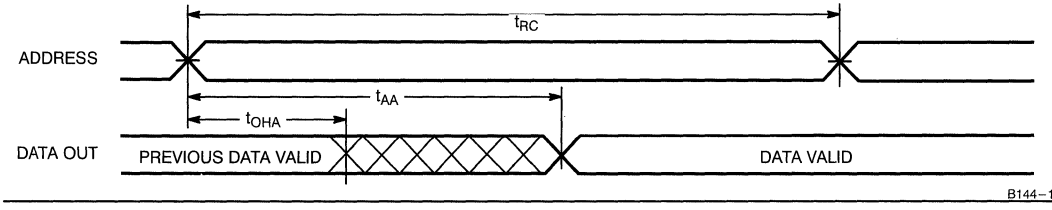
Parameter	Description	7B144–15 7B145–15		7B144–25 7B145–25		7B144–35 7B145–35		7B144–55 7B145–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[12]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[12]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[13]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid		25		30		35		40	ns
BUSY TIMING[14]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35		55	ns
INTERRUPT TIMING[14]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		35	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		35	ns
SEMAPHORE TIMING										
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

Notes:

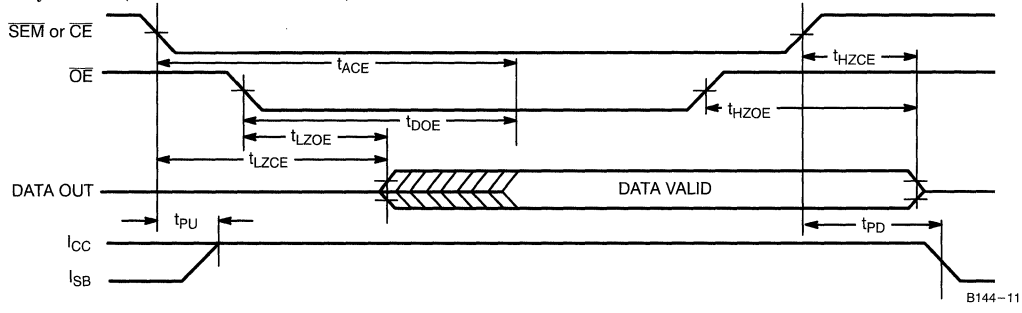
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.

Switching Waveforms

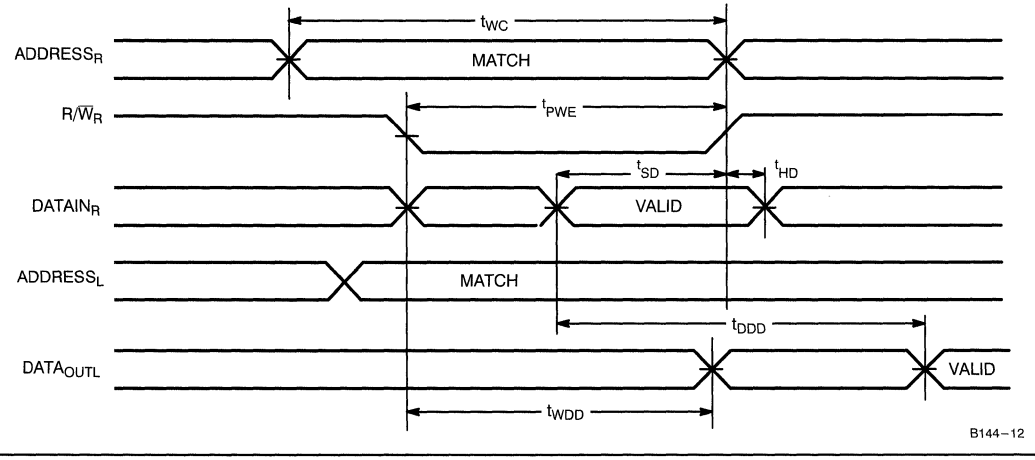
Read Cycle No. 1 (Either Port Address Access)[15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[15, 17, 18]



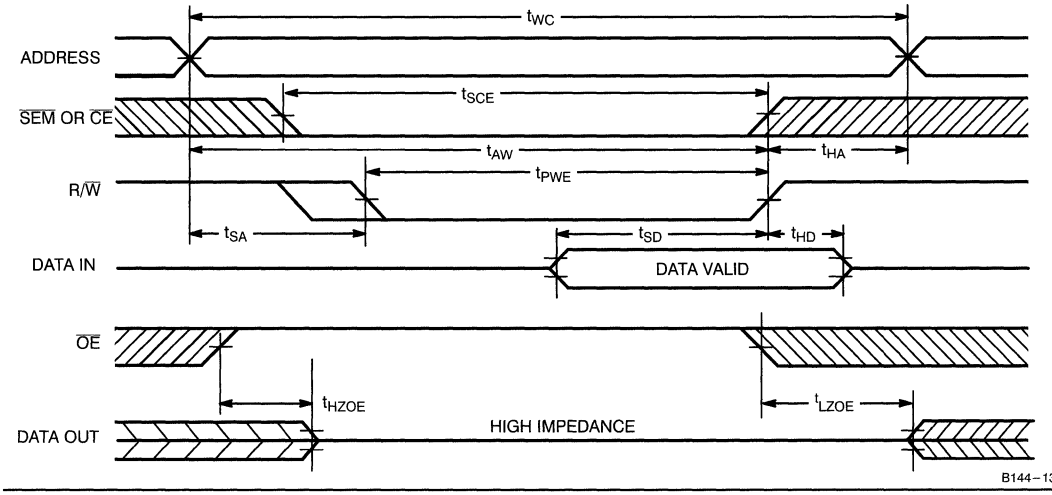
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[19, 20]



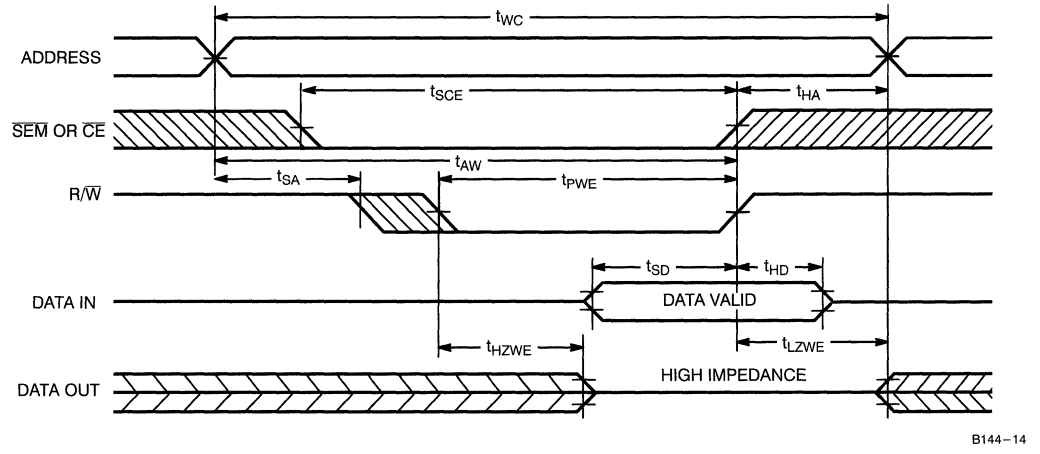
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21, 22, 23]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[21, 23, 24]

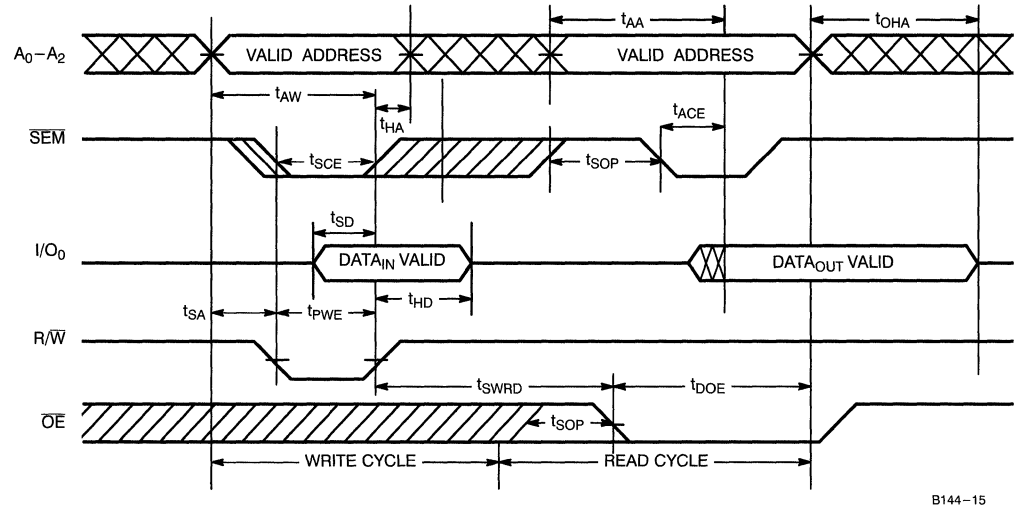


Notes:

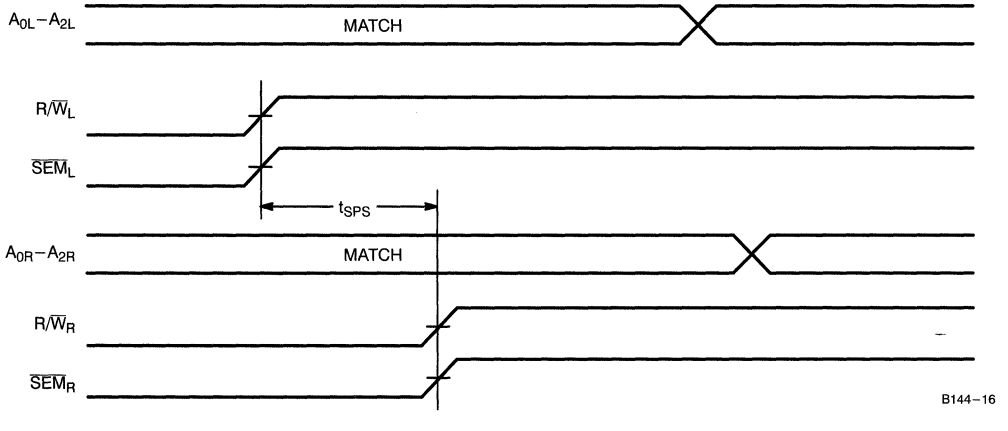
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[25]



Semaphore Contention[26, 27, 28]

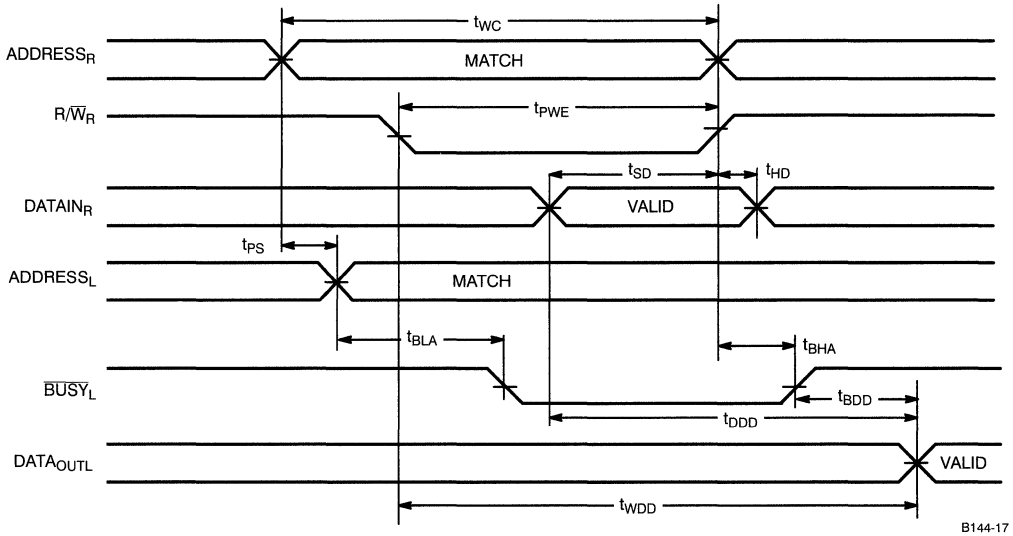


Notes:

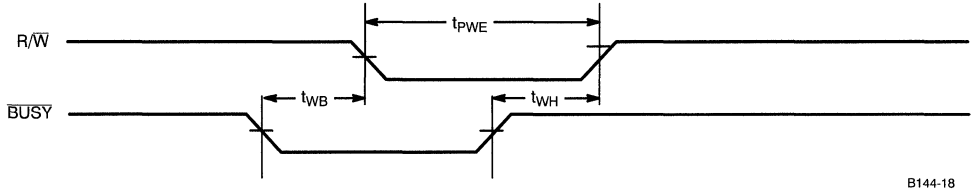
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[20]



Write Timing with Busy Input (M/$\overline{S}$=LOW)

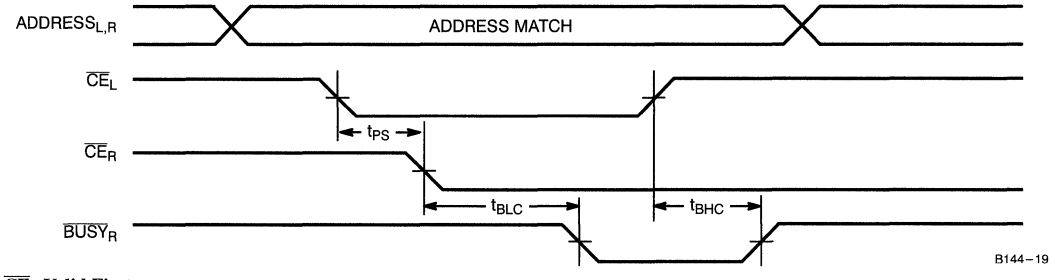


6

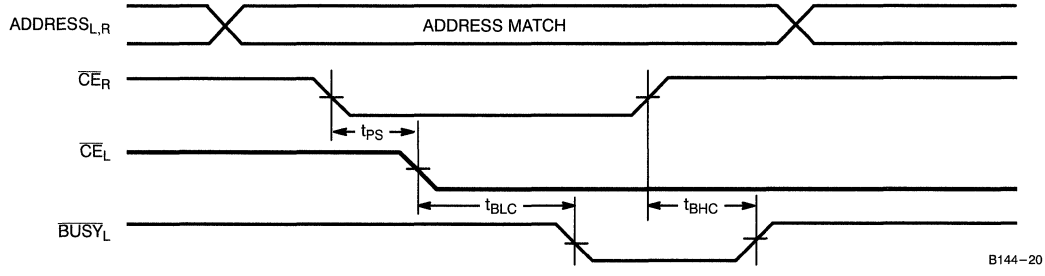
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

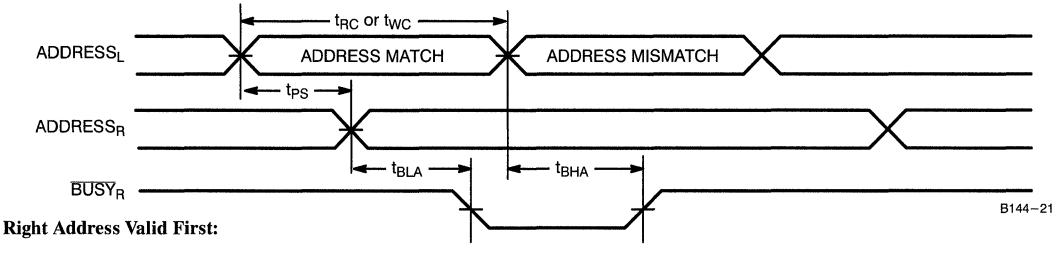


$\overline{CE}_R$ Valid First:

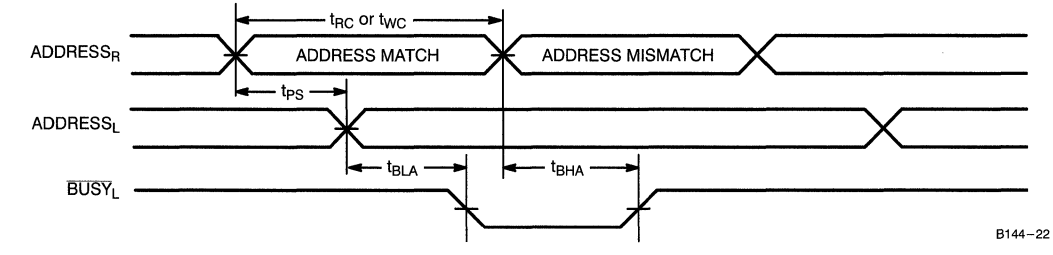


Busy Timing Diagram No. 2 (Address Arbitration)[29]

Left Address Valid First:



Right Address Valid First:



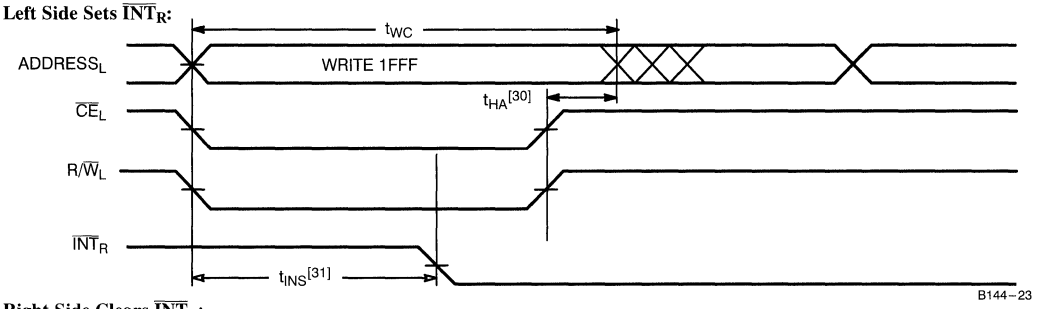
Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

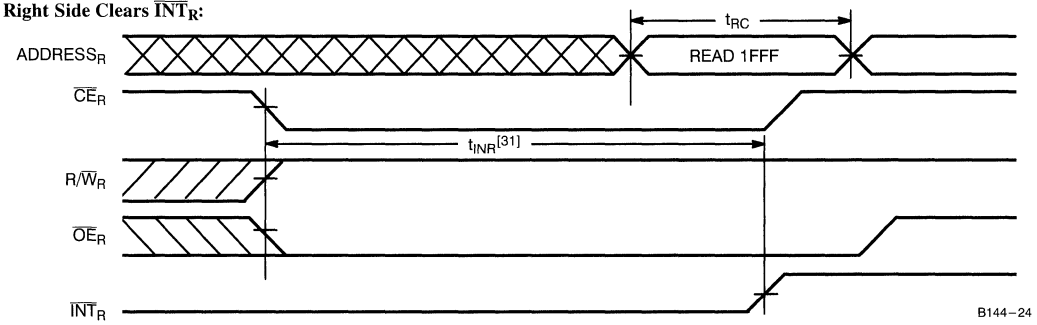
Switching Waveforms (continued)

Interrupt Timing Diagrams

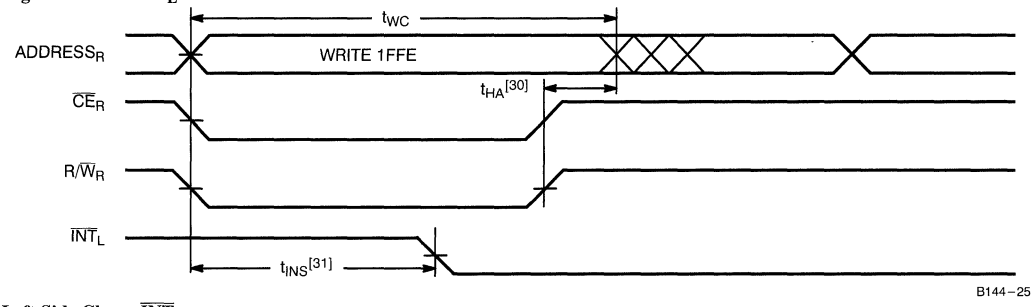
Left Side Sets $\overline{INT}_R$:



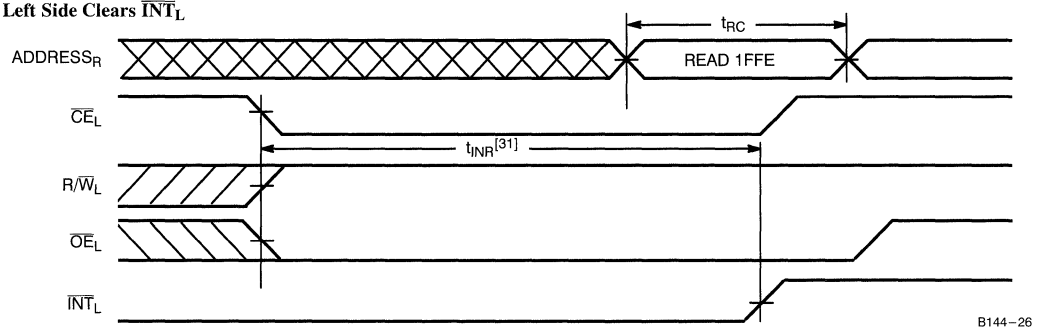
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



6

Architecture

The CY7B144/5 consists of a an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B144/5 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B144/5 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B144/5 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. all Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⎍	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

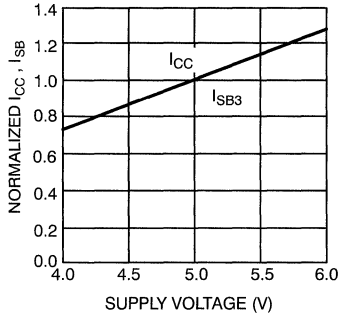
	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset Left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 3. Semaphore Operation Example

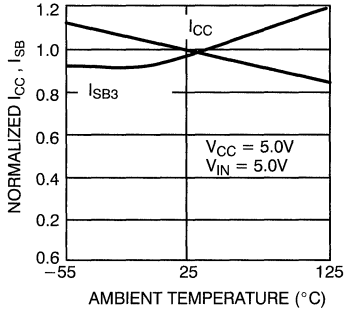
Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

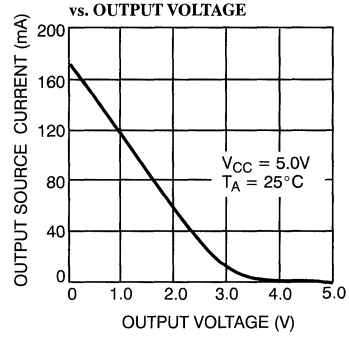
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



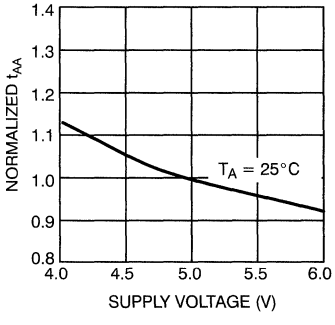
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



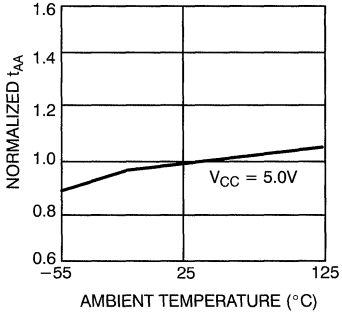
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



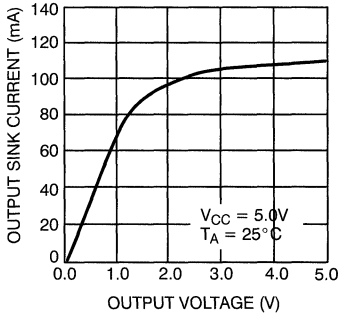
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



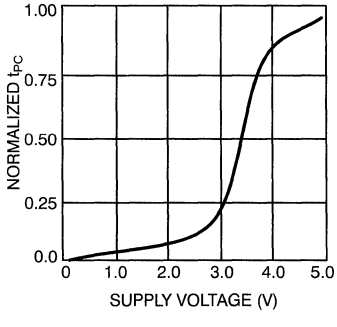
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



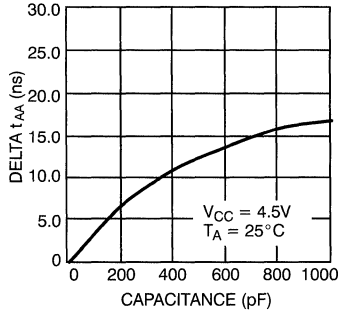
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



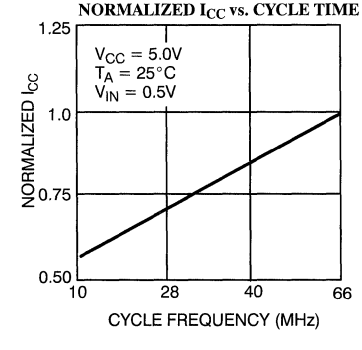
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B144–15AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B144–25AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B144–35AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B144–55AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–55AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B145–15AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B145–25AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B145–35AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B145–55AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–55AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38-00163-G

CY7C006
CY7C016

16K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **CMOS for optimum speed/power**
- **High-speed access**
  — 15 ns (commercial)
- **Low operating power: 140 mA (typ.)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin PLCC; 80-pin (7C016) and 64-pin (7C006) TQFP**
- **TTL compatible**
- **Capable of withstanding greater than 2001V ESD**
- **Pin compatible and functional equivalent to IDT7006 and IDT7016**

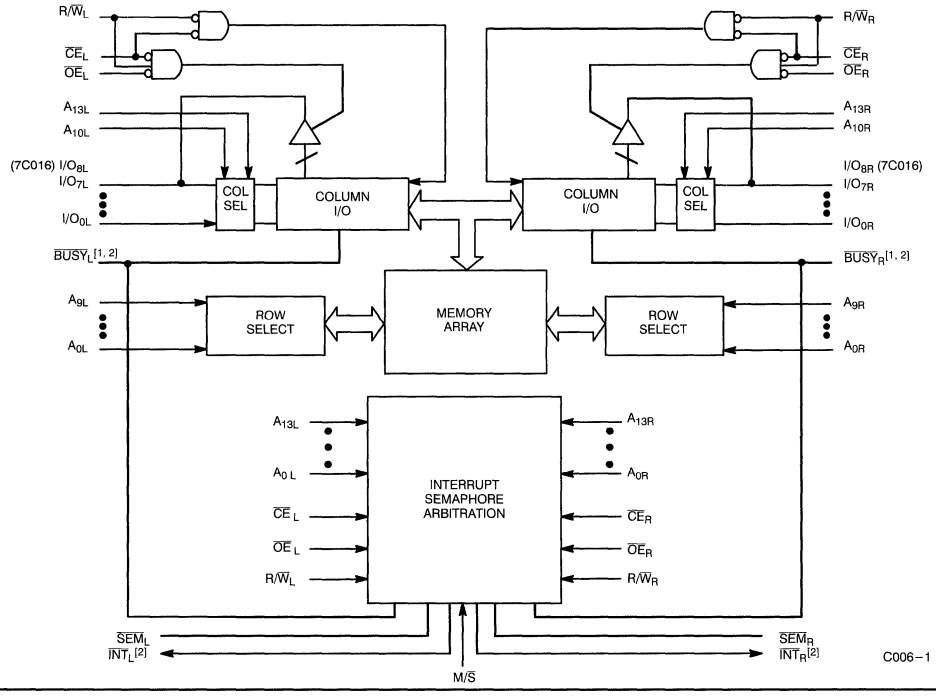
Functional Description

The CY7C006 and CY7C016 are high-speed CMOS 16K x 8 and 16K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C006/016 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C006/016 can be utilized as a standalone 128-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16-/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16-/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs,communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7C006 and CY7C016 are available in 68-pin PLCCs, and 80-pin (7C016) TQFP and 64-pin (7C006) TQFP.

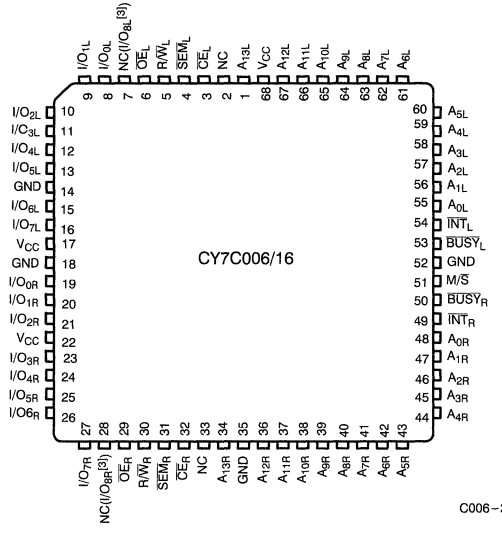
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

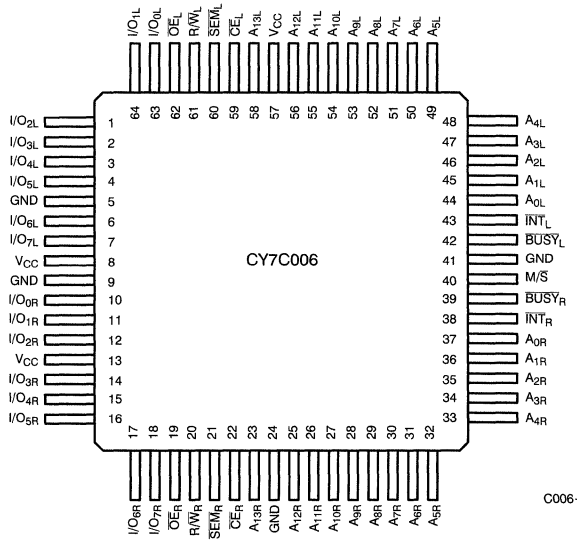
Pin Configurations

68-Pin LCC/PLCC
Top View



C006–2

64-Pin TQFP
Top View

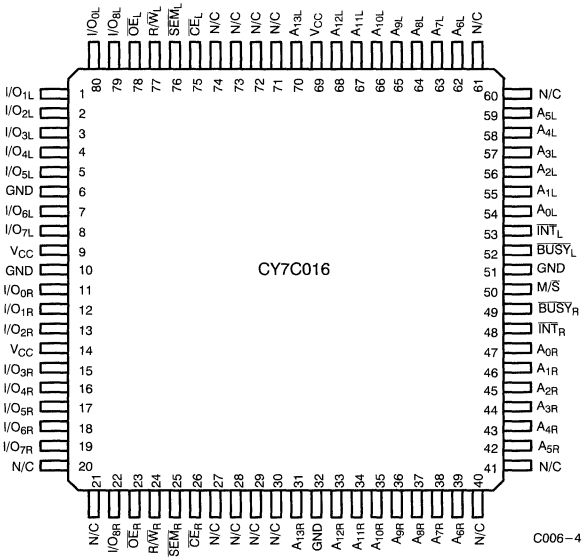


C006–3

Notes:
3. I/O for 7C016 only.

Pin Configurations (continued)

80-Pin TQFP
Top View



C006–4

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-13L}	A_{0R-13R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 3FFE and is cleared when left port reads location 3FFE. $\overline{INT}_R$ is set when left port writes location 3FFF and is cleared when right port reads location 3FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

	7C006–15 7C016–15	7C006–25 7C016–25	7C006–35 7C016–35	7C006–55 7C016–55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	260	220	210	200
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[4] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[5]

Parameter	Description	Test Conditions		7C006–15 7C016–15 Min.	Typ.	Max.	7C006–25 7C016–25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		170	260		160	220	mA
			Ind					160	270	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Com'l		50	70		40	60	mA
			Ind					40	75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Com'l		110	170		90	130	mA
			Ind					90	150	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[7]	Com'l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[7]	Com'l		100	150		80	120	mA
			Ind					80	130	

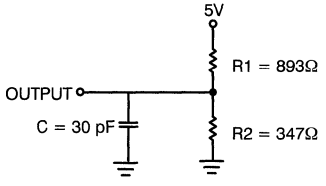
Parameter	Description	Test Conditions		7C006–35 7C016–35 Min.	Typ.	Max.	7C006–55 7C016–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		150	210		140	200	mA
			Ind		150	250		140	240	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Com'l		30	50		20	40	mA
			Ind		30	65		20	55	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[7]	Com'l		80	120		70	100	mA
			Ind		80	130		70	115	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[7]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[7]	Com'l		70	100		60	90	mA
			Ind		70	110		60	95	

Notes:
5. Pulse width < 20 ns.
6. See the last page of this specification for Group A subgroup testing information.
7. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance[8]

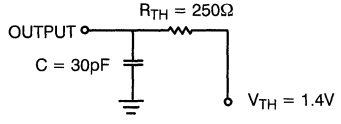
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



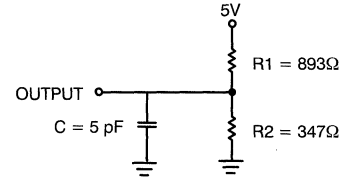
(a) Normal Load (Load 1)

C006–5



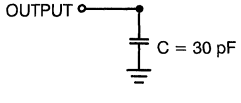
(b) Thévenin Equivalent (Load 1)

C006–6



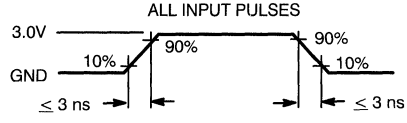
(c) Three-State Delay (Load 3)

C006–7



Load (Load 2)

C006–8



C006–9

Switching Characteristics Over the Operating Range[7,8]

Parameter	Description	7C006–15 7C016–15 Min.	7C006–15 7C016–15 Max.	7C006–25 7C016–25 Min.	7C006–25 7C016–25 Max.	7C006–35 7C016–35 Min.	7C006–35 7C016–35 Max.	7C006–55 7C016–55 Min.	7C006–55 7C016–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[8,9]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[10,11]	$\overline{OE}$ HIGH to High Z		10		15		15		25	ns
t_{LZCE}[10,11]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[10,11]	$\overline{CE}$ HIGH to High Z		10		15		15		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns

Notes:

8. Tested initially and after any design or process changes that may affect these parameters.
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
10. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
11. Test conditions used are Load 3.

Switching Characteristics Over the Operating Range[7, 10] (continued)

Parameter	Description	7C006–15 7C016–15		7C006–25 7C016–25		7C006–35 7C016–35		7C006–55 7C016–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}[12]	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[12]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[12]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[13]	Write Pulse to Data Delay		30		50		60		80	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid		25		30		35		60	ns
BUSY TIMING[14]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		17		25		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		17		25		30		ns
t_{BDD}[15]	$\overline{BUSY}$ HIGH to Data Valid		Note 15		Note 15		Note 15		Note 15	ns
INTERRUPT TIMING[14]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

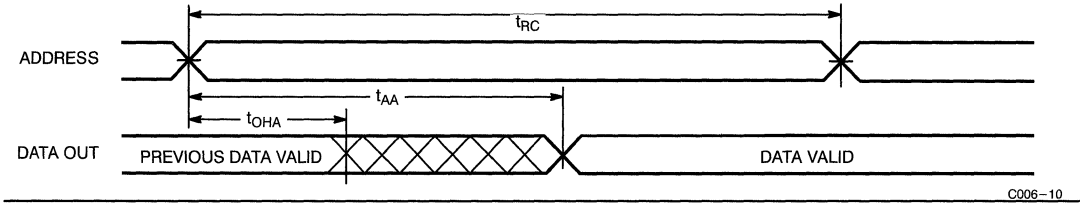
Notes:

12. Must be met by the device writing to the RAM under all operating conditions.
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.
15. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

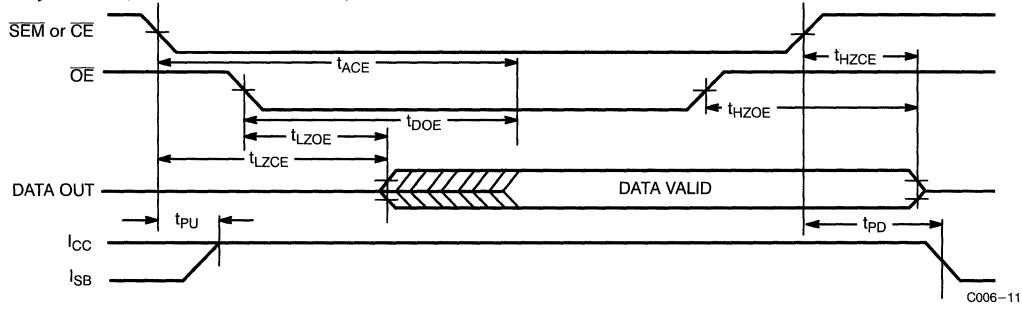
6

Switching Waveforms

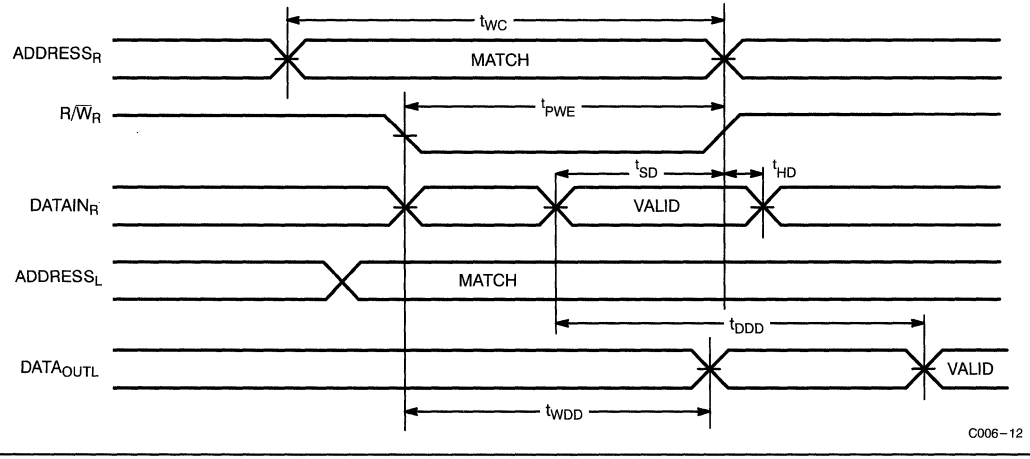
Read Cycle No. 1 (Either Port Address Access)[16, 17]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[15, 18, 19]



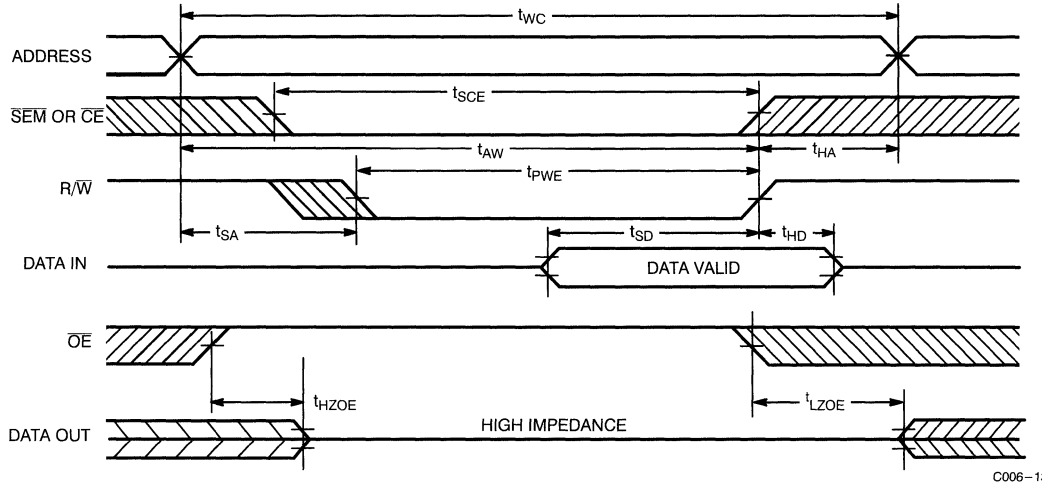
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[20, 21]



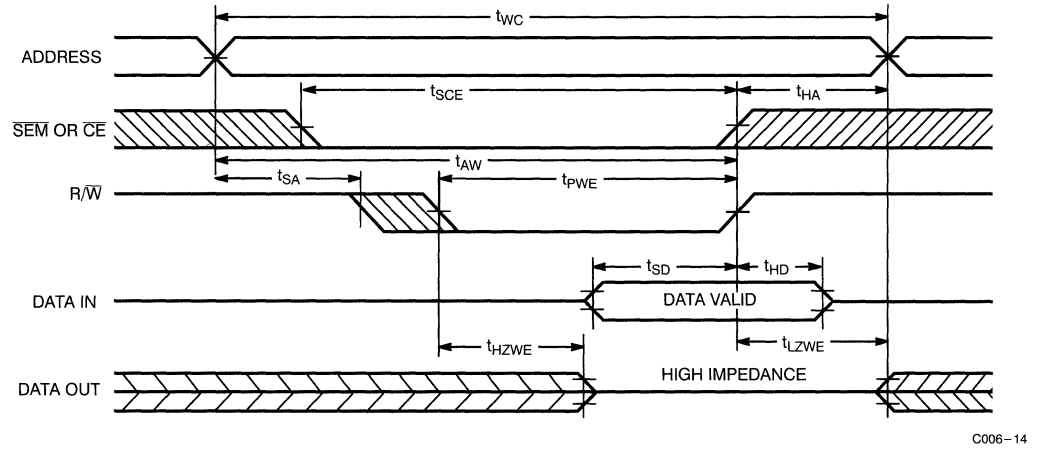
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[22, 23, 24]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[21, 23, 25]

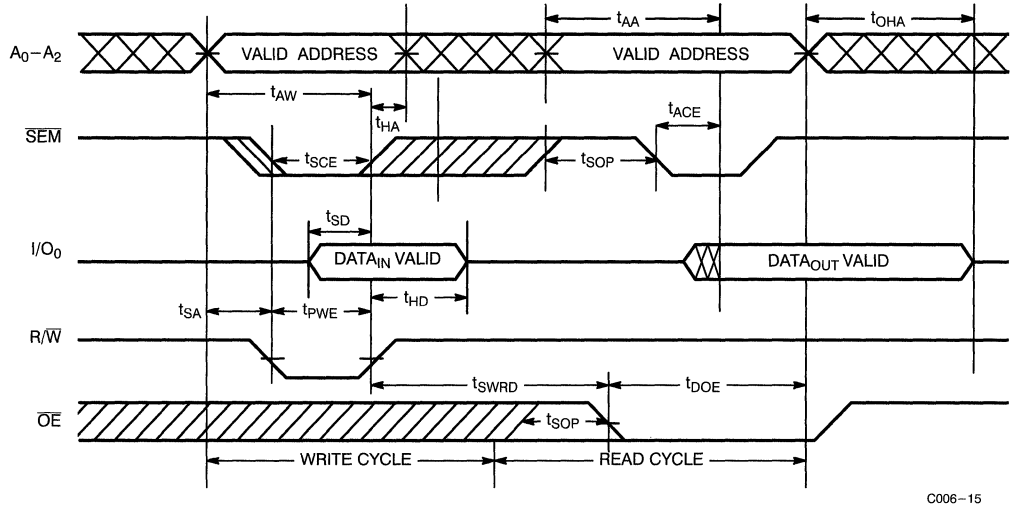


Notes:

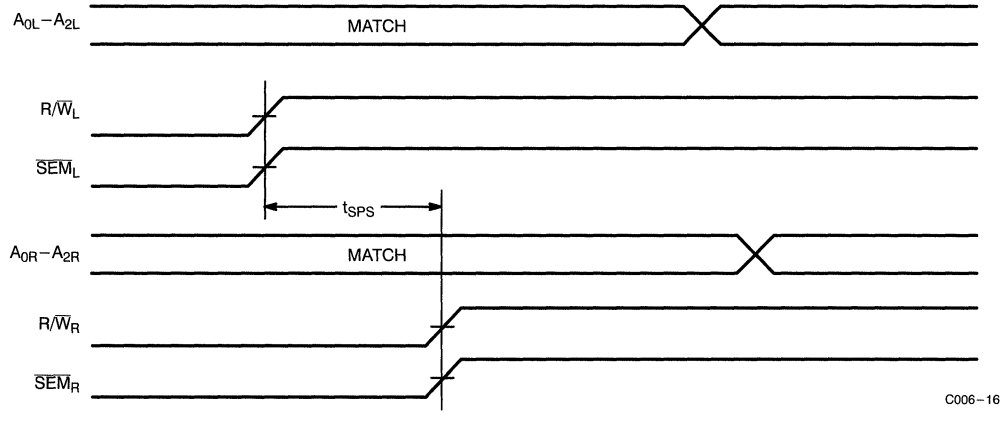
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[26]



Semaphore Contention[27, 28, 29]

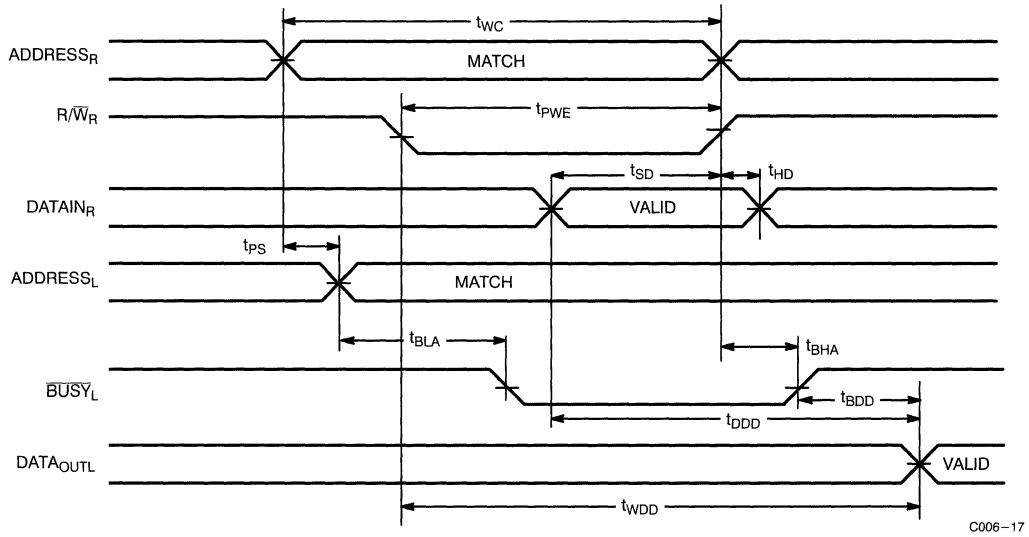


Notes:

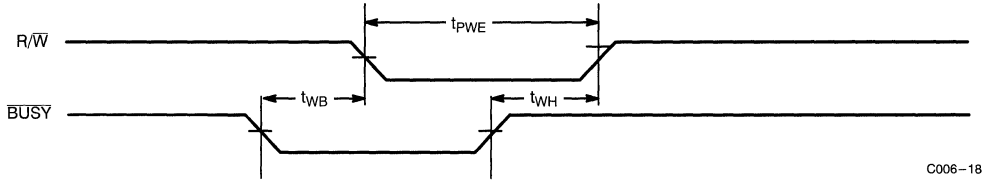
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[20]



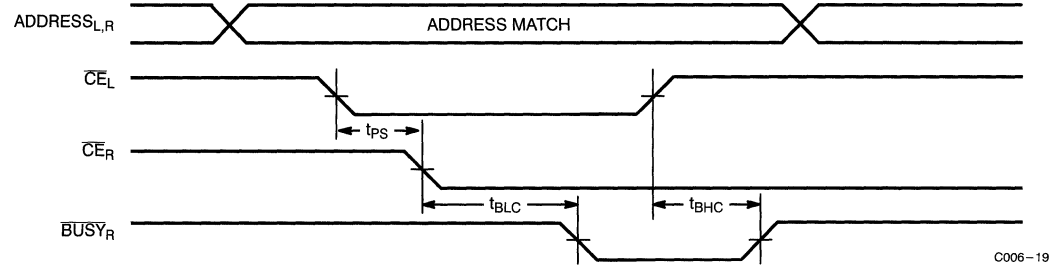
Write Timing with Busy Input (M/$\overline{S}$=LOW)



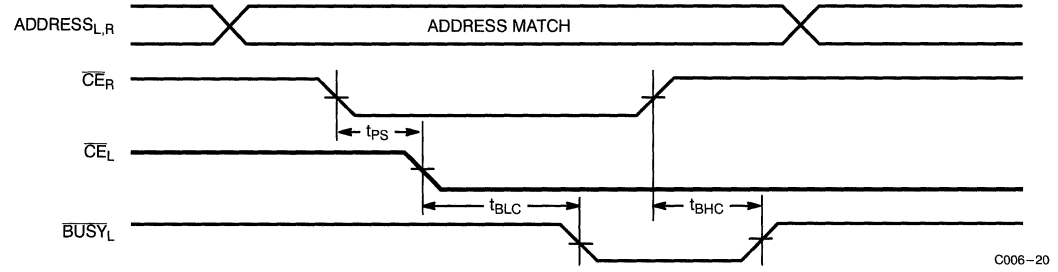
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[30]

$\overline{CE}_L$ Valid First:

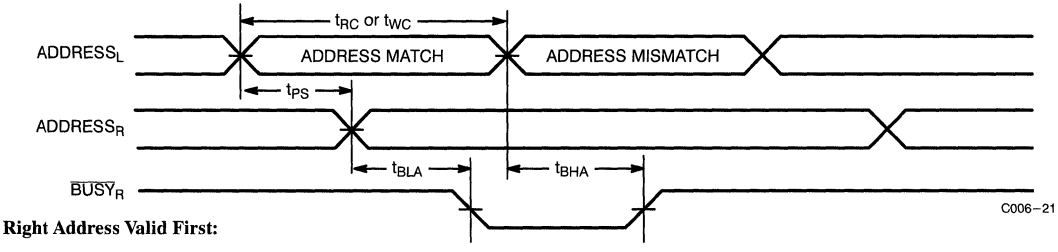


$\overline{CE}_R$ Valid First:

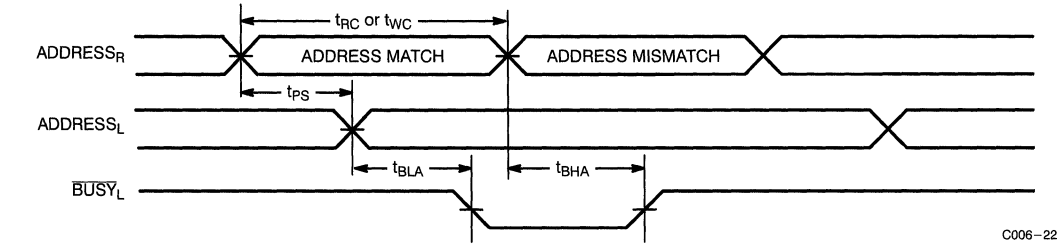


Busy Timing Diagram No. 2 (Address Arbitration)[29]

Left Address Valid First:



Right Address Valid First:



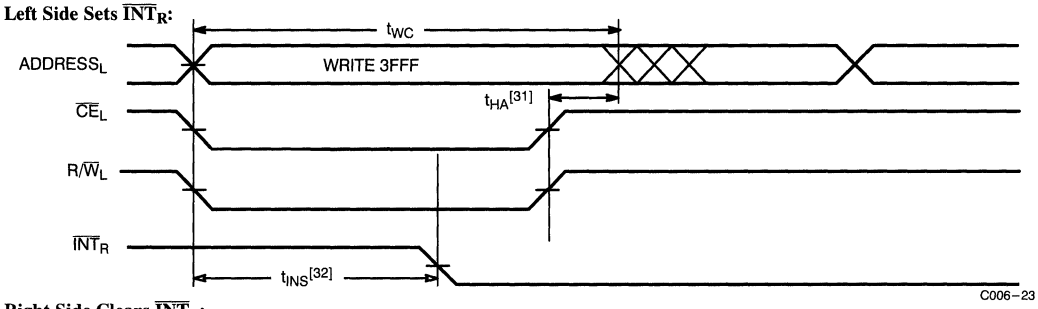
Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

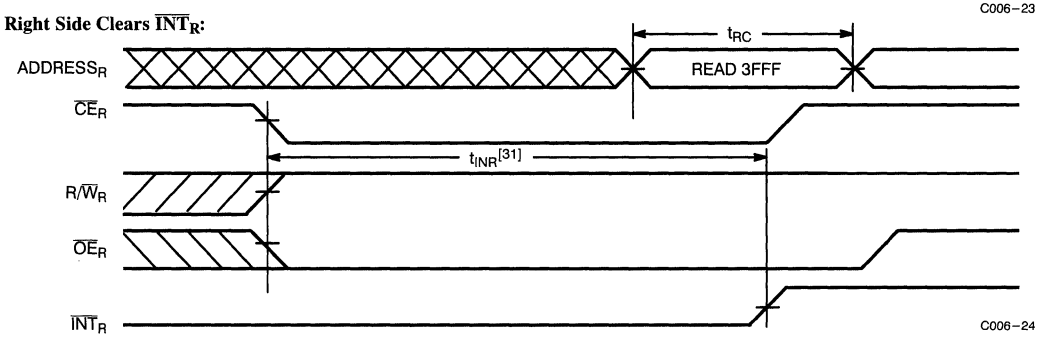
Switching Waveforms (continued)

Interrupt Timing Diagrams

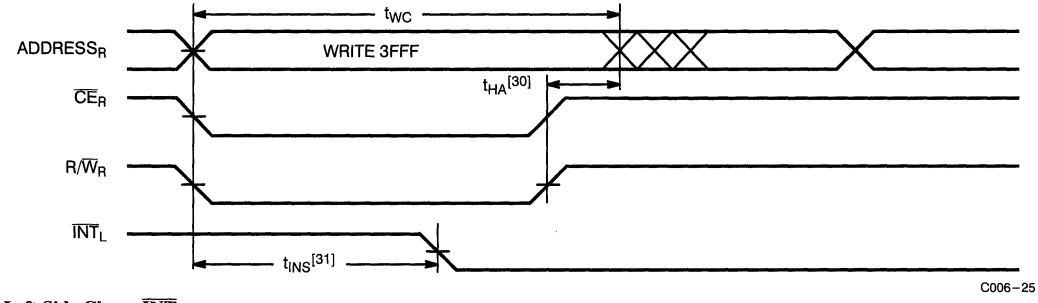
Left Side Sets $\overline{INT}_R$:



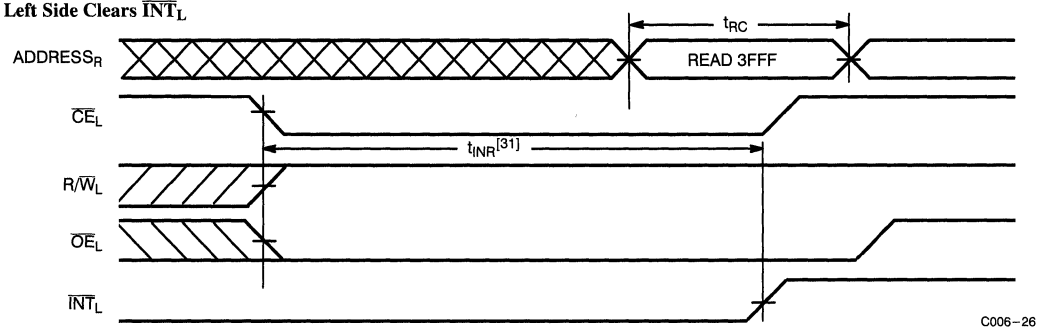
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Architecture

The CY7C006/016 consists of a an array of 16K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C006/016 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C006/016 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⎍	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7C006/016 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 3FFE(HEX), the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 3FFE(HEX). This flag is cleared when the left port reads location 3FFE(HEX). The message at 3FFE(HEX) is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C006/016 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006/016 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY_L}$=$\overline{BUSY_R}$=HIGH)

	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0L-13L}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0R-13R}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	3FFE	X
Reset Left $\overline{INT}$	X	L	L	3FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	3FFE	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	3FFE	H

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 3. Semaphore Operation Example

Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C006–15AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C006–25AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–25AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C006–35AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–35AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C006–55AC	A65	64-Lead Thin Quad Flat Package	Commercial
	CY7C006–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C006–55AI	A65	64-Lead Thin Quad Flat Package	Industrial
	CY7C006–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C016–15AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C016–25AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–25AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C016–35AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–35AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
55	CY7C016–55AC	A80	80-Lead Thin Quad Flat Package	Commercial
	CY7C016–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C016–55AI	A80	80-Lead Thin Quad Flat Package	Industrial
	CY7C016–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38−00163

CY7C024/0241
CY7C025/0251

4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with Sem, Int, Busy

Features

- **4K x 16 organization (CY7C024)**
- **4K x 18 organization (CY7C0241)**
- **8K x 16 organization (CY7C025)**
- **8K x 18 organization (CY7C0251)**
- **High-speed access**
  — 15 ns
- **Automatic power-down**
- **Low operating power**
  — I_{CC} = 150 mA (typ.)
- **Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device**
- **On chip arbitration logic**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Separate upper byte and lower byte control**
- **Pin select for Master or Slave**
- **Available in 84-pin PLCC and 100-pin TQFP**
- **Pin-compatible and functional equivalent to IDT7024/IDT7025**

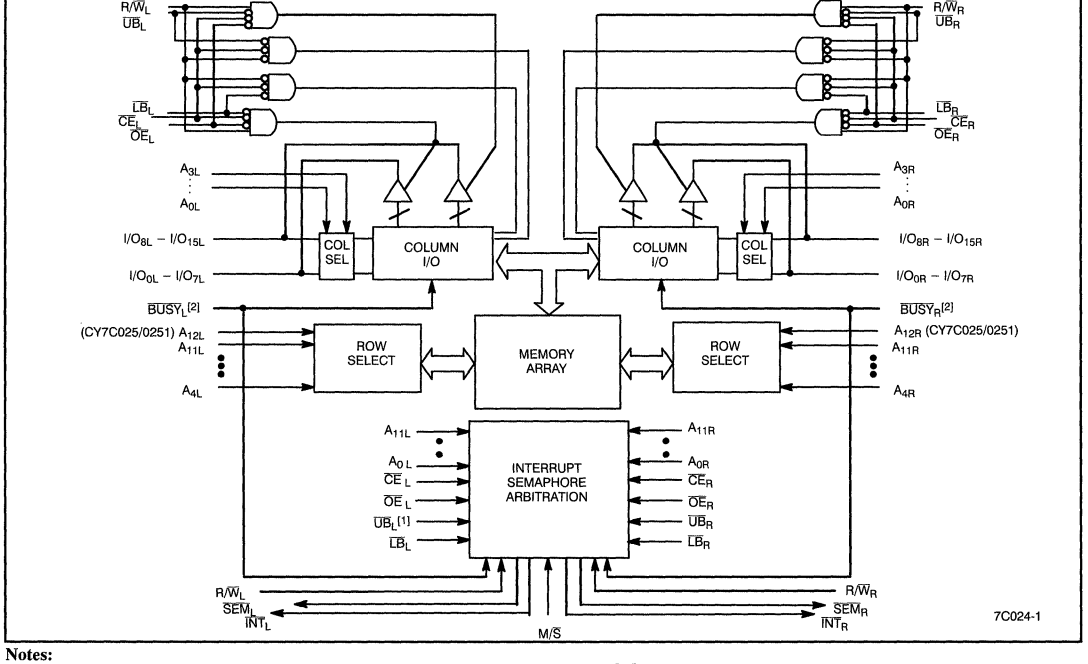
Functional Description

The CY7C024/0241 and CY7C025/0251 are low-power CMOS 4K x 16/18 and 8K x 16/18 dual-port static RAMs. Various arbitration schemes are included on the CY7C024/0241 and CY7C025/0251 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C024/0241 and CY7C025/0251 can be utilized as standalone 16-/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-/36-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 32-/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip select ($\overline{CE}$) pin.

The CY7C024/0241 and CY7C025/0251 are available in 84-pin PLCCs (CY7C024 and CY7C025 only) and 100-pin Thin Quad Plastic Flatpack (TQFP).

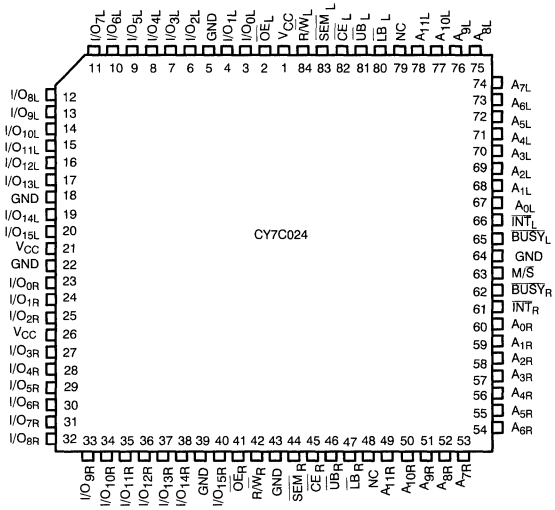
Logic Block Diagram



Notes:
1. LB=Lower Byte. UB=Upper Byte.
2. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

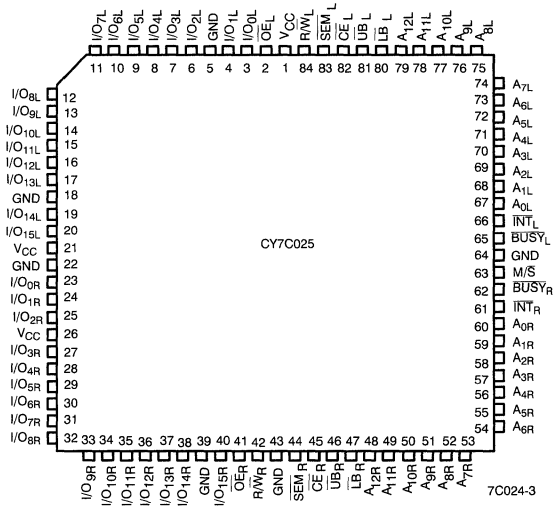
Pin Configurations

84-Pin PLCC
Top View



7C024-2

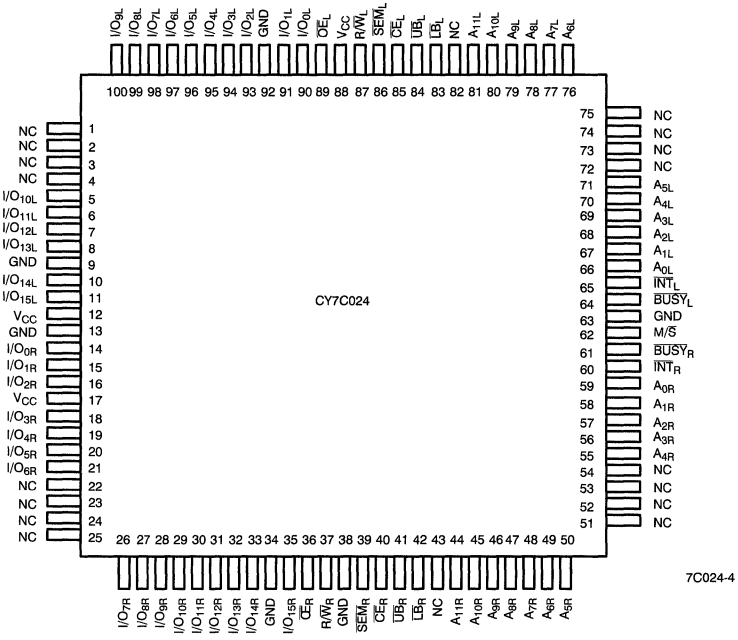
84-Pin PLCC
Top View



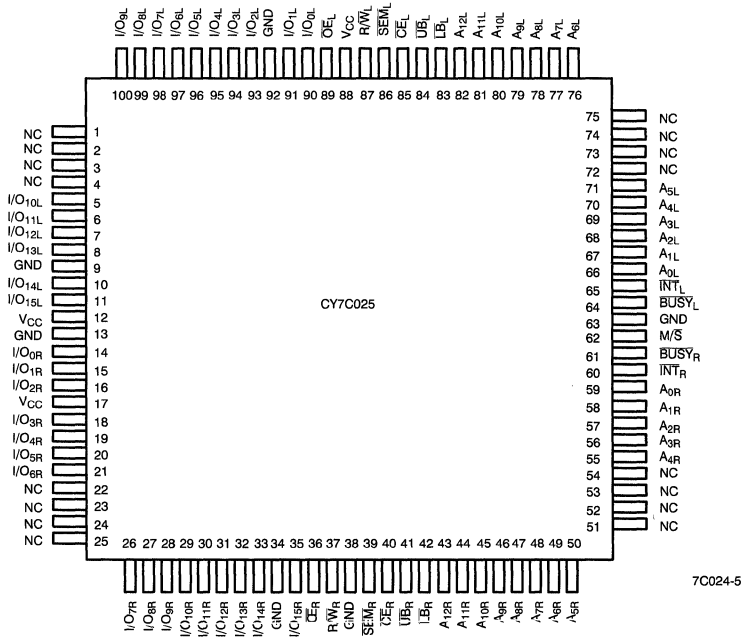
7C024-3

Pin Configurations (continued)

100-Pin TQFP
Top View



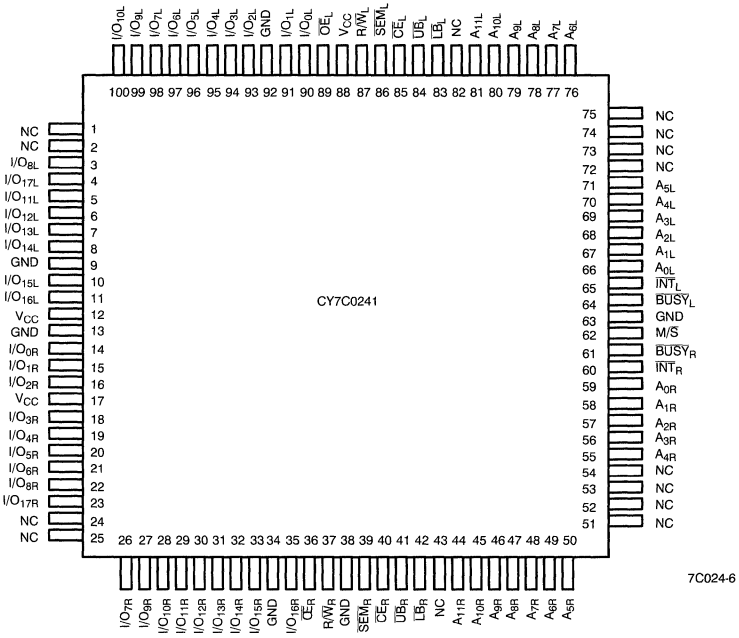
7C024-4

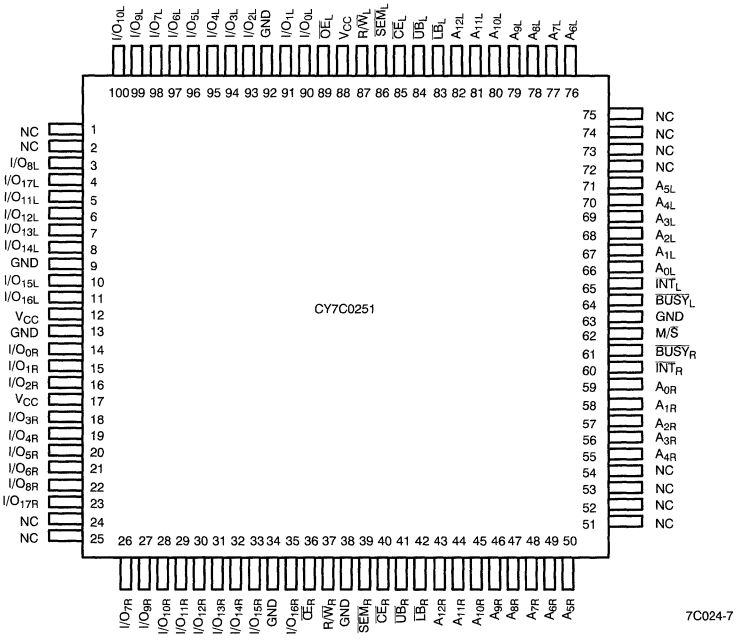


7C024-5

Pin Configurations (continued)

100-Pin TQFP
Top View





Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}-A_{12L}$	$A_{0R}-A_{12R}$	Address
$I/O_{0L}-I/O_{15L}$	$I/O_{0R}-I/O_{15R}$	Data Bus Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

	7C024/0241−15 7C025/0251−15	7C024/0241−25 7C025/0251−25	7C024/0241−35 7C025/0251−35	7C024/0241−55 7C025/0251−55
Maximum Access Time (ns)	15	25	35	55
Maximum Operating Current (mA)	280	250	230	220
Maximum Standby Current for I_{SB1} (mA)	70	60	50	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to + 150°C

Ambient Temperature with Power Applied ..... −55°C to + 125°C

Supply Voltage to Ground Potential ..... −0.3V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to + 7.0V

DC Input Voltage[3] ..... −0.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Note:
3. Pulse width < 20 ns.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C024/0241–15 7C025/0251–15 Min.	Typ.	Max.	7C024/0241–25 7C025/0251–25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		190	280		170	250	mA
			Ind					170	290	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		50	70		40	60	mA
			Ind						75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		120	180		100	140	mA
			Ind					100	160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		3	15		3	15	mA
			Ind					3	15	
I_{SB4}	Standby Current (Both Ports CMOS Levels)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		110	160		90	120	mA
			Ind					90	140	

Parameter	Description	Test Conditions		7C024/0241–35 7C025/0251–35 Min.	Typ.	Max.	7C024/0241–55 7C025/0251–55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4			2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA				0.4			0.4	V
V_{IH}	Input HIGH Voltage			2.2			2.2			V
V_{IL}	Input LOW Voltage					0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10		+10	−10		+10	μA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		−10		+10	−10		+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		160	230		150	220	mA
			Ind		160	260		150	250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		30	50		20	40	mA
			Ind		30	65		20	60	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		85	125		75	110	mA
			Ind		85	140		75	145	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		3	15		3	15	mA
			Ind		3	15		3	15	
I_{SB4}	Standby Current (Both Ports CMOS Levels)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		80	105		70	90	mA
			Ind		80	120		70	105	

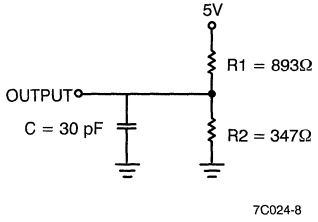
Notes:

4. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

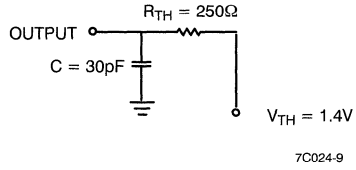
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

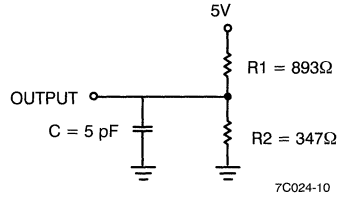
AC Test Loads and Waveforms



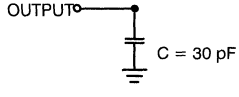
(a) Normal Load (Load 1)



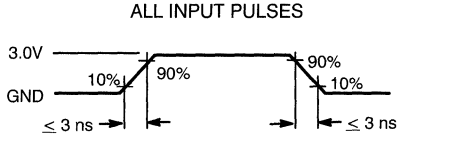
(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 3)



Load (Load 2) 7C024-11



Switching Characteristics Over the Operating Range[6]

Parameter	Description	7C024/0241–15 7C025/0251–15		7C024/0241–25 7C025/0251–25		7C024/0241–35 7C025/0251–35		7C024/0241–55 7C025/0251–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}[7]	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		20		25	ns
t_{LZOE}[8, 9]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[8, 9]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[8, 9]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[8, 9]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		25			ns
t_{ABE}[7]	Byte Enable Access Time		15		25		35		55	ns

Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C024/0241–15 7C025/0251–15		7C024/0241–25 7C025/0251–25		7C024/0241–35 7C025/0251–35		7C024/0241–55 7C025/0251–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}[7]	$\overline{CE}$ LOW to Write End	12		20		30		35		ns
t_{AW}	Address Set-Up to Write End	12		20		30		35		ns
t_{HA}	Address Hold From Write End	0		0		0		0		ns
t_{SA}[7]	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		35		ns
t_{SD}	Data Set-Up to Write End	10		15		15		20		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[9]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[9]	R/$\overline{W}$ HIGH to Low Z	0		0		0		0		ns
t_{WDD}[10]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[10]	Write Data Valid to Read Data Valid		25		35		35		45	ns
BUSY TIMING[11]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		40	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		40	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		35	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	13		20		30		40		ns
t_{BDD}[12]	$\overline{BUSY}$ HIGH to Data Valid		Note 12		Note 12		Note 12		Note 12	ns
INTERRUPT TIMING[11]										
t_{INS}	$\overline{INT}$ Set Time		15		20		25		30	ns
t_{INR}	$\overline{INT}$ Reset Time		15		20		25		30	ns
SEMAPHORE TIMING										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		12		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		10		10		15		ns
t_{SPS}	SEM Flag Contention Window	5		10		10		15		ns
t_{SAA}	SEM Address Access Time		15		25		35		55	ns

Notes:

10. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
11. Test conditions used are Load 2.
12. t_{BDD} is a calculated parameter and is the greater of $t_{WDD} - t_{PWE}$ (actual) or $t_{DDD} - t_{SD}$ (actual).

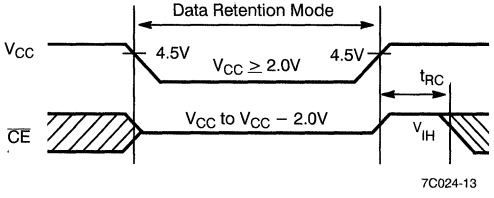
6

Data Retention Mode

The CY7C024/0241 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to V_{CC} – 0.2V.
2. $\overline{CE}$ must be kept between V_{CC} – 0.2V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 volts).

Timing

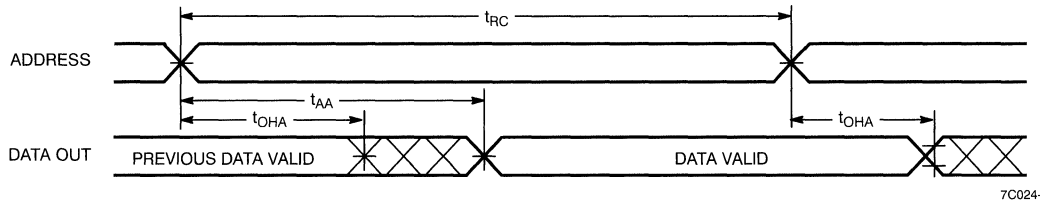


Parameter	Test Conditions[13]	Max.	Unit
ICC_{DR1}	@ VCC_{DR} = 2V	1.5	mA

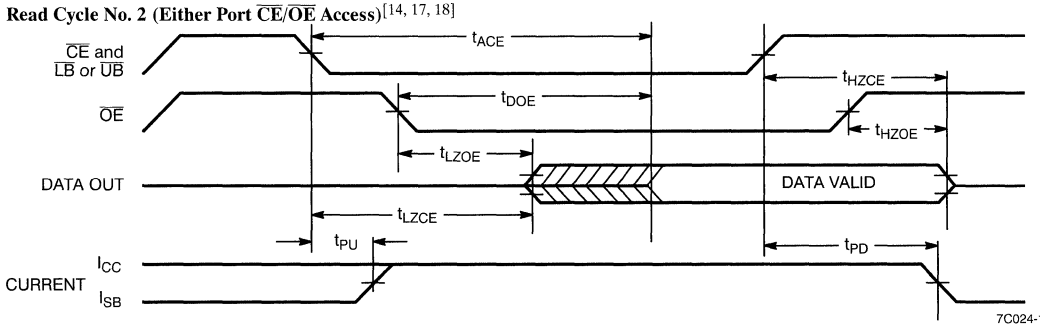
Note:
13. $\overline{CE}$ = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.

Switching Waveforms

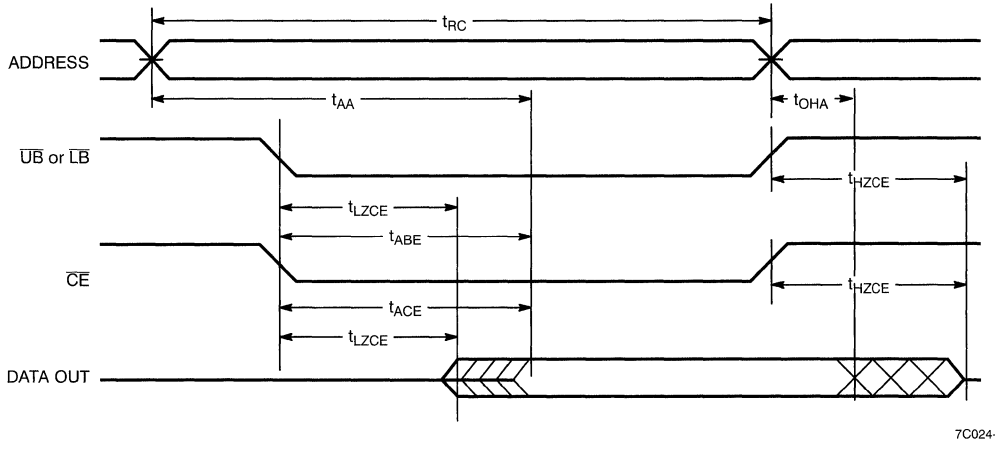
Read Cycle No. 1 (Either Port Address Access)[14, 15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[14, 17, 18]



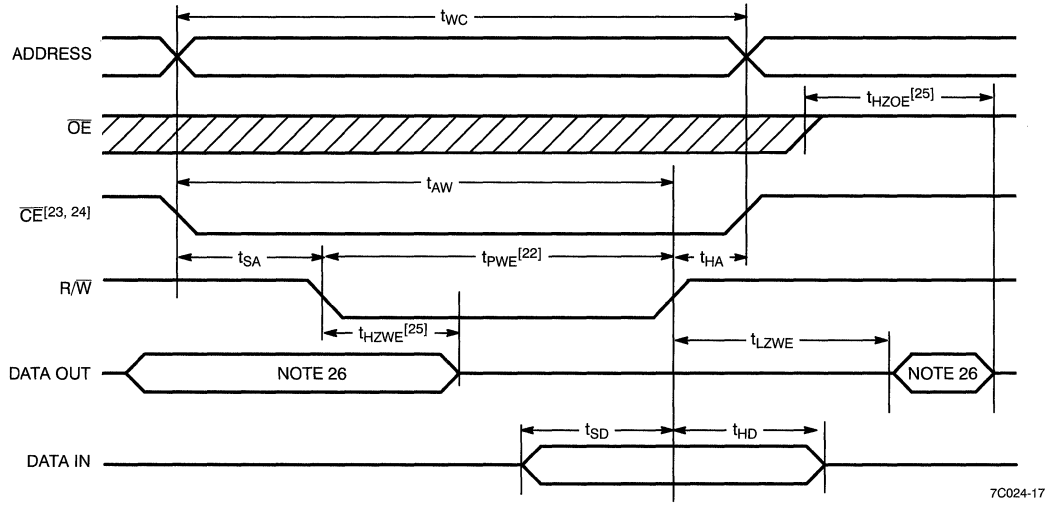
Read Cycle No. 3 (Either Port)[14, 16, 17, 18]



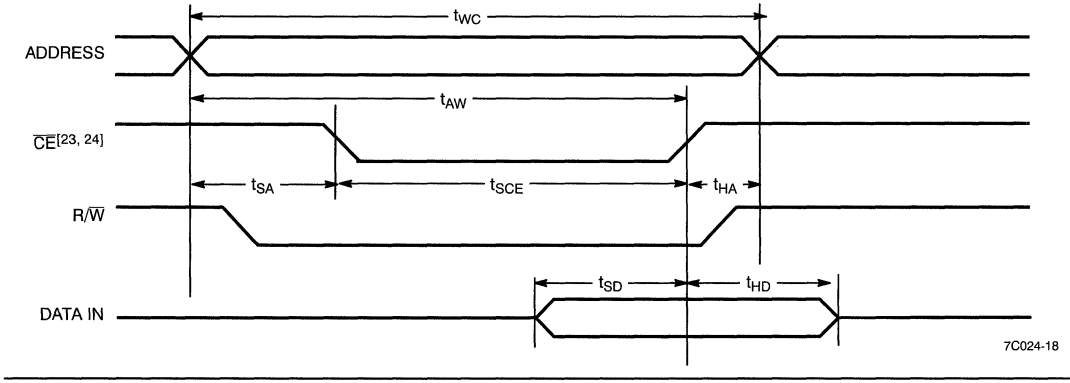
Notes:
14. $R/\overline{W}$ is HIGH for read cycles.
15. Device is continuously selected $\overline{CE} = V_{IL}$ and $\overline{UB}$ or $\overline{LB} = V_{IL}$. This waveform cannot be used for semaphore reads.
16. $\overline{OE} = V_{IL}$.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. To access RAM, $\overline{CE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

Switching Waveforms (continued)

Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[19, 20, 21, 22]



Write Cycle No. 2: $\overline{CE}$ Controlled Timing[19, 20, 21, 27]

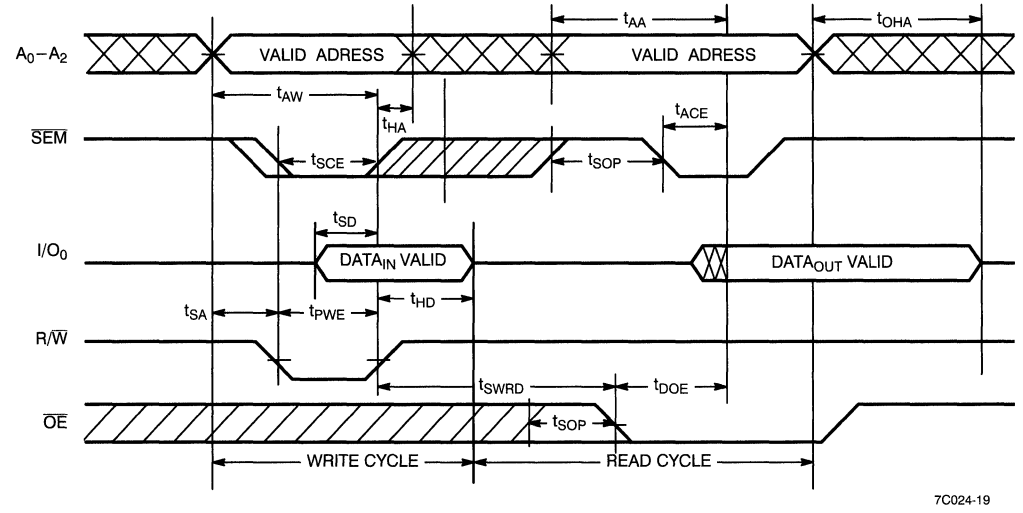


Notes:

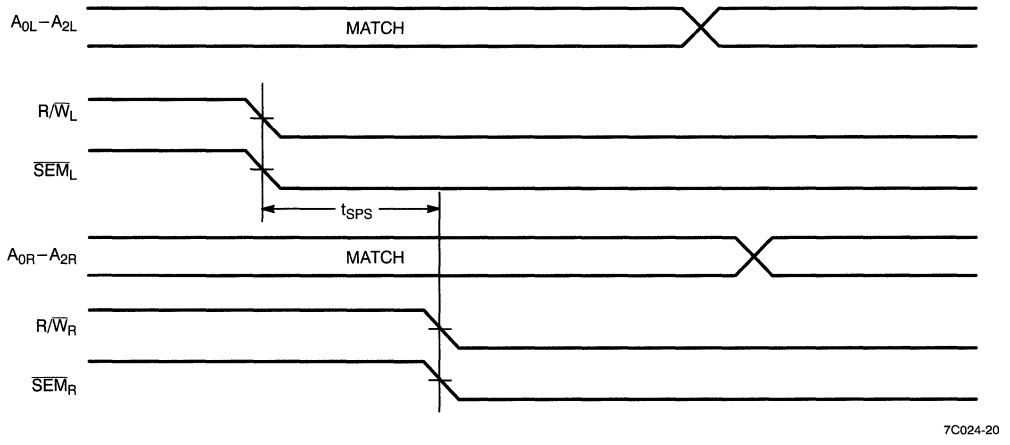
19. R/$\overline{W}$ must be HIGH during all address transitions.
20. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
21. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
24. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
25. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
26. During this period, the I/O pins are in the output state, and input signals must not be applied.
27. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[28]



Timing Diagram of Semaphore Contention[29, 30, 31]

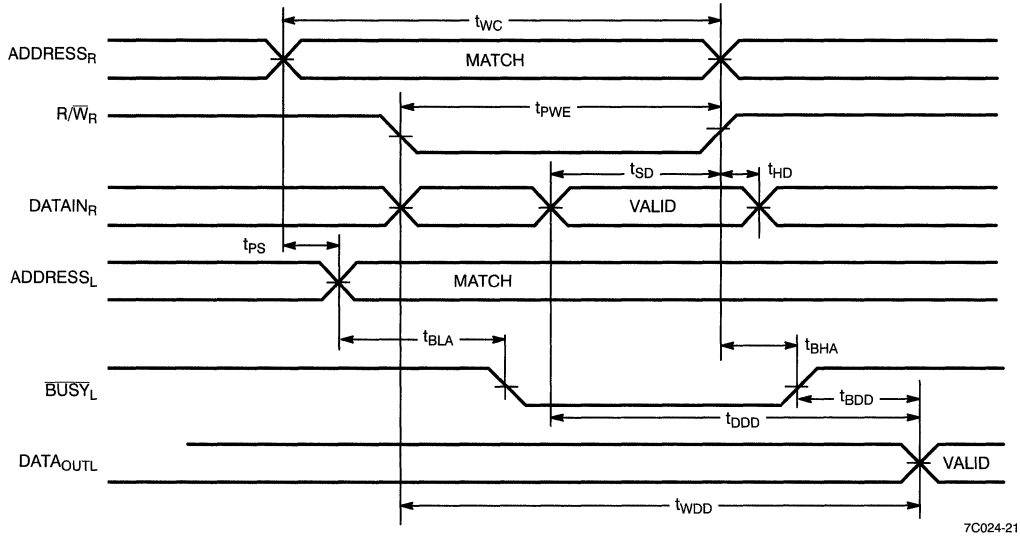


Notes:

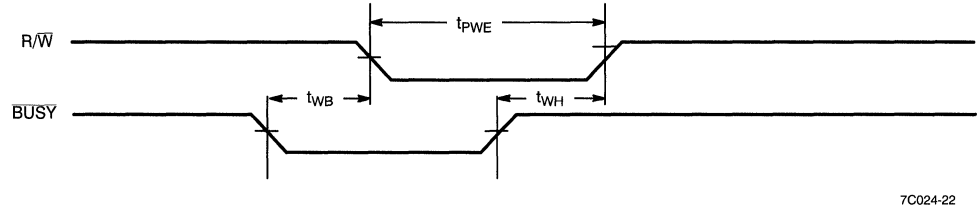
28. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
29. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
30. Semaphores are reset (available to both ports) at cycle start.
31. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[32]



Write Timing with Busy Input (M/$\overline{S}$=LOW)

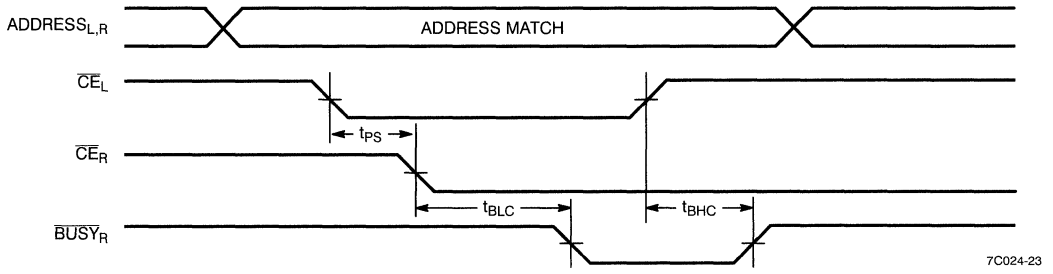


Note:
32. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

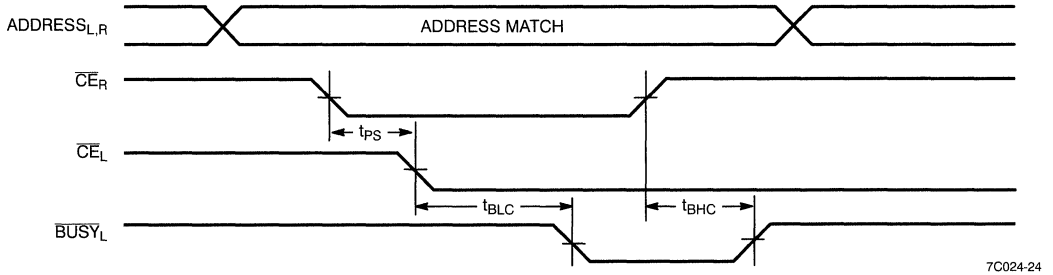
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[33]

$\overline{CE}_L$ Valid First:

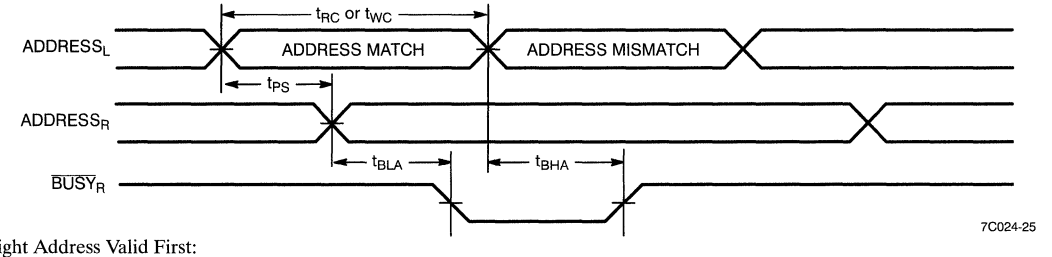


$\overline{CE}_R$ Valid First:

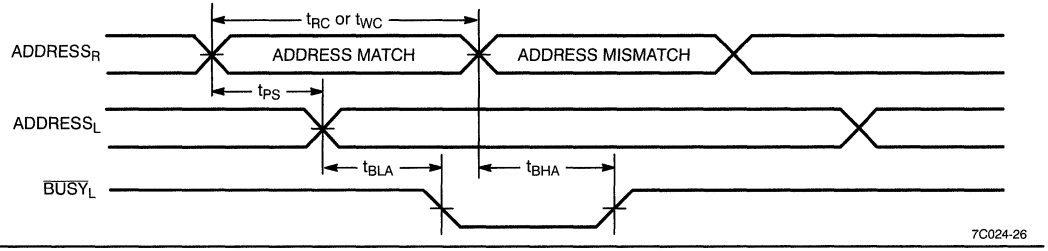


Busy Timing Diagram No. 2 (Address Arbitration)[33]

Left Address Valid First:



Right Address Valid First:

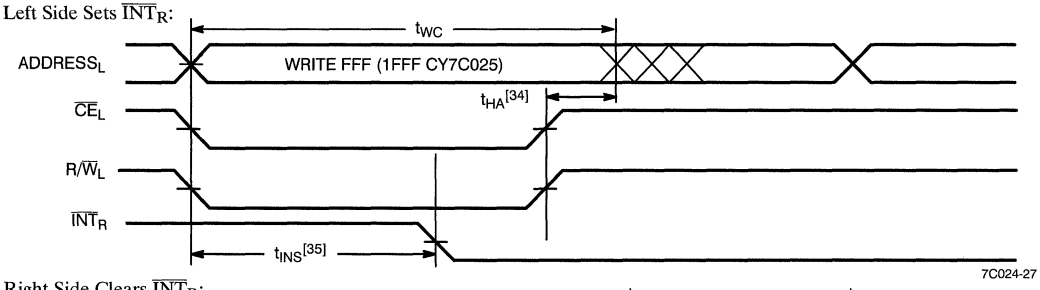


Note:
33. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

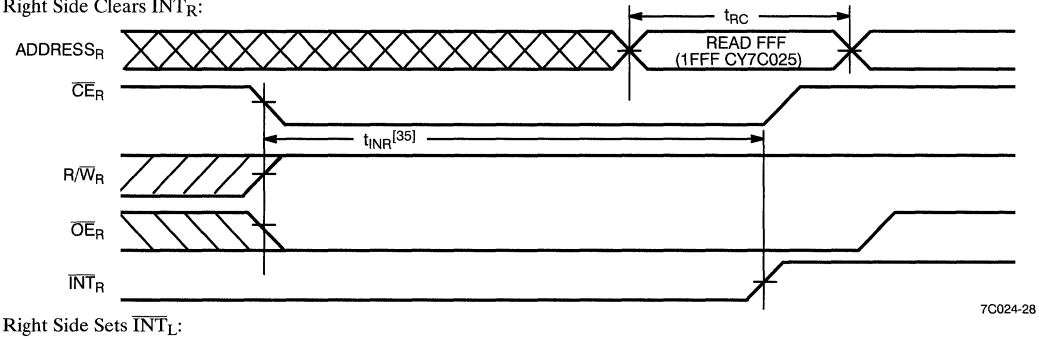
Switching Waveforms (continued)

Interrupt Timing Diagrams

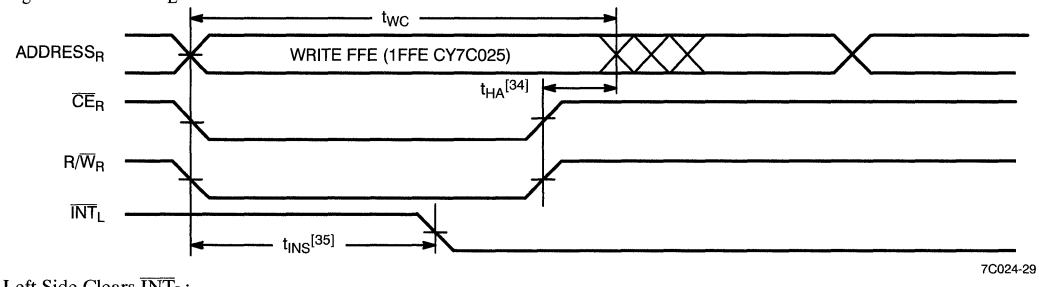
Left Side Sets $\overline{INT}_R$:



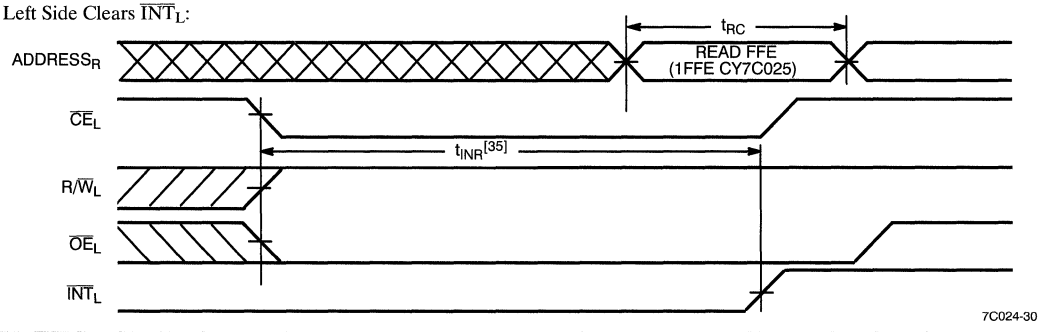
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:

34. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
35. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7C024/0241 and CY7C025/0251 consist of an array of 4K words of 16/18 bits each and 8K words of 16/18 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C024/0241 and CY7C025/0251 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C024/0241 and CY7C025/0251 have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7C024/0241 or CY7C025/0251 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024/0241, 1FFF for the CY7C025/0251) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024/0241, 1FFE for the CY7C025/0251) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and thus resetting the interrupt to it.

If your application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2*.

Busy

The CY7C024/0241 and CY7C025/0251 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but which one is not predictable. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C024/0241 and CY7C025/0251 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all sixteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

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Table 1. Non-Contending Read/Write

Inputs						Outputs		Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	$I/O_8-I/O_{15}$	$I/O_0-I/O_7$	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	⎍	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	⎍	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L=\overline{BUSY}_R$=HIGH)[36]

	Left Port					Right Port				
Function	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-11L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-11R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	(1)FFF	X	X	X	X	X	L[38]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	(1)FFF	H[37]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[37]	L	L	X	(1)FFE	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	(1)FFE	H[38]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	D_0-D_{15} Left	D_0-D_{15} Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes:
36. A_{0L-12L} and A_{0R-12R}, 1FFF/1FFE for the CY7C025.
37. If $\overline{BUSY}_R$=L, then no change.
38. If $\overline{BUSY}_L$=L, then no change.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C024–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–15JC	J83	84-Lead Plastic Leaded Chip Carrier	
25	CY7C024–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–25JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–25JI	J83	84-Lead Plastic Leaded Chip Carrier	
35	CY7C024–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–35JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–35JI	J83	84-Lead Plastic Leaded Chip Carrier	
55	CY7C024–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C024–55JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C024–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C024–55JI	J83	84-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C025–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–15JC	J83	84-Lead Plastic Leaded Chip Carrier	
25	CY7C025–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–25JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–25JI	J83	84-Lead Plastic Leaded Chip Carrier	
35	CY7C025–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–35JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–35JI	J83	84-Lead Plastic Leaded Chip Carrier	
55	CY7C025–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C025–55JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C025–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C025–55JI	J83	84-Lead Plastic Leaded Chip Carrier	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0241–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0241–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0241–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0241–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0241–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0251–15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
25	CY7C0251–25AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–25AI	A100	100-Pin Thin Quad Flat Pack	Industrial
35	CY7C0251–35AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–35AI	A100	100-Pin Thin Quad Flat Pack	Industrial
55	CY7C0251–55AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C0251–55AI	A100	100-Pin Thin Quad Flat Pack	Industrial

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Timing Technology 7

Timing Technology

CY7B991
CY7B992

Programmable Skew Clock Buffer (PSCB)

Features

- **All output pair skew <100 ps typical (250 max.)**
- **3.75- to 80-MHz output operation**
- **User-selectable output functions**
  - **— Selectable skew to 18 ns**
  - **— Inverted and non-inverted**
  - **— Operation at ½ and ¼ input frequency**
  - **— Operation at 2x and 4x input frequency (input as low as 3.75 MHz)**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **32-pin PLCC/LCC package**
- **Jitter < 200 ps peak-to-peak (< 25 ps RMS)**
- **Compatible with a Pentium ™-based processor**

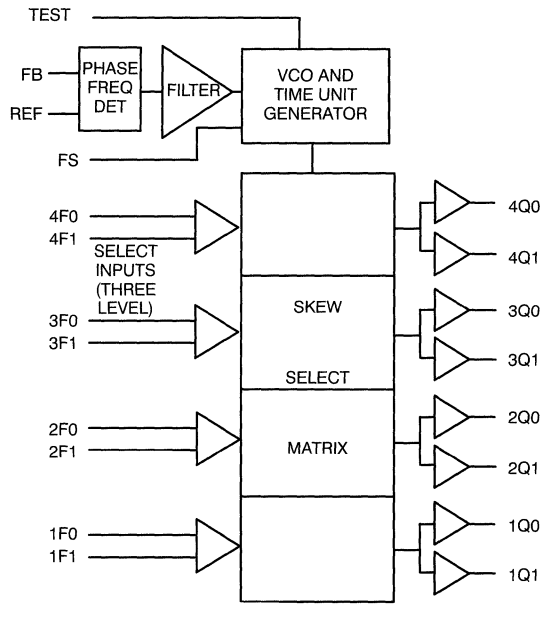
Functional Description

The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user-selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this "zero delay" capability of the PSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

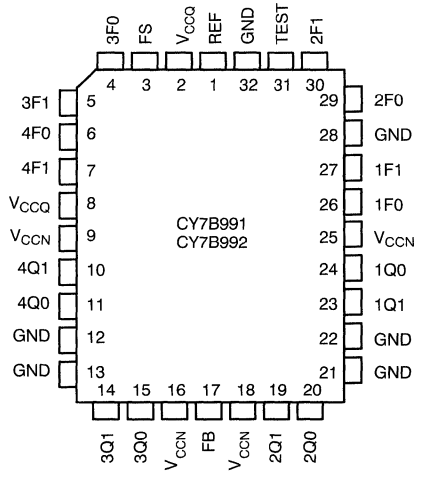
Logic Block Diagram



7B991-1

Pin Configuration

PLCC/LCC



7B991-2

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Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three-level frequency range select. See *Table 1.*
1F0, 1F1	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See *Table 2.*
2F0, 2F1	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See *Table 2.*
3F0, 3F1	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See *Table 2.*
4F0, 4F1	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See *Table 2.*
TEST	I	Three-level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	O	Output pair 1. See *Table 2.*
2Q0, 2Q1	O	Output pair 2. See *Table 2.*
3Q0, 3Q1	O	Output pair 3. See *Table 2.*
4Q0, 4Q1	O	Output pair 4. See *Table 2.*
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in *Table 1.*

Table 1. Frequency Range Select and t_U Calculation[1]

FS[2, 3]	f_{NOM} (MHz) Min.	f_{NOM} (MHz) Max.	$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. *Table 2* below shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations[1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see *Table 2*). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.

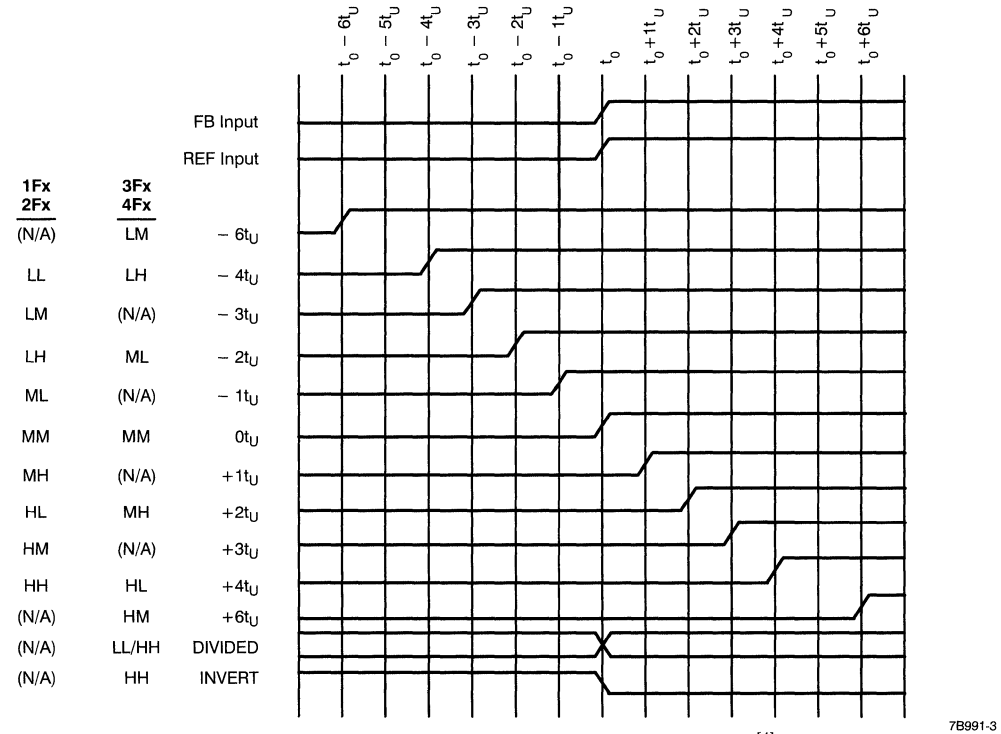


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output[4]

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991/CY7B992 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

4. FB connected to an output selected for "zero" skew (i.e., xF1 = xF0 = MID).
5. Indicates case temperature.

Electrical Characteristics Over the Operating Range[6]

Parameter	Description	Test Conditions	CY7B991 Min.	CY7B991 Max.	CY7B992 Min.	CY7B992 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 16 mA	2.4				V
		V_{CC} = Min., I_{OH} = − 40 mA			V_{CC}−0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} =46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		− 0.5	0.8	− 0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS, xFn)[7]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	− 500		− 500		µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = V_{CC}/2	− 50	50	− 50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		− 200		− 200	µA
I_{OS}	Output Short Circuit Current[8]	V_{CC} = Max., V_{OUT} = GND (25°C only)		− 250		N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open — Com'l		85		85	mA
		Mil/Ind		90		90	
I_{CCN}	Output Buffer Current per Output Pair[9]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}		14		19	mA
PD	Power Dissipation per Output Pair[10]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}		78		104[11]	mW

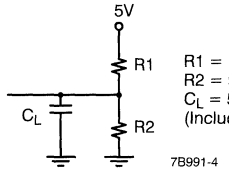
Capacitance[12]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

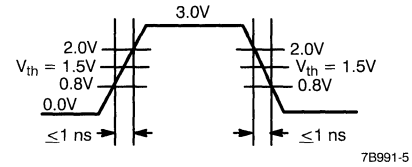
6. See the last page of this specification for Group A subgroup testing information.
7. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
8. CY7B991 should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B992 outputs should not be shorted to GND. Doing so may cause permanent damage.
9. Total output current per output pair can be approximated by the following expression that includes device current plus load current:
   CY7B991:
   I_{CCN} = [(4 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N] x 1.1
   CY7B992:
   I_{CCN} = [(3.5 + .17F) + [((1160 − 2.8F)/Z) + (.0025FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
10. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
    CY7B991:
    PD = [(22 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N] x 1.1
    CY7B992:
    PD = [(19.25 + 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] x 1.1
    See note 9 for variable definition.
11. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
12. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

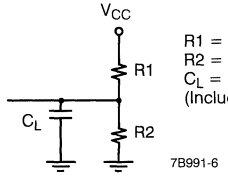


R1 = 130
R2 = 91
C_L = 50 pF (C_L = 30pF for −2 and −5 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B991)

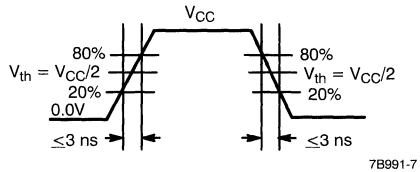


TTL Input Test Waveform (CY7B991)



R1 = 100
R2 = 100
C_L = 50 pF (C_L = 30pF for−2 and −5 devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B992)



CMOS Input Test Waveform (CY7B992)

Switching Characteristics Over the Operating Range[2, 13]

Parameter	Description		CY7B991−2[14] Min.	Typ.	Max.	CY7B992−2[14] Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2, 3]	40		80	40		80[15]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[16, 17]			0.05	0.20		0.05	0.20	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[16, 18, 19]			0.1	0.25		0.1	0.25	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[16, 20]			0.25	0.5		0.25	0.5	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[16, 20]			0.3	0.5		0.3	0.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[16, 20]			0.25	0.5		0.25	0.5	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[16, 20]			0.5	0.9		0.5	0.7	ns
t_{DEV}	Device-to-Device Skew[14, 21]				0.75			0.75	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.25	0.0	+0.25	− 0.25	0.0	+0.25	ns
t_{ODCV}	Output Duty Cycle Variation[22]		− 0.65	0.0	+0.65	− 0.5	0.0	+0.5	ns
t_{PWH}	Output HIGH Time Deviation from 50%[23, 24]				2.0			3.0	ns
t_{PWL}	Output LOW Time Deviation from 50%[23, 24]				1.5			3.0	ns
t_{ORISE}	Output Rise Time[23, 25]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time[23, 25]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time[26]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[14]			25			25	ps
		Peak-to-Peak[14]			200			200	ps

Switching Characteristics Over the Operating Range[2, 13] (continued)

Parameter	Description		CY7B991–5 Min.	CY7B991–5 Typ.	CY7B991–5 Max.	CY7B992–5 Min.	CY7B992–5 Typ.	CY7B992–5 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2, 3]	40		80	40		80[15]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[16, 17]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[16, 18]			0.25	0.5		0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[16, 20]			0.6	0.7		0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[16, 20]			0.5	1.0		0.6	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[16, 20]			0.5	0.7		0.5	0.7	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[16, 20]			0.5	1.0		0.6	1.7	ns
t_{DEV}	Device-to-Device Skew[14, 21]				1.25			1.25	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.5	0.0	+0.5	− 0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[22]		− 1.0	0.0	+1.0	− 1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50%[23, 24]				2.5			4.0	ns
t_{PWL}	Output LOW Time Deviation from 50%[23, 24]				3			4.0	ns
t_{ORISE}	Output Rise Time[23, 25]		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{OFALL}	Output Fall Time[23, 25]		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{LOCK}	PLL Lock Time[26]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[14]			25			25	ps
		Peak-to-Peak[14]			200			200	ps

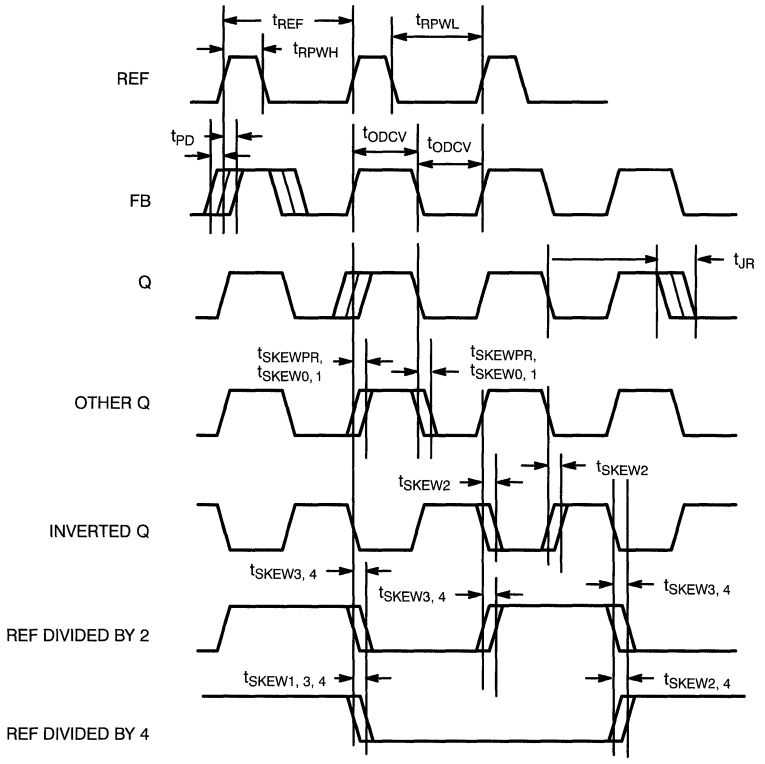
Notes:

13. Test measurement levels for the CY7B991 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B992 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
14. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
15. Except as noted, all CY7B992–2 and –5 timing parameters are specified to 80-MHz with a 30-pF load.
16. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
17. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
18. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
19. C_L=OpF. For C_L=30pF, t_{SKEW0}=0.35ns.
20. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
21. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)
22. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
23. Specified with outputs loaded with 30 pF for the CY7B99X–2 and –5 devices and 50 pF for the CY7B99X–7 devices. Devices are terminated through 50Ω to 2.06V (CY7B991) or $V_{CC}/2$ (CY7B992).
24. t_{PWH} is measured at 2.0V for the CY7B991 and 0.8 V_{CC} for the CY7B992. t_{PWL} is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
25. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or 0.8V_{CC} and 0.2V_{CC} for the CY7B992.
26. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics Over the Operating Range[2, 13] (continued)

Parameter	Description		CY7B991–7 Min.	CY7B991–7 Typ.	CY7B991–7 Max.	CY7B992–7 Min.	CY7B992–7 Typ.	CY7B992–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[1, 2]	15		30	15		30	MHz
		FS = MID[1, 2]	25		50	25		50	
		FS = HIGH[1, 2]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_U	Programmable Skew Unit		See *Table 1*						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1)[16, 17]			0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs)[16, 18]			0.3	0.75		0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[16, 20]			0.6	1.0		0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[16, 20]			1.0	1.5		1.0	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[16, 20]			0.7	1.2		0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[16, 20]			1.2	1.7		1.2	1.7	ns
t_{DEV}	Device-to-Device Skew[14, 21]				1.65			1.65	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		− 0.7	0.0	+0.7	− 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[22]		− 1.2	0.0	+1.2	− 1.5	0.0	+1.5	ns
t_{PWH}	Output HIGH Time Deviation from 50%[23, 24]				3			5.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[23, 24]				3.5			5.5	ns
t_{ORISE}	Output Rise Time[23, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[23, 25]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[26]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[14]			25			25	ps
		Peak-to-Peak[14]			200			200	ps

AC Timing Diagrams



Operational Mode Descriptions

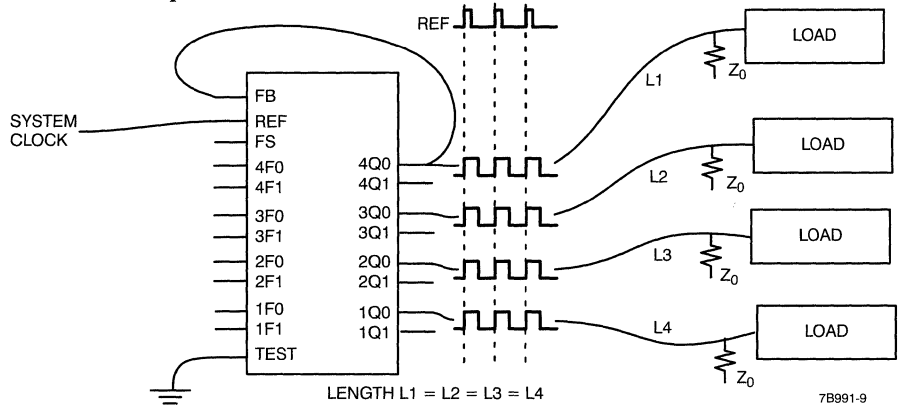


Figure 2. Zero-Skew and/or Zero-Delay Clock Driver

Figure 2 shows the PSCB configured as a zero-skew clock buffer. In this mode the 7B991/992 can be used as the basis for a low-skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

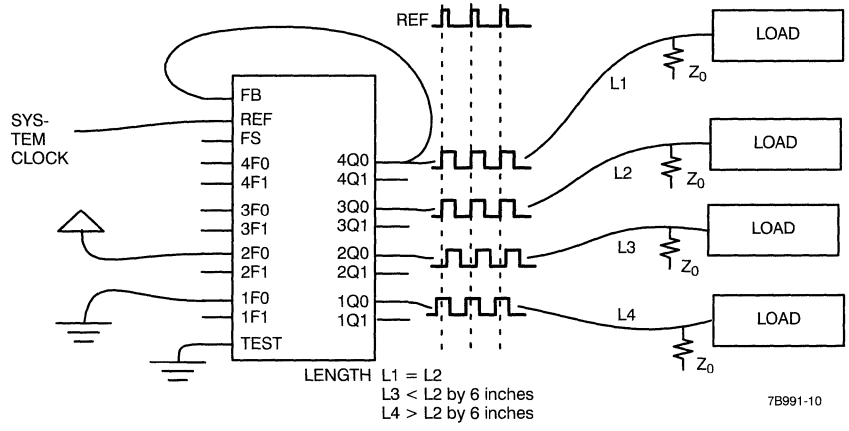


Figure 3. Programmable-Skew Clock Driver

Figure 3 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB can be programmed to stagger the timing of its outputs. The four groups of output pairs can each be programmed to different output timing. Skew timing can be adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0-ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to insure that all outputs have precise phase alignment.

Clock skews can be advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, it is possible to create wider output skews by proper selection of the xFn inputs. For example a $+10\ t_U$ between REF and 3Qx can be achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4\ t_U$ and 3Qx skews to $+6\ t_U$, a total of $+10\ t_U$ skew is realized.) Many other configurations can be realized by skewing both the output used as the FB input and skewing the other outputs.

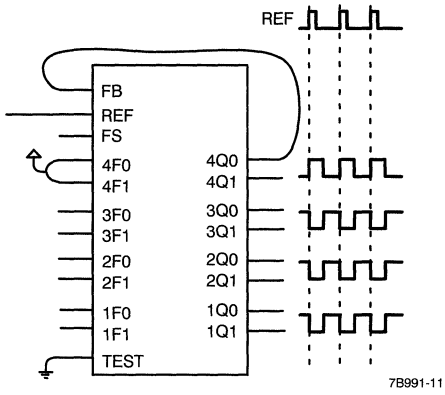


Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configuration would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 5 illustrates the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40-MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This will allow the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80-MHz operation because that is the frequency of the fastest output.

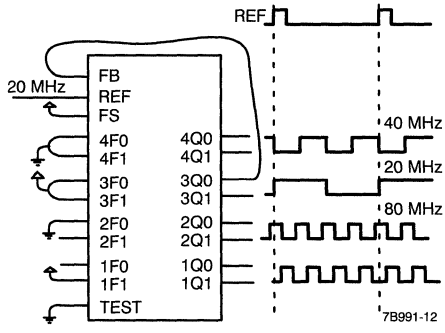


Figure 5. Frequency Multiplier with Skew Connections

Figure 6 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15- to 30-MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the "1X" clock. Without this feature, an external divider would need to be added, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the PSCB to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The PSCB can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

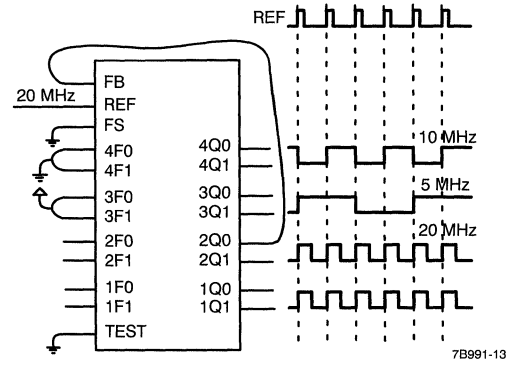


Figure 6. Frequency Divider Connections

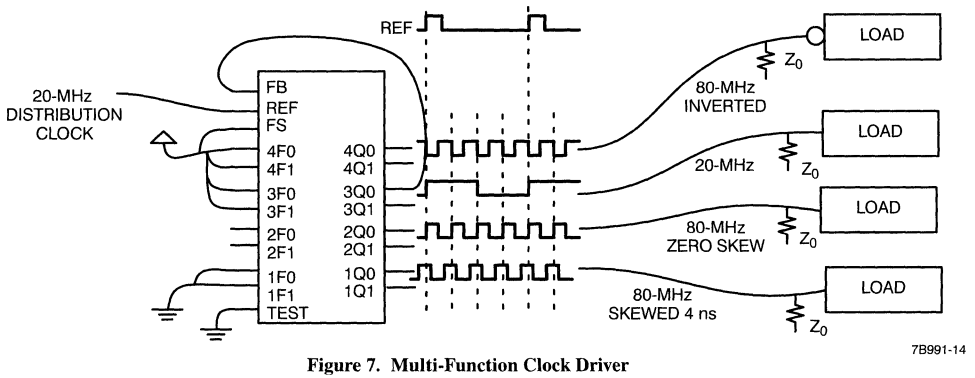


Figure 7. Multi-Function Clock Driver

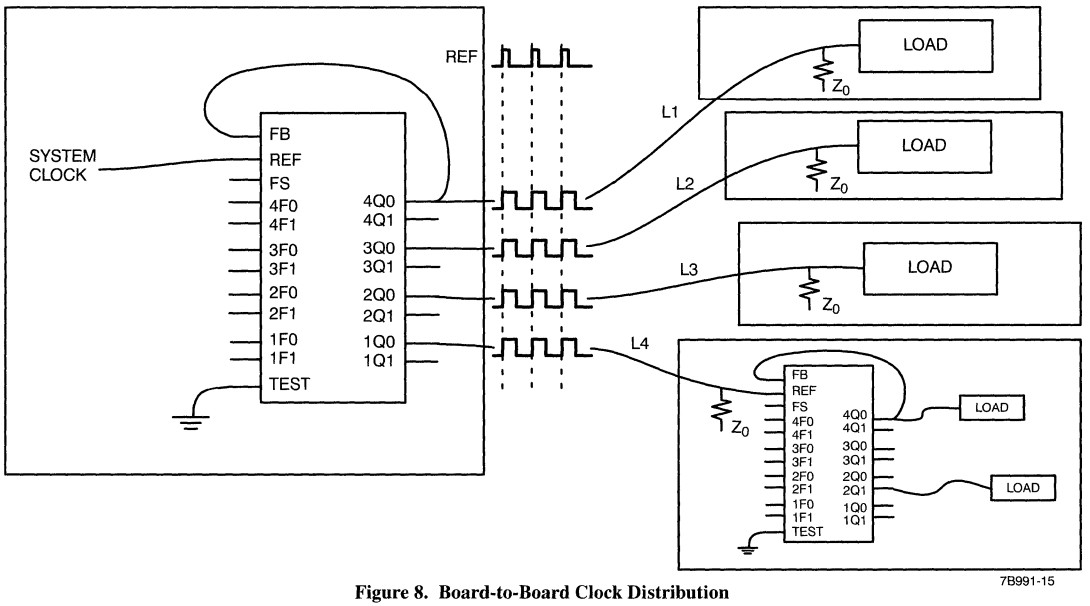


Figure 8. Board-to-Board Clock Distribution

Figure 8 shows the CY7B991/992 connected in series to construct a zero-skew clock distribution tree between boards. Delays of the downstream clock buffers can be programmed to compensate for the wire length (i.e., select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero-delay clock tree. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is recommended that not more than two clock buffers be connected in series.

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7B991–2JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
500	CY7B991–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–5JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
750	CY7B991–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B991–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B991–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
250	CY7B992–2JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
500	CY7B992–5JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–5JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
750	CY7B992–7JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B992–7JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B992–7LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
V_{IHH}	1, 2, 3
V_{IMM}	1, 2, 3
V_{ILL}	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{IHH}	1, 2, 3
I_{IMM}	1, 2, 3
I_{ILL}	1, 2, 3
I_{CCQ}	1, 2, 3
I_{CCN}	1, 2, 3

Document #: 38–00188–G

CY7B9910
CY7B9920

Low Skew Clock Buffer

Features

- **All outputs skew <100 ps typical (250 max.)**
- **15- to 80-MHz output operation**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **24-pin SOIC package**
- **Jitter: <200 ps peak to peak, <25 ps RMS**
- **Compatible with Pentium™-based processors**

Functional Description

The CY7B9910 and CY7B9920 Low Skew Clock Buffers offer low-skew system clock distribution. These multiple-output clock drivers optimize the timing of high-performance computer systems. Eight individual drivers can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B9910 TTL or CY7B9920 CMOS).

The completely integrated PLL allows "zero delay" capability. External divide capability, combined with the internal PLL, allows distribution of a low-frequency clock that can be multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO

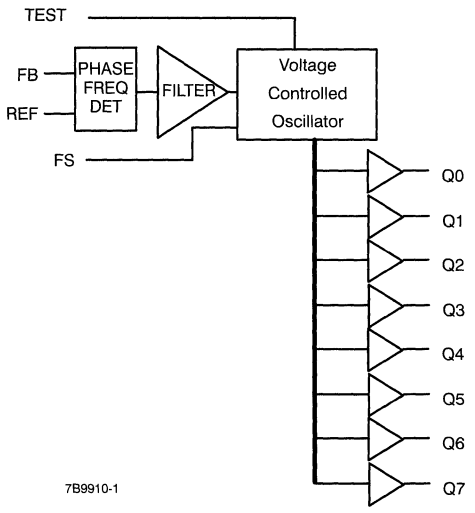
The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

Test Mode

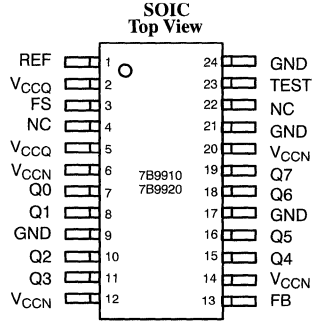
The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910/CY7B9920 to operate as explained above. (For testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase-locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

Logic Block Diagram



Pin Configuration



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Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS[9, 10, 11]	I	Three-level frequency range select.
TEST	I	Three-level select. See Test Mode section.
Q[0..7]	O	Clock outputs.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		CY7B9920		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −16 mA	2.4				V
		V_{CC} = Min., I_{OH} = −40 mA			V_{CC} − 0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} = 46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} − 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		−0.5	0.8	−0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC} − 1V	V_{CC}	V_{CC} − 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 − 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	−500		−500		µA
I_{IHH}	Input HIGH Current (Test, FS)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS)	V_{IN} = V_{CC}/2	−50	50	−50	50	µA
I_{ILL}	Input LOW Current (Test, FS)	V_{IN} = GND		−200		−200	µA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		CY7B9910 Min.	CY7B9910 Max.	CY7B9920 Min.	CY7B9920 Max.	Unit
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND (25°C only)			−250		N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open	Com'l		85		85	mA
			Mil/Ind		90		90	
I_{CCN}	Output Buffer Current per Output Pair[3]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			14		19	mA
PD	Power Dissipation per Output Pair[4]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			78		104[5]	mW

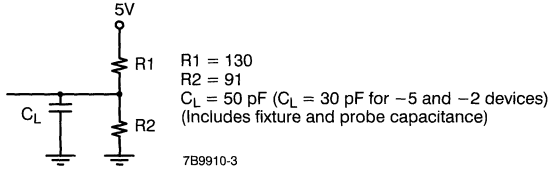
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

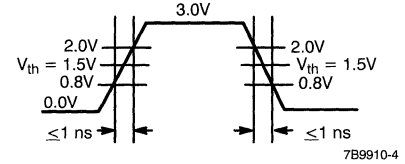
Notes:

1. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B9920 outputs are not short circuit protected.
3. Total output current per output pair can be approximated by the following expression that includes device current plus load current:
   CY7B9910:
   I_{CCN} = [(4 + 0.11F) + [((835 − 3F)/Z) + (.0022FC)]N] x 1.1
   CY7B9920:
   I_{CCN} = [(3.5+ .17F) + [((1160 − 2.8F)/Z) + (.0025FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F * C
4. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   CY7B9910:
   PD = [(22 + 0.61F) + [((1550 − 2.7F)/Z) + (.0125FC)]N] x 1.1
   CY7B9920:
   PD = [(19.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] x 1.1
   See note 3 for variable definition.
5. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
6. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

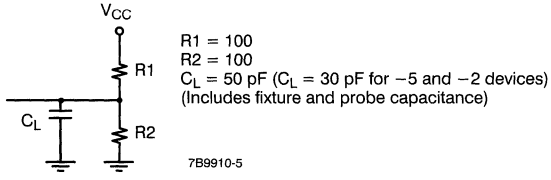
AC Test Loads and Waveforms



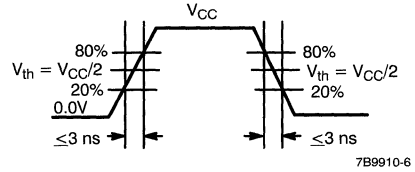
TTL AC Test Load (CY7B9910)



TTL Input Test Waveform (CY7B9910)



CMOS AC Test Load (CY7B9920)



CMOS Input Test Waveform (CY7B9920)

Switching Characteristics Over the Operating Range[7]

Parameter	Description		CY7B9910–2[8] Min.	Typ.	Max.	CY7B9920–2[8] Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		80[12]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.1	0.25		0.1	0.25	ns
t_{DEV}	Device-to-Device Skew[8, 15]				0.75			0.75	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		−0.25	0.0	+0.25	−0.25	0.0	+0.25	ns
t_{ODCV}	Output Duty Cycle Variation[16]		−0.65	0.0	+0.65	−0.65	0.0	+0.65	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak			200			200	ps
		RMS			25			25	ps

Parameter	Description		CY7B9910–5 Min.	Typ.	Max.	CY7B9920–5 Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		80[12]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.25	0.5		0.25	0.5	ns
t_{DEV}	Device-to-Device Skew[8, 15]				1.0			1.0	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		−0.5	0.0	+0.5	−0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[16]		−1.0	0.0	+1.0	−1.0	0.0	+1.0	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[8]			200			200	ps
		RMS[8]			25			25	ps

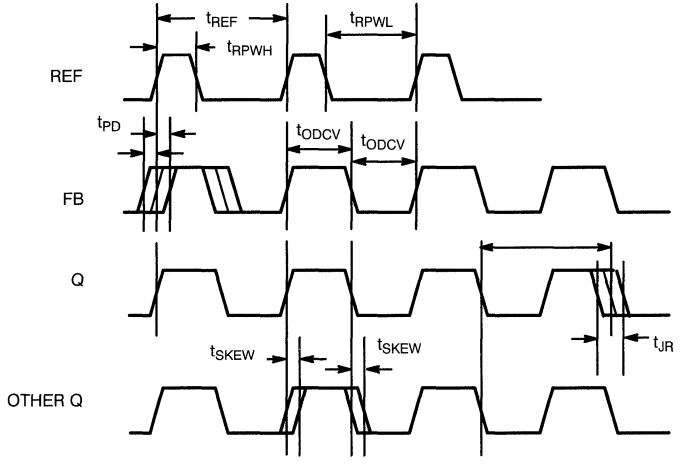
Notes:

7. Test measurement levels for the CY7B9910 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B9920 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions asume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
8. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
9. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
10. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be f_{NOM}/X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
11. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.
12. Except as noted, all CY7B9920–2 and –5 timing parameters are specified to 80-MHz with a 30-pF load.
13. SKEW is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
14. t_{SKEW} is defined as the skew between outputs.
15. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.).
16. t_{ODCV} is the deviation of the output from a 50% duty cycle.
17. Specified with outputs loaded with 30 pF for the CY7B99X0–2 and –5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
18. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B9910 or $0.8V_{CC}$ and $0.2V_{CC}$ for the CY7B9920.
19. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics Over the Operating Range[7] (continued)

Parameter	Description		CY7B9910–7 Min.	CY7B9910–7 Typ.	CY7B9910–7 Max.	CY7B9920–7 Min.	CY7B9920–7 Typ.	CY7B9920–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		50	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.3	0.75		0.3	0.75	ns
t_{DEV}	Device-to-Device Skew[8, 15]				1.5			1.5	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		– 0.7	0.0	+0.7	– 0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[16]		– 1.2	0.0	+1.2	– 1.2	0.0	+1.2	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[8]			200			200	ps
		RMS[8]			25			25	ps

AC Timing Diagrams



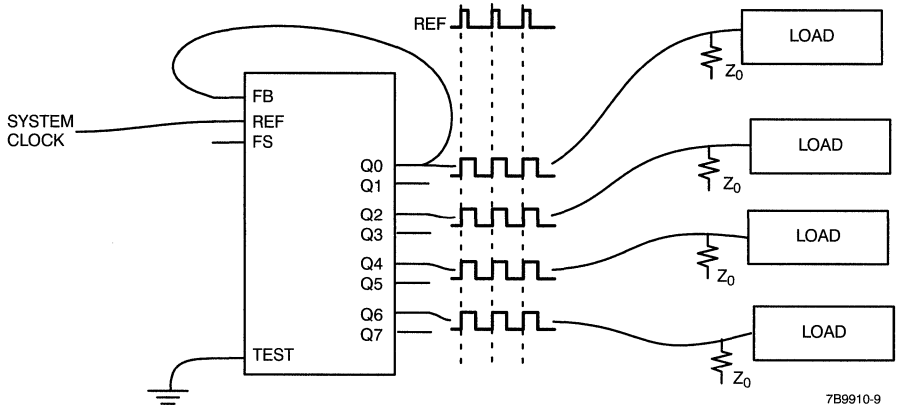


Figure 1. Zero-Skew and/or Zero-Delay Clock Driver

Operational Mode Descriptions

Figure 1 shows the device configured as a zero-skew clock buffer. In this mode the 7B9910/9920 can be used as the basis for a low-skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

Figure 2 shows the CY7B9910/9920 connected in series to construct a zero-skew clock distribution tree between boards. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.

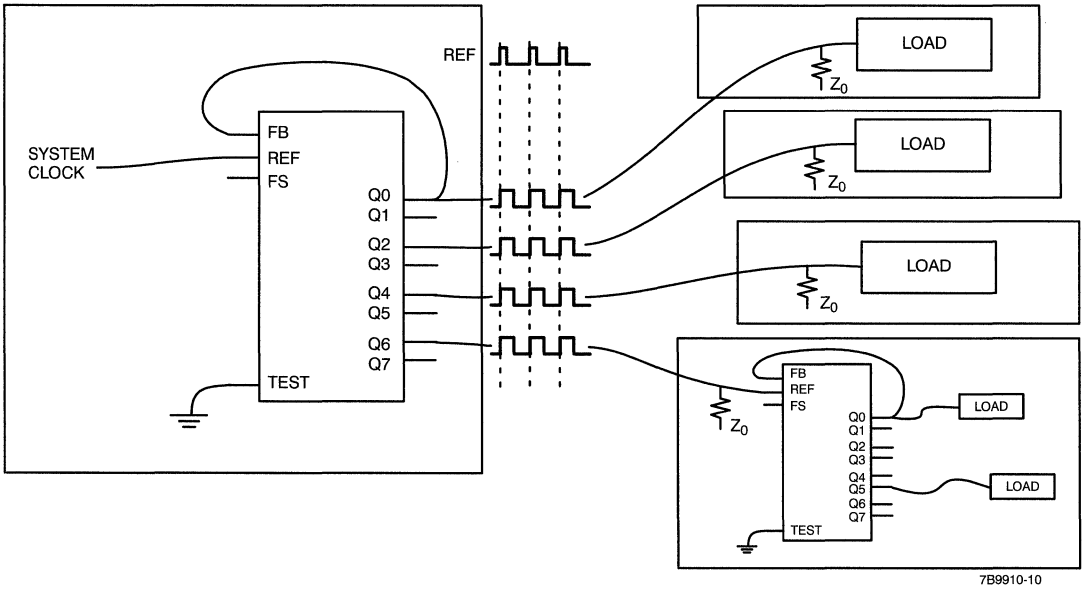


Figure 2. Board-to-Board Clock Distribution

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7B9910–2SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–2SC	S13	24-Lead Small Outline IC	
500	CY7B9910–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–5SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–5SI	S13	24-Lead Small Outline IC	Industrial
750	CY7B9910–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–7SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–7SI	S13	24-Lead Small Outline IC	Industrial

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Quality 8

Quality

Page Number

Description

Quality, Reliability, and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the beginning.

Some of the techniques used to insure product excellence are the following:

- Product Reliability is built into every product design, starting from the initial design conception.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Testing Categories

Three different testing categories are offered by Cypress:

1. Commercial operating range product: 0°C to +70°C.
2. Industrial operating range product: −40°C to +85°C.
3. Military SMD (Standard Military Drawing) product processed to QML Mil PRF 38535; Military operating range: −55°C to +125°C.

Miliary Product Assurance

Cypress under the QML program, uses MIL-STD-883 and MIL-PRF-38535 as baseline documents to determine our Test Methods, Procedures and General Specifications for Semiconductors.

Cypress's Military components and SMD products are processed per MIL-STD-883 using methods 5004 and 5005 to baseline our screening and quality conformance procedures. Refer to *Tables 3–7,* for the baseline flows and requirements. The processing performed by Cypress results in a product that meets the class B screening requirements as specified by these methods. Every device shipped, as a minimum, meets these requirements.

Commercial Product Assurance

Cypress is a ISO9000 certified supplier. All commercial and industrial temp range products are manufactured using the same controlled systems as our QML military product. *Tables 1* and *2* define the 100% screening and conformance inspection for commercial and industrial temp range product.

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883 Method	Product Temperature Ranges	
		Commercial 0°C to +70°C; Industrial −40°C to +85°C	
		Plastic	Hermetic
Visual/Mechanical			
• Internal Visual	2010	0.4% AQL	100%
• Hermeticity			
– Fine Leak	1014, Cond A or B (sample)	Does Not Apply	LTPD = 5
– Gross Leak	1014, Cond C	Does Not Apply	100%
Final Electrical	Per Device Specification		
• Static (DC), Functional, and Switching (AC) Tests	1. At Hot Temperature and Power Supply Extremes	100%	100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Note 1	Note 1
• Final Electrical Conformance	Cypress Method 17-00064	Note 1	Note 1

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883 Method	Product Temperature Ranges
		Commercial 0°C to +70°C; Industrial −40°C to +85°C
Final Electrical	Per Device Specification	
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supply Extremes	100%
	2. At Hot Temperature and Power Supply Extremes	100%
Cypress Quality Lot Acceptance		
• External Visual	2009	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	Note 1

Notes:
1. Lot acceptance testing is performed on every lot. AOQL (the Average Outgoing Quality Level) for 1995 was 0 PPM.

Table 3. Cypress QML/JAN/SMD/Military Product Screening Flows for Class B

Screen	Screening Per Method 5004 of MIL-STD-883	Product Temperature Ranges −55°C to +125°C	
		QML/JAN/SMD/Military Components[2]	Military Modules
Visual/Mechanical			
• Internal Visual	Method 2010, Cond B	100%	N/A
• Temperature Cycling	Method 1010, Cond C, (10 cycles)	100%	100%
• Constant Acceleration	Method 2001, Cond E (Min.), Y1 Orientation Only	100%	N/A
• Hermeticity: — Fine Leak — Gross Leak	 Method 1014, Cond A or B Method 1014, Cond C	 100% 100%	 N/A 100%
Burn-in			
• Pre-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%
• Burn-in Test	Method 1015, Cond D, 160 Hrs at 125°C Min. or 80 Hrs at 150°C	100%	100% (48 Hours at 125°C)
• Post-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA, for All Lots	5%	5%
Final Electrical Tests			
• Static Tests	Method 5005 Subgroups 1, 2, and 3	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Functional Tests	Method 5005 Subgroups 7, 8A, and 8B	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Switching	Method 5005 Subgroups 9, 10, and 11	100% Test to Applicable Device Specification	100% Test to Applicable Specification
Quality Conformance Tests			
• Group A	Method 5005, See *Table 4*	Sample	Sample
• Group B	Method 5005, See *Table 5*	Sample	Sample
• Group C[3]	Method 5005, See *Table* 6	Sample	Sample
• Group D[3]	Method 5005, See *Table* 7	Sample	Sample
External Visual	Method 2009	100%	100%

Notes:

2. QML product is allowed a reduction in screening requirements with DESC approval per MIL-PRF-38535.
3. Group C and D end-point electrical tests for QML/SMD/Military Grade products are performed to Group A subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.

8

Table 4. Group A Test Descriptions

Sub-group	Description	Sample Size/Accept No.	
		Components	Modules[4]
1	Static Tests at 25°C	116/0	116/0
2	Static Tests at Maximum Rated Operating Temperature	116/0	116/0
3	Static Tests at Minimum Rated Operating Temperature	116/0	116/0
4	Dynamic Tests at 25°C	116/0	116/0
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	116/0
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	116/0
7	Functional Tests at 25°C	116/0	116/0
8A	Functional Tests at Maximum Temperature	116/0	116/0
8B	Functional Tests at Minimum Temperature	116/0	116/0
9	Switching Tests at 25°C	116/0	116/0
10	Switching Tests at Maximum Temperature	116/0	116/0
11	Switching Tests at Minimum Temperature	116/0	116/0

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military products have a Group A sample test performed on each inspection lot per MIL-PRF-38535 or MIL-STD-883 and the applicable device specification.

Table 5. Group B Quality Tests

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[4]
2	Resistance to Solvents, Method 2015	3/0	3/0
3	Solderability, Method 2003[5]	22/0	3
5	Bond Strength, Method 2011[6]	15/0	NA

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 6. Group C Quality Tests

Sub-group	Description	LTPD	
		Components	Modules[4]
1	Steady State Life Test, End-Point Electricals, Method 1005, Cond D	45/0	15/0

Group C tests for all Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-PRF-38535/MIL-STD-883 from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

Table 7. Group D Quality Tests (Package Related)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
1	Physical Dimensions, Method 2016	15/0	15/0
2	Lead Integrity, Seal: Fine and Gross Leak, Method 2004 and 1014	45/0[5]	15/0 N/A for Seal
3	Thermal Shock, Temp-Cycling, Moisture Resistance, Seal: Fine and Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004, and 1014	15/0	15/0 N/A for Moisture Resistance; N/A for Fine Leak
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine and Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001, and 1014	15/0	15/0 N/A for Constant Acceleration; N/A for Fine Leak
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15/0	15/0 N/A for Fine Leak
6	Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018	3(0) or 5(1)	N/A
7	Adhesion of Lead Finish,[8] Method 2025	15/0	15/0
8	Lid Torque, Method 2024[9]	5(0)	N/A

Group D tests for all Military Grade procedures are performed per MIL-PRF-38535/MIL-STD-883 on each package type from each six months of production, based on the identification (or date) codes.

End-point electrical tests and parameters are performed per the applicable device specification.

Military Modules

- Military Temperature Grade Modules are designated with an 'M' suffix only. These modules are screened to standard combined flows and tested at both military temperature extremes.
- MIL-STD-883 Equivalent Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules. All MIL-STD-883 equivalent modules are assembled with fully compliant MIL-STD-883 components.

Notes:

4. Military Grade Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules. Alternate Group A method as detailed in JC-13-BP-123A.
5. Sample size is based upon leads taken from a minimum of 3 devices.
6. Sample size is based upon leads taken from a minimum of 4 devices.
7. Does not apply to leadless chip carriers.
8. Based on the number of leads.
9. Applies only to packages with glass seals.

Product Screening Summary Components

Commercial and Industrial Product

- Screened per *Table 1* product assurance flows
- Hermetic and molded packages available
- Incoming mechanical and electrical performance guaranteed:
  - 0.02% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.01% AQL External Visual Sample inspection
- Electrically tested to Cypress data sheet

Ordering Information

- Order Standard Cypress part number
- Parts marked the same as ordered part number
  Ex: CY7C122-15PC, PALC22V10-25PI

Military Product

- SMD and Military components are manufactured in compliance with paragraph 1.2.1 of MIL-STD-883. Compliant products are identified by an 'MB' suffix on the part number (CY7C122-25DMB) and the letter "C"
- QML devices are manufactured in accordance with MIL-PRF-38535. Compliant products are identified with the letter "Q."
- Military devices electrically tested to:
  - SMD devices are electrically tested to the applicable standard military drawing specifications

    OR
  - Cypress data sheet specifications
- All devices supplied in hermetic packages
- Quality conformance inspection: Method 5005, Groups A, B, C, and D performed as part of the standard process flow
- Burn-in performed on all devices
  - Cypress detailed circuit specification for non-JAN devices
- Static functional and switching tests performed at 25°C as well as temperature and power supply extremes on 100% of the product in every lot

Ordering Information

SMD Product:

- Order per military document
- Marked per military document
  Ex: 5962-8867001LA

Military Product:

- Order per Cypress standard military part number
- Marked the same as ordered part number
  Ex: CY7C122-25DMB

8

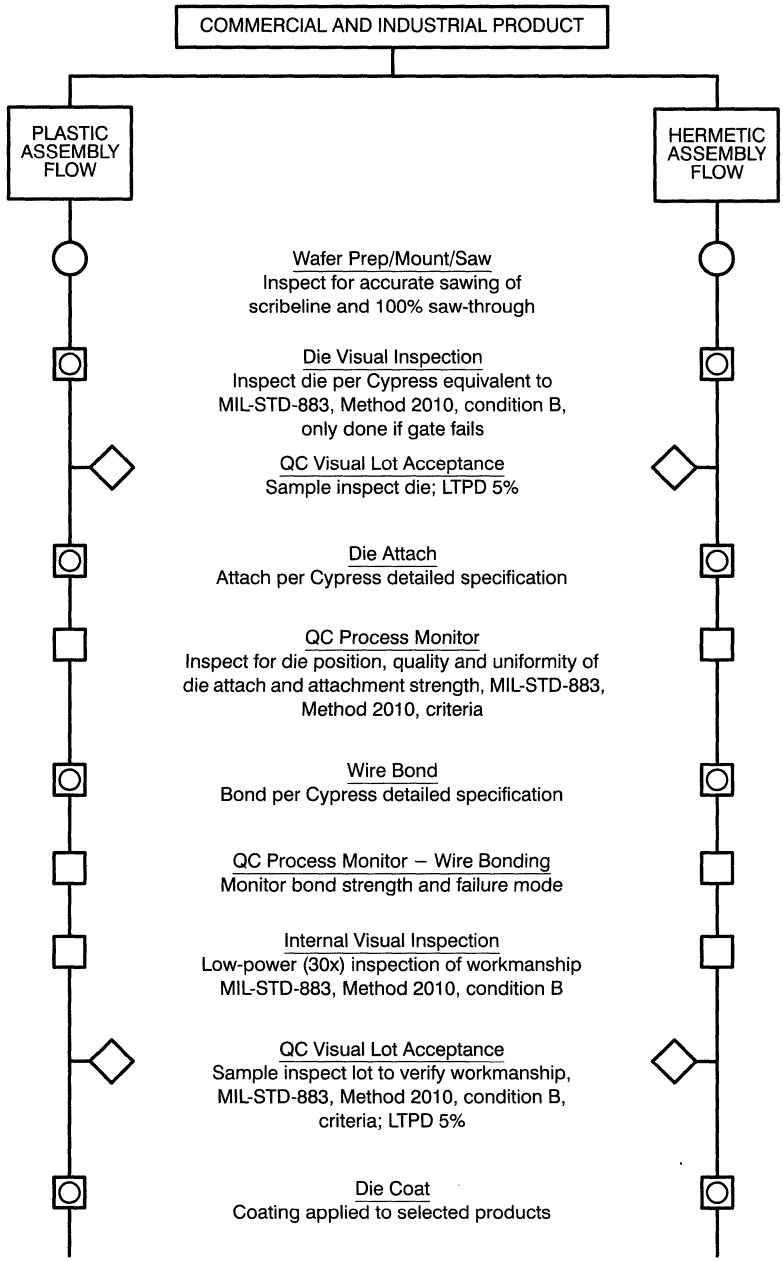
Product Quality Assurance Flow—Components

Area	PROCESS	Process Details
QC	INCOMING MATERIALS INSPECTION	All incoming materials are inspected to documented procedures covering the handling, inspection, storage, and release of raw materials used in the manufacture of Cypress products. Materials inspected are: wafers, masks, leadframes, ceramic packages and/or piece parts, molding compounds, gases, chemicals, etc.
FAB	DIFFUSION/ION IMPLANTATION	Sheet resistance, implant dose, species and CV characteristics are measured for all critical implants on every product run. Test wafers may be used to collect this data instead of actual production wafers. If this is done, they are processed with the standard product prior to collecting specific data. This insures accurate correlation between the actual product and the wafers used to monitor implantation.
FAB	OXIDATION	Sample wafers and sample sites are inspected on each run from various positions of the furnace load to inspect for oxide thickness.The integrity of critical oxides is monitored at electrical test.
FAB	PHOTOLITHOGRAPHY /ETCHING	Appearance of resist is checked by the operator after the spin operation. Also, after the film is developed, both dimensions and appearance are checked by the operator on a sample of wafers and locations upon each wafer. Final CDs and alignment are also sample inspected on several wafers and sites on each wafer on every product run.
FAB	METALIZATION	Film thickness is monitored on a daily basis. Step coverage cross-sections are performed on a periodic basis to insure coverage.
FAB	PASSIVATION	Film thickness is verified on a sample of wafers and locations on each run. Film stress is monitored on a weekly basis.
FAB	QC VISUAL OF WAFERS	
FAB	E-TEST	Electrical test is performed for final process electrical characteristics on every wafer.
FAB	QC MONITOR OF E-TEST DATA	Weekly review of all data trends; running averages, minimums, maximums, etc. are reviewed with the process control manager.
TEST	WAFER PROBE/SORT	Verify functionality, electrical characteristics, stress test devices.
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	Pass/fail lot based on yield and correct probe placement.

TO ASSEMBLY AND TEST

(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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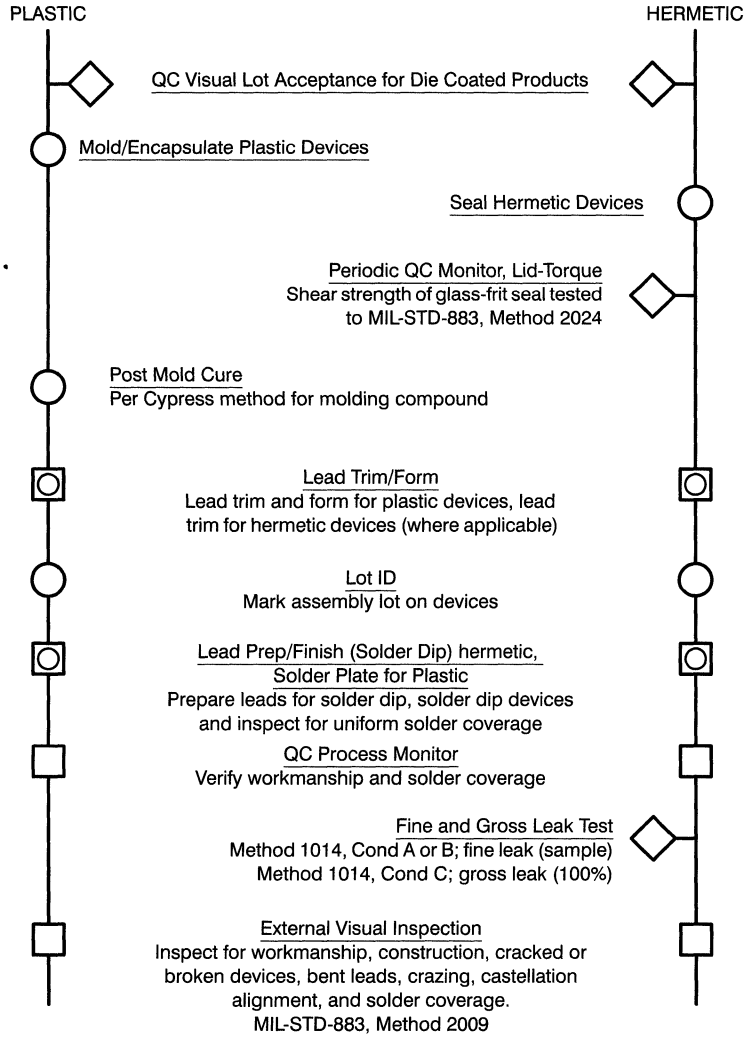
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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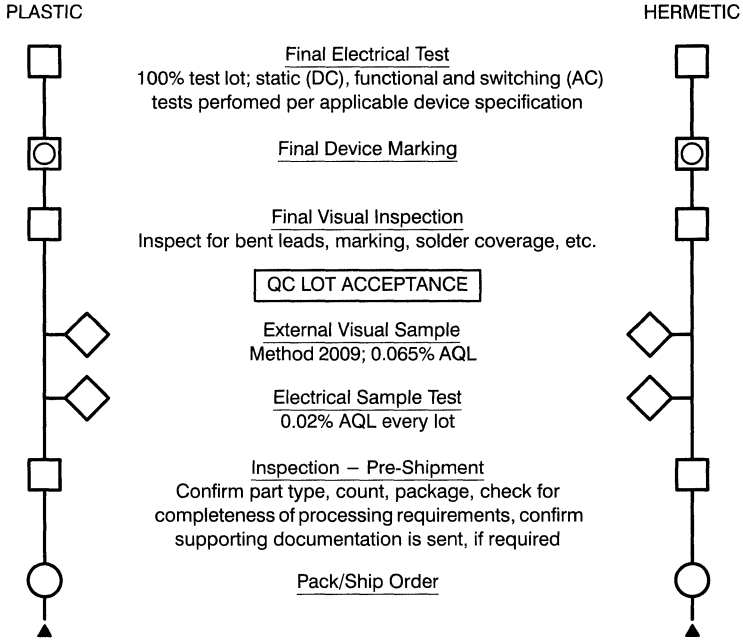
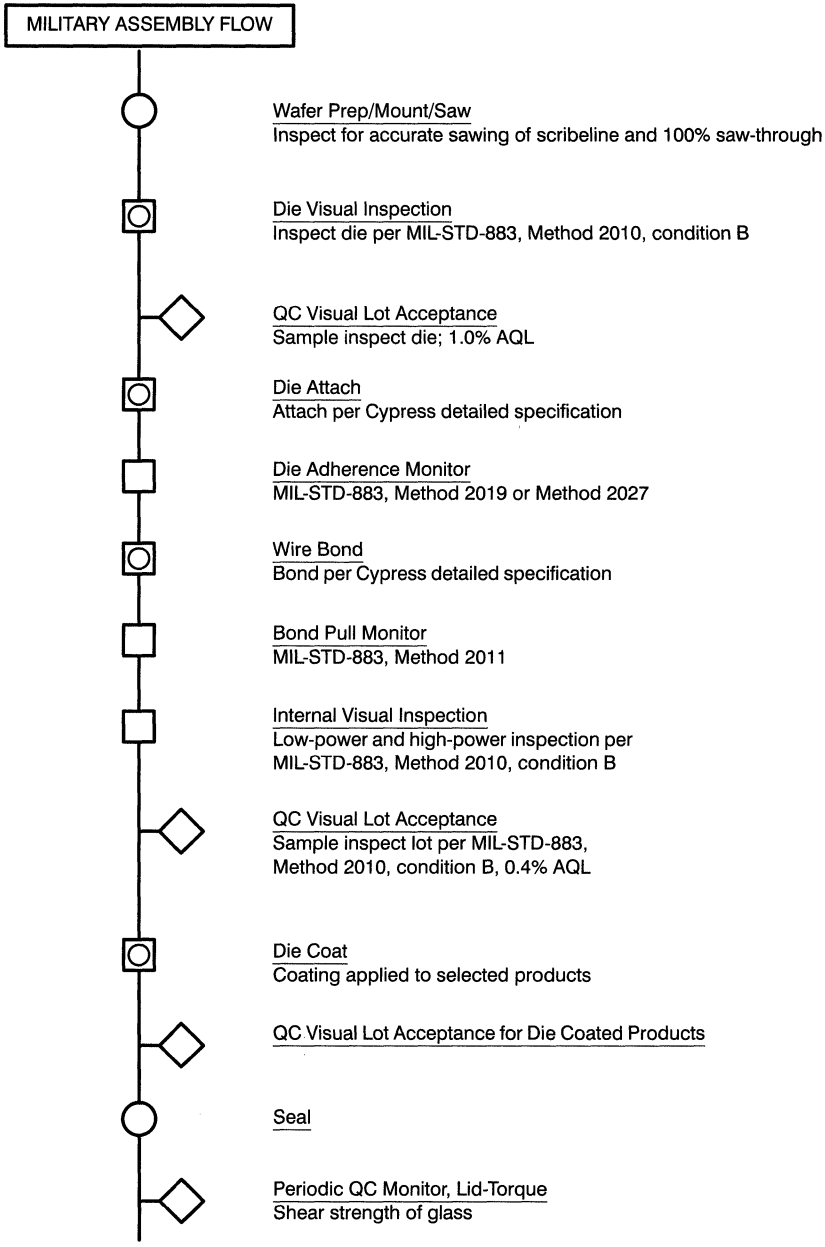
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Components
Military Components



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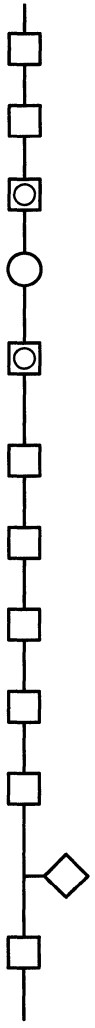
Product Quality Assurance Flow—Components (continued)
Military Components



Temperature Cycle
Method 1010, Cond C, 10 cycles

Constant Acceleration
Method 2001, Cond E, Y1 Orientation

Lead Trim
Lead trim when applicable

Lot ID
Mark assembly lot on devices

Lead Finish
Solder dip or matte tin plate applicable devices and inspect

QC Process Monitor
Verify workmanship and lead finish coverage

External Visual Inspection
Method 2009

Pre-Burn-In Electrical Test
Method 5004, per applicable device specification

Burn-In
Method 1015, condition D

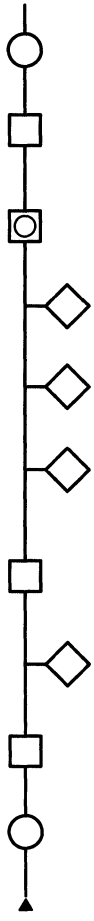
Post-Burn-In Electricals
Method 5004, per applicable device specification

PDA Calculation
Method 5004, 5%

Final Electrical Test
Method 5004; Static, functional and switching tests per applicable device specification

(continued)

Product Quality Assurance Flow—Components (continued)
Military Components



Lead Finish – Solder Dip
Solder dip applicable devices

Fine and Gross Leak Test
Method 1014, condition A or B, fine leak; condition C, gross leak

Final Device Marking
MIL-STD-883 or applicable device specification

Group B
Method 5005

Group A
Method 5005, per applicable device specification

Group C and D
Method 5005, in accordance with 1.2.1 of MIL-STD-883; JAN devices in accordance with MIL-PRF-38535

External Visual
Method 2009, 100% inspection

External Visual Sample
Method 2009, 0.01% AQL

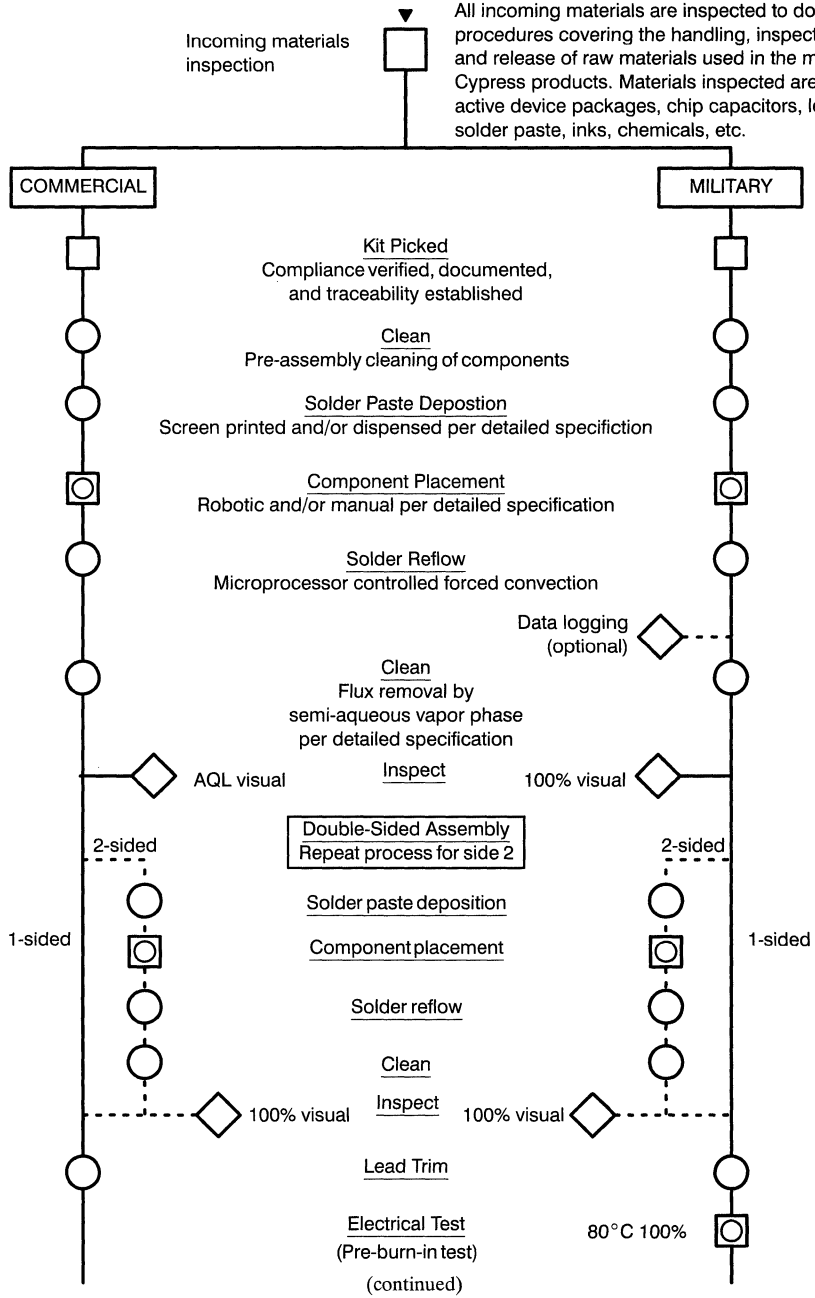
Plant Clearance

Pack/Ship Order

Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample Gate and Inspection

Product Quality Assurance Flow—Modules



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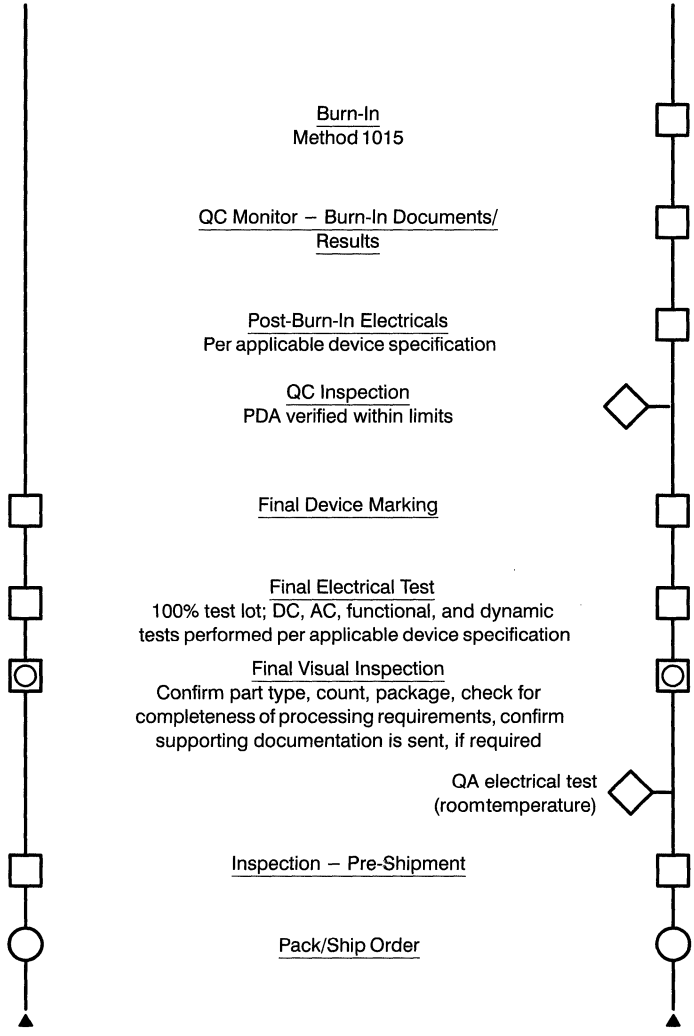
Product Quality Assurance Flow—Modules (continued)



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample gate and inspection

Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008, which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program monitors our most advanced technologies and packages. Every technology produced at a given fabrication site (Tech. – Fab.) and all assembly houses are monitored at least quarterly. If failures occur, detailed failure analyses are performed and corrective actions are implemented. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Quarterly Reliability Monitor Test Matrix

Stress	Sampling Strategy	Lots Tested per Quarter
HTOL	Technology–Fab Location	8
HTSSL	Technology–Fab Location	8
TEV	Technology–Fab Location	8
DRET	Technology–Fab Location	2
HAST	Technology–Fab Location	8
	Package–Assembly Location	10
TC	Technology–Fab Location	8
	Package–Assembly Location	12
PCT	Package–Assembly Location	10

Reliability Monitor Test Conditions

Test	Abbrev.	Temp. (°C)	R.H. (%)	Bias	Sample Size	LTPD	Read Points (hrs.)
High-Temperature Operating Life	HTOL	+125	N/A	5.75V Dynamic	116	2	96, 500, 1000
High-Temperature Steady-State Life	HTSSL	+125	N/A	5.75V Static	116	2	96, 500, 1000
Data Retention for Plastic Packages	DRET	+165	N/A	N/A	76	3	168, 1000
Data Retention for Ceramic Packages	DRET2	+250	N/A	N/A	76	3	168, 500
Pressure Cooker	PCT	+121	100	N/A	76	3	96, 168
Highly Accelerated Stress Test	HAST	+140	85	5.5V Static	76	3	128
Temperature Cycling	TC	−65 to +150°C	N/A	N/A	45	5	300, 1000 Cycles
Temperature Extreme Verification	TEV	Commercial Hot & Cold 0 to +70°C	N/A	N/A	116	2	N/A

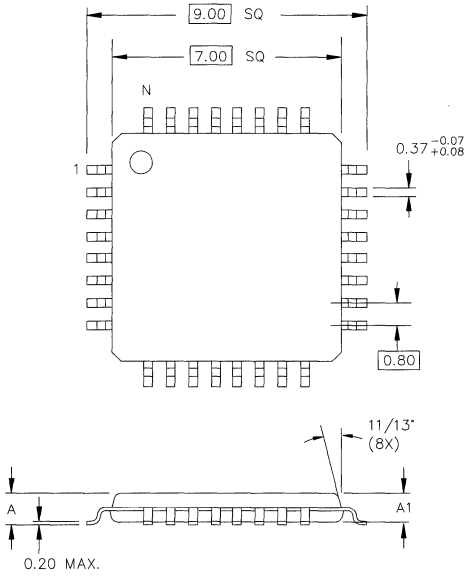
Packages 9

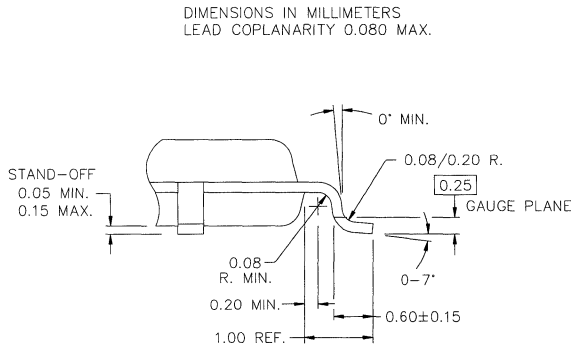
Package Diagrams

Package Diagrams

Thin Quad Flat Packs

32-Lead Plastic Thin Quad Flat Pack (TQFP) A32

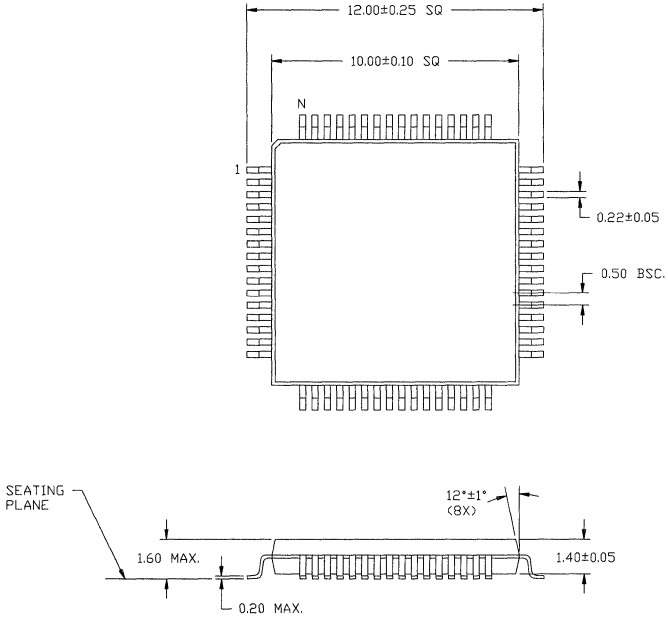




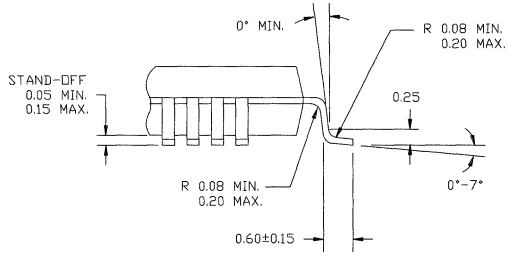
DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

Thin Quad Flat Packs (continued)

64-Pin Thin Quad Flat Pack A64

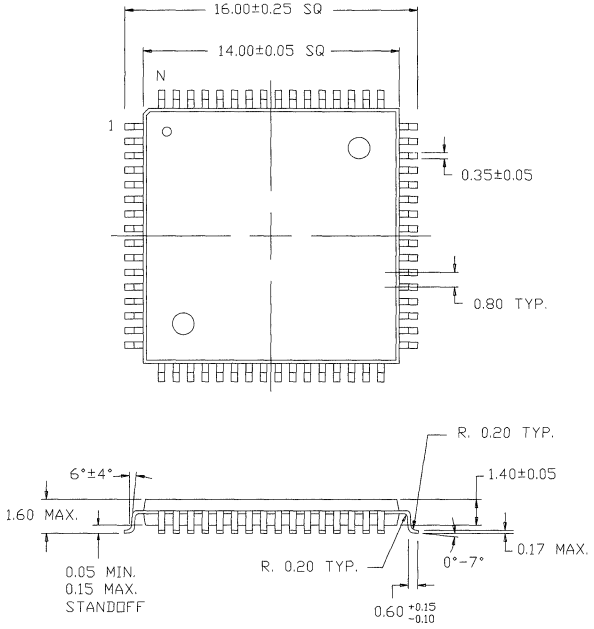


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



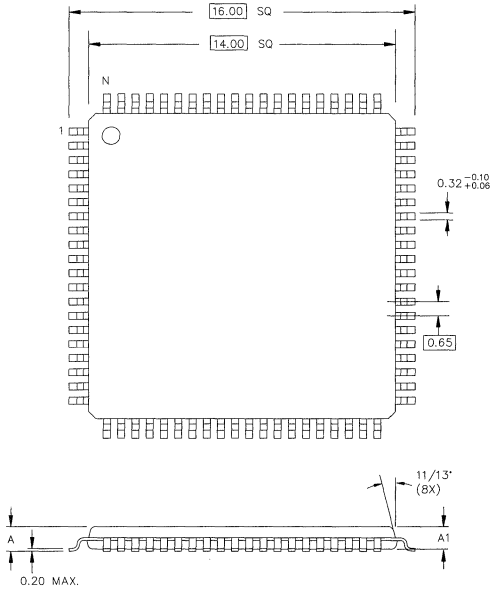
Thin Quad Flat Packs (continued)

64-Lead Thin Plastic Quad Flat Pack A65

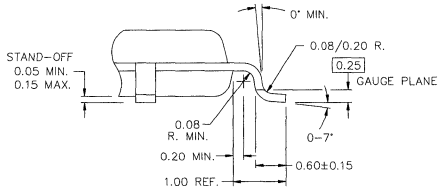


DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.100 MAX.

80-Pin Thin Plastic Quad Flat Pack A80



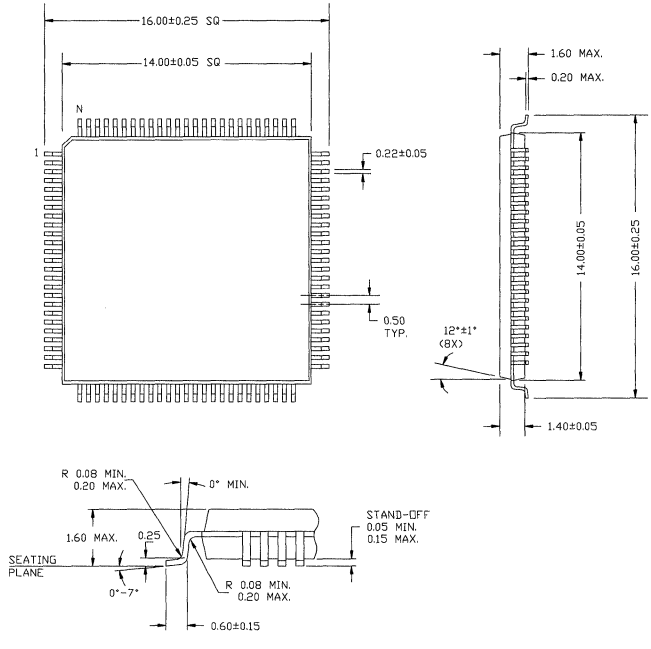
DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.080 MAX.



DIM. A	DIM. A1
1.60 MAX.	1.40±0.05 PKG. THICK
1.20 MAX.	1.00±0.05 PKG. THICK

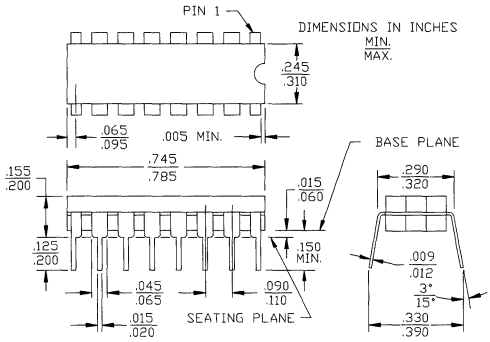
Thin Quad Flat Packs (continued)

100-Pin Plastic Thin Quad Flat Pack (TQFP) A100

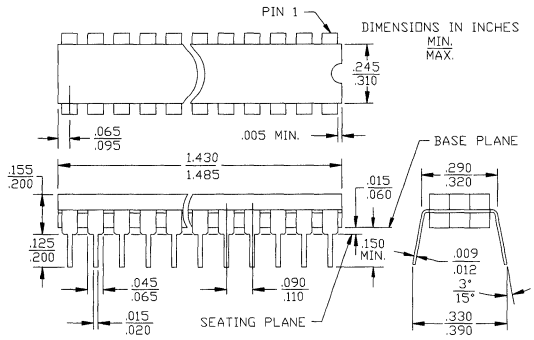


Ceramic Dual-In-Line Packages

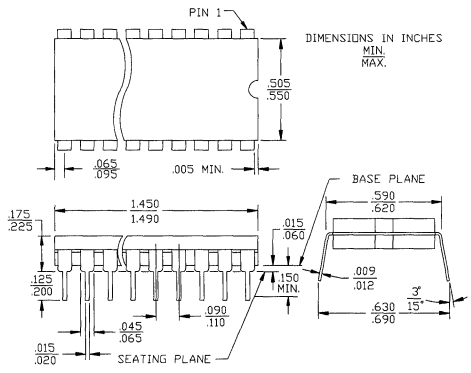
16-Lead (300-Mil) CerDIP D2
MIL–STD–1835 D–2 Config. A



28-Lead (300-Mil) CerDIP D22
MIL–STD–1835 D–15 Config. A

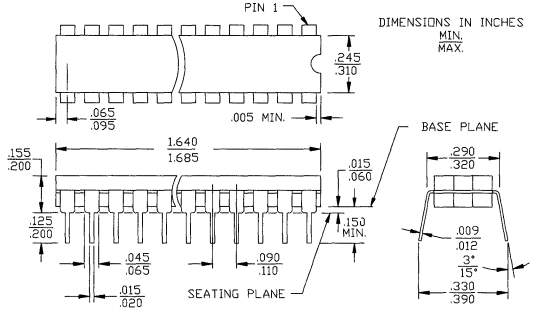


28-Lead (600-Mil) CerDIP D16
MIL–STD–1835 D–10 Config. A

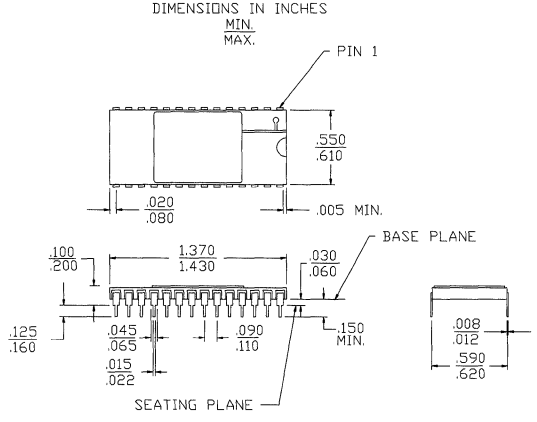


Ceramic Dual-In-Line Packages (continued)

32-Lead (300-Mil) CerDIP D32

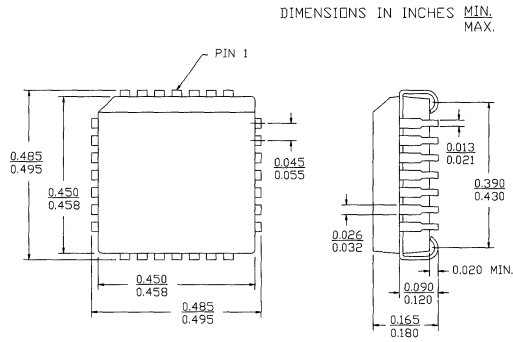


28-Lead (600-Mil) Sidebraze DIP D43

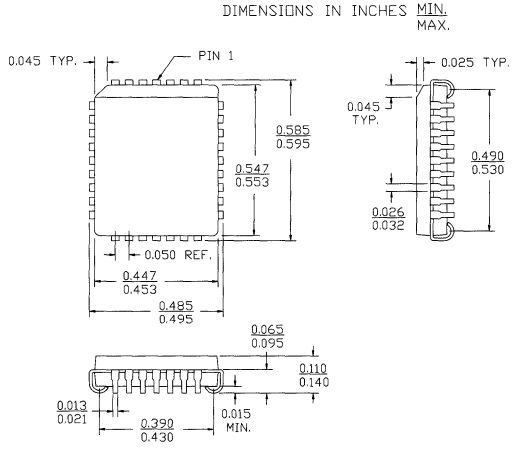


Plastic Leaded Chip Carriers

28-Lead Plastic Leaded Chip Carrier J64

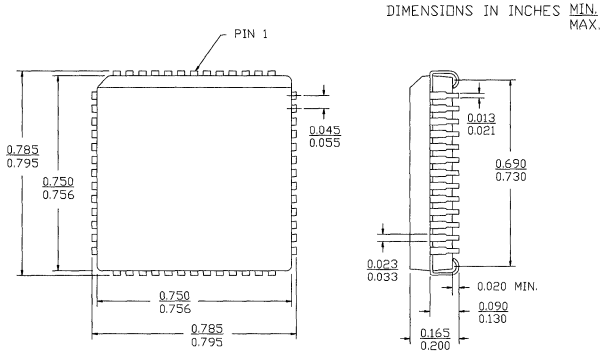


32-Lead Plastic Leaded Chip Carrier J65

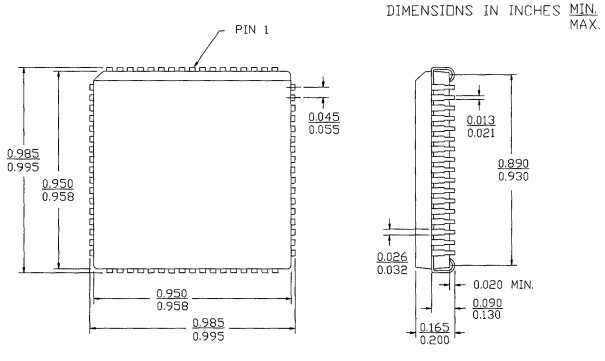


Plastic Leaded Chip Carriers (continued)

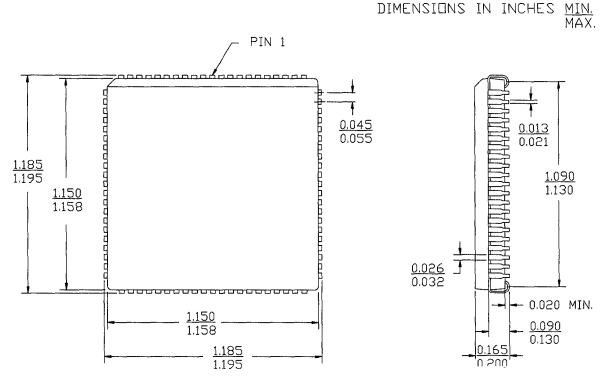
52-Lead Plastic Leaded Chip Carrier J69



68-Lead Plastic Leaded Chip Carrier J81

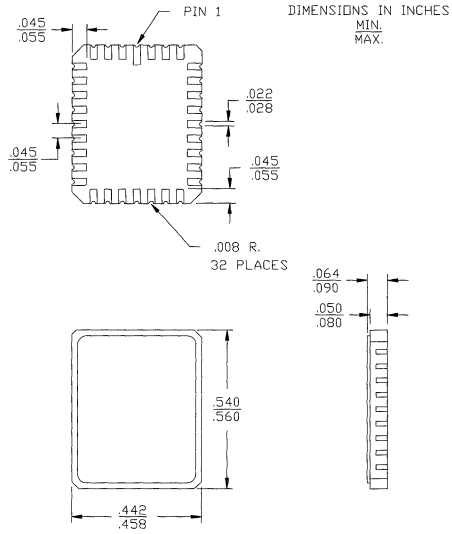


84-Lead Plastic Leaded Chip Carrier J83

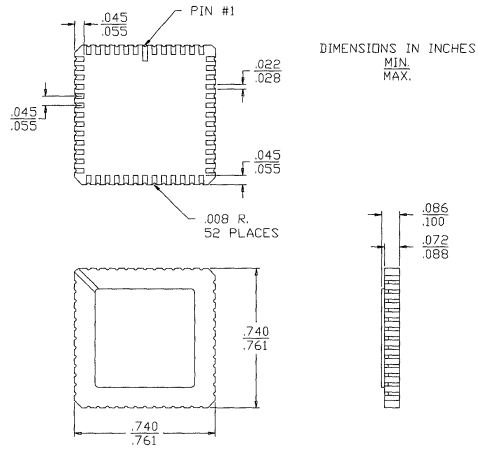


Ceramic Leadless Chip Carriers

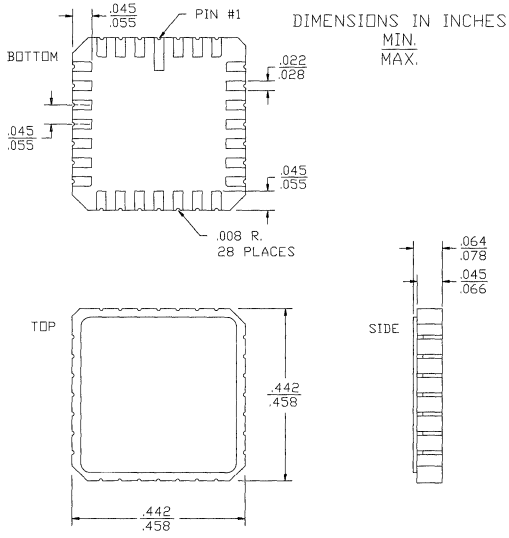
32-Pin Rectangular Leadless Chip Carrier L55
MIL–STD–1835 C–12



52-Square Leadless Chip Carrier L69

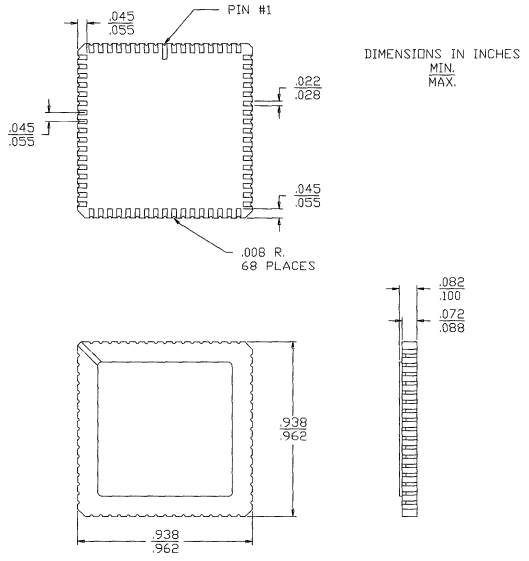


28-Square Leadless Chip Carrier L64
MIL–STD–1835 C–4



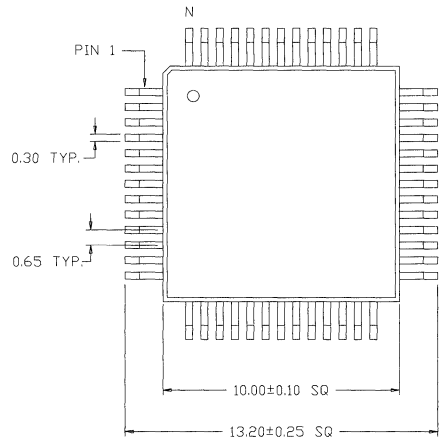
Ceramic Leadless Chip Carriers (continued)

68-Square Leadless Chip Carrier L81
MIL–STD–1835 C–7

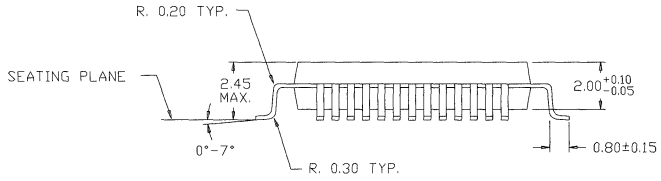


Plastic Quad Flatpacks

52-Lead Plastic Quad Flatpack N52

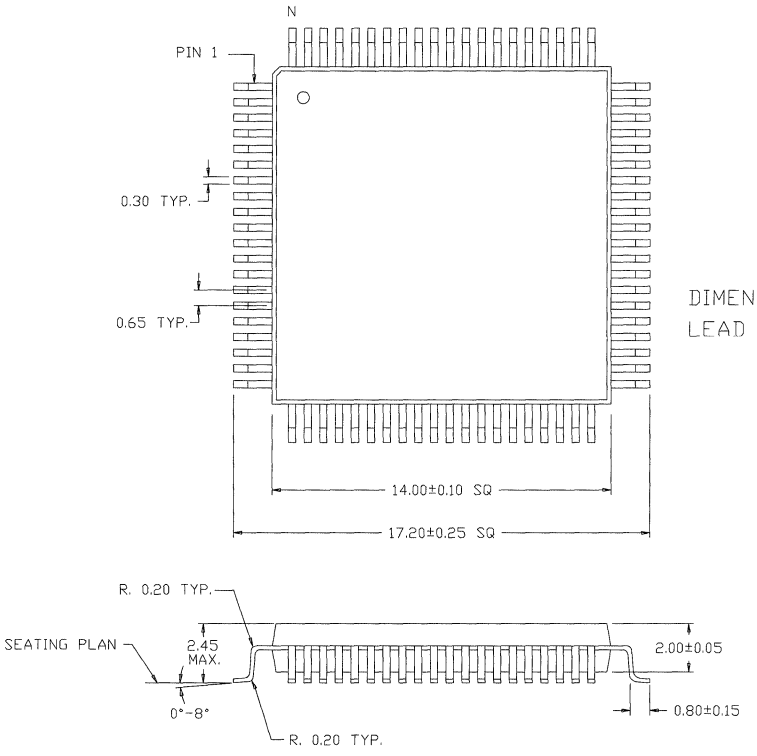


DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Plastic Quad Flatpacks (continued)

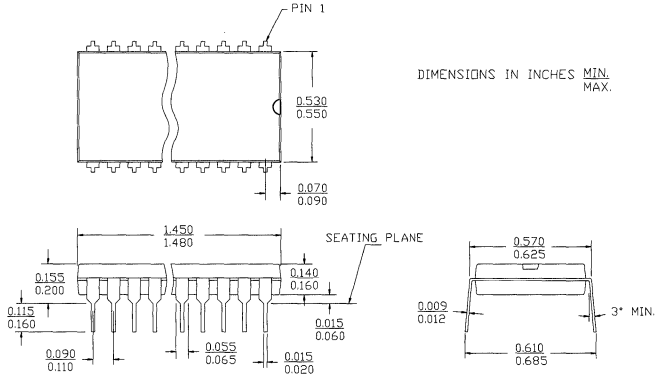
80-Lead Plastic Quad Flatpack N80



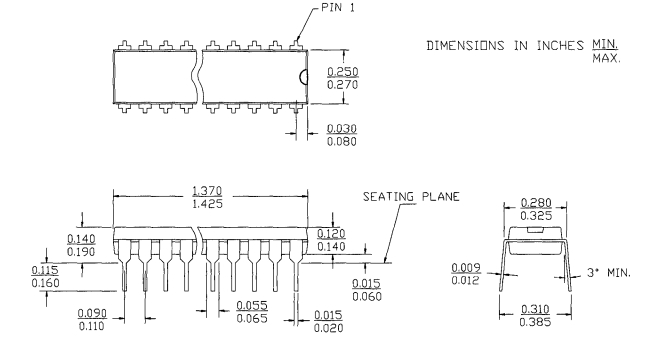
DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

Plastic Dual-In-Line Packages

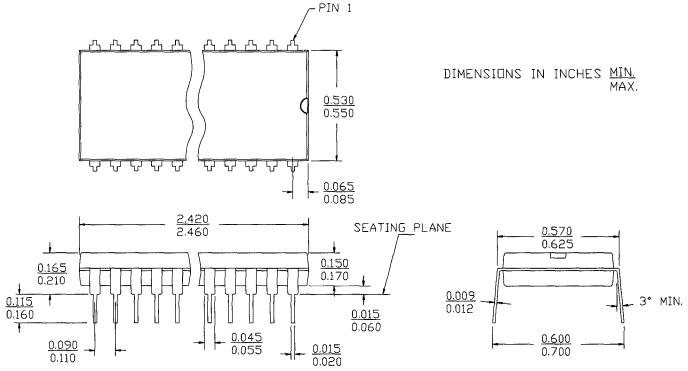
28-Lead (600-Mil) Molded DIP P15



28-Lead (300-Mil) Molded DIP P21

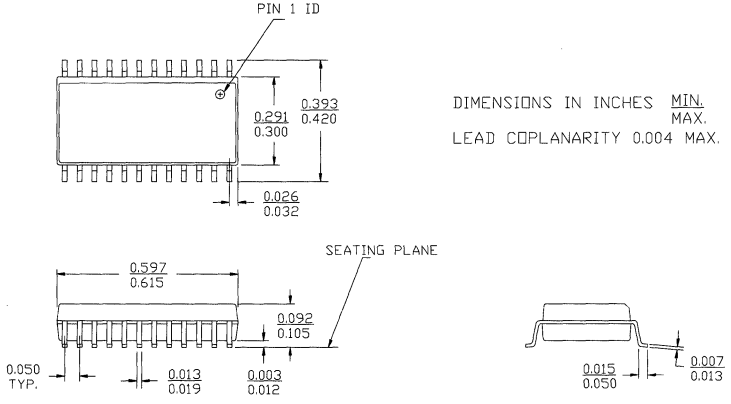


48-Lead (600-Mil) Molded DIP P25



Plastic Small Outline ICs

24-Lead (300-Mil) Molded SOIC S13

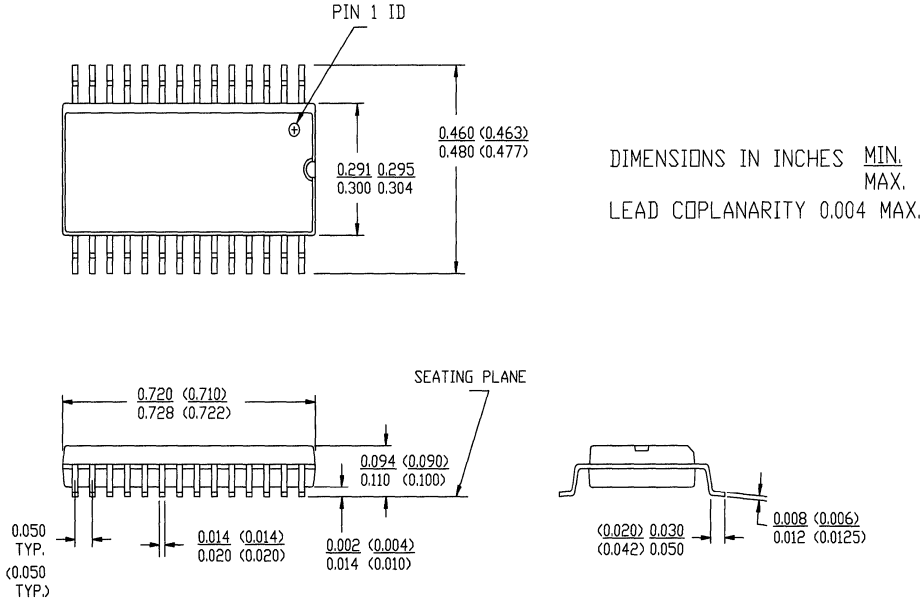


Plastic Small Outline ICs (continued)

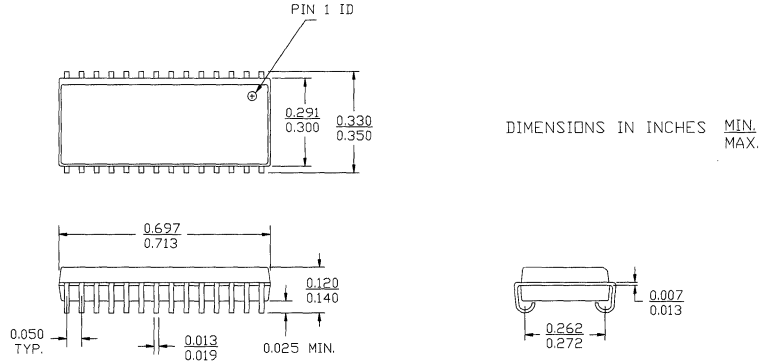
28-Lead 450-Mil (300-Mil Body Width) SOIC S22

.XXX / .XXX = HYUNDAI DIMENSIONS

(.XXX) / (.XXX) = ANAM DIMENSIONS

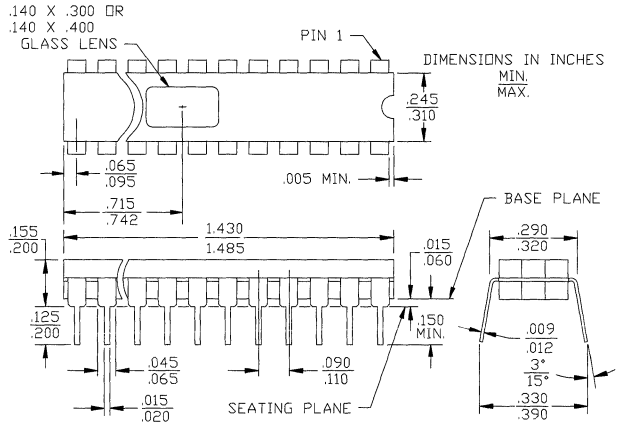


28-Lead (300-Mil) Molded SOJ V21



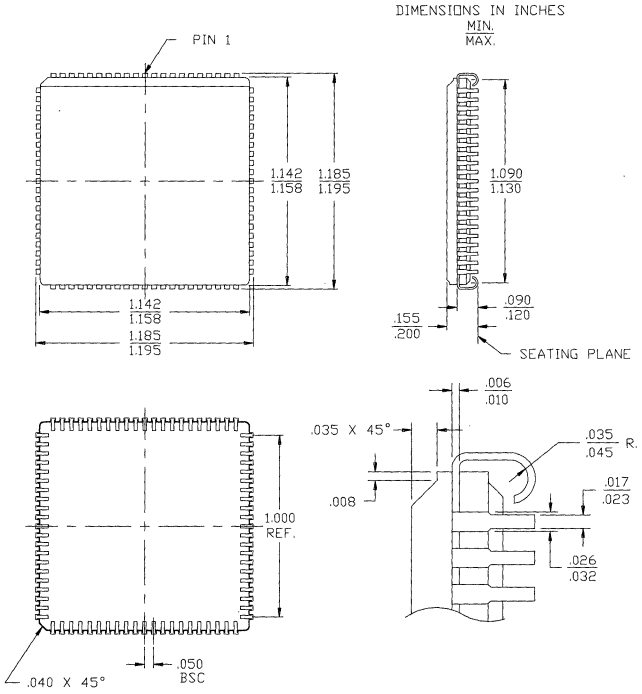
Ceramic Windowed Dual-In-Line Packages

28-Lead (300-Mil) Windowed CerDIP W22
MIL–STD–1835 D–15 Config. A



Ceramic J-Leaded Chip Carriers

84-Pin Ceramic Leaded Chip Carrier Y84



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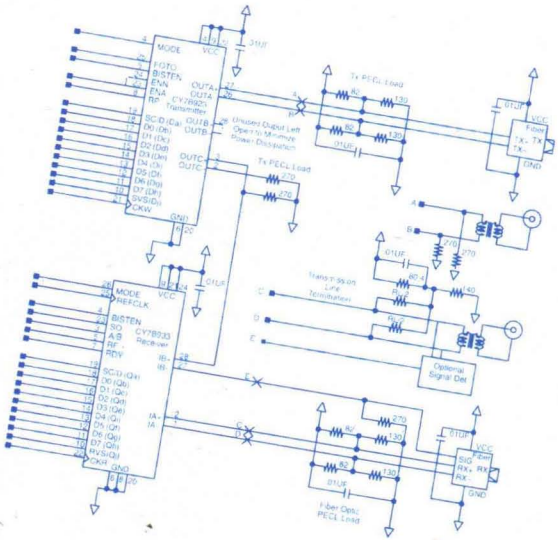

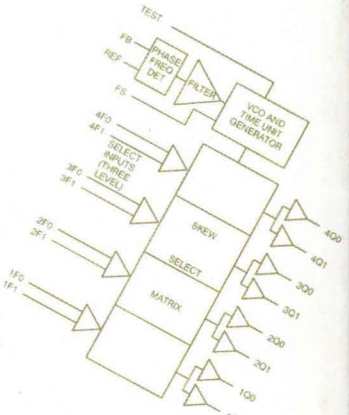

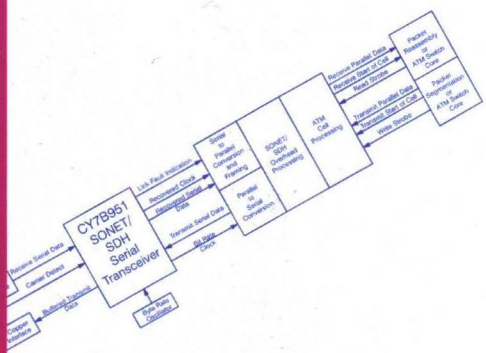

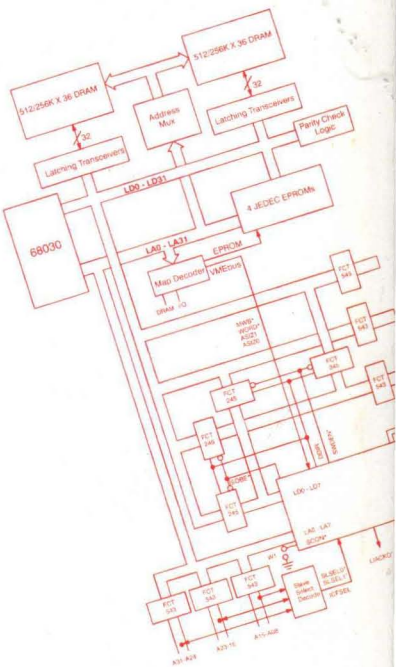

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