TEXAS INSTRUMENTS

Audio Power Amplifiers

Data Book

Data Book

Audio Power Amplifiers

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Analog and Mixed Signal

Audio Power Amplifiers Data Book

Literature Number: SLOD004

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INTRODUCTION

What you will find inside...	Texas Instruments' Audio Power Amplifier (APA) Data Book presents technical information on **over 40 differentiated APAs** from TI. This includes product previews of the soon to be released families. An entire section on application notes gives insight into how to select APAs and answers to frequently asked design questions. Following the application notes section is an overview of all TI's APA design tools. The **Plug-n-Play EVMs** and **software tools** are developed with one goal in mind: **Minimize Design Time**. The final section contains packaging specifications, including tape and reel dimensions for the **ultra-small MSOP PowerPAD™** package.
How the data book is organized...	1) Introduction and general information 2) Class-D APA Datasheets (sorted ascending by output power) 3) Class-AB APA Datasheets (sorted ascending by output power) 4) Preliminary Class-D and Class-AB Datasheets 5) Application Notes (sorted alphabetically by title) 6) Design Tools 7) Mechanical Data
New products and applications...	• TPA032D0x • TPA2000D2 • TPA01x2 • TPA02x2 • TPA02x3 • TPA0211 → Notebook PCs, Multimedia Speakers, Wireless Speakers, Hands-Free Car Kits, P.O.S. Terminals • TPA7x1 • TPA3x1 • TPA1x2 → Wireless Phones, Internet/Personal Audio, Personal FM Transceivers
Where to go for more information...	Download TI's latest datasheets and applications notes via the internet at: **http://www.ti.com/sc/docs/schome.htm** To provide full technical support, Texas Instruments has a large fully-staffed technical information center available to help you. Please turn to the last page of this data book for a complete listing of contacts ready to answer your questions.

Contents

The devices in **BOLD** type are in the Product Preview stage of development.

ALPHANUMERIC INDEX

How to Select an Audio Power Amplifier

Introduction

This section is written to help guide designers that are needing an audio power amplifier in a new or existing design. TI's large portfolio of over 35 devices provides a designer many options to choose from and helps insure a near perfect fit in their application. However, the quantity of products makes choosing the correct audio amplifier more difficult and time consuming. Knowing what devices map to which applications and the differentiating specifications that are most important help minimize the effort and time in the selection process. Table 1 maps TI's current offering of APAs to end equipment.

Table 1. End Equipment With Suggested TI APA Solution

Wireless Phones and Personal FM Transceivers		
Device	**Key Features**	**Page**
TPA701	• 700-mW mono speaker output drive • Ultra-low shutdown control maximizes battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–155
TPA711	• 700-mW mono speaker output drive • Configured to drive both speakers and headphones • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–175
TPA721	• 700-mW mono speaker output drive • Differential input for improved CMR • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–205
TPA0211†	• 2-W mono speaker output drive • Configured to drive both speakers and headphones • Tiny 8-pin MSOP PowerPAD package reduces PCB size • Upgrade to the TPA711 and TPA4861	4–3
Internet and Personal Audio		
Device	**Key Features**	**Page**
TPA102	• 150-mW output into stereo headphones • Shutdown control for maximum battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–17
TPA112	• 150-mW output into stereo headphones • Shutdown control for maximum battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–39
TPA122	• 150-mW output into stereo headphones • Shutdown control for maximum battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–63
TPA152	• Hi-Fi 75-mW stereo headphone driver • Improved depop circuitry	3–3
TPA301	• 350-mW mono speaker output drive • Low supply current and shutdown current for long battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–105
TPA311	• 350-mW mono speaker output drive • Configured to drive both speakers and headphones • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–125

† This device is in the Product Preview stage of development. Contact you local TI sales office for more information.

Internet and Personal Audio (continued)		
Device	**Key Features**	**Page**
TPA701	• 700-mW mono speaker output drive • Ultra low shutdown control maximizes battery life • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–155
TPA711	• 700-mW mono speaker output drive • Configured to drive both speakers and headphones • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–175
TPA721	• 700-mW mono speaker output drive • Tiny 8-pin MSOP PowerPAD package reduces PCB size	3–205
TPA0211†	• 2-W mono speaker output drive • Configured to drive both speakers and headphones • Tiny 8-pin MSOP PowerPAD package reduces PCB size • Upgrade to the TPA711 and TPA4861	4–3
TPA0213	• 2-W mono speaker output drive • Separate mono and stereo inputs for maximum flexibility • Optimized for battery life • Stereo headphone drive • Tiny 10-pin MSOP PowerPAD package reduces PCB size	3–597
TPA0223	• 2-W mono speaker output drive • Separate mono and stereo inputs for maximum flexibility • Optimized for fidelity • Stereo headphone drive • Tiny 10-pin MSOP PowerPAD package reduces PCB size	3–639
TPA0233	• 2-W mono speaker output drive • Mono output generated from internally mixed stereo inputs reduce external components • Optimized for battery life • Stereo headphone drive • Tiny 10-pin MSOP PowerPAD package reduces PCB size	3–671
TPA0243	• 2-W mono speaker output drive • Mono output generated from internally mixed stereo inputs reduce external components • Optimized for fidelity • Stereo headphone drive • Tiny 10-pin MSOP PowerPAD package reduces PCB size	3–703
TPA0253	• 1-W mono speaker output drive • Stereo headphone drive • Ultra low supply current and shutdown current for maximum battery life • Tiny 10-pin MSOP PowerPAD package reduces PCB size	3–271

† This device is in the Product Preview stage of development. Contact you local TI sales office for more information.

Notebook PC		
Device	**Key Features**	**Page**
TPA2000D2	• No output filter required • Efficient Class-D operation generates minimal heat and extends battery life • Industry standard 2-W stereo speaker output drive	2–3
TPA005D12	• Industry standard 2-W stereo speaker output drive • Efficient Class-D operation generates minimal heat and extends battery life	2–21
TPA005D14	• Industry standard 2-W stereo speaker output drive • Efficient Class-D operation generates minimal heat and extends battery life • Stereo headphone drive	2–27
TPA0112	• Industry standard 2-W stereo speaker output drive • Internal gain settings reduce external components • Stereo headphone drive • Optimized for battery life	3–39
TPA0122	• Industry standard 2-W stereo speaker output drive • Internal gain settings reduce external components • Stereo headphone drive • Optimized for fidelity	3–63
TPA0132	• Industry standard 2-W stereo speaker output drive • DC volume control increases flexibility and reduces external components • Stereo headphone drive • Optimized for battery life	3–413
TPA0142	• Industry standard 2-W stereo speaker output drive • DC volume control increases flexibility and reduces external components • Stereo headphone drive • Optimized for fidelity	3–441
TPA0152	• Industry standard 2-W stereo speaker output drive • Digital volume control increases flexibility and reduces external components • Stereo headphone drive • Optimized for battery life	3–3
TPA0162	• Industry standard 2-W stereo speaker output drive • Digital volume control increases flexibility and reduces external components • Stereo headphone drive • Optimized for fidelity	3–497
TPA0202	• Industry standard 2-W stereo speaker output drive • Industry's lowest THD+N provides hi-fi performance • Stereo headphone drive	3–525
TPA0102	• 1.5-W stereo speaker output drive • Stereo headphone drive	3–17
TPA0212	• Industry standard 2-W stereo speaker output drive • Internal gain settings reduce external components • Separate input MUX control pin for maximum control of the amplifier configuration (SE/BTL) • Stereo headphone drive • Optimized for battery life	3–565

† This device is in the Product Preview stage of development. Contact you local TI sales office for more information.

Notebook PC (continued)		
Device	**Key Features**	**Page**
TPA0222	• Industry standard 2-W stereo speaker output drive • Internal gain settings reduce external components • Separate input MUX control pin for maximum control of the amplifier configuration (SE/BTL) • Stereo headphone drive • Optimized for fidelity	3–607
TPA0232	• Industry standard 2-W stereo speaker output drive • DC volume control increases flexibility and reduces external components • Separate input MUX control pin for maximum control of the amplifier configuration (SE/BTL) • Stereo headphone drive • Optimized for battery life	3–643
TPA0242	• Industry standard 2-W stereo speaker output drive • DC volume control increases flexibility and reduces external components • Separate input MUX control pin for maximum control of the amplifier configuration (SE/BTL) • Stereo headphone drive • Optimized for fidelity	3–675
TPA0213	• Industry standard 2-W mono speaker output drive • Separate mono and stereo inputs for maximum flexibility • PC 99 Compatible (Portable) • Optimized for battery life • Stereo headphone drive	3–597
TPA0223	• Industry standard 2-W mono speaker output drive • Separate mono and stereo inputs for maximum flexibility • PC 99 Compatible (Desktop) • Optimized for fidelity • Stereo headphone drive	3–639
TPA0233	• Industry standard 2-W mono speaker output drive • Mono output generated from internally mixed stereo inputs to reduce external components • PC 99 Compatible (Portable) • Optimized for battery life • Stereo headphone drive	3–671
TPA0243	• Industry standard 2-W mono speaker output drive • Mono output generated from internally mixed stereo inputs to reduce external components • PC 99 Compatible (Desktop) • Optimized for fidelity • Stereo headphone drive	3–703

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Multimedia and Wireless Speakers		
Device	**Key Features**	**Page**
TPA2000D2	• No output filter required • Efficient Class-D operation generates minimal heat and extends battery life • Industry standard 2-W stereo speaker output drive	2–3
TPA005D12	• 2-W stereo output drive for satellite speakers • Efficient Class-D operation generates minimal heat and extends battery life	2–21
TPA005D14	• 2-W stereo output drive for satellite speakers • Efficient Class-D operation generates minimal heat and extends battery life • Stereo headphone drive	2–27
TPA032D01	• 10-W mono output drive for sub-woofer or satellite speakers • Efficient Class-D operation generates minimal heat eliminating bulky heat sinks	2–79
TPA032D02	• 10-W stereo output drive for sub-woofer or satellite speakers • Efficient Class-D operation generates minimal heat eliminating bulky heat sinks	2–99
TPA032D03	• 10-W stereo output drive for sub-woofer or satellite speakers • Efficient Class-D operation generates minimal heat eliminating bulky heat sinks • Stereo headphone drive	2–121
TPA032D04	• 10-W stereo output drive for sub-woofer or satellite speakers • Efficient Class-D operation generates minimal heat eliminating bulky heat sinks • Stereo headphone drive	2–143

Determining Output Power When Driving Headphones (Single Ended) vs. Speakers (Bridged)

The configuration of the amplifier dramatically affects how much power can be delivered to the speaker. Single ended (SE) configuration is most common in headphone or applications when the speakers use a common ground. It is referred to as single ended because only one terminal of the speaker is connected to the amplifier. The other terminal is tied to ground, see Figure 1. This technique requires only three conductors between the amplifier and speaker for a stereo solution, left positive, right positive and the third for ground. In terms of power provided to the load, the equation is straight forward, just remember to convert the supply voltage to an RMS value by dividing the peak to peak voltage by $2 \times (2)^{1/2}$ or 2.83. Once V_{RMS} is determined plug the value into Equation 1 to find the power delivered to the speaker:

$$P = \frac{\left(V_{RMS}\right)^2}{R_{LOAD}} \quad (1)$$

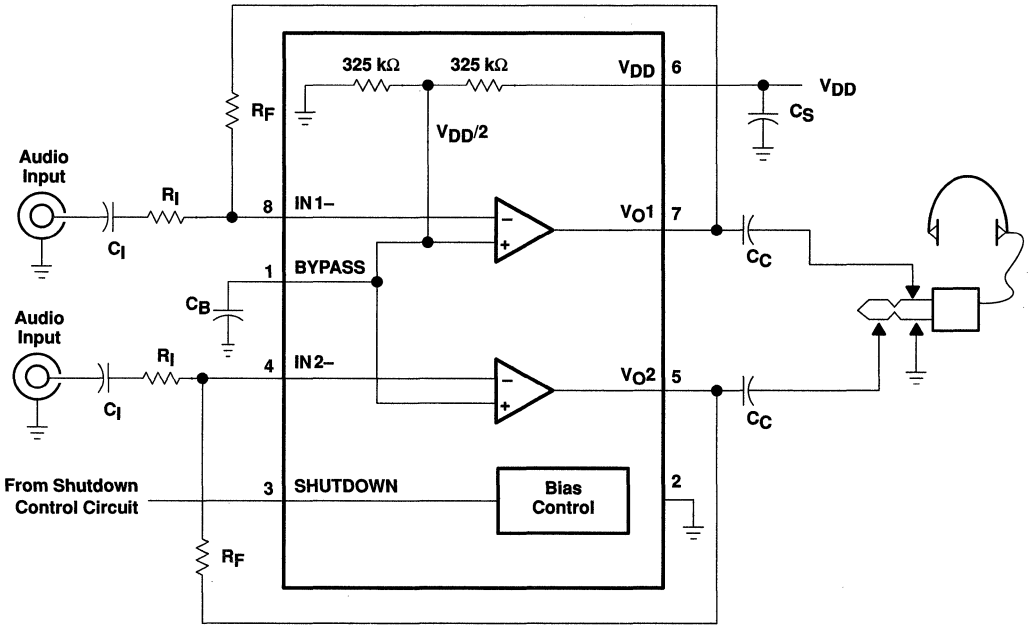

Figure 1. TPA102 Audio Power Amplifier in SE Configuration

A bridge-tied load (BTL) configuration consists of two amplifiers driving both ends of the load, see Figure 2. There are several potential benefits with this configuration. The first benefit is the elimination of the coupling capacitor requirement in the SE configuration used to block the DC offset from reaching the load. These capacitors can be quite large (40 – 1000 uF), are expensive and have the additional drawback of limiting low frequency performance. The BTL configuration cancels the DC offsets which eliminates the need for the blocking caps. Low frequency performance is then limited only by the input network, amplifier and speaker frequency response. The other major advantage is the differential drive to the speaker. The differential drive means that as one side is slewing up the other side is slewing down and vice versa. This effectively doubles the available voltage swing on the load. Doubling the voltage swing across the speaker quadruples the power delivered to the speakers.

BTL configurations are typically used in applications when the speaker and amplifier are contained in the same enclosure. For example, the circuit in Figure 2 is useful in wireless applications where only a mono speaker is required. The APA is capable of driving 700 mW to an 8-ohm speaker from a 5-V supply.

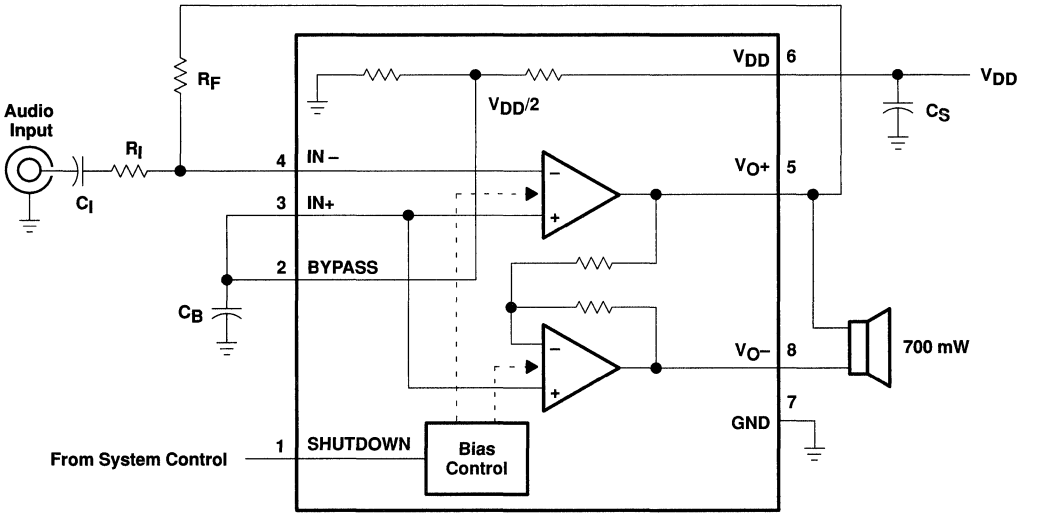

Figure 2. TPA701 Audio Power Amplifier in BTL Configuration

Determining the correct supply voltage to avoid clipping

The output voltage swing is key when determining the peak power capability of an amplifier. Figure 3 and Figure 4 show the theoretical output power from a 5-V supply into a 4-ohm load is 781 mW (SE) and 3.12 W (BTL) respectively. However, to avoid clipping the APA output voltage should not swing rail-to-rail. A few tenths to a volt of headroom from the top supply rail significantly decreases distortion (clipping).

For example, an amplifier with a 5-V single supply, driving a 4-ohm speaker has a typical peak to peak output swing around 4.5 V. This translates into 1.59 V_{RMS} If the speakers are 4 ohms and the supply voltage is 5 V the maximum output power from a SE and BTL configuration is:

$$P_{SE} = \frac{\left(\frac{4.5\ V}{2.83\ V}\right)^2}{4\Omega} \qquad P_{BTL} = \frac{\left(\frac{9\ V}{2.83\ V}\right)^2}{4\Omega}$$

$$P_{SE} = 0.63\ W \qquad P_{BTL} = 2.53\ W$$

A result from this analysis is lower speaker impedance yields higher output power. However, speakers with lower impedance are typically less efficient, especially speakers with an impedance below 4 ohms. Moreover, the APA's efficiency decreases as the speaker's impedance drops below 4 ohms. The degradation in the speaker's and APA's efficiency below 4 ohms negates the increase in output power.

Beyond lowering the speaker impedance to 4 ohms, the best way to increase the output power in a given SE or BTL configuration is by increasing the supply voltage. Figure 3 and Figure 4 are plots of the maximum theoretical output power vs supply voltage for SE and BTL amplifier configurations driving 4-, 8- and 32-ohm speakers.

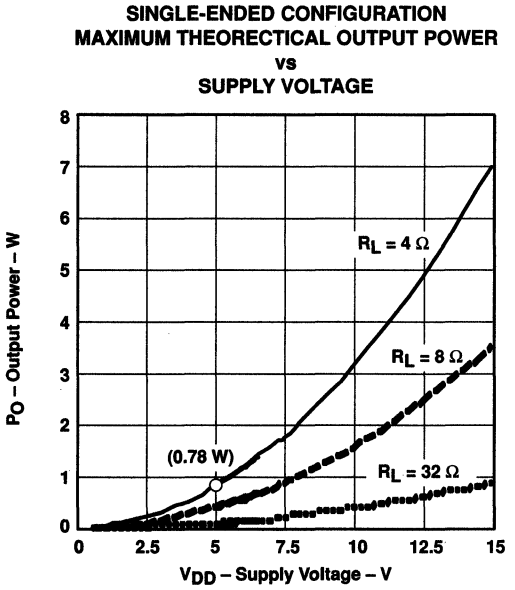

Figure 3. Maximum Theoretical Output Power vs Supply Voltage for a SE Audio Power Amplifier

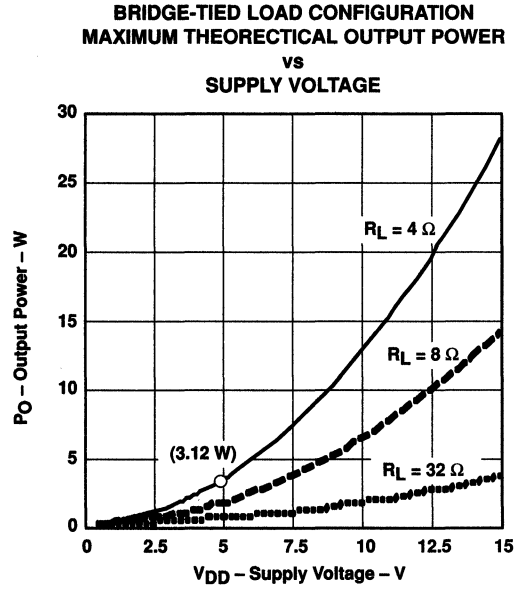

Figure 4. Maximum Theoretical Output Power vs Supply Voltage for a BTL Audio Power Amplifier

Conclusion

Knowing the maximum output power a given APA can deliver from a fixed supply voltage will save considerable time and effort when selecting a device. An APA with a BTL configuration will drive four times more power to the speaker than an APA in a SE configuration. Once the amplifier output configuration is selected there are basically two variables that limit the output power being supplied to the speaker; the APA's supply voltage and the speaker's impedance. Lowering the impedance of the speaker will increase the APA's output power, but the loss in speaker efficiency tends to offset the increase in output power. This means the only way to effectively increase the output power from a speaker is to increase the supply voltage to the amplifier.

AUDIO POWER AMPLIFIER CROSS REFERENCE

Part No.	Suggested TI Replacement	Vendor	Replacement Type	Page No.
LX1720	TPA2000D2	LinFinity	Similar functionality (see Note 4)	2–3
LX1720	TPA032D02	LinFinity	Similar functionality (see Note 4)	2–97
MS6308	TPA102	MOSA	Same functionality (see Note 3)	3–17
MS6308	TPA112	MOSA	Same functionality and pinout (see Note 2)	3–39
MS6308	TPA122	MOSA	Same functionality (see Note 3)	3–63
MS6308	TPA152	MOSA	Same functionality (see Note 3)	3–3
SSM2211	TPA4861	Analog Devices	Same functionality (see Note 3)	3–249
SSM2211	TPA701	Analog Devices	Same functionality (see Note 3)	3–155
SSM2211	TPA0211†	Analog Devices	Similar functionality (see Note 4)	4–3
SSM2250	TPA0213	Analog Devices	Similar functionality (see Note 4)	3–597
SSM2250	TPA0223	Analog Devices	Similar functionality (see Note 4)	3–639
SSM2250	TPA0233	Analog Devices	Similar functionality (see Note 4)	3–671
SSM2250	TPA0243	Analog Devices	Similar functionality (see Note 4)	3–703
MC34119	TPA301	Motorola	Same functionality (see Note 3)	3–105
MC34119	TPA701	Motorola	Similar functionality (see Note 4)	3–155
TDA8542	TPA0102	Philips	Similar functionality (see Note 4)	3–313
TDA8542	TPA0202	Philips	Similar functionality (see Note 4)	3–525
TDA8542	TPA0112	Philips	Similar functionality (see Note 4)	3–349
TDA8542	TPA0122	Philips	Similar functionality (see Note 4)	3–381
TDA8542	TPA0212	Philips	Similar functionality (see Note 4)	3–565
TDA8542	TPA0222	Philips	Similar functionality (see Note 4)	3–607
TDA7053A	TPA0132	Philips	Similar functionality (see Note 4)	3–413
TDA7053A	TPA0142	Philips	Similar functionality (see Note 4)	3–441
TDA7053A	TPA0232	Philips	Similar functionality (see Note 4)	3–643
TDA7053A	TPA0242	Philips	Similar functionality (see Note 4)	3–675
TDA1308	TPA152	Philips	Same functionality (see Note 3)	3–3
TDA1308	TPA102	Philips	Same functionality (see Note 3)	3–17
TDA1308	TPA112	Philips	Same functionality (see Note 3)	3–39
TDA1308	TPA122	Philips	Same functionality (see Note 3)	3–63

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2. The device has the Same functionality and pinout as the competitors device, but is NOT and exact equivalent
3. The device has the Same functionality as the competitors device, but is not pin–for–pin and/or parametrically equivalent.
4. The device has Similar functionality, but is not functionally equivalent to the competitors device.

Part No.	Suggested TI Replacement	Vendor	Replacement Type	Page No.
TDA8559	TPA152	Philips	Same functionality (see Note 3)	3–3
TDA8559	TPA102	Philips	Same functionality (see Note 3)	3–17
TDA8559	TPA112	Philips	Same functionality (see Note 3)	3–39
TDA8559	TPA122	Philips	Same functionality (see Note 3)	3–63
TDA1517	TPA1517	Philips	Same functionality (see Note 3)	3–707
TDA7052	TPA4861	Philips	Same functionality (see Note 3)	3–249
TDA7052	TPA0211†	Philips	Same functionality (see Note 3)	4–3
TDA7052A	TPA0132	Philips	Similar functionality (see Note 4)	3–413
TDA7052A	TPA0142	Philips	Similar functionality (see Note 4)	3–441
TDA7052A	TPA0232	Philips	Similar functionality (see Note 4)	3–643
TDA7052A	TPA0242	Philips	Similar functionality (see Note 4)	3–675
TDA8552	TPA0152	Philips	Similar functionality (see Note 4)	3–469
TDA8552	TPA0162	Philips	Similar functionality (see Note 4)	3–497
TDA8551	TPA0152	Philips	Similar functionality (see Note 4)	3–469
TDA8551	TPA0162	Philips	Similar functionality (see Note 4)	3–497
LM4663	TPA2000D2	National Semiconductor	Similar functionality (see Note 4)	2–3
LM4663	TPA005D14	National Semiconductor	Similar functionality (see Note 4)	2–25
LM4862	TPA701	National Semiconductor	Same functionality (see Note 3)	3–155
LM4862	TPA711	National Semiconductor	Similar functionality (see Note 4)	3–175
LM4862	TPA721	National Semiconductor	Similar functionality (see Note 4)	3–205
LM4862	TPA301	National Semiconductor	Similar functionality (see Note 4)	3–105
LM4862	TPA311	National Semiconductor	Similar functionality (see Note 4)	3–125
LM4835	TPA0132	National Semiconductor	Similar functionality (see Note 4)	3–413
LM4835	TPA0142	National Semiconductor	Similar functionality (see Note 4)	3–441
LM4835	TPA0232	National Semiconductor	Similar functionality (see Note 4)	3–643
LM4835	TPA0242	National Semiconductor	Similar functionality (see Note 4)	3–675
LM4835	TPA0112	National Semiconductor	Similar functionality (see Note 4)	3–349
LM4835	TPA0122	National Semiconductor	Similar functionality (see Note 4)	3–381
LM4835	TPA0212	National Semiconductor	Similar functionality (see Note 4)	3–565

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Part No.	Suggested TI Replacement	Vendor	Replacement Type	Page No.
LM4835	TPA0222	National Semiconductor	Similar functionality (see Note 4)	3–607
LM386	TPA301	National Semiconductor	Similar functionality (see Note 4)	3–105
LM4865	TPA711	National Semiconductor	Similar functionality (see Note 4)	3–175
LM4865	TPA0132	National Semiconductor	Similar functionality (see Note 4)	3–413
LM4865	TPA0142	National Semiconductor	Similar functionality (see Note 4)	3–441
LM4865	TPA0232	National Semiconductor	Similar functionality (see Note 4)	3–643
LM4865	TPA0242	National Semiconductor	Similar functionality (see Note 4)	3–675
LM4752	TPA032D02	National Semiconductor	Similar functionality (see Note 4)	2–97
LM4880	TPA122	National Semiconductor	Same functionality and pinout (see Note 2)	3–63
LM4880	TPA102	National Semiconductor	Same functionality (see Note 3)	3–17
LM4880	TPA112	National Semiconductor	Same functionality (see Note 3)	3–39
LM4881	TPA102	National Semiconductor	Same functionality and pinout (see Note 2)	3–17
LM4881	TPA112	National Semiconductor	Same functionality (see Note 3)	3–39
LM4881	TPA122	National Semiconductor	Same functionality and pinout (see Note 2)	3–63
LM4882	TPA311	National Semiconductor	Similar functionality (see Note 4)	3–125
LM4882	TPA301	National Semiconductor	Similar functionality (see Note 4)	3–105
LM4871	TPA4861	National Semiconductor	Same functionality and pinout (see Note 2)	3–249
LM4871	TPA701	National Semiconductor	Same functionality and pinout (see Note 2)	3–155
LM4871	TPA0211†	National Semiconductor	Similar functionality (see Note 4)	4–3
LM4864	TPA301	National Semiconductor	Same functionality and pinout (see Note 2)	3–105
LM4864	TPA311	National Semiconductor	Similar functionality (see Note 4)	3–125
LM4873	TPA0102	National Semiconductor	Same functionality (see Note 3)	3–313
LM4873	TPA0202	National Semiconductor	Same functionality (see Note 3)	3–525
LM4873	TPA0112	National Semiconductor	Similar functionality (see Note 4)	3–349
LM4873	TPA0122	National Semiconductor	Similar functionality (see Note 4)	3–381
LM4873	TPA0212	National Semiconductor	Similar functionality (see Note 4)	3–565
LM4873	TPA0222	National Semiconductor	Similar functionality (see Note 4)	3–607
LM4863	TPA0102	National Semiconductor	Similar functionality (see Note 4)	3–313
LM4863	TPA0202	National Semiconductor	Similar functionality (see Note 4)	3–525

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Part No.	Suggested TI Replacement	Vendor	Replacement Type	Page No.
LM4863	TPA0112	National Semiconductor	Similar functionality (see Note 4)	3–349
LM4863	TPA0122	National Semiconductor	Similar functionality (see Note 4)	3–381
LM4863	TPA0212	National Semiconductor	Similar functionality (see Note 4)	3–565
LM4863	TPA0222	National Semiconductor	Similar functionality (see Note 4)	3–607
LM4861	TPA4861	National Semiconductor	Same functionality and pinout (see Note 2)	3–249
LM4861	TPA0211†	National Semiconductor	Similar functionality (see Note 4)	4–3
LM4860	TPA4860	National Semiconductor	Same functionality and pinout (see Note 2)	3–225
LM4834	TPA0132	National Semiconductor	Similar functionality (see Note 4)	3–413
LM4834	TPA0142	National Semiconductor	Similar functionality (see Note 4)	3–441
LM4834	TPA0232	National Semiconductor	Similar functionality (see Note 4)	3–643
LM4834	TPA0242	National Semiconductor	Similar functionality (see Note 4)	3–675

† This device is in the Product Preview stage of development. Contact your local TI sales office for more information.

NOTES: 1. The device is an EXACT EQUIVALENT in functionality and parametrics to the competitors device.
2. The device has the Same functionality and pinout as the competitors device, but is NOT and exact equivalent
3. The device has the Same functionality as the competitors device, but is not pin–for–pin and/or parametrically equivalent.
4. The device has Similar functionality, but is not functionally equivalent to the competitors device.

Single-Ended Load Configuration

A configuration where one end of the load is connected to the audio power amplifier and the other end of the load is connected to ground. Used primary for headphone applications or where the audio power amplifier and speaker reside in different enclosures.

Bridged-Tied Load Configuration

A configuration where both ends of the load are connected to audio power amplifiers. This configuration effectively quadruples the output power capability of the system. Used primary in applications that are space constrained and where the audio power amplifier and speaker reside in the same enclosure.

PWM (Pulse Width Modulation)

Pulse-time modulation in which the value of each instantaneous sample of the modulating wave is caused to modulate the duration of a pulse. The modulation frequency may be fixed or variable. PWM is used in Class-D audio power amplifiers to achieve very high efficiency operation.

Class-A Amplifiers

Class-A, based on one output element, a vacuum tube, which was eventually replaced by a transistor. Class-A amplifiers add little distortion to the sound they amplify, But, they consume a great deal of power. In many applications, this would require systems with very large power supplies. As a result, the effective use of Class-A amplifiers in portable applications is severely limited.

Class-B Amplifiers

Class-B addressed the problem of power consumption. This type of APA features two elements or transistors in the output stage, both of which are shut off when no signal is present. Unfortunately, this arrangement introduces significant distortion into the signal as it moves through the zero crossover point.

Class-AB Amplifiers

Class-AB amplifiers removed the distortion by keeping each of the two transistors slightly on at all times. While this improves THD+N it also re-introduces the problem of power consumption. Class-AB amplifiers are ideal solutions in applications requiring moderate to high levels of fidelity and supply current.

Class-D Amplifiers

Class-D amplifiers process analog signals using PWM techniques, which is the key behind Class-D amplifiers' increased efficiency. The PWM signals are applied to power DMOS H-bridges, which provide high output current capability. High-frequency square waves of constant amplitude, but varying width, are output from the IC. These pulses of varying widths contain the audio information.

Total Harmonic Distortion + Noise (THD+N)

The root some square of all harmonic distortion components including their aliases plus any noise in the system. Commonly measured as a percentage of the fundamental signal. Harmonic distortion is distortion at frequencies that are whole number multiples of the test tone frequency. Values below 0.5% to 0.3% are negligible to the untrained ear.

Power Supply Rejection Ratio (PSRR)

The log of the ratio of a change in supply voltage to the change in output power multiplied by 20. The result is given in dB and measured at DC voltages. For example, the output of an audio power amplifier that has a PSRR equal to 70 dB would change by 31.6 mV if the supply voltage changed by 0.1 V. PSRR = $20 \times \log(V_{supply}/V_{out})$ dB.

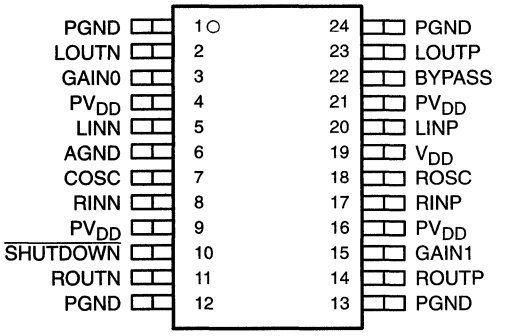
Crest Factor

The log of the ratio of peak output power to RMS output power multiplied by 10, typically given in decibels (dB). This is commonly referred to as dynamic range. As the crest factor increases the difference between the peaks and the normal loudness increases. Crest Factor = $10 \times \text{Log}(P_{PEAK}/P_{RMS})$

Contents

- **Modulation Scheme Optimized to Operate Without a Filter**
- **2 W Into 3-Ω Speakers (THD+N< 0.4%)**
- **< 0.08% THD+N at 1 W, 1 kHz, Into 4-Ω Load**
- **Extremely Efficient 3rd Generation 5-V Class-D Technology:**
  - **Low Supply Current (No Filter) . . . 8 mA**
  - **Low Supply Current (Filter) . . . 15 mA**
  - **Low Shutdown Current . . . 1 μA**
  - **Low Noise Floor . . . 56 μV_{RMS}**
  - **Maximum Efficiency into 3 Ω, 65 – 70%**
  - **Maximum Efficiency into 8 Ω, 75 – 85%**
  - **4 Internal Gain Settings . . . 8 – 23.5 dB**
  - **PSRR . . . –77 dB**
- **Integrated Depop Circuitry**
- **Short-Circuit Protection (Short to Battery, Ground, and Load)**
- **–40°C to 85°C Operating Temperature Range**

PWP PACKAGE
(TOP VIEW)



description

The TPA2000D2 is the third generation 5-V class-D amplifier from Texas Instruments. Improvements to previous generation devices include: lower supply current, lower noise floor, better efficiency, four different gain settings, smaller packaging, and fewer external components. The most significant advancement with this device is its modulation scheme that allows the amplifier to operate without the output filter. Eliminating the output filter saves the user approximately 30% in system cost and 75% in PCB area.

The TPA2000D2 is a monolithic class-D power IC stereo audio amplifier, using the high switching speed of power MOSFET transistors. These transistors reproduce the analog signal through high-frequency switching of the output stage. The TPA2000D2 is configured as a bridge-tied load (BTL) amplifier capable of delivering greater than 2 W of continuous average power into a 3-Ω load at less than 1% THD+N from a 5-V power supply in the high fidelity range (20 Hz to 20 kHz). With 1 W being delivered to a 4-Ω load at 1 kHz, the typical THD+N is less than 0.08%.

A BTL configuration eliminates the need for external coupling capacitors on the output. Low supply current of 8 mA makes the device ideal for battery-powered applications. Protection circuitry increases device reliability: thermal, over-current, and under-voltage shutdown.

Efficient class-D modulation enables the TPA2000D2 to operate at full power into 3-Ω loads at an ambient temperature of 85°C.

AVAILABLE OPTIONS

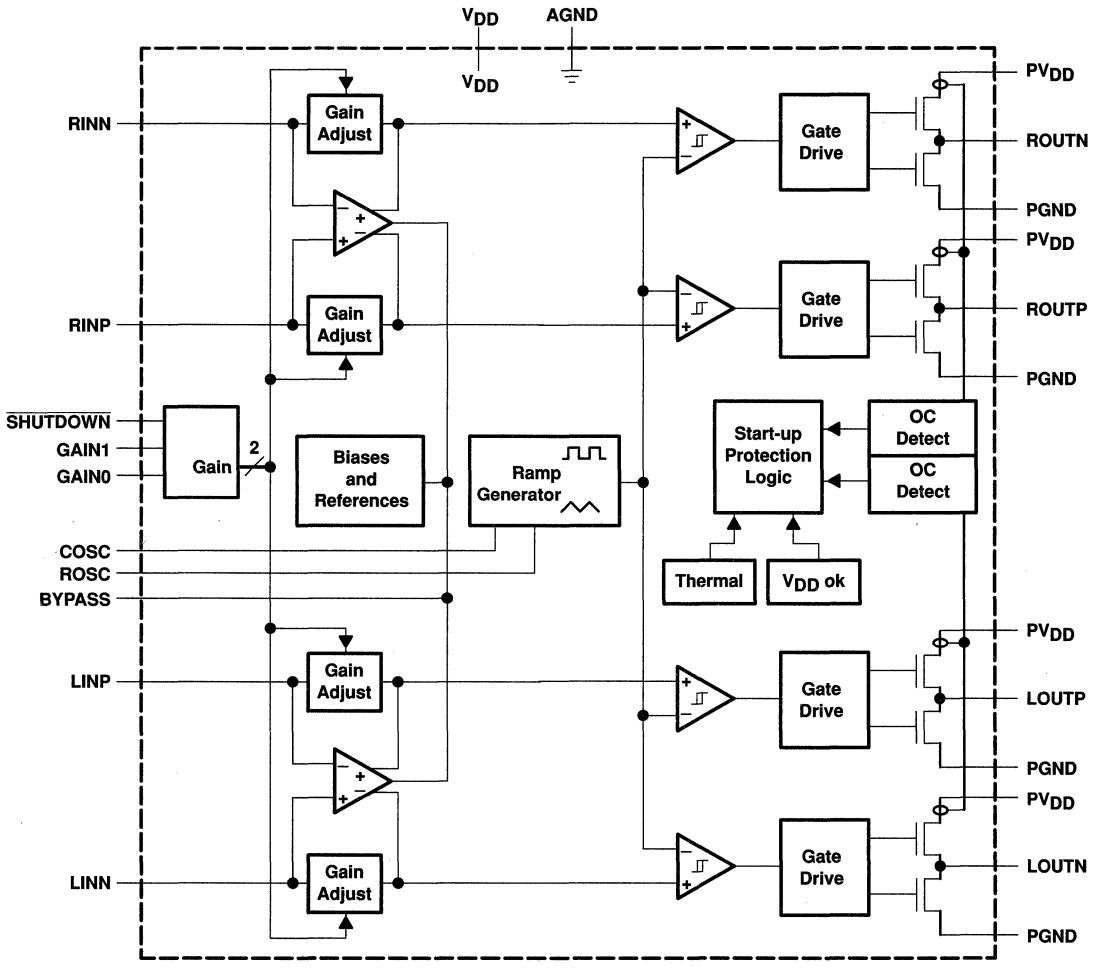
T_A	PACKAGED DEVICE
	TSSOP (PWP)
–40°C to 85°C	TPA2000D2PWP

NOTE: The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2000D2PWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Function

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	6	–	Analog ground
BYPASS	22	I	Tap to voltage divider for internal midsupply bias generator used for analog reference.
COSC	7	I	A capacitor connected to this terminal sets the oscillation frequency in conjunction with ROSC. For proper operation, connect a 220 pF capacitor from COSC to ground.
GAIN0	3	I	Bit 0 of gain control (TTL logic level)
GAIN1	15	I	Bit 1 of gain control (TTL logic level)
LINN	5	I	Left channel negative differential audio input
LINP	20	I	Left channel positive differential audio input
LOUTN	2	O	Left channel negative audio output
LOUTP	23	O	Left channel positive audio output
PGND	1, 24	–	Power ground for left channel H-bridge
	12, 13	–	Power ground for right channel H-bridge
PV_{DD}	4, 21	–	Power supply for left channel H-bridge
	9, 16	–	Power supply for right channel H-bridge
RINN	8	I	Right channel negative differential audio input
RINP	17	I	Right channel positive differential audio input
ROSC	18	I	A resistor connected to this terminal sets the oscillation frequency in conjunction with COSC. For proper operation, connect a 120 kΩ resistor from ROSC to ground.
ROUTN	11	O	Right channel negative audio output
ROUTP	14	O	Right channel positive output
$\overline{\text{SHUTDOWN}}$	10	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal; normal operation if a TTL logic high is placed on this terminal.
V_{DD}	19	–	Analog power supply

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD}, PV_{DD} ..... –0.3 V to 6 V
Input voltage, V_I ..... –0.3 V to V_{DD}+0.3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PWP	2.7 W	21.8 mW/°C	1.7 W	1.4 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{SHUTDOWN}$	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{SHUTDOWN}$		0.8	V
Operating free-air temperature, T_A		–40	85	°C
PWM Frequency		200	300	kHz

electrical characteristics, T_A = 25°C, V_{DD} = PV_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V			10	mV
PSRR	Power supply rejection ratio	V_{DD}=PV_{DD} = 4.5 V to 5.5 V		–77		dB
I_{IH}	High-level input current	V_{DD}=PV_{DD} = 5.5 V, V_I = V_{DD} = PV_{DD}			1	μA
I_{IL}	Low-level input current	V_{DD}=PV_{DD} = 5.5 V, V_I = 0 V	–1			μA
I_{DD}	Supply current	No filter (with or without speaker load)		8	10	mA
I_{DD}	Supply current	With filter ,L = 22 μH, C = 1 μF		15		mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, T_A = 25°C, V_{DD} = PV_{DD} = 5 V, R_L = 4 Ω, Gain = –2 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.1%, f = 1 kHz, R_L = 3 Ω		2		W
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 20 kHz		<0.5%		
B_{OM}	Maximum output power bandwidth	THD = 5%		20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYPASS)}$ = 0.4 μF		–60		dB
SNR	Signal-to-noise ratio			87		dBV
	Integrated noise floor	20 Hz to 20 kHz, No input		56		μV
Z_I	Input impedance			>20		kΩ

Table 1. Gain Settings

GAIN0	GAIN1	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	8	104
0	1	12	74
1	0	17.5	44
1	1	23.5	24

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output power	2, 3
	In-band output spectrum	vs Frequency	4
THD+N	Total harmonic distortion plus noise	vs Output power	5 – 7
		vs Frequency	8, 9

test set-up for graphs

The THD+N measurements shown do not use an LC output filter, but use a low pass filter with a cut-off frequency of 20 kHz so the switching frequency does not dominate the measurement. This is done to ensure that the THD+N measured is just the audible THD+N. The THD+N measurements are shown at the highest gain for worst case.

The LC output filter used in the efficiency curves (Figure 2 and 3) is shown in Figure 1.

L1 = L2 = 22 μH (DCR = 110 mΩ,
Part Number = SCD0703T–220 M–S,
Manufacturer = GCI)
C1 = C2 = 1 μF

The ferrite filter used in the efficiency curves (Figure 2 and 3) is shown in Figure 1, where L is a ferrite bead.

L1 = L2 = ferrite bead (part number = 2512067007Y3, manufacturer = Fair-Rite)
C1 = C2 = 1 nF

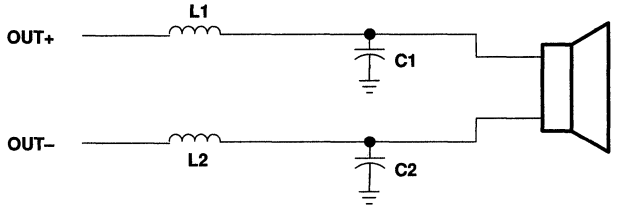


Figure 1. Class-D Output Filter

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
OUTPUT POWER

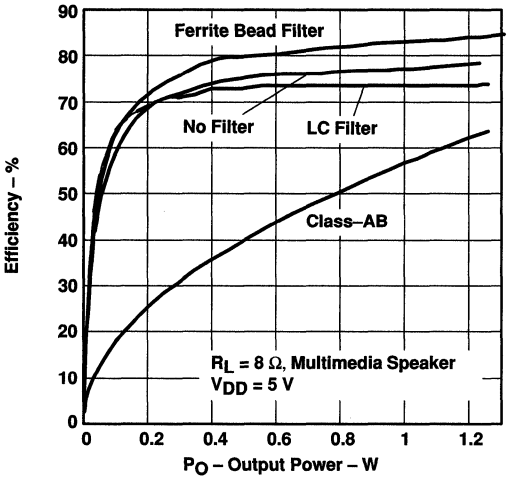


Figure 2

EFFICIENCY
vs
OUTPUT POWER

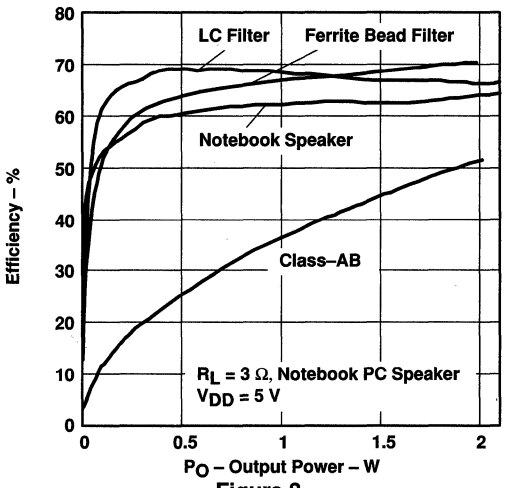


Figure 3

IN-BAND OUTPUT SPECTRUM

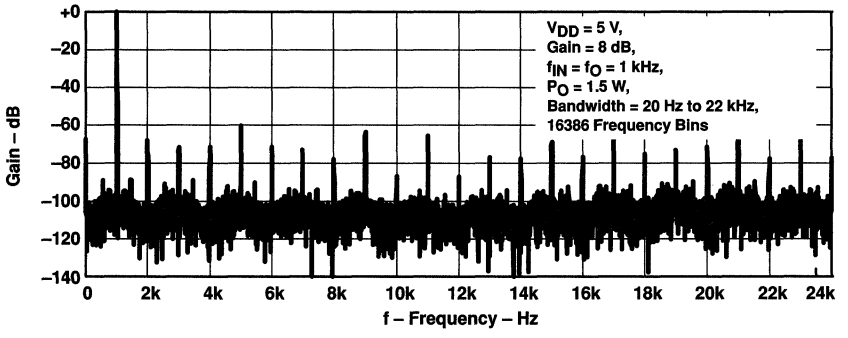


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

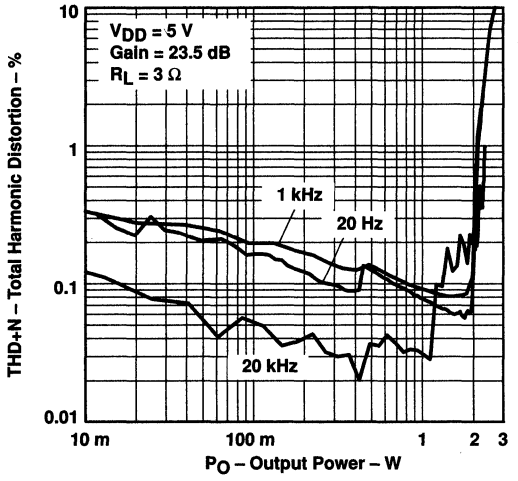


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

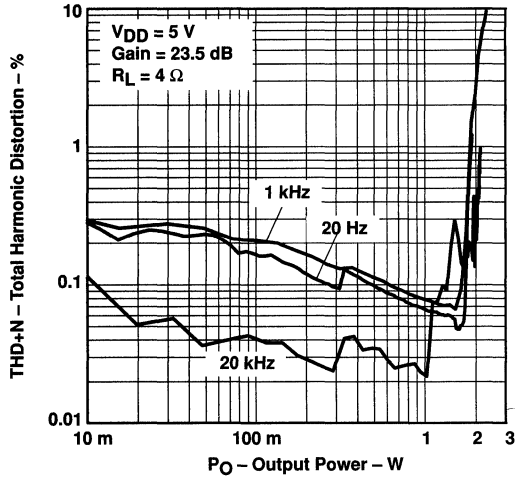


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

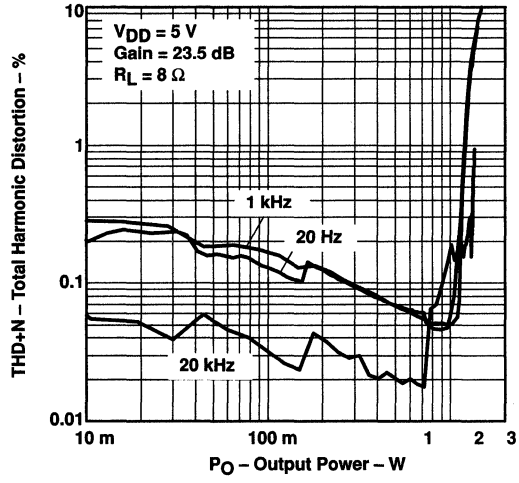


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

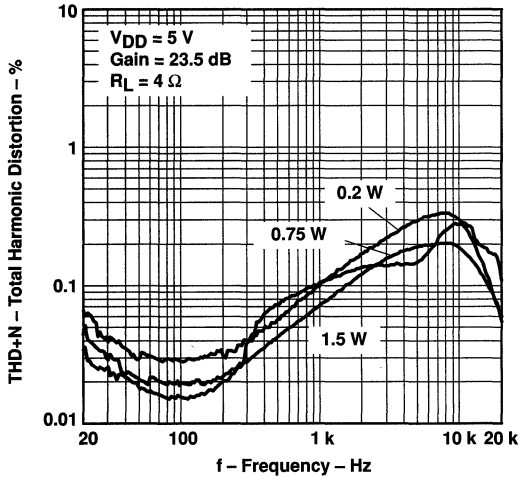


Figure 8

TYPICAL CHARACTERISTICS

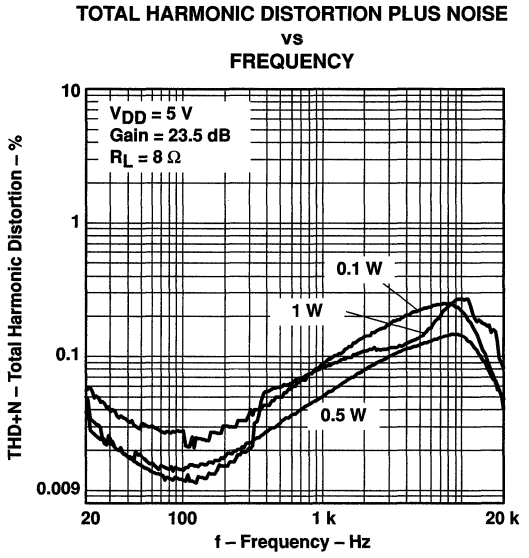


Figure 9

APPLICATION INFORMATION

eliminating the output filter with the TPA2000D2

This section will focus on why the user can eliminate the output filter with the TPA2000D2.

effect on audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential pre-filtered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 10. Note that even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing high loss thus causing a high supply current.

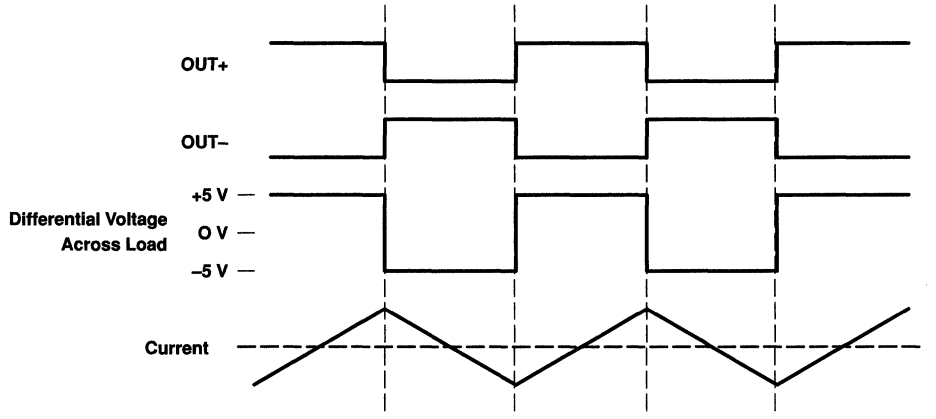


Figure 10. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With no Input

TPA2000D2 modulation scheme

The TPA2000D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT– are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT– is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT– is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION

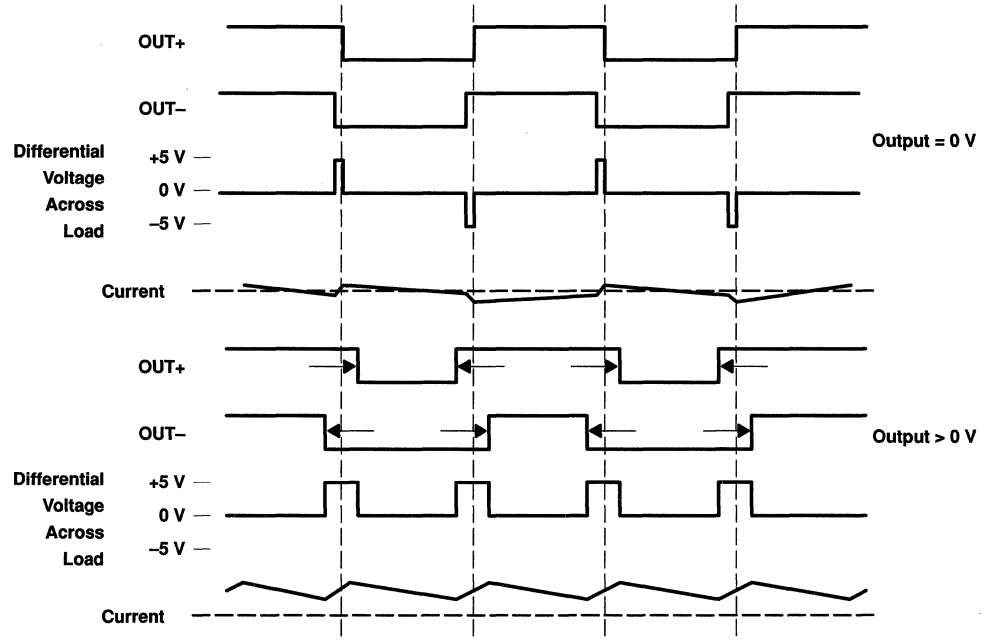


Figure 11. The TPA2000D2 Output Voltage and Current Waveforms Into an Inductive Load

efficiency: why you must use a filter with the traditional class-D modulation scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$ and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2000D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cut-off frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

APPLICATION INFORMATION

effects of applying a square wave into a speaker

Audio specialists have said for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency, $\eta_{MEASURED}$, minus the theoretical efficiency, $\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (1)$$

$$P_{SPKR} = P_{SUP} / P_{OUT} - P_{SUP\ THEORETICAL} / P_{OUT} \text{ (at max output power)} \quad (2)$$

$$P_{SPKR} = 1/\eta_{MEASURED} - 1/\eta_{THEORETICAL} \text{ (at max output power)} \quad (3)$$

The maximum efficiency of the TPA2000D2 with an 8-Ω load is 85%. Using equation 3 with the efficiency at maximum power from Figure 2 (78%), we see that there is an additional 106 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

when to use an output filter

Design the TPA2000D2 without the filter if the traces from amplifier to speaker are short. The TPA2000D2 passed FCC and CE radiated emissions with no shielding with speaker wires 8 inches long or less. Notebook PCs and powered speakers where the speaker is in the same enclosure as the amplifier are good applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without a filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA2000D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 2 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 20 kΩ, which is the absolute minimum input impedance of the TPA2000D2. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

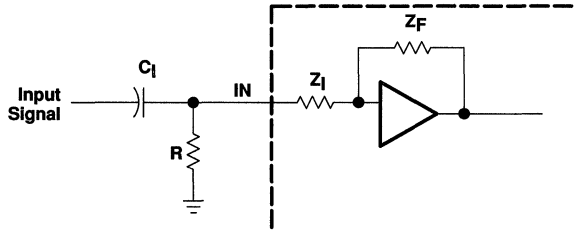
APPLICATION INFORMATION

Table 2. Gain Settings

GAIN0	GAIN1	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	8	104
0	1	12	74
1	0	17.5	44
1	1	23.5	24

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The –3 dB frequency can be calculated using equation 4:

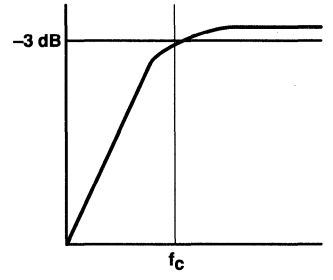
$$f_{-3\ dB} = \frac{1}{2\pi\ C_I(R \parallel Z_I)} \tag{4}$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 5.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \tag{5}$$



APPLICATION INFORMATION

The value of C_I is important as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ and the specification calls for a flat bass response down to 80 Hz. Equation 5 is reconfigured as equation 6.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (6)$$

In this example, C_I is 0.1 μF so one would likely choose a value in the range of 0.1 μF to 1 μF. If the gain is known and will be constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

C_I must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing CI for a given cut-off frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$C_I \leq C_{BYP} / 10 \quad (7)$$

power supply decoupling, C_S

The TPA2000D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, C_{BYP} should be 10 times larger than C_I.

$$C_{BYP} \geq 10 \times C_I \quad (8)$$

APPLICATION INFORMATION

differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of a channel. To use the TPA2000D2 EVM with a differential source, connect the positive lead of the audio source to the RINP (LINP) input and the negative lead from the audio source to the RINN (LINN) input. To use the TPA2000D2 with a single-ended source, ac ground the RINN and LINN inputs through a capacitor and apply the audio single to the RINP and LINP inputs. In a single-ended input application, the RINN and LINN inputs should be ac grounded at the audio source instead of at the device inputs for best noise performance.

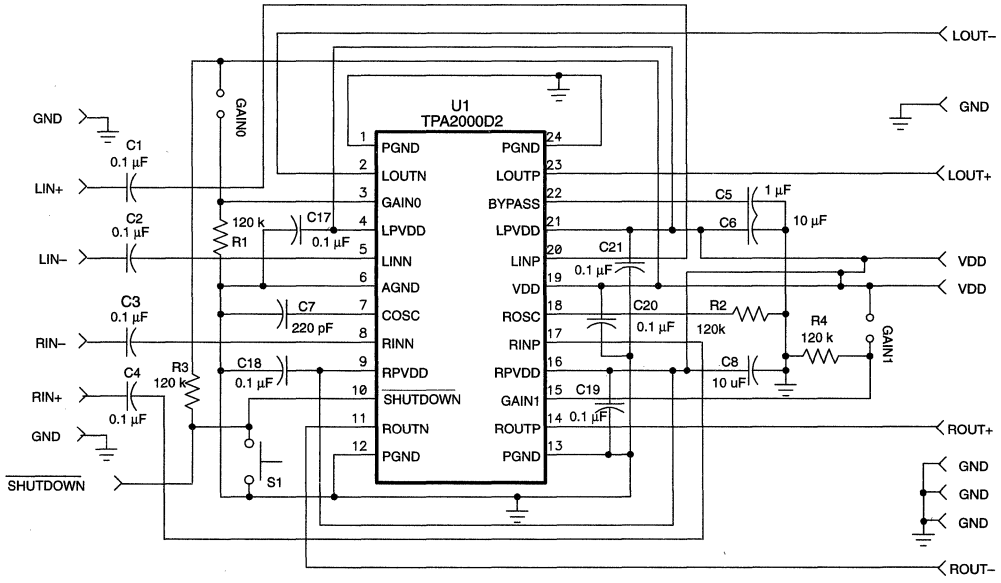
shutdown modes

The TPA2000D2 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)}$ = 1 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

evaluation circuit



NOTE: R1, R3, and R4 are used in the EVM but are not required for normal applications.

APPLICATION INFORMATION

Table 3. TPA2000D2 Evaluation Bill of Materials

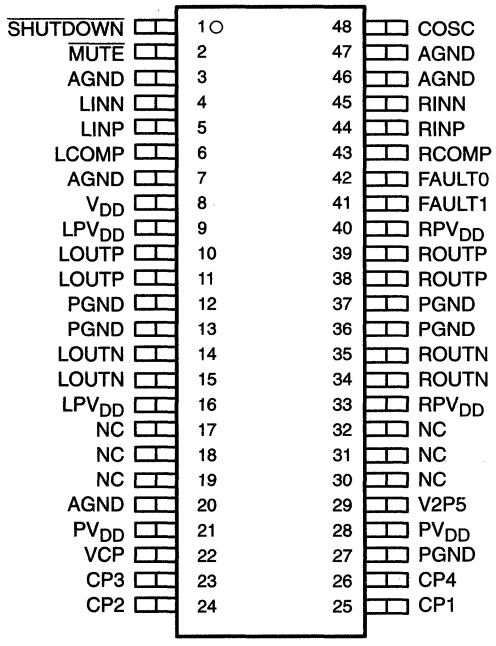
REFERENCE	DESCRIPTION	SIZE	QUANTITY	MANUFACTURER	PART NUMBER
C1–4, C17–21	Capacitor, ceramic chip, 0.1 µF, ±10%, X7R, 50 V	0805	9	Kemet	C0805C104K5RAC
C5	Capacitor, ceramic, 1.0 µF, +80%/–20%, Y5V, 16 V	0805	1	Murata	GRM40-Y5V105Z16
C6, C8	Capacitor, ceramic, 10 µF, +80%/–20%, Y5V, 16 V	1210	2	Murata	GRM235-Y5V106Z16
C7	Capacitor, ceramic, 220 pF, ±10%, XICON, 50 V	0805	2	Mouser	140–CC501B221K
R2, R1†, R3†, R4†	Resistor, chip, 120 kΩ, 1/10 W, 5%, XICON	0805	2	Mouser	260–120K
U1	IC, TPA2000D2, audio power amplifier, 2-W, 2-channel, class-D	24 pin TSSOP	1	TI	TPA2000D2PWP

† These components are used in the EVM, but they are not required for normal applications.

NOT RECOMMENDED FOR NEW DESIGNS

- **Choose TPA2000D2 For Upgrade**
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **2-W BTL Output Into 4 Ω**
- **5-W Peak Music Power**
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- **Shutdown Control . . . 0.2 μA**
- **Thermally-Enhanced PowerPAD™ Surface-Mount Packaging**
- **Thermal, Over-Current, and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPA005D12 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA005D12 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 2 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 5-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control is provided to limit total quiescent current to 0.2 μA, making the device ideal for battery-powered applications.

A full range of protection circuitry is included to increase device reliability: thermal, over-current, and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D12 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D12 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA005D12DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D12DCAR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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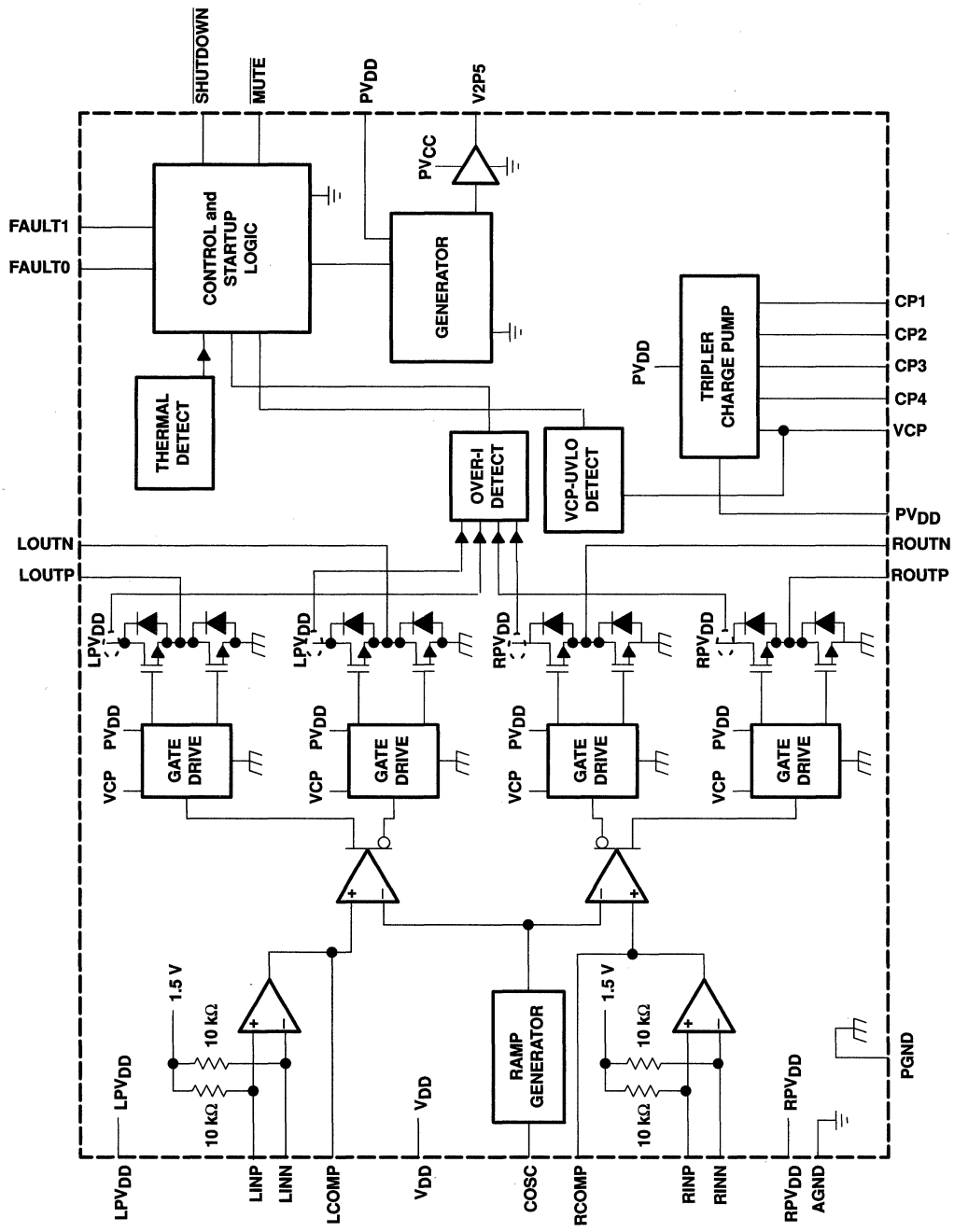
schematic



NOTE A. LPV_{DD}, RPV_{DD}, V_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 46, 47	Analog ground for headphone and Class-D analog sections
COSC	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.
CP1	25	First diode node for charge pump
CP2	24	First inverter switching node for charge pump
CP3	23	Second diode node for charge pump
CP4	26	Second inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
$\overline{MUTE}$	2	Active-low logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	17, 18, 19, 30, 31, 32	No connection
PGND	12, 13	Power ground for left-channel H-bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28	V_{DD} supply for charge-pump and gate-drive circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held at logic high, the device operates normally.
V2P5	29	2.5-V internal reference bypass
VCP	22	Storage capacitor terminal for charge pump
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0†	FAULT 1†	DESCRIPTION
1	1	No fault. — The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. — All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
1	0	Over-current fault. — The output transistors are all switched off. This causes the load to be in a high-impedance state. This is a latched fault and is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault. — All the low-side transistors are turned on, shorting the load to ground. This is latched fault and is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

† These logic levels assume a pullup to PV_{DD} from the open-drain outputs.

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)‡

Supply voltage, V_{DD} (PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}) ..... 5.5 V
Input voltage, V_I ($\overline{\text{SHUTDOWN}}$, $\overline{\text{MUTE}}$) ..... −0.3 V to 5.8 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Charge pump voltage, V_{CP} ..... PV_{DD} + 15 V
Continuous H-bridge output current ..... 2 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 5 A
Continuous total power dissipation ..... See Dissipation Ratings Table
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Operating case temperature range, T_C ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$† POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 mW

† Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	4.25			V
Low-level input voltage, V_{IL}			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, differential input voltage			1	V_{RMS}
PWM frequency	150		450	kHZ

electrical characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5 V, R_L = 4 Ω, T_C = 25°C, See Figure 1 (resistive load) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 4.5 V to 5.5 V		40		dB
I_{DD}	Supply current	No load, No filter		25	35	mA
I_{DD}(MUTE)	Supply current, mute mode	$\overline{MUTE}$ = 0 V		3.9	10	mA
I_{DD}(SD)	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		0.2	10	μA
I_{IH}	High-level input current	V_{IH} = 5.3 V			1	μA
I_{IL}	Low-level input current	V_{IL} = –0.3 V			–1	μA
$r_{DS(on)}$	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	I_D = 2 A		700	900	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel	I_D = 0.5 A	95%	99%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5 V, R_L = 4 Ω, T_C = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	RMS output power, THD = 0.5%, per channel			2		W
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz		0.2%		
	Efficiency	P_O = 1 W, R_L = 8 Ω		80%		
A_V	Gain			25		dB
	Left/right channel gain matching		95%	99%		
	Noise floor			–55		dBV
	Dynamic range			70		dB
	Crosstalk	f = 1 kHz		–55		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JP}$	Thermal resistance, junction-to-pad				10	°C/W
	Thermal shutdown temperature			165		°C

PARAMETER MEASUREMENT INFORMATION

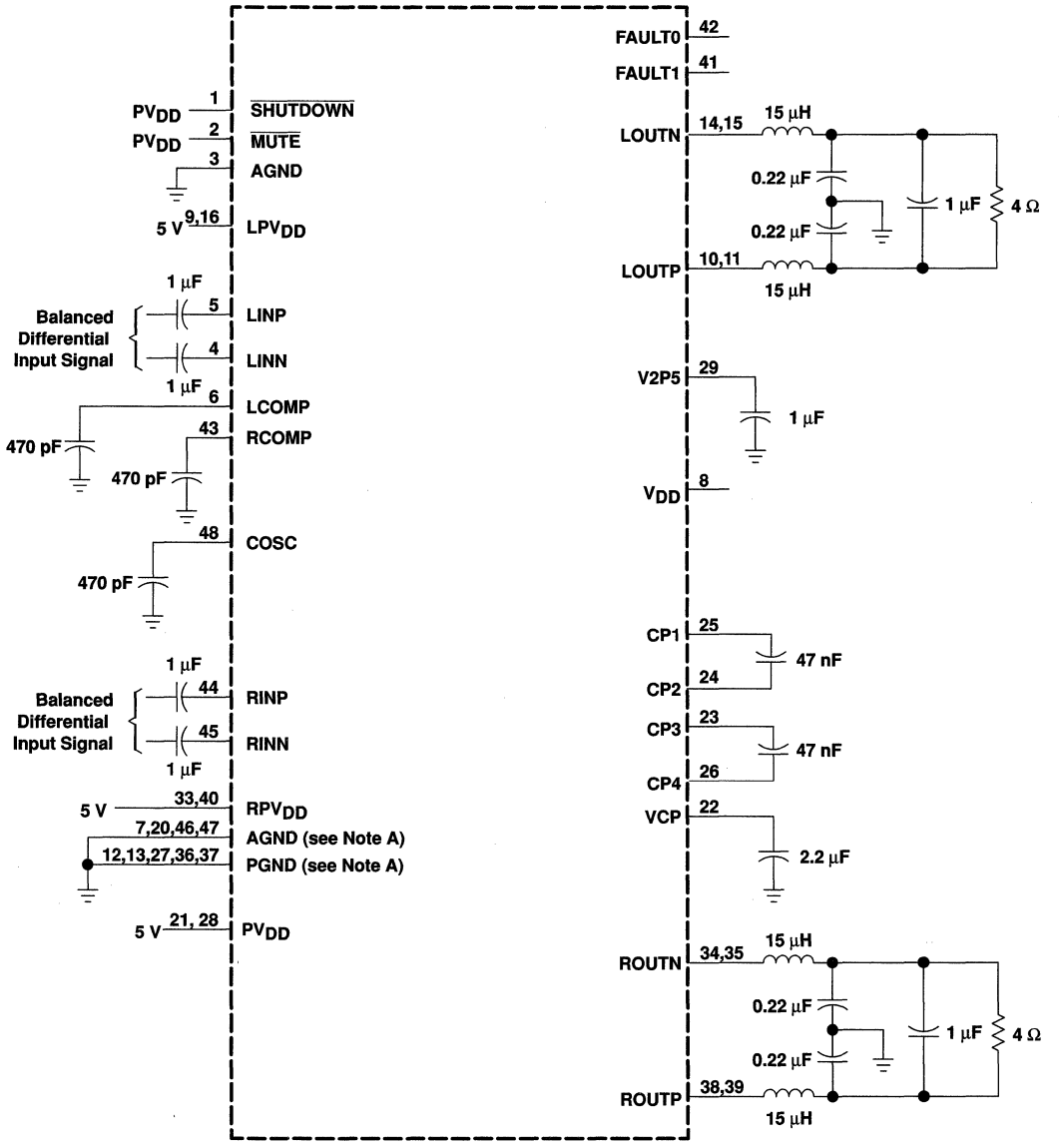
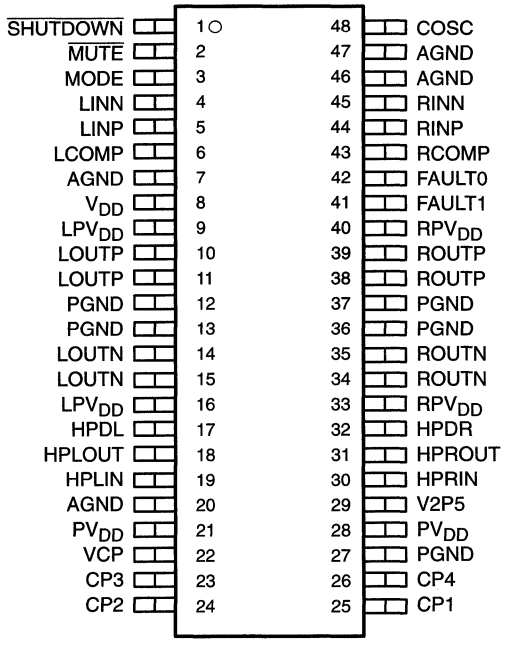


Figure 1. 5-V, 4-Ω Test Circuit, Class-D Amplifier

- **Choose TPA2000D2 For Upgrade**
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels, Plus Stereo Headphones**
- **2-W BTL Output Into 4 Ω**
- **5-W Peak Music Power**
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- **Shutdown Control . . . 0.2 μA**
- **Class-AB Headphone Amplifier**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal, Over-Current, and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



description

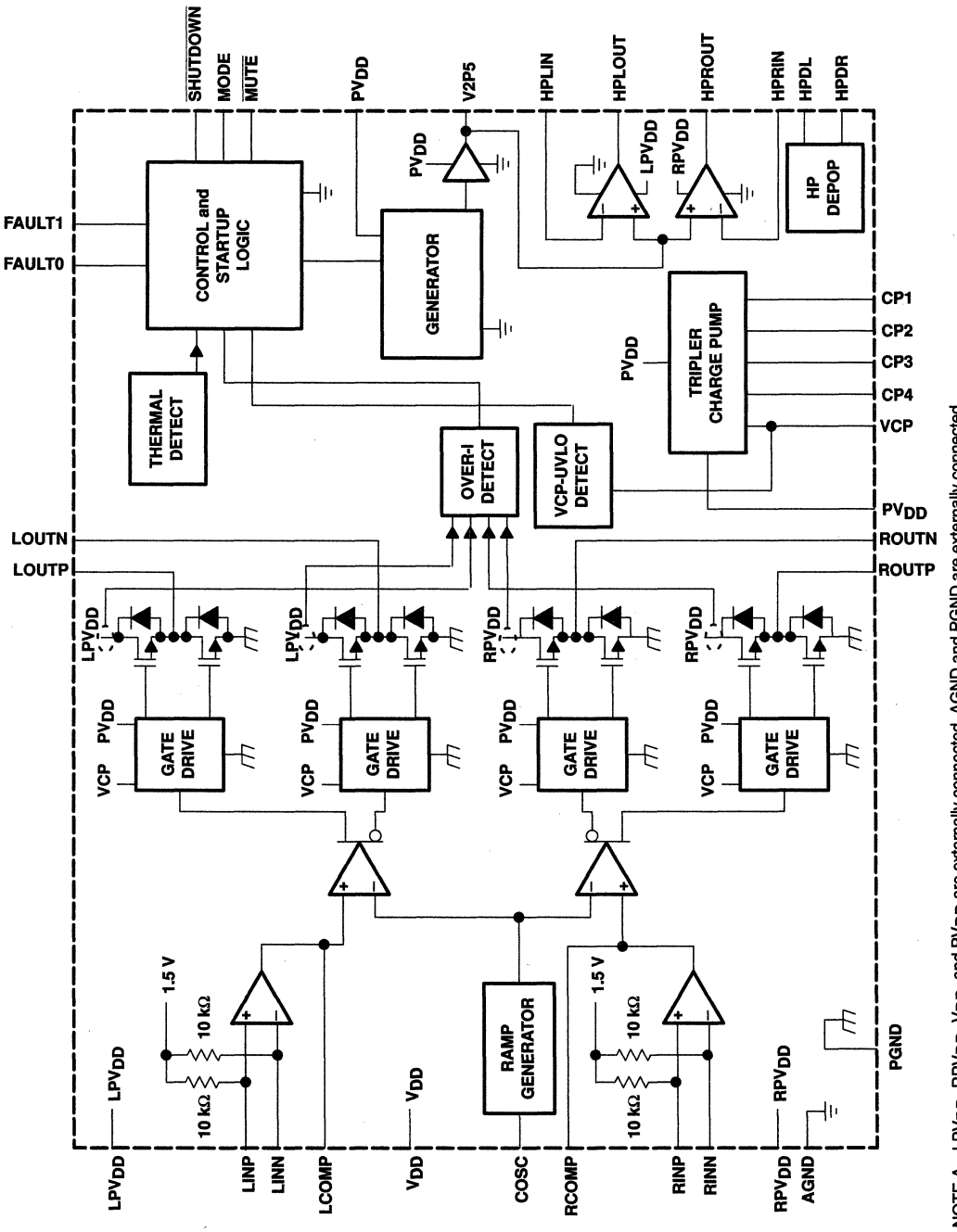
The TPA005D14 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA005D14 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 2 W of continuous average power into a 4-Ω load at 0.4% THD+N from a 5-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. Included is a Class-AB headphone amplifier with interface logic to select between the two modes of operation. Only one amplifier is active at any given time, and the other is in power-saving sleep mode. Also, a chip-level shutdown control is provided to limit total quiescent current to 0.2 μA, making the device ideal for battery-powered applications.

A full range of protection circuitry is included to increase device reliability: thermal, over-current, and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D14 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D14 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

schematic



NOTE A. LPV_{DD}, RPV_{DD}, V_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	7, 20, 46, 47	Analog ground for headphone and Class-D analog sections
COSC	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.
CP1	25	First diode node for charge pump
CP2	24	First inverter switching node for charge pump
CP3	23	Second diode node for charge pump
CP4	26	Second inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
HPDL	17	Depop control for left headphone
HPDR	32	Depop control for right headphone
HPLIN	19	Headphone amplifier left input
HPLOUT	18	Headphone amplifier left output
HPRIN	30	Headphone amplifier right input
HPROUT	31	Headphone amplifier right output
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
MODE	3	Logic-level mode input signal. When MODE is held low, the main Class-D amplifier is active. When MODE is held high, the head phone amplifier is active.
$\overline{MUTE}$	2	Active-low logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28	V_{DD} supply for charge-pump and gate-drive circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held at logic high, the device operates normally.
V2P5	29	2.5-V internal reference bypass
VCP	22	Storage capacitor terminal for charge pump
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0†	FAULT 1†	DESCRIPTION
1	1	No fault. — The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault — All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
1	0	Over-current fault — The output transistors are all switched off. This causes the load to be in a high-impedance state. This is a latched fault and is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault — All the low-side transistors are turned on, shorting the load to ground. This is latched fault and is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

† These logic levels assume a pullup to PV_{DD} from the open-drain outputs.

headphone amplifier faults

The thermal fault remains active when the device is in head phone mode. This fault operates exactly the same as it does for the Class-D amplifier (see Table 1).

If LPV_{DD} or RPV_{DD} drops below 4.5 V, the headphone is disabled by the under-voltage lockout circuitry. Once LPV_{DD} and RPV_{DD} exceed 4.5 V, the headphone amplifier is re-enabled. No fault is reported to the user.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA005D14DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D14DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)‡

Supply voltage, V_{DD} (PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}) ..... 5.5 V
Input voltage, V_I ($\overline{SHUTDOWN}$, $\overline{MUTE}$, MODE) ..... −0.3 V to 5.8 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Charge pump voltage, V_{CP} ..... PV_{DD} + 15 V
Continuous H-bridge output current ..... 2 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 5 A
Continuous total power dissipation ..... See Dissipation Ratings Table
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Operating case temperature range, T_C ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −40°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 mW

‡ See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	4.25			V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	150		450	kHZ

electrical characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 4.5 V to 5.5 V		−40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
I_{DD}(MUTE)	Supply current, mute mode	$\overline{MUTE}$ = 0 V		3.9	10	mA
I_{DD}(SD)	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		0.2	10	μA
I_{IH}	High-level input current	V_{IH} = 5.3 V			1	μA
I_{IL}	Low-level input current	V_{IL} = −0.3 V			−1	μA
$r_{DS(on)}$	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	I_D = 0.5 A		700	900	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel	I_D = 0.5 A	95%	98%		

operating characteristics, Class-D amplifier, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_A = 25°C$, See Figure 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	RMS output power	f = 1 kHz, THD = 0.5%, Per channel		2		W
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz		0.2%		
	Efficiency	P_O = 1 W, $R_L = 8\ \Omega$		80%		
A_V	Gain			20		dB
	Left/right channel gain matching		95%	99%		
	Noise floor			–55		dBV
	Dynamic range			70		dB
	Crosstalk	f = 1 kHz		–55		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

electrical characteristics, headphone amplifier, $PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 32\ \Omega$, $T_A = 25°C$, See Figure 3 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	PV_{DD} = 4.5 V to 5.5 V, A_V = –1 V/V		–60		dB
	Uncompensated gain range		–1		–10	V/V
I_{DD}	Supply current			8	10	mA
I_{DD}(MUTE)	Supply current, mute mode			1.5	2	mA
I_{DD}(SD)	Supply current, shutdown mode			0.2	10	µA
I_{IB}	Input bias current			30		µA

operating characteristics, headphone amplifier, $PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 32\ \Omega$, $T_A = 25°C$, See Figure 3 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%, f = 1 kHz, A_V = –10V/V		50		mW
	Supply voltage rejection ratio	f = 1 kHz		–60		dB
	Noise floor			–84		dBV
	Dynamic range			90		dB
	Crosstalk	f = 1 kHz		–38		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			>1		MΩ

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			165		°C

PARAMETER MEASUREMENT INFORMATION

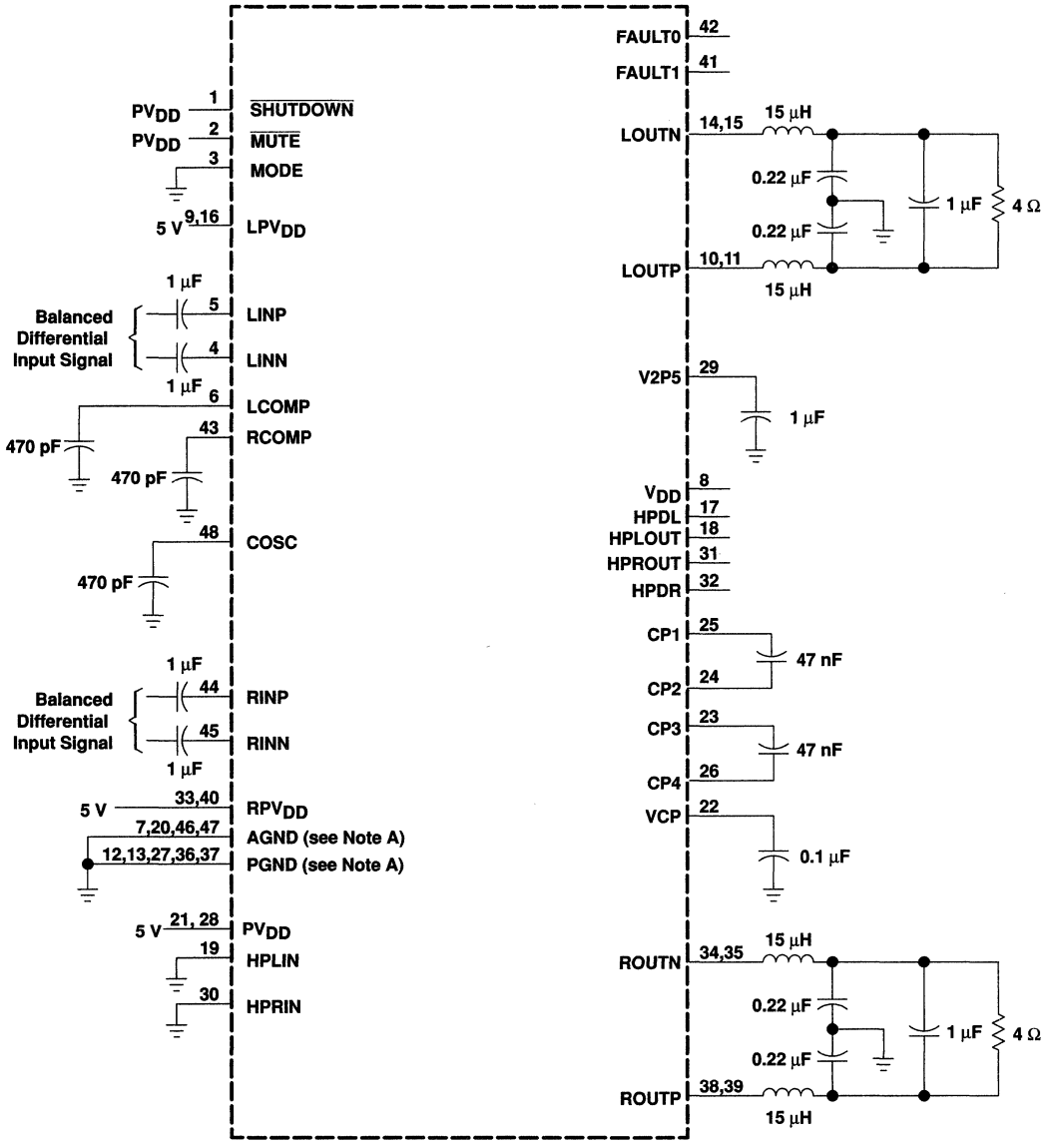


Figure 1. 5-V, 4-Ω Test Circuit, Class-D Amplifier

PARAMETER MEASUREMENT INFORMATION

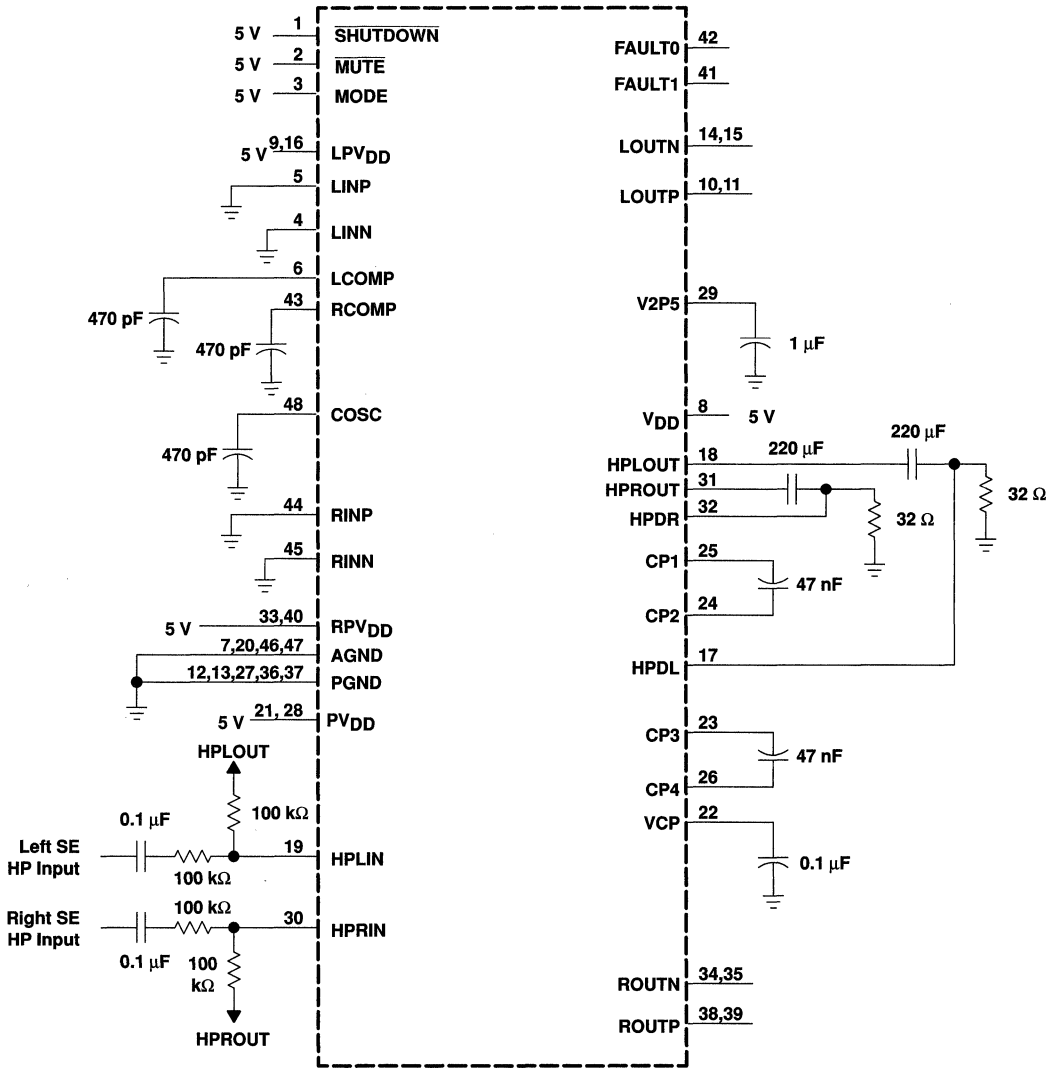


Figure 2. Headphone Test Circuit

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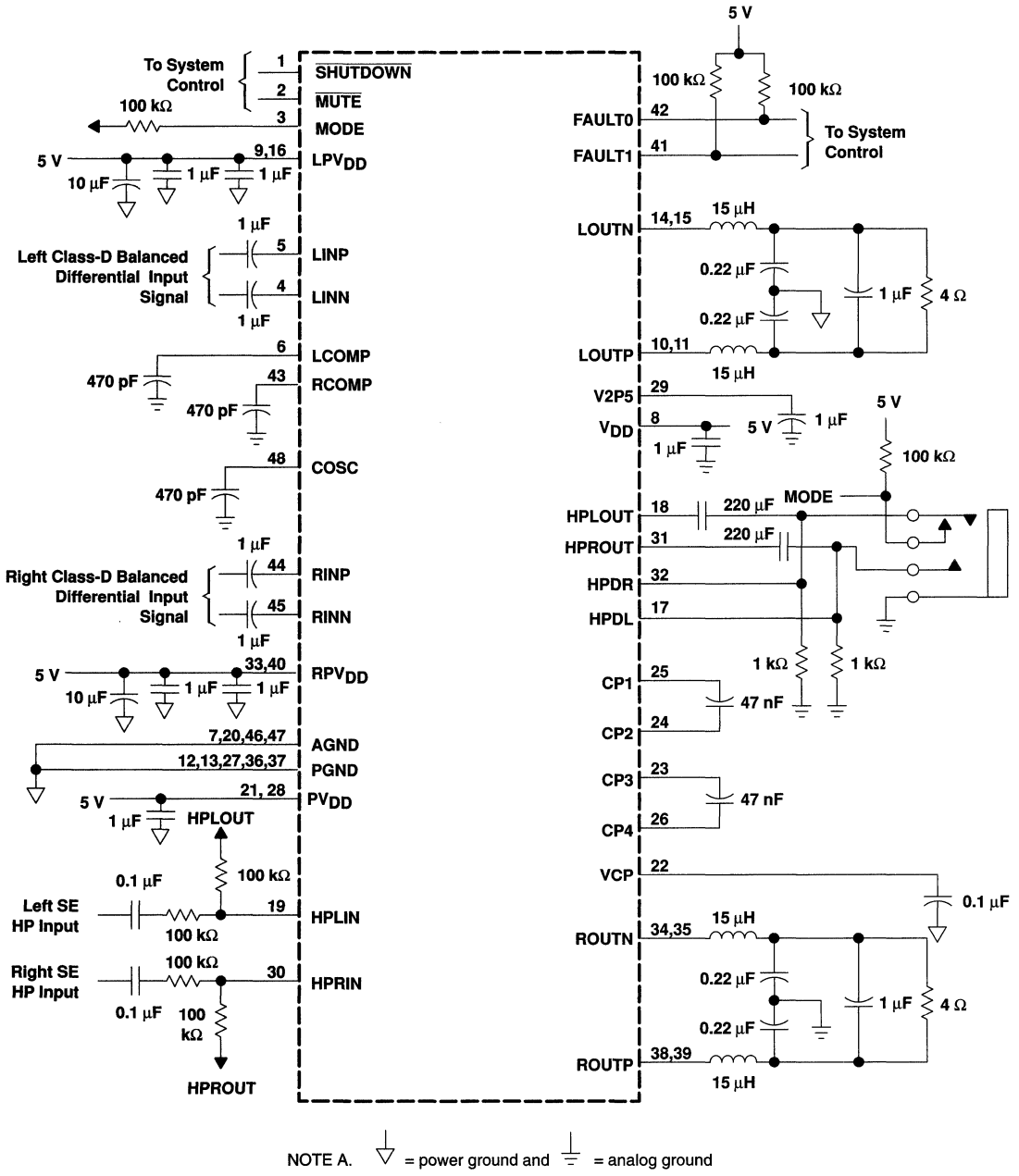
PARAMETER MEASUREMENT INFORMATION



NOTE A. ▽ = power ground and ⏚ = analog ground

Figure 3. TPA032D04 Typical Configuration Application Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Switching frequency	4
		vs Free-air temperature	5, 6
THD+N	Total harmonic distortion plus noise	vs Frequency	7, 9, 11 12, 14, 15
		vs Output power	8, 10, 13
	Gain and phase	vs Frequency	16, 17
	Crosstalk	vs Frequency	18
	Power dissipation	vs Output power	19
	Efficiency	vs Output power	20

SUPPLY CURRENT vs SWITCHING FREQUENCY

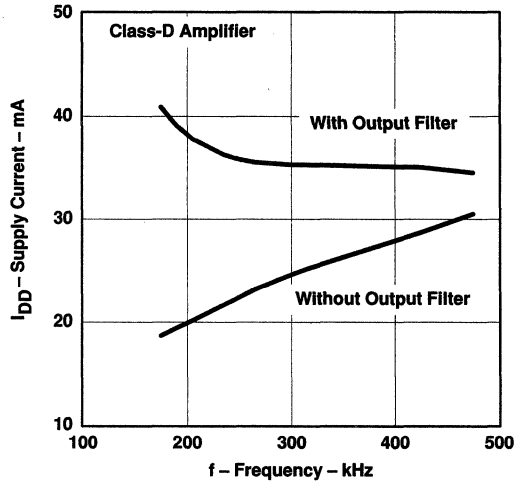


Figure 4

SUPPLY CURRENT vs FREE–AIR TEMPERATURE

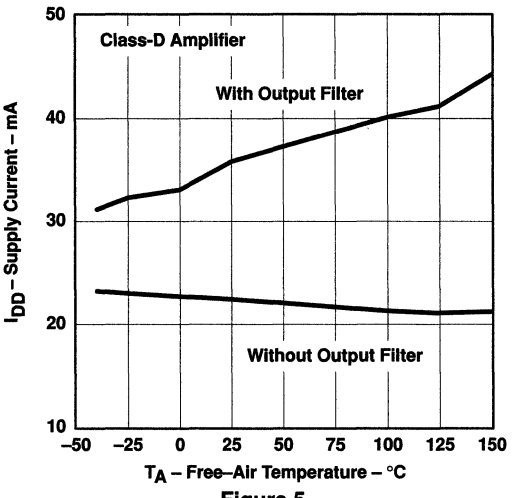


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE–AIR TEMPERATURE

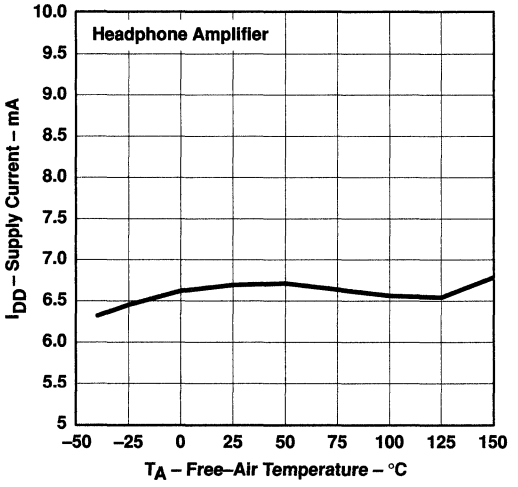


Figure 6

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

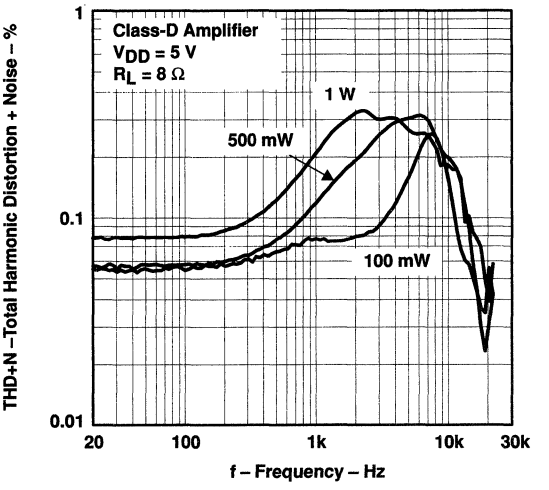


Figure 7

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

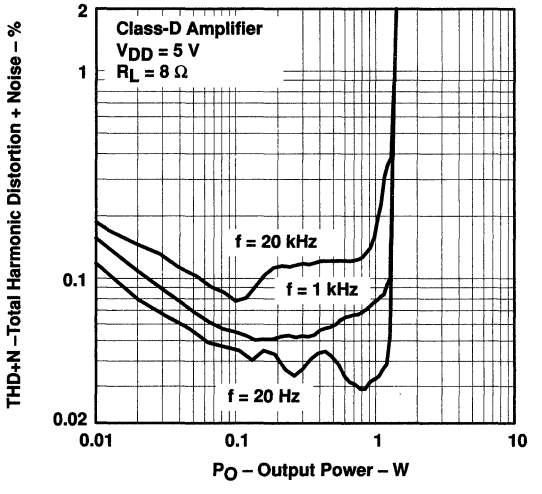


Figure 8

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

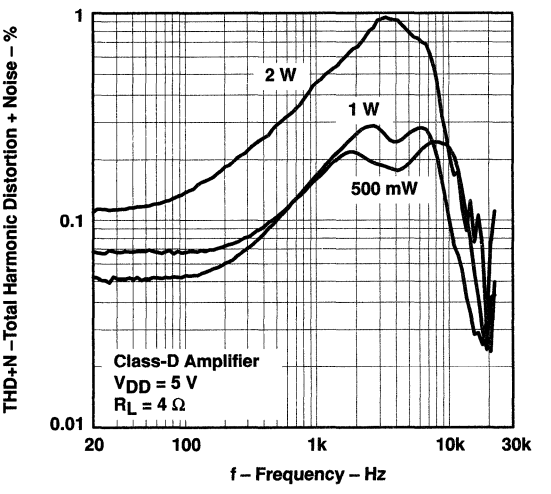


Figure 9

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

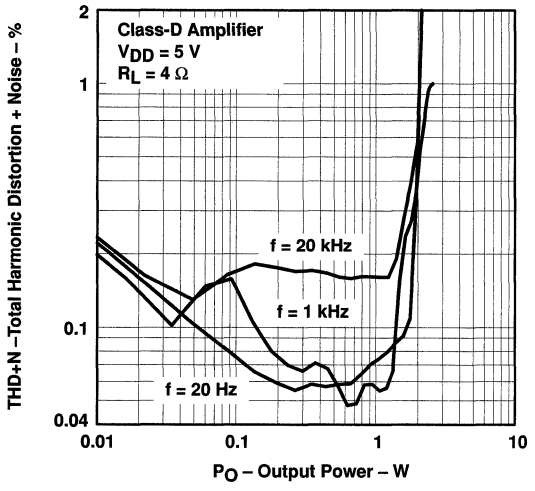


Figure 10

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

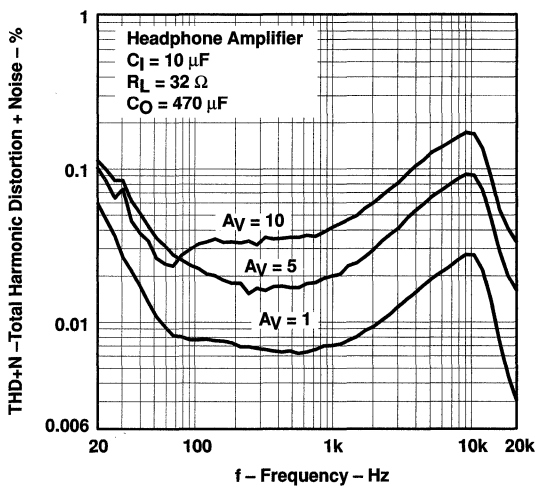


Figure 11

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

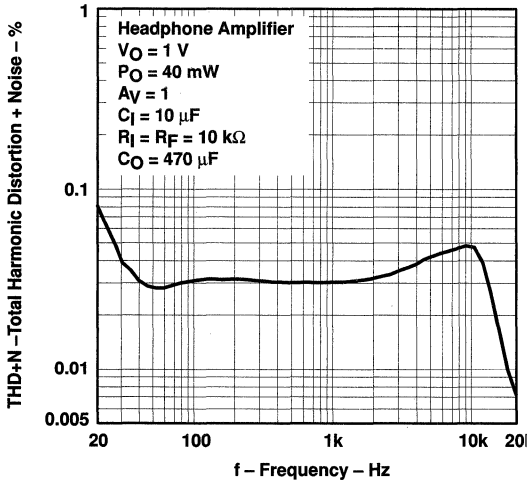


Figure 12

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

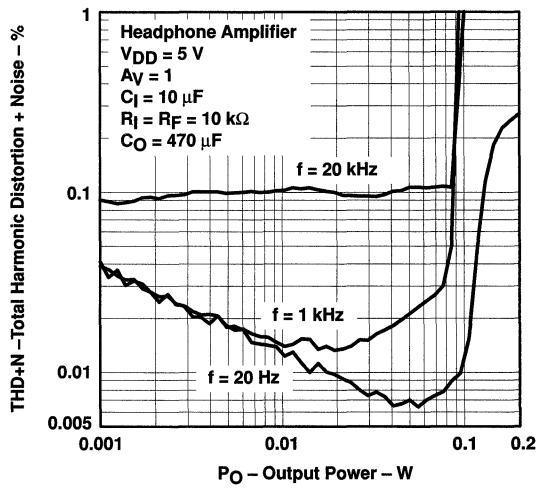


Figure 13

TYPICAL CHARACTERISTICS

HEADPHONE AMPLIFIER
TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

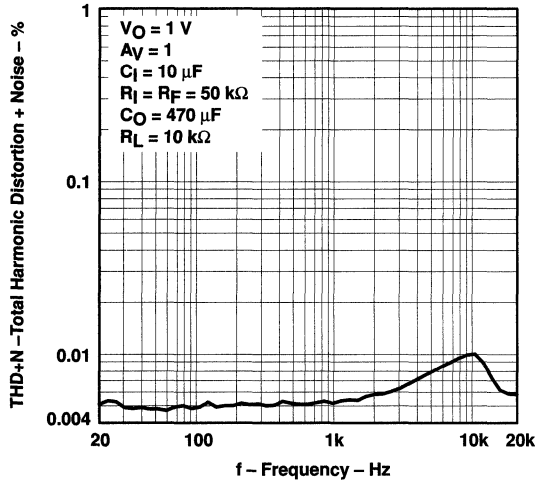


Figure 14

HEADPHONE AMPLIFIER
TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

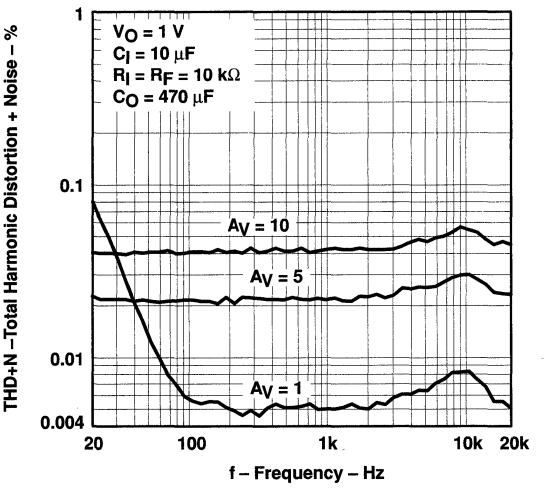


Figure 15

CLASS-D AMPLIFIER
GAIN and PHASE
vs
FREQUENCY

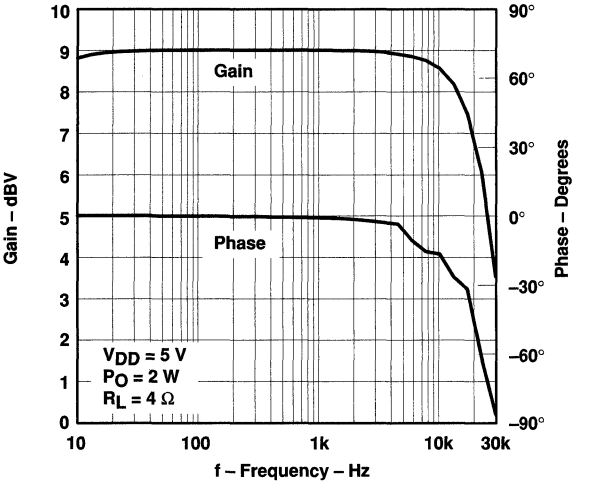


Figure 16

TYPICAL CHARACTERISTICS

HEADPHONE AMPLIFIER
GAIN and PHASE
vs
FREQUENCY

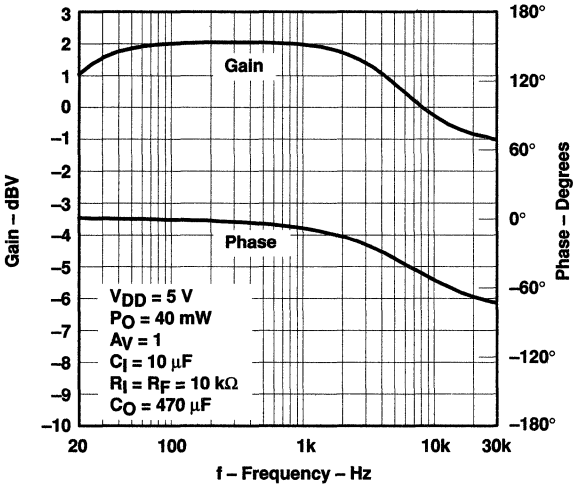


Figure 17

CLASS-D AMPLIFIER
CROSSTALK
vs
FREQUENCY

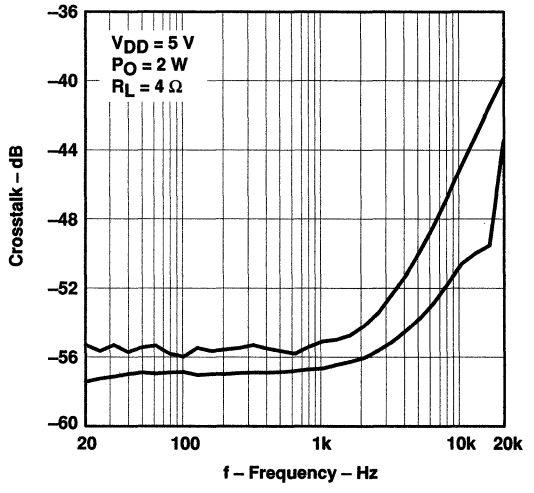


Figure 18

POWER DISSIPATION
vs
OUTPUT POWER

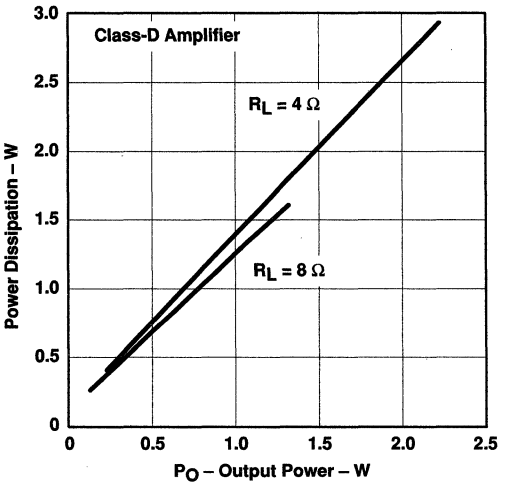


Figure 19

TYPICAL CHARACTERISTICS

EFFICIENCY vs OUTPUT POWER

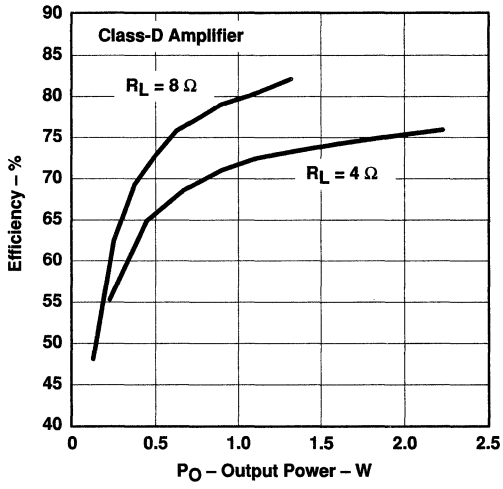


Figure 20

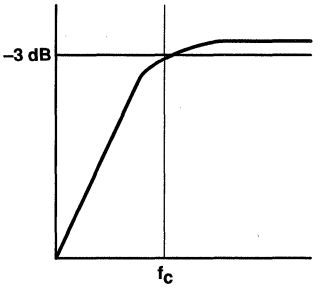
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_{IN}, the TPA005D14's input resistance forms a high-pass filter with the corner frequency determined in equation 1.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (1)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 1 is reconfigured as equation 2.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (2)$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA005D14 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor which should be located physically close to the TPA005D14. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA005D14 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device's various V_{DD} leads works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

The TPA005D14 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA005D14 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 0.2 μA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

For 8-Ω loads, double the inductor value and halve the common-mode capacitors (i.e., 15 μH to 30 μH). For more information, see application report SLOA023, *Reducing and Eliminating the Class-D Output Filter* and application report SLOA031, *Design Considerations for Class-D Audio Power Amplifiers.*

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low ON resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the ON resistance ($r_{DS(ON)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (Figure 21).

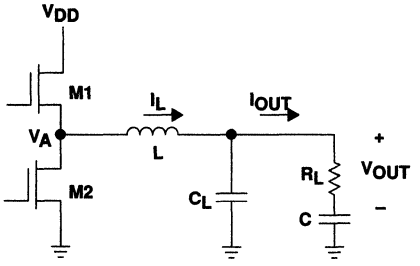


Figure 21. Half-Bridge Class-D Output Stage

Figures 22 and 23 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 21) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

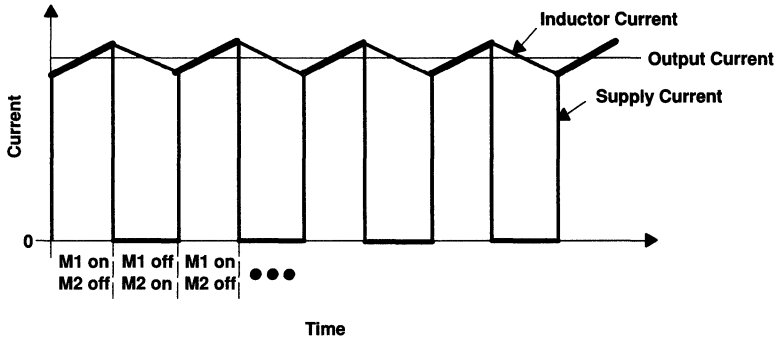


Figure 22. Class-D Currents

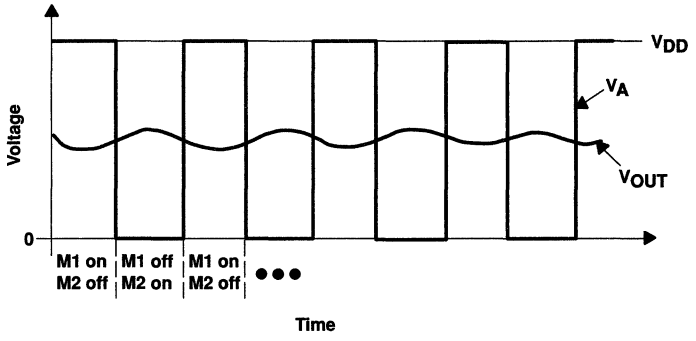


Figure 23. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average}\left(I_{DD}\right) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average}\left(I_{DD}\right) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right)$	$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 24.

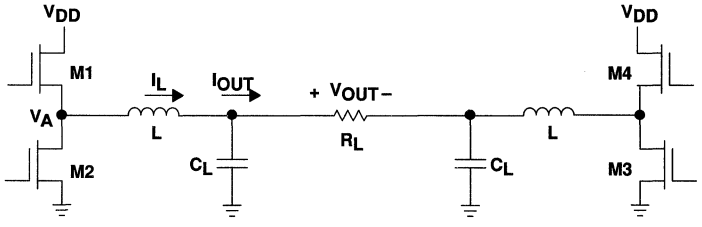


Figure 24. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is ON (saturated). Any $R_{DS(on)}$ above 0 Ω causes conduction loss. Figure 25 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

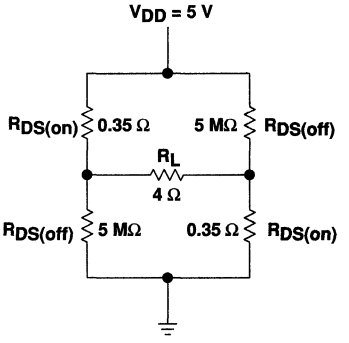


Figure 25. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2R_L}{I^2\,2r_{DS(on)} + I^2R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1,\ R_L = 4\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.35,\ R_L = 4\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A plot of the output, showing switching losses, is shown in Figure 26.

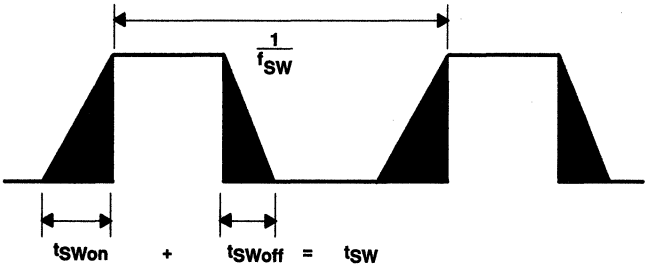


Figure 26. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 1-W per channel audio system with 8-Ω loads and a 5-V supply is almost 2.7 W. A similar linear amplifier such as the TPA005D14 has a maximum draw of 3.25 W under the same circumstances.

Table 2. Efficiency vs Output Power in 5-V 8-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	63.4	2	0.145
0.5	73	2.83	0.183
0.75	77.1	3.46	0.222
1	79.3	4	0.314
1.25	80.6	4.47†	0.3

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (Figure 27); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

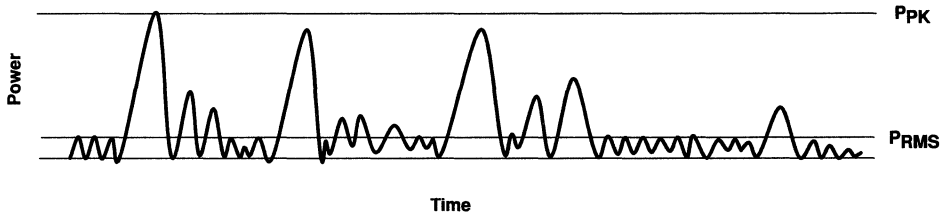


Figure 27. Audio Signal Showing Peak and RMS Power

Figure 28 is a comparison of a 5-V class-D amplifier to a similar linear amplifier playing music that has a 13.76-dB crest factor. From the plot, the power supply draw from a stereo amplifier that is playing music with a 13.76 dB crest factor is 1.02 W, while a class-D amplifier draws 420 mW under the same conditions. This means that just under 2.5 times the power supply is required for a linear amplifier over a class-D amplifier.

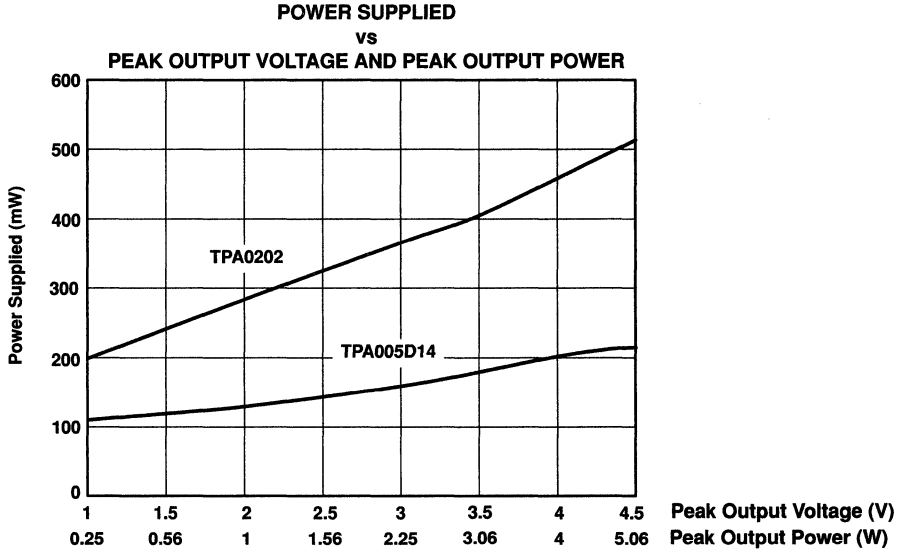


Figure 28. Audio Signal Showing Peak and RMS Power (With Music Applied)

APPLICATION INFORMATION

class-D effect on battery life

Battery operations for class-D amplifiers versus linear amplifiers have similar power supply savings results. The essential contributing factor to longer battery life is lower RMS supply current. Figure 29 compares the TPA005D14 supply current to the supply current of the TPA0202, a 2-W linear device, while playing music at different peak voltage levels.

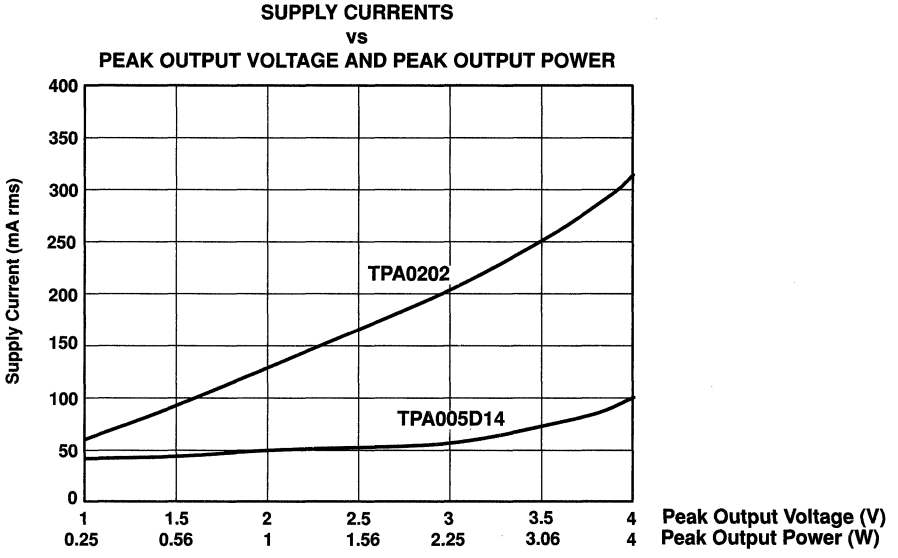


Figure 29. Supply Current vs Peak Output Voltage of TPA005D14 vs TPA0202 With Music Input

This plot shows that a linear amplifier has approximately three times more current draw at normal listening levels than a class-D amplifier. Thus, a class-D amplifier has approximately three times longer battery life at normal listening levels. If there is other circuitry in the system drawing supply current, that must also be taken into account when estimating battery life savings.

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA005D14 data sheet, one can see that when the TPA005D14 is operating from a 5-V supply into a 4-Ω speaker that 4 W peaks are available. Converting Watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4}{1}\right) = 6 \text{ dB} \quad (3)$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (4)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (12 dB crest factor)
= 500 mW (9 dB crest factor)
= 1000 mW (6 dB crest factor)
= 2000 mW (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA005D14 and maximum ambient temperatures is shown in Table 3.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 3. TPA005D14 Power Rating, 5-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	0.56	125°C
4	1000 mW (6 dB)	0.30	136°C†
4	500 mW (9 dB)	0.23	139°C†
4	250 mW (12 dB)	0.20	141°C†
4	120 mW (15 dB)	0.14	143°C†
4	63 mW (18 dB)	0.09	146°C†

† Case temperature (T_C) is rated to 125°C maximum.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DCA	5.6 W	44.8 mW/°C	3.5 W	2.9 W

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \quad (5)$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA005D14 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (6)$$

$$= 150 - 22.3(0.14 \times 2) = 143°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(0.56 \times 2) = 125°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with a 15 dB crest factor per channel.

Table 3 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA005D14 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 30) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

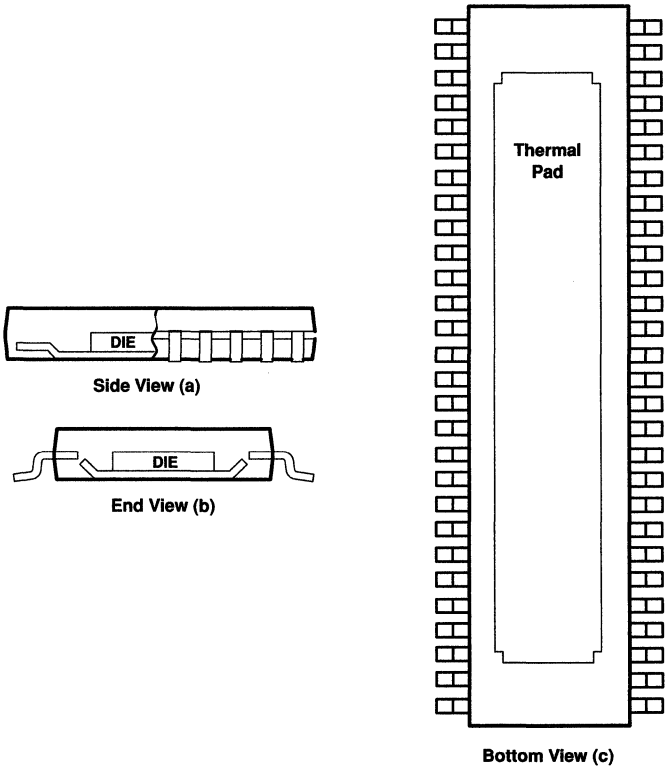
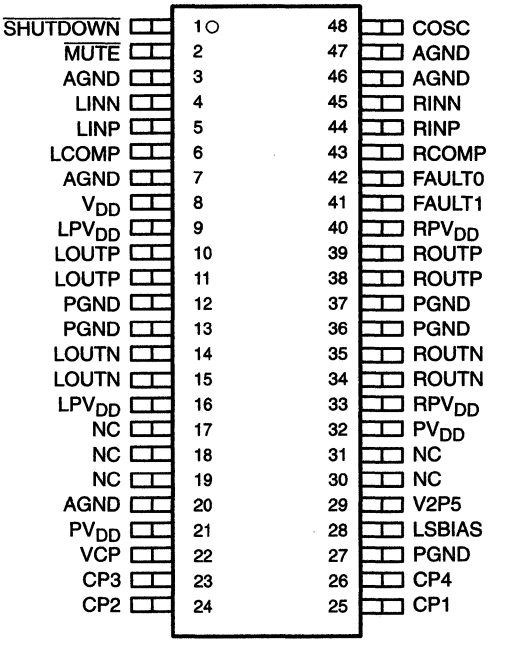


Figure 30. Views of Thermally Enhanced DCA Package

NOT RECOMMENDED FOR NEW DESIGNS

- **Choose TPA2000D2 For Upgrade**
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **2-W BTL Output into 4 Ω**
- **5-W Peak Music Power**
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- **Shutdown Control**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPA005D02 is a monolithic power IC stereo audio amplifier. It operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors. These transistors replicate the analog signal through high-frequency switching of the output stage. This allows the TPA005D02 to be configured as a bridge-tied load (BTL) amplifier.

When configured as a BTL amplifier, the TPA005D02 is capable of delivering up to 2 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 5-V power supply in the high fidelity range (20 Hz to 20 kHz).

A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control limits total supply current to 400 μA. This makes the device ideal for battery-powered applications.

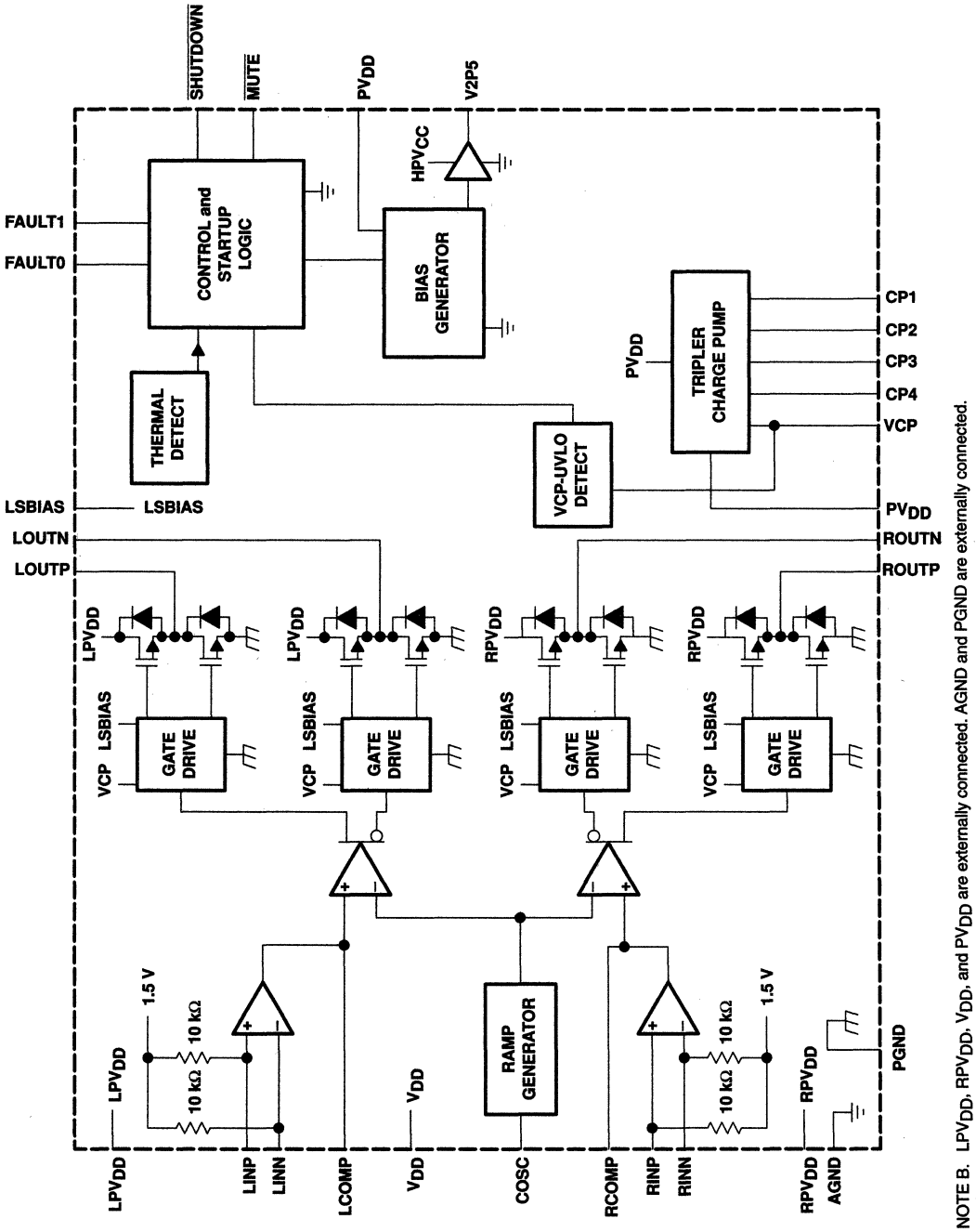
Protection circuitry increases device reliability: thermal and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D02 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D02 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.



NOTE B. LPV_{DD}, RPV_{DD}, V_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 46, 47	Analog ground for analog sections
COSC	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.
CP1	25	First diode node for charge pump
CP2	24	First inverter switching node for charge pump
CP3	23	Second diode node for charge pump
CP4	26	Second inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
LSBIAS	28	Level-shifter power supply, to be tied to VCP
$\overline{MUTE}$	2	Active-low logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	17, 18, 19, 30, 31	No internal connection
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 32	V_{DD} supply for charge-pump and internal logic circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held at logic high, the device operates normally.
V2P5	29	2.5-V internal reference bypass
VCP	22	Storage capacitor terminal for charge pump
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Amplifier Fault Table

FAULT 0†	FAULT 1†	DESCRIPTION
1	1	No fault—The device is operating normally.
1	0	Charge pump under-voltage lock-out (VCP-UV) fault—All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault—All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes. But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

† These logic levels assume a pull up to PV_{DD} from the open-drain outputs.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA005D02DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D02DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)‡

Supply voltage, V_{DD} (PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}) ..... 5.5 V
Bias voltage (LSBIAS) ..... 12 V to 20 V
Input voltage, V_I ($\overline{\text{SHUTDOWN}}$, $\overline{\text{MUTE}}$, MODE) ..... –0.3 V to 5.8 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Charge pump voltage, V_{CP} ..... PV_{DD} + 20 V
Continuous H-bridge output current ..... 2 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 5 A
Continuous total power dissipation, T_C = 25°C ..... 4.5 W§
Operating virtual junction temperature range, T_J ..... –40°C to 150°C
Operating case temperature range, T_C ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
§ Thermal shutdown activates when T_J = 125°C.
NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$¶ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	4.25			V
Low-level input voltage, V_{IL}			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	100		500	kHZ

electrical characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (resistive load) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 4.9$ V to 5.1 V		40		dB
I_{DD}	Supply current	No load or output filter		25	40	mA
$I_{DD(MUTE)}$	Supply current, mute mode	$\overline{MUTE} = 0$ V		10	15	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN} = 0$ V		400	2000	µA
I_{IH}	High-level input current	$V_{IH} = 5.3$ V			10	µA
I_{IL}	Low-level input current	$V_{IL} = -0.3$ V			−10	µA
$r_{DS(on)}$	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	$I_D = 0.5$ A		620	750	mΩ
$r_{DS(on)}$	Matching		95%	99.5%		

operating characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	RMS output power, THD = 0.5%, per channel			2		W
THD+N	Total harmonic distortion plus noise	$P_O = 1$ W, f = 1 kHz		0.2%		
	Efficiency	$R_L = 8\ \Omega$		80%		
A_V	Gain			24		dB
	Left/right channel gain matching			95%		
	Noise floor			60		dB
	Dynamic range			70		dB
	Crosstalk	f = 1 kHz		55		dB
	Frequency response bandwidth, post output filter, −3 dB		20		20,000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JP}$	Thermal resistance, junction-to-pad				10	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-pad†			22.3		°C/W

† Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

PARAMETER MEASUREMENT INFORMATION

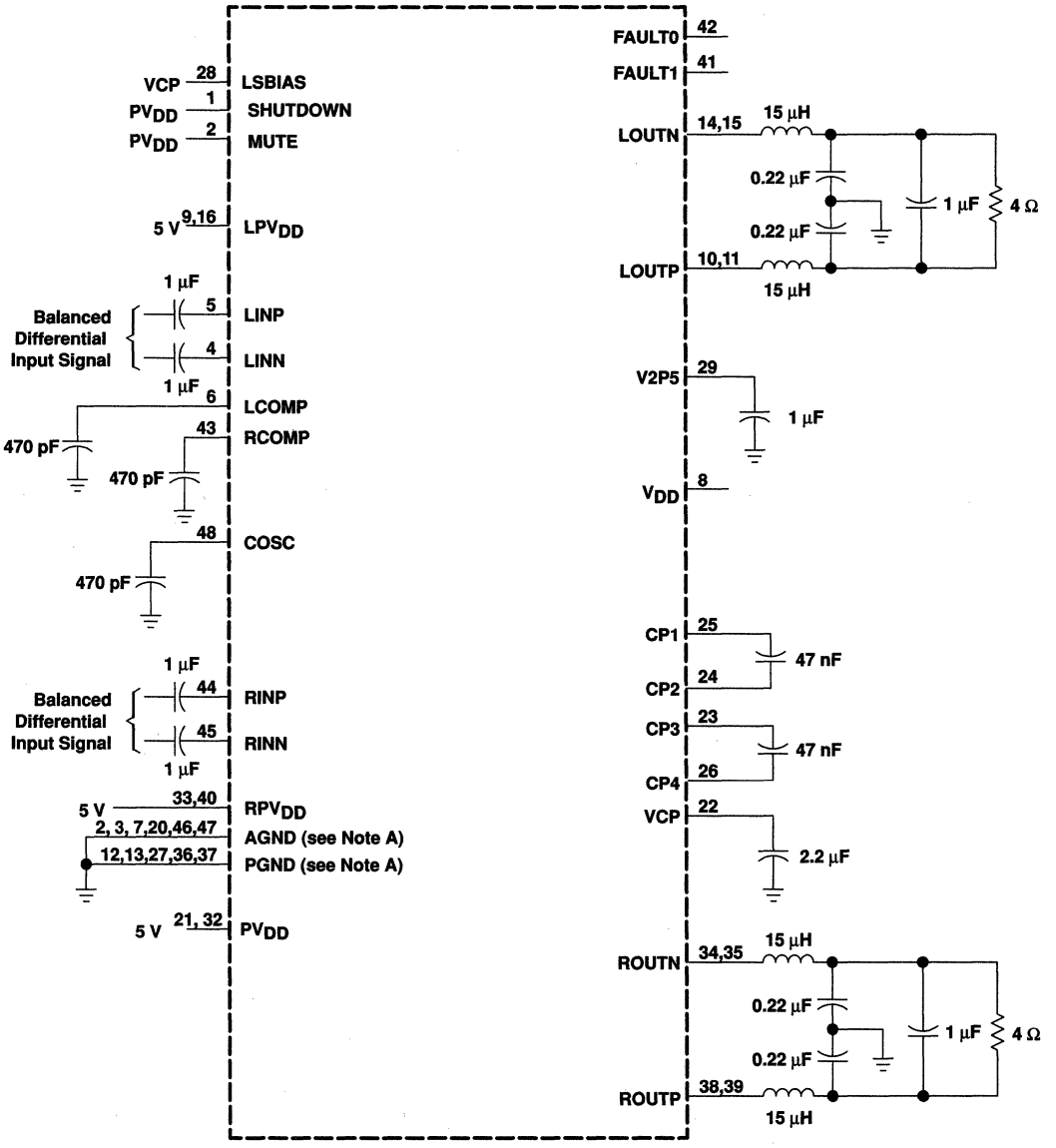


Figure 1. 5-V, 4-Ω Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Switching frequency	2
		vs Free-air temperature	3
THD+N	Total harmonic distortion plus noise	vs Frequency	4, 5
		vs Output power	6, 7
	Voltage amplification and phase shift	vs Frequency	8
	Crosstalk	vs Frequency	9
	Efficiency	vs Output power	10

SUPPLY CURRENT vs SWITCHING FREQUENCY

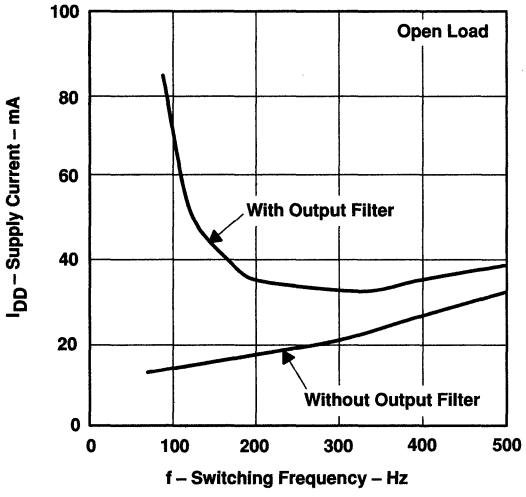


Figure 2

SUPPLY CURRENT vs FREE–AIR TEMPERATURE

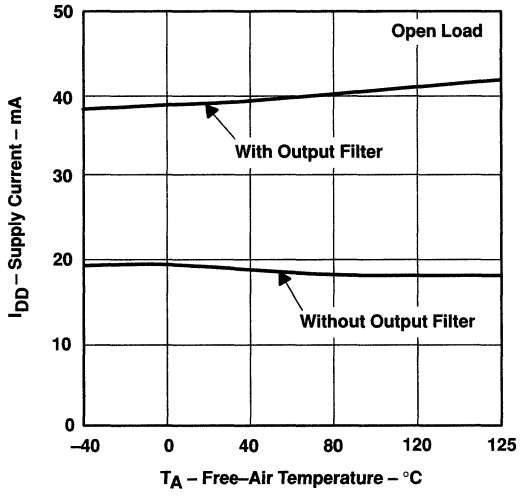


Figure 3

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

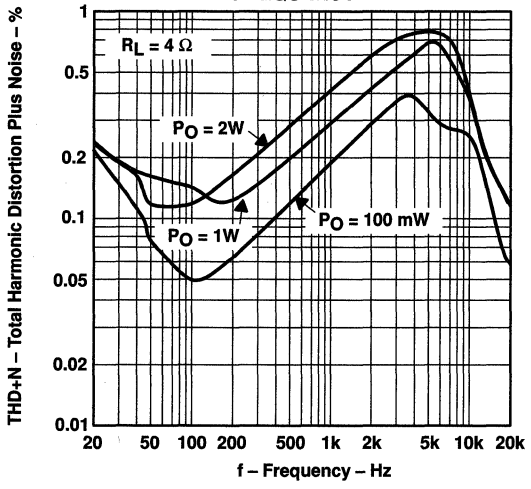


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

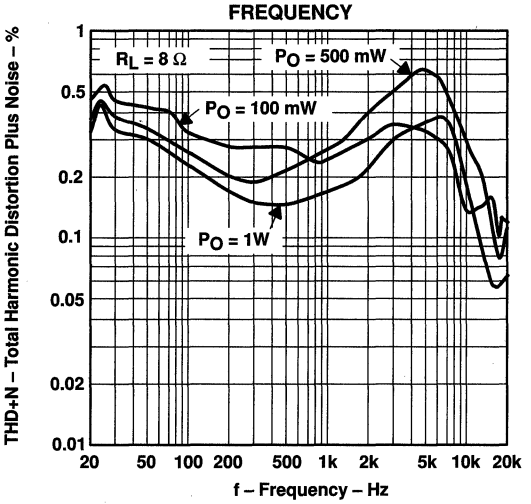


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

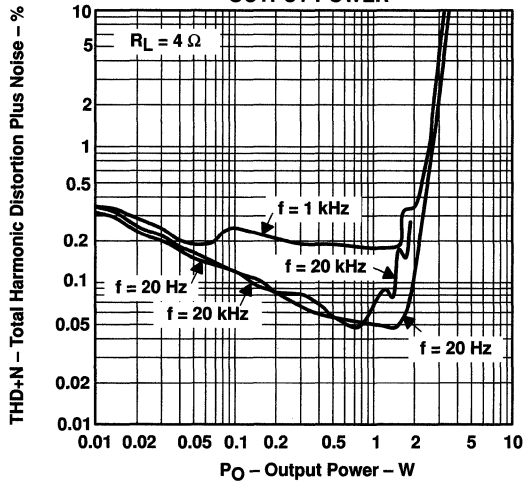


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

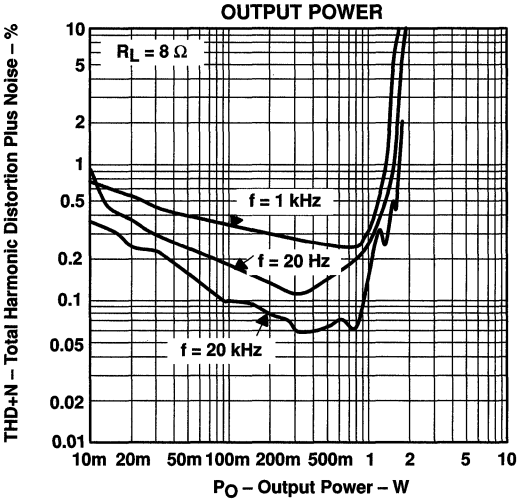


Figure 7

TYPICAL CHARACTERISTICS

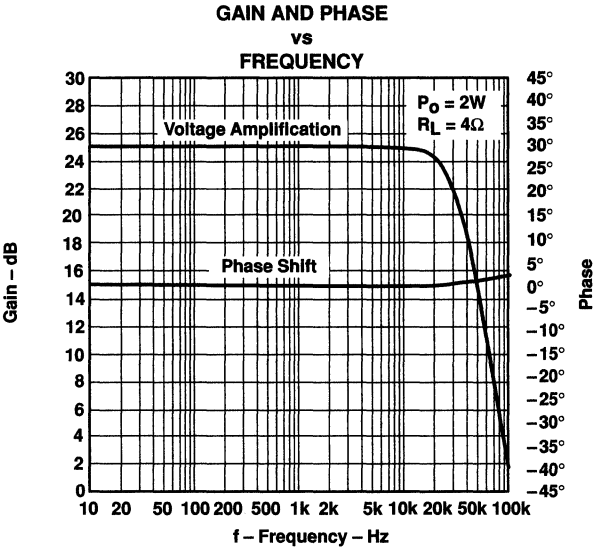


Figure 8

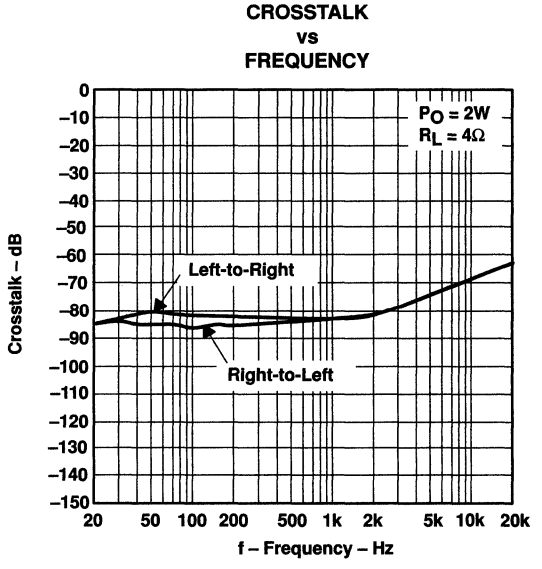


Figure 9

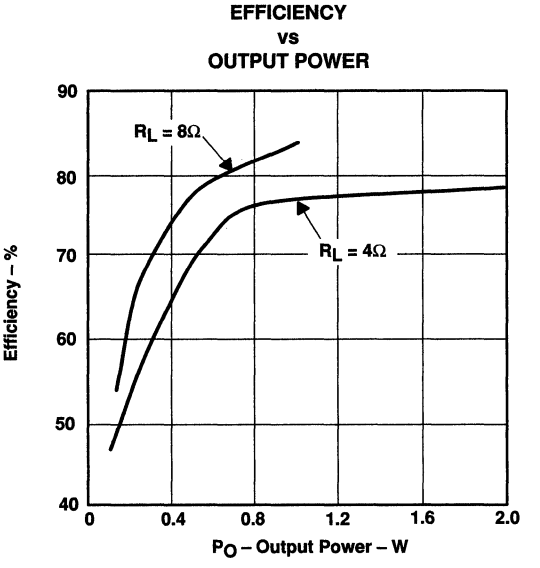


Figure 10

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 11) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

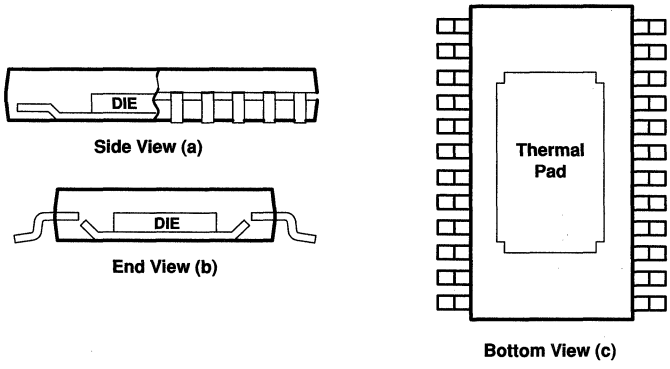
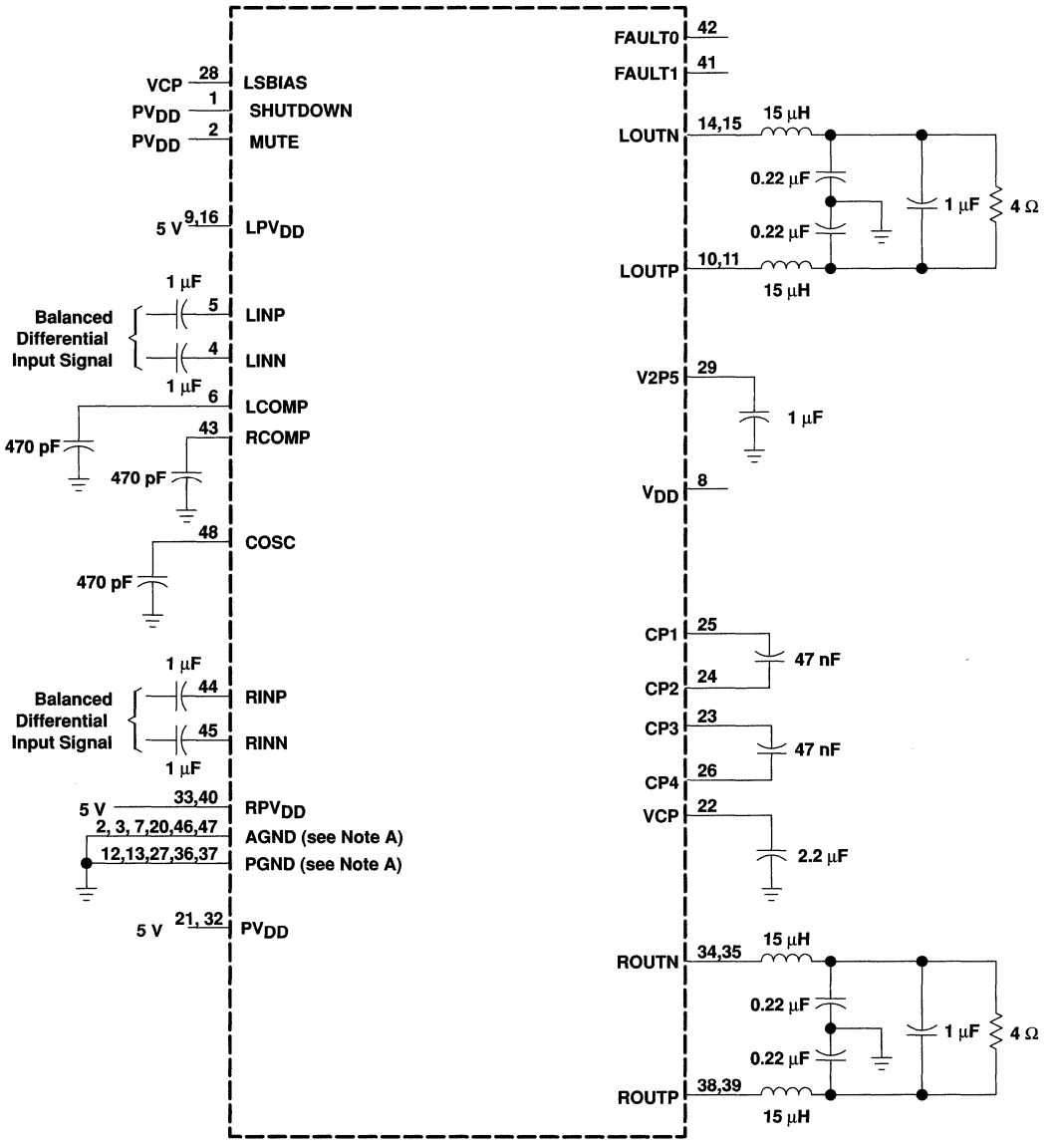


Figure 11. Views of Thermally Enhanced DCA Package

selection of components

Figure 12 is a schematic diagram of a typical notebook computer application circuit.

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 12. TPA005D02 Typical Configuration Application Circuit

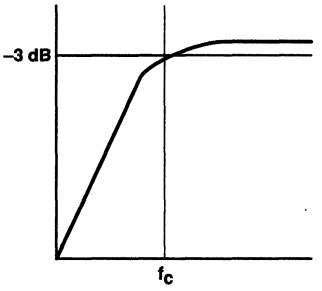
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_{IN}, the TPA005D002's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_{IN} C_I} \quad (8)$$

R_{IN} is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_{IN} f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA005D02 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor which should be located physically close to the TPA005D02. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA005D02 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA005D02 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA005D02 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 400 μA. Mute mode alone reduces I_{DD} to 10 mA.

Table 2. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The DC series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low ON resistance, little voltage is dropped across them, further reducing losses. The ideal class D amplifier is 100% efficient, which assumes that both the ON resistance ($R_{DS(ON)}$) and the switching times of the output transistors are zero.

the ideal class D amplifier

To illustrate how the output transistors of a class D amplifier operate, a half-bridge application is examined first (Figure 13).

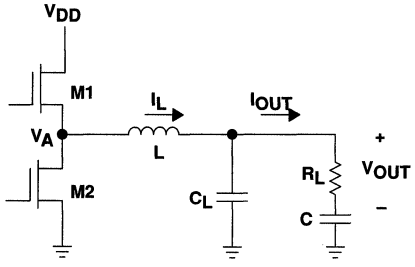


Figure 13. Half-Bridge Class D Output Stage

Figures 14 and 15 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 13) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

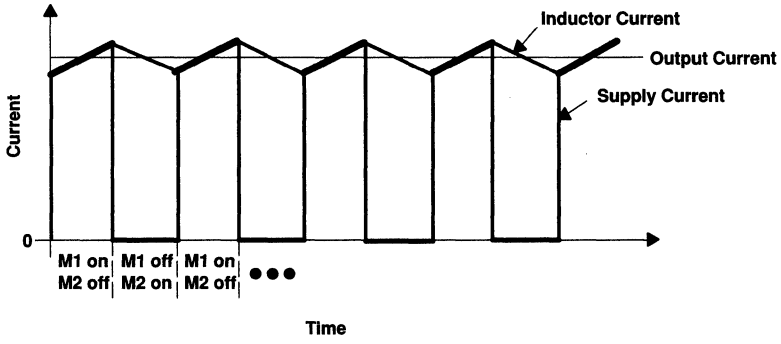


Figure 14. Class D Currents

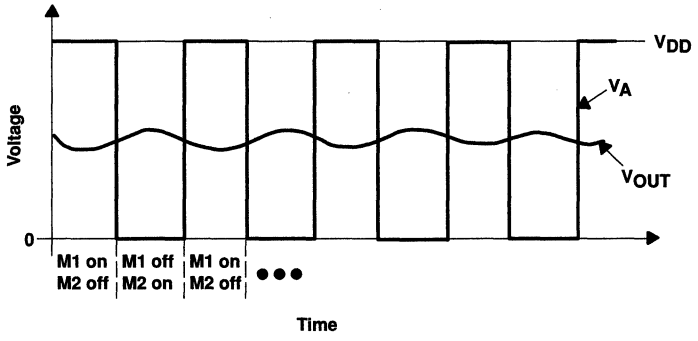


Figure 15. Class D Voltages

APPLICATION INFORMATION

the ideal class D amplifier (continued)

Given these plots, the efficiency of the class D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class D and linear amplifier and the efficiency is calculated.

CLASS D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average } (I_{DD}) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average } (I_{DD}) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}(I_{DD})$	$P_{SUP} = V_{DD} \times \text{Average}(I_{DD}) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 16.

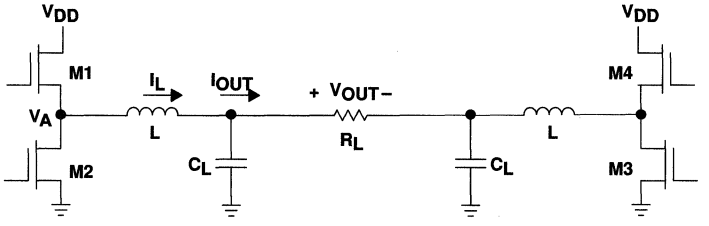


Figure 16. H-Bridge Class D Output Stage

APPLICATION INFORMATION

losses in a real-world class D amplifier

Losses make class D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $R_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $R_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is ON (saturated). Any $R_{DS(on)}$ above 0 Ω causes conduction loss. Figure 17 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

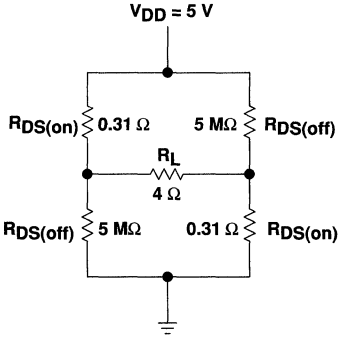


Figure 17. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2R_L}{I^2\,2R_{DS(on)} + I^2R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2R_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } R_{DS(on)} = 0.1,\ R_L = 4\right)$$

$$\text{Efficiency} = \eta = 87\% \left(\text{at all output levels } R_{DS(on)} = 0.31,\ R_L = 4\right)$$

APPLICATION INFORMATION

losses in a real-world class D amplifier (continued)

Losses due to rise and fall times are called switching losses. A plot of the output, showing switching losses, is shown in Figure 18.

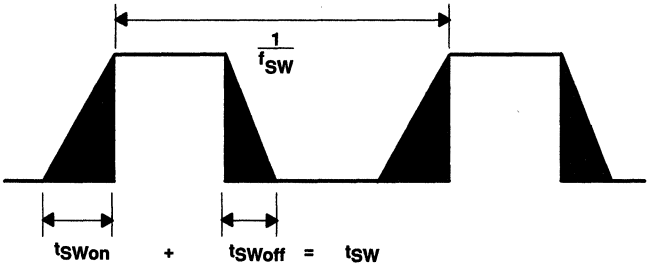


Figure 18. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 1-W per channel audio system with 8-Ω loads and a 5-V supply is almost 2.7 W. A similar linear amplifier such as the TPA005D02 has a maximum draw of 3.25 W under the same circumstances.

Table 3. Efficiency vs Output Power in 5-V 8-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	63.4	2	0.145
0.5	73	2.83	0.183
0.75	77.1	3.46	0.222
1	79.3	4	0.314
1.25	80.6	4.47†	0.3

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class D effect on power supply (continued)

There is a minor power supply savings with a class D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (Figure 19); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

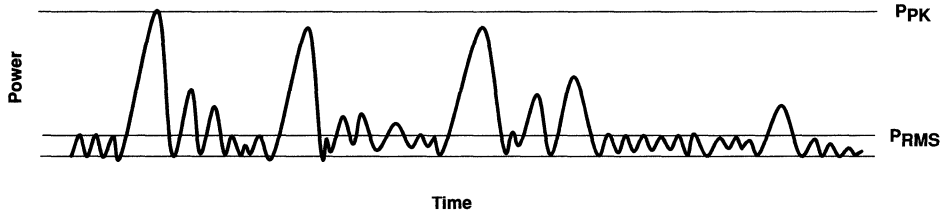


Figure 19. Audio Signal Showing Peak and RMS Power

Figure 20 is a comparison of a 5-V class D amplifier to a similar linear amplifier playing music that has a 13.76-dB crest factor. From the plot, the power supply draw from a stereo amplifier that is playing music with a 13.76 dB crest factor is 1.02 W, while a class D amplifier draws 420 mW under the same conditions. This means that just under 2.5 times the power supply is required for a linear amplifier over a class D amplifier.

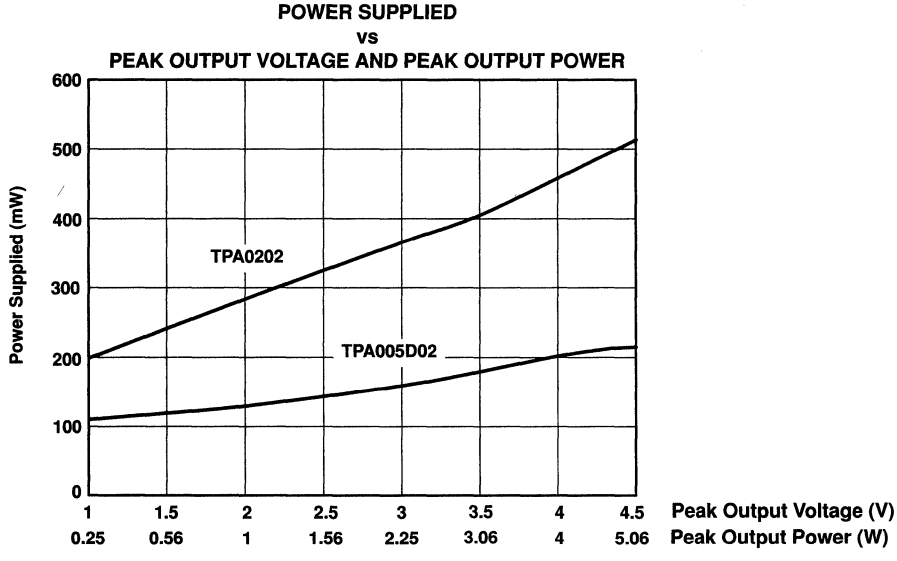


Figure 20. Audio Signal Showing Peak and RMS Power (with Music Applied)

APPLICATION INFORMATION

class D effect on battery life

Battery operations for class D amplifiers versus linear amplifiers have similar power supply savings results. The essential contributing factor to longer battery life is lower RMS supply current. Figure 21 compares the TPA005D02 supply current to the supply current of the TPA0202, a 2-W linear device, while playing music at different peak voltage levels.

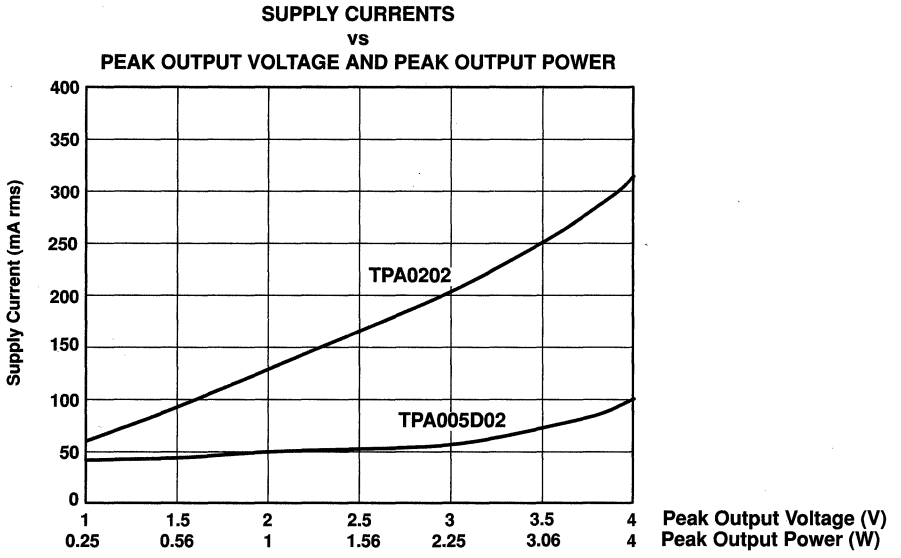


Figure 21. Supply Current vs Peak Output Voltage of TPA005D02 vs TPA0202 with Music Input

This plot shows that a linear amplifier has approximately three times more current draw at normal listening levels than a class D amplifier. Thus, a class D amplifier has approximately three times longer battery life at normal listening levels. If there is other circuitry in the system drawing supply current, that must also be taken into account when estimating battery life savings.

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA005D02 data sheet, one can see that when the TPA005D02 is operating from a 5-V supply into a 4-Ω speaker that 4 W peaks are available. Converting Watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4}{1}\right) = 6\text{ dB} \tag{17}$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{18}$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (12 dB crest factor)
= 500 mW (9 dB crest factor)
= 1000 mW (6 dB crest factor)
= 2000 mW (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA005D02 and maximum ambient temperatures is shown in Table 4.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA005D02 Power Rating, 5-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	0.56	125°C
4	1000 mW (6 dB)	0.30	136°C
4	500 mW (9 dB)	0.23	139°C
4	250 mW (12 dB)	0.20	141°C
4	120 mW (15 dB)	0.14	143°C
4	63 mW (18 dB)	0.09	146°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DCA	5.6 W	44.8 mW/°C	3.5 W	2.9 W

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \quad (19)$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA005D02 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (20)$$

$$= 150 - 22.3(0.14 \times 2) = 143°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(0.56 \times 2) = 125°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with a 15 dB crest factor per channel.

Table 4 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA005D02 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 59) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

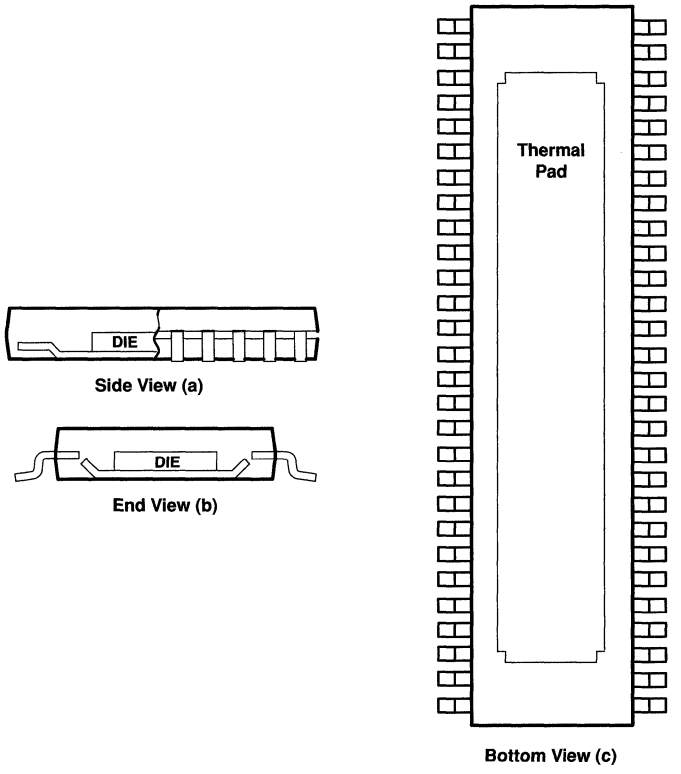
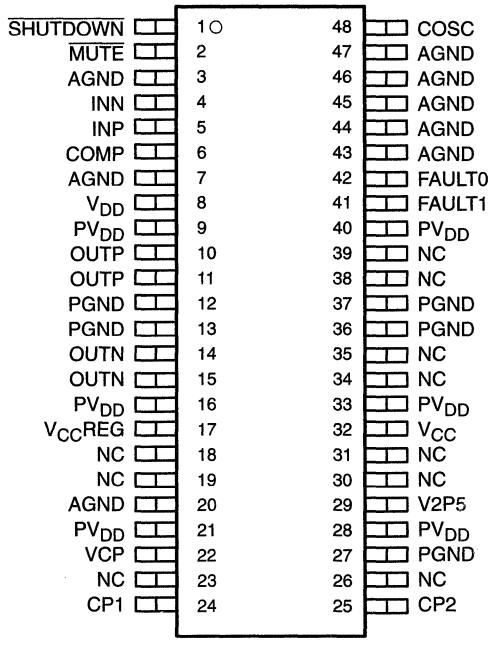


Figure 22. Views of Thermally Enhanced DCA Package

- **Extremely Efficient Class-D Mono Operation**
- **Drives Mono Speaker**
- **10-W BTL Output Into 4 Ω From 12 V**
- **32-W Peak Music Power**
- **Fully Specified for 12-V Operation**
- **Low Shutdown Current**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

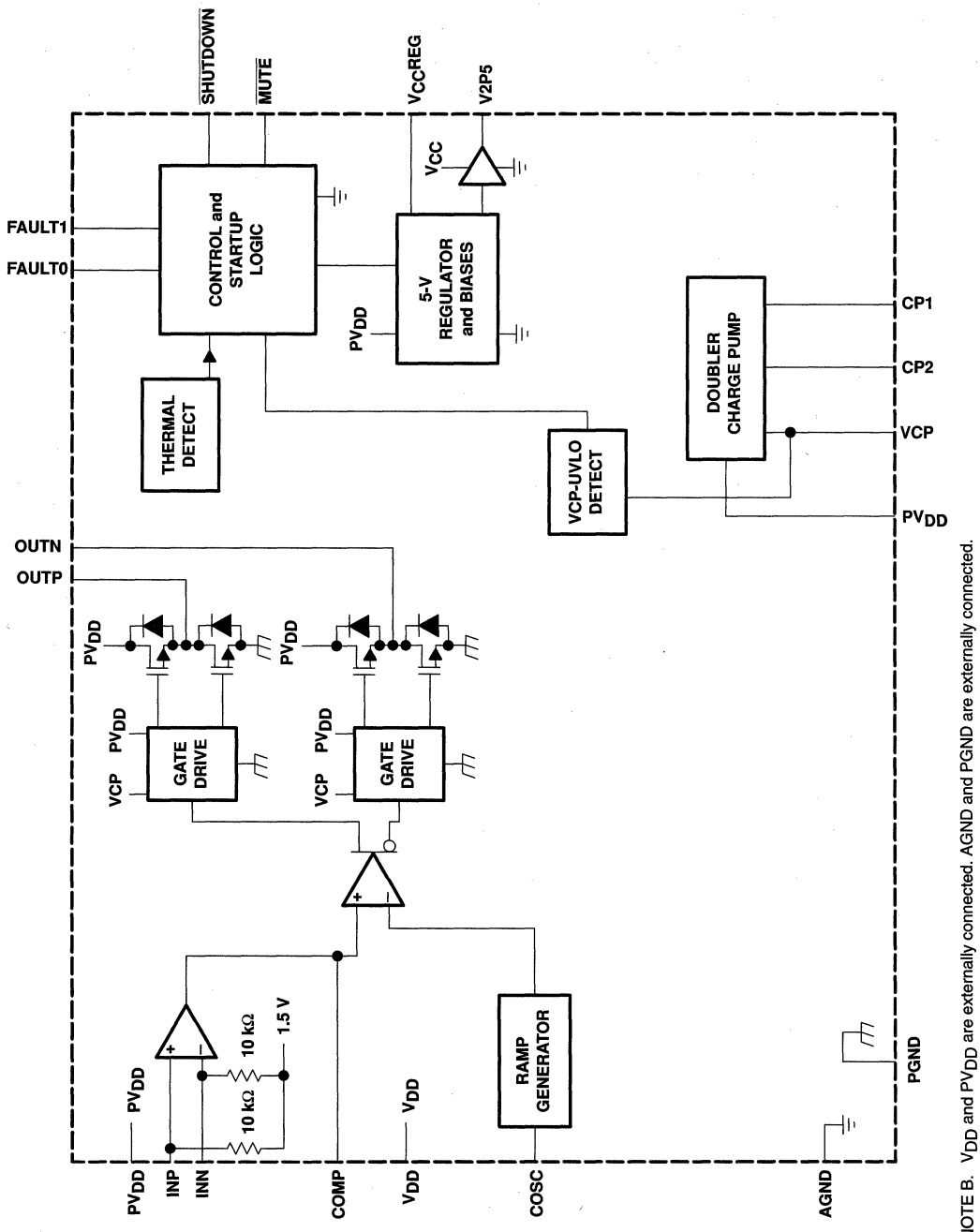
The TPA032D01 is a monolithic power IC mono audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA032D01 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 10 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 12-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control is provided to limit total supply current to 20 μA, making the device ideal for battery-powered applications.

The output stage is compatible with a range of power supplies from 8 V to 14 V. Protection circuitry is included to increase device reliability: thermal and under-voltage shutdown, with a status feedback terminal for use when any error condition is encountered.

The high switching frequency of the TPA032D01 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA032D01 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

schematic



NOTE B. V_{DD} and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 43, 44, 45, 46, 47	Analog ground for headphone and Class-D analog circuitry
COSC	48	Connect a capacitor from analog ground to this terminal to set the frequency of the ramp reference signal.
CP1	24	First diode node for charge pump
CP2	25	First inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
COMP	6	Compensation capacitor terminal for Class-D amplifier
INN	4	Class-D negative input
INP	5	Class-D positive input
OUTN	14, 15	Class-D amplifier negative output of H-bridge
OUTP	10, 11	Class-D amplifier positive output of H-bridge
PV_{DD}	9, 16	Class-D amplifier power supply
$\overline{MUTE}$	2	Active-low TTL logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held > high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	18, 19, 23, 26, 30, 31, 34, 35, 38, 39	Not connected
PGND	12, 13	Power ground for H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28, 33, 40	V_{DD} supply for charge-pump and gate drive circuitry
$\overline{SHUTDOWN}$	1	Active-low TTL logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held high, the device operates normally.
V2P5	29	2.5V internal reference bypass. This terminal requires a capacitor to ground.
V_{CC}	32	5V supply to circuitry. This terminal is typically connected to $V_{CC}REG$.
$V_{CC}REG$	17	5-V regulator output. This terminal requires a 1-μF capacitor to ground for stability reasons.
VCP	22	Connect a capacitor from this terminal to power ground to provide storage for the charge pump output voltage.
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0	FAULT 1	DESCRIPTION
1	1	No fault. The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. This is not a latched fault, however. FAULT1 is cleared by cycling $\overline{MUTE}$, $\overline{SHUTDOWN}$, or the power supply.
0	0	Thermal fault. All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes (not a latched fault). But the FAULTx terminals are still set and are cleared by cycling $\overline{MUTE}$, $\overline{SHUTDOWN}$, or the power supply.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA032D01DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA032D01DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)†

Supply voltage, (V_{DD}, PV_{DD}) ..... 14 V
Logic supply voltage, (V_{CC}) ..... 5.5 V
Input voltage, V_I ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$) ..... –0.3 V to 7 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Supply/load voltage, (FAULT0, FAULT1) ..... 7 V
Charge pump voltage, V_{CP} ..... PV_{DD} + 20 V
Continuous H-bridge output current (1 H-bridge conducting) ..... 3.5 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 7 A
Continuous V_{CC}REG output current, I_O (V_{CC}REG) ..... 150 mA
Continuous total power dissipation, T_C = 25°C ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 150°C
Operating case temperature range, T_C ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}	8		14	V
Logic supply voltage, V_{CC}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	–0.3		0.8	V
Audio inputs, LINN, LINP, RINN, RINP, differential input voltage			1	V_{RMS}
PWM frequency	100	250	500	kHZ

electrical characteristics Class-D amplifier, V_{DD} = PV_{DD} = 12 V, R_L = 4 Ω to 8 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = xPV_{DD} = 11 V to 13 V		–40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
$I_{DD(Mute)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	18	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		20	30	µA
$\|I_{IH}\|$	High-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IH} = 5.25 V			10	µA
$\|I_{IL}\|$	Low-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IL} = –0.3 V			10	µA
$r_{DS(on)}$	Static drain-to-source on-state resistance (high-side + low-side FETs)	I_{DD} = 0.5 A		720	800	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel		95%	98%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = 12 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	f = 1 kHz, THD = 0.5% Device soldered on PCB, See Note 2		10		W
	Efficiency	P_O = 10 W, f = 1 kHz		77%		
A_V	Gain			25		dB
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 23°C

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = 12 V, R_L = 8 Ω, T_A = 25°C, See Figure 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power,	THD = 0.5% Device soldered on PCB, See Note 2		7.5		W
	Efficiency	P_O = 7.5 W, f = 1 kHz		85%		
A_V	Gain			25		dB
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 85°C

operating characteristics, V_{CC} 5-V regulator, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V, I_O = 0 to 90 mA	4.5		5.5	V
I_{OS}	Short-circuit output current	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V†	90			mA

† Pulse width must be limited to prevent exceeding the maximum operating virtual junction temperature of 150°C.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			30		°C

PARAMETER MEASUREMENT INFORMATION

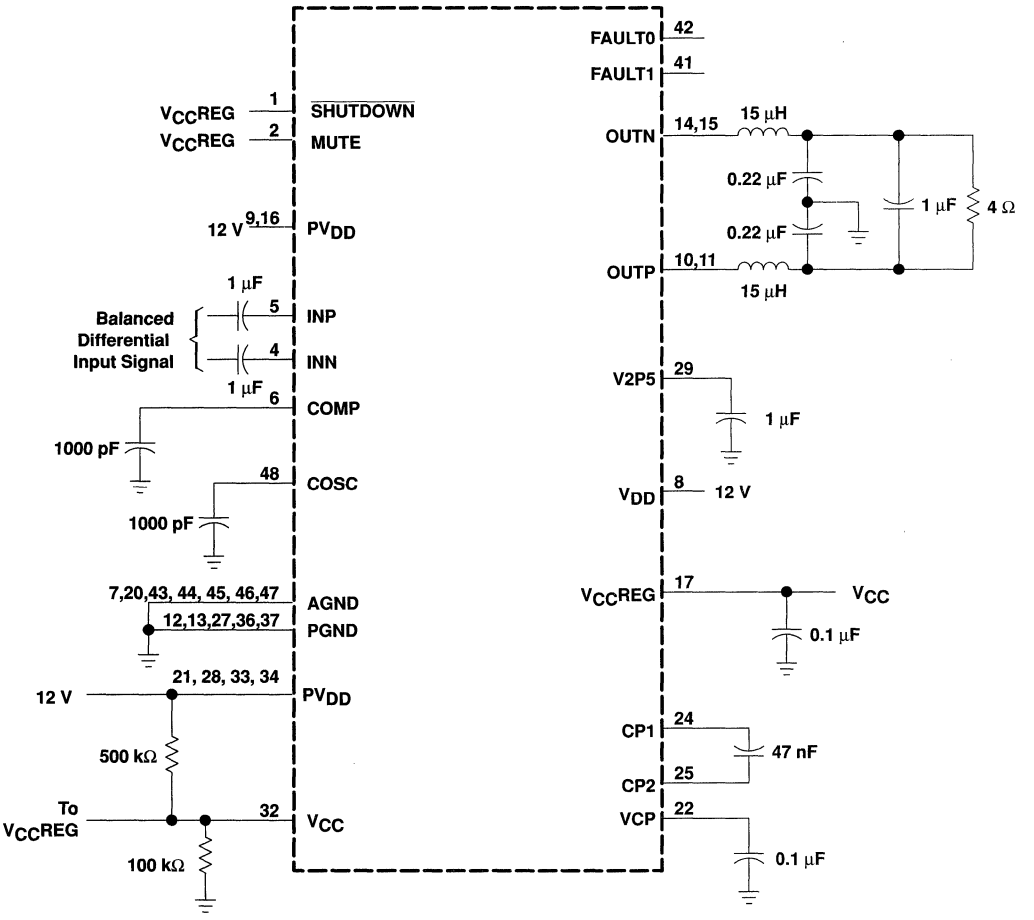


Figure 1. 12-V, 4-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

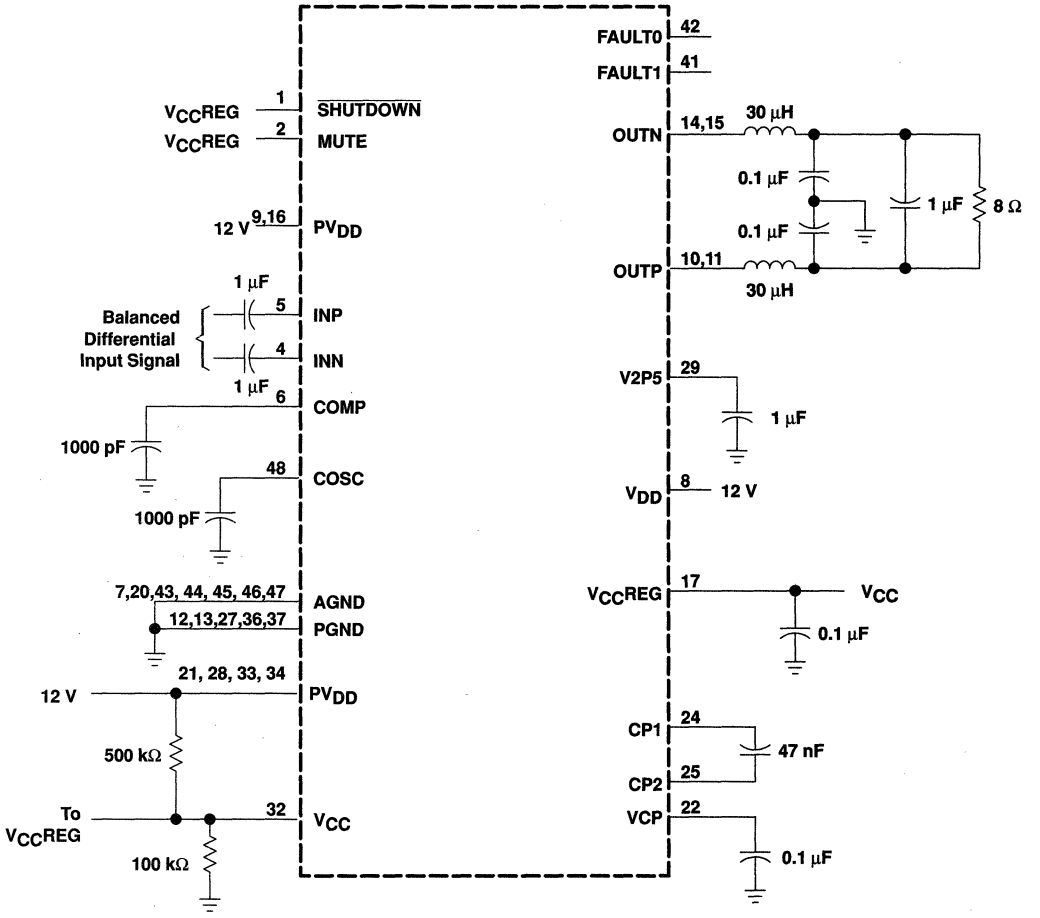
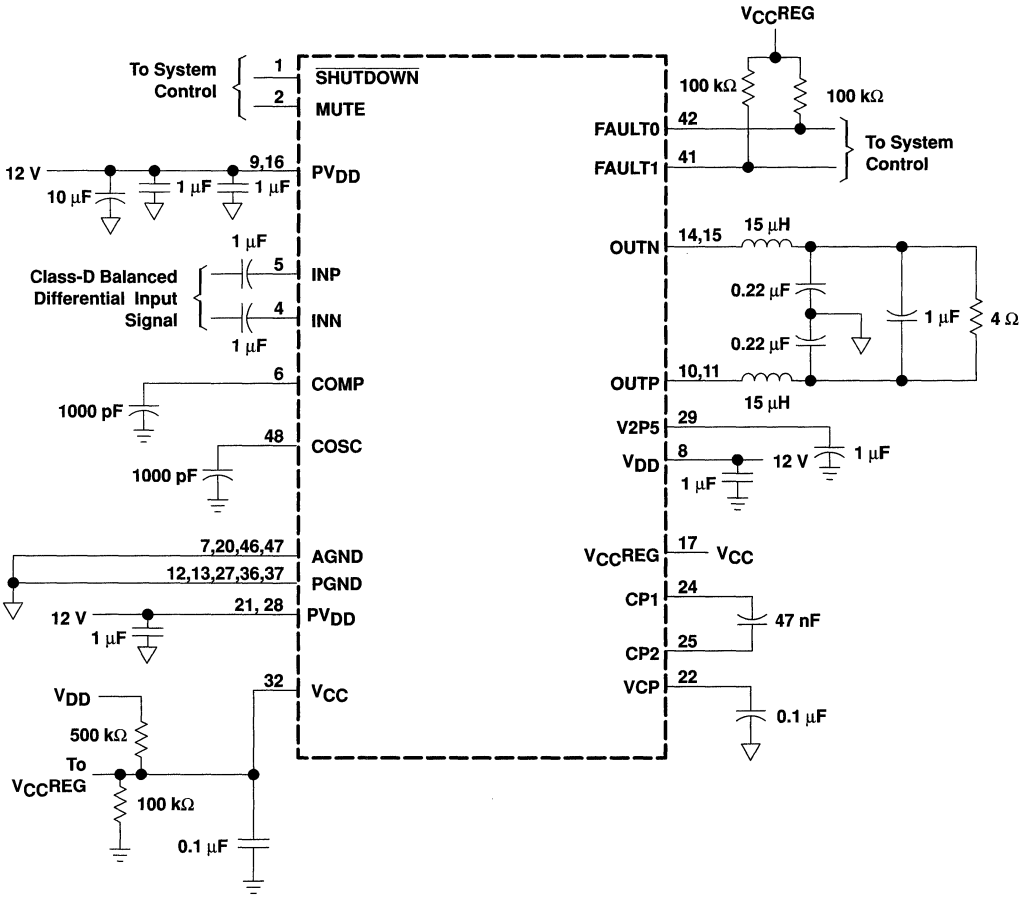


Figure 2. 12-V, 8-Ω Test Circuit

APPLICATION INFORMATION



NOTE A. ▽ = power ground and ⏚ = analog ground

Figure 3. TPA032D01 Typical Configuration Application Circuit

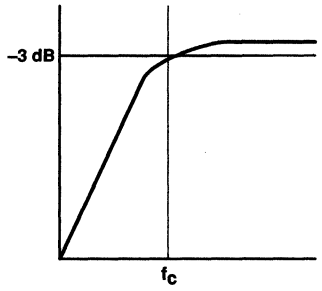
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and Z_I, the TPA032D01's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (8)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (9)$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input, as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA032D01 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor, which should be located physically close to the TPA032D01. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA032D01 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device's various V_{DD} leads, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

The TPA032D01 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA032D01 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of non-use for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 μA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low on-resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the on-resistance ($r_{DS(on)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (see Figure 4).

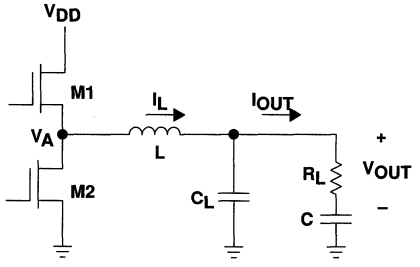


Figure 4. Half-Bridge Class-D Output Stage

Figures 5 and 6 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 4) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

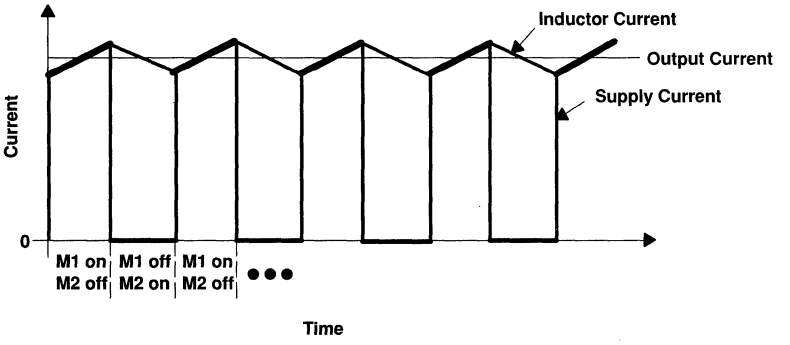


Figure 5. Class-D Currents

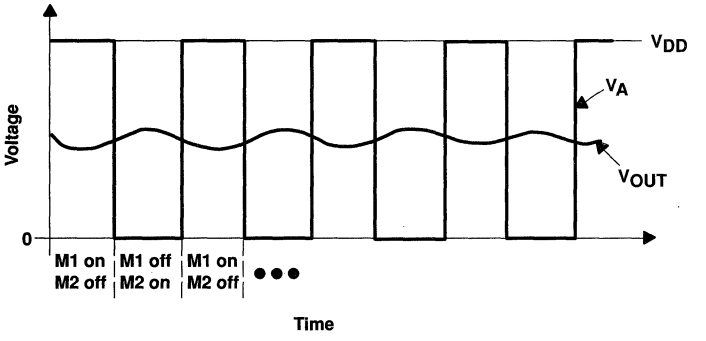


Figure 6. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average } (I_{DD}) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average } (I_{DD}) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}(I_{DD})$	$P_{SUP} = V_{DD} \times \text{Average}(I_{DD}) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 7.

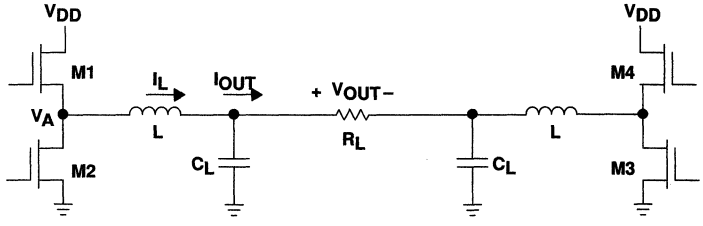


Figure 7. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is on (saturated). Any $r_{DS(on)}$ above 0 Ω causes conduction loss. Figure 8 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

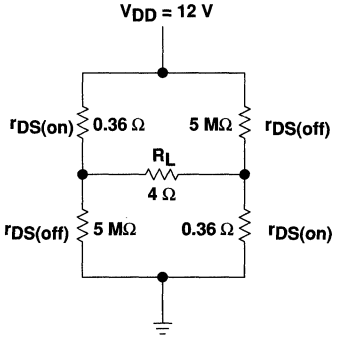


Figure 8. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2R_L}{I^2\,2r_{DS(on)} + I^2R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1\ \Omega,\ R_L = 4\ \Omega\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.36\ \Omega,\ R_L = 4\ \Omega\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A diagram of the output, showing switching losses, is shown in Figure 9.

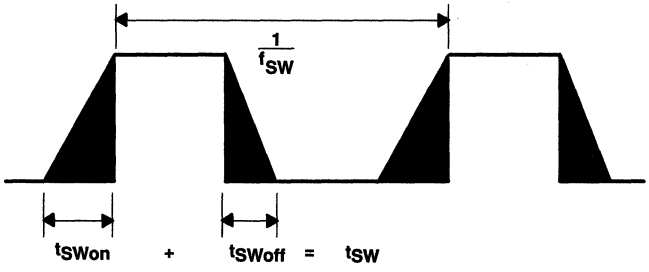


Figure 9. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 10-W per channel audio system with 4-Ω loads and a 12-V supply is almost 26 W. A similar linear amplifier such as the TPA032D01 has a maximum draw of greater than 50 W under the same circumstances.

Table 2. Efficiency vs Output Power in 12-V 4-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.5	41.7	2	0.35
2	66.7	4	0.5
5	75.1	6.32	0.83
8	78	8	1.13
10	77.9	8.94†	1.42

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (see Figure 10); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

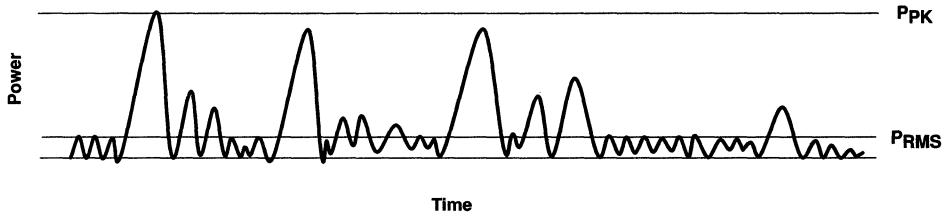


Figure 10. Audio Signal Showing Peak and RMS Power

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA032D01 data sheet, one can see that when the TPA032D01 is operating from a 12-V supply into a 4-Ω speaker that 20-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{20}{1}\right) = 6 \text{ dB} \quad (17)$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (18)$$

= 315 mW (18 dB crest factor)
= 630 mW (15 dB crest factor)
= 1.25 W (12 dB crest factor)
= 2.5 W (9 dB crest factor)
= 5 W (6 dB crest factor)
= 10 W (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 10 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, the internal dissipation in the TPA032D01 and maximum ambient temperatures are shown in Table 3.

crest factor and thermal considerations (continued)

Table 3. TPA032D01 Power Rating, 12-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
20	10 W (3 dB)	2.84	87°C
20	5 W (6 dB)	1.66	113°C
20	2.5 W (9 dB)	1.12	125°C
20	1.25 W (12 dB)	0.87	125°C
20	630 mW (15 dB)	0.7	125°C
20	315 mW (18 dB)	0.6	125°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA032D01 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{20}$$

$$= 150 - 22.3(0.35) = 125°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(1.42) = 118°C \text{ (3dB crest factor)}$$

(Maximum recommended case temperature is 125°C)

NOTE:
Internal dissipation of 0.7 W is estimated for a 10-W system with a 15 dB crest factor per channel.

The TPA032D01 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 11) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

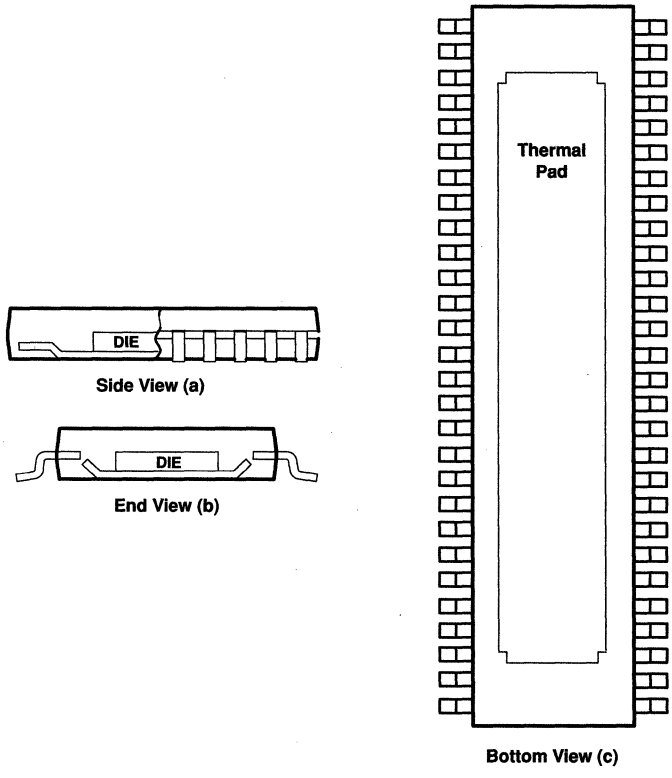
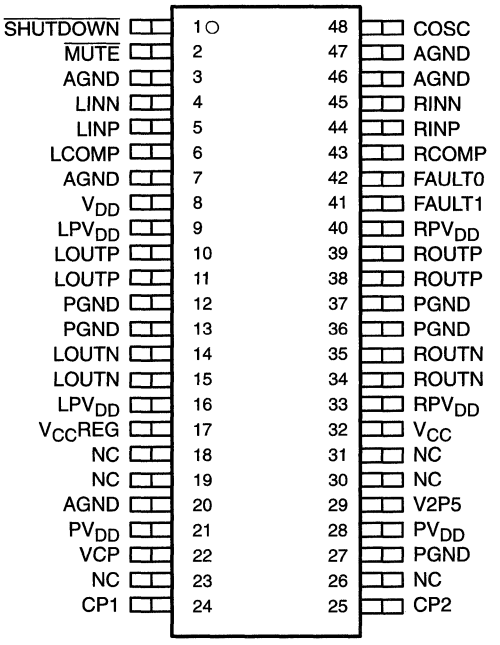


Figure 11. Views of Thermally Enhanced DCA Package

- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **10-W BTL Output Into 4 Ω From 12 V**
- **32-W Peak Music Power**
- **Fully Specified for 12-V Operation**
- **Low Shutdown Current**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

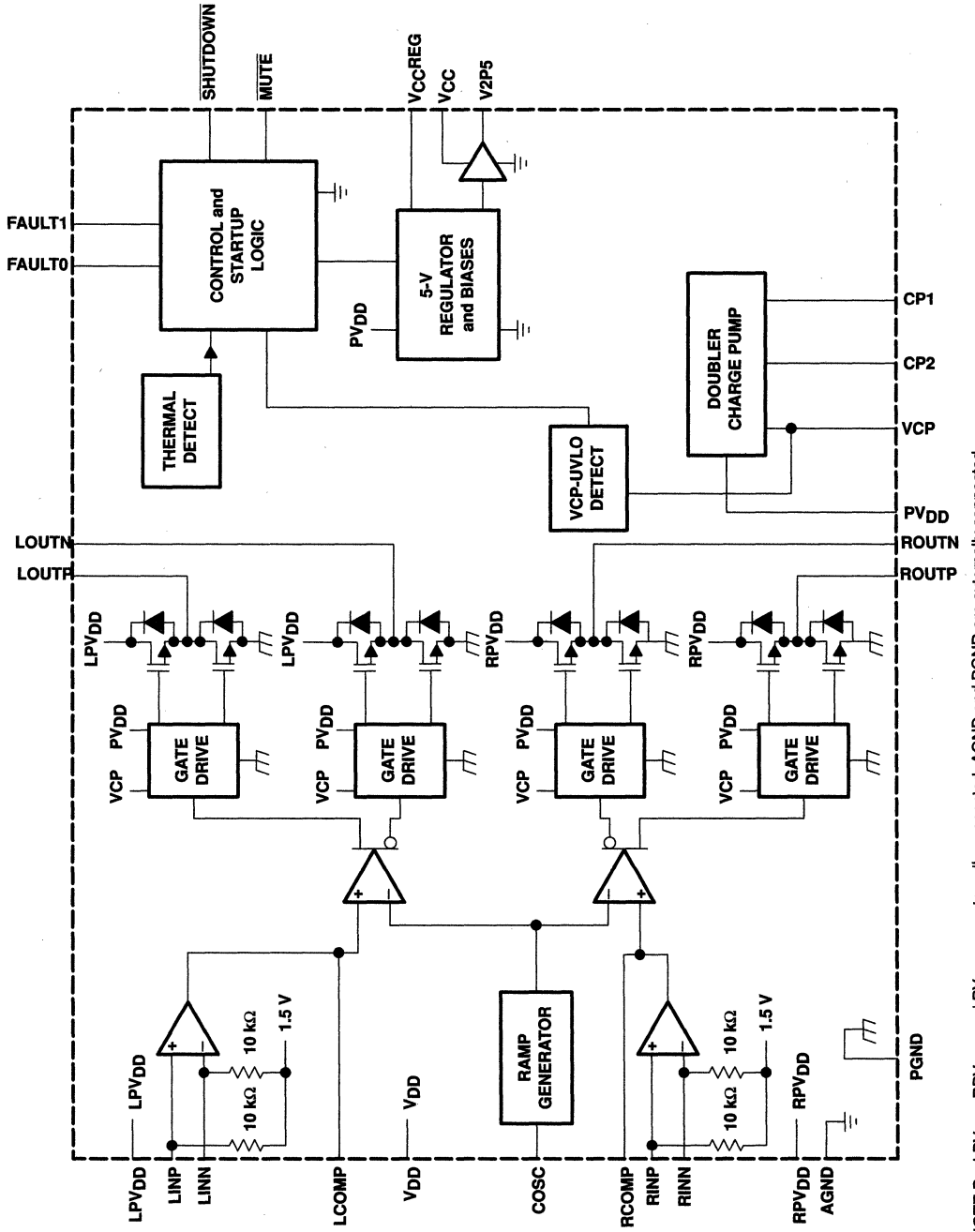
The TPA032D02 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA032D02 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 10 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 12-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control is provided to limit total supply current to 20 μA, making the device ideal for battery-powered applications.

The output stage is compatible with a range of power supplies from 8 V to 14 V. Protection circuitry is included to increase device reliability: thermal and under-voltage shutdown, with a status feedback terminal for use when any error condition is encountered.

The high switching frequency of the TPA032D02 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA032D02 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

schematic



NOTE B. LPV_{DD}, RPV_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 46, 47	Analog ground for Class-D analog circuitry
COSC	48	Connect a capacitor from analog ground to this terminal to set the frequency of the ramp reference signal.
CP1	24	First diode node for charge pump
CP2	25	First inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
$\overline{MUTE}$	2	Active-low TTL logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held > high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	18, 19, 23, 26, 30, 31	No connection
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28	V_{DD} supply for charge-pump and gate drive circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low TTL logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held high, the device operates normally.
V_{CC}	32	5V supply to logic. This terminal is typically connected to $V_{CC}REG$.
$V_{CC}REG$	17	5-V regulator output. This terminal requires a 1-μF capacitor to ground for stability reasons.
V2P5	29	2.5V internal reference bypass. This terminal requires a capacitor to ground.
VCP	22	Connect a capacitor from this terminal to power ground to provide storage for the charge pump output voltage.
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0	FAULT 1	DESCRIPTION
1	1	No fault. The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. This is not a latched fault, however. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault. All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes (not a latched fault). But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA032D02DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA032D02DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)†

Supply voltage, (V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}) ..... 14 V
Logic supply voltage, (V_{CC}) ..... 5.5 V
Input voltage, V_I ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$) ..... −0.3 V to 7 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Supply/load voltage, (FAULT0, FAULT1) ..... 7 V
Charge pump voltage, V_{CP} ..... PV_{DD} + 20 V
Continuous H-bridge output current (1 H-bridge conducting) ..... 3.5 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 7 A
Continuous V_{CC}REG output current, I_O (V_{CC}REG) ..... 150 mA
Continuous total power dissipation, T_C = 25°C ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Operating case temperature range, T_C ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}	8		14	V
Logic supply voltage, V_{CC}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	−0.3		0.8	V
Audio inputs, LINN, LINP, RINN, RINP, differential input voltage			1	V_{RMS}
PWM frequency	100	250	500	kHZ

electrical characteristics Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω to 8 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = xPV_{DD} = 11 V to 13 V		–40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
$I_{DD(Mute)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	18	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		20	30	µA
$\|I_{IH}\|$	High-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IH} = 5.25 V			10	µA
$\|I_{IL}\|$	Low-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IL} = –0.3 V			10	µA
$r_{DS(on)}$	Static drain-to-source on-state resistance (high-side + low-side FETs)	I_{DD} = 0.5 A		720	800	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel		95%	98%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	f = 1 kHz, THD = 0.5%, per channel, Device soldered on PCB, See Note 2		10		W
	Efficiency	P_O = 10 W, f = 1 kHz		77%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 23°C

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 8 Ω, T_A = 25°C, See Figure 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power,	THD = 0.5%, per channel, Device soldered on PCB, See Note 2		7.5		W
	Efficiency	P_O = 7.5 W, f = 1 kHz		85%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 85°C

operating characteristics, V_{CC} 5-V regulator, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V, I_O = 0 to 90 mA	4.5		5.5	V
I_{OS}	Short-circuit output current	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V†	90			mA

† Pulse width must be limited to prevent exceeding the maximum operating virtual junction temperature of 150°C.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			30		°C

PARAMETER MEASUREMENT INFORMATION

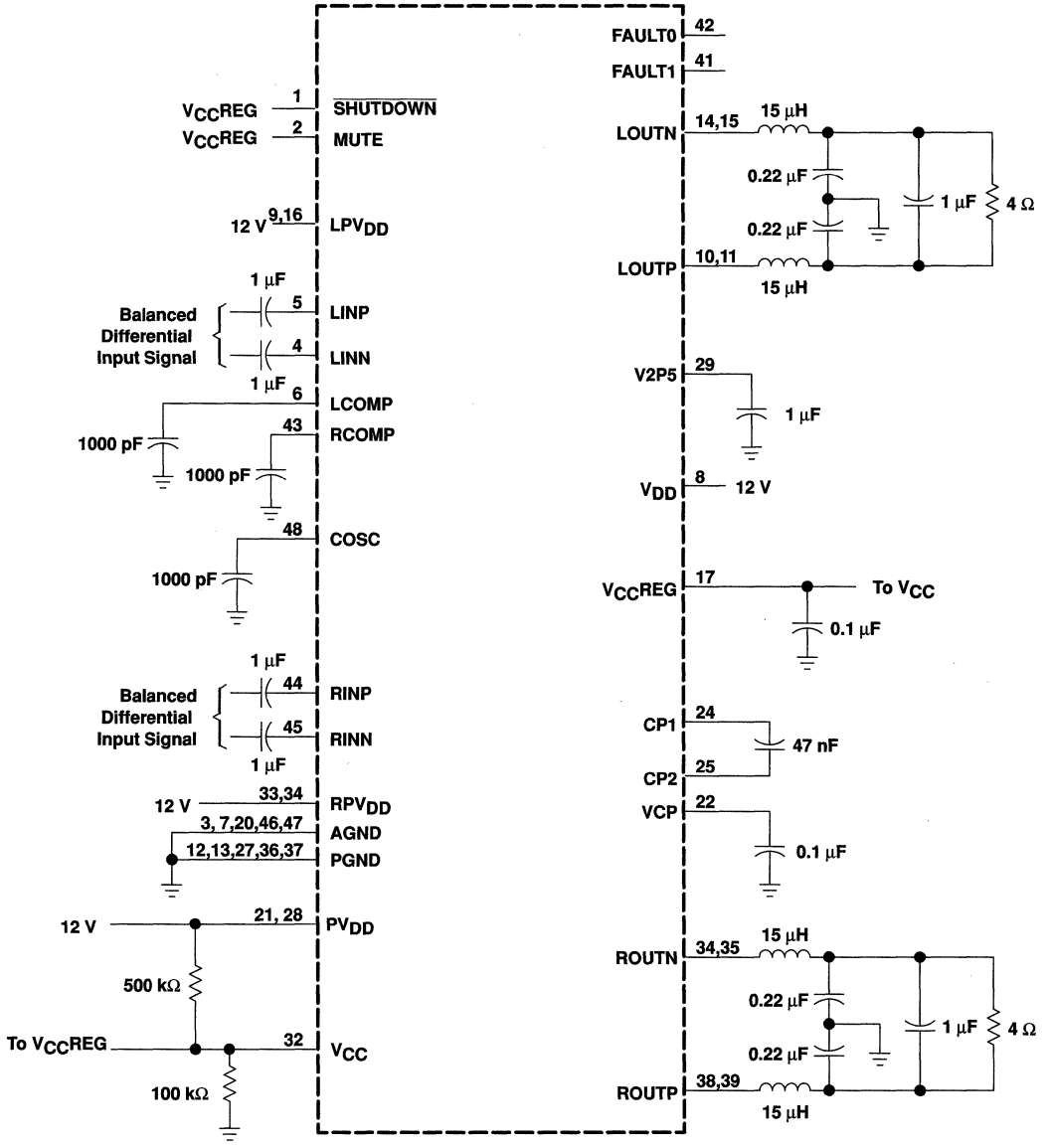


Figure 1. 12-V, 4-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

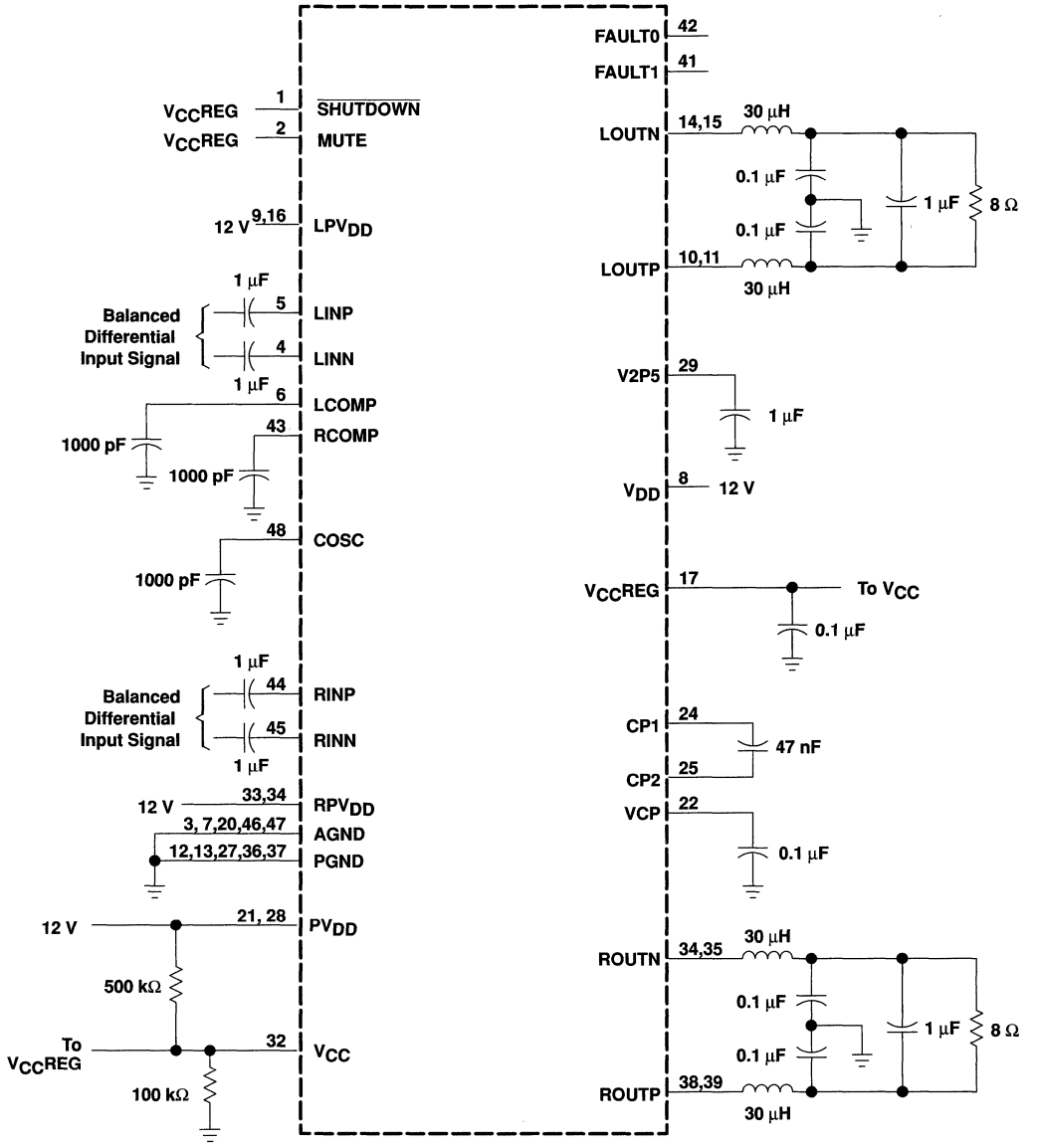
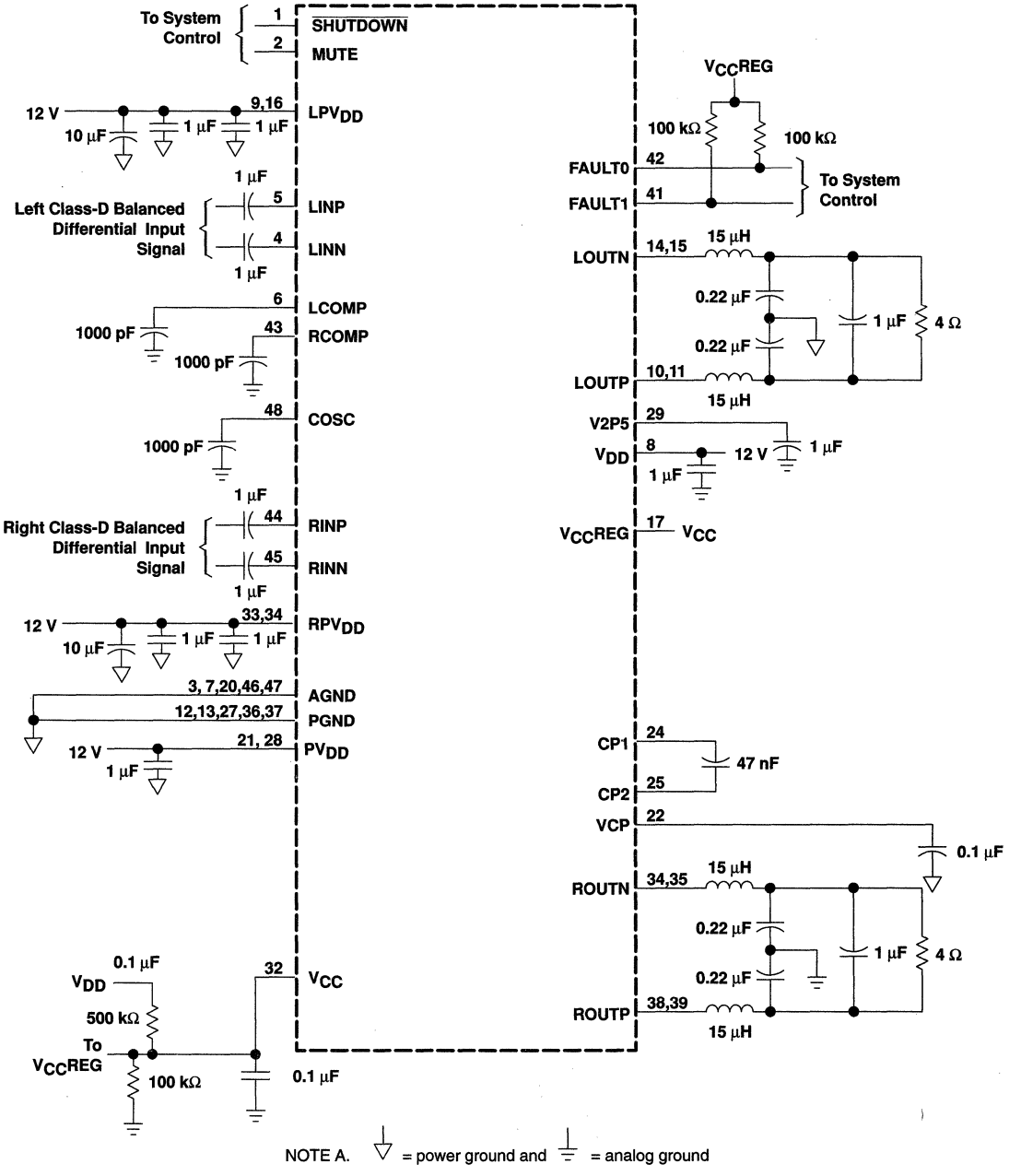


Figure 2. 12-V, 8-Ω Test Circuit

APPLICATION INFORMATION



NOTE A. ▽ = power ground and ⏚ = analog ground

Figure 3. TPA032D02 Typical Configuration Application Circuit

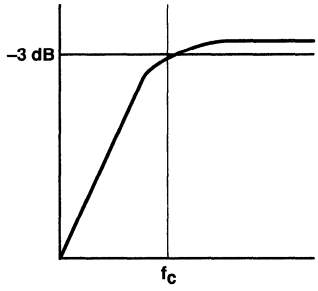
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and Z_I, the TPA032D02's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (8)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input, as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA032D02 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor, which should be located physically close to the TPA032D02. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA032D02 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA032D02 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA032D02 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of non-use for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 µA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low on-resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the on-resistance ($r_{DS(on)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (see Figure 4).

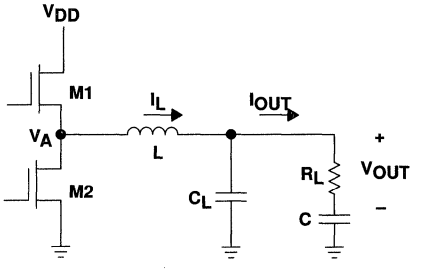


Figure 4. Half-Bridge Class-D Output Stage

Figures 5 and 6 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 4) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

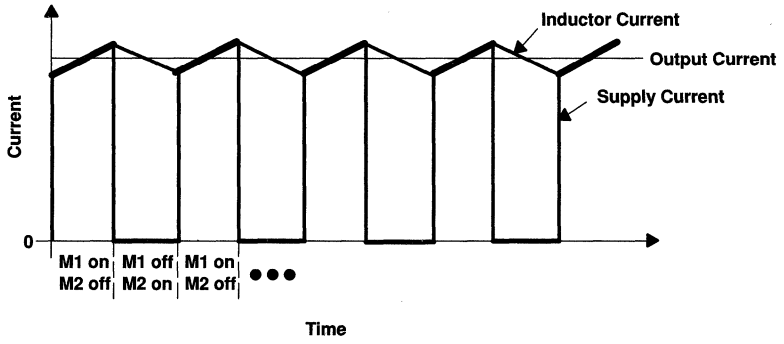


Figure 5. Class-D Currents

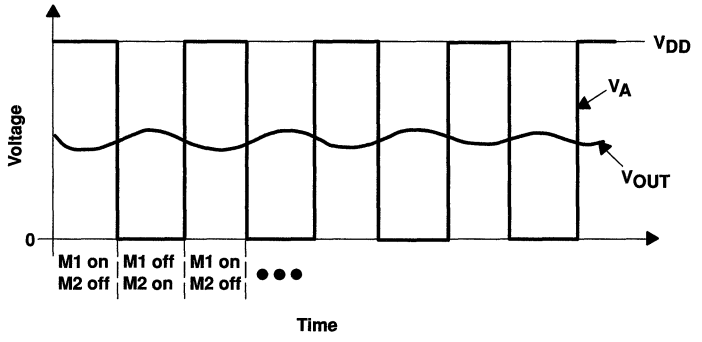


Figure 6. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average}\left(I_{DD}\right) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average}\left(I_{DD}\right) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right)$	$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 7.

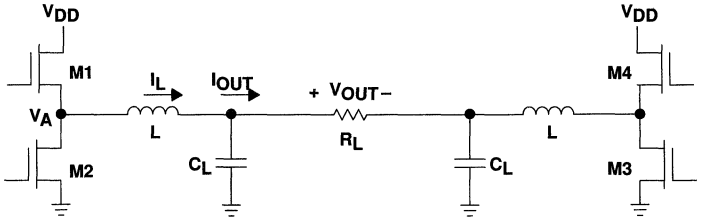


Figure 7. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is on (saturated). Any $r_{DS(on)}$ above 0 Ω causes conduction loss. Figure 8 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

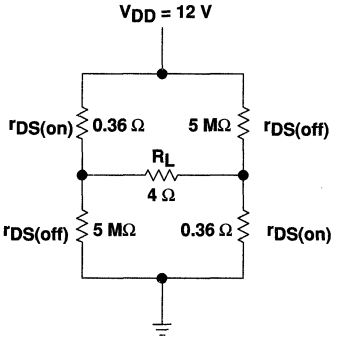


Figure 8. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2R_L}{I^2\,2r_{DS(on)} + I^2R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1\ \Omega,\ R_L = 4\ \Omega\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.36\ \Omega,\ R_L = 4\ \Omega\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A diagram of the output, showing switching losses, is shown in Figure 9.

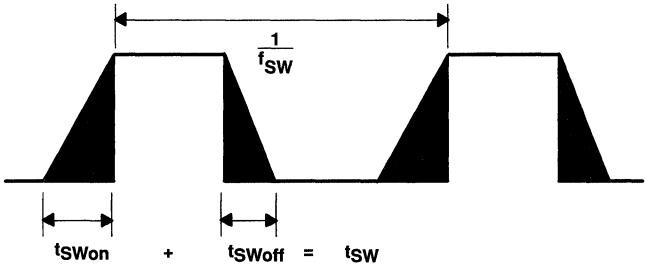


Figure 9. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 10-W per channel audio system with 4-Ω loads and a 12-V supply is almost 26 W. A similar linear amplifier such as the TPA032D02 has a maximum draw of greater than 50 W under the same circumstances.

Table 2. Efficiency vs Output Power in 12-V 4-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.5	41.7	2	0.7
2	66.7	4	1.0
5	75.1	6.32	1.66
8	78	8	2.26
10	77.9	8.94†	2.84

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (see Figure 10); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

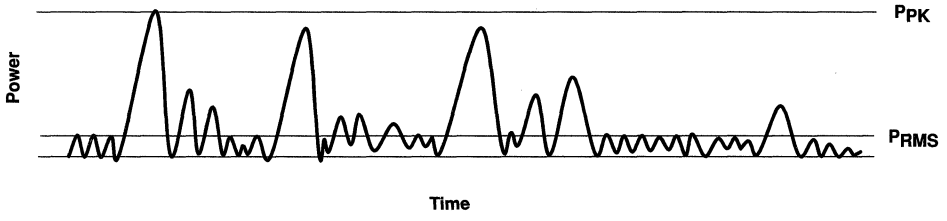


Figure 10. Audio Signal Showing Peak and RMS Power

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA032D02 data sheet, one can see that when the TPA032D02 is operating from a 12-V supply into a 4-Ω speaker that 20-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{20}{1}\right) = 6\ \text{dB} \tag{17}$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{18}$$

= 315 mW (18 dB crest factor)
= 630 mW (15 dB crest factor)
= 1.25 W (12 dB crest factor)
= 2.5 W (9 dB crest factor)
= 5 W (6 dB crest factor)
= 10 W (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 10 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, the internal dissipation in the TPA032D02 and maximum ambient temperatures are shown in Table 3.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 3. TPA032D02 Power Rating, 12-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
20	10 W (3 dB)	2.84	23°C
20	5 W (6 dB)	1.66	75°C
20	2.5 W (9 dB)	1.12	100°C
20	1.25 W (12 dB)	0.87	111°C
20	630 mW (15 dB)	0.7	118°C
20	315 mW (18 dB)	0.6	123°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA032D02 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{20}$$

$$= 150 - 22.3(0.7 \times 2) = 118°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(2.84 \times 2) = 23°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 1.4 W is estimated for a 10-W system with a 15 dB crest factor per channel.

The TPA032D02 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 11) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

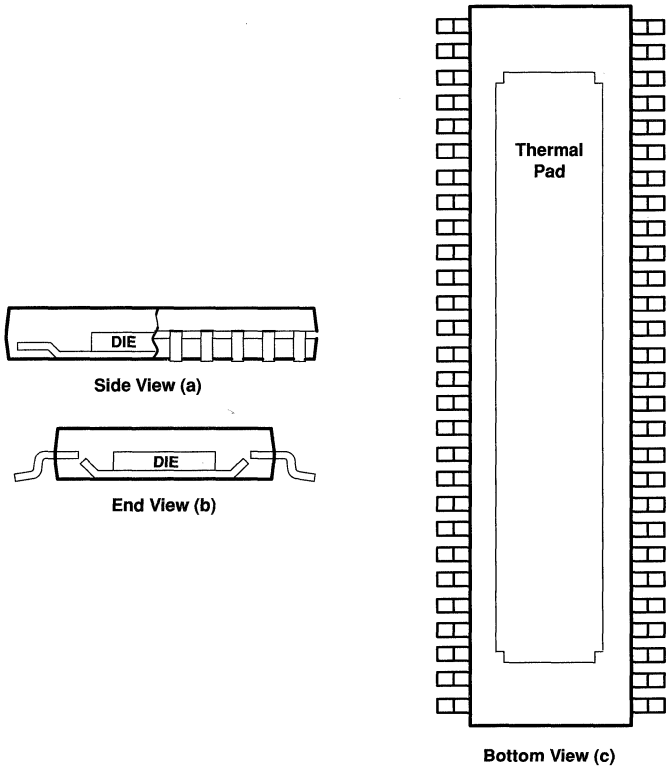
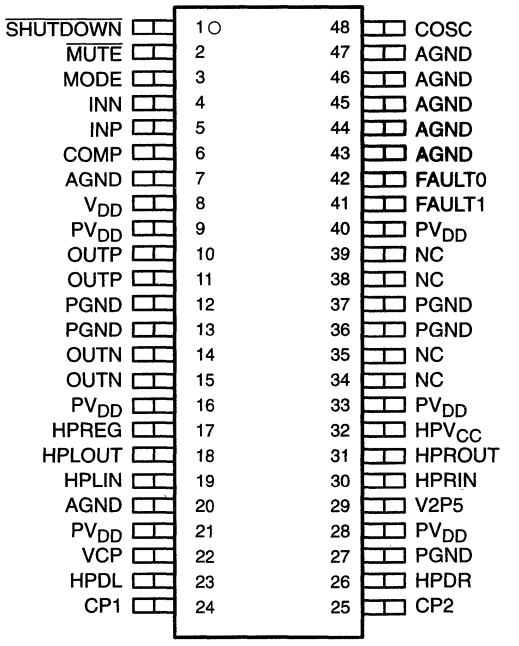


Figure 11. Views of Thermally Enhanced DCA Package

- **Extremely Efficient Class-D Mono Operation**
- **Drives Mono Speaker, Plus Stereo Headphones**
- **10-W BTL Output Into 4 Ω From 12 V**
- **32-W Peak Music Power**
- **Fully Specified for 12-V Operation**
- **Low Shutdown Current**
- **Class-AB Headphone Amplifier**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

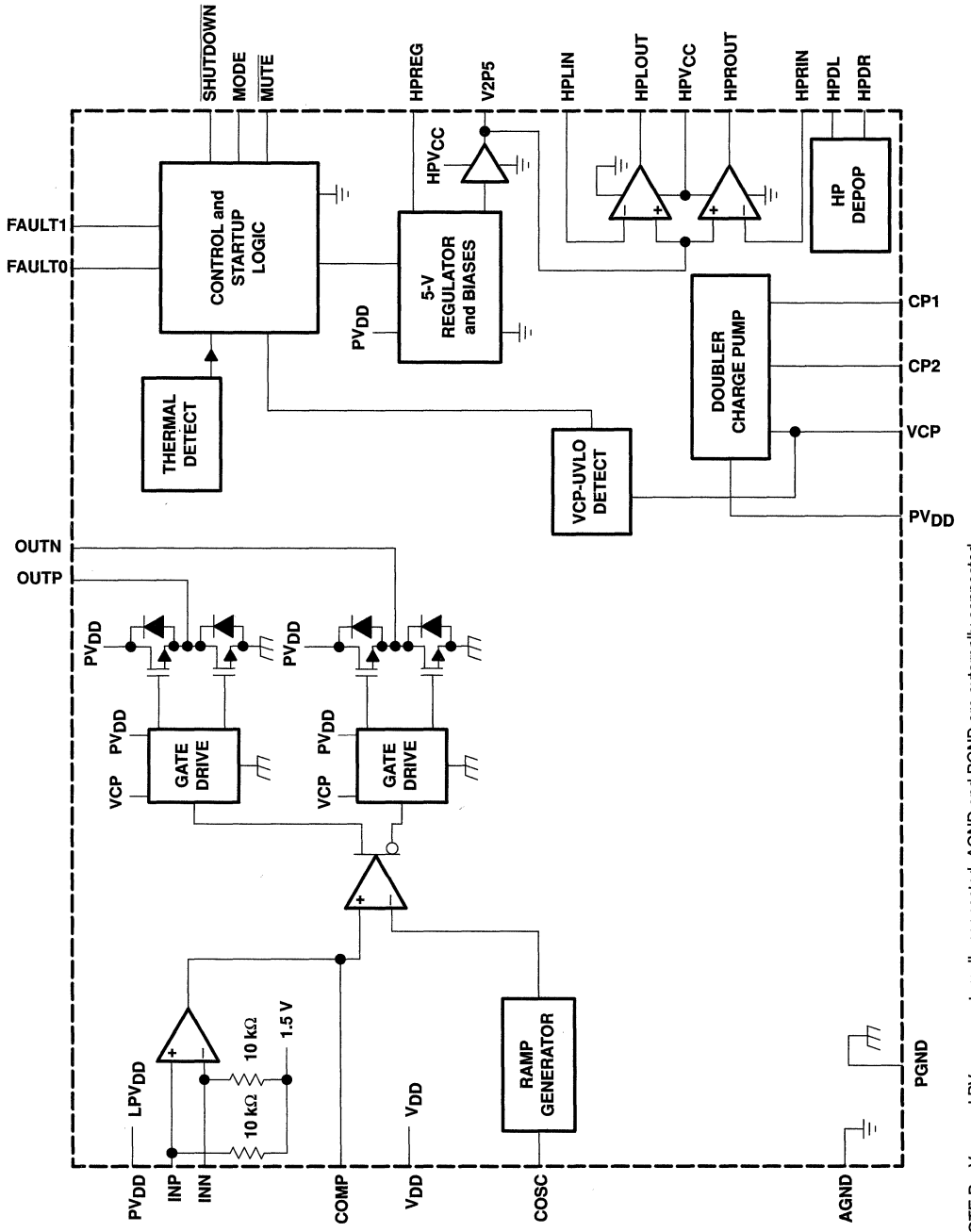
The TPA032D03 is a monolithic power IC mono audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA032D03 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 10 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 12-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. Included is a Class-AB headphone amplifier with interface logic to select between the two modes of operation. Only one amplifier is active at any given time, and the other is in power-saving sleep mode. Also, a chip-level shutdown control is provided to limit total supply current to 20 μA, making the device ideal for battery-powered applications.

The output stage is compatible with a range of power supplies from 8 V to 14 V. Protection circuitry is included to increase device reliability: thermal and under-voltage shutdown, with a status feedback terminal for use when any error condition is encountered.

The high switching frequency of the TPA032D03 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA032D03 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

schematic



NOTE B. V_{DD} and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	7, 20, 43, 44, 45, 46, 47	Analog ground for headphone and Class-D analog sections
COMP	6	Compensation capacitor terminal for Class-D amplifier
COSC	48	Connect a capacitor from analog ground to this terminal to set the frequency of the ramp reference signal.
CP1	24	First diode node for charge pump
CP2	25	First inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
HPDL	23	Depop control for left headphone
HPDR	26	Depop control for right headphone
HPLIN	19	Headphone amplifier left input
HPLOUT	18	Headphone amplifier left output
HPREG	17	5-V regulator output. This terminal requires a 1-μF capacitor to ground for stability reasons.
HPRIN	30	Headphone amplifier right input
HPROUT	31	Headphone amplifier right output
HPV_{CC}	32	5V supply to headphone amplifier and logic. This terminal is typically connected to HPREG.
INN	4	Class-D negative input
INP	5	Class-D positive input
MODE	3	TTL logic-level mode input signal. When MODE is held low, the main Class-D amplifier is active. When MODE is held > high, the head phone amplifier is active.
$\overline{\text{MUTE}}$	2	Active-low TTL logic-level mute input signal. When $\overline{\text{MUTE}}$ is held low, the selected amplifier is muted. When $\overline{\text{MUTE}}$ is held > high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	34, 35, 38, 39	No connection
OUTN	14, 15	Class-D amplifier negative output of H-bridge
OUTP	10, 11	Class-D amplifier positive output of H-bridge
PGND	12, 13	Power ground for H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for H-bridge only
PV_{DD}	9, 16, 21, 28, 33, 40	V_{DD} supply for charge-pump, headphone regulator, Class-D amplifier, and gate drive circuitry
$\overline{\text{SHUTDOWN}}$	1	Active-low TTL logic-level shutdown input signal. When $\overline{\text{SHUTDOWN}}$ is held low, the device goes into shutdown mode. When $\overline{\text{SHUTDOWN}}$ is held high, the device operates normally.
V2P5	29	2.5V internal reference bypass. This terminal requires a capacitor to ground.
VCP	22	Connect a capacitor from this terminal to power ground to provide storage for the charge pump output voltage.
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0	FAULT 1	DESCRIPTION
1	1	No fault. The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. This is not a latched fault, however. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault. All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes (not a latched fault). But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

headphone amplifier faults

The thermal fault remains active when the device is in head phone mode. This fault operation has exactly the same as it does for the Class-D amplifier (see Table 1).

If HPV_{CC} drops below approximately 4.5 V, the head phone is disabled. Once HPV_{CC} exceeds approximately 4.5 V, the head phone amplifier is re-enabled. No fault is reported to the user.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA032D03DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA032D03DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)†

Supply voltage, (V_{DD}, PV_{DD}) ..... 14 V
Headphone supply voltage, (HPV_{CC}) ..... 5.5 V
Input voltage, V_I ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$) ..... –0.3 V to 7 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Supply/load voltage, (FAULT0, FAULT1) ..... 7 V
Charge pump voltage, V_{CP} ..... PV_{DD} + 20 V
Continuous H-bridge output current (1 H-bridge conducting) ..... 3.5 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 7 A
Continuous HPREG output current, I_O (HPREG) ..... 150 mA
Continuous total power dissipation, T_C = 25°C ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 150°C
Operating case temperature range, T_C ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}	8		14	V
Headphone supply voltage, HPV_{CC}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	–0.3		0.8	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	100	250	500	kHZ

electrical characteristics Class-D amplifier, V_{DD} = PV_{DD} = 12 V, R_L = 4 Ω to 8 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = 11 V to 13 V		–40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
$I_{DD(Mute)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	18	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		20	30	µA
$\|I_{IH}\|$	High-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IH} = 5.25 V			10	µA
$\|I_{IL}\|$	Low-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IL} = –0.3 V			10	µA
$r_{DS(on)}$	Static drain-to-source on-state resistance (high-side + low-side FETs)	I_{DD} = 0.5 A		720	800	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel		95%	98%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = 12 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	f = 1 kHz, THD = 0.5%, Device soldered on PCB, See Note 2		10		W
	Efficiency	P_O = 10 W, f = 1 kHz		77%		
A_V	Gain			25		dB
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 23°C

operating characteristics, Class-D amplifier, $V_{DD} = PV_{DD} = 12$ V, $R_L = 8\ \Omega$, $T_A = 25°C$, See Figure 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power,	THD = 0.5% Device soldered on PCB, See Note 2		7.5		W
	Efficiency	P_O = 7.5 W, f = 1 kHz		85%		
A_V	Gain			25		dB
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, $T_A = 85°C$

electrical characteristics, headphone amplifier, $HPV_{CC} = 5$ V, $R_L = 32\ \Omega$, $T_A = 25°C$, See Figure 3 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio			–60		dB
	Uncompensated gain range		–1		–10	V/V
I_{DD}	Supply current			9	12	mA
$I_{DD(MUTE)}$	Supply current, mute mode			9	12	mA
$I_{DD(S/D)}$	Supply current, shutdown mode			20	30	μA

operating characteristics, headphone amplifier, $HPV_{CC} = 5$V, $R_L = 32\ \Omega$, gain set at –10V/V, $T_A = 25°C$, See Figure 3 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%, f = 1 kHz		50		mW
	Crosstalk	f = 1 kHz		–60		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20	kHz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			>1		MΩ

operating characteristics, HPREG 5-V regulator, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD}$ = 8 V to 14 V, I_O = 0 to 90 mA	4.5		5.5	V
I_{OS}	Short-circuit output current	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD}$ = 8 V to 14 V†	90			mA

† Pulse width must be limited to prevent exceeding the maximum operating virtual junction temperature of 150°C.

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			30		°C

PARAMETER MEASUREMENT INFORMATION

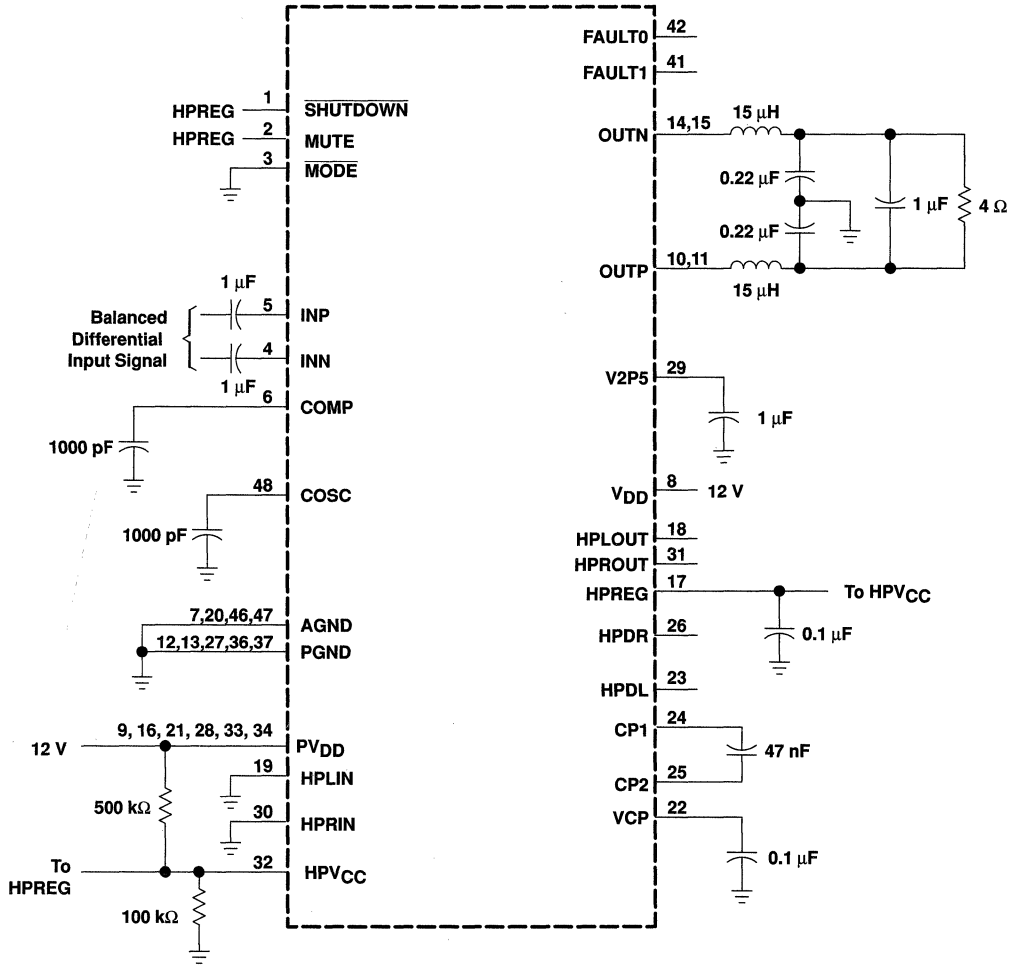


Figure 1. 12-V, 4-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

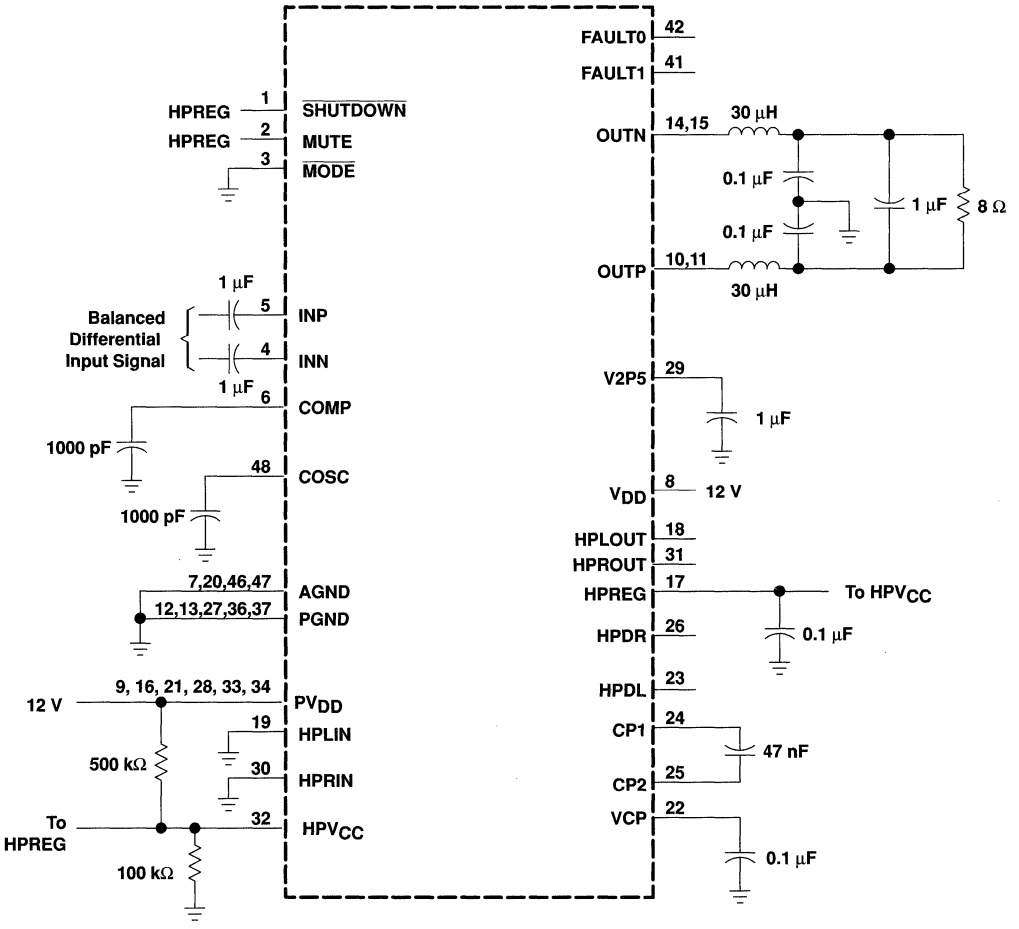


Figure 2. 12-V, 8-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

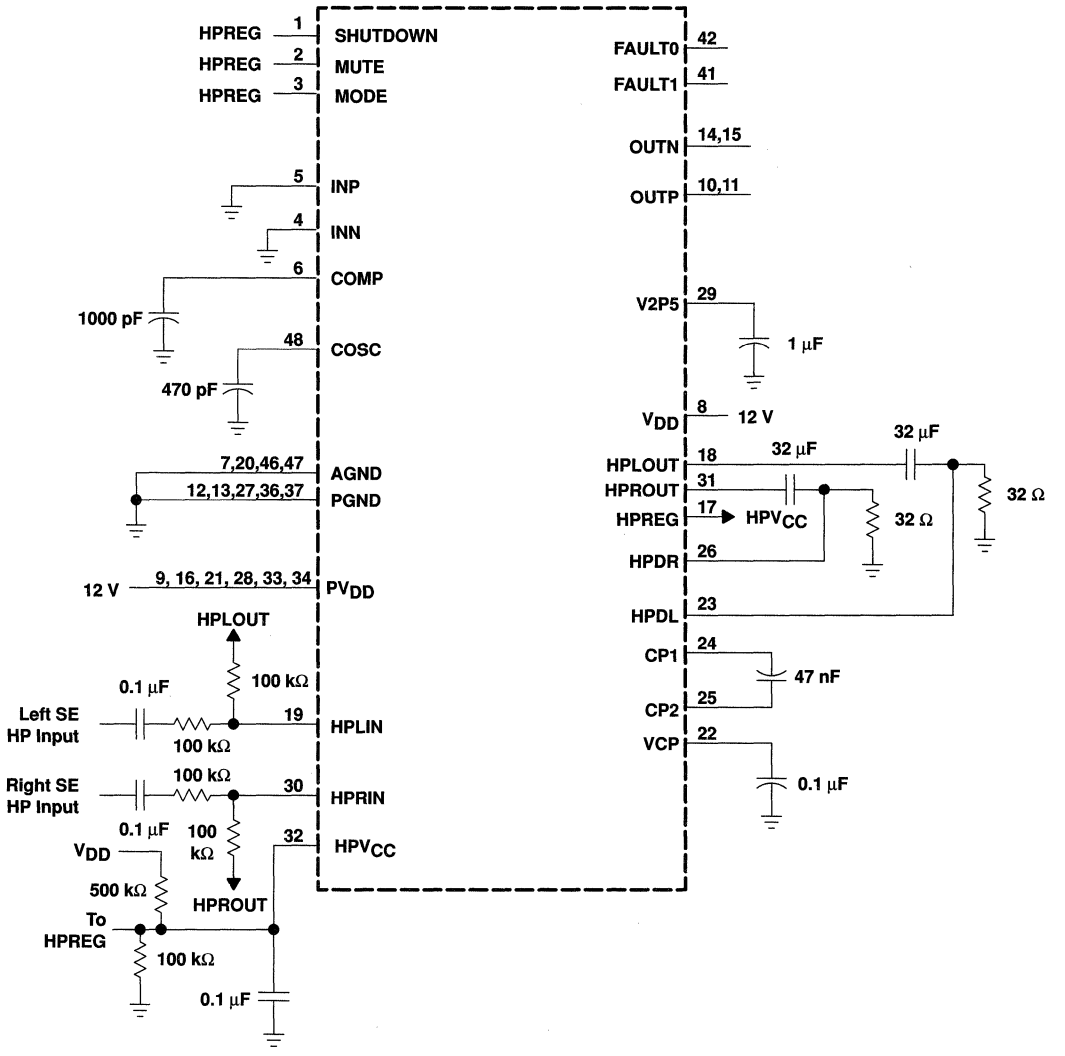
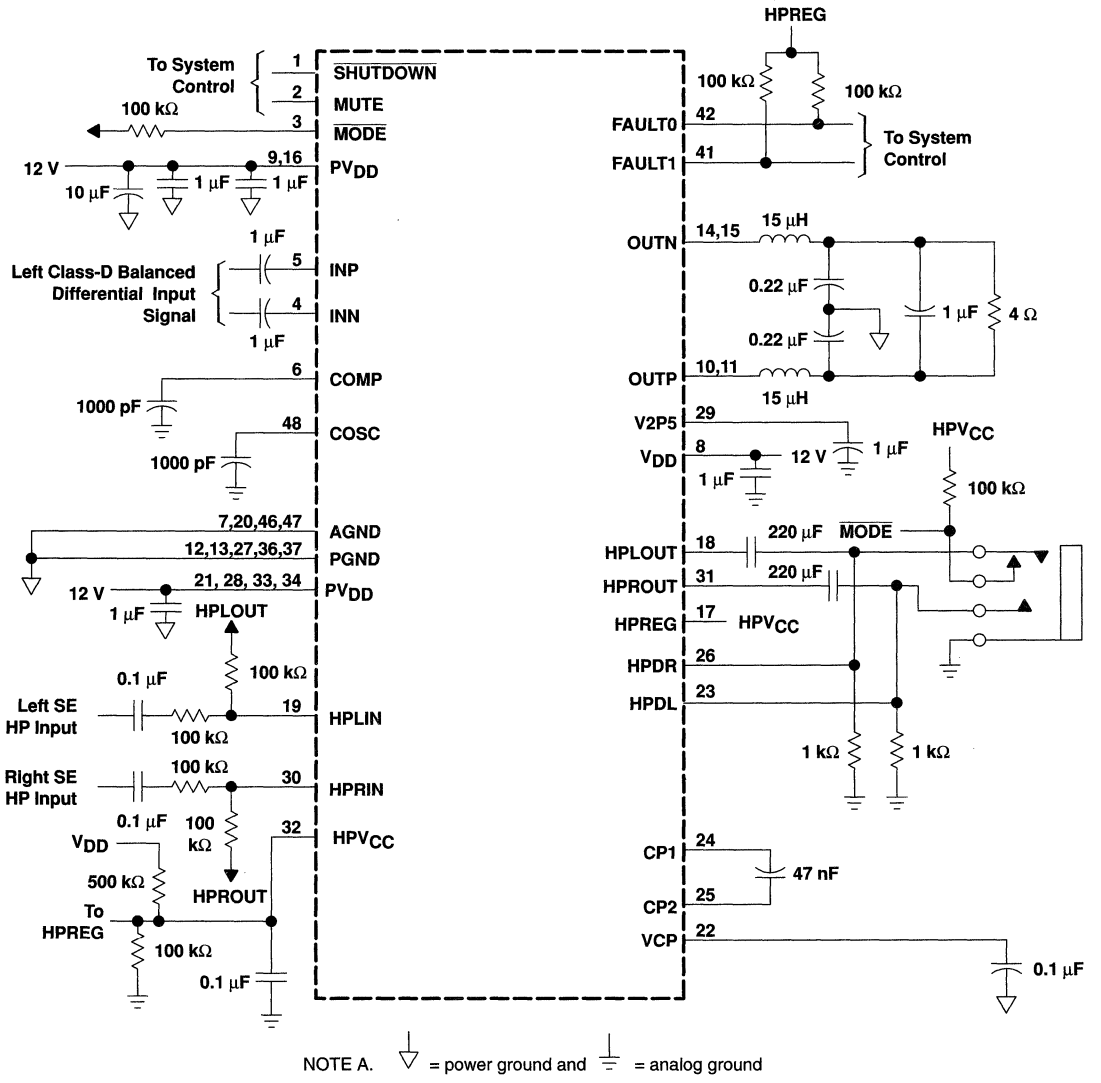


Figure 3. Headphone Test Circuit

APPLICATION INFORMATION



NOTE A. ▽ = power ground and ⏚ = analog ground

Figure 4. TPA032D03 Typical Configuration Application Circuit

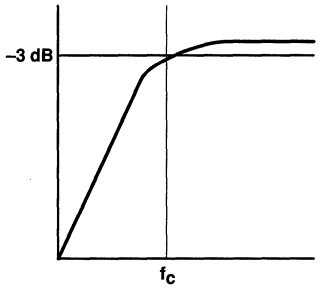
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and Z_I, the TPA032D03's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (8)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input, as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA032D03 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor, which should be located physically close to the TPA032D03. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA032D03 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA032D03 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA032D03 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of non-use for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 μA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low on-resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the on-resistance ($r_{DS(on)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (see Figure 5).

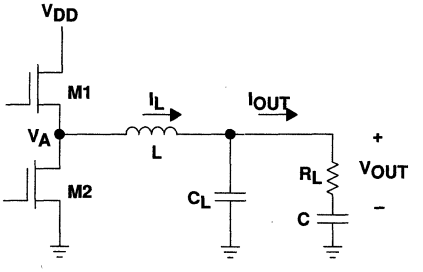


Figure 5. Half-Bridge Class-D Output Stage

Figures 6 and 7 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 5) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

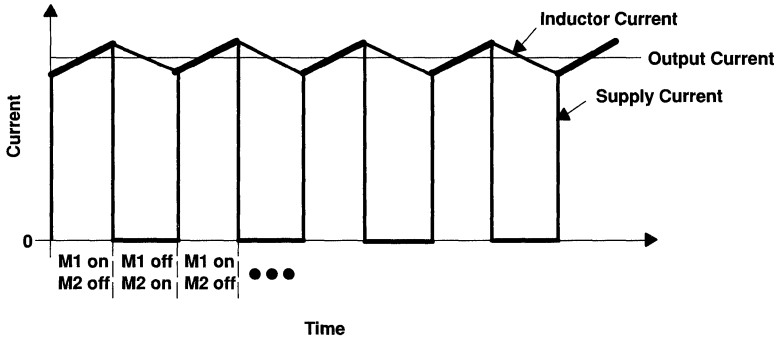


Figure 6. Class-D Currents

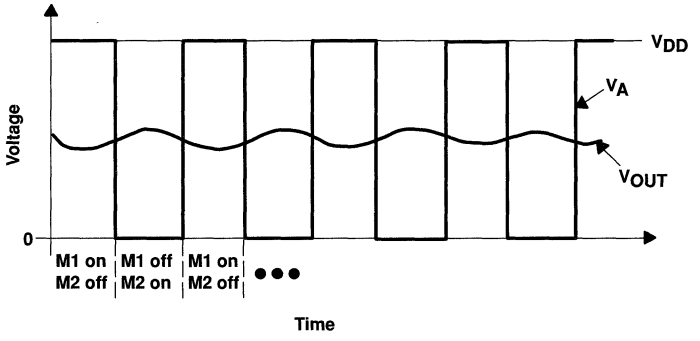


Figure 7. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average } (I_{DD}) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average } (I_{DD}) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}(I_{DD})$	$P_{SUP} = V_{DD} \times \text{Average}(I_{DD}) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 8.

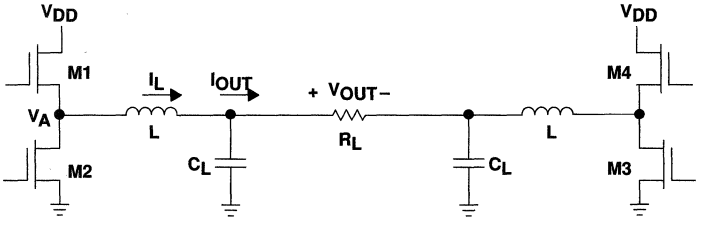


Figure 8. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is on (saturated). Any $r_{DS(on)}$ above 0 Ω causes conduction loss. Figure 9 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

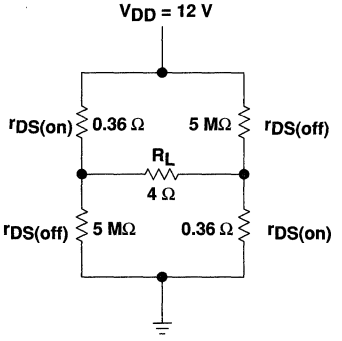


Figure 9. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2 R_L}{I^2\, 2r_{DS(on)} + I^2 R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1\ \Omega,\ R_L = 4\ \Omega\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.36\ \Omega,\ R_L = 4\ \Omega\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A diagram of the output, showing switching losses, is shown in Figure 10.

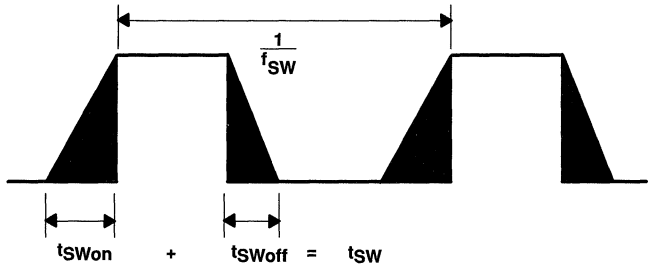


Figure 10. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 10-W per channel audio system with 4-Ω loads and a 12-V supply is almost 26 W. A similar linear amplifier such as the TPA032D03 has a maximum draw of greater than 50 W under the same circumstances.

Table 2. Efficiency vs Output Power in 12-V 4-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.5	41.7	2	0.35
2	66.7	4	0.5
5	75.1	6.32	0.83
8	78	8	1.13
10	77.9	8.94†	1.42

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (see Figure 11); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

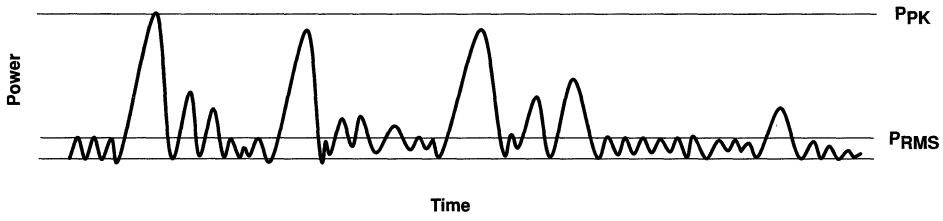


Figure 11. Audio Signal Showing Peak and RMS Power

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA032D03 data sheet, one can see that when the TPA032D03 is operating from a 12-V supply into a 4-Ω speaker that 20-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{20}{1}\right) = 6 \text{ dB} \quad (17)$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (18)$$

= 315 mW (18 dB crest factor)
= 630 mW (15 dB crest factor)
= 1.25 W (12 dB crest factor)
= 2.5 W (9 dB crest factor)
= 5 W (6 dB crest factor)
= 10 W (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 10 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, the internal dissipation in the TPA032D03 and maximum ambient temperatures are shown in Table 3.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 3. TPA032D03 Power Rating, 12-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
20	10 W (3 dB)	2.84	87°C
20	5 W (6 dB)	1.66	113°C
20	2.5 W (9 dB)	1.12	125°C
20	1.25 W (12 dB)	0.87	125°C
20	630 mW (15 dB)	0.7	125°C
20	315 mW (18 dB)	0.6	125°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA032D03 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{20}$$

$$= 150 - 22.3(0.35) = 125°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(1.42) = 118°C \text{ (3dB crest factor)}$$

(Maximum recommended case temperature is 125°C)

NOTE:

Internal dissipation of 0.7 W is estimated for a 10-W system with a 15 dB crest factor per channel.

The TPA032D03 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 12) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

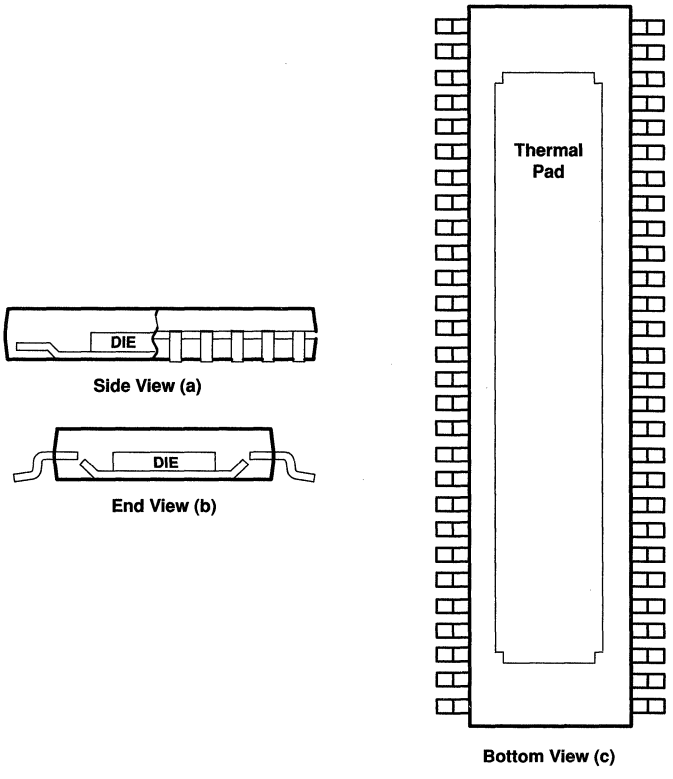
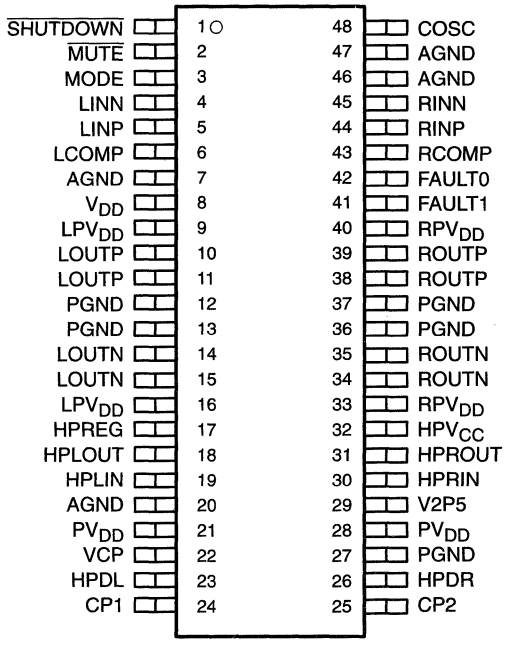


Figure 12. Views of Thermally Enhanced DCA Package

- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels, Plus Stereo Headphones**
- **10-W BTL Output Into 4 Ω From 12 V**
- **32-W Peak Music Power**
- **Fully Specified for 12-V Operation**
- **Low Shutdown Current**
- **Class-AB Headphone Amplifier**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



description

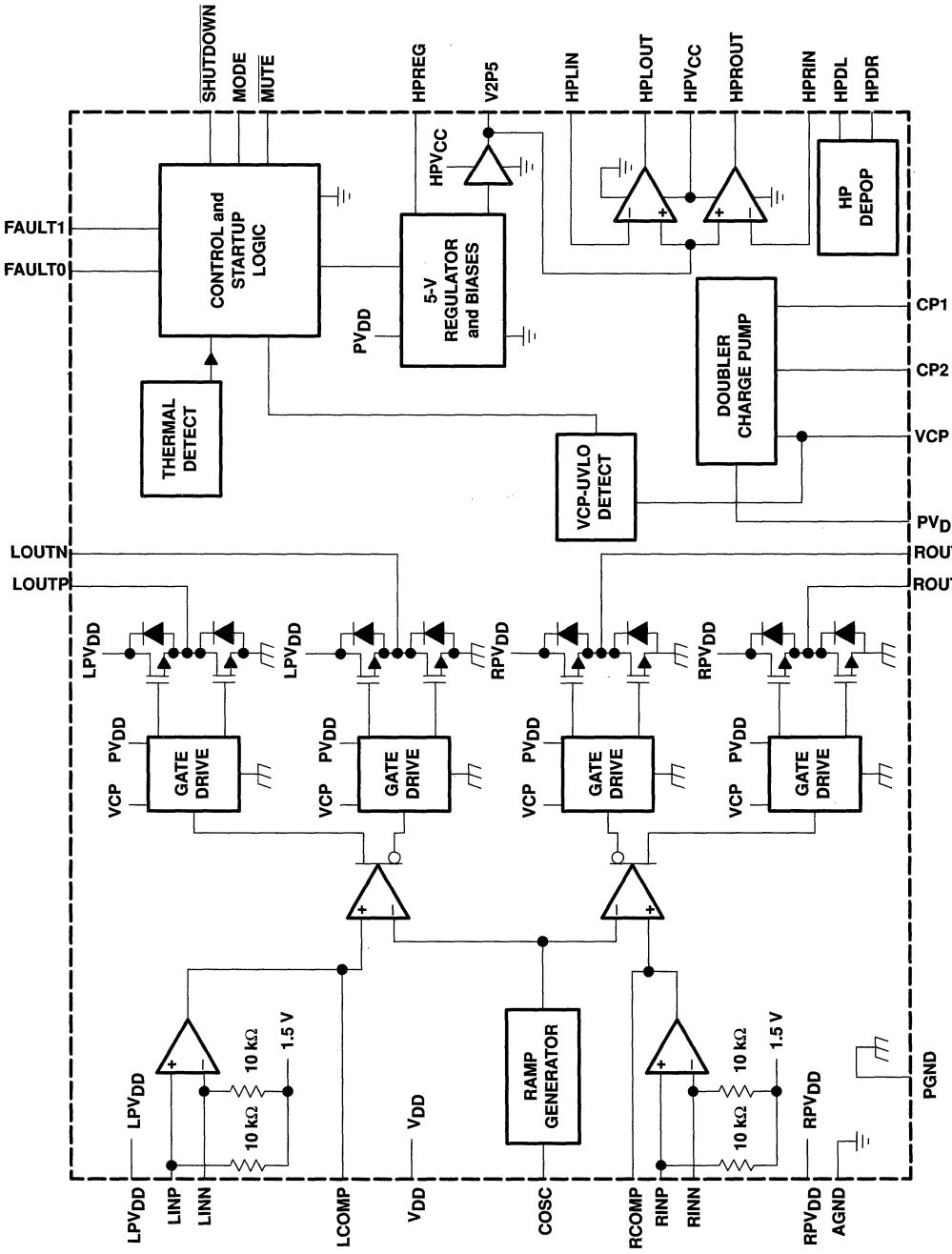
The TPA032D04 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA032D04 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 10 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 12-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. Included is a Class-AB headphone amplifier with interface logic to select between the two modes of operation. Only one amplifier is active at any given time, and the other is in power-saving sleep mode. Also, a chip-level shutdown control is provided to limit total supply current to 20 μA, making the device ideal for battery-powered applications.

The output stage is compatible with a range of power supplies from 8 V to 14 V. Protection circuitry is included to increase device reliability: thermal and under-voltage shutdown, with a status feedback terminal for use when any error condition is encountered.

The high switching frequency of the TPA032D04 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA032D04 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

schematic



NOTE B. LPV_{DD}, RPV_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	7, 20, 46, 47	Analog ground for headphone and Class-D analog sections
COSC	48	Connect a capacitor from analog ground to this terminal to set the frequency of the ramp reference signal.
CP1	24	First diode node for charge pump
CP2	25	First inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
HPDL	23	Depop control for left headphone
HPDR	26	Depop control for right headphone
HPLIN	19	Headphone amplifier left input
HPLOUT	18	Headphone amplifier left output
HPREG	17	5-V regulator output. This terminal requires a 1-μF capacitor to ground for stability reasons.
HPRIN	30	Headphone amplifier right input
HPROUT	31	Headphone amplifier right output
HPV_{CC}	32	5V supply to headphone amplifier and logic. This terminal is typically connected to HPREG.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
MODE	3	TTL logic-level mode input signal. When MODE is held low, the main Class-D amplifier is active. When MODE is held > high, the head phone amplifier is active.
$\overline{MUTE}$	2	Active-low TTL logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held > high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28	V_{DD} supply for charge-pump, headphone regulator, and gate drive circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low TTL logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held high, the device operates normally.
V2P5	29	2.5V internal reference bypass. This terminal requires a capacitor to ground.
VCP	22	Connect a capacitor from this terminal to power ground to provide storage for the charge pump output voltage.
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0	FAULT 1	DESCRIPTION
1	1	No fault. The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. This is not a latched fault, however. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault. All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes (not a latched fault). But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

headphone amplifier faults

The thermal fault remains active when the device is in head phone mode. This fault operation has exactly the same as it does for the Class-D amplifier (see Table 1).

If HPV_{CC} drops below approximately 4.5 V, the head phone is disabled. Once HPV_{CC} exceeds approximately 4.5 V, the head phone amplifier is re-enabled. No fault is reported to the user.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
–40°C to 125°C	TPA032D04DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA032D04DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)†

Supply voltage, (V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}) ..... 14 V
Headphone supply voltage, (HPV_{CC}) ..... 5.5 V
Input voltage, V_I ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$) ..... −0.3 V to 7 V
Output current, I_O (FAULT0, FAULT1), open drain terminated ..... 1 mA
Supply/load voltage, (FAULT0, FAULT1) ..... 7 V
Charge pump voltage, V_{CP} ..... PV_{DD} + 20 V
Continuous H-bridge output current (1 H-bridge conducting) ..... 3.5 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) ..... 7 A
Continuous HPREG output current, I_O (HPREG) ..... 150 mA
Continuous total power dissipation, T_C = 25°C ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Operating case temperature range, T_C ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}	8		14	V
Headphone supply voltage, HPV_{CC}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	−0.3		0.8	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	100	250	500	kHZ

electrical characteristics Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω to 8 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = xPV_{DD} = 11 V to 13 V		–40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
$I_{DD(Mute)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	18	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		20	30	µA
$\|I_{IH}\|$	High-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IH} = 5.25 V			10	µA
$\|I_{IL}\|$	Low-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IL} = –0.3 V			10	µA
$r_{DS(on)}$	Static drain-to-source on-state resistance (high-side + low-side FETs)	I_{DD} = 0.5 A		720	800	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel		95%	98%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	f = 1 kHz, THD = 0.5%, per channel, Device soldered on PCB, See Note 2		10		W
	Efficiency	P_O = 10 W, f = 1 kHz		77%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 23°C

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 8 Ω, T_A = 25°C, See Figure 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power,	THD = 0.5%, per channel, Device soldered on PCB, See Note 2		7.5		W
	Efficiency	P_O = 7.5 W, f = 1 kHz		85%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			–60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		–50		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 85°C

electrical characteristics, headphone amplifier, HPV_{CC} = 5 V, R_L = 32 Ω, T_A = 25°C, See Figure 3 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio			–60		dB
	Uncompensated gain range		–1		–10	V/V
I_{DD}	Supply current			9	12	mA
$I_{DD(MUTE)}$	Supply current, mute mode			9	12	mA
$I_{DD(S/D)}$	Supply current, shutdown mode			20	30	µA

operating characteristics, headphone amplifier, HPV_{CC} = 5V, R_L = 32 Ω, gain set at –10V/V, T_A = 25°C, See Figure 3 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%, f = 1 kHz		50		mW
	Crosstalk	f = 1 kHz		–60		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20	kHz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			>1		MΩ

operating characteristics, HPREG 5-V regulator, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V, I_O = 0 to 90 mA	4.5		5.5	V
I_{OS}	Short-circuit output current	V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 8 V to 14 V†	90			mA

† Pulse width must be limited to prevent exceeding the maximum operating virtual junction temperature of 150°C.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			30		°C

PARAMETER MEASUREMENT INFORMATION

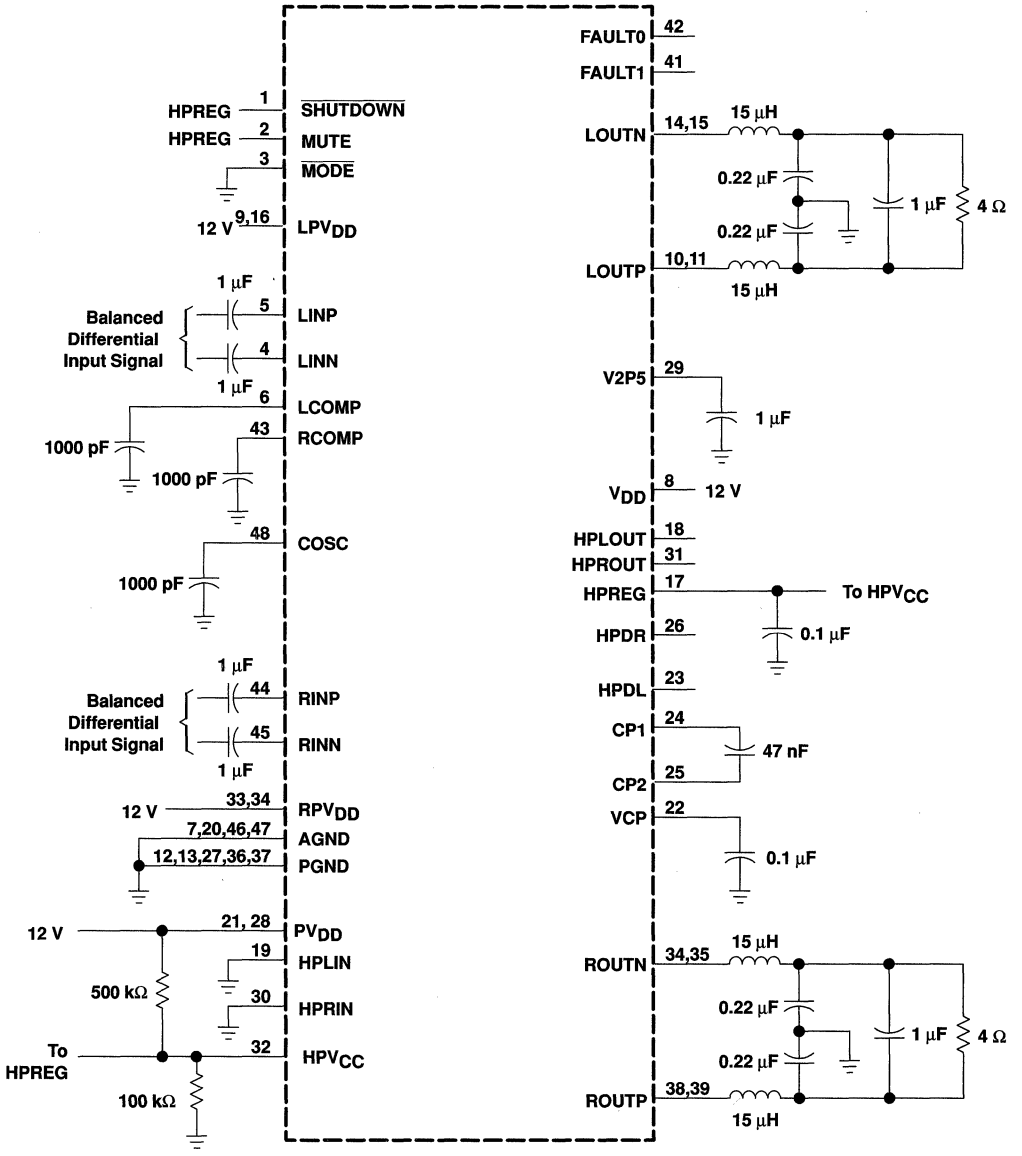


Figure 1. 12-V, 4-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

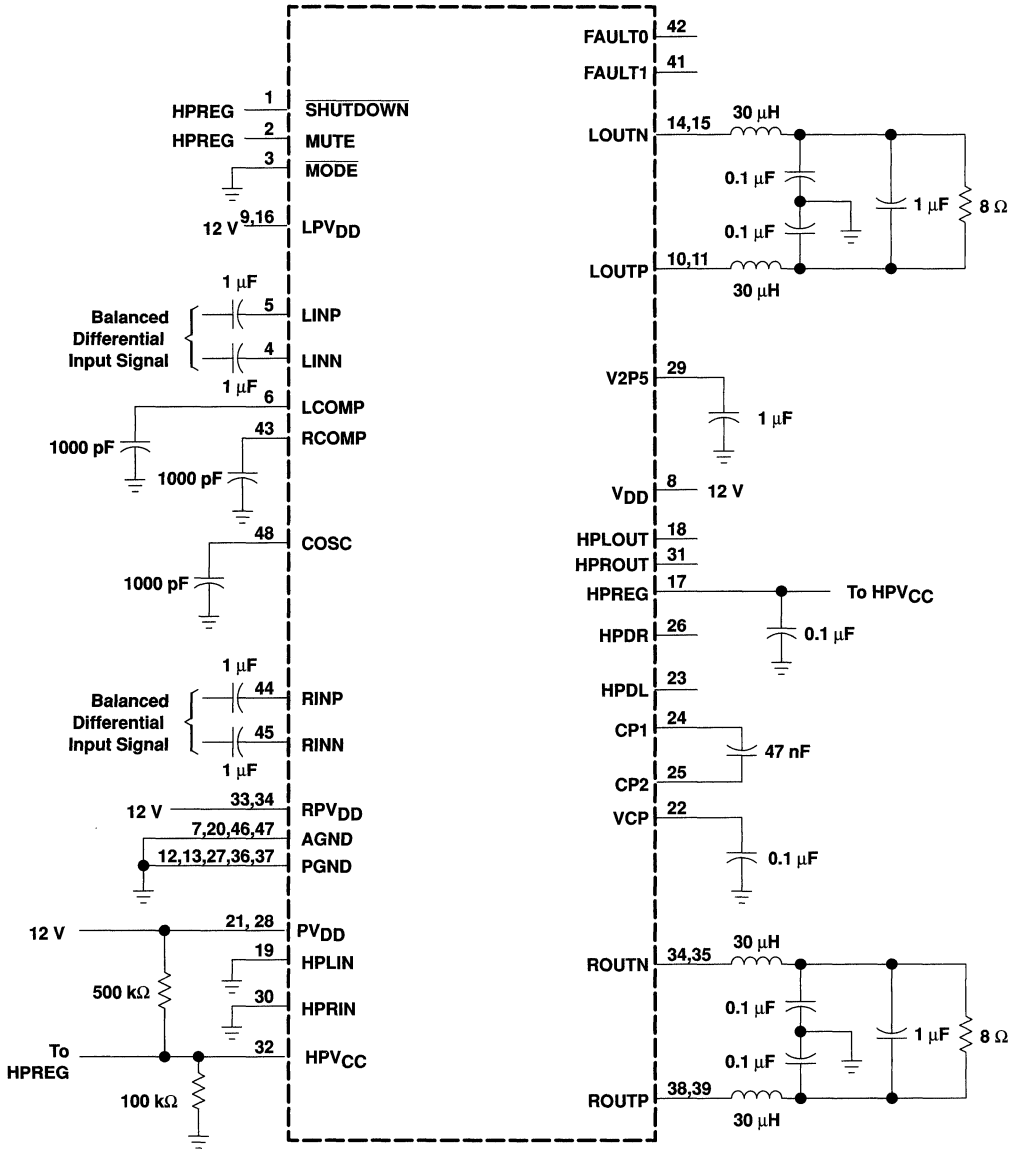


Figure 2. 12-V, 8-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

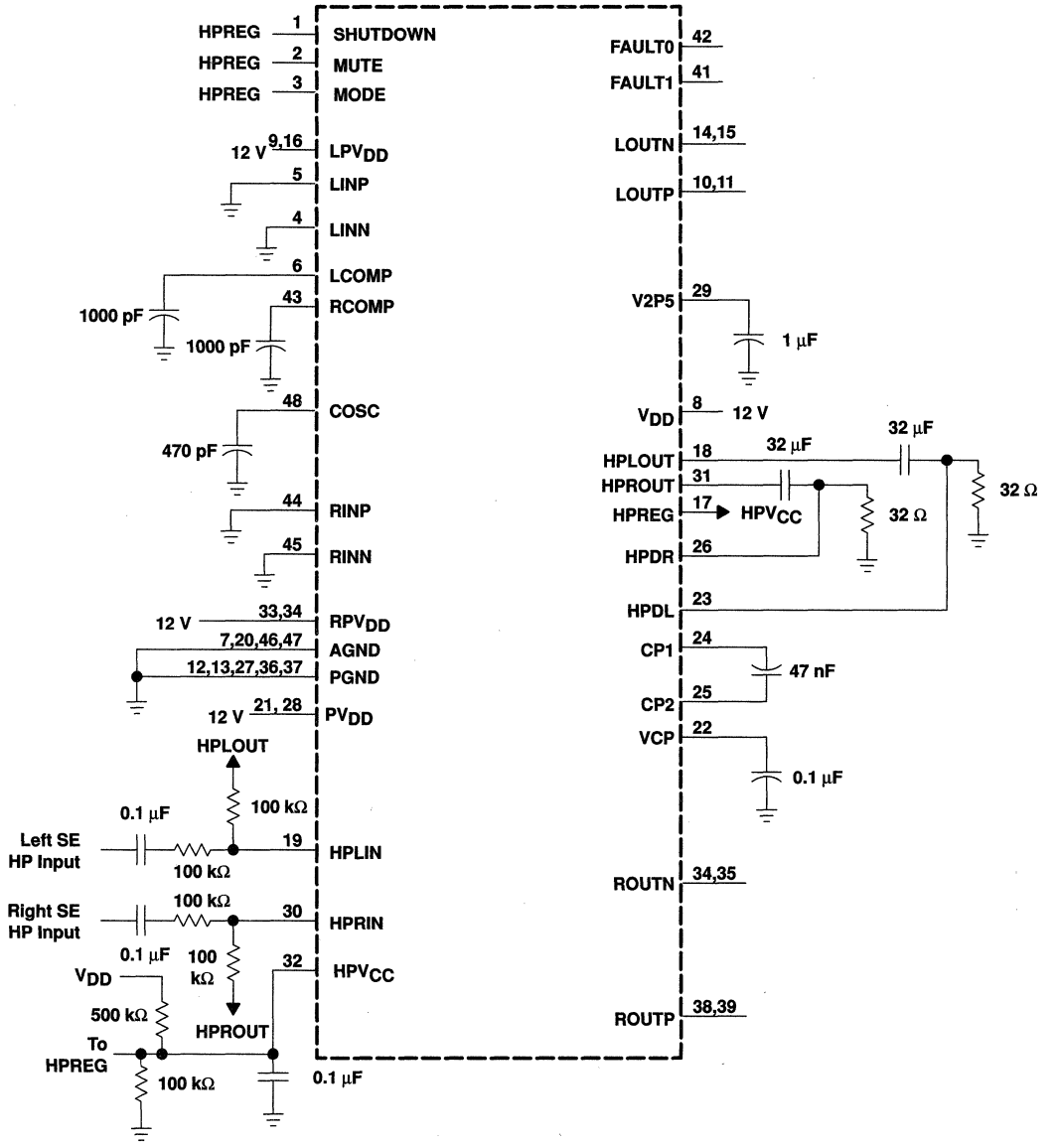


Figure 3. Headphone Test Circuit

APPLICATION INFORMATION

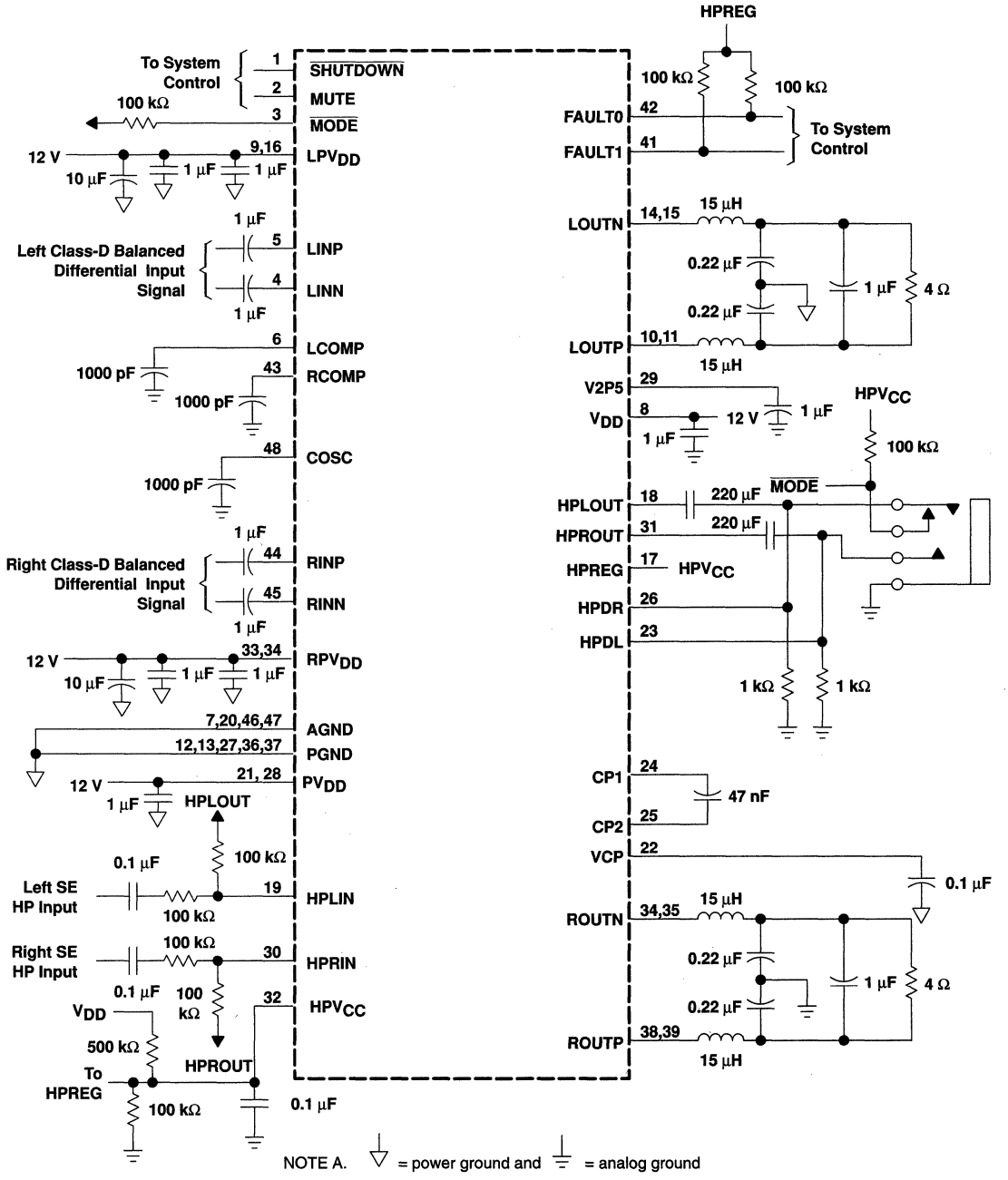


Figure 4. TPA032D04 Typical Configuration Application Circuit

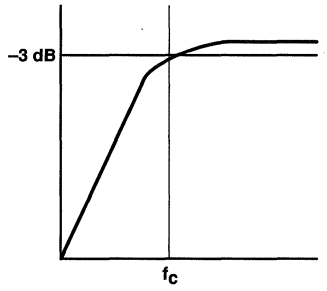
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and Z_I, the TPA032D04's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (8)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input, as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA032D04 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor, which should be located physically close to the TPA032D04. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA032D04 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA032D04 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA032D04 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of non-use for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 μA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low on-resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the on-resistance ($r_{DS(on)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (see Figure 5).

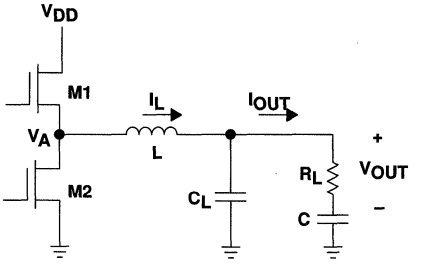


Figure 5. Half-Bridge Class-D Output Stage

Figures 6 and 7 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 5) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

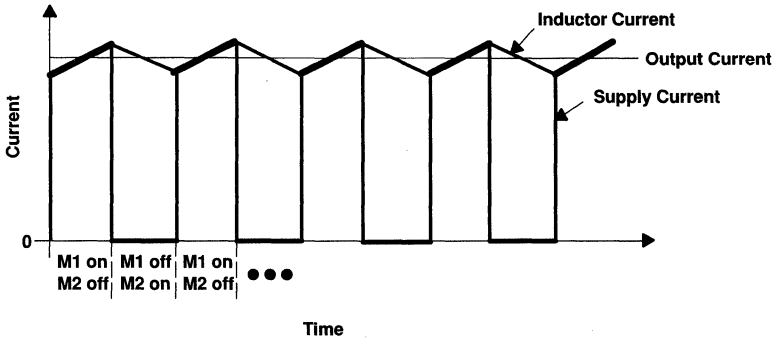


Figure 6. Class-D Currents

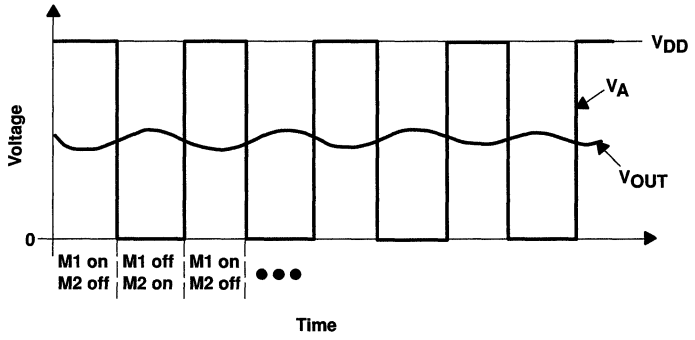


Figure 7. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average}\left(I_{DD}\right) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average}\left(I_{DD}\right) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right)$	$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 8.

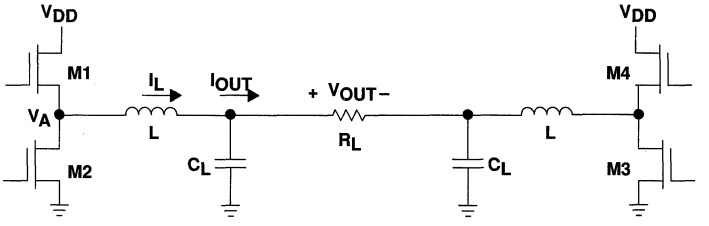


Figure 8. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is on (saturated). Any $r_{DS(on)}$ above 0 Ω causes conduction loss. Figure 9 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

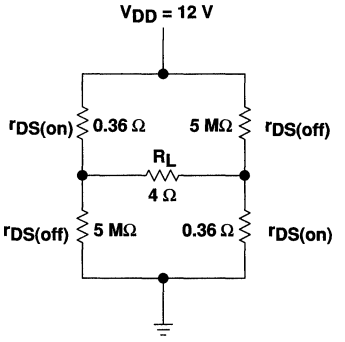


Figure 9. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2 R_L}{I^2\, 2r_{DS(on)} + I^2 R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1\ \Omega,\ R_L = 4\ \Omega\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.36\ \Omega,\ R_L = 4\ \Omega\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A diagram of the output, showing switching losses, is shown in Figure 10.

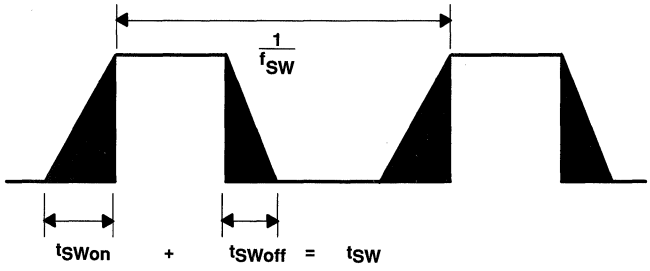


Figure 10. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 10-W per channel audio system with 4-Ω loads and a 12-V supply is almost 26 W. A similar linear amplifier such as the TPA032D04 has a maximum draw of greater than 50 W under the same circumstances.

Table 2. Efficiency vs Output Power in 12-V 4-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.5	41.7	2	0.7
2	66.7	4	1.0
5	75.1	6.32	1.66
8	78	8	2.26
10	77.9	8.94†	2.84

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (see Figure 11); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

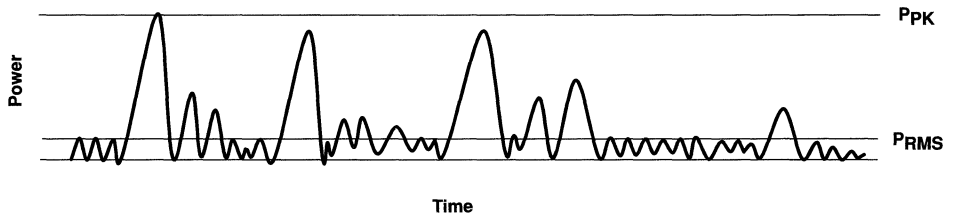


Figure 11. Audio Signal Showing Peak and RMS Power

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA032D04 data sheet, one can see that when the TPA032D04 is operating from a 12-V supply into a 4-Ω speaker that 20-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{20}{1}\right) = 6 \text{ dB} \quad (17)$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB – 18 dB = – 12 dB (15 dB crest factor)
6.0 dB – 15 dB = – 9 dB (15 dB crest factor)
6.0 dB – 12 dB = – 6 dB (12 dB crest factor)
6.0 dB – 9 dB = – 3 dB (9 dB crest factor)
6.0 dB – 6 dB = – 0 dB (6 dB crest factor)
6.0 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (18)$$

= 315 mW (18 dB crest factor)
= 630 mW (15 dB crest factor)
= 1.25 W (12 dB crest factor)
= 2.5 W (9 dB crest factor)
= 5 W (6 dB crest factor)
= 10 W (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 10 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, the internal dissipation in the TPA032D04 and maximum ambient temperatures are shown in Table 3.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 3. TPA032D04 Power Rating, 12-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
20	10 W (3 dB)	2.84	23°C
20	5 W (6 dB)	1.66	75°C
20	2.5 W (9 dB)	1.12	100°C
20	1.25 W (12 dB)	0.87	111°C
20	630 mW (15 dB)	0.7	118°C
20	315 mW (18 dB)	0.6	123°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA032D04 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{20}$$

$$= 150 - 22.3(0.7 \times 2) = 118°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(2.84 \times 2) = 23°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 1.4 W is estimated for a 10-W system with a 15 dB crest factor per channel.

The TPA032D04 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 12) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

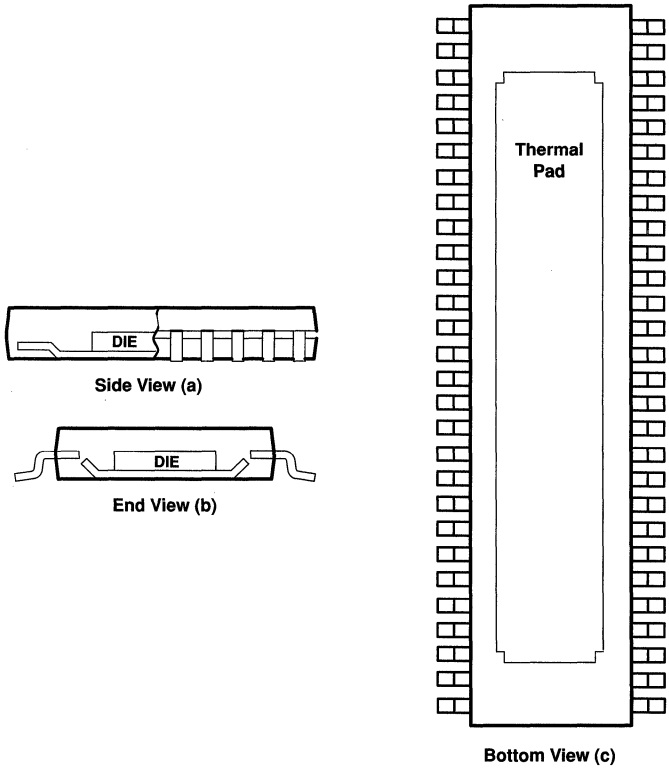
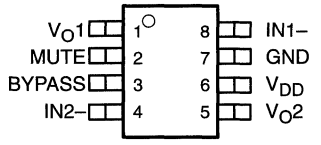


Figure 12. Views of Thermally Enhanced DCA Package

Contents

- **High-Fidelity Line-Out/HP Driver**
- **75-mW Stereo Output**
- **PC Power Supply Compatible**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
- **Pin Compatible With TPA302**

D PACKAGE
(TOP VIEW)



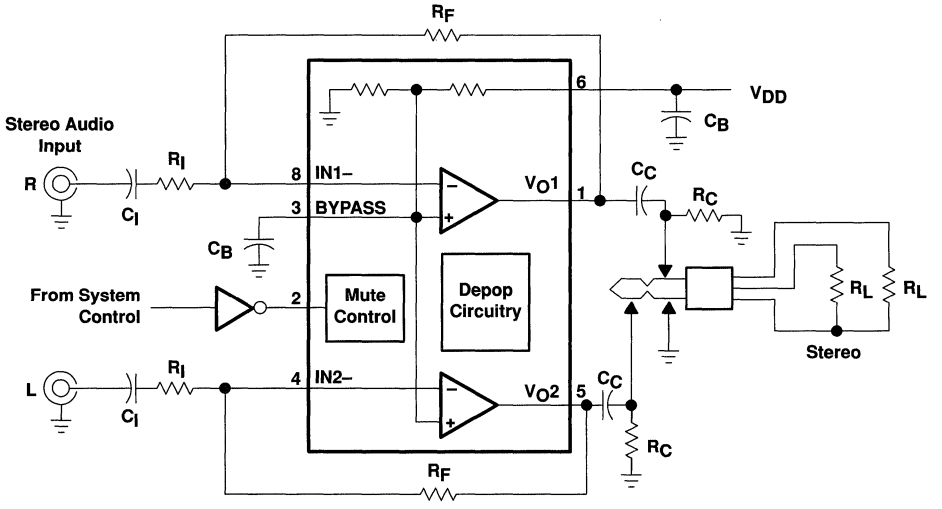
description

The TPA152 is a stereo audio power amplifier capable of less than 0.1% THD+N at 1 kHz when delivering 75 mW per channel into a 32-Ω load. THD+N is less than 0.2% across the audio band of 20 to 20 kHz. For 10 kΩ loads, the THD+N performance is better than 0.005% at 1 kHz, and less than 0.01% across the audio band of 20 to 20 kHz.

The TPA152 is ideal for use as an output buffer for the audio CODEC in PC systems. It is also excellent for use where a high-performance head phone/line-out amplifier is needed. Depop circuitry is integrated to reduce transients during power up, power down, and mute mode.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10. The TPA152 is packaged in the 8-pin SOIC (D) package that reduces board space and facilitates automated assembly.

typical application circuit



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE
–40°C to 85°C	TPA152D†

† The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA152DR)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	3		BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
GND	7		GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
MUTE	2	I	A logic high puts the device into MUTE mode.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
V_O1	1	O	V_O1 is the audio output for channel 1.
V_O2	5	O	V_O2 is the audio output for channel 1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage , V_I ..... –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation ..... internally limited (See Dissipation Rating Table)
Operating junction temperature range, T_J ..... –40°C to 150° C
Operating case temperature range, T_C ..... –40°C to 125° C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	724 mW	5.8 mW/°C	464 mW	376 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	4.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage				10	mV
	Supply ripple rejection ratio	V_{DD} = 4.9 V to 5.1 V		81		dB
I_{DD}	Supply current	See Figure 13		5.5	14	mA
$I_{DD(MUTE)}$	Supply current in MUTE			5.5	14	mA
Z_I	Input impedance			>1		MΩ

ac operating characteristics V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.03%, Gain = 1, See Figure 1		75†		mW
THD+N	Total harmonic distortion plus noise	P_O = 75 mW, See Figure 2 20 Hz–20 kHz, Gain = 1,		0.2%		
B_{OM}	Maximum output power bandwidth	A_V = 5, THD <0.6%, See Figure 2		>20		kHz
	Phase margin	Open loop, See Figure 16		80°		
	Supply ripple rejection ratio	1 kHz, C_B = 1 µF, See Figure 12		65		dB
	Mute attenuation	See Figure 15		110		dB
	Ch/Ch output separation	See Figure 13		102		dB
	Signal-to-Noise ratio	V_O = 1 $V_{(rms)}$, Gain = 1 See Figure 11		104		dB
V_n	Noise output voltage	See Figure 10		6		µV(rms)

† Measured at 1 kHz.

NOTES: 1. The dc output voltage is approximately V_{DD}/2.
2. Output power is measured at the output pins of the IC at 1 kHz.

ac operating characteristics V_{DD} = 5 V, T_A = 25°C, R_L = 10 kΩ

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion plus noise	V_I = 1 $V_{(rms)}$, See Figure 6	20 Hz–20 kHz, Gain = 1,			0.005%		
		$V_{O(PP)}$ = 4 V, See Figure 8	20 Hz–20 kHz, Gain = 1,			0.005%		
B_{OM}	Maximum output power bandwidth	G = 5,	THD <0.02%,	See Figure 6		>20		kHz
	Phase margin	Open loop,	See Figure 16			80°		
k_{SVR}	Supply voltage rejection ratio	1 kHz,	C_B = 1 µF,	See Figure 12		65		dB
	Mute attenuation	See Figure 15				110		dB
	Ch/Ch output separation	See Figure 13				102		dB
	Signal-to-Noise ratio	V_O = 1 $V_{(rms)}$,	Gain = 1,	See Figure 11		104		dB
V_n	Noise output voltage	See Figure 10				6		µV(rms)

† Measured at 1 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4
THD+N	Total harmonic distortion plus noise	vs Frequency	2, 3, 6, 8, 9
THD+N	Total harmonic distortion plus noise	vs Output voltage	5, 7
V_n	Output noise voltage	vs Frequency	10
SNR	Signal-to-noise ratio	vs Gain	11
	Supply ripple rejection ratio	vs Frequency	12
	Crosstalk	vs Frequency	13, 14
	Mute Attenuation	vs Frequency	15
	Open-loop gain and phase	vs Frequency	16, 17
	Closed-loop gain and phase	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
P_O	Output power	vs Load resistance	20
P_D	Power dissipation	vs Output power	21

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

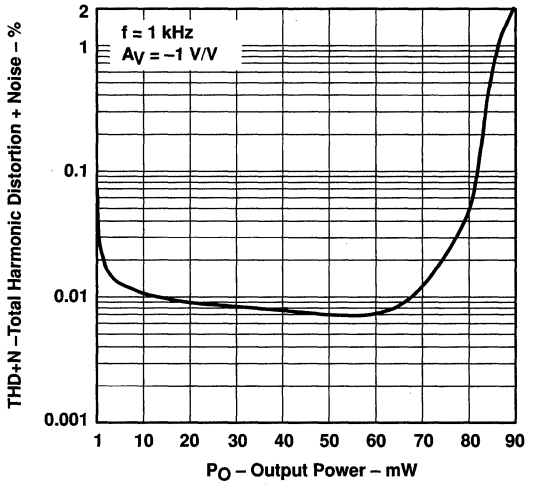


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

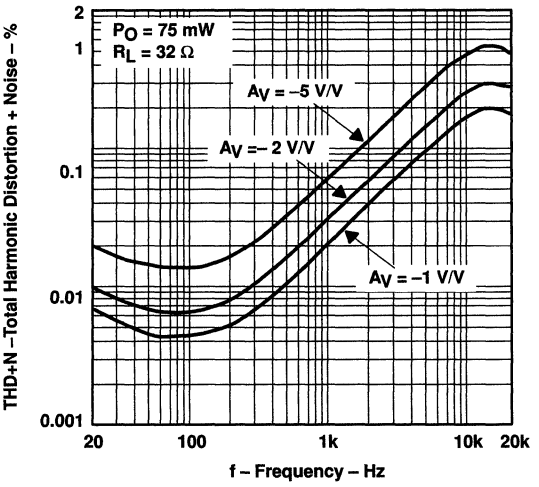


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

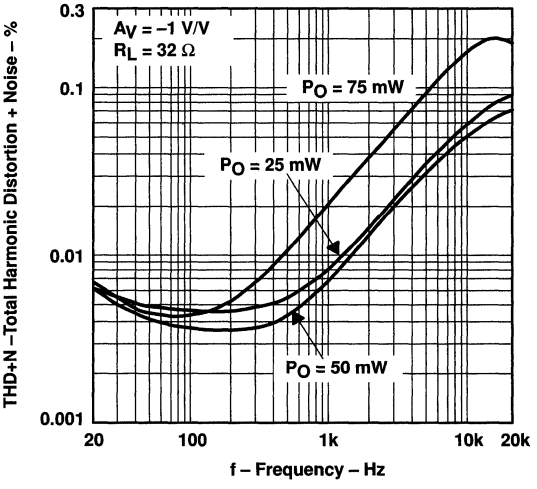


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

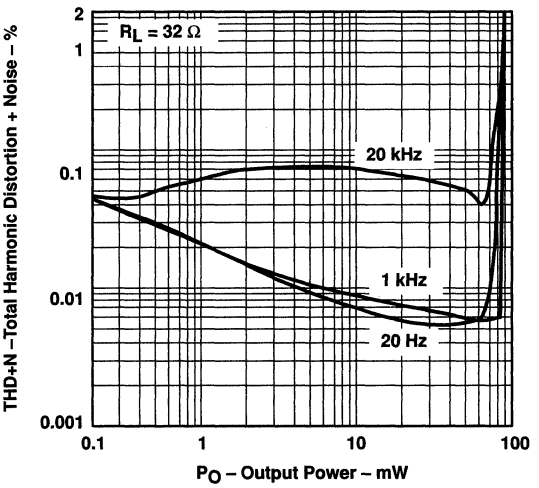


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

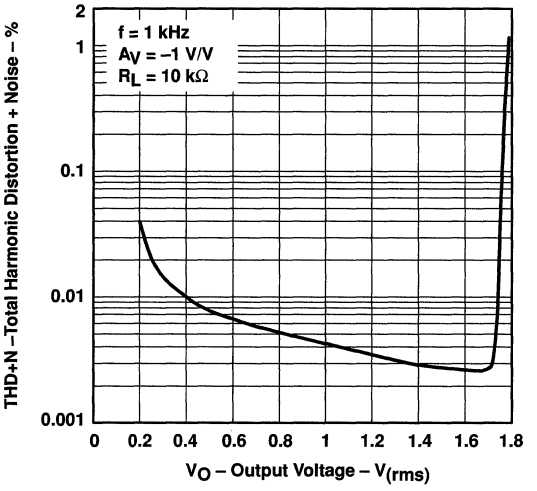


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

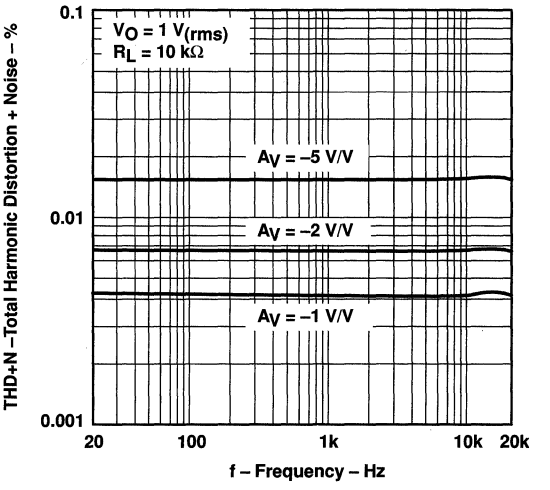


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

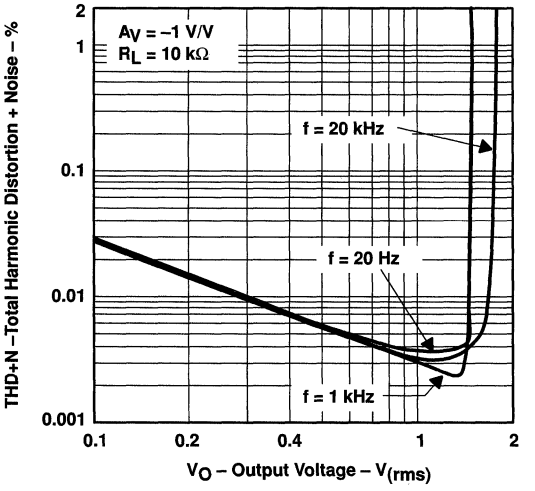


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

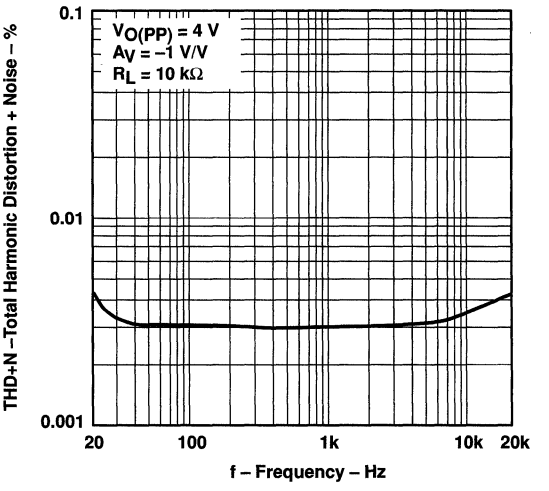


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

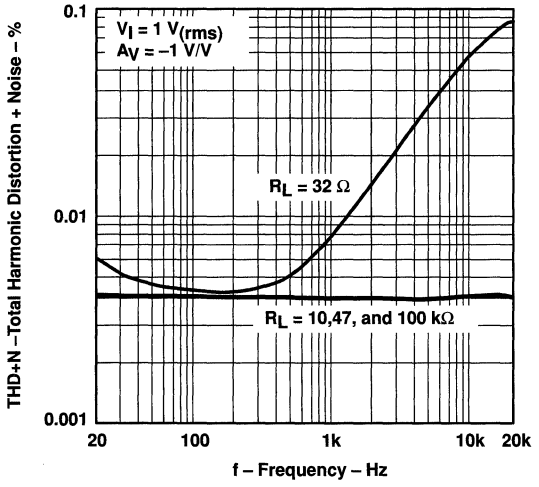


Figure 9

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

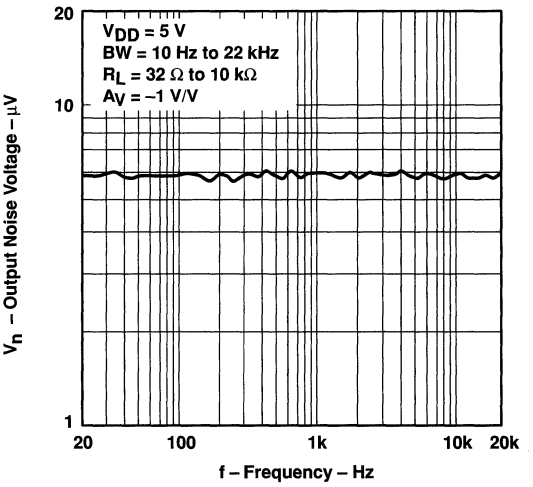


Figure 10

SIGNAL-TO-NOISE RATIO
vs
GAIN

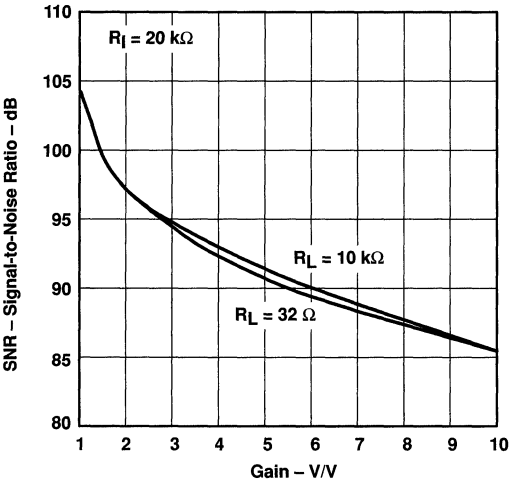


Figure 11

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

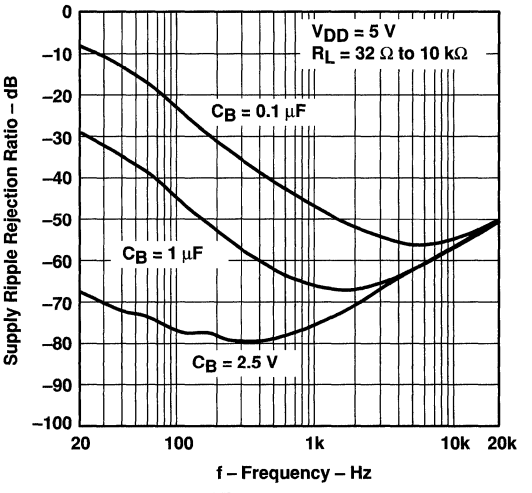


Figure 12

TYPICAL CHARACTERISTICS

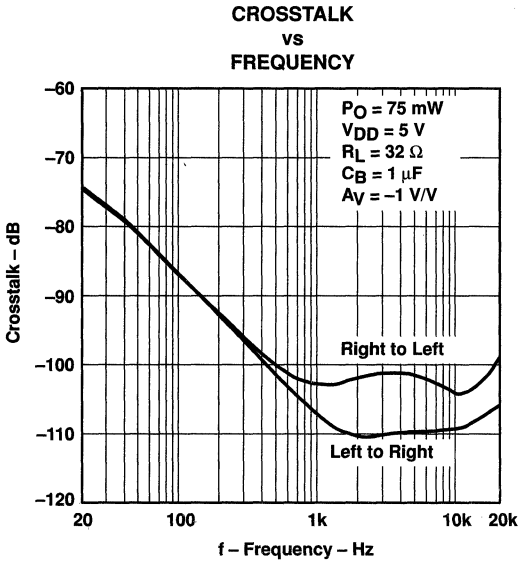


Figure 13

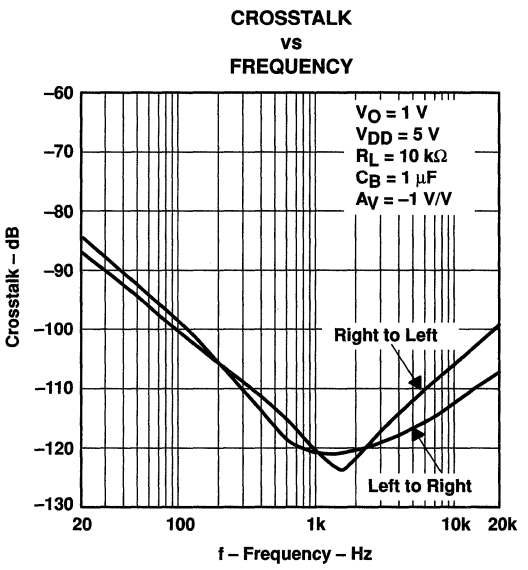


Figure 14

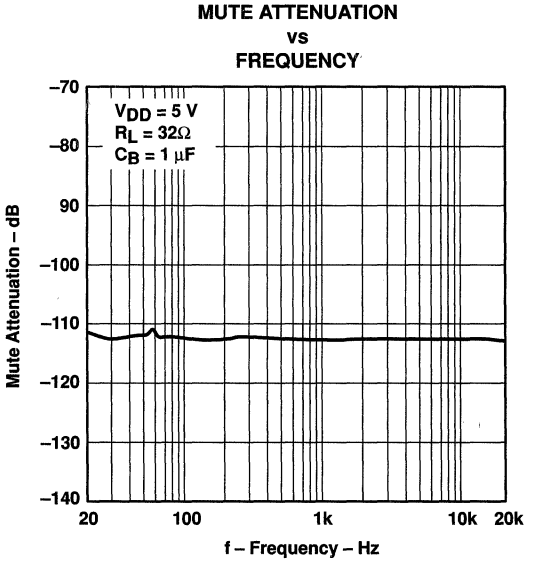


Figure 15

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

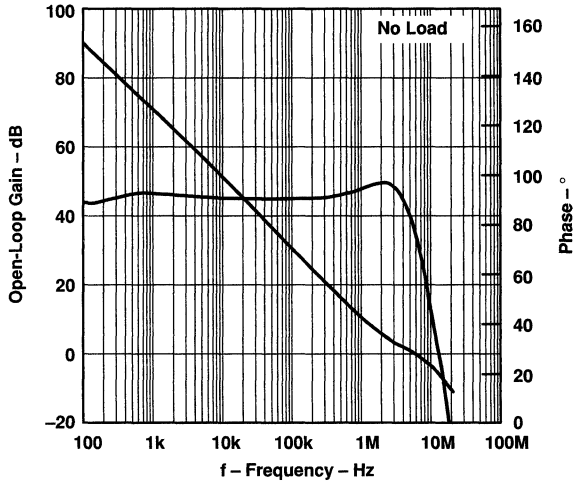


Figure 16

**CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY**

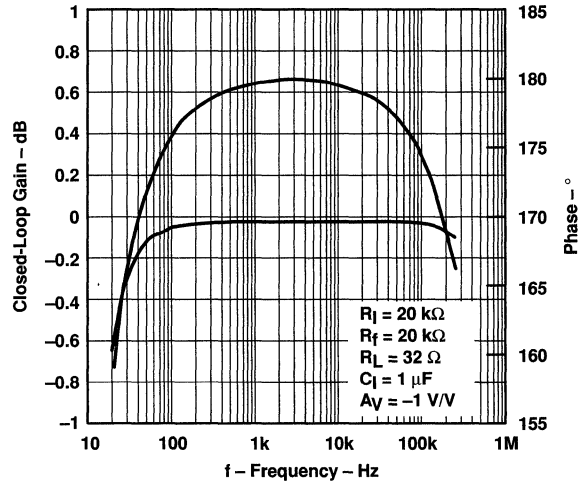


Figure 17

TYPICAL CHARACTERISTICS

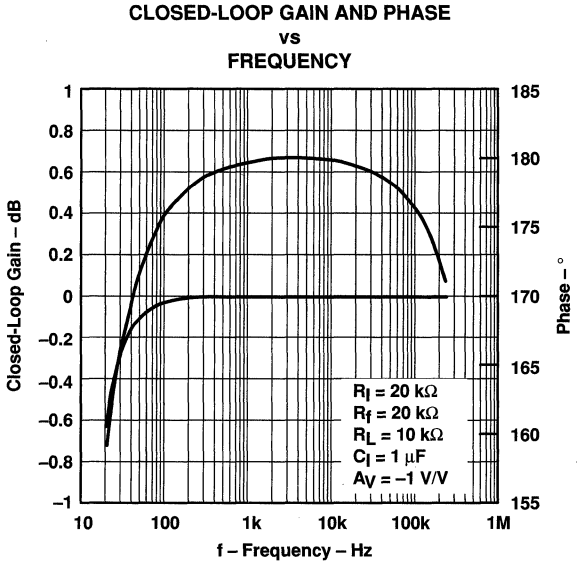


Figure 18

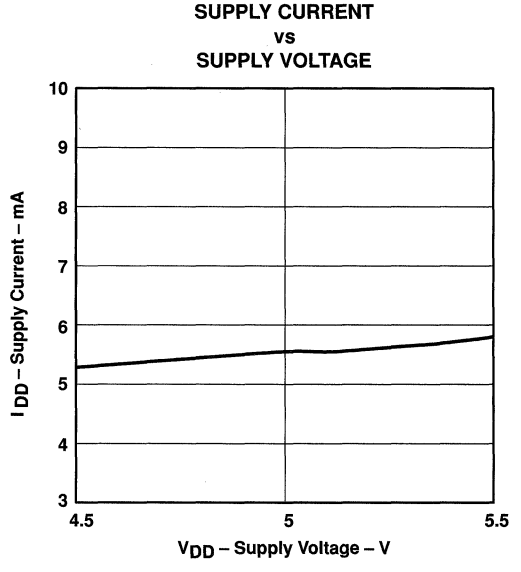


Figure 19

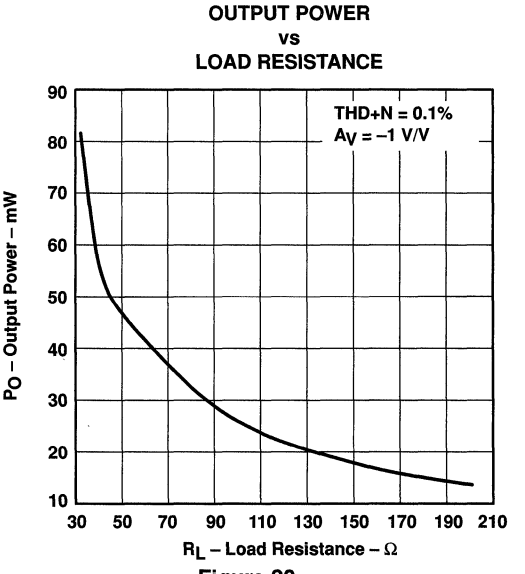


Figure 20

TYPICAL CHARACTERISTICS

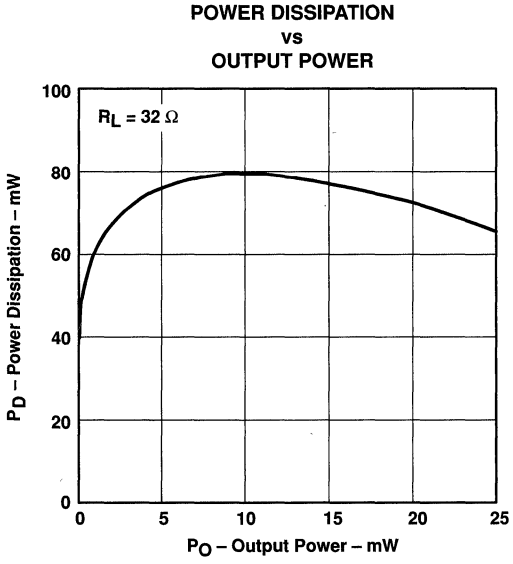
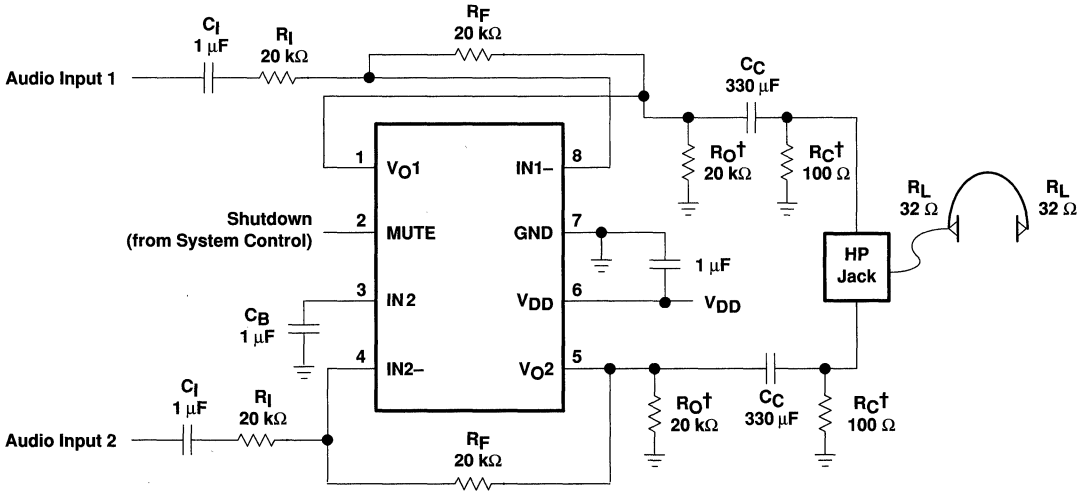


Figure 21

APPLICATION INFORMATION

selection of components

Figure 22 is a schematic diagram of a typical application circuit.



† These resistors are optional. Adding these resistors improves the depop performance of the TPA152.

Figure 22. TPA152 Typical Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA152 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA152 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be −1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example if R_F is 100 kΩ and C_F is 5 pF then $f_{co(\text{lowpass})}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(\text{highpass})}} \tag{5}$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA152 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \tag{6}$$

As an example, consider a circuit where C_B is 1 μF, C_I is 1 μF and R_I is 20 kΩ. Inserting these values into the equation 9 results in:

$$6.25 \leq 50$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 μF	73 Hz
10,000 Ω	68 μF	0.23 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{8}$$

output pull-down resistor, R_C + R_O

Placing a 100-Ω resistor, R_C, from the output side of the coupling capacitor to ground insures the coupling capacitor, C_C, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones.

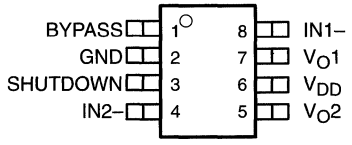
Placing a 20-kΩ resistor, R_O, from the output of the IC to ground insures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10-kΩ loads.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

- 150 mW Stereo Output
- PC Power Supply Compatible
  - Fully Specified for 3.3 V and 5 V Operation
  - Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - PowerPAD™ MSOP
- Pin Compatible With LM4881

DGN PACKAGE
(TOP VIEW)

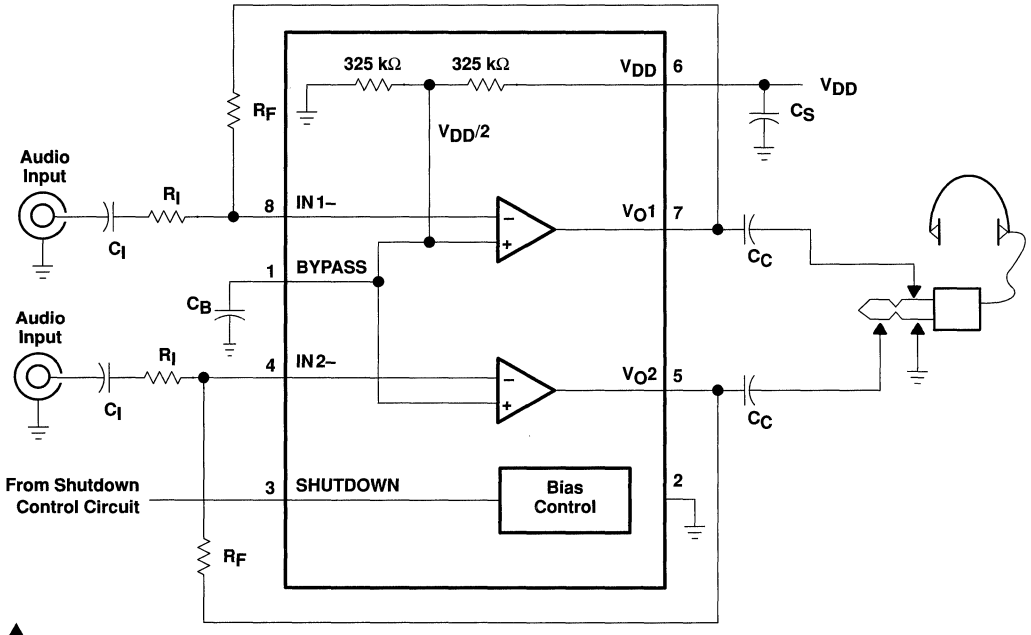


description

The TPA102 is a stereo audio power amplifier packaged in an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	MSOP Symbolization
	MSOP†	
–40°C to 85°C	TPA102DGN	TI AAC

† The DGN package is available in left-ended tape and reel only (e.g., TPA102DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
SHUTDOWN	3	I	Puts the device in a low quiescent current mode when held high.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
V_O1	7	O	V_O1 is the audio output for channel 1.
V_O2	5	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation ..... internally limited
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14 W‡	17.1 mW/°C	1.37 W	1.11 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		83		dB
I_{DD}	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			10	50	μA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 70 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection ratio	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		76		dB
I_{DD}	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			60	100	μA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 150 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	f = 1 kHz		68		dB
	Channel/Channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20–20 kHz		0.5%		
B_{OM}	Maximum output power BW	A_V = 10, THD <2%		>20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection ratio	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		97		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20–20 kHz		0.4%		
B_{OM}	Maximum output power BW	A_V = 10, THD <2%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		97		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Power output	3, 6, 9, 12, 15, 18
	Power supply rejection ratio	vs Frequency	19, 20
V_n	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23–26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain	vs Frequency	29, 30
	Phase margin		
	Output power	vs Load resistance	31, 32
I_{DD}	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39–44
	Phase		
	Power dissipation	vs Output power	45, 46

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

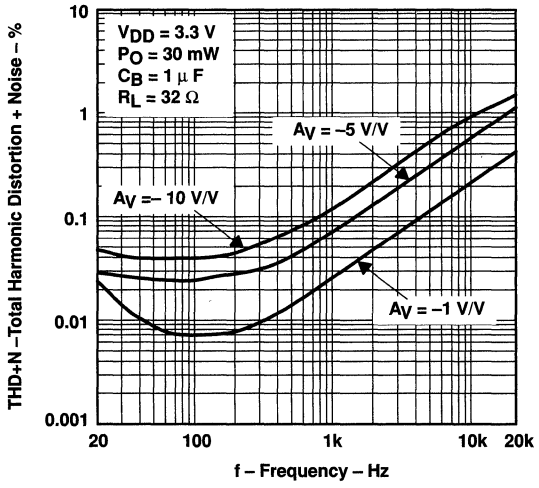


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

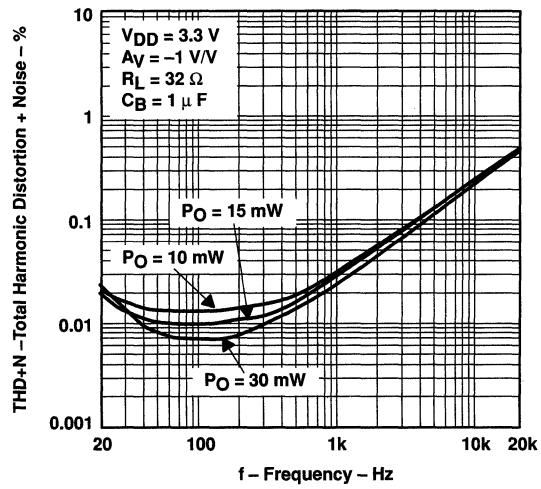


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

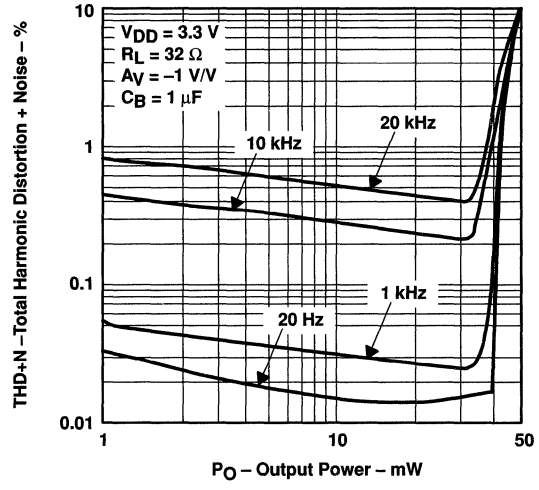


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

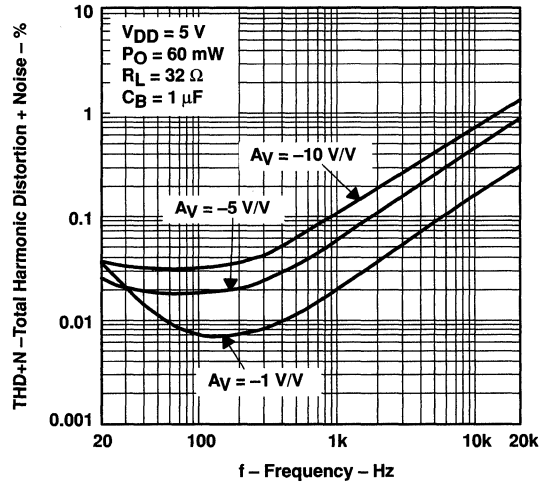


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

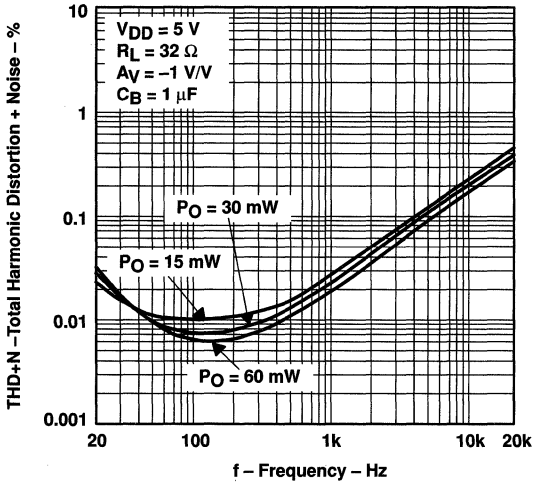


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

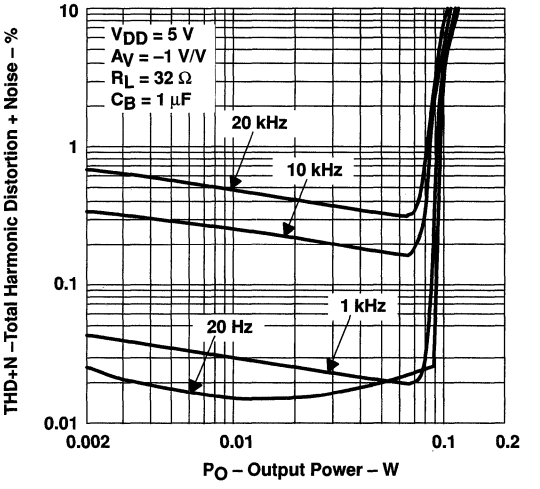


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

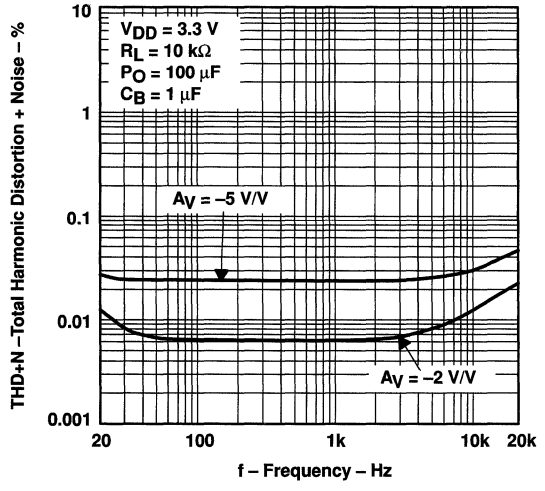


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

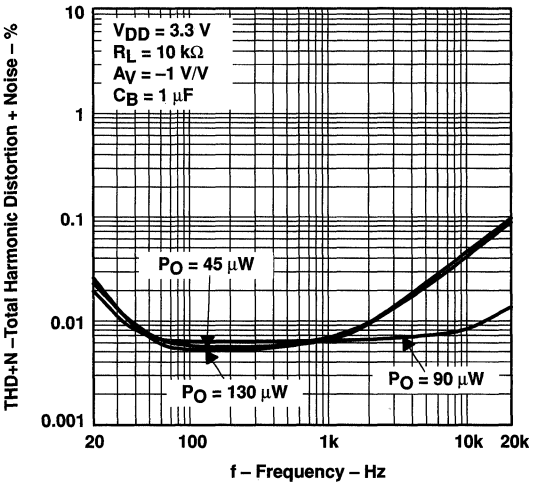


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

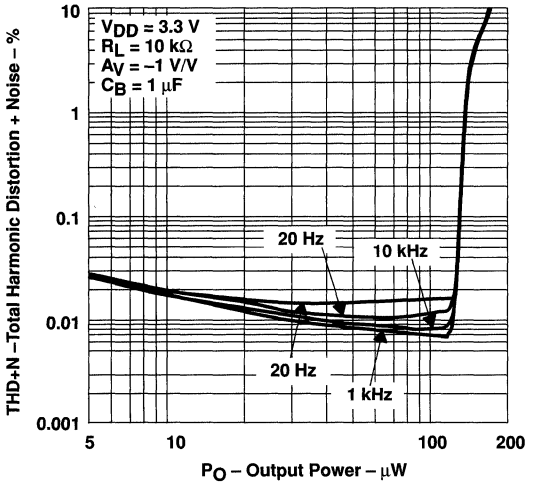


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

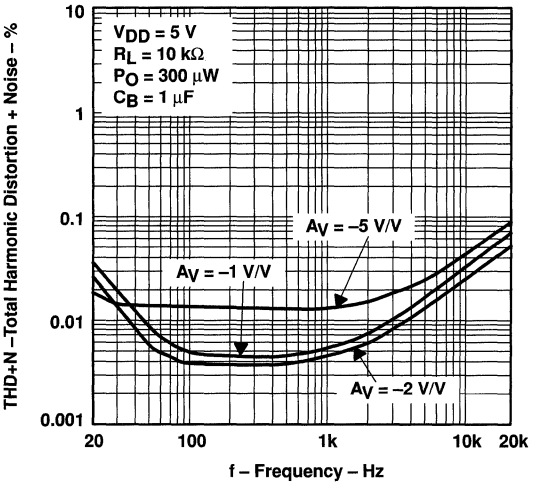


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

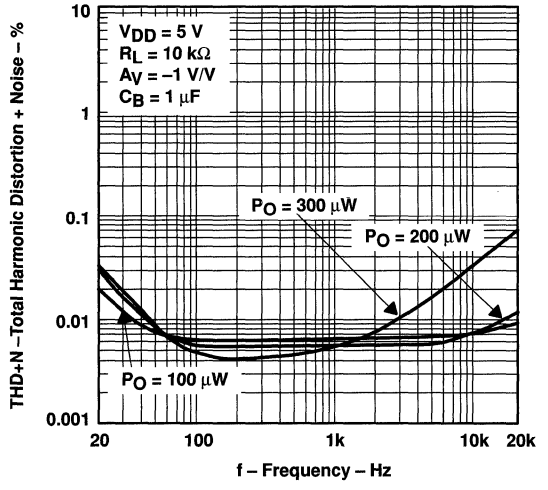


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

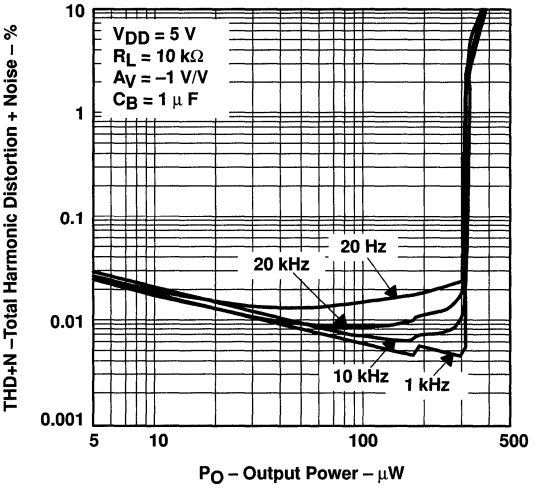


Figure 12

TYPICAL CHARACTERISTICS

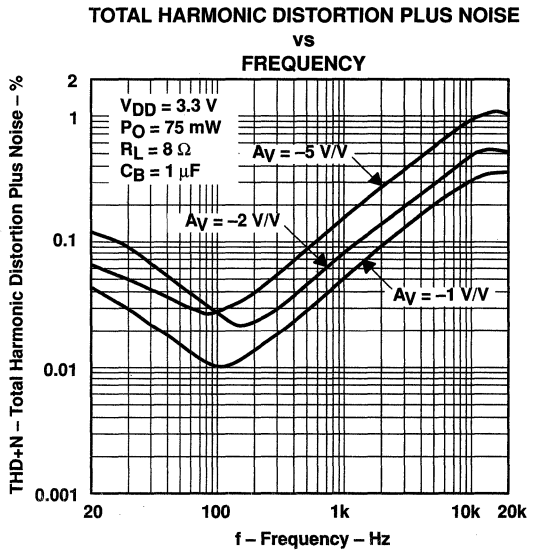
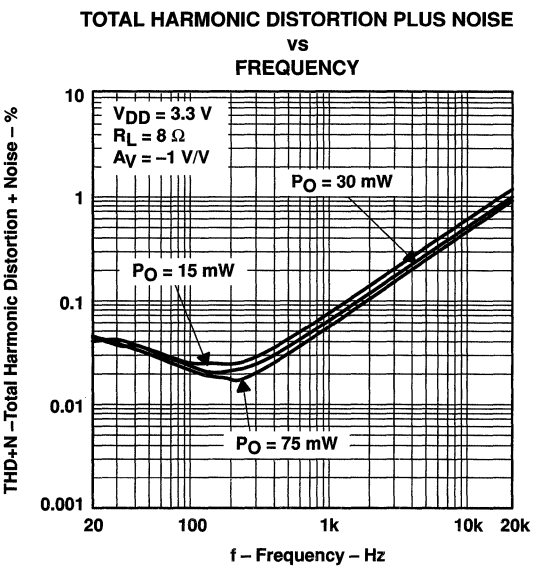


Figure 13



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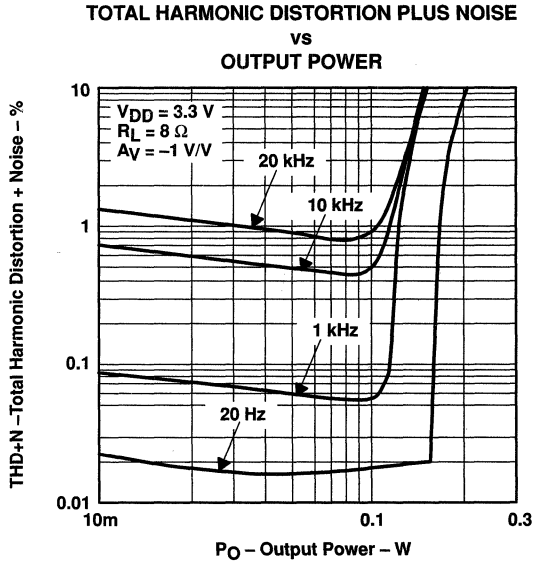


Figure 15

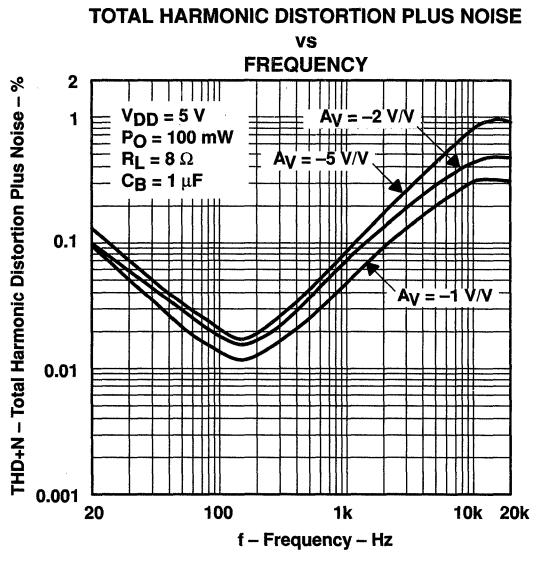


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

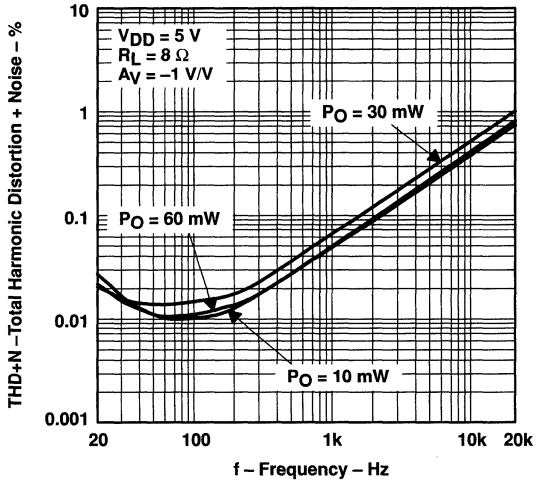


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

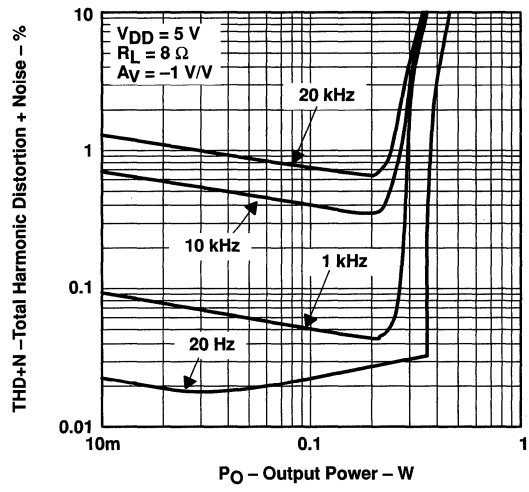


Figure 18

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

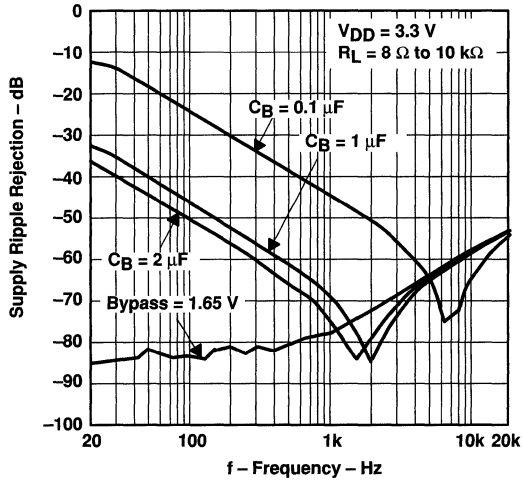


Figure 19

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

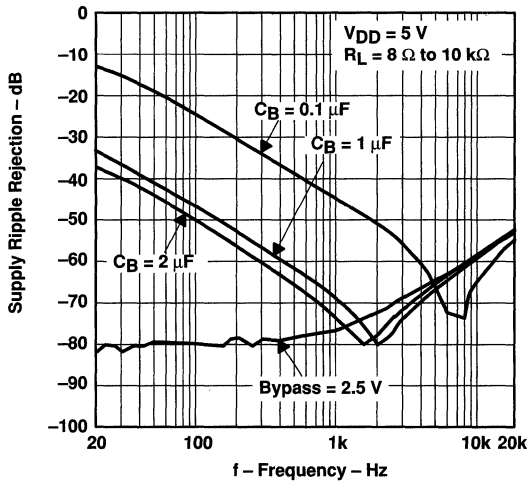
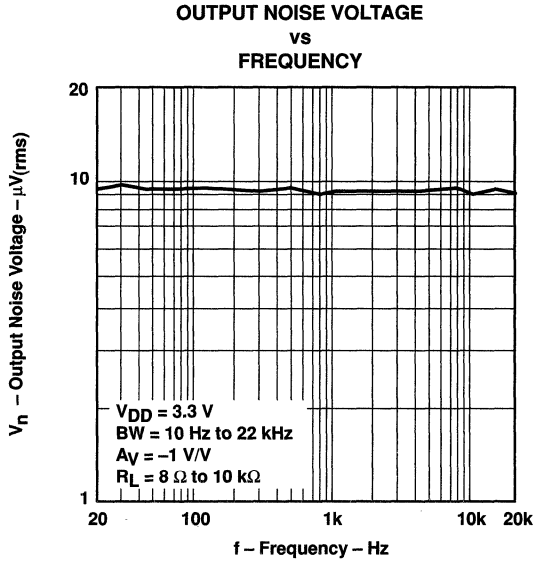


Figure 20

TYPICAL CHARACTERISTICS



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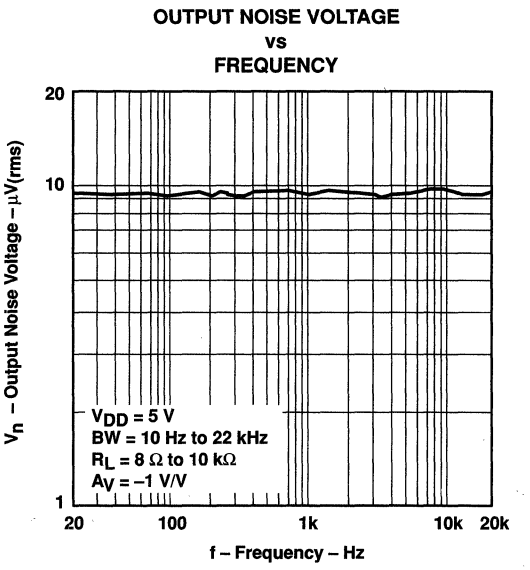

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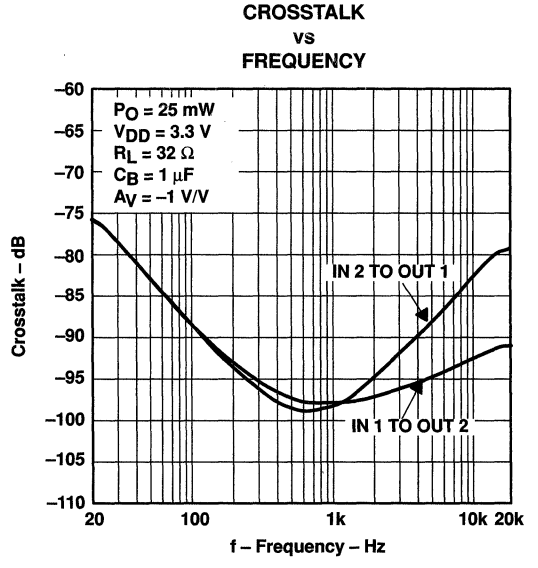

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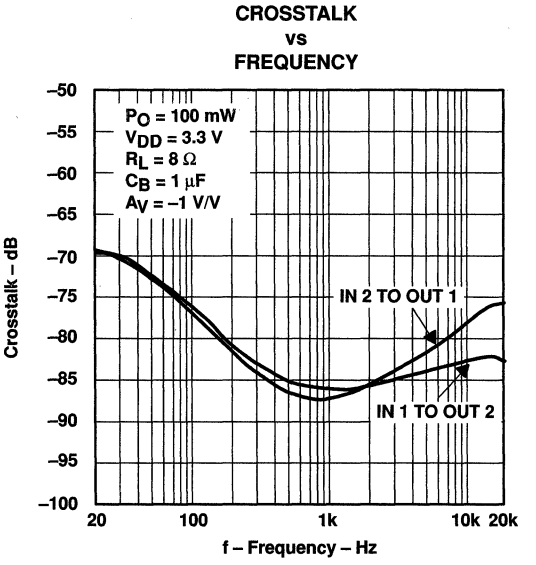


Figure 24

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

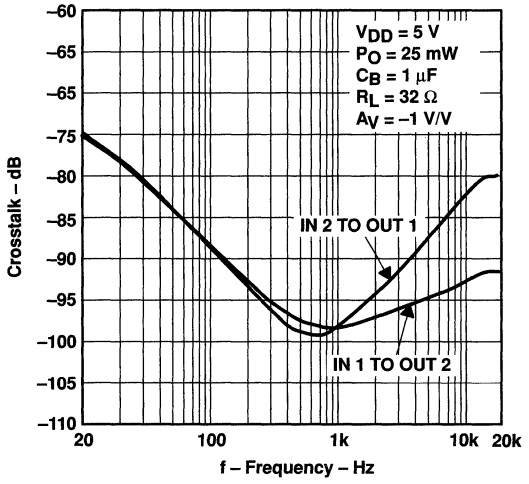


Figure 25

CROSSTALK
vs
FREQUENCY

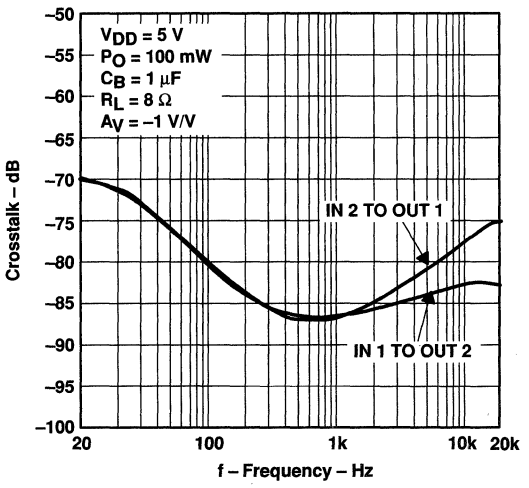


Figure 26

MUTE ATTENUATION
vs
FREQUENCY

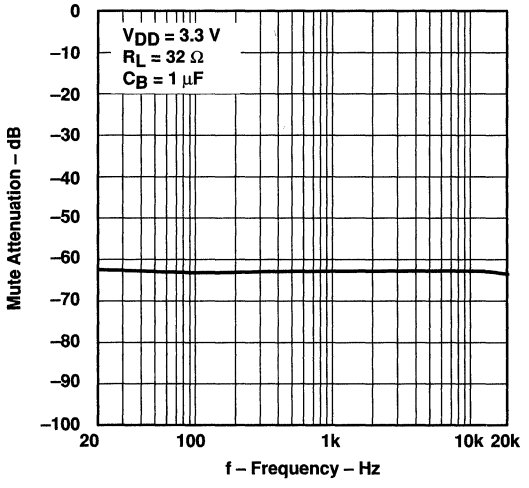


Figure 27

MUTE ATTENUATION
vs
FREQUENCY

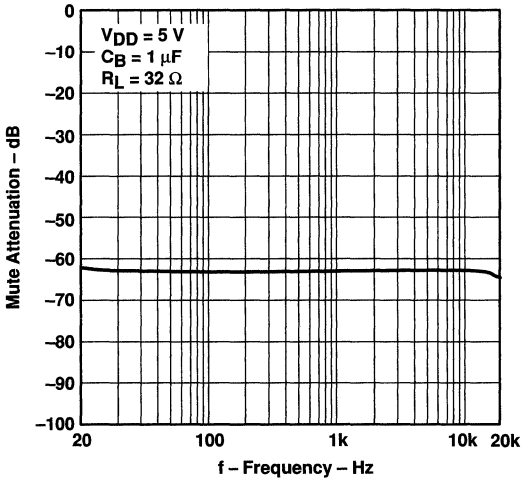


Figure 28

TYPICAL CHARACTERISTICS

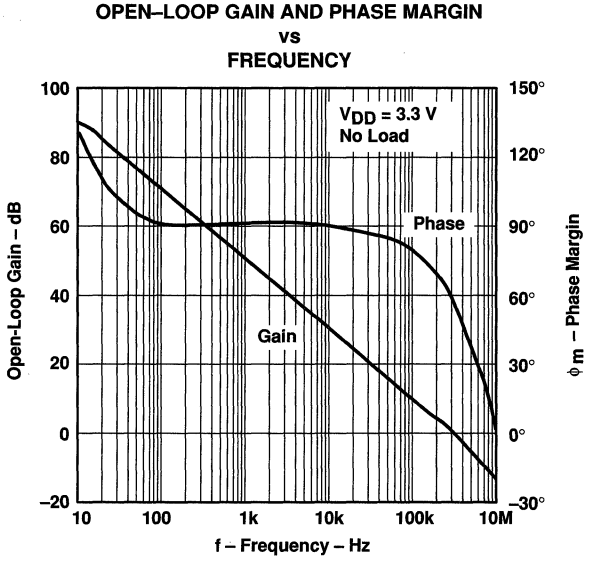


Figure 29

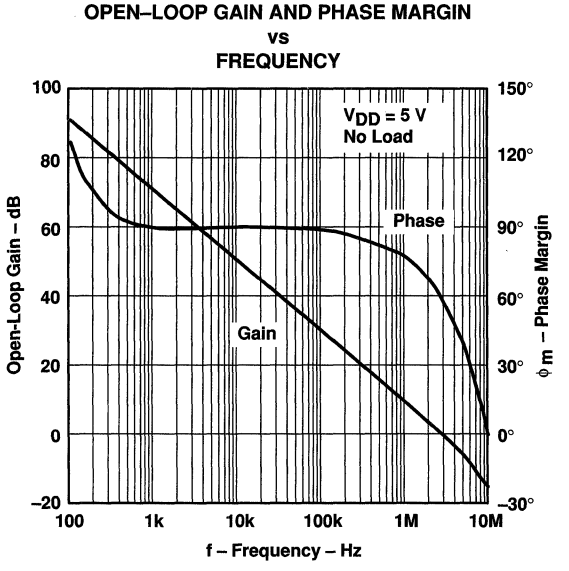


Figure 30

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

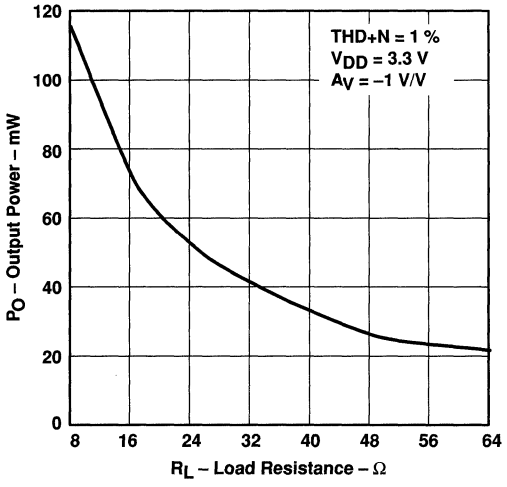


Figure 31

OUTPUT POWER
vs
LOAD RESISTANCE

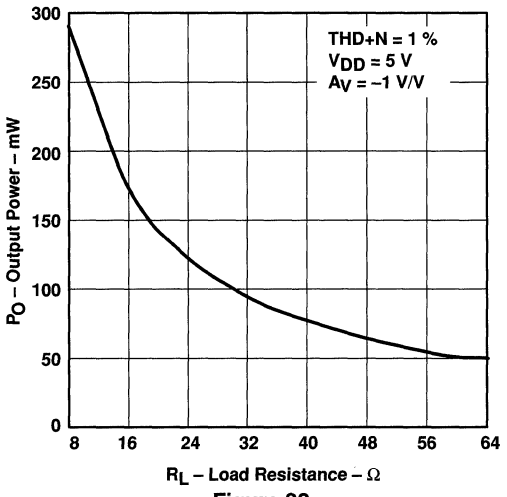


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

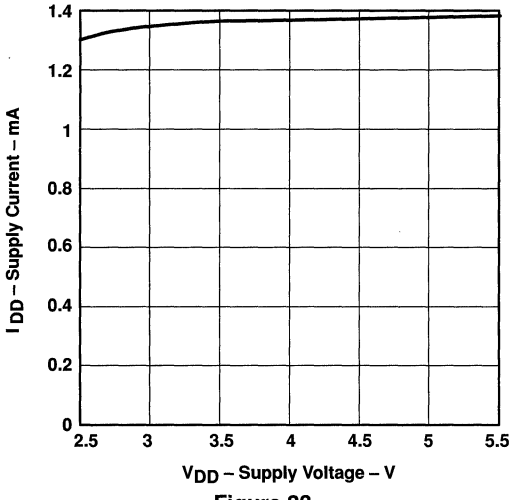


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

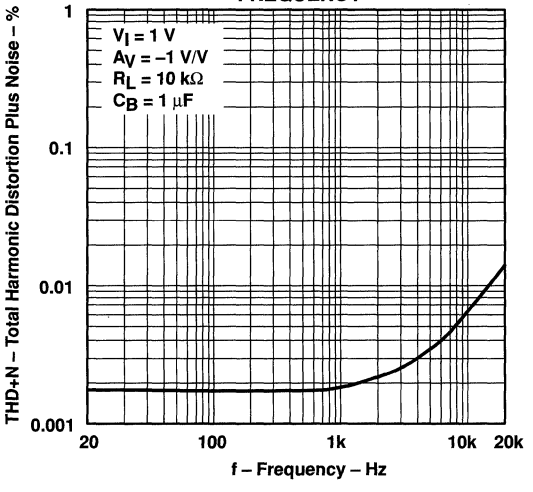


Figure 34

TYPICAL CHARACTERISTICS

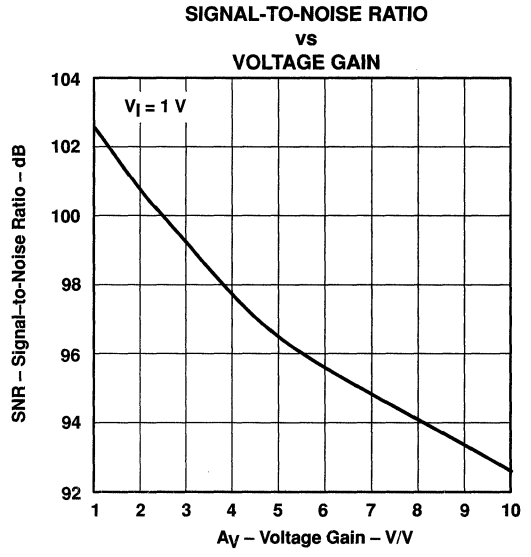


Figure 35

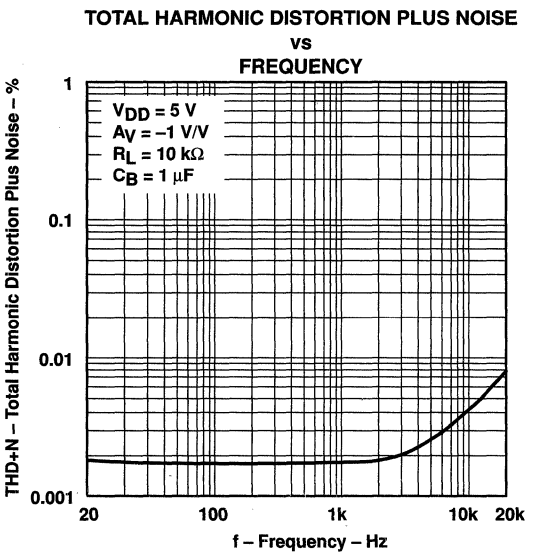


Figure 36

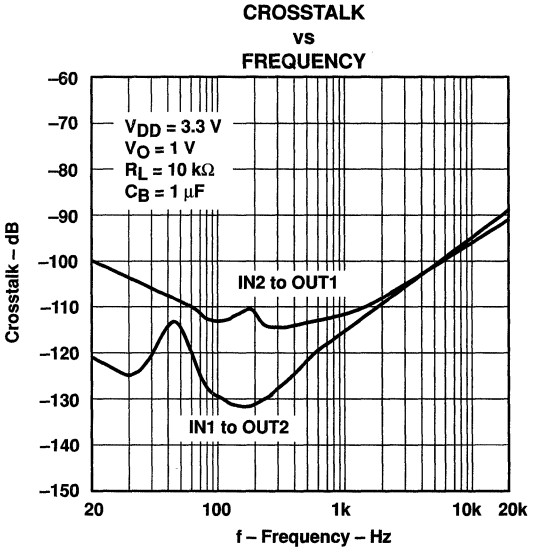


Figure 37

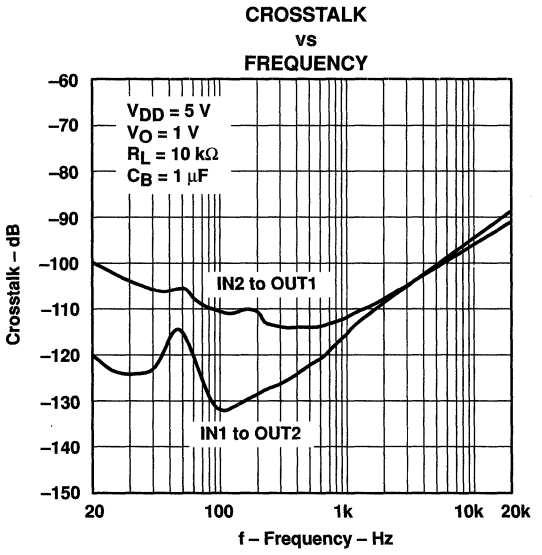


Figure 38

TYPICAL CHARACTERISTICS

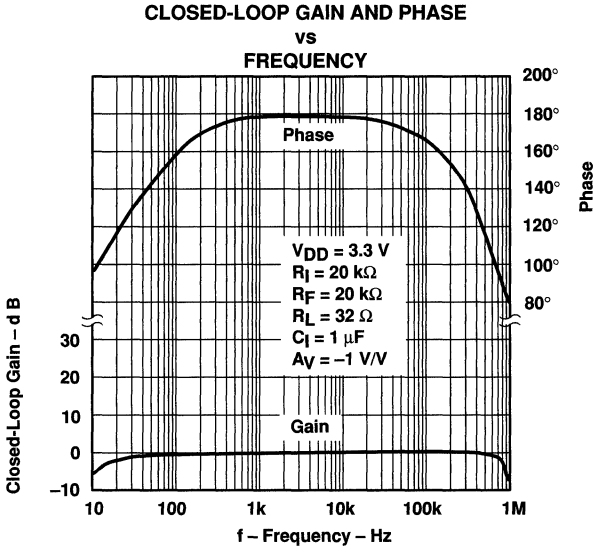


Figure 39

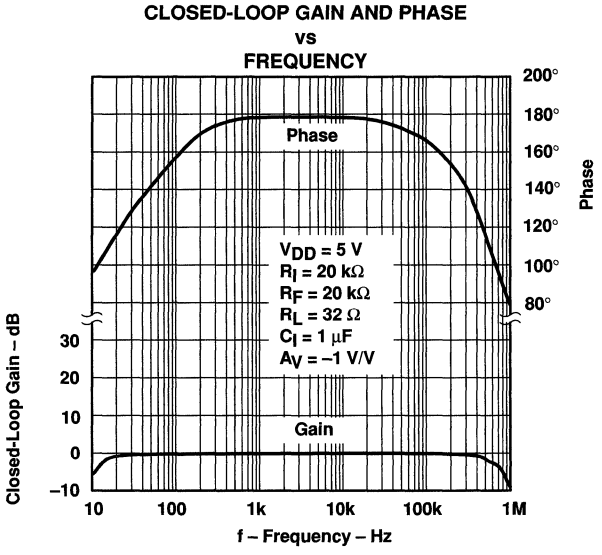


Figure 40

TYPICAL CHARACTERISTICS

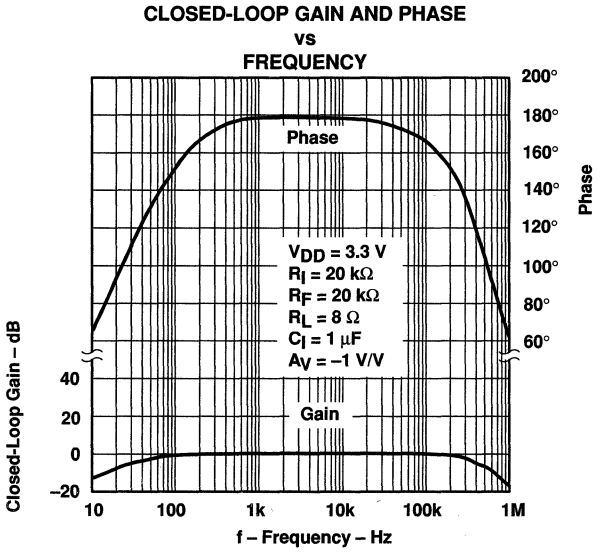


Figure 41

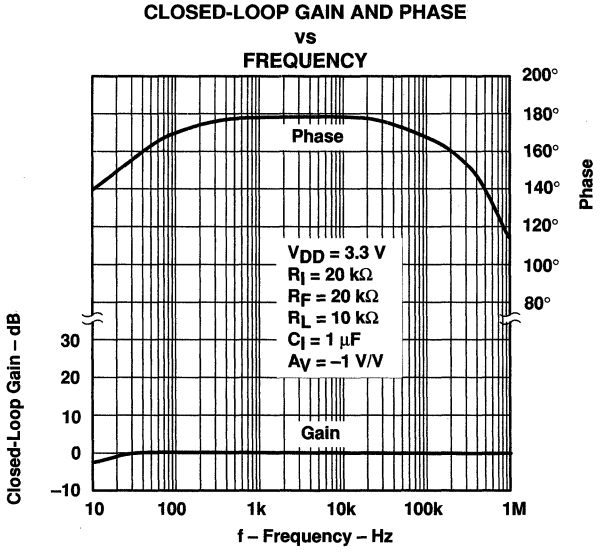


Figure 42

TYPICAL CHARACTERISTICS

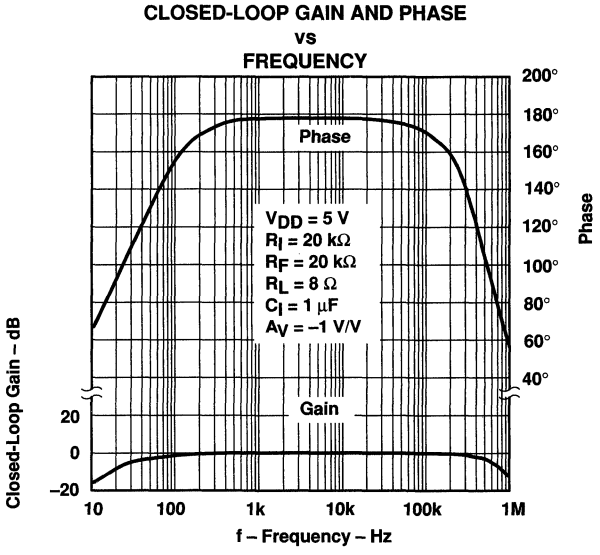


Figure 43

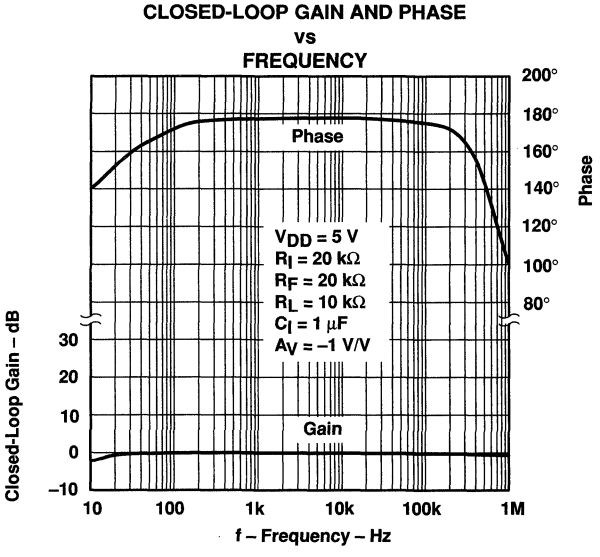


Figure 44

TYPICAL CHARACTERISTICS

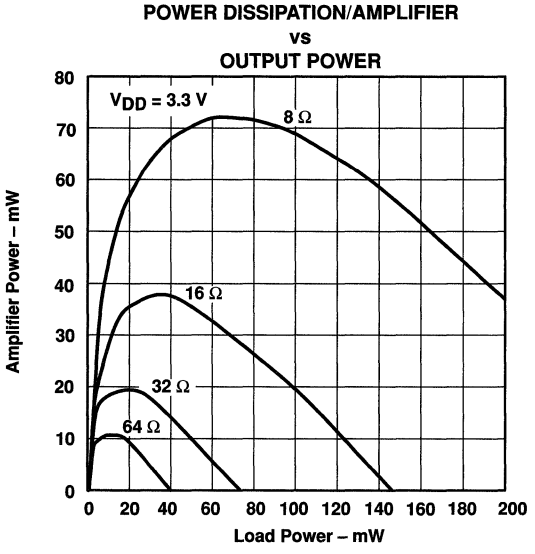


Figure 45

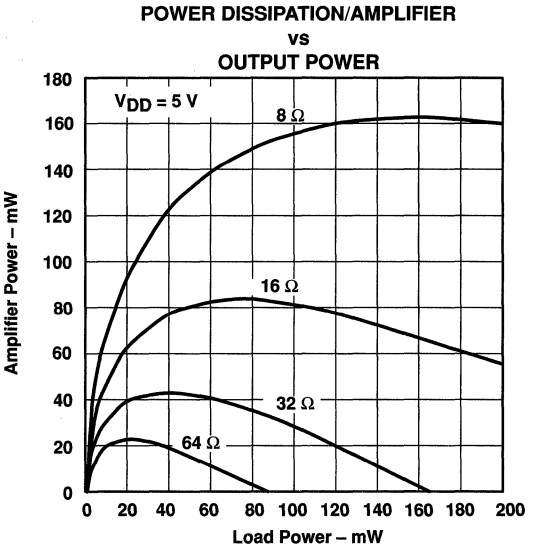


Figure 46

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA102 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA102 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be −1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example, if R_F is 100 kΩ and C_F is 5 pF then $f_{c(\text{lowpass})}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(\text{highpass})}} \tag{5}$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA102 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \tag{6}$$

As an example, consider a circuit where C_B is 1 μF, C_I is 1 μF, and R_I is 20 kΩ. Inserting these values into the equation 9 results in: $6.25 \leq 50$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{8}$$

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

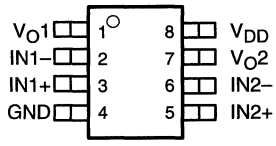
5-V versus 3.3-V operation

The TPA102 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA102 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed when $V_{O(PP)} = 4$ V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

SLOS212C – AUGUST 1998 – REVISED MARCH 2000

- 150-mW Stereo Output
- Wide Range of Supply Voltages
  - Fully Specified for 3.3 V and 5 V Operation
  - Operational From 2.5 V to 5.5 V
- Thermal and Short-Circuit Protection
- Surface Mount Packaging
  - PowerPAD™ MSOP
  - SOIC
- Standard Operational Amplifier Pinout

D OR DGN PACKAGE
(TOP VIEW)

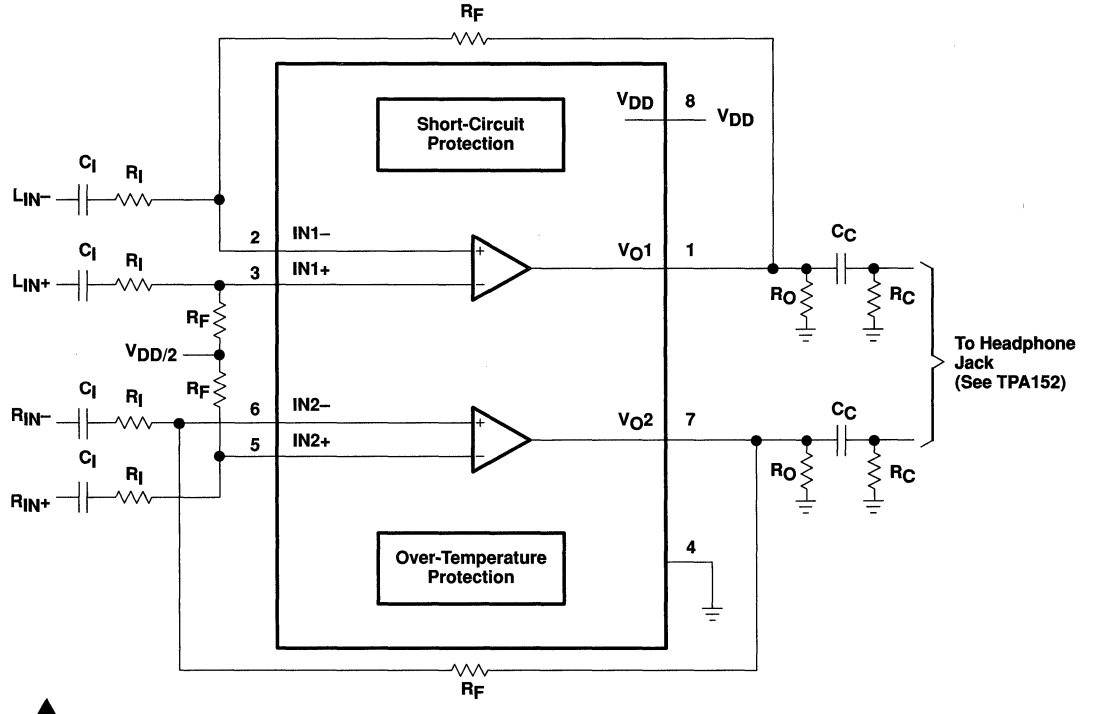


description

The TPA112 is a stereo audio power amplifier packaged in an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA112D	TPA112DGN	TI AAD

† The D and DGN package is available in left-ended tape and reel only (e.g., TPA112DR, TPA112DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN1+	3	I	IN1+ is the noninverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
IN2+	5	I	IN2+ is the noninverting input for channel 2.
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_O1	1	O	V_O1 is the audio output for channel 1.
V_O2	7	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Differential input voltage, V_I ..... –0.3 V to V_{DD} + 0.3 V
Input current, I_I ..... ±2.5 µA
Output current, I_O ..... ±250 mA
Continuous total power dissipation ..... internally limited
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W‡	17.1 mW/°C	1.37 W	1.11 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		83		dB
$I_{DD(q)}$	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			10	50	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 70 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		58°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		76		dB
$I_{DD(q)}$	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			60	100	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 150 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		56°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20–20 kHz		0.5%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		58°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20–20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		56°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Power output	3, 6, 9, 12, 15, 18
PSSR	Power supply rejection ratio	vs Frequency	19, 20
V_n	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23 – 26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain	vs Frequency	29, 30
	Phase margin	vs Frequency	29, 30
	Phase	vs Frequency	39 – 44
	Output power	vs Load resistance	31, 32
I_{CC}	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39 – 44
	Power dissipation/amplifier	vs Output power	45, 46

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

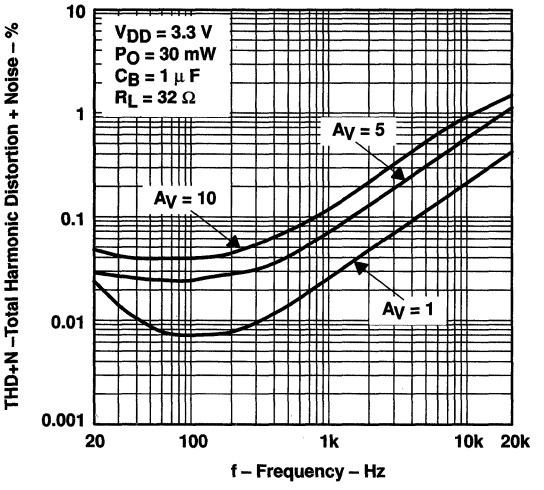


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

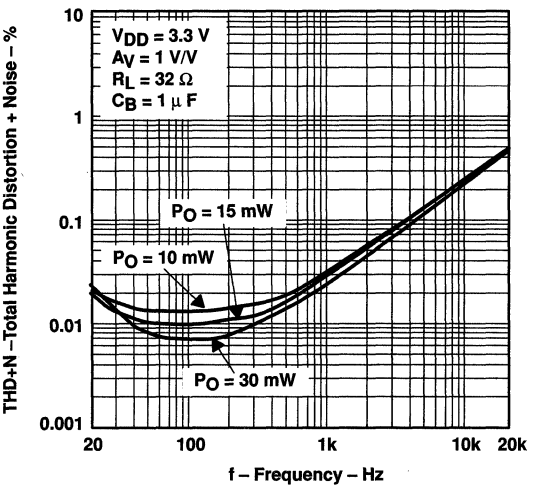


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

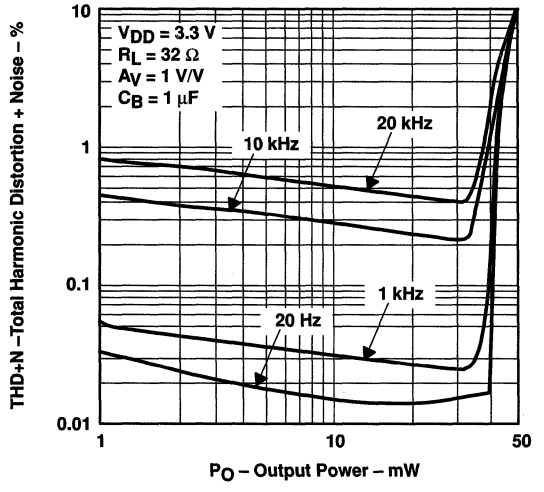


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

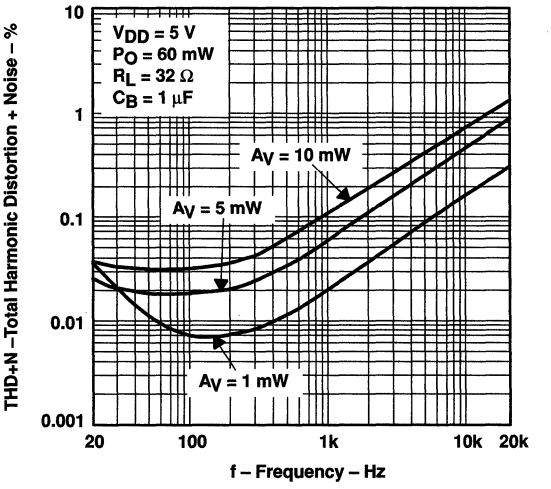


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

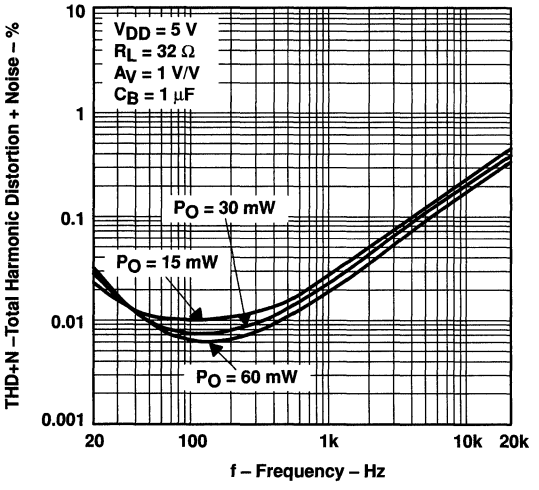


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

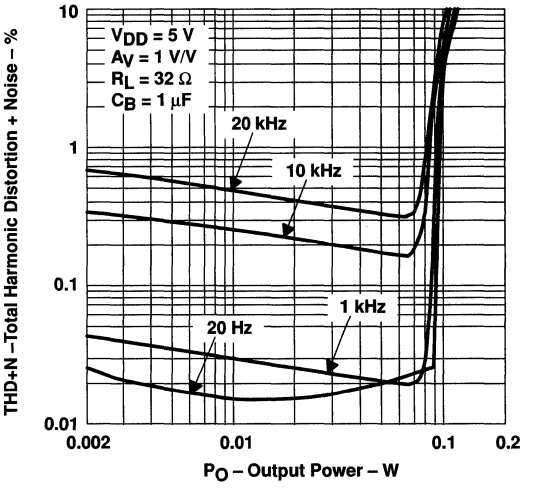


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

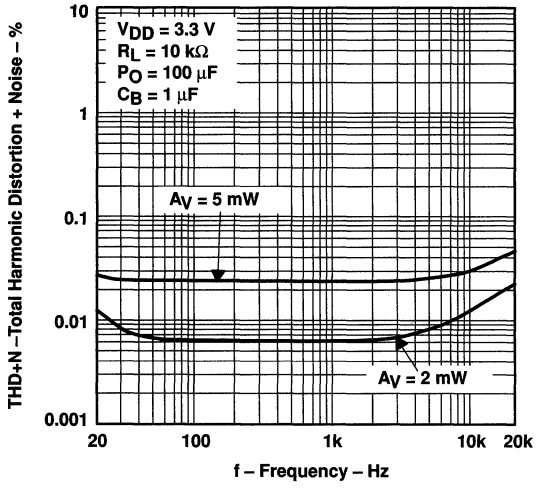


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

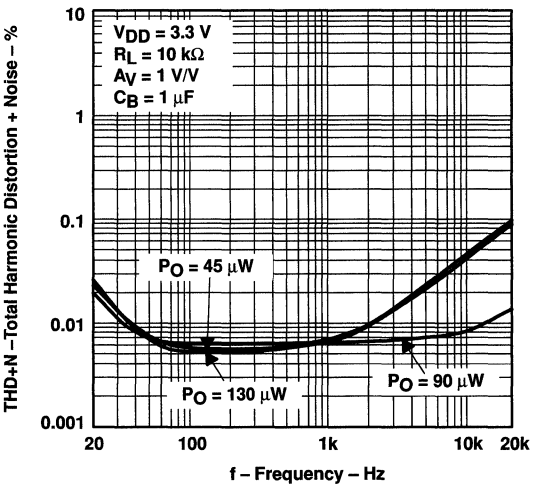


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

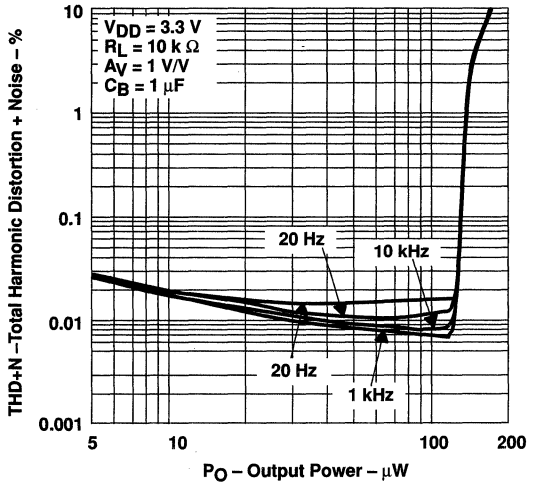


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

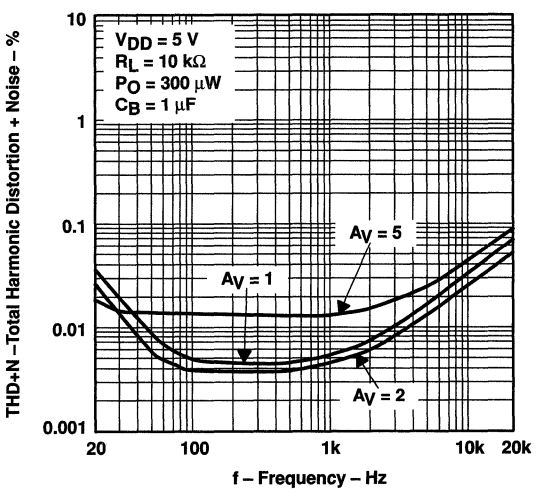


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

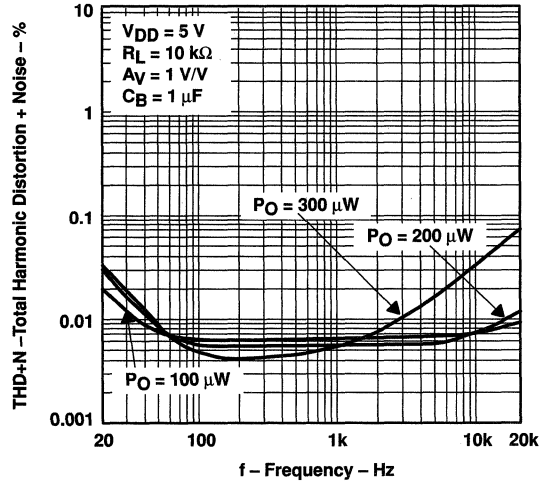


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

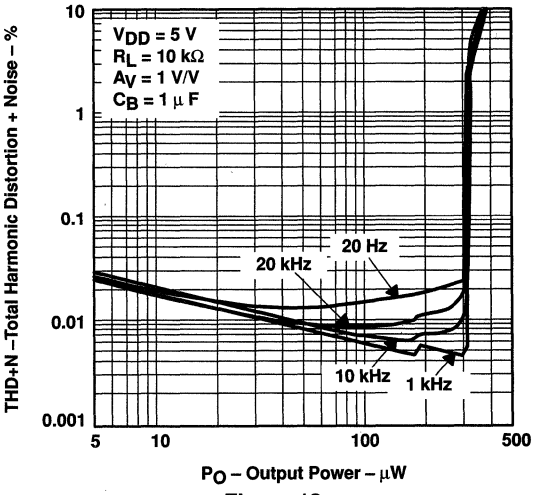


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

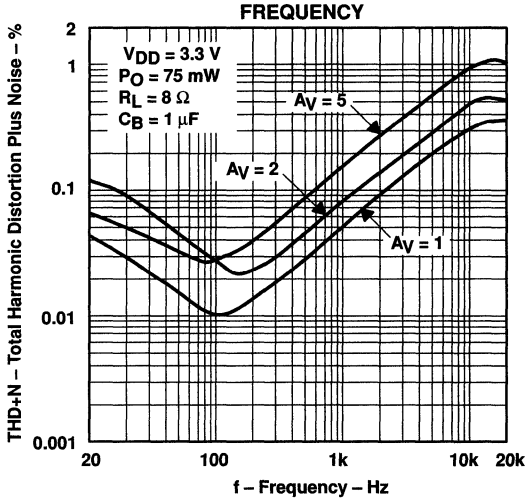


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

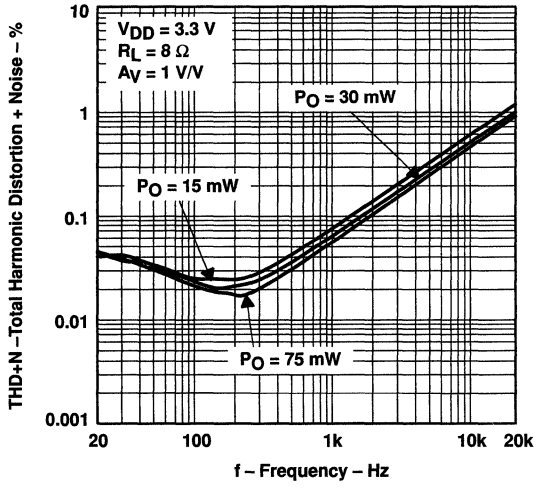


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

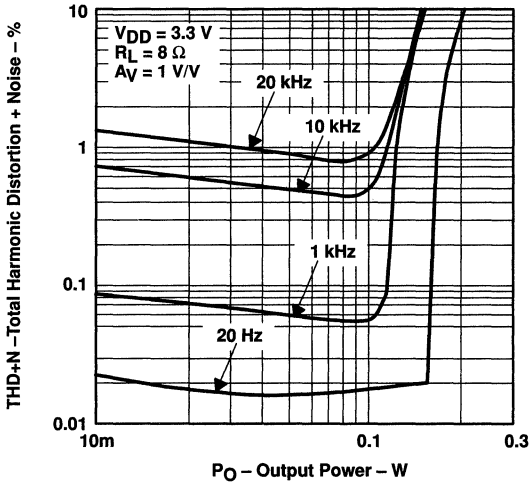


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

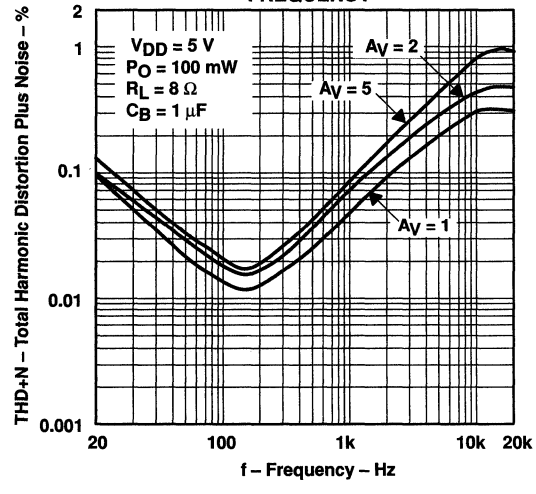


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

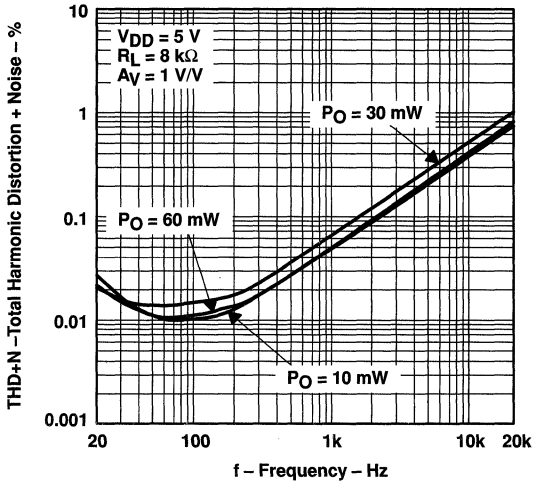


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

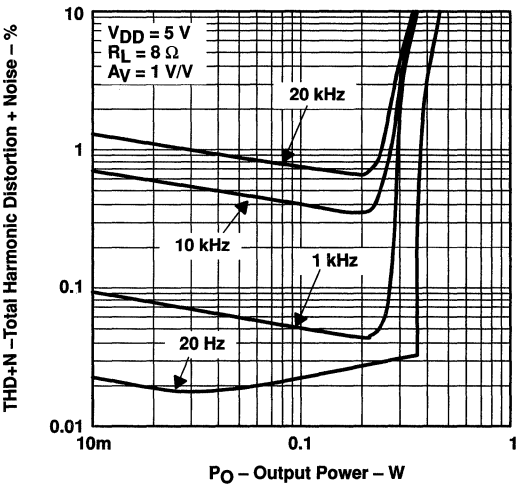


Figure 18

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

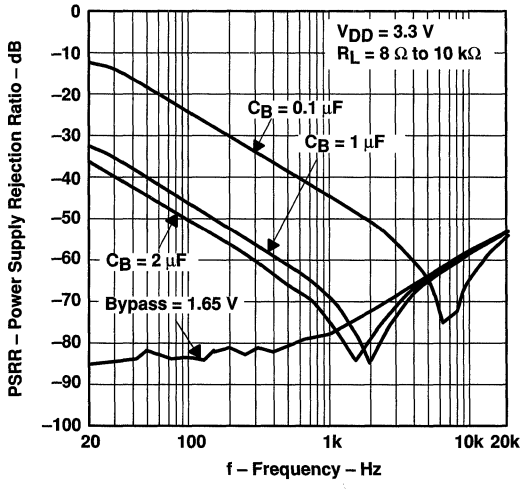


Figure 19

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

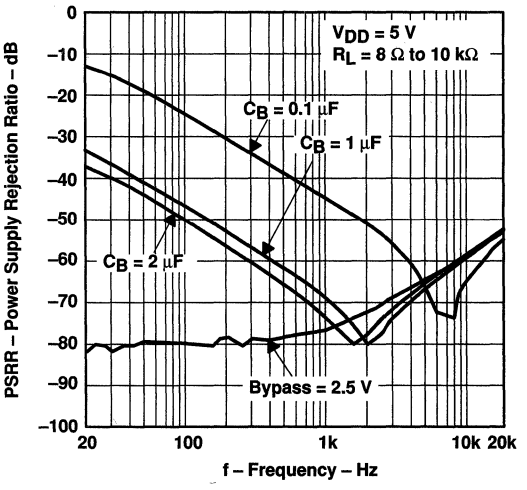


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

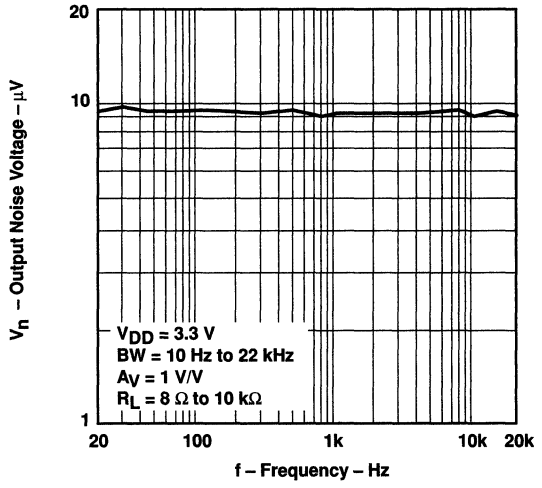


Figure 21

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

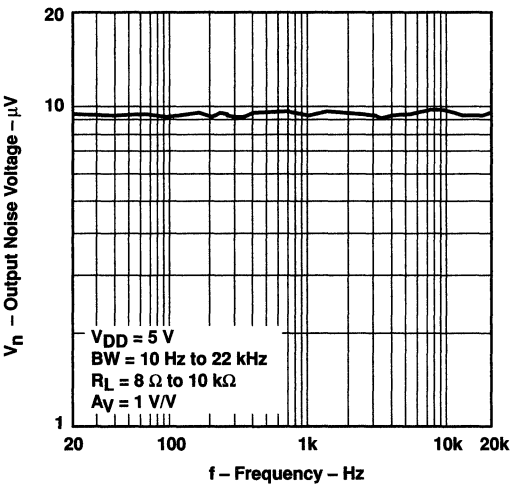


Figure 22

CROSSTALK
vs
FREQUENCY

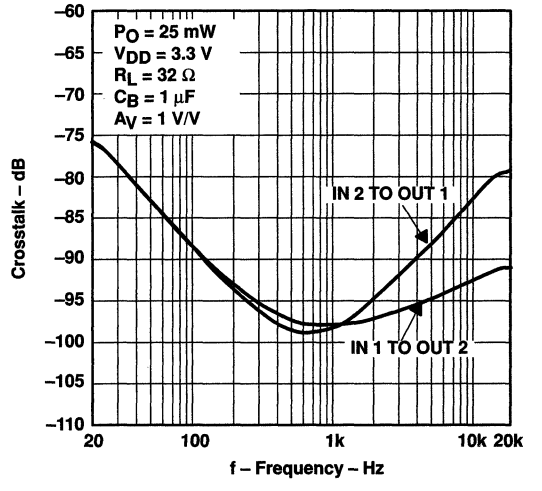


Figure 23

CROSSTALK
vs
FREQUENCY

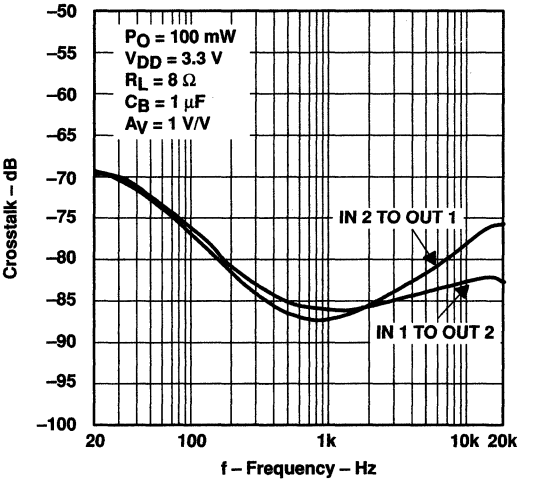


Figure 24

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

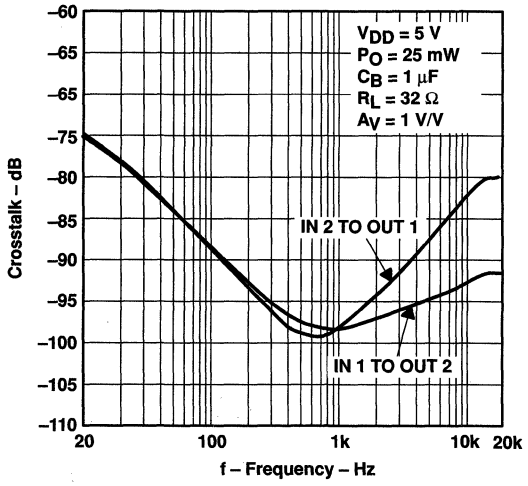


Figure 25

CROSSTALK
vs
FREQUENCY

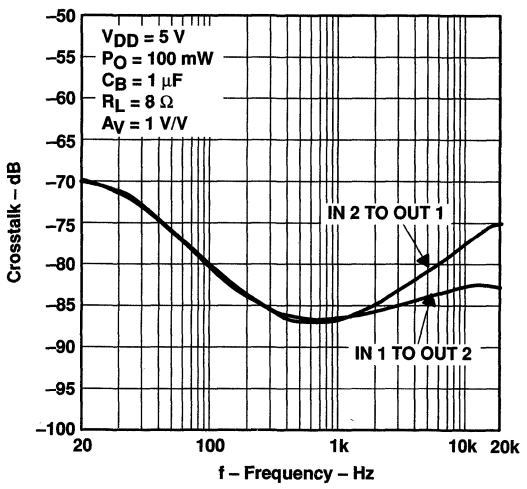


Figure 26

MUTE ATTENUATION
vs
FREQUENCY

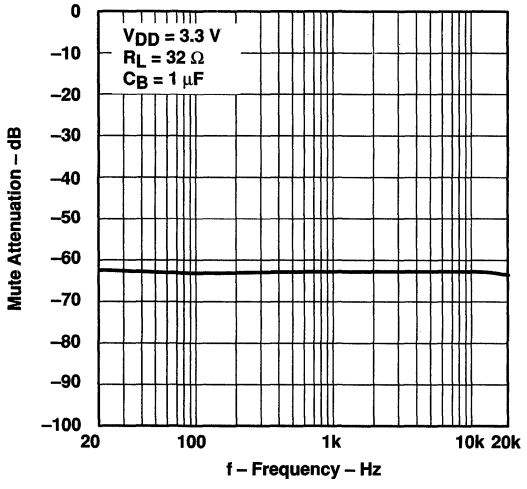


Figure 27

MUTE ATTENUATION
vs
FREQUENCY

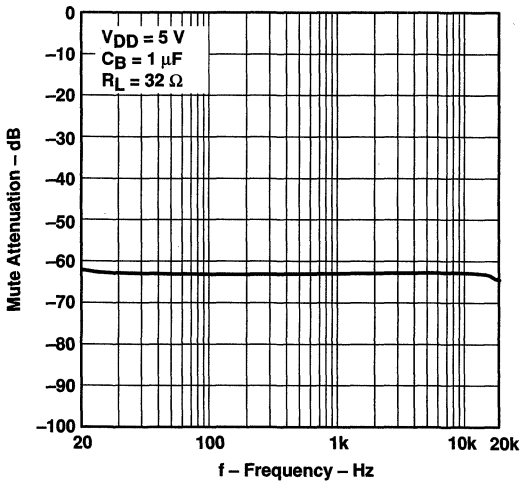


Figure 28

TYPICAL CHARACTERISTICS

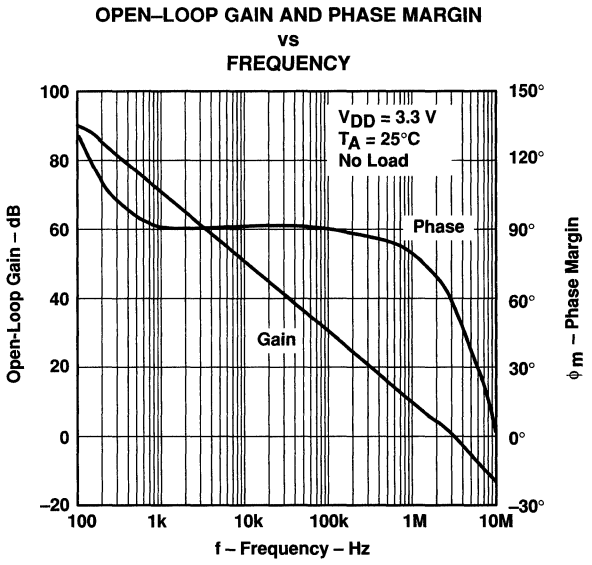


Figure 29

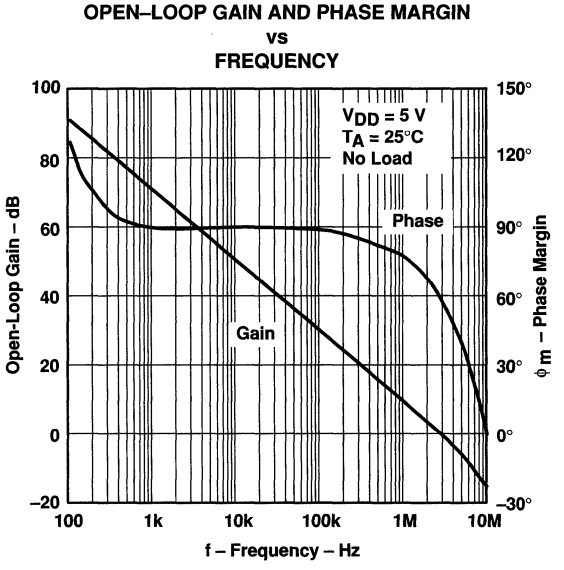


Figure 30

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

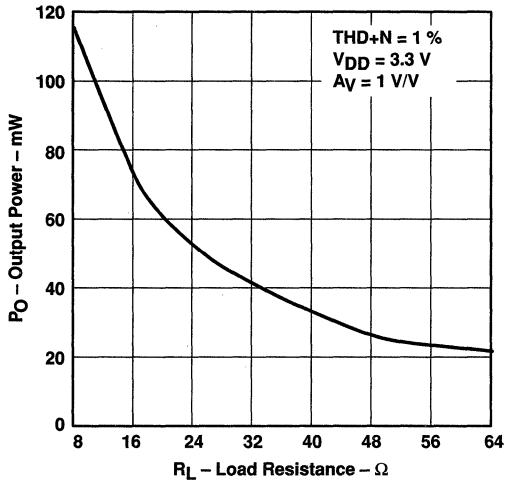


Figure 31

OUTPUT POWER
vs
LOAD RESISTANCE

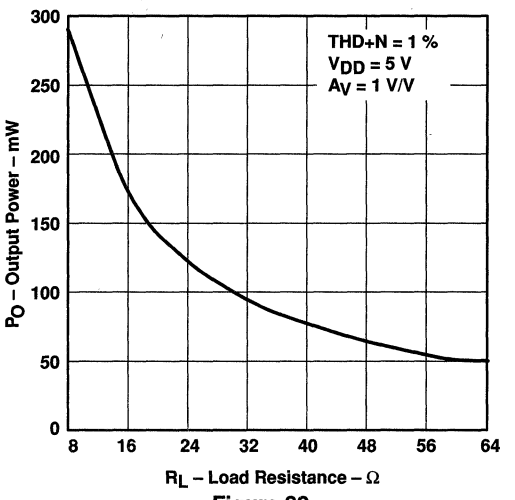


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

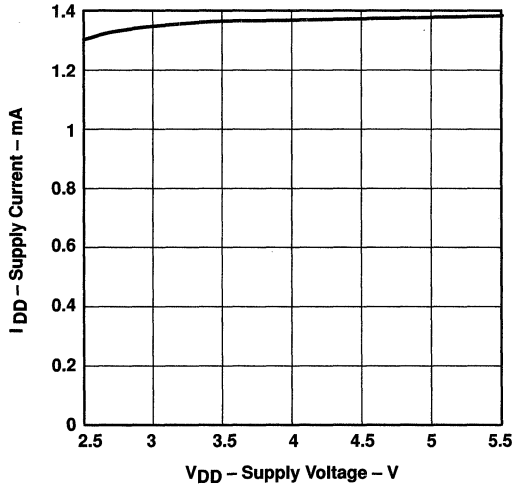


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

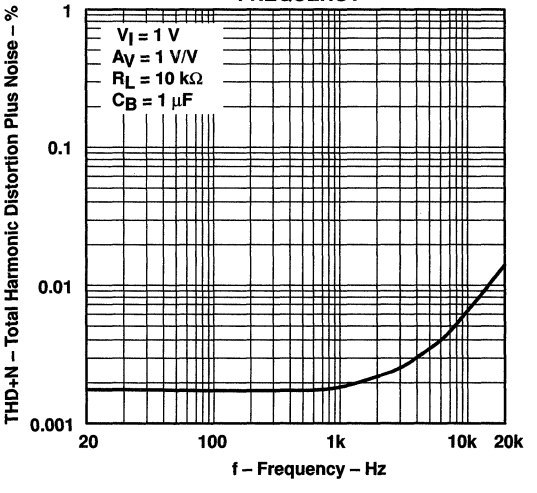


Figure 34

TYPICAL CHARACTERISTICS

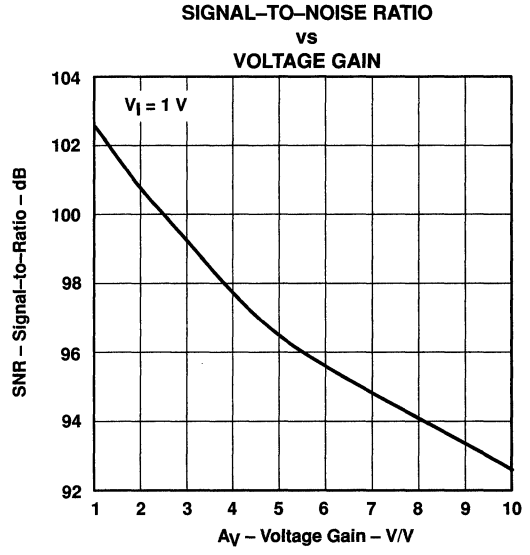


Figure 35

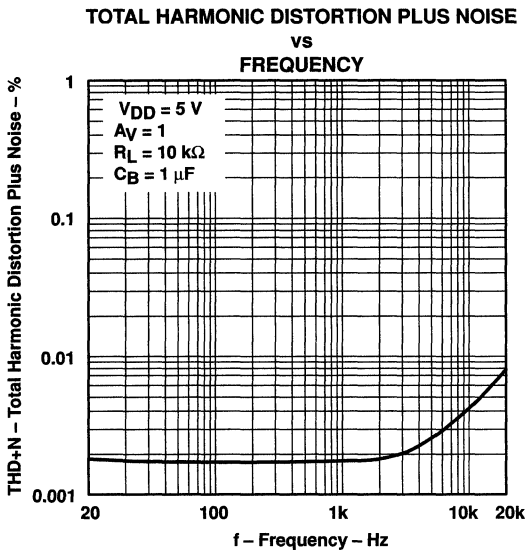


Figure 36

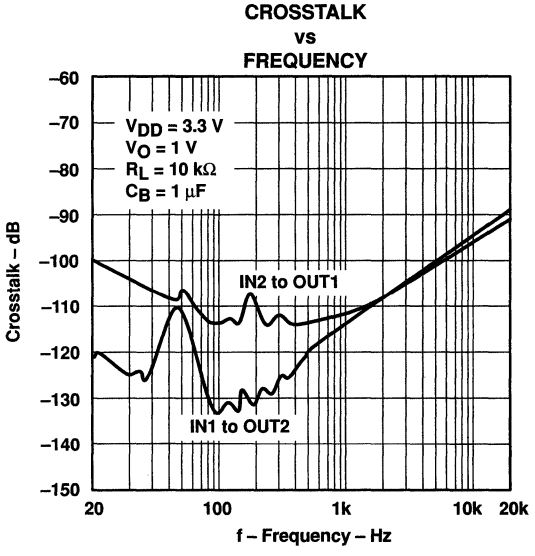


Figure 37

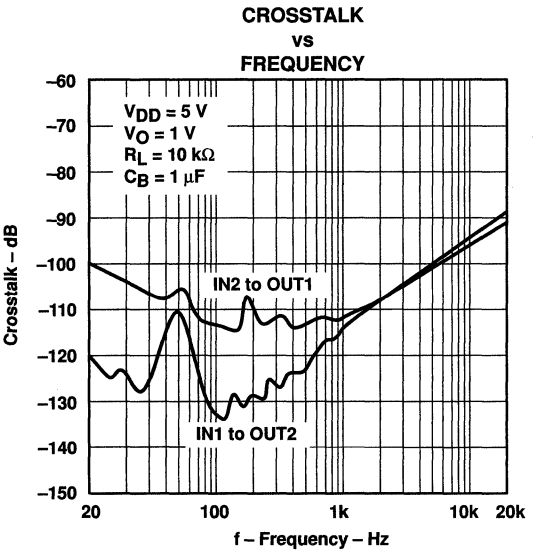


Figure 38

TYPICAL CHARACTERISTICS

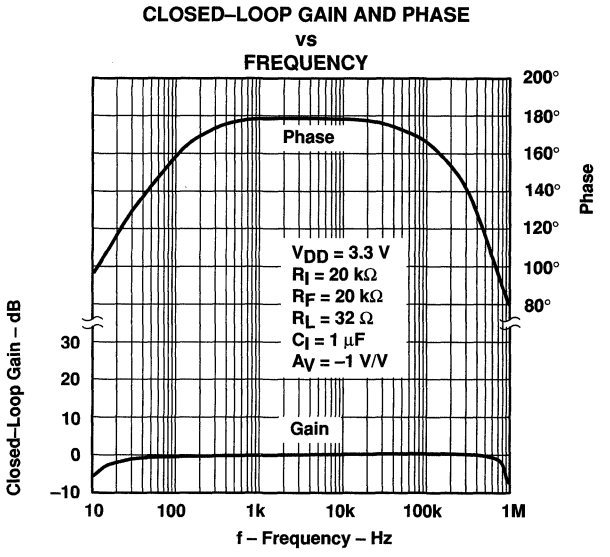


Figure 39

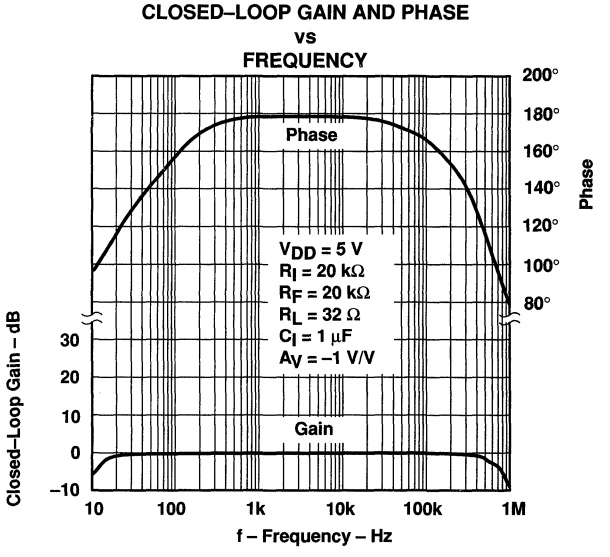


Figure 40

TYPICAL CHARACTERISTICS

CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY

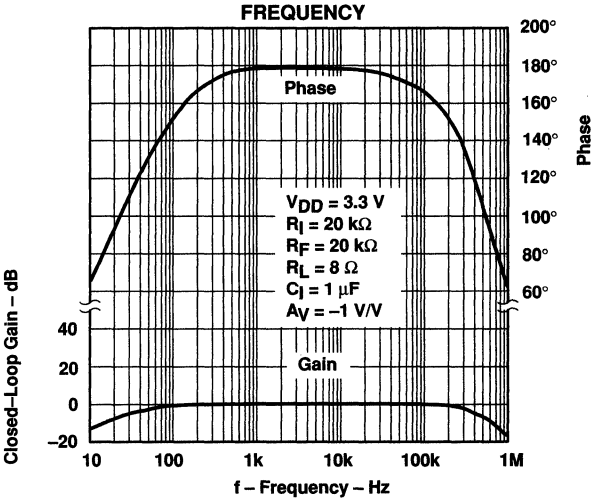


Figure 41

CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY

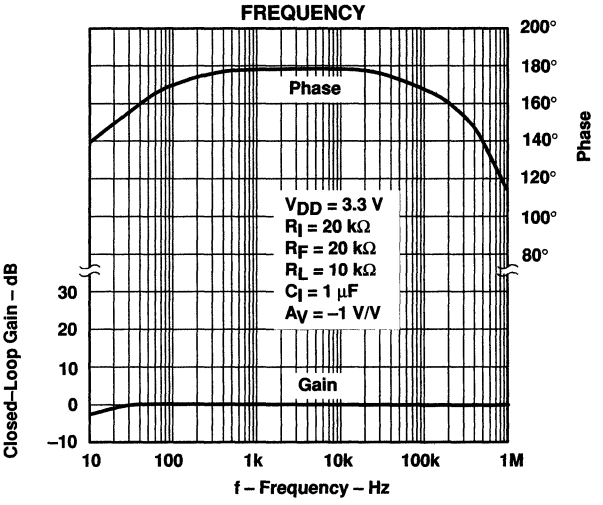


Figure 42

TYPICAL CHARACTERISTICS

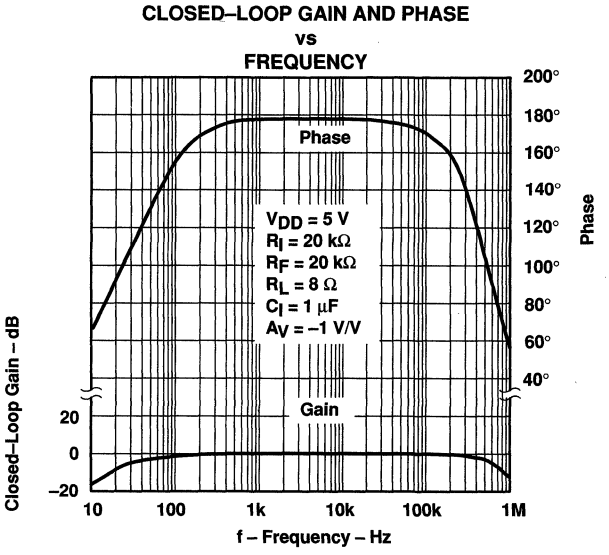


Figure 43

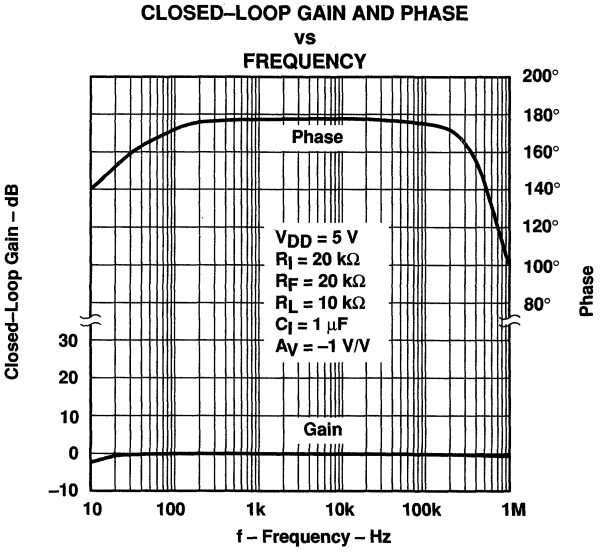


Figure 44

TYPICAL CHARACTERISTICS

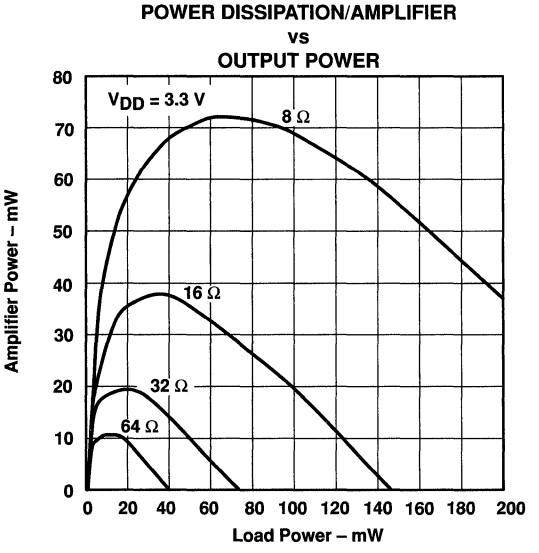


Figure 45

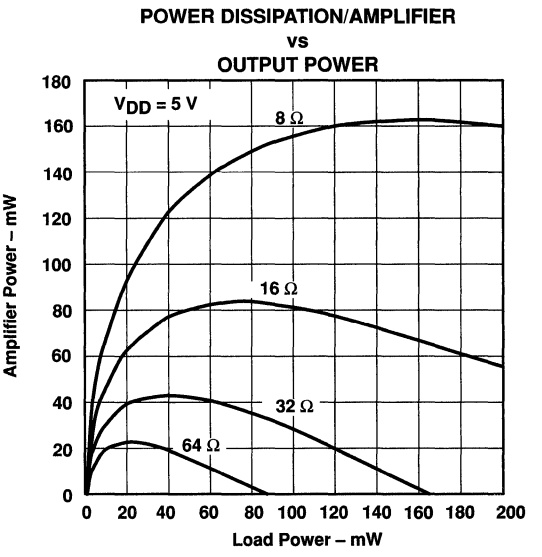


Figure 46

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA112 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA112 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be −1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

APPLICATION INFORMATION

gain setting resistors, R_F and R_I (continued)

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 kΩ and C_F is 5 pF then $f_{co(lowpass)}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{co(highpass)}} \quad (5)$$

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA112 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

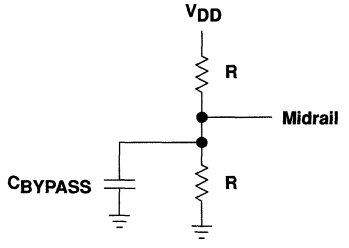
APPLICATION INFORMATION

midrail voltage

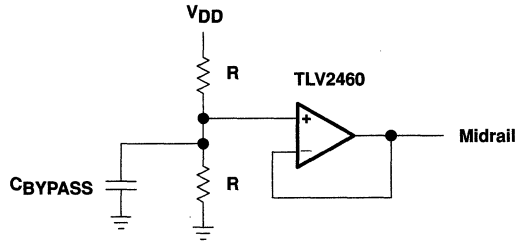
The TPA112 is a single-supply amplifier, so it must be properly biased to accommodate audio signals. Normally, the amplifier is biased at $V_{DD}/2$, but it can actually be biased at any voltage between V_{DD} and ground. However, biasing the amplifier at a point other than $V_{DD}/2$ will reduce the amplifier's maximum output swing. In some applications where the circuitry driving the TPA112 has a different midrail voltage, it might make sense to use the same midrail voltage for the TPA112, and possibly eliminate the use of the dc-blocking caps.

There are two concerns with the midrail voltage source: the amount of noise present, and its output impedance. Any noise present on the midrail voltage source that is not present on the audio input signal will be input to the amplifier, and passed to the output (and increased by the gain of the circuit). Common-mode noise will be cancelled out by the differential configuration of the circuit.

The output impedance of the circuit used to generate the midrail voltage needs to be low enough so as not to be influenced by the audio signal path. A common method of generating the midrail voltage is to form a voltage divider from the supply to ground, with a bypass capacitor from the common node to ground. This capacitor improves the PSRR of the circuit. However, this circuit has a limited range of output impedances, so to achieve very low output impedances, the voltage generated by the voltage divider is fed into a unity-gain amplifier to lower the output impedance of the circuit.



a) Midrail Voltage Generator Using a Simple Resistor-Divider



b) Buffered Midrail Voltage Generator to Provide Low Output Impedance

Figure 47. Midrail Voltage Generator

If a voltage step is applied to a speaker, it will pop. To reduce popping, the midrail voltage should rise at a sub-sonic rate; that is, a rate less than the rise time of a 20-Hz waveform. If the voltage rises faster than that, there is the possibility of a pop from the speaker.

Pop can also be heard in the speaker if the midrail voltage rises faster than either the input coupling capacitor, or the output coupling capacitor. If midrail rises first, then the charging of the input and output capacitors will be heard in the speaker. To keep this noise as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{(C_B \times R_{SOURCE})} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \qquad (6)$$

Where C_{BYPASS} is the value of the bypass capacitor, and R_{SOURCE} is the equivalent source impedance of the voltage divider (the parallel combination of the two resistors). For example, if the voltage divider is constructed using two 20-kΩ resistors, then R_{SOURCE} is 10 kΩ.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from the resistor divider with equivalent resistance of R_{SOURCE}. To keep the start-up pop as low as possible, the relationship shown in equation 7 should be maintained.

$$\frac{1}{(C_B \times R_{SOURCE})} \leq \frac{1}{(C_I R_I)} \tag{7}$$

As an example, consider a circuit where C_B is 1 µF, R_{SOURCE} = 160 kΩ, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into the equation 9 results in:

$$6.25 \leq 50$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 8.

$$f_{(out\ high)} = \frac{1}{2\pi R_L C_C} \tag{8}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

output pull-down resistor, $R_C + R_O$

Placing a 100-Ω resistor, R_C, from the output side of the coupling capacitor to ground insures the coupling capacitor, C_C, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones.

Placing a 20-kΩ resistor, R_O, from the output of the IC to ground insures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10-kΩ loads.

using low-ESR capacitors

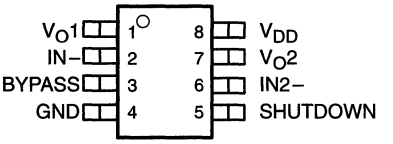
Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA112 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA112 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed when $V_{O(PP)} = 4$ V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

- 150 mW Stereo Output
- PC Power Supply Compatible
  - Fully Specified for 3.3 V and 5 V Operation
  - Operation to 2.5 V
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
  - PowerPAD™ MSOP
  - SOIC
- Pin Compatible With LM4880 and LM4881 (SOIC)

D OR DGN PACKAGE
(TOP VIEW)

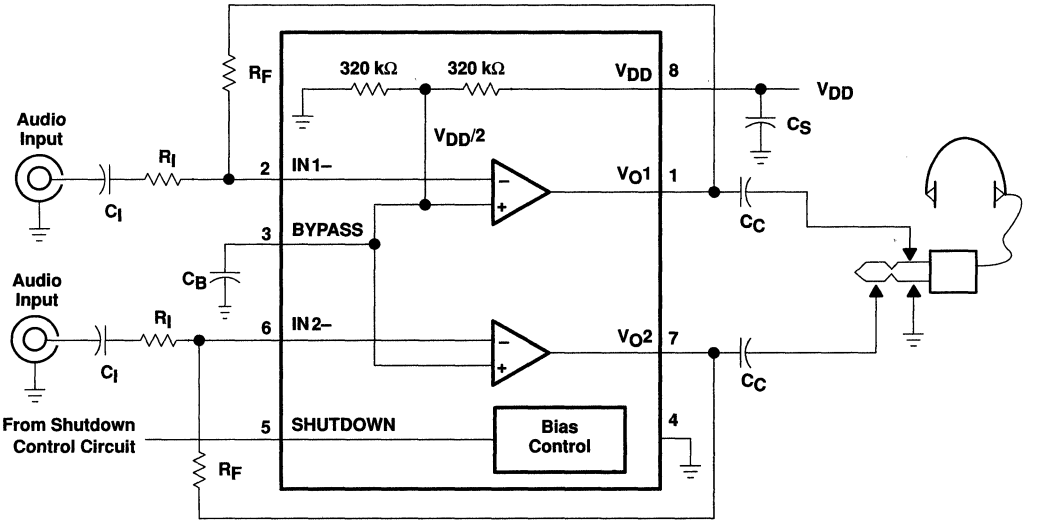


description

The TPA122 is a stereo audio power amplifier packaged in either an 8-pin SOIC, or an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

typical application circuit



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA122D	TPA122DGN	TI AAE

† The D and DGN package is available in left-ended tape and reel only (e.g., TPA122DR, TPA122DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_O1	1	O	V_O1 is the audio output for channel 1.
V_O2	7	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation ..... internally limited
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W‡	17.1 mW/°C	1.37 W	1.11 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		83		dB
I_{DD}	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			10	50	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 70 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/Channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		76		dB
I_{DD}	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			60	100	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		70†		mW
THD+N	Total harmonic distortion + noise	P_O = 150 mW, 20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10, THD <5%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection ratio	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20–20 kHz		0.5%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		58°		
	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20–20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		56°		
	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		μV(rms)

† Measured at 1 kHz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Power output	3, 6, 9, 12, 15, 18
	Supply ripple rejection	vs Frequency	19, 20
V_n	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23 – 26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain and phase margin	vs Frequency	29, 30
	Output power	vs Load resistance	31, 32
	Closed-Loop gain and phase	vs Frequency	39 – 44
	Output power	vs Load resistance	31, 32
I_{DD}	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39 – 44
	Power dissipation/amplifier	vs Output power	45, 46

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

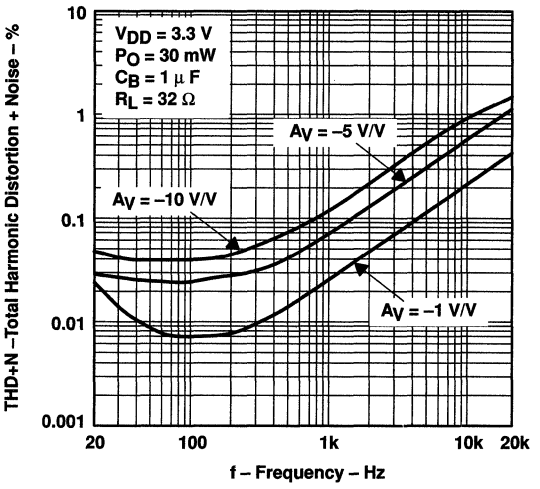


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

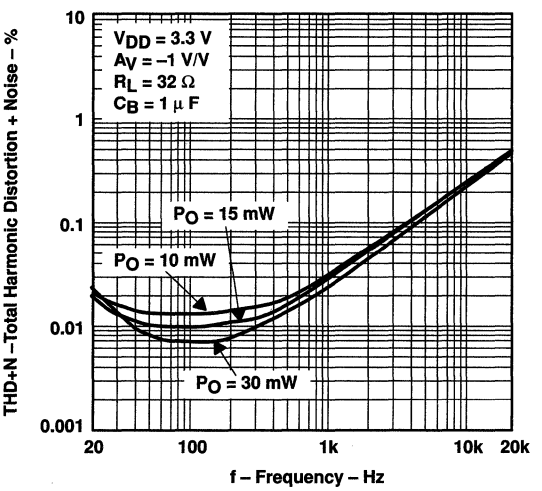


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

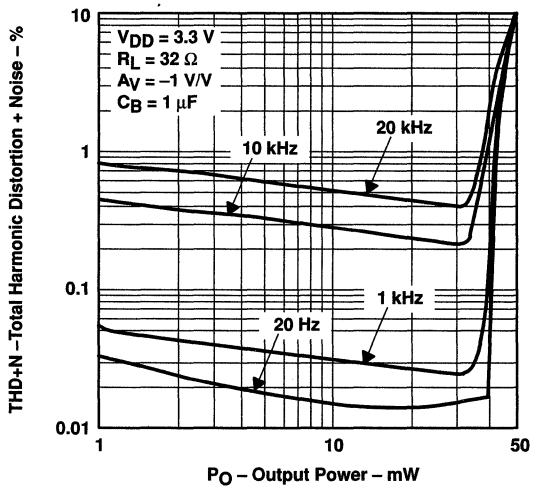


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

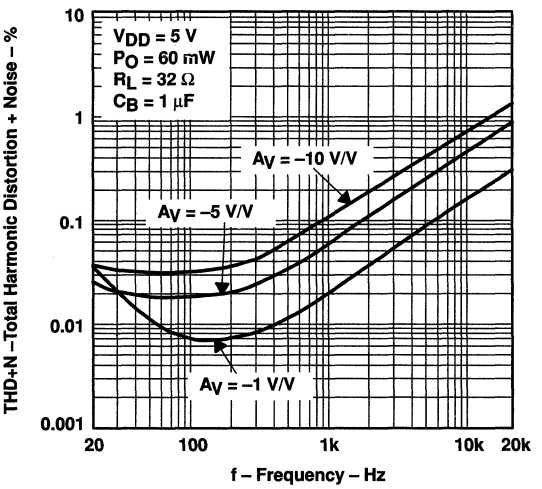


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

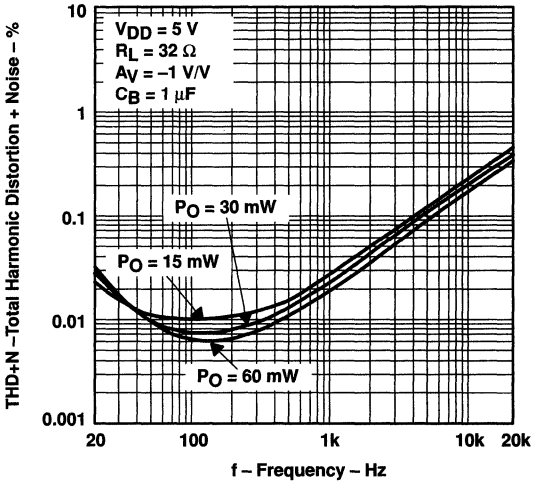


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

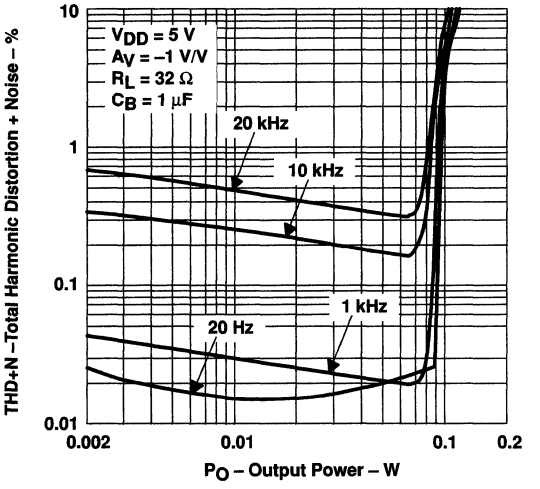


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

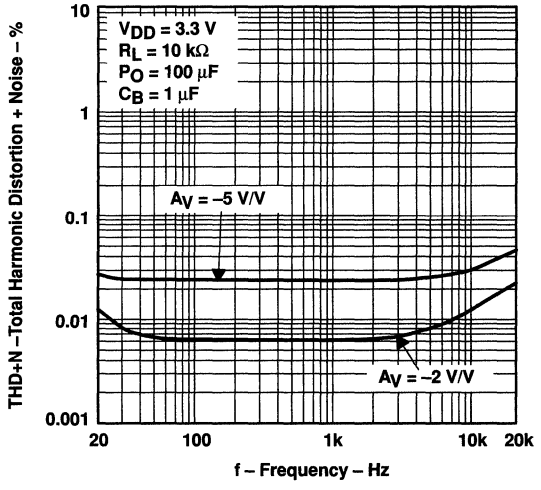


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

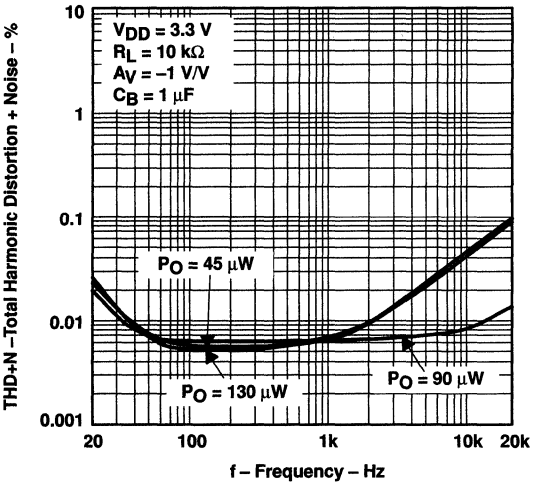


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

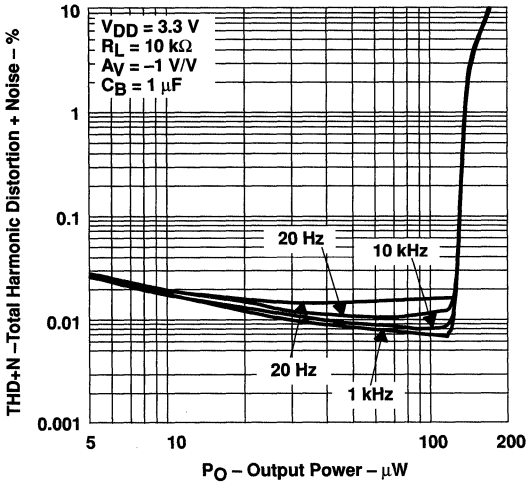


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

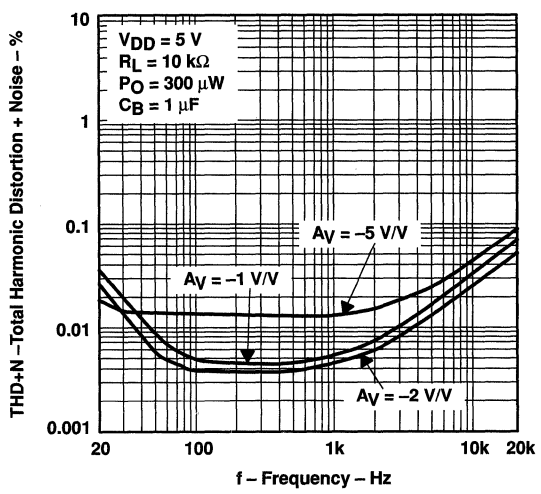


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

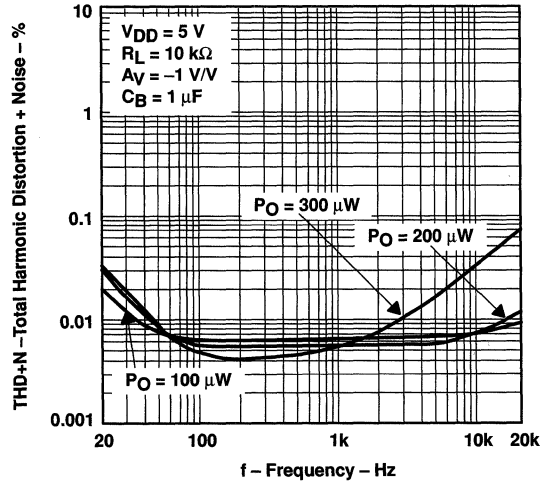


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

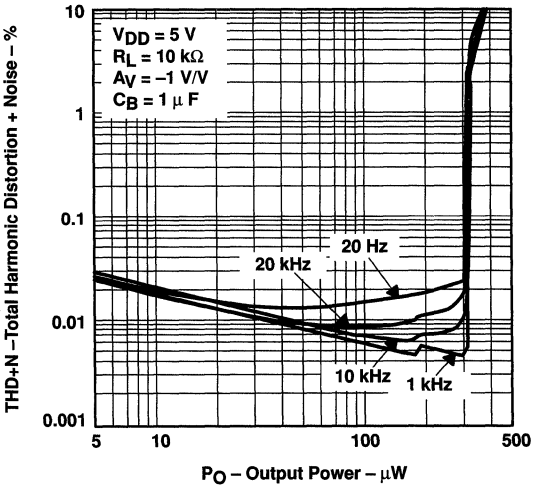


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

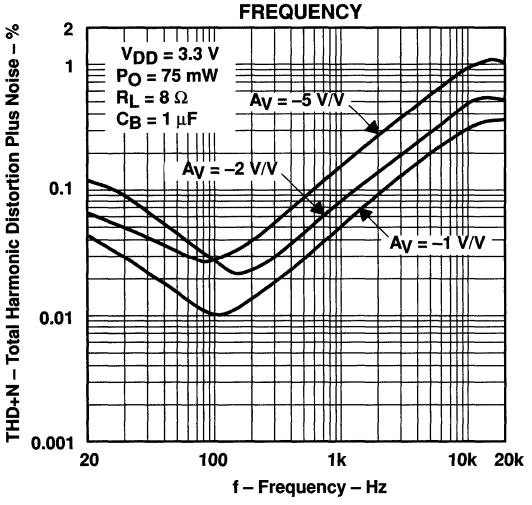


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

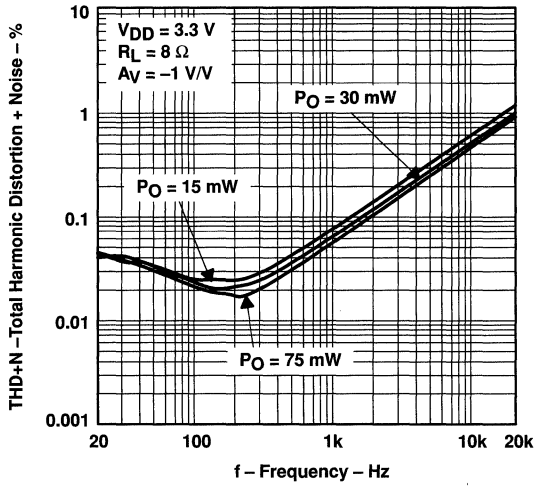


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

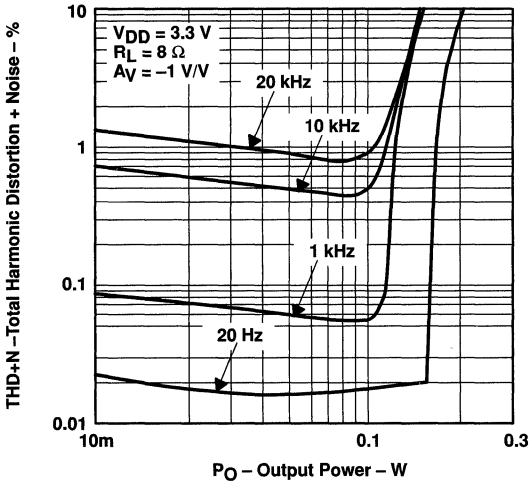


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

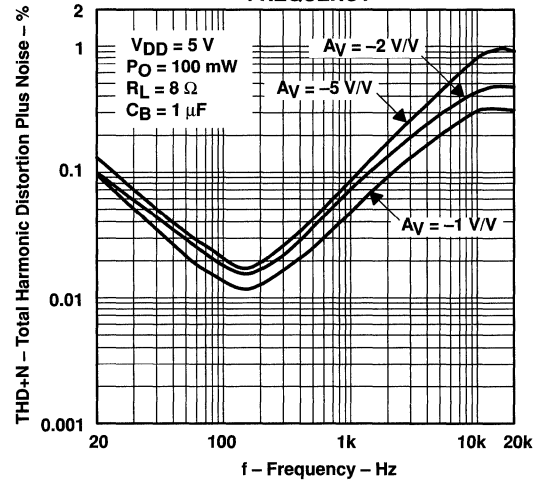


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

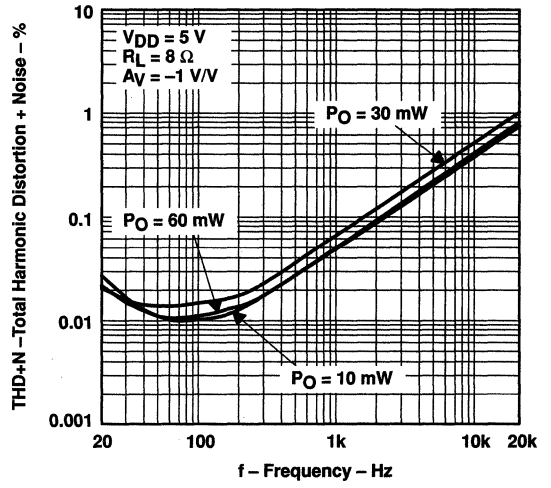


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

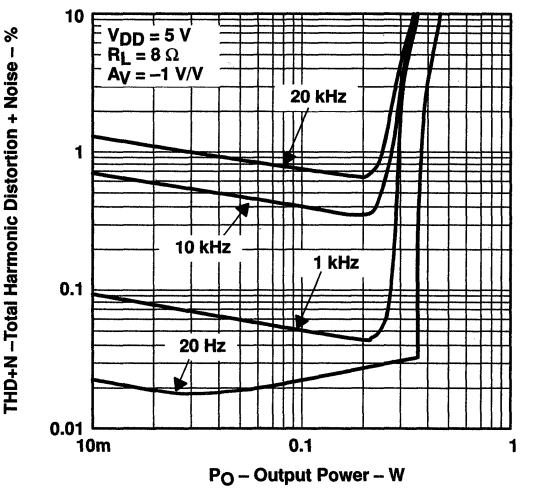


Figure 18

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

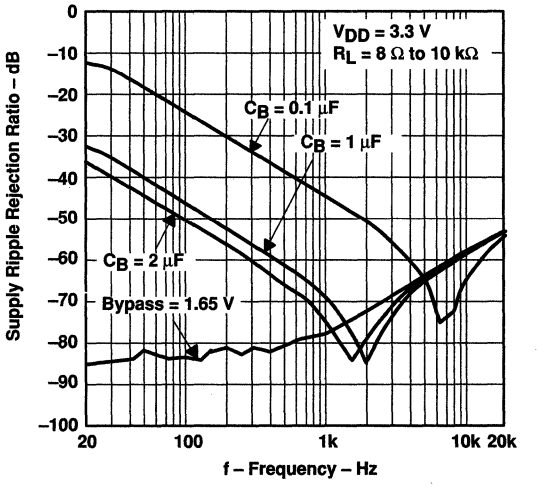


Figure 19

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

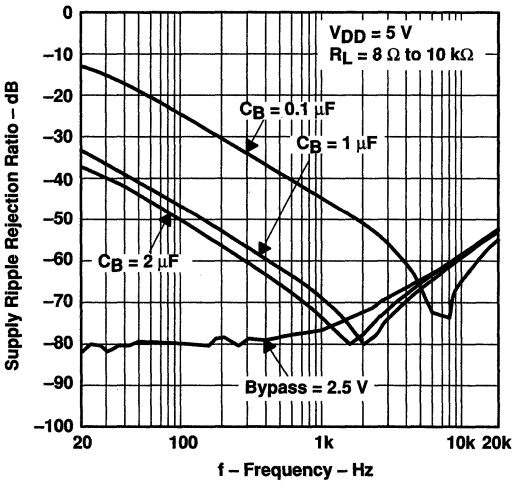


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

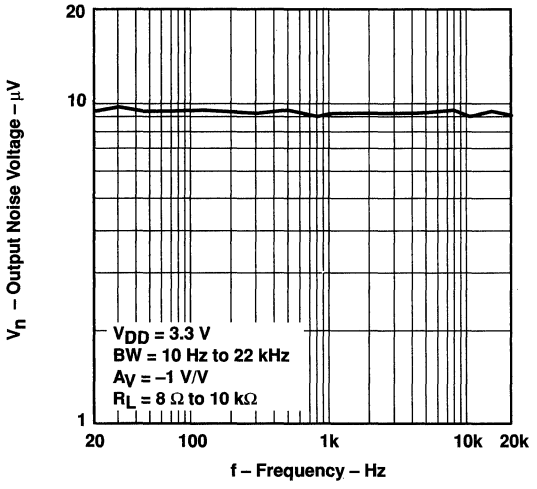


Figure 21

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

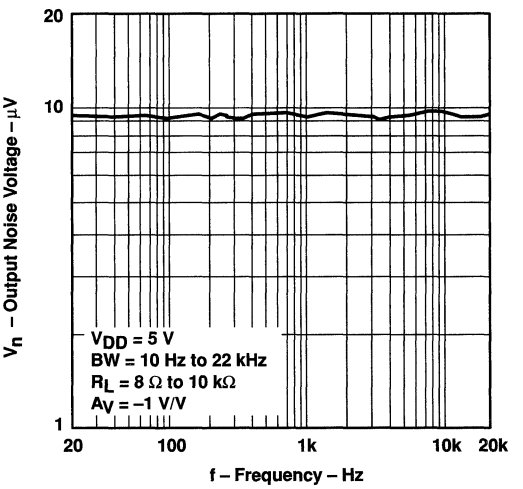


Figure 22

CROSSTALK
vs
FREQUENCY

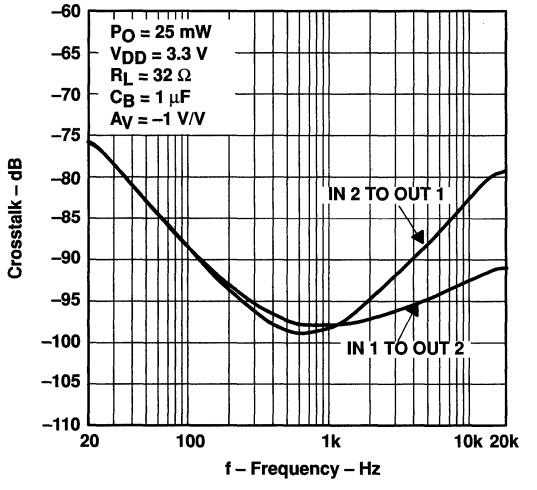


Figure 23

CROSSTALK
vs
FREQUENCY

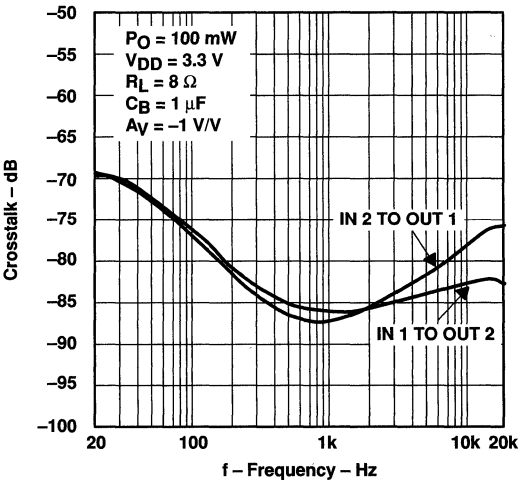


Figure 24

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

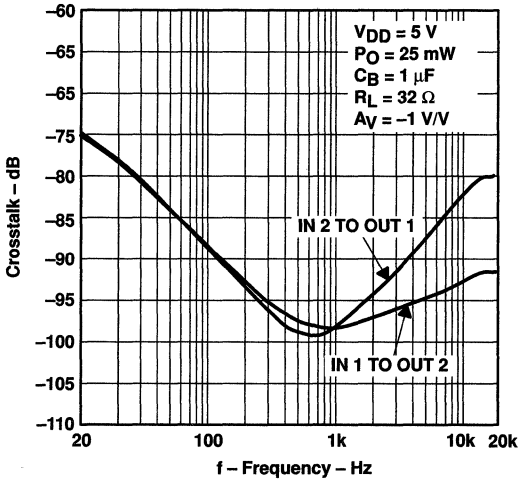


Figure 25

CROSSTALK
vs
FREQUENCY

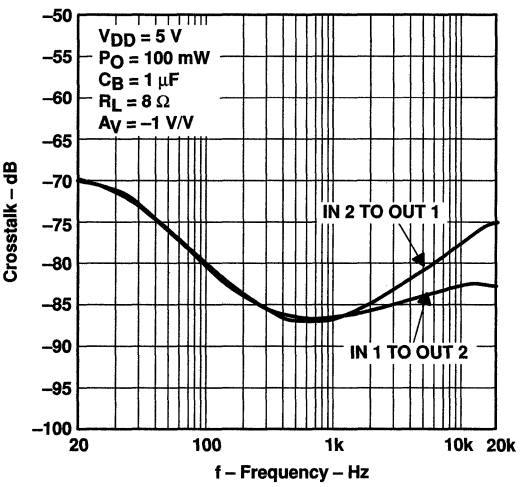


Figure 26

MUTE ATTENUATION
vs
FREQUENCY

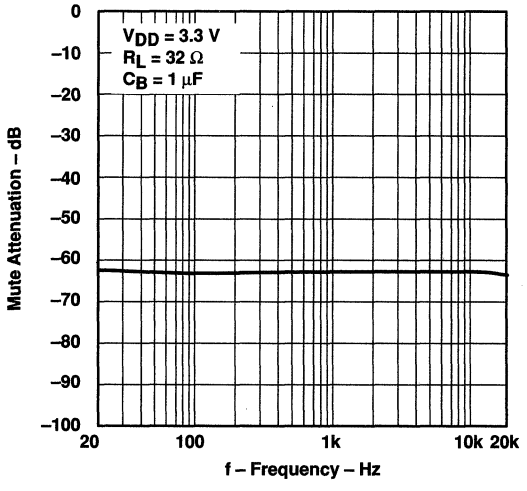


Figure 27

MUTE ATTENUATION
vs
FREQUENCY

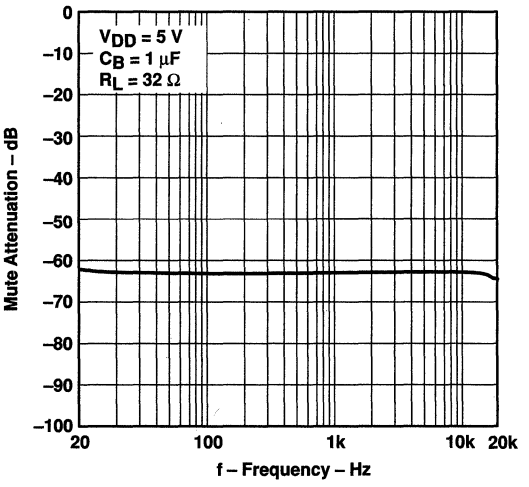


Figure 28

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY

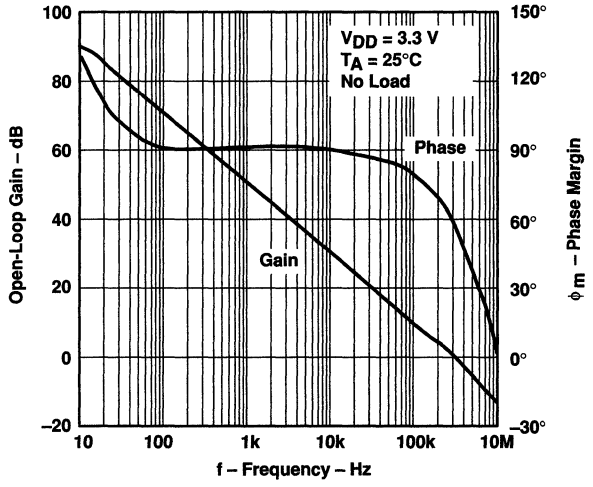


Figure 29

OPEN-LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY

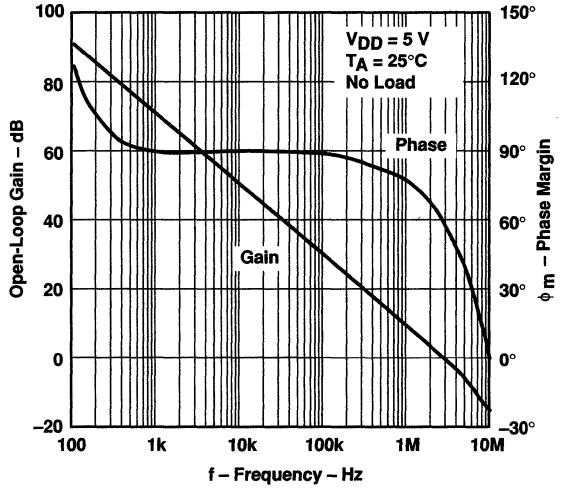


Figure 30

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

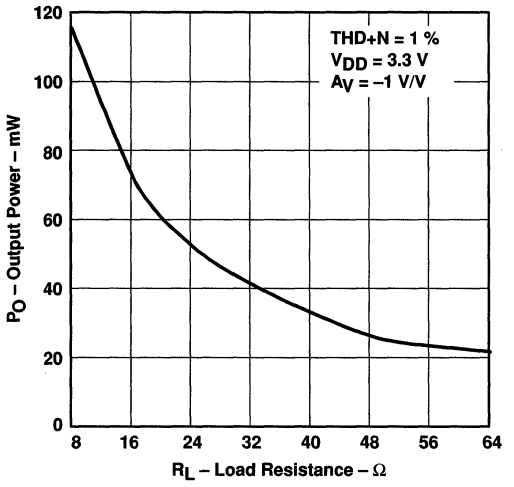


Figure 31

OUTPUT POWER
vs
LOAD RESISTANCE

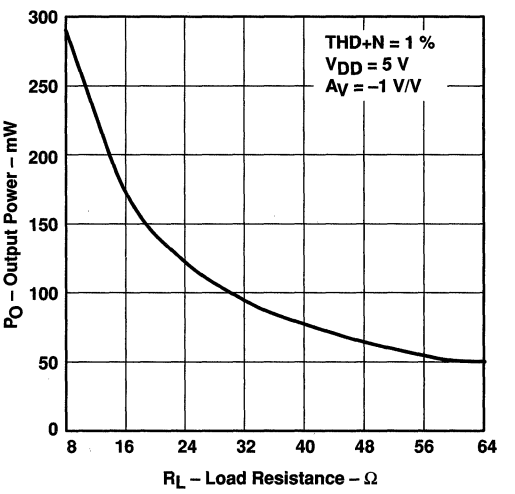


Figure 32

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

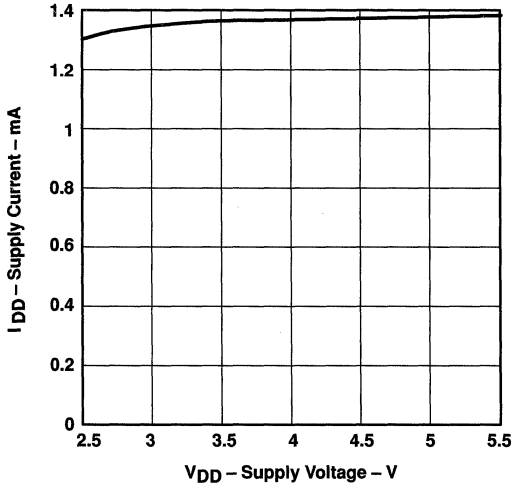


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

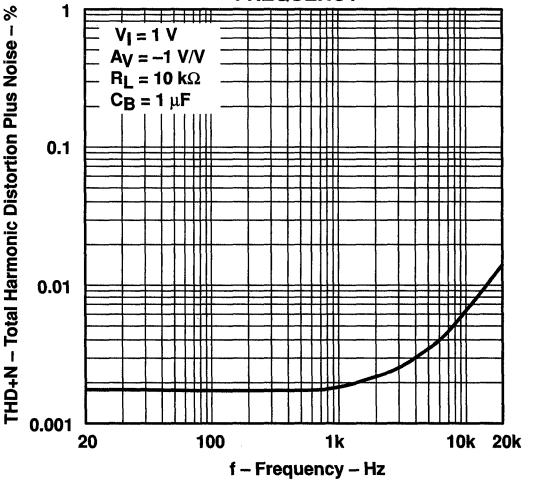


Figure 34

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO
vs
VOLTAGE GAIN

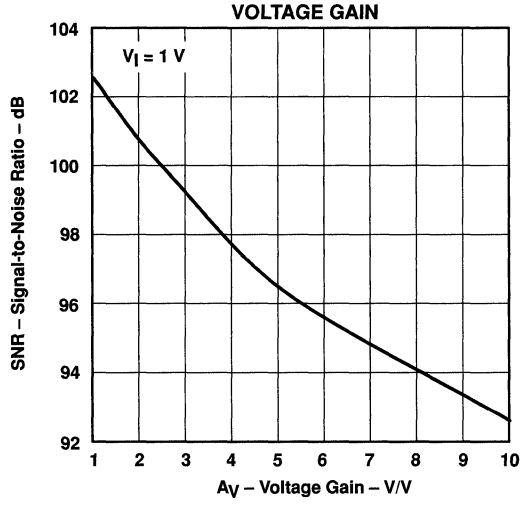


Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

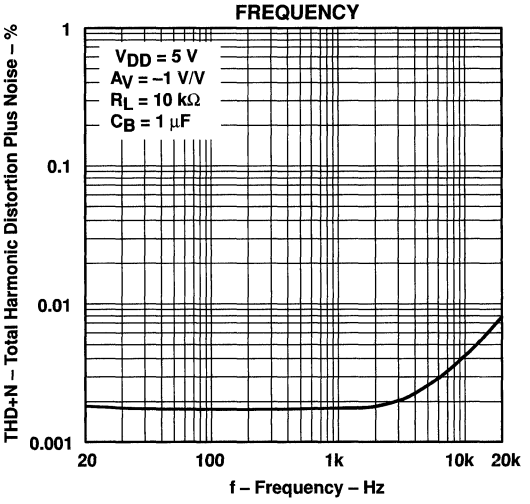


Figure 36

CROSSTALK
vs
FREQUENCY

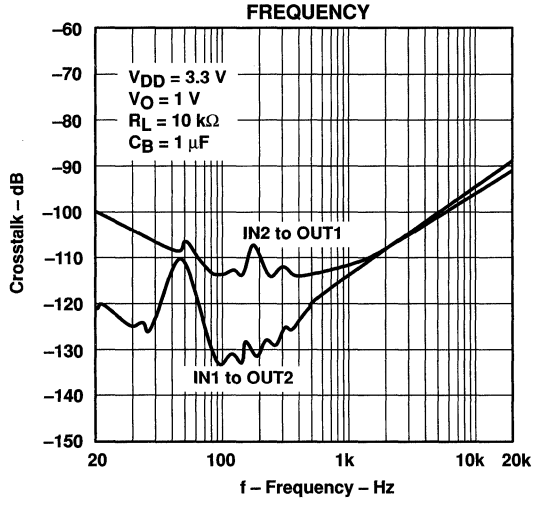


Figure 37

CROSSTALK
vs
FREQUENCY

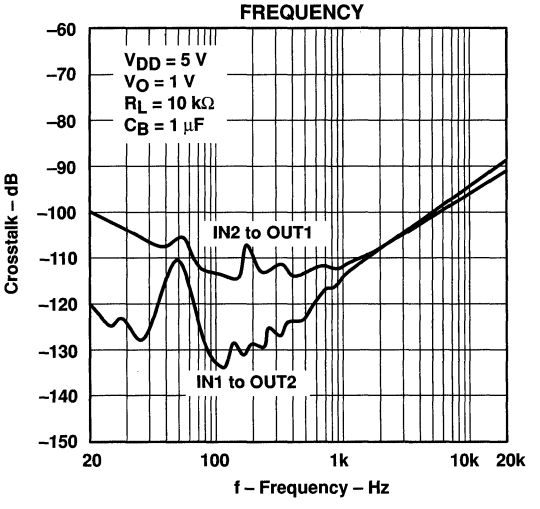


Figure 38

TYPICAL CHARACTERISTICS

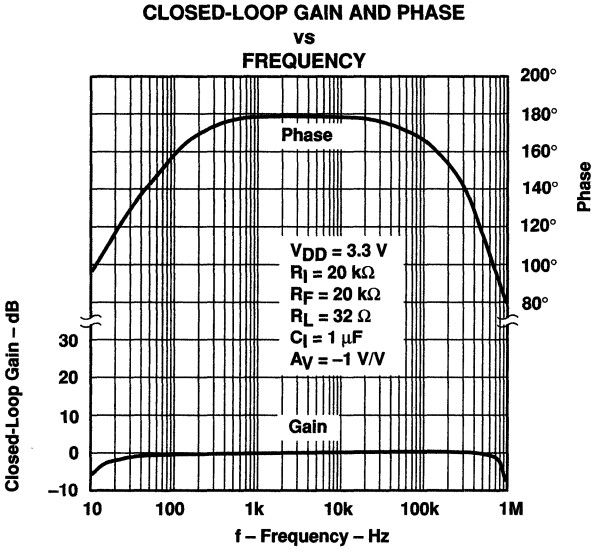


Figure 39

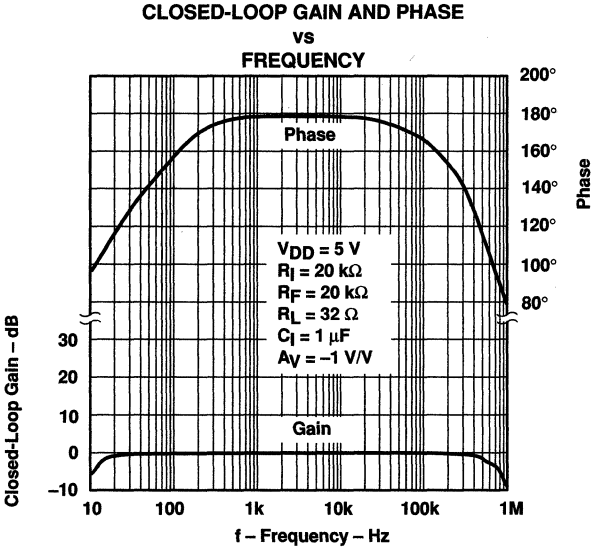


Figure 40

TYPICAL CHARACTERISTICS

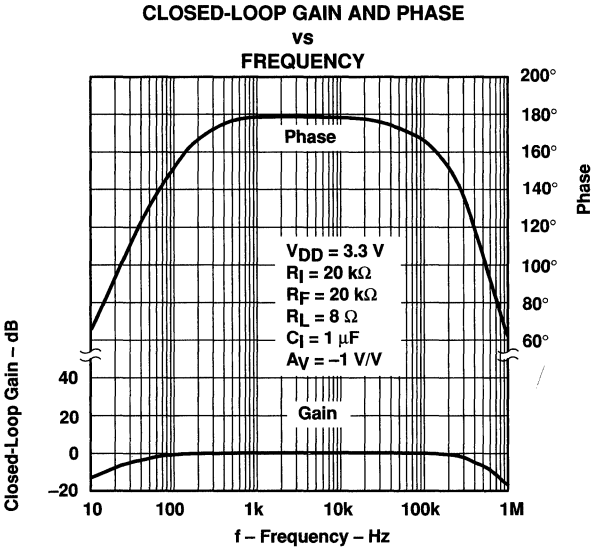


Figure 41

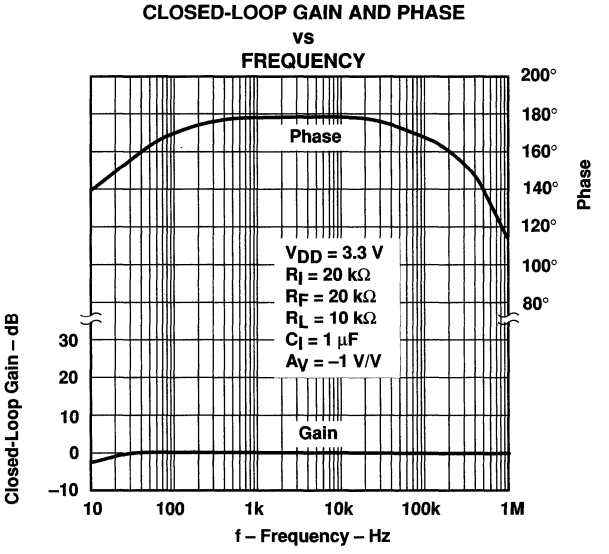


Figure 42

TYPICAL CHARACTERISTICS

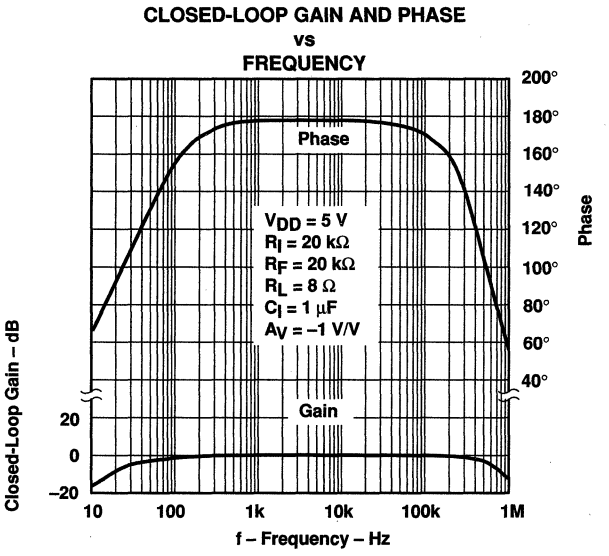


Figure 43

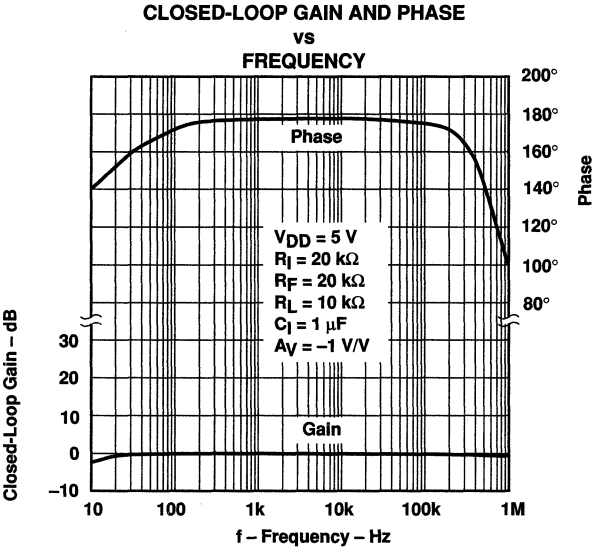


Figure 44

TYPICAL CHARACTERISTICS

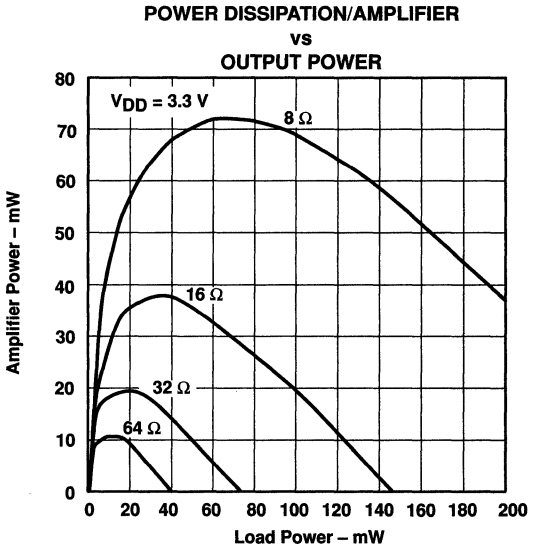


Figure 45

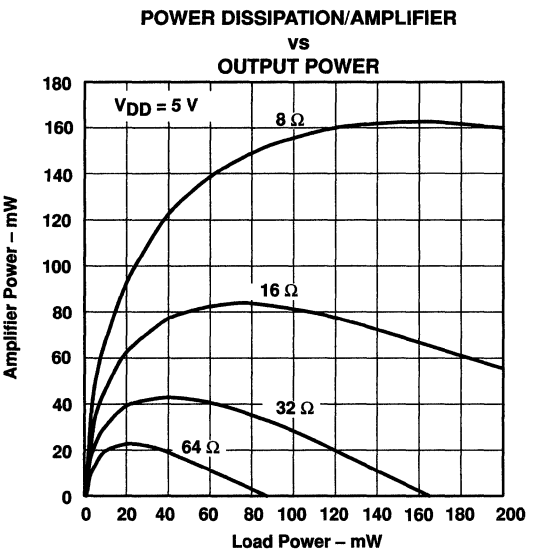


Figure 46

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA122 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA122 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be −1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

APPLICATION INFORMATION

gain setting resistors, R_F and R_I (continued)

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 kΩ and C_F is 5 pF then $f_{c(lowpass)}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(highpass)}} \quad (5)$$

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA122 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \tag{6}$$

As an example, consider a circuit where C_B is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into the equation 9 results in: $6.25 \leq 50$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 160\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{8}$$

APPLICATION INFORMATION

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

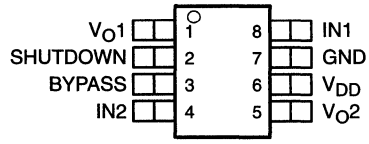
5-V versus 3.3-V operation

The TPA122 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA122 can produce a maximum voltage swing ofV_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

SLOS174B – JANUARY 1997 – REVISE MARCH 2000

- **300-mW Stereo Output**
- **PC Power Supply Compatibility 5-V and 3.3-V Specified Operation**
- **Shutdown Control**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
- **Functional Equivalent of the LM4880**

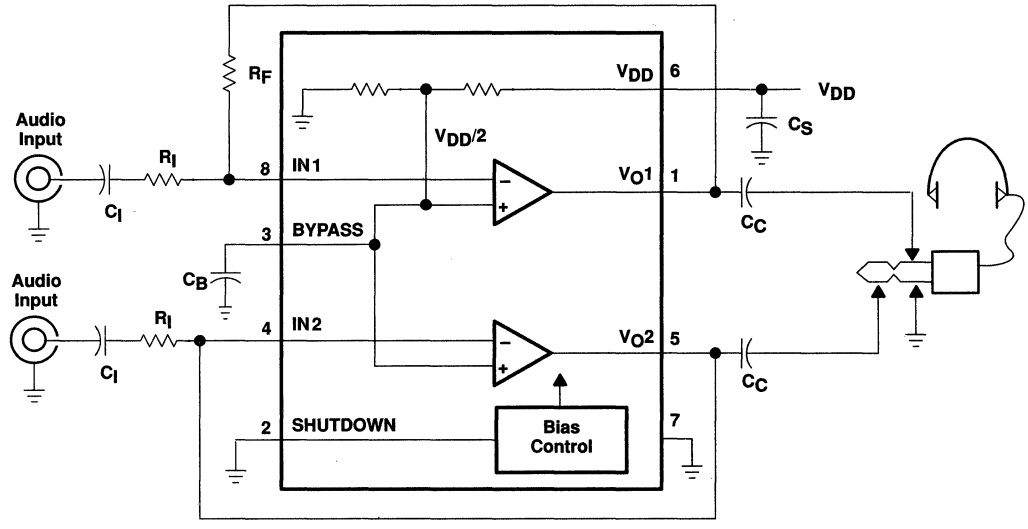
D PACKAGE
(TOP VIEW)



description

The TPA302 is a stereo audio power amplifier capable of delivering 250 mW of continuous average power into an 8-Ω load at less than 0.06% THD+N from a 5-V power supply or up to 300 mW at 1% THD+N. The TPA302 has high current outputs for driving small unpowered speakers at 8 Ω or headphones at 32 Ω. For headphone applications driving 32-Ω loads, the TPA302 delivers 60 mW of continuous average power at less than 0.06% THD+N. The amplifier features a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The amplifier is available in an 8-pin SOIC (D) package that reduces board space and facilitates automated assembly.

typical application circuit



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	SMALL OUTLINE† (D)
–40°C to 85°C	TPA302D

† The D packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA302DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} . . . . . 6 V
Input voltage , V_I . . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . . Internally Limited (See Dissipation Rating Table)
Operating junction temperature range, T_J . . . . . –40°C to 150° C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	731 mW	5.8 mW/°C	460 mW	380 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current			2.25	5	mA
V_{IO}	Input offset voltage			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		55		dB
$I_{DD(SD)}$	Quiescent current in shutdown			0.6	20	µA

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.08%		100		mW
			THD < 1%		125		
			THD < 0.08%, R_L = 32 Ω		25		
			THD < 1%, R_L = 32 Ω		35		
B_{OM}	Maximum output power bandwidth	Gain = 10, 1% THD			20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = –1			10		µVrms

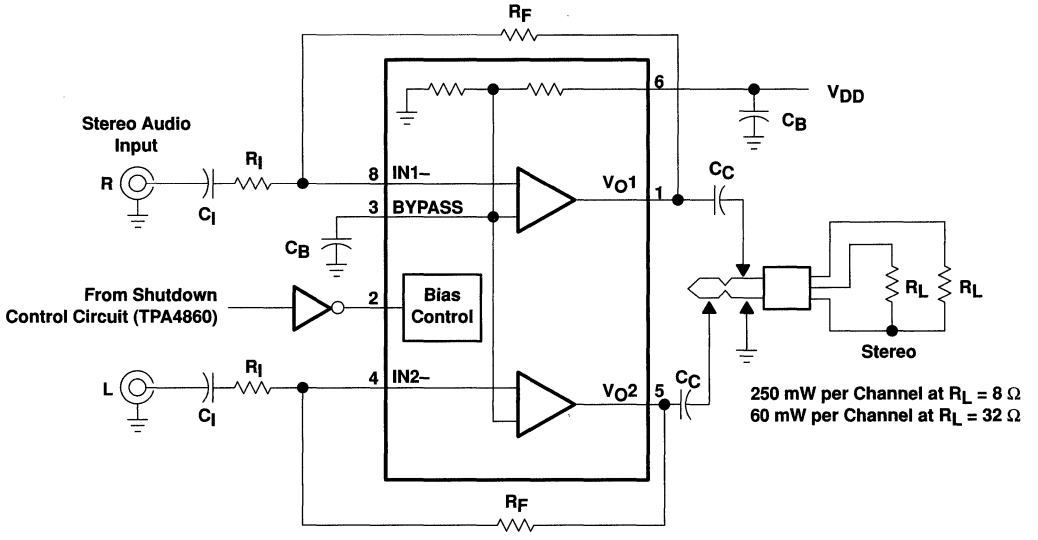
dc electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{DD}	Supply current			4	10	mA
V_{OO}	Output offset voltage	See Note 1		5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		65		dB
$I_{DD(SD)}$	Quiescent current in shutdown			0.6		μA

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
P_O	Output power	Gain = –1, f = 1 kHz	THD < 0.06%		250		mW
			THD < 1%		300		
			THD < 0.06%, R_L = 32 Ω		60		
			THD < 1%, R_L = 32 Ω		80		
B_{OM}	Maximum output power bandwidth	Gain = 10,	1% THD		20		kHz
B_1	Unity gain bandwidth	Open loop			1.5		MHz
	Channel separation	f = 1 kHz			75		dB
	Supply ripple rejection ratio	f = 1 kHz			45		dB
V_n	Noise output voltage	Gain = –1			10		μVrms

typical application



TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1–3, 7–9, 13–15, 19–21
		vs Output power	4–6, 10–12 16–18, 22–24
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	25 26
V_n	Output noise voltage	vs Frequency	27, 28
	Maximum package power dissipation	vs Free-air temperature	29
	Power dissipation	vs Output power	30, 31
P_{Omax}	Maximum output power	vs Free-air temperature	32, 33
P_O	Output power	vs Load resistance vs Supply voltage	34 35
	Open loop response		36
	Closed loop response		37
	Crosstalk	vs Frequency	38, 39
	Supply ripple rejection ratio	vs Frequency	40, 41

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

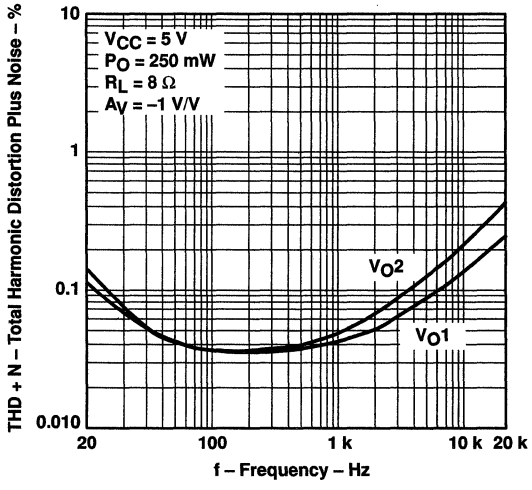


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

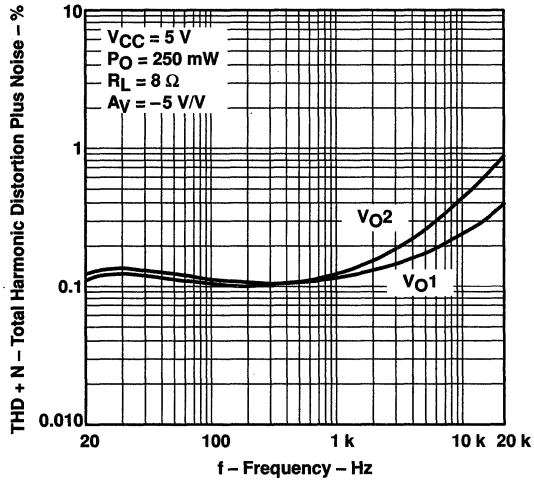


Figure 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

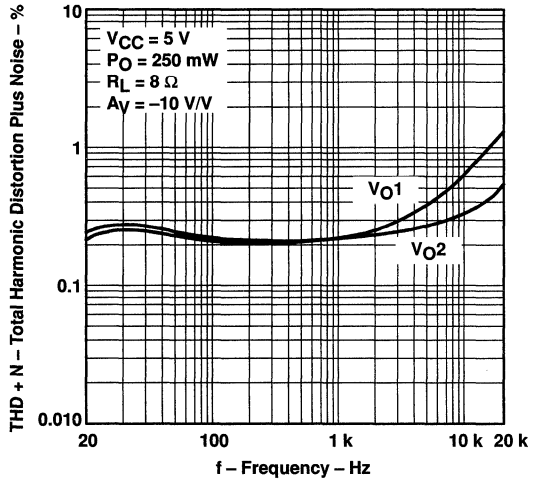


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

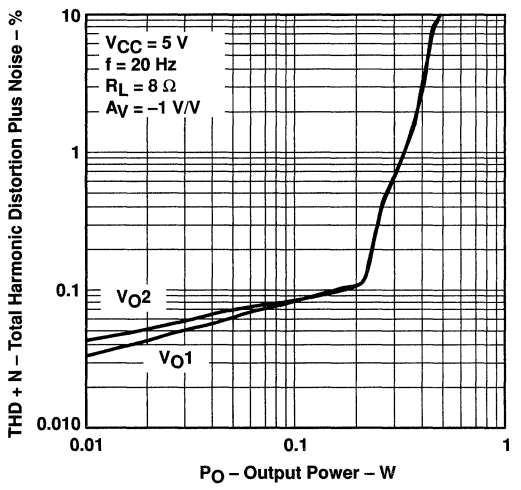


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

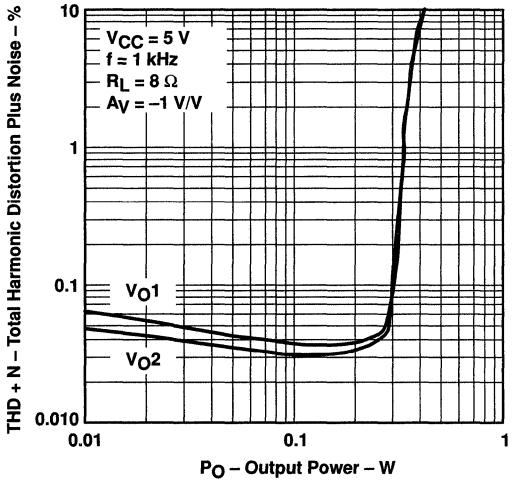


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

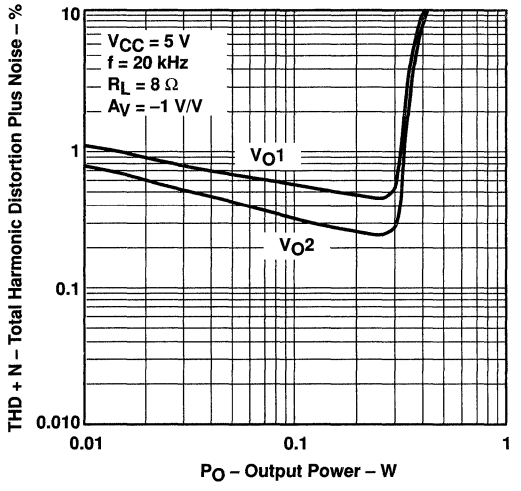


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

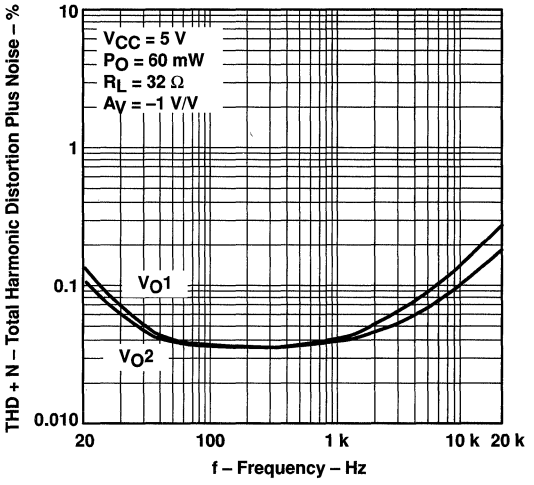


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

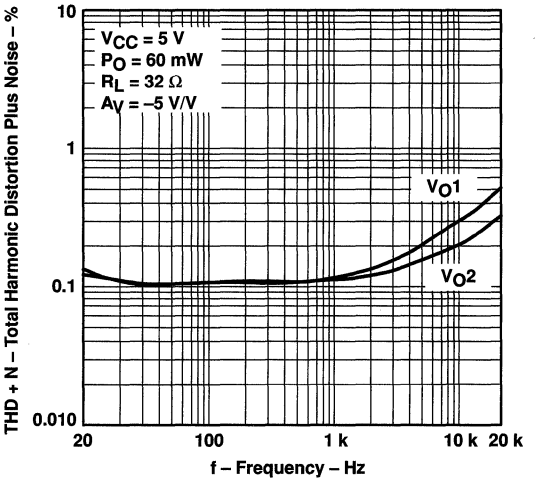


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

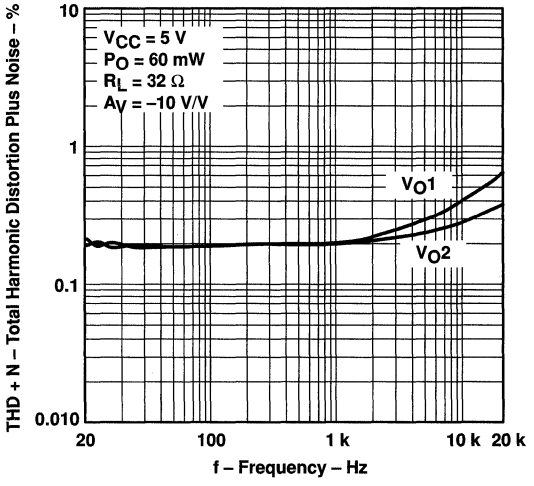


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

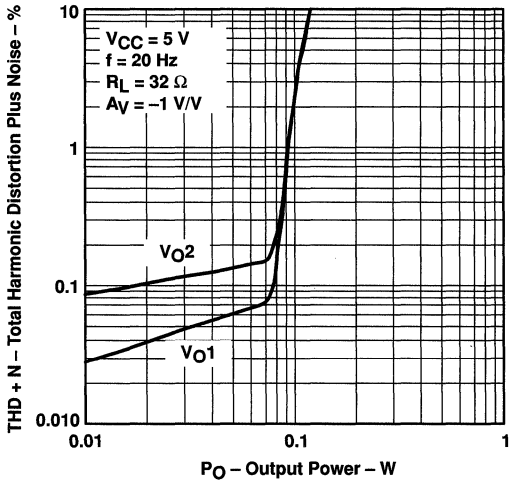


Figure 10

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

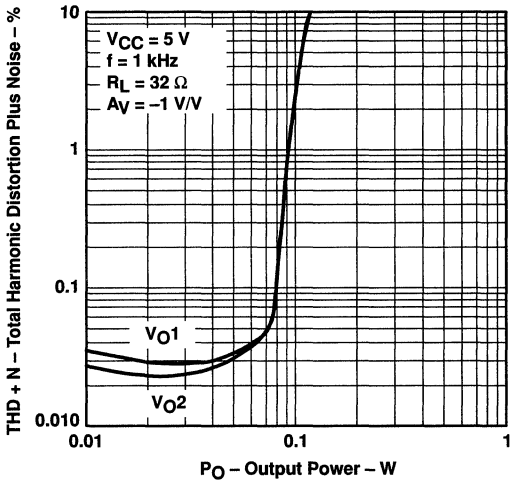


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

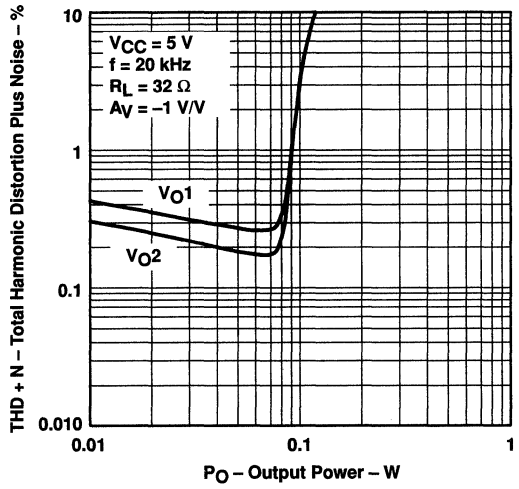


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

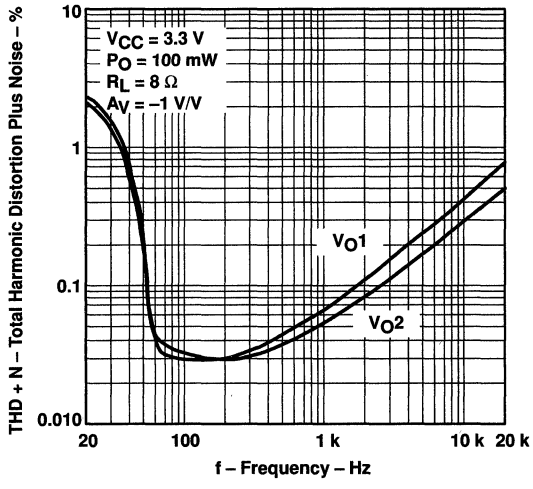


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

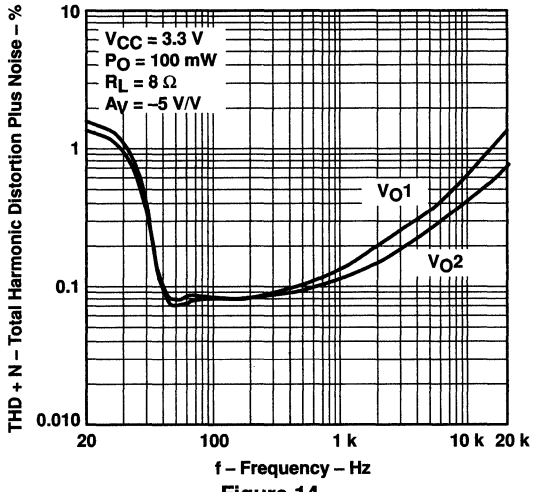


Figure 14

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

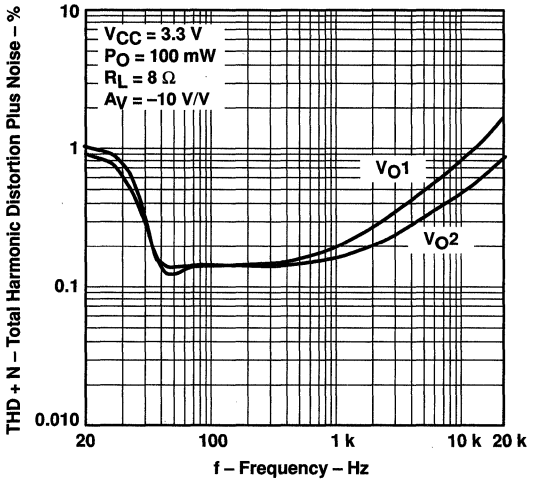


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

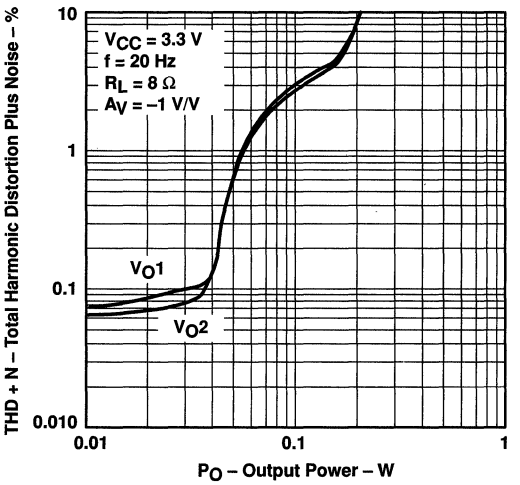


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

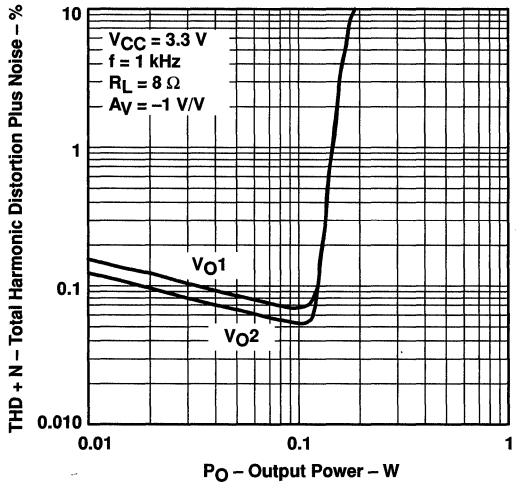


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

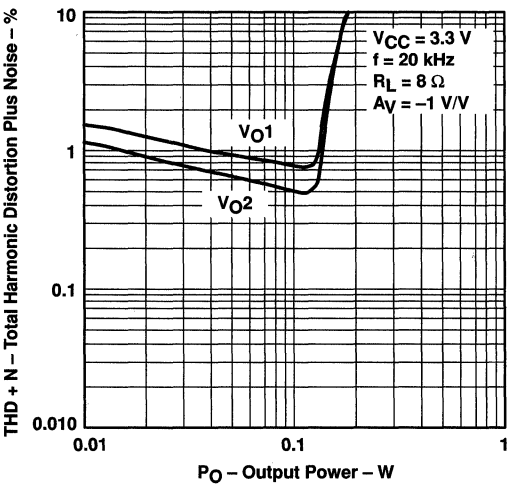


Figure 18

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

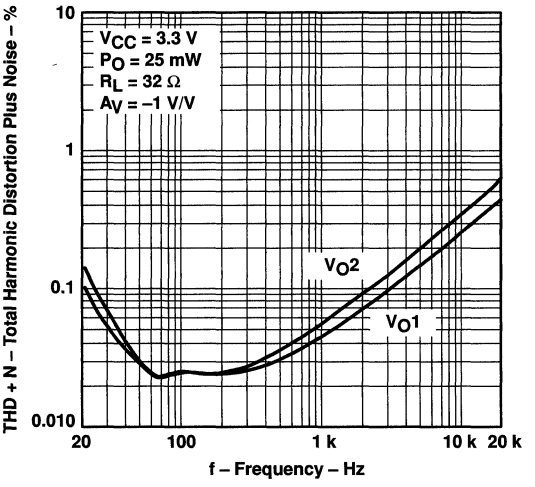


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

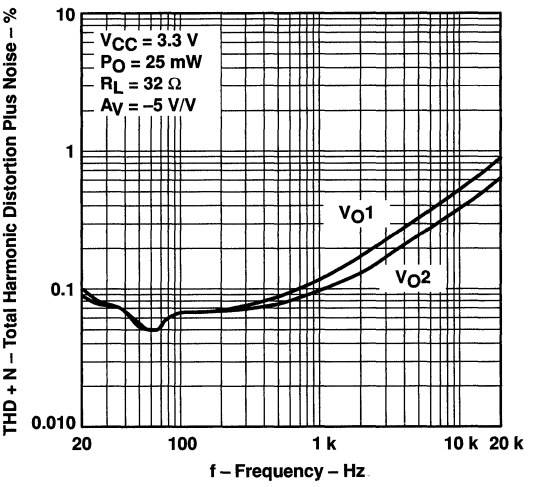


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

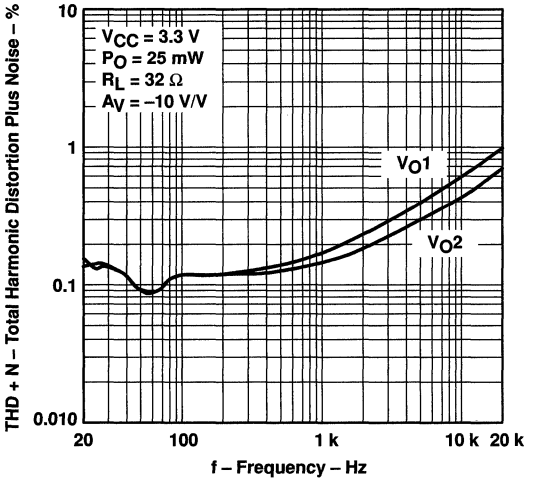


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

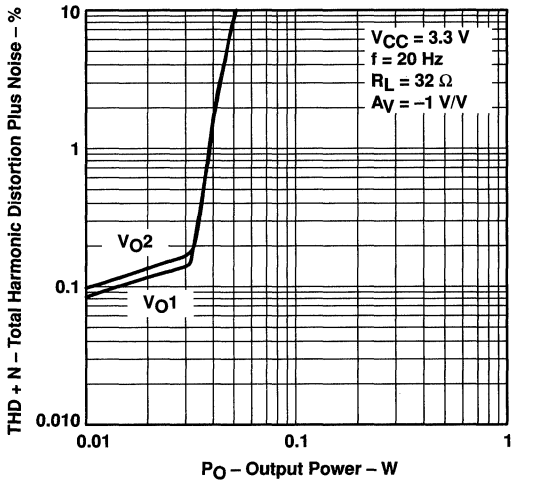


Figure 22

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

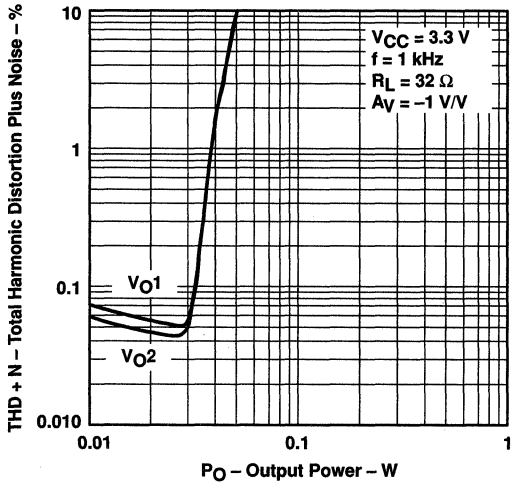


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

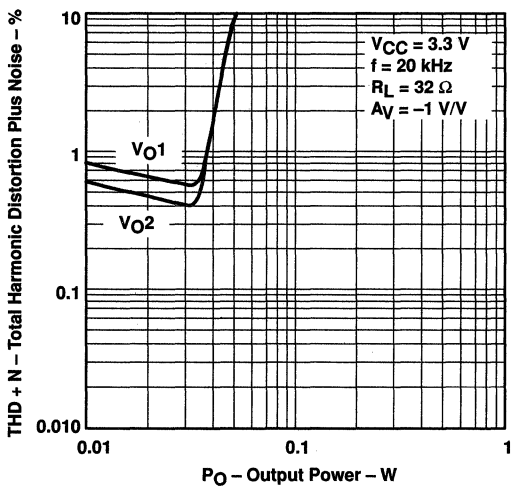


Figure 24

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

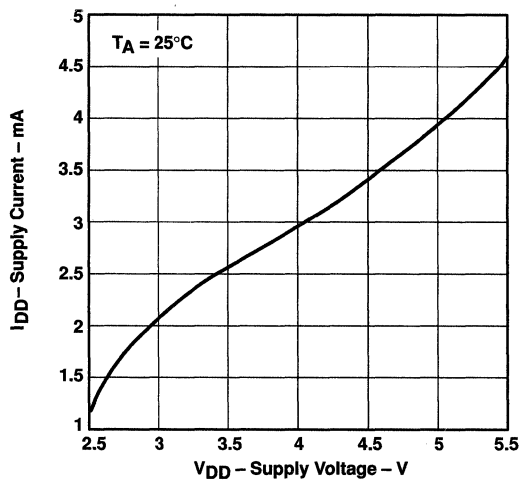


Figure 25

SUPPLY CURRENT DISTRIBUTION
vs
FREE-AIR TEMPERATURE

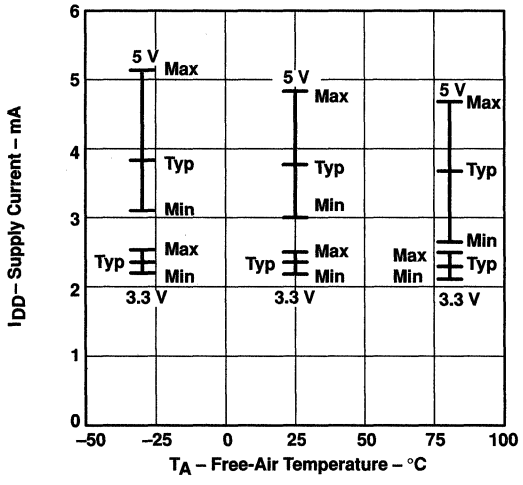


Figure 26

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

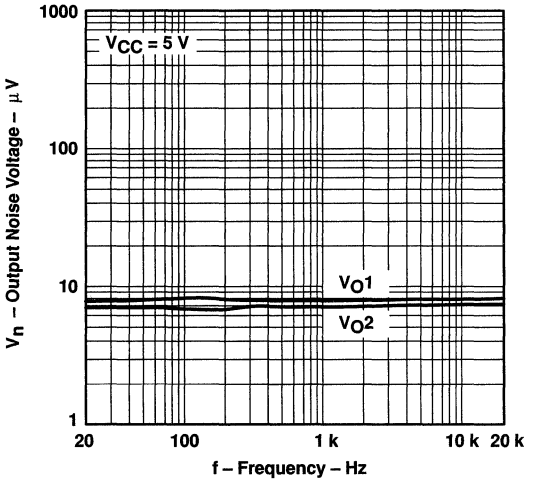


Figure 27

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

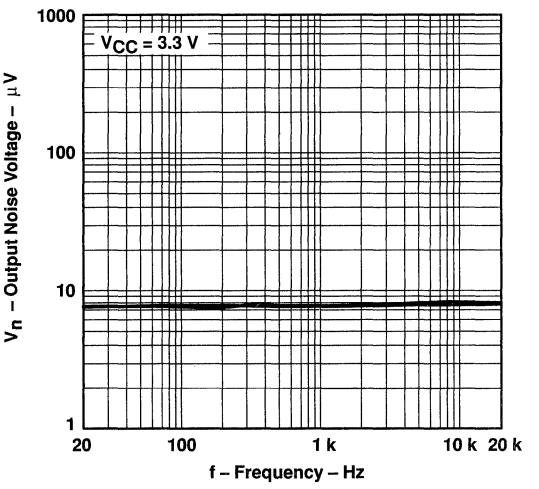


Figure 28

MAXIMUM PACKAGE POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

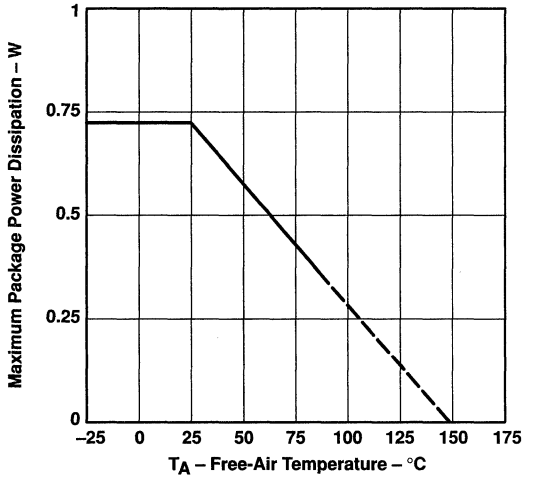


Figure 29

POWER DISSIPATION
vs
OUTPUT POWER

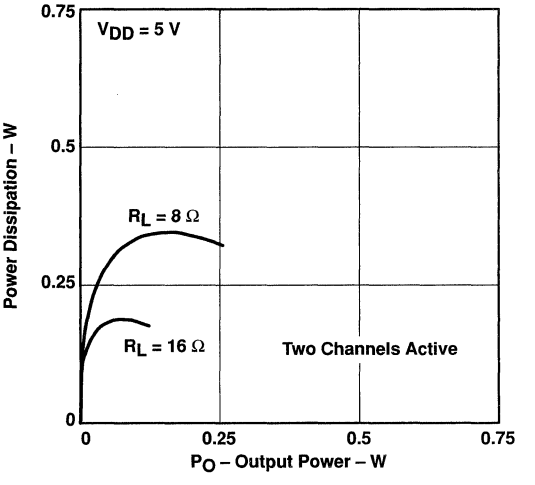


Figure 30

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
OUTPUT POWER

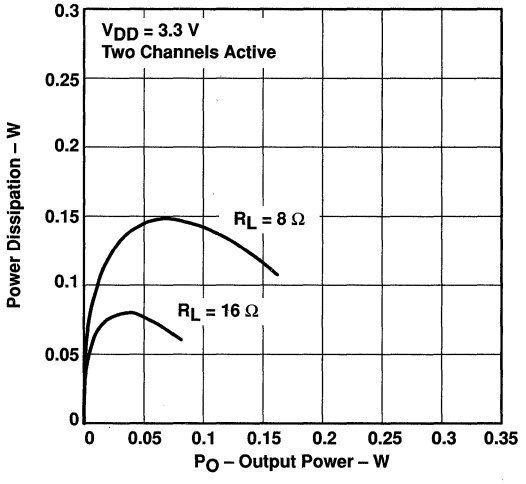


Figure 31

MAXIMUM OUTPUT POWER
vs
FREE-AIR TEMPERATURE

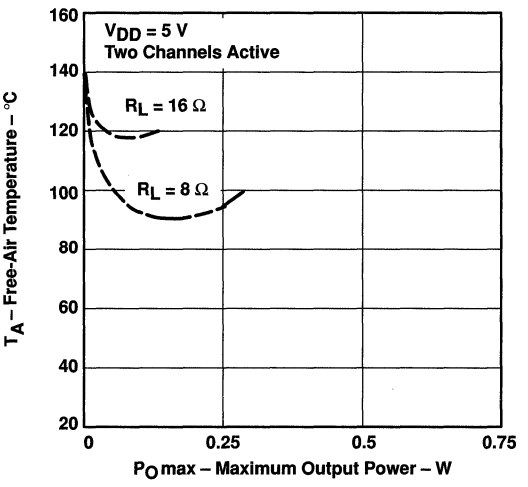


Figure 32

MAXIMUM OUTPUT POWER
vs
FREE-AIR TEMPERATURE

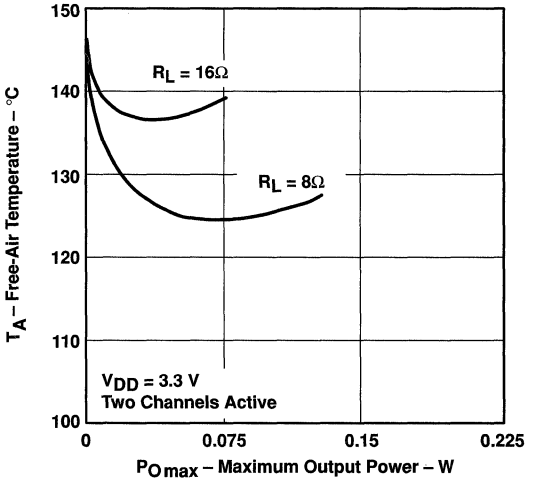


Figure 33

OUTPUT POWER
vs
LOAD RESISTANCE

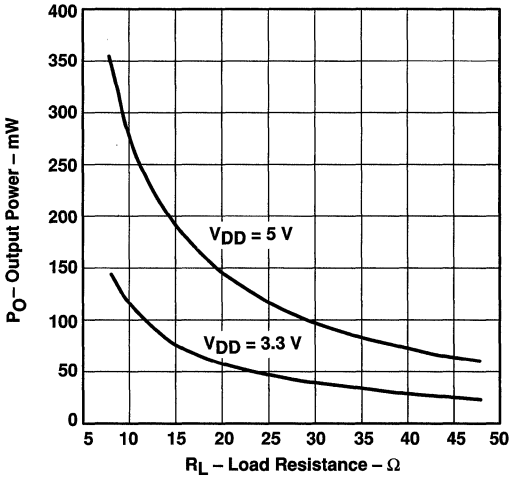


Figure 34

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

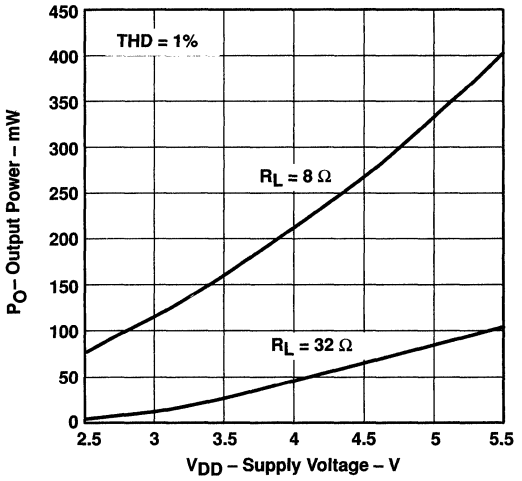


Figure 35

OPEN LOOP RESPONSE

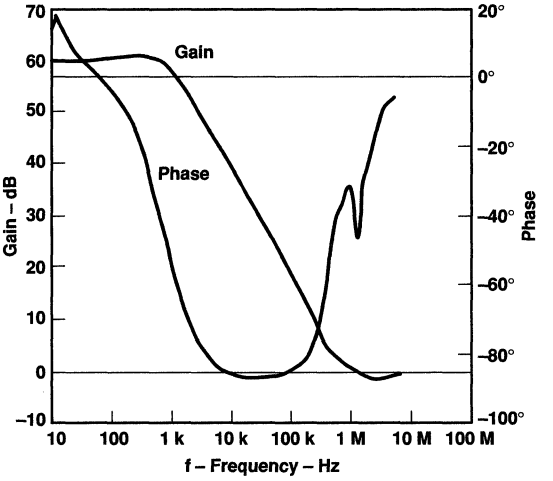


Figure 36

CLOSED LOOP RESPONSE

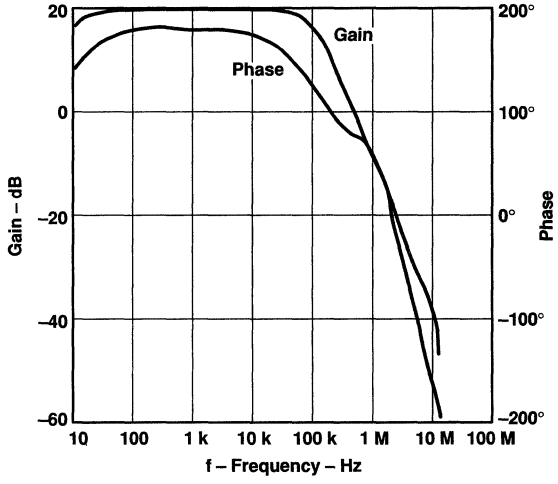


Figure 37

CROSSTALK
vs
FREQUENCY

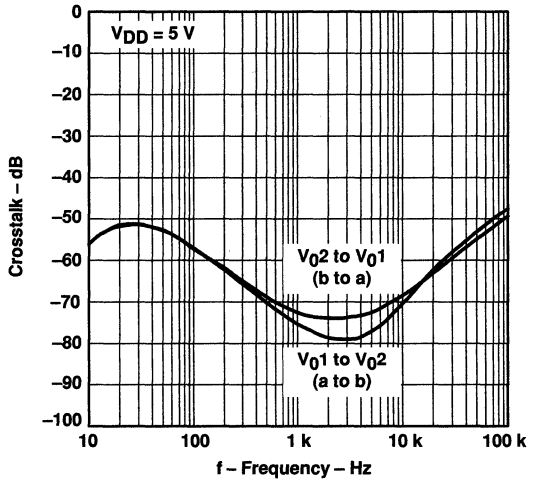


Figure 38

TYPICAL CHARACTERISTICS

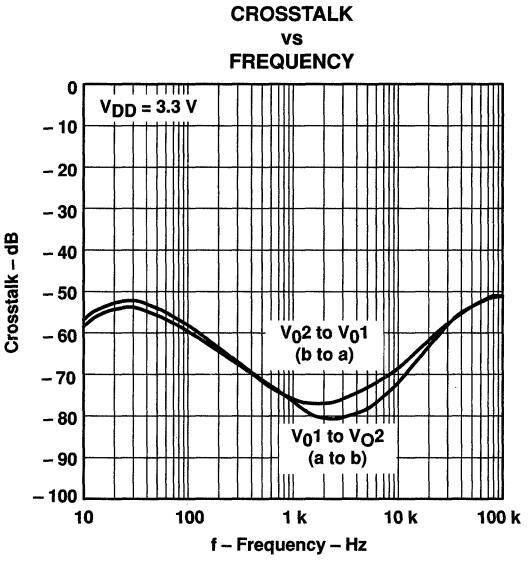


Figure 39

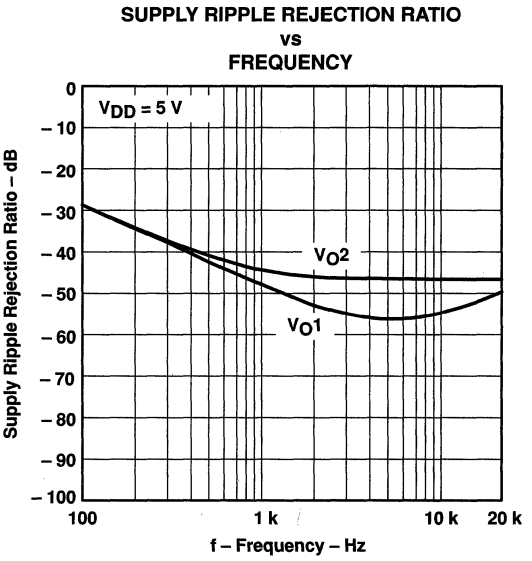


Figure 40

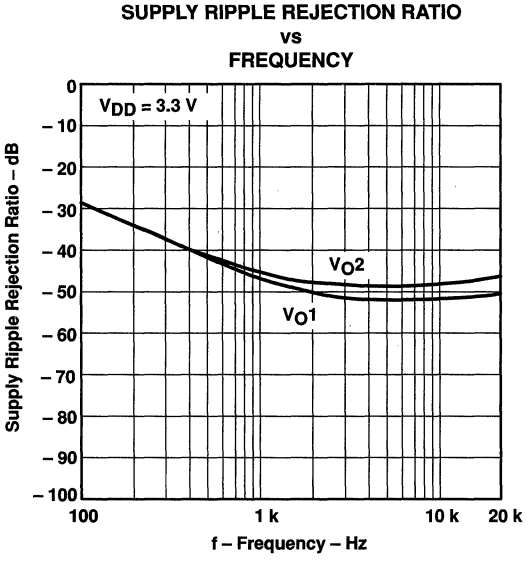
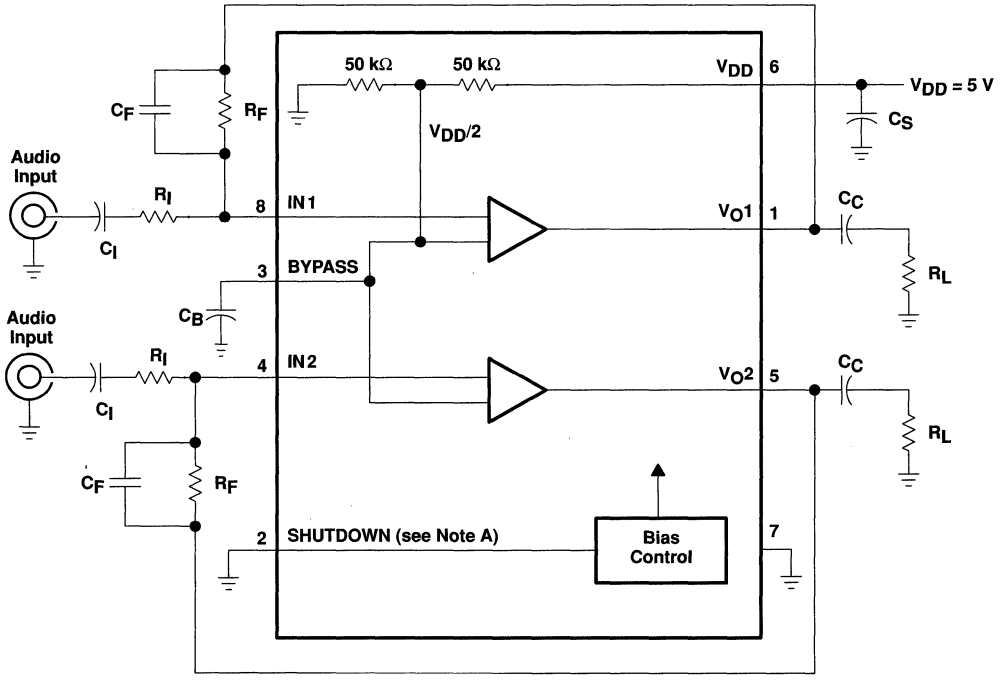


Figure 41

APPLICATION INFORMATION

selection of components

Figure 42 is a schematic diagram of a typical application circuit.



NOTE A. SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 42. TPA302 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA302 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{1}$$

Given that the TPA302 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{2}$$

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be −5 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{3}$$

For example if R_F is 100 kΩ and C_F is 5 pF then $f_{c(\text{lowpass})}$ is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(\text{highpass})} = \frac{1}{2\pi R_I C_I} \tag{4}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{c(\text{highpass})}} \tag{5}$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (>10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA302 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \tag{6}$$

As an example, consider a circuit where C_B is 0.1 μF, C_I is 0.22 μF and R_I is 10 kΩ. Inserting these values into the equation 9 results in: $400 \leq 454$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drives the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	68 μF	293 Hz
32 Ω	68 μF	73 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{8}$$

shutdown mode

The TPA302 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} < 1$ μA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 43 provides an easy way to determine what output power can be expected out of the TPA302 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

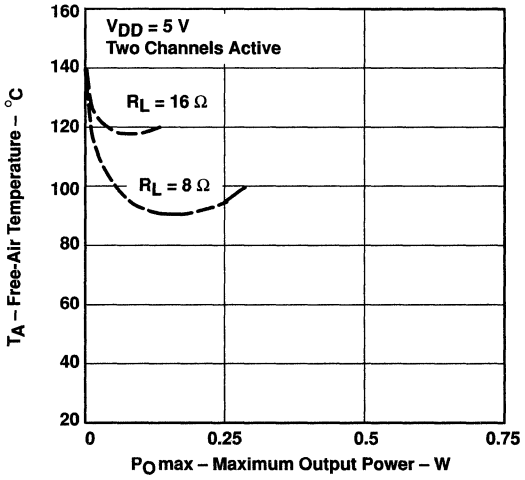


Figure 43. Free-Air Temperature Versus Maximum Output Power

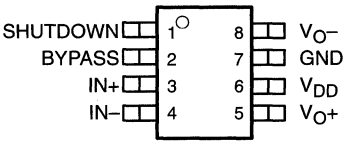
5-V versus 3.3-V operation

The TPA302 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA302 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

SLOS208C – JANUARY1998 – REVISED MARCH 2000

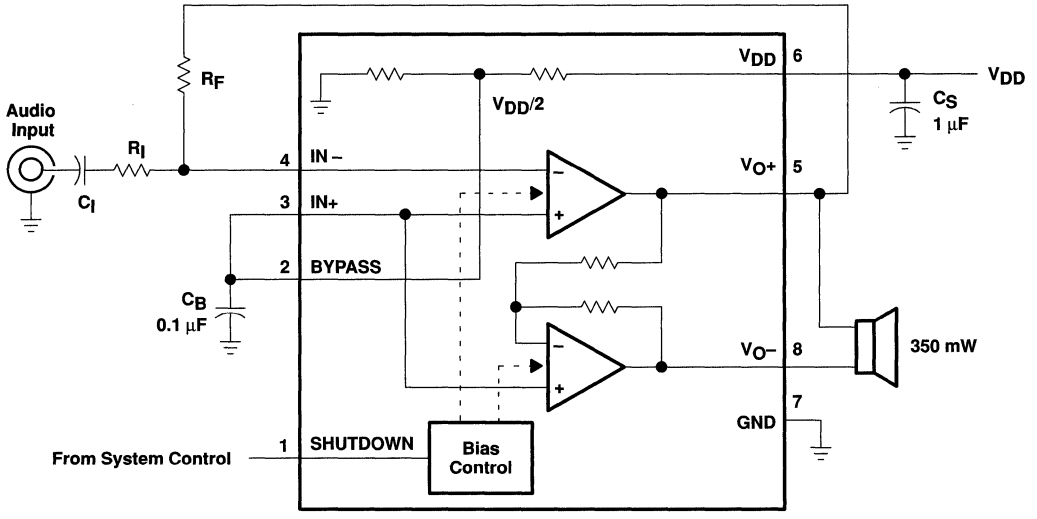
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility**
  2.5 V – 5.5 V
- **Output Power for R_L = 8 Ω**
  - **350 mW at V_{DD} = 5 V, BTL**
  - **250 mW at V_{DD} = 3.3 V, BTL**
- **Ultra-Low Quiescent Current in Shutdown Mode . . . 0.15 μA**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA301 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA301 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a quiescent current of 0.15 μA during shutdown. The TPA301 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.



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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA301D	TPA301DGN	AAA

† The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA301DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-μF to 1-μF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN–	4	I	IN– is the inverting input. IN– is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} < 1 μA).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive BTL output.
V_O–	8	O	V_O– is the negative BTL output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	See Note 1		5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		85		dB
$I_{DD(q)}$	Supply current (see Figure 3)	BTL mode		0.7	1.5	mA
$I_{DD(sd)}$	Supply current, shutdown mode (see Figure 4)			0.15	5	μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately V_{DD}/2.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%,	See Figure 9		250		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW, Gain = 2,	f = 20 Hz to 4 kHz, See Figure 7		1.3%		
	Maximum output power bandwidth	Gain = 2, See Figure 7	THD = 3%,		10		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 15		1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 2	C_B = 1 μF,		71		dB
V_n	Noise output voltage	Gain = 1, R_L = 32 Ω,	C_B = 0.1 μF, See Figure 19		15		μV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		78		dB
$I_{DD(q)}$	Quiescent current (see Figure 3)			0.7	1.5	mA
$I_{DD(sd)}$	Quiescent current, shutdown mode (see Figure 4)			0.15	5	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	See Figure 13		700		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW, Gain = 2,	f = 20 Hz to 4 kHz, See Figure 11		1%		
	Maximum output power bandwidth	Gain = 2, See Figure 11	THD = 2%,		10		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 16		1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 2	C_B = 1 μF,		65		dB
V_n	Noise output voltage	Gain = 1, R_L = 32 Ω,	C_B = 0.1 μF, See Figure 20		15		μV(rms)

PARAMETER MEASUREMENT INFORMATION

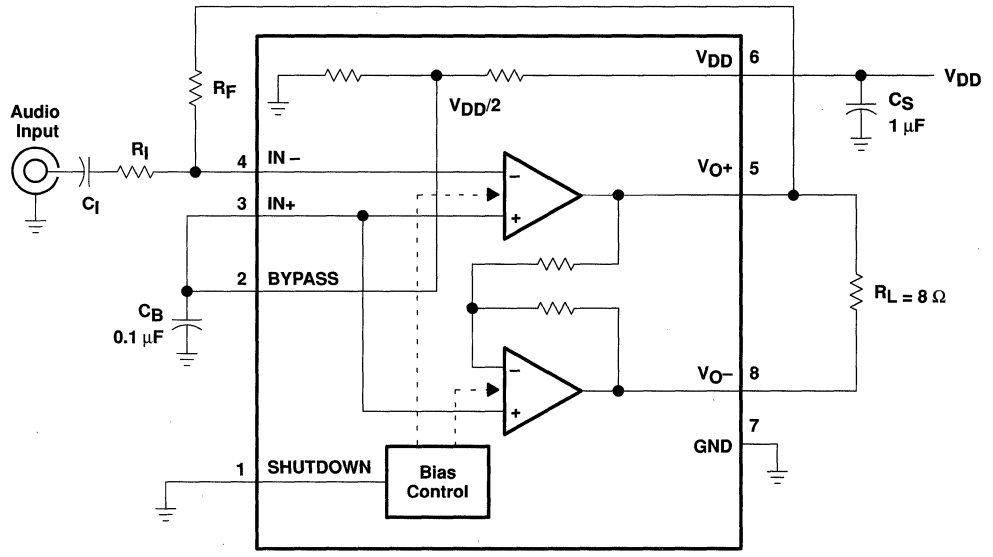


Figure 1. Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
k_{SVR}	Supply voltage rejection ratio	vs Frequency	2
I_{DD}	Supply current	vs Supply voltage	3, 4
P_O	Output power	vs Supply voltage	5
		vs Load resistance	6
THD+N	Total harmonic distortion plus noise	vs Frequency	7, 8, 11, 12
		vs Output power	9, 10, 13, 14
	Open loop gain and phase	vs Frequency	15, 16
	Closed loop gain and phase	vs Frequency	17, 18
V_n	Output noise voltage	vs Frequency	19, 20
P_D	Power dissipation	vs Output power	21, 22

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

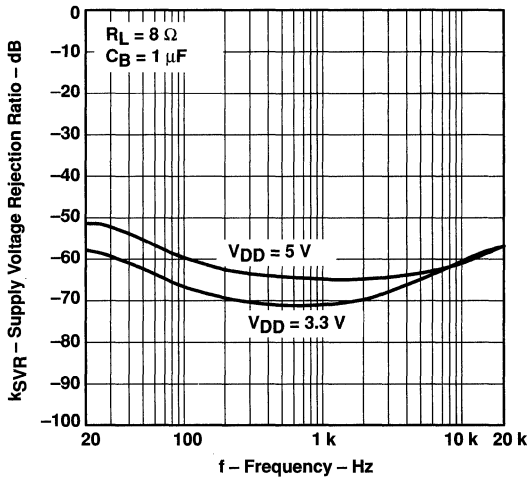


Figure 2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

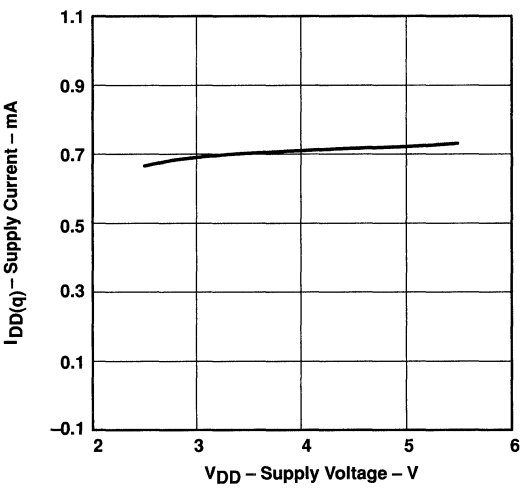


Figure 3

SUPPLY CURRENT (SHUTDOWN)
vs
SUPPLY VOLTAGE

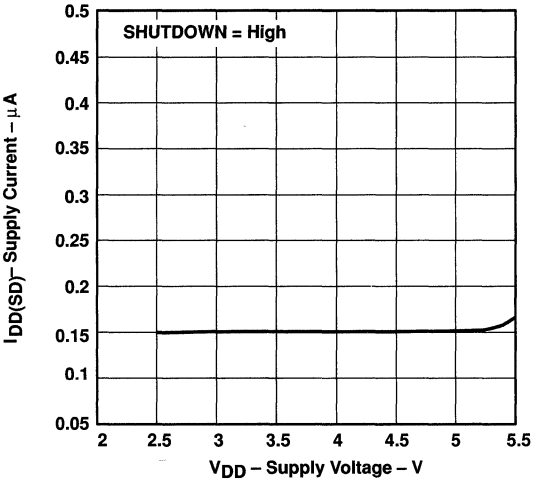


Figure 4

TYPICAL CHARACTERISTICS

**OUTPUT POWER
vs
SUPPLY VOLTAGE**

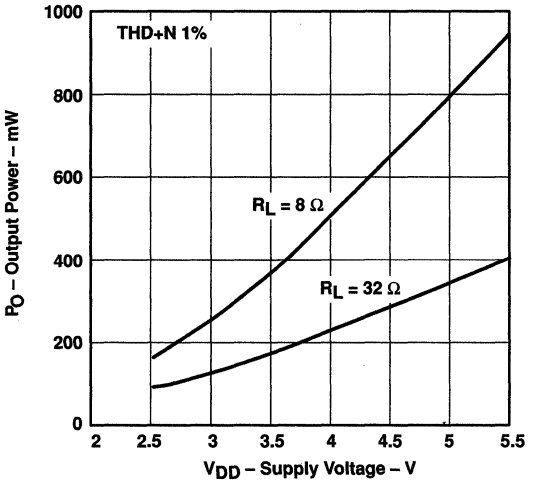


Figure 5

**OUTPUT POWER
vs
LOAD RESISTANCE**

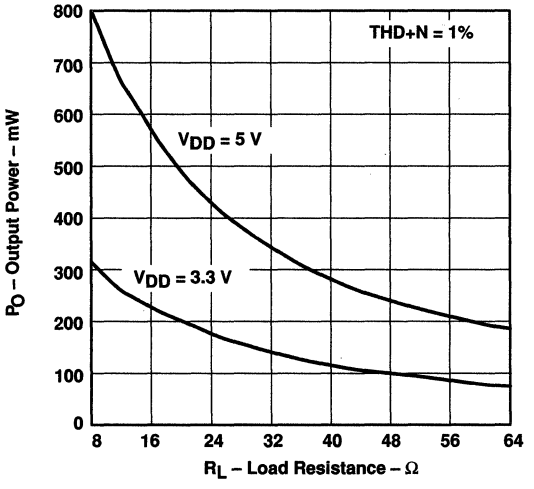


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

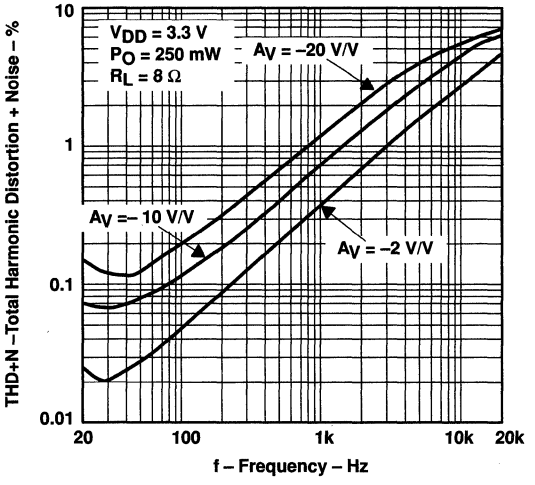


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

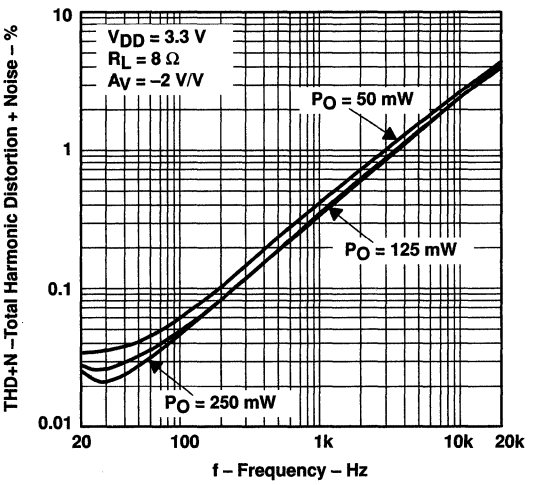


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

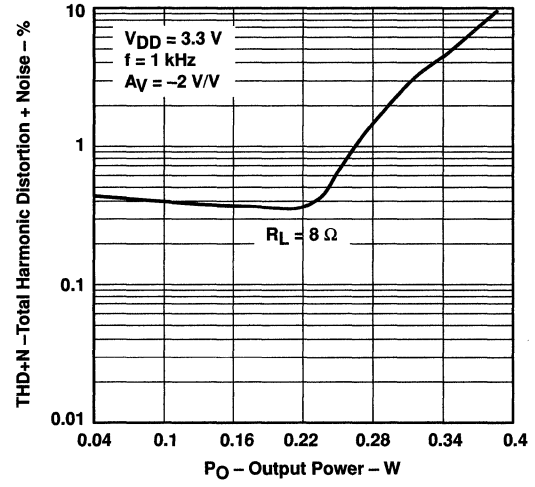


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

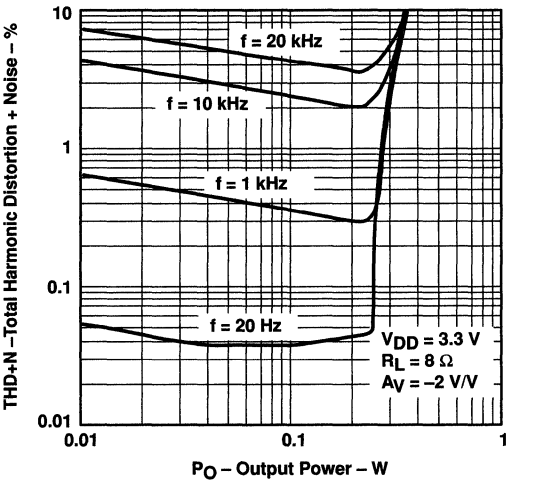


Figure 10

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

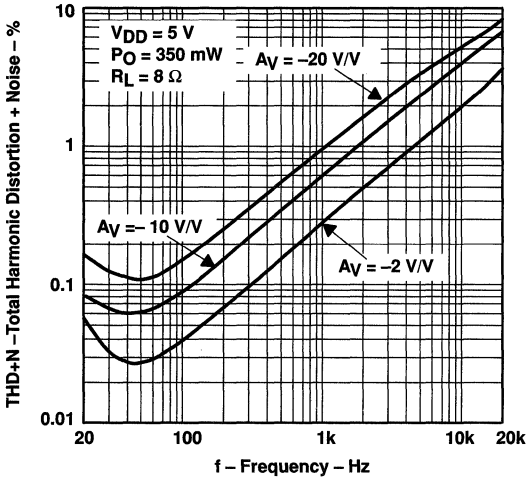


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

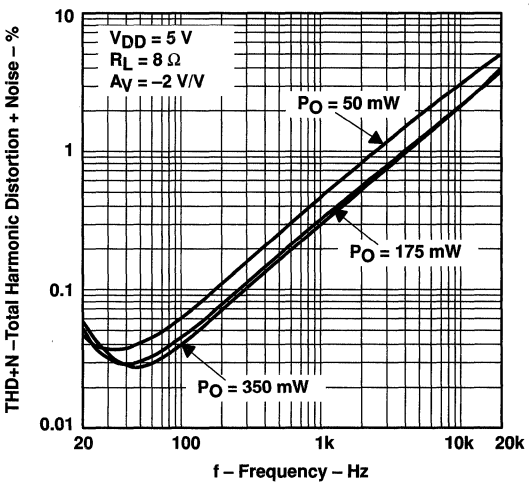


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

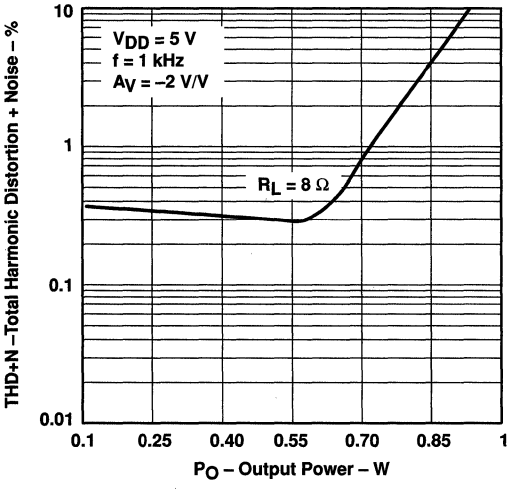


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

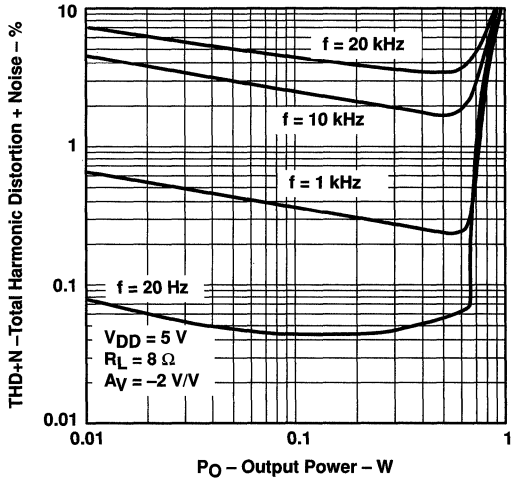


Figure 14

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

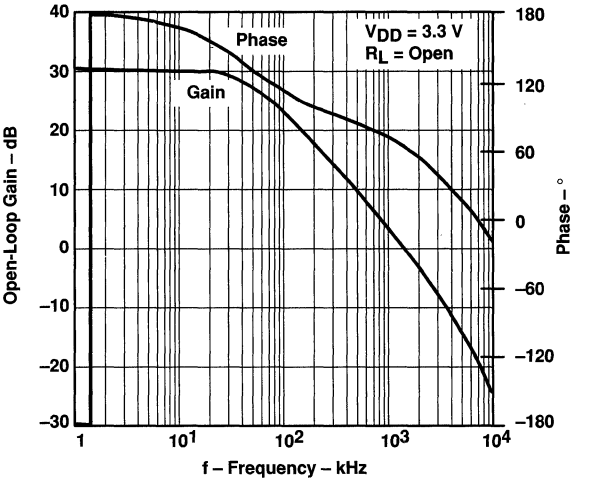


Figure 15

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

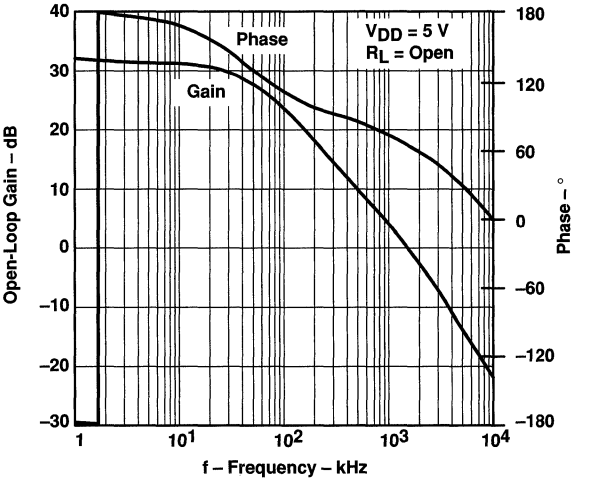


Figure 16

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

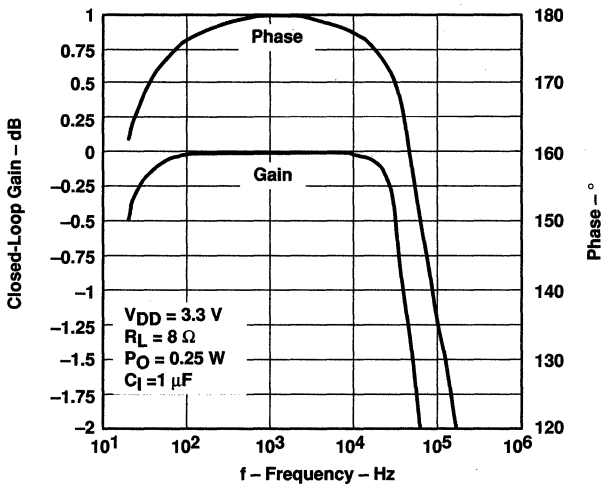


Figure 17

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

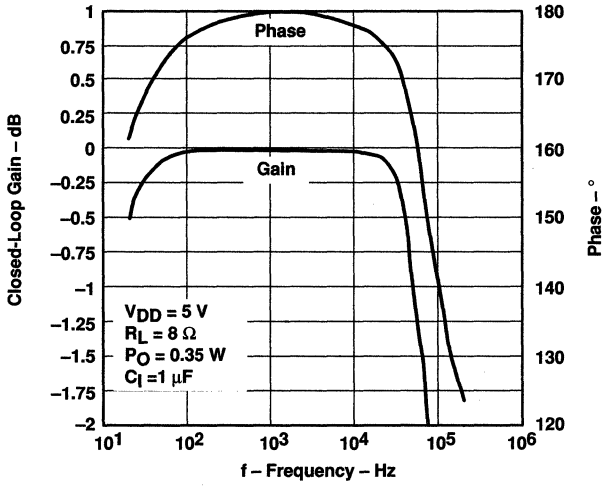


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

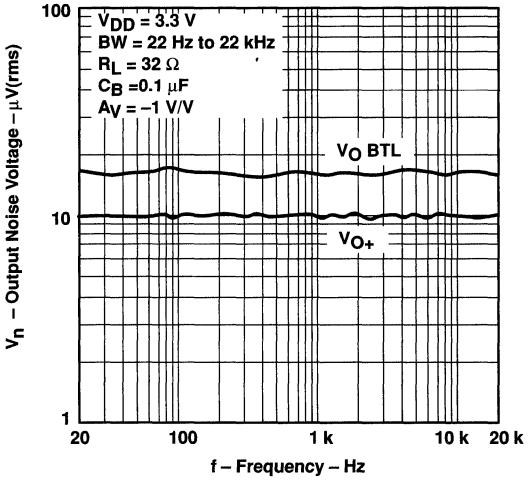


Figure 19

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

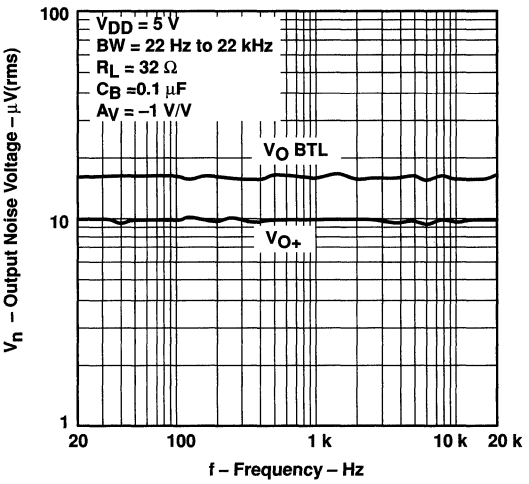


Figure 20

POWER DISSIPATION
vs
OUTPUT POWER

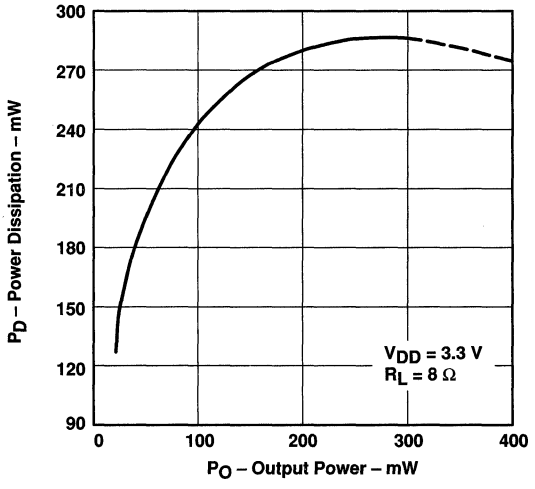


Figure 21

POWER DISSIPATION
vs
OUTPUT POWER

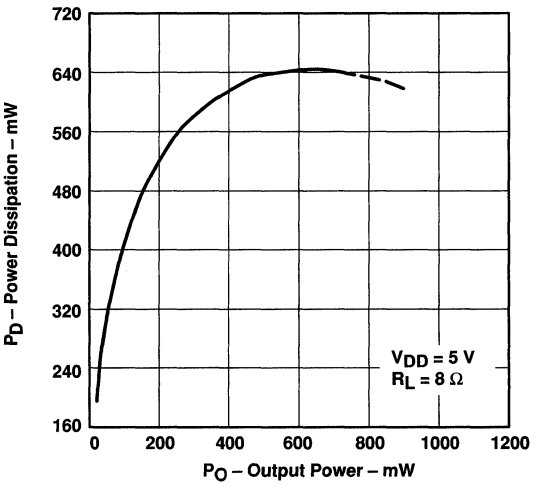


Figure 22

APPLICATION INFORMATION

bridge-tied load

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA301 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but power to the load should be initially considered. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

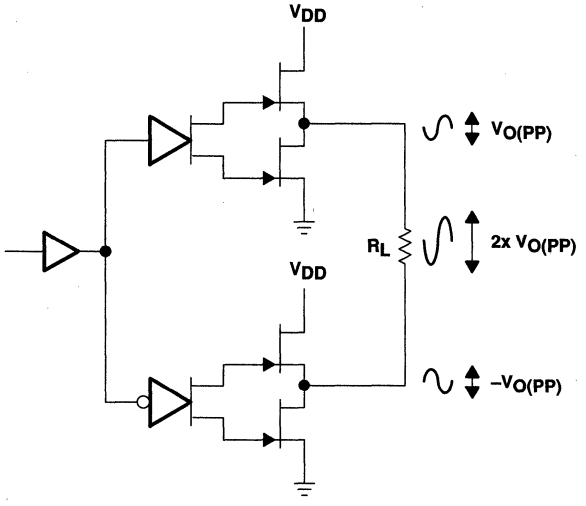


Figure 23. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, eliminating the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

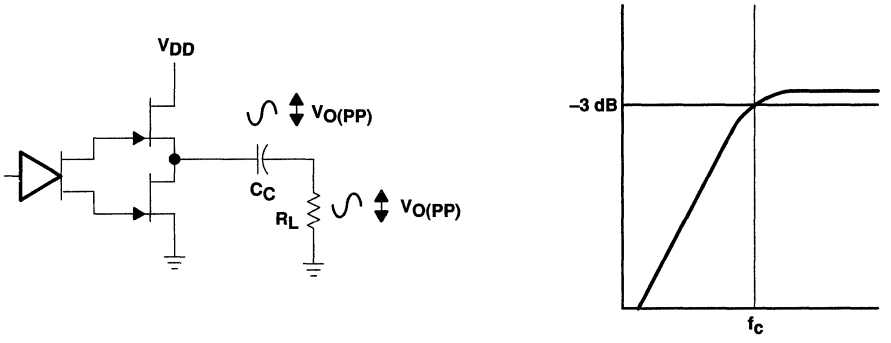


Figure 24. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

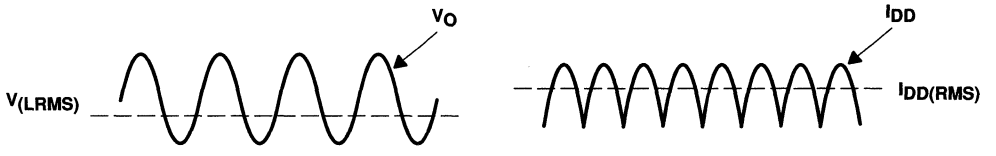


Figure 25. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-to-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

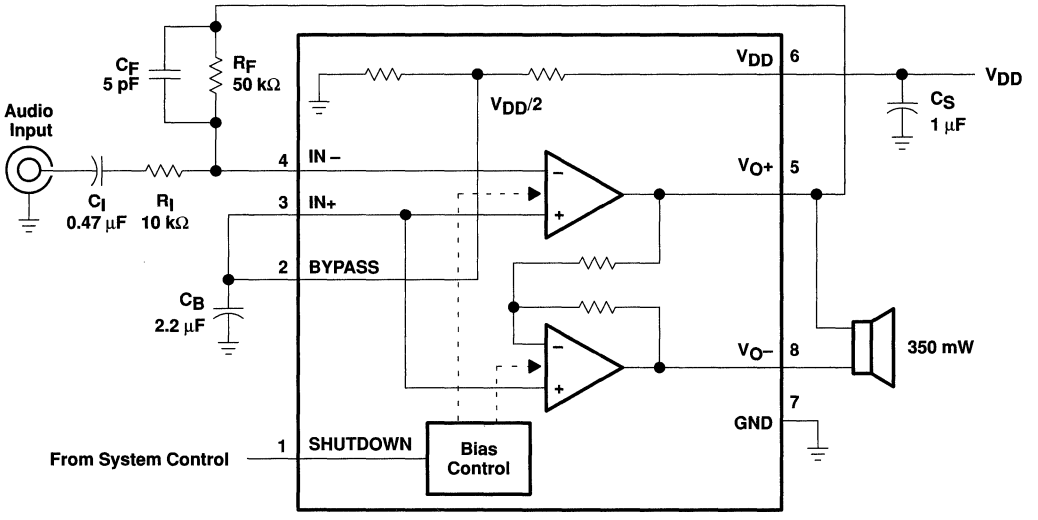


Figure 26. TPA301 Application Circuit

The following sections discuss the selection of the components used in Figure 26.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA301 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = A_V = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA301 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

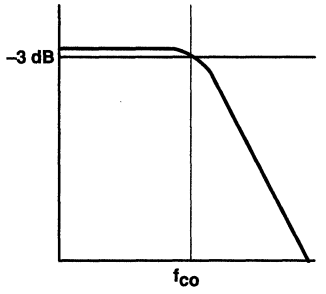
APPLICATION INFORMATION

component selection (continued)

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V, and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor, C_F, of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

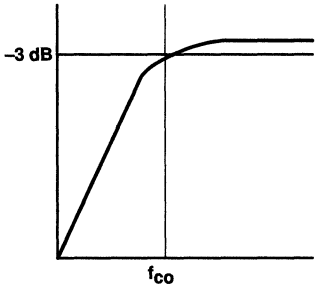


For example, if R_F is 100 kΩ and C_F is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \quad (9)$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA301 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained, which insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \tag{10}$$

As an example, consider a circuit where C_B is 2.2 μF, C_I is 0.47 μF, R_F is 50 kΩ and R_I is 10 kΩ. Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, C_B, values of 2.2 μF to 1 μF ceramic or tantalum **low-ESR** capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA301 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA301 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA301 data sheet, one can see that when the TPA301 is operating from a 5-V supply into a 8-Ω speaker 350 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10 \text{Log} P_W = 10\text{Log } 3500 \text{ mW} = -4.6 \text{ dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$-4.6 \text{ dB} - 15 \text{ dB} = -19.6 \text{ dB (15 dB headroom)}$$
$$-4.6 \text{ dB} - 12 \text{ dB} = -16.6 \text{ dB (12 dB headroom)}$$
$$-4.6 \text{ dB} - 9 \text{ dB} = -13.6 \text{ dB (9 dB headroom)}$$
$$-4.6 \text{ dB} - 6 \text{ dB} = -10.6 \text{ dB (6 dB headroom)}$$
$$-4.6 \text{ dB} - 3 \text{ dB} = -7.6 \text{ dB (3 dB headroom)}$$

Converting dB back into watts:

$$P_W = 10^{PdB/10}$$
$$= 11 \text{ mW (15 dB headroom)}$$
$$= 22 \text{ mW (12 dB headroom)}$$
$$= 44 \text{ mW (9 dB headroom)}$$
$$= 88 \text{ mW (6 dB headroom)}$$
$$= 175 \text{ mW (3 dB headroom)}$$

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 350 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA301 and maximum ambient temperatures is shown in Table 2.

Table 2. TPA301 Power Rating, 5-V, 8-Ω, BTL

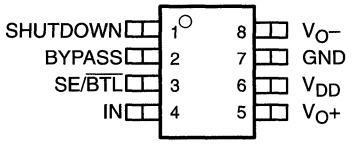
PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	MAXIMUM AMBIENT TEMPERATURE
			0 CFM
350	350 mW	600	46°C
350	175 mW (3 dB)	500	64°C
350	88 mW (6 dB)	380	85°C
350	44 mW (9 dB)	300	98°C
350	22 mW (12 dB)	200	115°C
350	11 mW (15 dB)	180	119°C

Table 2 shows that the TPA301 can be used to its full 350-mW rating without any heat sinking in still air up to 46°C.

SLOS207B – JANUARY 1998 – REVISED MARCH 2000

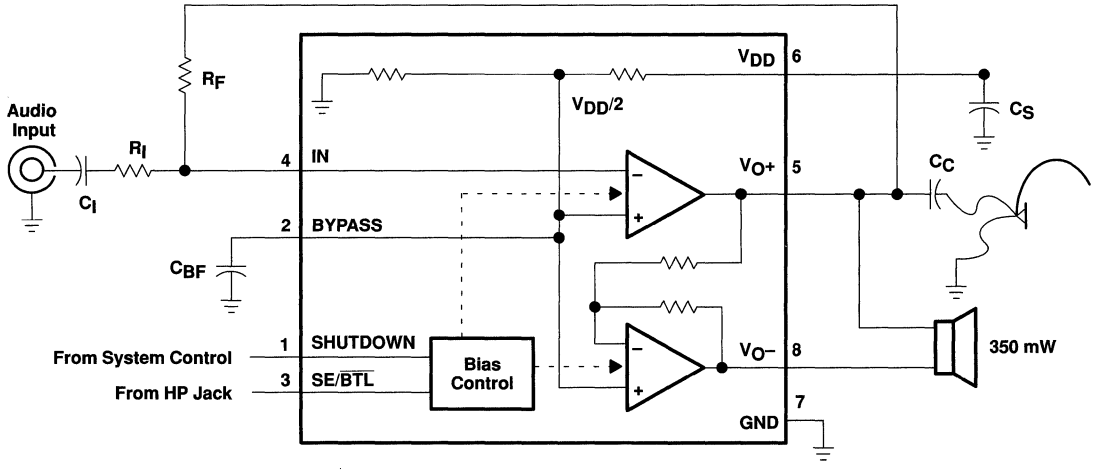
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility**
  2.5 V – 5.5 V
- **Output Power for R_L = 8 Ω**
  - **350 mW at V_{DD} = 5 V, BTL**
  - **250 mW at V_{DD} = 5 V, SE**
  - **250 mW at V_{DD} = 3.3 V, BTL**
  - **75 mW at V_{DD} = 3.3 V, SE**
- **Shutdown Control**
  - **I_{DD} = 7 μA at 3.3 V**
  - **I_{DD} = 60 μA at 5 V**
- **BTL to SE Mode Control**
- **Integrated Depop Circuitry**
- **Thermal and Short-Circuit Protection**
- **Surface Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA311 is a bridge-tied load (BTL) or single-ended (SE) audio power amplifier developed especially for low-voltage applications where internal speakers and external earphone operation are required. Operating with a 3.3-V supply, the TPA311 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. A unique feature of the TPA311 is that it allows the amplifier to switch from BTL to SE *on the fly* when an earphone drive is required. This eliminates complicated mechanical switching or auxiliary devices just to drive the external load. This device features a shutdown mode for power-sensitive applications with special depop circuitry to virtually eliminate speaker noise when exiting shutdown mode and during power cycling. The TPA311 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.



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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA311D	TPA311DGN	AAB

† The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA311DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN	4	I	IN is the audio input terminal.
SE/$\overline{\text{BTL}}$	3	I	When SE/$\overline{\text{BTL}}$ is held low, the TPA311 is in BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the TPA311 is in SE mode.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} = 60 µA, V_{DD} = 5 V).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive output for BTL and SE modes.
V_O–	8	O	V_O– is the negative output in BTL mode and a high-impedance output in SE mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W§	17.1 mW/°C	1.37 W	1.11 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A (see Table 3)	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)	See Note 1			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V	BTL mode		85		dB
			SE mode		83		
I_{DD}	Supply current (see Figure 6)	BTL mode			0.7	1.5	mA
		SE mode			0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)				7	50	μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%,	BTL mode,	See Figure 14		250		mW
		THD = 0.5%,	SE mode			110		
THD + N	Total harmonic distortion plus noise	P_O = 250 mW, See Figure 12	f = 20 Hz to 4 kHz,	Gain = 2,		1.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 3%,	See Figure 12		10		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 36			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 μF,	BTL mode,		71		dB
		f = 1 kHz, See Figure 3	C_B = 1 μF,	SE mode,		86		
V_n	Noise output voltage	Gain = 1, BTL,	C_B = 0.1 μF, See Figure 42	R_L = 32 Ω,		15		μV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)				5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V	BTL mode		78		dB
			SE mode		76		
I_{DD}	Supply current (see Figure 6)	BTL mode			0.7	1.5	mA
		SE mode			0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)				60	100	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%,	BTL mode,	See Figure 18		700		mW
		THD = 0.5%,	SE mode			300		
THD + N	Total harmonic distortion plus noise	P_O = 350 mW, See Figure 16	f = 20 Hz to 4 kHz,	Gain = 2,		1%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 16		10		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 37			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 µF,	BTL mode,		65		dB
		f = 1 kHz, See Figure 4	C_B = 1 µF,	SE mode,		75		
V_n	Noise output voltage	Gain = 1, BTL,	C_B = 0.1 µF, See Figure 43	R_L = 32 Ω,		15		µV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

PARAMETER MEASUREMENT INFORMATION

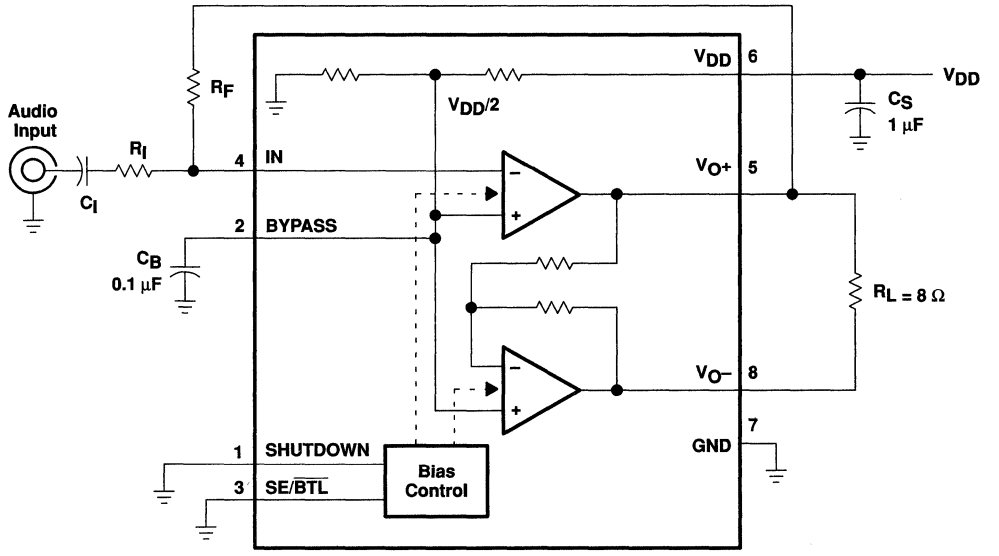


Figure 1. BTL Mode Test Circuit

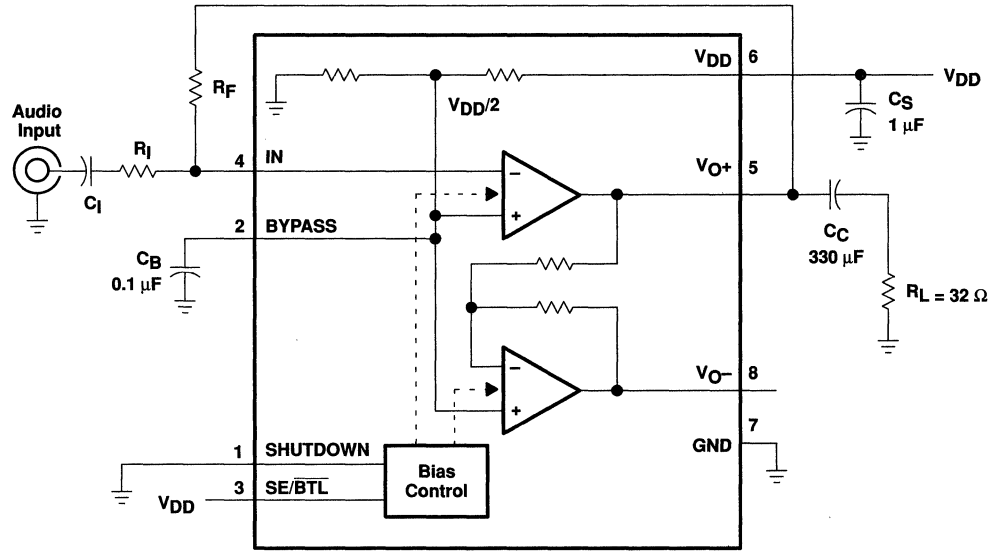


Figure 2. SE Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply voltage rejection ratio	vs Frequency	3, 4, 5
I_{DD}	Supply current	vs Supply voltage	6, 7
P_O	Output power	vs Supply voltage	8, 9
		vs Load resistance	10, 11
THD+N	Total harmonic distortion plus noise	vs Frequency	12, 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33
		vs Output power	14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35
	Open loop gain and phase	vs Frequency	36, 37
	Closed loop gain and phase	vs Frequency	38, 39, 40, 41
V_n	Output noise voltage	vs Frequency	42, 43
P_D	Power dissipation	vs Output power	44, 45, 46, 47

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

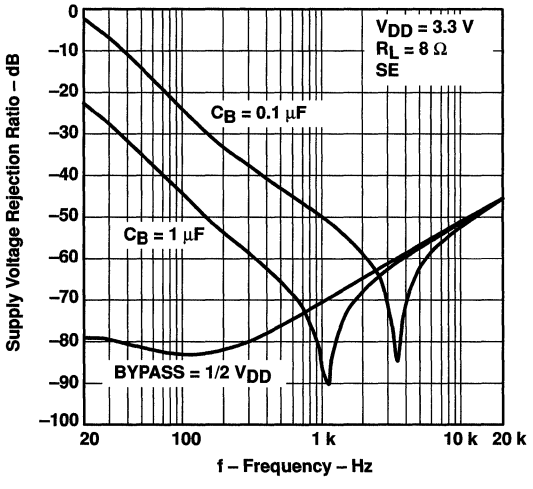


Figure 3

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

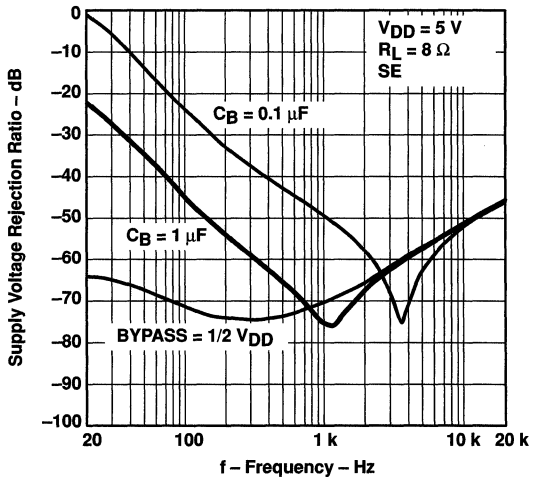


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

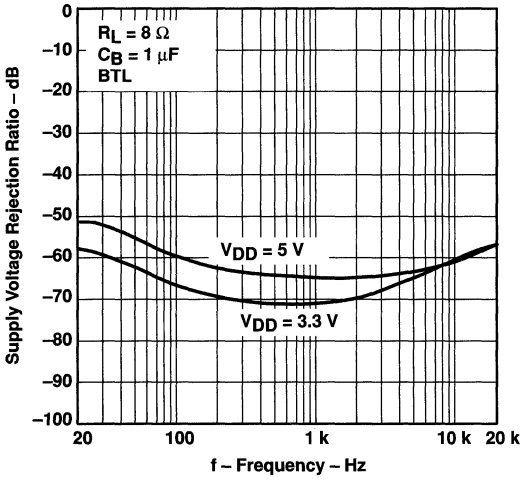


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

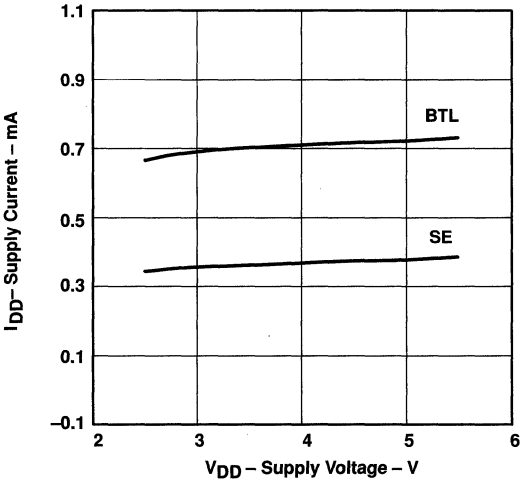


Figure 6

SUPPLY CURRENT (SHUTDOWN)
vs
SUPPLY VOLTAGE

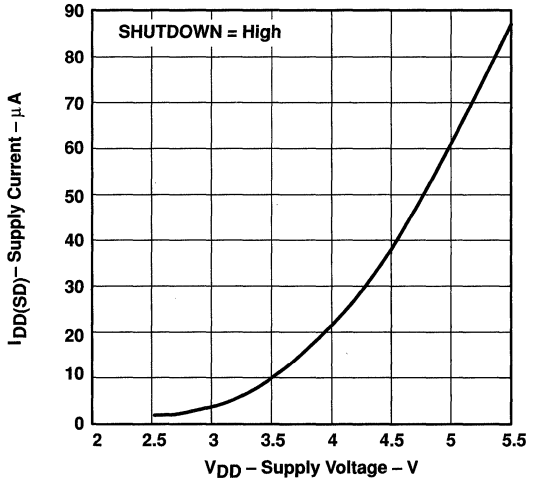


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

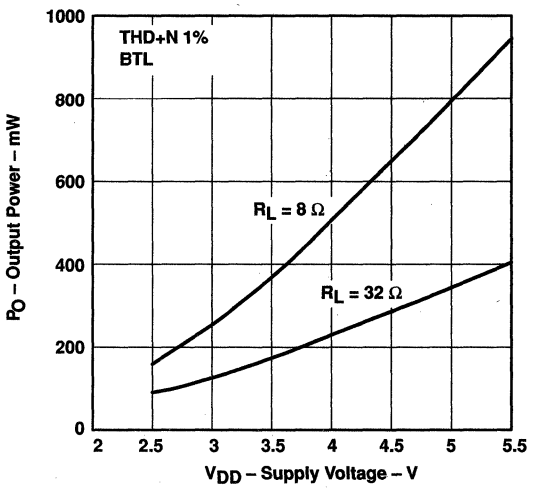


Figure 8

OUTPUT POWER
vs
SUPPLY VOLTAGE

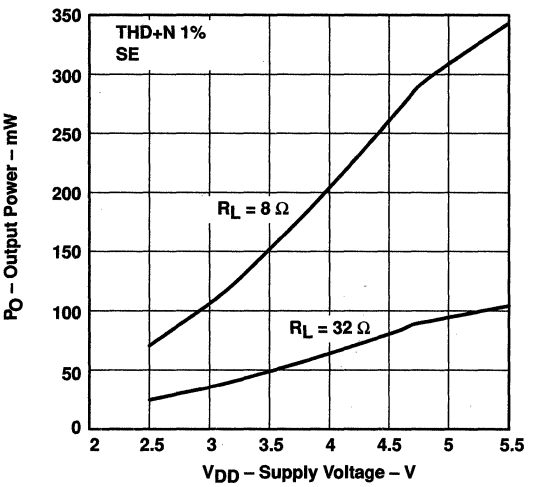


Figure 9

OUTPUT POWER
vs
LOAD RESISTANCE

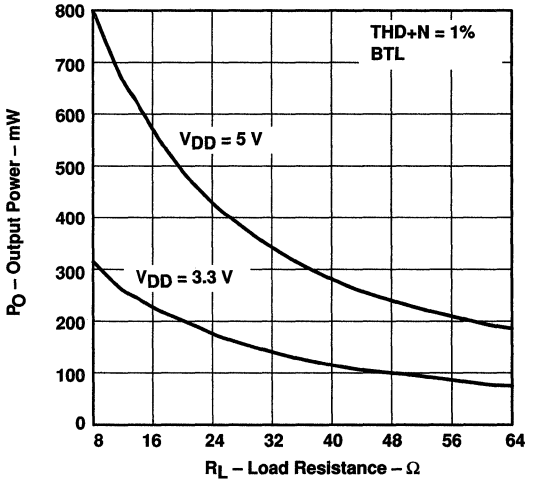


Figure 10

OUTPUT POWER
vs
LOAD RESISTANCE

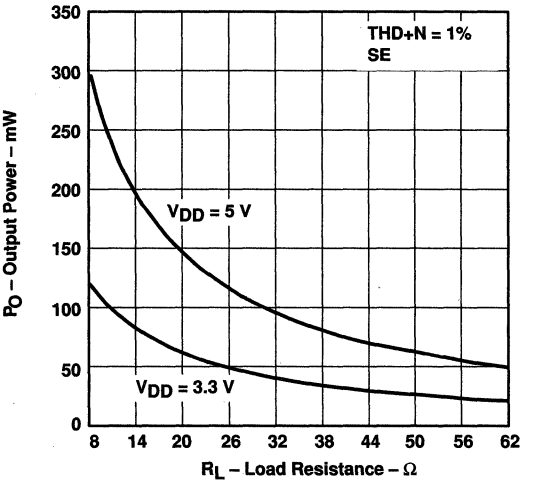


Figure 11

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

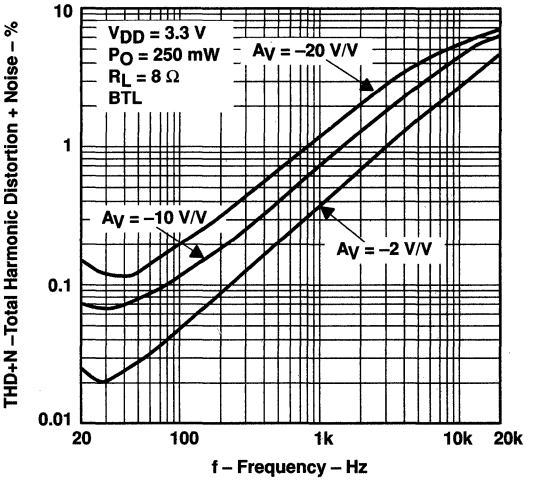


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

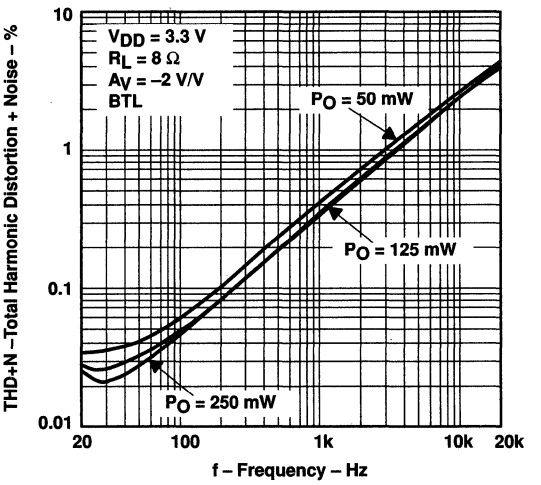


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

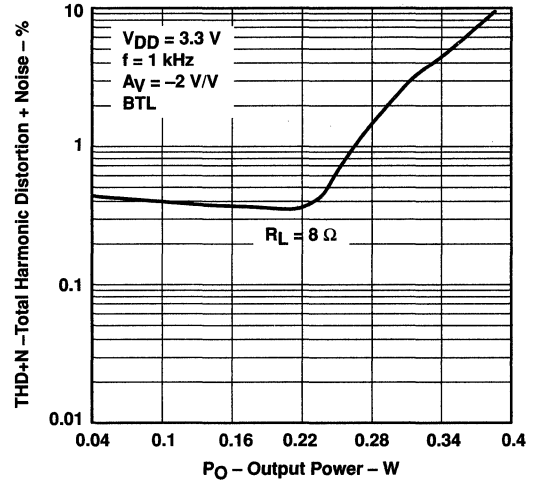


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

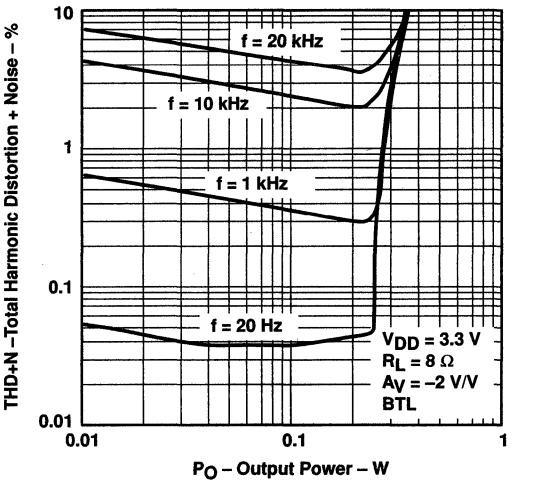


Figure 15

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

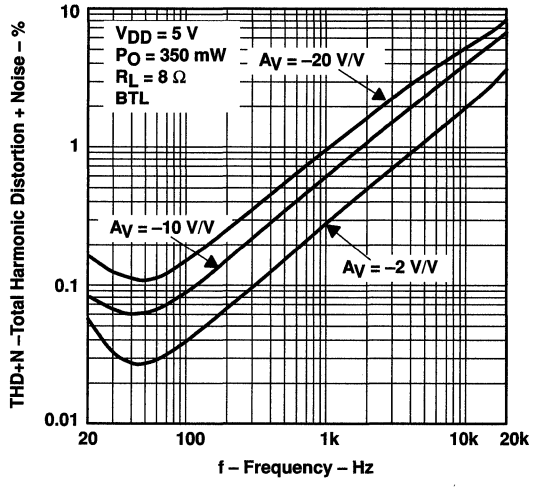


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

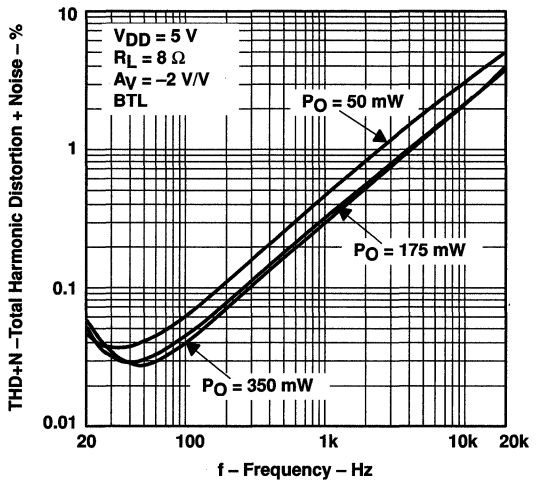


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

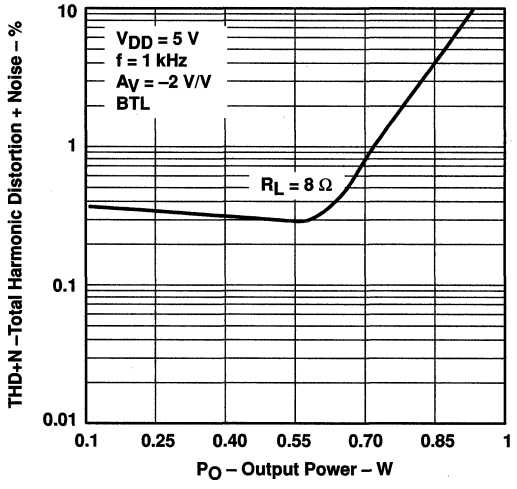


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

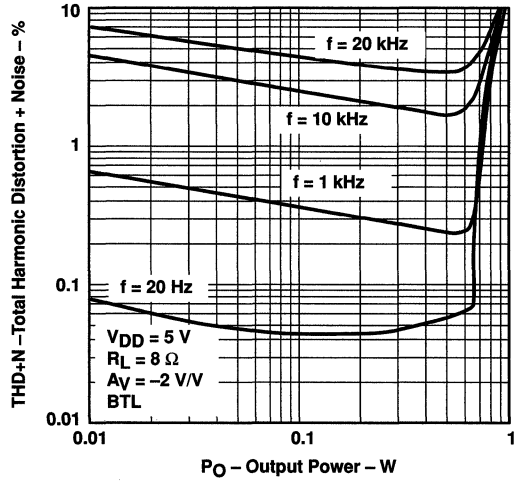


Figure 19

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

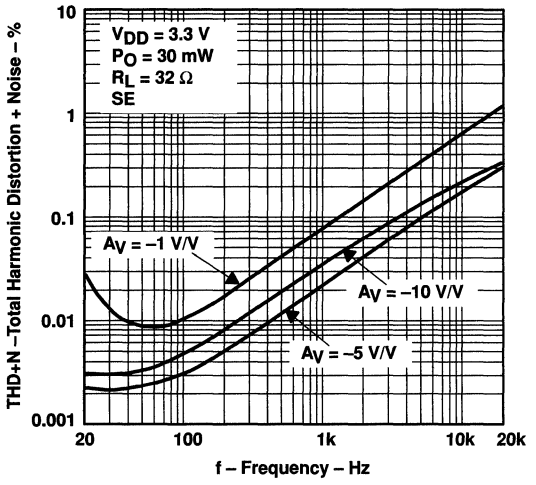


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

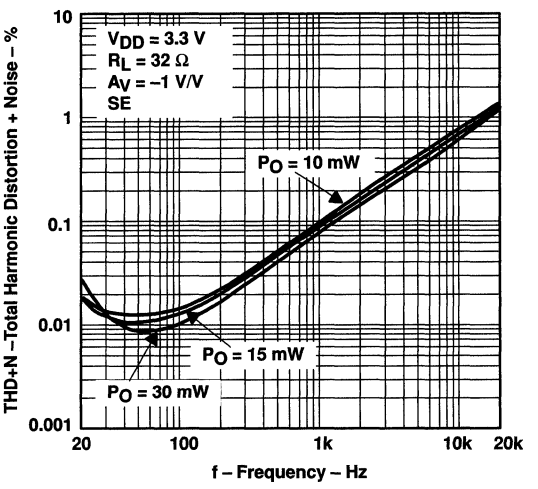


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

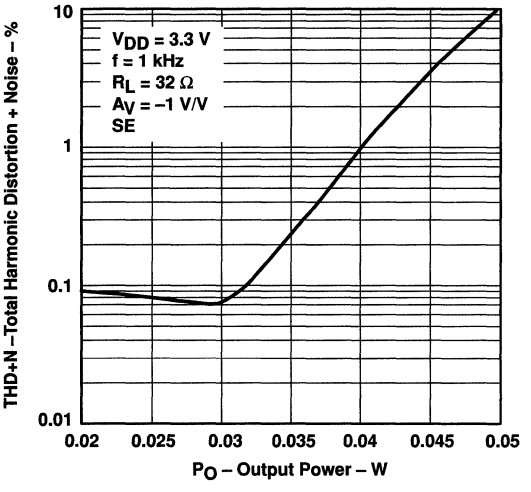


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

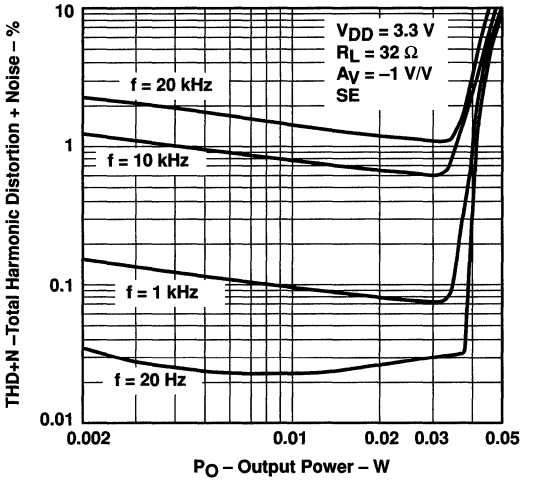


Figure 23

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

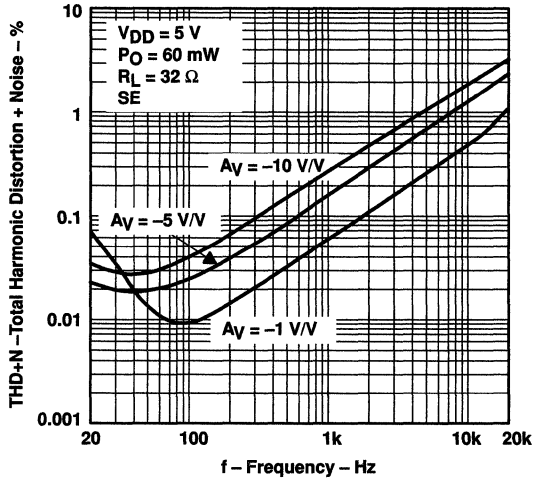


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

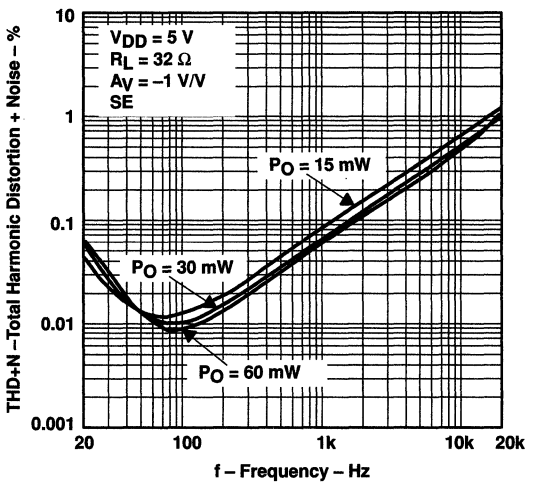


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

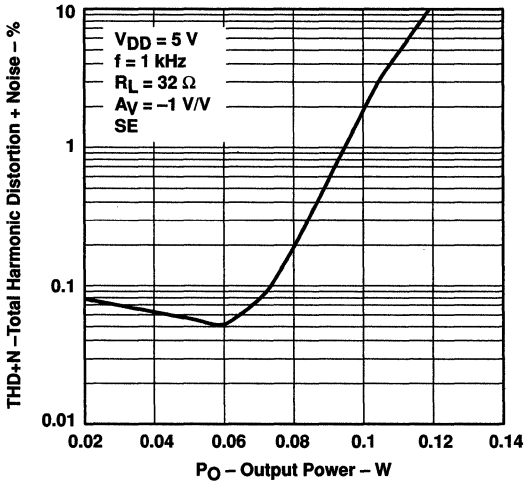


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

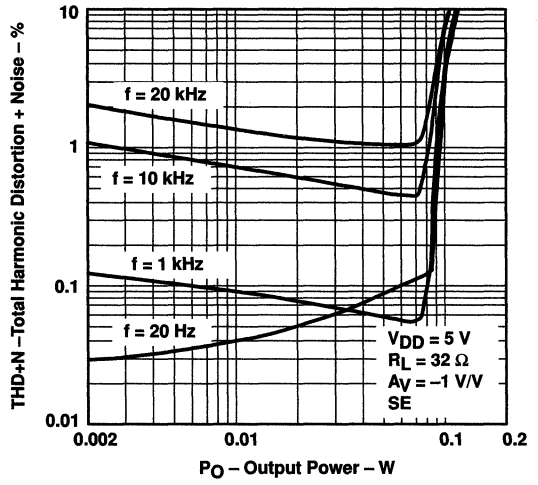


Figure 27

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

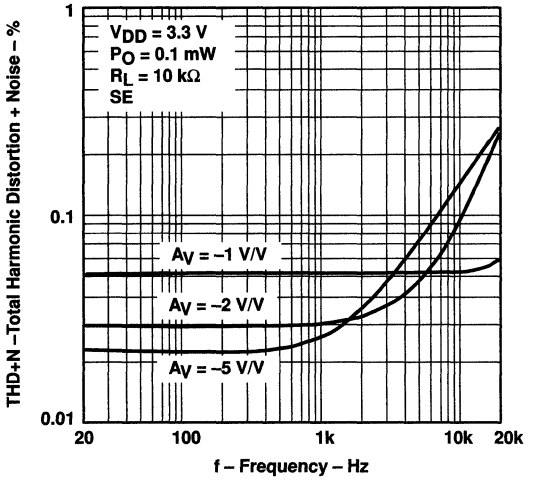


Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

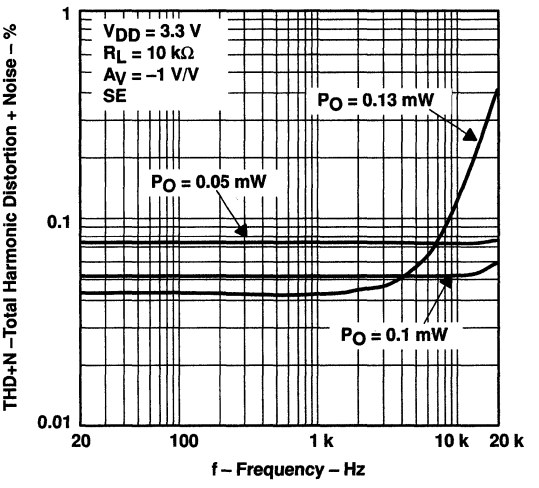


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

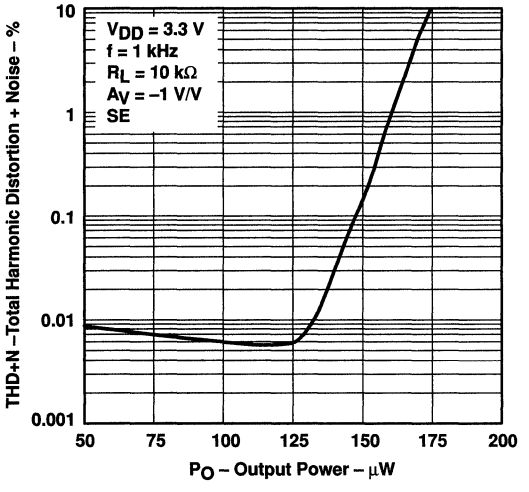


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

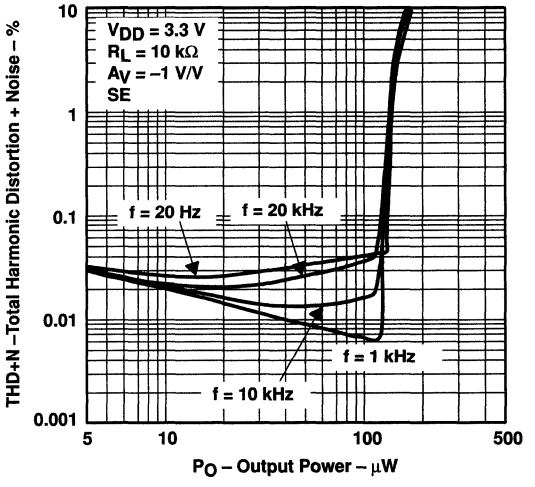


Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

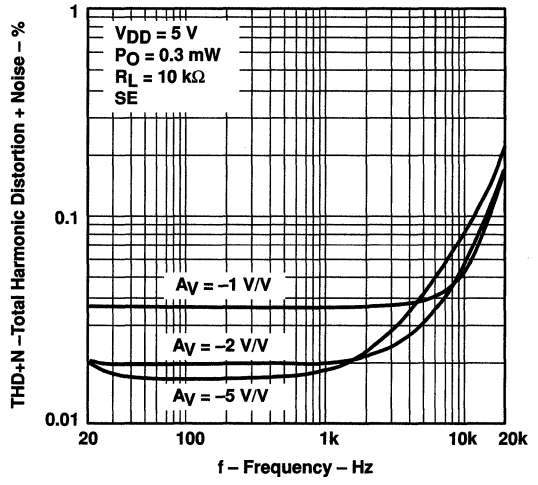


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

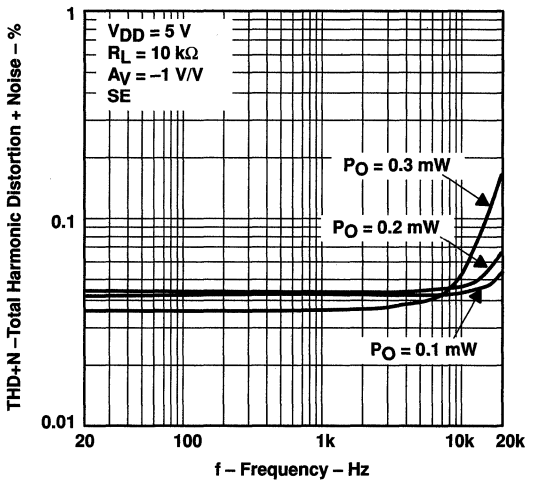


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

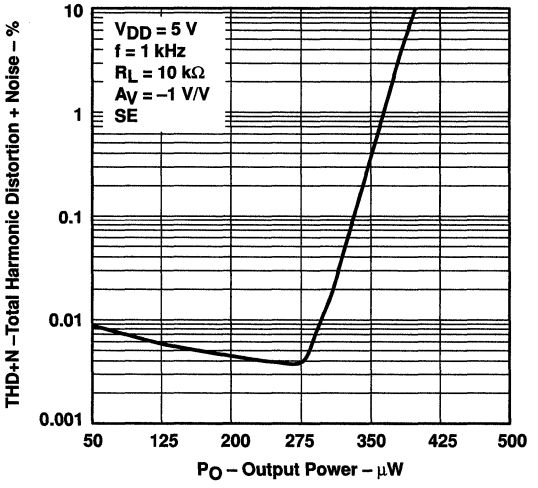


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

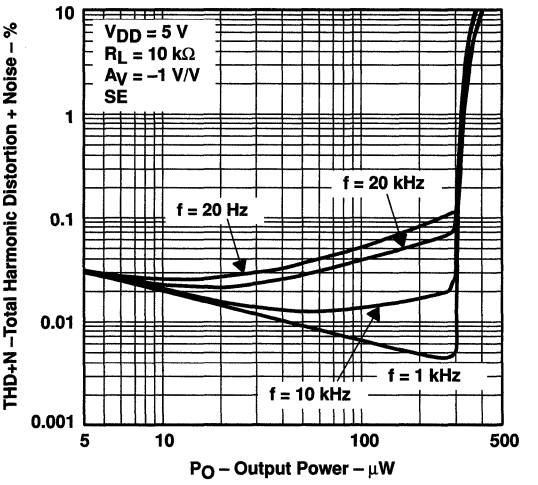


Figure 35

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

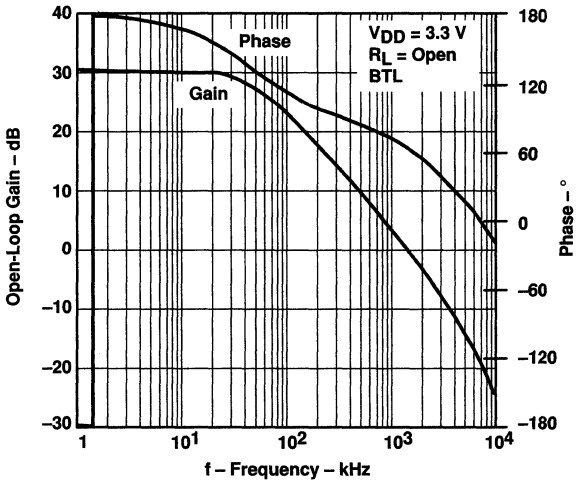


Figure 36

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

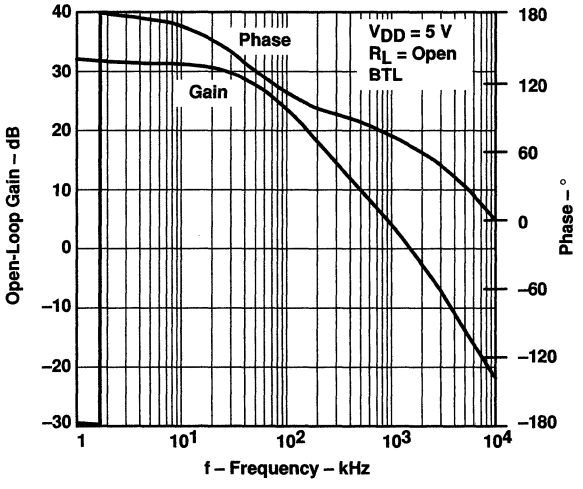


Figure 37

TYPICAL CHARACTERISTICS

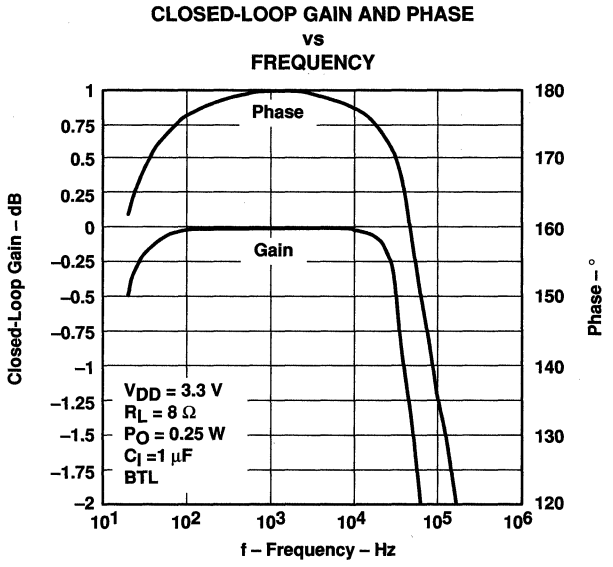


Figure 38

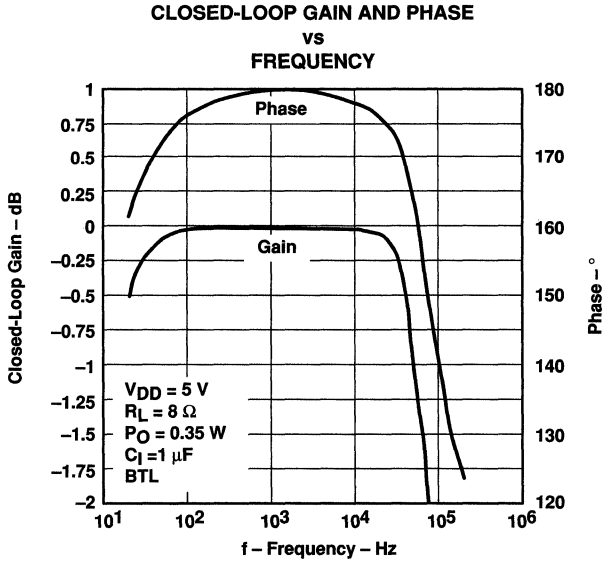


Figure 39

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

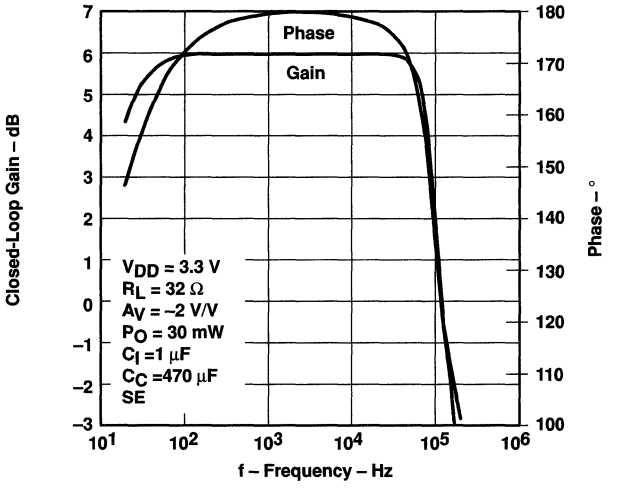


Figure 40

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

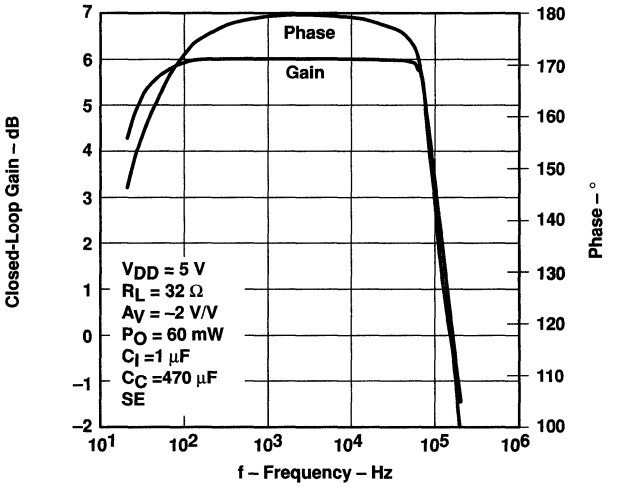


Figure 41

TYPICAL CHARACTERISTICS

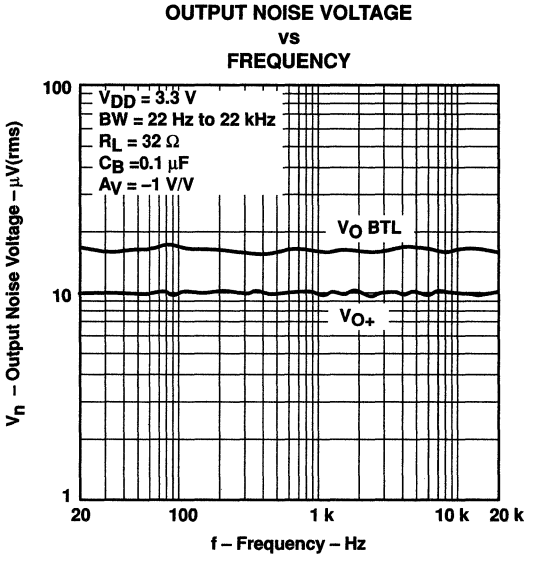


Figure 42

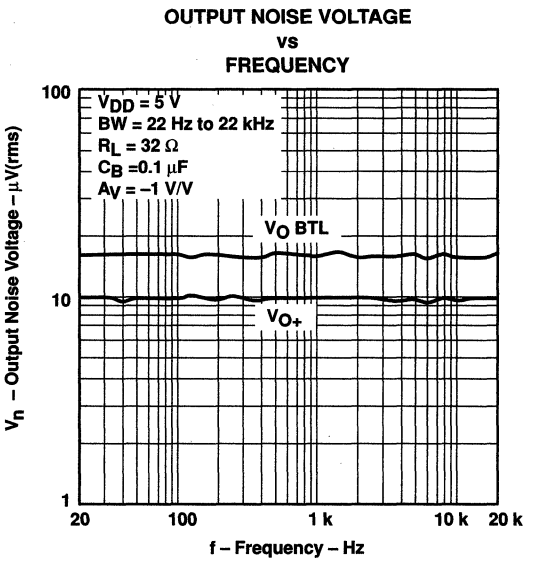


Figure 43

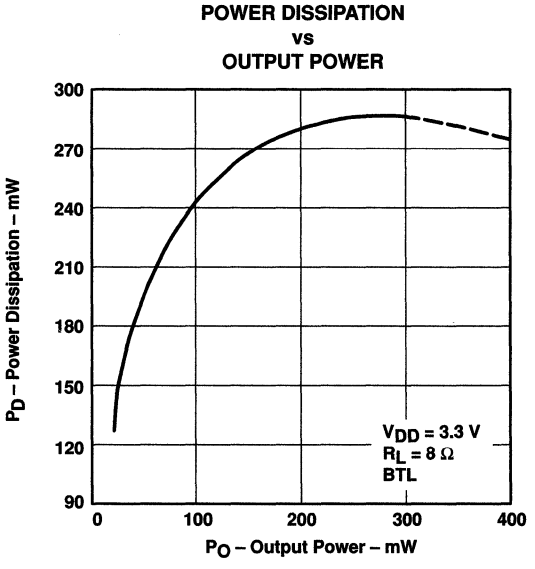


Figure 44

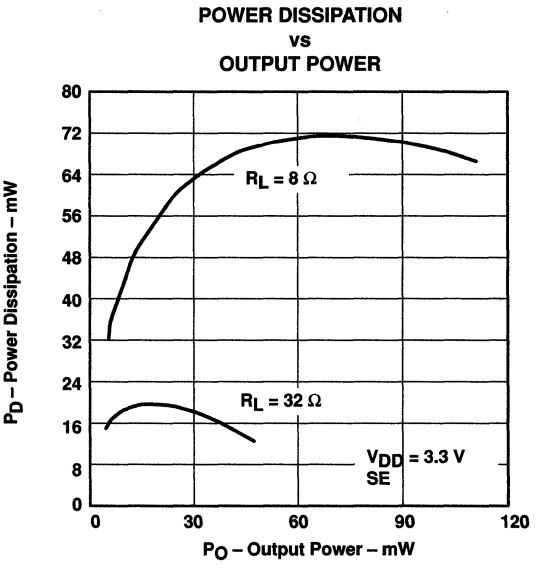


Figure 45

TYPICAL CHARACTERISTICS

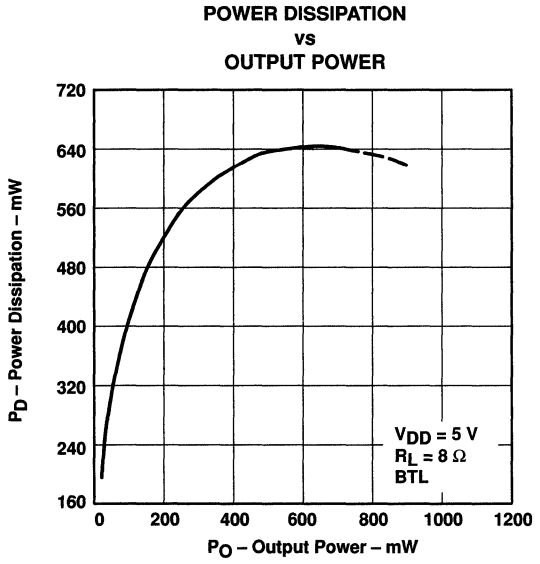


Figure 46

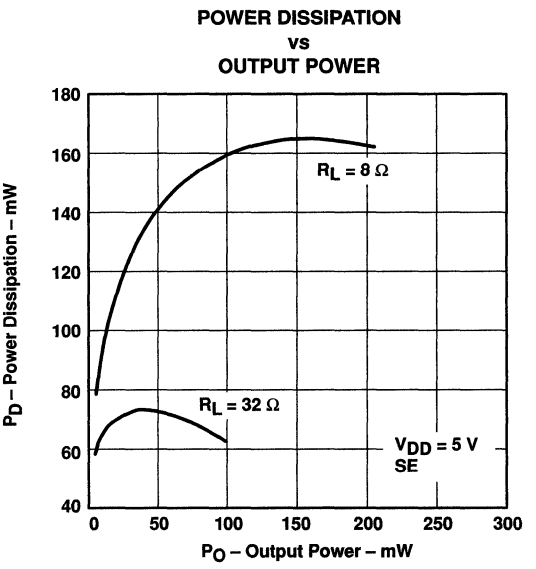


Figure 47

APPLICATION INFORMATION

bridge-tied load versus single-ended mode

Figure 48 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA311 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

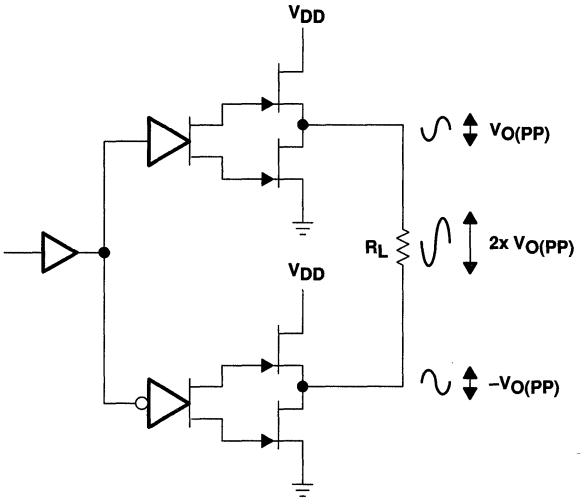


Figure 48. Bridge-Tied Load Configuration

In typical portable handheld equipment, a sound channel operating at 3.3 V and using bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In terms of sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 49. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), tend to be expensive, heavy, and occupy valuable PCB area. These capacitors also have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

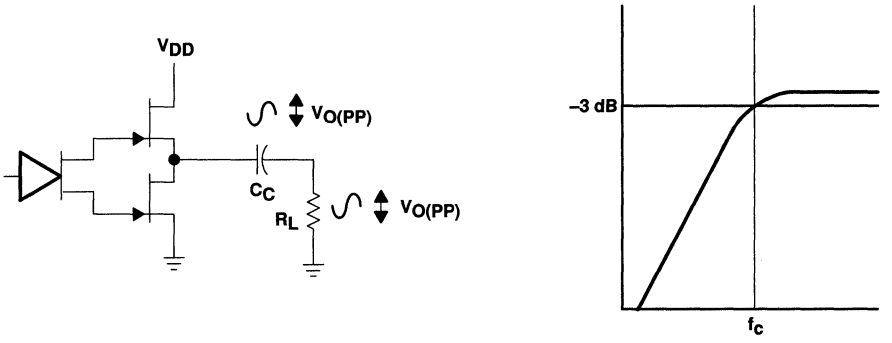


Figure 49. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable, considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 50).

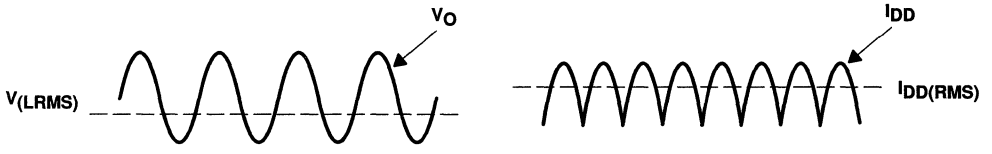


Figure 50. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency Vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 51 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

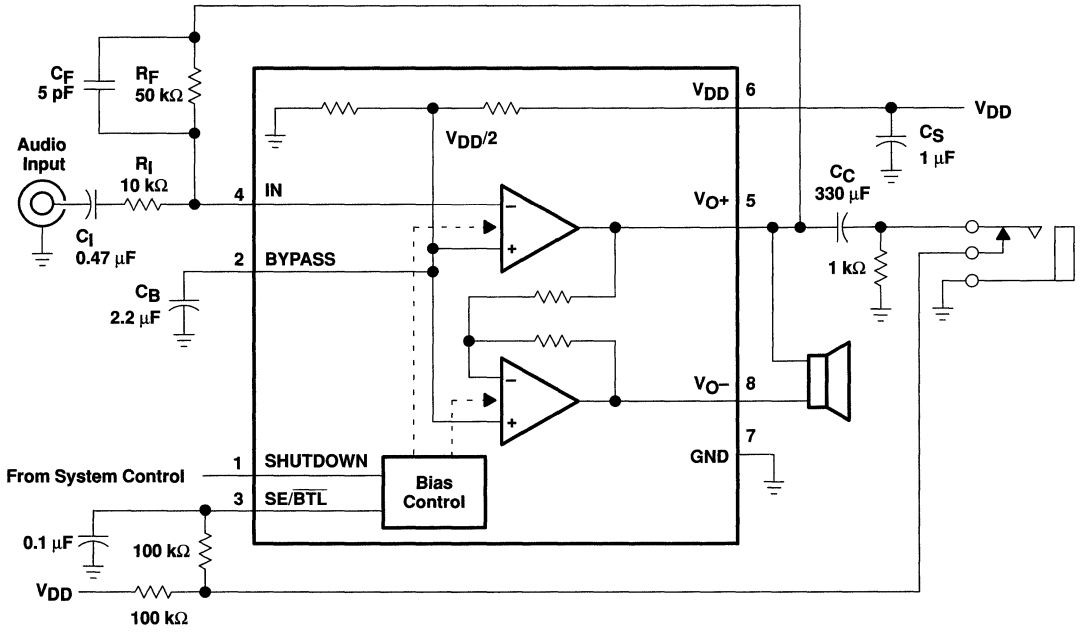


Figure 51. TPA311 Application Circuit

The following sections discuss the selection of the components used in Figure 51.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA311 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = A_V = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA311 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

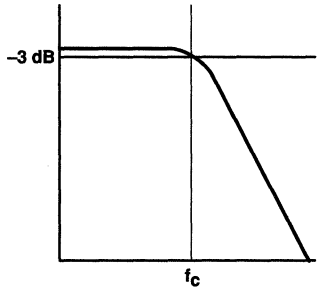
APPLICATION INFORMATION

component selection (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor, C_F, of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

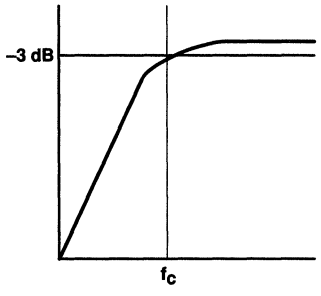


For example, if R_F is 100 kΩ and C_F is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA311 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained, which insures the input capacitor is fully charged before the bypass capacitor is fuly charged and the amplifier starts up.

$$\frac{10}{(C_B \times 250\ k\Omega)} \leq \frac{1}{(R_F + R_I)\ C_I} \tag{10}$$

As an example, consider a circuit where C_B is 2.2 µF, C_I is 0.47 µF, R_F is 50 kΩ and R_I is 10 kΩ. Inserting these values into the equation 10 we get: $18.2 \leq 35.5$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 2.2 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

In SE mode (see Figure 51), the load is driven from the primary amplifier output (V_O+, terminal 5).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = A_V = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

APPLICATION INFORMATION

single-ended operation (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{10}{(C_B \times 250\ k\Omega)} \leq \frac{1}{(R_F + R_I)\ C_I} \lll \frac{1}{R_L C_C} \qquad (12)$$

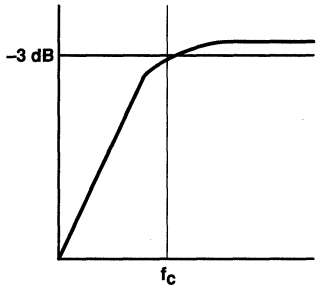
As an example, consider a circuit where C_B is 0.2.2 µF, C_I is 0.47 µF, C_C is 330 µF, R_F is 50 kΩR_L is 32 Ω, and R_I is 10 kΩ. Inserting these values into the equation 12 we get:

18.2 < 35.5 ⋘ 94.7 which satisfies the rule.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{c(high\ pass)} = \frac{1}{2\pi R_L C_C} \qquad (13)$$



The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates an 8-Ω load is adequate, earphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA311 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional earphone amplifier in applications where internal speakers are driven in BTL mode but external earphone or speaker must be accommodated. Internal to the TPA311, two separate amplifiers drive V_O+ and V_O-. The SE/$\overline{\text{BTL}}$ input (terminal 3) controls the operation of the follower amplifier that drives V_O- (terminal 8). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA311 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the V_O- amplifier is in a high output impedance state, which configures the TPA311 as an SE driver from V_O+ (terminal 5). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level TTL source or, more typically, from a resistor divider network as shown in Figure 52.

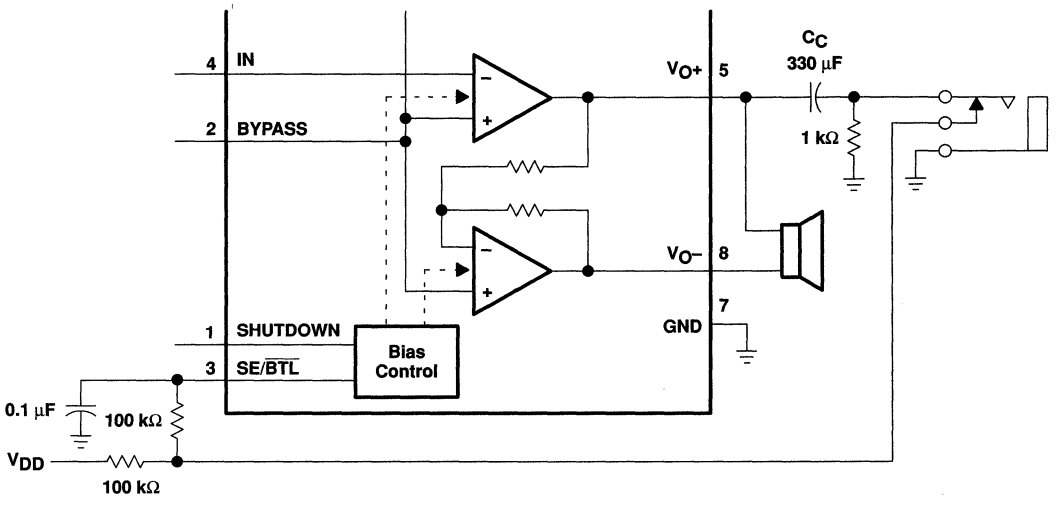


Figure 52. TPA311 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) mono earphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the V_O- amplifier is shutdown causing the BTL speaker to mute (virtually open-circuits the speaker). The V_O+ amplifier then drives through the output capacitor (C_C) into the earphone jack.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA311 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA311 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level of operation from 5-V supplies.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA311 data sheet, one can see that when the TPA311 is operating from a 5-V supply into a 8-Ω speaker that 350 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right)$$
$$= 10\text{Log}\left(\frac{350\ \text{mW}}{1\ \text{W}}\right)$$
$$= -4.6\ \text{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

−4.6 dB − 15 dB = − 19.6 dB (15 dB headroom)
−4.6 dB − 12 dB = − 16.6 dB (12 dB headroom)
−4.6 dB − 9 dB = − 13.6 dB (9 dB headroom)
−4.6 dB − 6 dB = − 10.6 dB (6 dB headroom)
−4.6 dB − 3 dB = − 7.6 dB (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
= 11 mW (15 dB headroom)
= 22 mW (12 dB headroom)
= 44 mW (9 dB headroom)
= 88 mW (6 dB headroom)
= 175 mW (3 dB headroom)

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 350 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA311 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA311 Power Rating, 5-V, 8-Ω, BTL

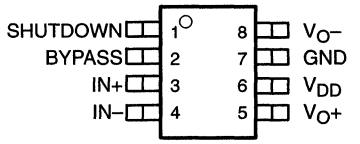
PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	MAXIMUM AMBIENT TEMPERATURE	
			0 CFM SOIC	0 CFM DGN
350	350 mW	600	46°C	114°C
350	175 mW (3 dB)	500	64°C	120°C
350	88 mW (6 dB)	380	85°C	125°C
350	44 mW (9 dB)	300	98°C	125°C
350	22 mW (12 dB)	200	115°C	125°C
350	11 mW (15 dB)	180	119°C	125°C

Table 3 shows that the TPA311 can be used to its full 350-mW rating without any heat sinking in still air up to 46°C.

SLOS229B – NOVEMBER1998 – REVISED MARCH 2000

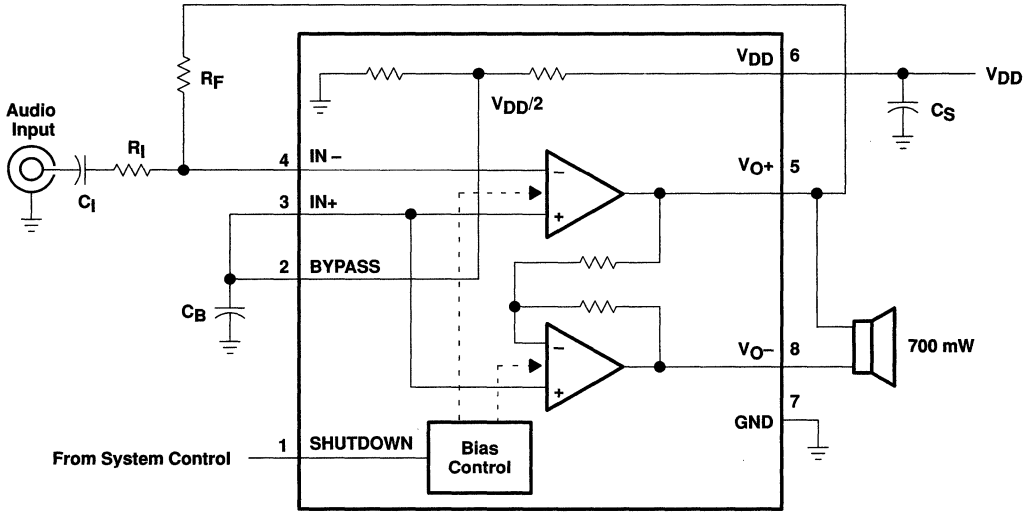
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility 2.5 V – 5.5 V**
- **Output Power for R_L = 8 Ω**
  - **700 mW at V_{DD} = 5 V, BTL**
  - **250 mW at V_{DD} = 3.3 V, BTL**
- **Ultra-Low Quiescent Current in Shutdown Mode . . . 1.5 nA**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA701 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA701 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 0.6% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a supply current of 1.5 nA during shutdown. The TPA701 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP SYMBOLIZATION
	SMALL OUTLINE† (D)	MSOP‡ (DGN)	
–40°C to 85°C	TPA701D	TPA701DGN	ABA

† In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

‡ The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA701DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 2.2-µF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN–	4	I	IN– is the inverting input. IN– is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} = 1.5 nA).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive BTL output.
V_O–	8	O	V_O– is the negative BTL output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)	See Note 1			20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		85		dB
I_{DD}	Supply current	BTL mode		1.25	2.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)	See Note 2		1.5	1000	nA

NOTES: 1. At 3 V < V_{DD} < 5 V the dc output voltage is approximately V_{DD}/2.
2. This parameter is measured with no external capacitors connected to the device.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 3	THD = 0.2%,	See Figure 9			250		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 200 Hz to 4 kHz,	See Figure 7		0.55%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 7		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 15			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz,	C_B = 1 µF,	See Figure 2		79		dB
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 µF,	See Figure 19		17		µV(rms)

NOTE 3: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)				20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		78		dB
I_{DD}	Supply current			1.25	2.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)			5	1500	nA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	See Figure 13			700†		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 200 Hz to 4 kHz,	See Figure 11		0.5%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 11		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 16			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz,	C_B = 1 µF,	See Figure 2		80		dB
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 µF,	See Figure 20		17		µV(rms)

† The DGN package, properly mounted, can conduct 700 mW RMS power continuously. The D package, can only conduct 350 mW RMS power continuously, with peaks to 700 mW.

PARAMETER MEASUREMENT INFORMATION

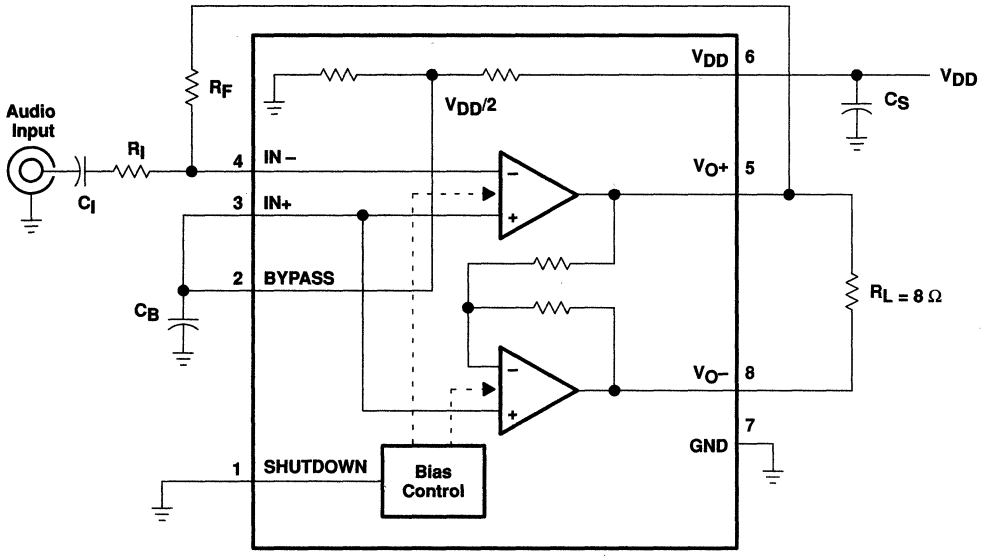


Figure 1. BTL Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply ripple rejection ratio	vs Frequency	2
I_{DD}	Supply current	vs Supply voltage	3, 4
P_O	Output power	vs Supply voltage	5
		vs Load resistance	6
THD+N	Total harmonic distortion plus noise	vs Frequency	7, 8, 11, 12
		vs Output power	9, 10, 13, 14
	Open loop gain and phase	vs Frequency	15, 16
	Closed loop gain and phase	vs Frequency	17, 18
V_n	Output noise voltage	vs Frequency	19, 20
P_D	Power dissipation	vs Output power	21, 22

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

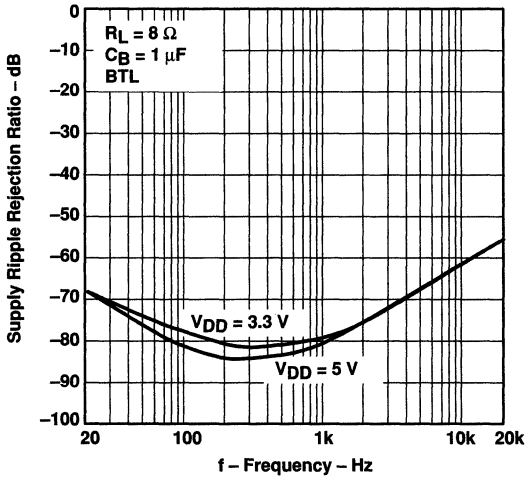


Figure 2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

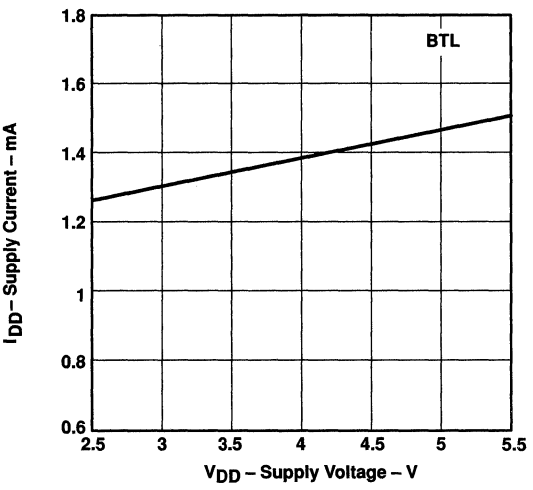


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

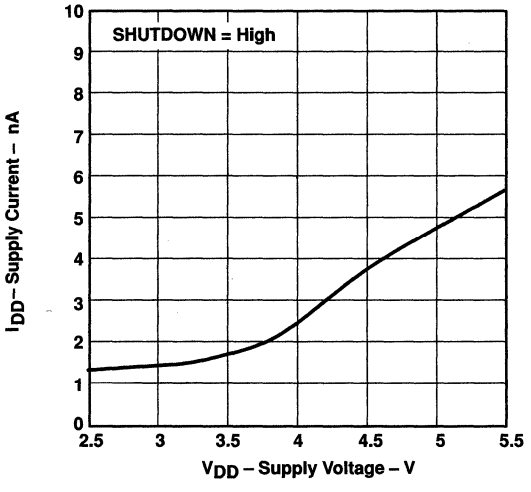


Figure 4

TYPICAL CHARACTERISTICS

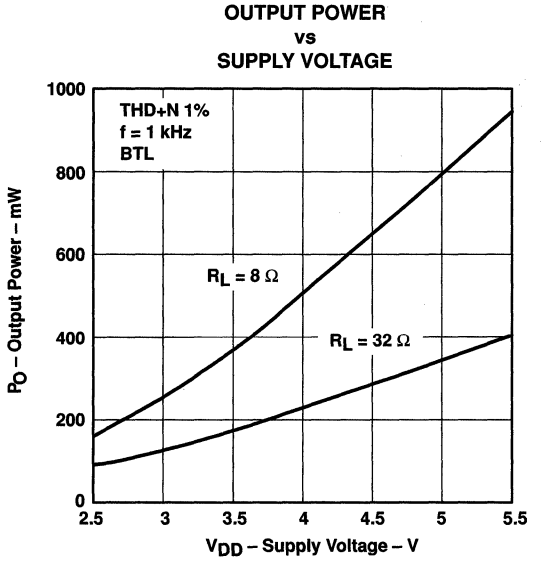


Figure 5

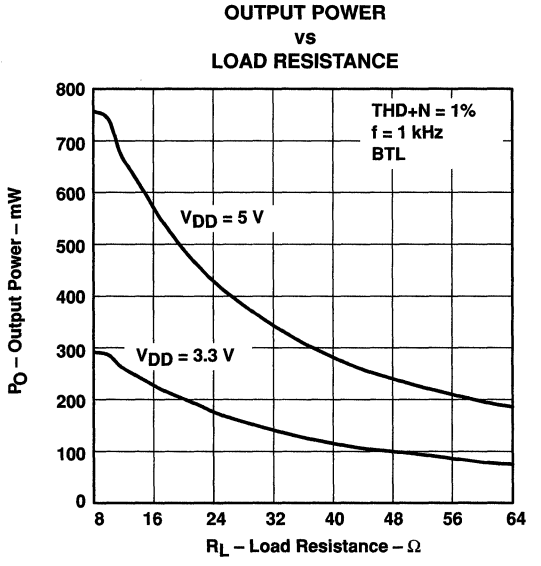


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

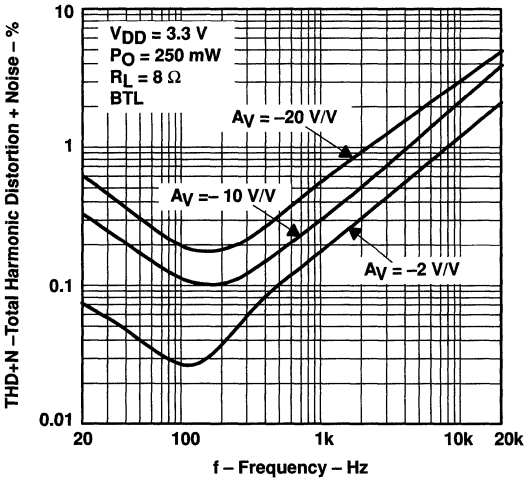


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

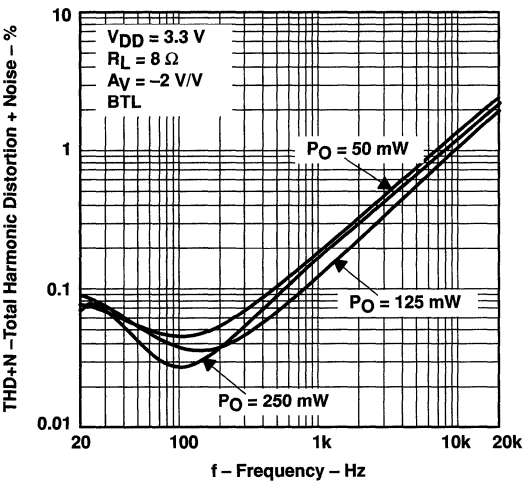


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

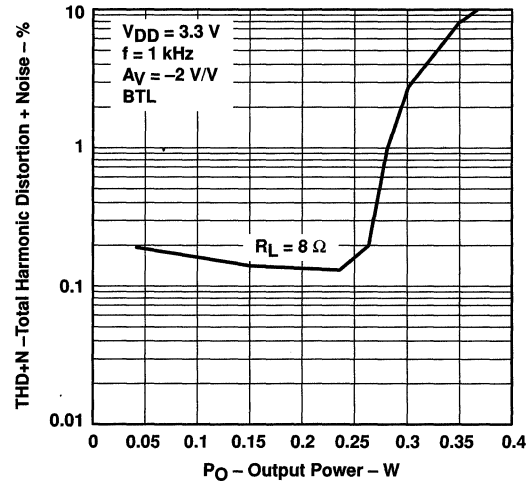


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

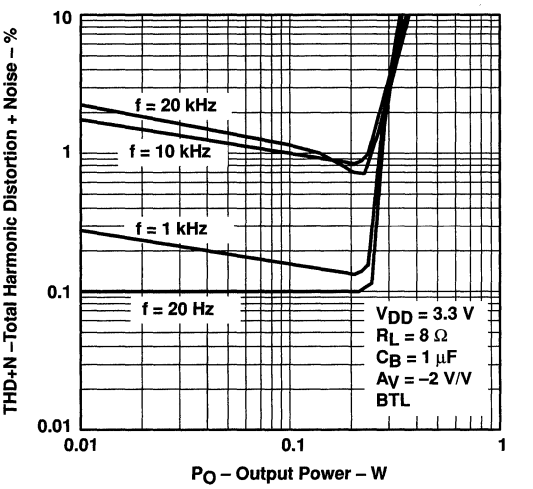


Figure 10

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

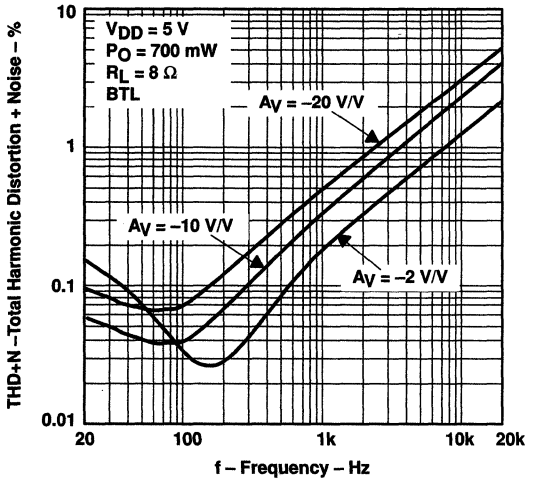


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

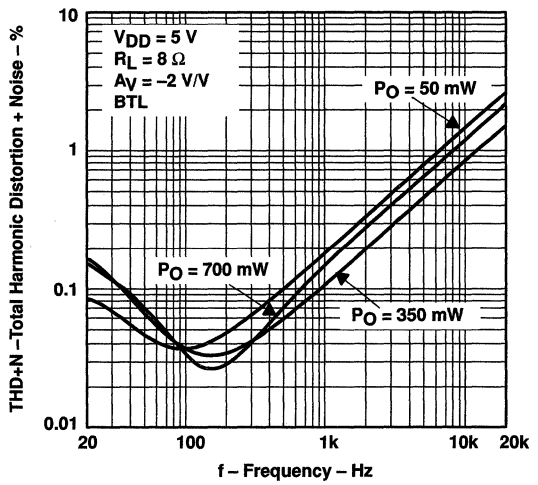


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

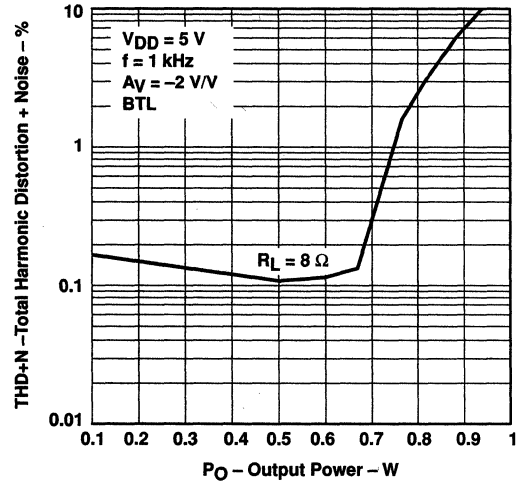


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

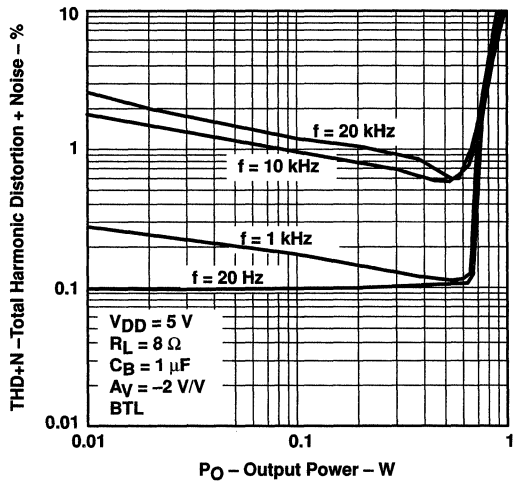


Figure 14

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

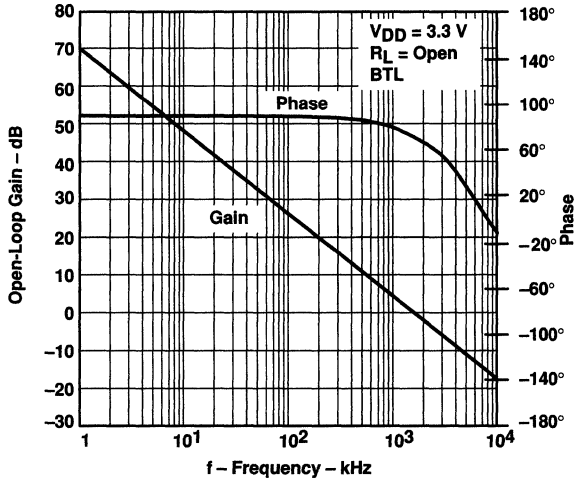


Figure 15

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

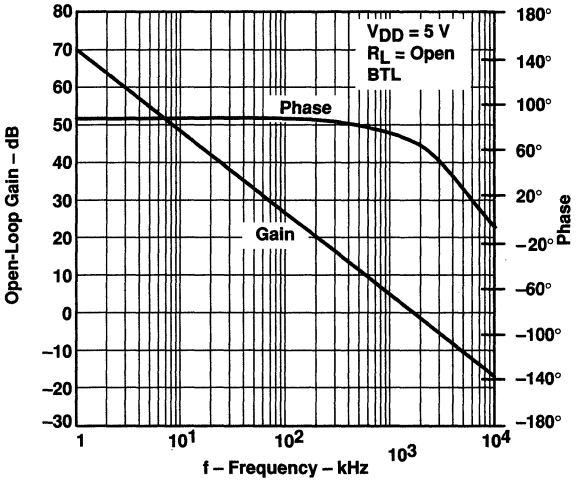


Figure 16

TYPICAL CHARACTERISTICS

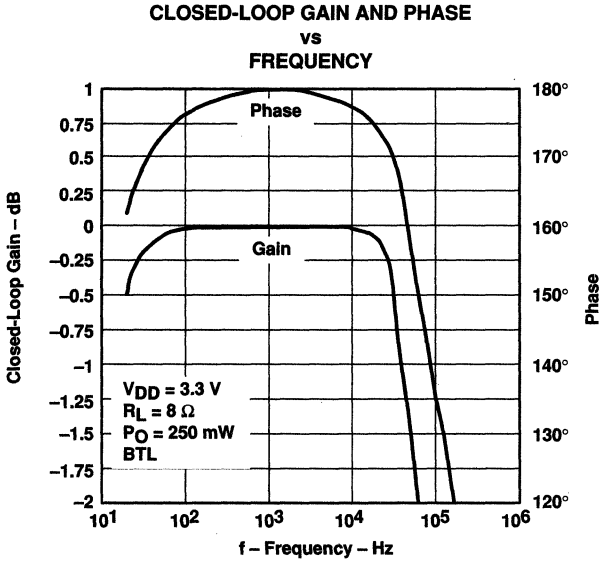


Figure 17

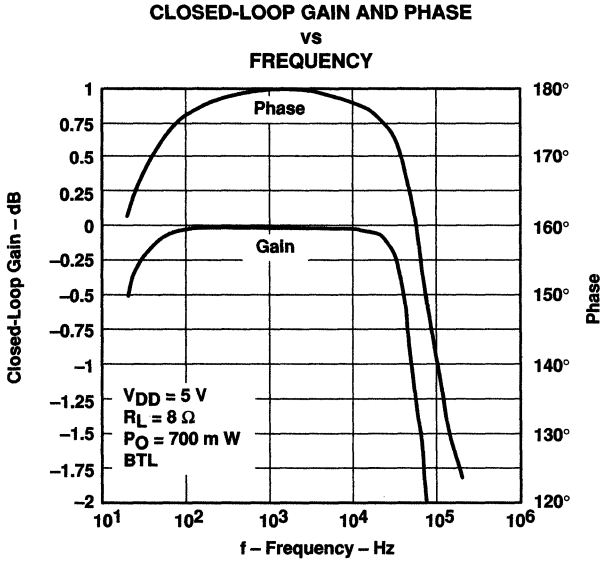


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

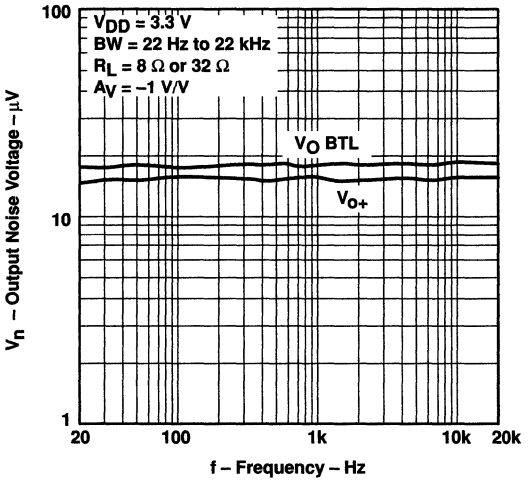


Figure 19

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

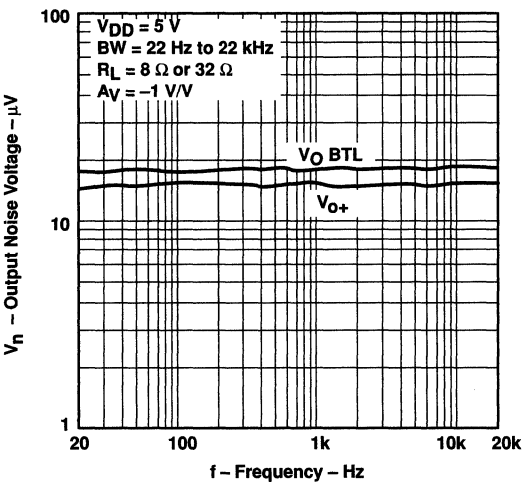


Figure 20

POWER DISSIPATION
vs
OUTPUT POWER

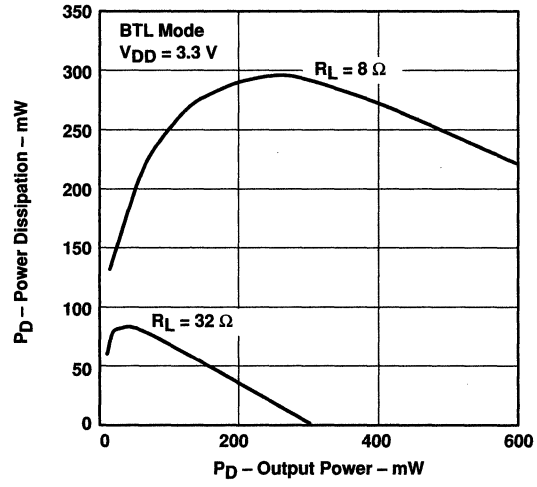


Figure 21

POWER DISSIPATION
vs
OUTPUT POWER

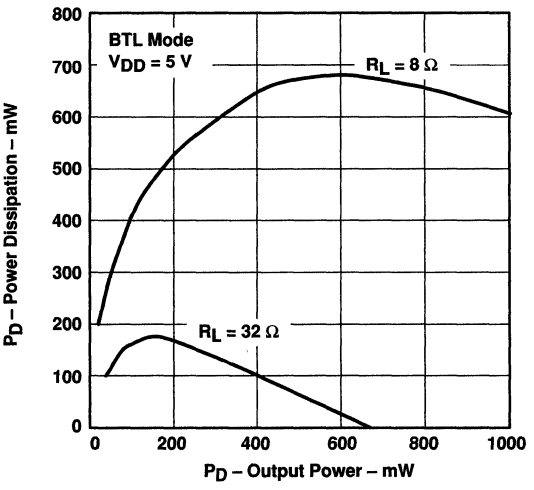


Figure 22

APPLICATION INFORMATION

bridged-tied load

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA701 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

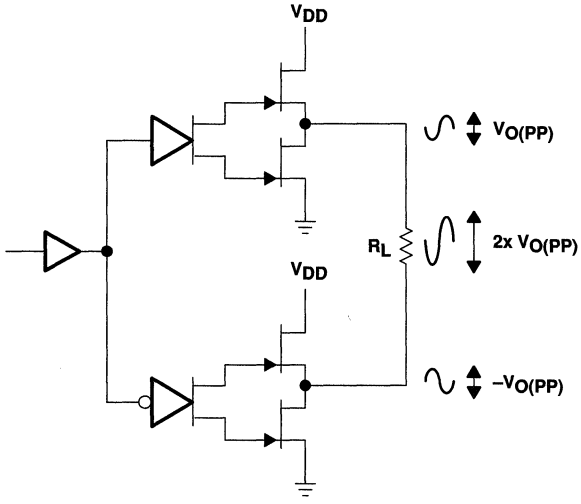


Figure 23. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (2)$$

APPLICATION INFORMATION

bridged-tied load (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

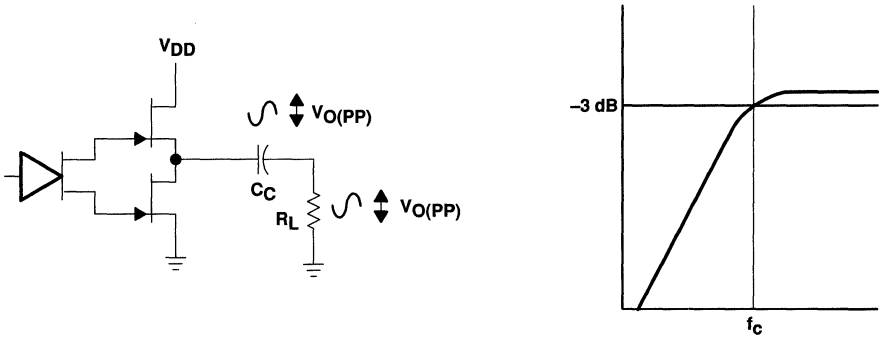


Figure 24. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

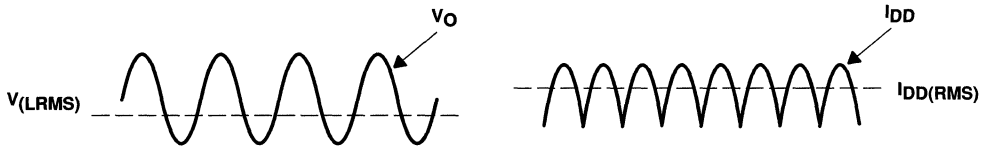


Figure 25. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency Vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-to-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

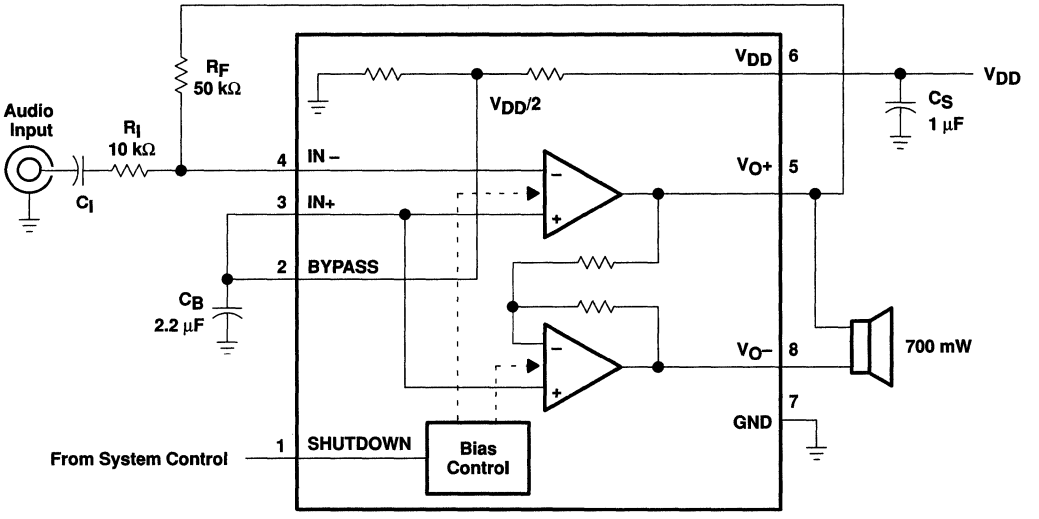


Figure 26. TPA701 Application Circuit

The following sections discuss the selection of the components used in Figure 26.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA701 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA701 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

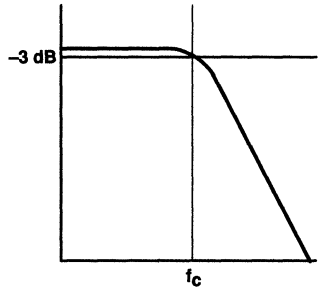
$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

APPLICATION INFORMATION

component selection (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

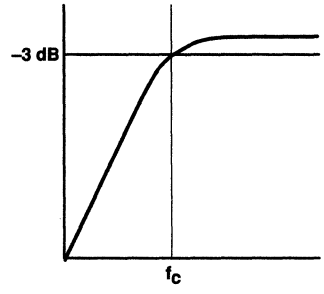


$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.



$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA701 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained. This insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \qquad (10)$$

As an example, consider a circuit where C_B is 2.2 µF, C_I is 0.47 µF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 2.2 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA701 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA701 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power of operation from 5-V supplies for a given output-power level.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA701 data sheet, one can see that when the TPA701 is operating from a 5-V supply into a 8-Ω speaker that 700 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{700\ mW}{1W} = -1.5\ dB$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

–1.5 dB – 15 dB = –16.5 (15 dB headroom)
–1.5 dB – 12 dB = –13.5 (12 dB headroom)
–1.5 dB – 9 dB = –10.5 (9 dB headroom)
–1.5 dB – 6 dB = –7.5 (6 dB headroom)
–1.5 dB – 3 dB = –4.5 (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
= 22 mW (15 dB headroom)
= 44 mW (12 dB headroom)
= 88 mW (9 dB headroom)
= 175 mW (6 dB headroom)
= 350 mW (3 dB headroom)

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 700 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA701 and maximum ambient temperatures is shown in Table 2.

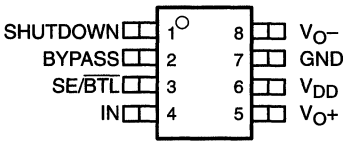
Table 2. TPA701 Power Rating, 5-V, 8-Ω, BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	D PACKAGE (SOIC)	DGN PACKAGE (MSOP)
			MAXIMUM AMBIENT TEMPERATURE	MAXIMUM AMBIENT TEMPERATURE
700	700 mW	675	34°C	110°C
700	350 mW (3 dB)	595	47°C	115°C
700	176 mW (6 dB)	475	68°C	122°C
700	88 mW (9 dB)	350	89°C	125°C
700	44 mW (12 dB)	225	111°C	125°C

Table 2 shows that the TPA701 can be used to its full 700-mW rating without any heat sinking in still air up to 110°C and 34°C for the DGN package (MSOP) and D pacakge (SOIC) respectively.

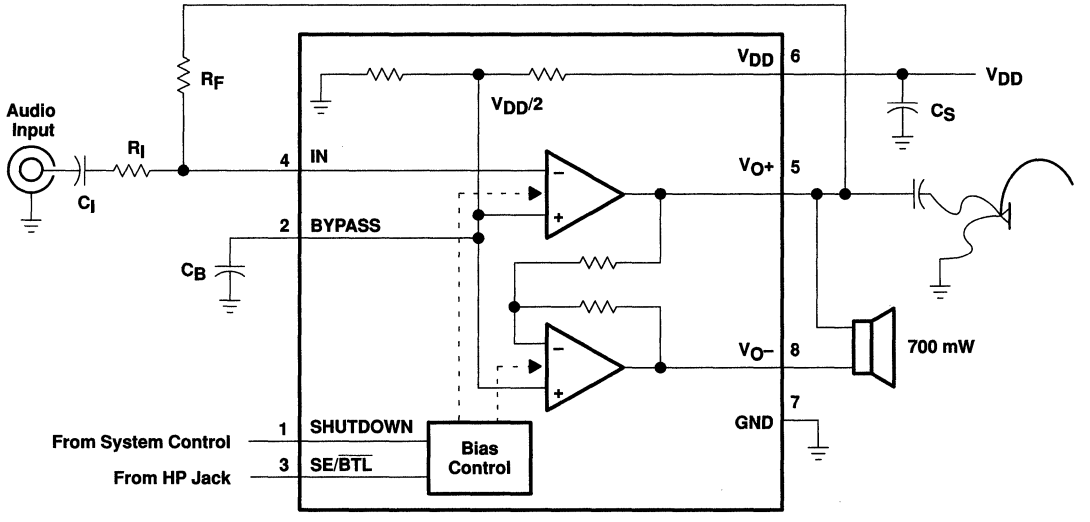
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility**
  2.5 V – 5.5 V
- **Output Power**
  - **700 mW at V_{DD} = 5 V, BTL, R_L = 8 Ω**
  - **85 mW at V_{DD} = 5 V, SE, R_L = 32 Ω**
  - **250 mW at V_{DD} = 3.3 V, BTL, R_L = 8 Ω**
  - **37 mW at V_{DD} = 3.3 V, SE, R_L = 32 Ω**
- **Shutdown Control**
  - **I_{DD} = 7 μA at 3.3 V**
  - **I_{DD} = 50 μA at 5 V**
- **BTL to SE Mode Control**
- **Integrated Depop Circuitry**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA711 is a bridge-tied load (BTL) or single-ended (SE) audio power amplifier developed especially for low-voltage applicationswhere internal speakers and external earphone operation are required. Operating with a 3.3-V supply, the TPA711 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 0.6% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. A unique feature of the TPA711 is that it allows the amplifier to switch from BTL to SE *on the fly* when an earphone drive is required. This eliminates complicated mechanical switching or auxiliary devices just to drive the external load. This device features a shutdown mode for power-sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The TPA711 is available in an 8-pin SOIC and the surface-mount PowerPAD MSOP package, which reduces board space by 50% and height by 40%.



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP SYMBOLIZATION
	SMALL OUTLINE† (D)	MSOP‡ (DGN)	
–40°C to 85°C	TPA711D	TPA711DGN	ABB

† In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

‡ The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA311DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 2.2-µF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN	4	I	IN is the audio input terminal.
SE/$\overline{\text{BTL}}$	3	I	When SE/$\overline{\text{BTL}}$ is held low, the TPA711 is in BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the TPA711 is in SE mode.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} = 7 µA).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_{O+}	5	O	V_{O+} is the positive output for BTL and SE modes.
V_{O-}	8	O	V_{O-} is the negative output in BTL mode and a high-impedance output in SE mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A (see Table 3)	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)	See Note 1				20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V	BTL mode		85		dB
			SE mode		83		
I_{DD}	Supply current (see Figure 6)	BTL mode			1.25	2.5	mA
		SE mode			0.65	1.25	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)				7	50	μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately V_{DD}/2.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.2%,	BTL mode,	See Figure 14		250		mW
		THD = 0.1%, See Figure 22	SE mode,	R_L = 32 Ω,		37		
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 200 Hz to 4 kHz,	See Figure 12		0.55%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 12		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 36			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 μF,	BTL mode,		79		dB
		f = 1 kHz, See Figure 3	C_B = 1 μF,	SE mode,		70		
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 μF,	See Figure 42		17		μV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)					20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V	BTL mode		78		dB
			SE mode		76		
I_{DD}	Supply current (see Figure 6)	BTL mode			1.25	2.5	mA
		SE mode			0.65	1.25	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)				50	100	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.3%,	BTL mode,	See Figure 18		700†		mW
		THD = 0.1%, See Figure 26	SE mode,	R_L = 32 Ω,		85		
THD + N	Total harmonic distortion plus noise	P_O = 700 mW,	f = 200 Hz to 4 kHz,	See Figure 16		0.5%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 16		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 37			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 µF,	BTL mode,		80		dB
		f = 1 kHz, See Figure 4	C_B = 1 µF,	SE mode,		73		
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 µF,	See Figure 43		17		µV(rms)

† The DGN package, properly mounted, can conduct 700 mW RMS power continuously. The D package, can only conduct 350 mW RMS power continuously, with peaks to 700 mW.

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

PARAMETER MEASUREMENT INFORMATION

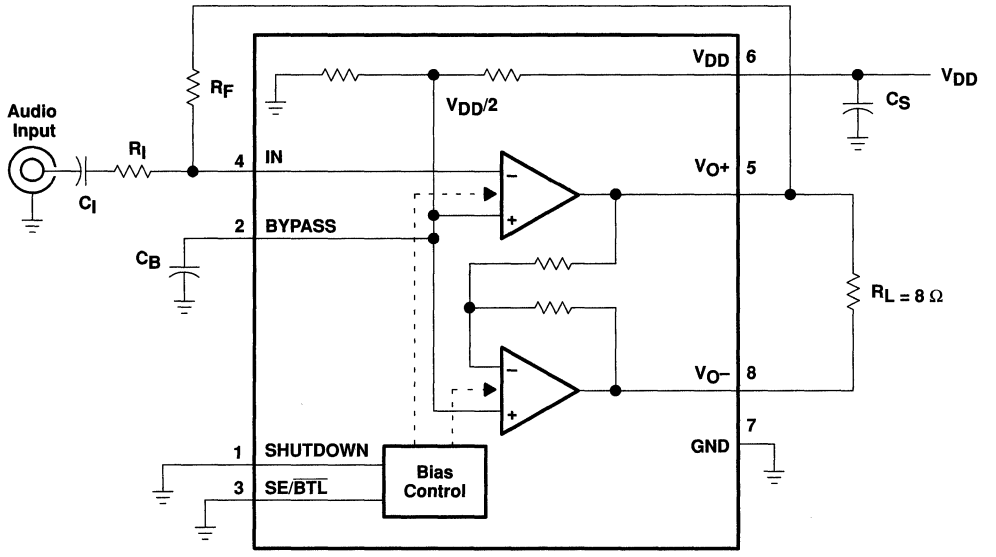


Figure 1. BTL Mode Test Circuit

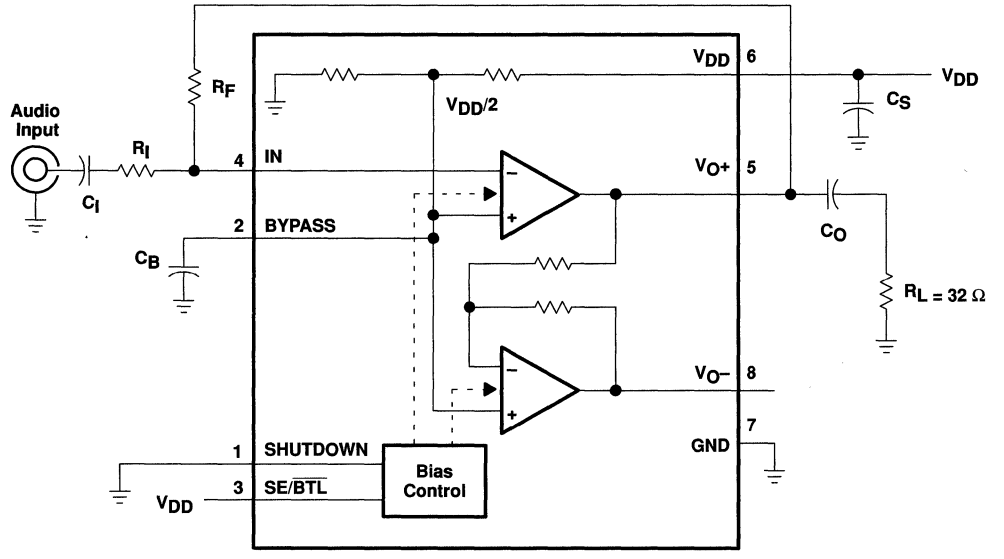


Figure 2. SE Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply ripple rejection ratio	vs Frequency	3, 4, 5
I_{DD}	Supply current	vs Supply voltage	6, 7
P_O	Output power	vs Supply voltage	8, 9
		vs Load resistance	10, 11
THD+N	Total harmonic distortion plus noise	vs Frequency	12, 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33
		vs Output power	14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35
	Open loop gain and phase	vs Frequency	36, 37
	Closed loop gain and phase	vs Frequency	38, 39, 40, 41
V_n	Output noise voltage	vs Frequency	42, 43
P_D	Power dissipation	vs Output power	44, 45, 46, 47

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

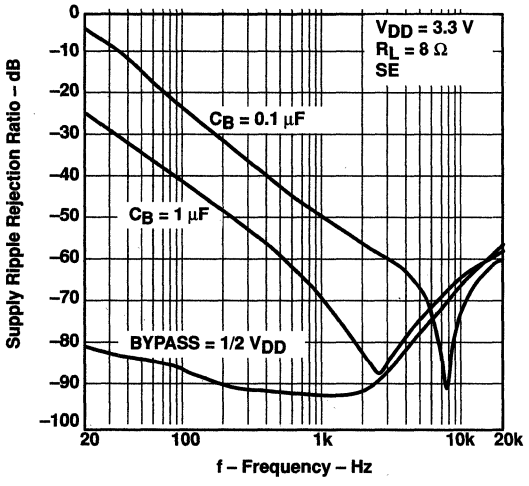


Figure 3

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

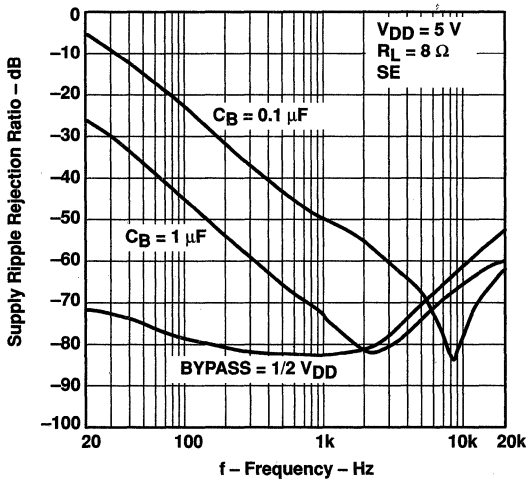


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

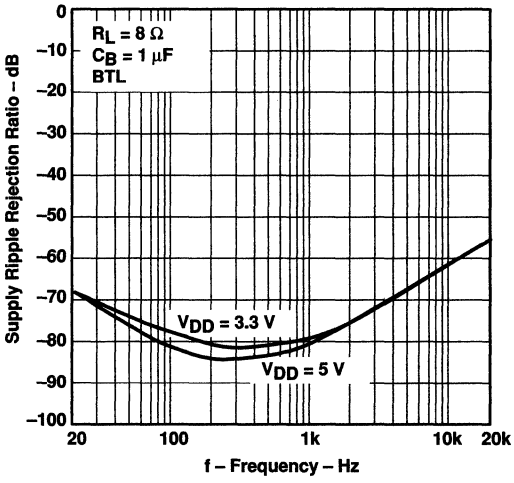


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

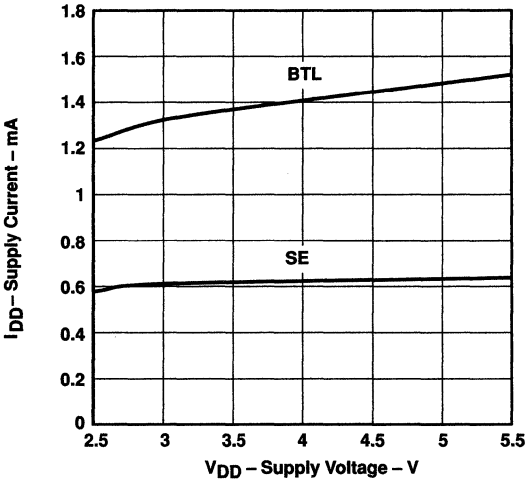


Figure 6

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

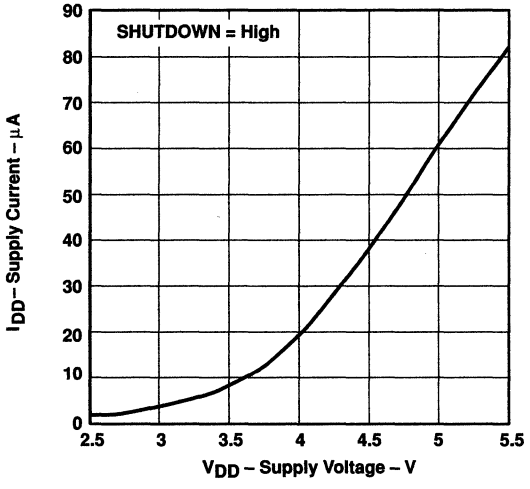


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

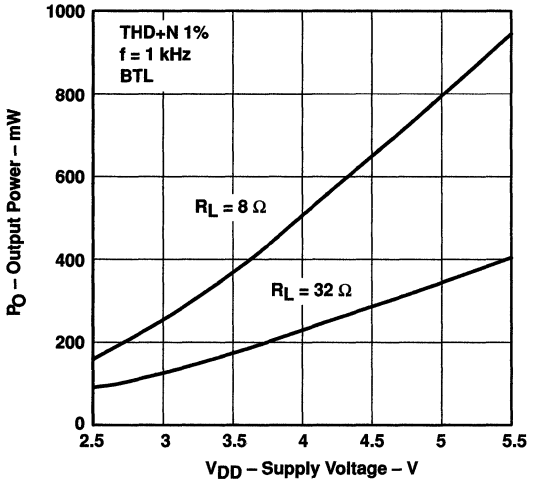


Figure 8

OUTPUT POWER
vs
SUPPLY VOLTAGE

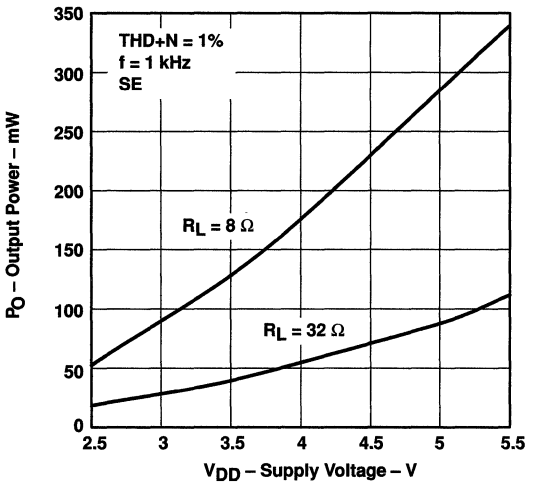


Figure 9

OUTPUT POWER
vs
LOAD RESISTANCE

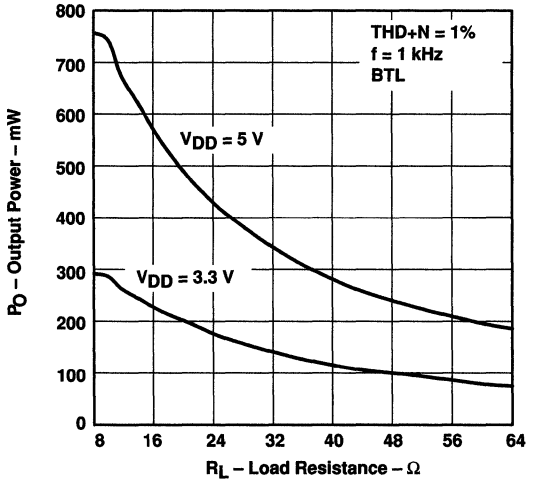


Figure 10

OUTPUT POWER
vs
LOAD RESISTANCE

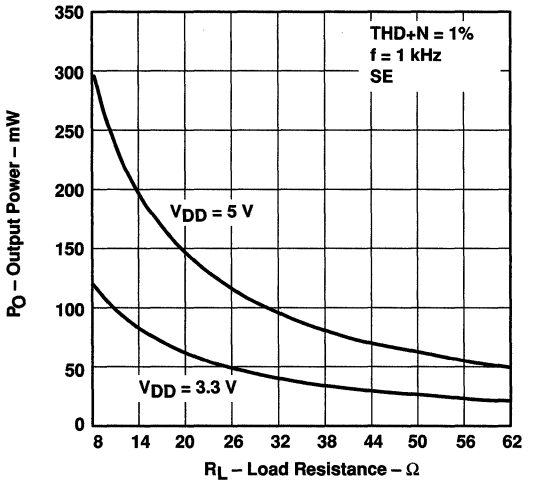


Figure 11

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

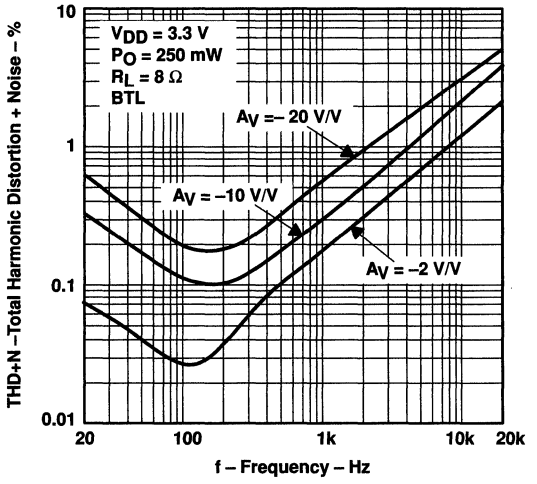


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

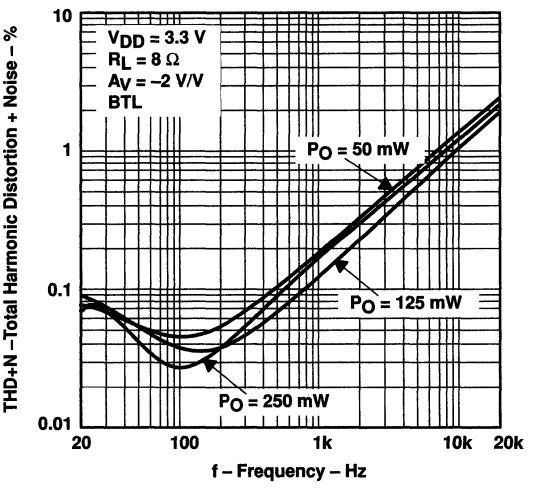


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

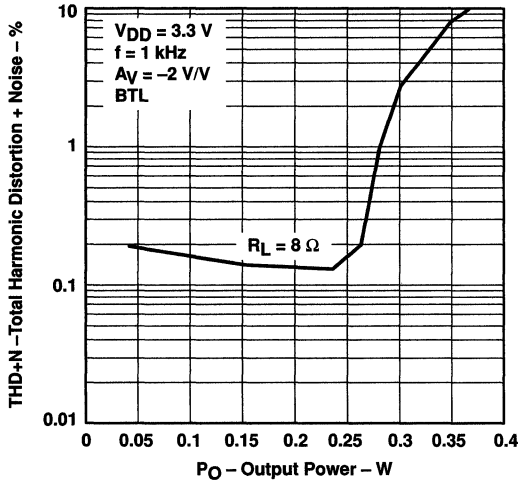


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

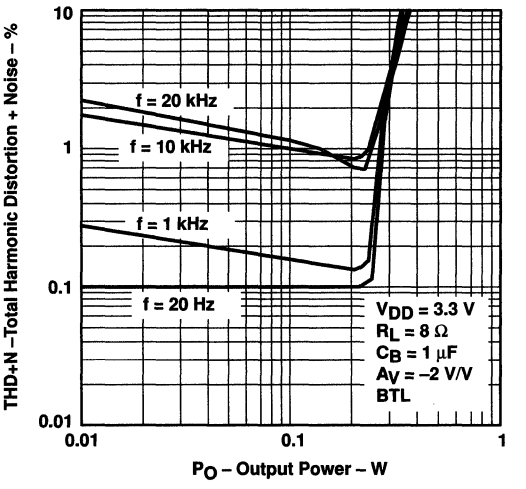


Figure 15

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

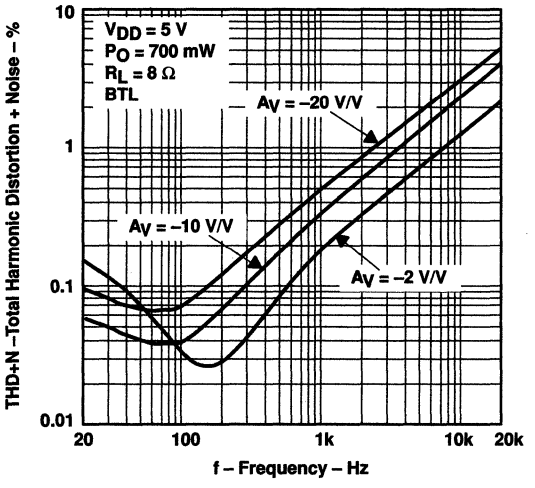


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

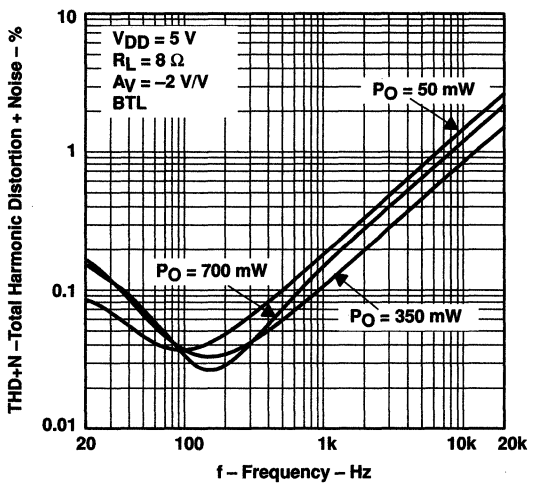


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

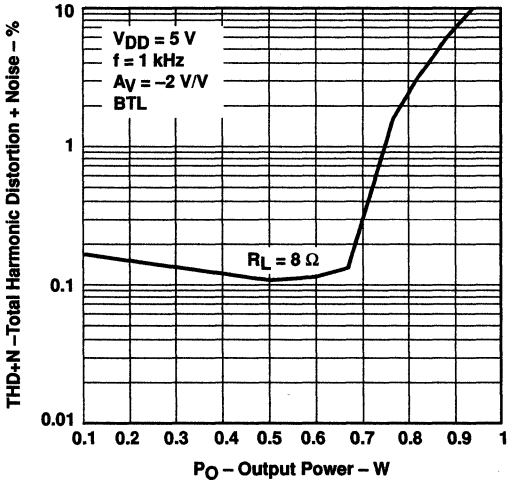


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

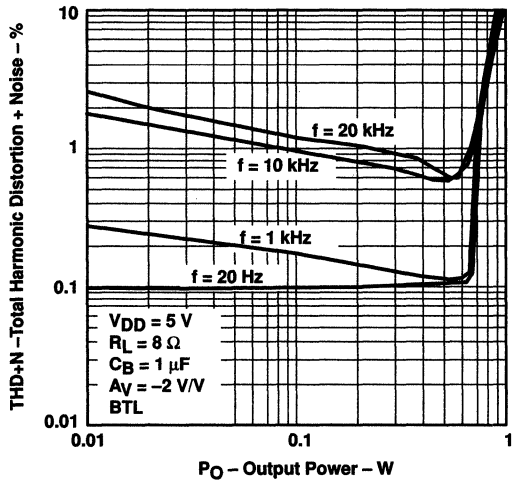


Figure 19

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

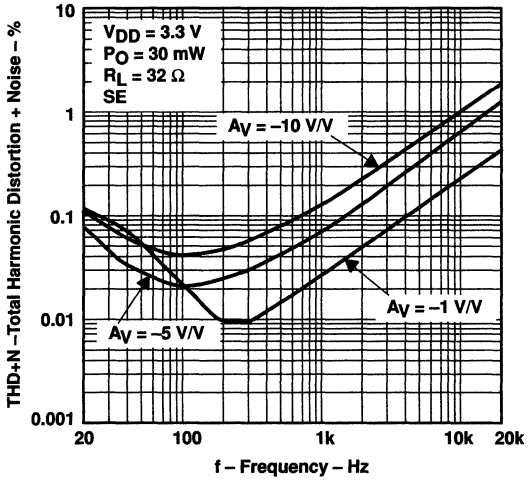


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

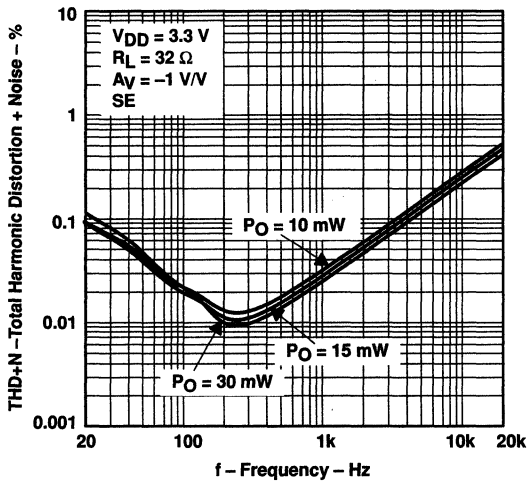


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

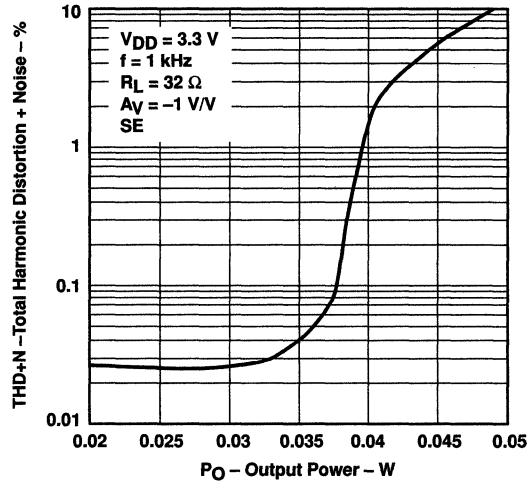


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

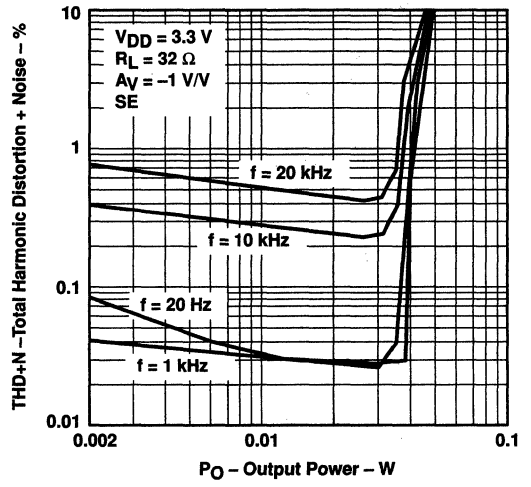


Figure 23

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

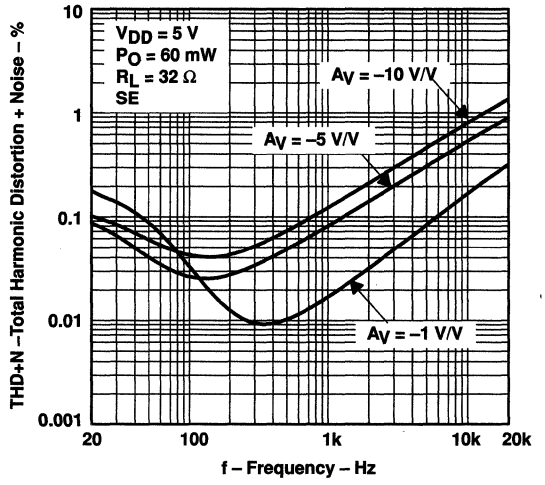


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

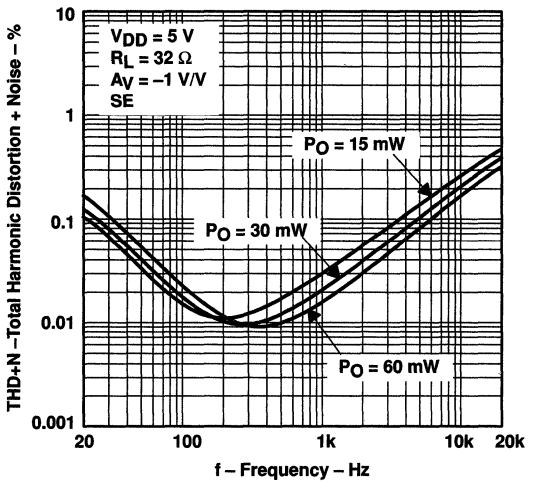


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

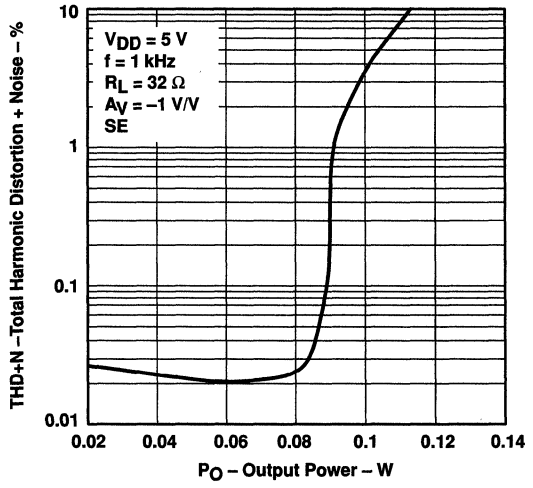


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

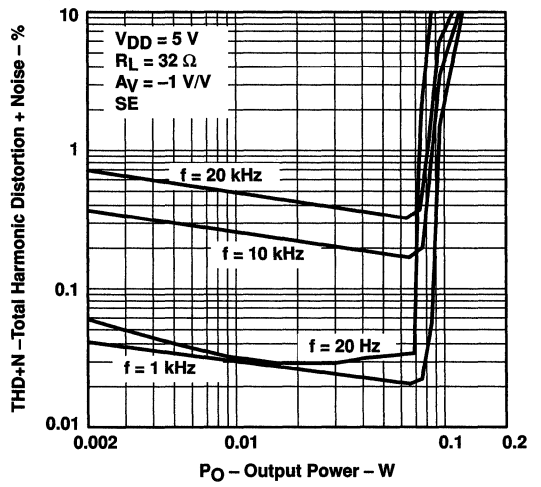


Figure 27

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

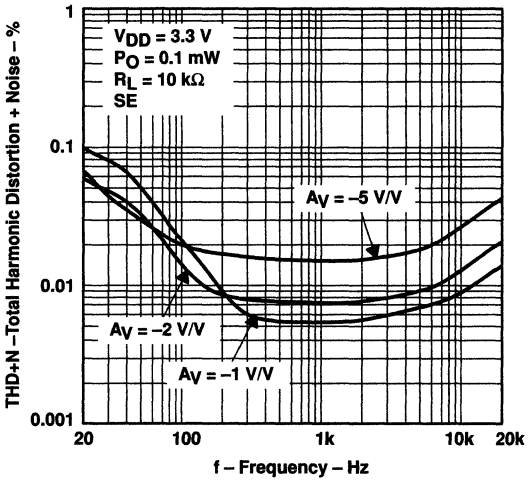


Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

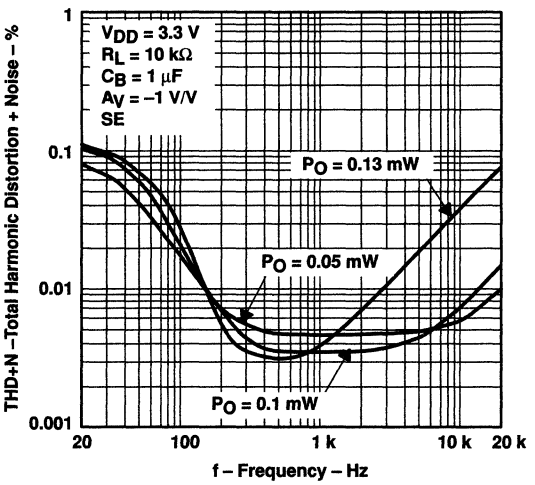


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

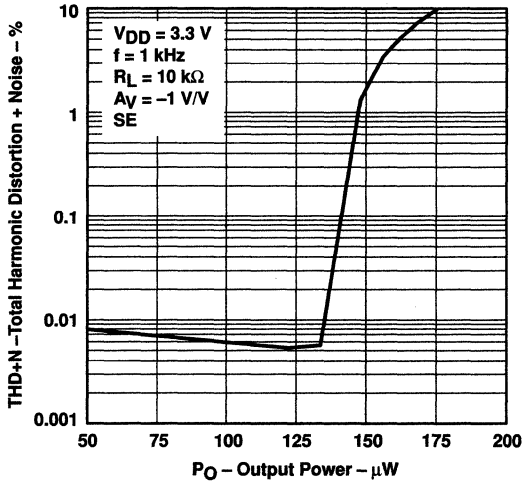


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

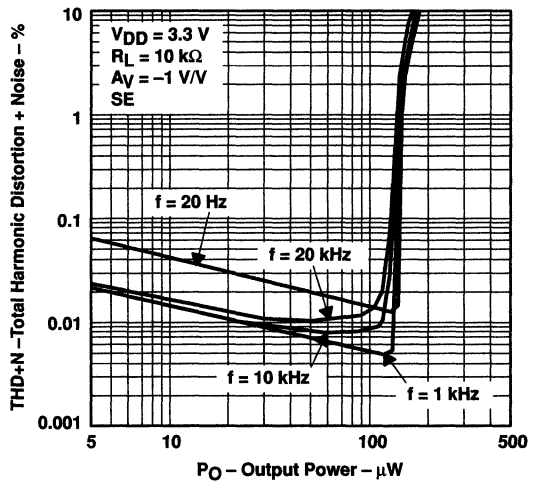


Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

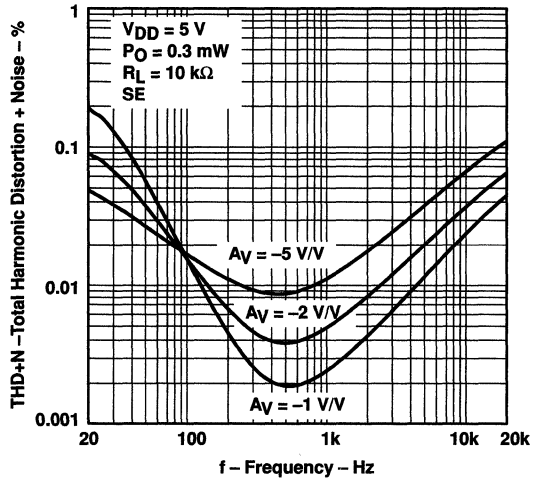


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

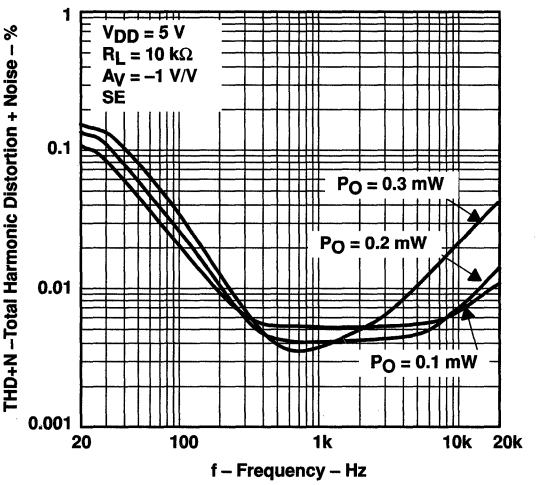


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

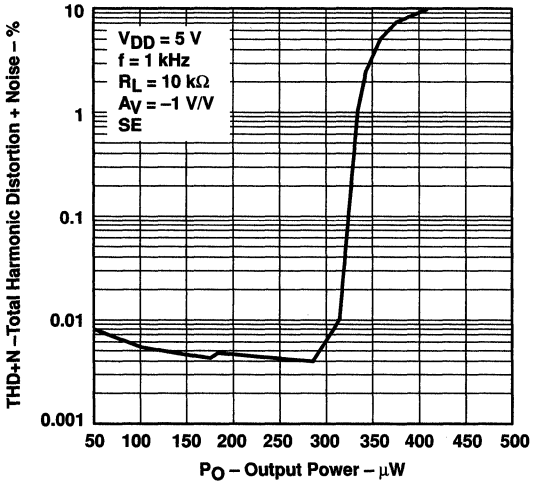


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

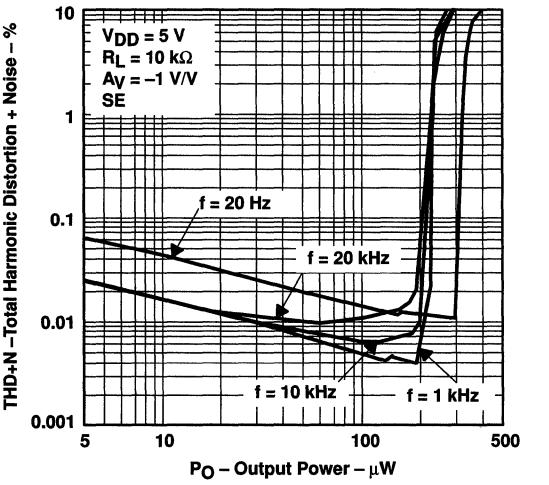


Figure 35

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

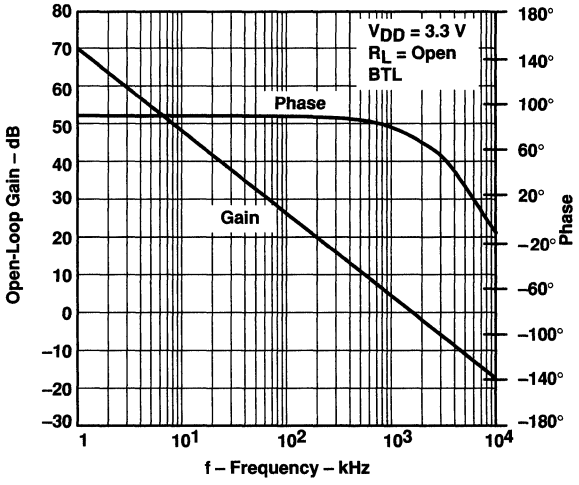


Figure 36

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

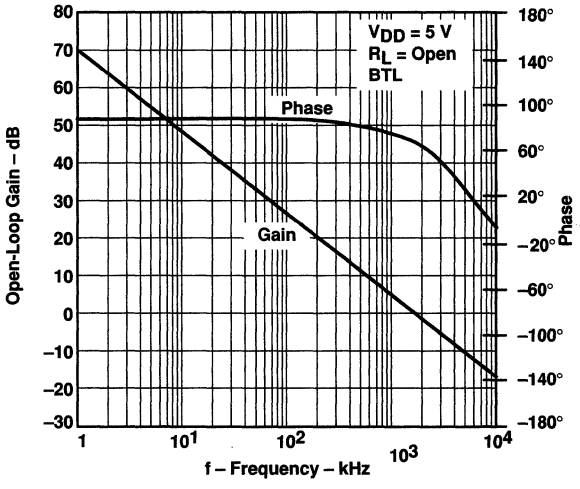


Figure 37

TYPICAL CHARACTERISTICS

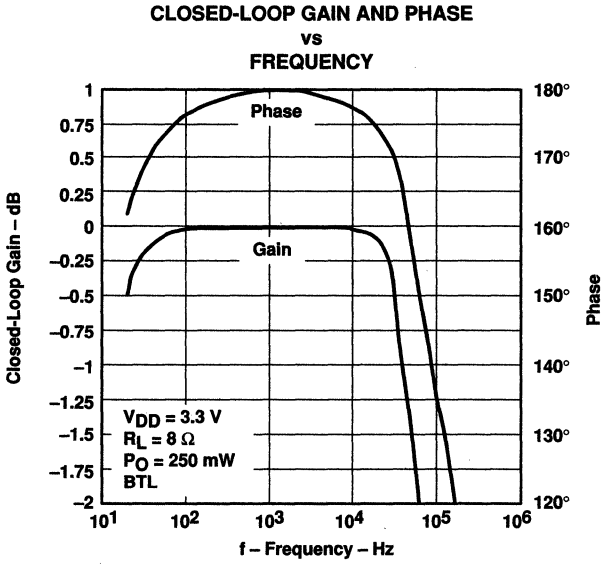


Figure 38

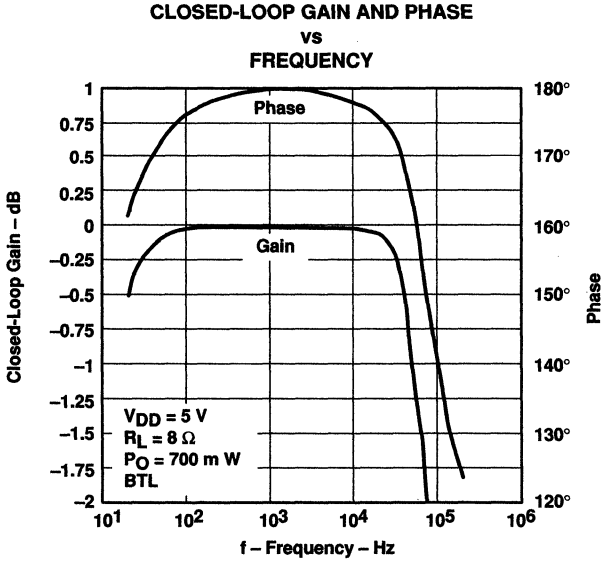


Figure 39

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

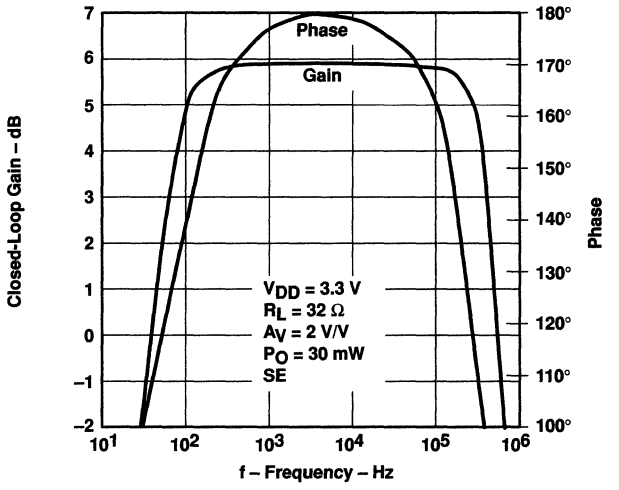


Figure 40

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

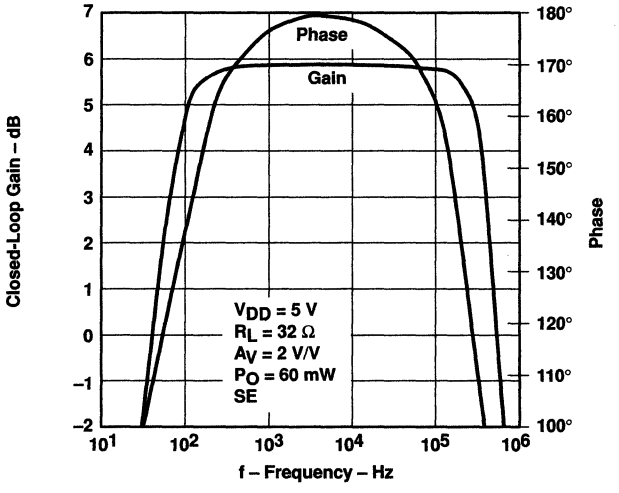


Figure 41

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

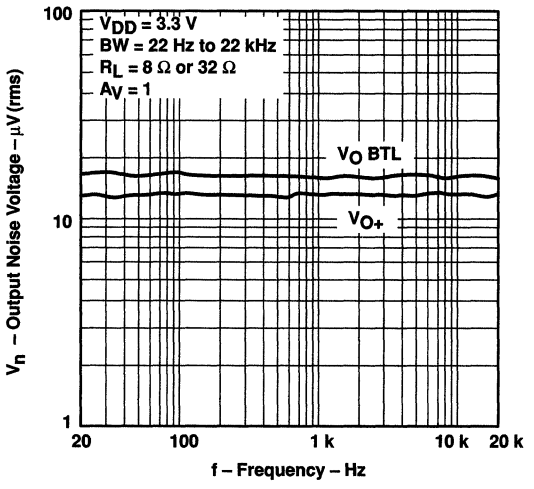


Figure 42

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

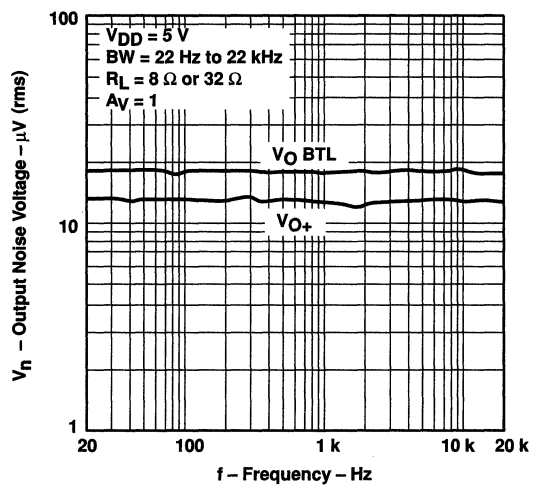


Figure 43

POWER DISSIPATION
vs
OUTPUT POWER

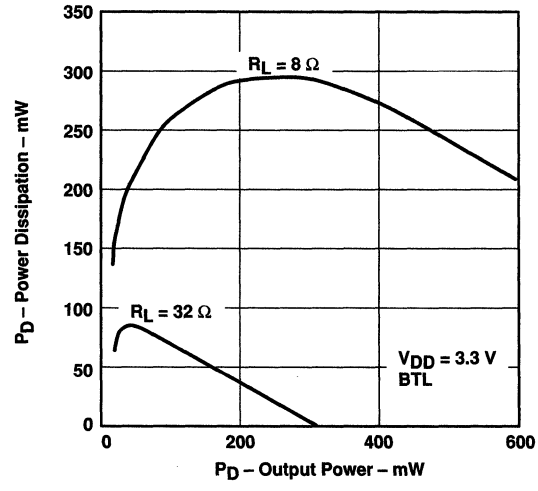


Figure 44

POWER DISSIPATION
vs
OUTPUT POWER

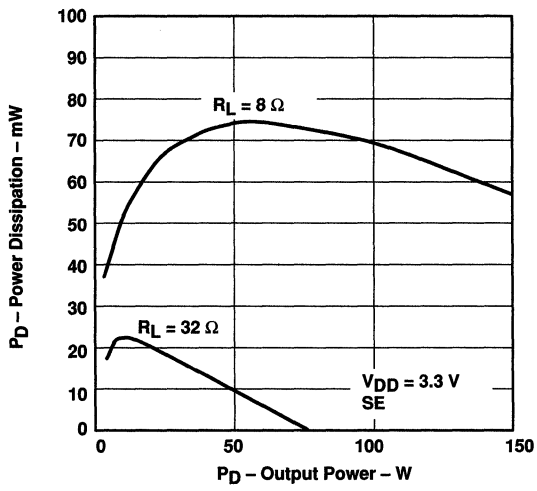


Figure 45

TYPICAL CHARACTERISTICS

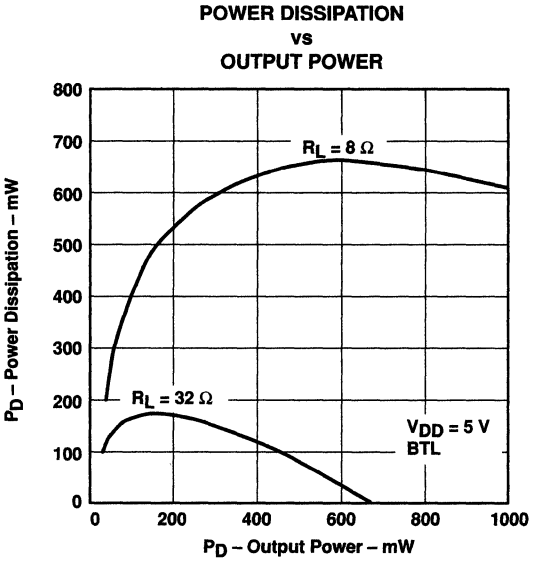


Figure 46

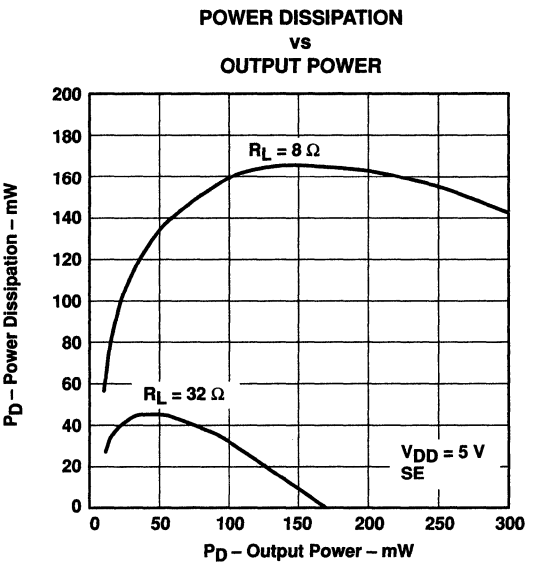


Figure 47

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 48 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA711 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (1)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

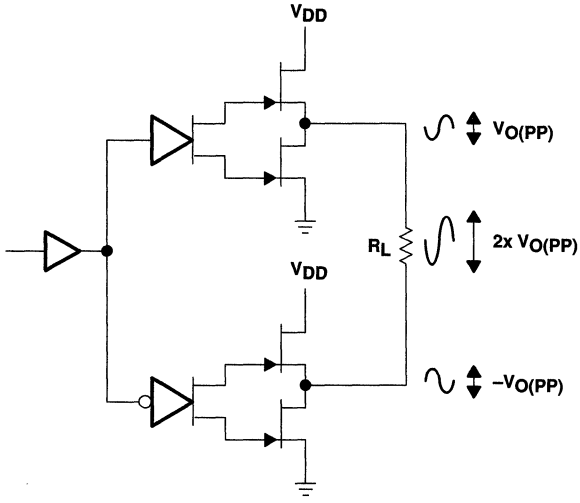


Figure 48. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 49. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (2)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

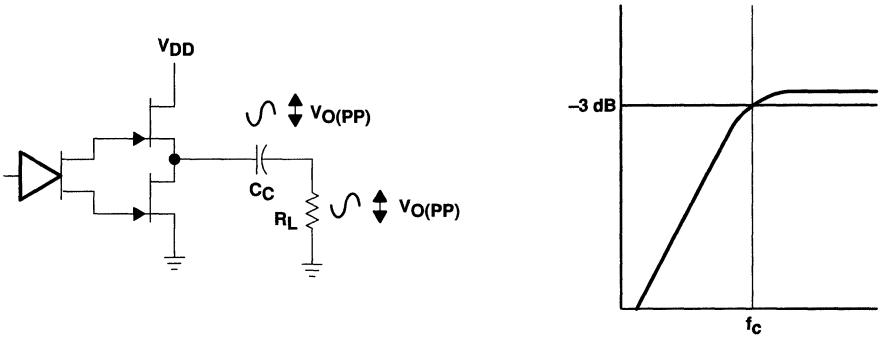


Figure 49. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 50).

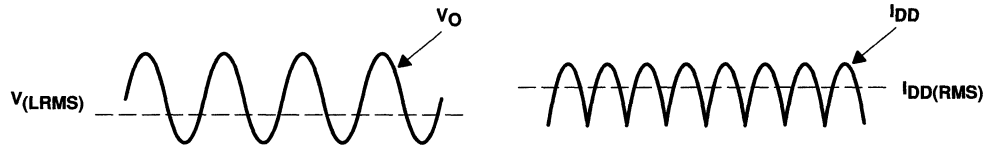


Figure 50. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency Vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-to-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 51 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of −10 V/V.

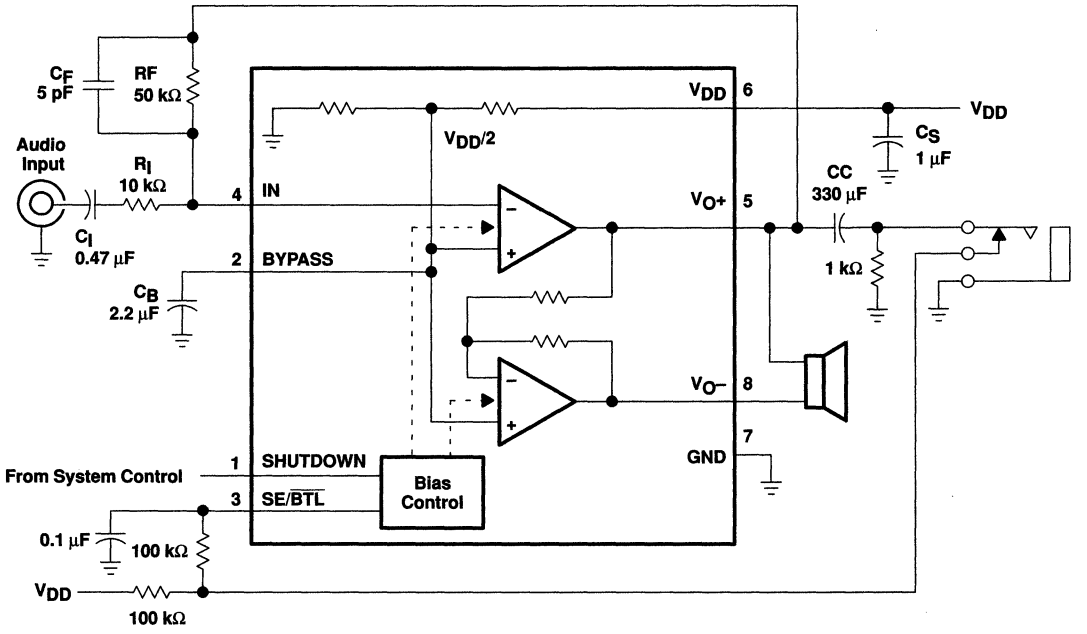


Figure 51. TPA711 Application Circuit

The following sections discuss the selection of the components used in Figure 51.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA711 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA711 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

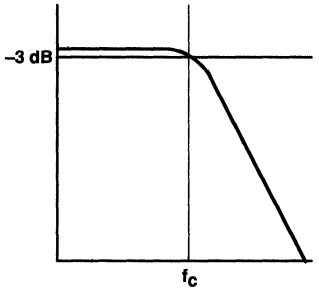
$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

APPLICATION INFORMATION

component selection (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

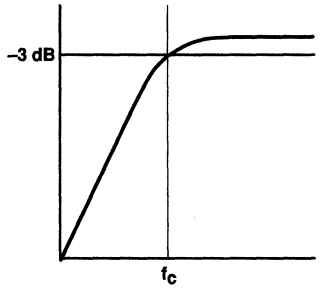


$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then f_c is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.



$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA711 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained. This insures the input capacitor is fully charged before the bypass capacitor is fuly charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \tag{10}$$

As an example, consider a circuit where C_B is 2.2 µF, C_I is 0.47 µF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 2.2 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

In SE mode (see Figure 51), the load is driven from the primary amplifier output (V_O+, terminal 5).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

APPLICATION INFORMATION

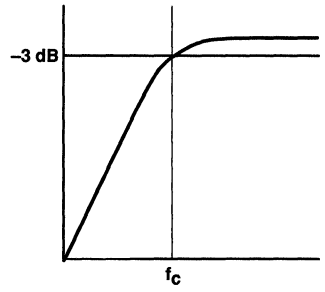
component selection (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \ll \frac{1}{R_L C_C} \qquad (12)$$

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.



$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \qquad (13)$$

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, an 8-Ω load is adequate, earphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA711 to easily switch between BTL and SE modes is one of its most important cost-saving features. This feature eliminates the requirement for an additional earphone amplifier in applications where internal speakers are driven in BTL mode but external earphone or speaker must be accommodated. Internal to the TPA711, two separate amplifiers drive V_O+ and V_O–. The SE/$\overline{\text{BTL}}$ input (terminal 3) controls the operation of the follower amplifier that drives V_O– (terminal 8). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA711 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the V_O– amplifier is in a high output impedance state, which configures the TPA711 as an SE driver from V_O+ (terminal 5). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level TTL source or, more typically, from a resistor divider network as shown in Figure 52.

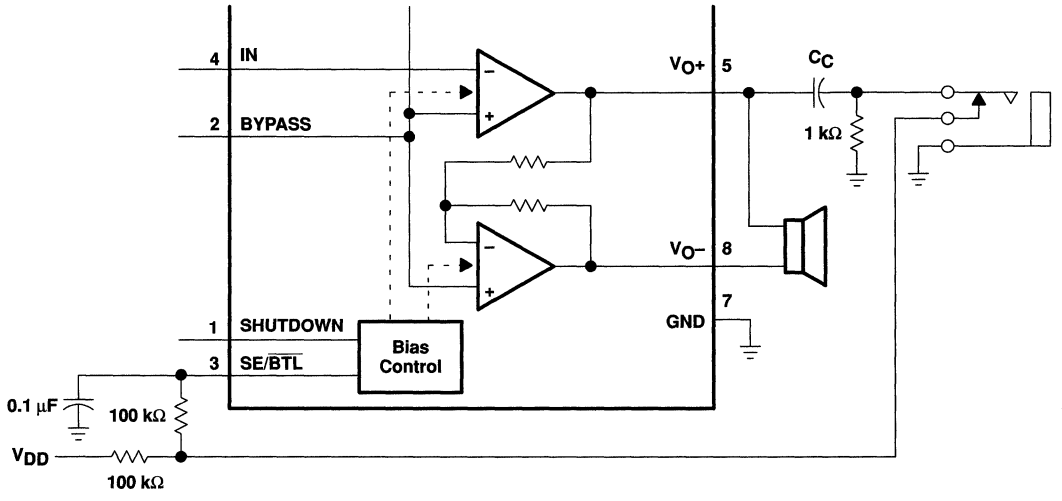


Figure 52. TPA711 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) mono earphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the V_O– amplifier is shut down causing the BTL speaker to mute (virtually open-circuits the speaker). The V_O+ amplifier then drives through the output capacitor (C_C) into the earphone jack.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA711 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA711 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power of operation from 5-V supplies for a given output-power level.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA711 data sheet, one can see that when the TPA711 is operating from a 5-V supply into a 8-Ω speaker that 700 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{700\ \text{mW}}{1\text{W}}\right) = -1.5\ \text{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

–1.5 dB – 15 dB = –16.5 (15 dB headroom)
–1.5 dB – 12 dB = –13.5 (12 dB headroom)
–1.5 dB – 9 dB = –10.5 (9 dB headroom)
–1.5 dB – 6 dB = –7.5 (6 dB headroom)
–1.5 dB – 3 dB = –4.5 (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
= 22 mW (15 dB headroom)
= 44 mW (12 dB headroom)
= 88 mW (9 dB headroom)
= 175 mW (6 dB headroom)
= 350 mW (3 dB headroom)

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 700 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA711 and maximum ambient temperatures is shown in Table 3.

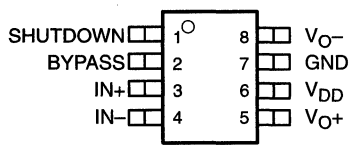
Table 3. TPA711 Power Rating, 5-V, 8-Ω, BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	D PACKAGE (SOIC)	DGN PACKAGE (MSOP)
			MAXIMUM AMBIENT TEMPERATURE	MAXIMUM AMBIENT TEMPERATURE
700	700 mW	675	34°C	110°C
700	350 mW (3 dB)	595	47°C	115°C
700	176 mW (6 dB)	475	68°C	122°C
700	88 mW (9 dB)	350	89°C	125°C
700	44 mW (12 dB)	225	111°C	125°C

Table 3 shows that the TPA711 can be used to its full 700-mW rating without any heat sinking in still air up to 110°C and 34°C for the DGN package (MSOP) and D pacakge (SOIC) respectively.

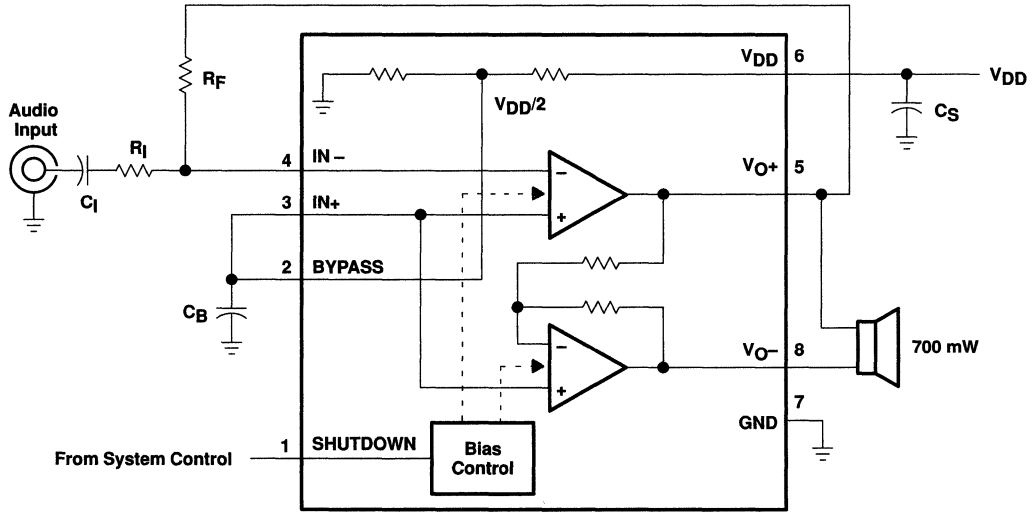
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility 2.5 V – 5.5 V**
- **Output Power for R_L = 8 Ω**
  - **700 mW at V_{DD} = 5 V, BTL**
  - **250 mW at V_{DD} = 3.3 V, BTL**
- **Integrated Depop Circuitry**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA721 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA721 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 0.6% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a supply current of 7 μA during shutdown. The TPA721 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP‡ (DGN)	
–40°C to 85°C	TPA721D	TPA721DGN	ABC

† In the D package, the maximum output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.

‡ The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA301DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-μF to 2.2-μF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN–	4	I	IN– is the inverting input. IN– is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} < 7 μA).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive BTL output.
V_O–	8	O	V_O– is the negative BTL output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)	See Note 1			20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		85		dB
I_{DD}	Supply current	BTL mode		1.25	2.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)			7	50	μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately V_{DD}/2.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%,	See Figure 9			250		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 200 Hz to 4 kHz,	See Figure 7		0.55%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 7		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 15			1.4		MHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	C_B = 1 μF,	See Figure 2		79		dB
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 μF,	See Figure 19		17		μV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage (measured differentially)				20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		78		dB
I_{DD}	Supply current			1.25	2.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)			50	100	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	See Figure 13			700†		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 200 Hz to 4 kHz,	See Figure 11		0.5%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%,	See Figure 11		20		kHz
B_1	Unity-gain bandwidth	Open Loop,	See Figure 16			1.4		MHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz,	C_B = 1 μF,	See Figure 2		80		dB
V_n	Noise output voltage	Gain = 1,	C_B = 0.1 μF,	See Figure 20		17		μV(rms)

† The DGN package, properly mounted, can conduct 700 mW RMS power continuously. The D package can only conduct 350 mW RMS power continuously wtih peaks to 700 mW.

PARAMETER MEASUREMENT INFORMATION

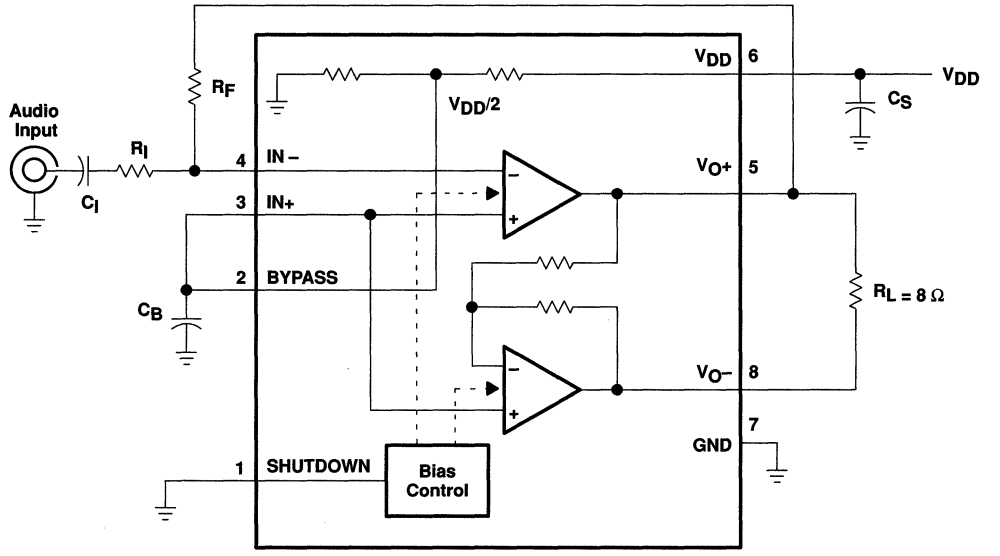


Figure 1. BTL Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
k_{SVR}	Supply ripple rejection ratio	vs Frequency	2
I_{DD}	Supply current	vs Supply voltage	3, 4
P_O	Output power	vs Supply voltage	5
		vs Load resistance	6
THD+N	Total harmonic distortion plus noise	vs Frequency	7, 8, 11, 12
		vs Output power	9, 10, 13, 14
	Open loop gain and phase	vs Frequency	15, 16
	Closed loop gain and phase	vs Frequency	17, 18
V_n	Output noise voltage	vs Frequency	19, 20
P_D	Power dissipation	vs Output power	21, 22

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

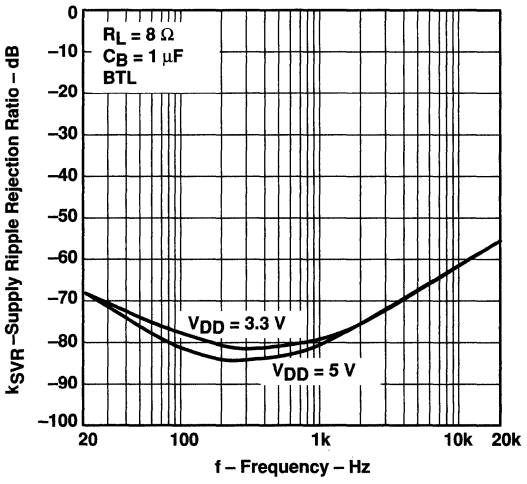


Figure 2

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

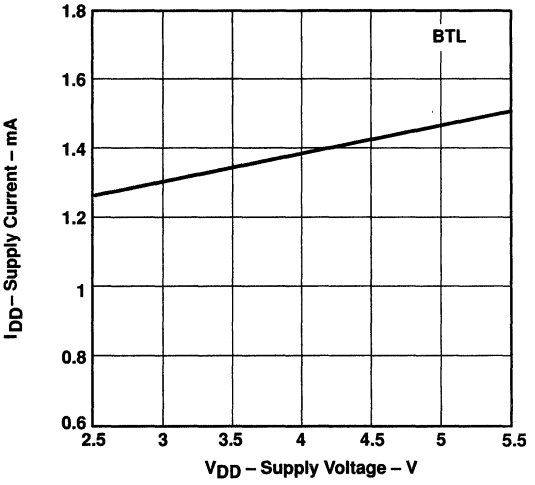


Figure 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

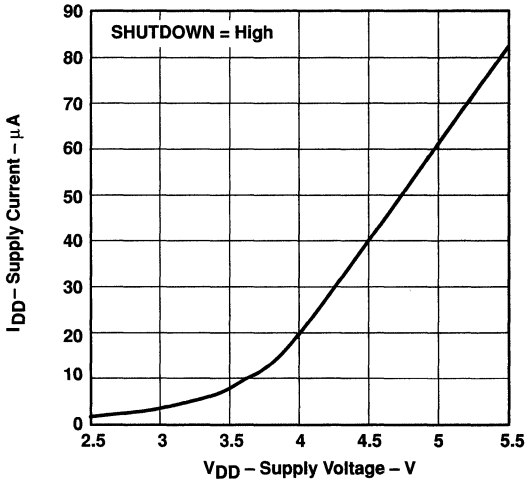


Figure 4

TYPICAL CHARACTERISTICS

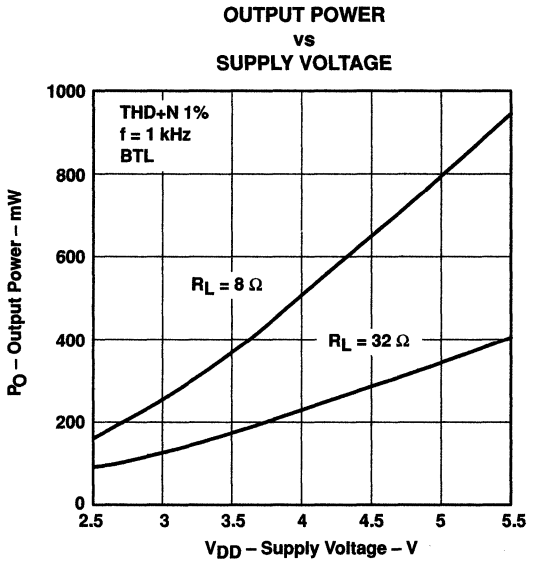


Figure 5

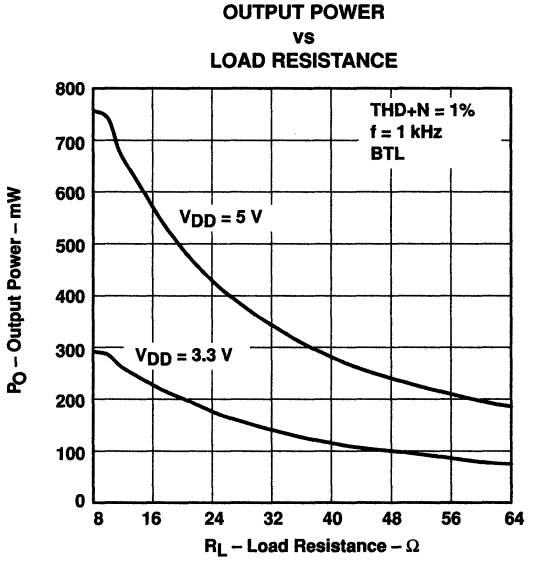


Figure 6

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

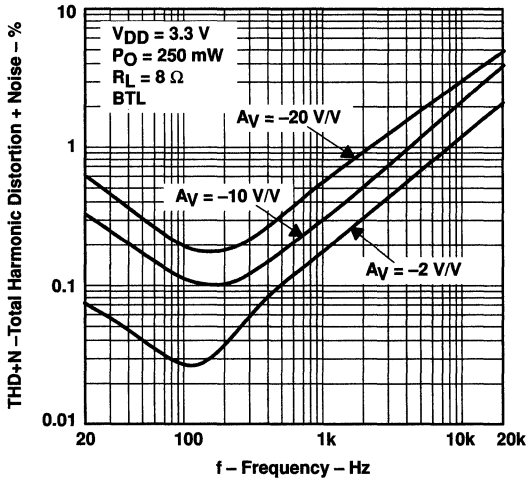


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

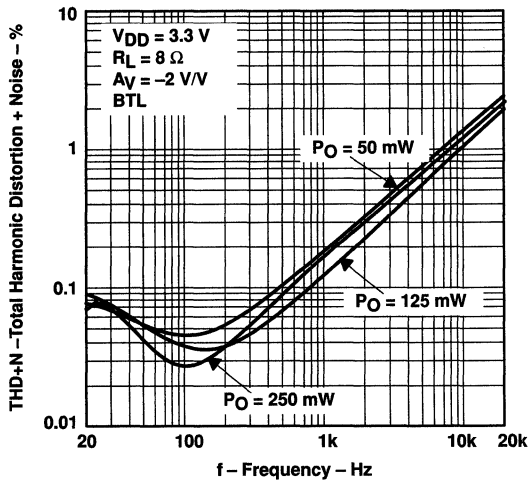


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

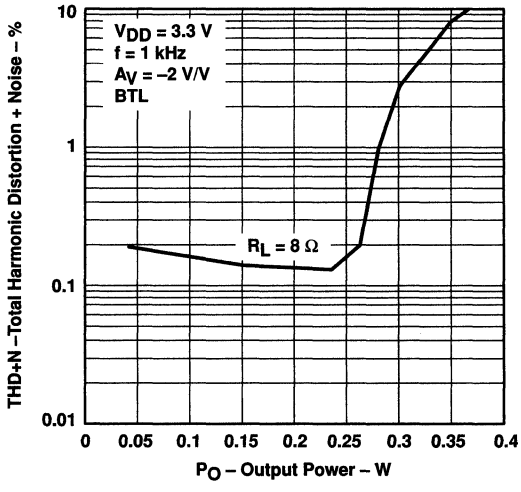


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

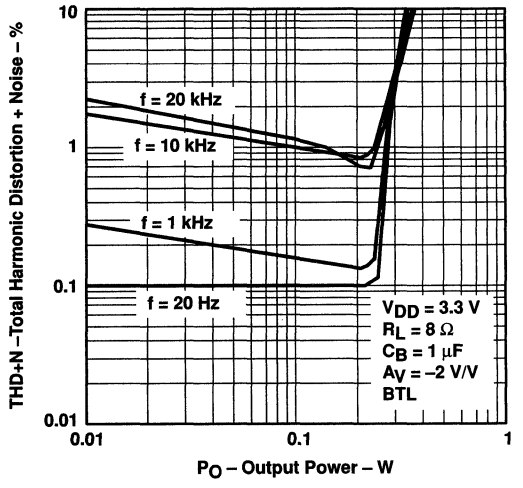


Figure 10

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

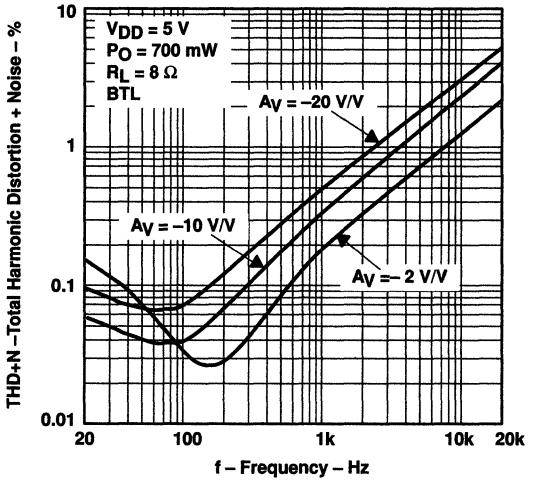


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

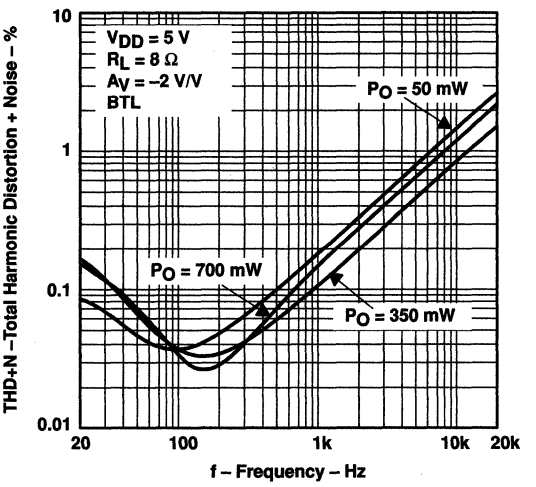


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

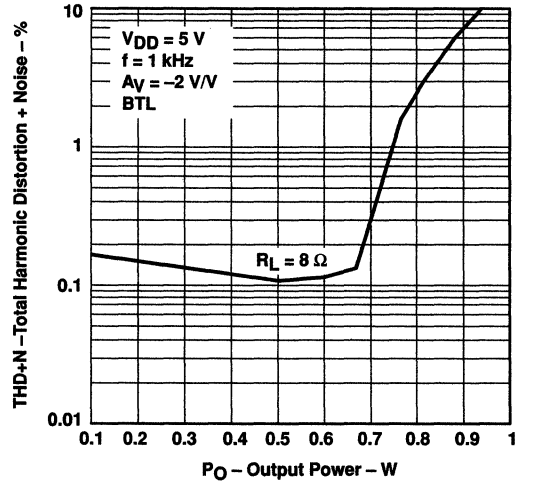


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

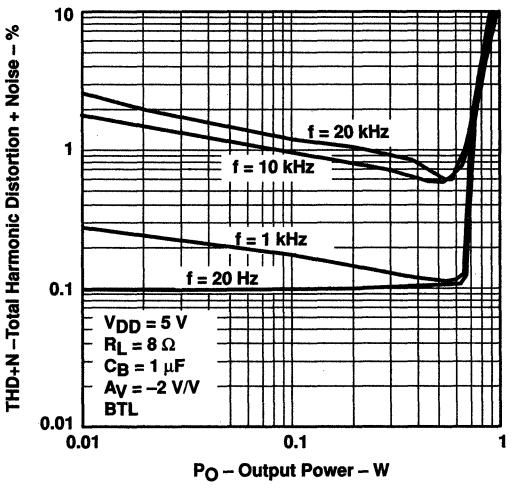


Figure 14

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

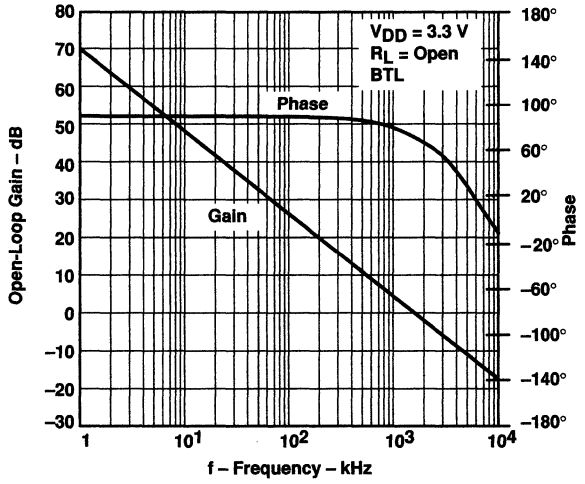


Figure 15

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

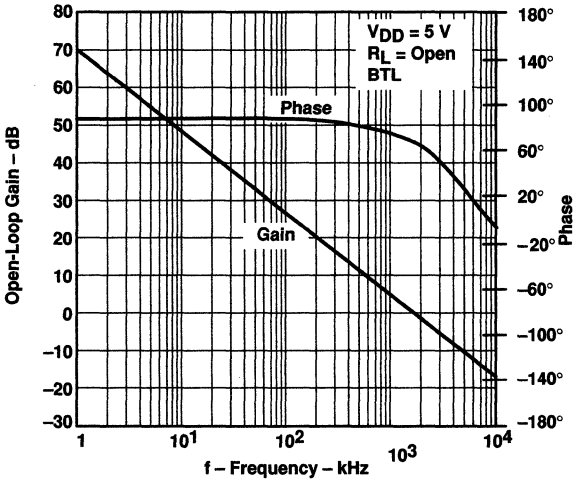


Figure 16

TYPICAL CHARACTERISTICS

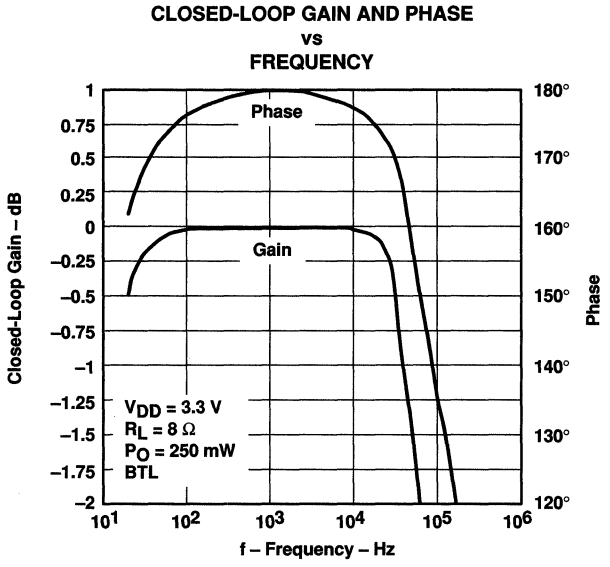


Figure 17

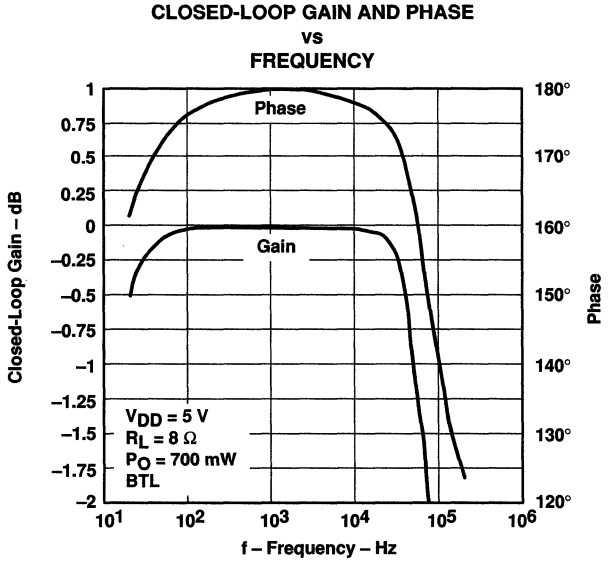


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

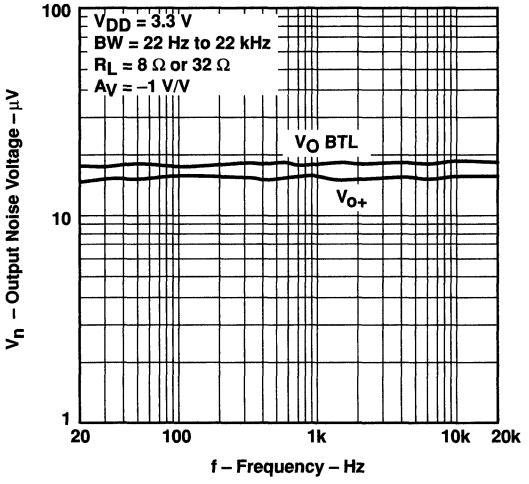


Figure 19

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

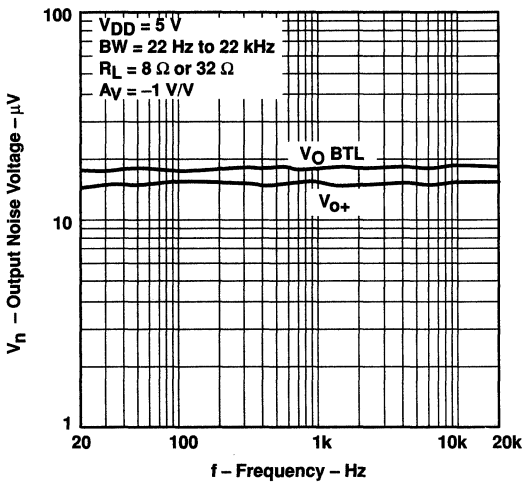


Figure 20

POWER DISSIPATION
vs
OUTPUT POWER

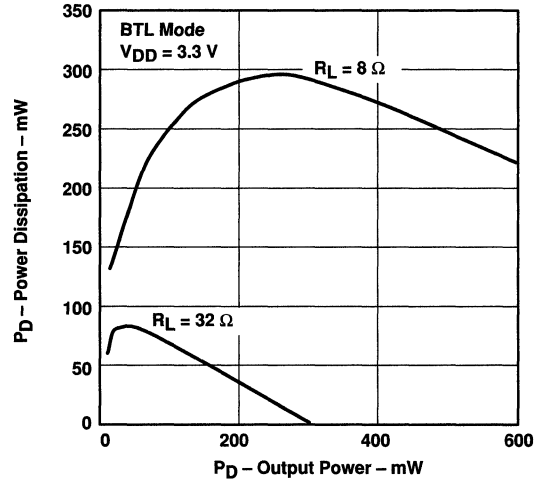


Figure 21

POWER DISSIPATION
vs
OUTPUT POWER

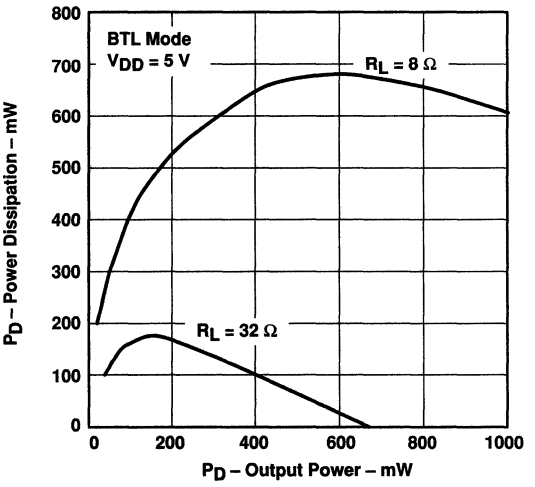


Figure 22

APPLICATION INFORMATION

bridged-tied load

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA721 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (1)$$

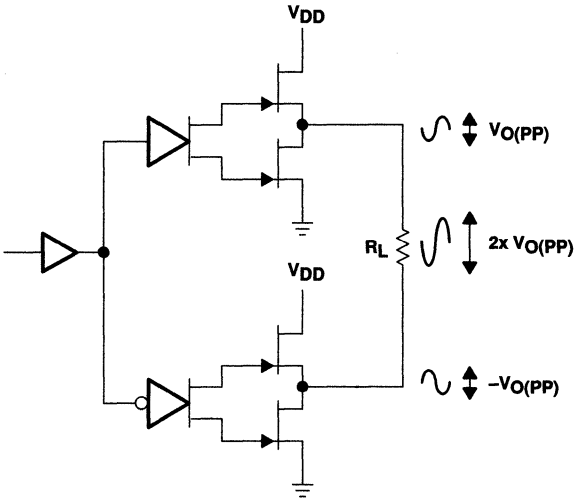


Figure 23. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \quad (2)$$

APPLICATION INFORMATION

bridged-tied load (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

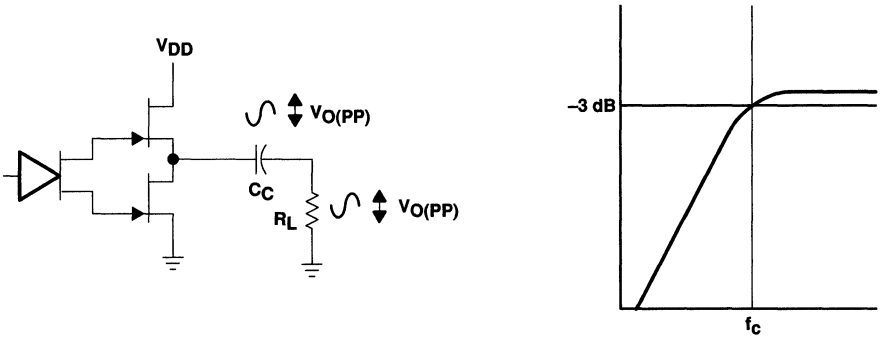


Figure 24. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

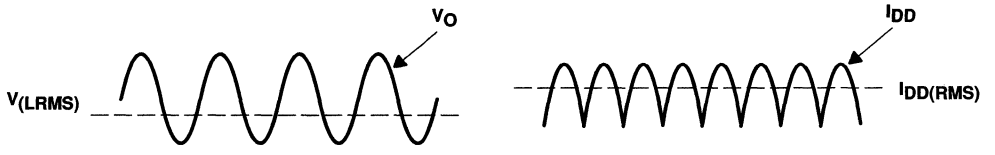


Figure 25. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-to-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

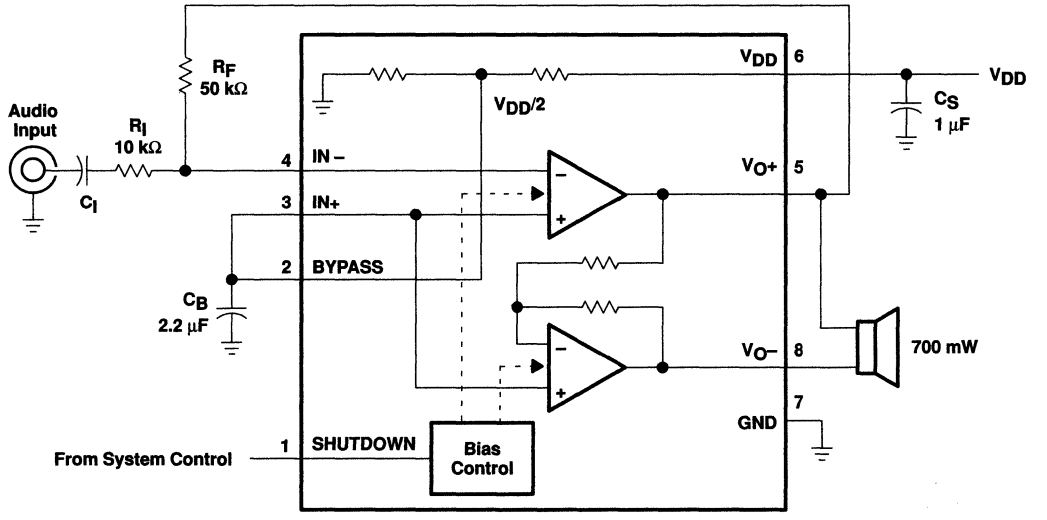


Figure 26. TPA721 Application Circuit

The following sections discuss the selection of the components used in Figure 26.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA721 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA721 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

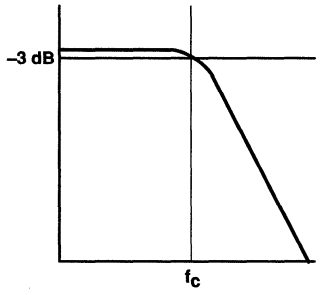
$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

APPLICATION INFORMATION

gain setting resistors, R_F and R_I (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

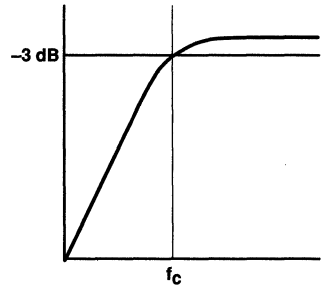


$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

For example, if R_F is 100 kΩ and C_F is 5 pF, then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.



$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \quad (9)$$

APPLICATION INFORMATION

input capacitor, C_I (continued)

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA721 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained. This insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \leq \frac{1}{\left(R_F + R_I\right) C_I} \qquad (10)$$

As an example, consider a circuit where C_B is 2.2 μF, C_I is 0.47 μF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the equation 10 we get:

$$18.2 \leq 35.5$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 2.2 μF ceramic or tantalum **low-ESR** capacitors are recommended for the best THD and noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA721 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA721 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power than operation from 5-V supplies for a given output-power level.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA721 data sheet, one can see that when the TPA721 is operating from a 5-V supply into a 8-Ω speaker that 700 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}P_W = 10\text{Log } 700 \text{ mW} = -1.5 \text{ dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

–1.5 dB – 15 dB = –16.5 (15 dB headroom)
–1.5 dB – 12 dB = –13.5 (12 dB headroom)
–1.5 dB – 9 dB = –10.5 (9 dB headroom)
–1.5 dB – 6 dB = –7.5 (6 dB headroom)
–1.5 dB – 3 dB = –4.5 (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10}$$
= 22 mW (15 dB headroom)
= 44 mW (12 dB headroom)
= 88 mW (9 dB headroom)
= 175 mW (6 dB headroom)
= 350 mW (3 dB headroom)

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 700 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA721 and maximum ambient temperatures is shown in Table 2.

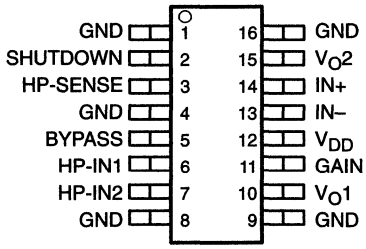
Table 2. TPA721 Power Rating, 5-V, 8-Ω, BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	D PACKAGE (SOIC)	DGN PACKAGE (MSOP)
			MAXIMUM AMBIENT TEMPERATURE (0 CFM)	MAXIMUM AMBIENT TEMPERATURE (0 CFM)
700	700 mW	675	34°C	110°C
700	350 mW (3 dB)	595	47°C	115°C
700	176 mW (6 dB)	475	68°C	122°C
700	88 mW (9 dB)	350	89°C	125°C
700	44 mW (12 dB)	225	111°C	125°C

Table 2 shows that the TPA721 can be used to its full 700-mW rating without any heat sinking in still air up to 110°C and 34°C for the DGN package (MSOP) and D pacakge (SOIC) respectively.

- 1-W BTL Output (5 V, 0.2 % THD+N)
- 3.3-V and 5-V Operation
- No Output Coupling Capacitors Required
- Shutdown Control (I_{DD} = 0.6 μA)
- Headphone Interface Logic
- Uncompensated Gains of 2 to 20 (BTL Mode)
- Surface-Mount Packaging
- Thermal and Short-Circuit Protection
- High Power Supply Rejection (56-dB at 1 kHz)
- LM4860 Drop-In Compatible

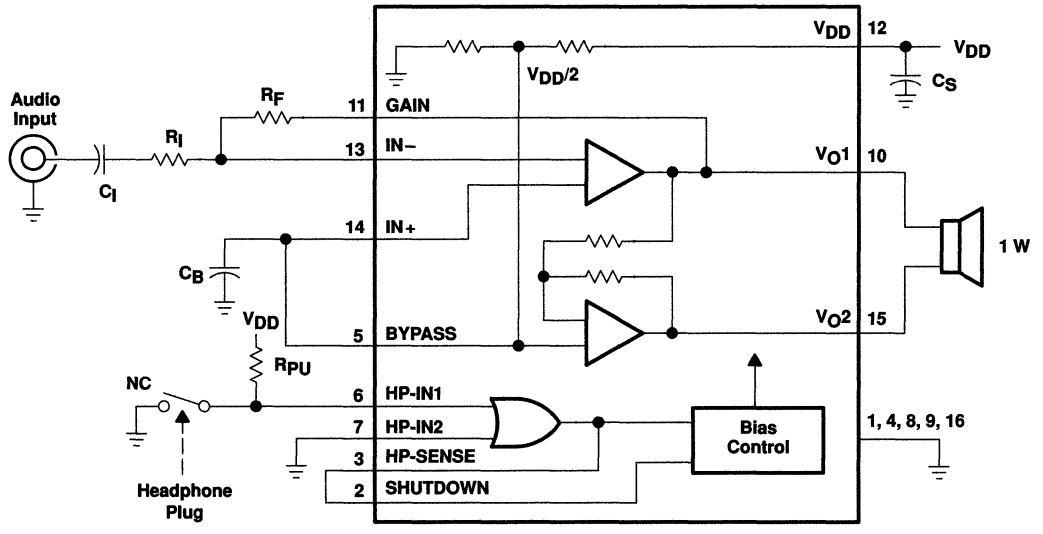
D PACKAGE
(TOP VIEW)



description

The TPA4860 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.4 % THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of this amplifier are a shutdown function for power-sensitive applications as well as headphone interface logic that mutes the output when the speaker drive is not required. Internal thermal and short-circuit protection increases device reliability. It also includes headphone interface logic circuitry to facilitate headphone applications. The amplifier is available in a 16-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.

typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE (D)
–40°C to 85°C	TPA4860D

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (See Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	1250 mW	10 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	V_{DD} = 3.3 V	1.25	2.7	V
	V_{DD} = 5 V	1.25	4.5	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature range, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4860			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage (measured differentially)	See Note 1		5	20	mV
	Supply ripple rejection ratio	V_{DD} = 3.2 V to 3.4 V		75		dB
I_{DD}	Quiescent current			2.5		mA
$I_{DD(M)}$	Quiescent current, mute mode			750		µA
$I_{DD(SD)}$	Quiescent current, shutdown mode			0.6		µA
V_{IH}	High-level input voltage (HP-IN)			1.7		V
V_{IL}	Low-level input voltage (HP-IN)			1.7		V
V_{OH}	High-level output voltage (HP-SENSE)	I_O = 100 µA	2.5	2.8		V
V_{OL}	Low-level output voltage (HP-SENSE)	I_O = –100 µA		0.2	0.8	V

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4860			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		350		mW
			THD = 2%, f = 1 kHz, A_V = 2		500		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4860			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
	Supply ripple rejection ratio	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current			3.5		mA
$I_{DD(M)}$	Supply current, mute			750		µA
$I_{DD(SD)}$	Supply current, shutdown			0.6		µA
V_{IH}	High-level input voltage (HP-IN)			2.5		V
V_{IL}	Low-level input voltage (HP-IN)			2.5		V
V_{OH}	High-level output voltage (HP-SENSE)	I_O = 500 µA	2.5	2.8		V
V_{OL}	Low-level output voltage (HP-SENSE)	I_O = −500 µA		0.2	0.8	V

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4860			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Maximum package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum output power	vs Free-air temperature	28
	Output power	vs Load Resistance	29
		vs Supply Voltage	30
	Open loop frequency response	vs Frequency	31
	Supply ripple rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

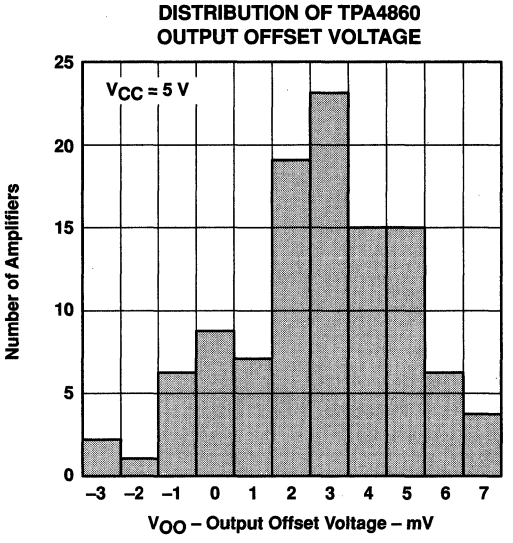


Figure 1

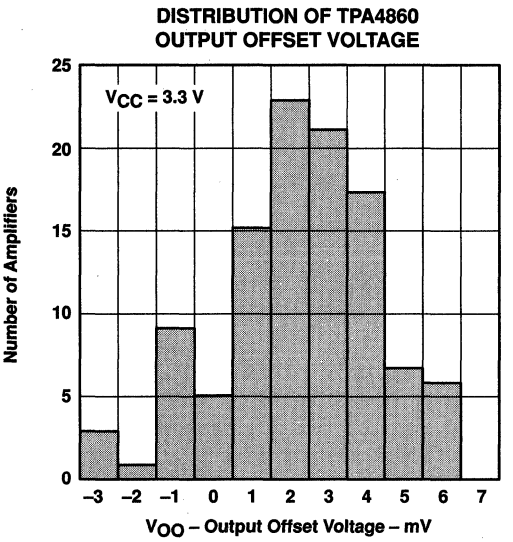


Figure 2

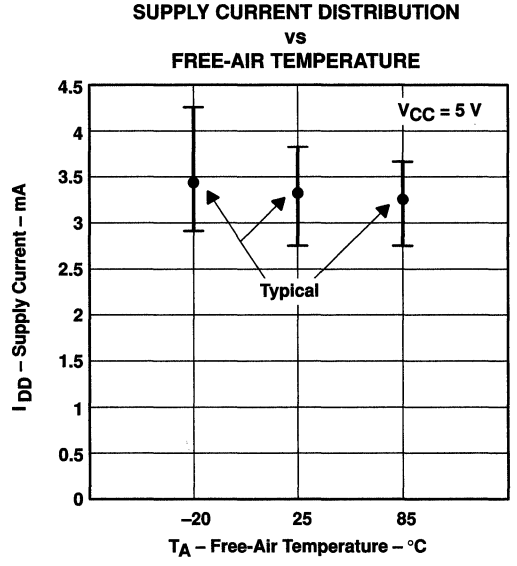


Figure 3

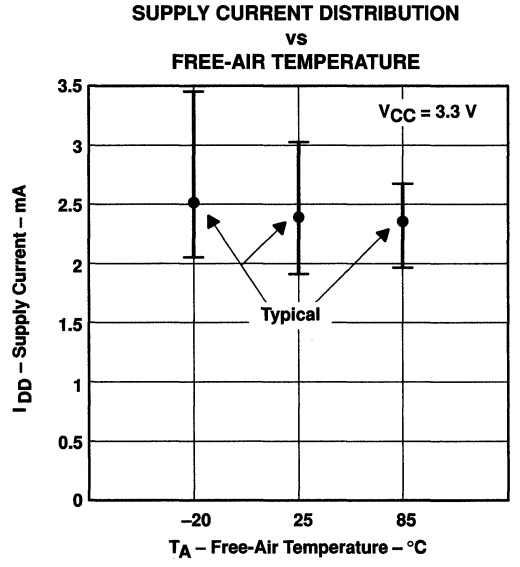


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

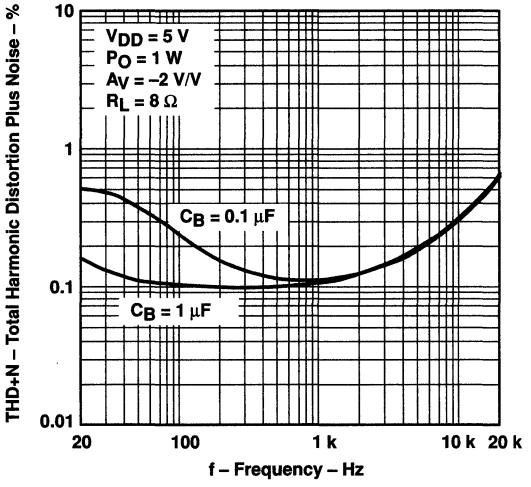


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

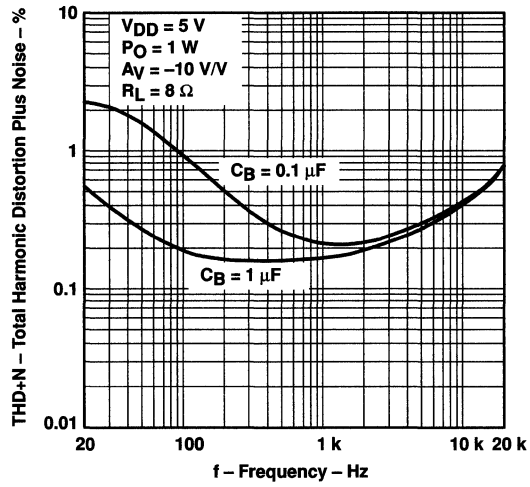


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

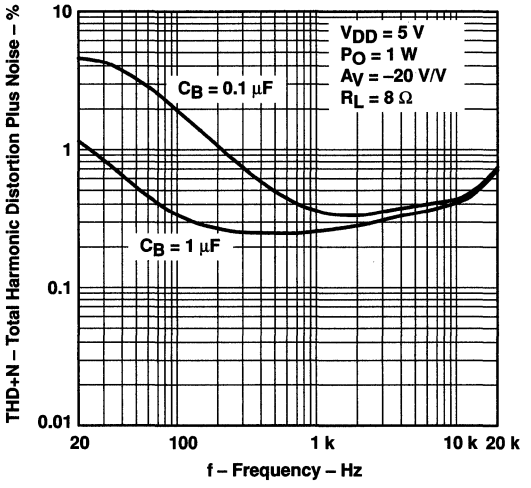


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

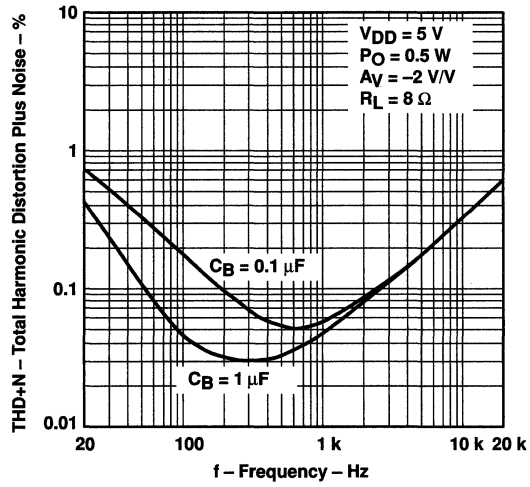


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

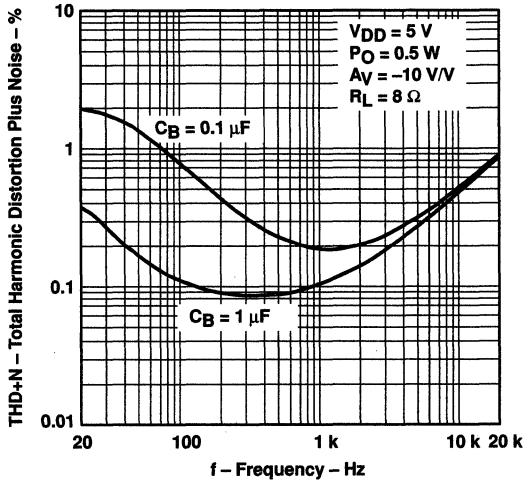


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

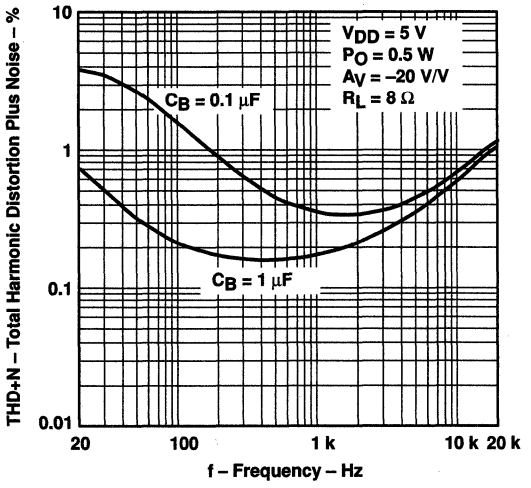


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

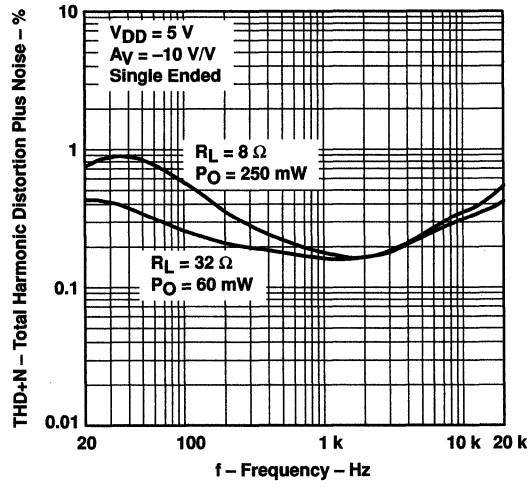


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

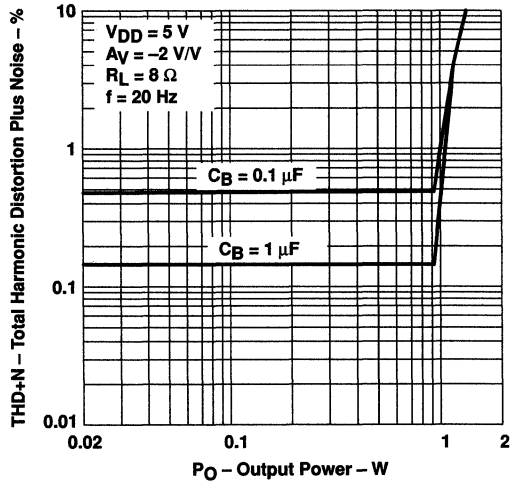


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

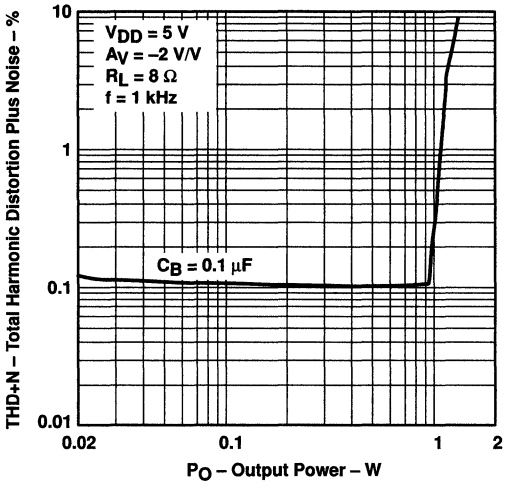


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

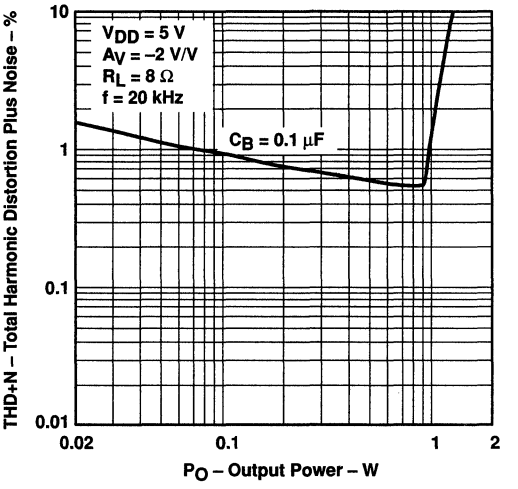


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

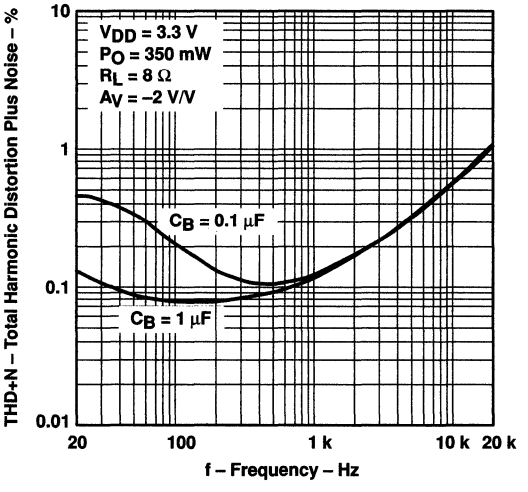


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

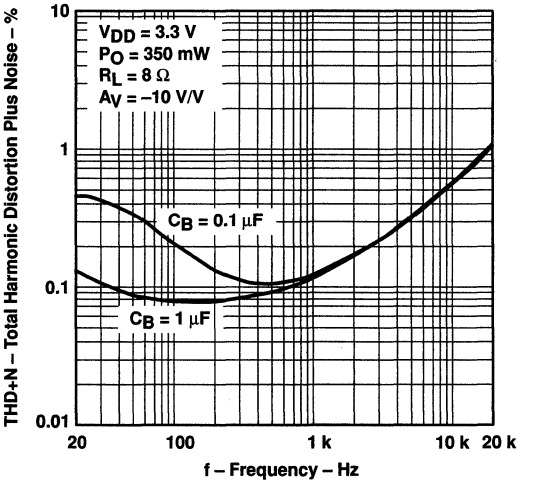


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

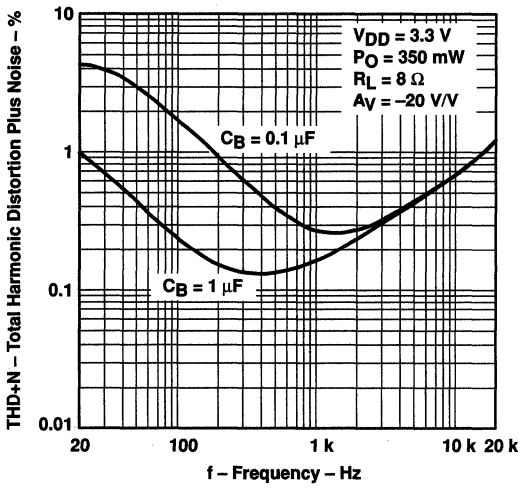


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

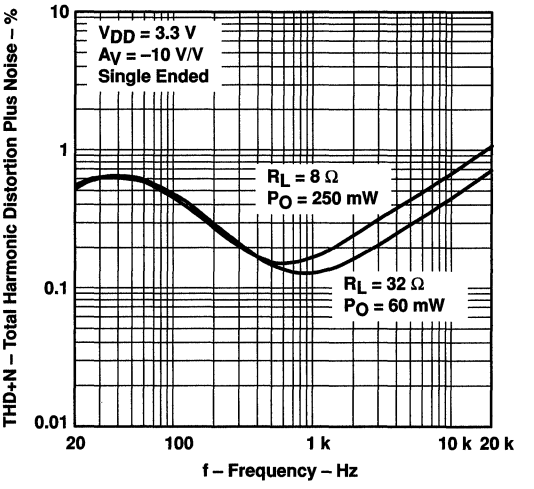


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

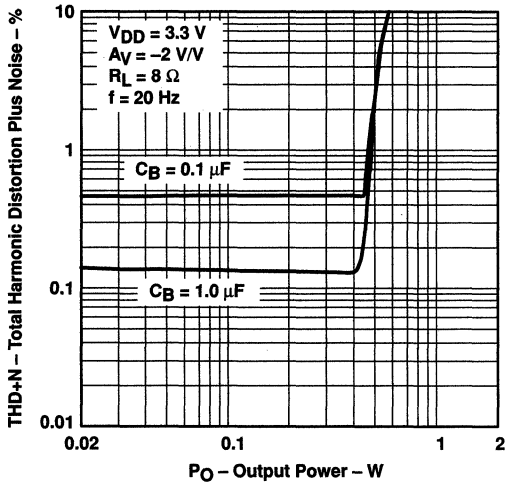


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

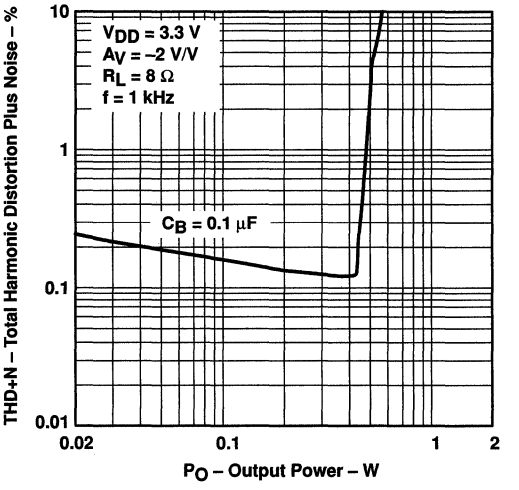


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

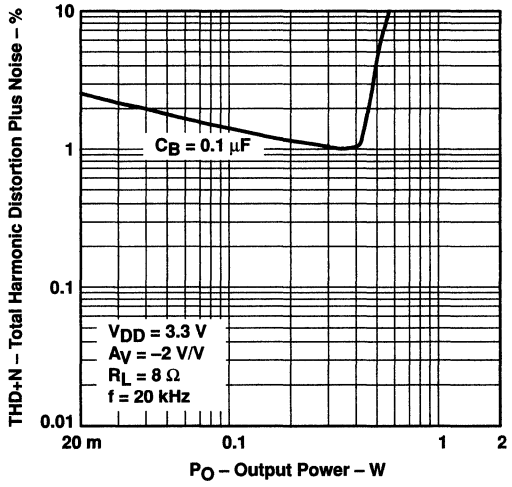


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

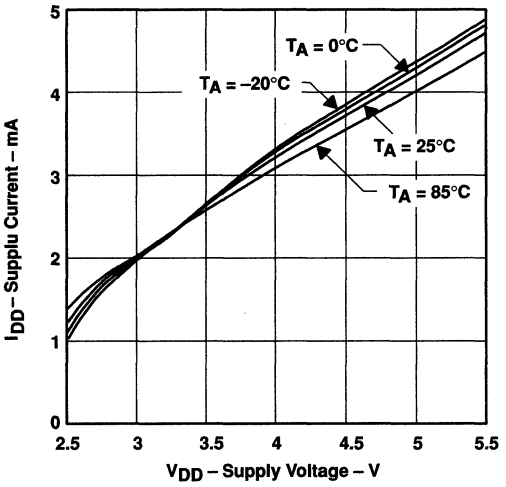


Figure 22

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

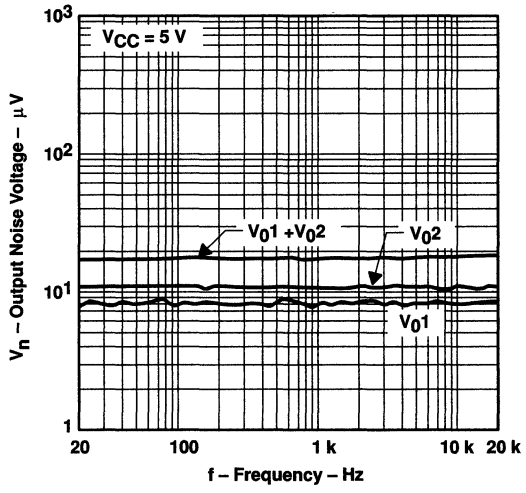


Figure 23

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

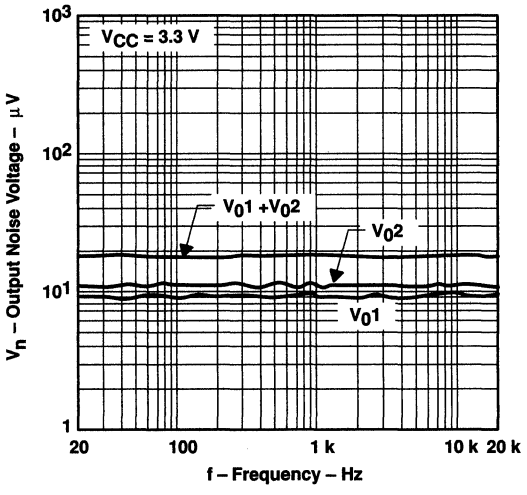


Figure 24

TYPICAL CHARACTERISTICS

MAXIMUM PACKAGE POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

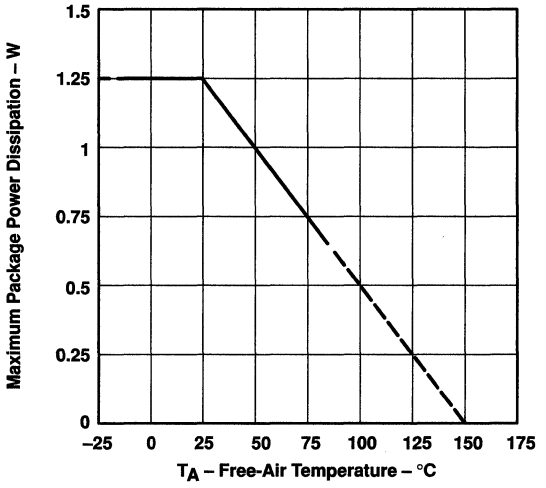


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

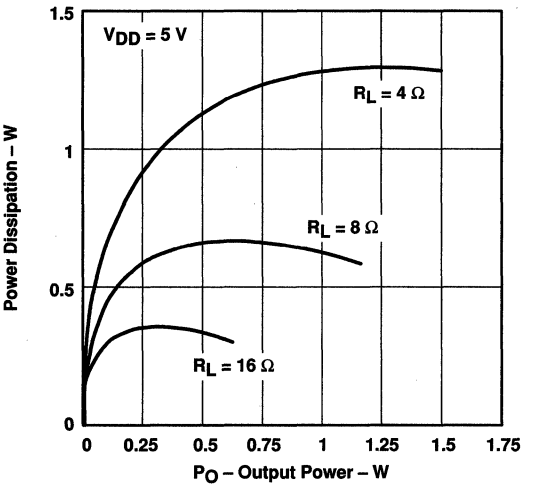


Figure 26

POWER DISSIPATION
vs
OUTPUT POWER

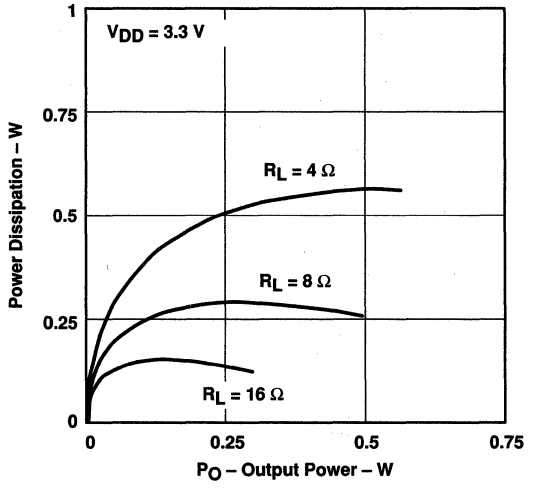


Figure 27

MAXIMUM OUTPUT POWER
vs
FREE-AIR TEMPERATURE

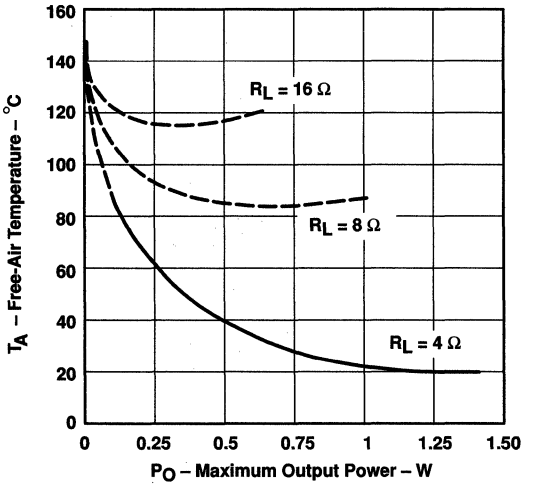


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

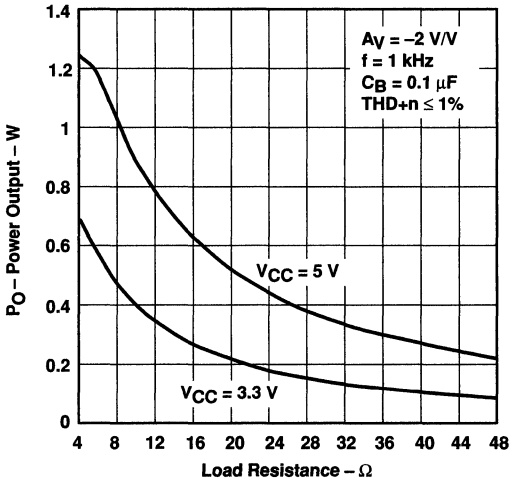


Figure 29

OUTPUT POWER
vs
SUPPLY VOLTAGE

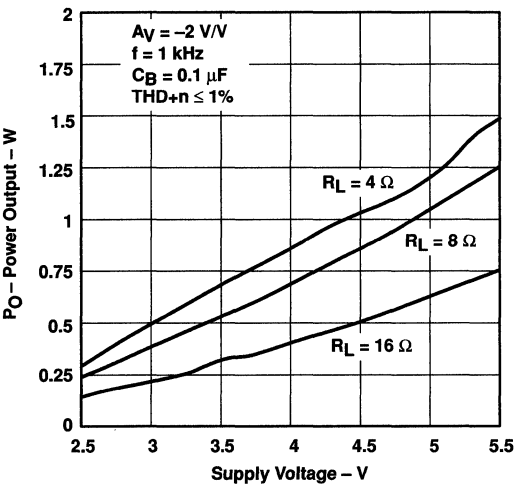


Figure 30

OPEN LOOP FREQUENCY RESPONSE

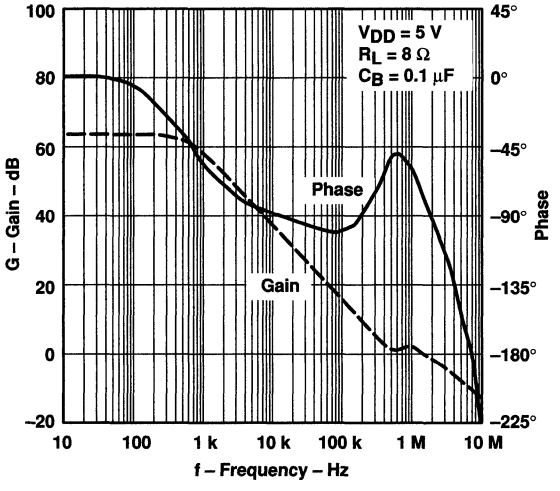


Figure 31

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

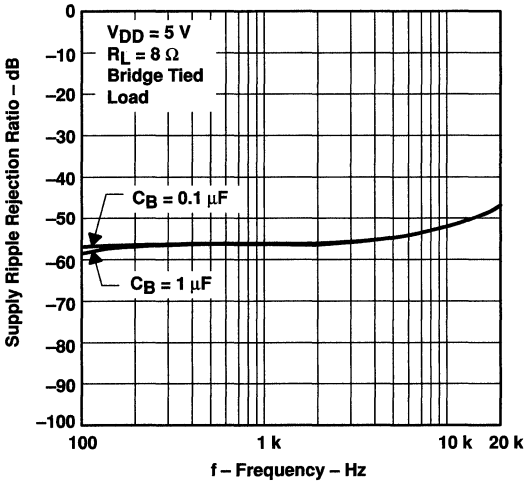


Figure 32

TYPICAL CHARACTERISTICS

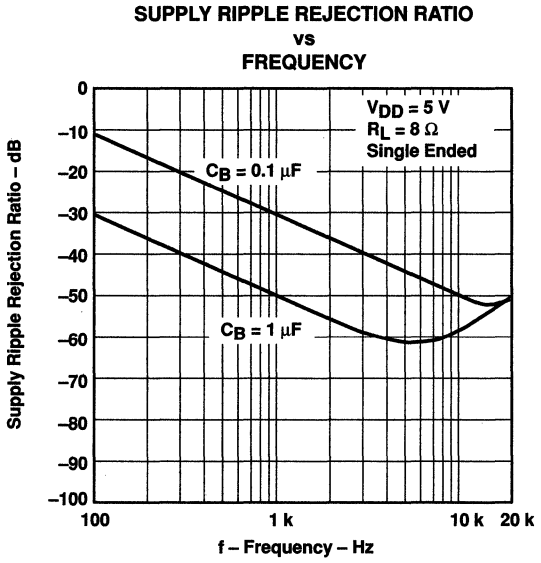


Figure 33

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a bridge tied load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging twice the voltage into the power equation, where voltage is squared, yields 4 times the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

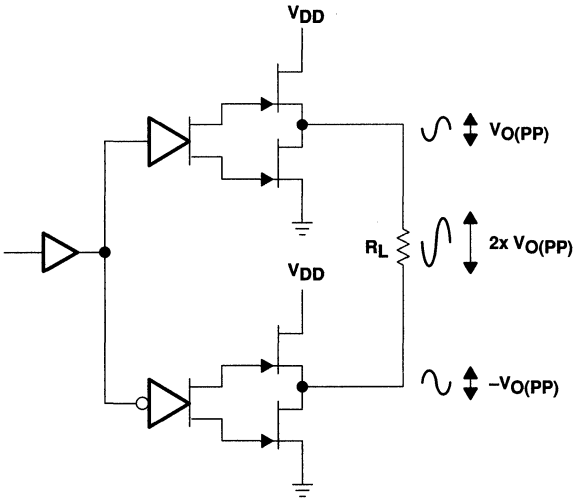


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into a 8-Ω speaker from a singled-ended (SE) limit of 250 mW to 1 W. In sound power, that is a 6-dB improvement which is loudness that can be heard. In addition to increased power there are frequency response concerns, consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 40 μF to 1000 μF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

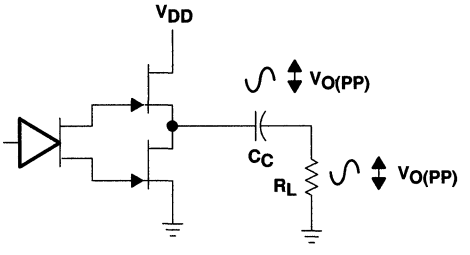


Figure 35. Single-Ended Configuration

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 times the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy to use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 36).

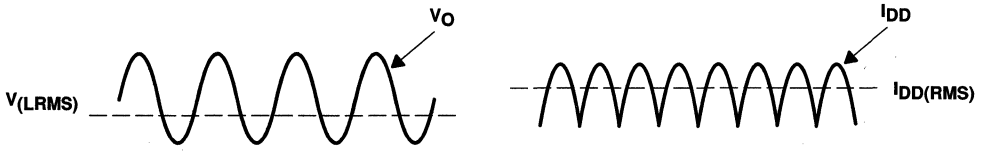


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistor are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

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$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers whether they are SE or BTL configured is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4860 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

APPLICATION INFORMATION

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.

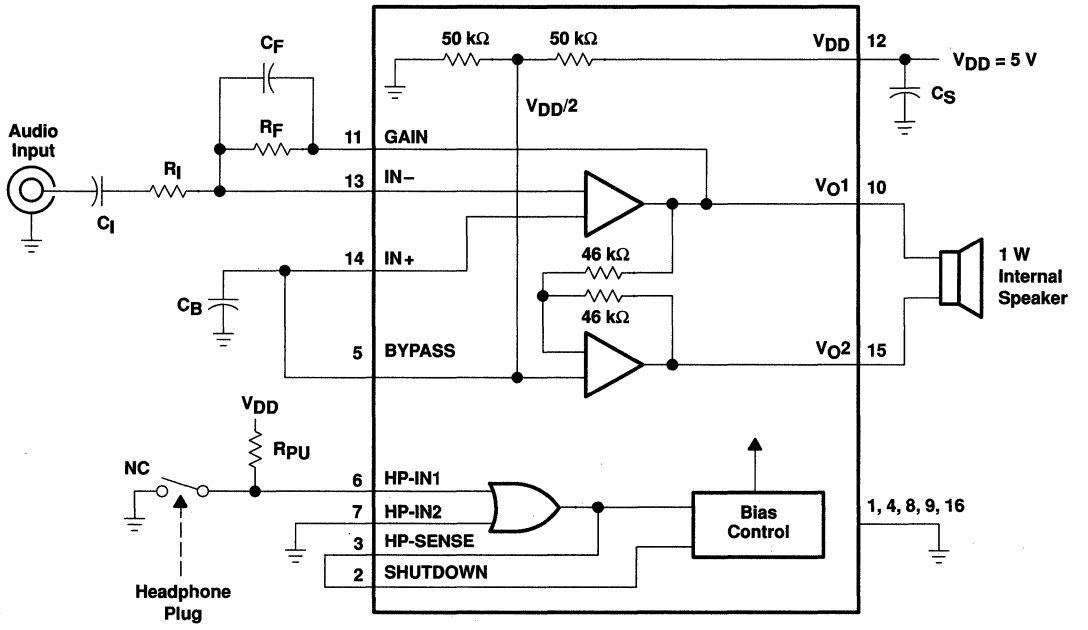

Figure 37. TPA4860 Typical Notebook Computer Application Circuit

gain setting resistors, R_F and R_I

The gain for the TPA4860 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4860 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

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gain setting resistors, R_F and R_I (continued)

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (7)$$

For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA4860 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

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midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \qquad (10)$$

As an example, consider a circuit where C_B is 0.1 μF, C_I is 0.22 μF and R_I is 10 kΩ. Inserting these values into the equation 9 we get: 400 ≤ 454 which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (OUT1, terminal 10).

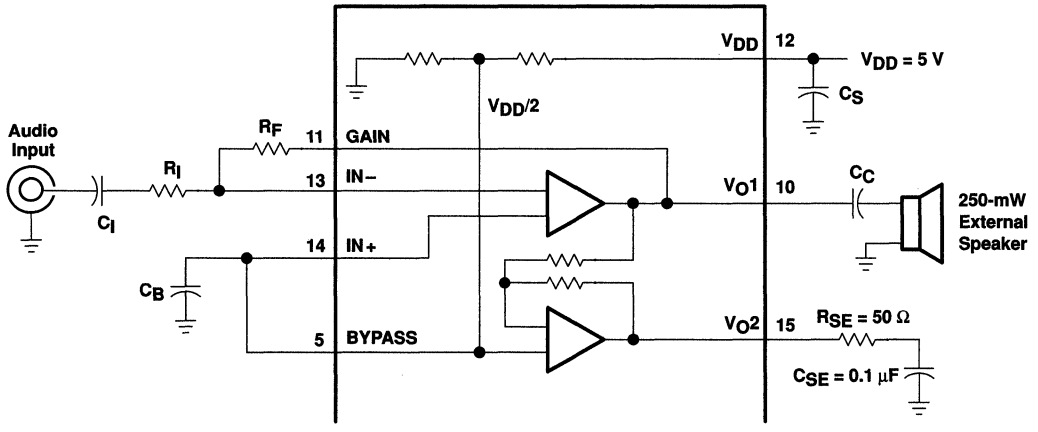

Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \qquad (11)$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-μF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

APPLICATION INFORMATION

single-ended operation (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{12}$$

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{c\ high} = \frac{1}{2\pi R_L C_C} \tag{13}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drives the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	68 µF	293 Hz
32 Ω	68 µF	73 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 2 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

headphone sense circuitry, R_{pu}

The TPA4860 is commonly used in systems where there is an internal speaker and a jack for driving external loads (i.e., headphones). In these applications, it is usually desirable to mute the internal speaker(s) when the external load is in use. The headphone inputs (HP-1, HP-2) and headphone output (HP-SENSE) of the TPA4860 were specifically designed for this purpose. Many standard headphone jacks are available with an internal single-pole single-throw (SPST) switch that makes or breaks a circuit when the headphone plug is inserted. Asserting either or both HP-1 and/or HP-2 high mutes the output stage of the amplifier and causes HP-SENSE to go high. In battery-powered applications where power conservation is critical HP-SENSE can be connected to the shutdown input as shown in Figure 39. This places the amplifier in a very low current state for maximum power savings. Pullup resistors in the range from 1 kΩ to 10 kΩ are recommended for 5-V and 3.3-V operation.

APPLICATION INFORMATION

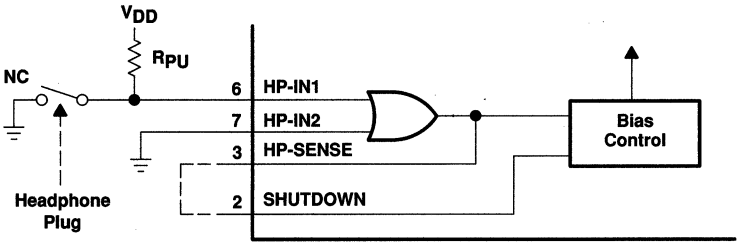

Figure 39. Schematic Diagram of Typical Headphone Sense Application

Table 3 details the logic for the mute function of the TPA4860.

Table 3. Truth Table for Headphone Sense and Shutdown Functions

INPUTS†			OUTPUT	AMPLIFIER STATE
HP-1	HP-2	SHUTDOWN	HP-SENSE	
Low	Low	Low	Low	Active
Low	High	Low	High	Mute
High	Low	Low	High	Mute
High	High	Low	High	Mute
X	X	High	X	Shutdown

† Inputs should never be left unconnected.
X = do not care

shutdown mode

The TPA4860 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} < 1\ \mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 40 provides an easy way to determine what output power can be expected out of the TPA4860 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

APPLICATION INFORMATION

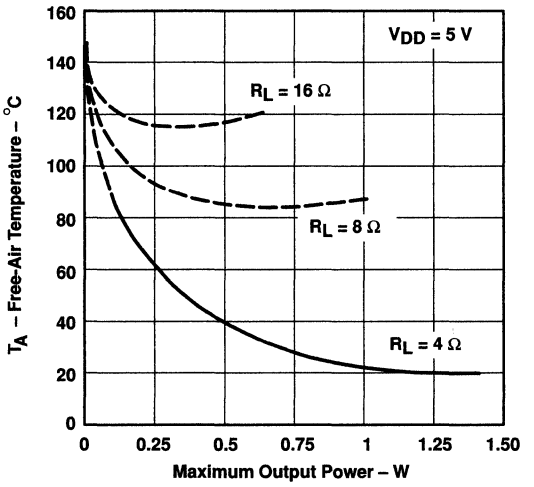

Figure 40. Free-Air Temperature Versus Maximum Continuous Output Power

5-V versus 3.3-V operation

The TPA4860 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in TPA4860 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load to less than 0.33 W before distortion begins to become significant.

Operation at 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

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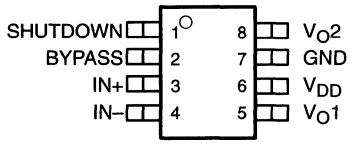
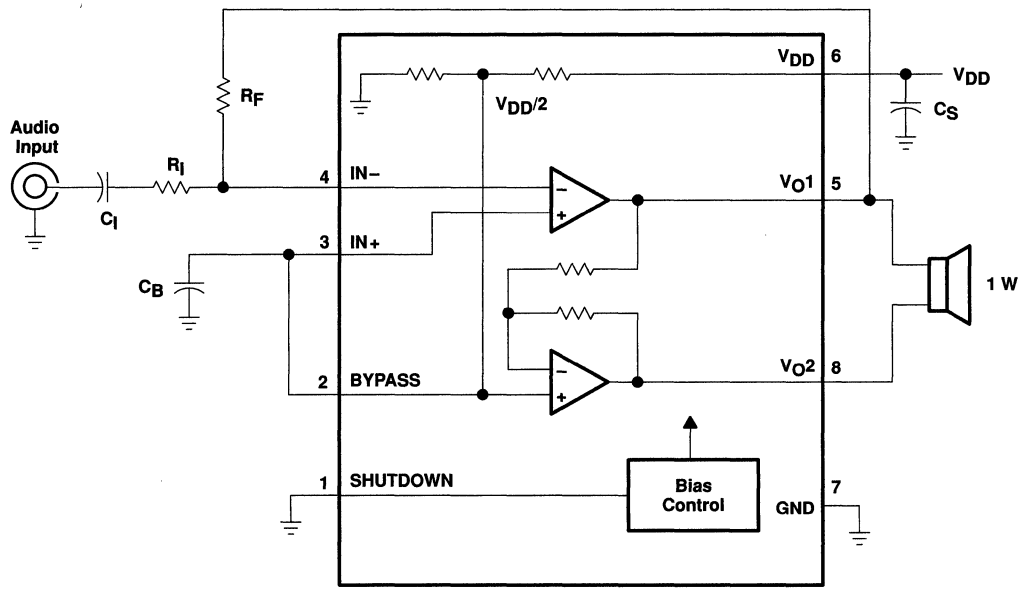
- 1-W BTL Output (5 V, 0.11 % THD+N)
- 3.3-V and 5-V Operation
- No Output Coupling Capacitors Required
- Shutdown Control (I_{DD} = 0.6 μA)
- Uncompensated Gains of 2 to 20 (BTL Mode)
- Surface-Mount Packaging
- Thermal and Short-Circuit Protection
- High Supply Ripple Rejection Ratio (56 dB at 1 kHz)
- LM4861 Drop-In Compatible

D PACKAGE
(TOP VIEW)



description

The TPA4861 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.2% THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of the amplifier are a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The TPA4861 works seamlessly with TI's TPA4860 in stereo applications. The amplifier is available in an 8-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE† (D)
–40°C to 85°C	TPA4861D

† The D package is available tape and reeled. To order a tape and reeled part, add the suffix R to the part number (e.g., TPA4861DR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1 μF – 1.0 μF capacitor when used as an audio power amplifier.
GND	7		GND is the ground connection.
IN–	4	I	IN– is the inverting input. IN– is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high ($I_{DD} \leq 0.6$ μA).
V_O1	5	O	V_O1 is the positive BTL output.
V_O2	8	O	V_O2 is the negative BTL output.
V_{DD}	6		V_{DD} is the supply voltage terminal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... Internally Limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25$°C	DERATING FACTOR	$T_A = 70$°C	$T_A = 85$°C
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	1.25	2.7	V
	V_{DD} = 5 V	1.25	4.5	V
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1			20	mV
PSRR	Power supply rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 3.2 V to 3.4 V		75		dB
I_{DD}	Supply current			2.5		mA
$I_{DD(SD)}$	Supply current, shutdown			0.6		μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS		TPA4861			UNIT
					MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz,	A_V = –2 V/V		400		mW
			THD = 2%, f = 1 kHz,	A_V = –2 V/V		500		mW
B_{OM}	Maximum output power bandwidth		Gain = –10 V/V,	THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop			1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz,	C_B = 0.1 μF		56		dB
		SE	f = 1 kHz,	C_B = 0.1 μF		30		dB
V_n	Noise output voltage, see Note 3		Gain = –2 V/V			20		μV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1			20	mV
PSRR	Power supply rejection ratio ($\Delta V_{DD}/\Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
I_{DD}	Supply current			3.5		mA
$I_{DD(SD)}$	Supply current, shutdown			0.6		μA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS		TPA4861			UNIT
					MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz,	A_V = –2 V/V		1000		mW
			THD = 2%, f = 1 kHz,	A_V = –2 V/V		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = –10 V/V,	THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop			1.5		MHz
	Supply ripple rejection ratio	BTL	f = 1 kHz,	C_B = 0.1 μF		56		dB
		SE	f = 1 kHz,	C_B = 0.1 μF		30		dB
V_n	Noise output voltage, see Note 3		Gain = –2 V/V			20		μV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Maximum package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum power output	vs Free-air temperature	28
	Output power	vs Load resistance	29
		vs Supply voltage	30
	Open-loop gain	vs Frequency	31
k_{SVR}	Supply ripple rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TPA4861
OUTPUT OFFSET VOLTAGE

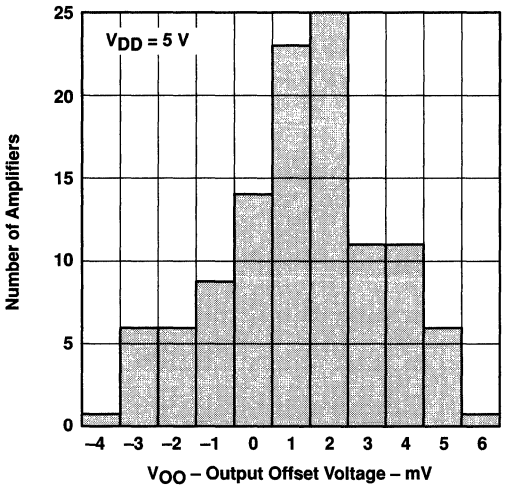


Figure 1

DISTRIBUTION OF TPA4861
OUTPUT OFFSET VOLTAGE

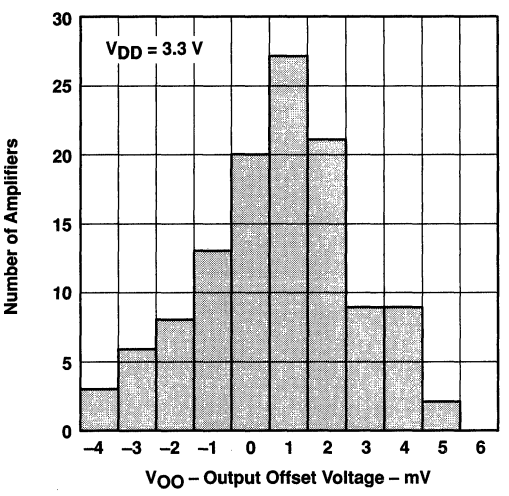


Figure 2

SUPPLY CURRENT DISTRIBUTION
vs
FREE-AIR TEMPERATURE

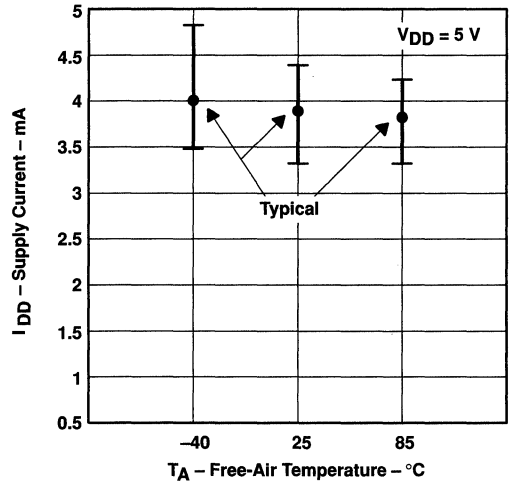


Figure 3

SUPPLY CURRENT DISTRIBUTION
vs
FREE-AIR TEMPERATURE

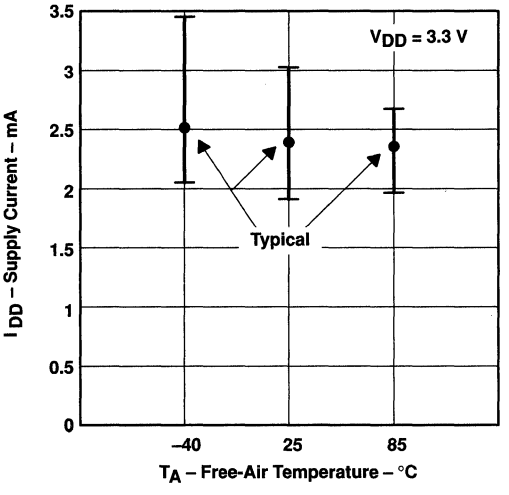


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

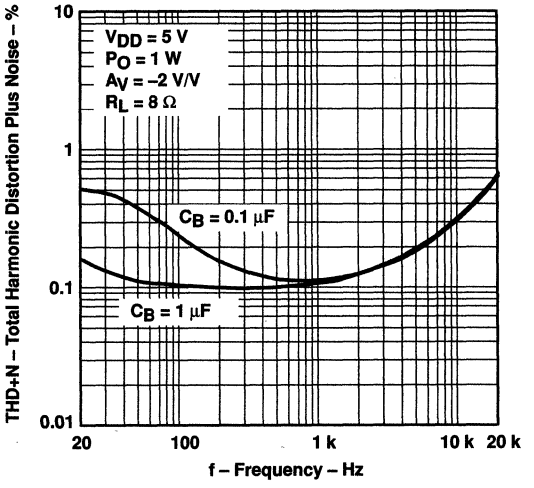


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

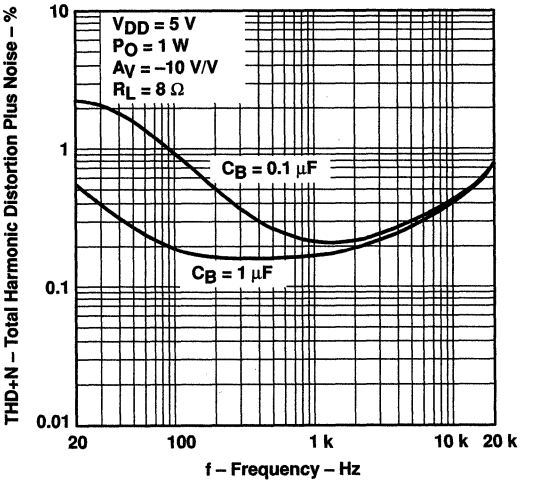


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

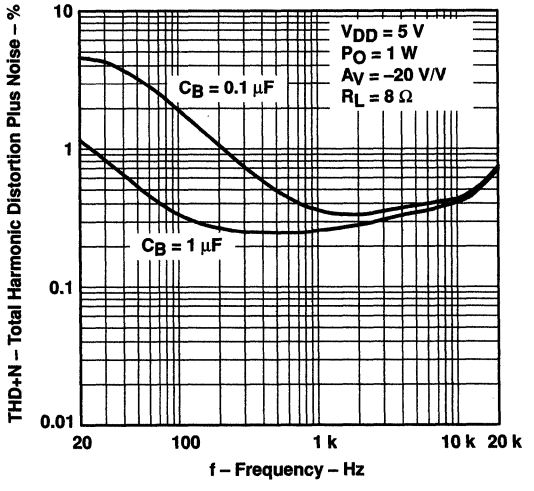


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

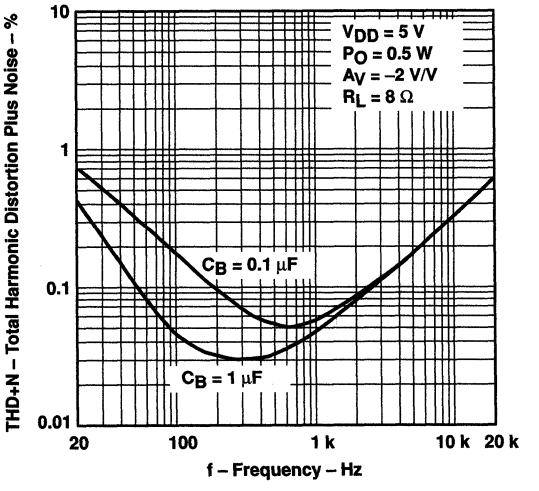


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

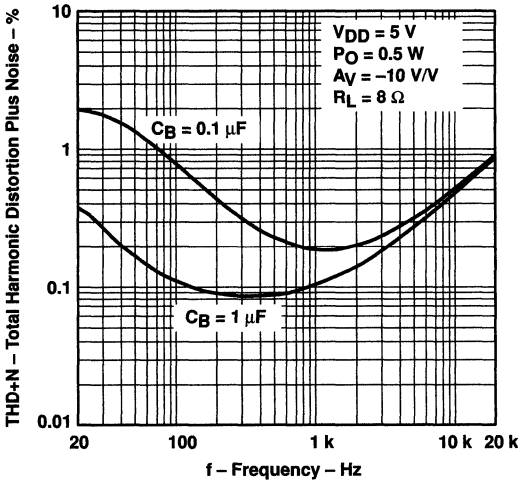


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

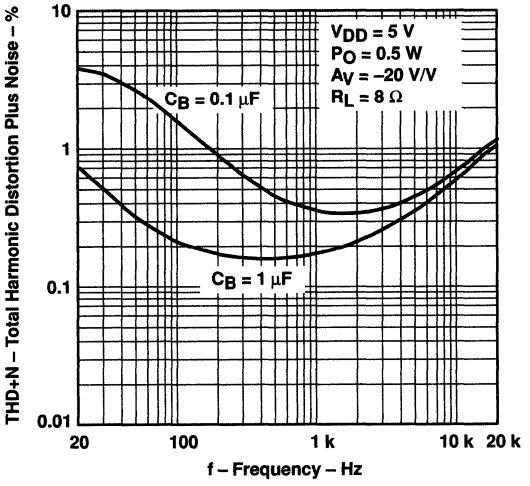


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

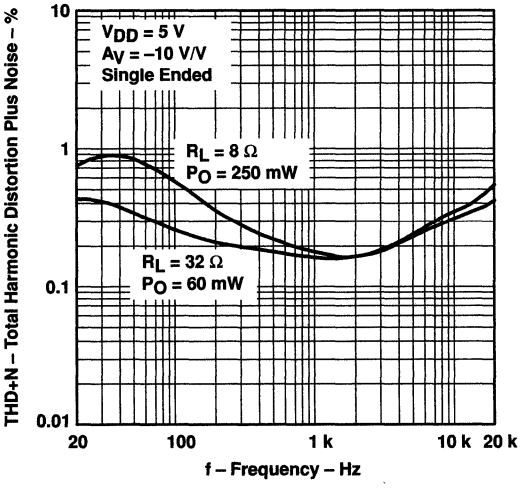


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

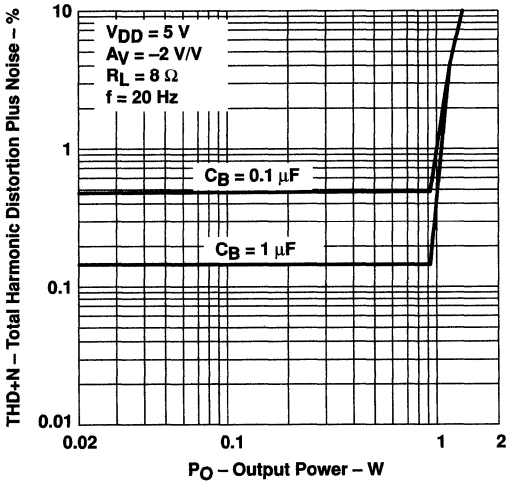


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

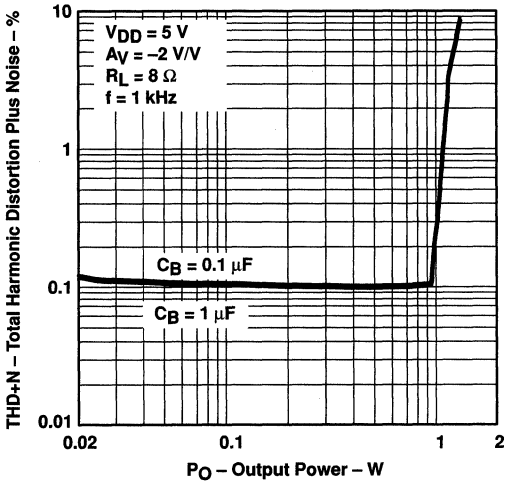


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

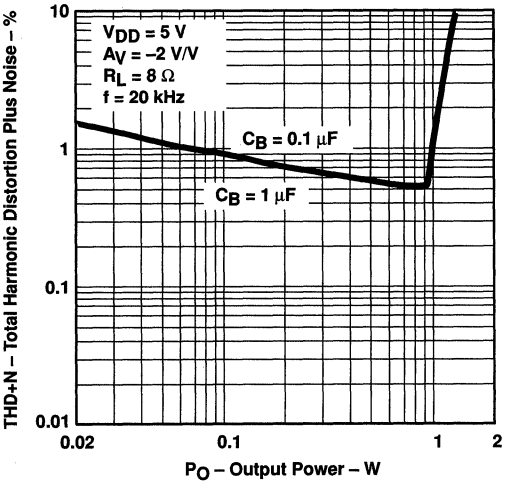


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

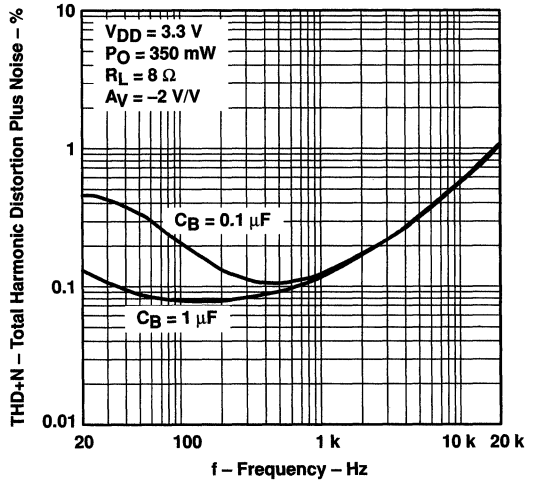


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

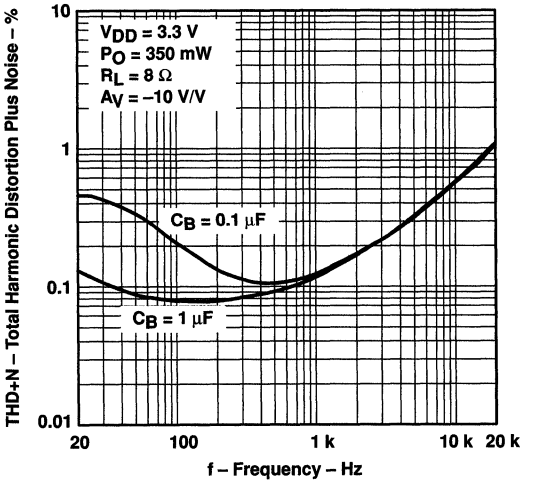


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

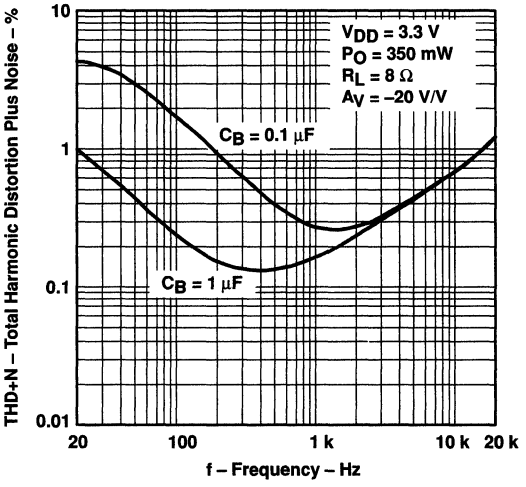


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

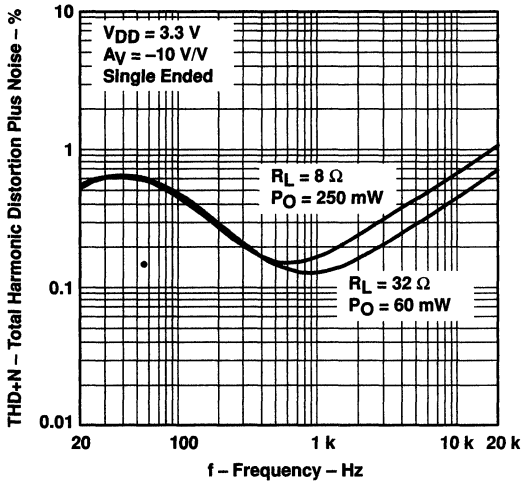


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

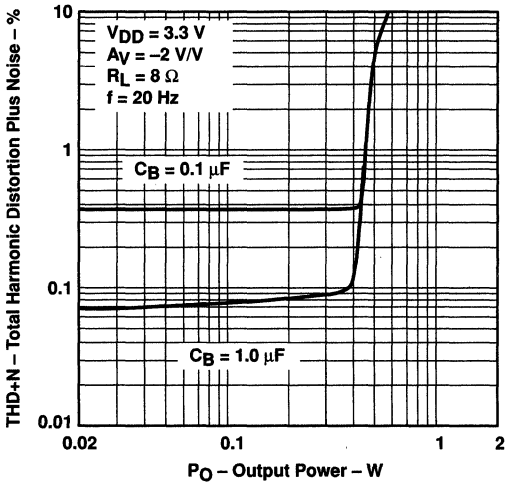


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

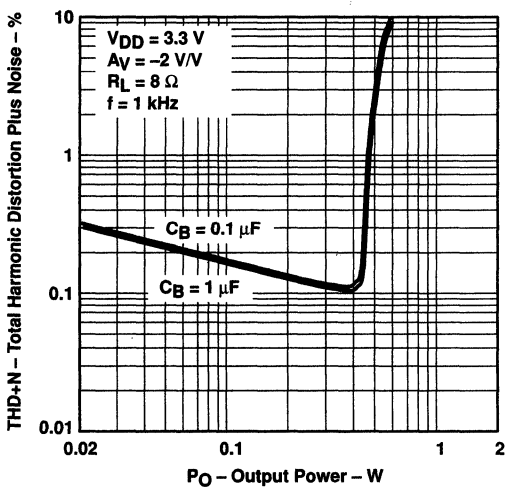


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

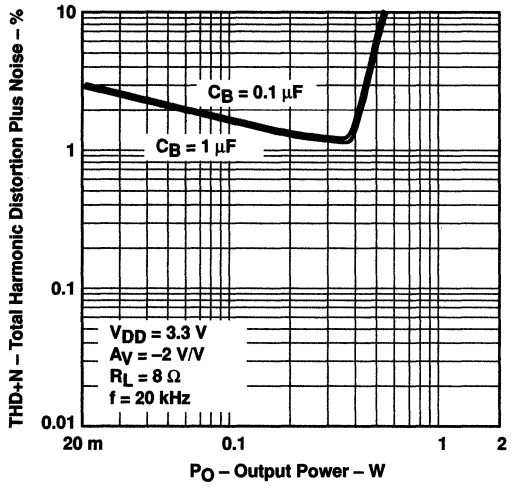


Figure 21

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

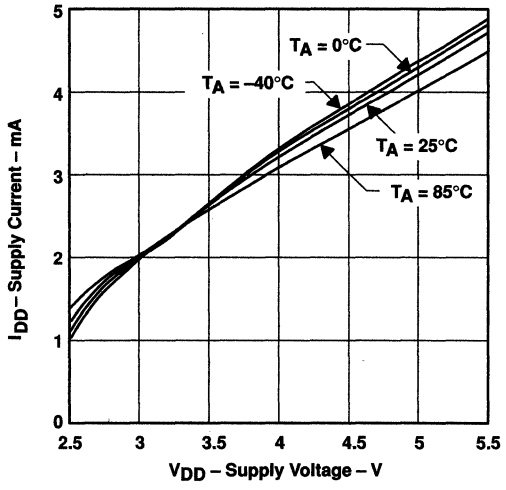


Figure 22

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

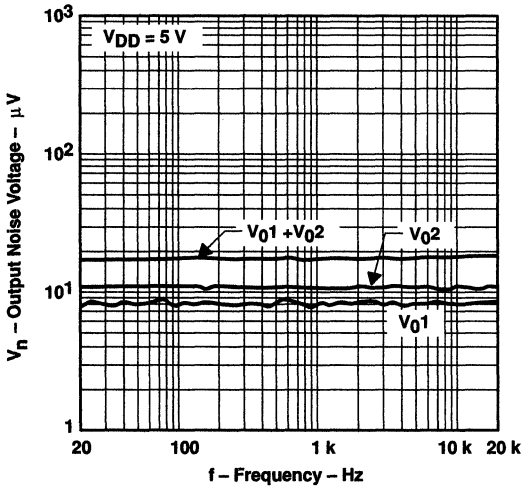


Figure 23

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

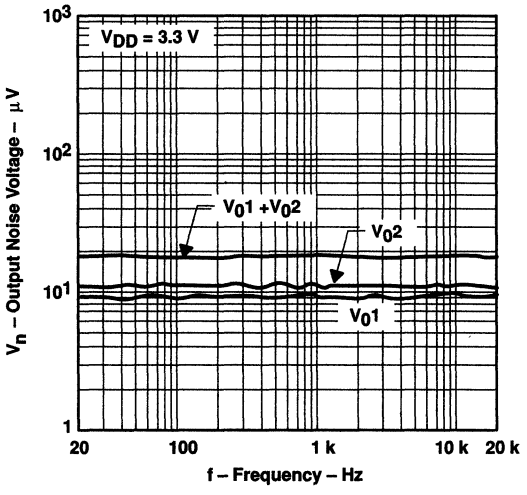


Figure 24

TYPICAL CHARACTERISTICS

MAXIMUM PACKAGE POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

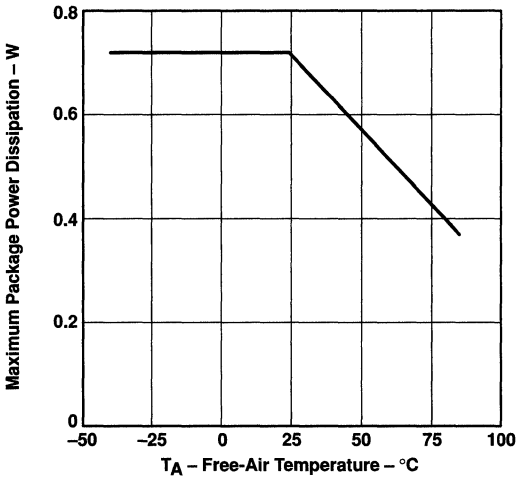


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

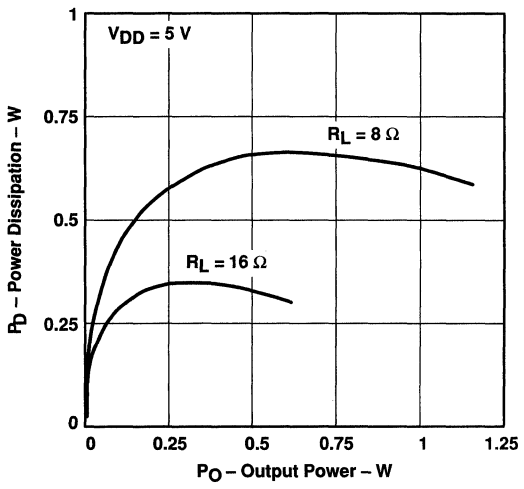


Figure 26

POWER DISSIPATION
vs
OUTPUT POWER

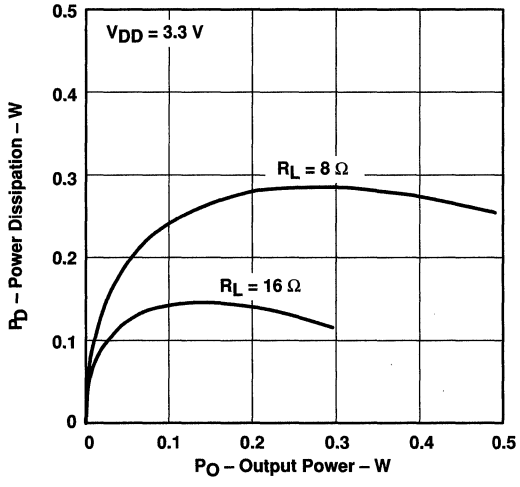


Figure 27

MAXIMUM OUTPUT POWER
vs
FREE-AIR TEMPERATURE

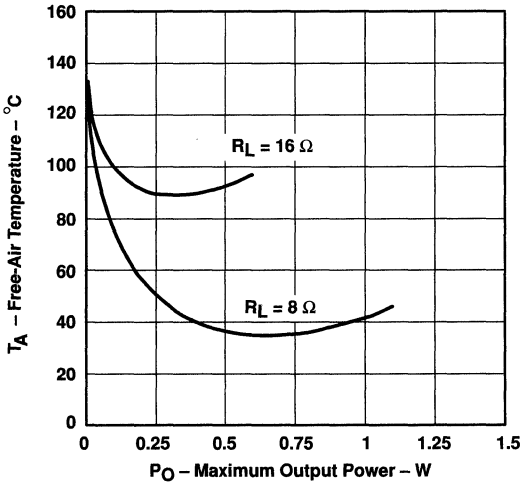


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

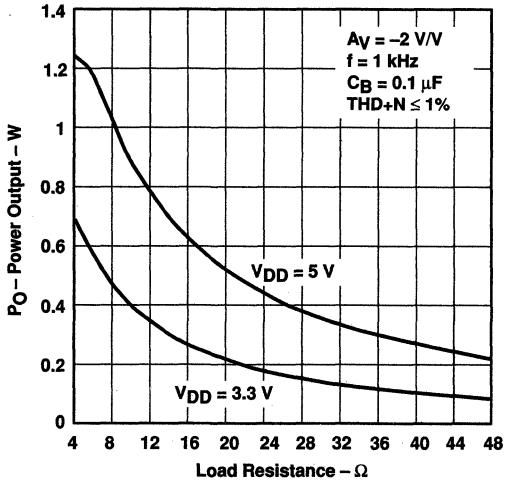


Figure 29

OUTPUT POWER
vs
SUPPLY VOLTAGE

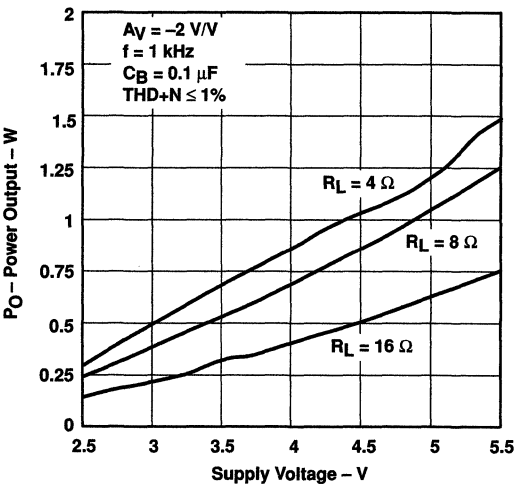


Figure 30

OPEN-LOOP GAIN
vs
FREQUENCY

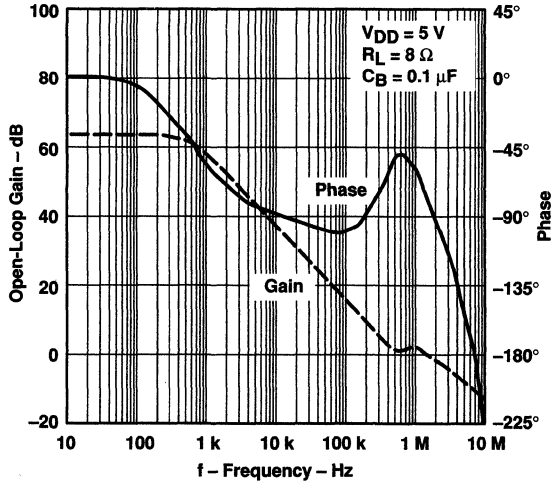


Figure 31

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

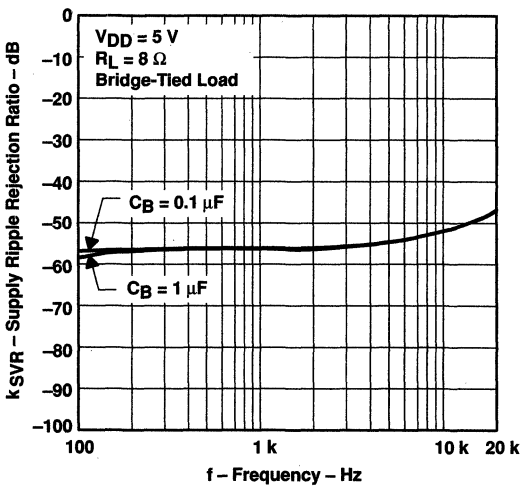


Figure 32

TYPICAL CHARACTERISTICS

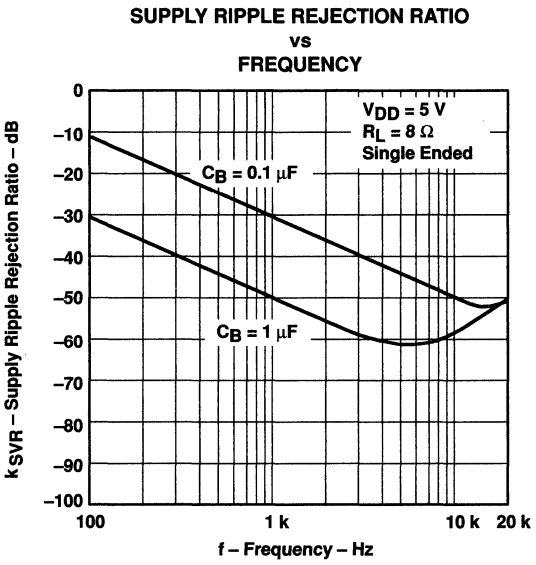


Figure 33

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a bridge-tied load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially, let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This, in effect, doubles the voltage swing on the load as compared to a ground-referenced load. Plugging twice the voltage into the power equation, where voltage is squared, yields 4 times the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

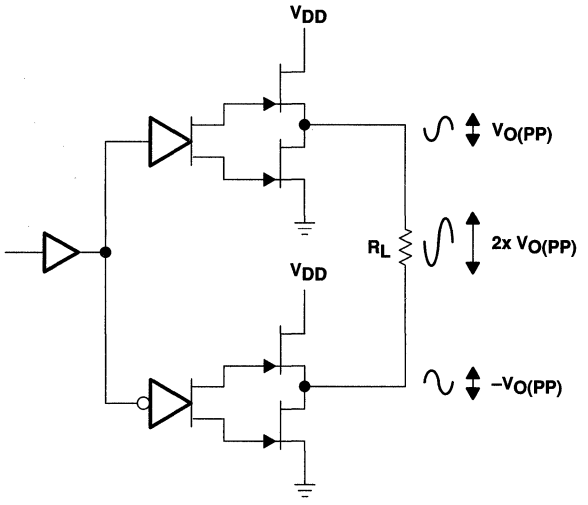


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power, frequency response is a concern; consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 40 μF to 1000 μF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

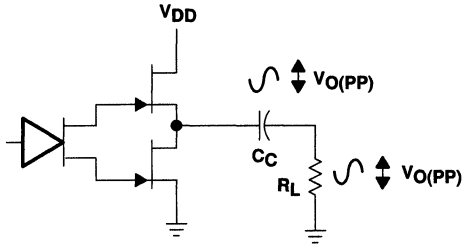


Figure 35. Single-Ended Configuration

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 times the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 36).

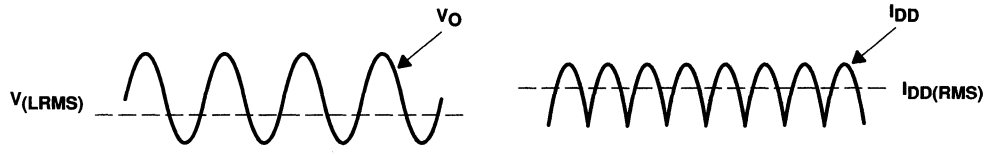


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistor are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak-to-Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

APPLICATION INFORMATION

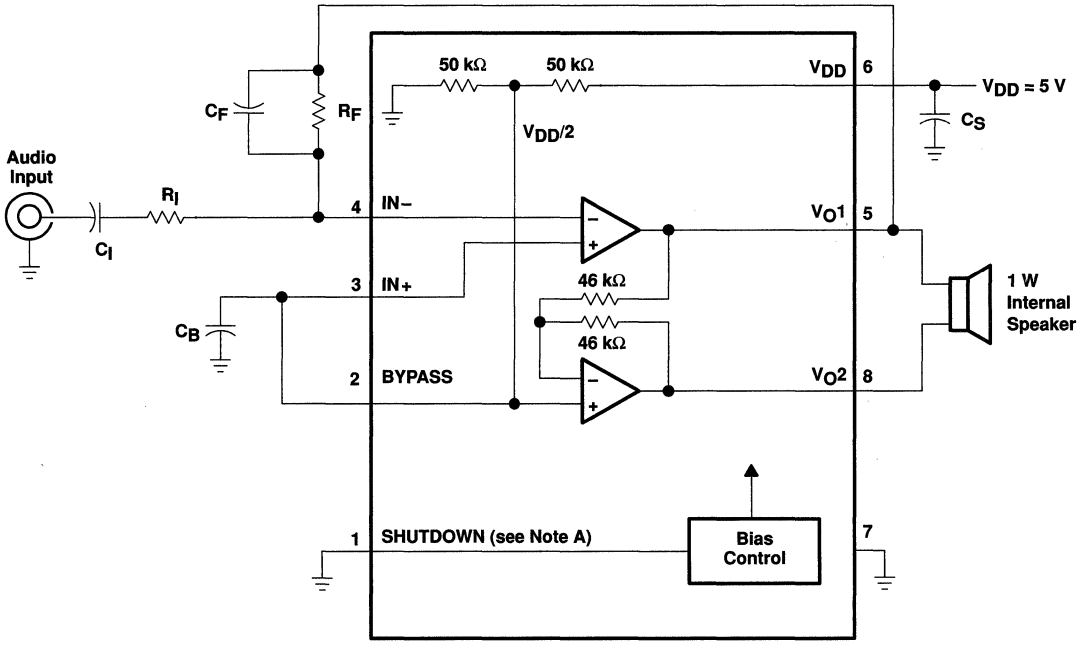
BTL amplifier efficiency (continued)

A final point to remember about linear amplifiers, whether they are SE or BTL configured, is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4861 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.



NOTE A. SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 37. TPA4861 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA4861 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4861 is a MOS amplifier, the input impedance is very high; consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA4861 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \qquad (10)$$

As an example, consider a circuit where C_B is 0.1 μF, C_I is 0.22 μF and R_I is 10 kΩ. Inserting these values into the equation 9 we get:

$$400 \leq 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (V_O1, terminal 5).

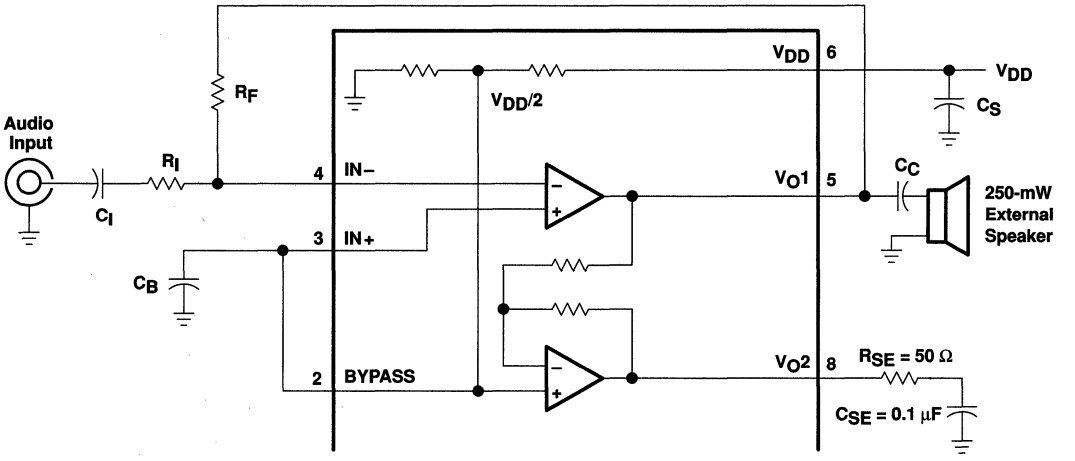


Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-µF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{(C_B \times 25\ \text{k}\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{12}$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{out\ high} = \frac{1}{2\pi R_L C_C} \quad (13)$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drives the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
8 Ω	68 µF	293 Hz
32 Ω	68 µF	73 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 2 indicates, most of the bass response is attenuated into 8-Ω loads, while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

shutdown mode

The TPA4861 employs a shutdown mode of operation designed to reduce supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)}$ = 0.6 µA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 39 provides an easy way to determine what output power can be expected out of the TPA4861 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

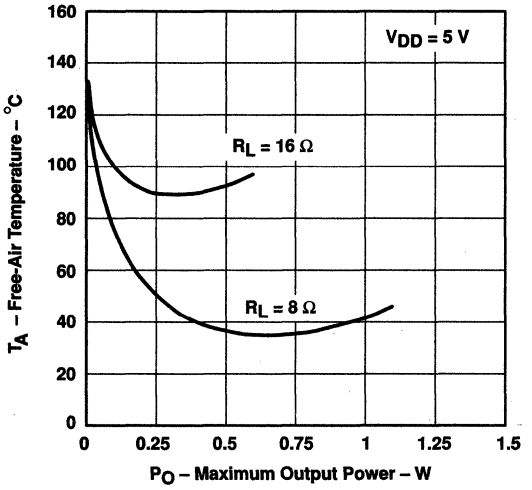


Figure 39. Free-Air Temperature vs Maximum Continuous Output Power

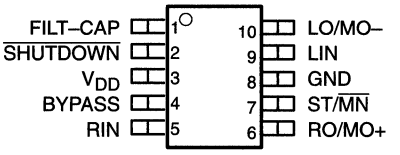
5-V versus 3.3-V operation

The TPA4861 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in TPA4861 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load to less than 0.33 W before distortion begins to become significant.

Operation at 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds of the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **1 W Into 8-Ω From 5-V Supply**
- **0.3 W Into 8-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Mono (BTL) Signal Created by Summing Left and Right Signals Internally**
- **Wide Power Supply Compatibility 2.5 V to 5.5 V**
- **Low Supply Current**
  - **3.2 mA Typical at 5 V**
  - **2.7 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)

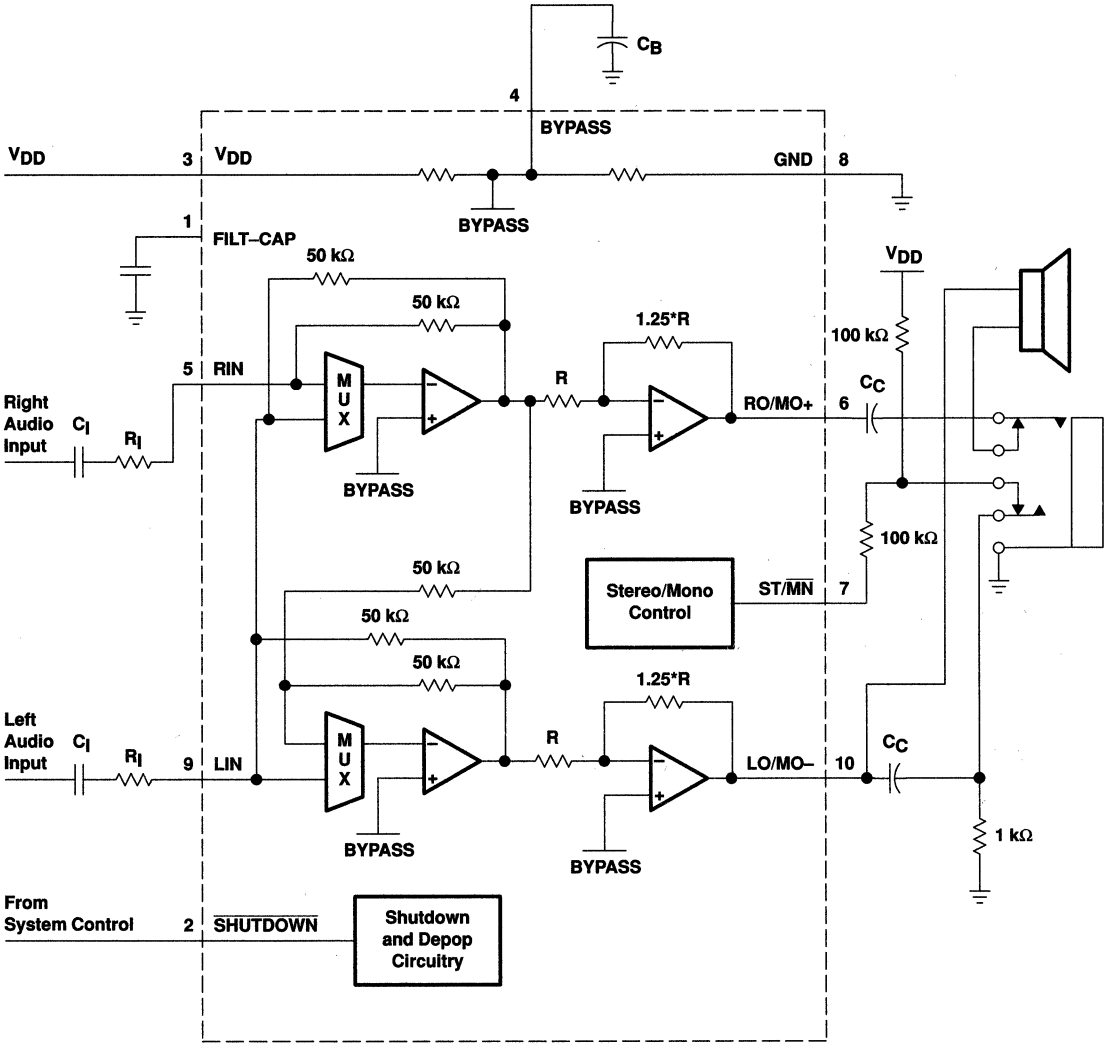


description

The TPA0253 is a 1-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 8-Ω impedance. The mono signal is created by summing left and right inputs internally. The amplifier can be reconfigured on-the-fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0253 can delivery 1-W of power into a 8-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0253 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.


CB
4
BYPASS
VDD
3
VDD
GND
8
BYPASS
1
FILT–CAP
50 kΩ
50 kΩ
1.25*R
VDD
100 kΩ
5
RIN
R
CC
Right
Audio
Input
CI
RI
MUX
RO/MO+
6
BYPASS
BYPASS
100 kΩ
50 kΩ
Stereo/Mono
Control
ST/MN
7
50 kΩ
50 kΩ
1.25*R
Left
Audio
Input
CI
RI
9
LIN
MUX
R
LO/MO–
10
CC
BYPASS
BYPASS
1 kΩ
From
System Control
2
SHUTDOWN
Shutdown
and Depop
Circuitry

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
–40°C to 85°C	TPA0253DGQ	AEL

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0253DGQR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FILT–CAP	1		Terminal used to filter power supply
$\overline{\text{SHUTDOWN}}$	2	I	TTL–compatible shutdown terminal
VDD	3	I	Positive power supply
BYPASS	4	I	Mid–rail bias voltage
RIN	5	I	Right–channel input terminal
RO/MO+	6	O	Right–output in SE mode and mono positive output in BTL mode
ST/$\overline{\text{MN}}$	7	I	Selects between Stereo and Mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
GND	8		Ground terminal
LIN	9	I	Left–channel input terminal
LO/MO–	10	O	Left–output in SE mode and mono negative output in BTL mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{MN}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{SHUTDOWN}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{MN}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{SHUTDOWN}$			0.8	
Operating free-air temperature, T_A			−40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_{IO} = 0.1%,	Gain = 8 dB			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.9 V to 3.1 V,	BTL mode		65		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 3.3 V,	$V_I = V_{DD}$			1	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 3.3 V,	V_I = 0			1	µA
Z_I	Input impedance				50		kΩ
I_{DD}	Supply current				2.7	4	mA
$I_{DD(SD)}$	Supply current, shutdown mode				1	10	µA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω, f = 1 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.1%,	BTL mode,	Gain = 14 dB		300		mW
		THD = 0.1% Gain = 1.9 dB	SE mode,	R_L = 32 Ω		30		
THD + N	Total harmonic distortion plus noise	P_O = 250 mW,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 1.9 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	CB = 0.47 µF	BTL mode		46		dB
				SE mode		68		
V_n	Noise output voltage	CB = 0.47 µF,	f = 20 Hz to 20 kHz	BTL mode		83		μV_{RMS}
				SE mode		33		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_{IO} = 0,	Gain = 8 dB			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V,	BTL mode		62		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V,	$V_I = V_{DD}$			1	μA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V,	V_I = 0			1	μA
Z_I	Input impedance				50		kΩ
I_{DD}	Supply current				3.2	4.8	mA
$I_{DD(SD)}$	Supply current, shutdown mode				1	10	μA

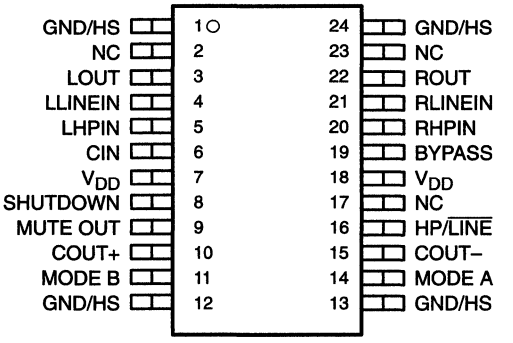
operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, f = 1 kHz (unless otherwise noted)

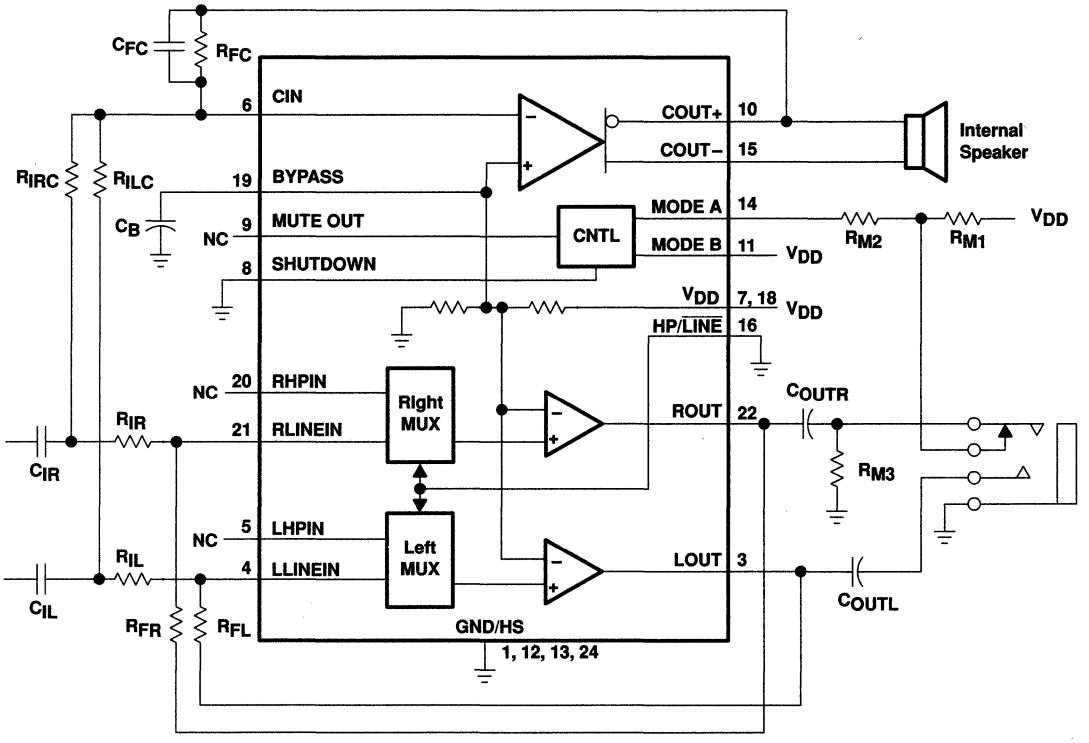
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.1%,	BTL mode			1		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		85		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz			0.33%		
B_{OM}	Maximum output power bandwidth	Gain = 8 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	CB = 0.47 μF	BTL mode		46		dB
				SE mode		60		
V_n	Noise output voltage	CB = 0.47 μF,	f = 20 Hz to 20 kHz	BTL mode		85		μV_{RMS}
				SE mode		34		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

- **Desktop Computer Amplifier Solution**
  - **1.75-W Bridge Tied Load (BTL) Center Channel**
  - **500-mW L/R Single-Ended Channels**
- **Low Distortion Output**
  - **< 0.05% THD+N at Full Power**
- **Full 3.3-V and 5-V Specifications**
- **Surface-Mount Power Package 24-Pin TSSOP**
- **L/R Input MUX Feature**
- **Shutdown Control . . . I_{DD} = 5 μA**

PWP PACKAGE
(TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description

The TPA0103 is a 3-channel audio power amplifier in a 24-pin TSSOP thermal package primarily targeted at desktop PC or notebook applications. The left/right (L/R) channel outputs are single ended (SE) and capable of delivering 500 mW of continuous RMS power per channel into 4-Ω loads. The center channel output is a bridged tied load (BTL) configuration for delivering maximum output power from PC power supplies. Combining the SE line drivers and high power center channel amplifiers in a single TSSOP package simplifies design and frees up board space for other features. Full power distortion levels of less than 0.25% THD+N into 4-Ω loads from a 5-V supply voltage are typical. Low-voltage application are also well served by the TPA0103 providing 800 mW to the center channel into 4-Ω loads with a 3.3-V supply voltage.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10. A two channel input MUX circuit is integrated on the L/R channel inputs to allow two sets of stereo inputs to the amplifier. In the typical application, the center channel amplifier is driven from a mix of the L/R inputs to produce a monaural representation of the stereo signal. The center channel amplifier can be shut down independently of the L/R output for speaker muting in headphone applications. The TPA0103 also features a full shutdown function for power sensitive applications holding the bias current to 5 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of less than 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0103 to operate at full power at ambient temperature of up to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP† (PWP)
–40°C to 85°C	TPA0103PWP

† The PWP package is available in left-ended tape and reel only (e.g., TPA0103PWPLE).

Terminal Functions

<table>
<tr><th colspan="2">TERMINAL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><th>NAME</th><th>NO.</th><th></th><th></th></tr>
<tr><td>BYPASS</td><td>19</td><td></td><td>Bypass. BYPASS is a tap to the voltage divider for the internal mid-supply bias.</td></tr>
<tr><td>CIN</td><td>6</td><td>I</td><td>Center channel input</td></tr>
<tr><td>COUT+</td><td>10</td><td>O</td><td>Center channel + output. COUT+ is in an active or high-impedance state unless the device is in a mute state when the MODE A terminal (14) is high and the MODE B terminal (11) is low.</td></tr>
<tr><td>COUT–</td><td>15</td><td>O</td><td>Center channel – output. COUT– is in an active or high-impedance state unless the device is in a mute state when the MODE A terminal (14) is high and the MODE B terminal (11) is low.</td></tr>
<tr><td>GND/HS</td><td>1, 12, 13, 24</td><td></td><td>Ground. GND/HS is the ground connection for circuitry, directly connected to thermal pad.</td></tr>
<tr><td>MODE A, MODE B</td><td>14, 11</td><td>I</td><td>Mode select. MODE A and MODE B determine the output modes of the TPA0103.
<table>
<tr><th>TERMINAL</th><th>3 CHANNEL</th><th>MUTE</th><th>CENTER ONLY</th><th>L/R ONLY</th></tr>
<tr><td>MODE A</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>MODE B</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>HP/$\overline{\text{LINE}}$</td><td>16</td><td>I</td><td>Input MUX control input, hold high to select (L/R) HPIN (5, 20), hold low to select (L/R) LINEIN (4, 21). HP/$\overline{\text{LINE}}$ is normally connected to ground when inputs are connected to (L/R) LINEIN.</td></tr>
<tr><td>LHPIN</td><td>5</td><td>I</td><td>Left channel headphone input, selected when the HP/$\overline{\text{LINE}}$ terminal (16) is held high</td></tr>
<tr><td>LLINEIN</td><td>4</td><td>I</td><td>Left channel line input, selected when the HP/$\overline{\text{LINE}}$ terminal (16) is held low</td></tr>
<tr><td>LOUT</td><td>3</td><td>O</td><td>Left channel output. LOUT is active when the MODE A terminal (14) is low and the MODE B terminal (11) is don't care.</td></tr>
<tr><td>MUTE OUT</td><td>9</td><td>O</td><td>When the MODE A terminal (14) is high and the MODE B terminal (11) is low, MUTE OUT is high and the device is in a mute state. Otherwise MUTE OUT is low.</td></tr>
<tr><td>NC</td><td>2, 17, 23</td><td></td><td>No internal connection</td></tr>
<tr><td>RHPIN</td><td>20</td><td>I</td><td>Right channel headphone input, selected when the HP/$\overline{\text{LINE}}$ terminal (16) is held high</td></tr>
<tr><td>RLINEIN</td><td>21</td><td>I</td><td>Right channel line input, selected when the HP/$\overline{\text{LINE}}$ terminal (16) is held low</td></tr>
<tr><td>ROUT</td><td>22</td><td>O</td><td>Right channel output. ROUT is active when the MODE A terminal (14) is low and the MODE B terminal (11) is don't care.</td></tr>
<tr><td>SHUTDOWN</td><td>8</td><td>I</td><td>Places entire IC in shutdown mode when held high, $I_{DD} = 5\ \mu A$</td></tr>
<tr><td>V_{DD}</td><td>7, 18</td><td>I</td><td>Supply voltage input. The V_{DD} terminals must be connected together.</td></tr>
</table>

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Continuous output current (COUT+, COUT–, LOUT, ROUT) ..... 2 A
Continuous total power dissipation ..... internally limited
Operating virtual junction temperature range, T_J ..... –40°C to 150°C
Operating virtual case temperature range, T_C ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP‡	2.7 W	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}		3	5	5.5	V
Operating junction temperature, T_J			125		°C

dc electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS			NOM	TYP	MAX	UNIT
I_{DD}	Supply current	$V_{DD} = 5$ V	3 Channel			19	25	mA
			L and R or Center only			9	15	mA
		$V_{DD} = 3.3$ V	3 Channel			13	20	mA
			L and R or Center only			3	10	mA
V_{OO}	Output offset voltage (measured differentially)	$V_{DD} = 5$ V,	Gain = 2,	See Note 1		5	35	mV
$I_{DD(MUTE)}$	Supply current in mute mode	$V_{DD} = 5$ V				800		µA
$I_{DD(SD)}$	I_{DD} in shutdown	$V_{DD} = 5$ V				5	15	µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power (each channel) (see Note 2)	THD = 0.2%,	BTL,	Center channel		1.75		W
		THD = 1%,	BTL,	Center channel		2.1		
		THD = 0.2%,	SE,	L/R channels		535		mW
		THD = 1%,	SE,	L/R channels		575		
THD+N	Total harmonic distortion plus noise	P_O = 1.5 W,	f = 20 to 20 kHz			0.25%		
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %			>20		kHz
	Phase margin	Open loop				85		°
	Supply ripple rejection ratio	f = 1 kHz	Center channel			80		dB
			L/R channels			58		
		f = 20 – 20 kHz	Center channel			60		
			L/R channels			30		
	Mute attenuation					85		dB
	Channel-to-channel output separation	f = 1 kHz				95		dB
	Line/HP input separation					100		dB
Z_I	Input impedance					2		MΩ
	Signal-to-noise ratio	V_O = 1 V(rms)	BTL,	Center channel		94		dB
			SE,	L/R channels		100		
V_n	Output noise voltage	BTL,	Center channel			20		μV(rms)
		SE,	L/R channels			9		

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power (each channel) (see Note 2)	THD = 0.2%	BTL,	Center channel		800		mW
		THD = 1%	BTL,	Center channel		850		
		THD = 0.2%,	SE,	L/R channels		215		
		THD = 1%,	SE,	L/R channels		235		
THD+N	Total harmonic distortion plus noise	P_O = 750 mW,	f = 20 to 20 kHz			0.8%		
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %			>20		kHz
	Phase margin	Open loop				85		°
	Supply ripple rejection ratio	f = 1 kHz	Center channel			70		dB
			L/R channels			62		
		f = 20 – 20 kHz	Center channel			55		
			L/R channels			30		
	Mute attenuation					85		dB
	Channel-to-channel output separation	f = 1 kHz				95		dB
	Line/HP input separation					100		dB
Z_I	Input impedance					2		MΩ
	Signal-to-noise ratio	V_O = 1 V(rms)	BTL,	Center channel		93		dB
			SE,	L/R channels		100		
V_n	Output noise voltage	BTL,	Center channel			21		μV(rms)
		SE,	L/R channels			10		

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

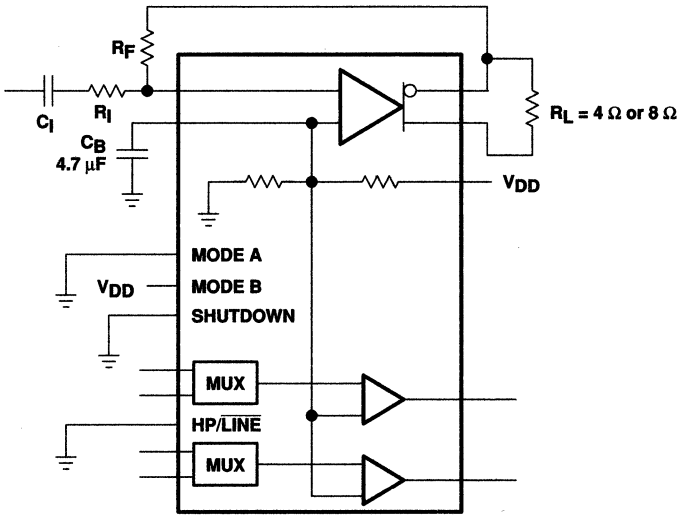


Figure 1. BTL Test Circuit

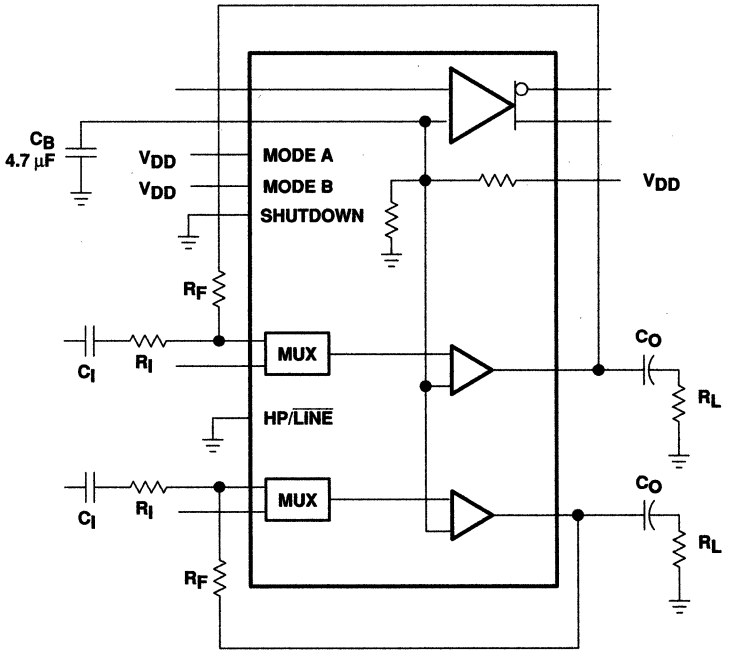


Figure 2. SE Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Output power	3, 4, 7, 10–12, 15, 18, 21, 24, 27, 30, 33, 36
		vs Frequency	5, 6, 8, 9, 13, 14, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35
V_n	Output noise voltage	vs Frequency	37,38
	Supply ripple rejection ratio	vs Frequency	39, 40
	Crosstalk	vs Frequency	41, 42
	Open loop response	vs Frequency	43, 44
	Closed loop response	vs Frequency	45 – 48
I_{DD}	Supply current	vs Supply voltage	49
P_O	Output power	vs Supply voltage vs Load resistance	50, 51 52, 53
P_D	Power dissipation	vs Output power	54 – 57

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

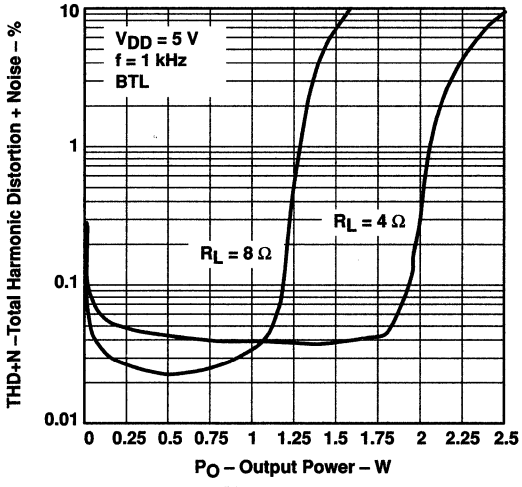


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

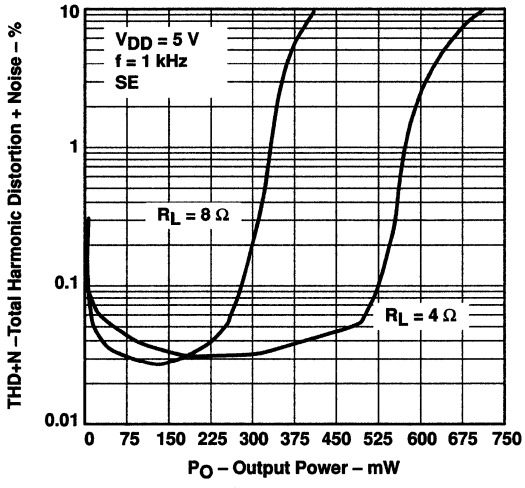


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

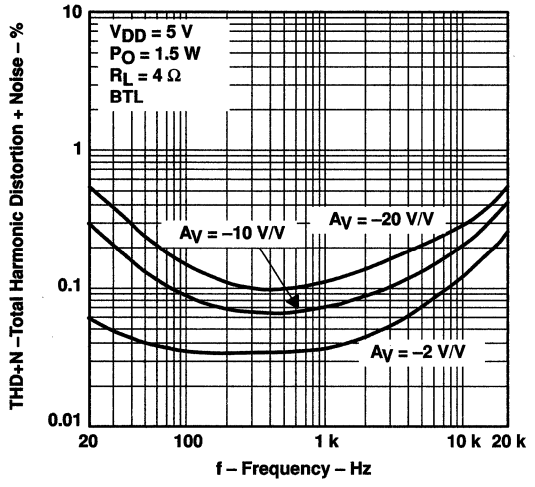


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

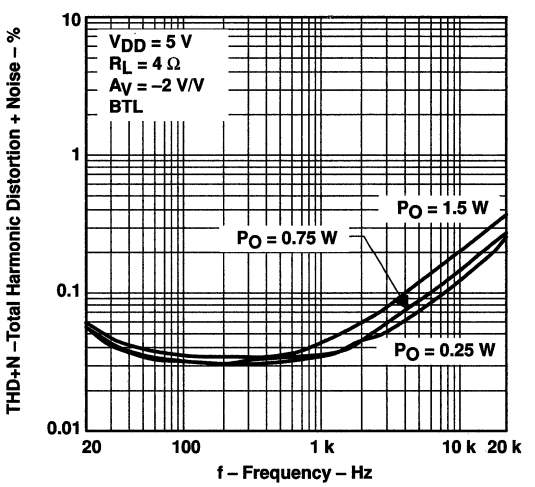


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

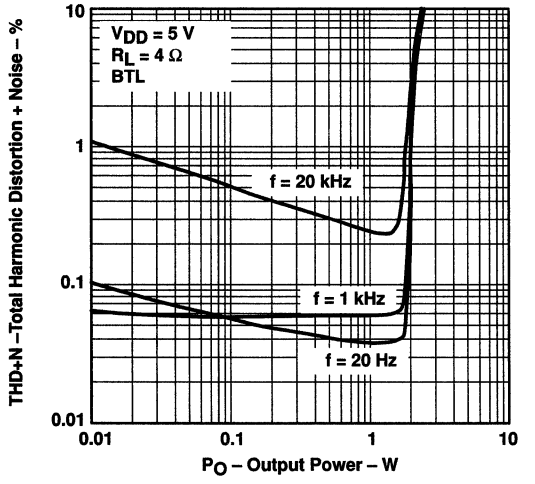


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

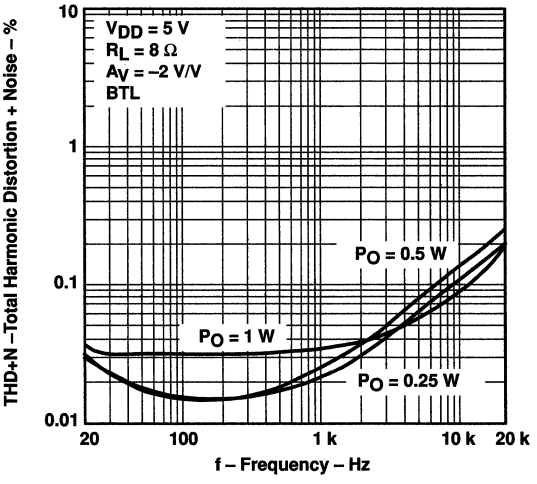


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

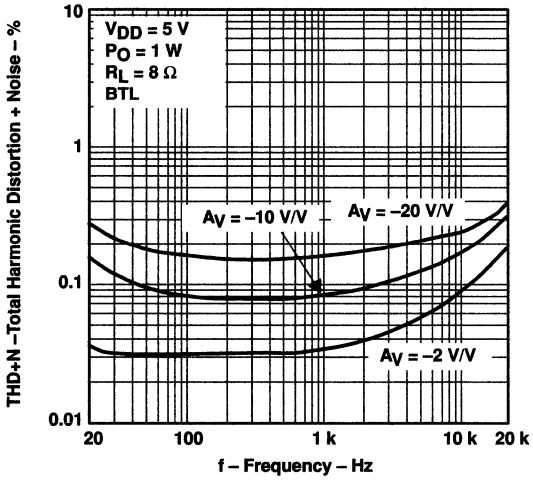


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

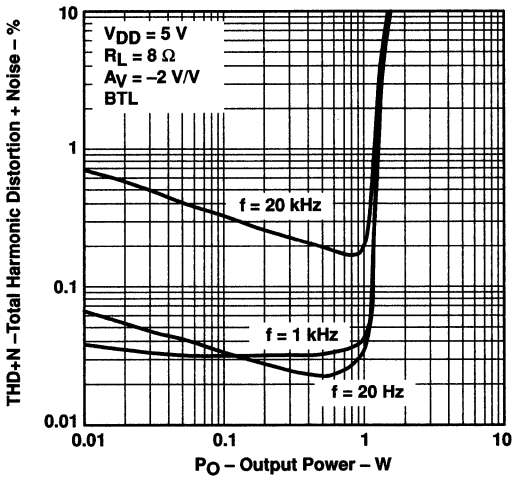


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

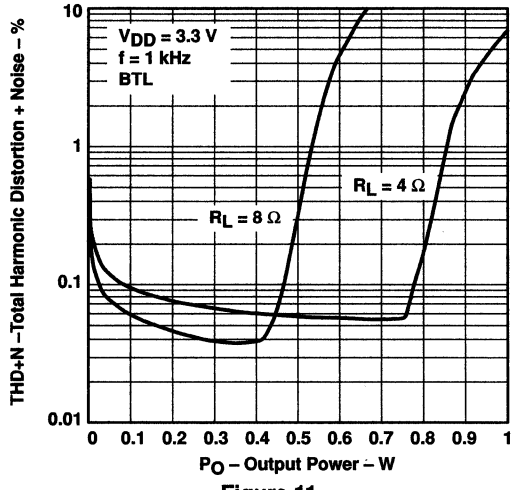


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

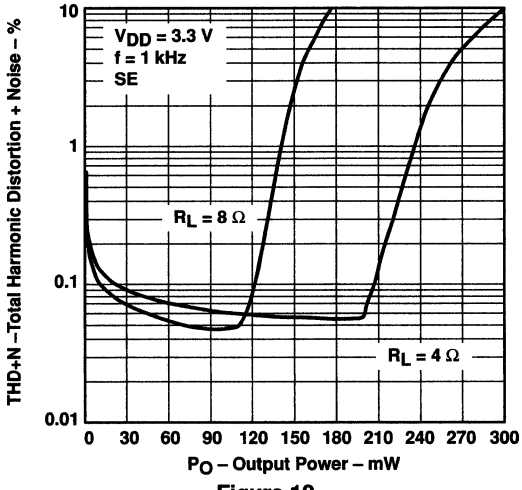


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

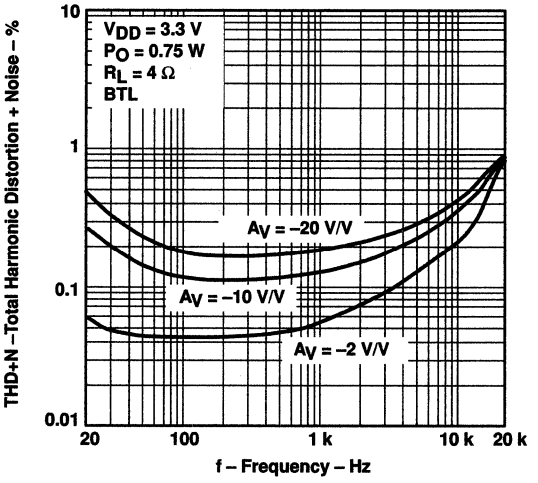


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

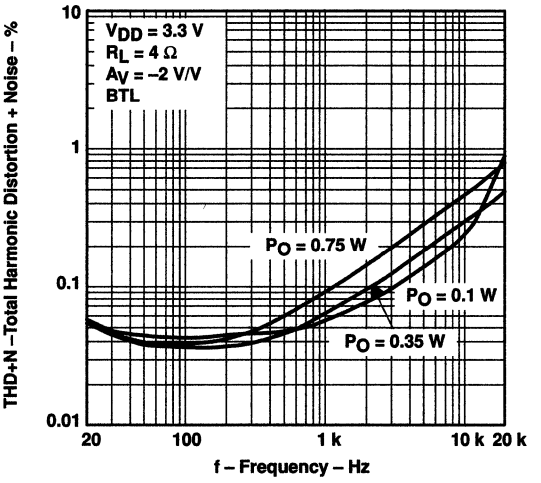


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

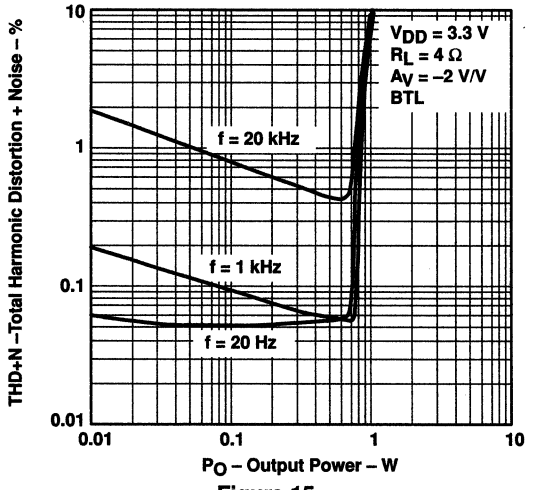


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

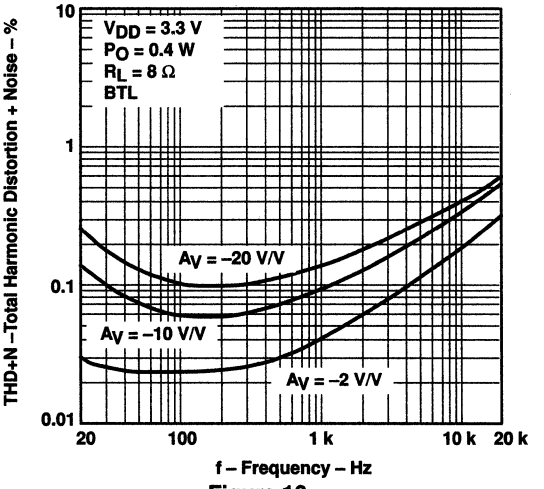


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

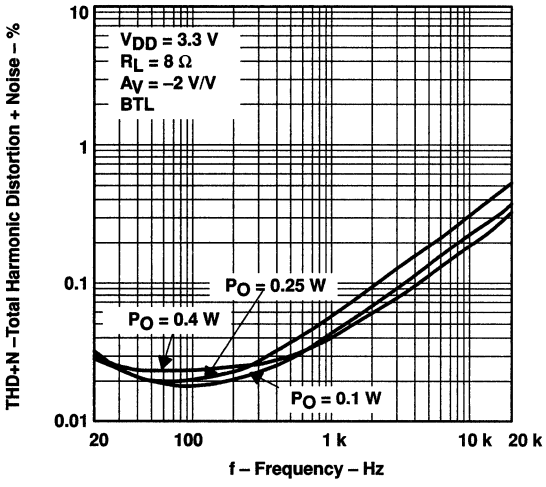


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

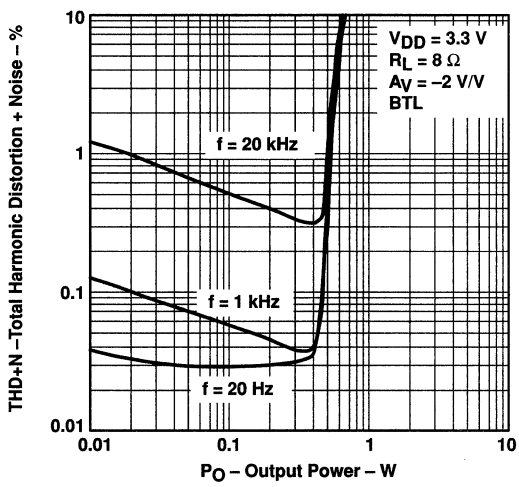


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

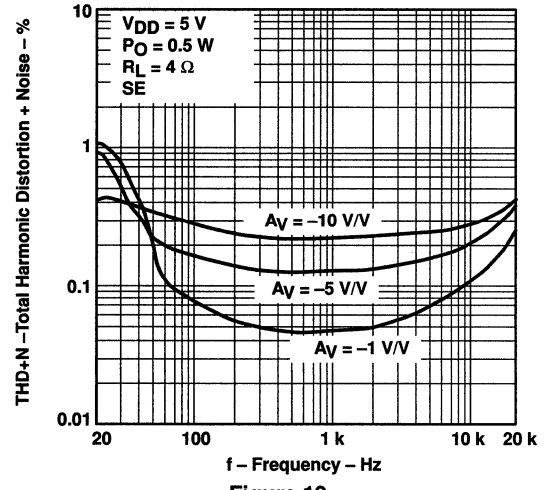


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

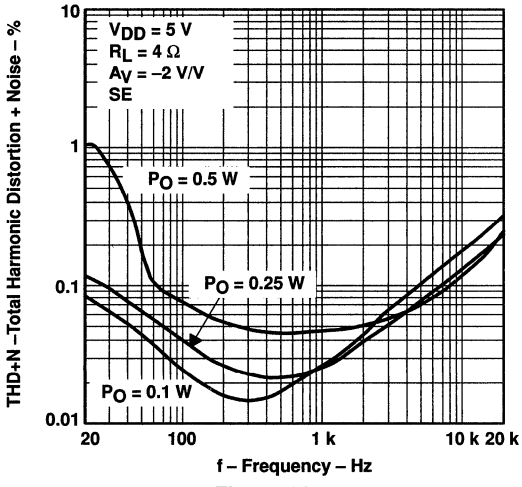


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

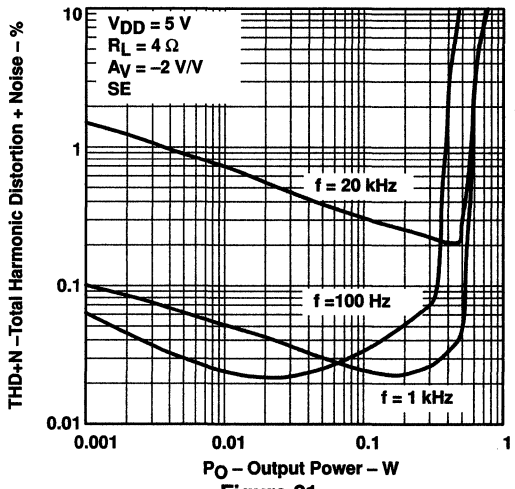


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

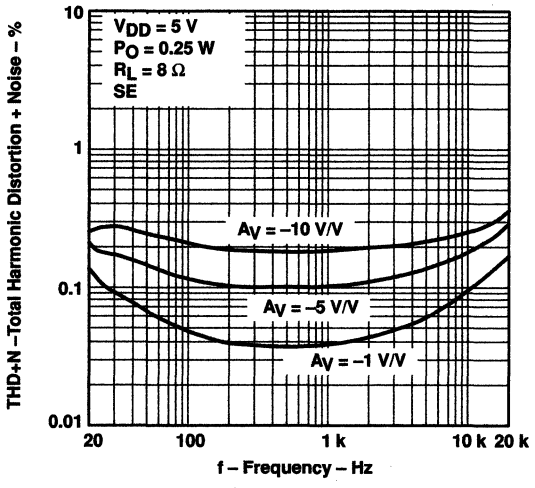


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

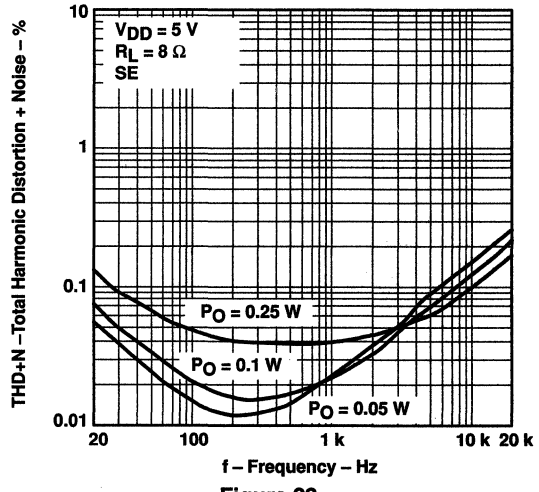


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

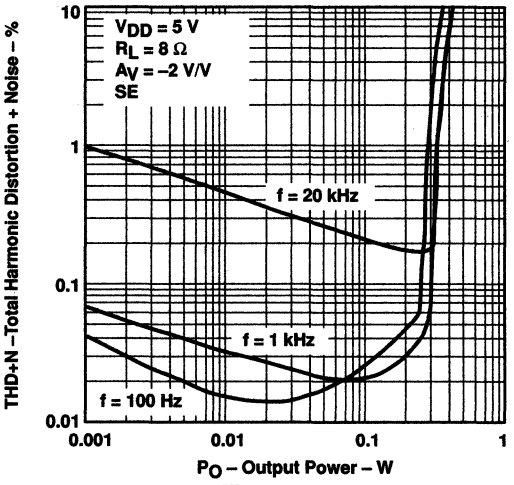


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

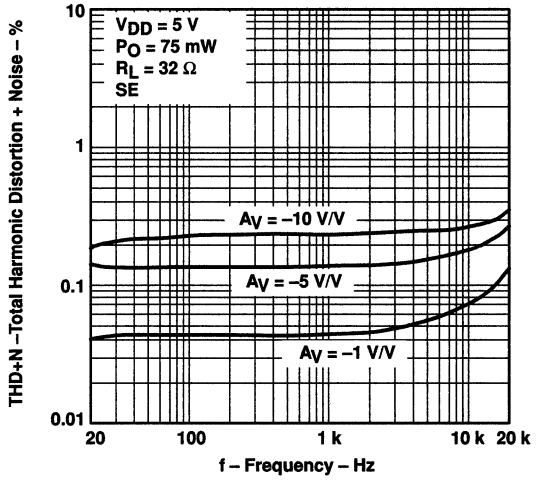


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

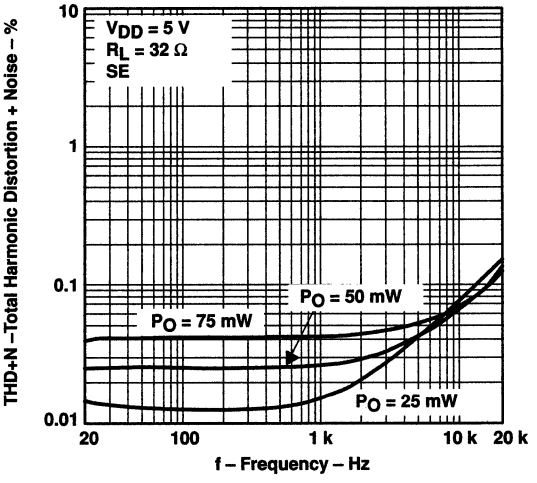


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

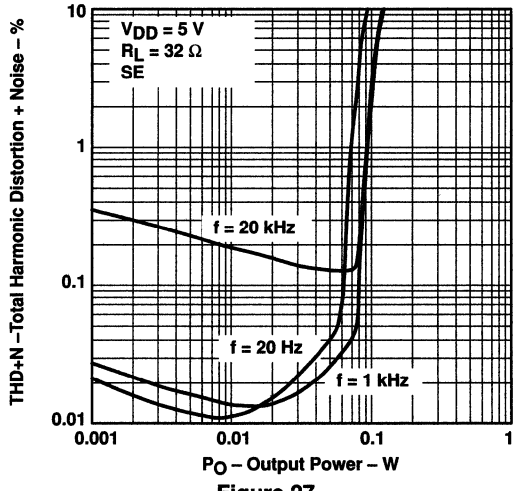


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

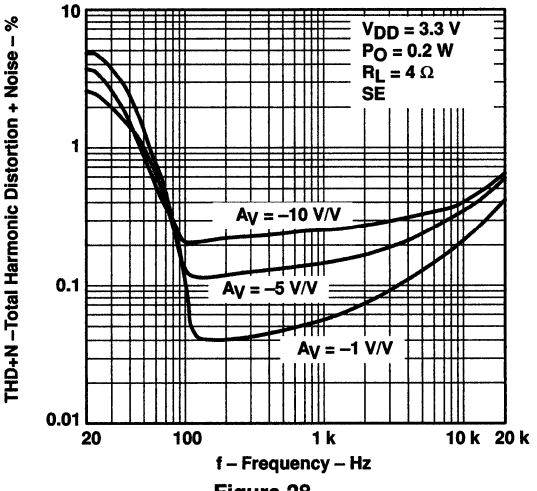


Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

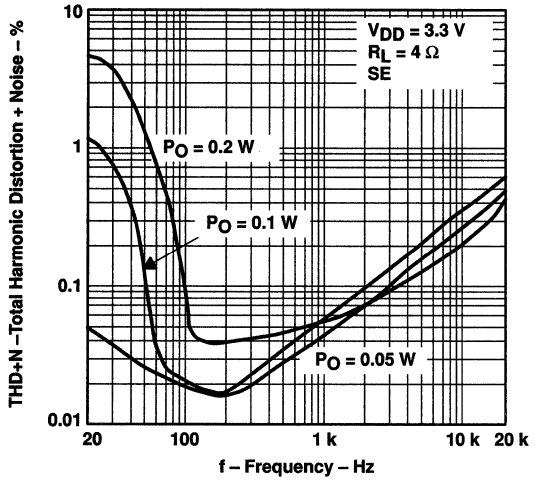


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

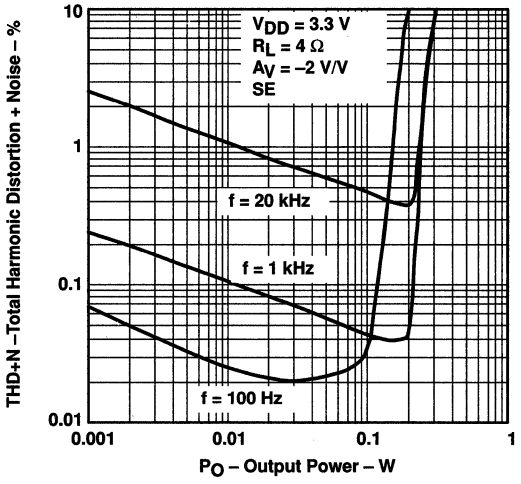


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

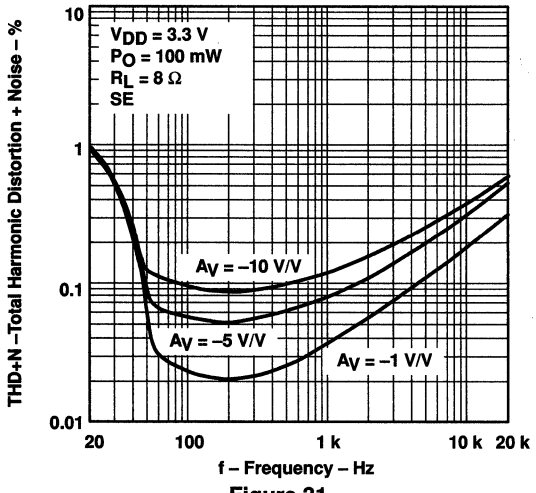


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

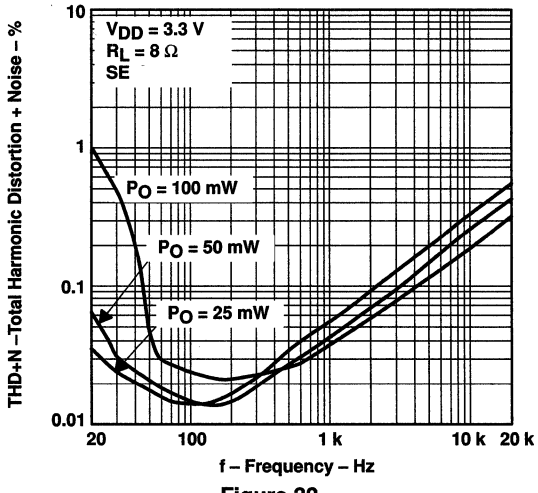


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

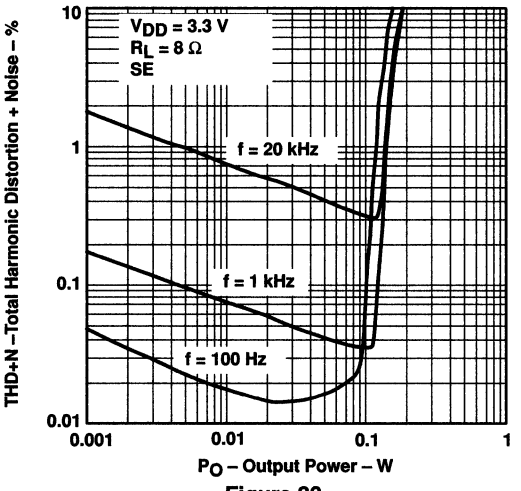


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

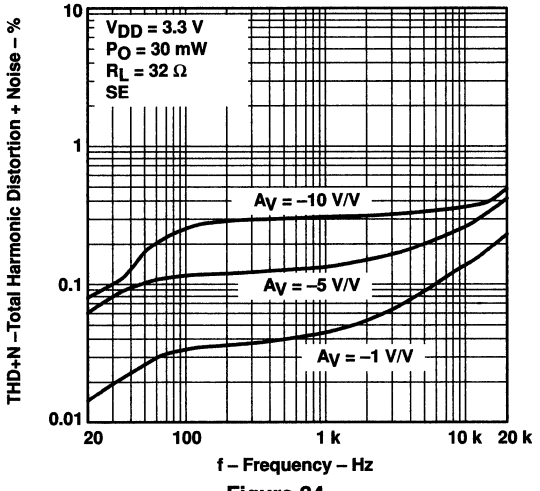


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

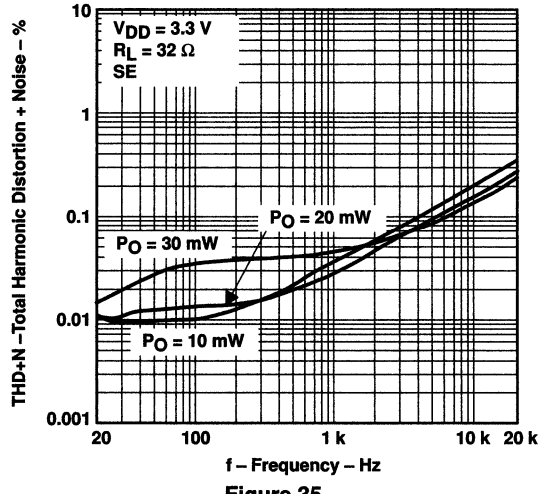


Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

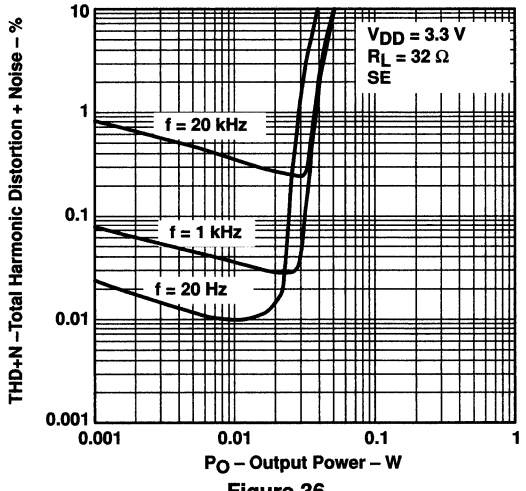


Figure 36

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

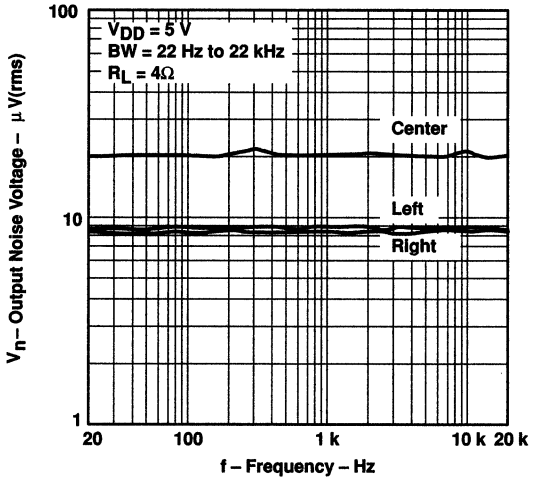


Figure 37

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

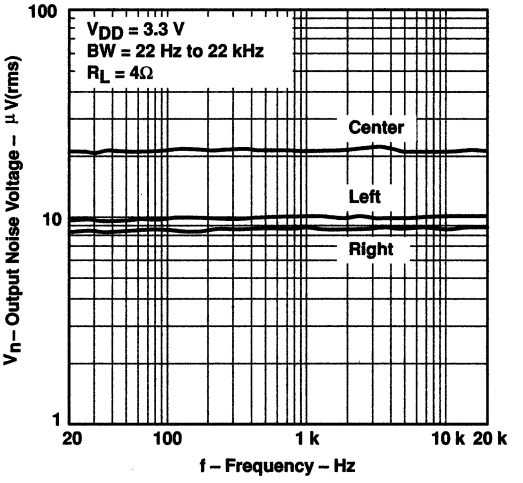


Figure 38

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

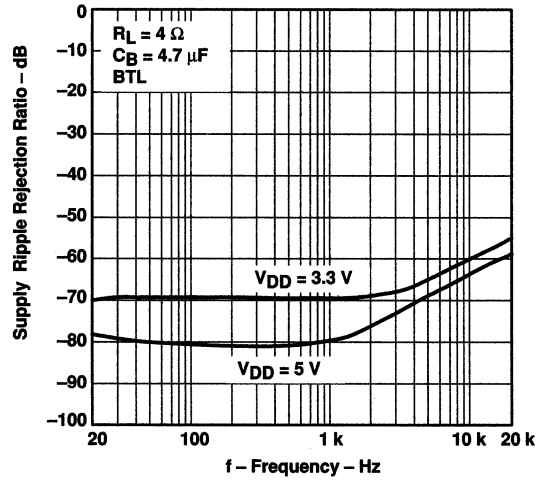


Figure 39

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

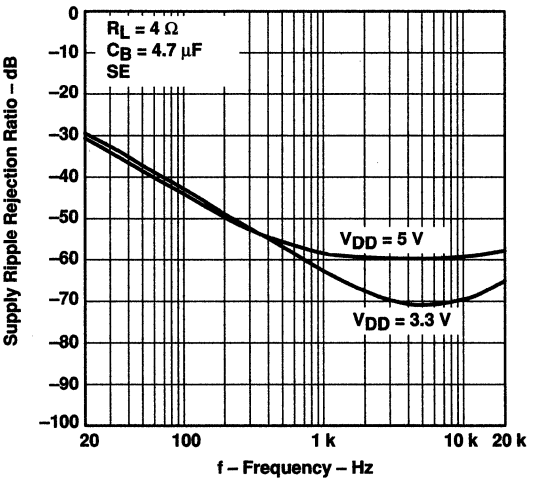


Figure 40

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

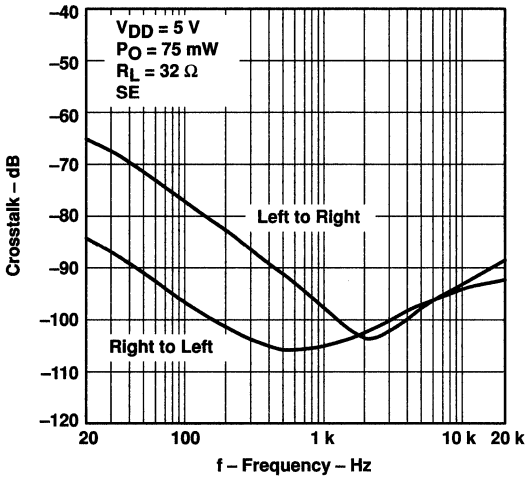


Figure 41

CROSSTALK vs FREQUENCY

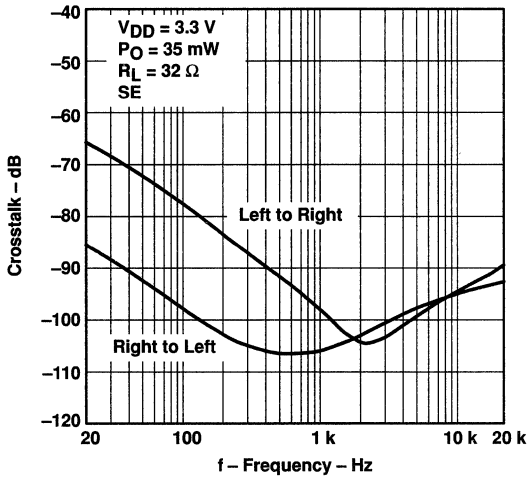


Figure 42

OPEN LOOP RESPONSE

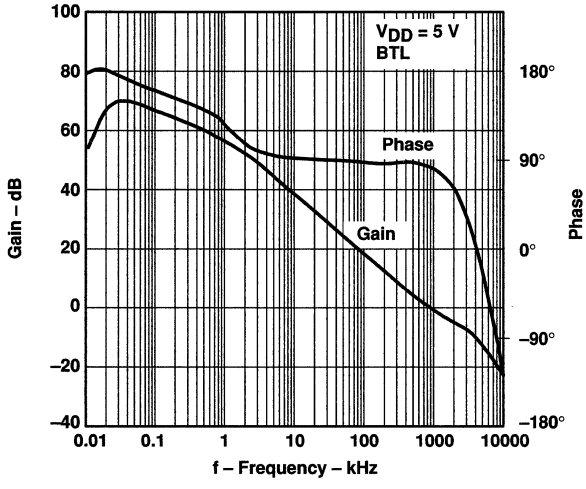


Figure 43

TYPICAL CHARACTERISTICS

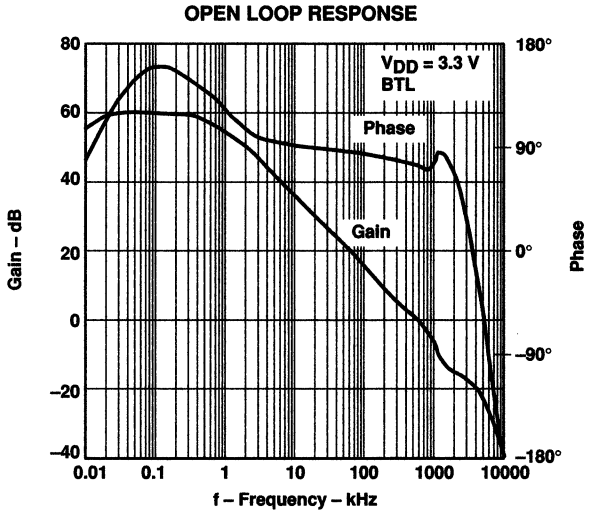


Figure 44

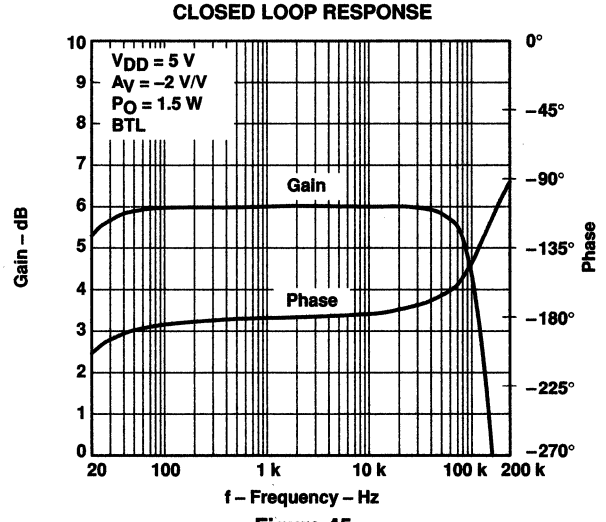


Figure 45

TYPICAL CHARACTERISTICS

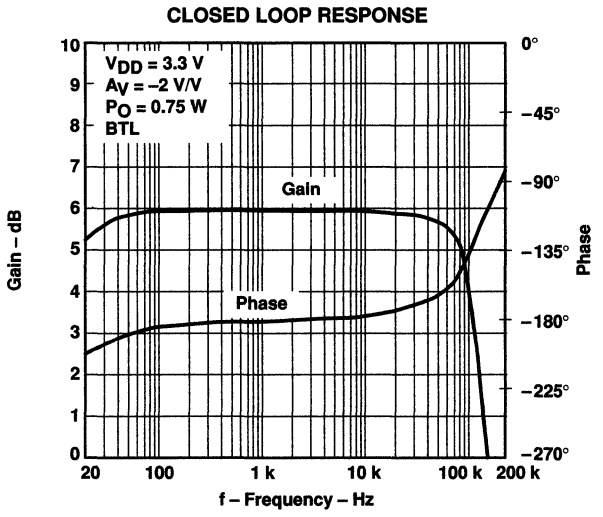


Figure 46

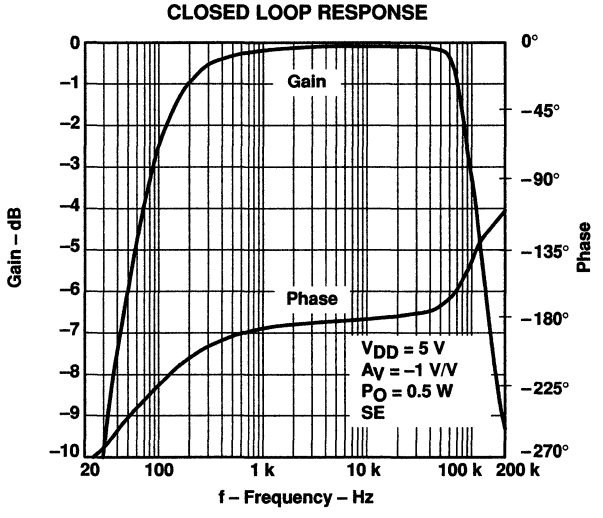


Figure 47

TYPICAL CHARACTERISTICS

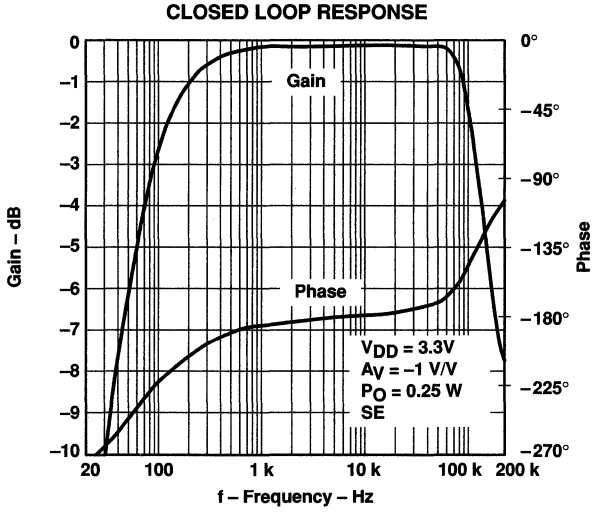


Figure 48

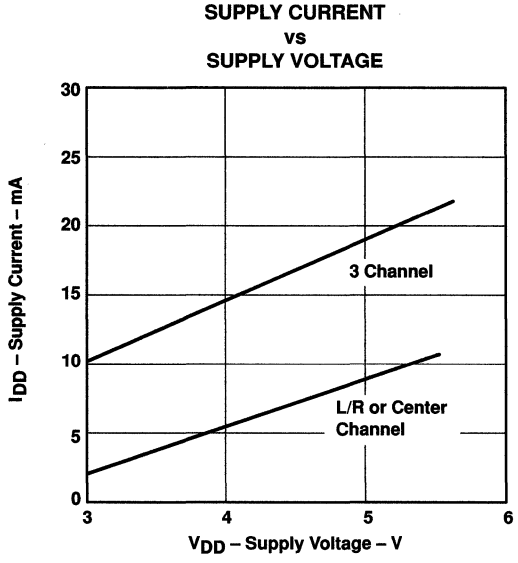


Figure 49

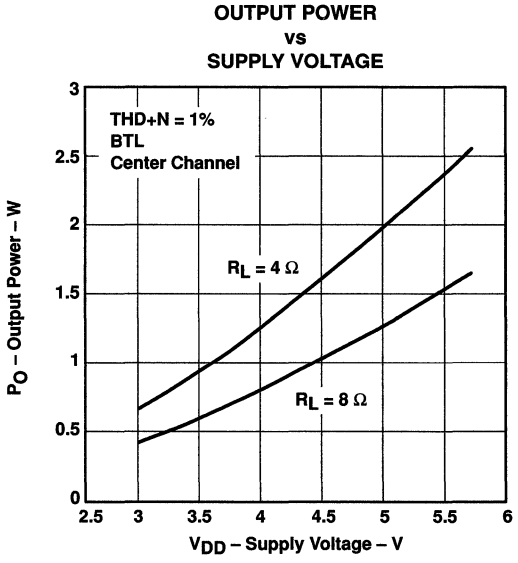


Figure 50

TYPICAL CHARACTERISTICS

OUTPUT POWER vs SUPPLY VOLTAGE

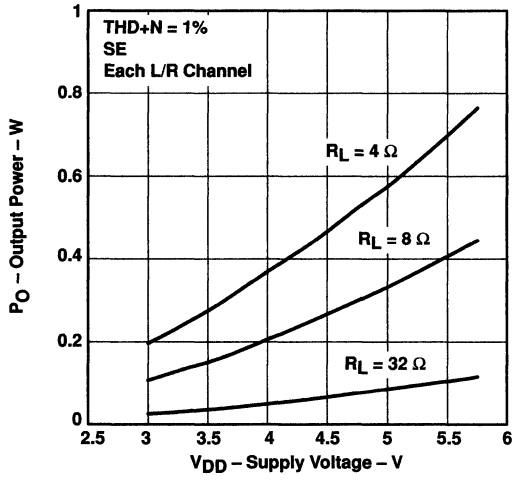


Figure 51

OUTPUT POWER vs LOAD RESISTANCE

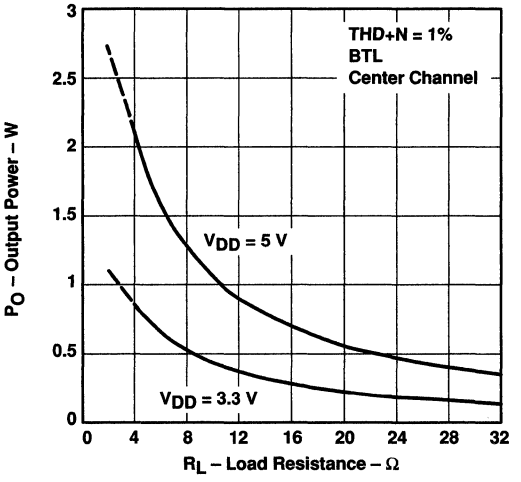


Figure 52

OUTPUT POWER vs LOAD RESISTANCE

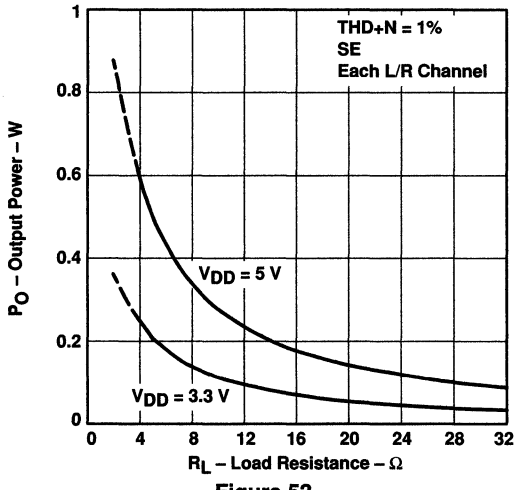


Figure 53

POWER DISSIPATION vs OUTPUT POWER

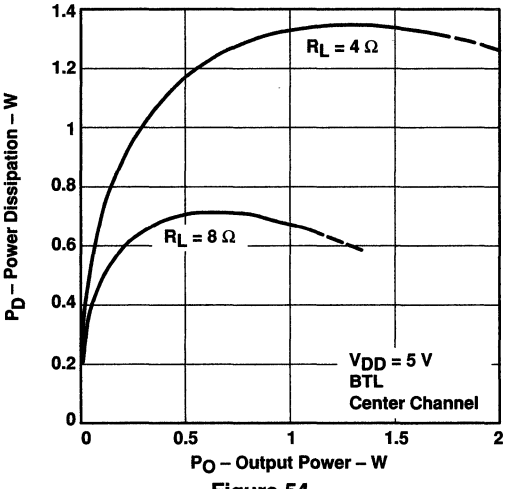


Figure 54

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
OUTPUT POWER

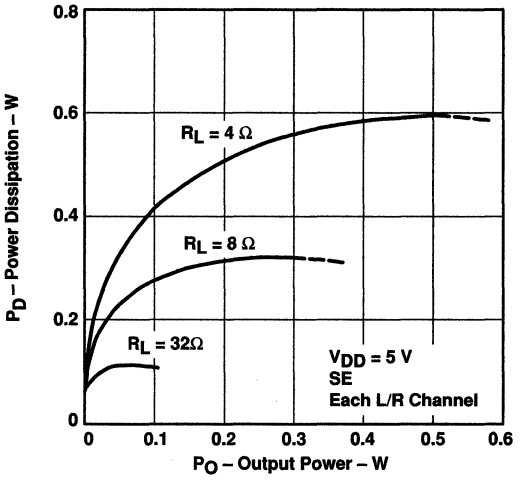


Figure 55

POWER DISSIPATION
vs
OUTPUT POWER

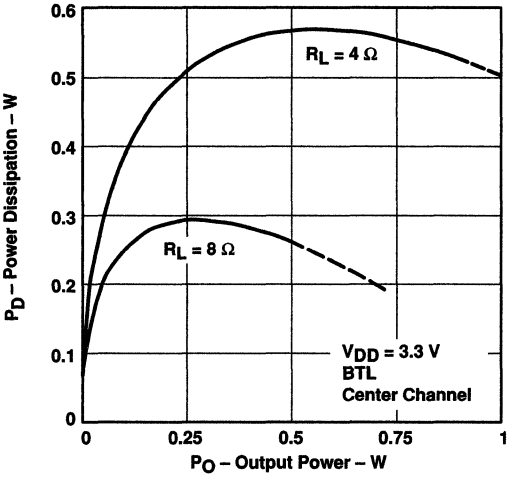


Figure 56

POWER DISSIPATION
vs
OUTPUT POWER

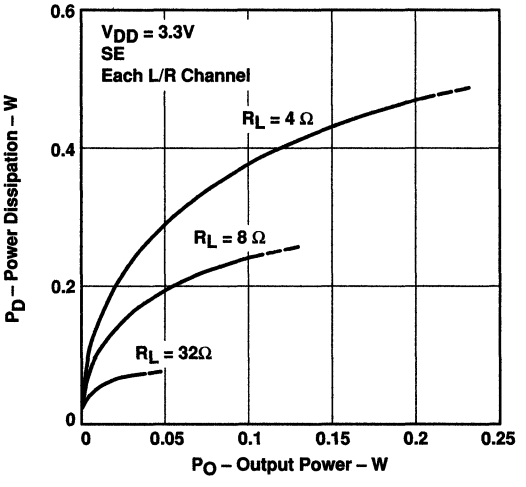


Figure 57

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

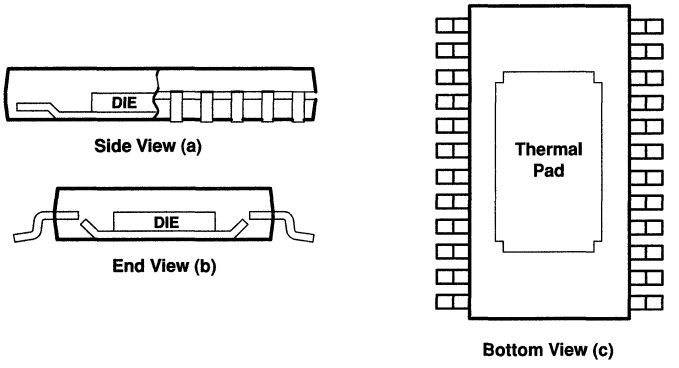


Figure 58. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0103 center-channel BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

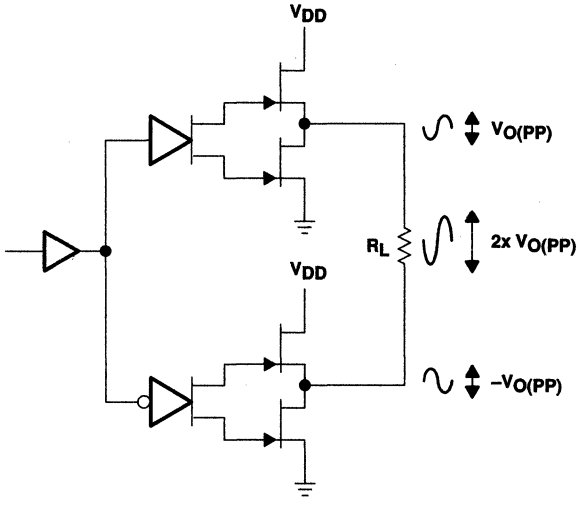


Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration of the L/R channels as shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

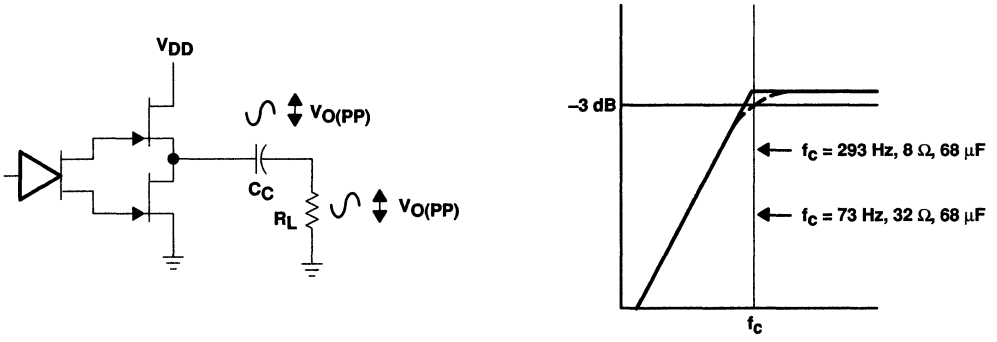


Figure 60. Single-Ended Configuration and Frequency Response

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).

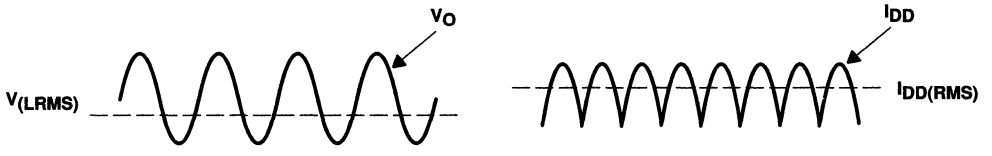


Figure 61. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

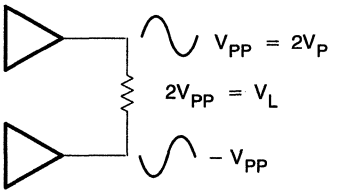
Where:

$$P_{L(BTL)} = \frac{V_L\text{rms}^2}{R_L} = \frac{V_{PP}^2}{2R_L}, \quad V_{PP} = \sqrt{P_L R_L 2}$$

$$V_L\text{rms(BTL)} = \frac{V_{PP}}{2\sqrt{2}} \times 2 = \frac{V_{PP}}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, V_{PP}}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{V_{PP}}{\pi\, R_L}$$



$$\text{Efficiency of a BTE Configuration} = \frac{P_L}{P_{SUP}} = \frac{V_{PP}^2}{2R_L} \times \frac{\pi\, R_L}{V_{DD}V_{PP}} = \frac{V_{PP}\pi}{2V_{DD}} = \frac{\pi\sqrt{2P_L R_L}}{2V_{DD}} \tag{4}$$

Equation 4 can also be used for SE operations.

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. As the numerator values of R_L and P_L decrease, efficiency decreases.

APPLICATION INFORMATION

For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0103 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to chose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 62 and Figure 63 are a schematic diagrams of typical computer application circuits.

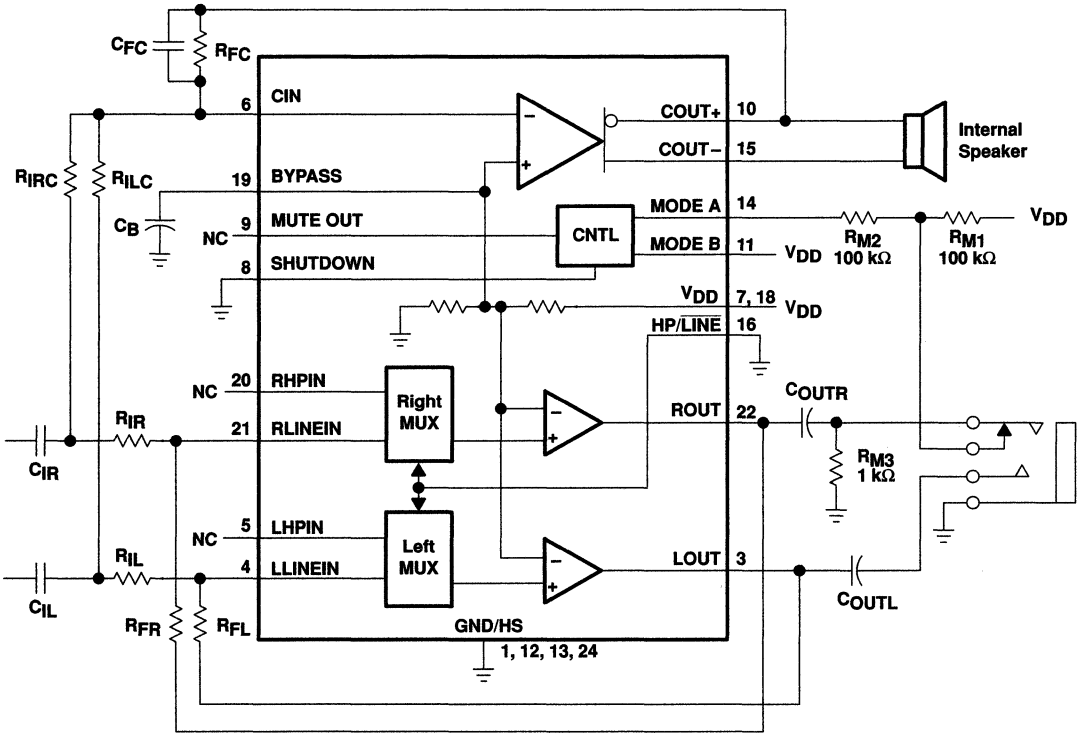
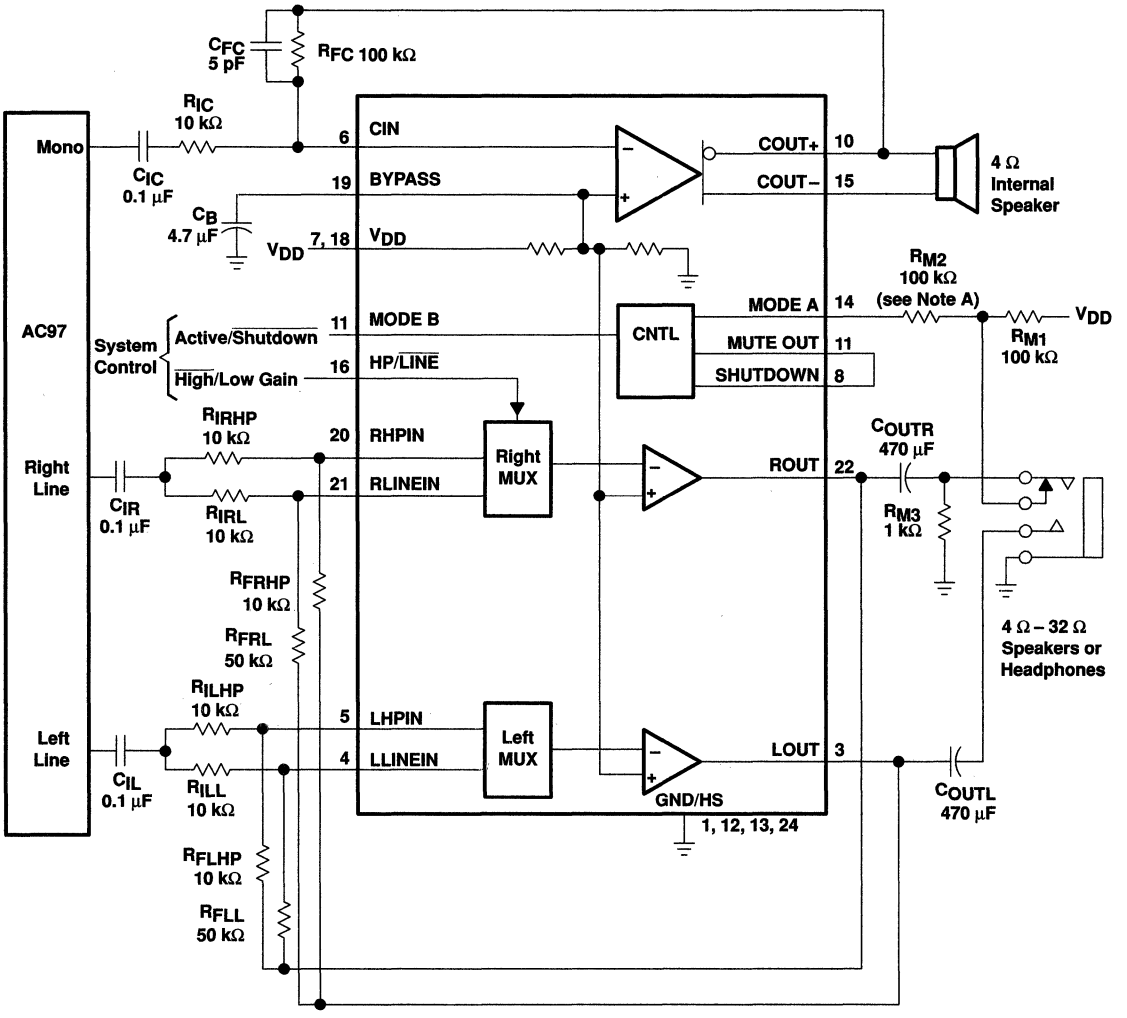


Figure 62. TPA0103 Minimum Configuration Application Circuit

APPLICATION INFORMATION



NOTE A. This connection is for ultralow current in shutdown mode.

Figure 63. TPA0103 Full Configuration Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0103 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 6. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{6}$$

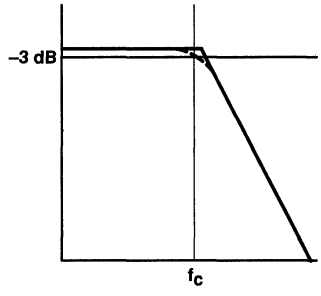
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0103 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 7.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{7}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 8.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{8}$$



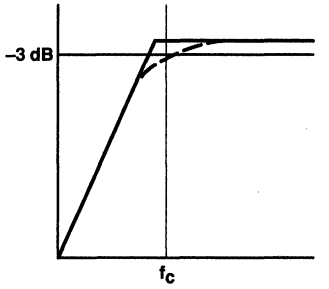
For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 9.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (9)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 10.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (10)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0103 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 11 should be maintained.

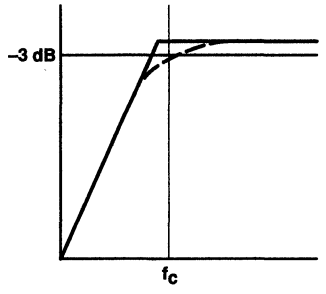
$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \tag{11}$$

As an example, consider a circuit where C_B is 0.1 μF, C_I is 0.22 μF and R_I is 10 kΩ. Inserting these values into the equation 10 we get 400 ≤ 454 which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 12.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \tag{12}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the relationship shown in equation 13.

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{13}$$

mode control resistor network, R_{M1}, R_{M2}, R_{M3}

Using a readily available 1/8-in. (3.5-mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider (see Figure 64) pulls the MODE A input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the MODE A input is pulled high. When the input goes high, the center BTL amplifier is shutdown causing the speaker to mute. The SE amplifiers then drive through the output capacitors (C_O) into the headphone jack.

Input MUX operation

The HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 64). The primary function of the MUX is to allow different gain settings for different types of audio loads. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{Gain}_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \tag{14}$$

If, for example $R_{I(HP)}$ = 20 kΩ and $R_{F(HP)}$ = 20 kΩ then SE $\text{Gain}_{(HP)}$ = –1

$$\text{Gain}_{(LINE)} = -\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \tag{15}$$

If, for example $R_{I(LINE)}$ = 10 kΩ and $R_{F(LINE)}$ = 100 kΩ then $\text{Gain}_{(LINE)}$ = –10

APPLICATION INFORMATION

Input MUX operation (continued)

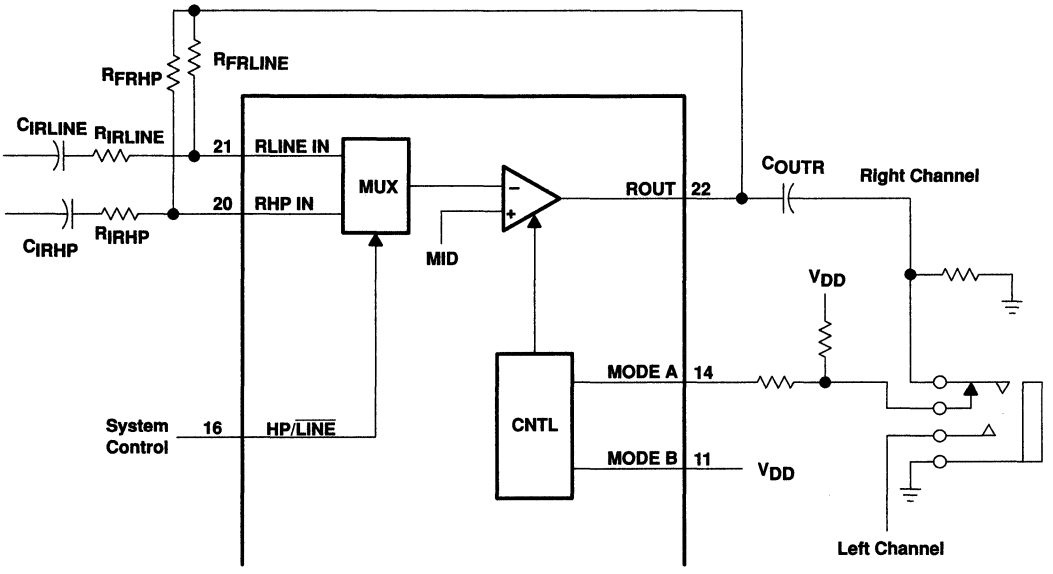


Figure 64. TPA0103 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important.

mute and shutdown modes

The TPA0103 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} = 5\ \mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces I_{DD} <1 mA.

APPLICATION INFORMATION

mute and shutdown modes (continued)

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
MODE A	HP/$\overline{\text{LINE}}$	MODE B	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	3 Channel
X	X	—	High	High	X	Mute
X	X	High	Low	High	X	Mute
Low	High	Low	Low	Low	L/R HP	3 Channel
High	Low	Low	Low	High	L/R Line	Mute
High	High	Low	Low	High	L/R HP	Mute
Low	Low	High	Low	Low	L/R Line	Center BTL
Low	High	High	Low	Low	L/R HP	Center BTL
High	Low	High	Low	Low	L/R Line	L/R SE
High	High	High	Low	Low	L/R HP	L/R SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0103 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0103 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0103 data sheet, one can see that when the TPA0103 is operating from a 5-V supply into a 4-Ω speaker that 2 W RMS levels are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right)$$
$$= 10\text{Log}\left(\frac{2}{1}\right)$$
$$= 3\text{ dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$3\text{ dB} - 15\text{ dB} = -12\text{ dB (15 dB headroom)}$$

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
$$P_W = -12\text{ dB} = 63\text{ mW (15 dB headroom)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 1.5 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA0103 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0103 Power Rating, 5-V, 4-Ω, Three Channel

CONFIGURATION	HEADROOM†	POWER DISSIPATION			T_A (MAX)‡	
		2 × L/R + CENTER = TOTAL			35°C/W	25°C/W
Center only, P_O = 2 W max	0 dB	0	1.25 W	1.25 W	81°C	93°C
	15 dB	0	0.6 W	0.6 W	104°C	110°C
L/R only, P_O = 500 mW max	0 dB	0.6 W	0	1.2 W	83°C	95°C
	15 dB	0.2 W	0	0.4 W	111°C	115°C
Center, P_O = 2 W max and L/R , P_O = 500 mW max	0 dB	0.6 W	1.25 W	2.45 W	39°C	63°C
	15 dB	0.2 W	0.6 W	1 W	90°C	100°C

† The 2 W max at 0 dB is a maximum level tone that is very loud. 15 dB is a typical headroom requirement for music.
‡ This parameter is based on a maximum junction temperature (T_J) of 125°C.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP‡	2.8 W	22.1 mW/°C	1.8 W	1.4 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 LFM and 300 LFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 22.1 mW/°C and 53.7 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

For 0 LFM:

$$= \frac{1}{22.1 \text{ mW/°C}}$$

$$= 45°C/W$$

For 300 LFM:

$$= \frac{1}{53.7 \text{ mW/°C}}$$

$$= 18°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for the two SE channels and added to the center channel dissipation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0103 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D$$

$$= 125 - 45(0.2 \times 2 + 0.6) = 80°C \text{ (15 dB headroom, 0 LFM)}$$

$$= 125 - 18(0.2 \times 2 + 0.6) = 107°C \text{ (15 dB headroom, 300 LFM)}$$

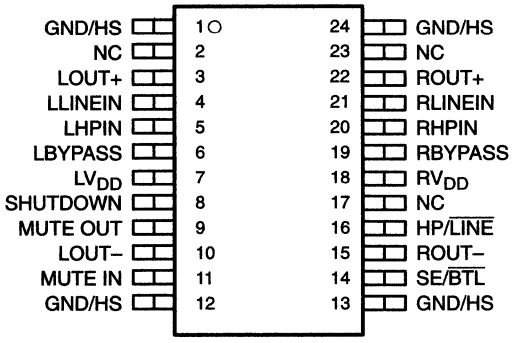
NOTE:

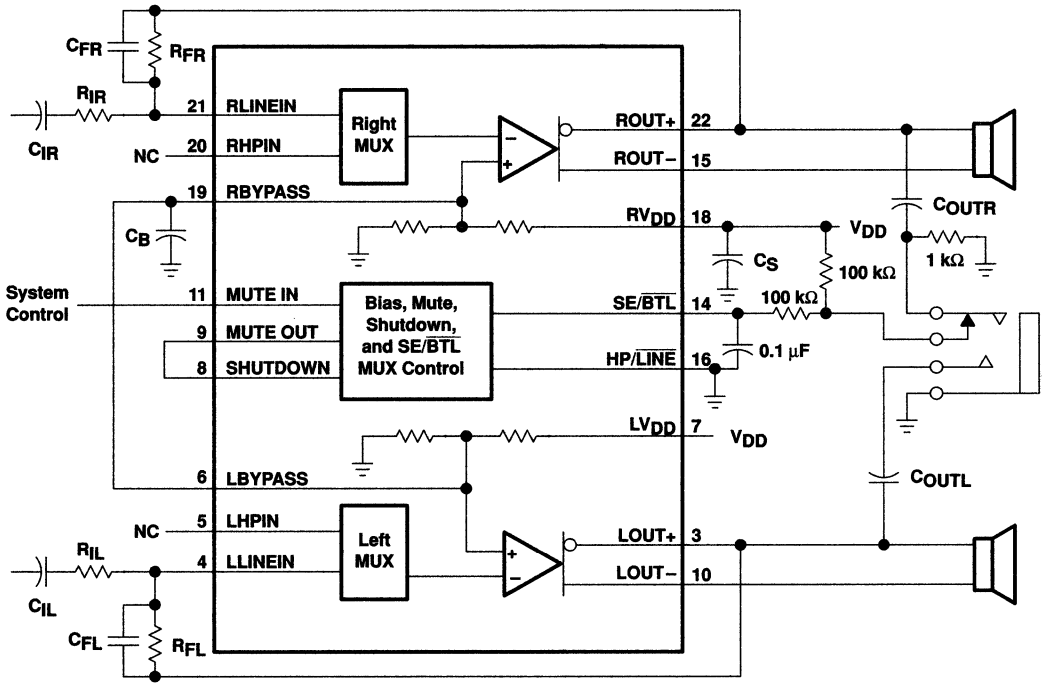
Internal dissipation of 1 W is estimated for a 3-channel system with 15 dB headroom per channel (see Table 4 for more information).

Table 4 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA0103 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. However, sustained operation above 125°C is not recommended. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

- **High Power with PC Power Supply**
  - **1.5 W/Ch at 5 V**
  - **600 mW/Ch at 3 V**
- **Ultra-Low Distortion**
  < 0.05% THD+N at 1.5 W and 4-Ω Load
- **Bridge-Tied Load (BTL) or Single Ended (SE) Modes**
- **Stereo Input MUX**
- **Surface-Mount Power Package**
  24-Pin TSSOP PowerPAD™
- **Shutdown Control . . . I_{DD} < 10 μA**

PWP PACKAGE
(TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

description

The TPA0102 is a stereo audio power amplifier in a 24-pin TSSOP thermal package capable of delivering greater than 1.5 W of continuous RMS power per channel into 4-Ω loads. This device functionality provides a very efficient upgrade path from the TPA4860 and TPA4861 mono amplifiers where three separate devices are required for stereo applications: two for speaker drive, plus a third for headphone drive. The TPA0102 simplifies design and frees up board space for other features. Full power distortion levels of less than 0.1% THD+N from a 5-V supply are typical. This provides significant improvement in fidelity for speech and music over the popular TPA4860/61 series. Low-voltage applications are also well served by the TPA0102 providing 600-mW per channel into 4-Ω loads with a 3.3-V supply voltage.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the TPA0102 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. Using the TPA0102 to drive line outputs up to 500 mW/channel into external 4 Ω loads is ideal for small non-powered external speakers in portable multimedia systems. The TPA0102 also features a shutdown function for power sensitive applications, holding the supply current below 5 μA. In speakerphone or other monaural applications, the TPA0102 is configured through the power supply terminals to activate only half of the amplifier which reduces supply current by approximately one-half over stereo applications.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0102 to operate at full power into 4-Ω loads at ambient temperature of up to 55°C. Into 8-Ω loads, the operating ambient temperature increases to 100°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP (PWP)
40°C to 85°C	TPA0102PWP

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND/HS	1, 12, 13, 24		Ground connection for circuitry, directly connected to thermal pad
HP/$\overline{\text{LINE}}$	16	I	Input MUX control input, hold high to select L/RHPIN (5, 20), hold low to select L/RLINEIN (4, 21)
LBYPASS	6		Tap to voltage divider for left channel internal mid-supply bias
LHP IN	5	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
LLINE IN	4	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
LOUT+	3	O	Left channel + output in BTL mode, + output in SE mode
LOUT–	10	O	Left channel – output in BTL mode, high-impedance state in SE mode
LV_{DD}	7	I	Supply voltage input for left channel and for primary bias circuits
MUTE IN	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute
MUTE OUT	9	O	Follows MUTE IN terminal (11), provides buffered output
NC	2, 17, 23		No internal connection
RBYPASS	19		Tap to voltage divider for right channel internal mid–supply bias
RHP IN	20	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
RLINE IN	21	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
ROUT+	22	O	Right channel + output in BTL mode, + output in SE mode
ROUT–	15	O	Right channel – output in BTL mode, high impedance state in SE mode
RV_{DD}	18	I	Supply voltage input for right channel
SE/$\overline{\text{BTL}}$	14	I	Hold low for BTL mode, hold high for SE mode
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, $I_{DD} < 1\ \mu A$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			3	5	5.5	V
Operating free-air temperature, T_A	V_{DD} = 5 V, 250 mW/ch average power,	4-Ω stereo BTL drive, With proper PCB design	–40		85	°C
	V_{DD} = 5 V, 1.5 W/ch average power,	4-Ω stereo BTL drive, With proper PCB design	–40		55	
Common mode input voltage, V_{ICM}	V_{DD} = 5 V		1.25		4.5	V
	V_{DD} = 3.3 V		1.25		2.7	

dc electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP†	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 5 V	Stereo BTL		19	25	mA
			Stereo SE		9	15	mA
			Mono BTL		9	15	mA
			Mono SE		3	10	mA
		V_{DD} = 3.3 V	Stereo BTL		13	20	mA
			Stereo SE		3	10	mA
			Mono BTL		3	10	mA
			Mono SE		3	10	mA
V_{OO}	Output offset voltage (measured differentially)	V_{DD} = 5 V	Gain = 2,	See Note 1	5	25	mV
$I_{DD(MUTE)}$	Supply current in mute mode	V_{DD} = 5 V			800		µA
$I_{DD(SD)}$	I_{DD} in shutdown	V_{DD} = 5 V			5	15	µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%,	BTL		1.25		W
		THD = 1%,	BTL		1.5		
		THD = 0.2%,	SE		500		mW
		THD = 1%,	SE		600		
THD+N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 to 20 kHz		200		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL			72°		
		Open Load			71°		
		SE			52°		
	Power supply ripple rejection	f = 1 kHz			75		dB
		f = 20 – 20 kHz,			60		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage				25		μV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%	BTL		600		mW
		THD = 1%	BTL		750		
		THD = 0.2%,	SE		200		
		THD = 1%,	SE		250		
THD+N	Total harmonic distortion plus noise	P_O = 600 mW,	f = 20 to 20 kHz		250		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL			92°		
		Open Load			70°		
		SE			57°		
	Power supply ripple rejection	f = 1 kHz			70		dB
		f = 20 – 20 kHz			55		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage				25		μV(rms)

NOTE 2 Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

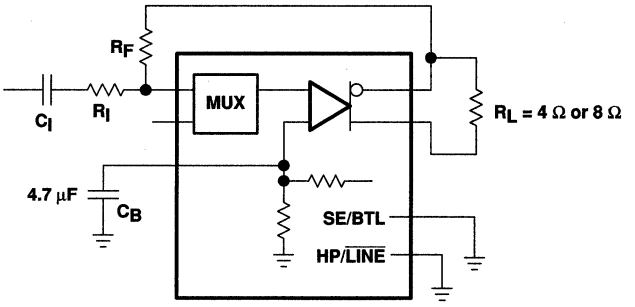


Figure 1. BTL Test Circuit

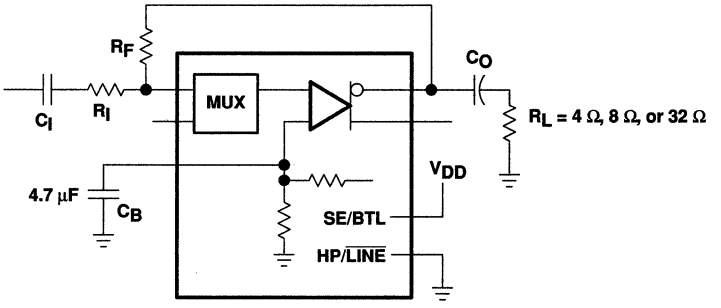


Figure 2. SE Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Frequency	4, 5, 7, 8, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24, 26, 27, 29, 30, 32, 33
		vs Output power	3, 6, 9, 10, 13, 16, 19, 22, 25, 28, 31, 34
V_n	Output noise voltage	vs Frequency	35, 36
	Supply ripple rejection ratio	vs Frequency	37, 38
	Crosstalk	vs Frequency	39–40
	Open loop response	vs Frequency	43, 44
	Closed loop response	vs Frequency	45 – 48
I_{DD}	Supply current	vs Supply voltage	49
P_O	Output power	vs Supply voltage vs Load resistance	50,51 52,53
P_D	Power dissipation	vs Output power	54 – 57

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

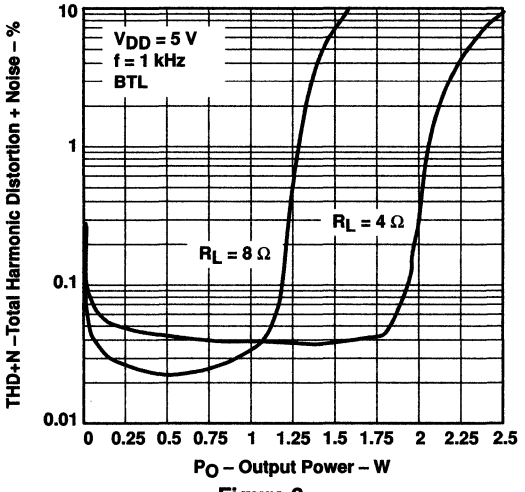


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

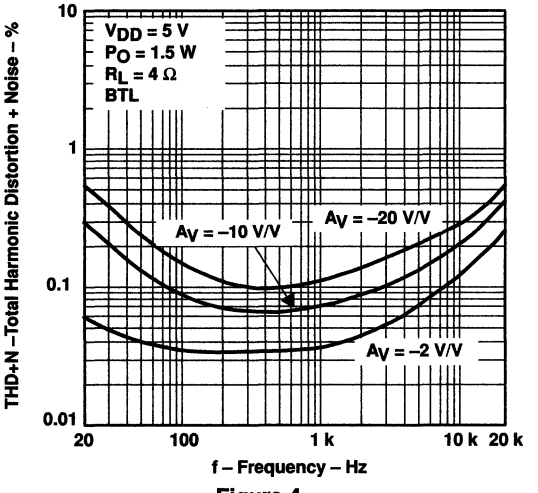


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

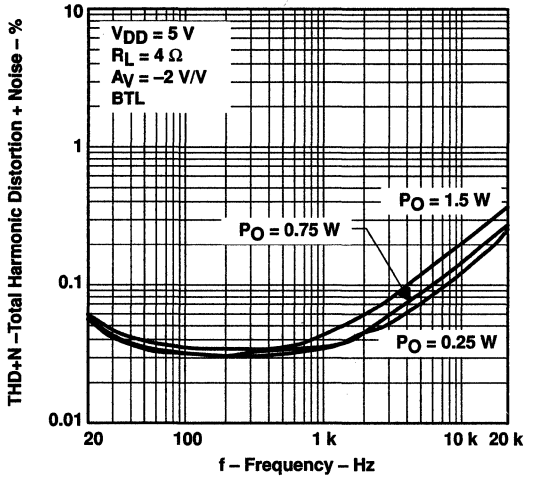


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

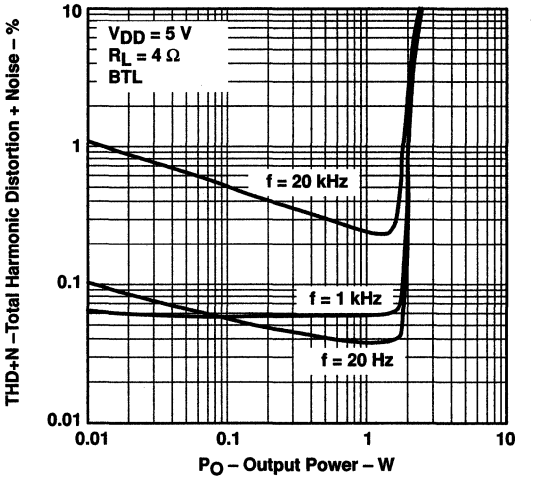


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

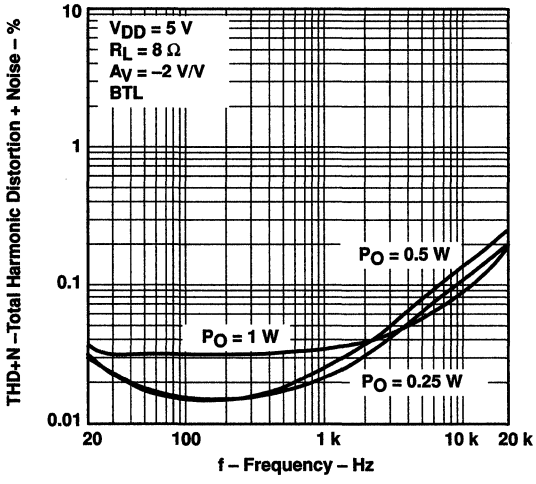


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

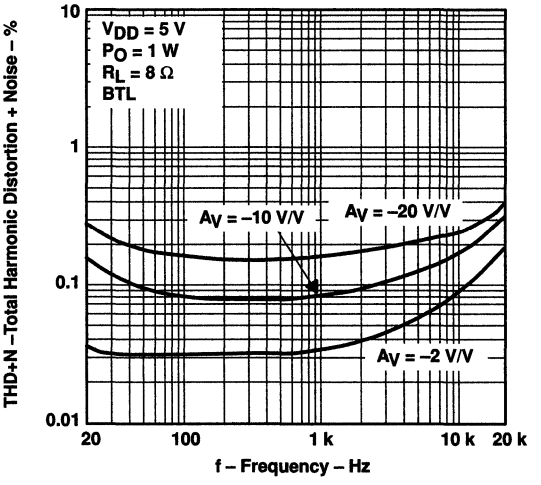


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

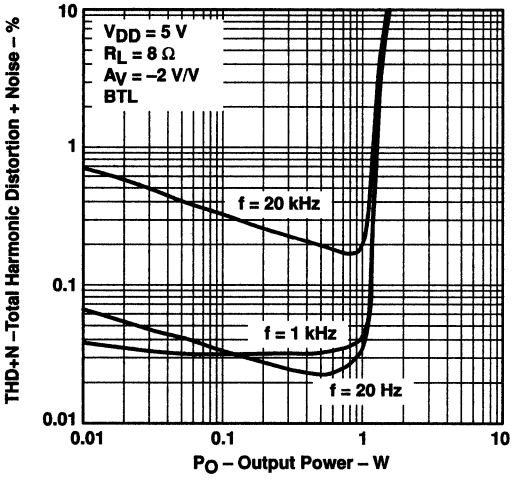


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

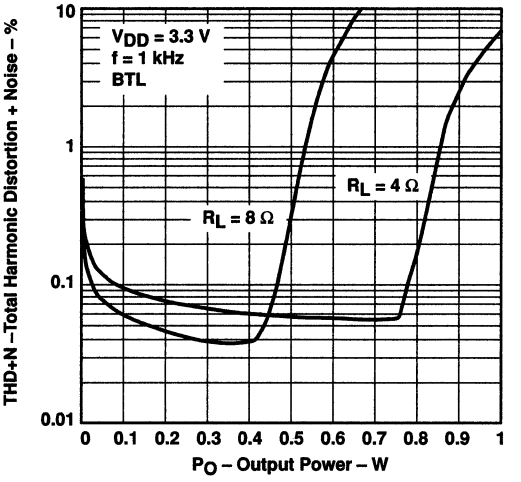


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

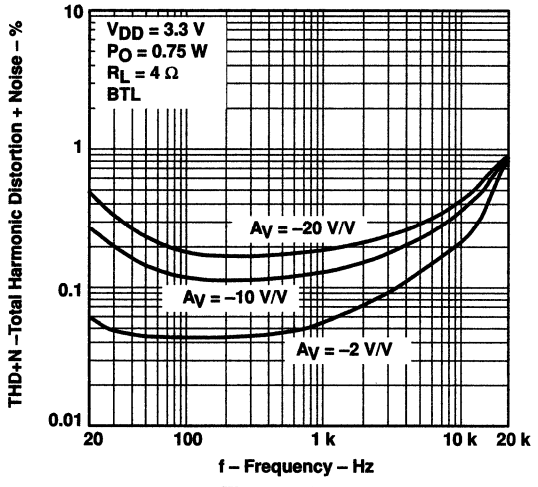


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

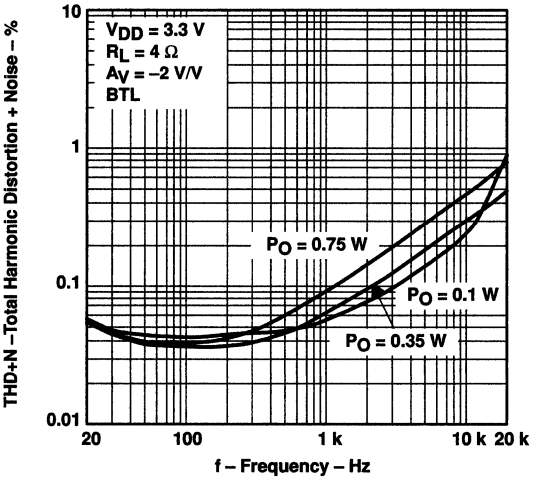


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

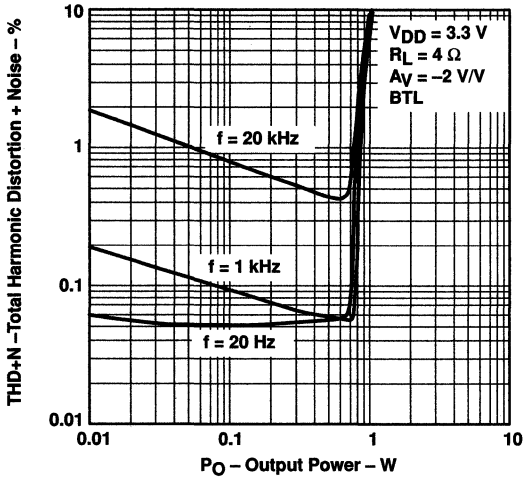


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

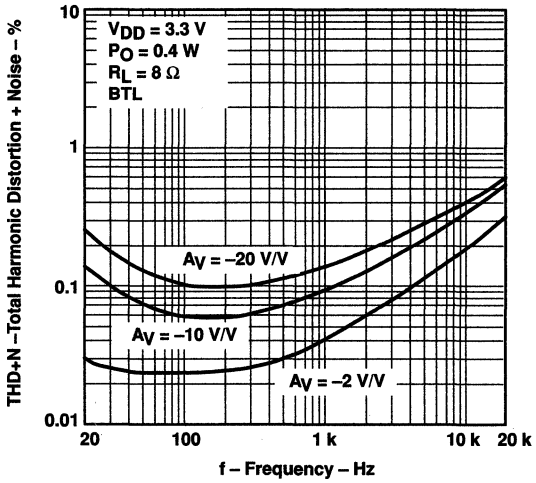


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

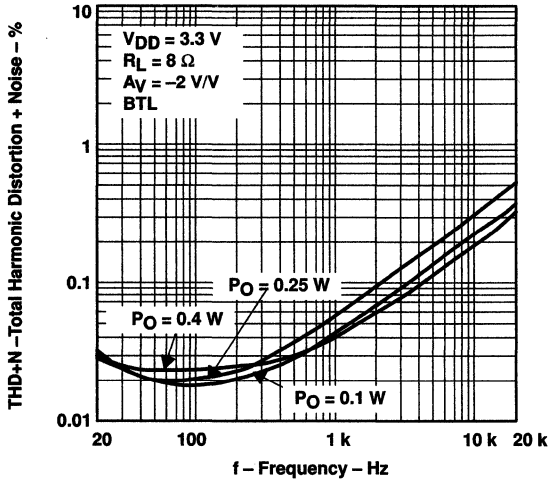


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

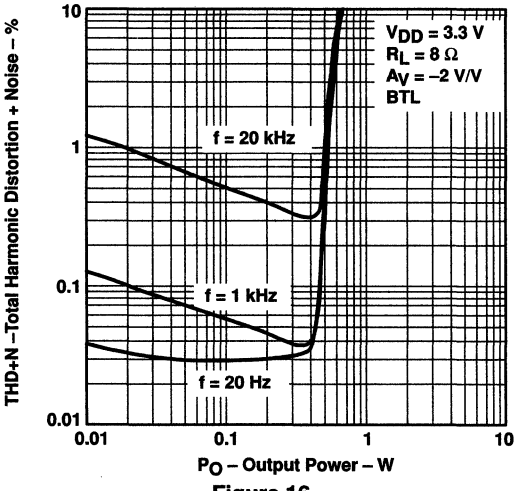


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

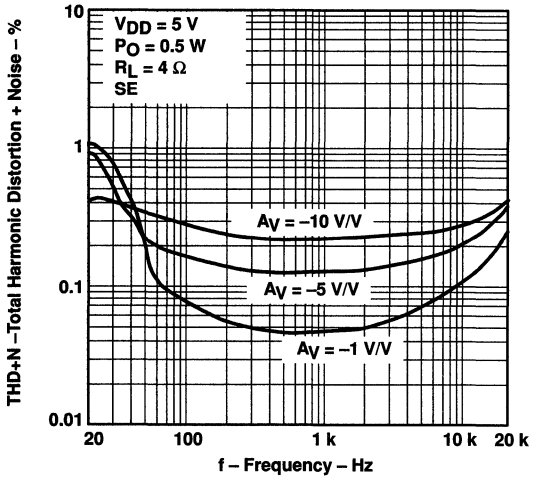


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

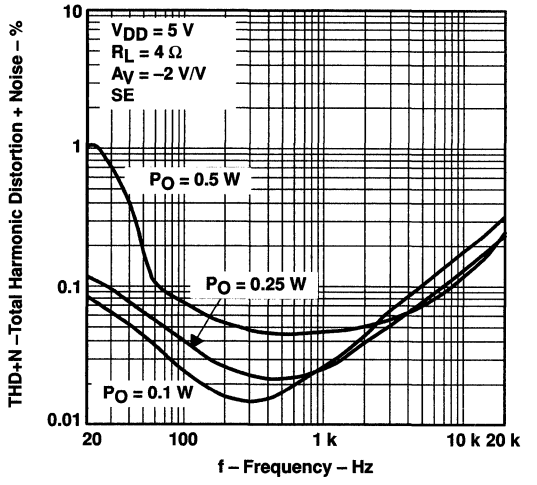


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

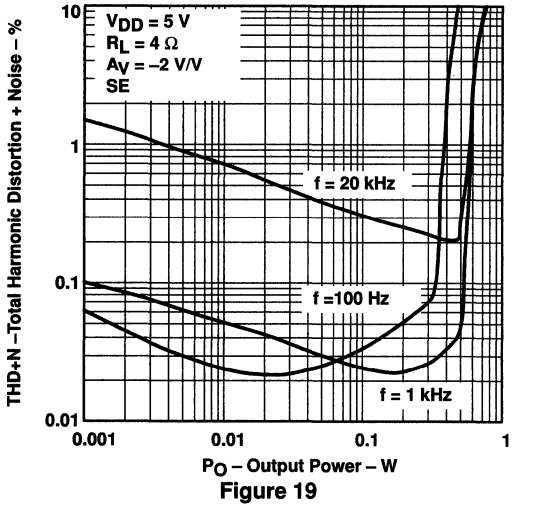


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

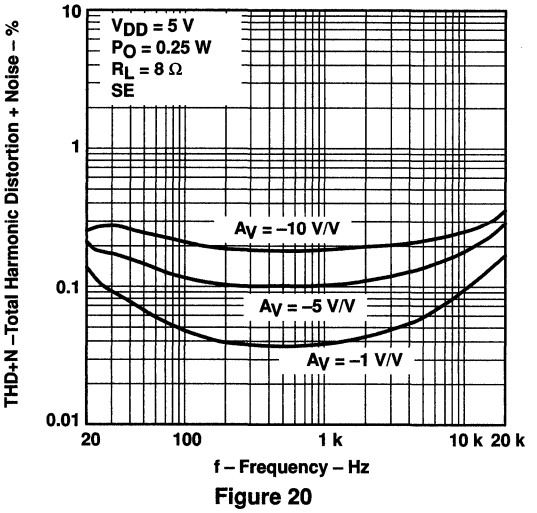


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

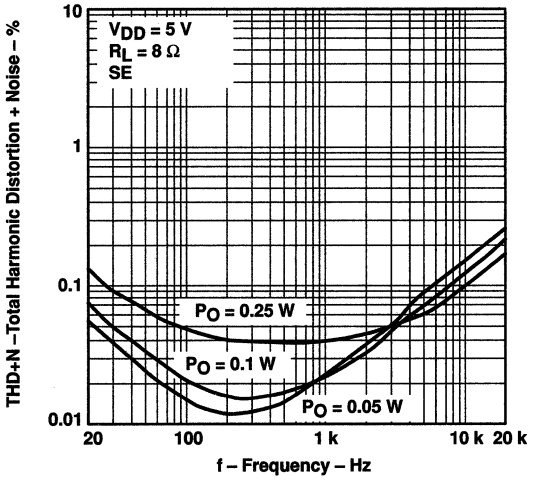


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

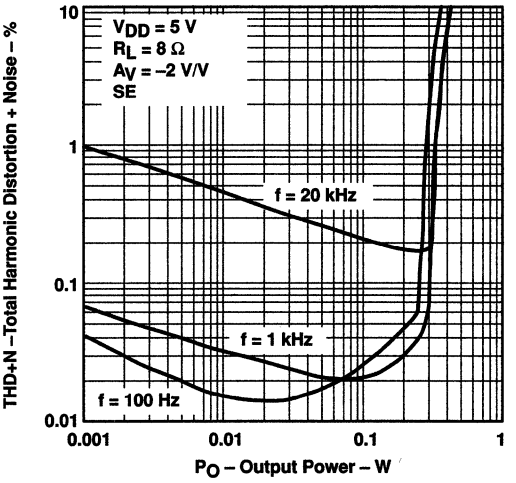


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

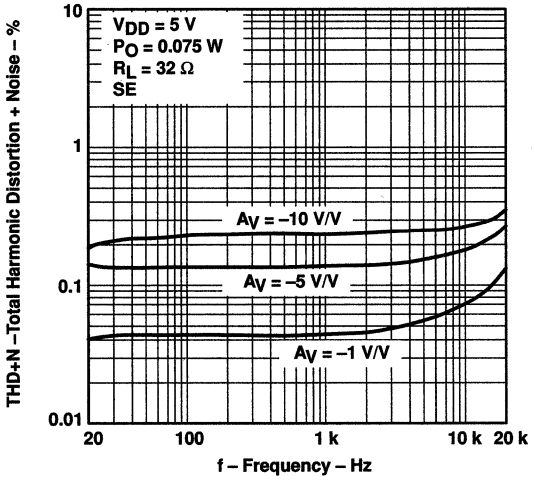


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

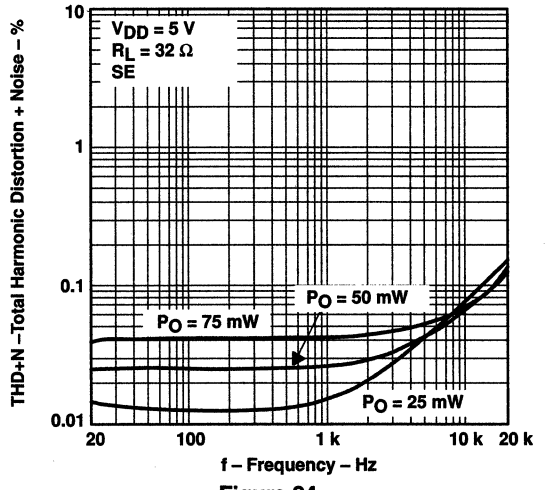


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

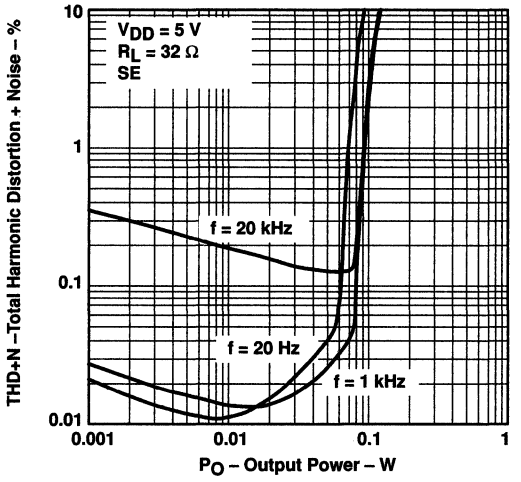


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

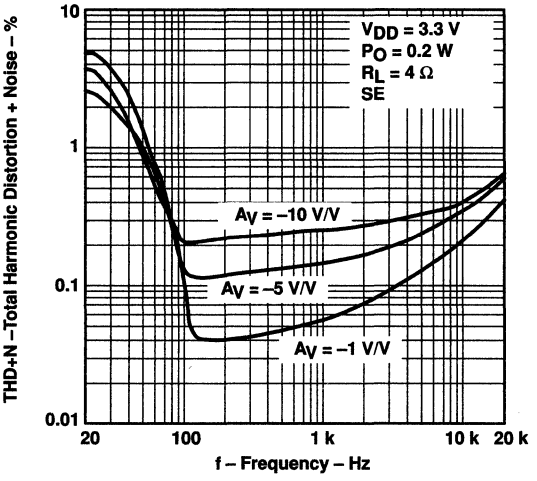


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

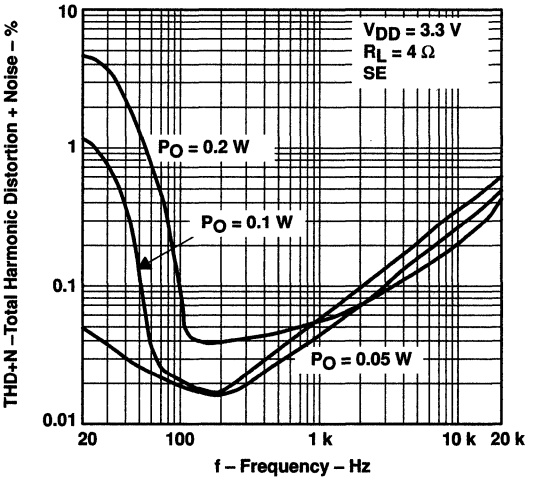


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

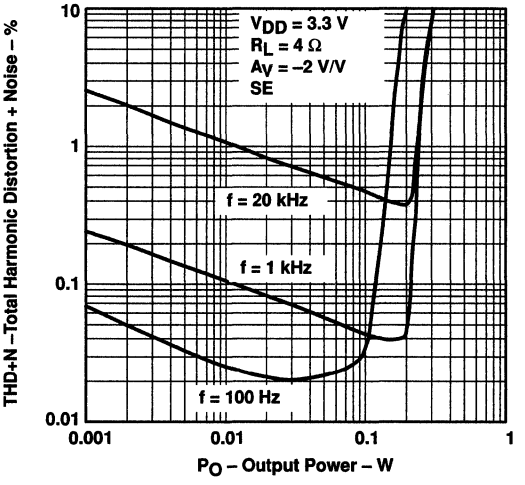


Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

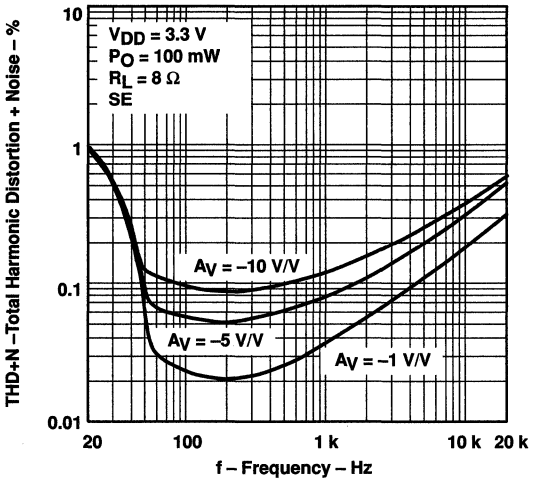


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

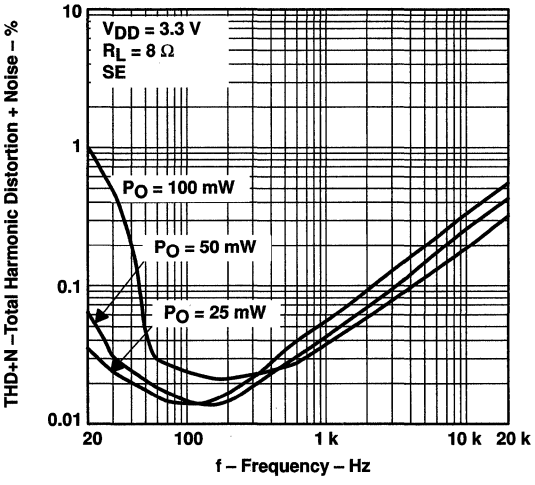


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

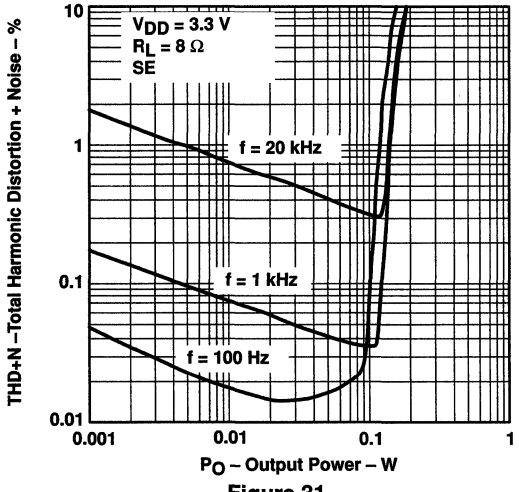


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

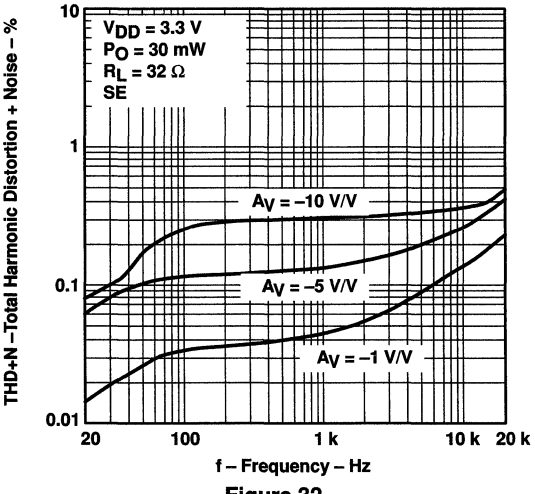


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

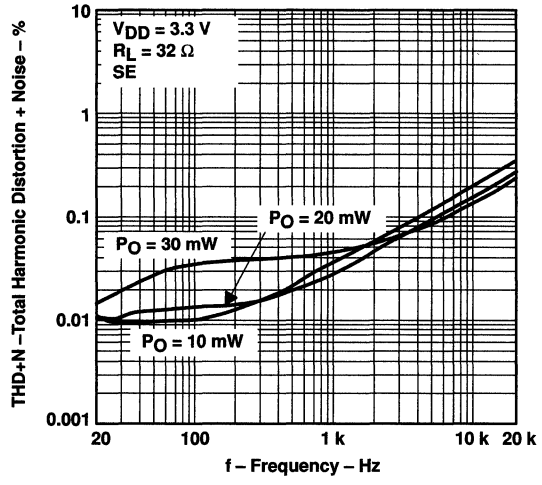


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

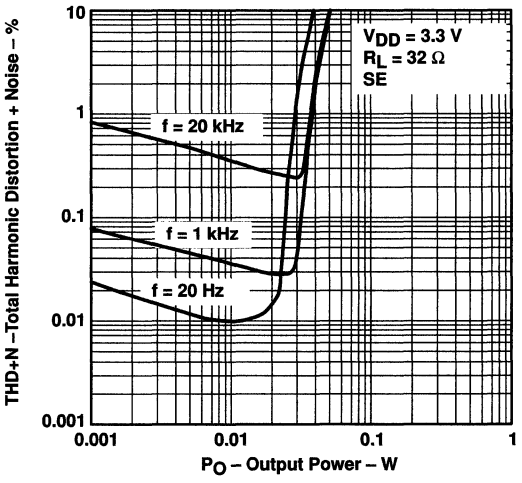


Figure 34

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

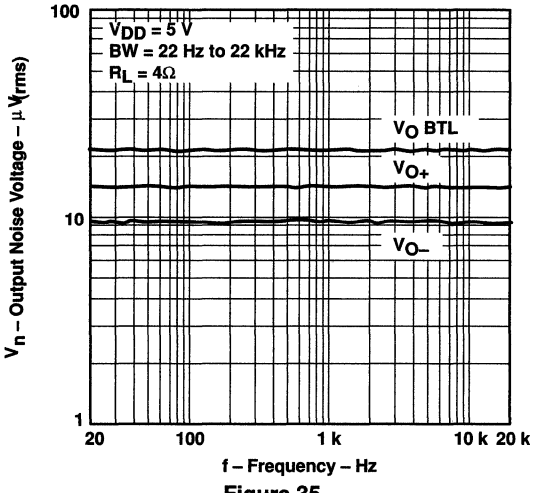


Figure 35

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

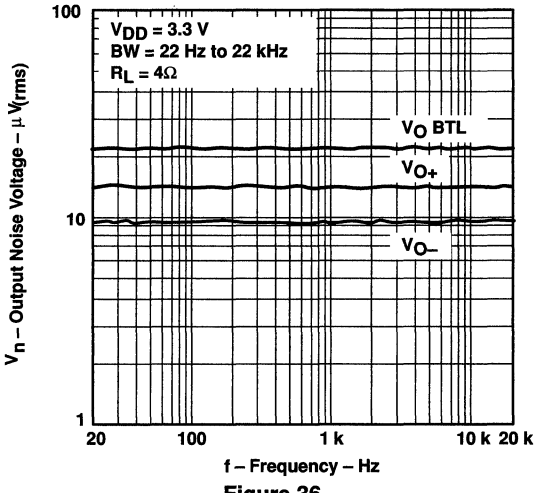


Figure 36

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

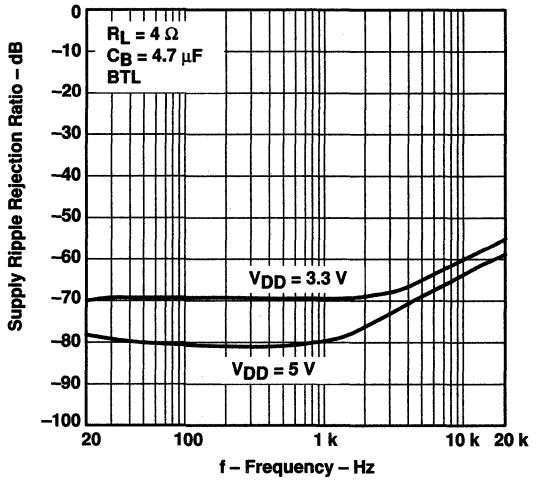


Figure 37

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

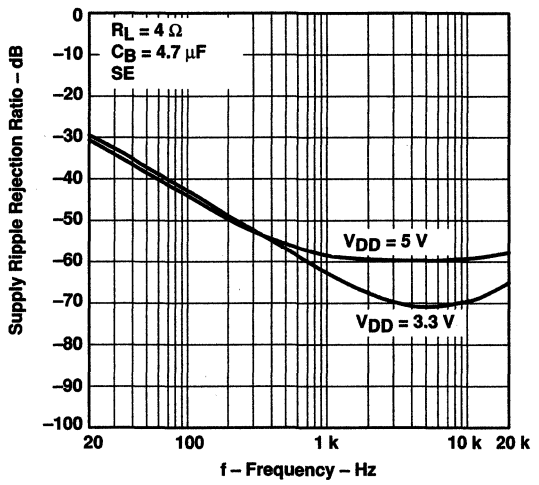


Figure 38

CROSSTALK
vs
FREQUENCY

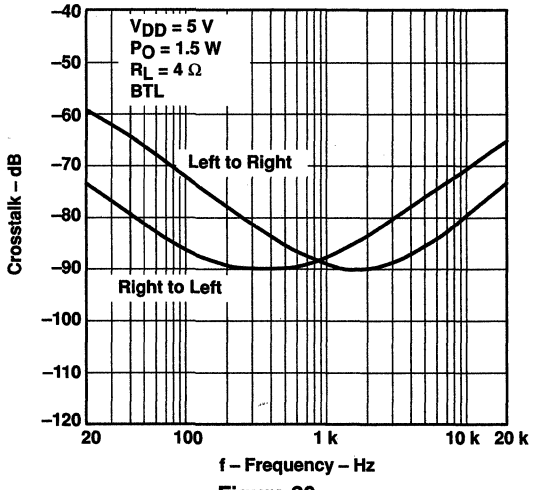


Figure 39

CROSSTALK
vs
FREQUENCY

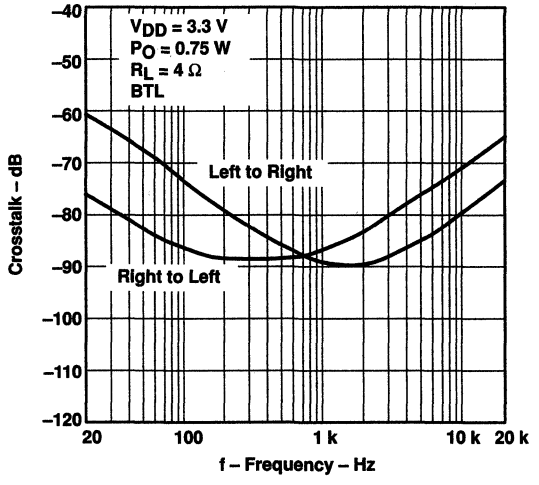


Figure 40

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

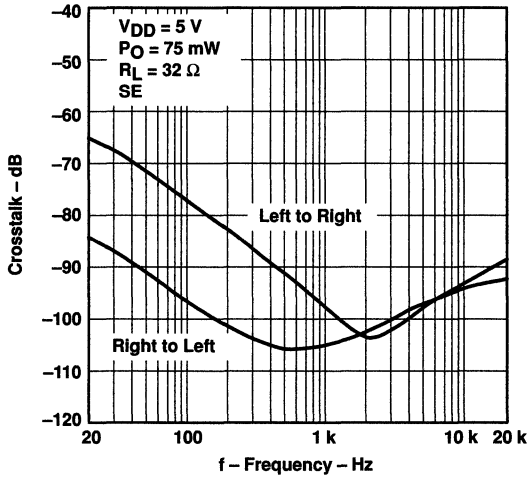


Figure 41

CROSSTALK
vs
FREQUENCY

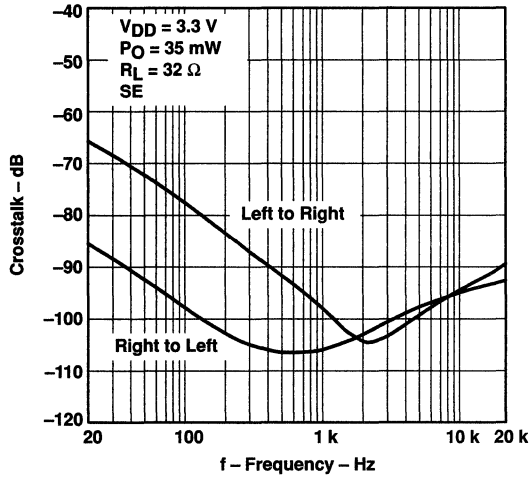


Figure 42

OPEN LOOP RESPONSE

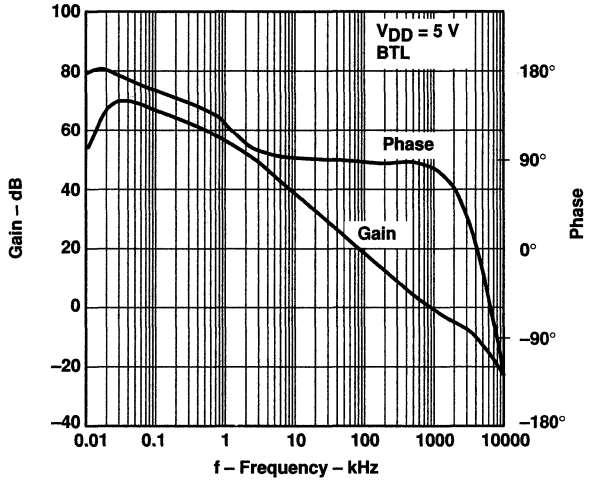


Figure 43

TYPICAL CHARACTERISTICS

OPEN LOOP RESPONSE

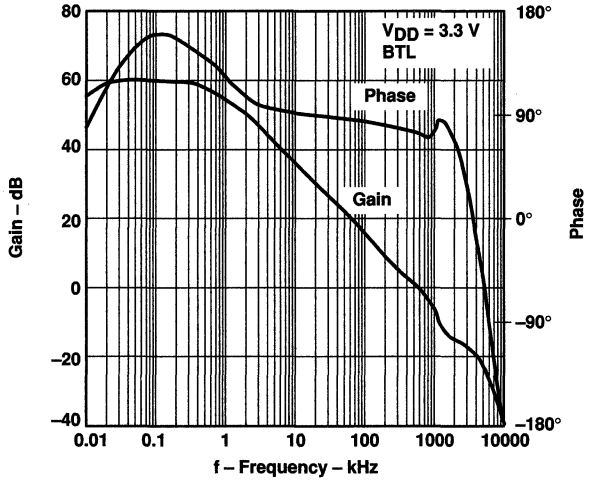


Figure 44

CLOSED LOOP RESPONSE

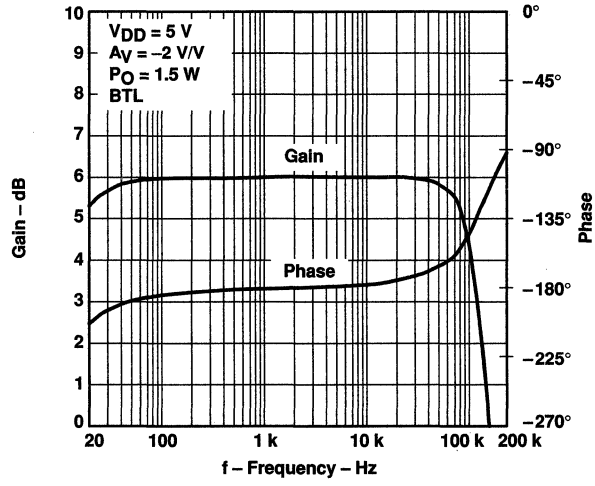


Figure 45

TYPICAL CHARACTERISTICS

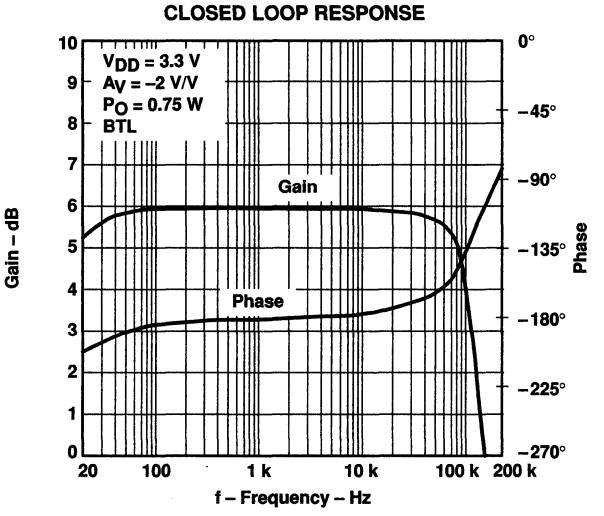


Figure 46

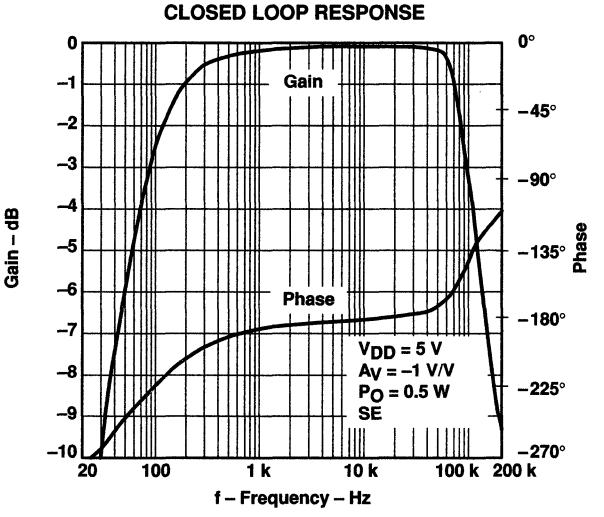


Figure 47

TYPICAL CHARACTERISTICS

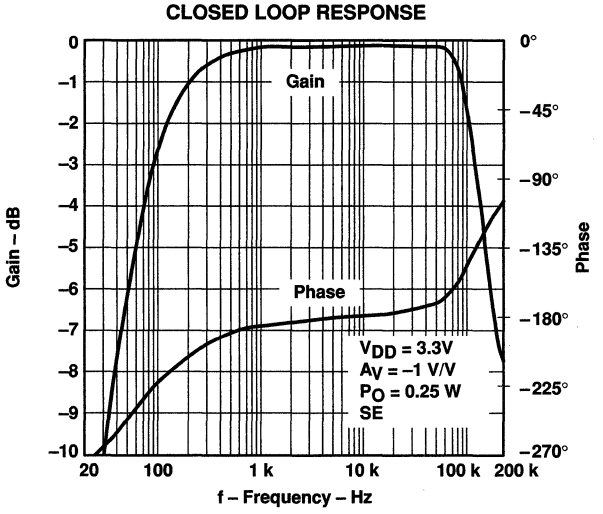


Figure 48

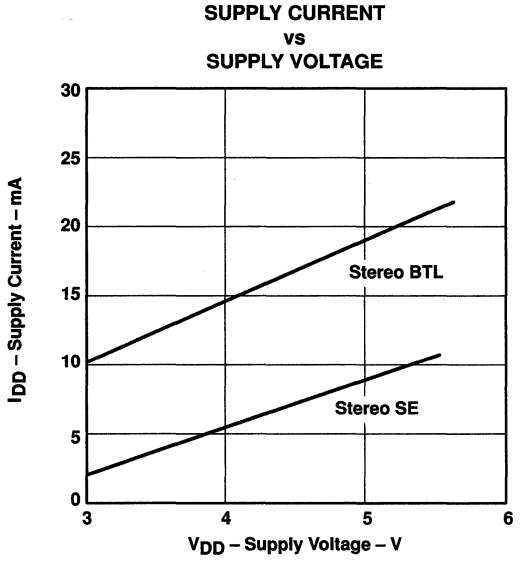


Figure 49

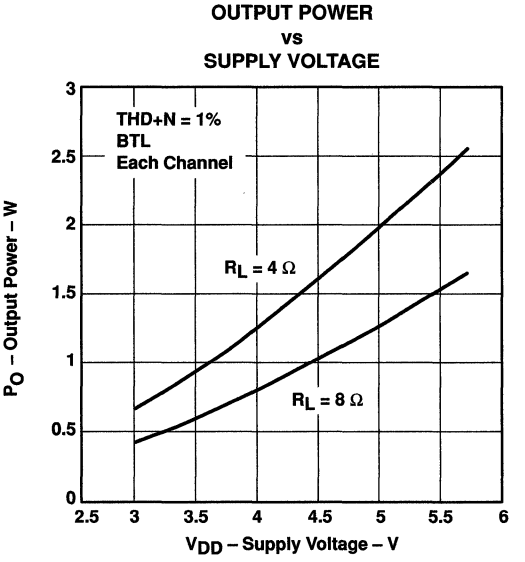


Figure 50

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

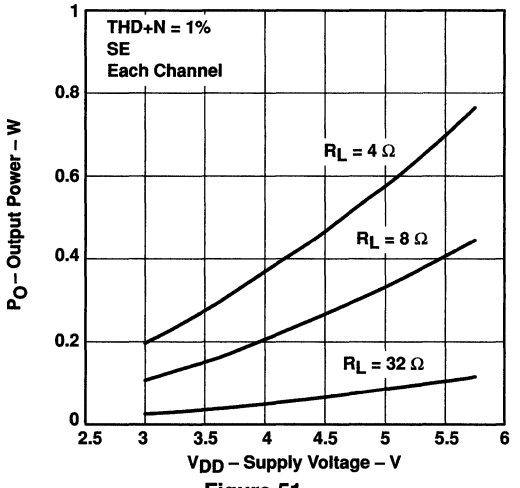


Figure 51

OUTPUT POWER
vs
LOAD RESISTANCE

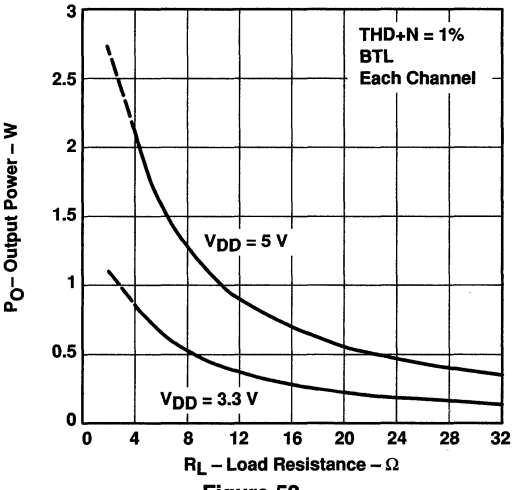


Figure 52

OUTPUT POWER
vs
LOAD RESISTANCE

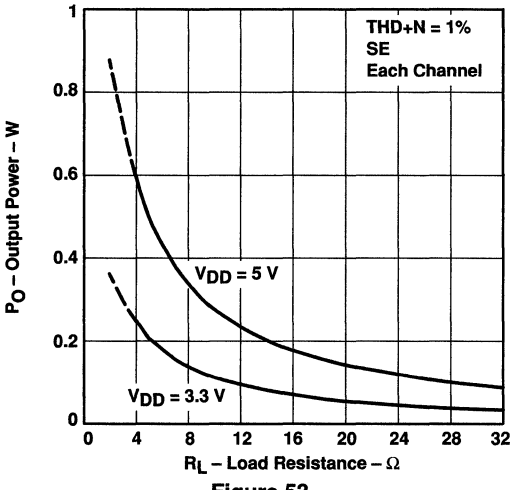


Figure 53

POWER DISSIPATION
vs
OUTPUT POWER

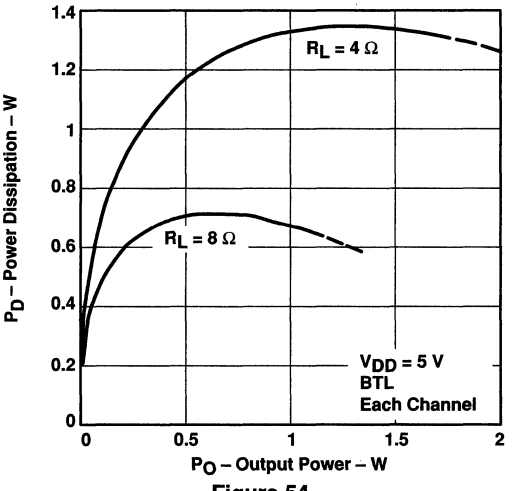


Figure 54

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
OUTPUT POWER

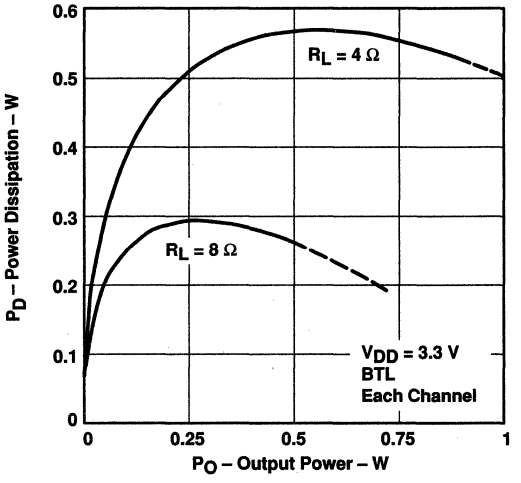


Figure 55

POWER DISSIPATION
vs
OUTPUT POWER

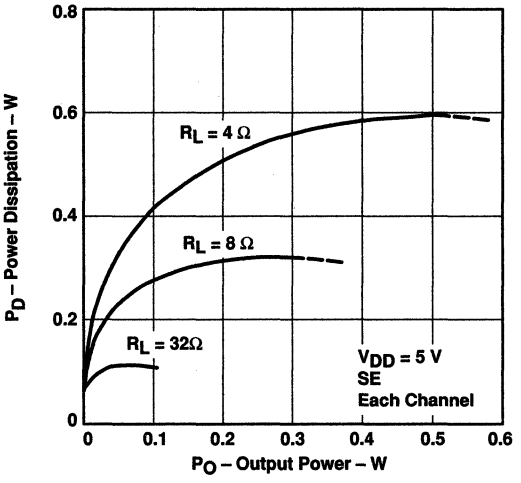


Figure 56

POWER DISSIPATION
vs
OUTPUT POWER

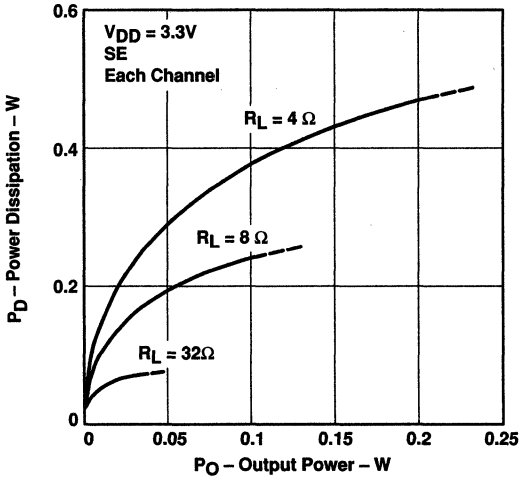


Figure 57

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

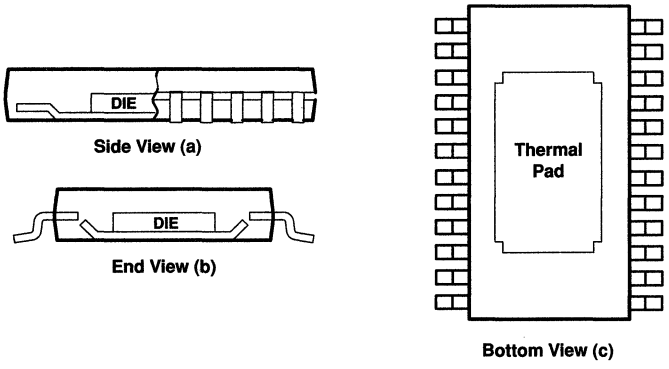


Figure 58. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0102 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

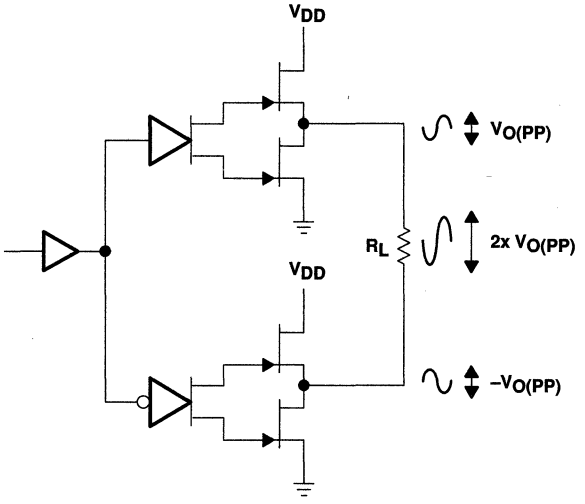


Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

$$f_c = \frac{1}{2\pi R_L C_C} \quad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

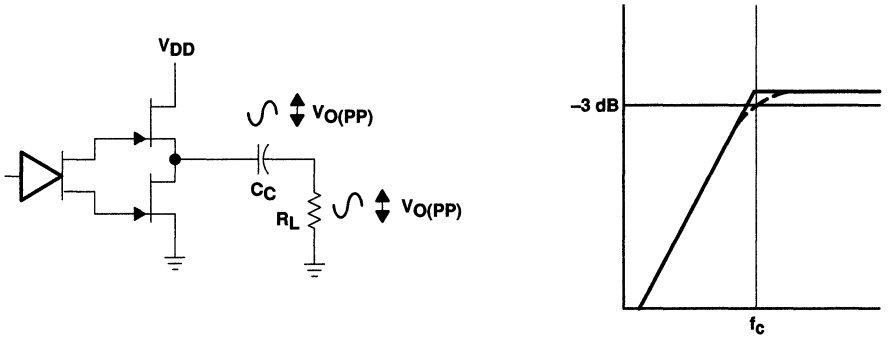


Figure 60. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).

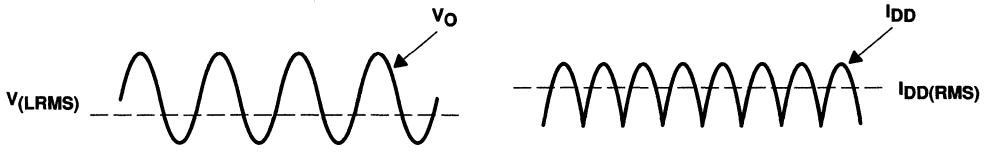


Figure 61. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0102 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1, then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to chose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 62 and Figure 63 are a schematic diagrams of a typical notebook computer application circuits.

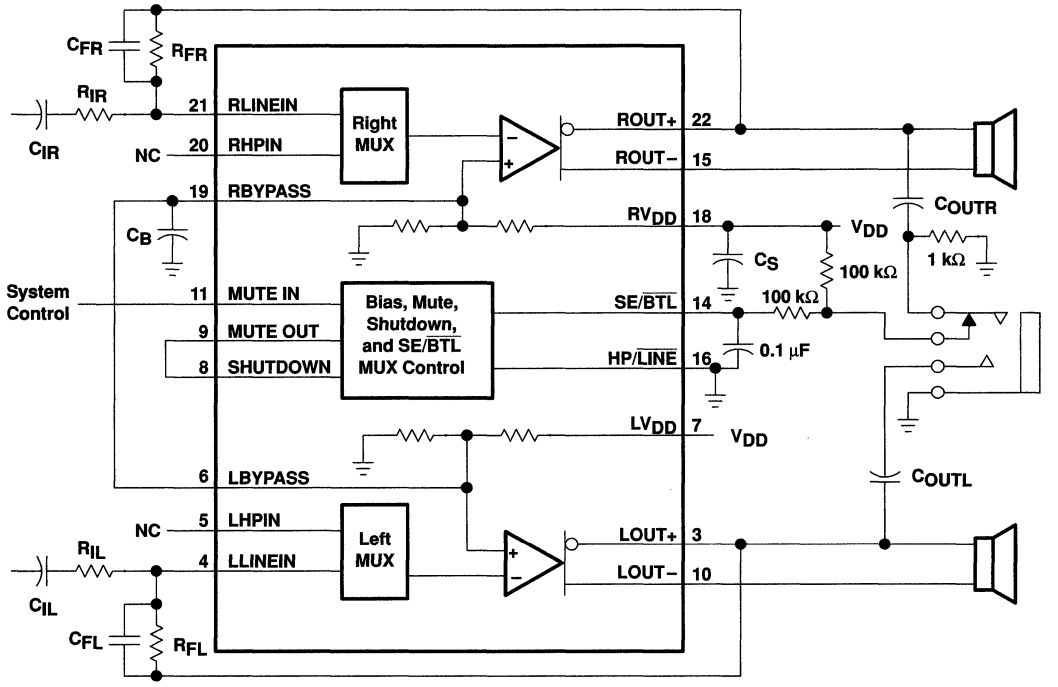
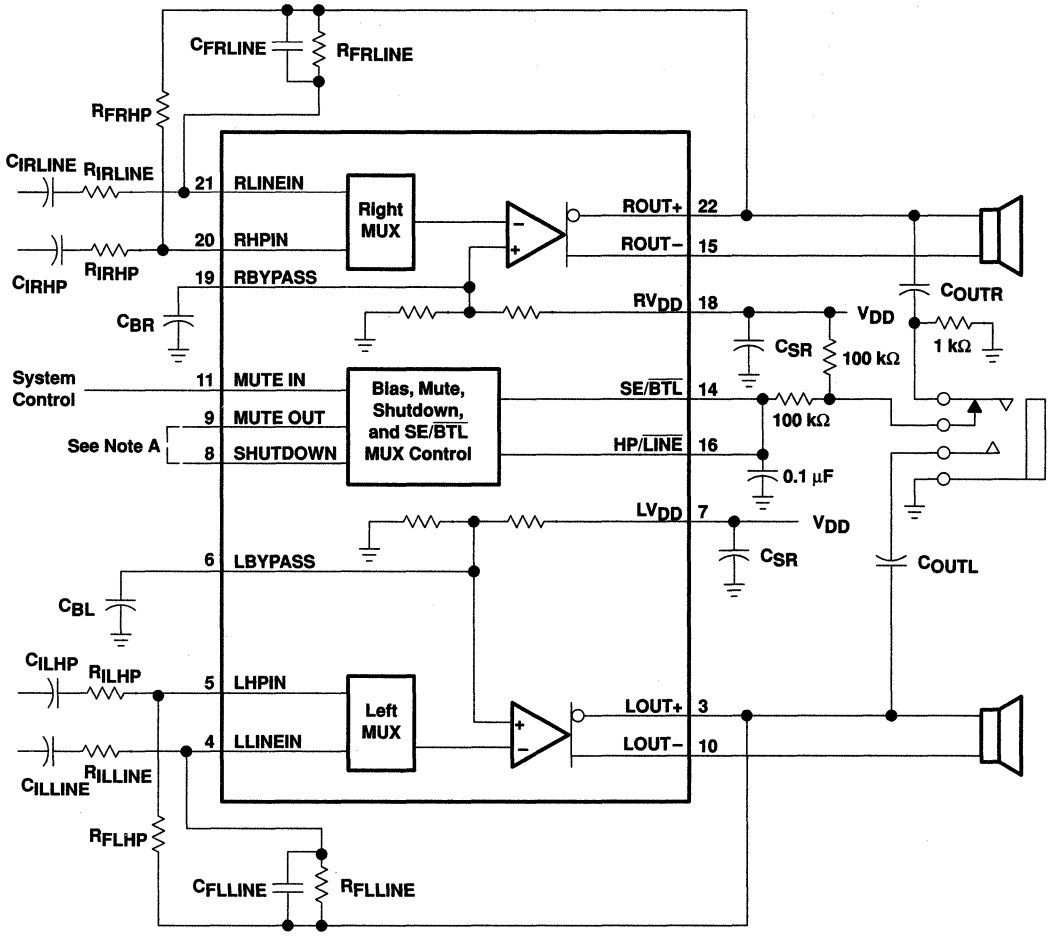


Figure 62. TPA0102 Minimum Configuration Application Circuit

APPLICATION INFORMATION



NOTE A. This connection is for ultralow current in shutdown mode.

Figure 63. TPA0102 Full Configuration Application Circuit

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0102 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \quad (5)$$

APPLICATION INFORMATION

gain setting resistors, R_F and R_I (continued)

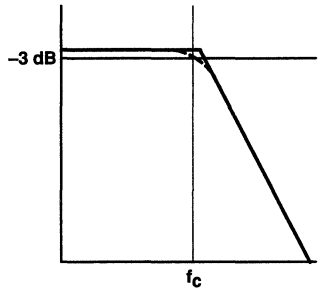
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0102 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

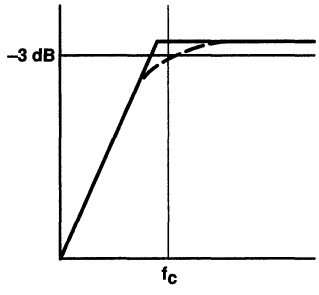


For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0102 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \quad (10)$$

As an example, consider a circuit where C_B is 0.1 μF, C_I is 0.22 μF and R_I is 10 kΩ. Inserting these values into the equation 10 we get 400 ≤ 454 which satisfies the rule. Bypass capacitor, C_B, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

In Figure 63, the full feature configuration, two bypass capacitors are used. This provides the maximum separation between right and left drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used as shown in Figure 62. It is critical that terminals 6 and 19 be tied together in this configuration.

APPLICATION INFORMATION

single-ended operation

In SE mode (see Figure 59 and Figure 60), the load is driven from the primary amplifier output for each channel (OUT+, terminals 22 and 3).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

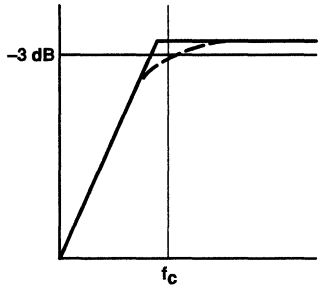
The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{12}$$

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \tag{13}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0102 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0102, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 14) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 10 and 15). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0102 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0102 as an SE driver from LOUT+ and ROUT+ (terminals 3 and 22). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 64.

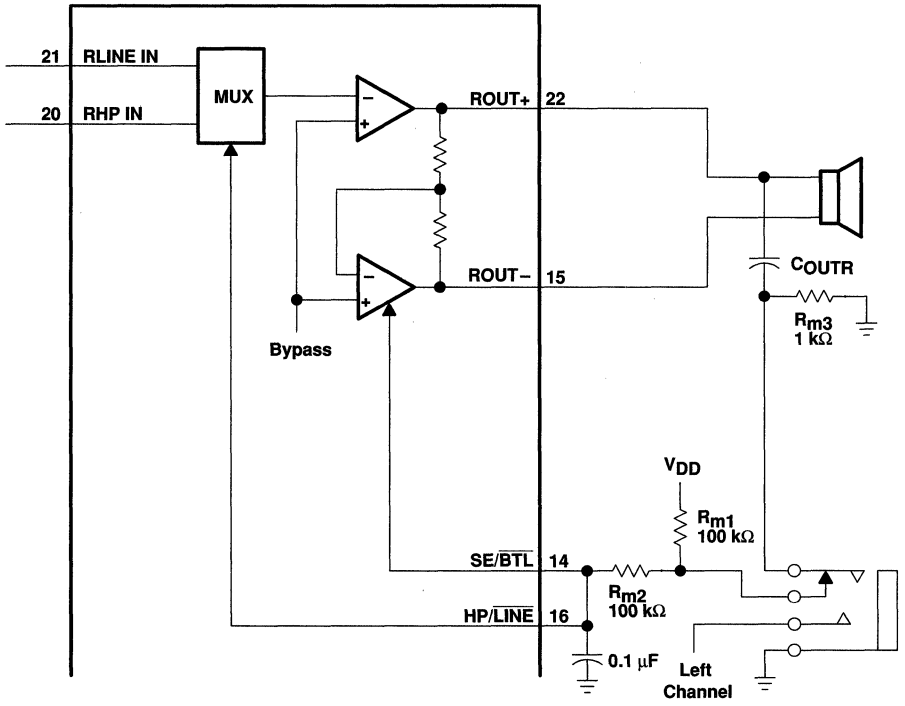


Figure 64. TPA0102 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

As shown in the full feature application (Figure 63), the input MUX control can be tied to the SE/$\overline{\text{BTL}}$ input. The benefits of doing this are described in the following input MUX operation section.

APPLICATION INFORMATION

Input MUX operation

Working in concert with the SE/$\overline{\text{BTL}}$ feature, the HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 65). The primary function of the MUX is to allow different gain settings for BTL versus SE mode. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{SE Gain}_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \quad (14)$$

If, for example $R_{I(HP)}$ = 20 kΩ and $R_{F(HP)}$ = 20 kΩ then $\text{SE Gain}_{(HP)}$ = –1

$$\text{BTL Gain}_{(LINE)} = -2\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \quad (15)$$

If, for example $R_{I(LINE)}$ = 20 kΩ and $R_{F(LINE)}$ = 100 kΩ then $\text{BTL Gain}_{(LINE)}$ = –10

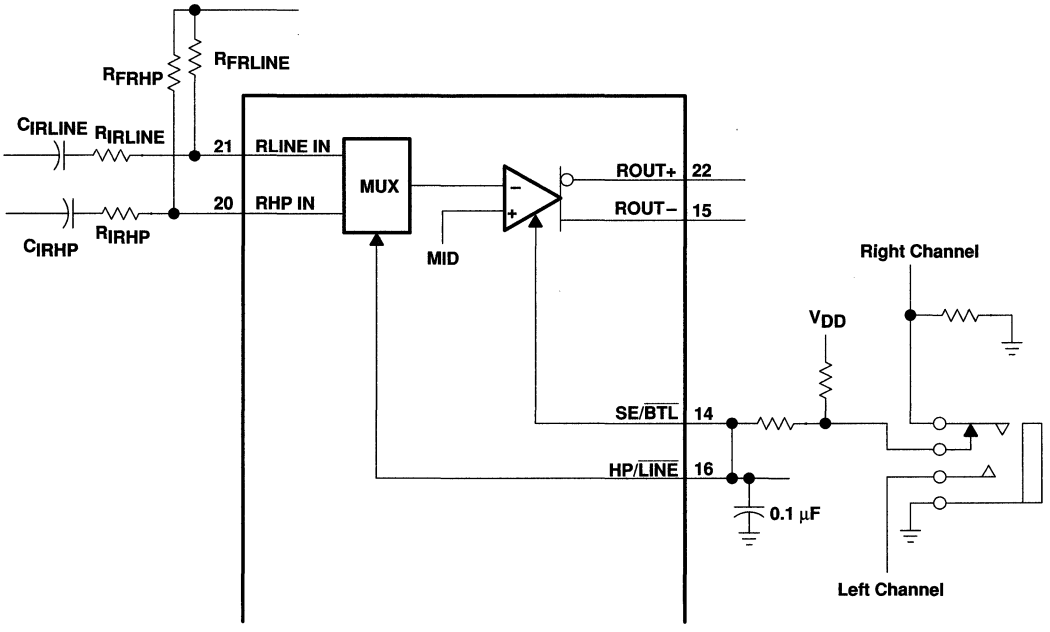


Figure 65. TPA0102 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

APPLICATION INFORMATION

mute and shutdown modes

The TPA0102 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} < 1$ μA. SHUTDOWN or MUTE IN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces $I_{DD} < 1$ mA.

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0102 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0102 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed to $V_{O(PP)} = 4$ V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0102 data sheet, one can see that when the TPA0102 is operating from a 5-V supply into a 4-Ω speaker that 1.5 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right)$$
$$= 10\text{Log}\left(\frac{1.5}{1}\right)$$
$$= 1.76\ \text{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

1.76 dB – 15 dB = – 13.24 dB (15 dB headroom)
1.76 dB – 12 dB = – 10.24 dB (12 dB headroom)
1.76 dB – 9 dB = – 7.24 dB (9 dB headroom)
1.76 dB – 6 dB = – 4.24 dB (6 dB headroom)
1.76 dB – 3 dB = – 1.24 dB (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$
= 47 mW (15 dB headroom)
= 94 mW (12 dB headroom)
= 188 mW (9 dB headroom)
= 376 mW (6 dB headroom)
= 752 mW (3 dB headroom)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 1.5 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA0102 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0102 Power Rating, 5-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
1.5	1.5 W	1.35	28°C
1.5	752 mW (3 dB)	1.3	33°C
1.5	376 mW (6 dB)	0.9	69°C
1.5	188 mW (9 dB)	0.7	87°C
1.5	94 mW (12 dB)	0.55	100°C
1.5	47 mW (15 dB)	0.4	114°C

APPLICATION INFORMATION

headroom and thermal considerations (continued)

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP‡	2.8 W	22.1 mW/°C	1.8 W	1.4 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 22 mW/°C and 54 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

$$= \frac{1}{0.022}$$

$$= 45°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0102 is 150 °C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D$$

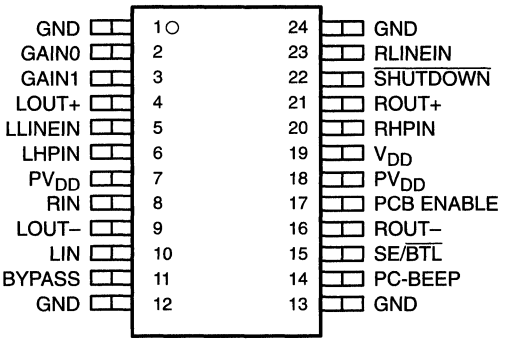
$$= 150 - 45(0.4 \times 2) = 114°C \text{ (15 dB headroom, 0 CFM)}$$

NOTE:
Internal dissipation of 0.4 W is estimated for a 1.5-W system with 15 dB headroom per channel.

Table 4 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA0102 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

- Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load
- Internal Gain Control, Which Eliminates External Gain-Setting Resistors
- 2-W/Ch Output Power Into 3-Ω Load
- PC-Beep Input
- Depop Circuitry
- Stereo Input MUX
- Fully Differential Input
- Low Supply Current and Shutdown Current
- Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™

PWP PACKAGE
(TOP VIEW)



description

The TPA0112 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0112 has less than 0.8% THD+N across its specified frequency range.

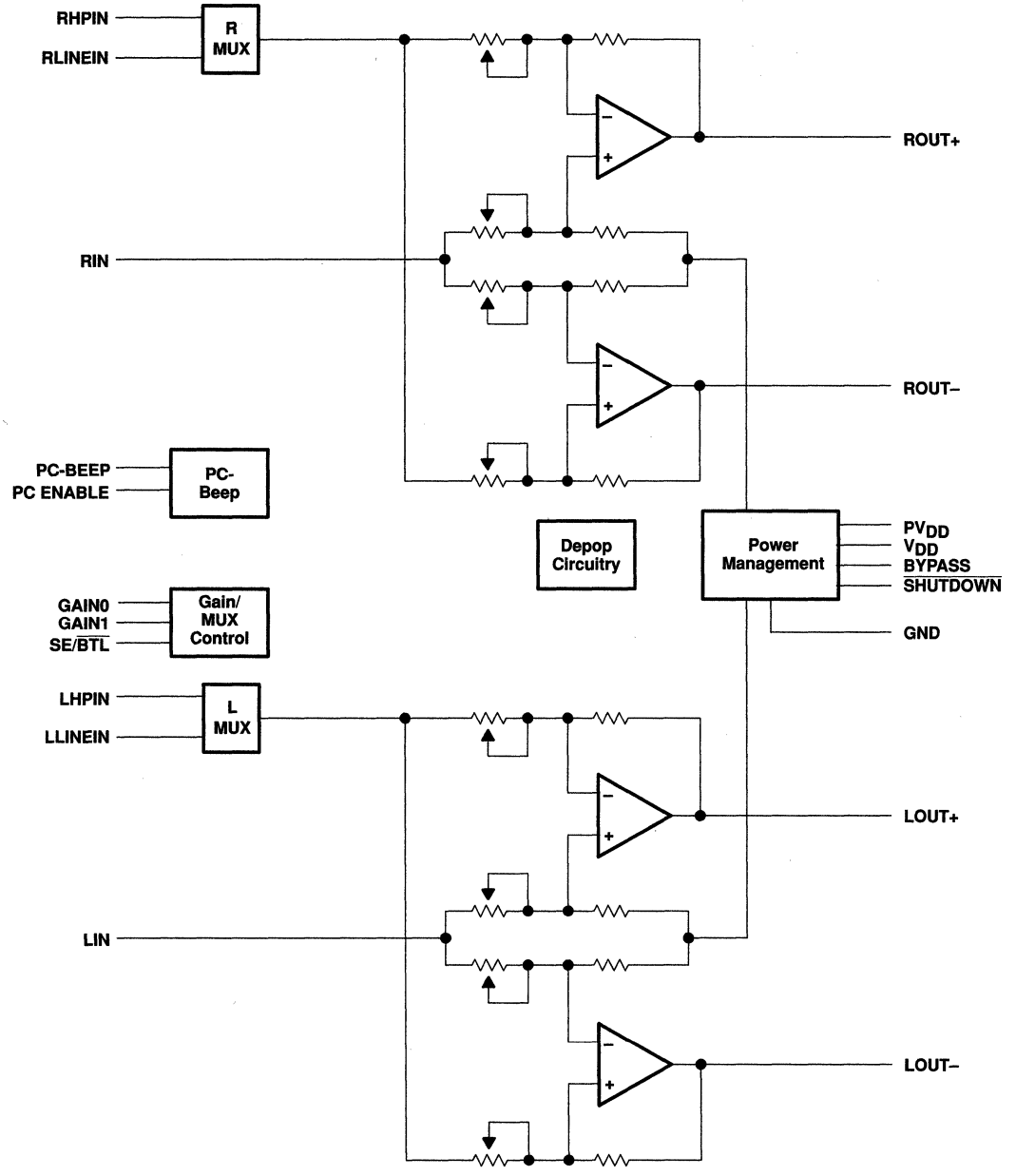
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of –2, –6, –12, and –24 V/V are provided, while SE gain is always configured as –1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0112 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this reduces the gain to –1 V/V.

The TPA0112 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0112 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0112PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0112PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PCB ENABLE	17	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4 V to 5 V		77		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		6	8	mA
		SE mode		3	4	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω	f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.75%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		16		µV RMS
			SE mode		30		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–7, 10–13, 16–19, 21
		vs Frequency	2, 3, 8, 9, 14, 15, 20, 22
		vs Output voltage	23
V_n	Output noise voltage	vs Bandwidth	24
	Supply ripple rejection ratio	vs Frequency	25, 26
	Crosstalk	vs Frequency	27–29
	Shutdown attenuation	vs Frequency	30
SNR	Signal-to-noise ratio	vs Frequency	31
	Closed loop respone		32–35
P_O	Output power	vs Load resistance	36, 37
P_D	Power dissipation	vs Output power	38, 39
		vs Ambient temperature	40

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

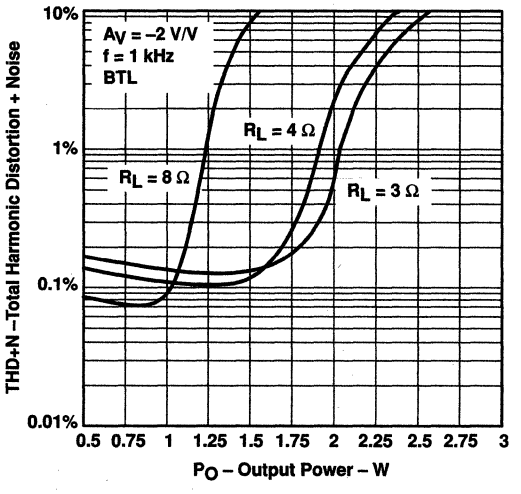


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

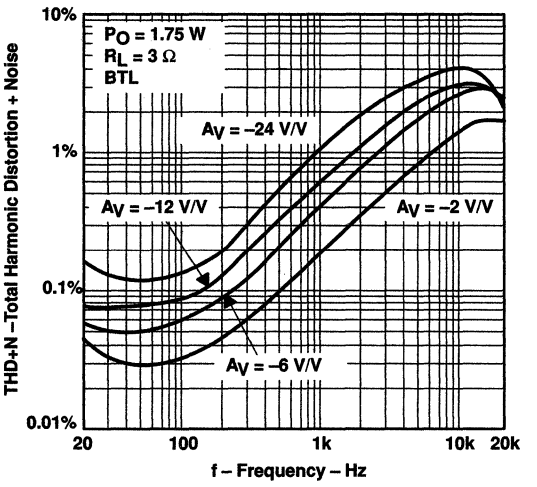


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

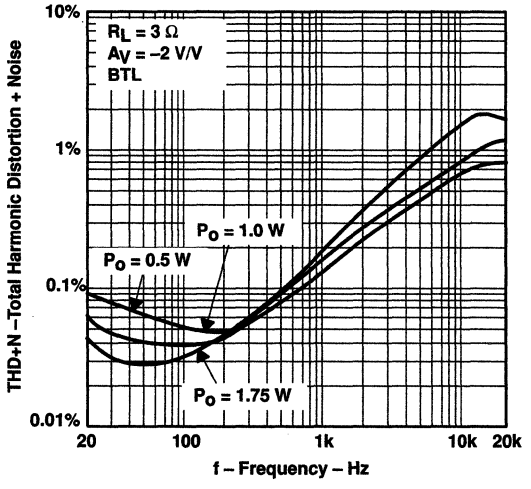


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

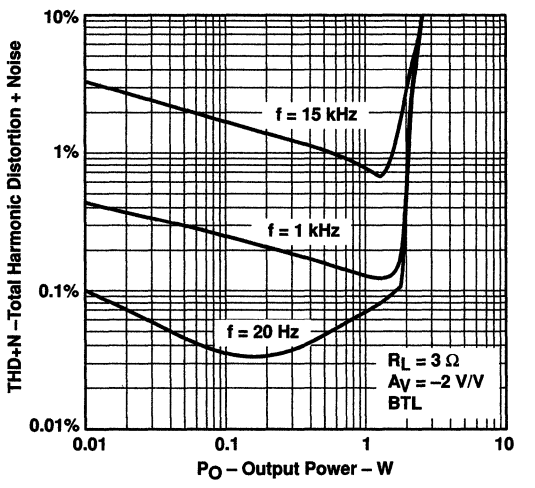


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

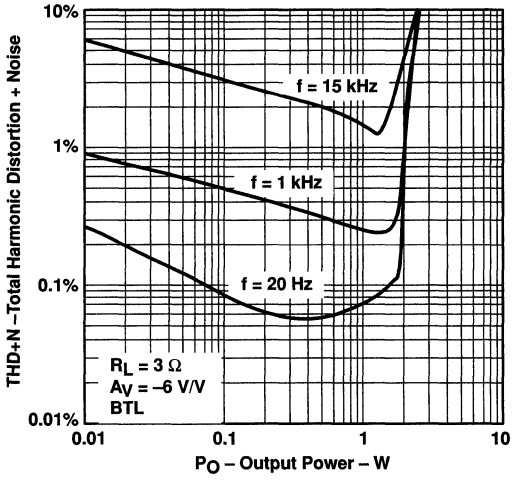


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

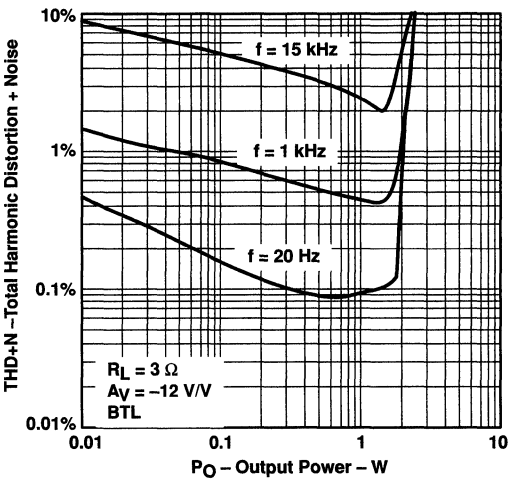


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

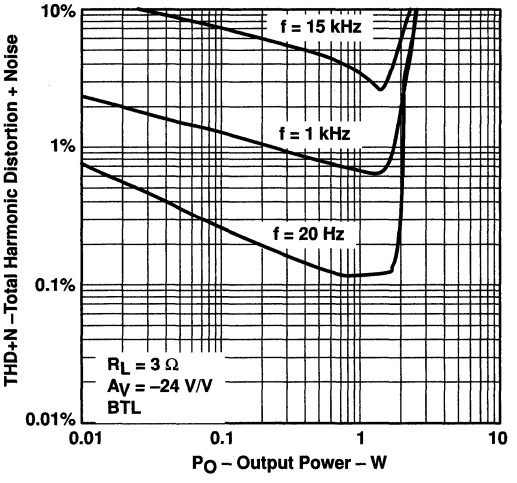


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

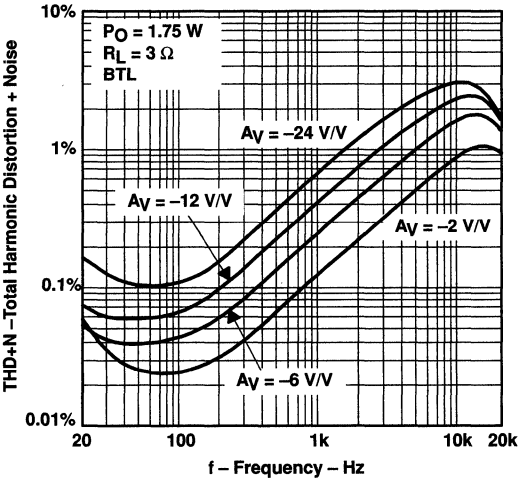


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

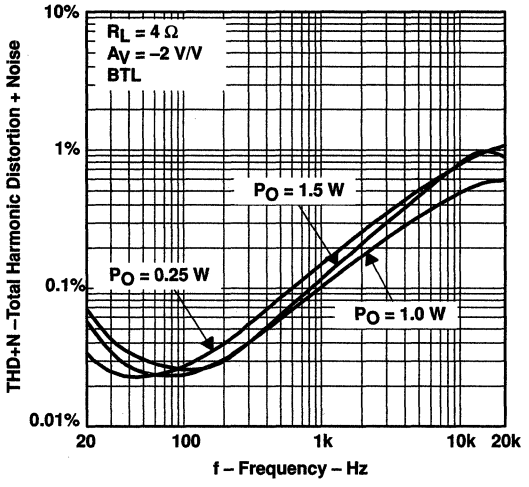


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

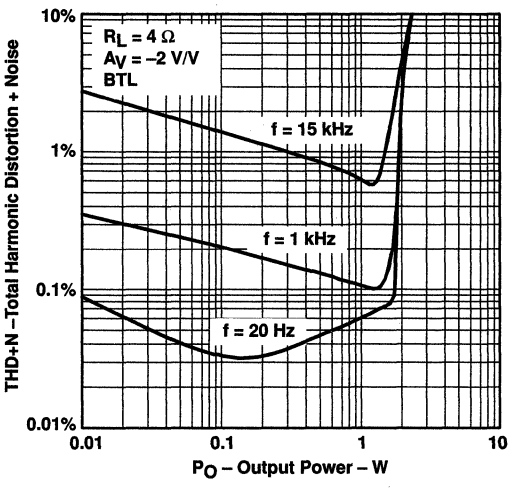


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

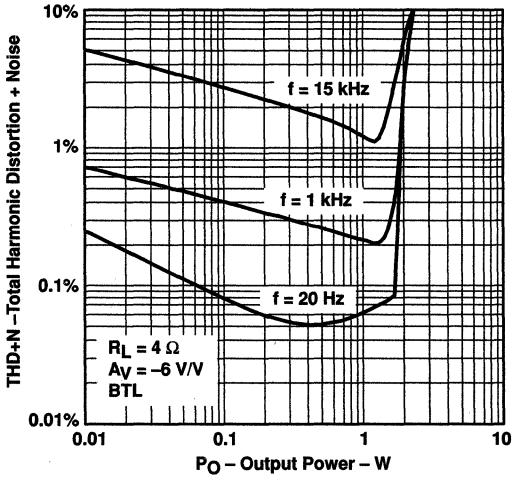


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

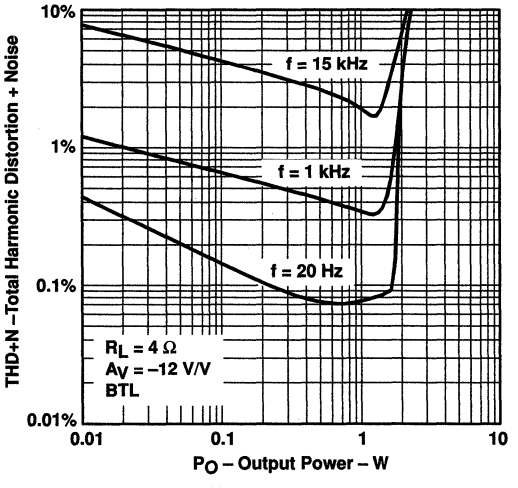


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

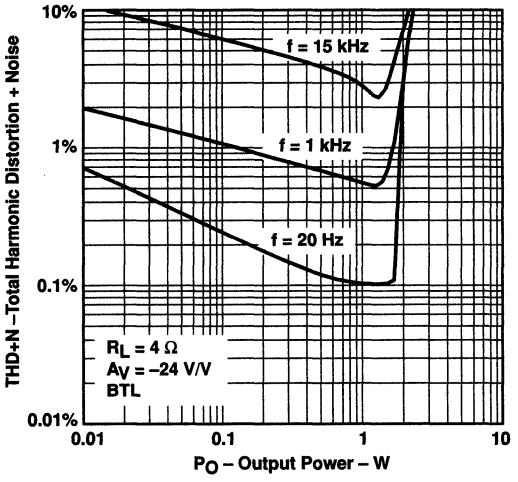


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

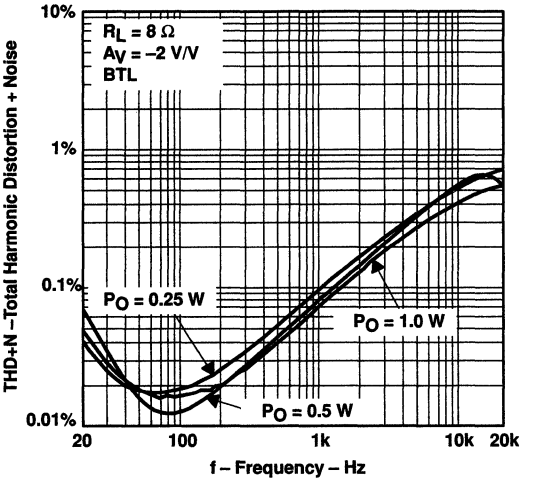


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

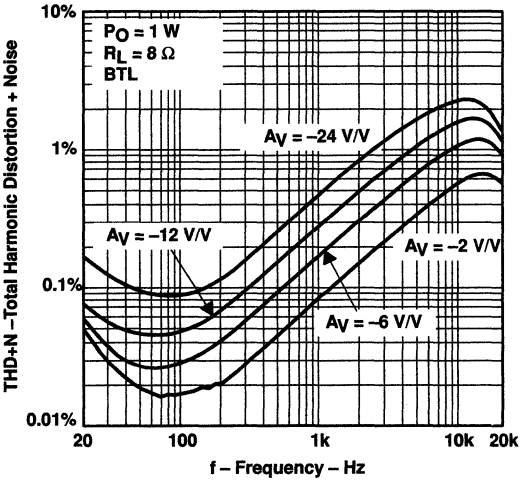


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

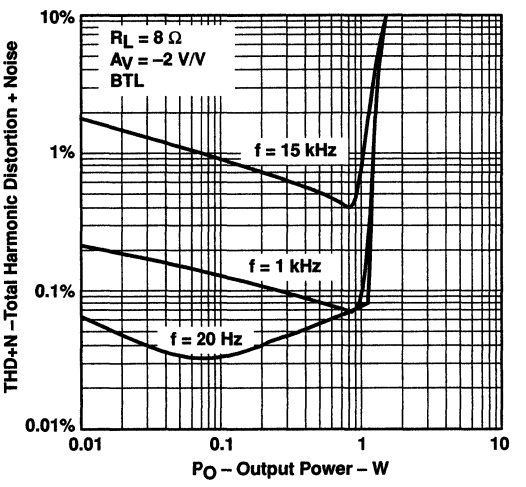


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

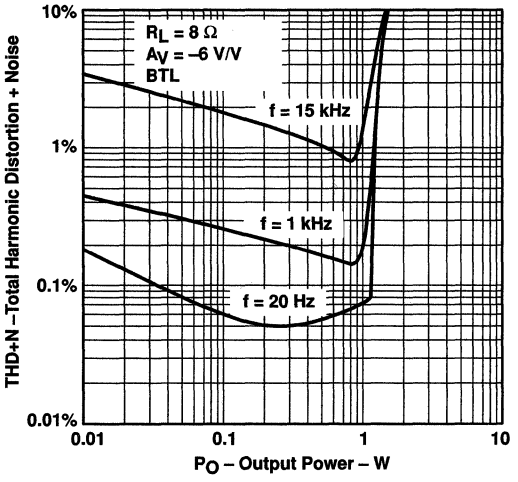


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

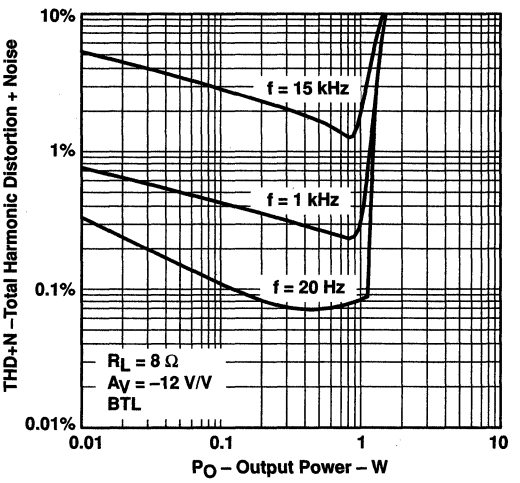


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

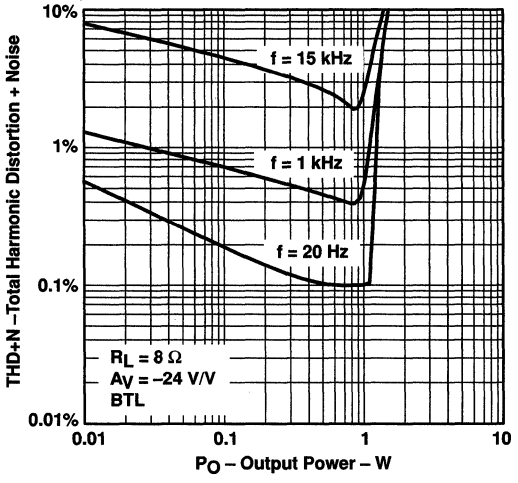


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

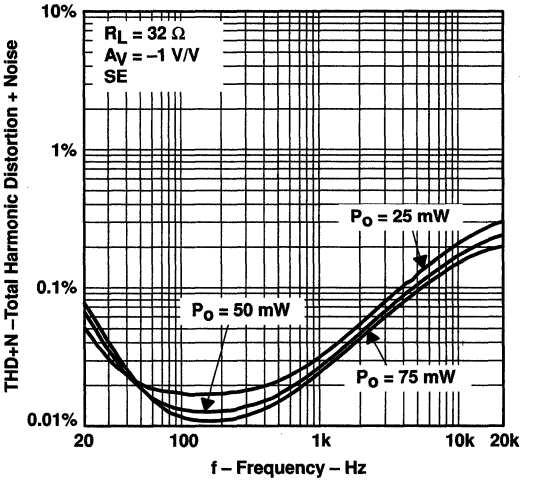


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

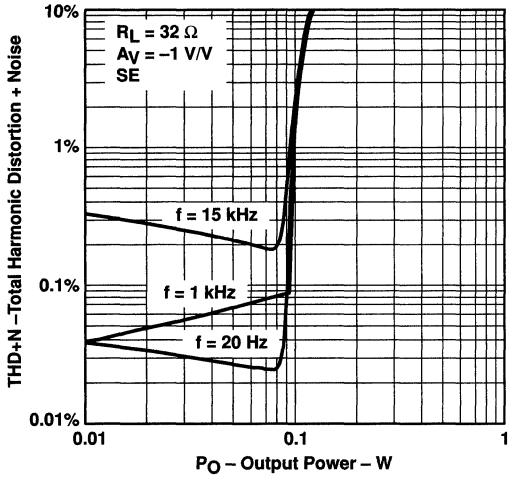


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

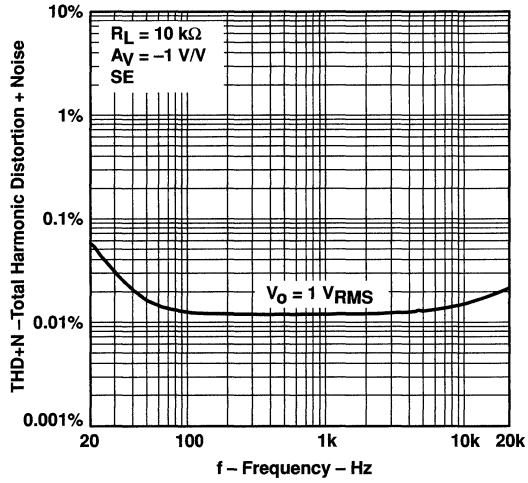


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

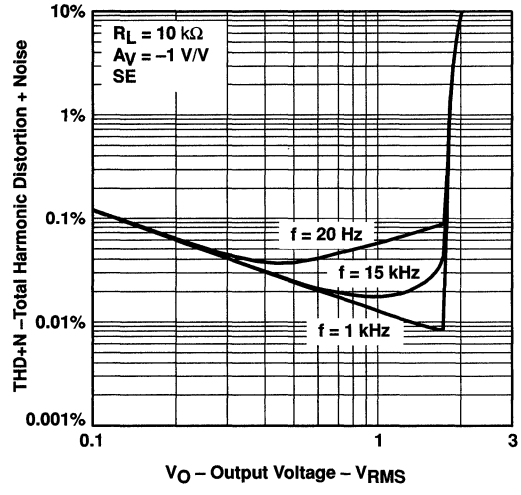


Figure 23

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

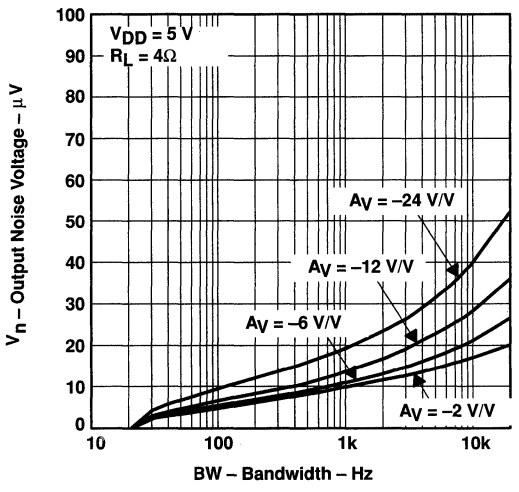


Figure 24

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

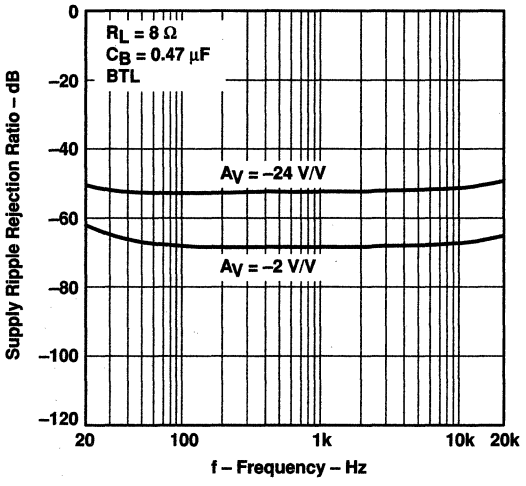


Figure 25

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

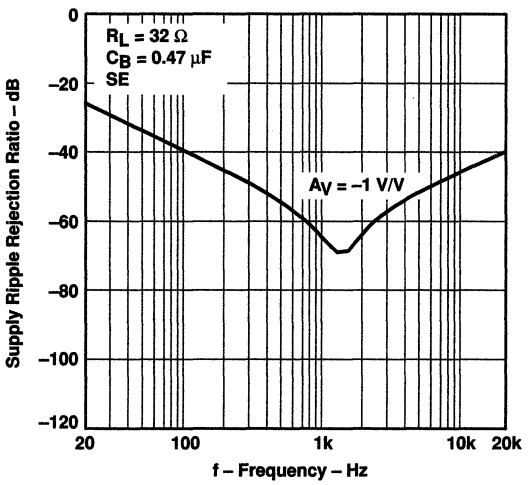


Figure 26

CROSSTALK
vs
FREQUENCY

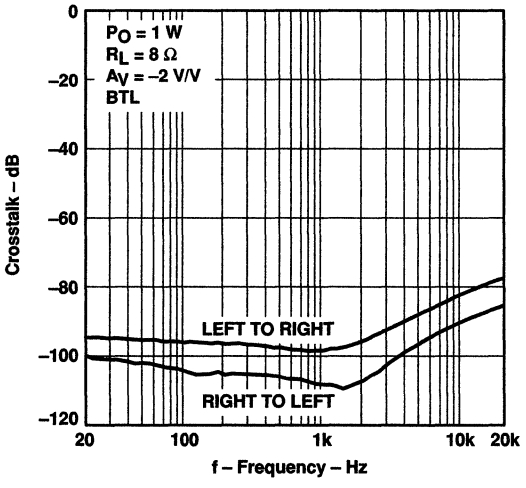


Figure 27

CROSSTALK
vs
FREQUENCY

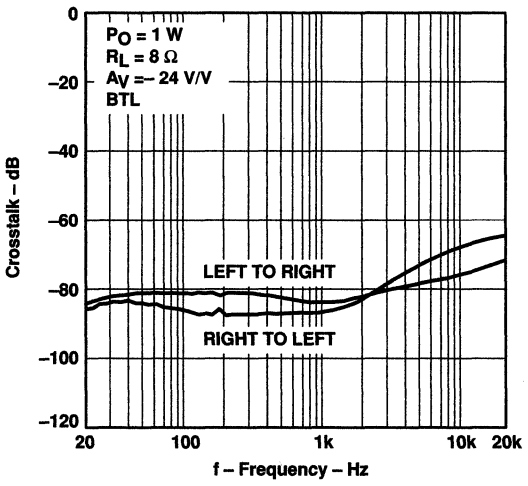


Figure 28

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

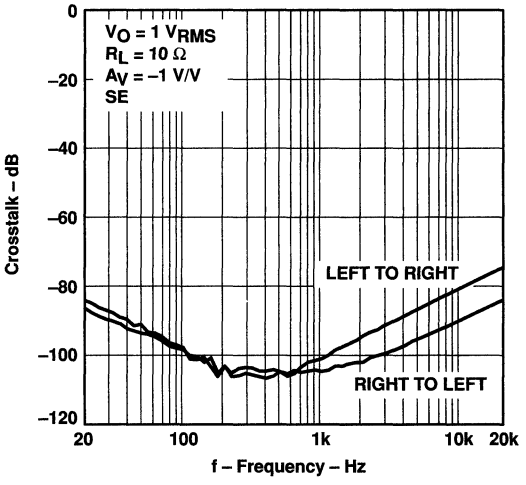


Figure 29

SHUTDOWN ATTENUATION
vs
FREQUENCY

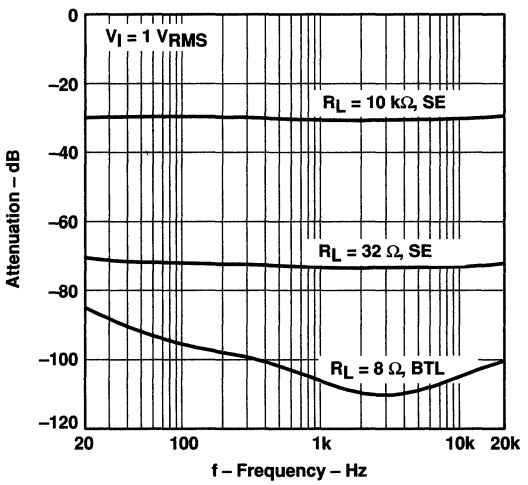


Figure 30

SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

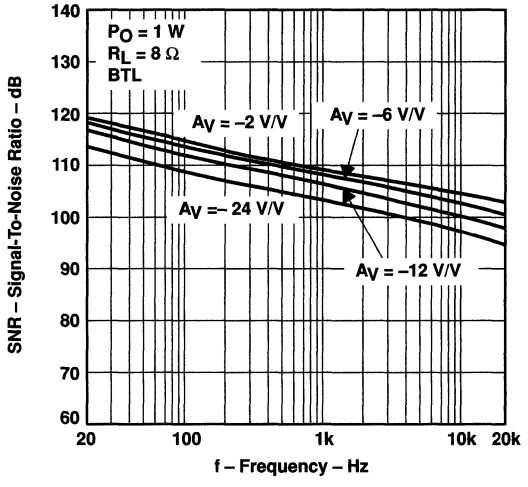


Figure 31

TYPICAL CHARACTERISTICS

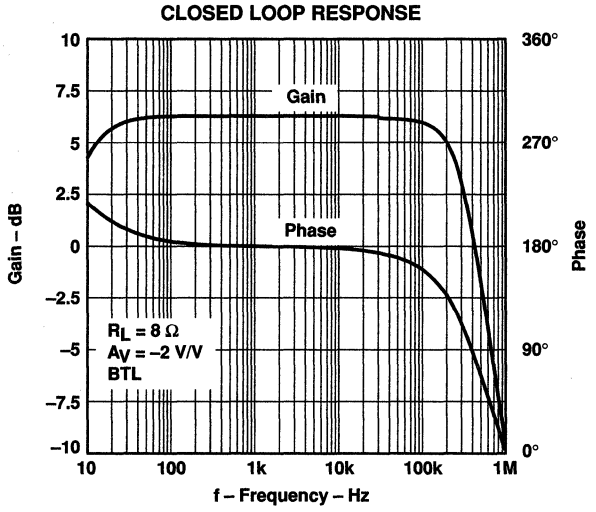


Figure 32

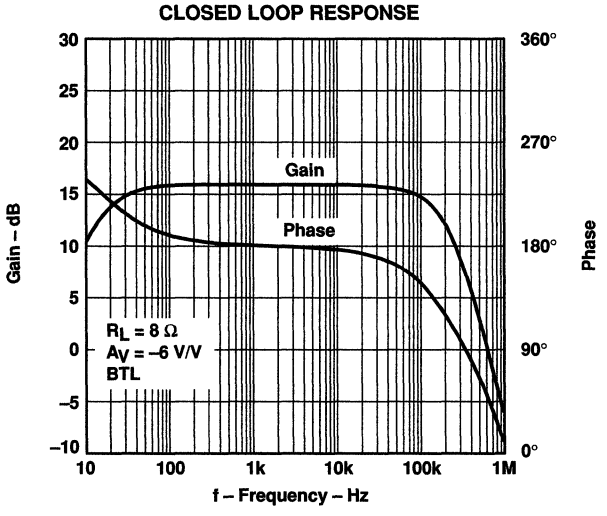


Figure 33

TYPICAL CHARACTERISTICS

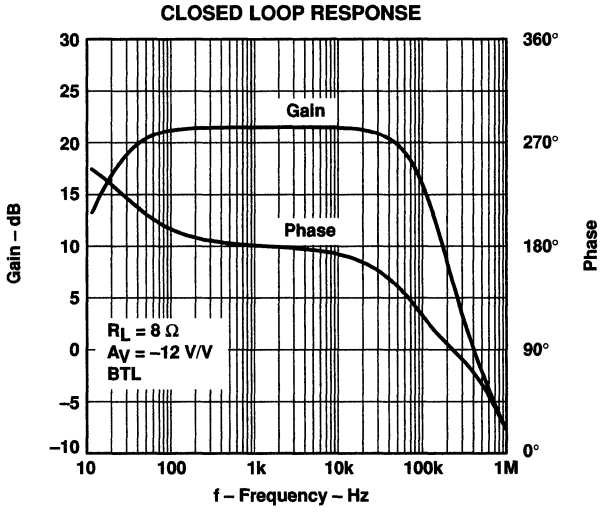


Figure 34

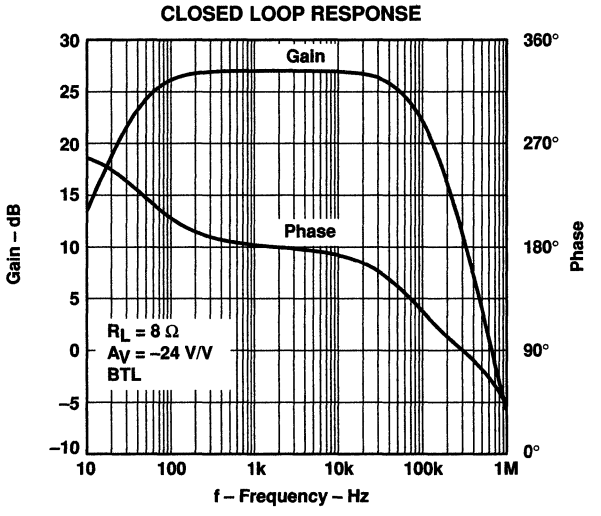


Figure 35

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

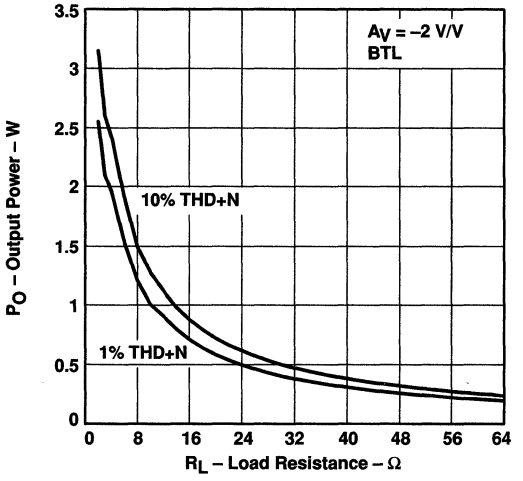


Figure 36

OUTPUT POWER
vs
LOAD RESISTANCE

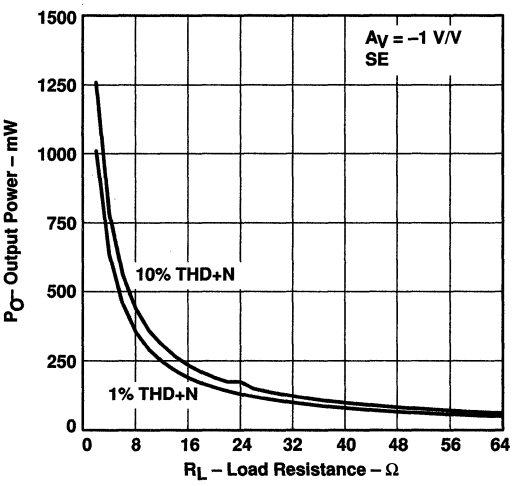


Figure 37

POWER DISSIPATION
vs
OUTPUT POWER

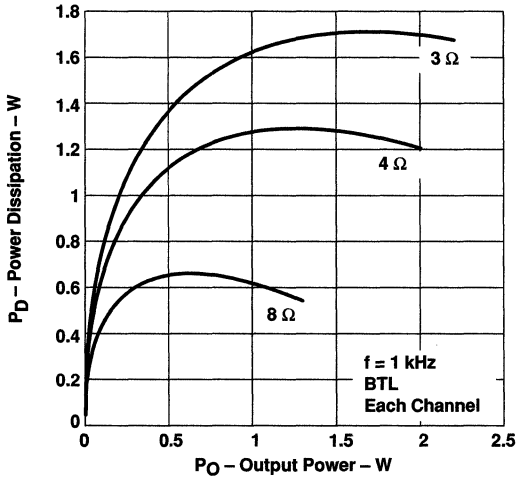


Figure 38

POWER DISSIPATION
vs
OUTPUT POWER

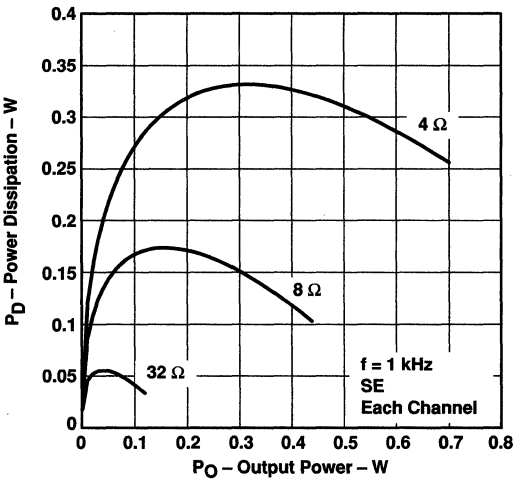


Figure 39

TYPICAL CHARACTERISTICS

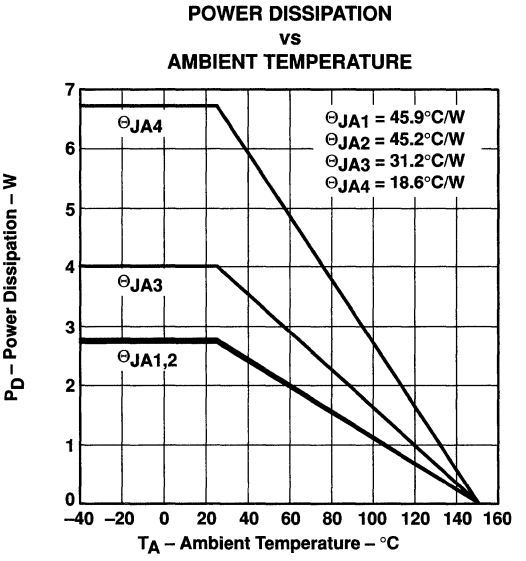


Figure 40

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 41) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

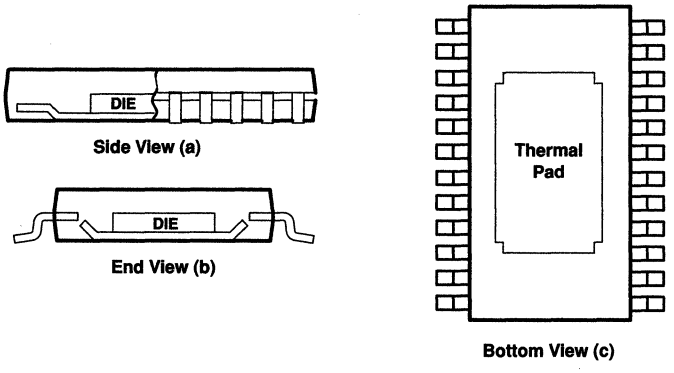
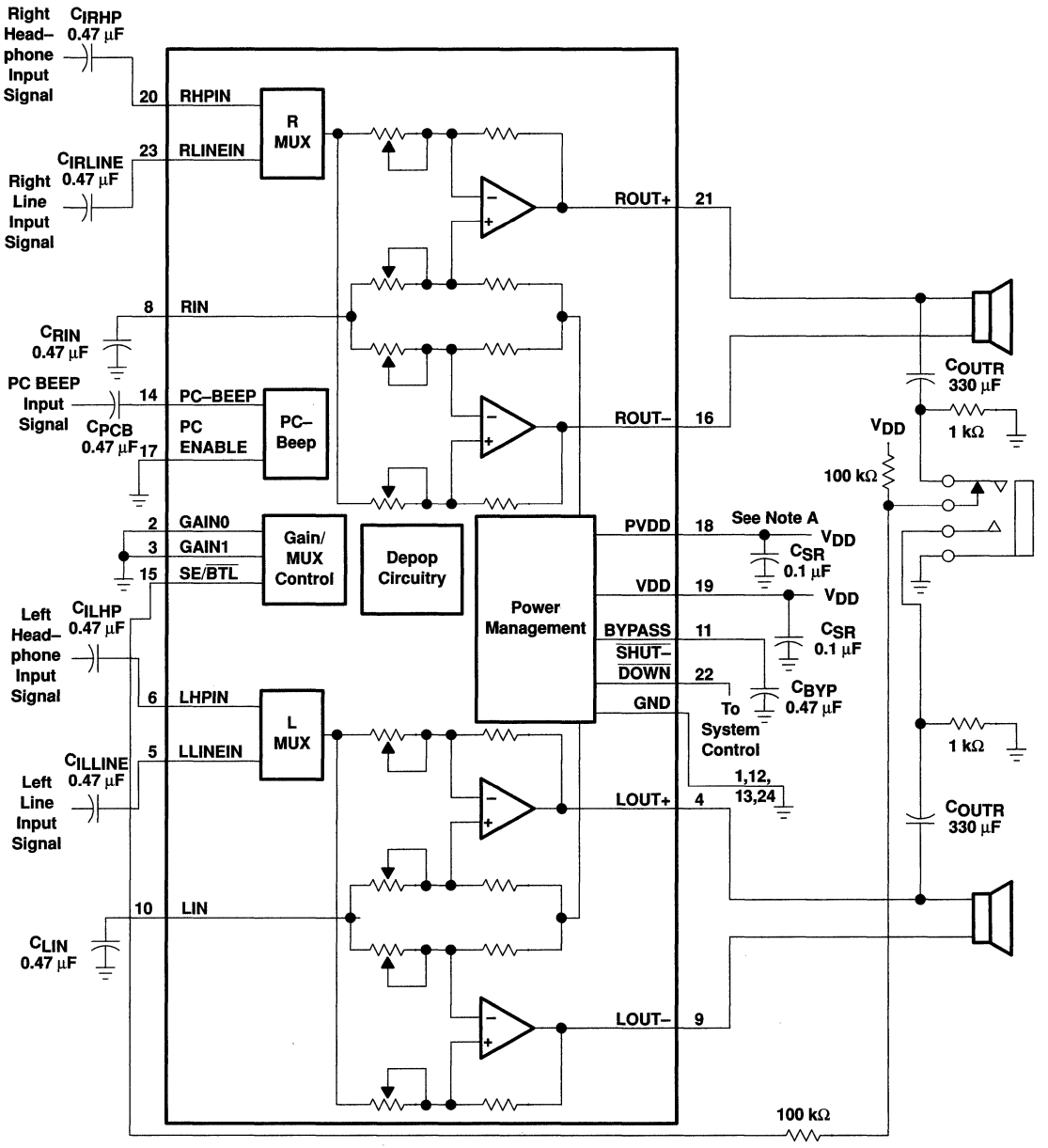


Figure 41. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

selection of components

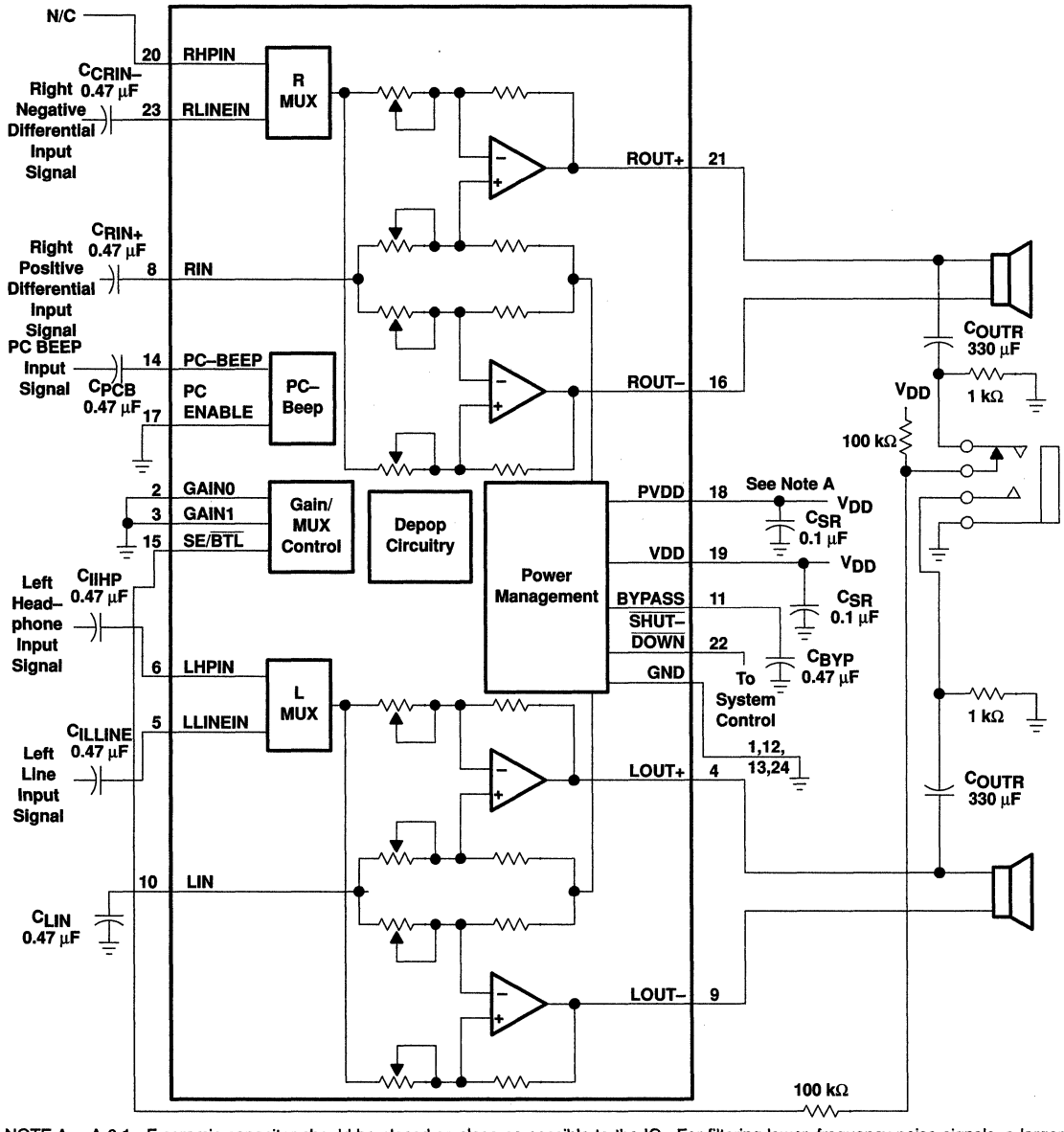
Figure 42 and Figure 43 are a schematic diagrams of typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 42. Typical TPA0112 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 43. Typical TPA0112 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA0112 is set by two input terminals, GAIN0 and GAIN1.

Table 1. Gain Settings

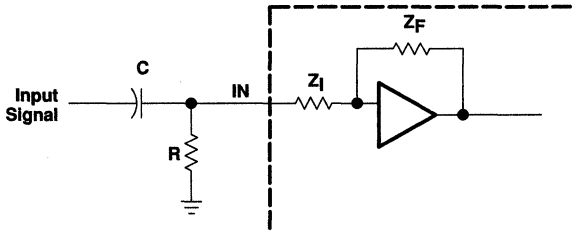
GAIN0	GAIN1	SE/$\overline{\text{BTL}}$	A_V
0	0	0	–2 V/V
0	1	0	–6 V/V
1	0	0	–12 V/V
1	1	0	–24 V/V
X	X	1	–1 V/V

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependant on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA0112. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The input impedance at each gain setting is given in the table below:

A_V	Z_I
–24 V/V	14 kΩ
–12 V/V	26 kΩ
–6 V/V	45.5 kΩ
–2 V/V	91 kΩ

APPLICATION INFORMATION

The –3 dB frequency can be calculated using equation 1:

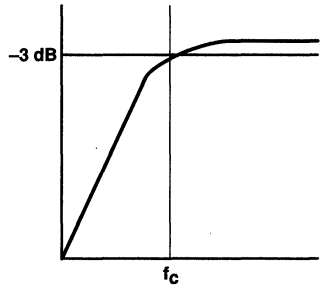
$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA0112 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

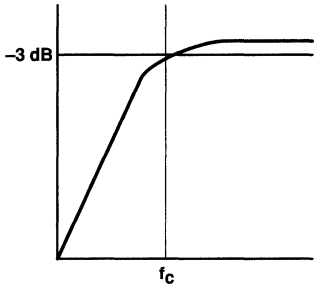
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 44 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0112 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

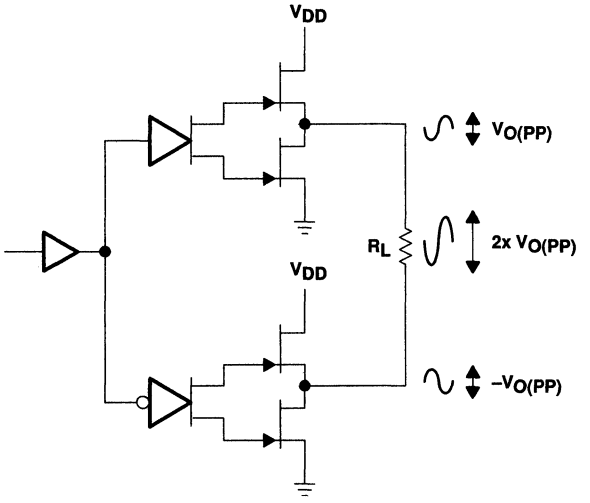


Figure 44. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 45. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

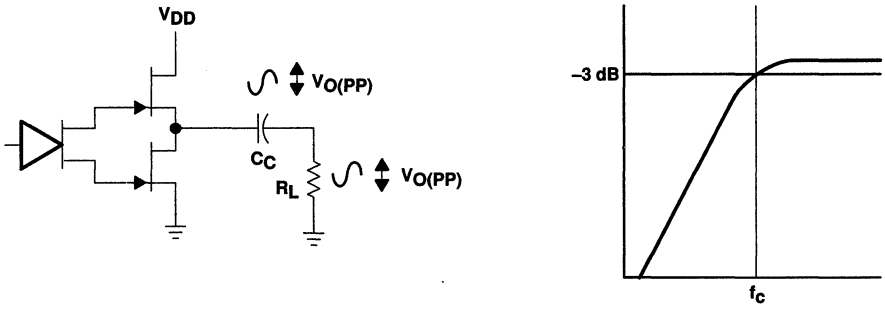


Figure 45. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 44 and Figure 45), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 46).

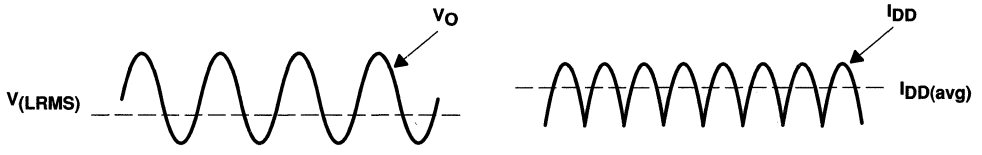


Figure 46. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

APPLICATION INFORMATION

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0112 data sheet, one can see that when the TPA0112 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{10}$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0112 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0112 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 5. TPA0112 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0112 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0112 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0112 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0112, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0112 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0112 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 47.

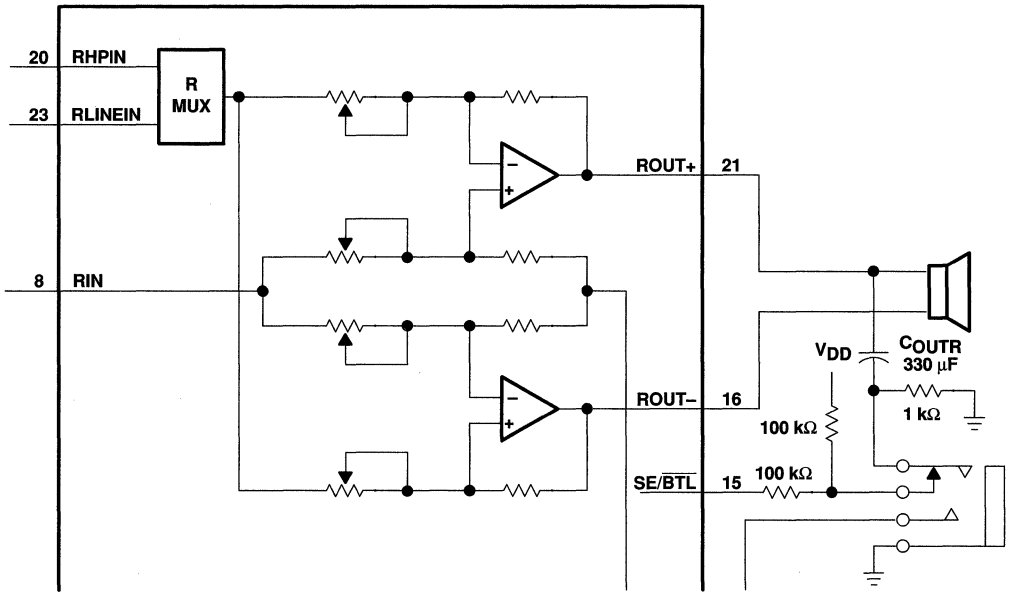


Figure 47. TPA0112 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 μs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy equation 14:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

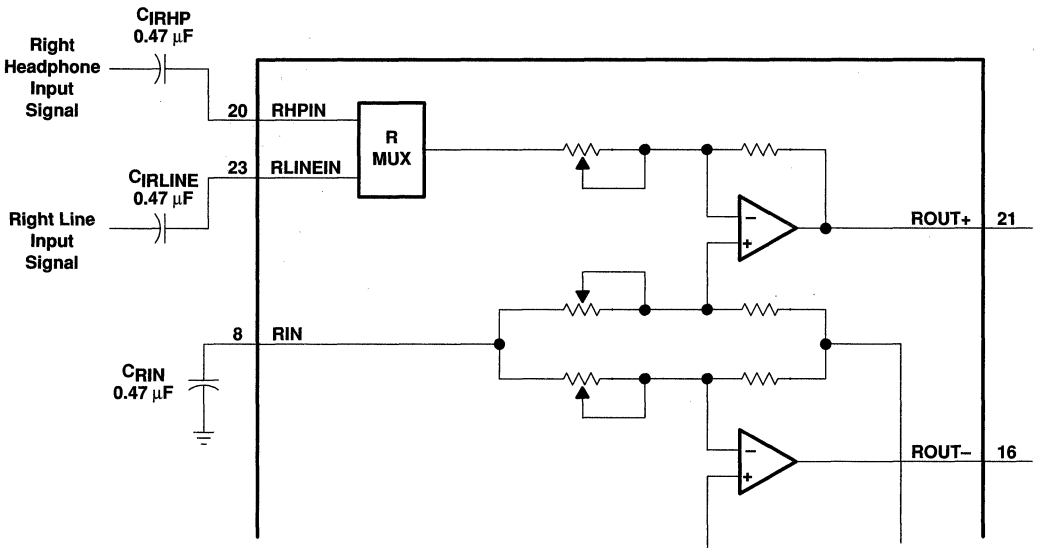


Figure 48. TPA0112 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0112 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

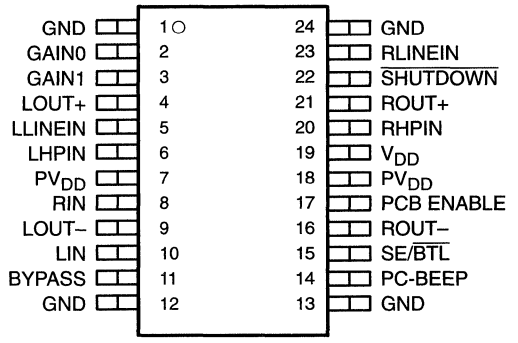
Table 6. Shutdown and Mute Mode Functions

INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0122 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0122 has less than 0.5% THD+N across its specified frequency range.

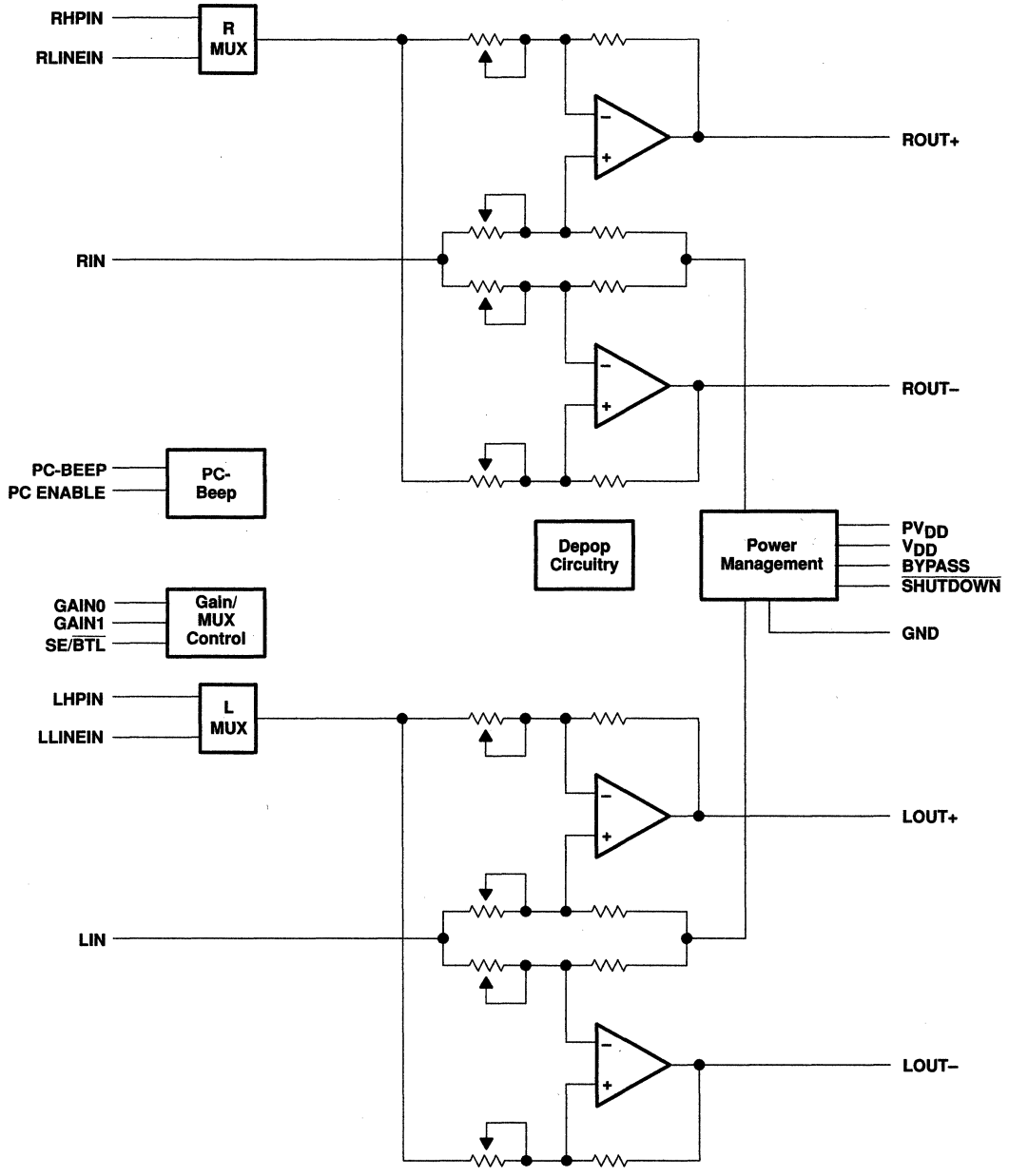
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by two terminals (GAIN0 and GAIN1). BTL gain settings of –2, –6, –12, and –24 V/V are provided, while SE gain is always configured as –1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0122 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and reduces the gain to –1 V/V.

The TPA0122 consumes only 18 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0122 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0122PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0122PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PCB ENABLE	17	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		77		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		18		mA
		SE mode		9		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω	f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.5%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		16		µV RMS
			SE mode		30		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–7, 10–14, 16–19, 21
		vs Frequency	2, 3, 8, 9, 14, 15, 20, 22
		vs Output voltage	23
V_n	Output noise voltage	vs Bandwidth	24
	Supply ripple rejection ratio	vs Frequency	25, 26
	Crosstalk	vs Frequency	27–29
	Shutdown attenuation	vs Frequency	30
SNR	Signal-to-noise ratio	vs Frequency	31
	Closed loop response		32–35
P_O	Output power	vs Load resistance	36, 37
P_D	Power dissipation	vs Output power	38, 39
		vs Ambient temperature	40

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

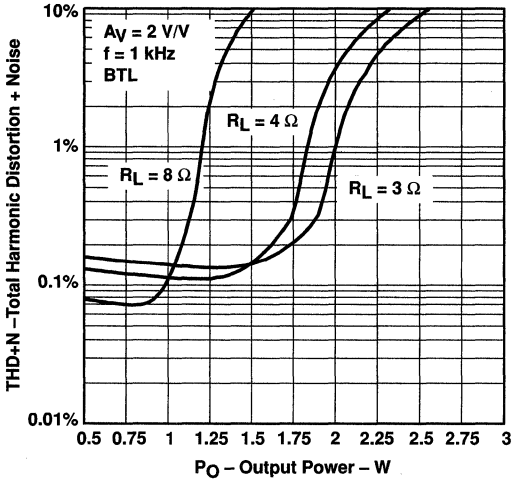


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

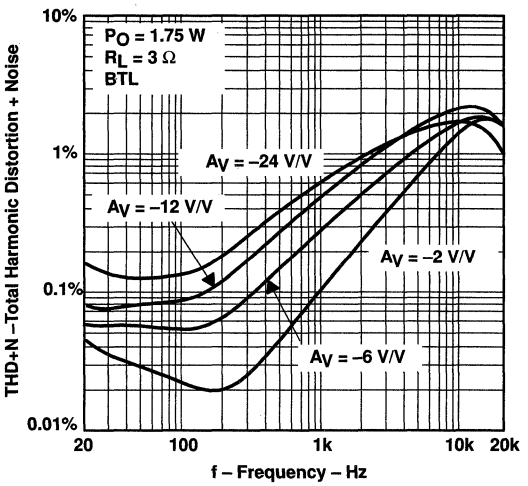


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

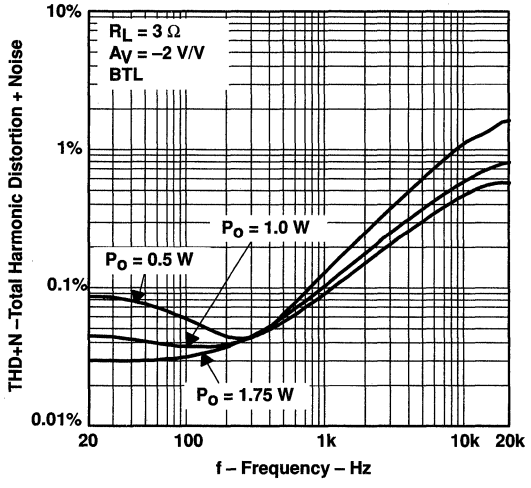


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

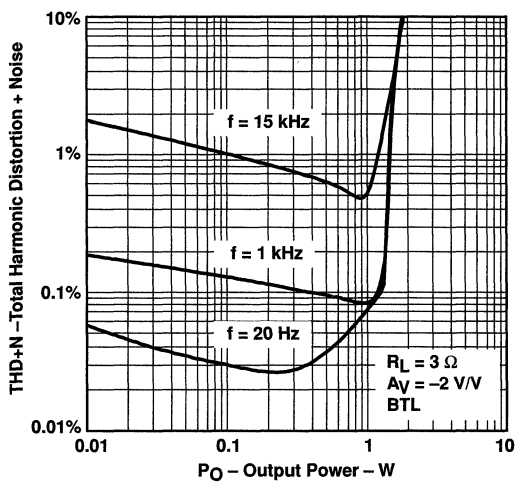


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

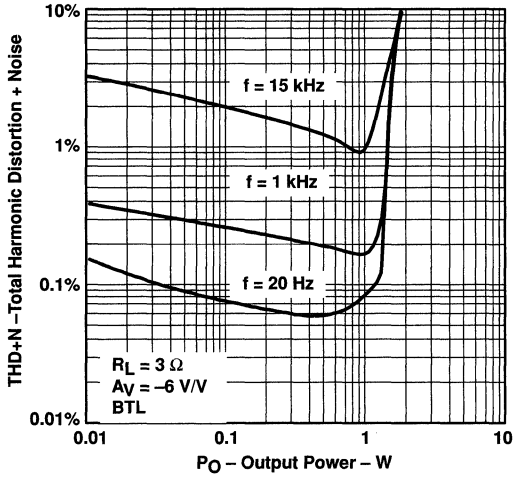


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

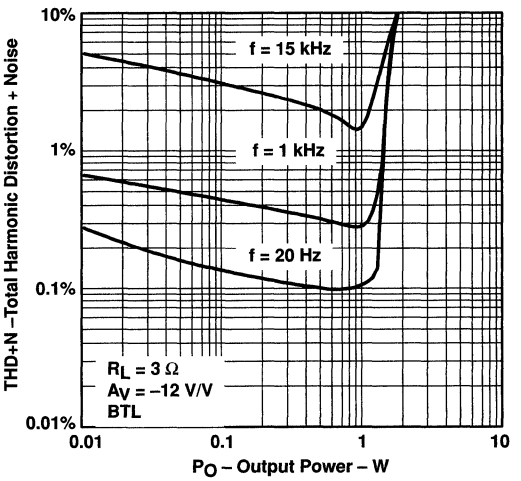


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

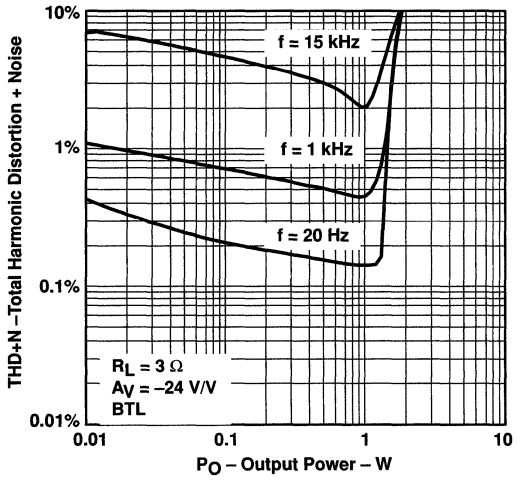


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

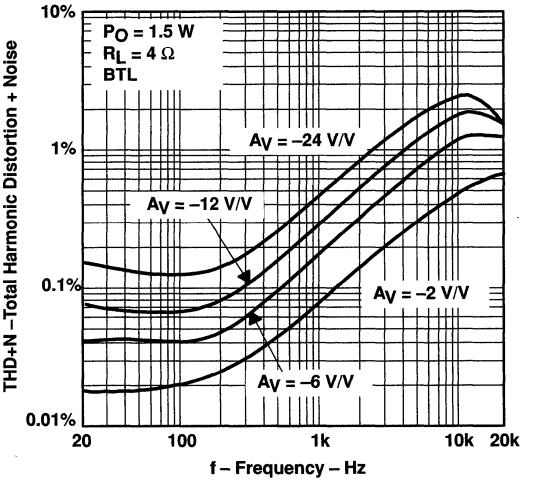


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

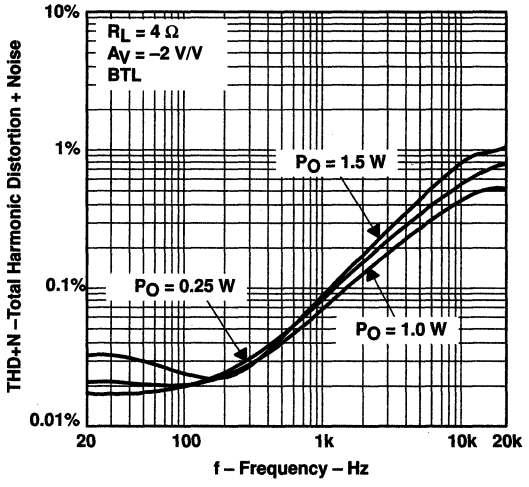


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

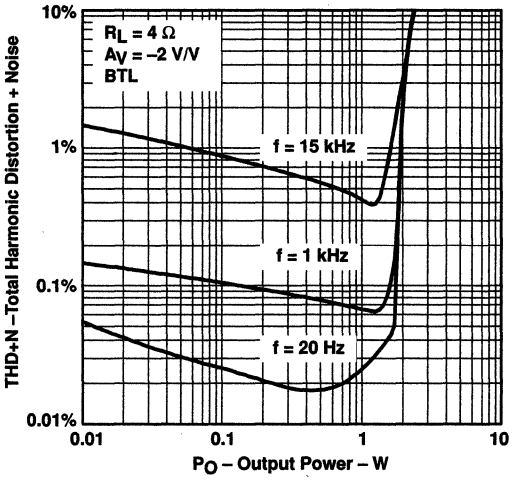


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

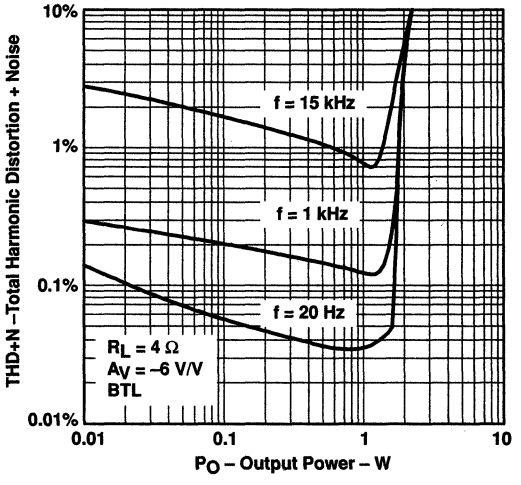


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

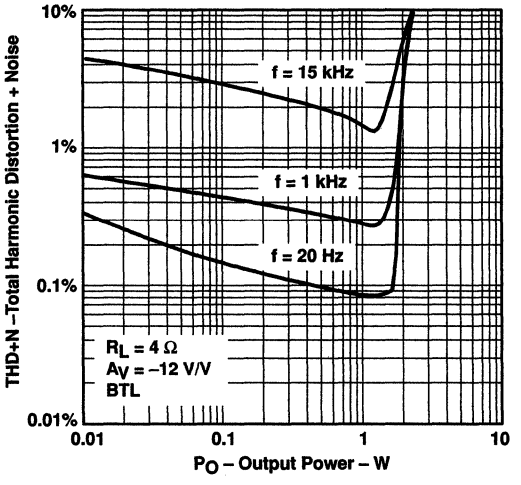


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

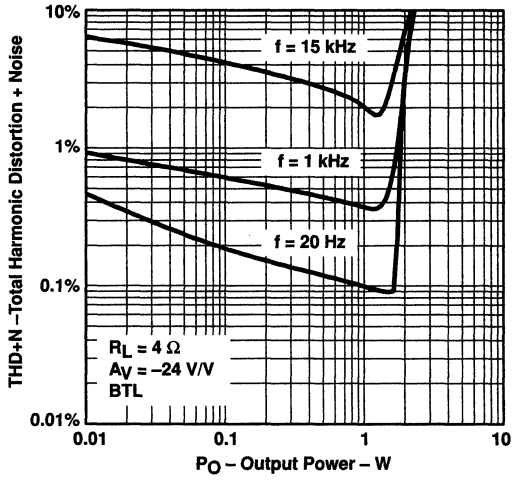


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

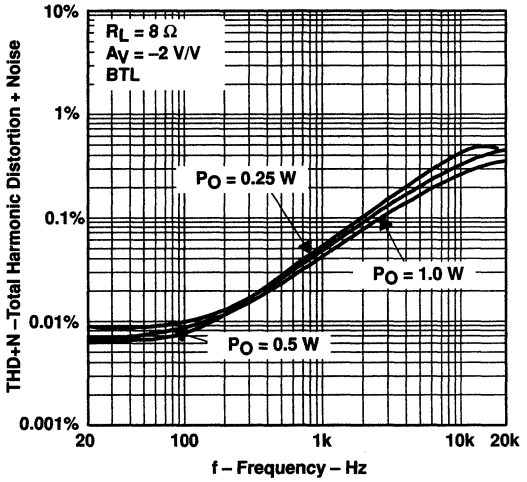


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

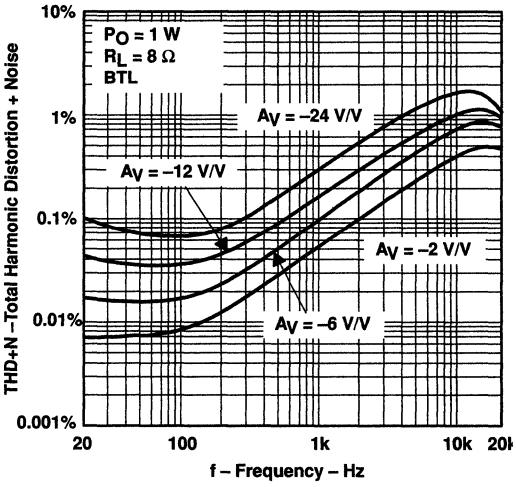


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

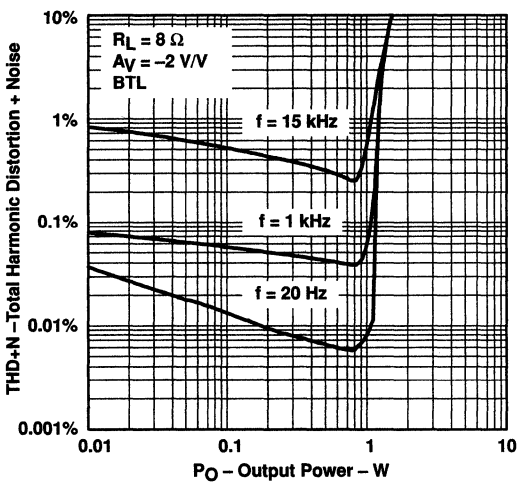


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

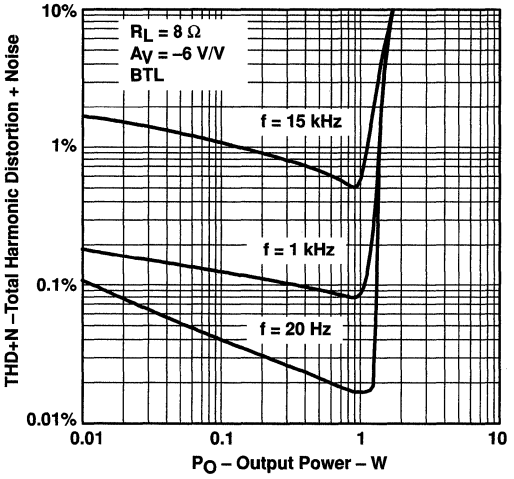


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

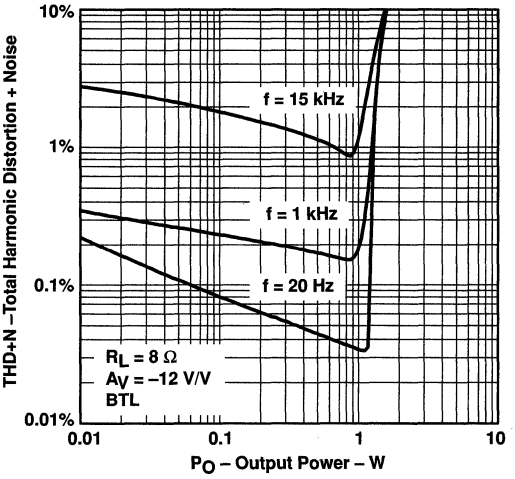


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

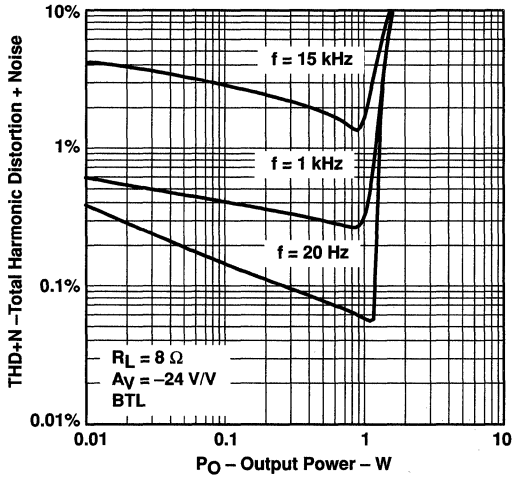


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

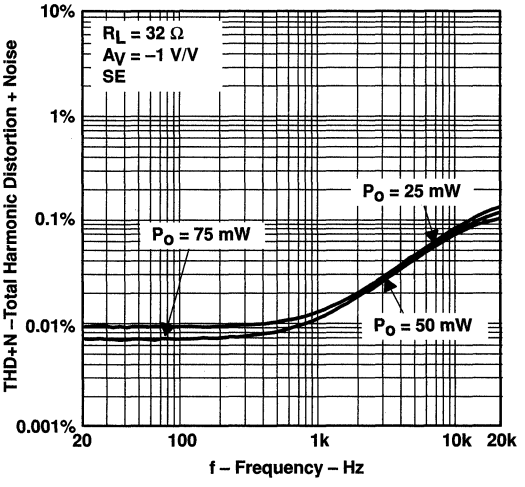


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

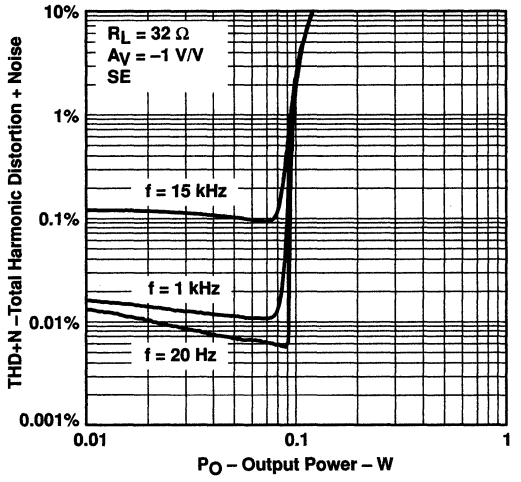


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

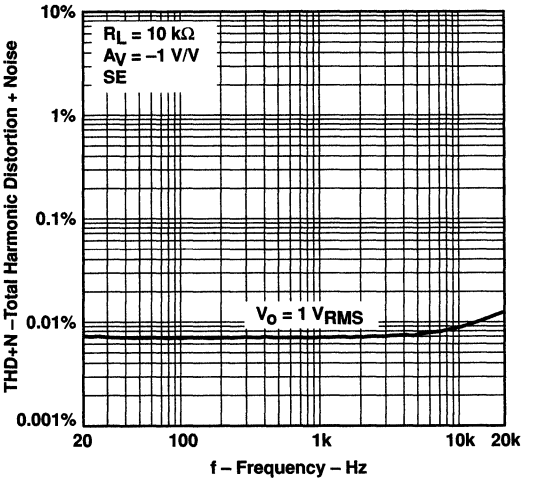


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

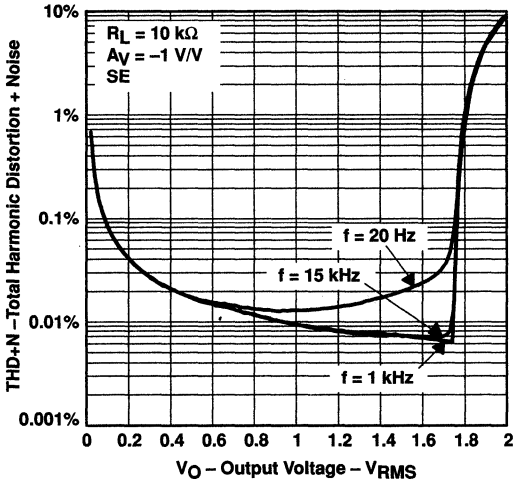


Figure 23

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

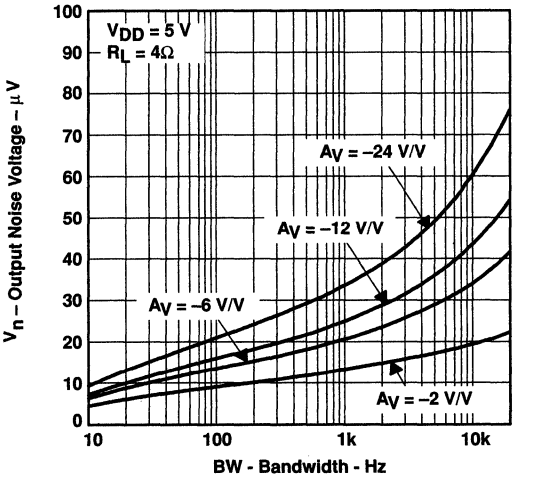


Figure 24

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

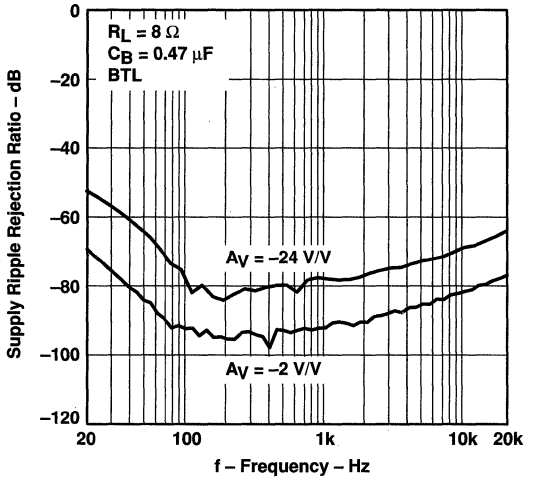


Figure 25

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

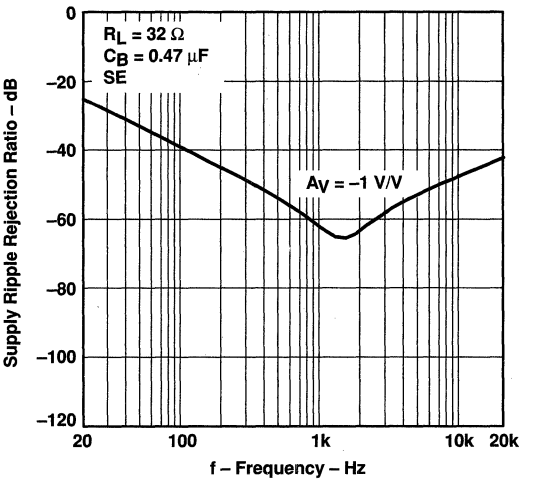


Figure 26

CROSSTALK
vs
FREQUENCY

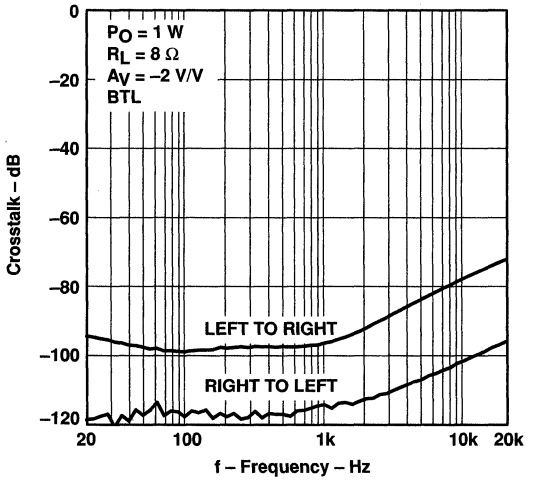


Figure 27

CROSSTALK
vs
FREQUENCY

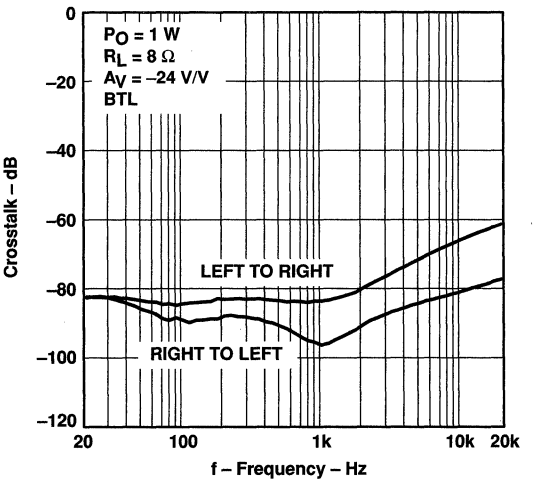


Figure 28

TYPICAL CHARACTERISTICS

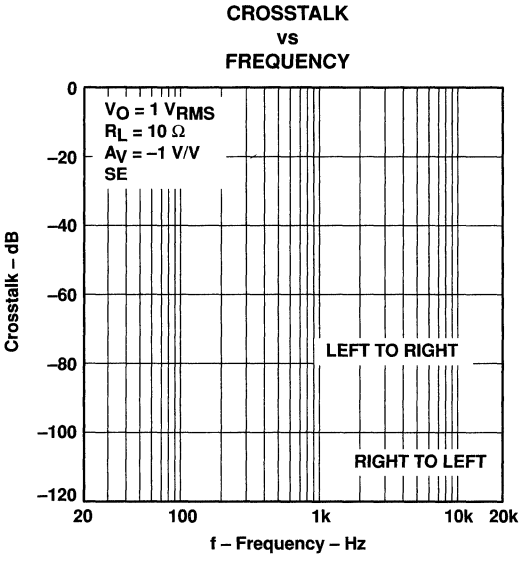


Figure 29

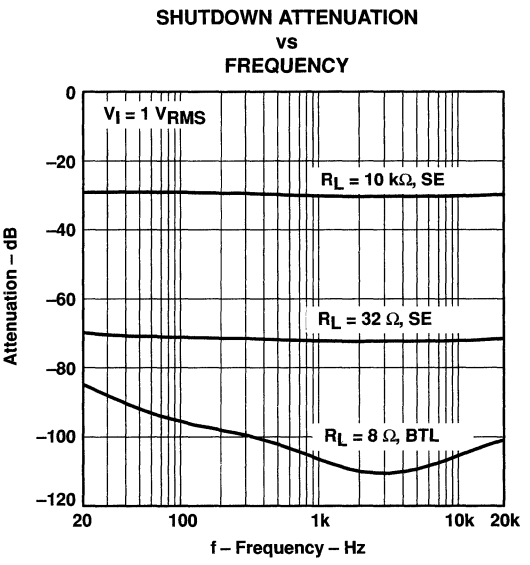


Figure 30

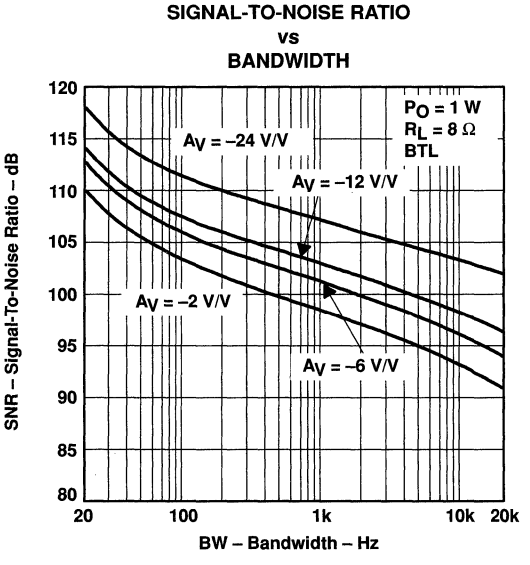


Figure 31

TYPICAL CHARACTERISTICS

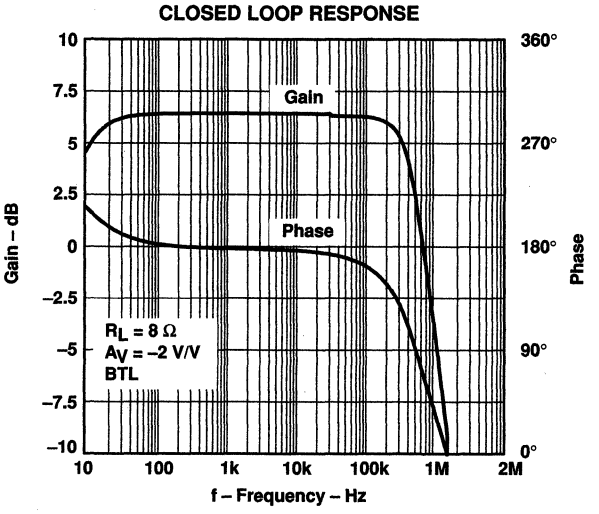


Figure 32

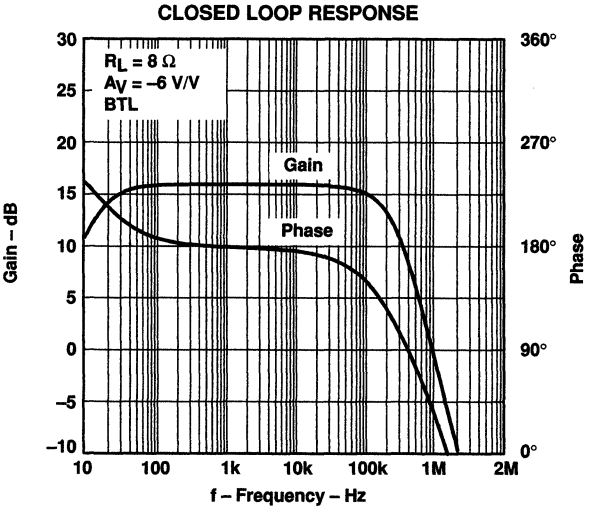


Figure 33

TYPICAL CHARACTERISTICS

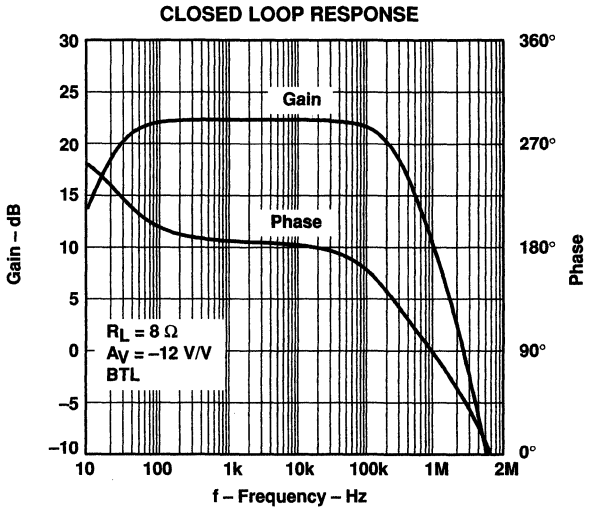


Figure 34

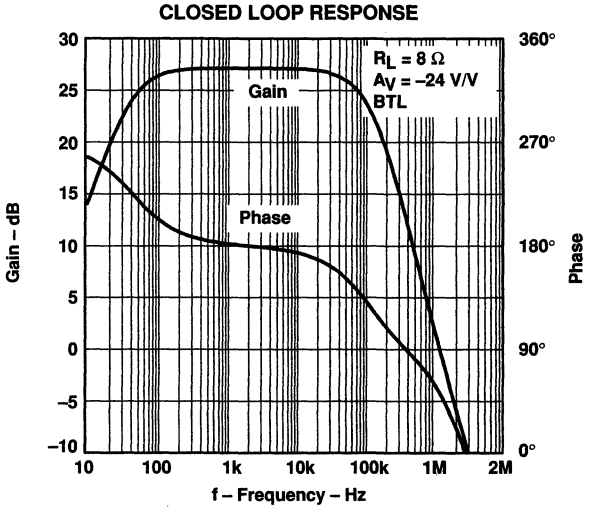


Figure 35

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

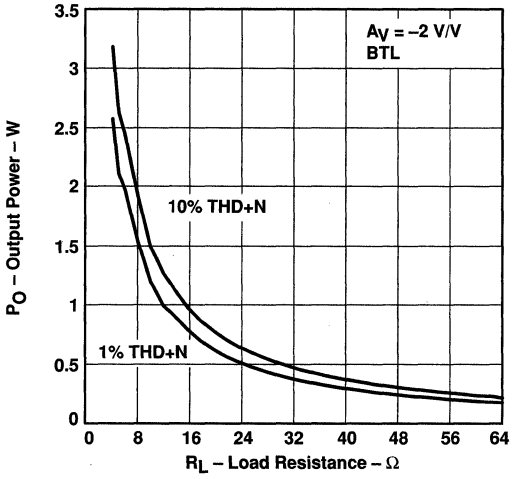


Figure 36

OUTPUT POWER
vs
LOAD RESISTANCE

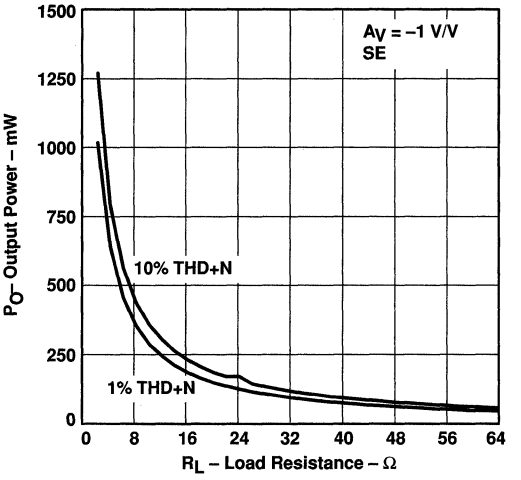


Figure 37

POWER DISSIPATION
vs
OUTPUT POWER

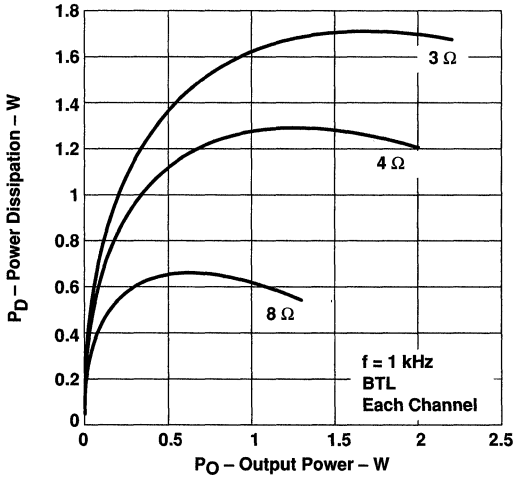


Figure 38

POWER DISSIPATION
vs
OUTPUT POWER

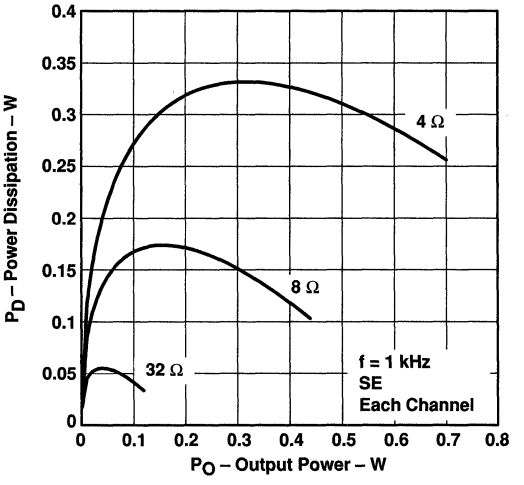


Figure 39

APPLICATION INFORMATION

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

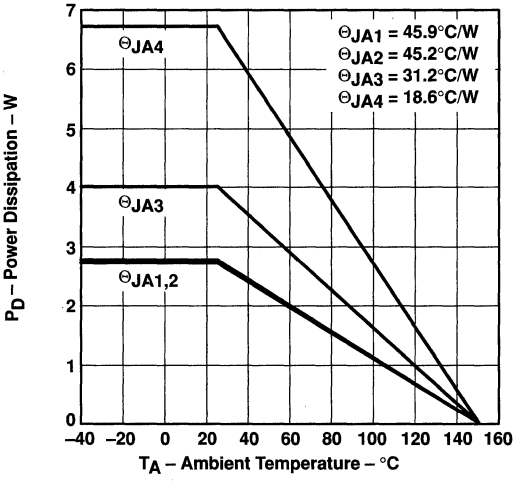


Figure 40

APPLICATION INFORMATION

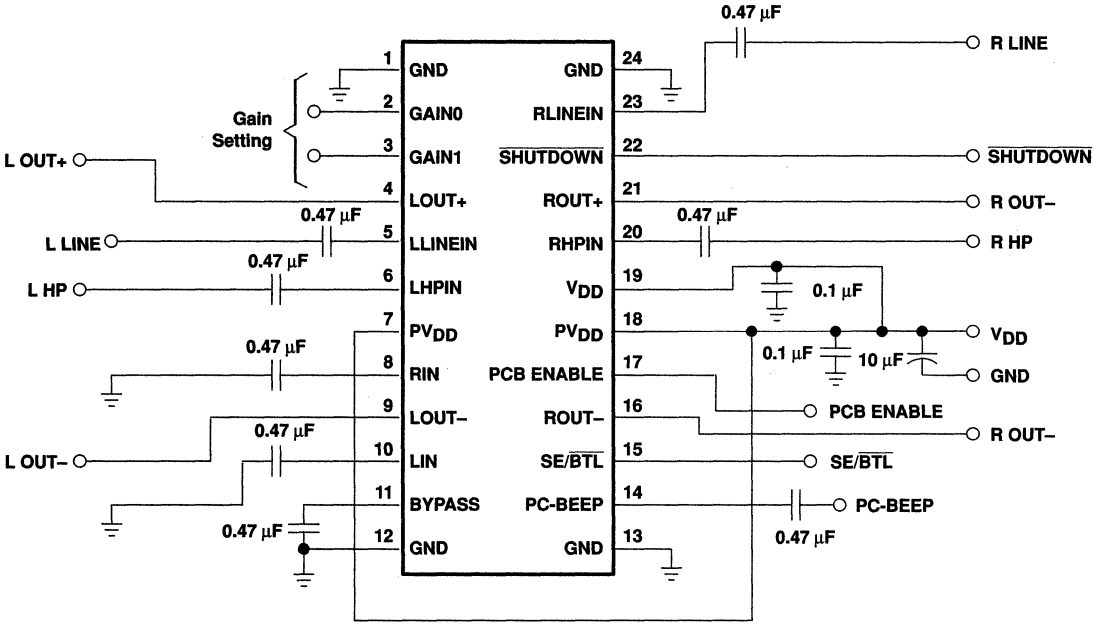
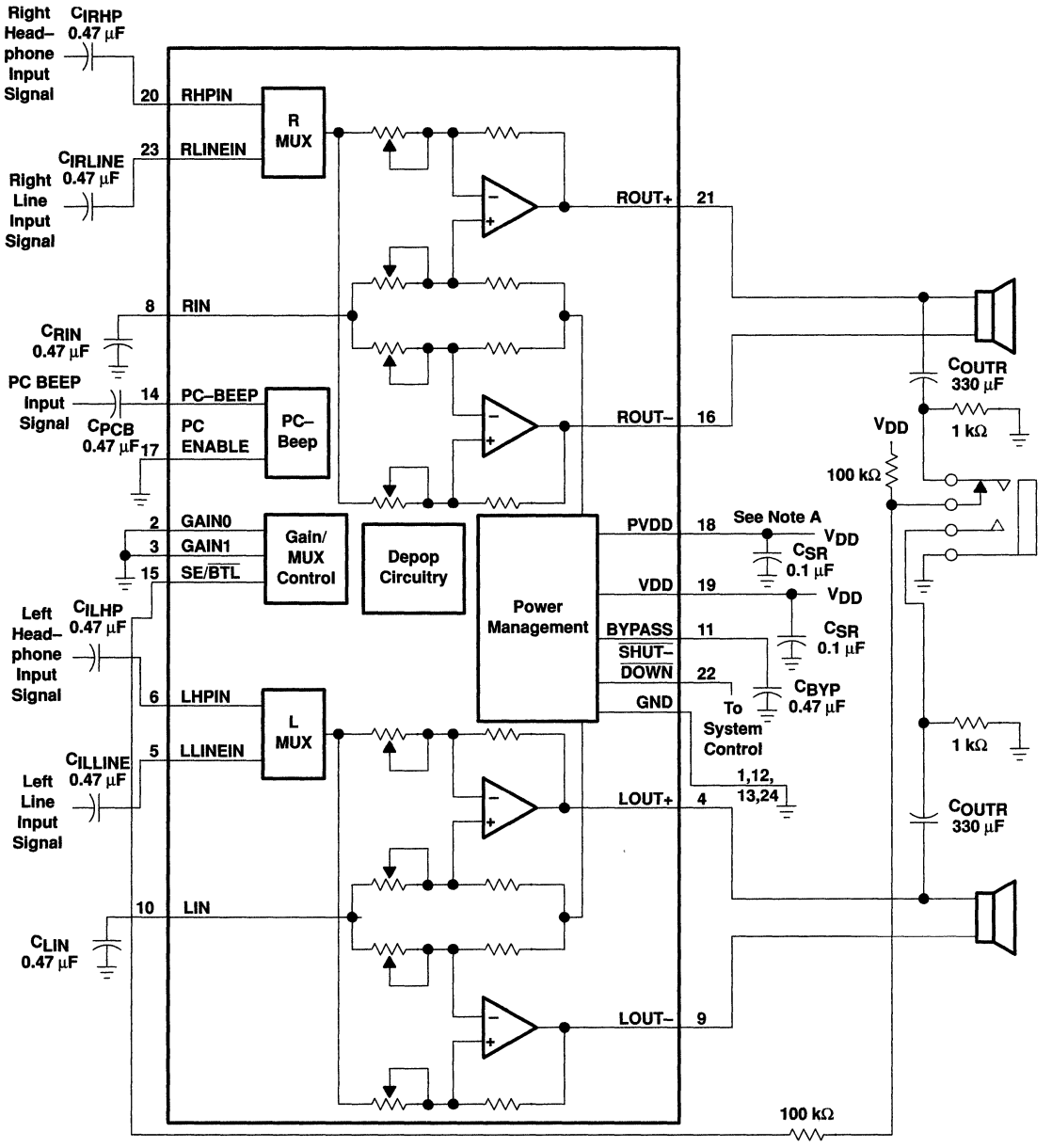


Figure 41. Typical TPA0122 Application Circuit

selection of components

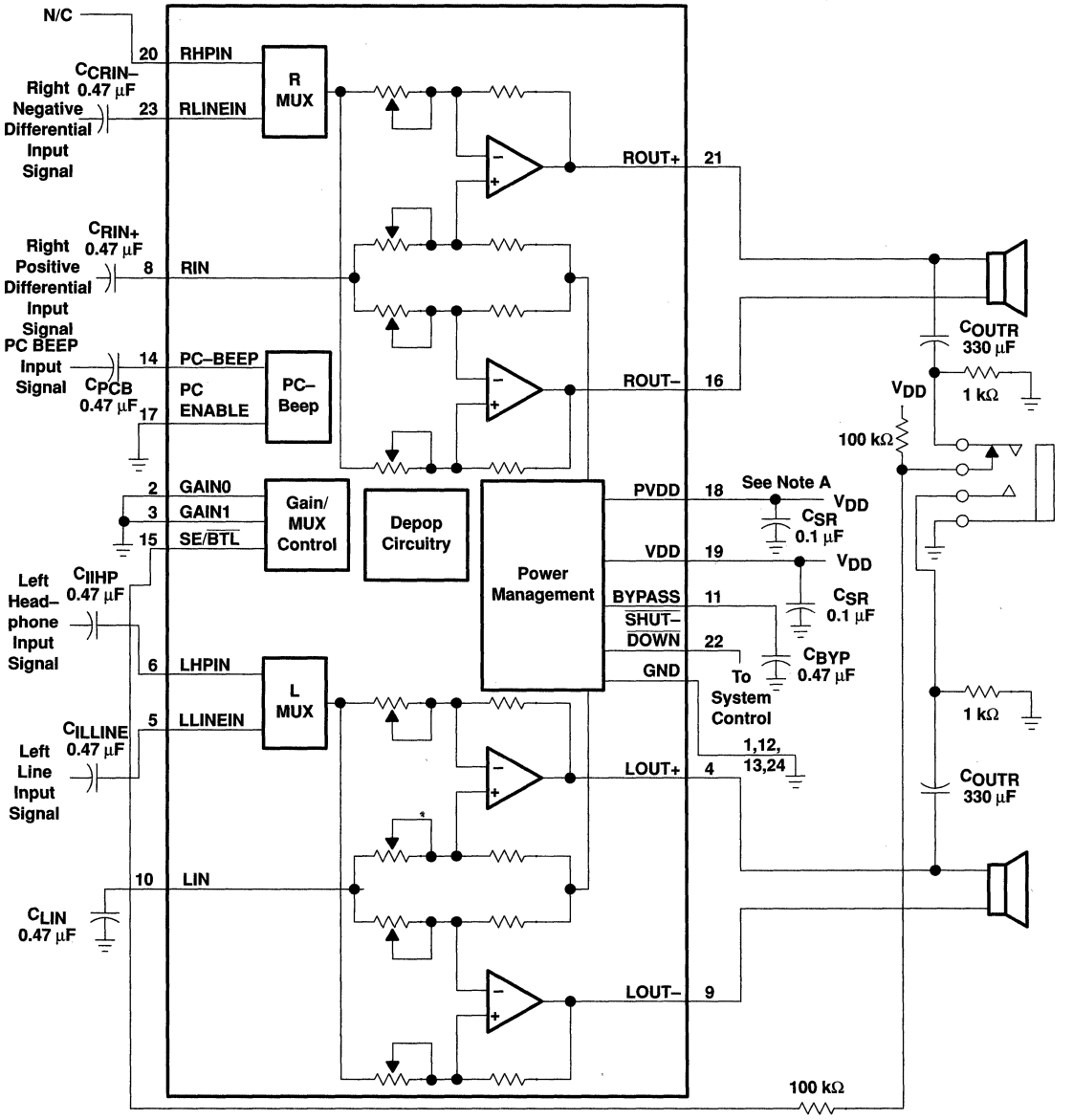
Figure 42 and Figure 43 are a schematic diagrams of typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 42. Typical TPA0122 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 43. Typical TPA0122 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA0122 is set by two input terminals, GAIN0 and GAIN1.

Table 1. Gain Settings

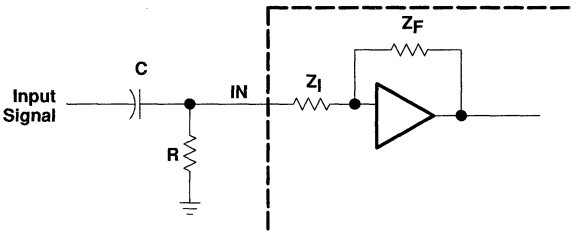
GAIN0	GAIN1	SE/$\overline{BTL}$	A_V
0	0	0	–2 V/V
0	1	0	–6 V/V
1	0	0	–12 V/V
1	1	0	–24 V/V
X	X	1	–1 V/V

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependant on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA0122. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The input resistance at each gain setting is given in the table below:

A_V	Z_I
–24 V/V	14 kΩ
–12 V/V	26 kΩ
–6 V/V	45.5 kΩ
–2 V/V	91 kΩ

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The –3 dB frequency can be calculated using equation 1:

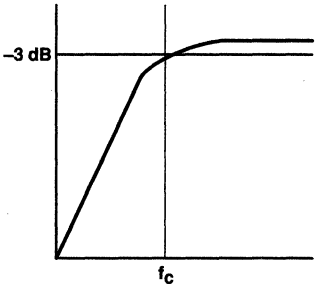
$$f_{-3\,dB} = \frac{1}{2\pi\, C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA0122 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

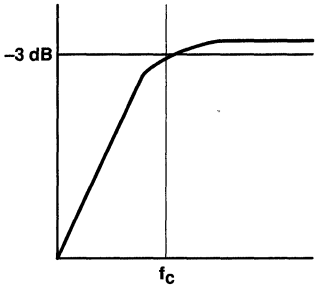
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

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Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 44 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0122 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

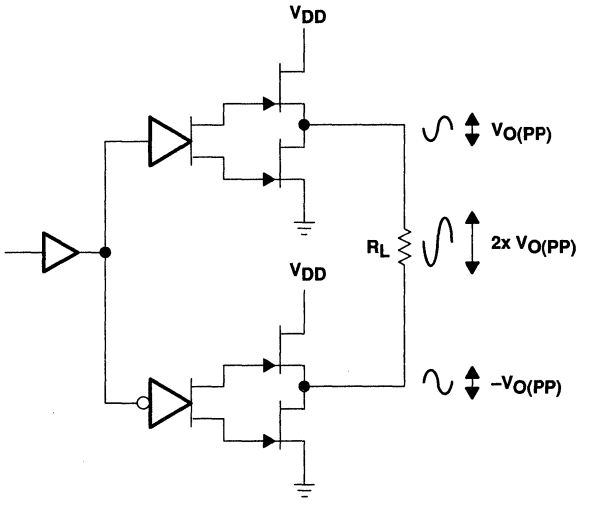


Figure 44. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 45. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

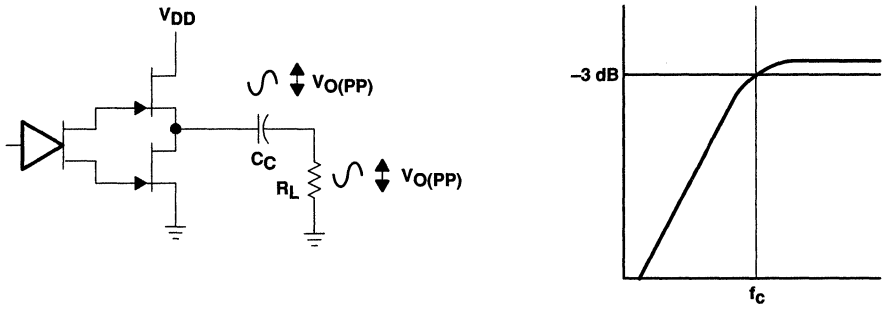


Figure 45. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 44 and Figure 45), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 46).

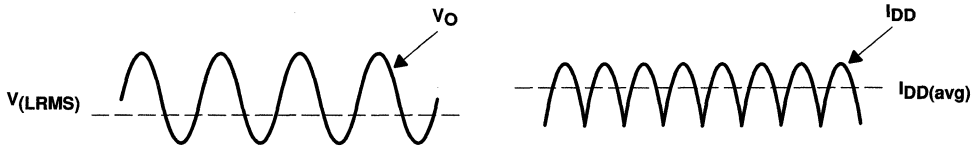


Figure 46. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

APPLICATION INFORMATION

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0122 data sheet, one can see that when the TPA0122 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0122 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0122 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 5. TPA0122 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0122 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$
$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

TableS 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0122 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0122 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0122, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0122 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0122 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 47.

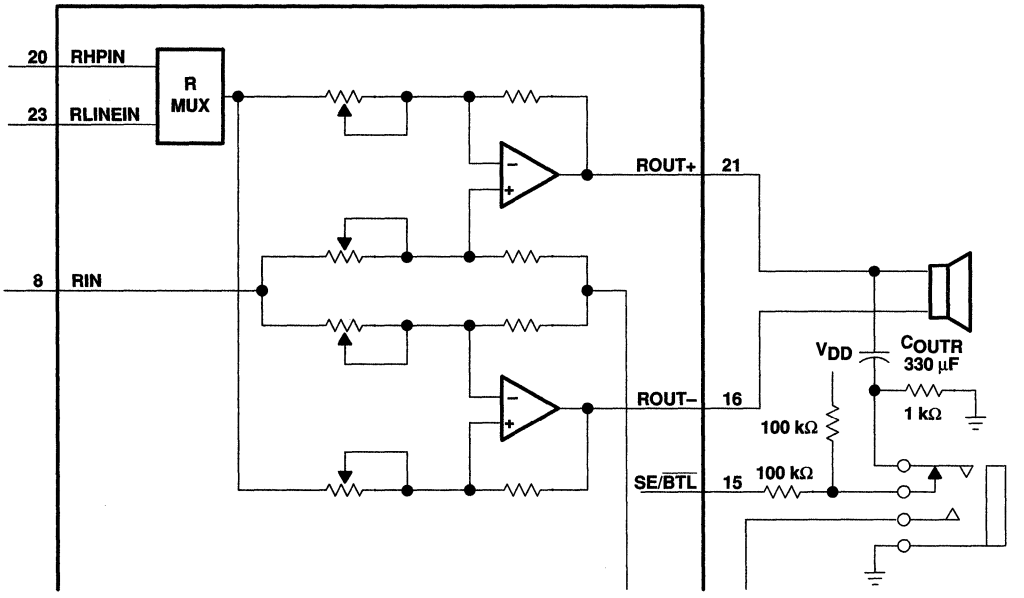


Figure 47. TPA0122 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy equation 14:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

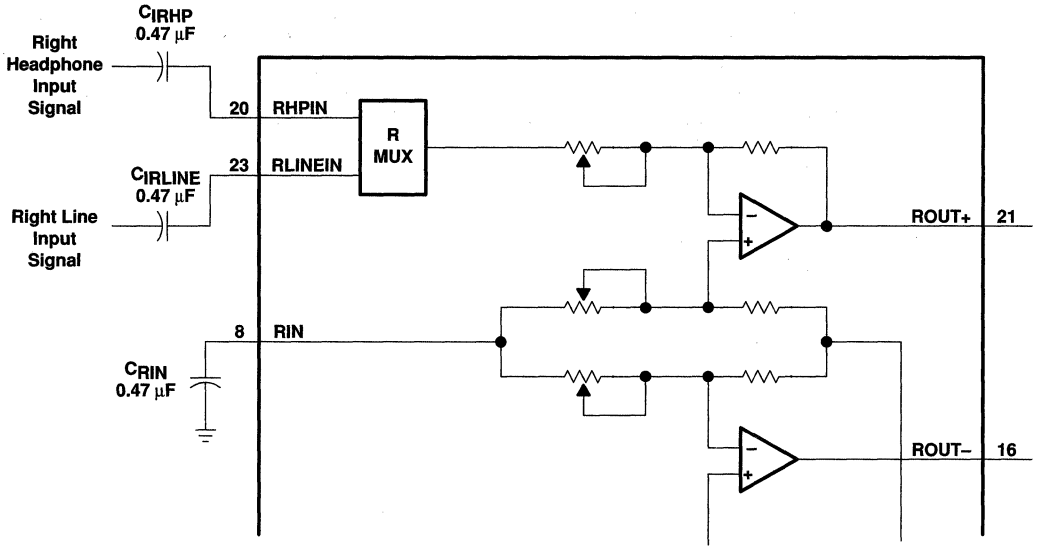


Figure 48. TPA0122 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0122 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

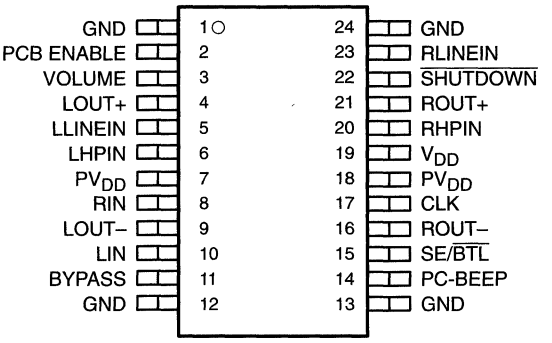
Table 6. Shutdown and Mute Mode Functions

INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume Control From +20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0132 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0132 has less than 0.4% THD+N across its specified frequency range.

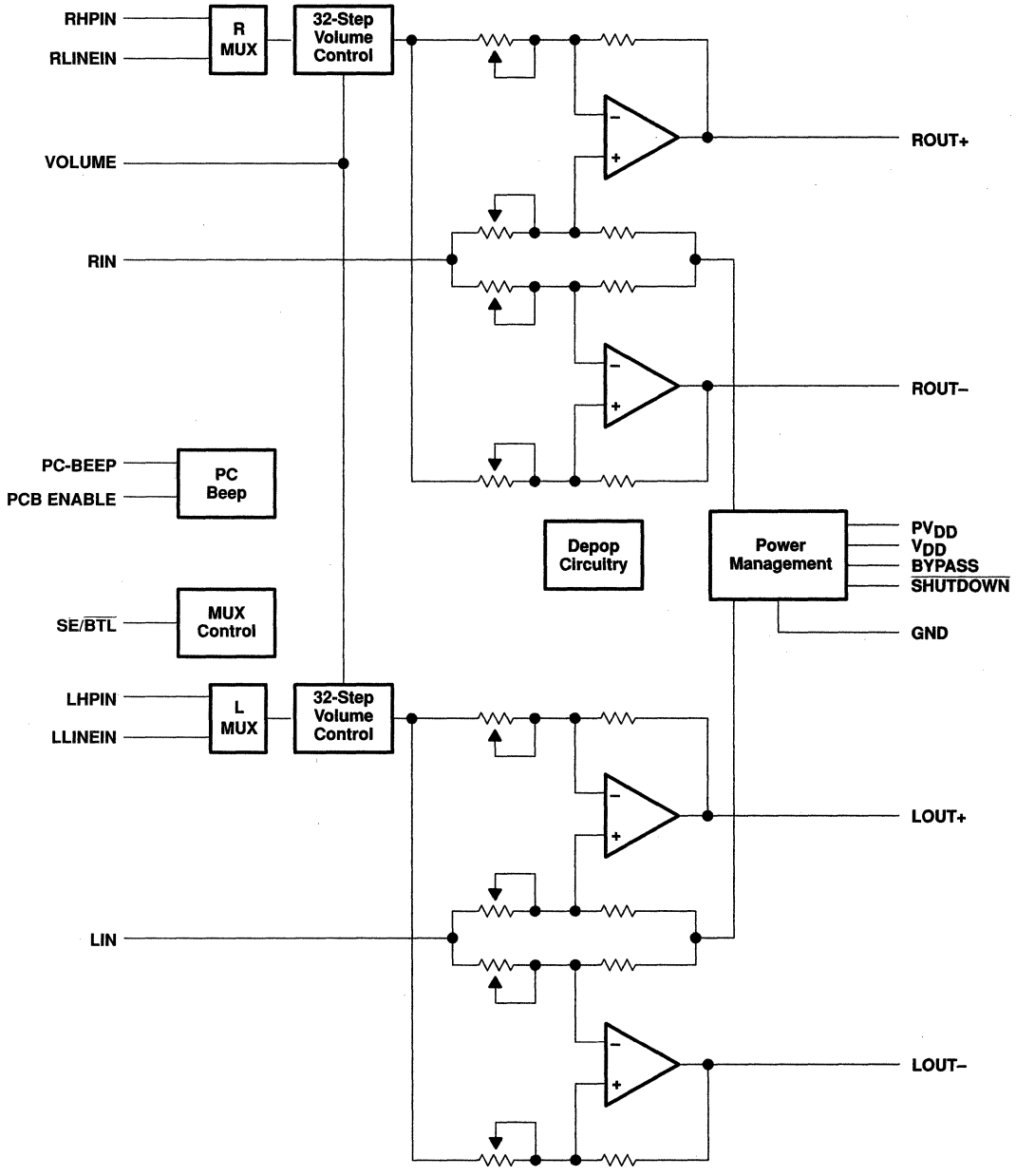
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by means of a dc voltage input on the VOLUME terminal. There are 31 discrete steps covering the range of +20 dB (maximum volume setting) to –40 dB (minimum volume setting) in 2 dB steps. When the VOLUME terminal exceeds 3.54 V, the device is muted. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0132 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this effectively reduces the gain by 6 dB.

The TPA0132 consumes only 10 mA of supply current during normal operation. A miserly shutdown mode is included that reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0132 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0132PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0132PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0132 generates an internal clock. An external clock can override the internal clock input to this terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
PCB ENABLE	2	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	3	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to –40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W§	21.8 mW/°C	1.7 W	1.4 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4 V to 5 V		67		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
Z_I	Input impedance			See Figure 28		
I_{DD}	Supply current	BTL mode		10	15	mA
		SE mode		5	7.5	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.4%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		34		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

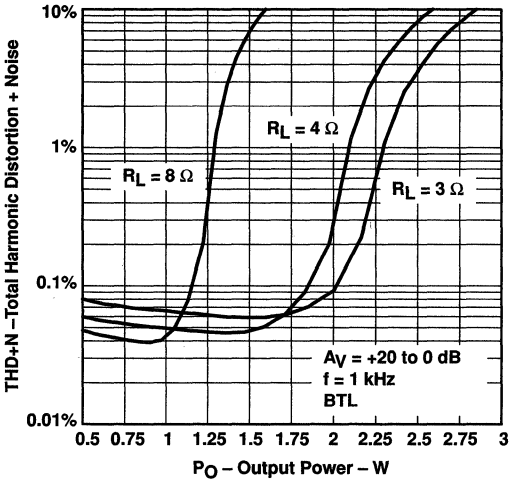


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
GAIN

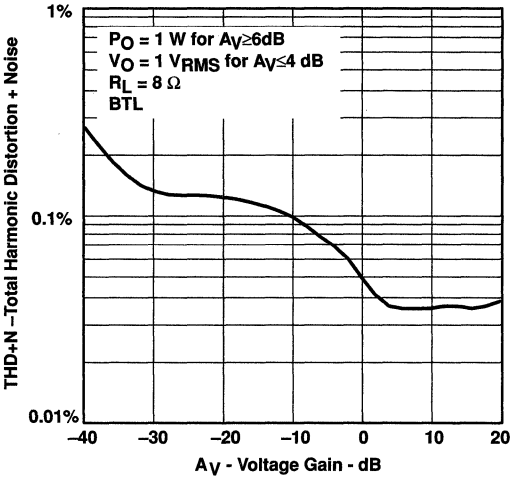


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

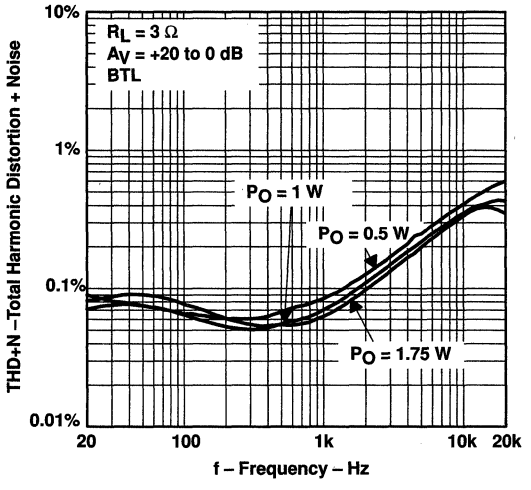


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

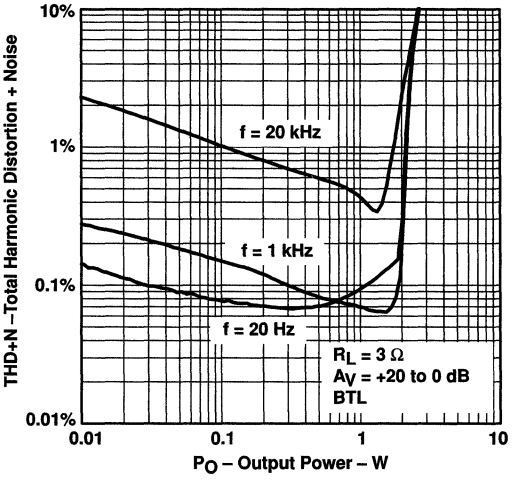


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

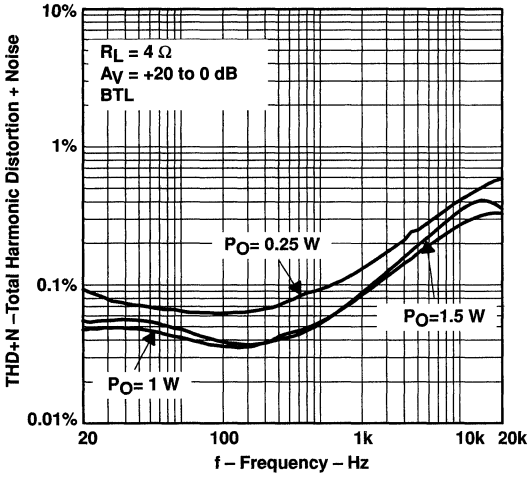


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

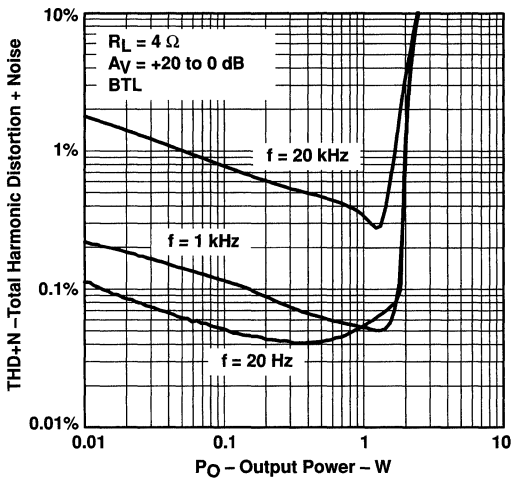


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

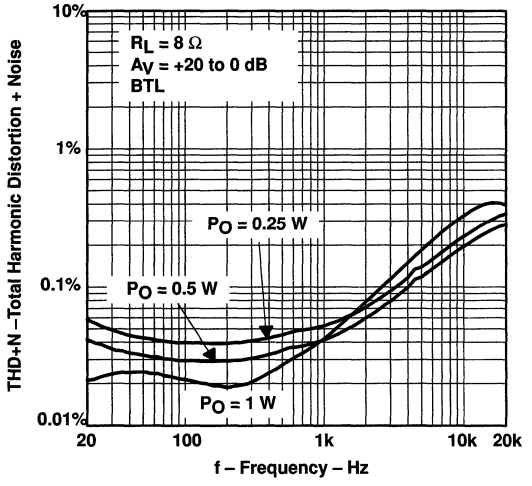


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

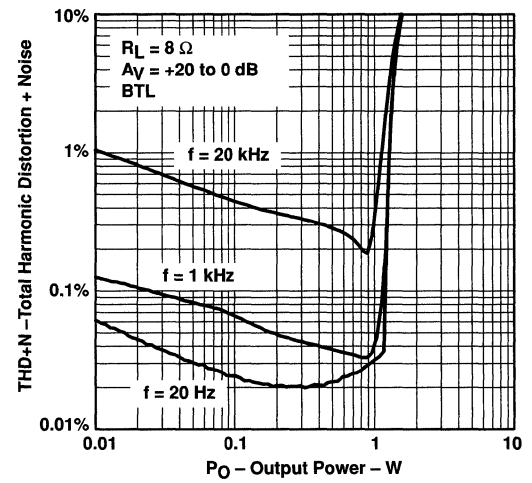


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

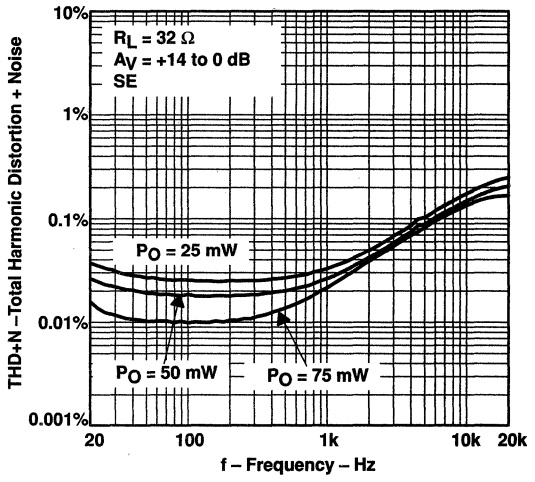


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

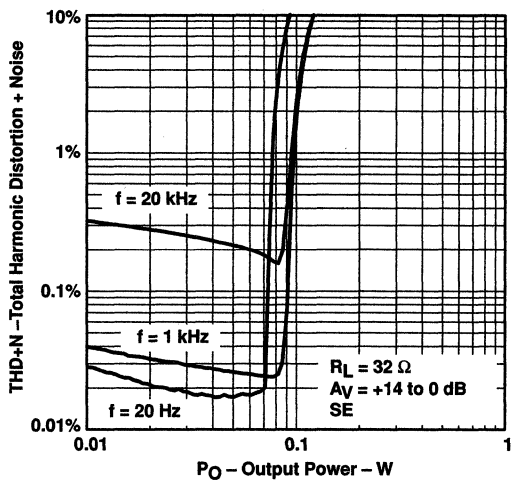


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

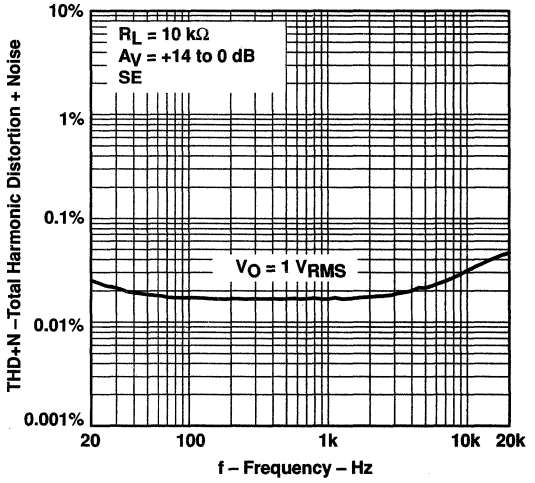


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

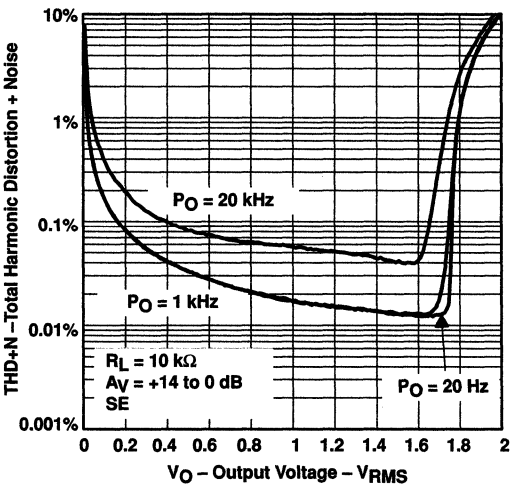


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

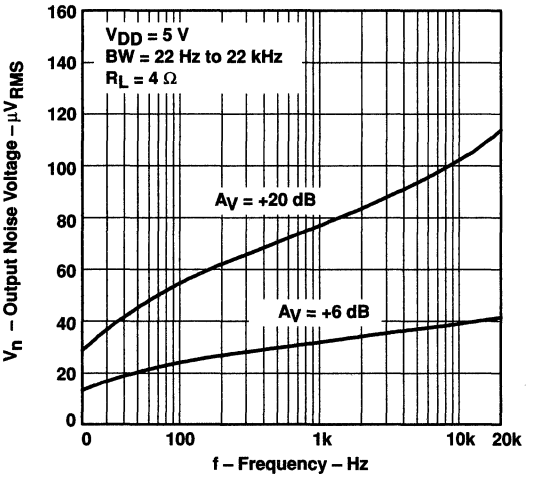


Figure 13

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

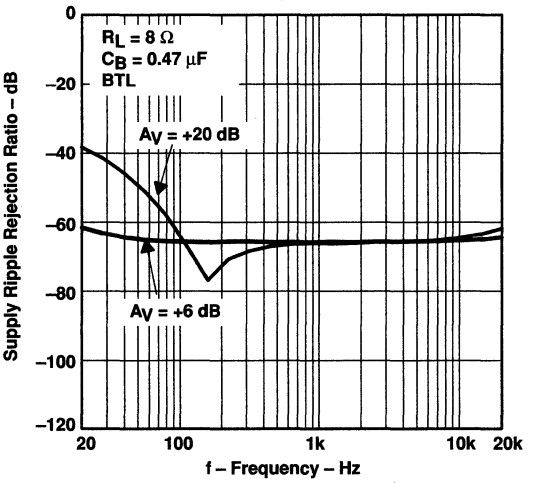


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

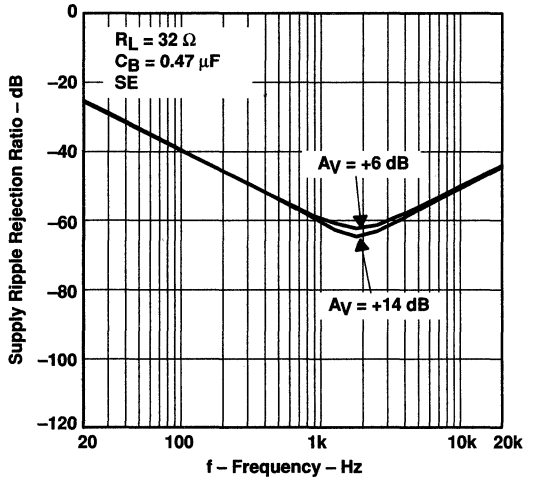


Figure 15

CROSSTALK
vs
FREQUENCY

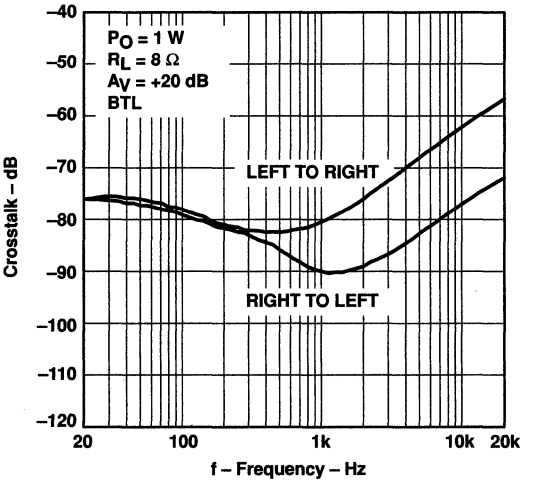


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

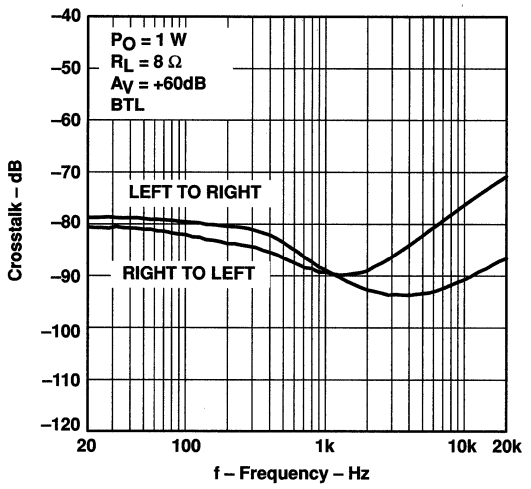


Figure 17

CROSSTALK
vs
FREQUENCY

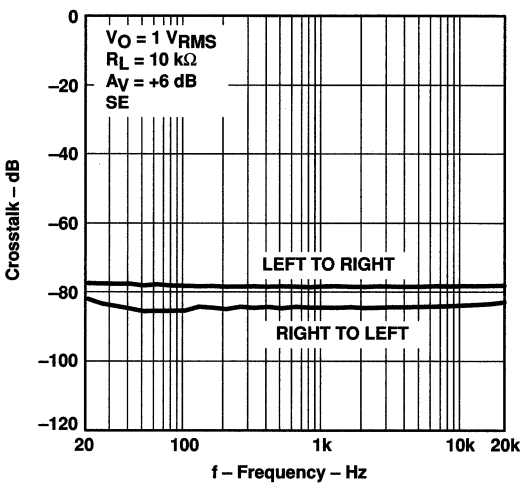


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

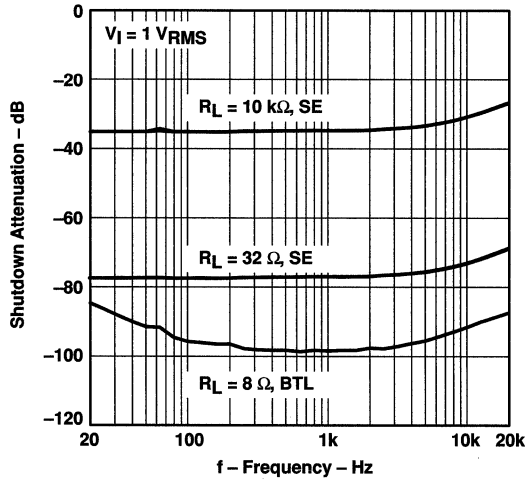


Figure 19

SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

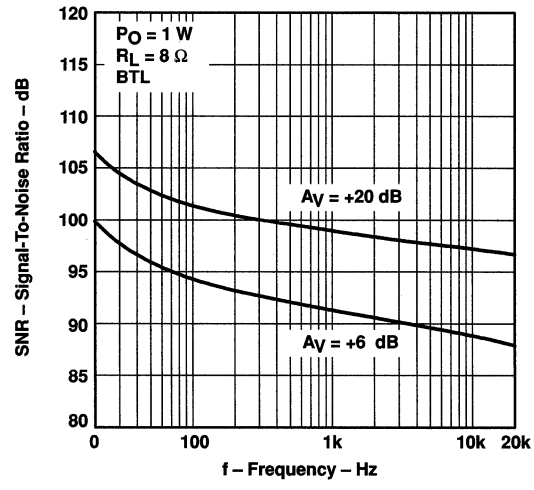


Figure 20

TYPICAL CHARACTERISTICS

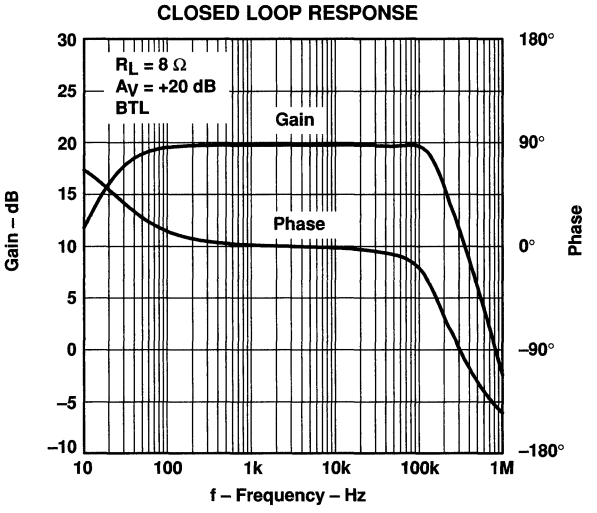


Figure 21

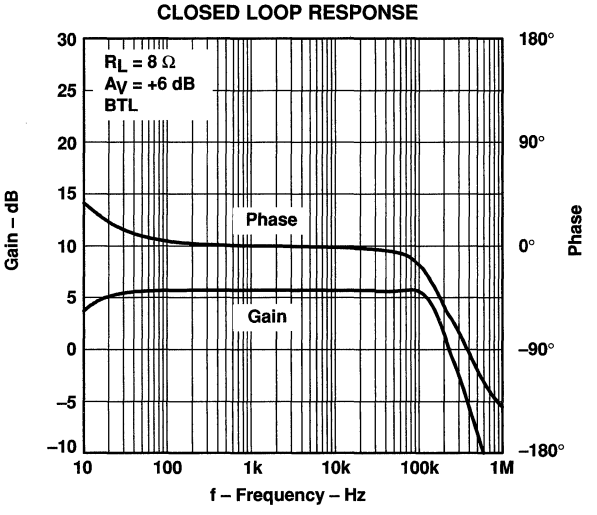


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

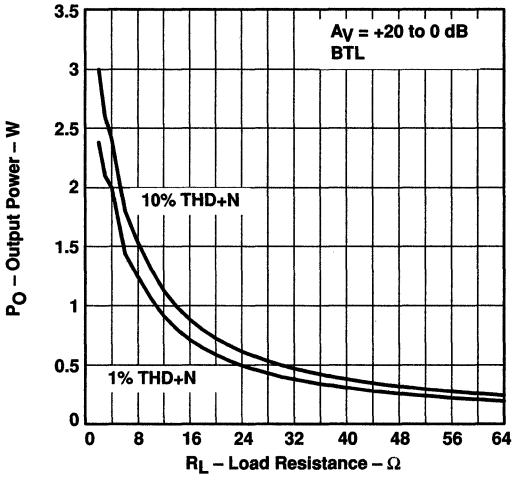


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

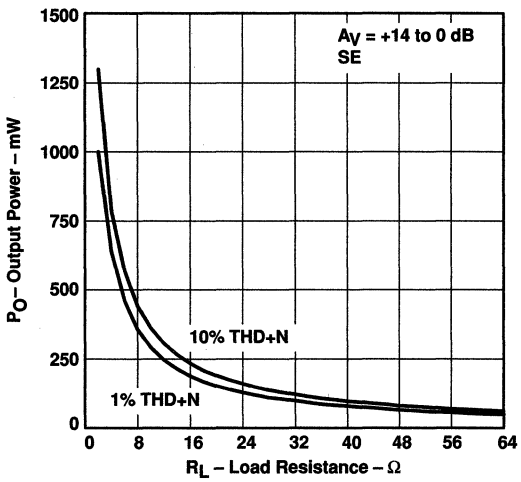


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

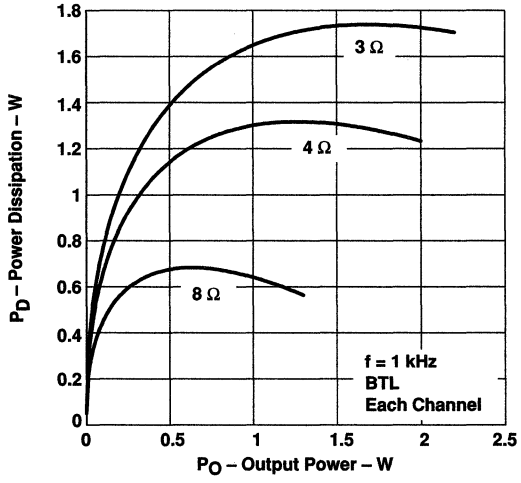


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

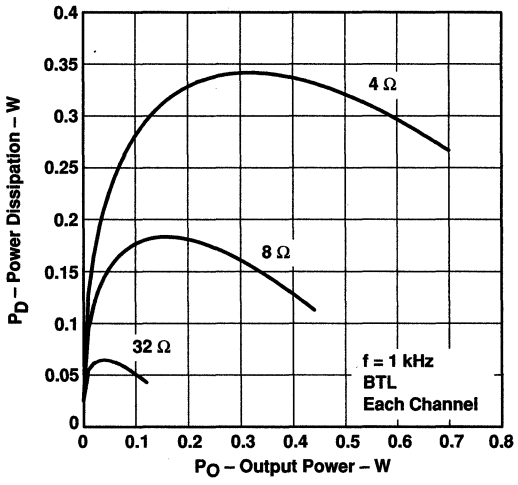


Figure 26

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

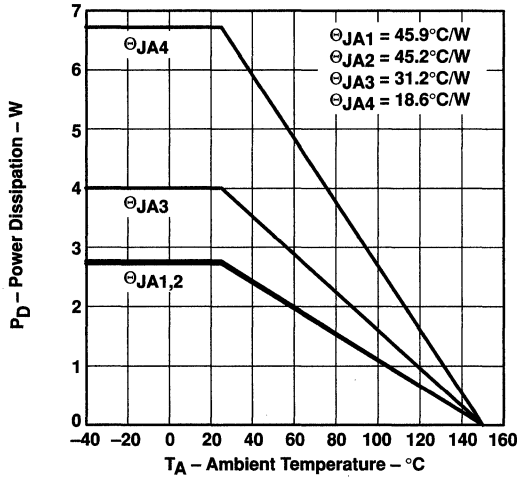


Figure 27

INPUT IMPEDANCE
vs
GAIN

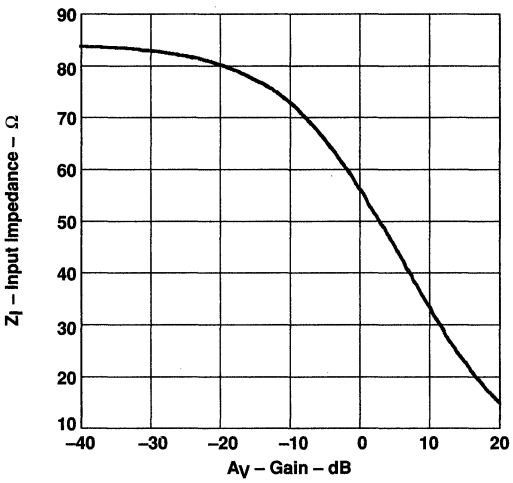


Figure 28

APPLICATION INFORMATION

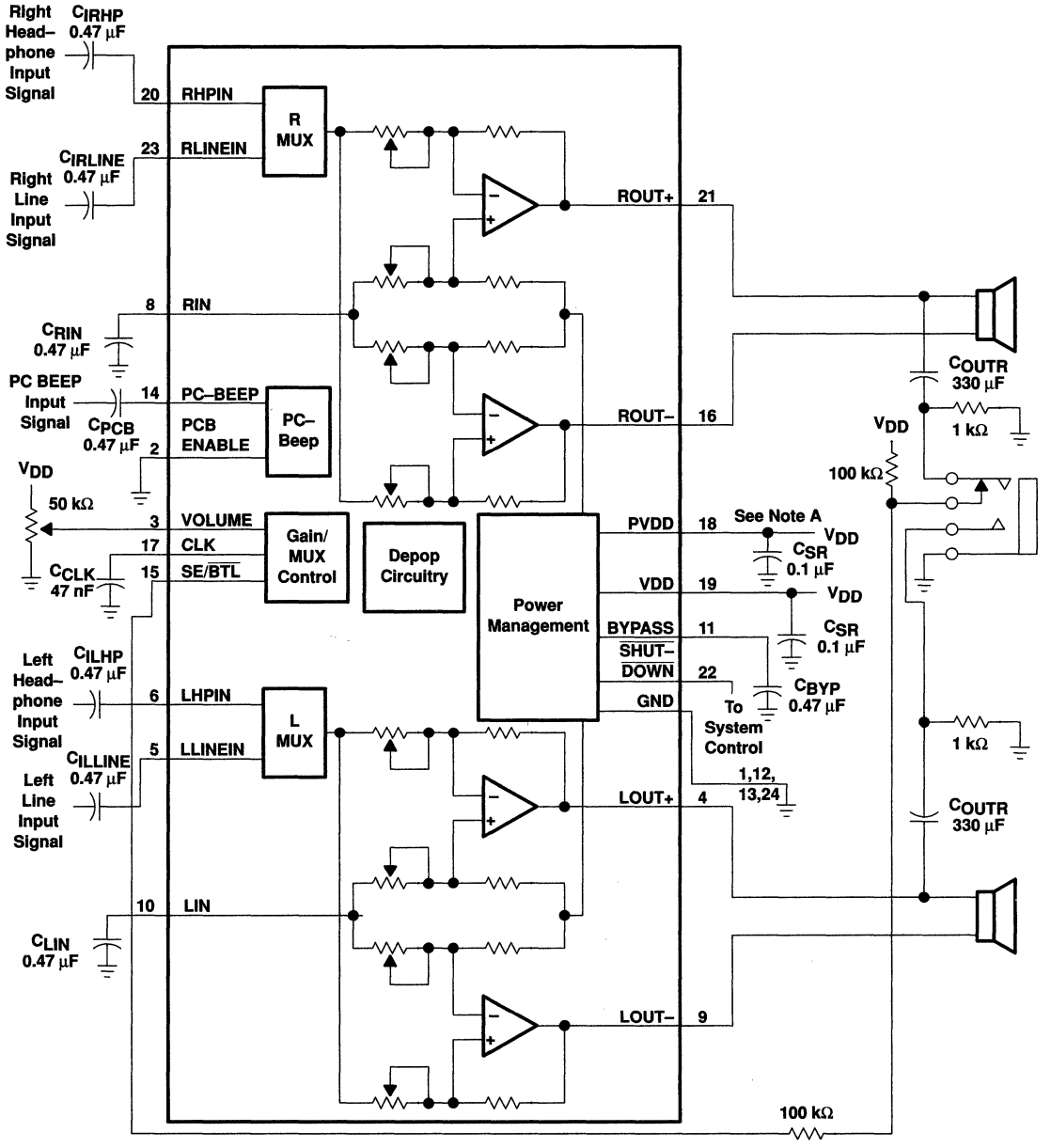
Table 1. DC Volume Control

VOLUME (Terminal 3)		GAIN of AMPLIFIER (dB)
FROM (V)	TO (V)	
0	0.15	20
0.15	0.28	18
0.28	0.39	16
0.39	0.5	14
0.5	0.61	12
0.61	0.73	10
0.73	0.84	8
0.84	0.95	6
0.95	1.06	4
1.06	1.17	2
1.17	1.28	0
1.28	1.39	−2
1.39	1.5	−4
1.5	1.62	−6
1.62	1.73	−8
1.73	1.84	−10
1.84	1.95	−12
1.95	2.07	−14
2.07	2.18	−16
2.18	2.29	−18
2.29	2.41	−20
2.41	2.52	−22
2.52	2.63	−24
2.63	2.74	−26
2.74	2.86	−28
2.86	2.97	−30
2.97	3.08	−32
3.08	3.2	−34
3.2	3.31	−36
3.31	3.42	−38
3.42	3.54	−40
3.54	5	−85

selection of components

Figure 29 and Figure 30 are a schematic diagrams of typical notebook computer application circuits.

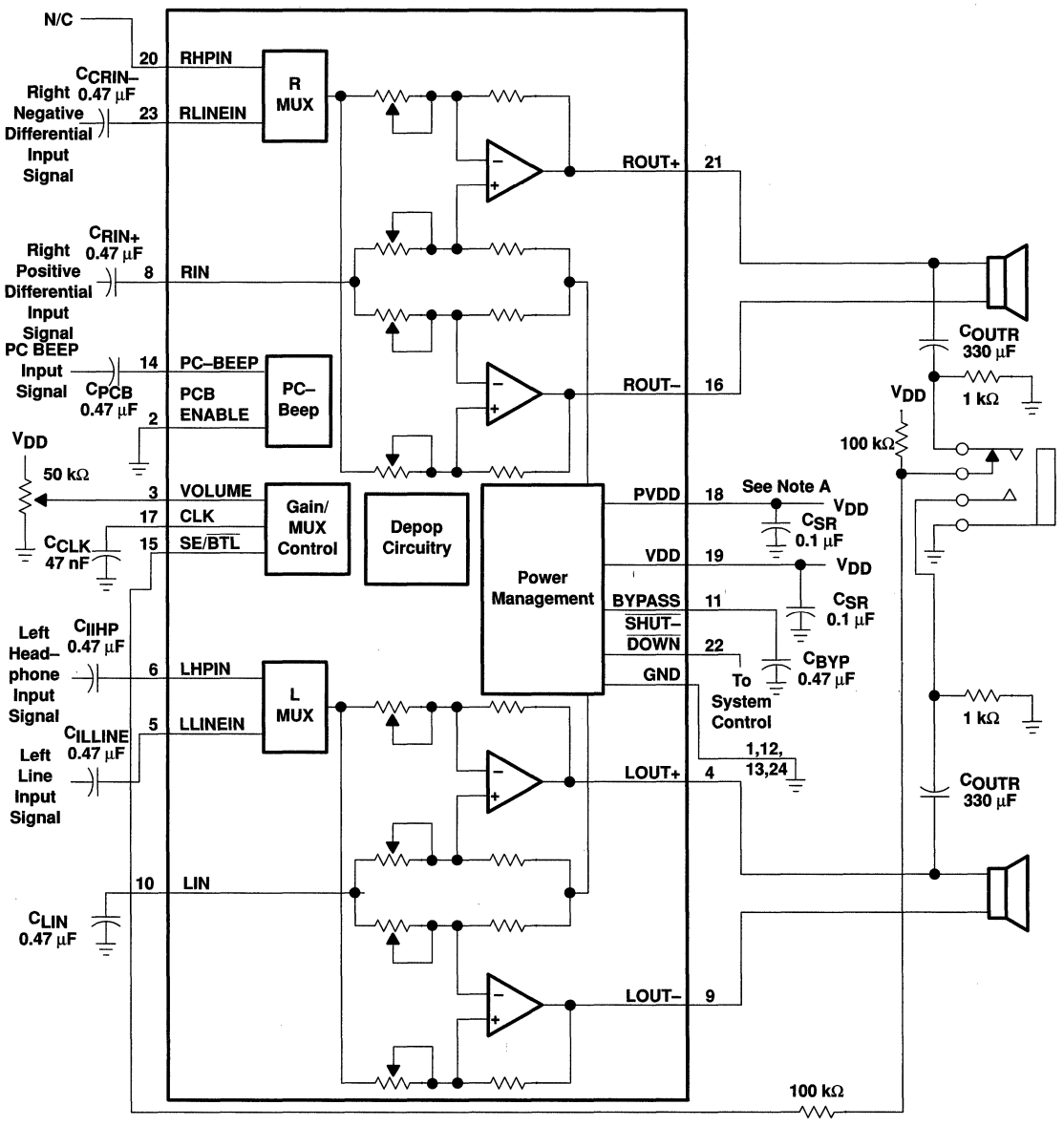
APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 29. Typical TPA0132 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0132 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.

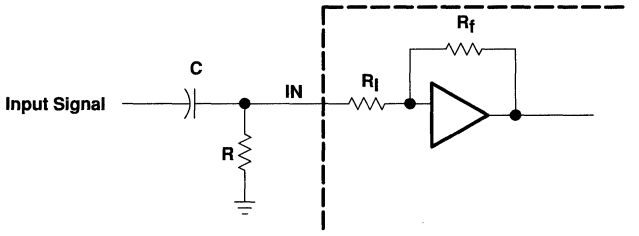


Figure 31. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 28.

The –3 dB frequency can be calculated using the following formula:

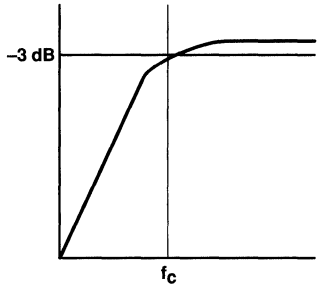
$$f_{-3\ dB} = \frac{1}{2\pi\ C(R \parallel R_I)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_{IN} C_I} \quad (2)$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0132 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

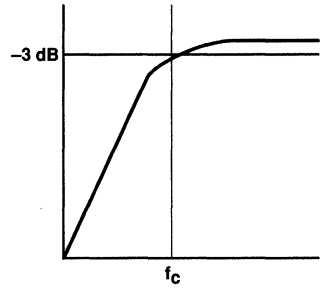
Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 32 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0132 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

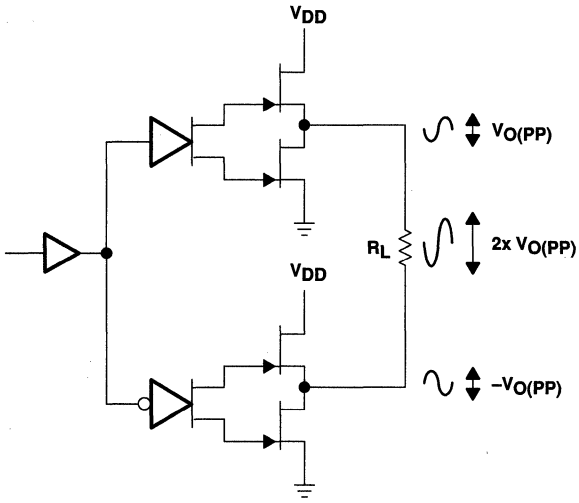


Figure 32. Bridge-Tied Load Configuration

APPLICATION INFORMATION

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 33. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

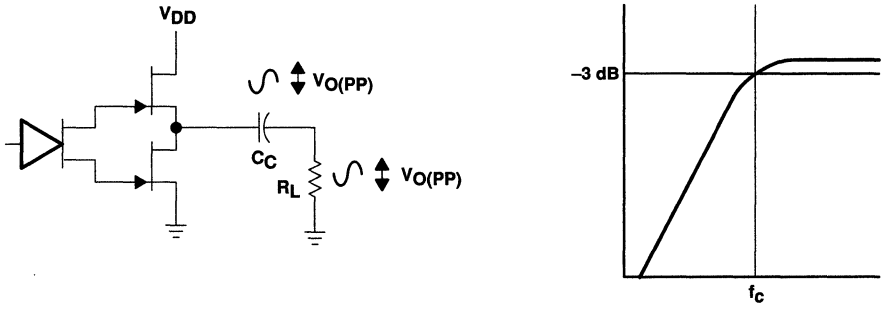


Figure 33. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 32 and Figure 33), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

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An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 34).

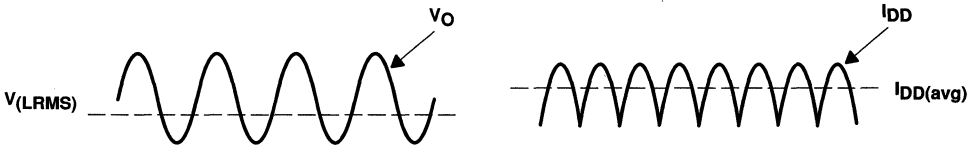

Figure 34. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2 V_{DD} V_P}{\pi R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2 R_L}}{\frac{2 V_{DD} V_P}{\pi R_L}} = \frac{\pi V_P}{4 V_{DD}}$$

Where:

$$V_P = \sqrt{2 P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

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Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0132 data sheet, one can see that when the TPA0132 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \qquad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

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Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

$$= 63 \text{ mW (18 dB crest factor)}$$

$$= 125 \text{ mW (15 dB crest factor)}$$

$$= 250 \text{ mW (9 dB crest factor)}$$

$$= 500 \text{ mW (6 dB crest factor)}$$

$$= 1000 \text{ mW (3 dB crest factor)}$$

$$= 2000 \text{ mW (15 dB crest factor)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0132 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0132 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 5. TPA0132 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

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The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (12)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0132 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0132 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0132 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0132, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0132 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0132 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 35.

APPLICATION INFORMATION

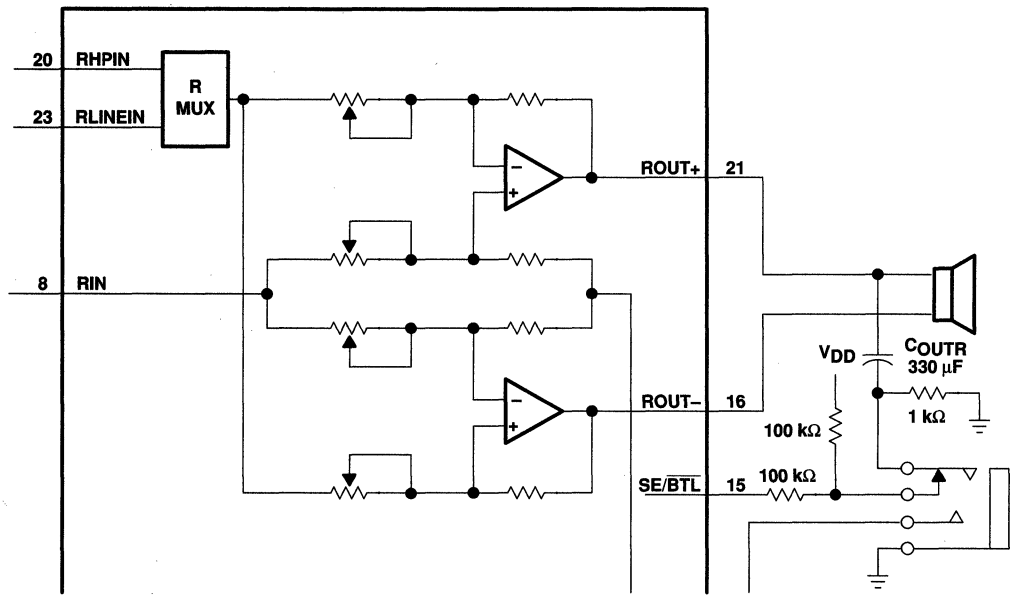


Figure 35. TPA0132 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

APPLICATION INFORMATION

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

Input MUX operation

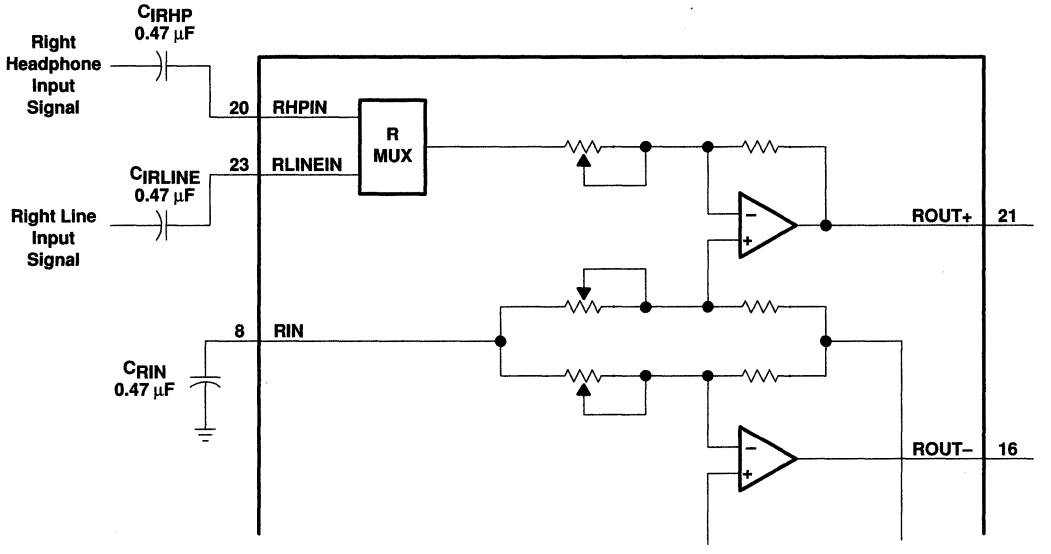


Figure 36. TPA0132 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

APPLICATION INFORMATION

shutdown modes

The TPA0132 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

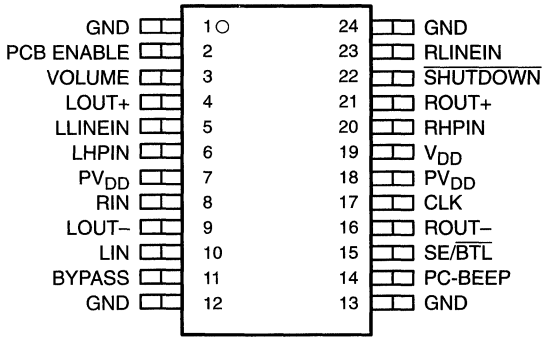
Table 6. Shutdown and Mute Mode Functions

INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume Control From 20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0142 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0142 has less than 0.22% THD+N across its specified frequency range.

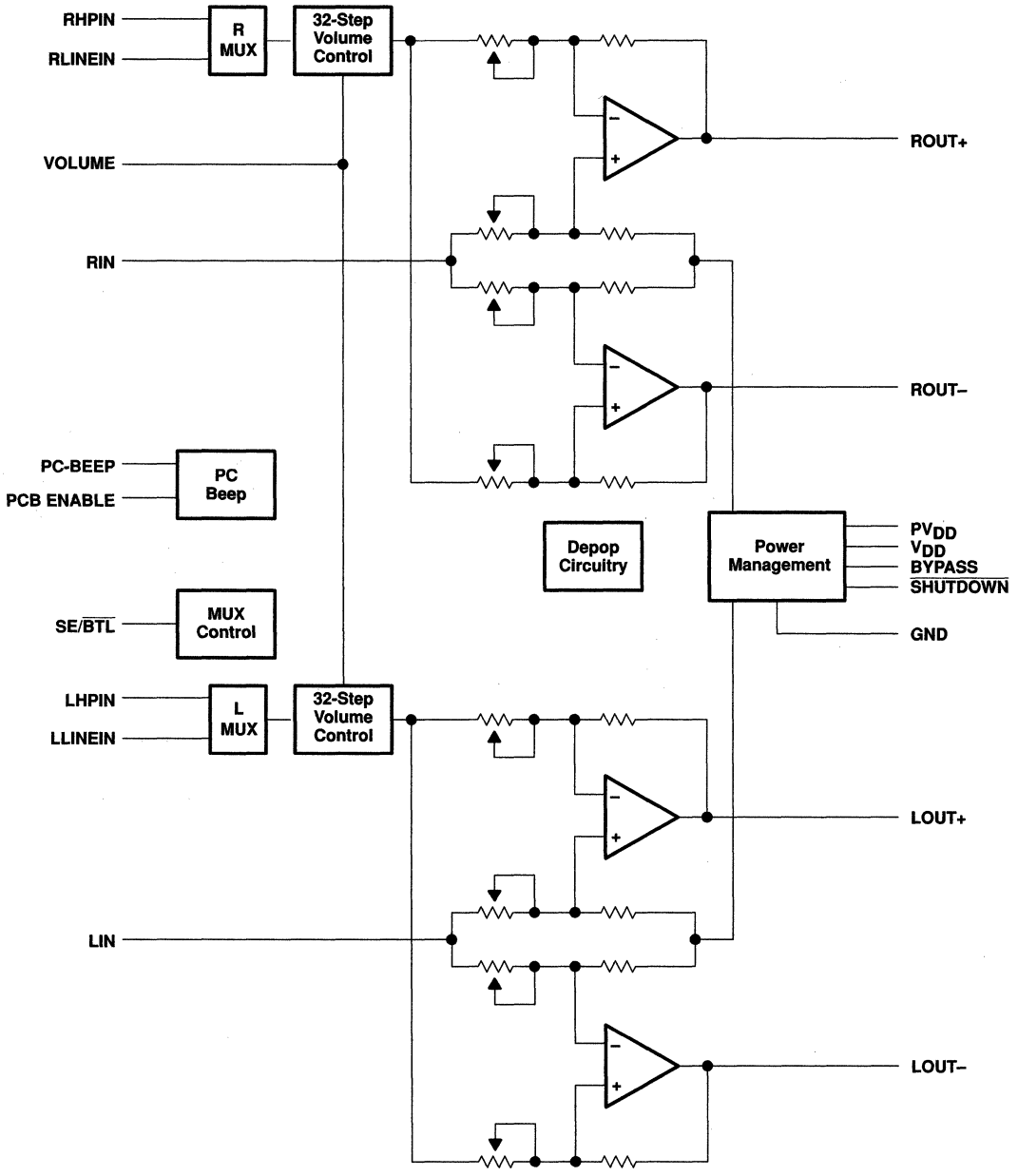
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by a dc voltage input on the VOLUME terminal. There are 31 discrete steps covering the range of 20 dB (maximum volume setting) to –40 dB (minimum volume setting) in 2 dB steps. When the VOLUME terminal exceeds 3.54 V, the device is muted. An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0142 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this effectively reduces the gain by 6 dB.

The TPA0142 consumes only 20 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0142 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0142PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0142PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0142 generates an internal clock. An external clock can override the internal clock input to this terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
PCB ENABLE	2	I	If this terminal is high, the detection circuitry for PC-BEEP is overridden and passes PC-BEEP through the amplifier, regardless of its amplitude. If PCB ENABLE is floating or low, the amplifier continues to operate normally.
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	3	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to –40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
	Supply ripple rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		20		mA
		SE mode		10		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.22%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		34		µV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Bandwidth	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Bandwidth	20
	Closed loop respone		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

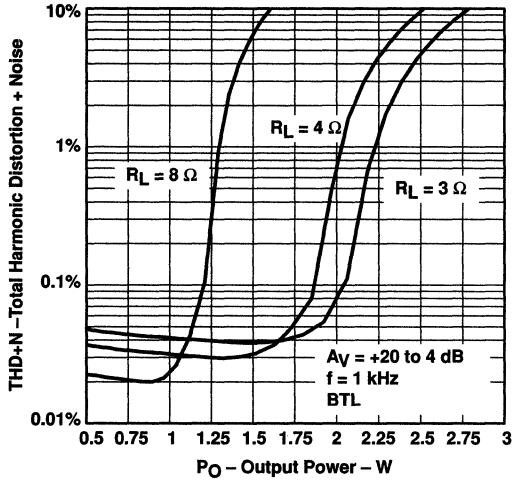


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
VOLTAGE GAIN

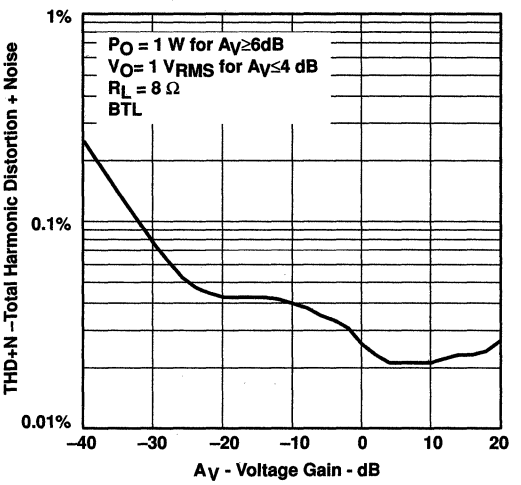


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

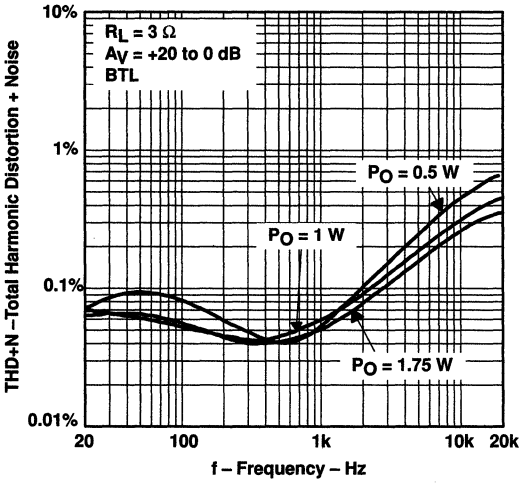


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

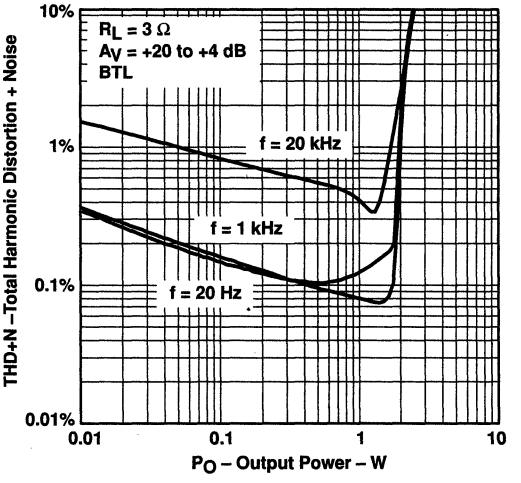


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

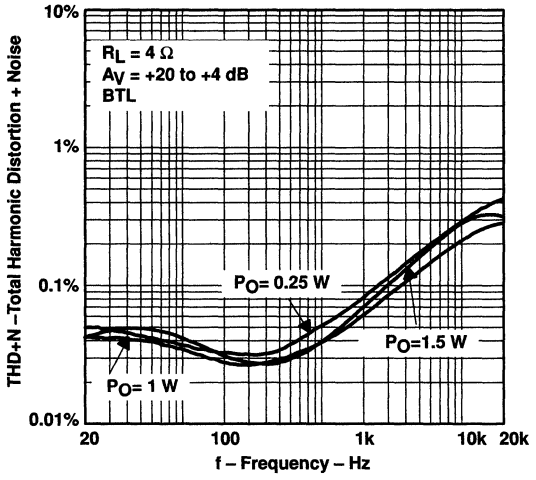


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

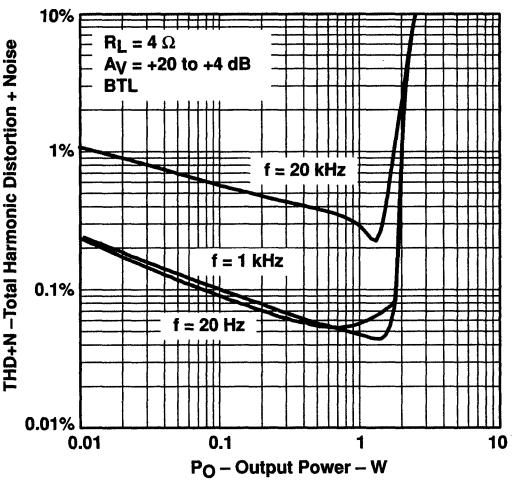


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

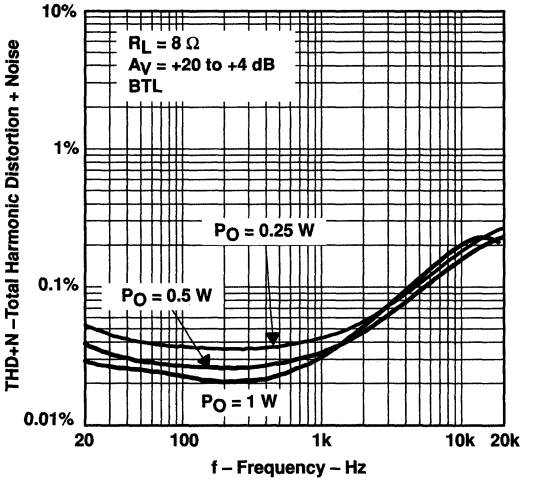


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

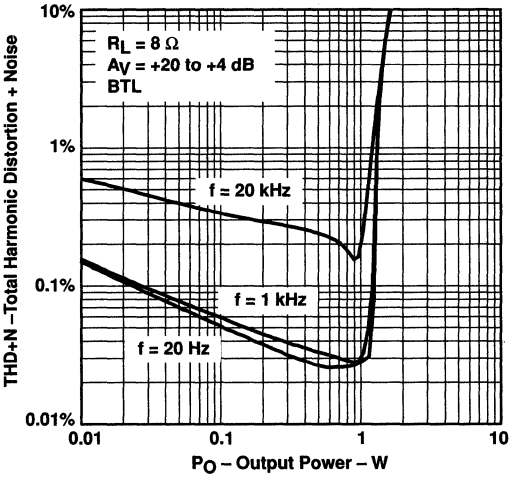


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

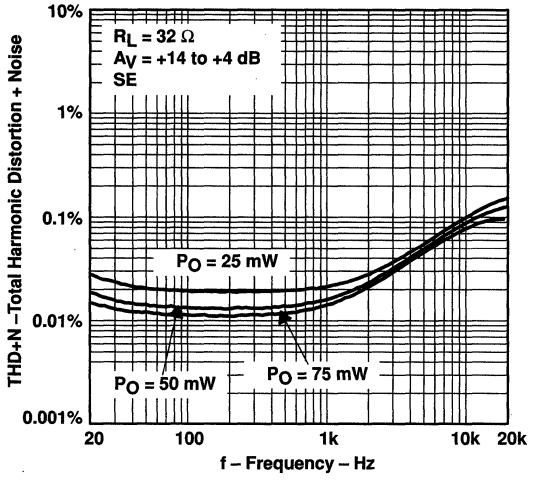


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

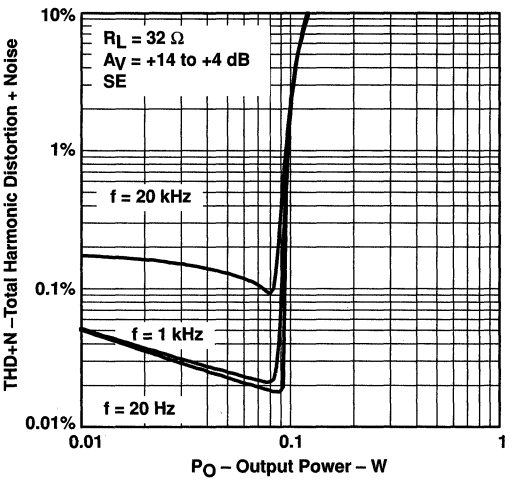


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

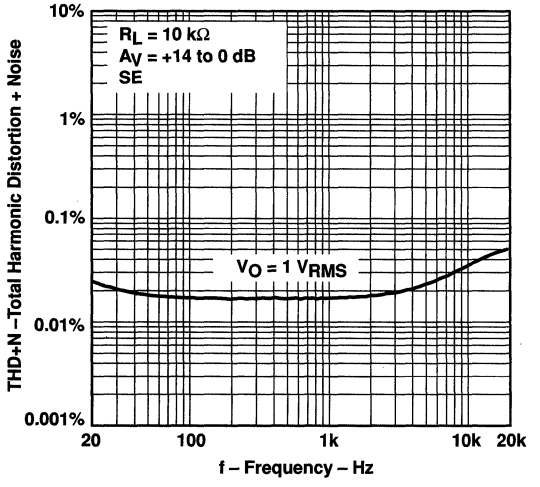


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

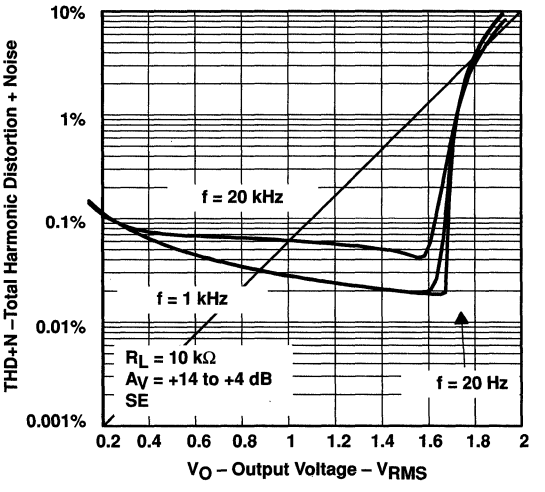


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE vs BANDWIDTH

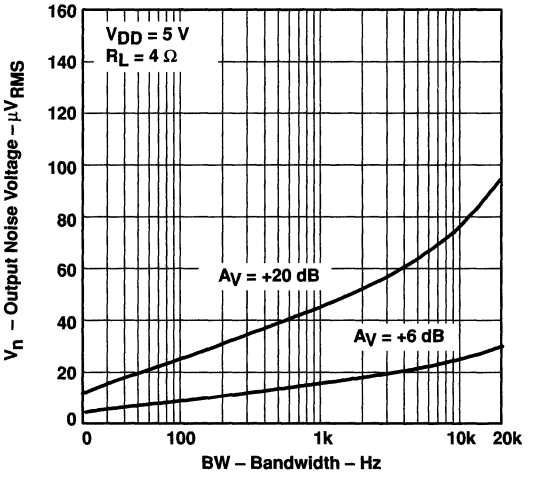


Figure 13

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

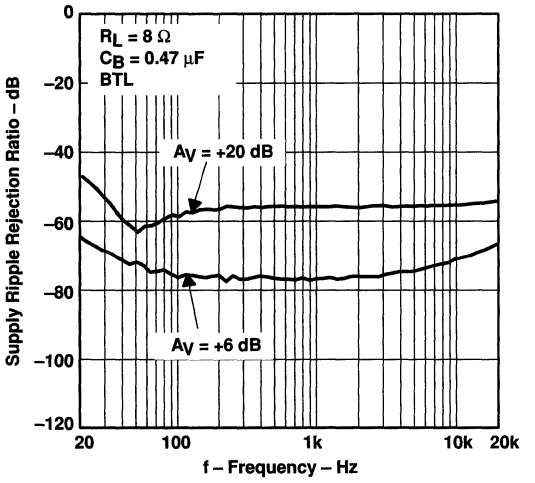


Figure 14

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

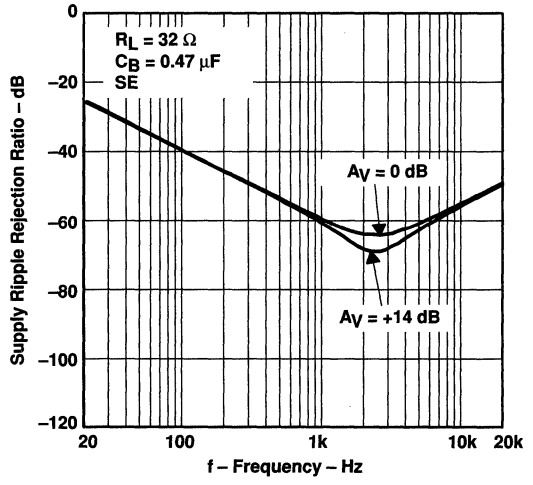


Figure 15

CROSSTALK vs FREQUENCY

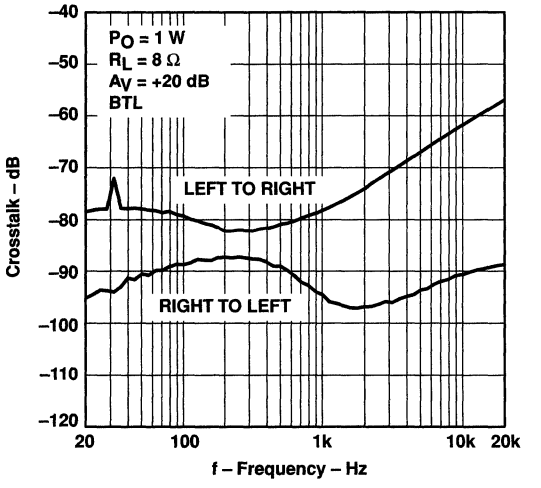


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

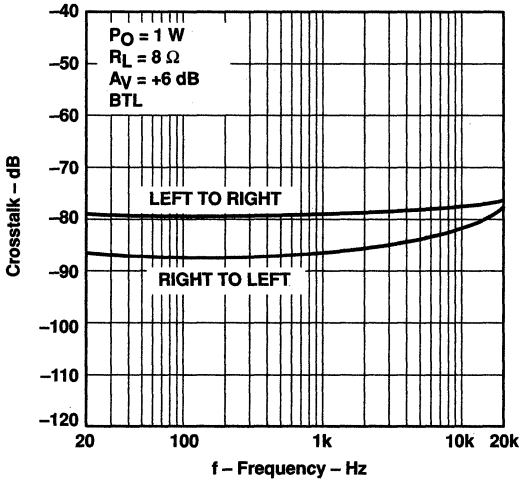


Figure 17

CROSSTALK
vs
FREQUENCY

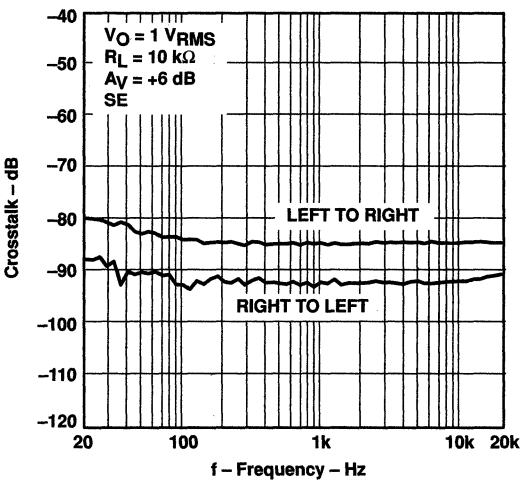


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

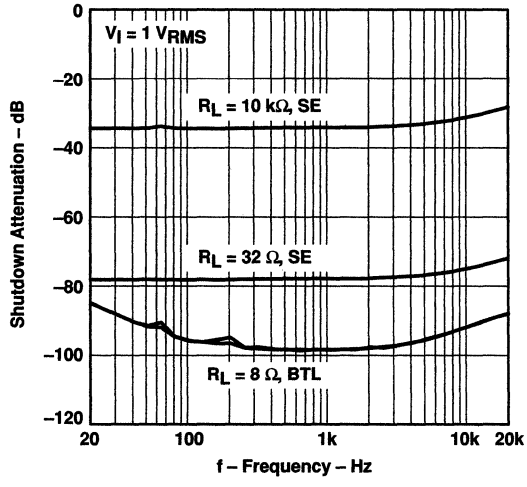


Figure 19

SIGNAL-TO-NOISE RATIO
vs
BANDWIDTH

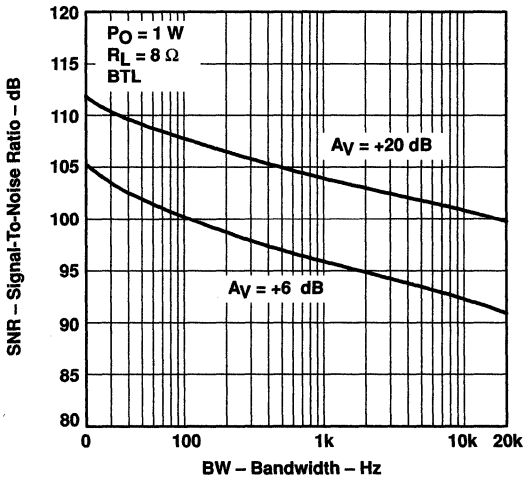


Figure 20

TYPICAL CHARACTERISTICS

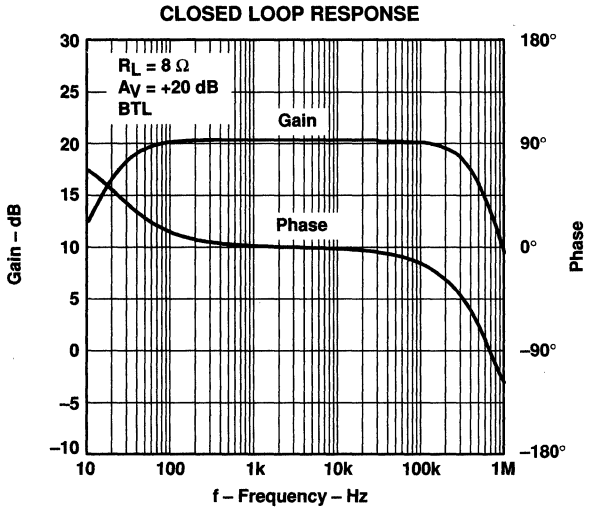


Figure 21

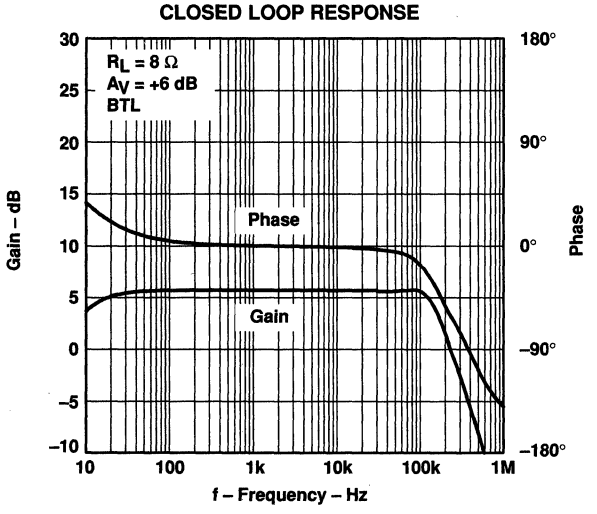


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

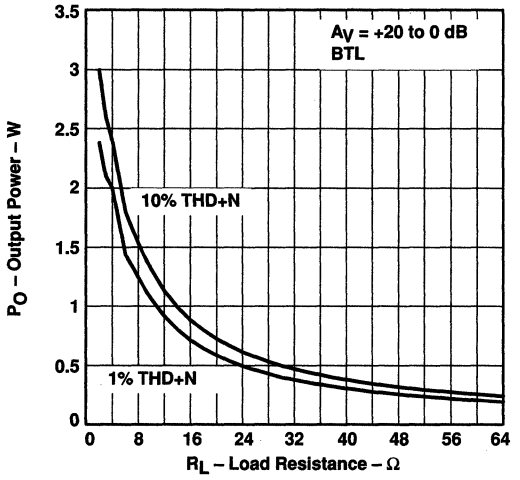


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

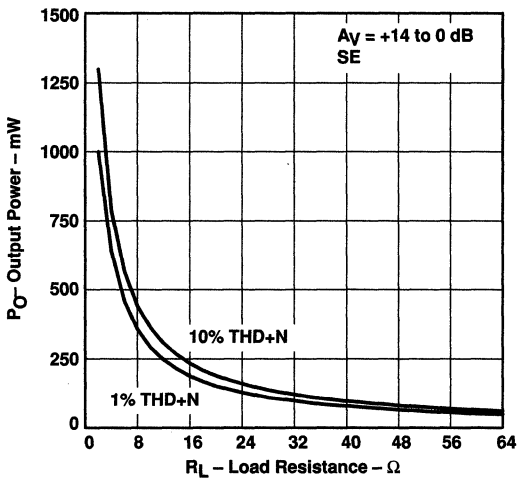


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

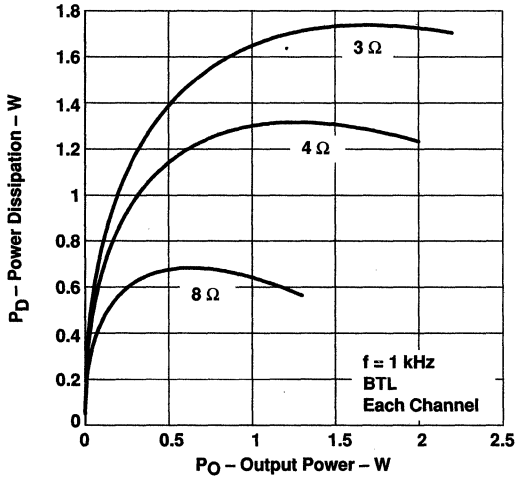


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

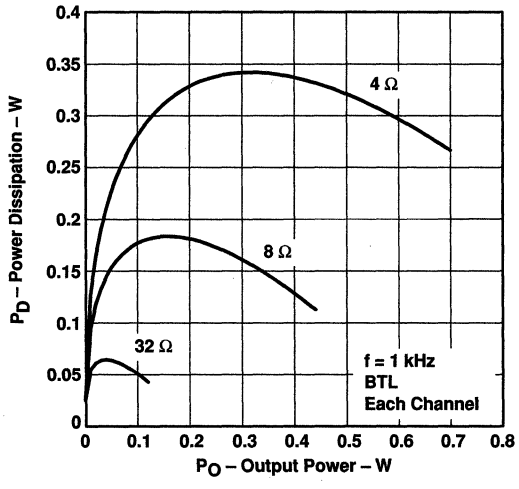


Figure 26

TYPICAL CHARACTERISTICS

**POWER DISSIPATION
vs
AMBIENT TEMPERATURE**

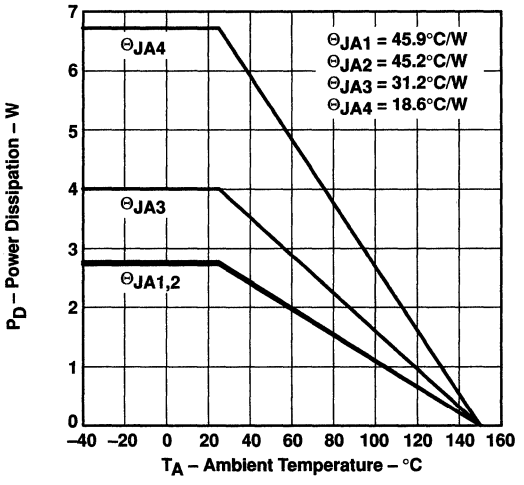


Figure 27

**INPUT IMPEDANCE
vs
GAIN**

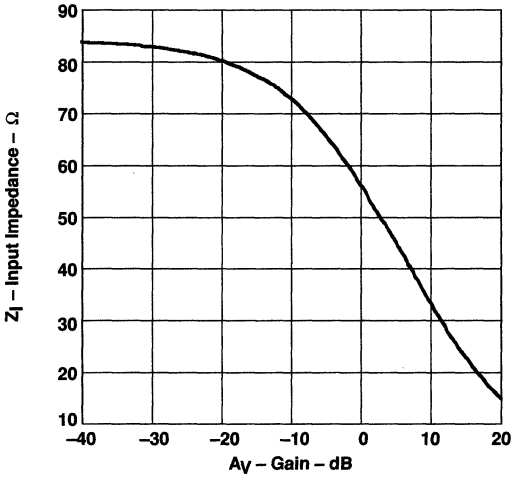


Figure 28

APPLICATION INFORMATION

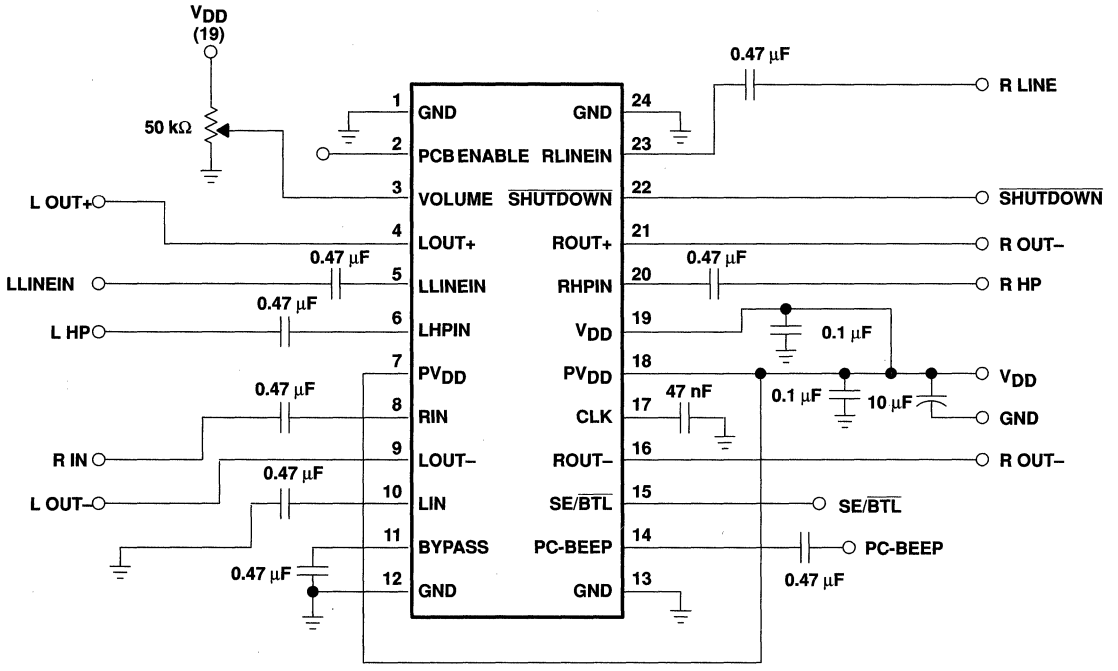


Figure 29. Typical TPA0142 Application Circuit

APPLICATION INFORMATION

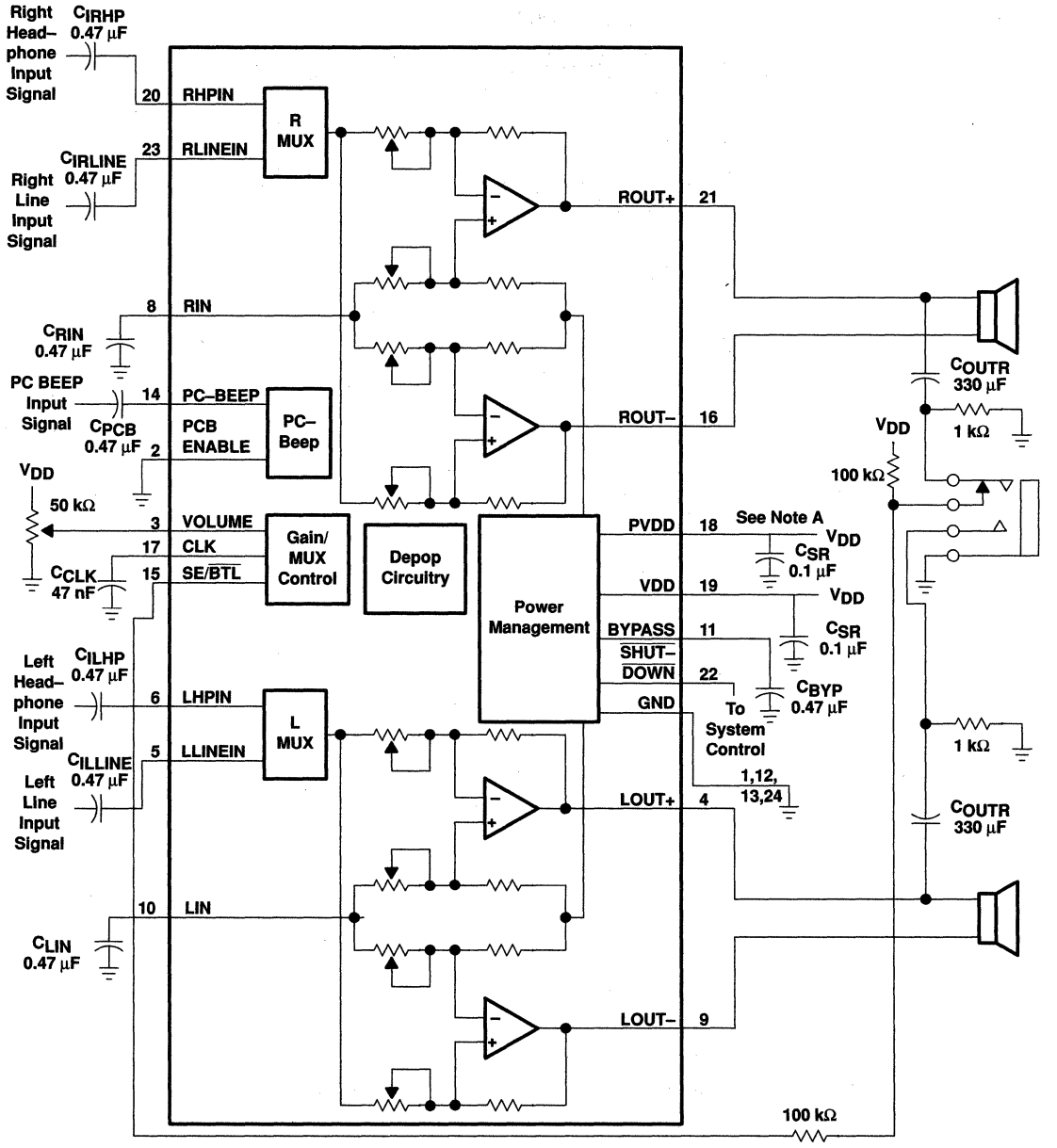
Table 1. DC Volume Control

VOLUME (Terminal 3)		GAIN of AMPLIFIER (dB)
FROM (V)	TO (V)	
0	0.15	20
0.15	0.28	18
0.28	0.39	16
0.39	0.5	14
0.5	0.61	12
0.61	0.73	10
0.73	0.84	8
0.84	0.95	6
0.95	1.06	4
1.06	1.17	2
1.17	1.28	0
1.28	1.39	−2
1.39	1.5	−4
1.5	1.62	−6
1.62	1.73	−8
1.73	1.84	−10
1.84	1.95	−12
1.95	2.07	−14
2.07	2.18	−16
2.18	2.29	−18
2.29	2.41	−20
2.41	2.52	−22
2.52	2.63	−24
2.63	2.74	−26
2.74	2.86	−28
2.86	2.97	−30
2.97	3.08	−32
3.08	3.2	−34
3.2	3.31	−36
3.31	3.42	−38
3.42	3.54	−40
3.54	5	−85

selection of components

Figure 30 and Figure 31 are a schematic diagrams of typical notebook computer application circuits.

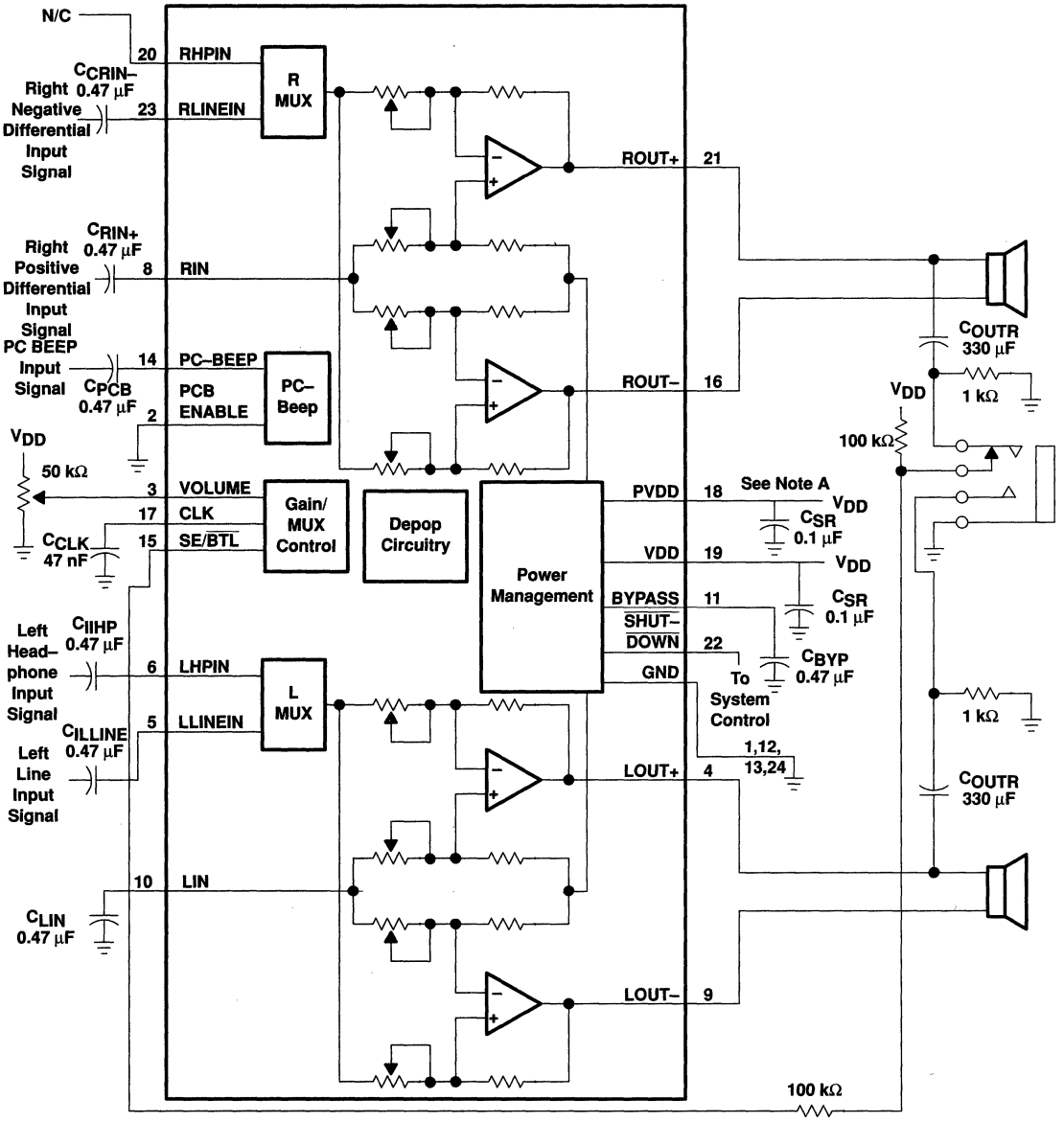
APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0142 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0142 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.

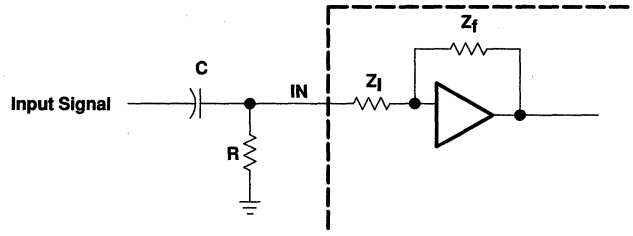


Figure 32. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 28:

The –3 dB frequency can be calculated using the following formula:

$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \quad (1)$$

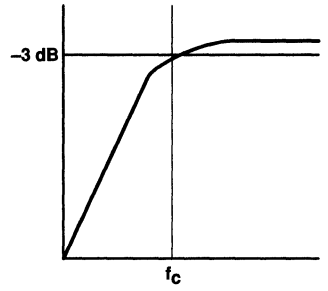
If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_{IN} C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0142 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

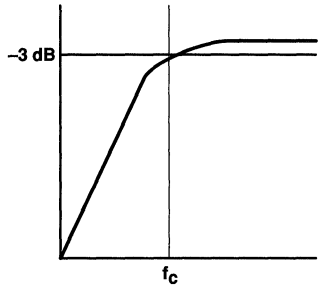
Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 33 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0142 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

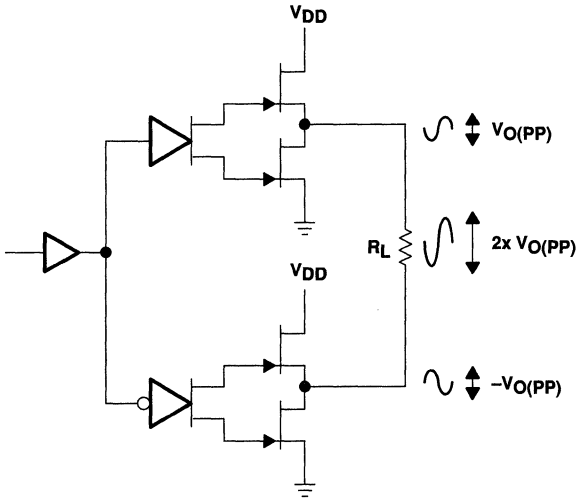


Figure 33. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 34. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \qquad (6)$$

APPLICATION INFORMATION

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

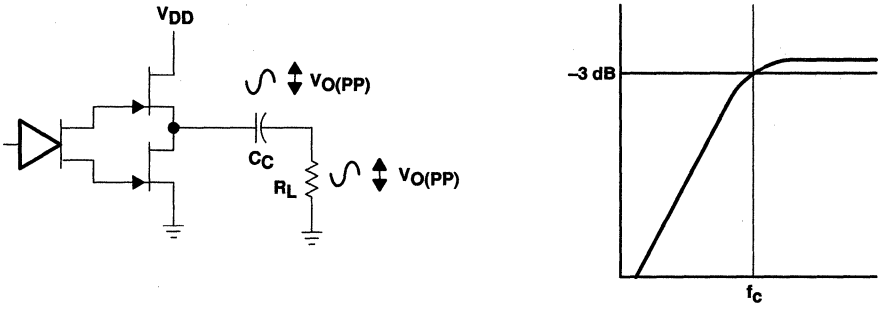


Figure 34. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 33 and Figure 34), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 35).

APPLICATION INFORMATION

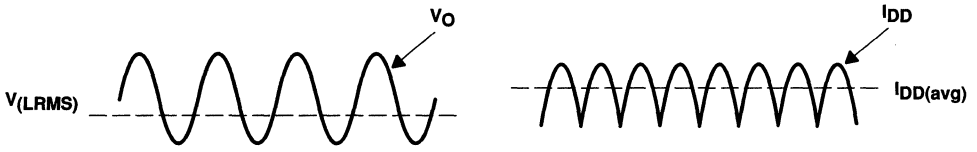


Figure 35. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\dfrac{V_P{}^2}{2\, R_L}}{\dfrac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

APPLICATION INFORMATION

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0142 data sheet, one can see that when the TPA0142 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\text{ W}}{1\text{ W}} = 6\text{ dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

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This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0142 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0142 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 5. TPA0142 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (12)$$

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To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0142 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0142 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0142 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0142, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0142 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0142 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 36.

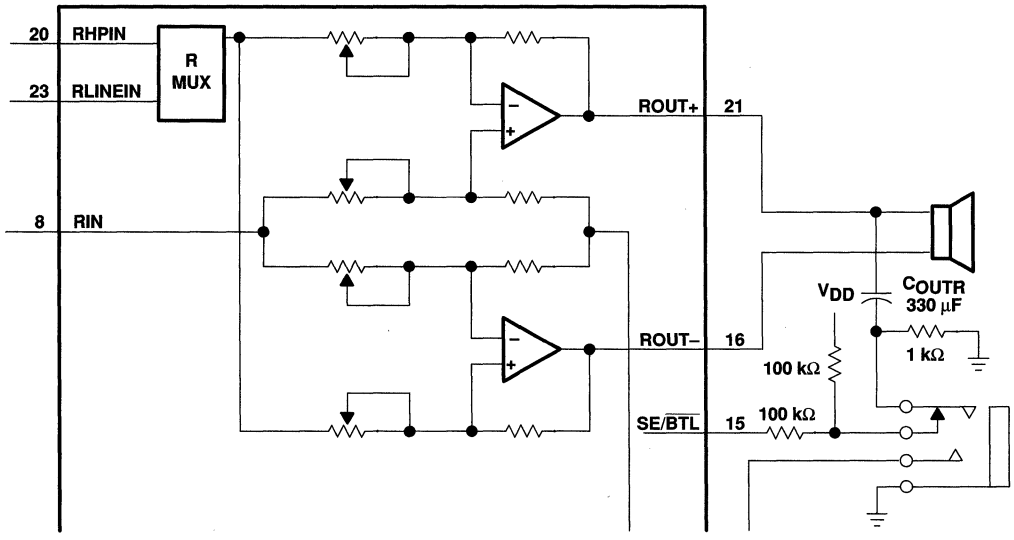


Figure 36. TPA0142 Resistor Divider Network Circuit

APPLICATION INFORMATION

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

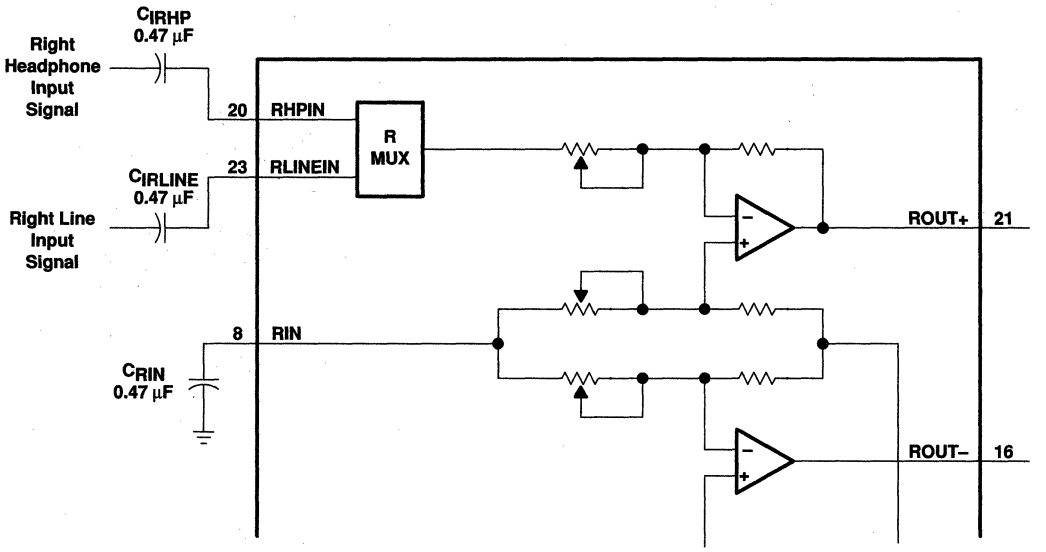


Figure 37. TPA0142 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0142 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

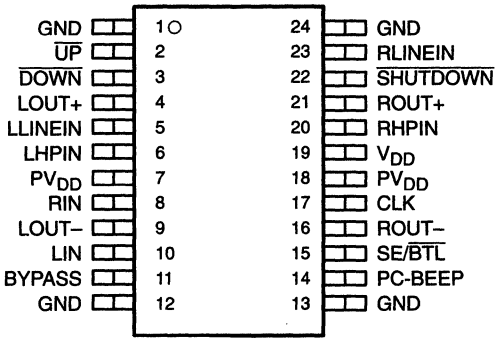
Table 6. Shutdown and Mute Mode Functions

INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Digital Volume Control From +20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0152 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0152 has less than 0.3% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

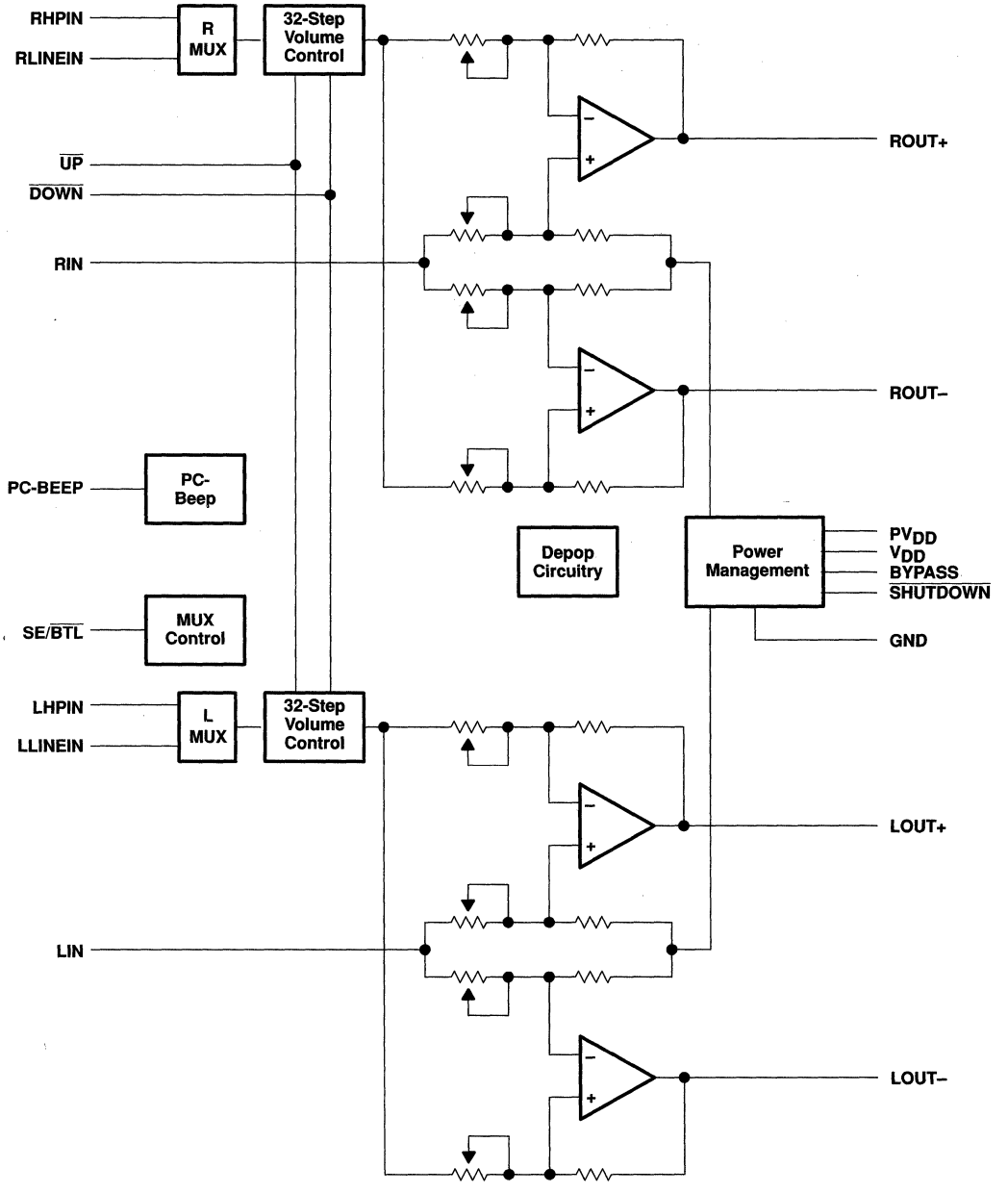
The overall gain of the amplifier is controlled digitally by the UP and DOWN terminals. At power up, the gain is set at the lowest level, –85 dB. It can then be adjusted to any of 31 discrete steps by pulling the voltage down at the desired pin to logic low. The gain is adjusted in the initial stage of the amplifier as opposed to the power output stage. As a result, the THD changes very little over all volume levels.

An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0152 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. This effectively reduces the gain by 6 dB.

The TPA0152 consumes only 10 mA of supply current during normal operation. A miserly shutdown mode is included that reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0152 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0152PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0152PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0152 generates an internal clock. An external clock can override the internal clock input to this terminal.
$\overline{\text{DOWN}}$	3	I	A momentary pulse on this terminal decreases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left-channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
LOUT–	9	O	Left-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
ROUT–	16	O	Right-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
$\overline{\text{UP}}$	2	I	A momentary pulse on this terminal increases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}			900	nA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		10		mA
		SE mode		5		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.3%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		17		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10, 12
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11, 14
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop respone		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	22
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

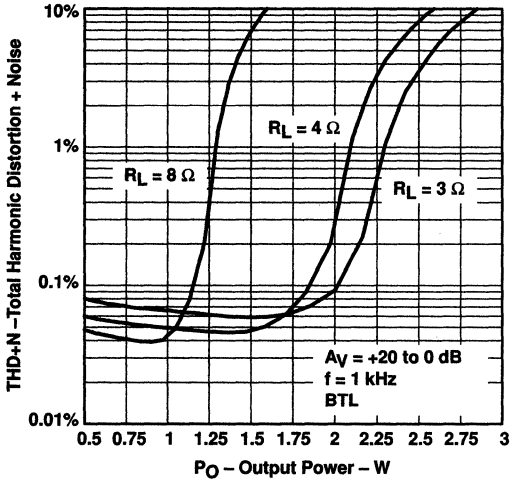


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
GAIN

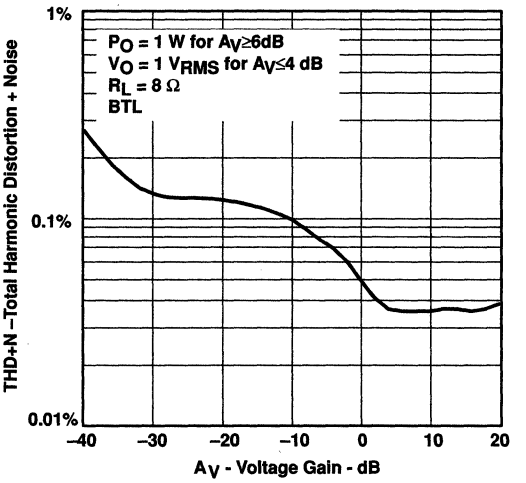


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

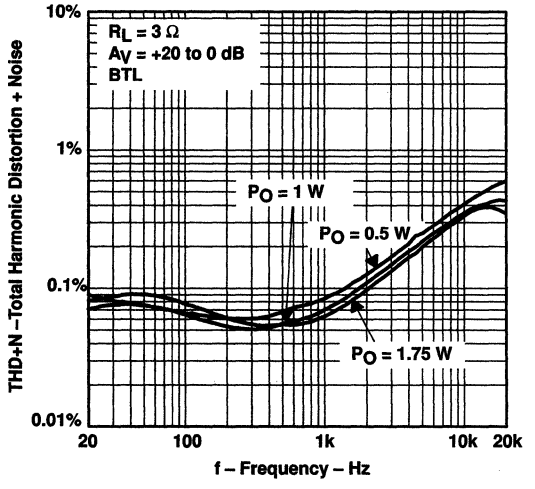


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

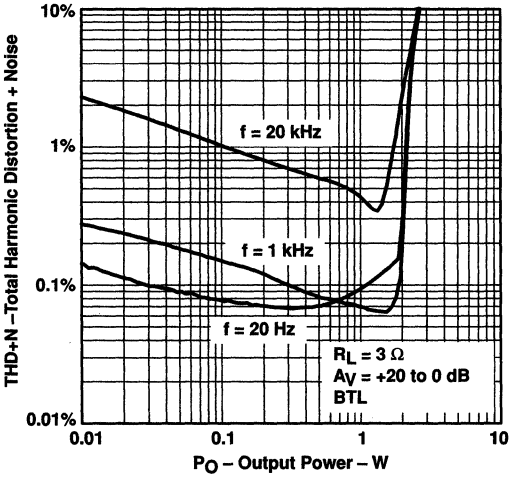


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

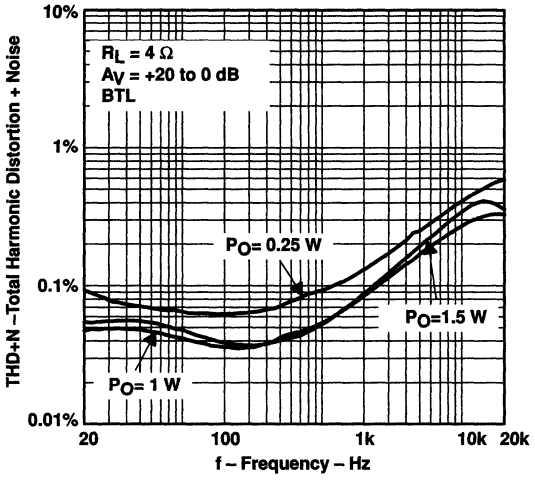


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

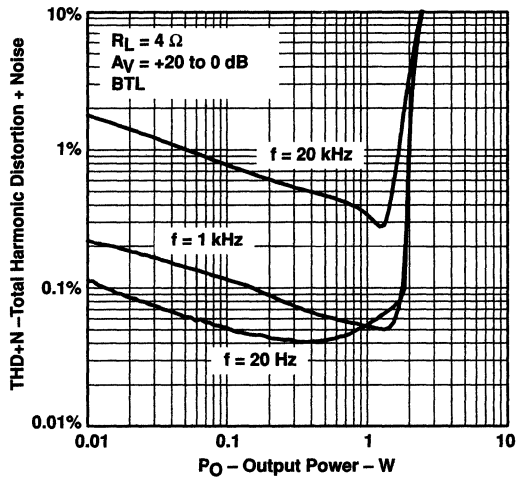


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

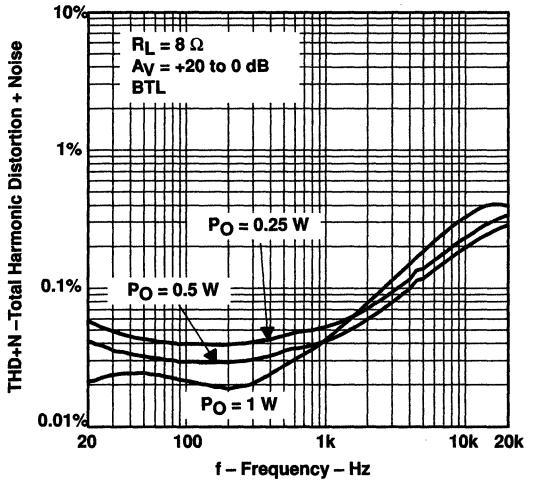


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

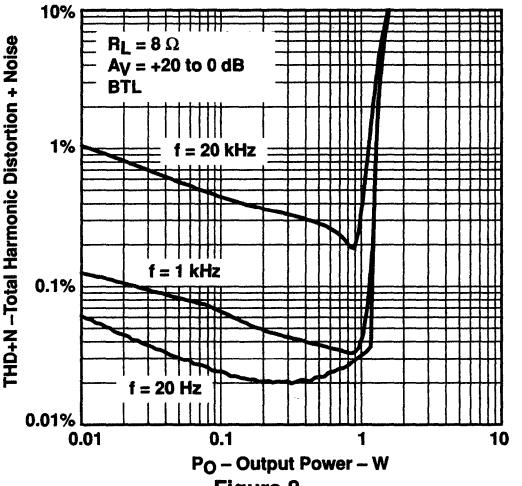


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

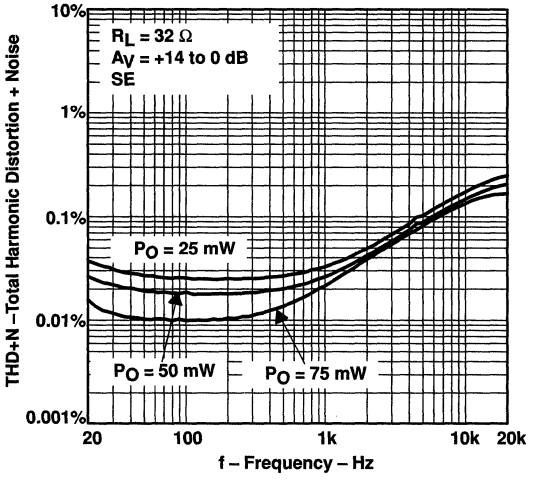


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

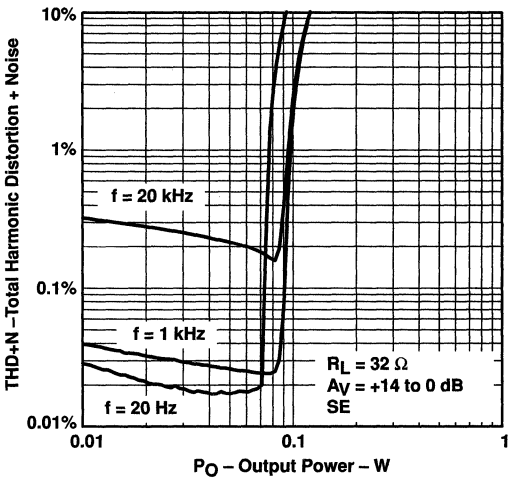


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

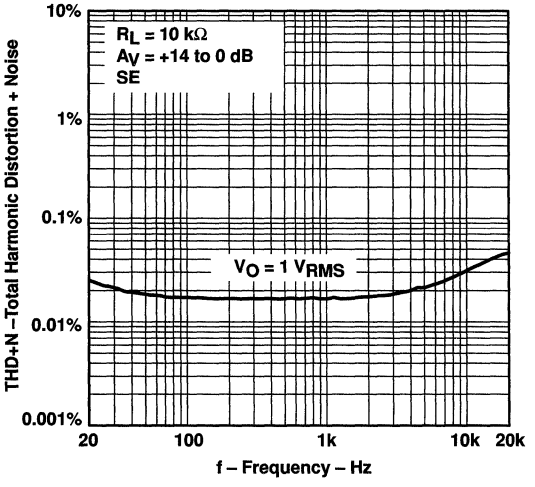


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

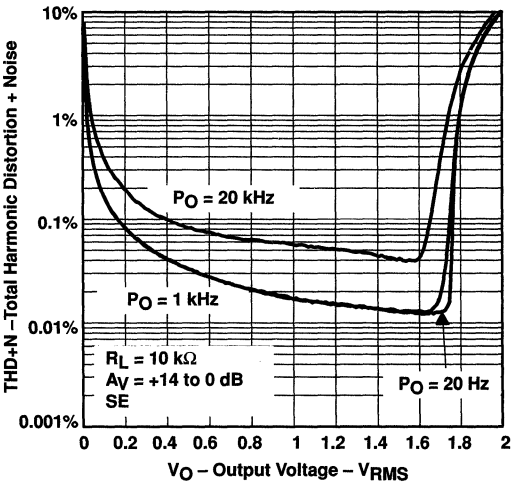


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

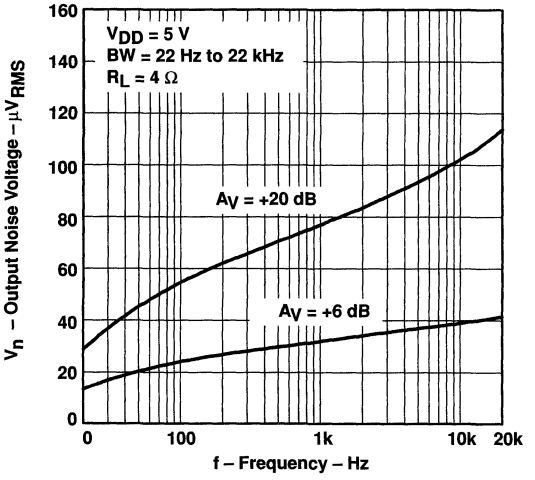


Figure 13

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

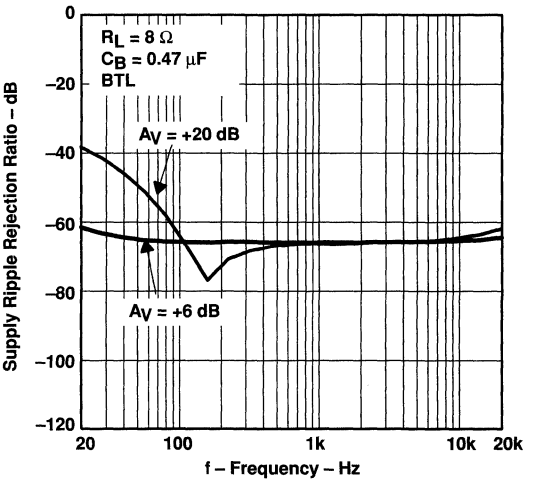


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

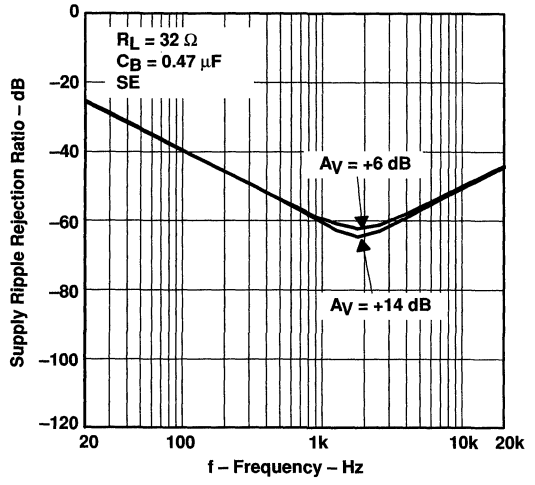


Figure 15

CROSSTALK
vs
FREQUENCY

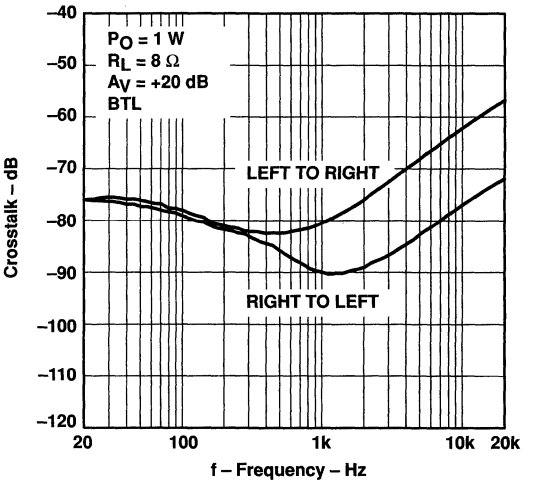


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

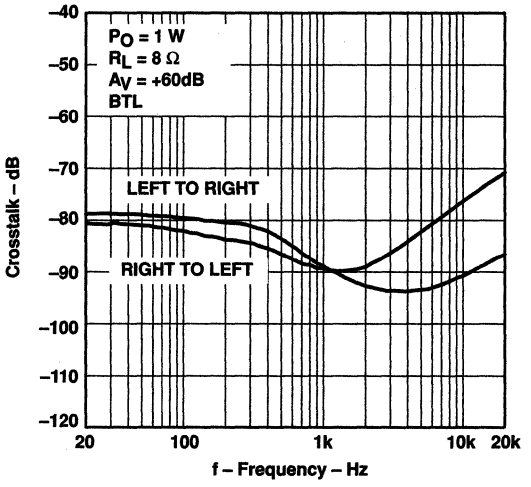


Figure 17

CROSSTALK
vs
FREQUENCY

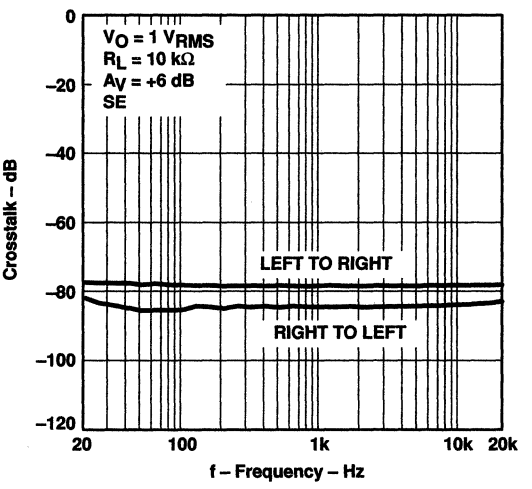


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

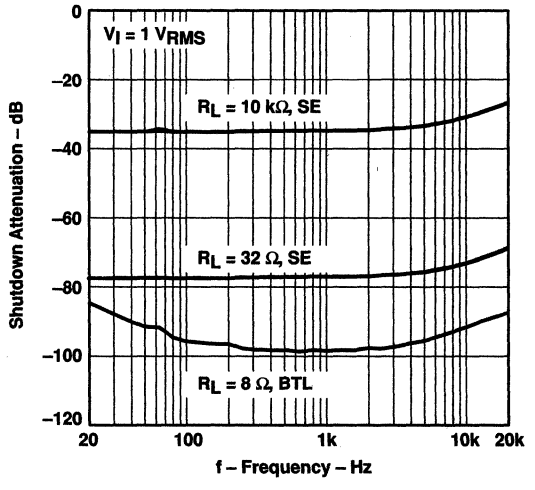


Figure 19

SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

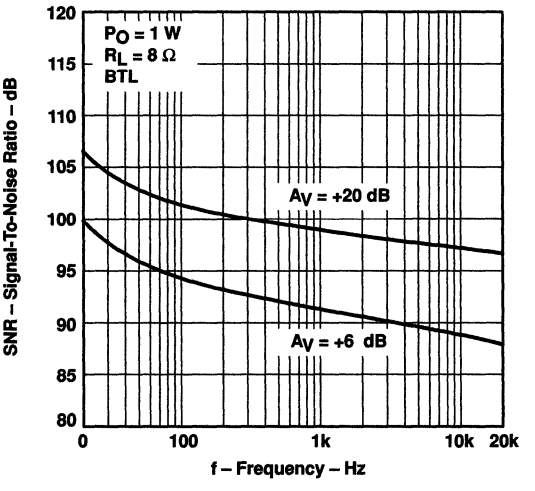


Figure 20

TYPICAL CHARACTERISTICS

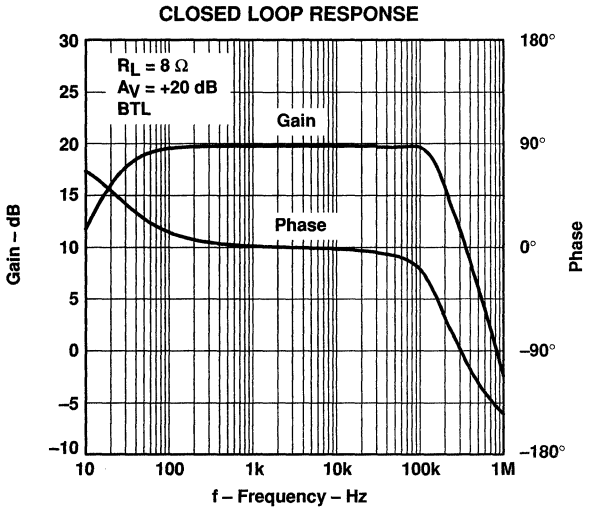


Figure 21

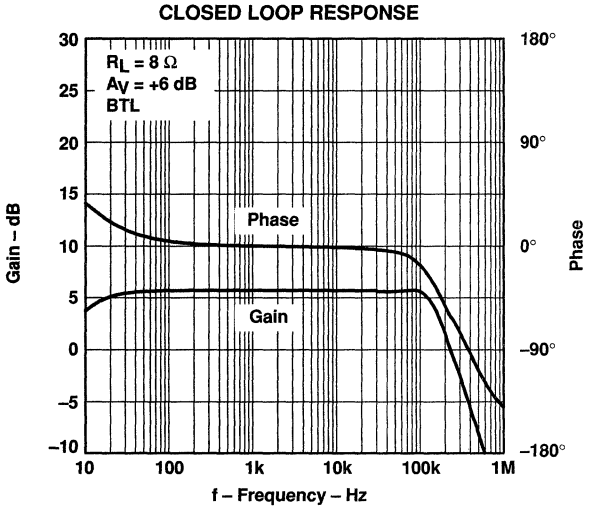


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

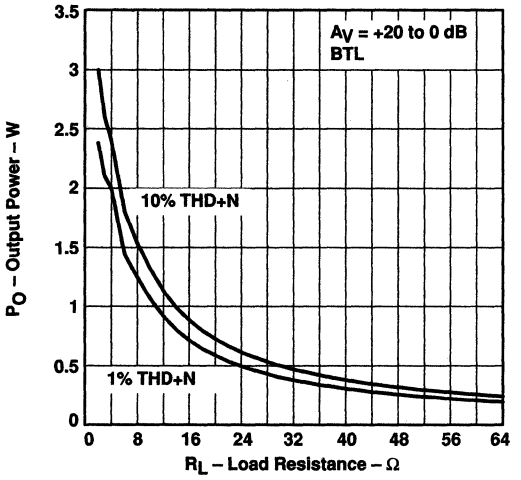


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

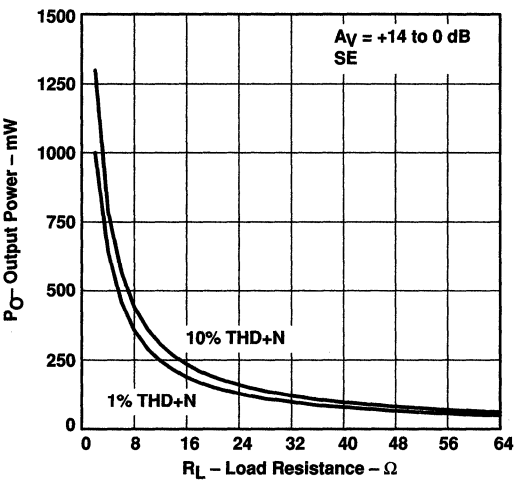


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

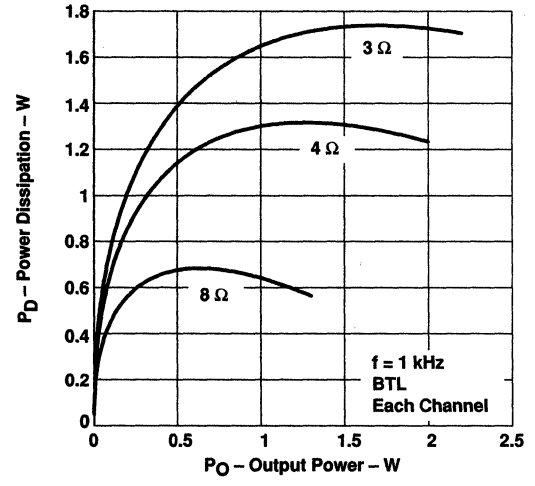


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

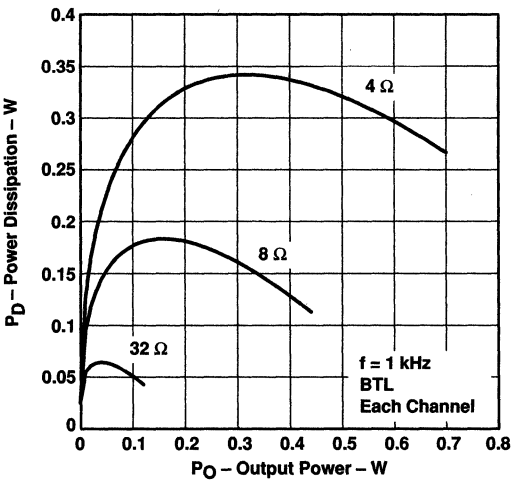


Figure 26

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

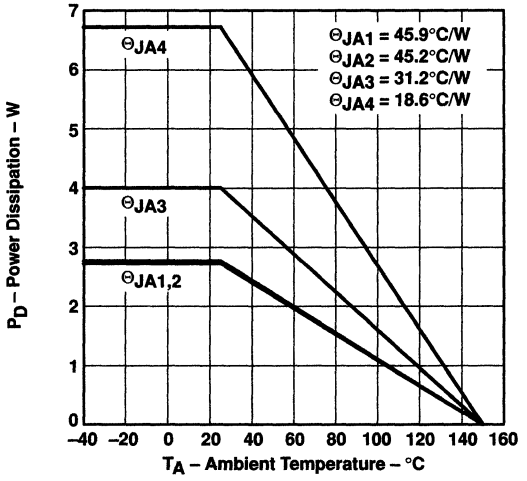


Figure 27

INPUT IMPEDANCE
vs
GAIN

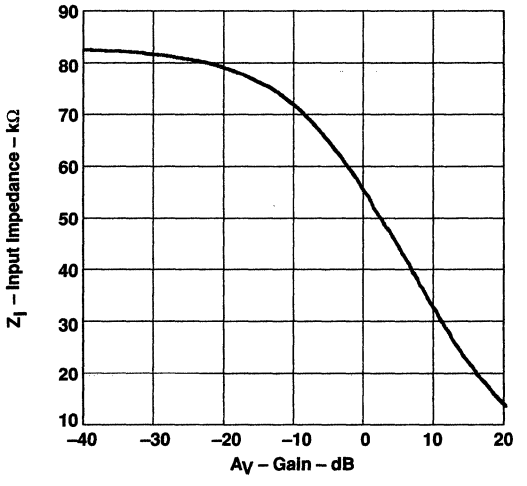


Figure 28

APPLICATION INFORMATION

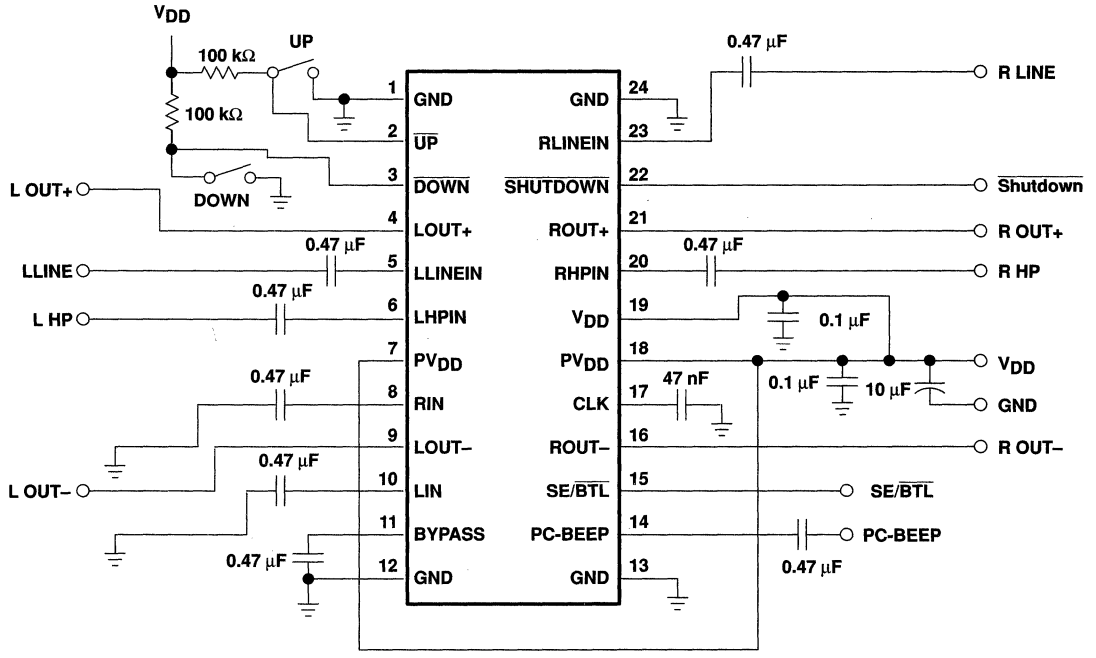
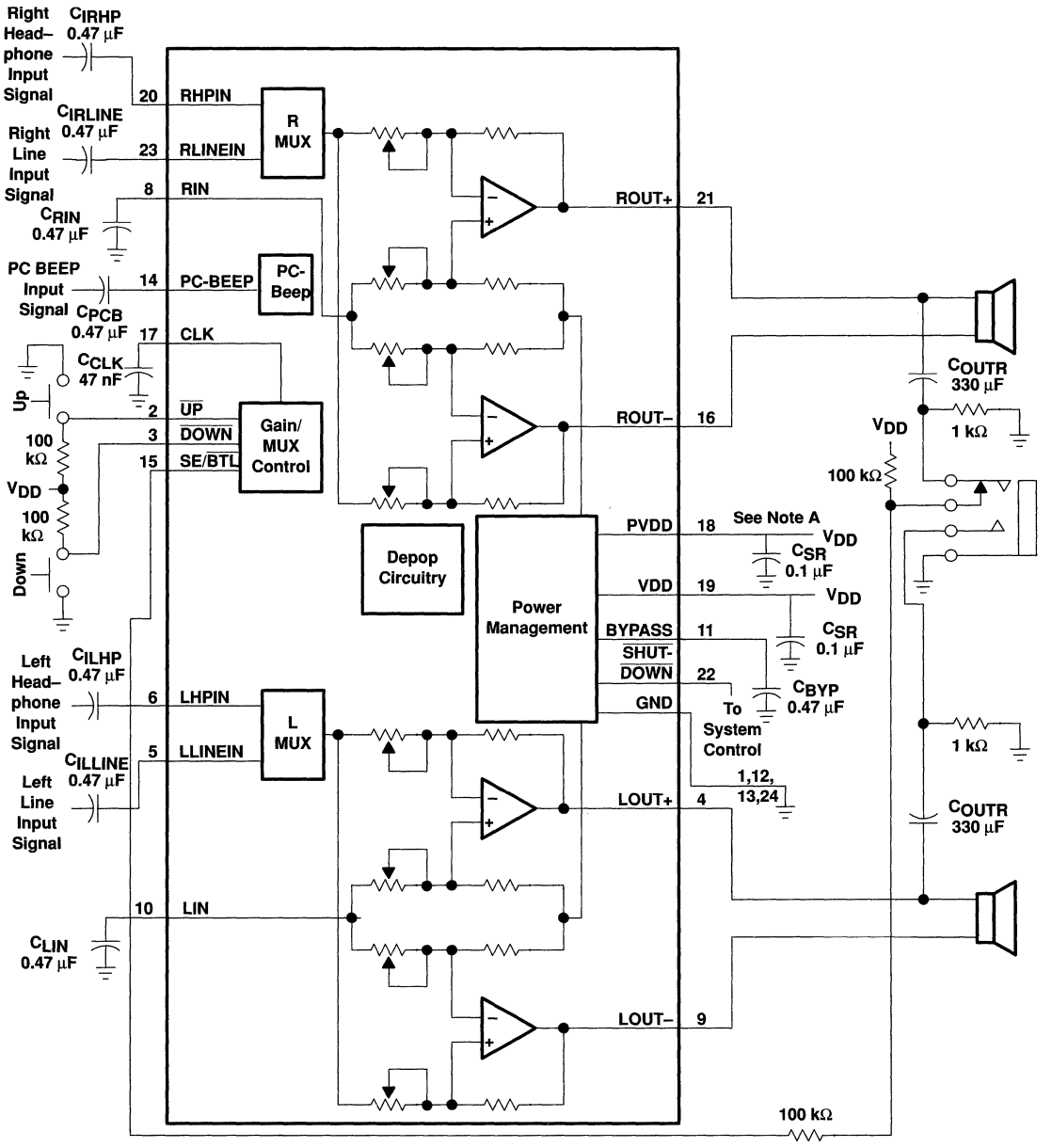


Figure 29. Typical TPA0152 Application Circuit

selection of components

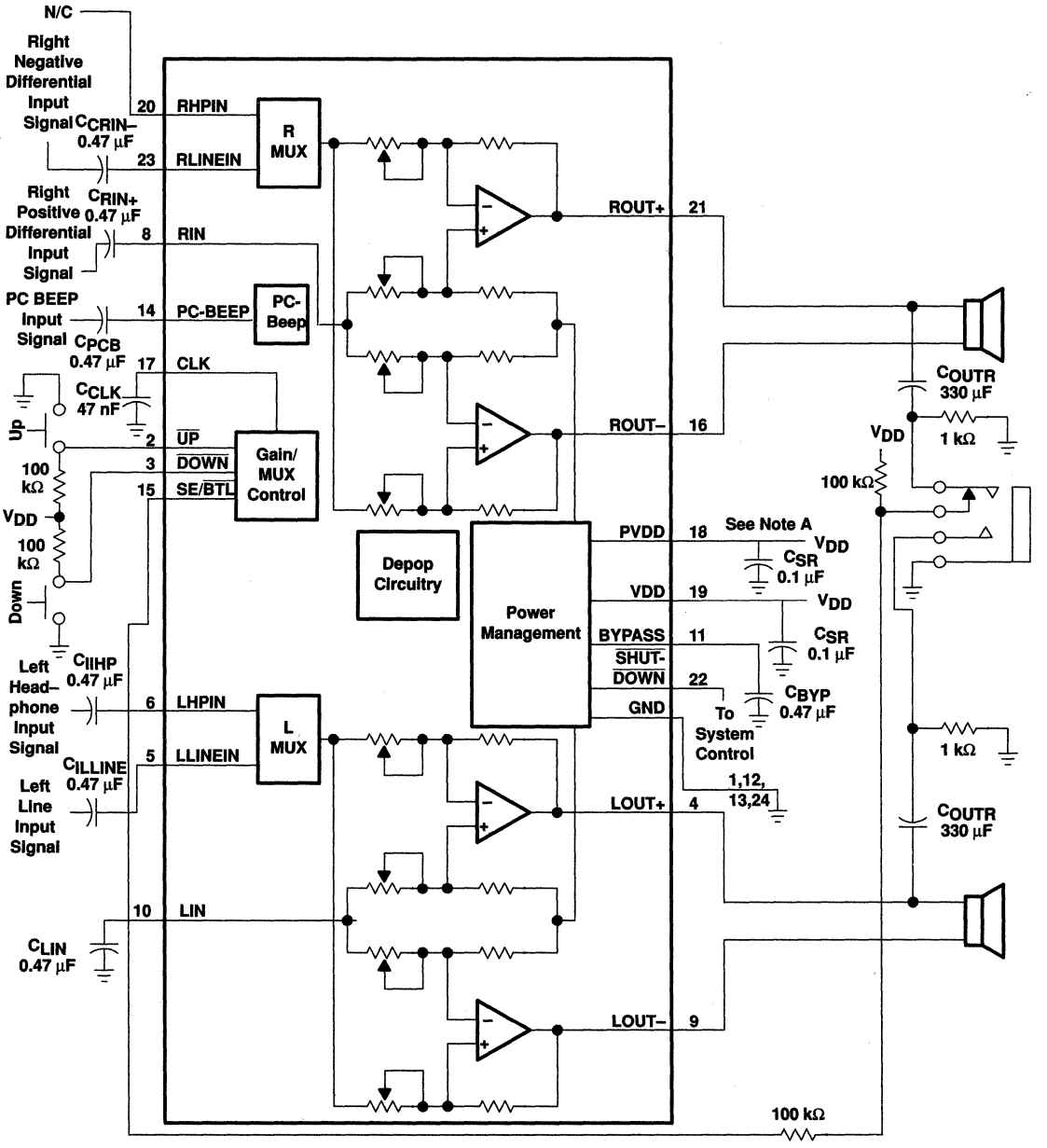
Figure 30 and Figure 31 are a schematic diagrams of typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0152 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



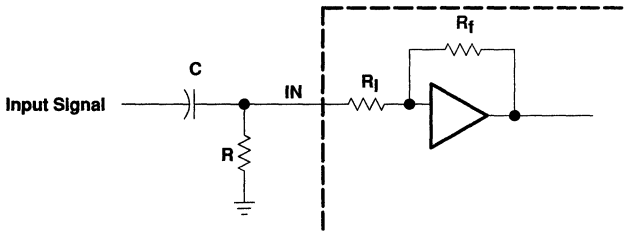
NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0152 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The input resistance at each gain setting is given in the Figure 28.

The –3 dB frequency can be calculated using equation 1.

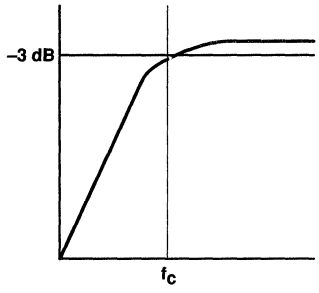
$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \tag{1}$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_{IN}, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \tag{2}$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_C} \tag{3}$$

APPLICATION INFORMATION

input capacitor, C_I (continued)

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0152 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

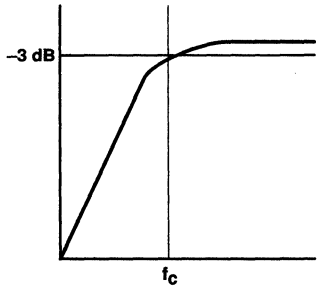
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0152 BTL amplifier consists of two class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

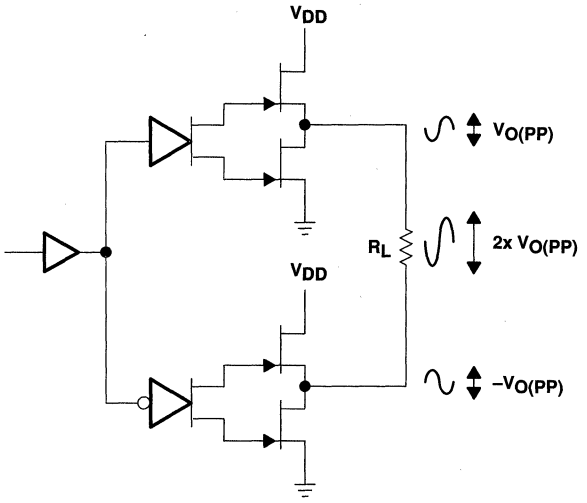


Figure 32. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 33. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

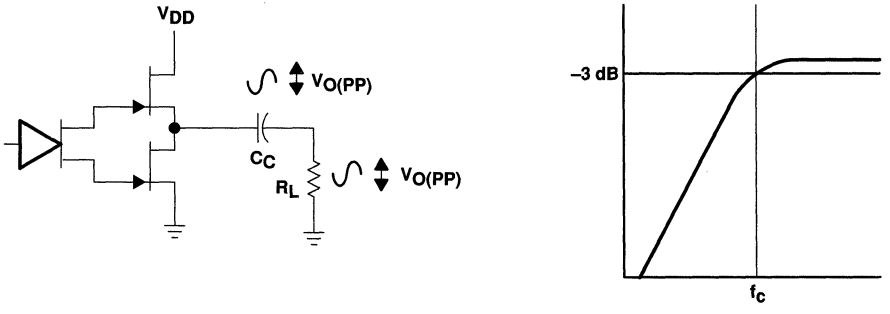


Figure 33. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor section.

single-ended operation

In SE mode (see Figure 32 and Figure 33), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 34).

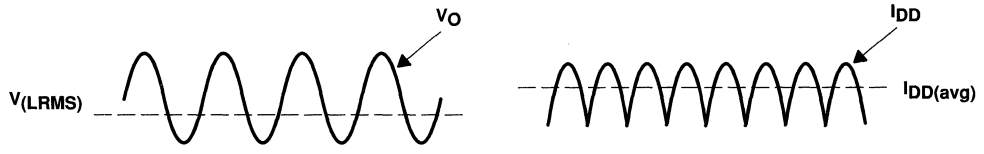


Figure 34. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L\,\text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^{\,2}}{2R_L}$$

and $$P_{SUP} = V_{DD}\, I_{DD}\text{avg} \text{ and } I_{DD}\text{avg} = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

APPLICATION INFORMATION

Therefore,

$$P_{SUP} = \frac{2\ V_{DD}\ V_P}{\pi\ R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\ R_L}}{\frac{2\ V_{DD}\ V_P}{\pi\ R_L}} = \frac{\pi\ V_P}{4\ V_{DD}}$$

Where:

$$V_P = \sqrt{2\ P_L\ R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\ \sqrt{2\ P_L\ R_L}}{4\ V_{DD}} \qquad (8)$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0152 data sheet, one can see that when the TPA0152 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting Watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4W}{1W}\right) = 6\ \text{dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0152 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA0152 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA0152 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dispation rating table on page 4. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0122 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0152 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0152 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0152, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0152 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0152 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 35.

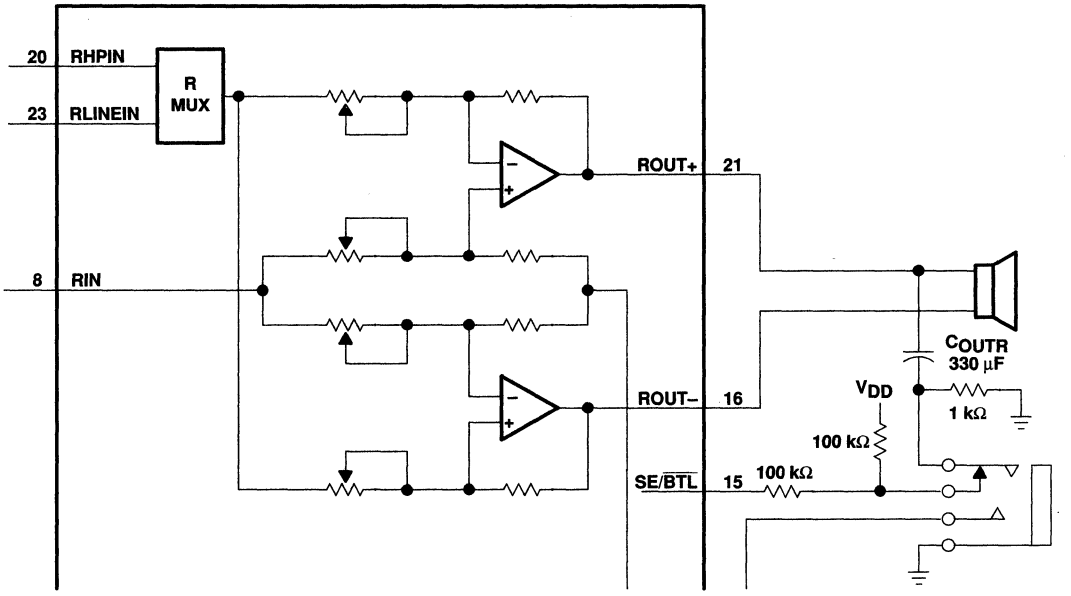


Figure 35. TPA0152 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

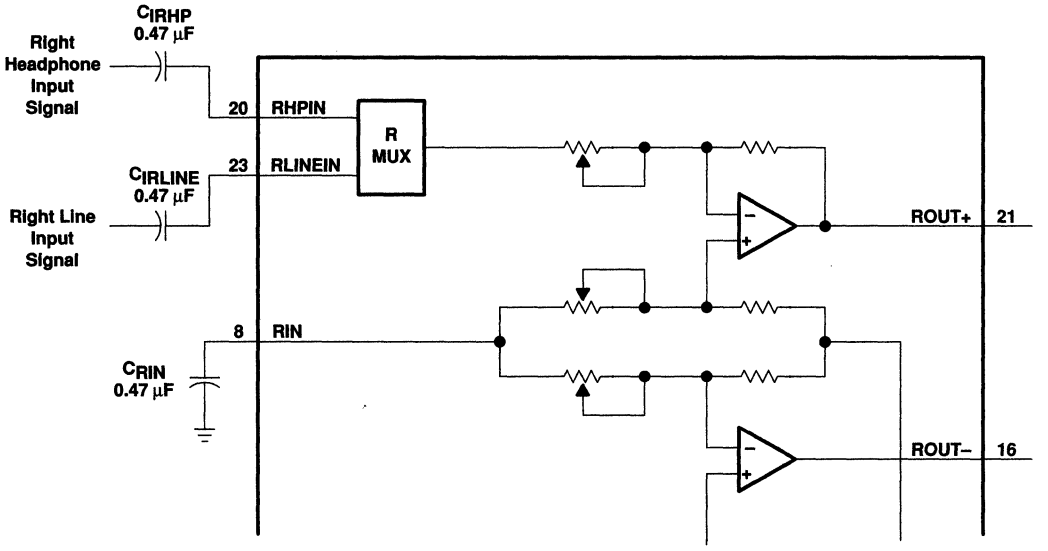


Figure 36. TPA0152 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0152 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

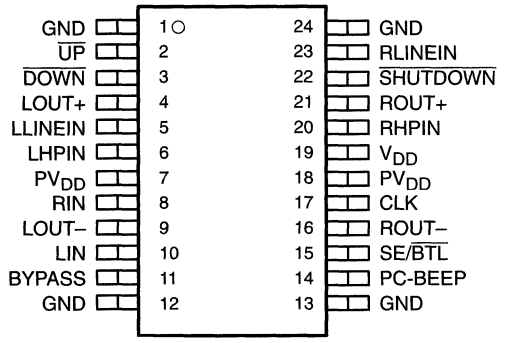
Table 5. Shutdown and Mute Mode Functions

INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Digital Volume Control From 20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0162 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0162 has less than 0.22% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

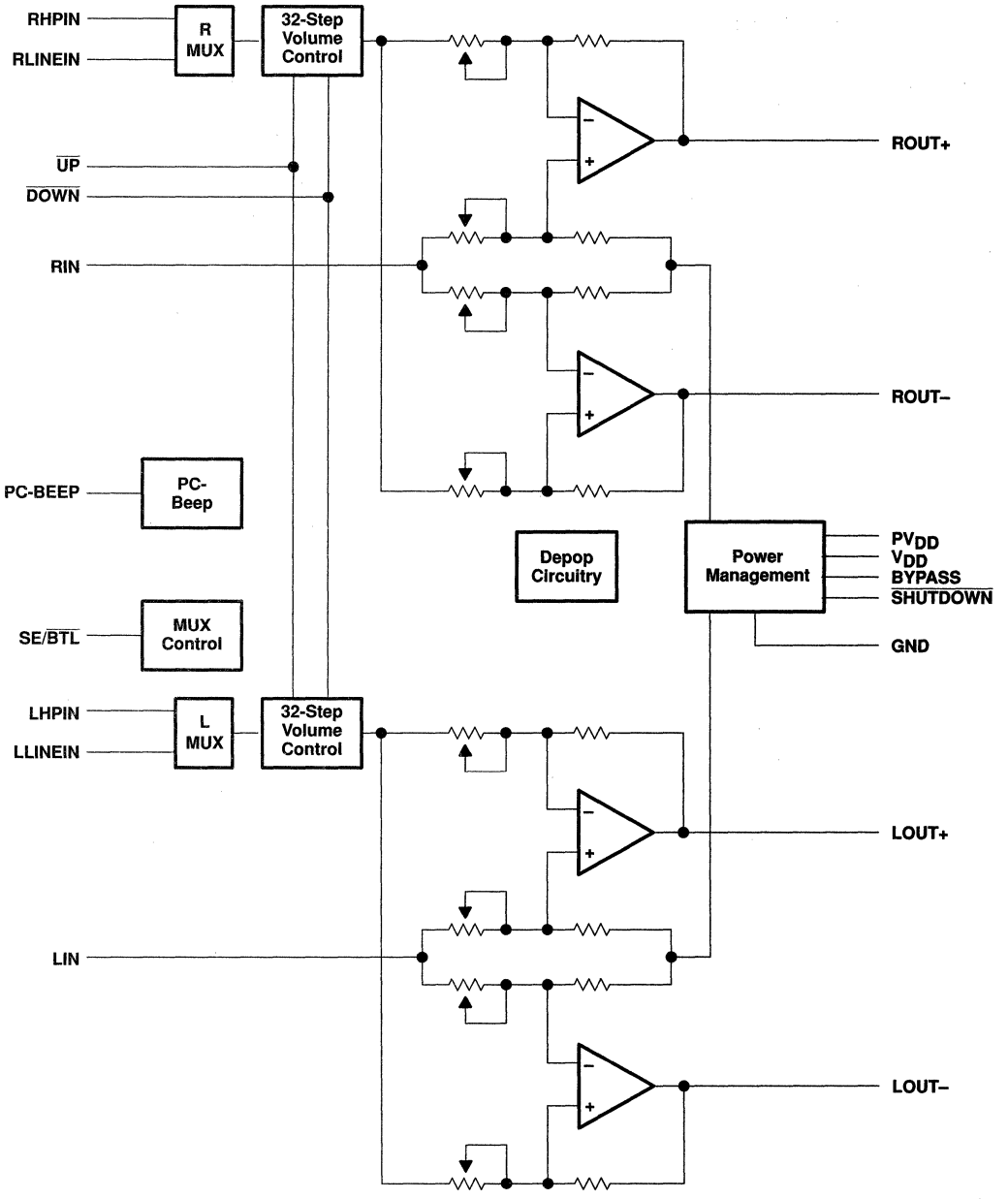
The overall gain of the amplifier is controlled digitally by the UP and DOWN terminals. At power up, the gain is set at the lowest level, –85 dB. It can then be adjusted to any of 31 discrete steps by pulling the voltage down at the desired pin to logic low. The gain is adjusted in the initial stage of the amplifier as opposed to the power output stage. As a result, the THD changes very little over all volume levels.

An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0162 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. This effectively reduces the gain by 6 dB.

The TPA0162 consumes only 20 mA of supply current during normal operation. A miserly shutdown mode is included that reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0162 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0162PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0162PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0162 generates an internal clock. An external clock can override the internal clock input to this terminal.
$\overline{\text{DOWN}}$	3	I	A momentary pulse on this terminal decreases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left-channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
LOUT–	9	O	Left-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low.
ROUT+	21	O	Right-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
ROUT–	16	O	Right-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input MUX control input. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and BTL output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
$\overline{\text{UP}}$	2	I	A momentary pulse on this terminal increases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		20		mA
		SE mode		10		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.22%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		17		µV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Bandwidth	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Bandwidth	20
	Closed loop respone		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

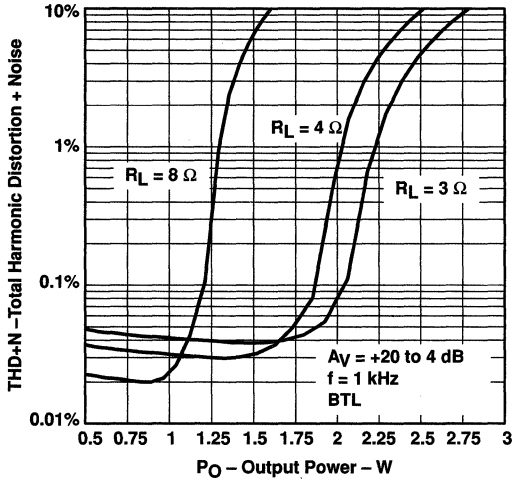


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
VOLTAGE GAIN

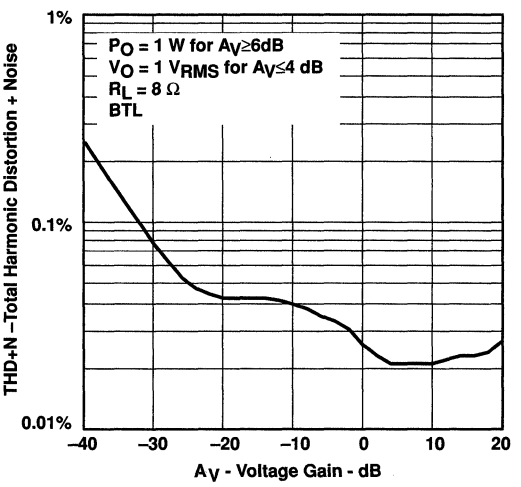


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

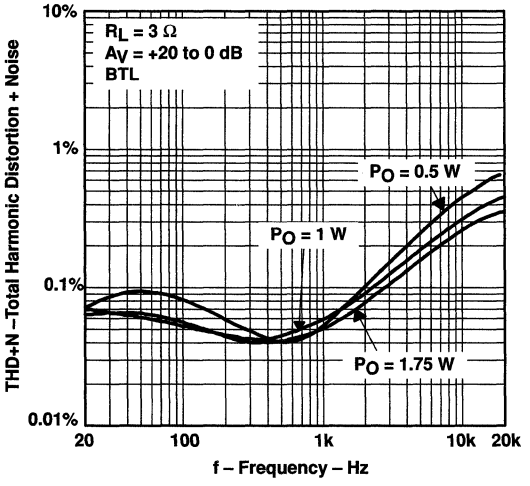


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

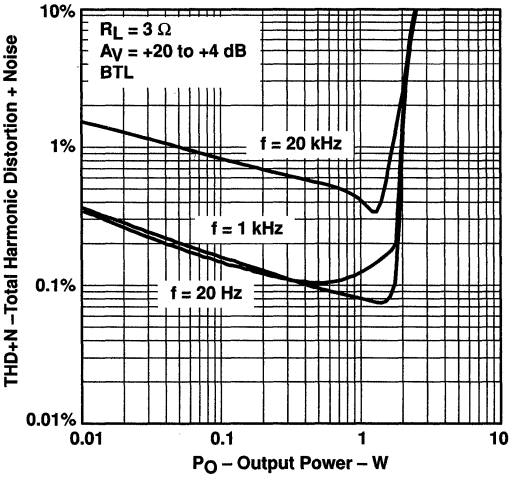


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

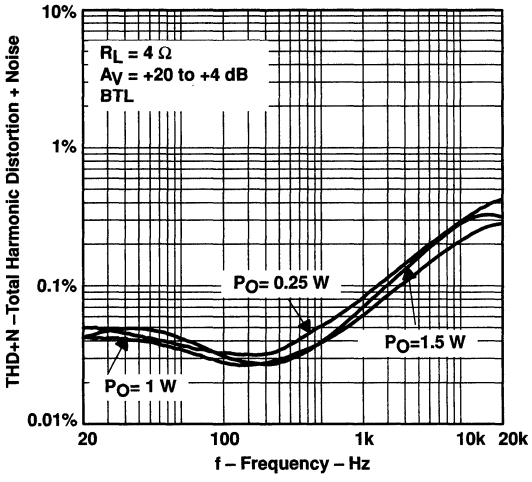


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

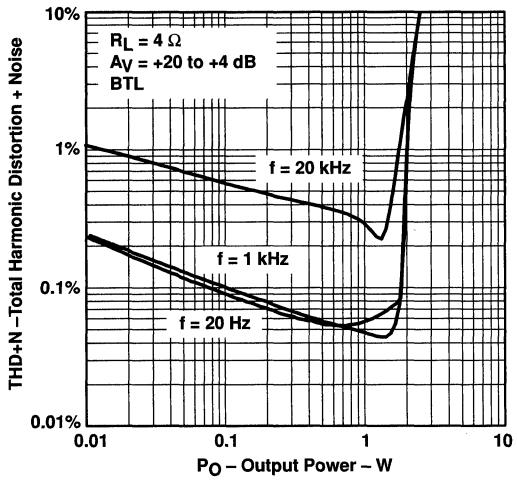


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

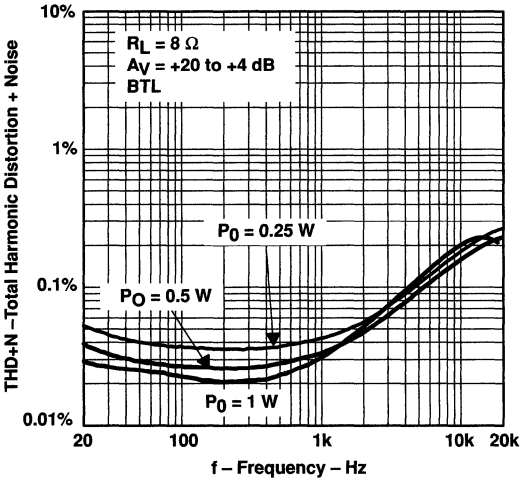


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

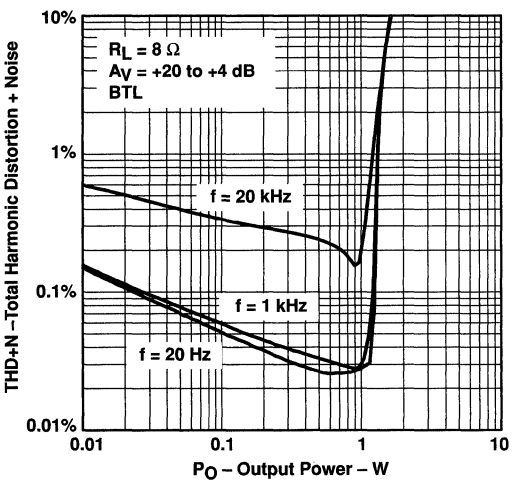


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

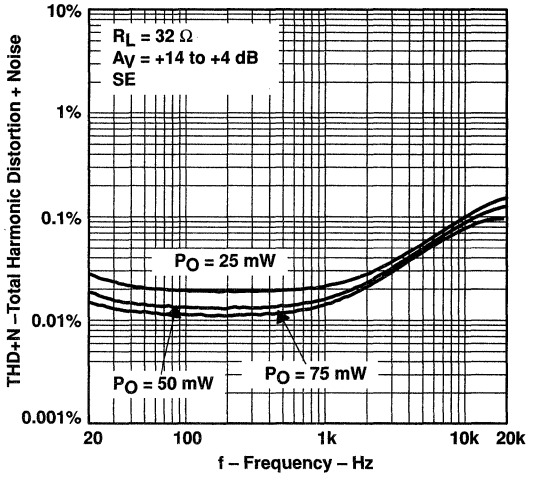


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

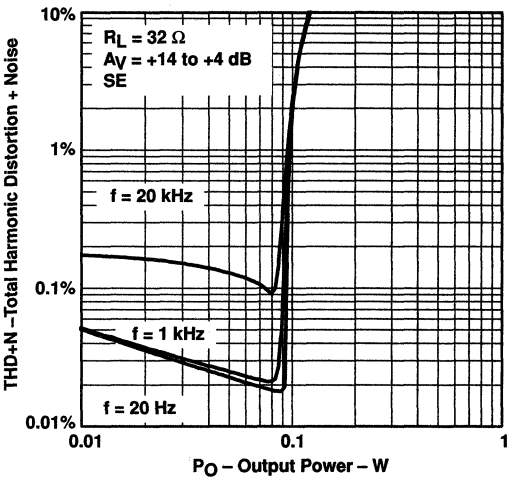


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

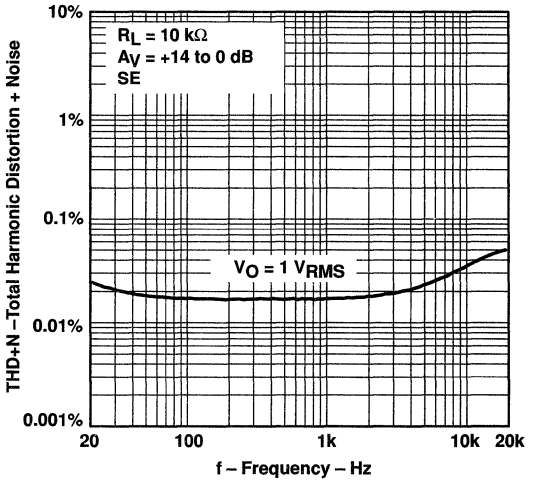


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

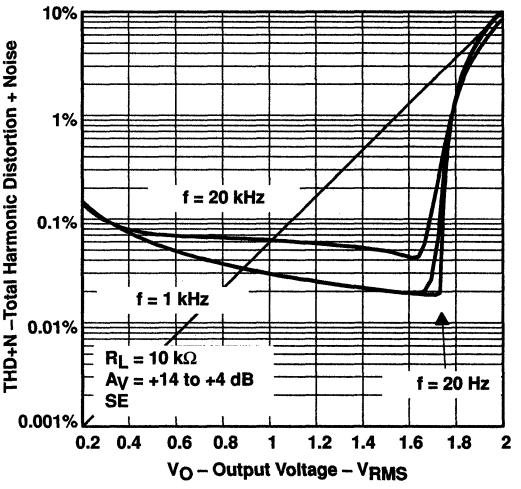


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

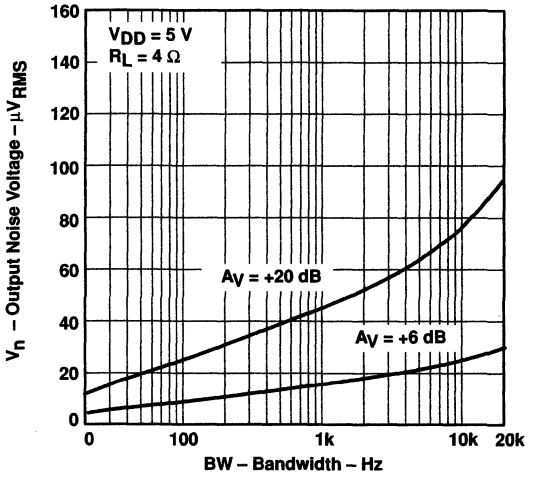


Figure 13

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

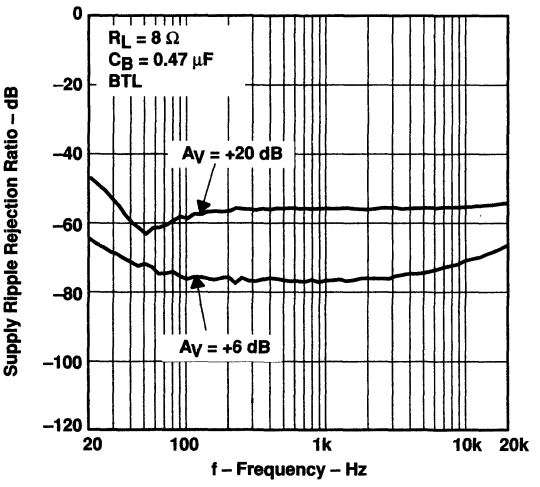


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

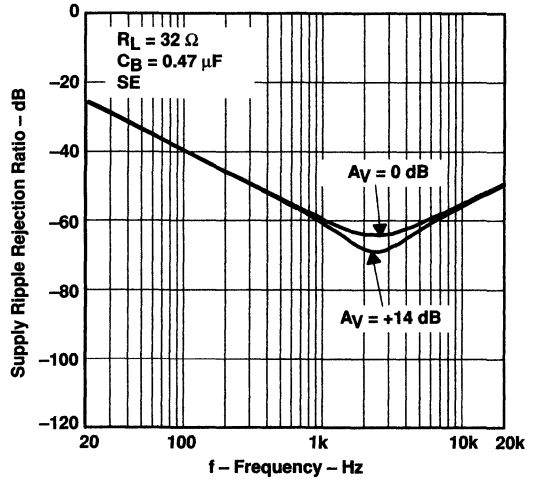


Figure 15

CROSSTALK
vs
FREQUENCY

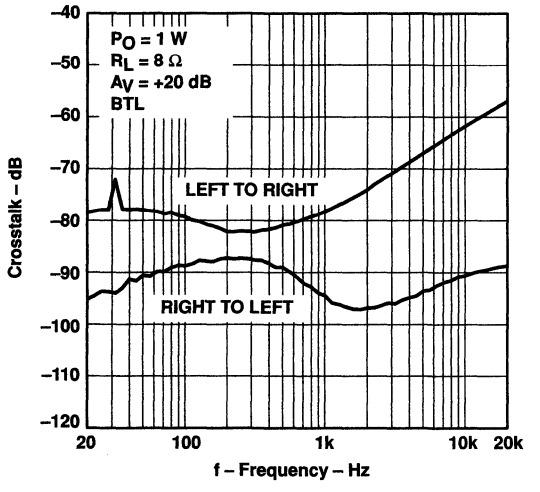


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

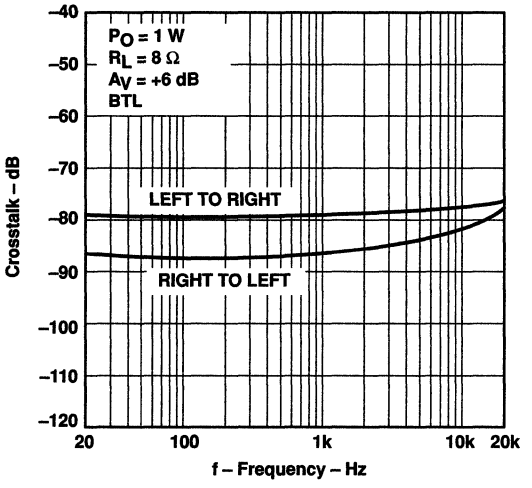


Figure 17

CROSSTALK
vs
FREQUENCY

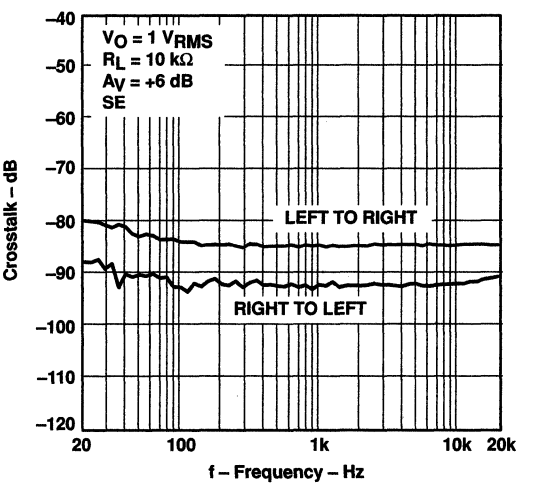


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

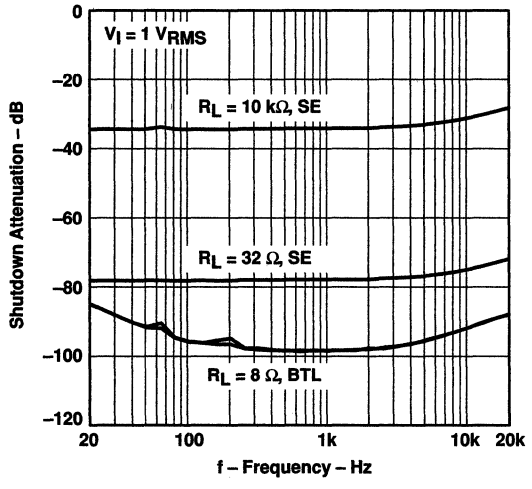


Figure 19

SIGNAL-TO-NOISE RATIO
vs
BANDWIDTH

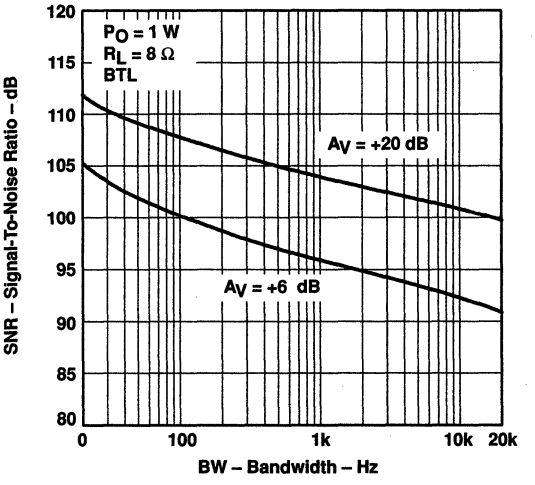


Figure 20

TYPICAL CHARACTERISTICS

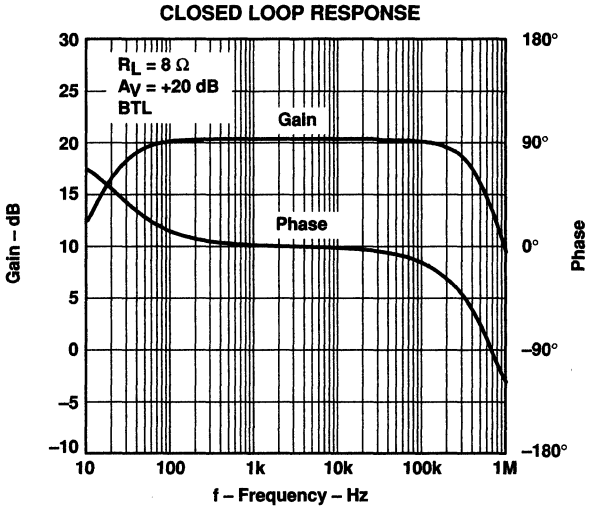


Figure 21

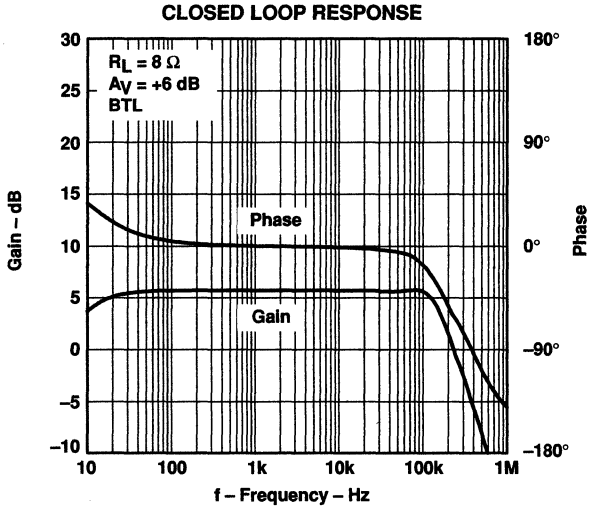


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

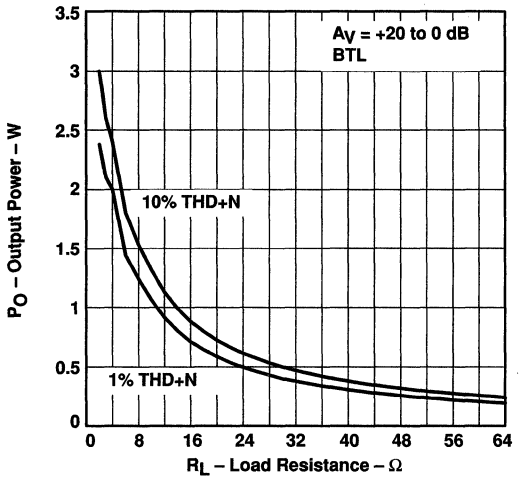


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

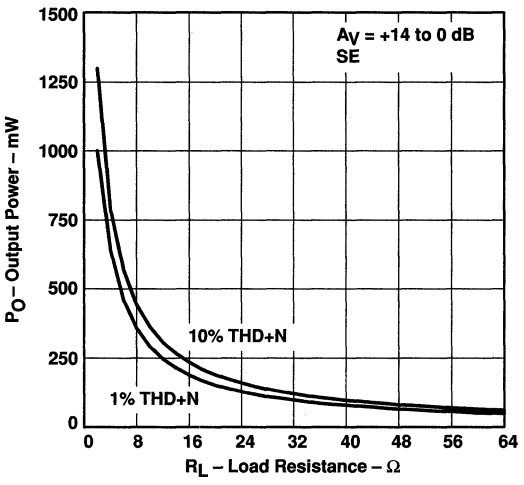


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

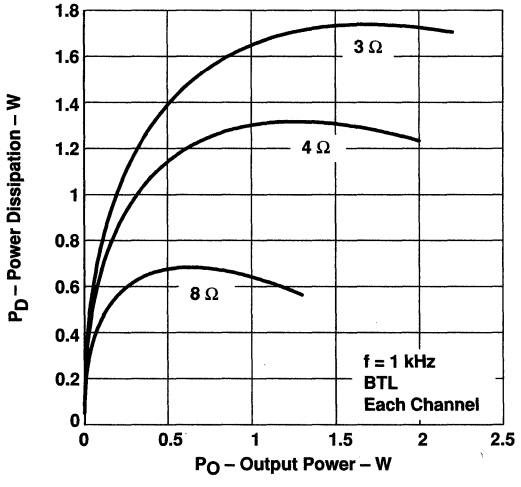


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

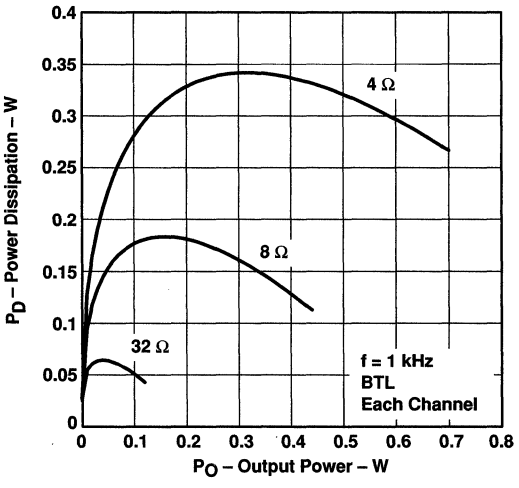


Figure 26

APPLICATION INFORMATION

**POWER DISSIPATION
vs
AMBIENT TEMPERATURE**

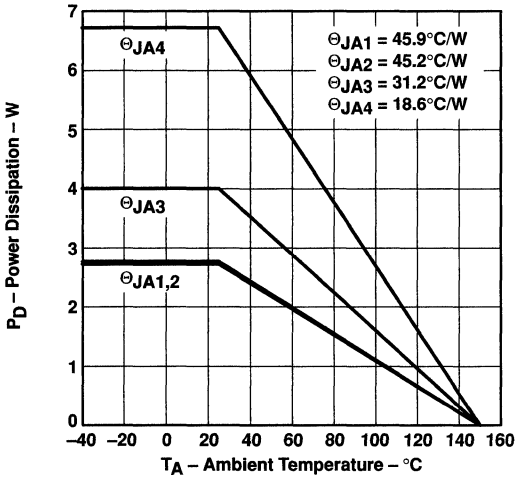


Figure 27

**INPUT IMPEDANCE
vs
GAIN**

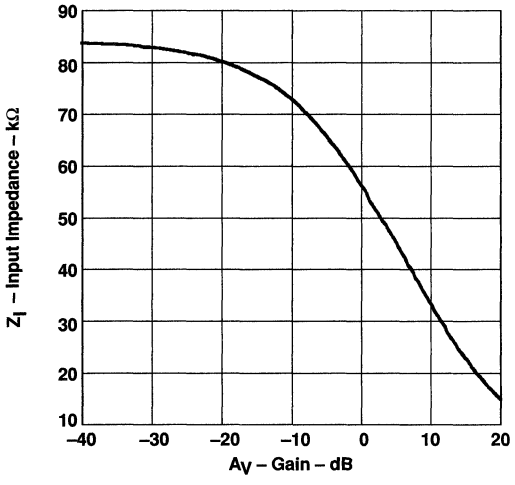


Figure 28

APPLICATION INFORMATION

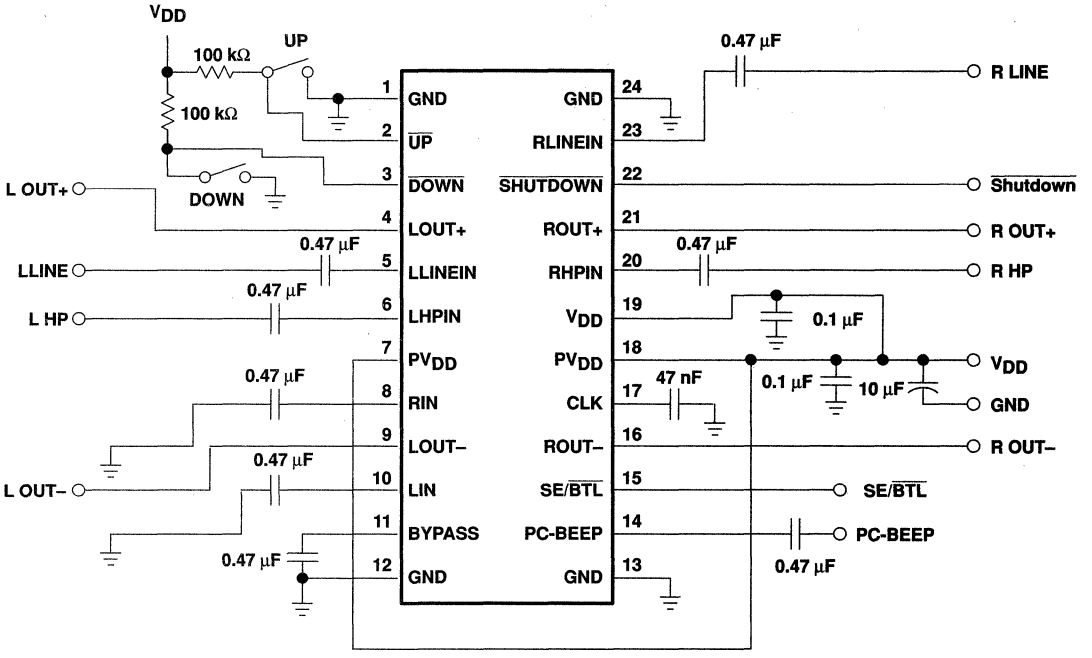
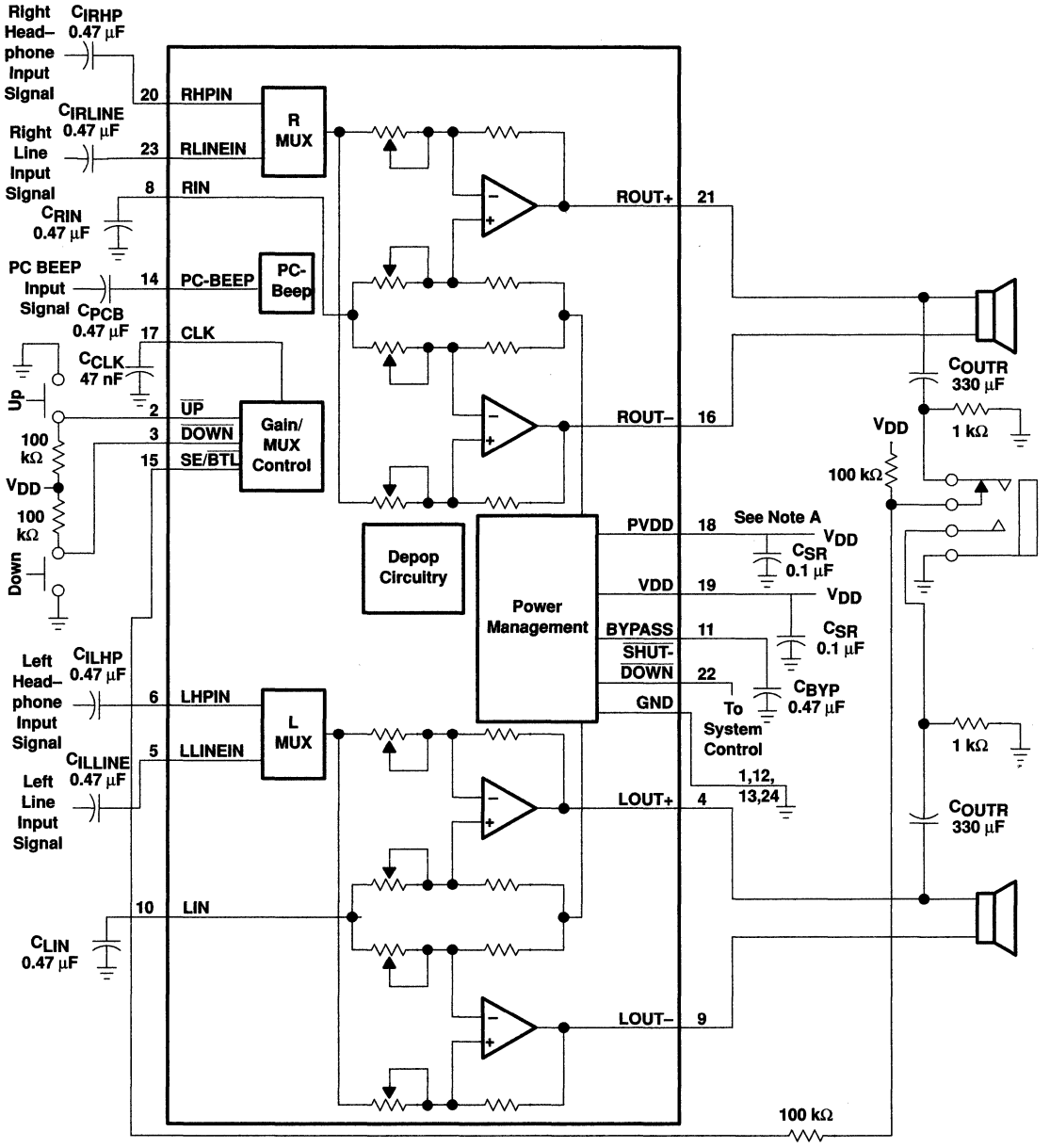


Figure 29. Typical TPA0162 Application Circuit

selection of components

Figure 30 and Figure 31 are a schematic diagrams of typical notebook computer application circuits.

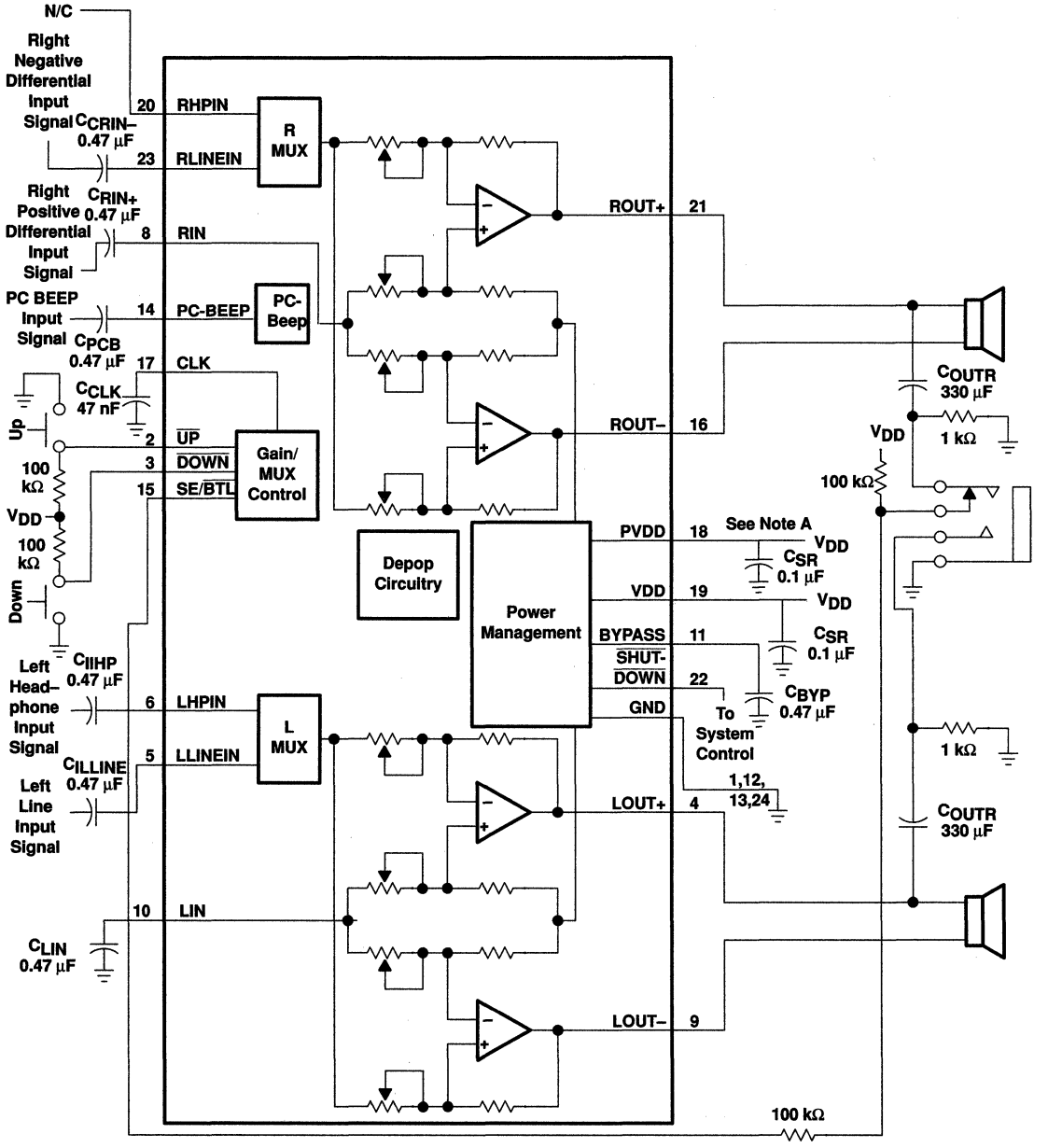
APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0162 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



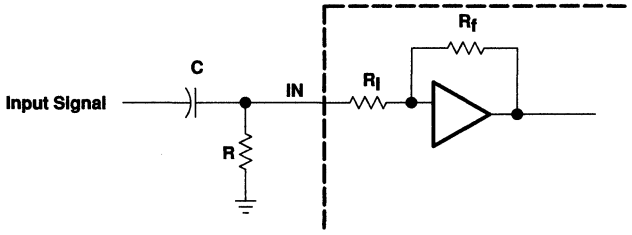
NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0162 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The input resistance at each gain setting is given in Figure 28.

The –3 dB frequency can be calculated using equation 1:

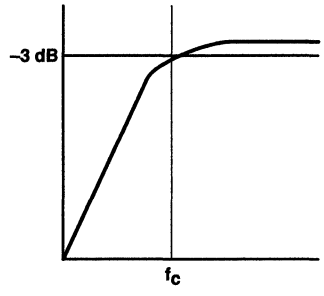
$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0162 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

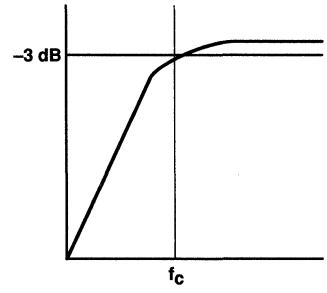
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 32 shows a class-AB audio power amplifier (APA) in a BTL configuration. The TPA0162 BTL amplifier consists of two class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

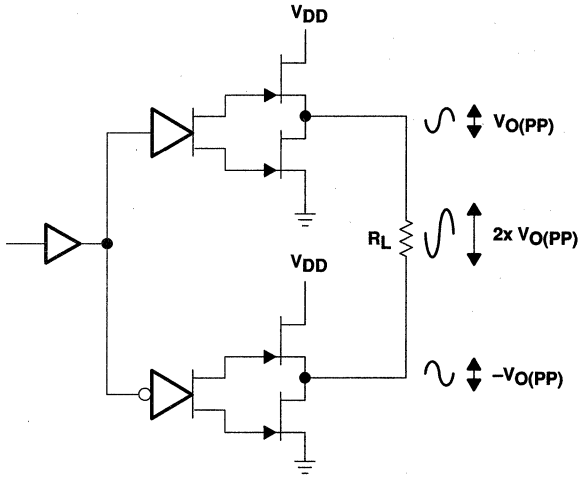


Figure 32. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 33. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

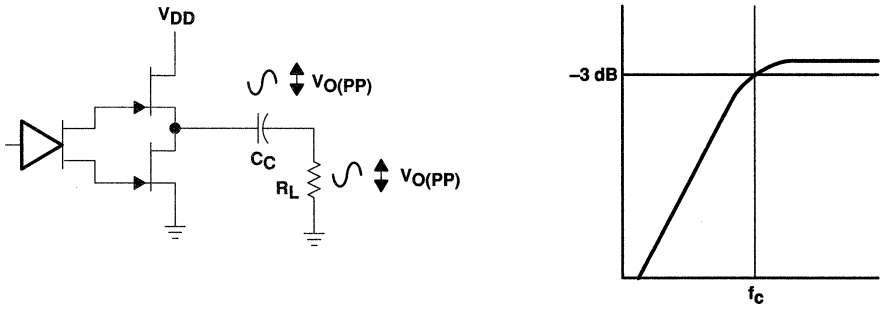


Figure 33. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor section.

single-ended operation

In SE mode (see Figure 32 and Figure 33), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 34).

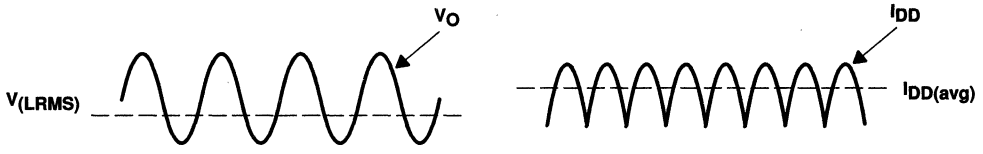


Figure 34. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}\text{avg} \text{ and } I_{DD}\text{avg} = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Therefore,

$$P_{SUP} = \frac{2\ V_{DD}\ V_P}{\pi\ R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\ R_L}}{\frac{2\ V_{DD}\ V_P}{\pi\ R_L}} = \frac{\pi\ V_P}{4\ V_{DD}}$$

Where:

$$V_P = \sqrt{2\ P_L\ R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\ \sqrt{2\ P_L\ R_L}}{4\ V_{DD}} \qquad (8)$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature the internal dissipated power at the average output power level must be used. From the TPA0162 data sheet, one can see that when the TPA0162 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{4W}{1W}\right) = 6\ \text{dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0162 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA0162 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 4. TPA0162 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table on page 4. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (12)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0162 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$
$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0162 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0162 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0162, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0162 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0162 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 35.

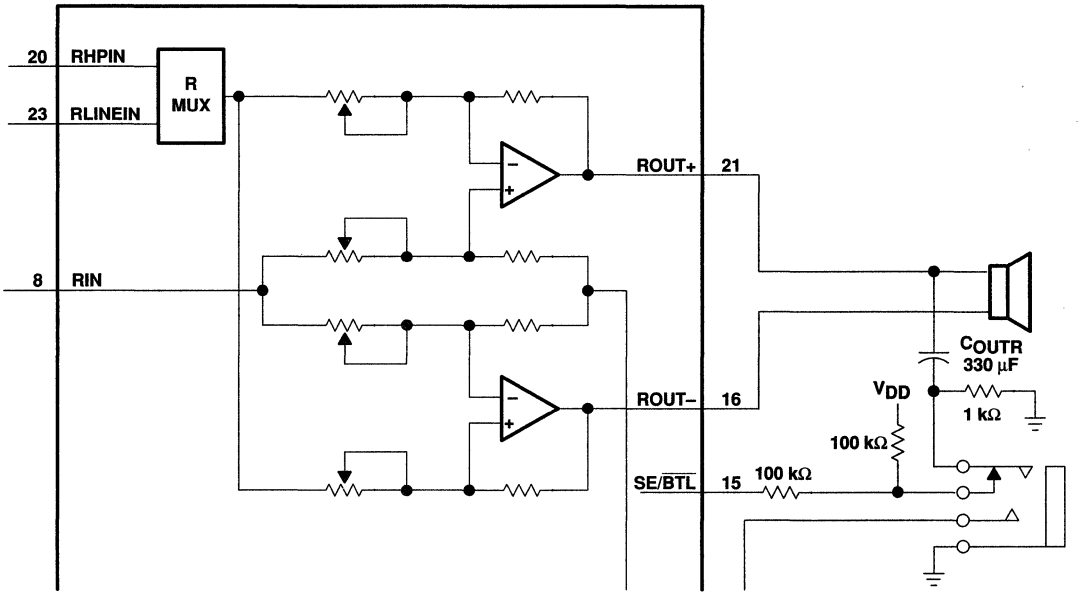


Figure 35. TPA0162 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut-down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically, but may be selected manually by pulling PCB ENABLE high. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be a accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 μs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

When PCB ENABLE is held high, PC BEEP is selected and the LINEIN and HPIN inputs are deactivated regardless of the input signal. PCB ENABLE has an internal 100 kΩ pulldown resistor and will trip at approximately $V_{DD}/2$.

If it is desired to ac couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

APPLICATION INFORMATION

Input MUX operation

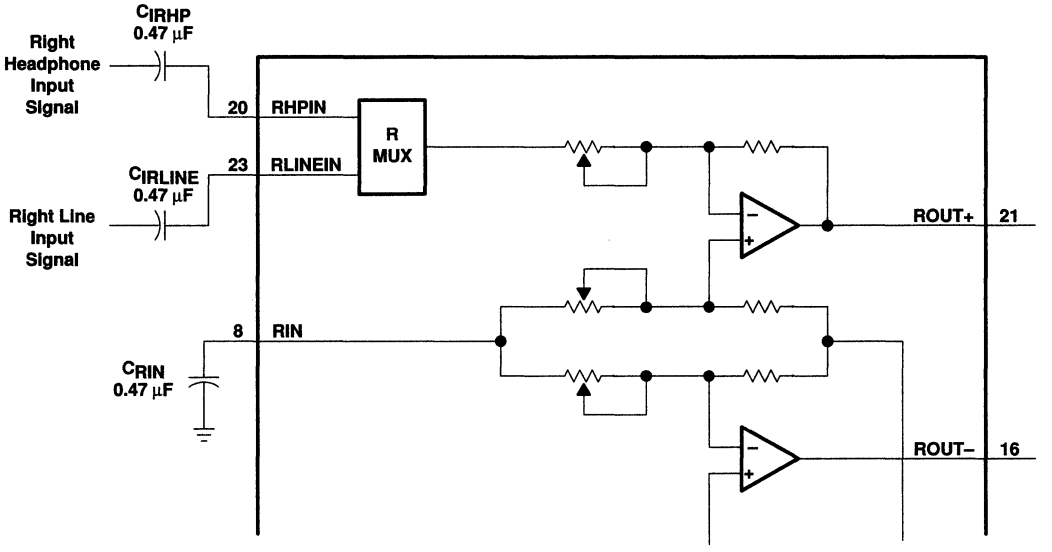


Figure 36. TPA0162 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

shutdown modes

The TPA0162 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

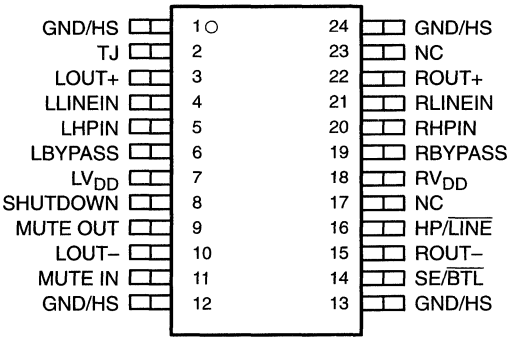
Table 5. Shutdown and Mute Mode Functions

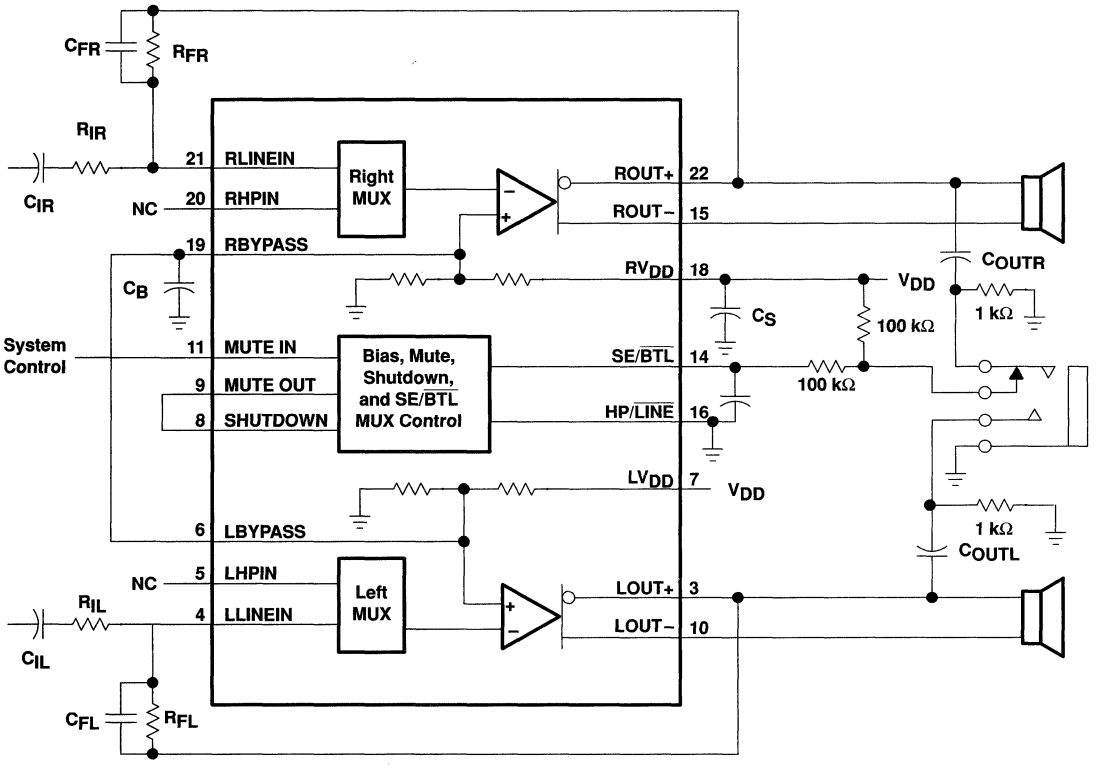
INPUTS†		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Integrated Depop Circuitry**
- **High Power with PC Power Supply**
  - **2 W/Ch at 5 V into a 3-Ω Load**
  - **800 mW/Ch at 3 V**
- **Fully Specified for Use With 3-Ω Loads**
- **Ultra-Low Distortion**
  - **0.05% THD+N at 2 W and 3-Ω Load**
- **Bridge-Tied Load (BTL) or Single-Ended (SE) Modes**
- **Stereo Input MUX**
- **Surface-Mount Power Package**
  24-Pin TSSOP PowerPAD™
- **Shutdown Control . . . I_{DD} = 5 μA**

PWP PACKAGE
(TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

description

The TPA0202 is a stereo audio power amplifier in a 24-pin TSSOP thermal package capable of delivering greater than 2 W of continuous RMS power per channel into 3-Ω loads. The TPA0202 simplifies design and frees up board space for other features. Full power distortion levels of less than 0.1% THD+N from a 5-V supply are typical. Low-voltage applications are also well served by the TPA0202 providing 800-mW per channel into 3-Ω loads with a 3.3-V supply voltage.

The TPA0202 has integrated depop circuitry that virtually eliminates transients that cause noise in the speakers during power up and when using the mute and shutdown modes.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the TPA0202 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. Using the TPA0202 to drive line outputs up to 700 mW/channel into external 3-Ω loads is ideal for small non-powered external speakers in portable multimedia systems. The TPA0202 also features a shutdown function for power sensitive applications, holding the supply current at 5 μA.

The PowerPAD package† (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0202 to operate at full power into 3-Ω loads at ambient temperature of up to 85°C with 300 CFM of forced-air cooling. Into 8-Ω loads, the operating ambient temperature increases to 100°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP‡ (PWP)
–40°C to 85°C	TPA0202PWP

‡ The PWP packages are available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA0202PWPR).

† See Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (Literature Number SLMA002) for more information on the PowerPAD package.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND/HS	1, 12, 13, 24		Ground connection for circuitry, directly connected to thermal pad
HP/$\overline{\text{LINE}}$	16	I	Input MUX control input, hold high to select LHP IN or RHP IN (5, 20), hold low to select LLINE IN or RLINE IN (4, 21)
LBYPASS	6		Tap to voltage divider for left channel internal mid-supply bias
LHP IN	5	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
LLINE IN	4	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
LOUT+	3	O	Left channel + output in BTL mode, + output in SE mode
LOUT–	10	O	Left channel – output in BTL mode, high-impedance state in SE mode
LV_{DD}	7	I	Supply voltage input for left channel and for primary bias circuits
MUTE IN	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute
MUTE OUT	9	O	Follows MUTE IN terminal (11), provides buffered output
NC	17, 23		No internal connection
RBYPASS	19		Tap to voltage divider for right channel internal mid–supply bias
RHPIN	20	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high
RLINEIN	21	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low
ROUT+	22	O	Right channel + output in BTL mode, + output in SE mode
ROUT–	15	O	Right channel – output in BTL mode, high impedance state in SE mode
RV_{DD}	18	I	Supply voltage input for right channel
SE/$\overline{\text{BTL}}$	14	I	Hold low for BTL mode, hold high for SE mode
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, $I_{DD} = 5\ \mu A$
TJ	2	O	Sources a current proportional to the junction temperature. This terminal should be left unconnected during normal operation. For more information, see the *junction temperature measurement* section of this document.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP‡	2.7 W	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}			3	5	5.5	V
Operating free-air temperature, T_A	V_{DD} = 5 V, 250 mW/ch average power,	4-Ω stereo BTL drive, with proper PCB design	–40		85	°C
	V_{DD} = 5 V, 2 W/ch average power,	3-Ω stereo BTL drive, with proper PCB design and 300 CFM forced-air cooling	–40		85	
Common mode input voltage, V_{ICM}	V_{DD} = 5 V		1.25		4.5	V
	V_{DD} = 3.3 V		1.25		2.7	

dc electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS			TYP†	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 5 V	Stereo BTL		19	25	mA
			Stereo SE		9	15	mA
			Mono BTL		9	15	mA
			Mono SE		3	10	mA
		V_{DD} = 3.3 V	Stereo BTL		13	20	mA
			Stereo SE		5	10	mA
			Mono BTL		5	10	mA
			Mono SE		3	6	mA
V_{OO}	Output offset voltage (measured differentially)	V_{DD} = 5 V,	Gain = 2,	See Note 1	5	25	mV
$I_{DD(MUTE)}$	Supply current in mute mode	V_{DD} = 5 V			1.5		mA
$I_{DD(SD)}$	I_{DD} in shutdown	V_{DD} = 5 V			5	15	µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 3 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%,	BTL,	See Figure 3	2		W
		THD = 1%,	BTL,	See Figure 3	2.2		
THD+N	Total harmonic distortion plus noise	P_O = 2W,	f = 20 – 20 kHz,	See Figure 5	200		m%
		V_I = 1 V,	R_L = 10 kΩ,	A_V = 1 V/V	100		m%
B_{OM}	Maximum output power bandwidth	A_V = 10 V/V	THD < 1 %,	See Figure 5	>20		kHz
	Phase margin	R_L = 4 Ω,	Open Loop,	See Figure 43	85°		
	Supply ripple rejection ratio	f = 1 kHz,	See Figure 37		80		dB
		f = 20 – 20 kHz,	See Figure 37		60		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz,	See Figure 39		85		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage	See Figure 35			21		μV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 3 Ω

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
P_O	Output power (each channel) see Note 2	THD = 0.2%,	BTL,	See Figure 10	800		mW
		THD = 1%,	BTL,	See Figure 10	900		
THD+N	Total harmonic distortion plus noise	P_O = 800 mW,	f = 20 – 20 kHz,	See Figure 11	350		m%
		V_I = 1 V,	R_L = 10 kΩ,	A_V = 1 V/V	200		m%
B_{OM}	Maximum output power bandwidth	A_V = 10 V/V	THD < 1 %,	See Figure 11	>20		kHz
	Phase margin	R_L = 4 Ω,	Open Loop,	See Figure 44	85°		
	Supply ripple rejection ratio	f = 1 kHz,	See Figure 37		70		dB
		f = 20 – 20 kHz,	See Figure 37		55		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz,	See Figure 40		85		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage	See Figure 37			21		μV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

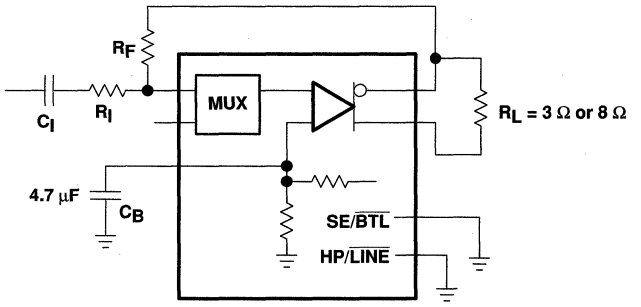


Figure 1. BTL Test Circuit

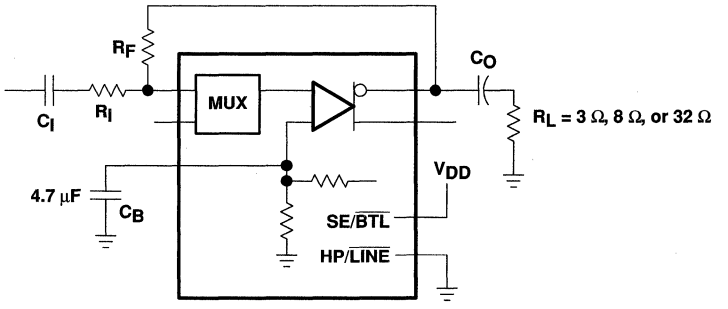


Figure 2. SE Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Frequency	4, 5, 7, 8, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24, 26, 27, 29, 30 32, 33
		vs Output power	3, 6, 9, 10, 13, 16, 19, 22, 25, 28, 31, 34
V_n	Output noise voltage	vs Frequency	35,36
	Supply ripple rejection ratio	vs Frequency	37,38
	Crosstalk	vs Frequency	39 – 42
	Open loop response	vs Frequency	43,44
	Closed loop response	vs Frequency	45, 48
I_{DD}	Supply current	vs Supply voltage	49
P_O	Output power	vs Supply voltage vs Load resistance	50, 51 52, 53
P_D	Power dissipation	vs Output power	54 – 57

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

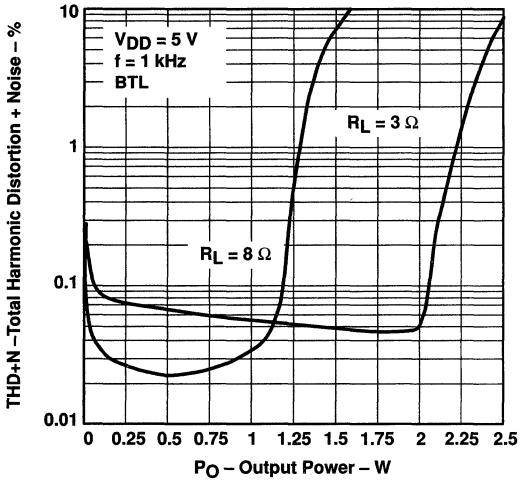


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

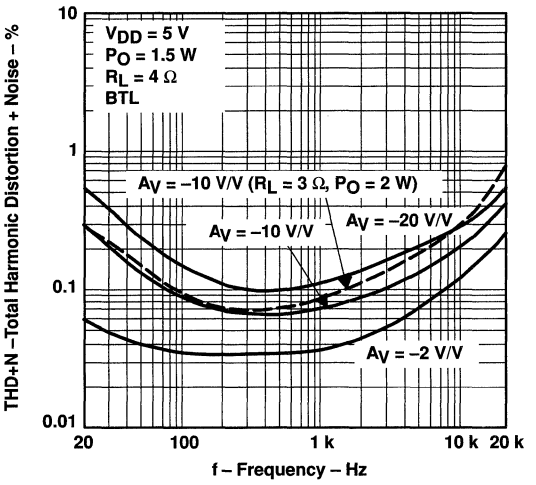


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

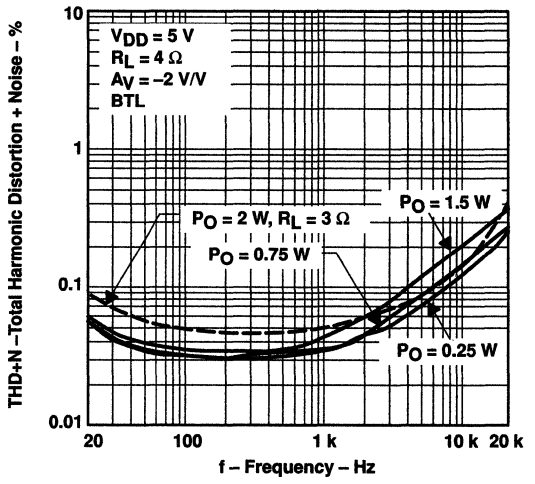


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

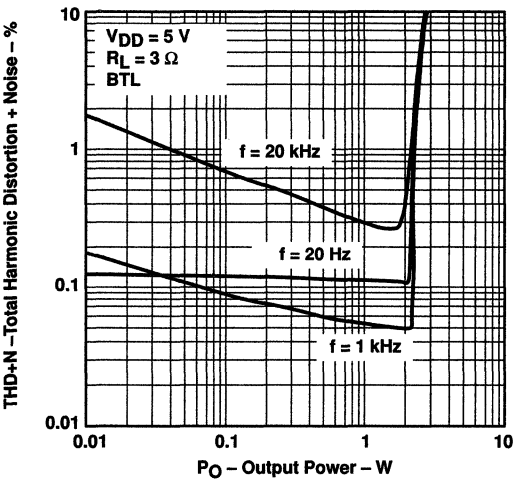


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

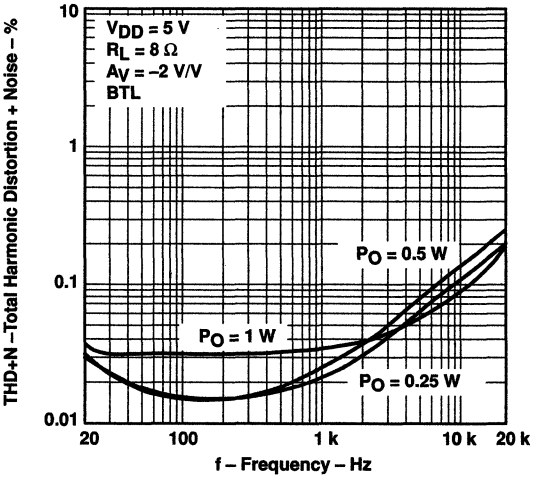


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

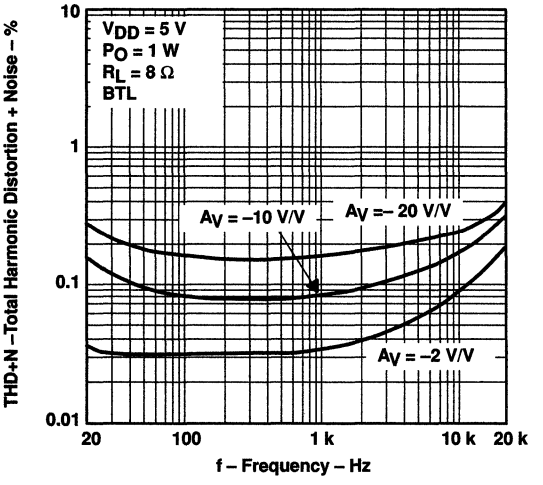


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

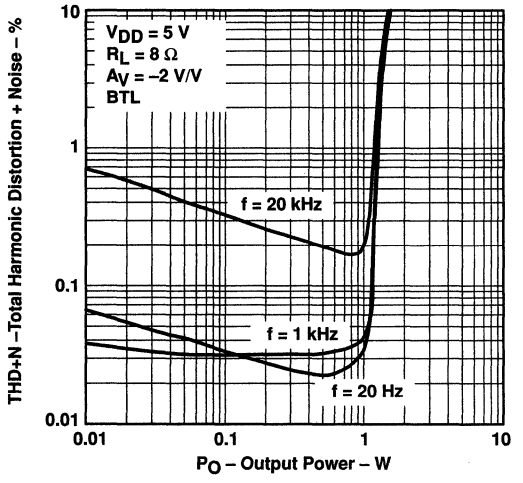


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

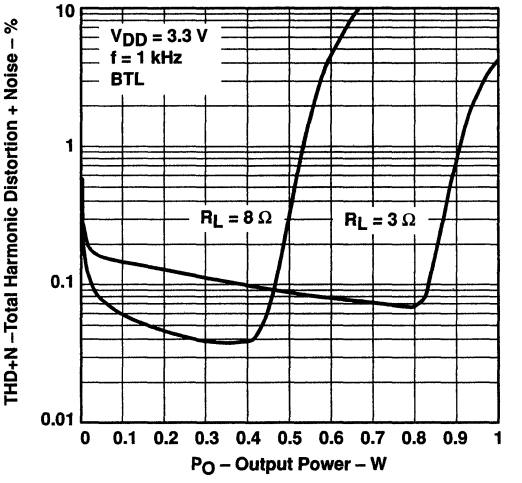


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

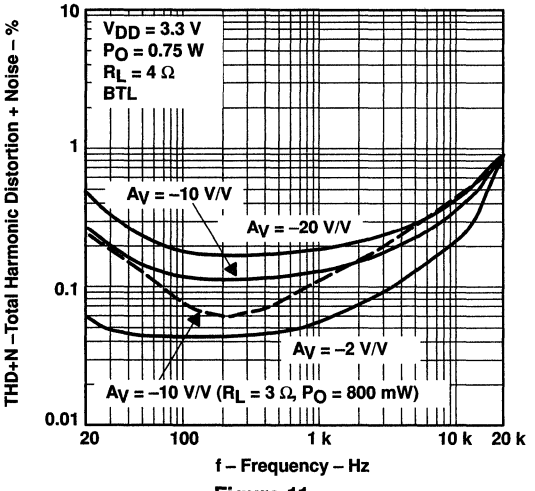


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

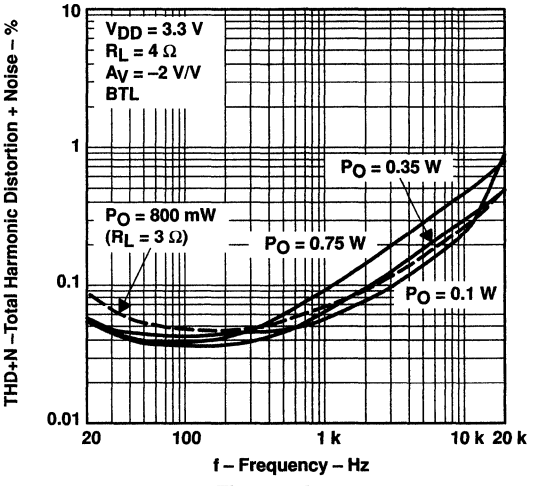


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

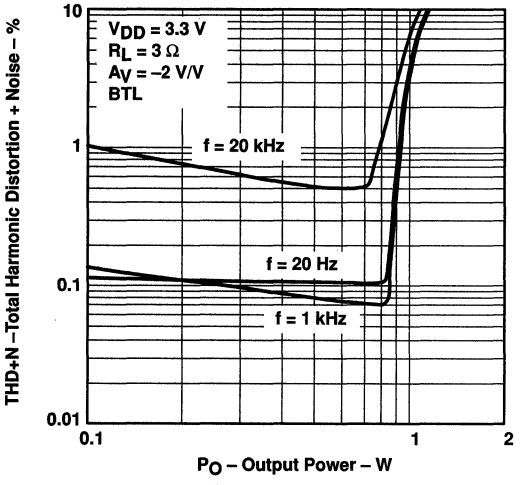


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

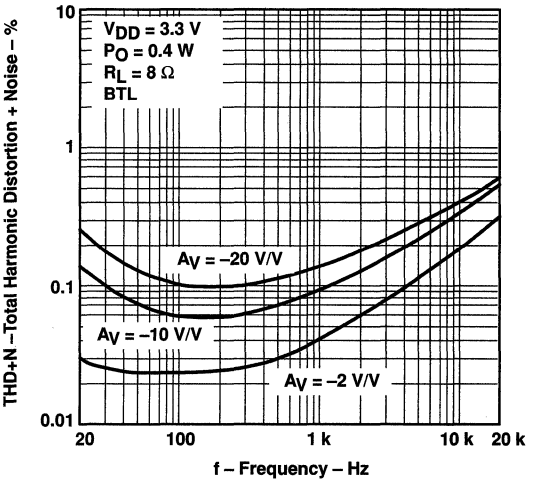


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

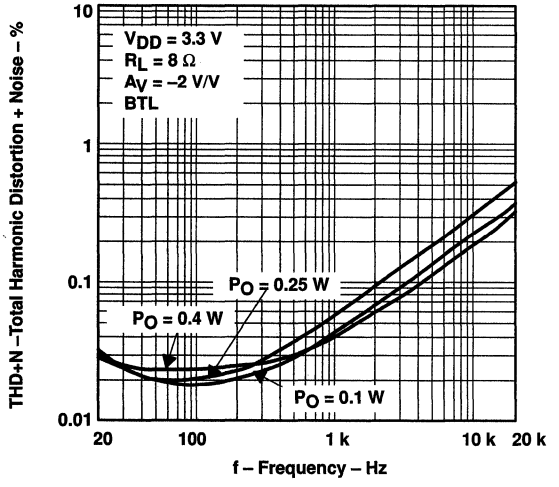


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

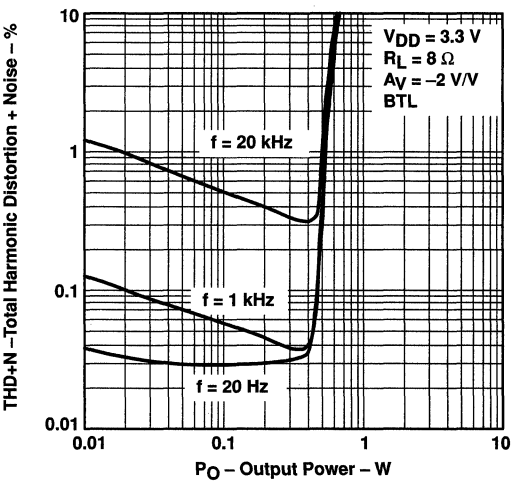


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

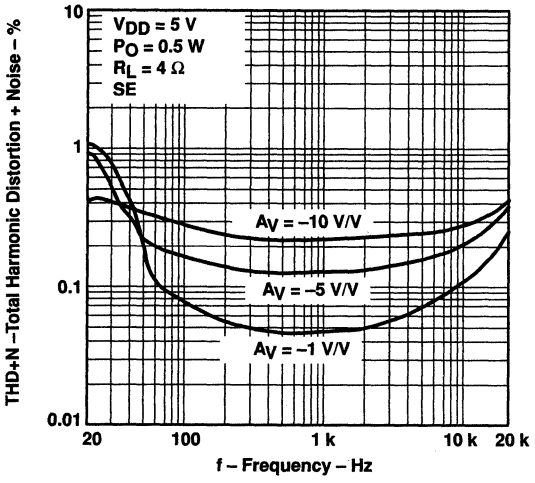


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

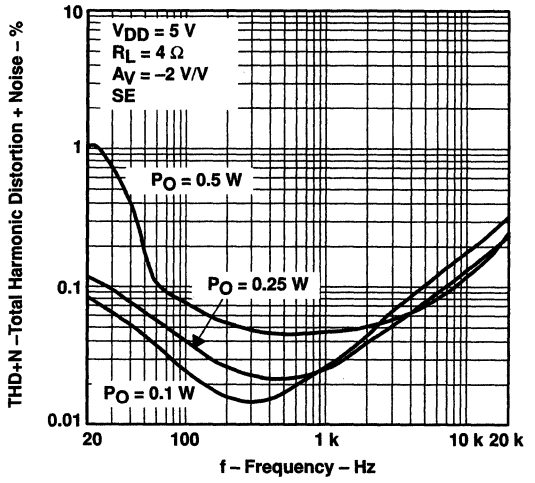


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

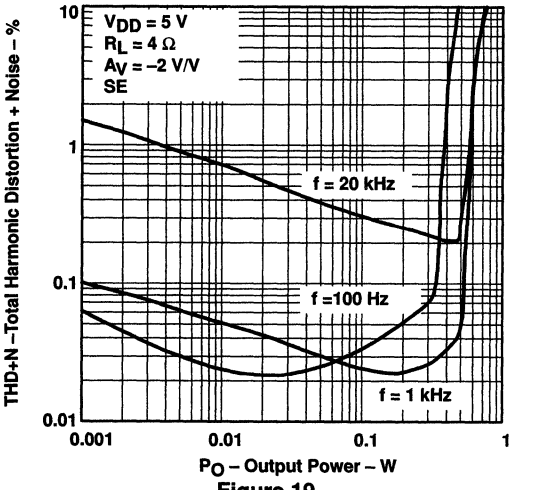


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

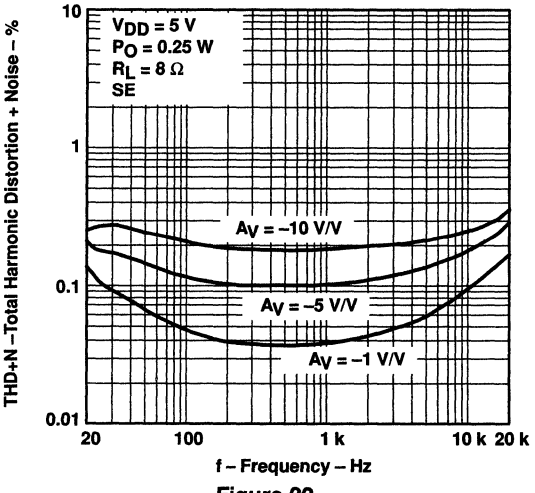


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

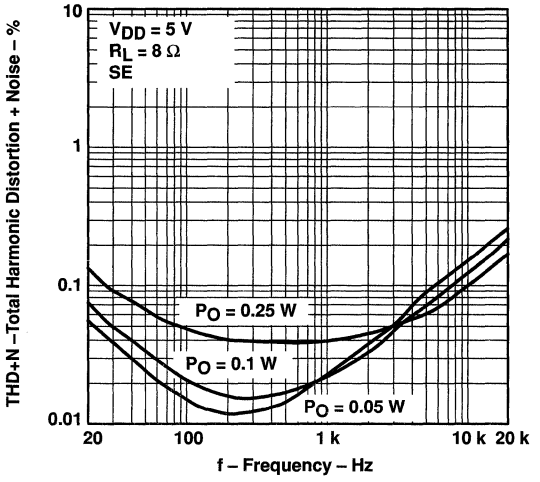


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

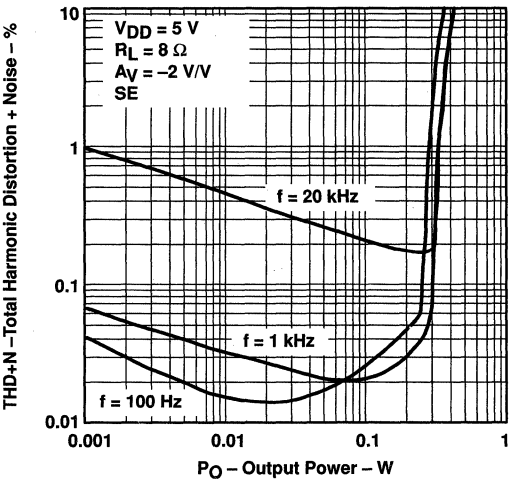


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

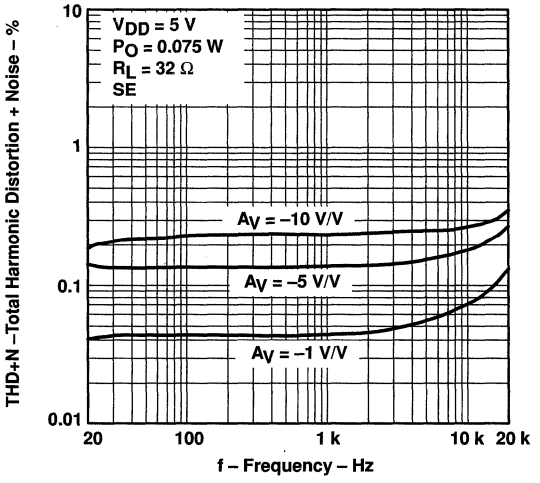


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

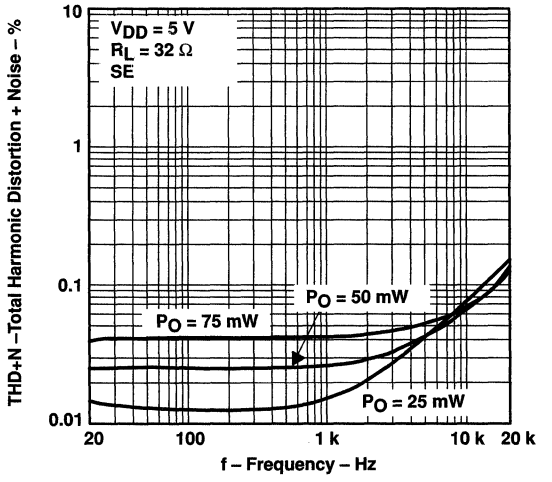


Figure 24

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

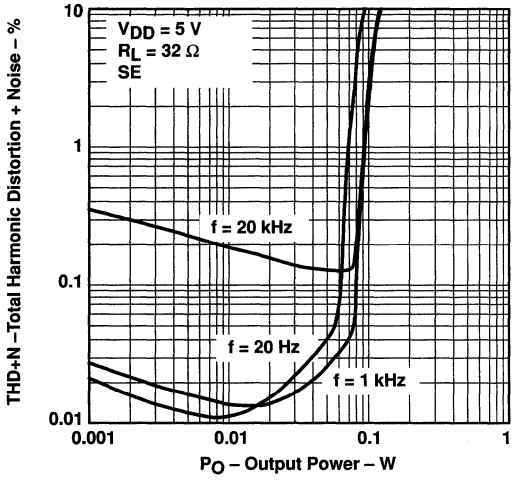


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

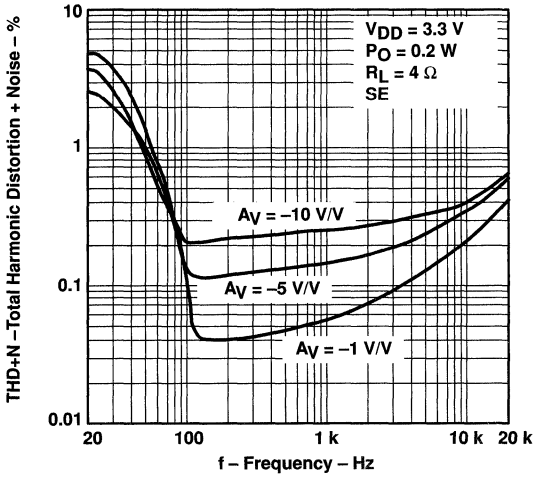


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

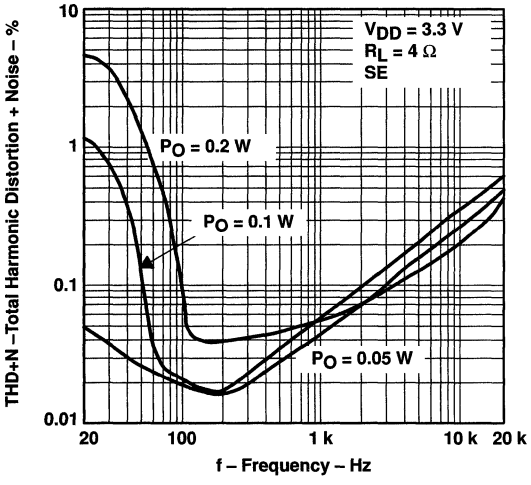


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

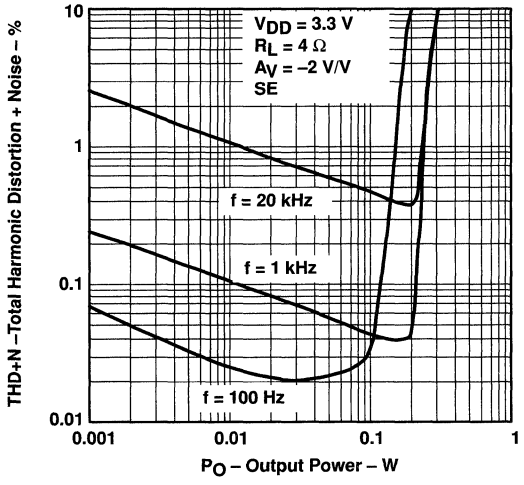


Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

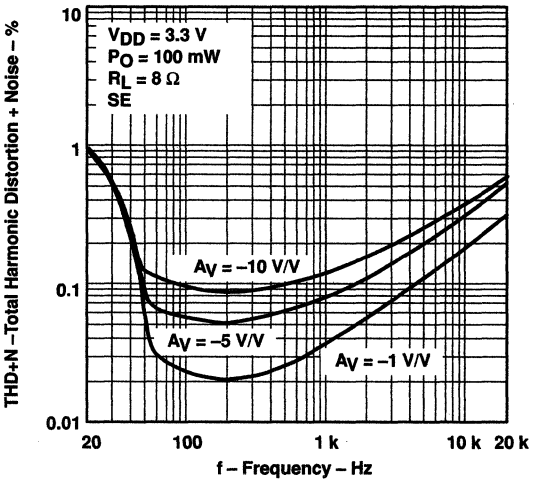


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

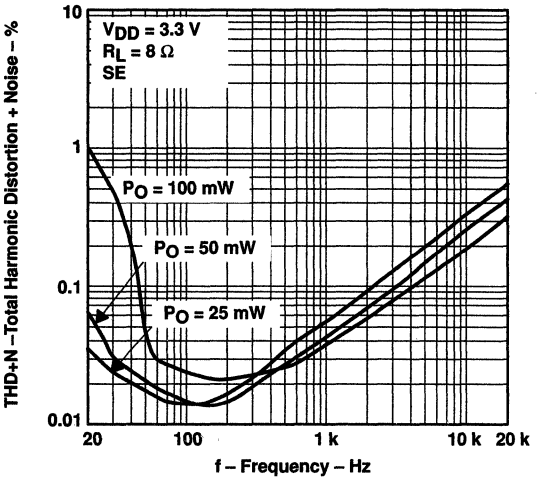


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

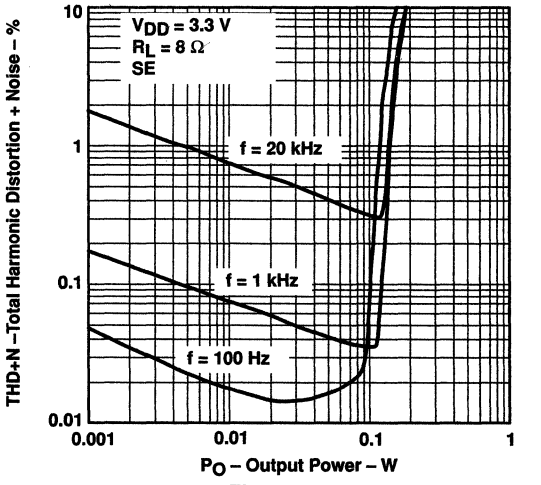


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

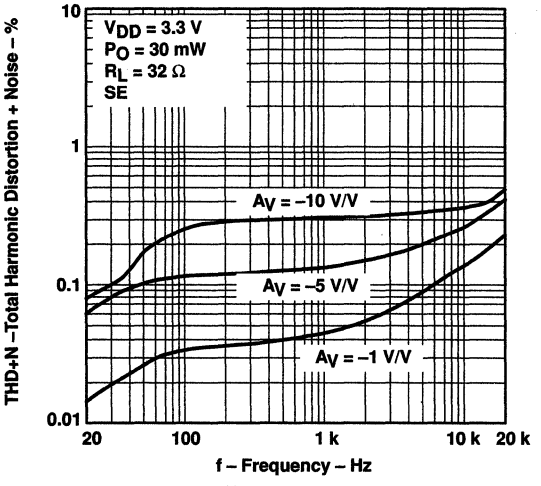


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

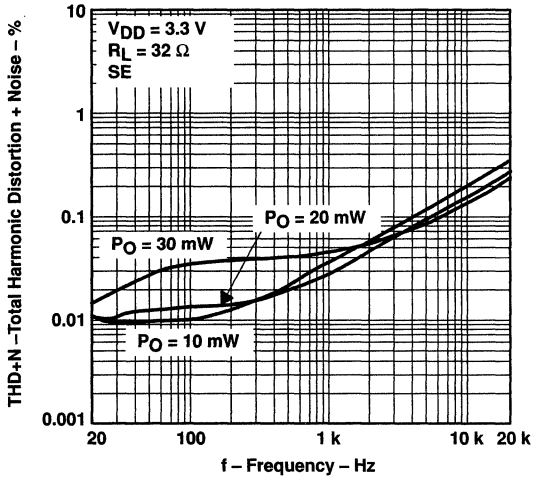


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

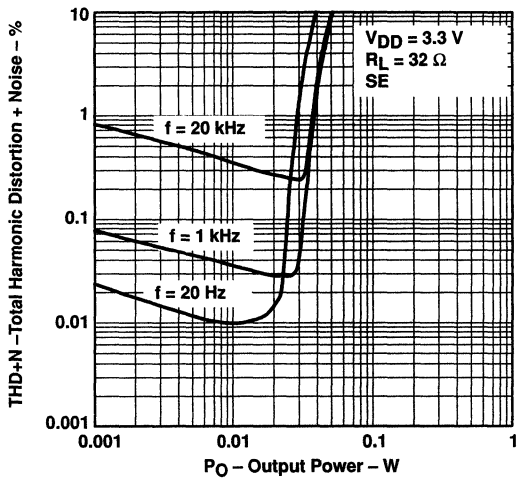


Figure 34

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

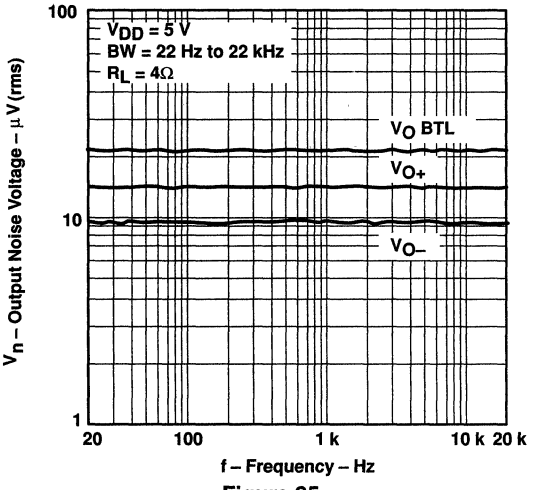


Figure 35

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

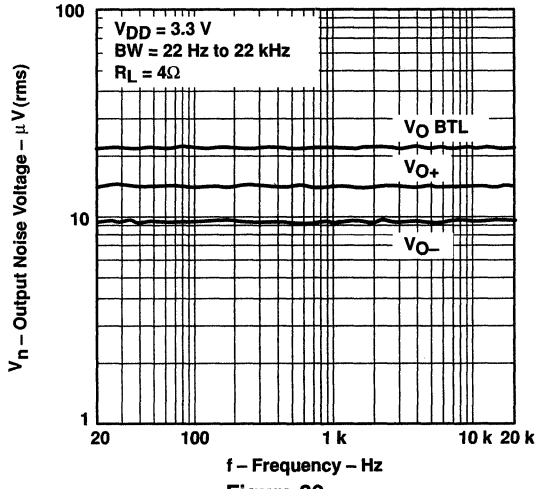


Figure 36

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

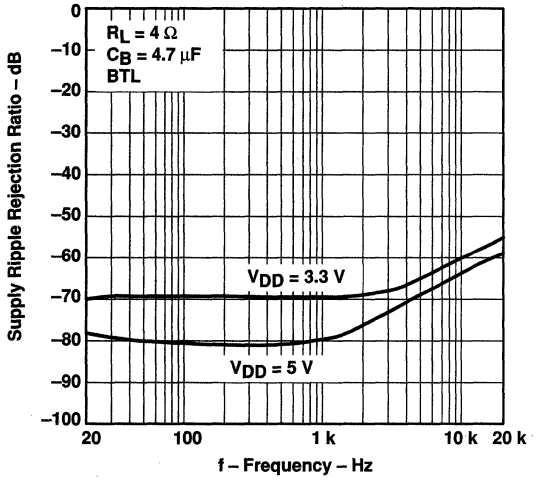


Figure 37

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

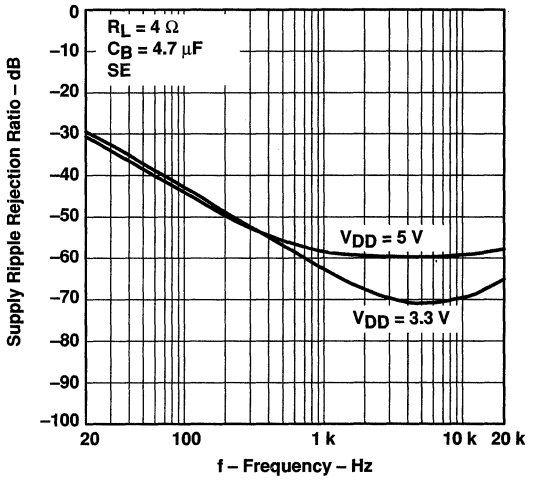


Figure 38

CROSSTALK
vs
FREQUENCY

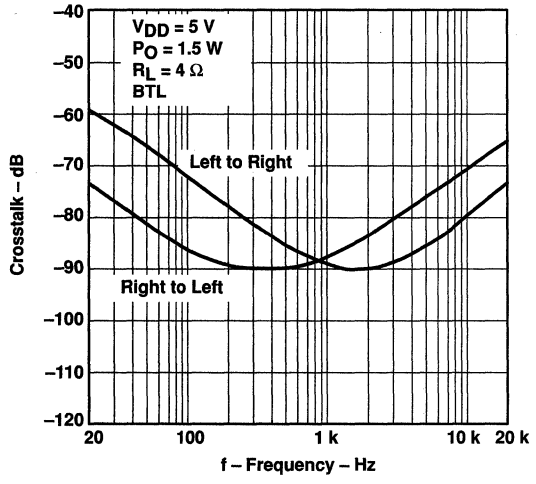


Figure 39

CROSSTALK
vs
FREQUENCY

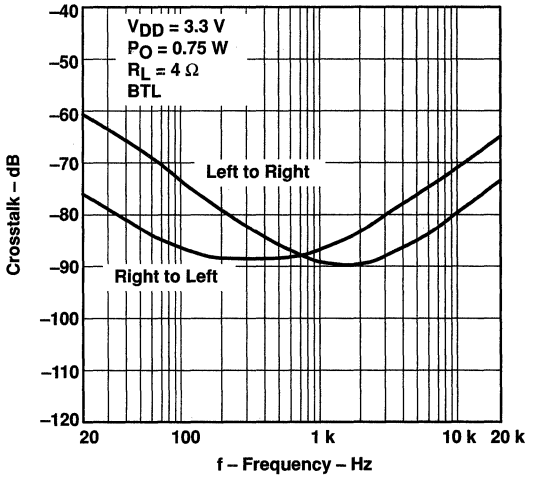


Figure 40

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

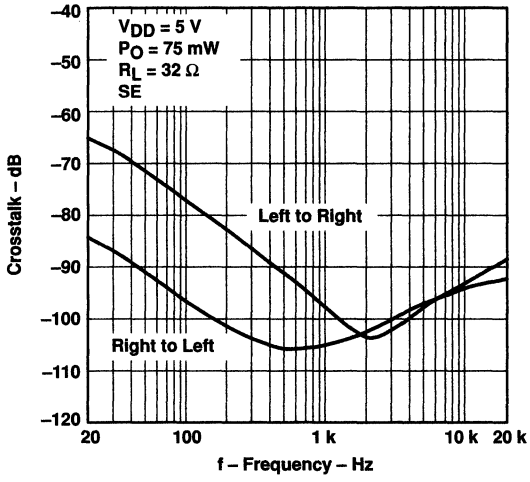


Figure 41

CROSSTALK vs FREQUENCY

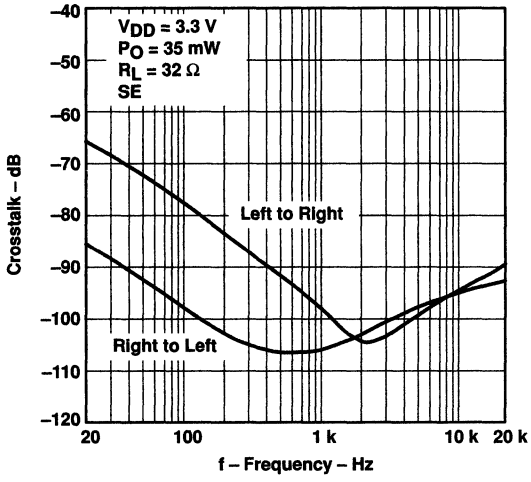


Figure 42

OPEN LOOP RESPONSE

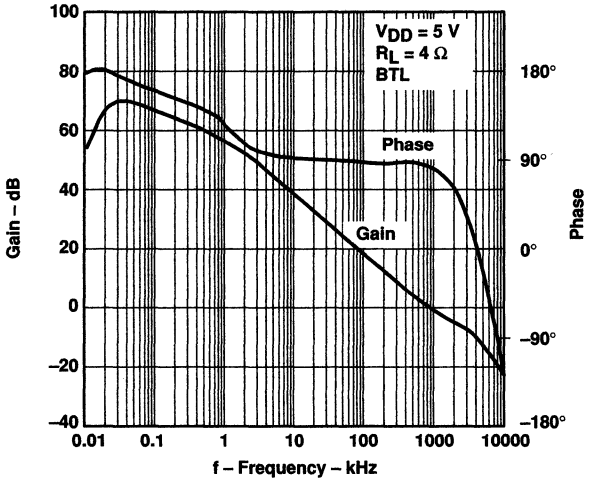


Figure 43

TYPICAL CHARACTERISTICS

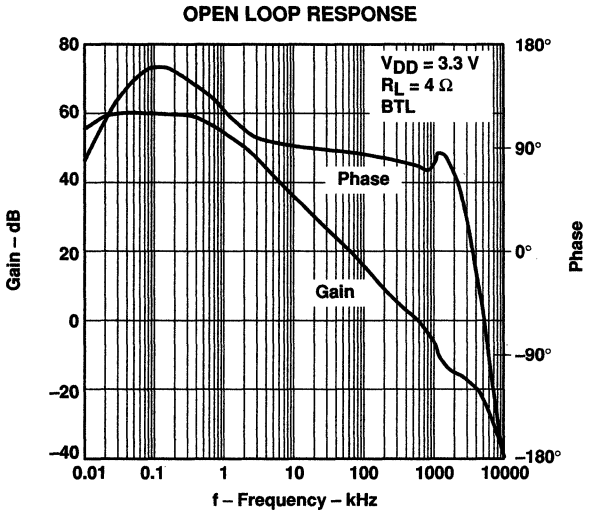


Figure 44

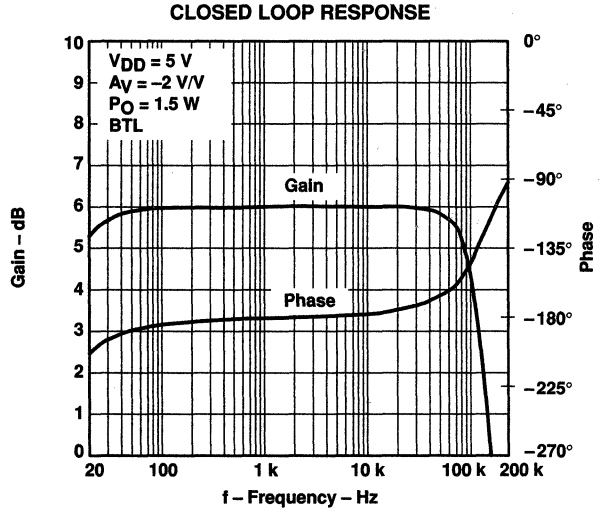


Figure 45

TYPICAL CHARACTERISTICS

CLOSED LOOP RESPONSE

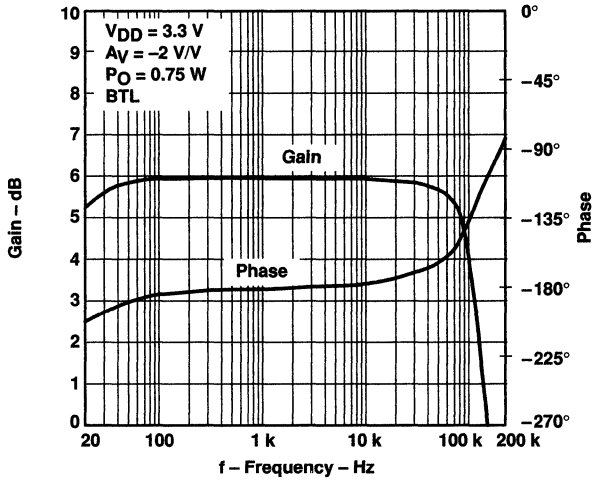


Figure 46

CLOSED LOOP RESPONSE

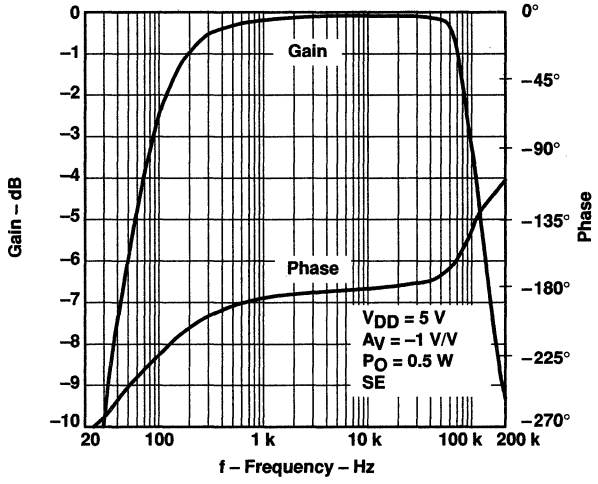


Figure 47

TYPICAL CHARACTERISTICS

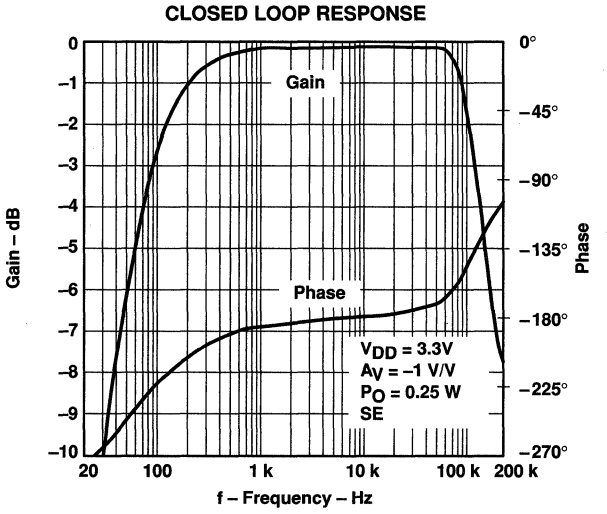


Figure 48

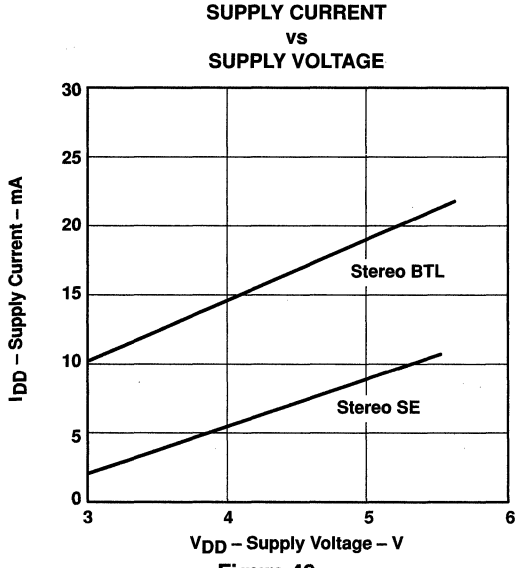


Figure 49

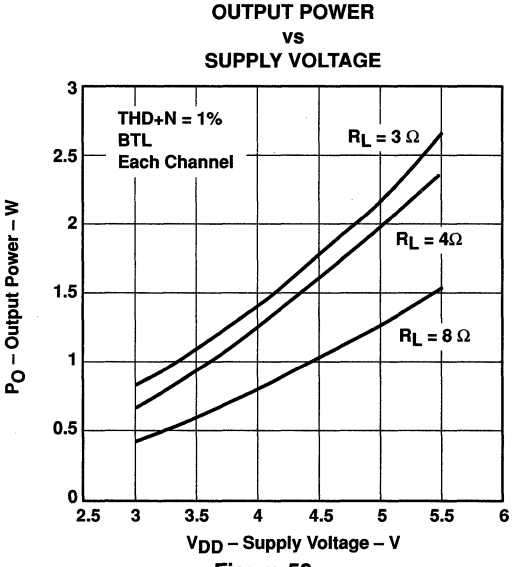


Figure 50

TYPICAL CHARACTERISTICS

OUTPUT POWER vs SUPPLY VOLTAGE

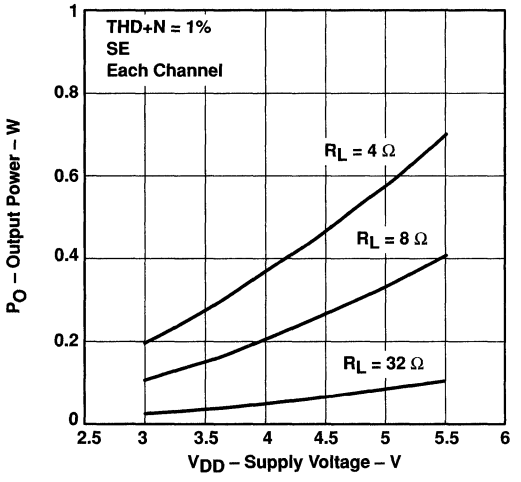


Figure 51

OUTPUT POWER vs LOAD RESISTANCE

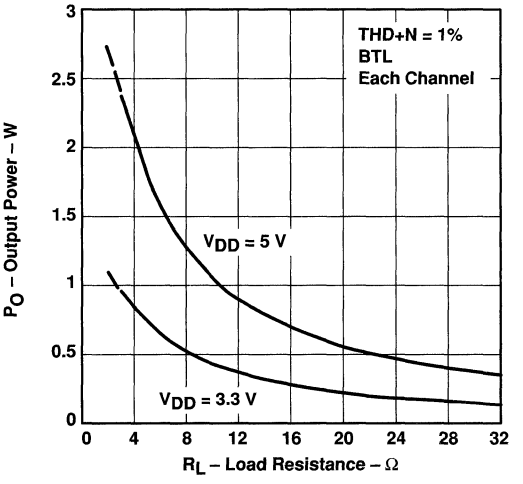


Figure 52

OUTPUT POWER vs LOAD RESISTANCE

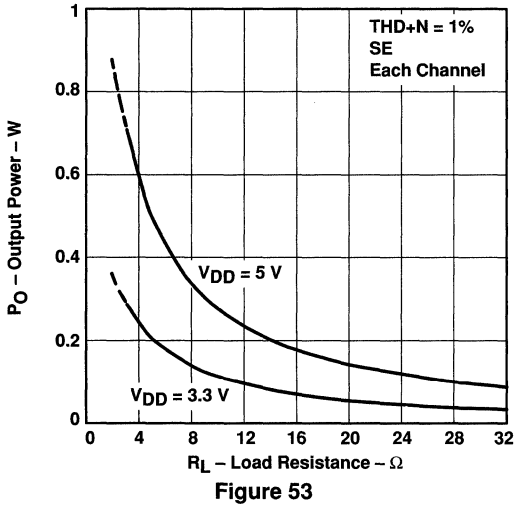


Figure 53

POWER DISSIPATION vs OUTPUT POWER

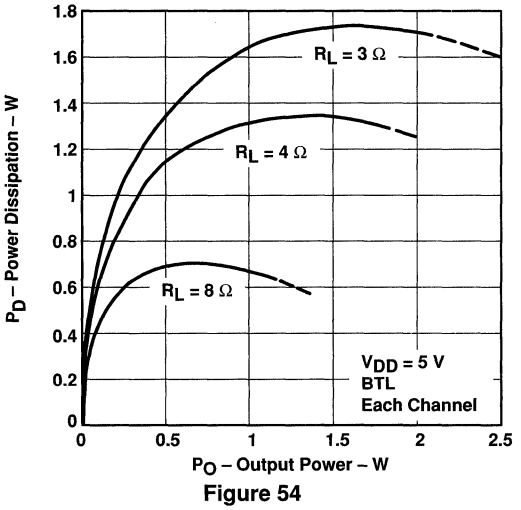


Figure 54

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs OUTPUT POWER

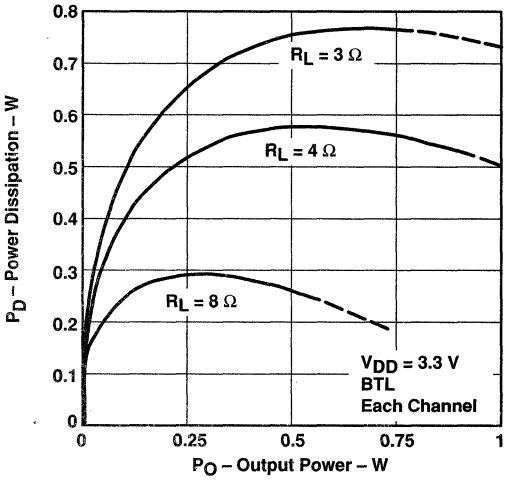


Figure 55

POWER DISSIPATION vs OUTPUT POWER

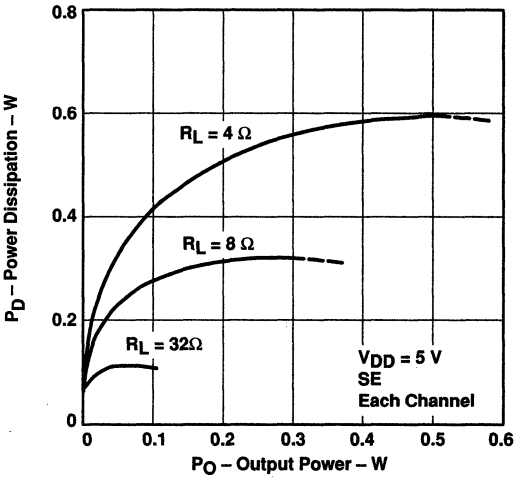


Figure 56

POWER DISSIPATION vs OUTPUT POWER

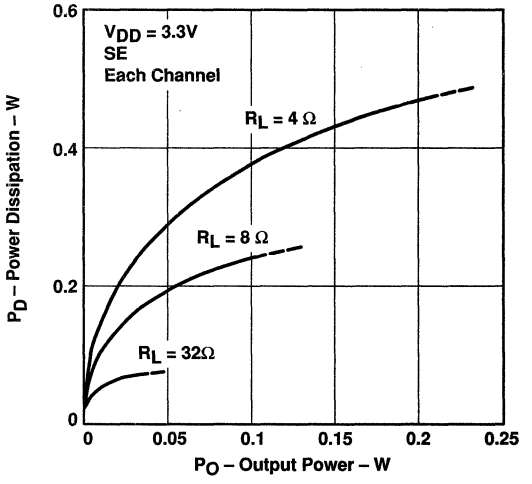


Figure 57

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface-mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

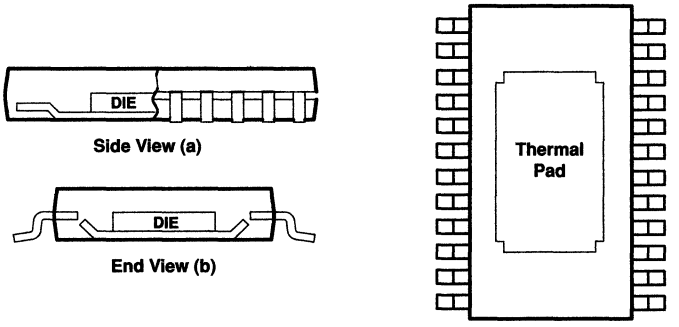


Figure 58. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0202 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \qquad (1)$$

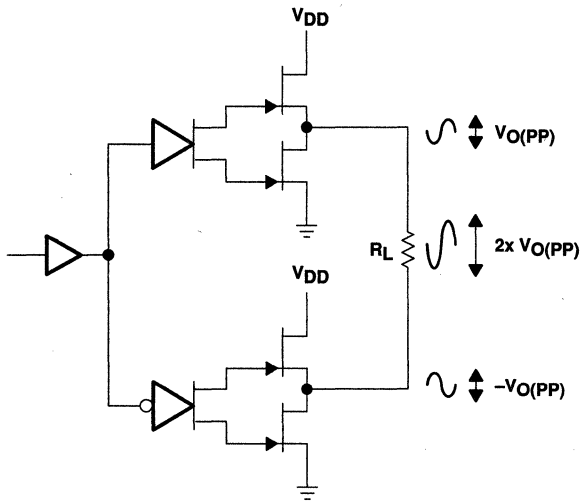


Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \qquad (2)$$

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

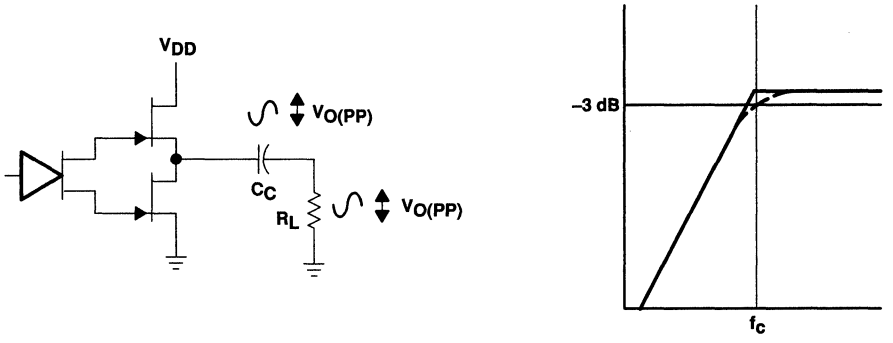


Figure 60. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).

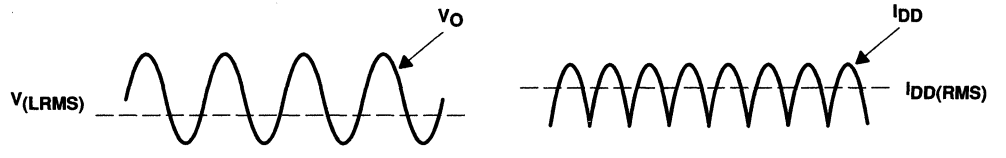


Figure 61. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD}\text{rms} = \frac{V_{DD}\, 2V_P}{\pi\, R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\, R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\, V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

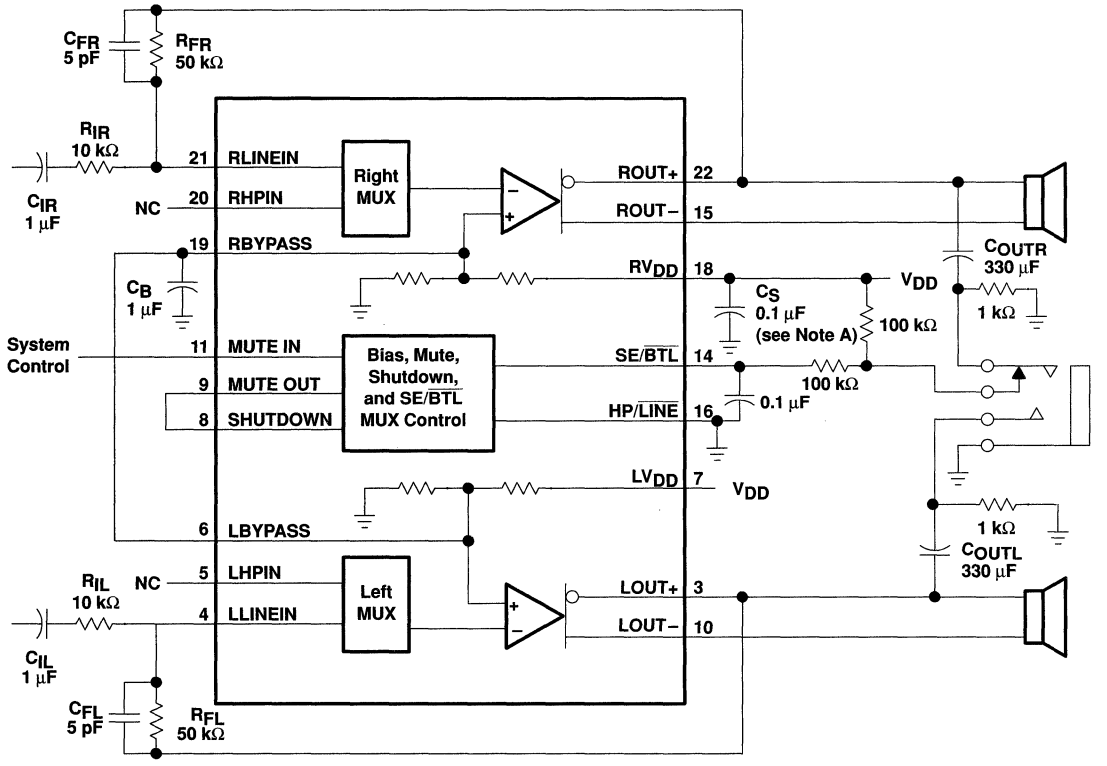
A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0202 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1, then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

selection of components

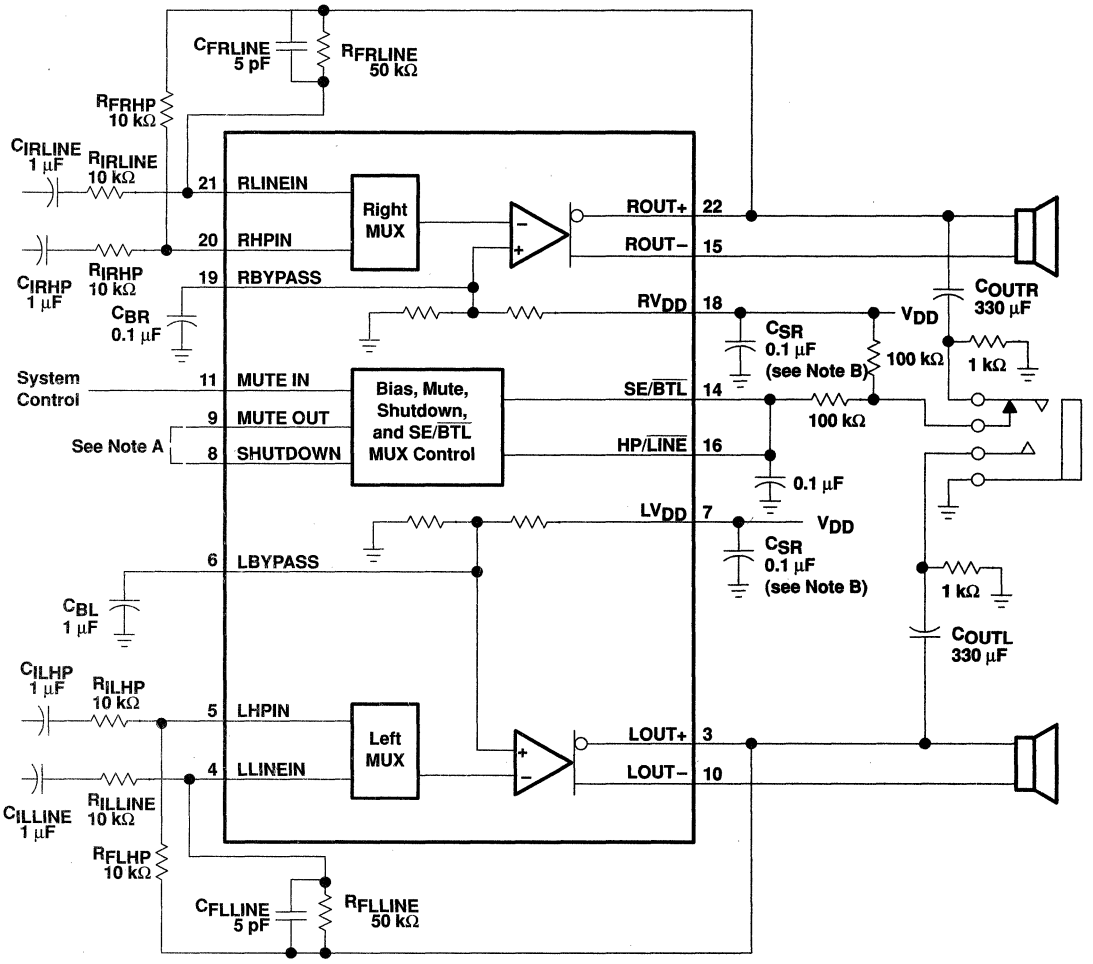
Figure 62 and Figure 63 are a schematic diagrams of a typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 62. TPA0202 Minimum Configuration Application Circuit

APPLICATION INFORMATION



NOTES: A. This connection is for ultra-low current in shutdown mode.
B. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 63. TPA0202 Full Configuration Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0202 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

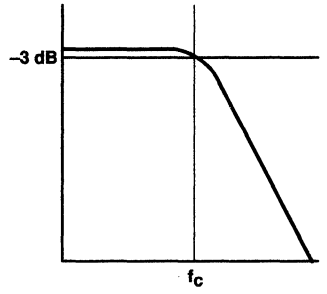
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0202 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{7}$$



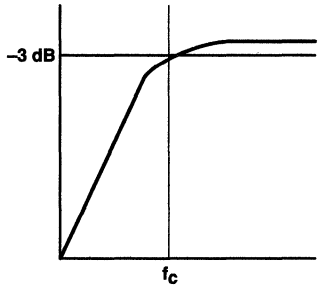
For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \quad (8)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0202 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. The capacitor is fed from a 100-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{(C_B \times 100\ k\Omega)} \leq \frac{1}{C_I(R_I + R_F)} \qquad (10)$$

As an example, consider a circuit where C_B is 1 µF, C_I is 0.22 µF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the equation 10 we get $10 \leq 75$, which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

In Figure 63, the full feature configuration, two bypass capacitors are used. This provides the maximum separation between right and left drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used as shown in Figure 62. It is critical that terminals 6 and 19 be tied together in this configuration.

load considerations

Extremely low impedance loads (below 4 Ω) coupled with certain external component selections, board layouts, and cabling can cause oscillations in the system. Using a single air-cored inductor in series with the load eliminates any spurious oscillations that might occur. An inductance of approximately 1 µH has been shown to eliminate such oscillations. There are no special considerations when using 4 Ω and above loads with this amplifier.

optimizing depop operation

Circuitry has been included in the TPA0202 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. If high impedances are used for the feedback and input resistors, it is possible for the input capacitor to drift downwards from mid-rail during mute and shutdown. A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations, and to limit the size of the gain-setting resistors. The time constant of the input coupling capacitor (C_I) and the gain-setting resistors (R_I and R_F) needs to be shorter than the time constant formed by the bypass capacitor (C_B) and the output impedance of the mid-rail generator, which is nominally 100 kΩ (see equation 10).

The effective output impedance of the mid-rail generator is actually greater than 100 kΩ due to a PNP transistor clamping the input node (see Figure 64).

APPLICATION INFORMATION

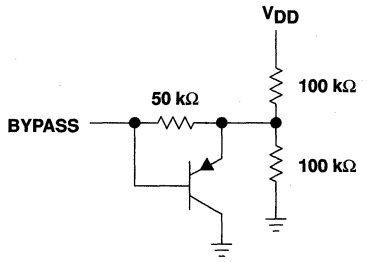


Figure 64. PNP Transistor Clamping of BYPASS Terminal

The PNP transistor limits the voltage drop across the 50 kΩ resistor by slewing the internal node slowly when power is applied. At start-up, the xBYPASS capacitor is at 0. The PNP is pulling the mid-point of the bias circuit down, so the capacitor sees a lower effective voltage, and thus charges slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

If the expression in equation 10 cannot be fulfilled or the small amount of pop is still unacceptable for the application, then external circuitry must be added that can eliminate the pop heard during power up and while transitioning out of mute or shutdown modes.

By holding the device in SE mode when the pop normally occurs, no pop can be heard through the BTL-connected speakers (as the negative output is in a high impedance state when the amplifier is in SE mode).

From a hardware point of view, the easiest way to implement this is to drive the SE/BTL terminal from the general-purpose input-output (GPIO) in the system. If the SE/BTL terminal is normally connected to a headphone socket (as shown in Figure 65), then the GPIO signal must either be taken through an OR gate (see Figure 65) or isolated with a diode (any signal diode) (see Figure 66).

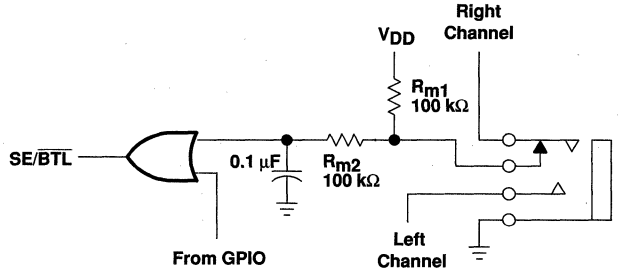


Figure 65. Implementation with an OR Gate

APPLICATION INFORMATION

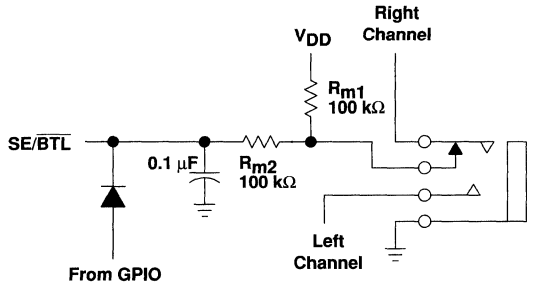


Figure 66. Implementation with a Diode

The OR gate and diode isolate the GPIO terminal from the headphone switch. In these implementations, the headphone switch has priority.

When the amplifier is in mute mode, the output stage continues to be biased. This causes the transition out of mute mode to be very fast with only a short delay (from 100 ms to 500 ms). During power up or the transition out of shutdown mode, a longer delay (from 1 s to 2 s) is required. The exact delay time required is dependent on the values of the external components used with the amplifier (see Figure 67).

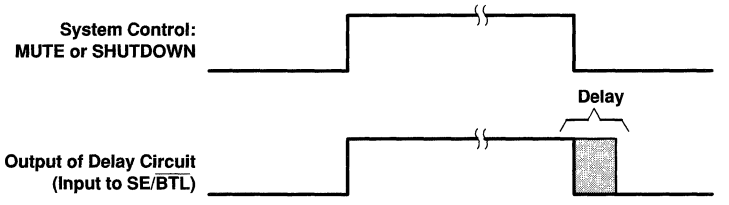


Figure 67. Transition Delay Timing

single-ended operation

In SE mode (see Figure 59 and Figure 60), the load is driven from the primary amplifier output for each channel (OUT+, terminals 22 and 3).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship (see equation 12):

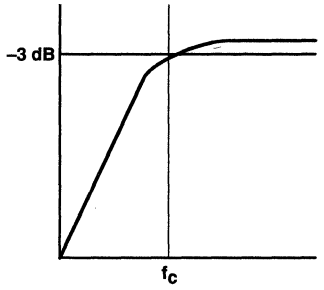
$$\frac{1}{(C_B \times 25\ k\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \tag{12}$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 14.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (14)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0202 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0202, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 14) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 10 and 15). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0202 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0202 as an SE driver from LOUT+ and ROUT+ (terminals 3 and 22). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 68.

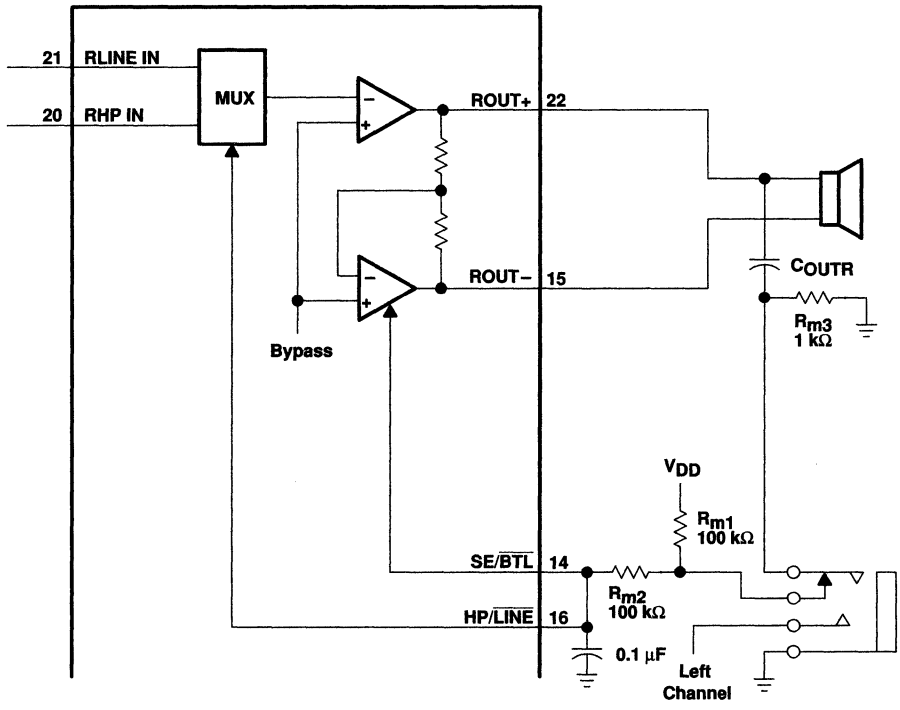


Figure 68. TPA0202 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

As shown in the full feature application (Figure 63), the input MUX control can be tied to the SE/$\overline{\text{BTL}}$ input. The benefits of doing this are described in the following input MUX operation section.

APPLICATION INFORMATION

Input MUX operation

Working in concert with the SE/$\overline{\text{BTL}}$ feature, the HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 69). The primary function of the MUX is to allow different gain settings for BTL versus SE mode. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{SE Gain}_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \quad (15)$$

If, for example $R_{I(HP)}$ = 10 kΩ and $R_{F(HP)}$ = 10 kΩ then SE $\text{Gain}_{(HP)}$ = –1

$$\text{BTL Gain}_{(LINE)} = -2\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \quad (16)$$

If, for example $R_{I(LINE)}$ = 10 kΩ and $R_{F(LINE)}$ = 50 kΩ then BTL $\text{Gain}_{(LINE)}$ = –10

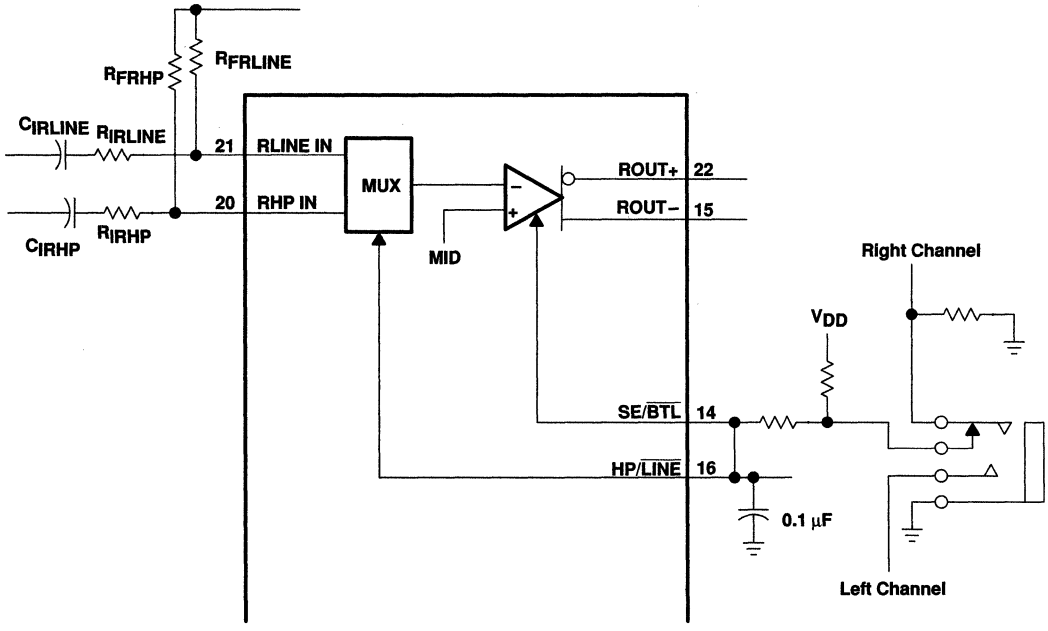


Figure 69. TPA0202 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

APPLICATION INFORMATION

mute and shutdown modes

The TPA0202 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 5 μA. SHUTDOWN or MUTE IN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces I_{DD} to 1.5 mA.

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0202 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0202 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications to improve the efficiency.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0202 data sheet, one can see that when the TPA0202 is operating from a 5-V supply into a 3-Ω speaker that 2 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right) \quad (17)$$

$$= 10\text{Log}\left(\frac{2}{1}\right)$$

$$= 3.0 \text{ dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

3.0 dB – 15 dB = – 12 dB (15 dB headroom)
3.0 dB – 12 dB = – 9 dB (12 dB headroom)
3.0 dB – 9 dB = – 6 dB (9 dB headroom)
3.0 dB – 6 dB = – 3 dB (6 dB headroom)
3.0 dB – 3 dB = 0 dB (3 dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (18)$$

$$= 63 \text{ mW (15 dB headroom)}$$

$$= 120 \text{ mW (12 dB headroom)}$$

$$= 250 \text{ mW (9 dB headroom)}$$

$$= 500 \text{ mW (6 dB headroom)}$$

$$= 1000 \text{ mW (3 dB headroom)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0202 and maximum ambient temperatures is shown in Table 4.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

Table 4. TPA0202 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2	2 W	1.7	–3°C
2	1000 mW (3 dB)	1.6	6°C
2	500 mW (6 dB)	1.4	24°C
2	250 mW (9 dB)	1.1	51°C
2	120 mW (12 dB)	0.8	78°C
2	63 mW (15 dB)	0.6	96°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP‡	2.8 W	22.1 mW/°C	1.8 W	1.4 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 22 mW/°C and 54 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

For 0 CFM :

$$= \frac{1}{0.022}$$

$$= 45°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0202 is 150 °C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (20)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB headroom, 0 CFM)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB headroom per channel.

Table 4 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0202 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

junction temperature measurement

Characterizing a PCB layout with respect to thermal impedance is very difficult, as it is usually impossible to know the junction temperature of the IC in question. The TPA0202 terminal 2 (TJ) sources a current proportional to the junction temperature. The circuit internal to TJ is shown in Figure 70.

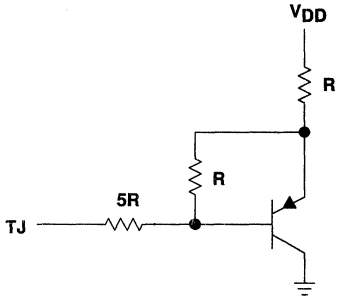
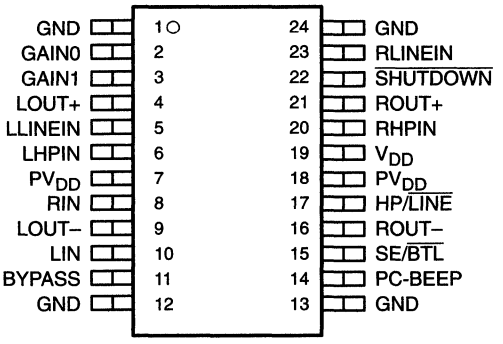


Figure 70. TJ Terminal Internal Circuit

Connect an ammeter between TJ and ground to measure the current. As the resistors have a tolerance of ±20%, this measurement must be calibrated on each device. The intent of this function is in characterization of the PCB and end equipment and not a real-time measurement of temperature. Typically a 25°C reading is –120 μA for a 3.3-V supply and –135 μA for a 5-V supply. The slope is approximately 0.25 μA/°C for both V_{DD} = 3.3 V and V_{DD} = 5 V. To reduce quiescent current, do not ground TJ in normal operation. It can be connected to V_{DD} or left floating as it has a resistor connected across the base-emitter junction.

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2-W/Ch Output Power Into 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0212 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0212 has less than 0.8% THD+N across its specified frequency range.

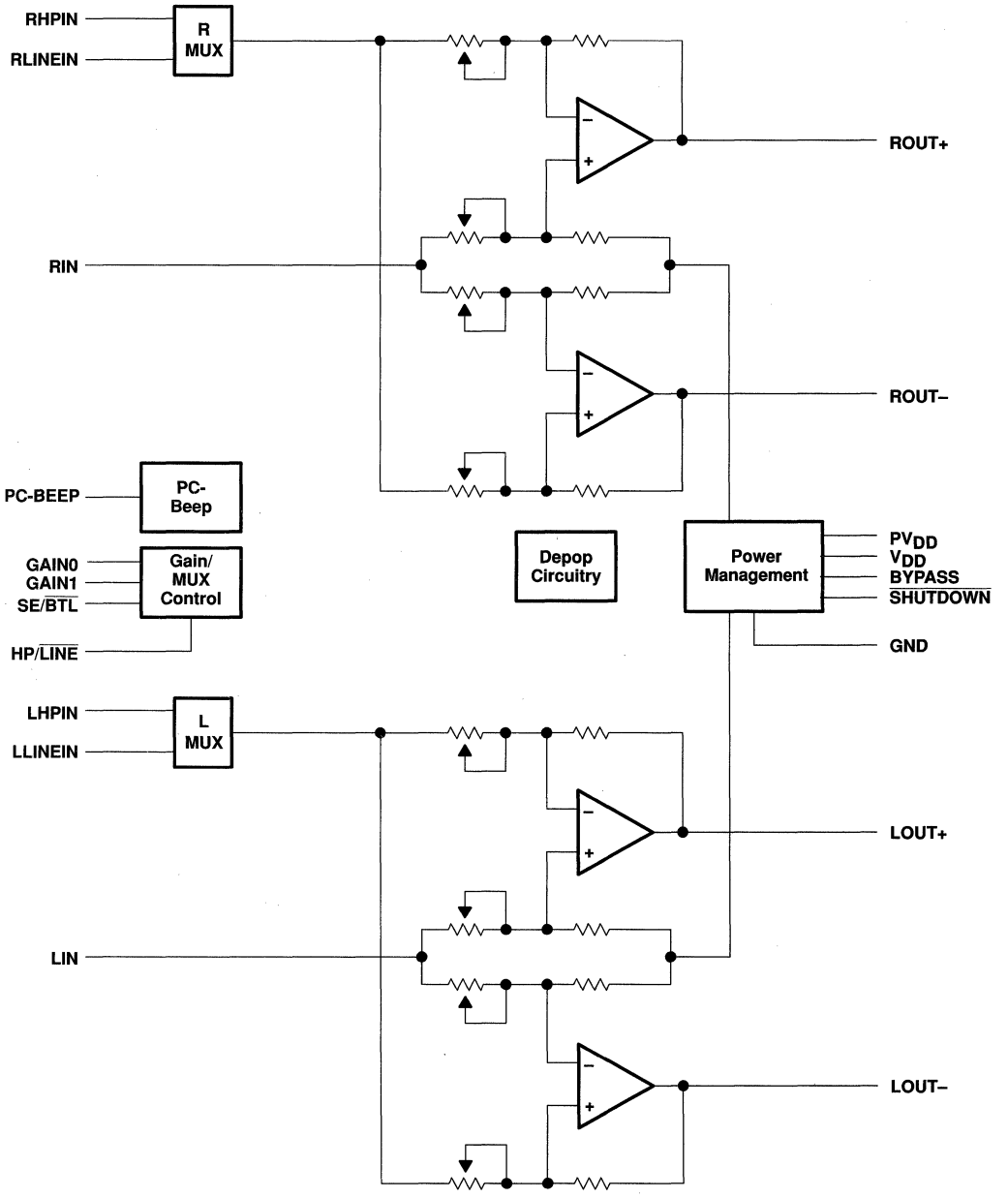
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of 2, 6, 12, and 24 V/V are provided, while SE gain is always configured as 1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0212 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this reduces the gain to 1 V/V.

The TPA0212 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0212 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0212PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0212PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
HP/$\overline{\text{LINE}}$	17	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$, HP/$\overline{LINE}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$, HP/$\overline{LINE}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = –2 V/V			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4 V to 5 V		77		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		6	8	mA
		SE mode		3	4	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω	f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.75%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		16		µV RMS
			SE mode		30		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–7, 10–13, 16–19, 21
		vs Frequency	2, 3, 8, 9, 14, 15, 20, 22
		vs Output voltage	23
V_n	Output noise voltage	vs Bandwidth	24
	Supply ripple rejection ratio	vs Frequency	25, 26
	Crosstalk	vs Frequency	27–29
	Shutdown attenuation	vs Frequency	30
SNR	Signal-to-noise ratio	vs Frequency	31
	Closed loop respone		32–35
P_O	Output power	vs Load resistance	36, 37
P_D	Power dissipation	vs Output power	38, 39
		vs Ambient temperature	40

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

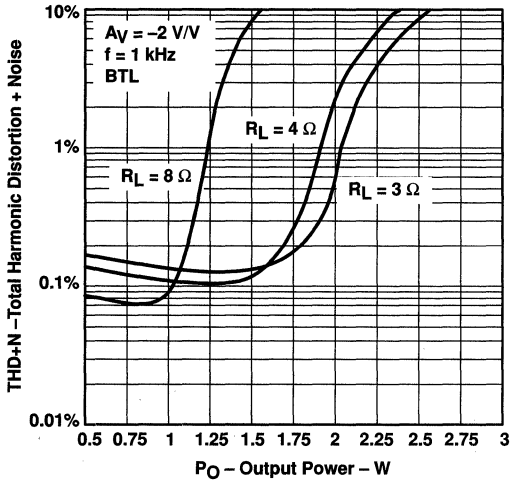


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

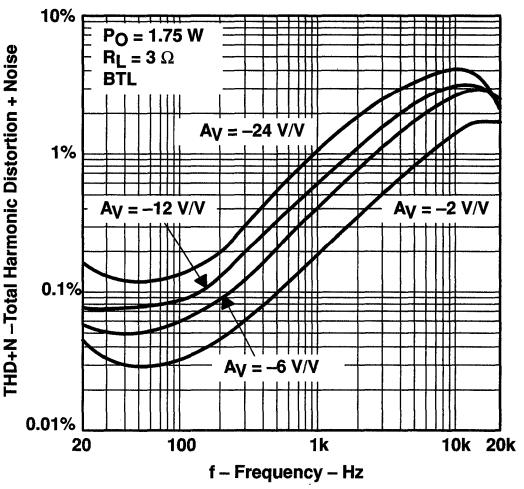


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

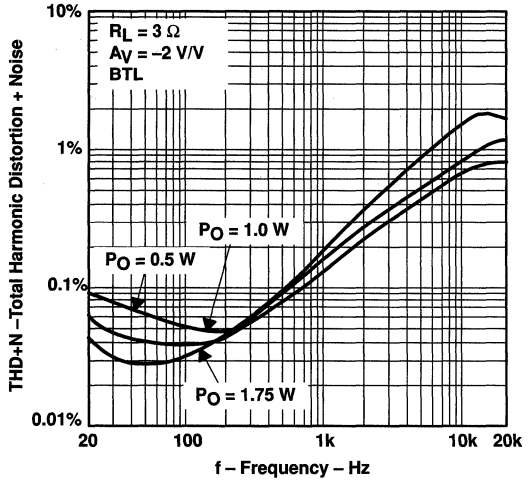


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

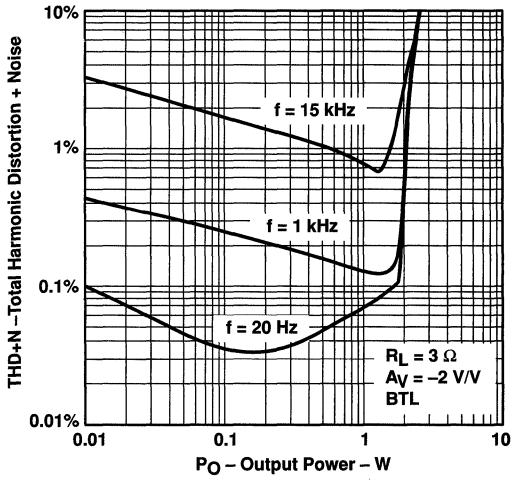


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

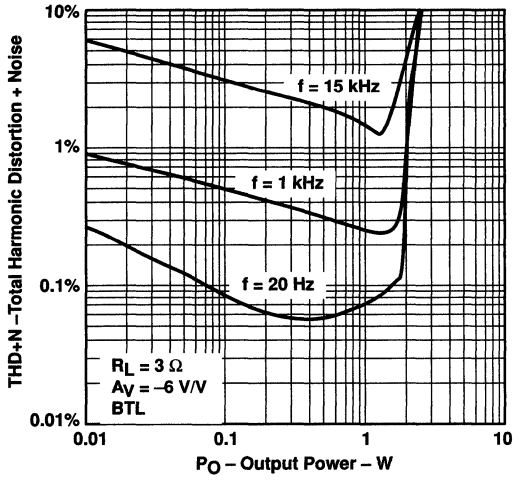


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

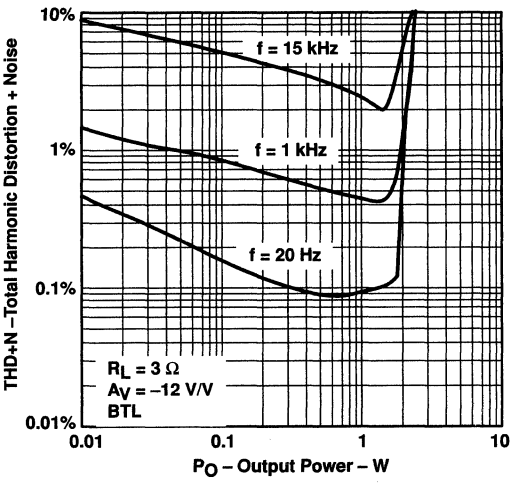


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

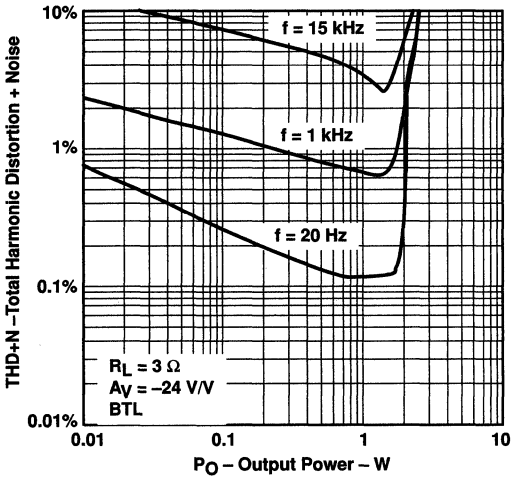


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

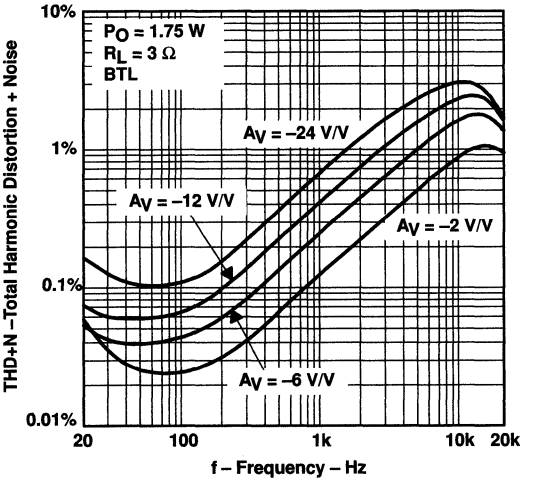


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

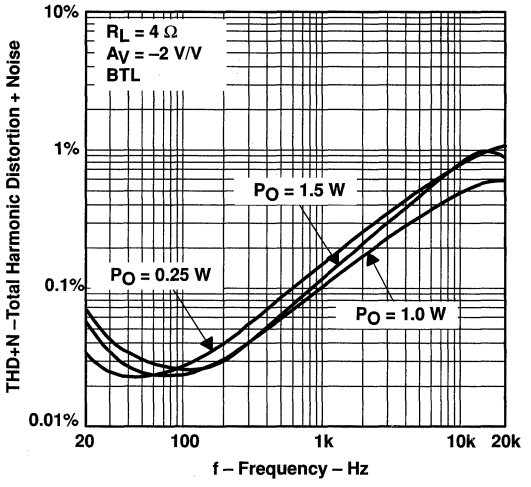


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

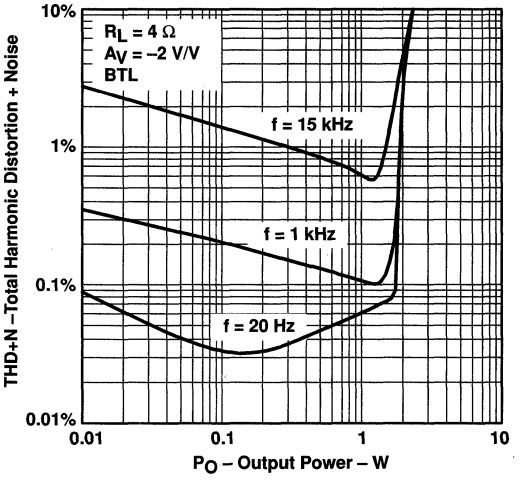


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

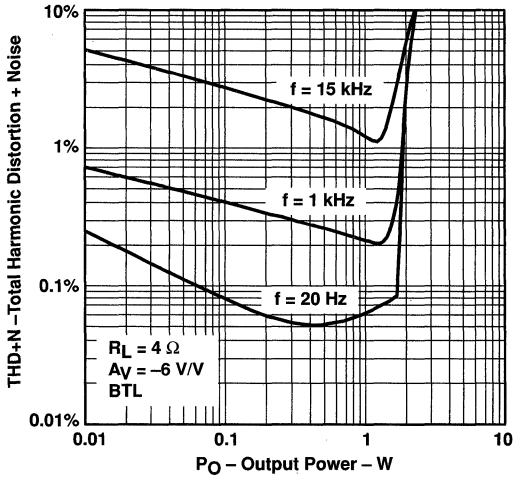


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

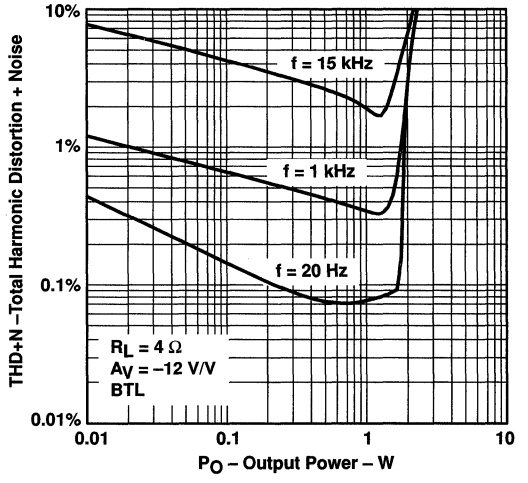


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

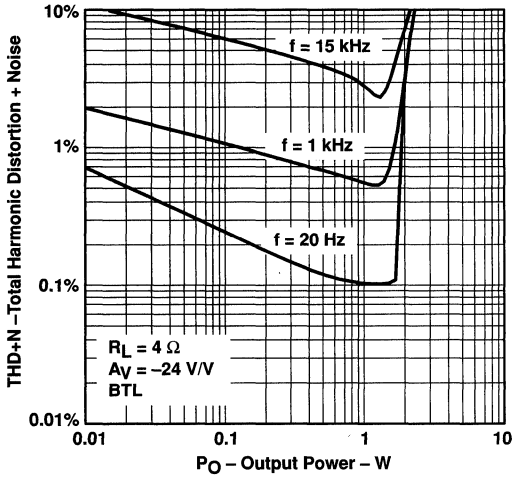


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

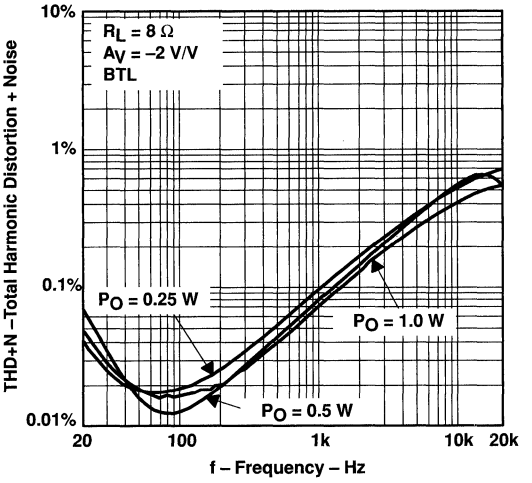


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

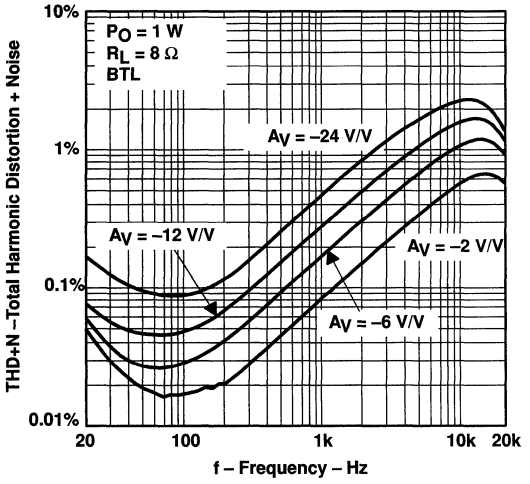


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

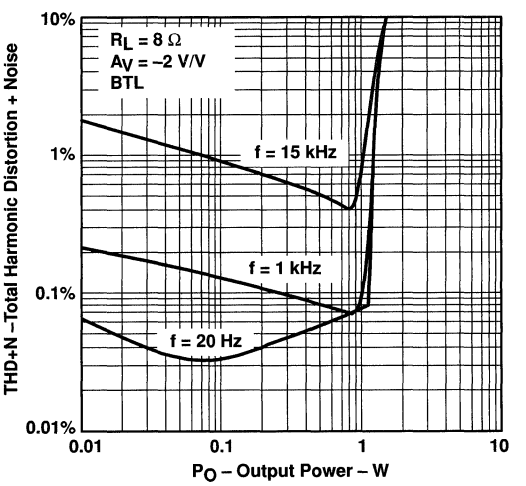


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

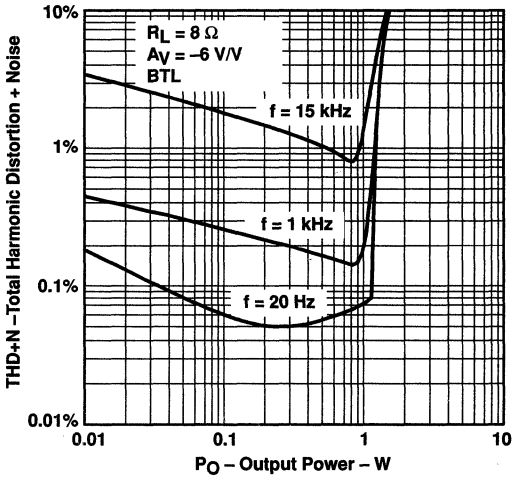


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

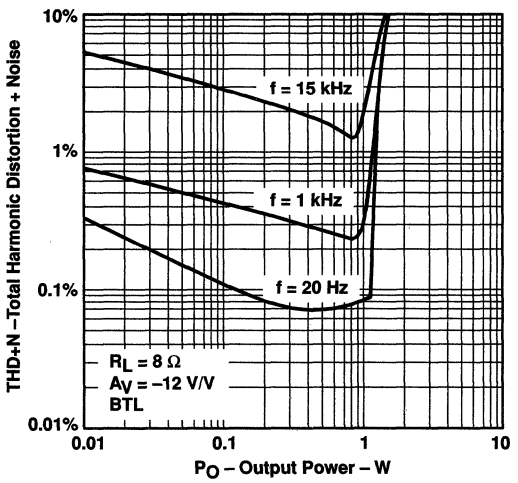


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

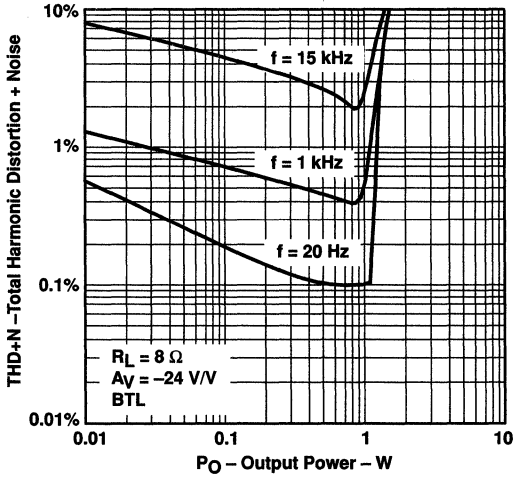


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

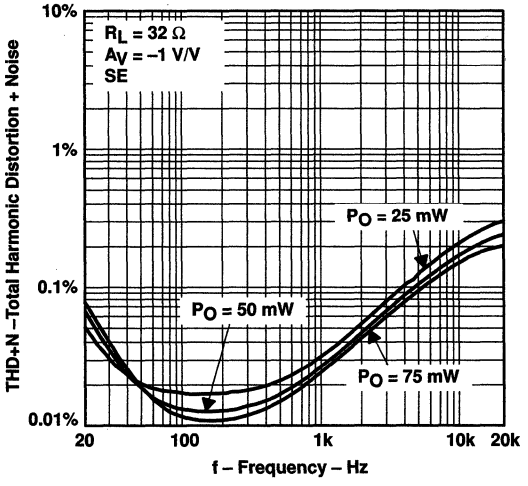


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

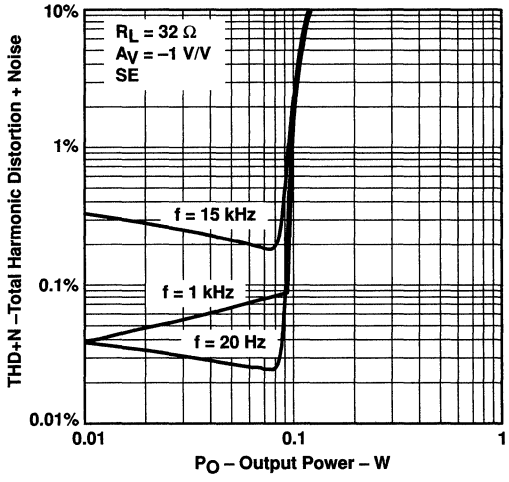


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

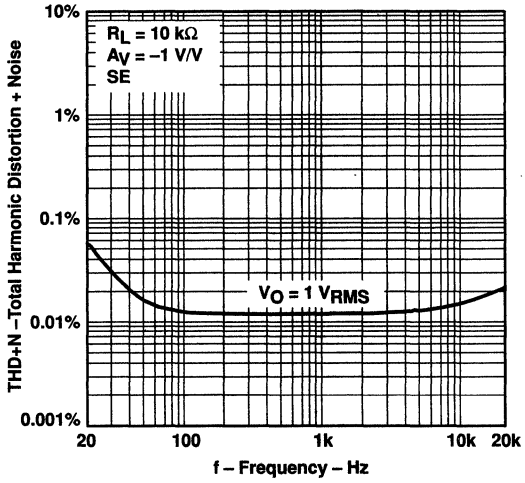


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

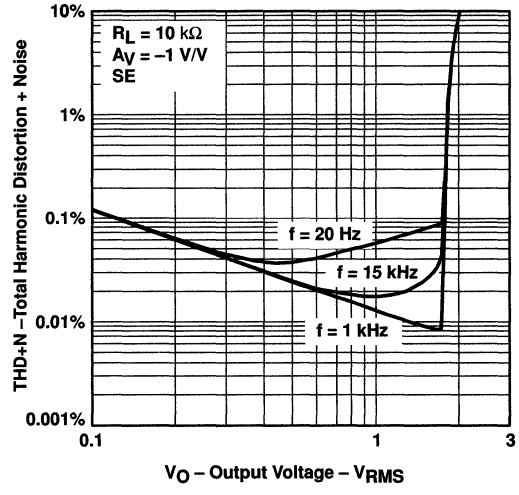


Figure 23

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

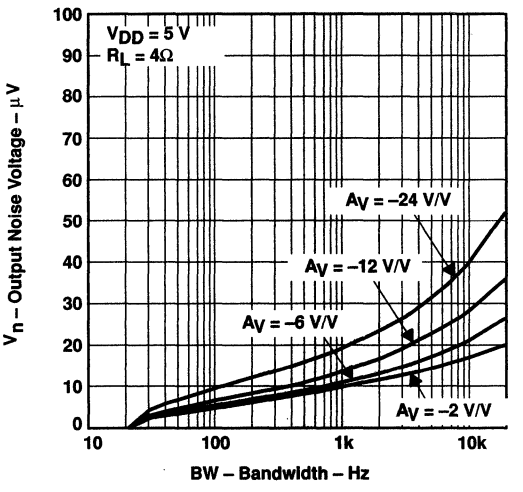


Figure 24

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

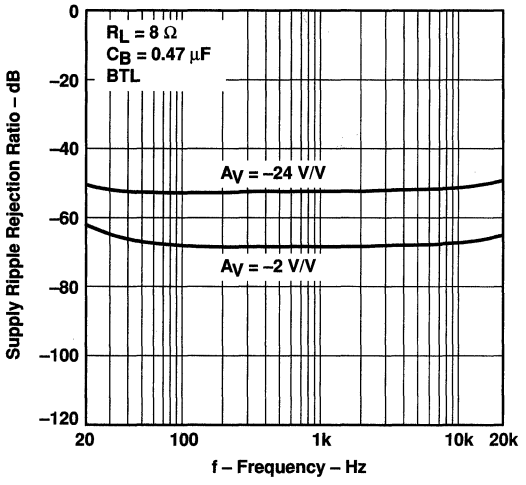


Figure 25

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

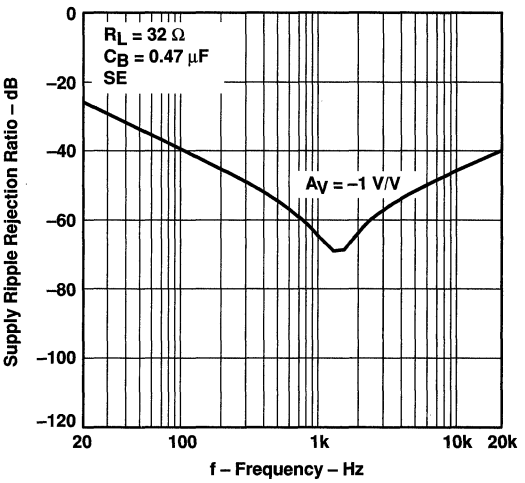


Figure 26

CROSSTALK
vs
FREQUENCY

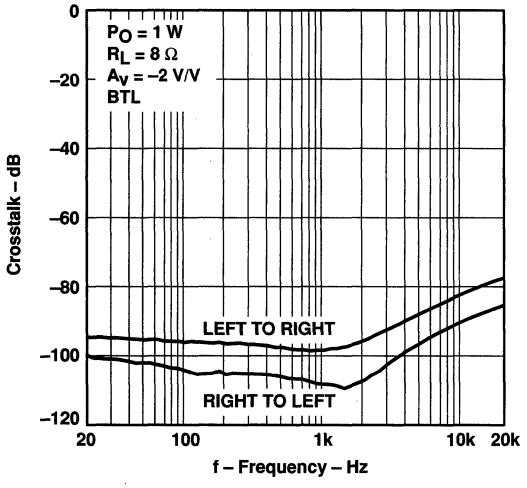


Figure 27

CROSSTALK
vs
FREQUENCY

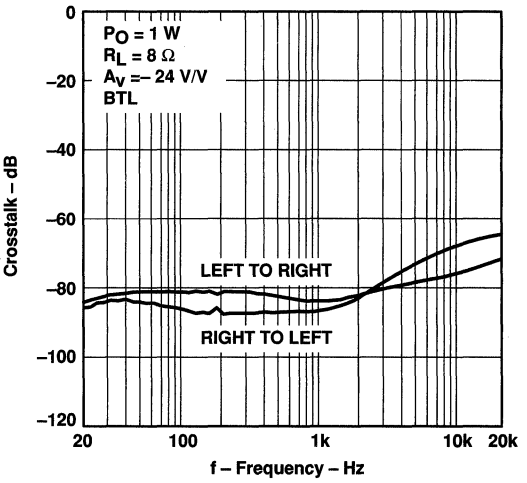


Figure 28

TYPICAL CHARACTERISTICS

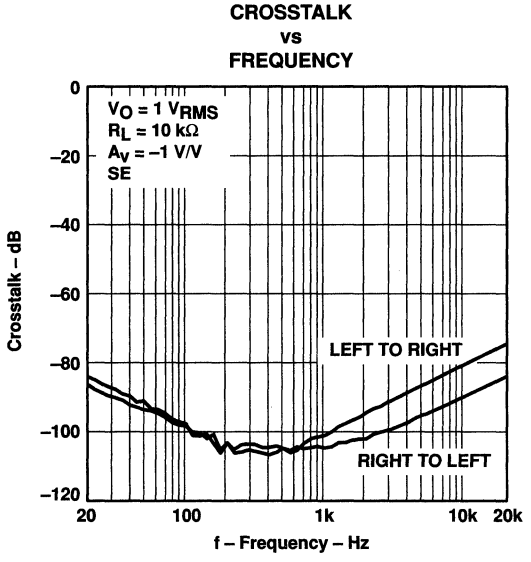


Figure 29

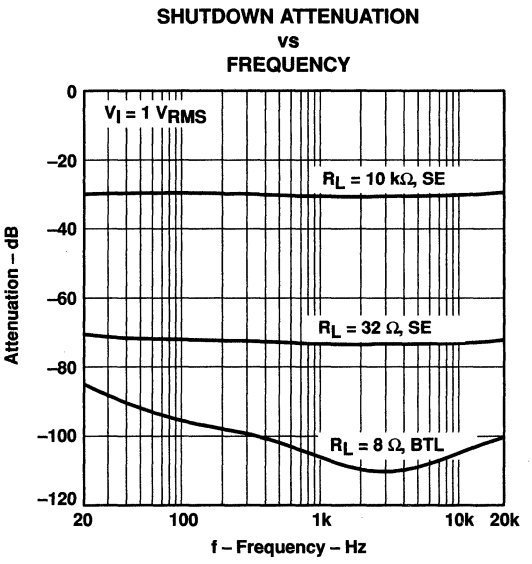


Figure 30

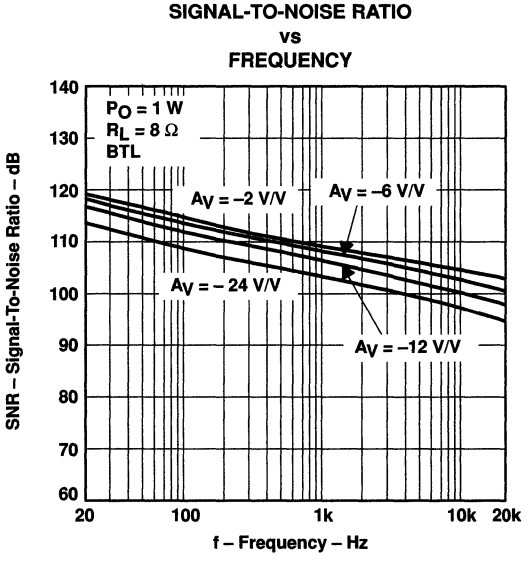


Figure 31

TYPICAL CHARACTERISTICS

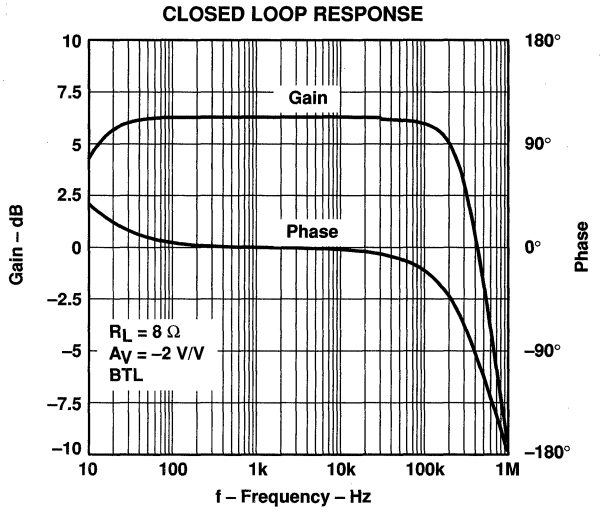


Figure 32

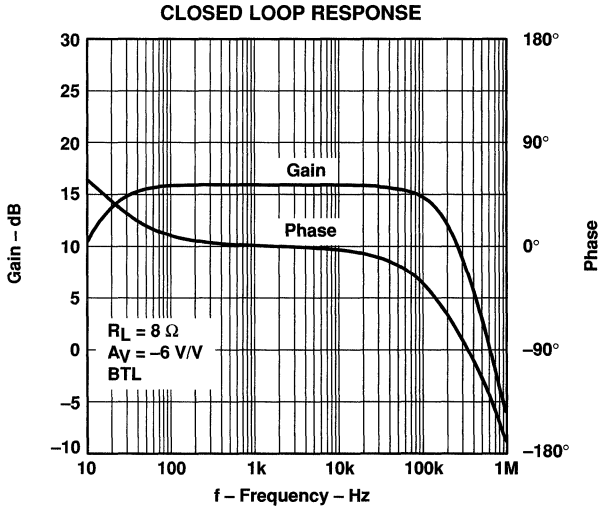


Figure 33

TYPICAL CHARACTERISTICS

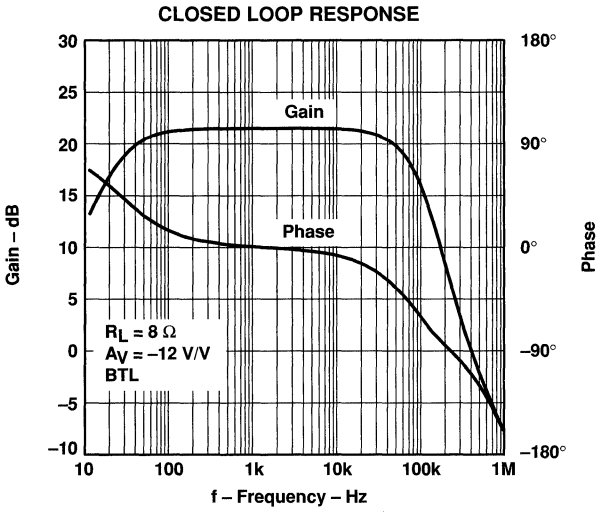


Figure 34

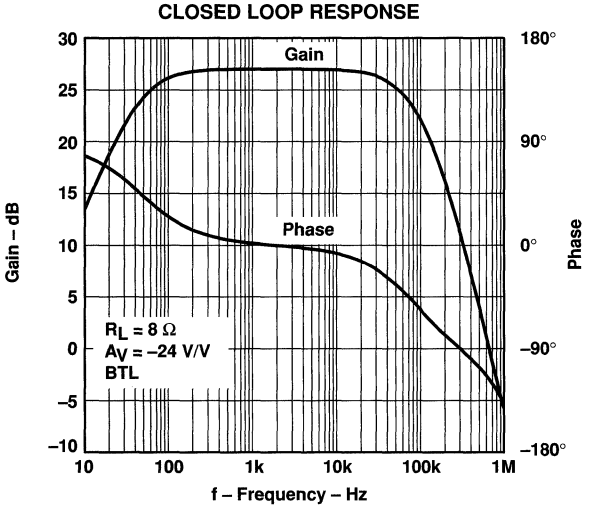


Figure 35

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

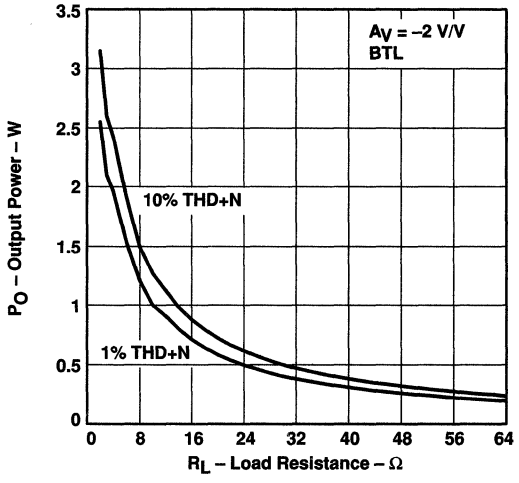


Figure 36

OUTPUT POWER
vs
LOAD RESISTANCE

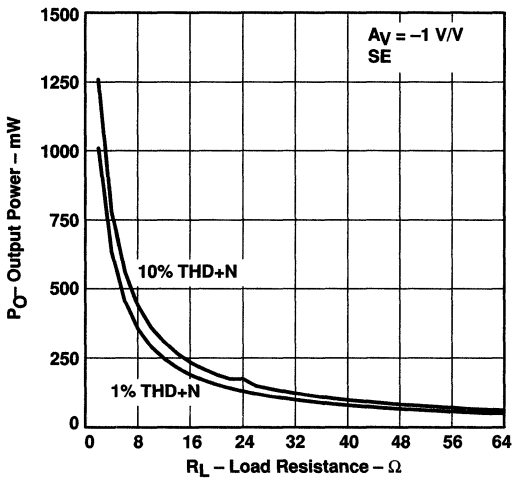


Figure 37

POWER DISSIPATION
vs
OUTPUT POWER

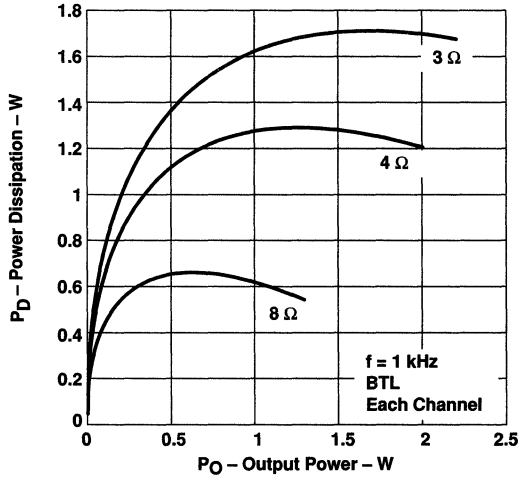


Figure 38

POWER DISSIPATION
vs
OUTPUT POWER

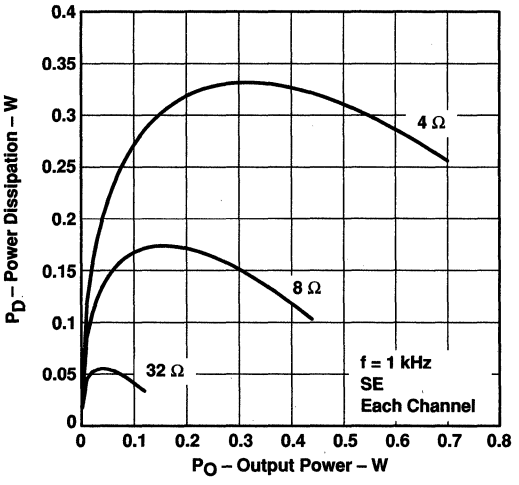


Figure 39

TYPICAL CHARACTERISTICS

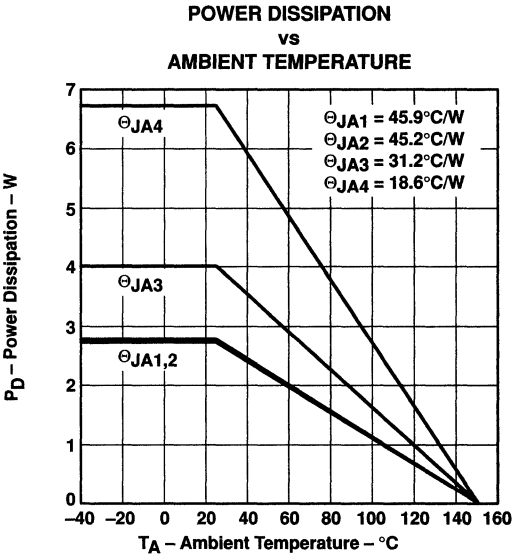


Figure 40

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 41) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

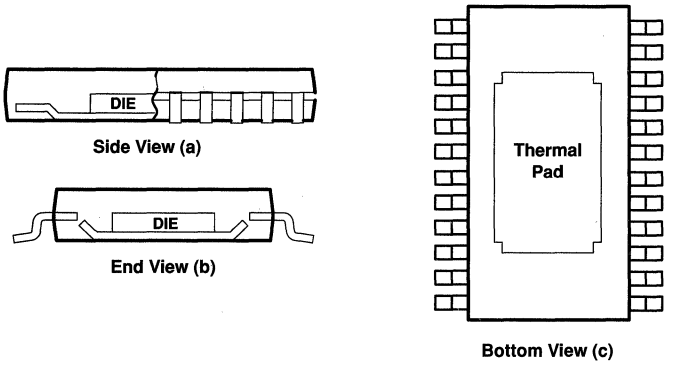
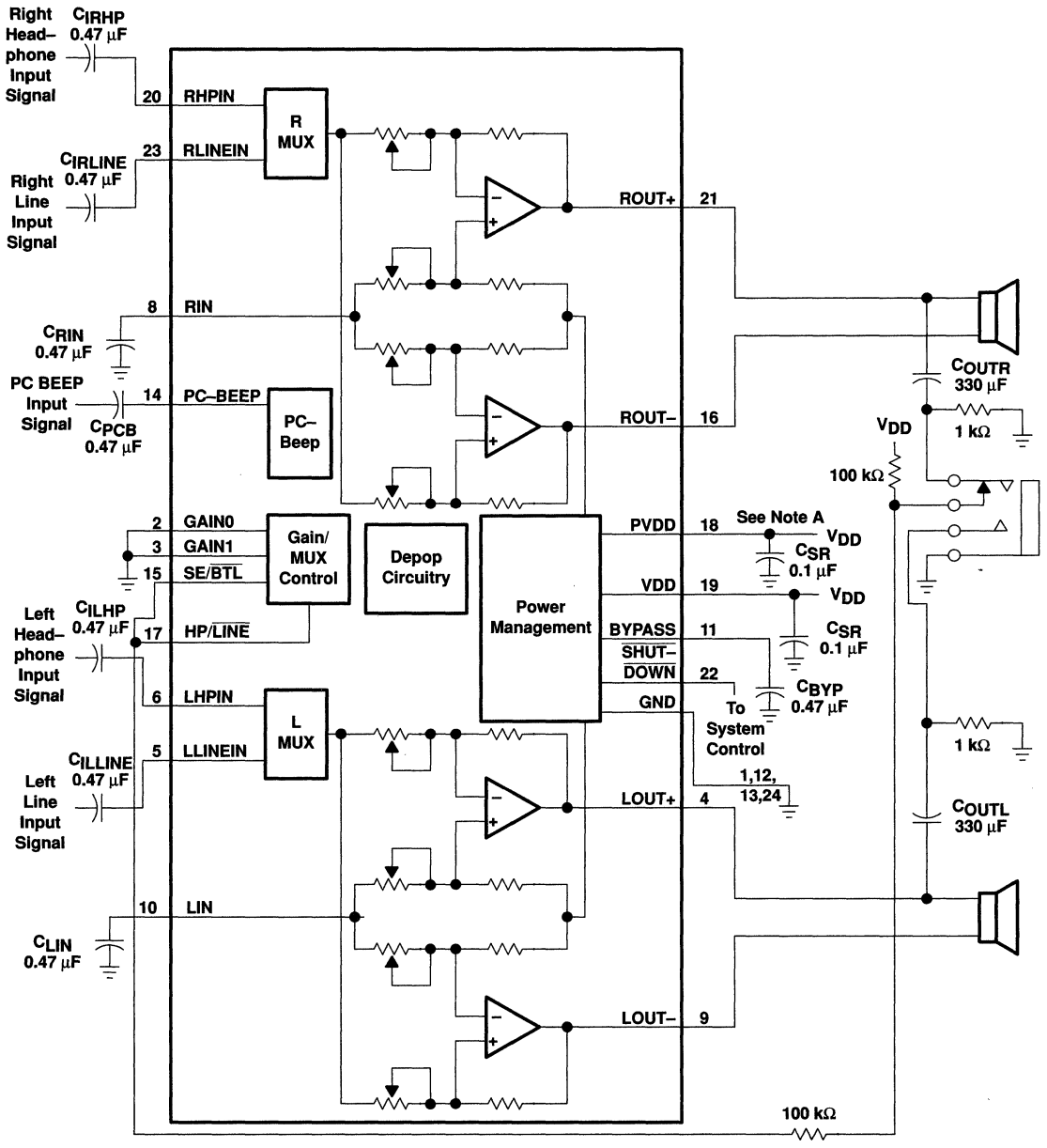


Figure 41. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

selection of components

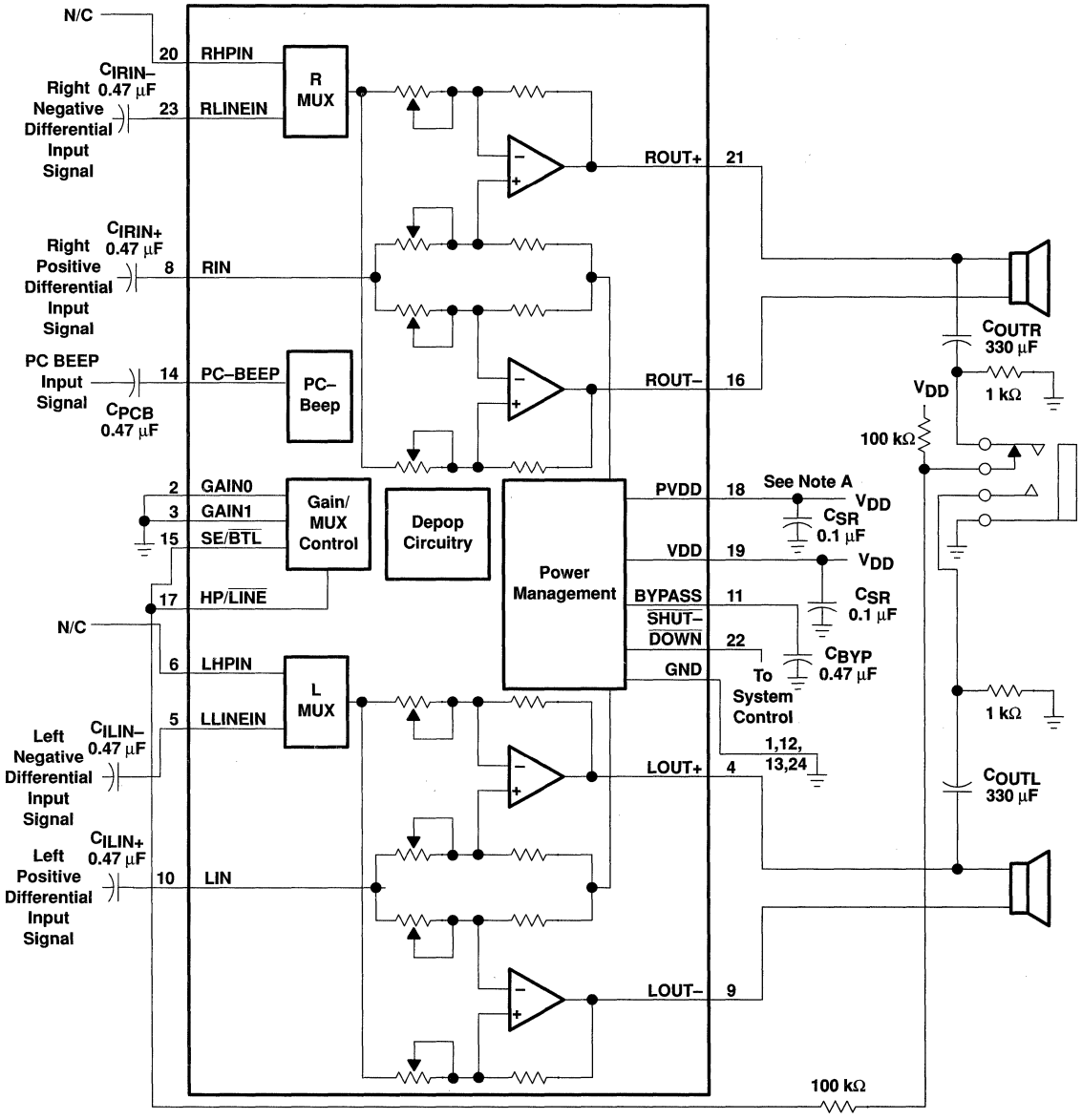
Figure 42 and Figure 43 are schematic diagrams of typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 42. Typical TPA0212 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 43. Typical TPA0212 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA0212 is set by two input terminals, GAIN0 and GAIN1.

Table 1. Gain Settings

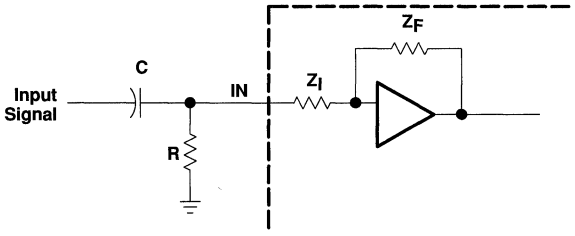
GAIN0	GAIN1	SE/$\overline{BTL}$	A_V
0	0	0	–2 V/V
0	1	0	–6 V/V
1	0	0	–12 V/V
1	1	0	–24 V/V
X	X	1	–1 V/V

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependant on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA0212. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The typical input impedance at each gain setting is given in the table below:

A_V	Z_I
–24 V/V	14 kΩ
–12 V/V	26 kΩ
–6 V/V	45.5 kΩ
–2 V/V	91 kΩ

APPLICATION INFORMATION

The –3 dB frequency can be calculated using equation 1:

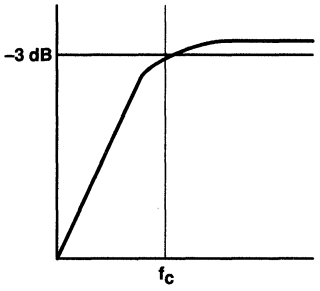
$$f_{-3\,dB} = \frac{1}{2\pi\, C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA0212 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

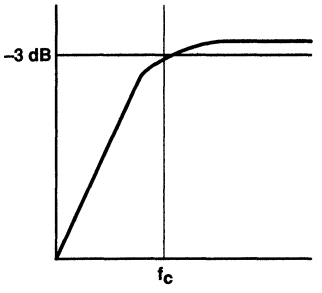
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

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Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 44 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0212 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

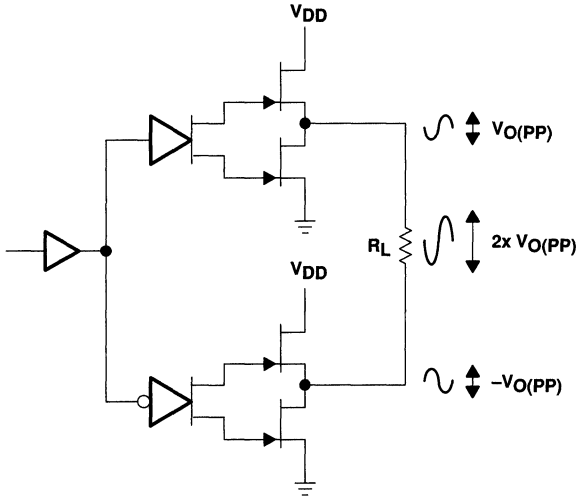

Figure 44. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 45. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

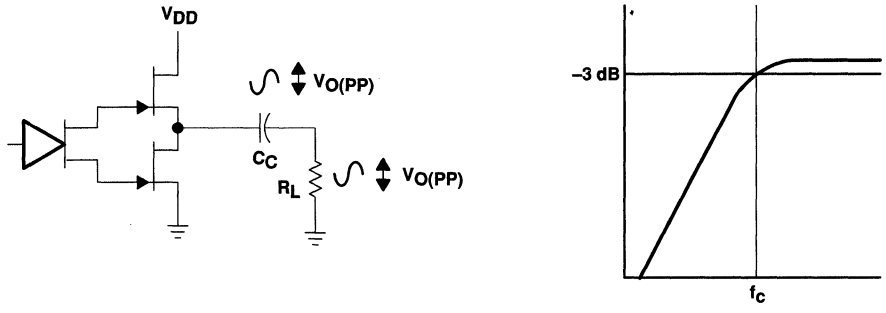

Figure 45. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 44 and Figure 45), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

input MUX operation

The input MUX allows two separate inputs to be applied to the amplifier. This allows the designer to choose which input is active independent of the state of the SE/$\overline{\text{BTL}}$ terminal. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs are active.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 46).

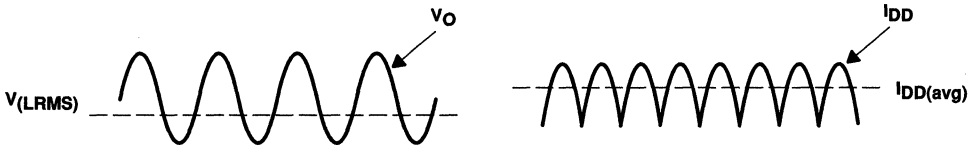

Figure 46. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

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$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \quad (7)$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = \frac{1}{\pi} \times \frac{V_P}{R_L}\,[\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\,V_{DD}\,V_P}{\pi\,R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\,R_L}}{\frac{2\,V_{DD}\,V_P}{\pi\,R_L}} = \frac{\pi\,V_P}{4\,V_{DD}}$$

Where:

$$V_P = \sqrt{2\,P_L\,R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi\sqrt{2\,P_L\,R_L}}{4\,V_{DD}} \quad (8)$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA0212 data sheet, one can see that when the TPA0212 is operating from a 5-V supply into a 3-Ω speaker 4-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0212 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0212 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 5. TPA0212 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8-Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0212 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$
$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0212 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0212 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0212, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0212 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0212 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 47.

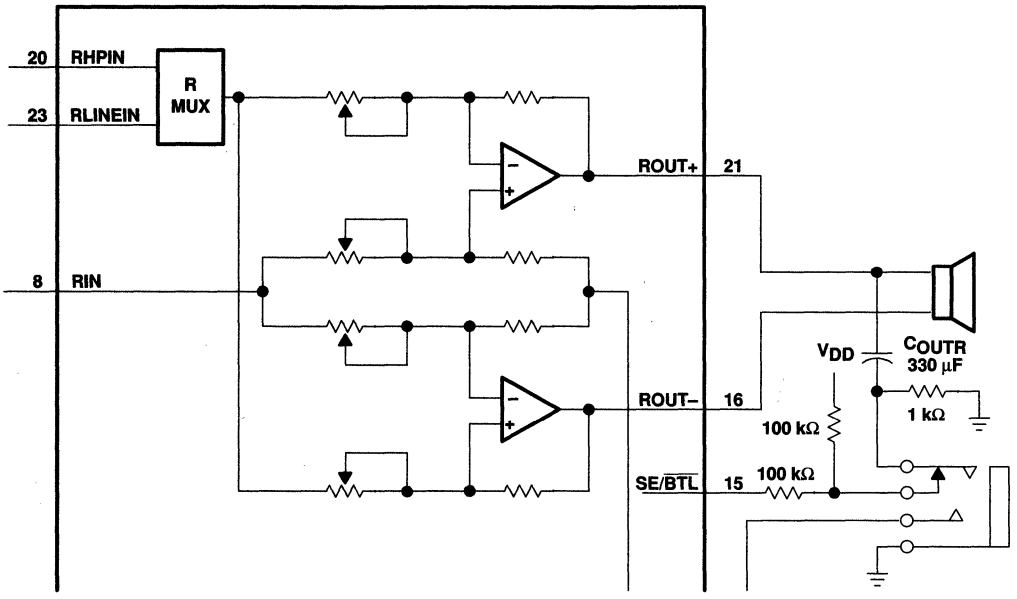


Figure 47. TPA0212 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 μs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy equation 14:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

shutdown modes

The TPA0212 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

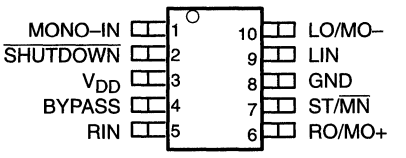
Table 6. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS†			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4-Ω From 5-V Supply**
- **0.6 W Into 4-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Separate Inputs for the Mono (BTL) Signal, and Stereo (SE) Left/Right Signals**
- **Wide Power Supply Compatibility 2.5 V to 5.5 V**
- **Low Supply Current**
  - **4.2 mA Typical at 5 V**
  - **3.6 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)

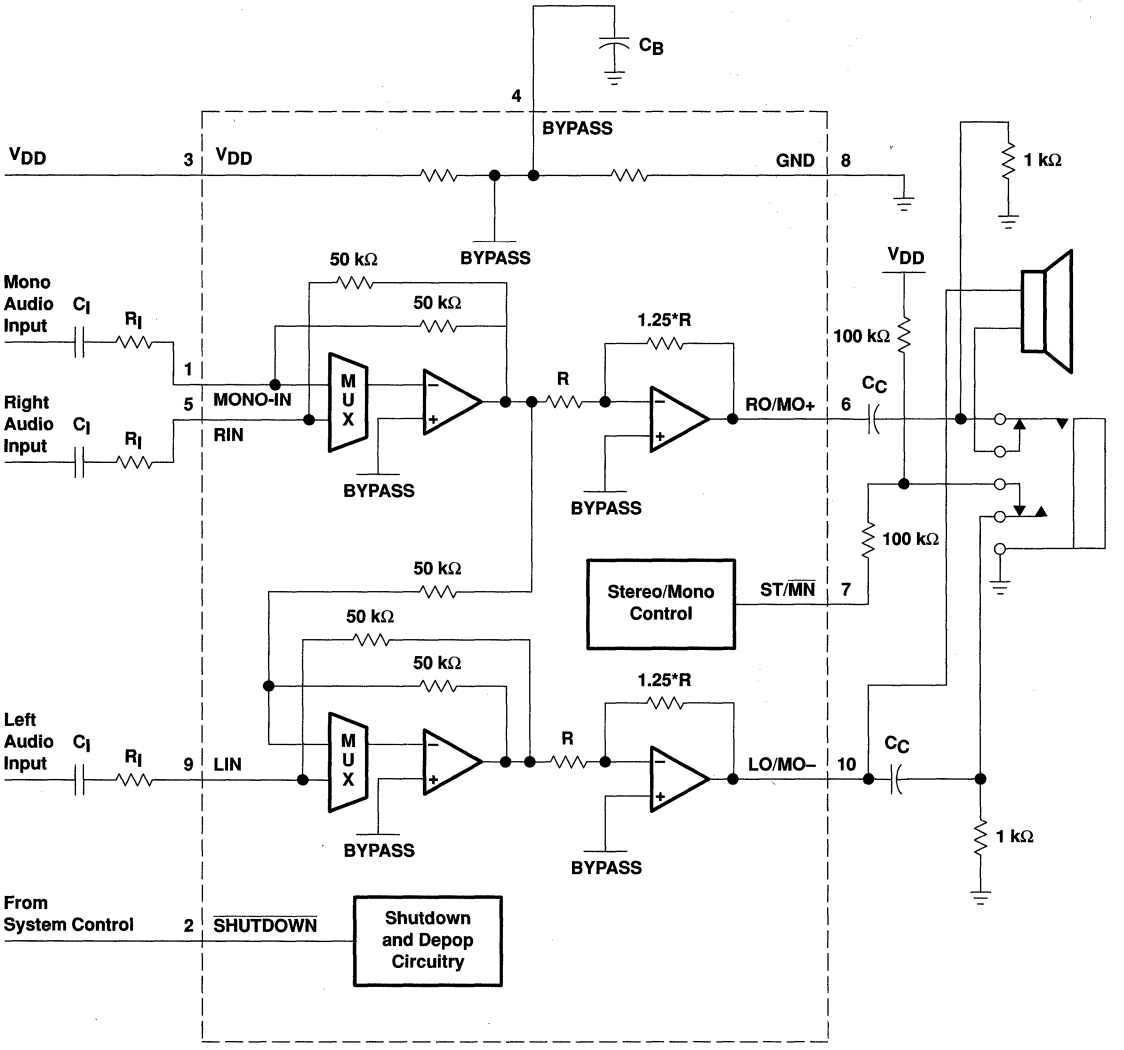


description

The TPA0213 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The amplifier can be reconfigured on-the-fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, Digital Personal Audio players, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0213 can deliver 2-W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode.

The TPA0213 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.


CB
4
BYPASS
VDD
3
VDD
GND
8
1 kΩ
50 kΩ
BYPASS
VDD
Mono
Audio
Input
CI
RI
50 kΩ
1.25*R
100 kΩ
1
MONO-IN
M
U
X
R
CC
Right
Audio
Input
CI
RI
5
RIN
RO/MO+
6
BYPASS
BYPASS
100 kΩ
50 kΩ
Stereo/Mono
Control
ST/MN
7
50 kΩ
50 kΩ
1.25*R
Left
Audio
Input
CI
RI
9
LIN
M
U
X
R
LO/MO–
10
CC
BYPASS
BYPASS
1 kΩ
From
System Control
2
SHUTDOWN
Shutdown
and Depop
Circuitry

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
–40°C to 85°C	TPA0213DGQ	AEH

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0213DGQR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MONO-IN	1	I	Mono input terminal
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
V_{DD}	3	I	V_{DD} is the supply voltage terminal.
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
RIN	5	I	Right-channel input terminal
RO/MO+	6	O	Right-output in SE mode and mono positive output in BTL mode
ST/$\overline{\text{MN}}$	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO–	10	O	Left-output in SE mode and mono negative output in BTL mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{MN}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{SHUTDOWN}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{MN}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{SHUTDOWN}$			0.8	
Operating free-air temperature, T_A			−40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_{IO} = 0,	Gain = 8 dB			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.9 V to 3.1 V,	BTL mode		65		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 3.3 V,	V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 3.3 V,	V_I = 0			1	µA
Z_I	Input impedance				50		kΩ
I_{DD}	Supply current				3.6	5.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode				1	10	µA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω, f = 1 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			660		mW
		THD = 0.1%,	SE mode,	R_L = 32 Ω		33		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 8 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	CB = 0.47 µF	BTL mode		52		dB
				SE mode		62		
V_n	Noise output voltage	CB = 0.47 µF,	f = 20 Hz to 20 kHz	BTL mode		42		μV_{RMS}
				SE mode		21		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	V_{IO} = 0,	Gain = 8 dB			30	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V,	BTL mode		62		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V,	$V_I = V_{DD}$			1	μA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V,	V_I = 0			1	μA
Z_I	Input impedance				50		kΩ
I_{DD}	Supply current				4.2	6.3	mA
$I_{DD(SD)}$	Supply current, shutdown mode				1	10	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.3%,	BTL mode			2		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		90		mW
THD + N	Total harmonic distortion plus noise	P_O = 1.5 W,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 6 dB,	THD = 2%			20		kHz
	Supple ripple rejection ratio	f = 1 kHz,	CB = 0.47 μF	BTL mode		52		dB
				SE mode		62		
V_n	Noise output voltage	CB = 0.47 μF,	f = 20 Hz to 20 kHz	BTL mode		42		μV_{RMS}
				SE mode		21		

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

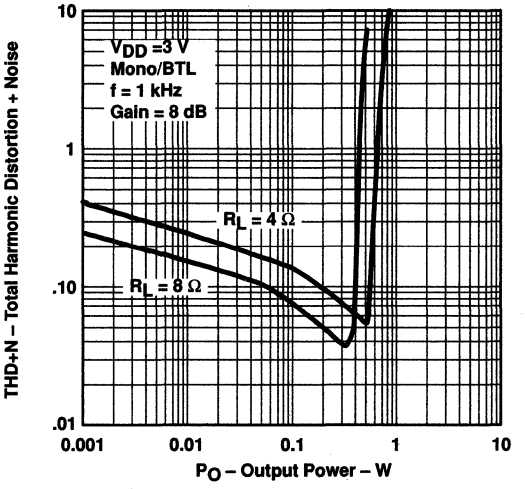


Figure 1

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

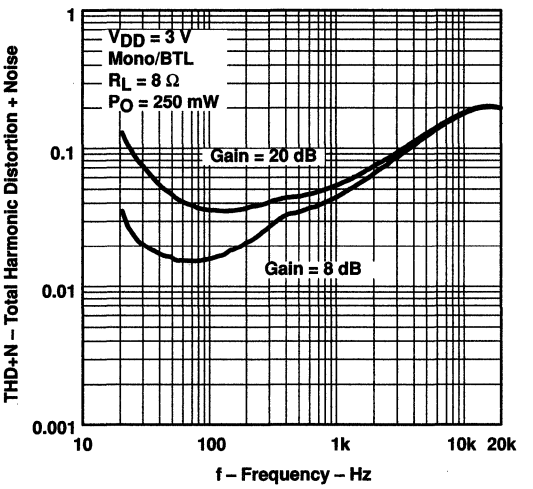


Figure 2

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

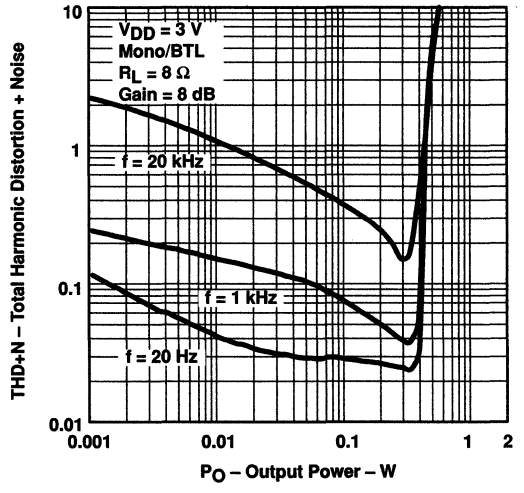


Figure 3

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

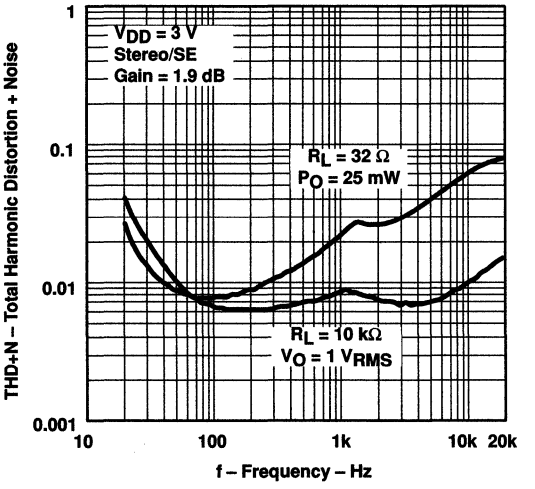


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

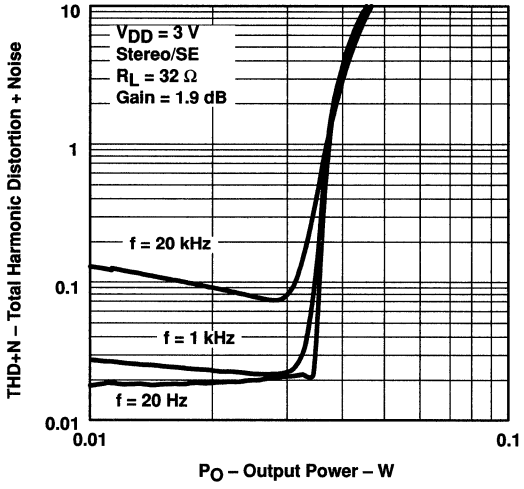


Figure 5

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

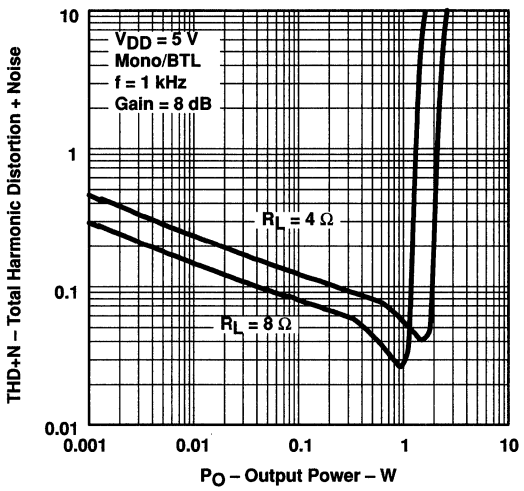


Figure 6

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

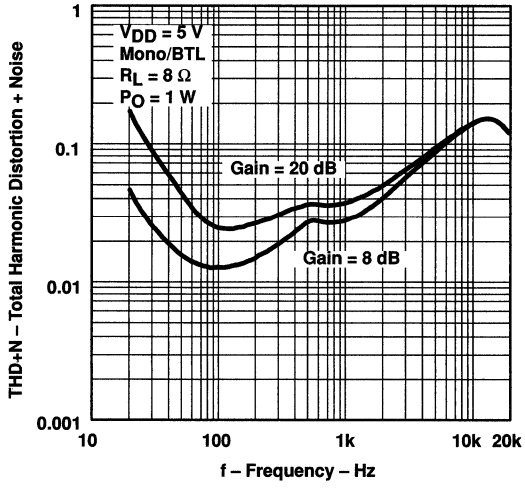


Figure 7

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

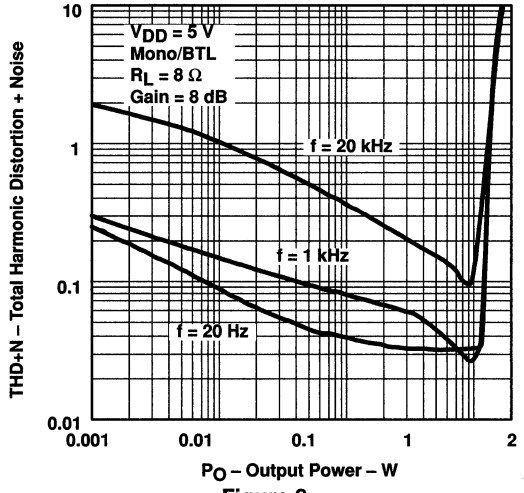


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

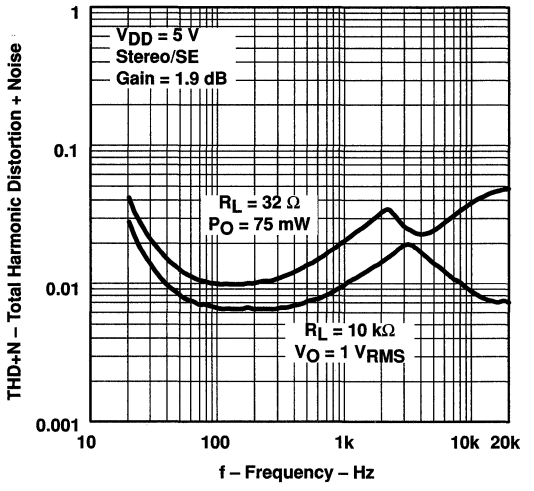


Figure 9

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

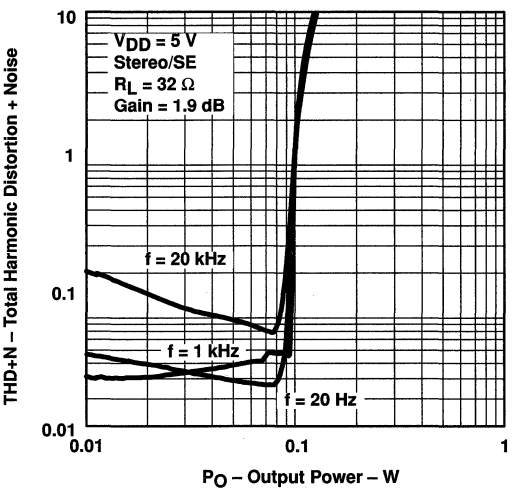


Figure 10

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

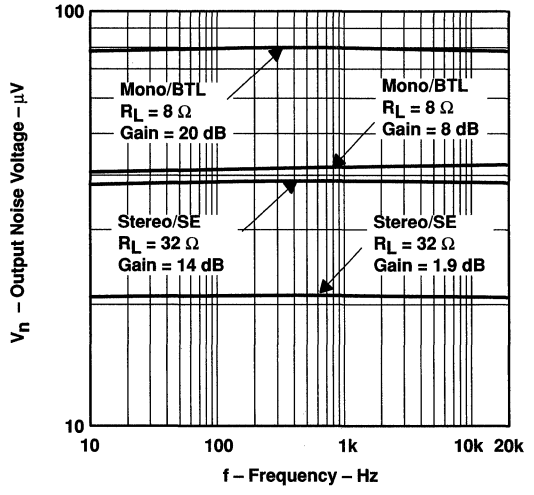


Figure 11

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

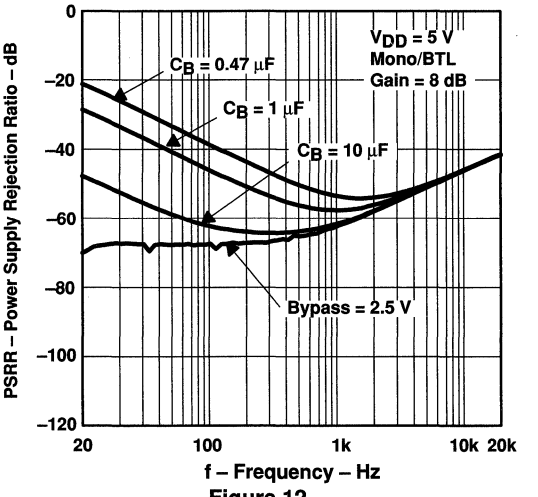


Figure 12

TYPICAL CHARACTERISTICS

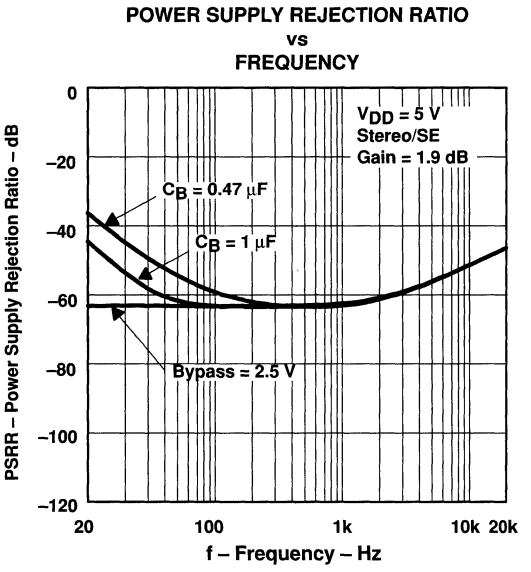
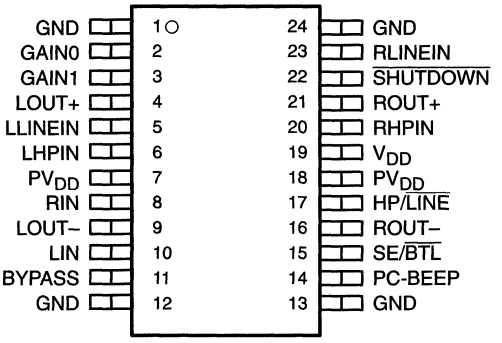


Figure 13

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **2-W/Ch Output Power Into 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0222 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0222 has less than 0.5% THD+N across its specified frequency range.

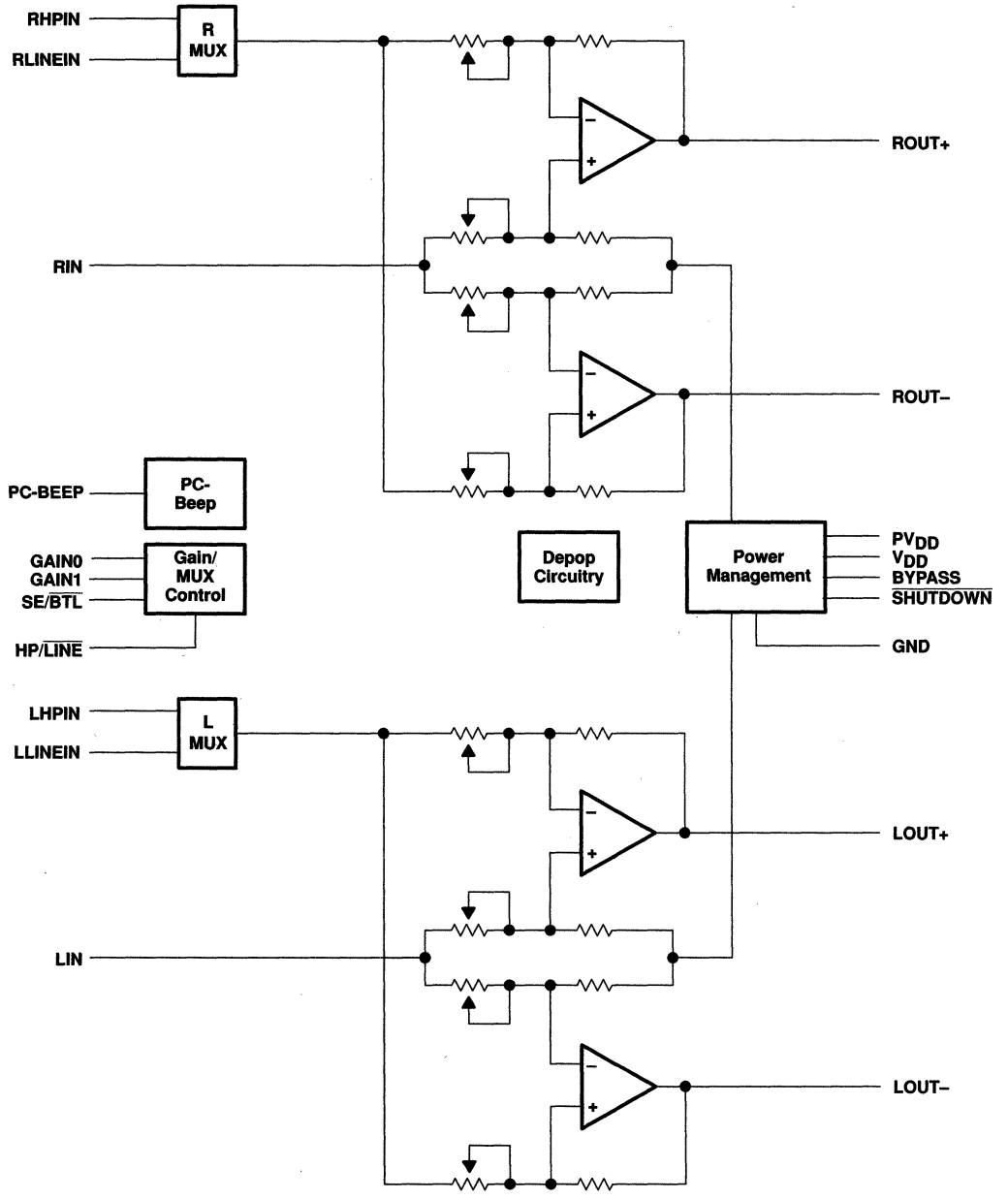
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by two terminals (GAIN0 and GAIN1). BTL gain settings of 2, 6, 12, and 24 V/V are provided, while SE gain is always configured as 1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0222 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and reduces the gain to 1 V/V.

The TPA0222 consumes only 18 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0222 to operate at full power into 8-Ω loads at an ambient temperature of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0222PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0222PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
GAIN0	2	I	Bit 0 of gain control
GAIN1	3	I	Bit 1 of gain control
GND	1, 12, 13, 24		Ground connection for circuitry. Connected to the thermal pad
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in BTL mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in BTL mode and high-impedance in SE mode
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
HP/$\overline{\text{LINE}}$	17	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in BTL mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in BTL mode and high-impedance in SE mode
$\overline{\text{SHUTDOWN}}$	22	I	Places entire IC in shutdown mode when held low, except PC-BEEP remains active
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$	4		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = –2 V/V			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		77		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		18		mA
		SE mode		9		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω, Gain = –2 V/V, BTL mode

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%, R_L = 4 Ω	f = 1 kHz,		1.9		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.5%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		68		dB
SNR	Signal-to-noise ratio				105		dB
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		16		µV RMS
			SE mode		30		
Z_I	Input impedance				See Table 1		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4–7, 10–13, 16–19, 21
		vs Frequency	2, 3, 8, 9, 14, 15, 20, 22
		vs Output voltage	23
V_n	Output noise voltage	vs Bandwidth	24
	Supply ripple rejection ratio	vs Frequency	25, 26
	Crosstalk	vs Frequency	27–29
	Shutdown attenuation	vs Frequency	30
SNR	Signal-to-noise ratio	vs Bandwidth	31
	Closed loop respone		32–35
P_O	Output power	vs Load resistance	36, 37
P_D	Power dissipation	vs Output power	38, 39
		vs Ambient temperature	40

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

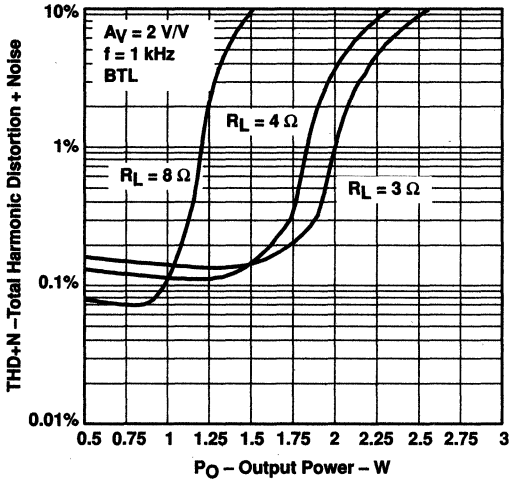


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

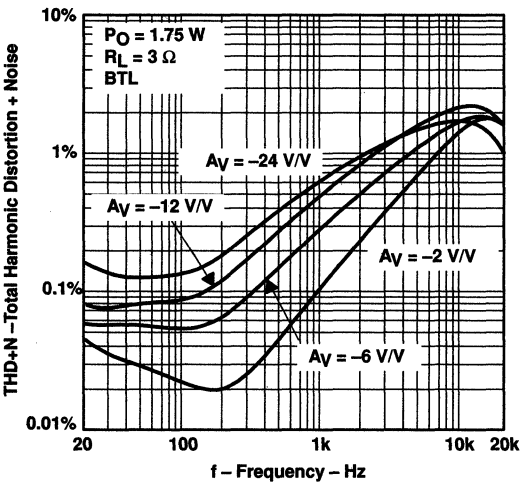


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

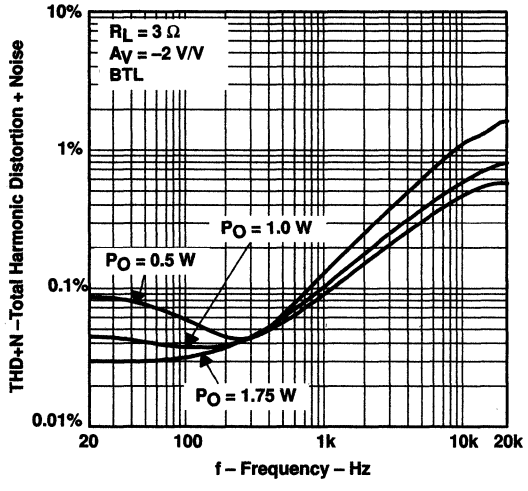


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

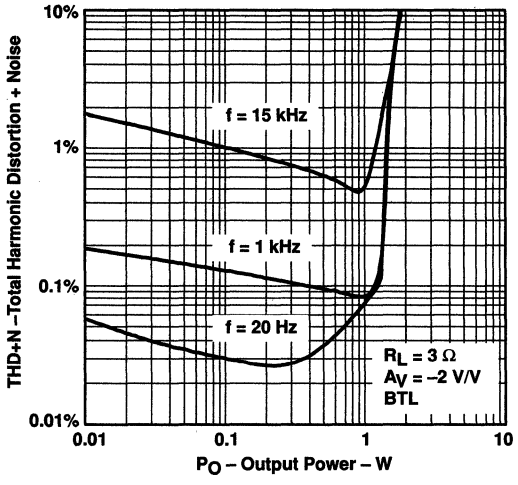


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

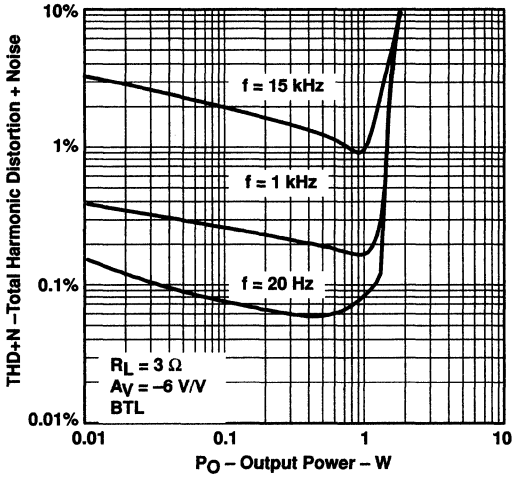


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

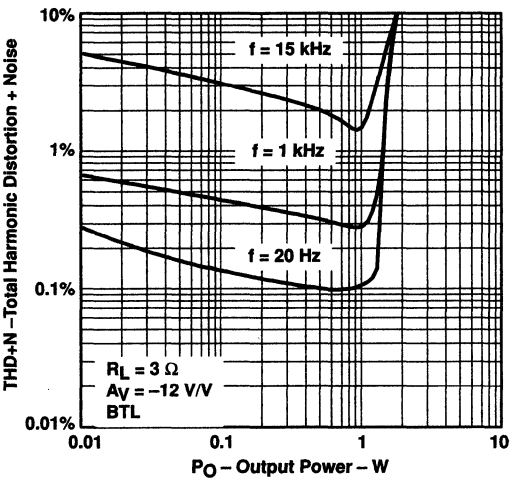


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

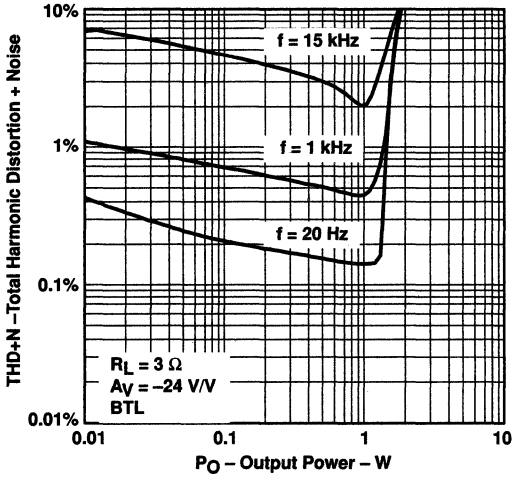


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

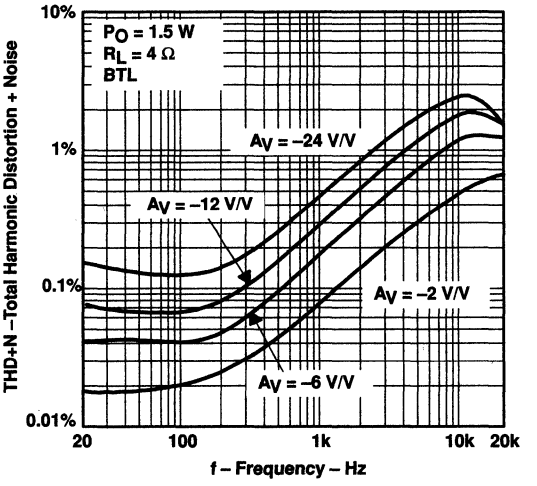


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

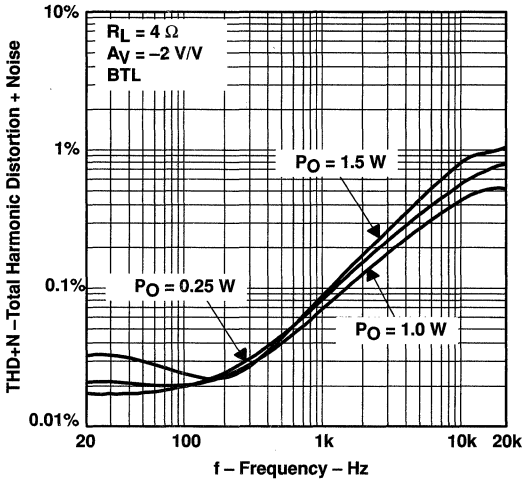


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

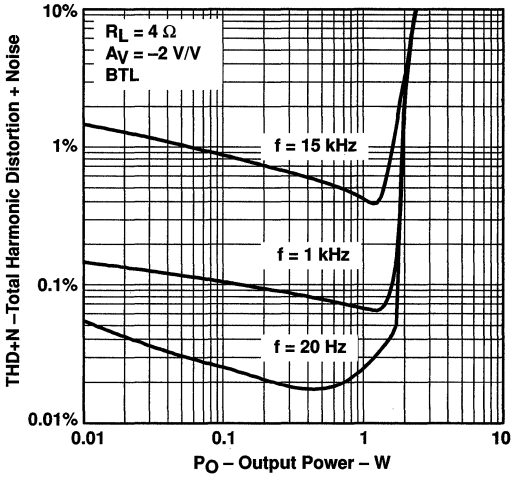


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

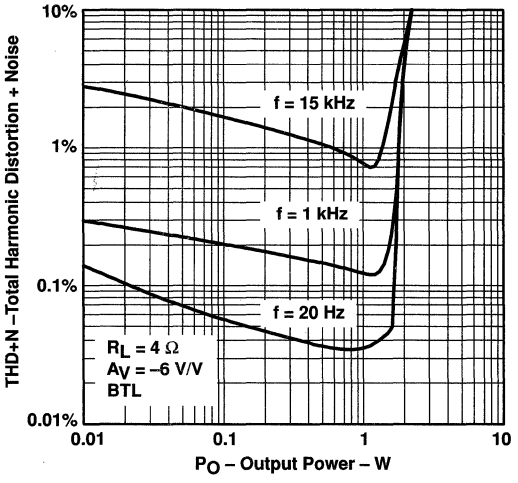


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

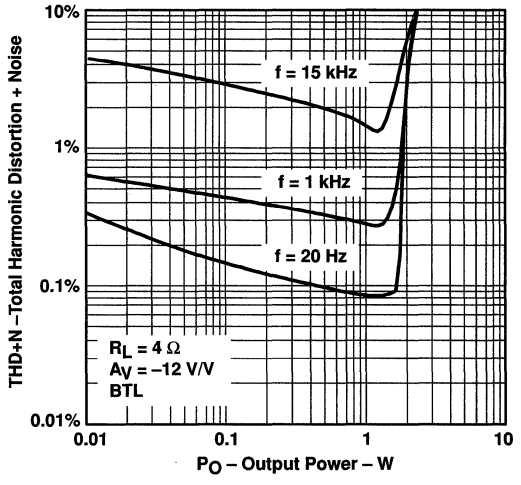


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

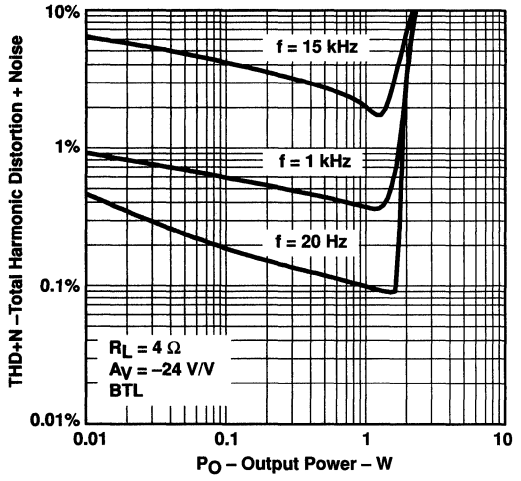


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

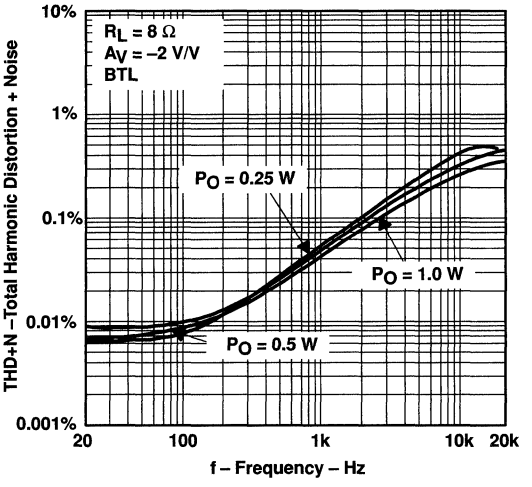


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

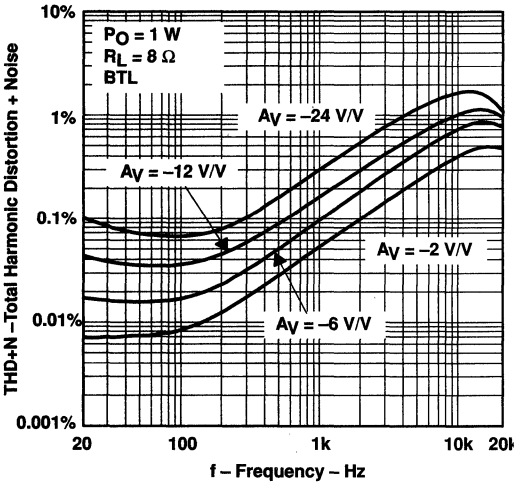


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

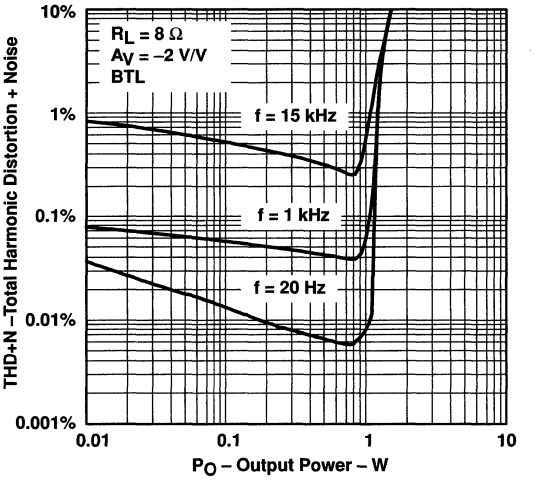


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

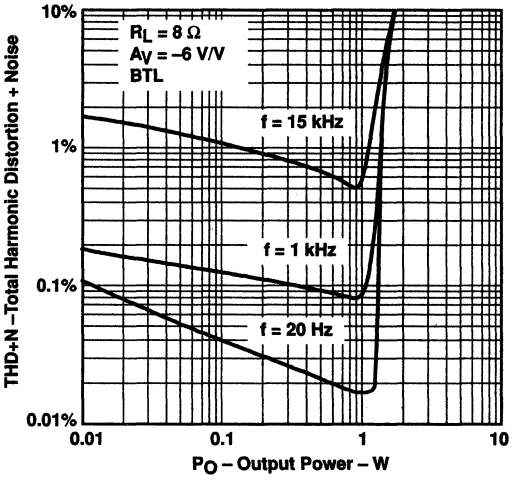


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

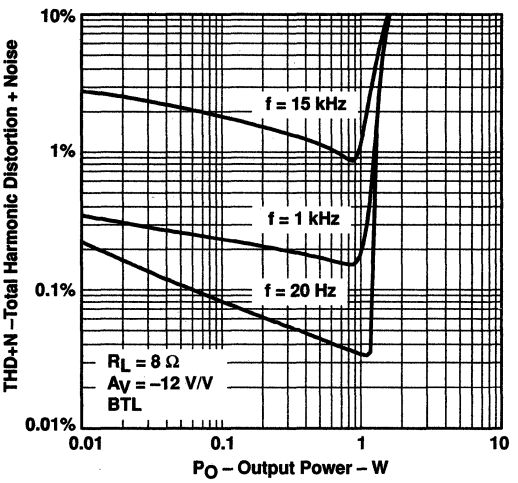


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

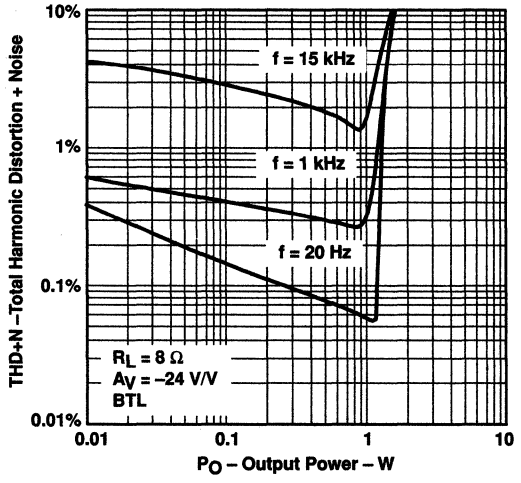


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

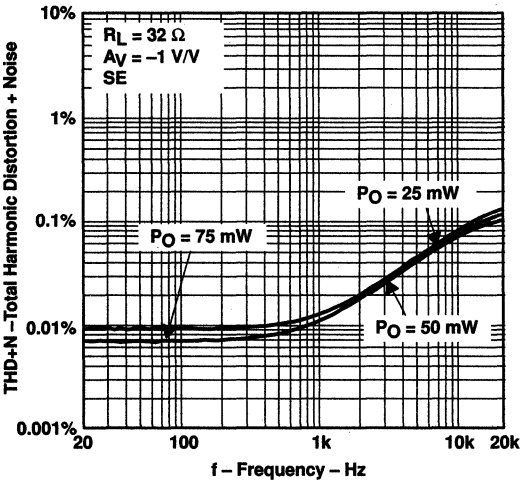


Figure 20

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

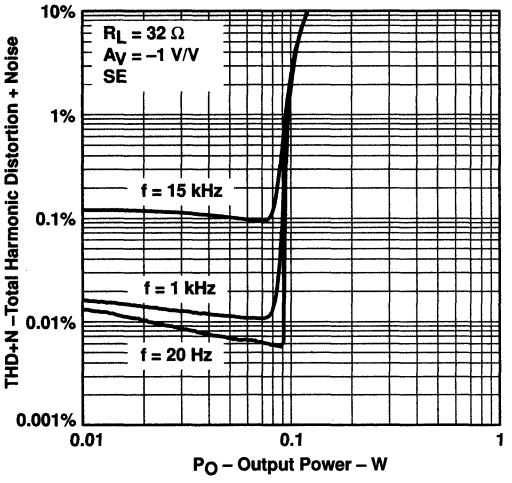


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

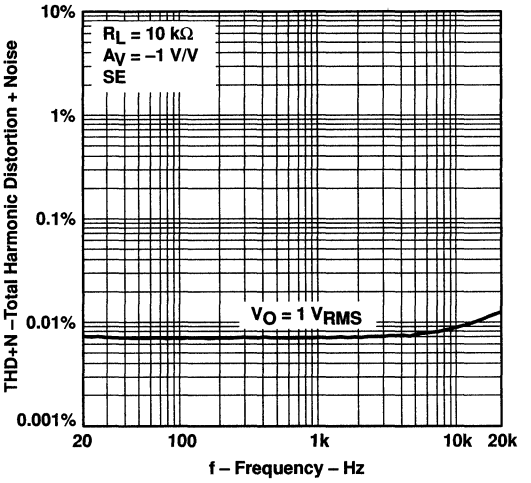


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

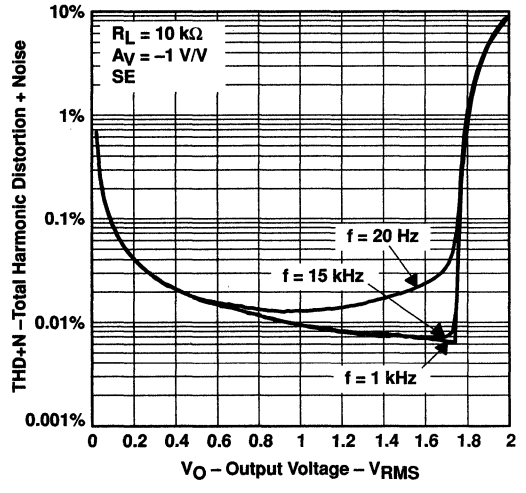


Figure 23

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

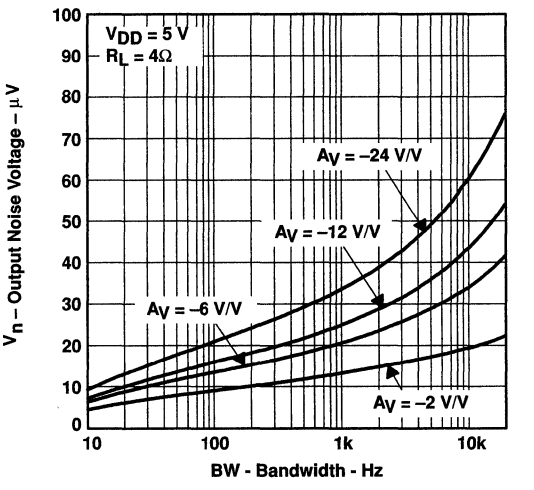


Figure 24

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

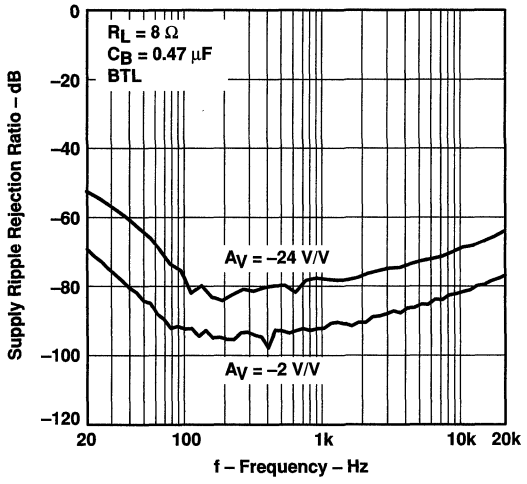


Figure 25

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

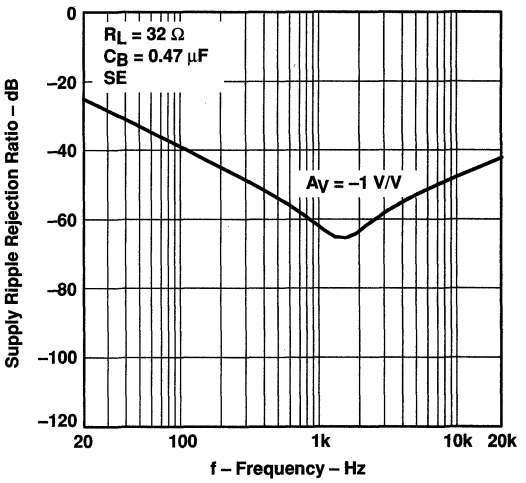


Figure 26

CROSSTALK
vs
FREQUENCY

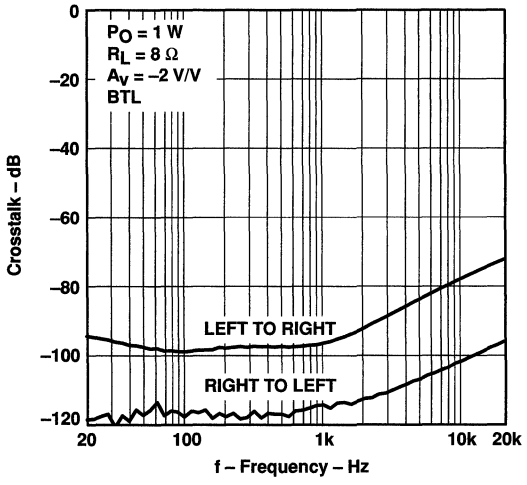


Figure 27

CROSSTALK
vs
FREQUENCY

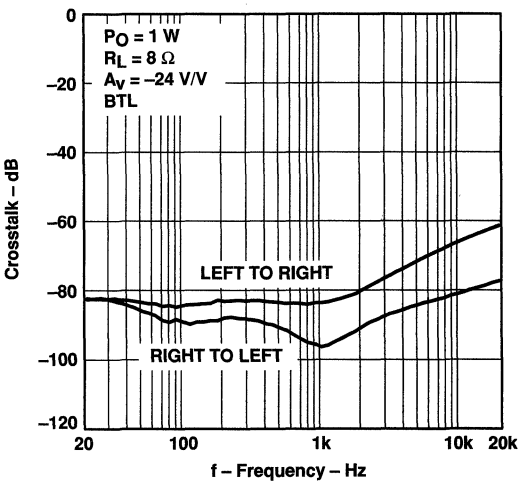


Figure 28

TYPICAL CHARACTERISTICS

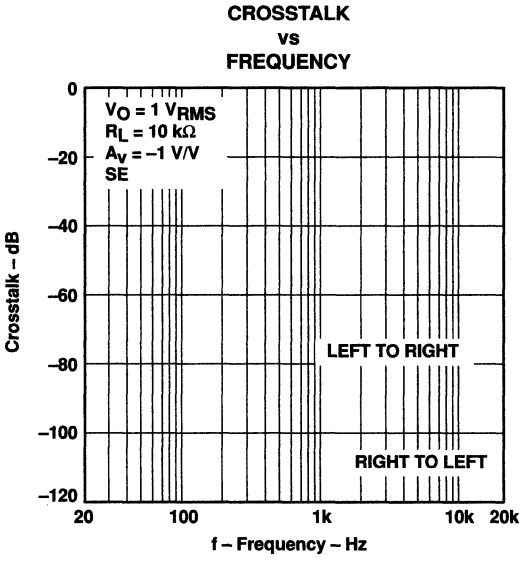


Figure 29

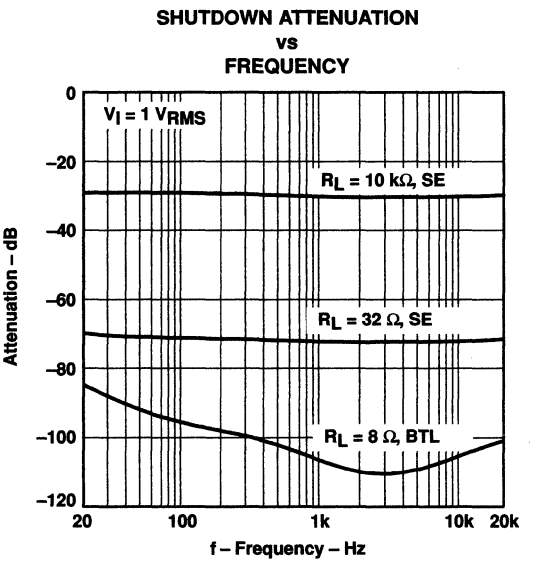


Figure 30

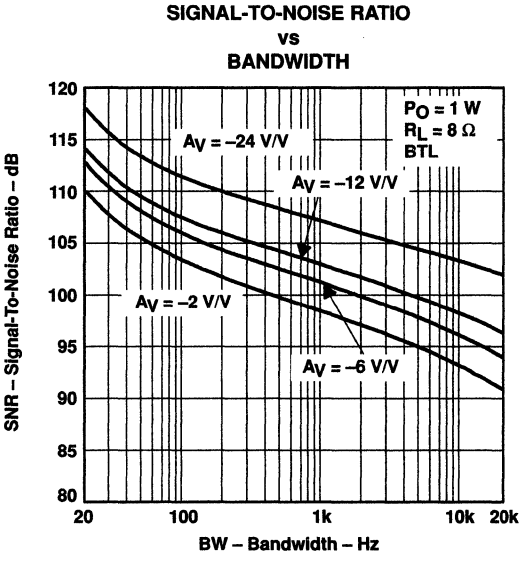


Figure 31

TYPICAL CHARACTERISTICS

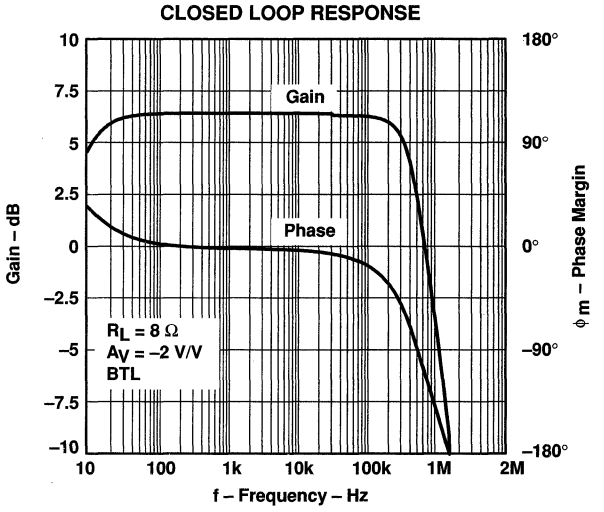


Figure 32

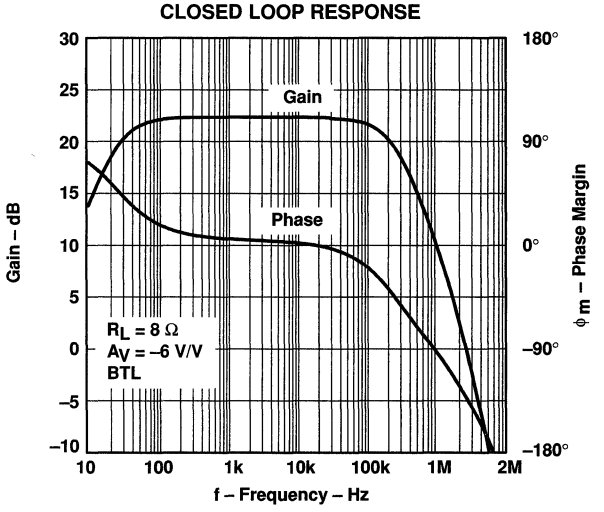


Figure 33

TYPICAL CHARACTERISTICS

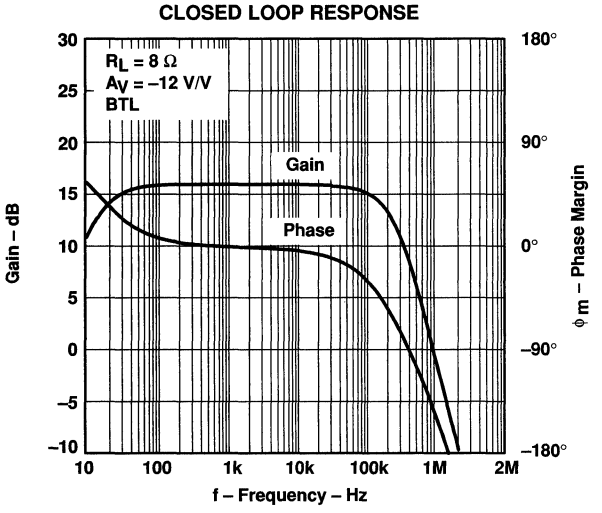


Figure 34

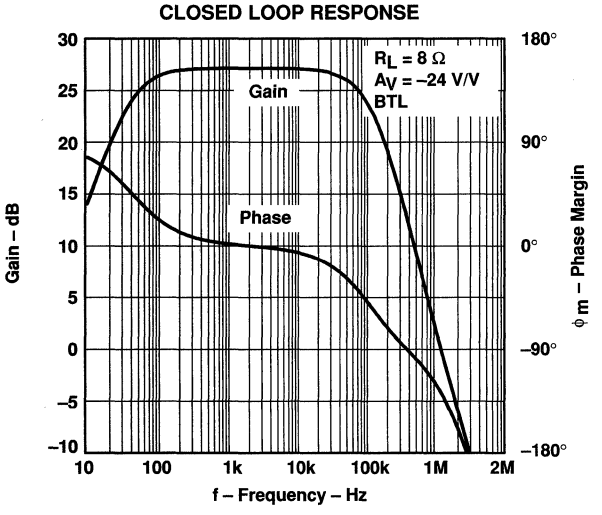


Figure 35

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

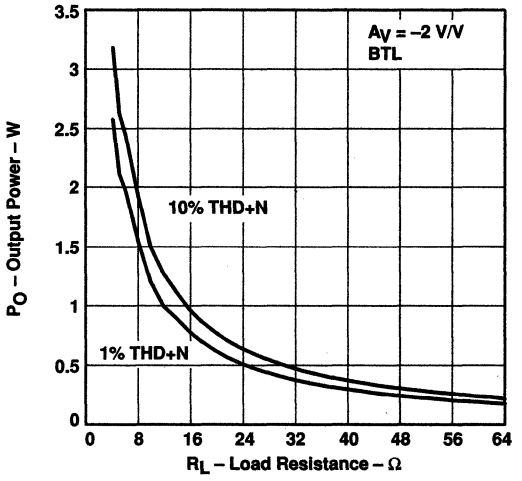


Figure 36

OUTPUT POWER
vs
LOAD RESISTANCE

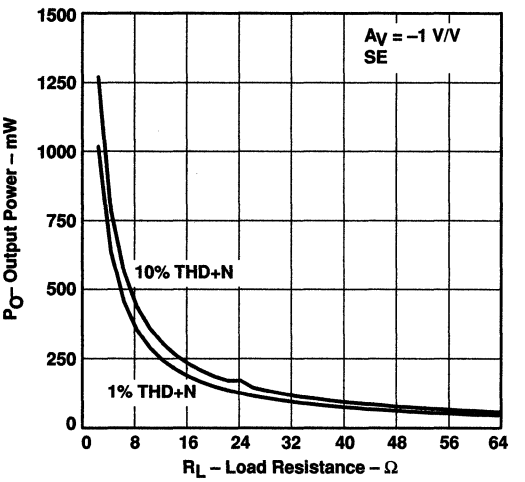


Figure 37

POWER DISSIPATION
vs
OUTPUT POWER

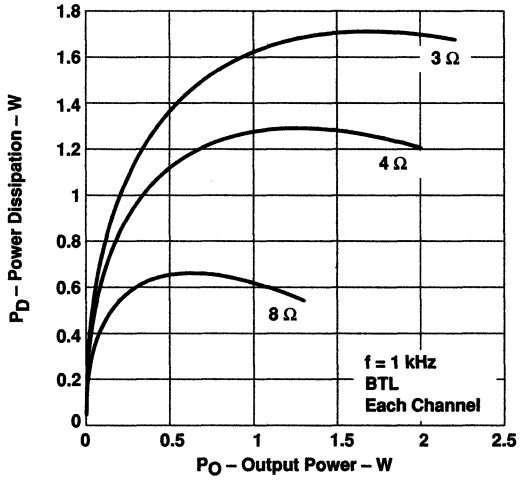


Figure 38

POWER DISSIPATION
vs
OUTPUT POWER

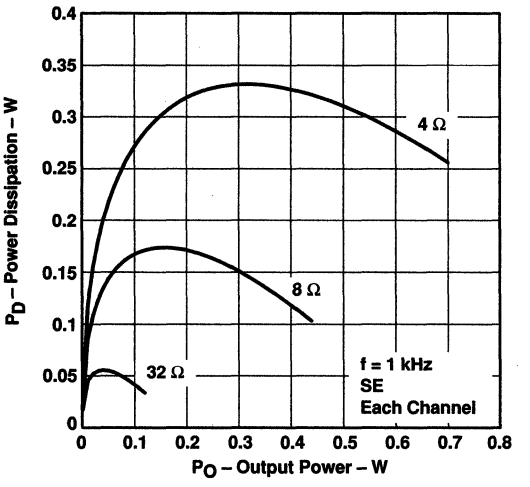


Figure 39

APPLICATION INFORMATION

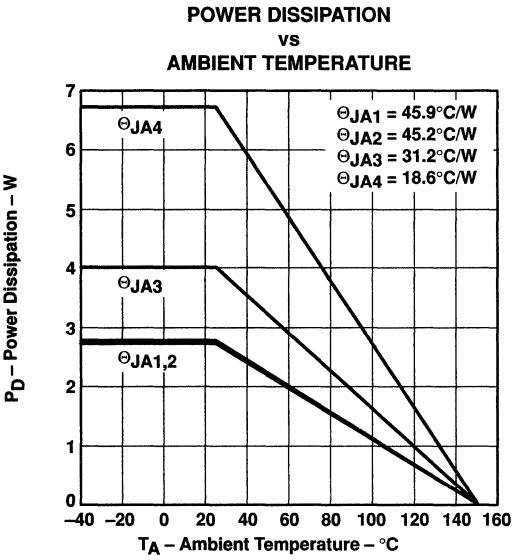


Figure 40

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 41) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

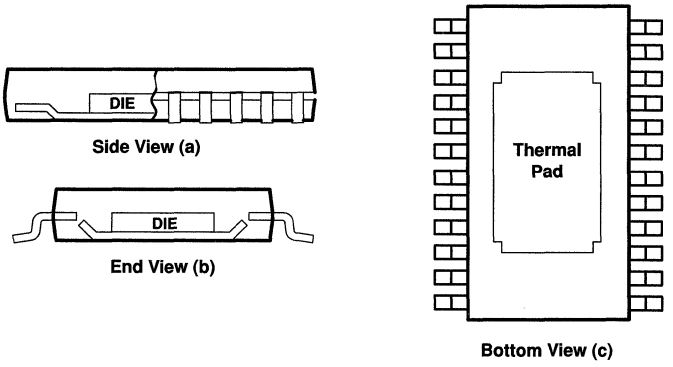
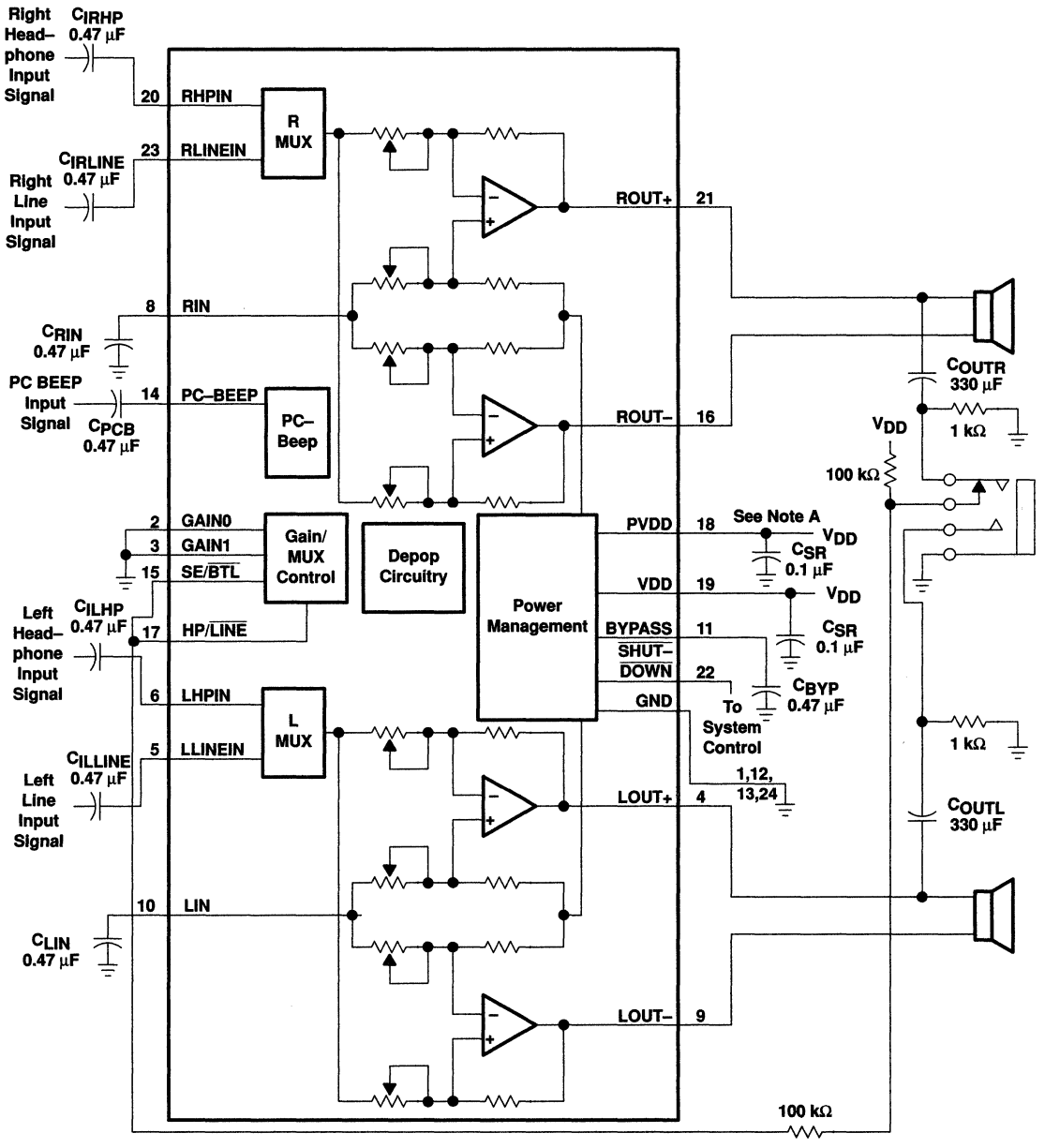


Figure 41. Views of Thermally Enhanced PWP Package

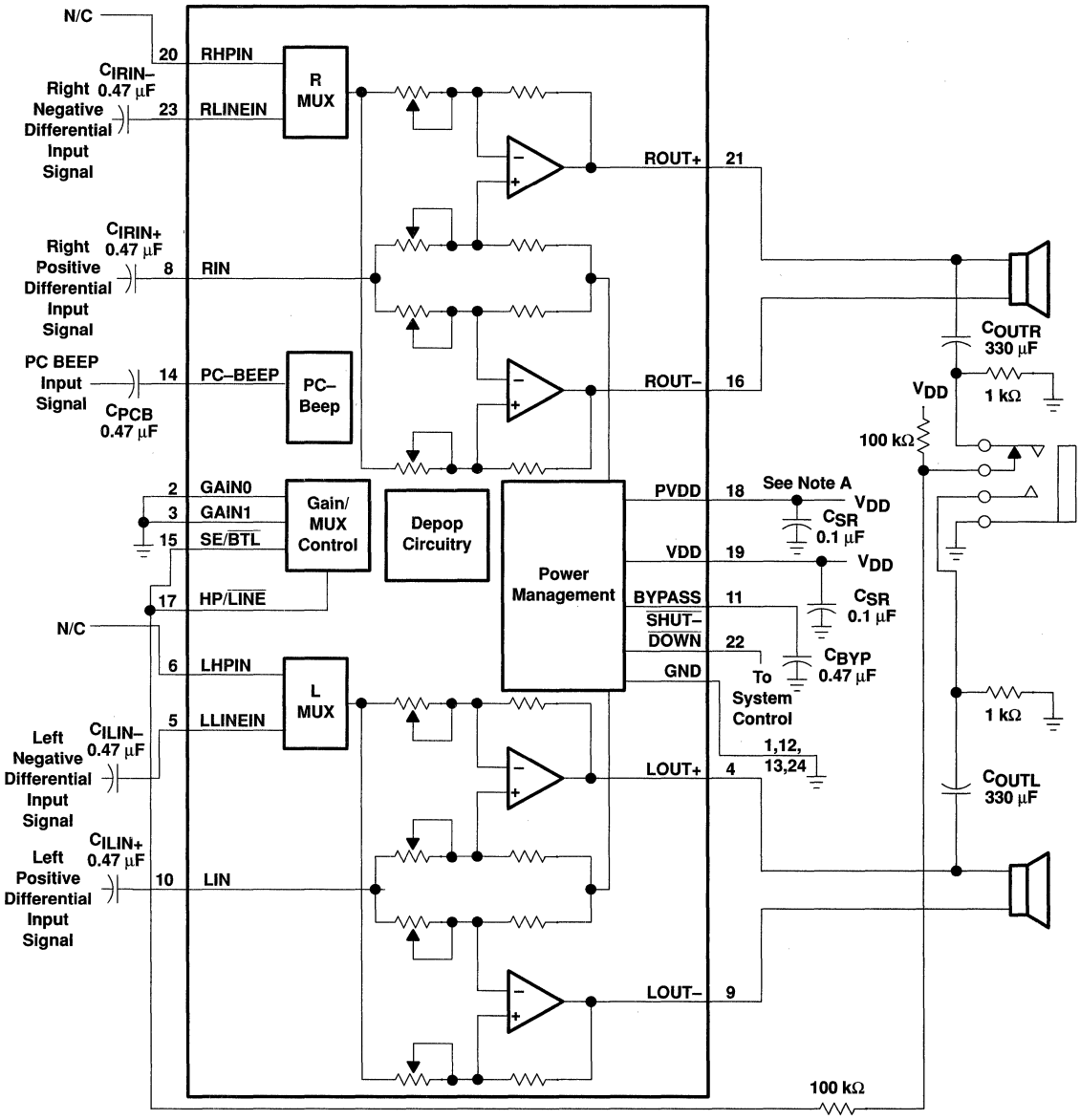
Figure 42 and Figure 43 are schematic diagrams of typical notebook computer application circuits.



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 42. Typical TPA0222 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 43. Typical TPA0222 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

gain setting via GAIN0 and GAIN1 inputs

The gain of the TPA0222 is set by two input terminals, GAIN0 and GAIN1.

Table 1. Gain Settings

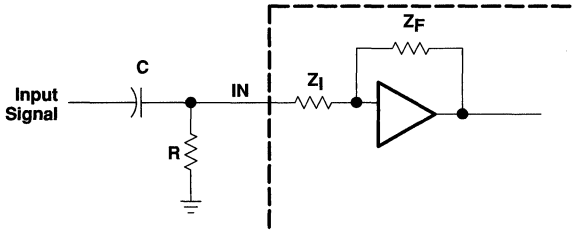
GAIN0	GAIN1	SE/$\overline{\text{BTL}}$	A_V
0	0	0	–2 V/V
0	1	0	–6 V/V
1	0	0	–12 V/V
1	1	0	–24 V/V
X	X	1	–1 V/V

The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance, Z_I, to be dependant on the gain setting. The actual gain settings are controlled by ratios of resistors, so the actual gain distribution from part-to-part is quite good. However, the input impedance will shift by 30% due to shifts in the actual resistance of the input impedance.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 10 kΩ, which is the absolute minimum input impedance of the TPA0222. At the higher gain settings, the input impedance could increase as high as 115 kΩ.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.



The typical input resistance at each gain setting is given in the table below:

A_V	Z_I
–24 V/V	14 kΩ
–12 V/V	26 kΩ
–6 V/V	45.5 kΩ
–2 V/V	91 kΩ

APPLICATION INFORMATION

The –3 dB frequency can be calculated using equation 1:

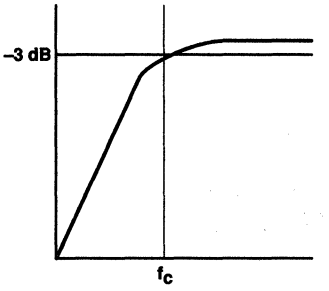
$$f_{-3\,dB} = \frac{1}{2\pi\, C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (2)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA0222 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

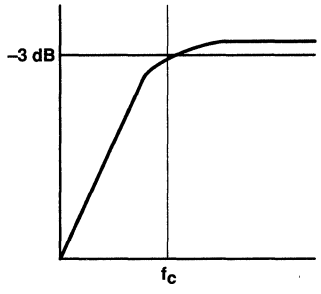
The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

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Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 44 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0222 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

APPLICATION INFORMATION

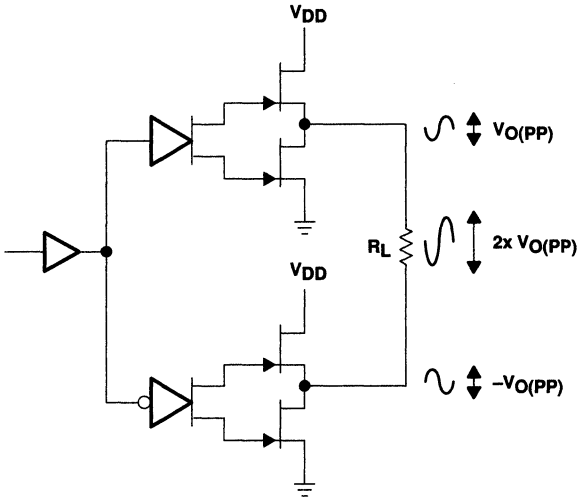


Figure 44. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 45. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

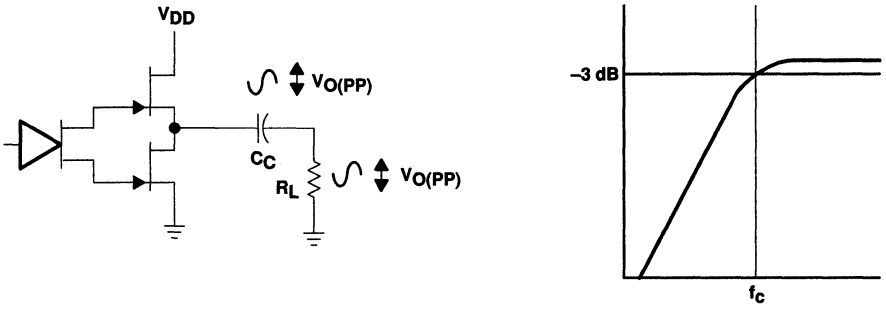


Figure 45. Single-Ended Configuration and Frequency Response

APPLICATION INFORMATION

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 44 and Figure 45), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1 V/V.

input MUX operation

The input MUX allows two separate inputs to be applied to the amplifier. This allows the designer to choose which input is active independent of the state of the SE/$\overline{\text{BTL}}$ terminal. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs are active.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 46).

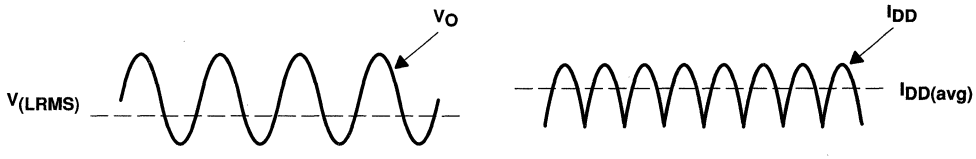


Figure 46. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

APPLICATION INFORMATION

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

and $P_{SUP} = V_{DD}\, I_{DD}avg$ and $I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA0222 data sheet, one can see that when the TPA0222 is operating from a 5-V supply into a 3-Ω speaker 4-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \tag{9}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{10}$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0222 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0222 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 5. TPA0222 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8-Ω load than for a 3-Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8-Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of a 3-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0222 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \tag{13}$$
$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

TableS 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0222 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0222 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0222, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0222 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0222 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 47.

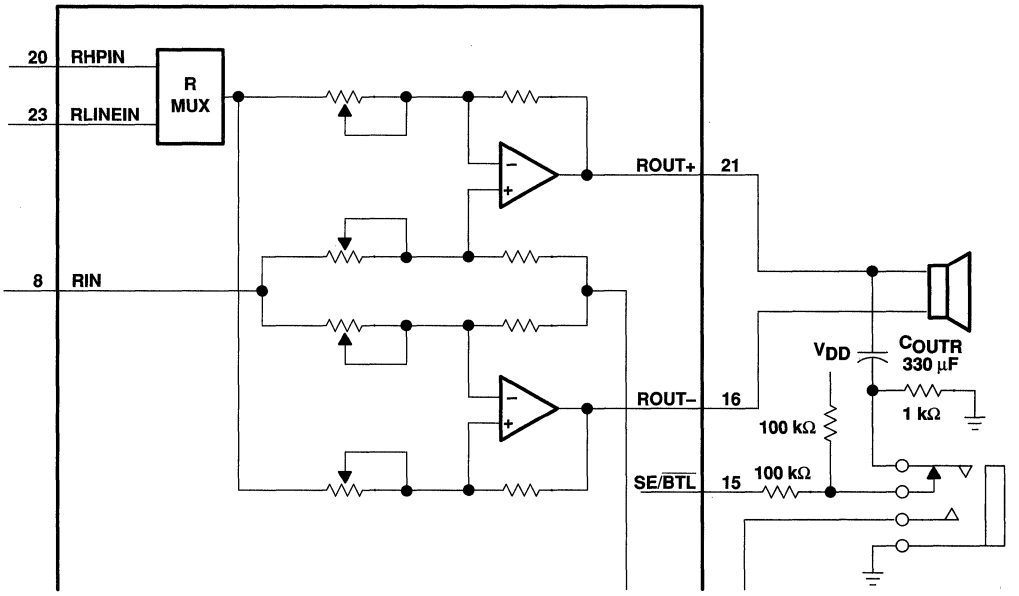


Figure 47. TPA0222 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

APPLICATION INFORMATION

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 μs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy equation 14:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

shutdown modes

The TPA0222 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

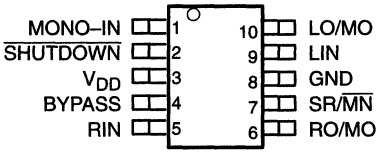
Table 6. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS†			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4-Ω From 5-V Supply**
- **0.6 W Into 4-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Separate Inputs for the Mono (BTL) Signal and Stereo (SE) Left/Right Signals**
- **Wide Power Supply Compatibility 3 V to 5 V**
- **Meets PC99 Desktop Specs (Target)**
- **Low Supply Current**
  - **11 mA Typical at 5 V**
  - **10 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)

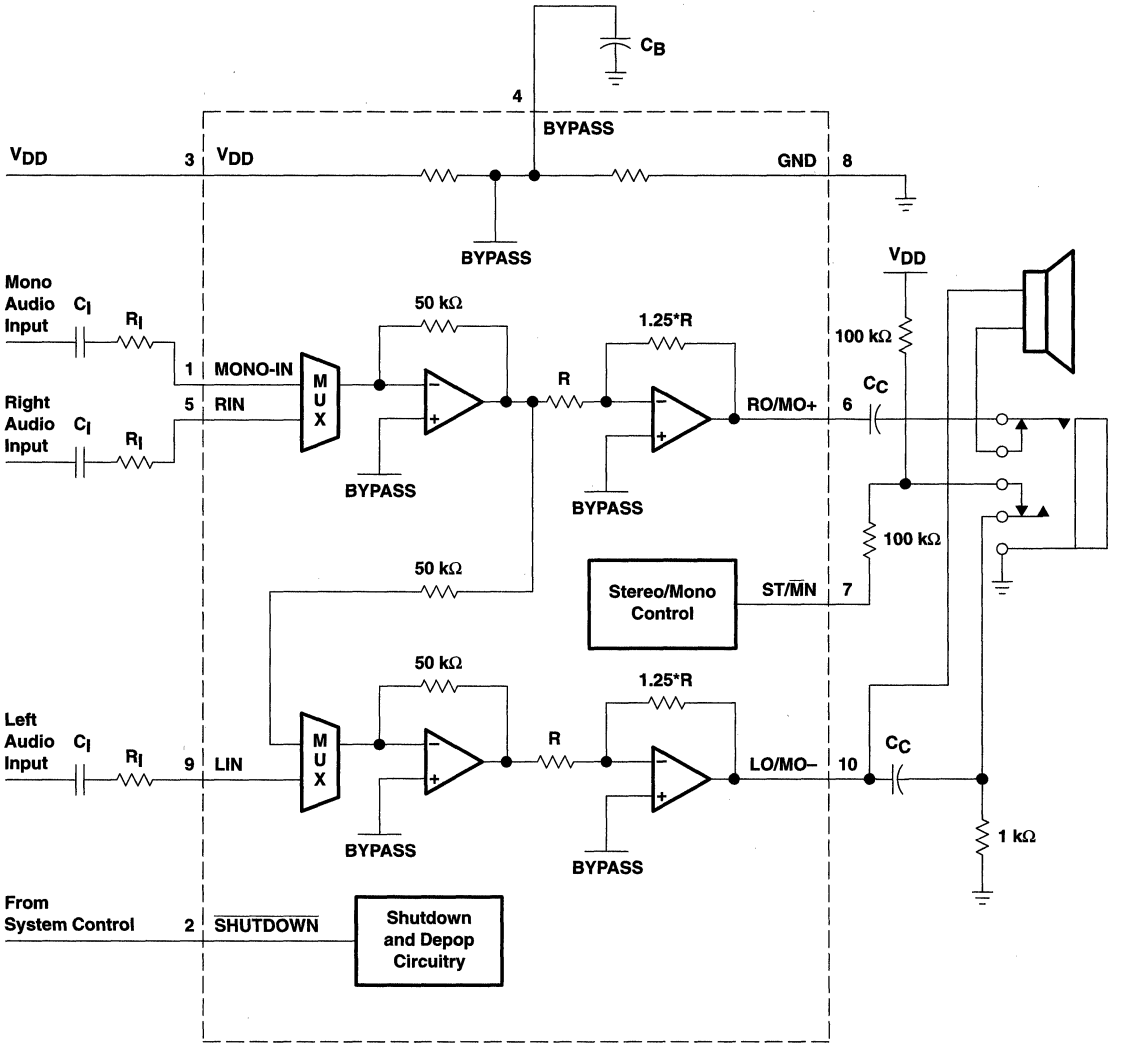


description

The TPA0223 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The amplifier can be reconfigured on-the-fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, Digital Personal Audio players, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0223 can delivery 2-W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0223 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
–40°C to 85°C	TPA0223DGQ	AEI

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0223DGQR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MONO-IN	1	I	Mono input terminal
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
V_{DD}	3	I	V_{DD} is the supply voltage terminal.
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
RIN	5	I	Right-channel input terminal
RO/MO	6	O	Right-output in SE mode and mono positive output in BTL mode
SR/$\overline{\text{MN}}$	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO	10	O	Left-output in SE mode and mono negative output in BTL mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} . . . . . 6 V
Input voltage, V_I . . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			10	13	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			660		mW
		THD = 0.1%,	SE mode,	R_L = 32 Ω		33		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW,	f = 20 Hz to 20 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			11	15	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

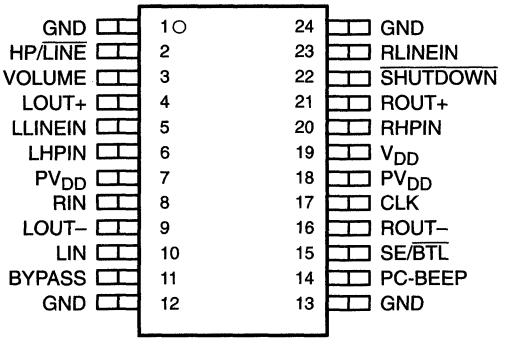
operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			2		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		95		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 2.5,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume Control From +20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0232 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0232 has less than 0.4% THD+N across its specified frequency range.

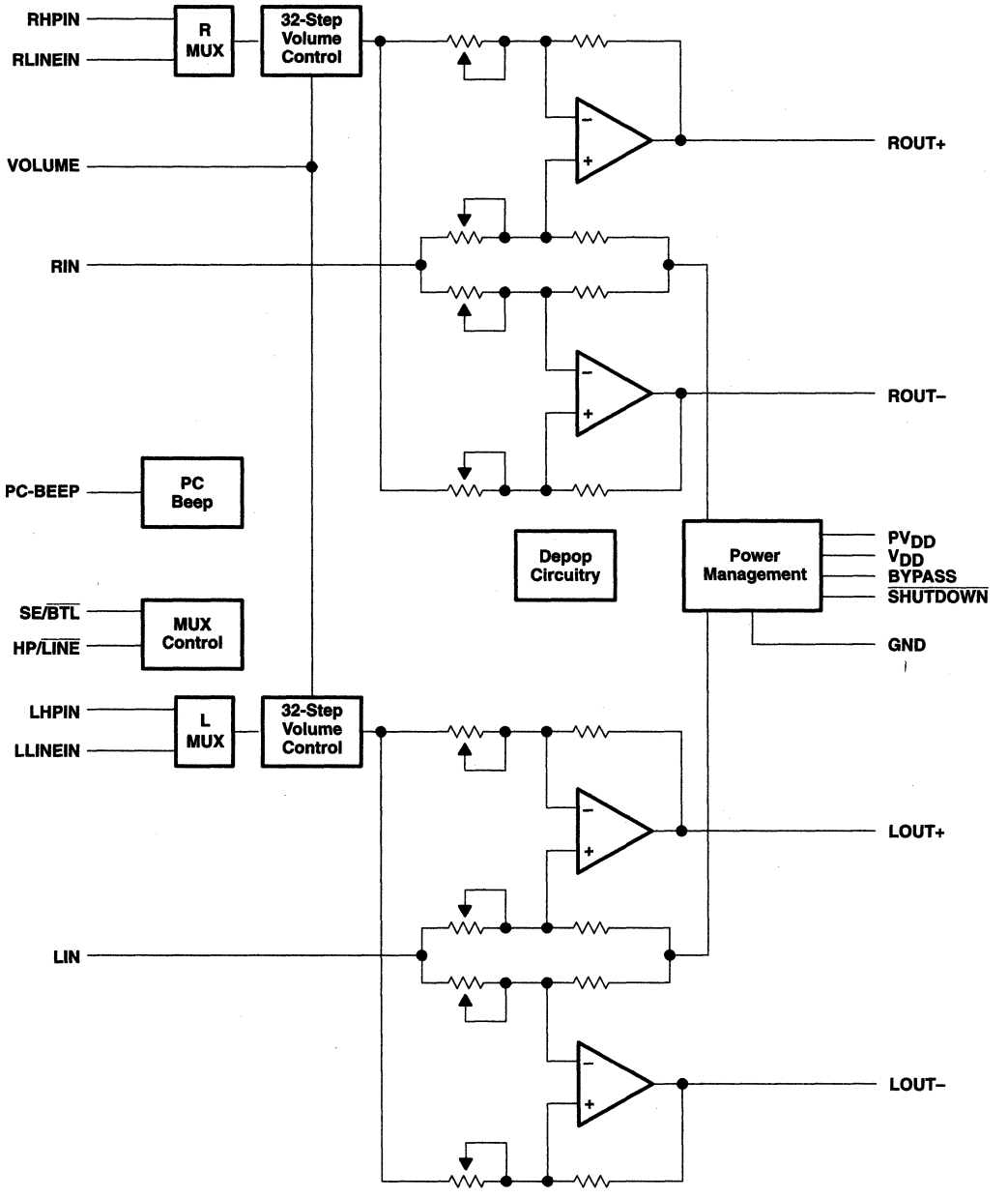
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by means of a dc voltage input on the VOLUME terminal. There are 31 discrete steps covering the range of +20 dB (maximum volume setting) to –40 dB (minimum volume setting) in 2 dB steps. When the VOLUME terminal exceeds 3.54 V, the device is muted. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0232 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this effectively reduces the gain by 6 dB.

The TPA0232 consumes only 10 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0232 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0232PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0232PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0232 generates an internal clock. An external clock can override the internal clock input to this terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad.
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs.
LLINEIN	5	I	Left channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
HP/$\overline{\text{LINE}}$	2	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs.
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	3	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to –40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W§	21.8 mW/°C	1.7 W	1.4 W

§ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{BTL}$, HP/$\overline{LINE}$	4		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{BTL}$, HP/$\overline{LINE}$		3	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2 V/V			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 4 V to 5 V		67		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
Z_I	Input impedance			See Figure 28		
I_{DD}	Supply current	BTL mode		10	15	mA
		SE mode		5	7.5	
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.4%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		34		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

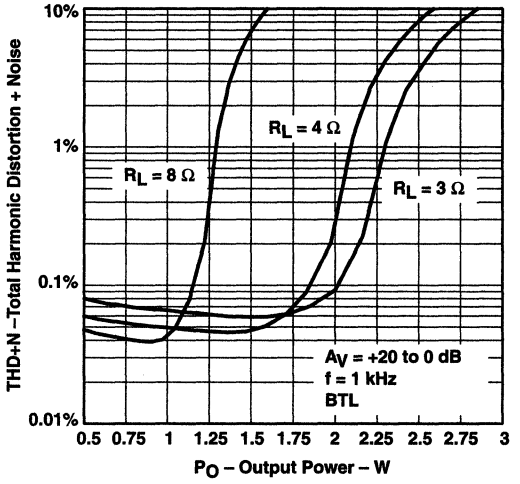


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
VOLTAGE GAIN

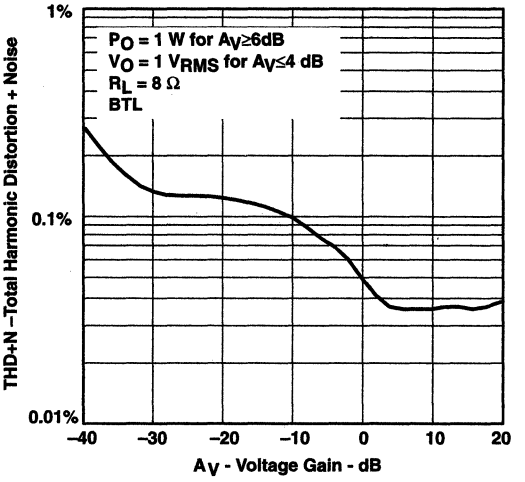


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

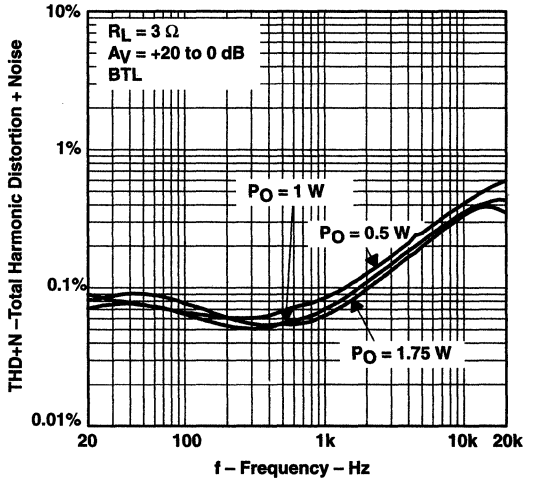


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

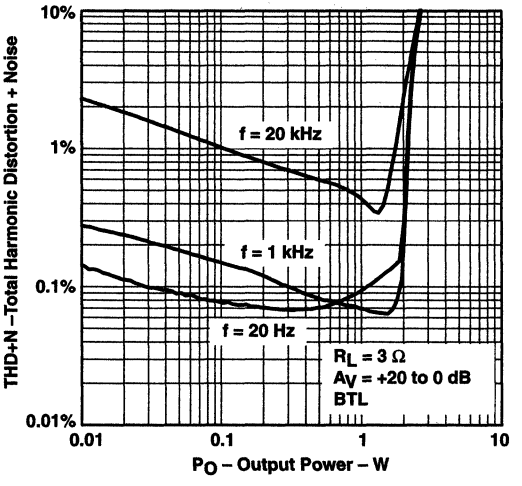


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

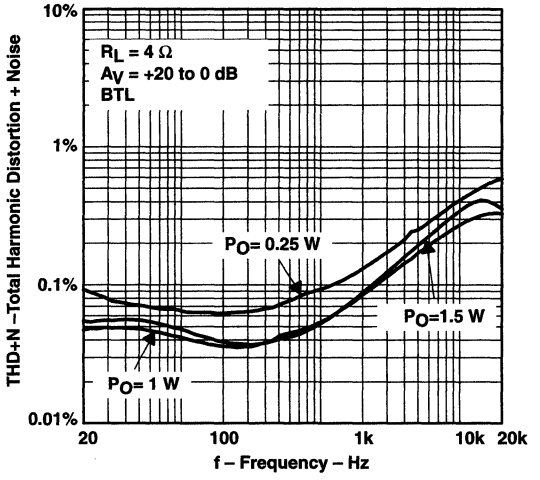


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

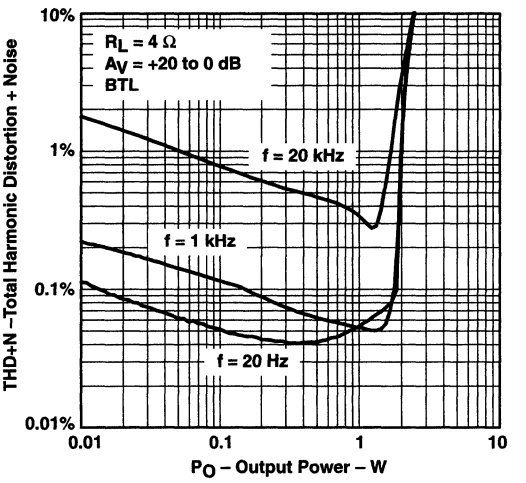


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

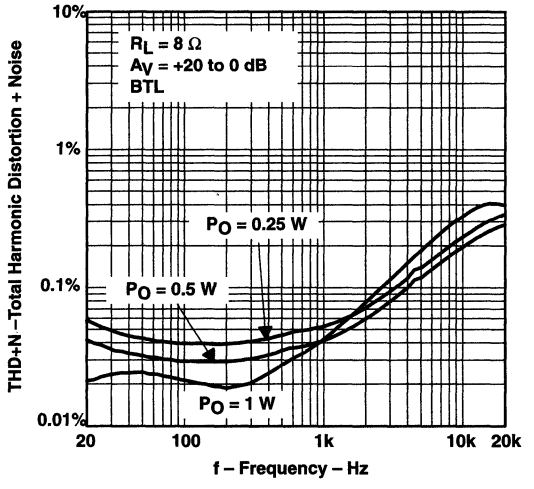


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

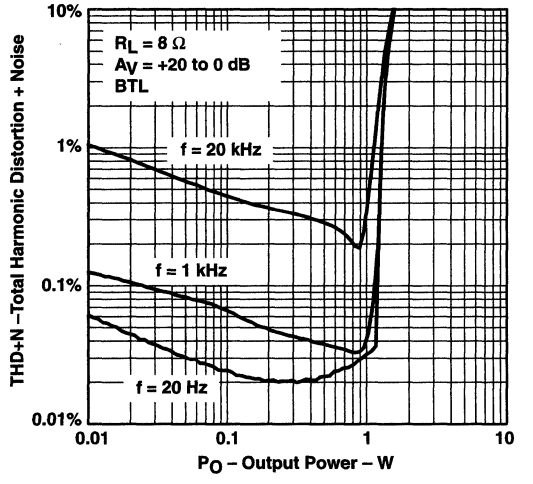


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

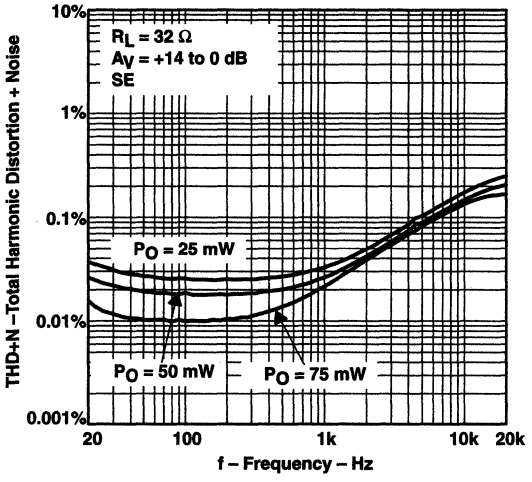


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

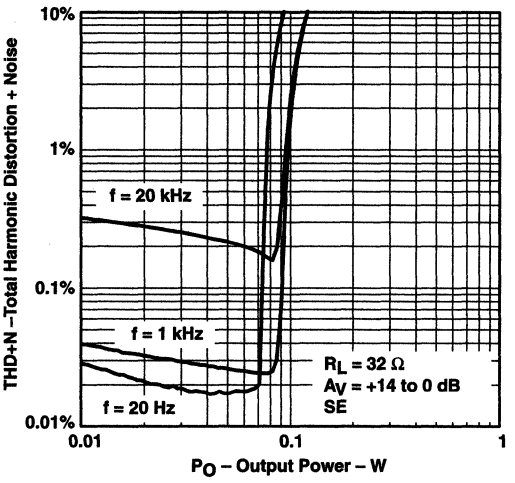


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

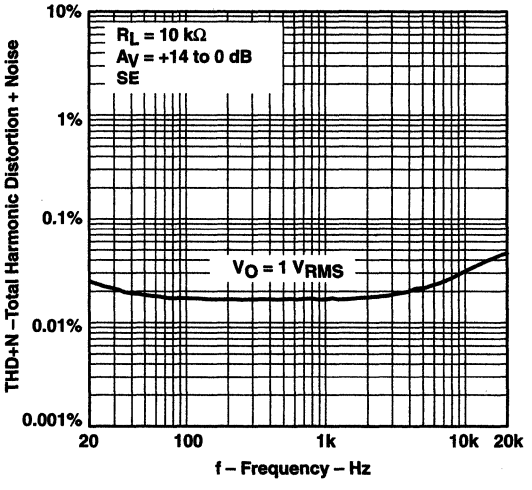


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

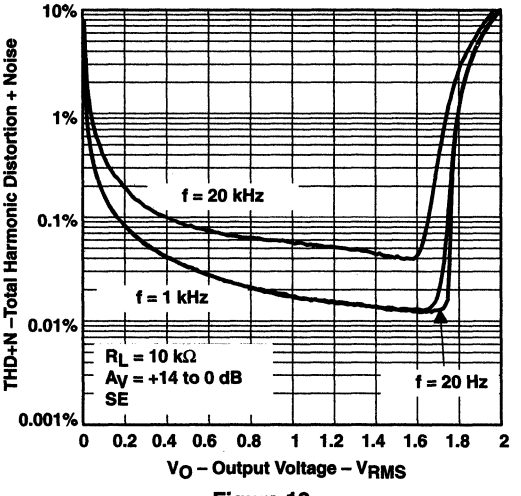


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

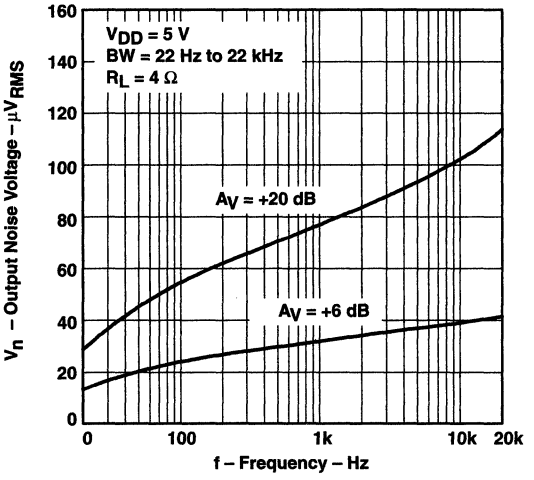


Figure 13

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

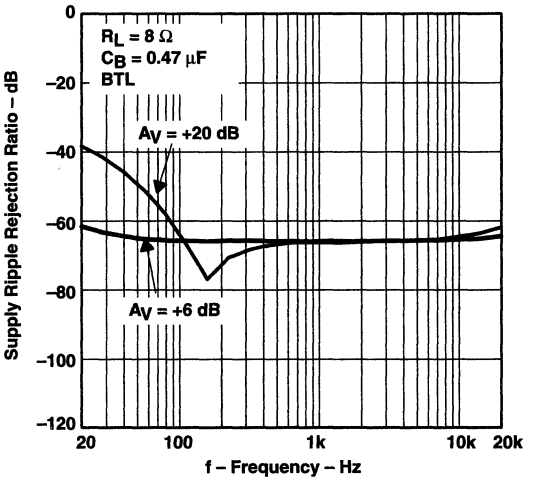


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

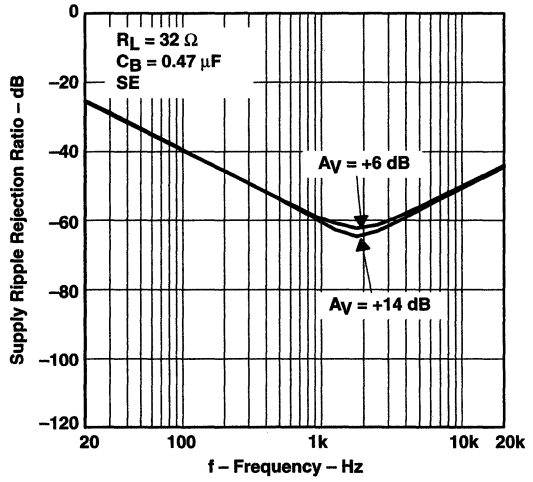


Figure 15

CROSSTALK
vs
FREQUENCY

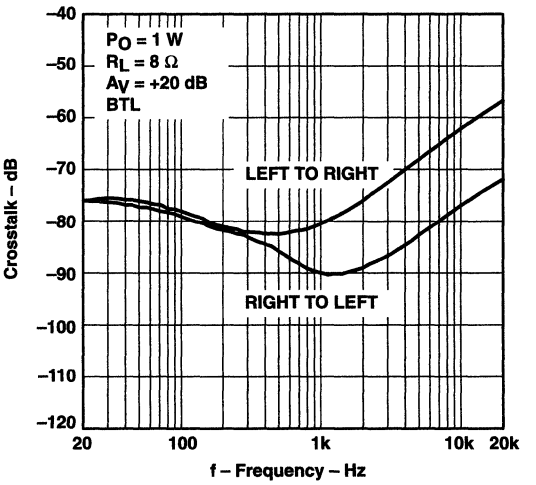


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

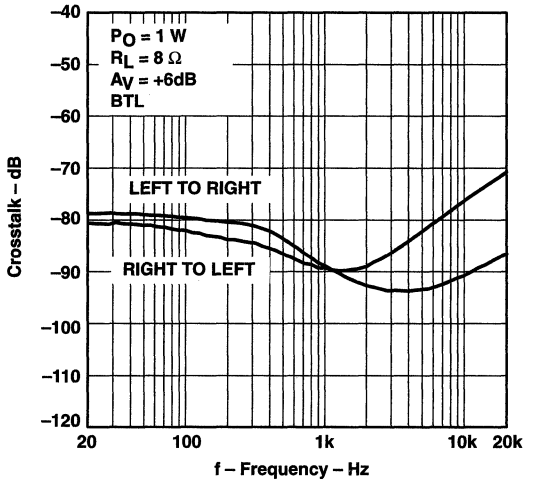


Figure 17

CROSSTALK
vs
FREQUENCY

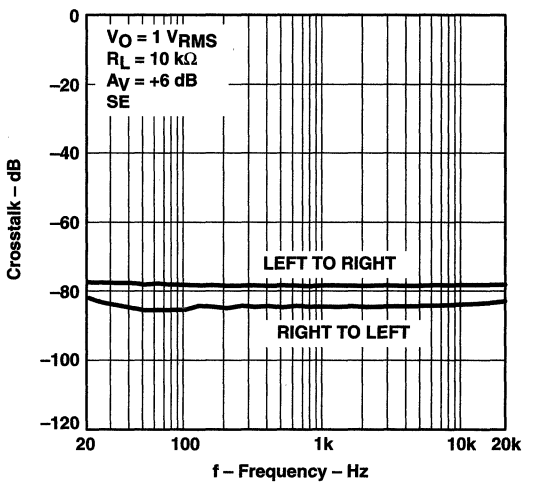


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

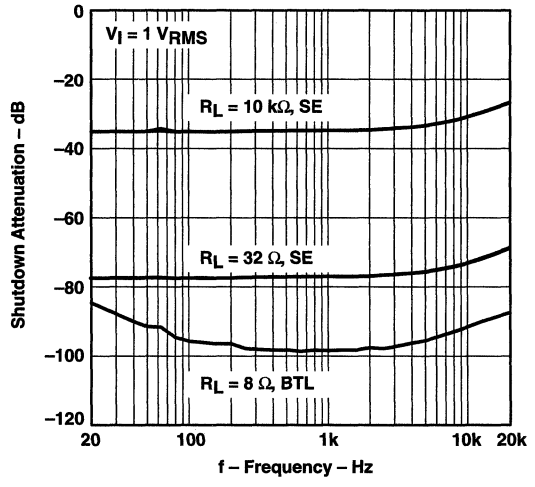


Figure 19

SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

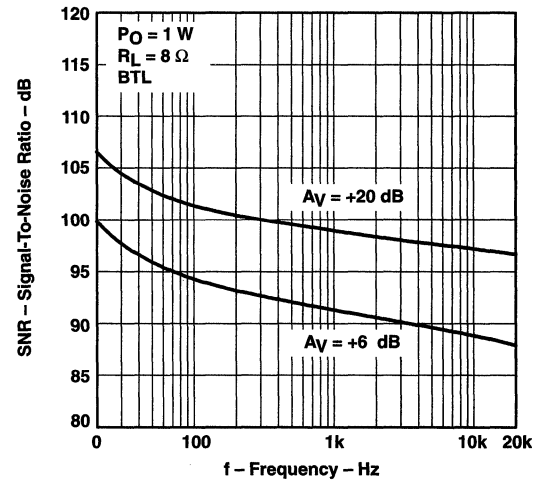


Figure 20

TYPICAL CHARACTERISTICS

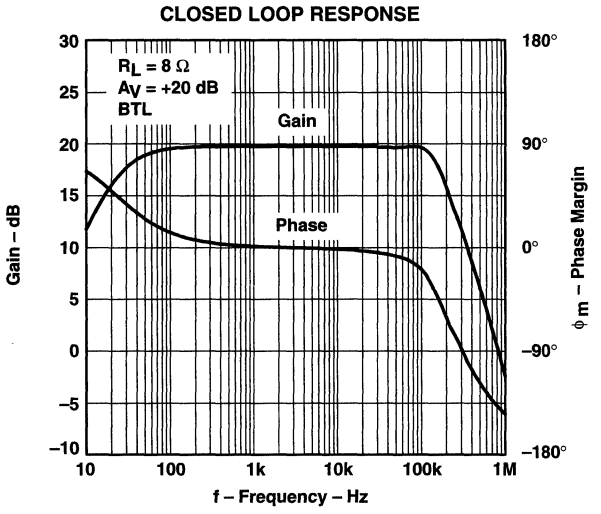


Figure 21

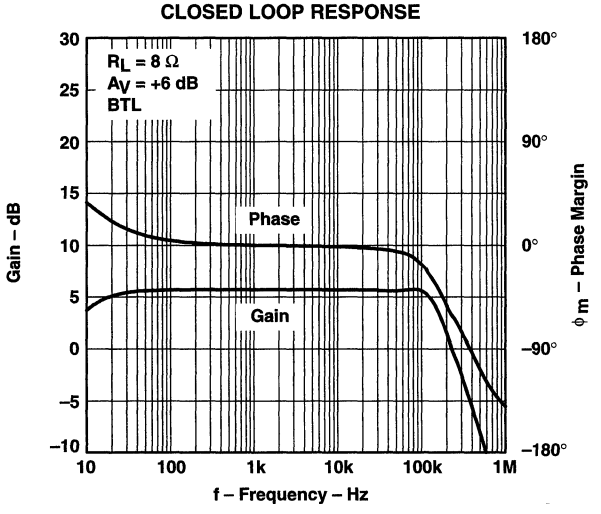


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

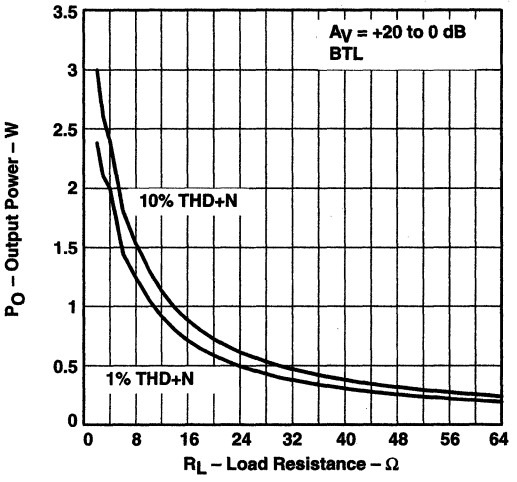


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

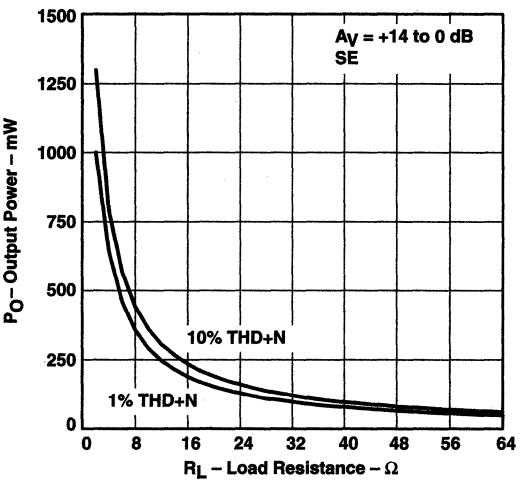


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

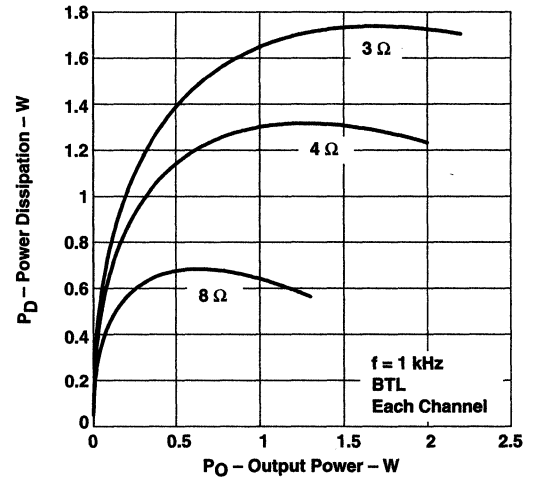


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

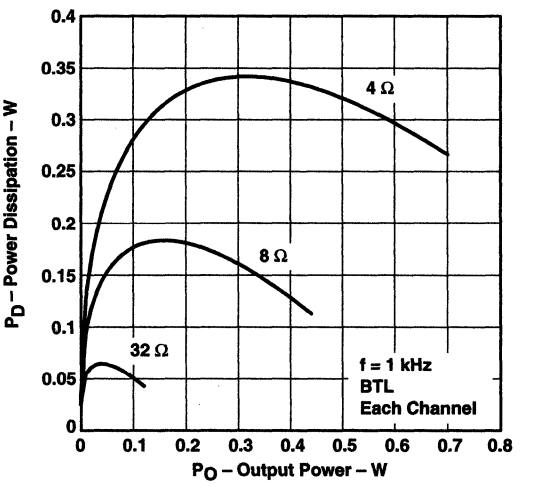


Figure 26

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

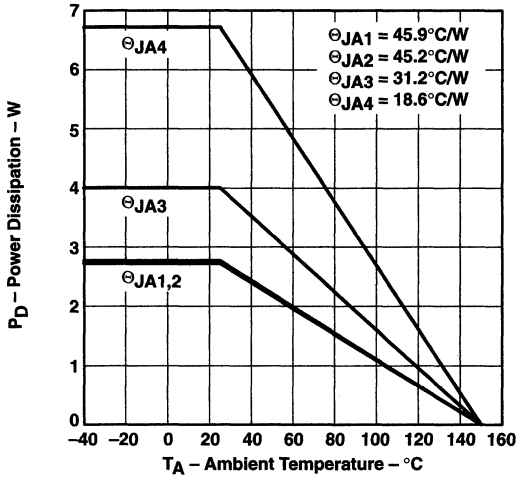


Figure 27

INPUT IMPEDANCE
vs
GAIN

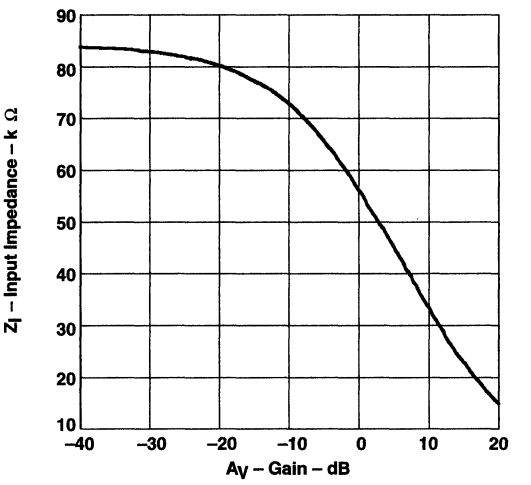


Figure 28

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 29) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

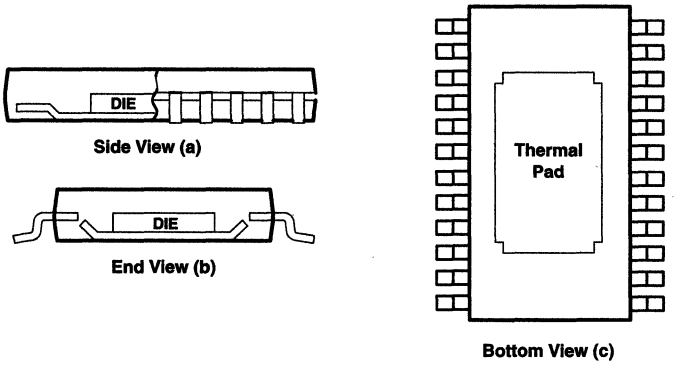


Figure 29. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

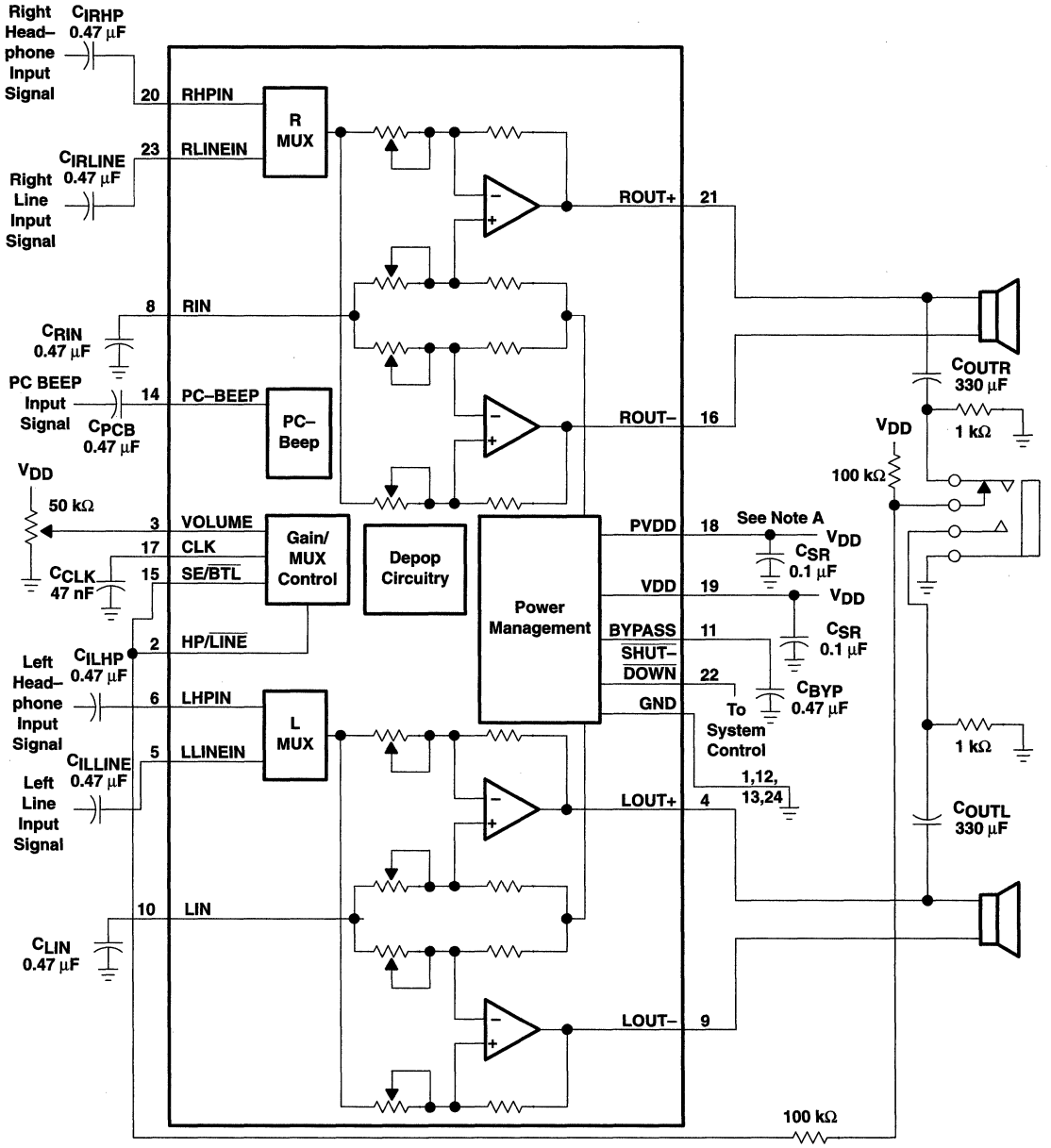
Table 1. DC Volume Control

VOLUME (Terminal 3)		GAIN of AMPLIFIER (dB)
FROM (V)	TO (V)	
0	0.15	20
0.15	0.28	18
0.28	0.39	16
0.39	0.5	14
0.5	0.61	12
0.61	0.73	10
0.73	0.84	8
0.84	0.95	6
0.95	1.06	4
1.06	1.17	2
1.17	1.28	0
1.28	1.39	−2
1.39	1.5	−4
1.5	1.62	−6
1.62	1.73	−8
1.73	1.84	−10
1.84	1.95	−12
1.95	2.07	−14
2.07	2.18	−16
2.18	2.29	−18
2.29	2.41	−20
2.41	2.52	−22
2.52	2.63	−24
2.63	2.74	−26
2.74	2.86	−28
2.86	2.97	−30
2.97	3.08	−32
3.08	3.2	−34
3.2	3.31	−36
3.31	3.42	−38
3.42	3.54	−40
3.54	5	−85

selection of components

Figure 30 and Figure 31 are schematic diagrams of typical notebook computer application circuits.

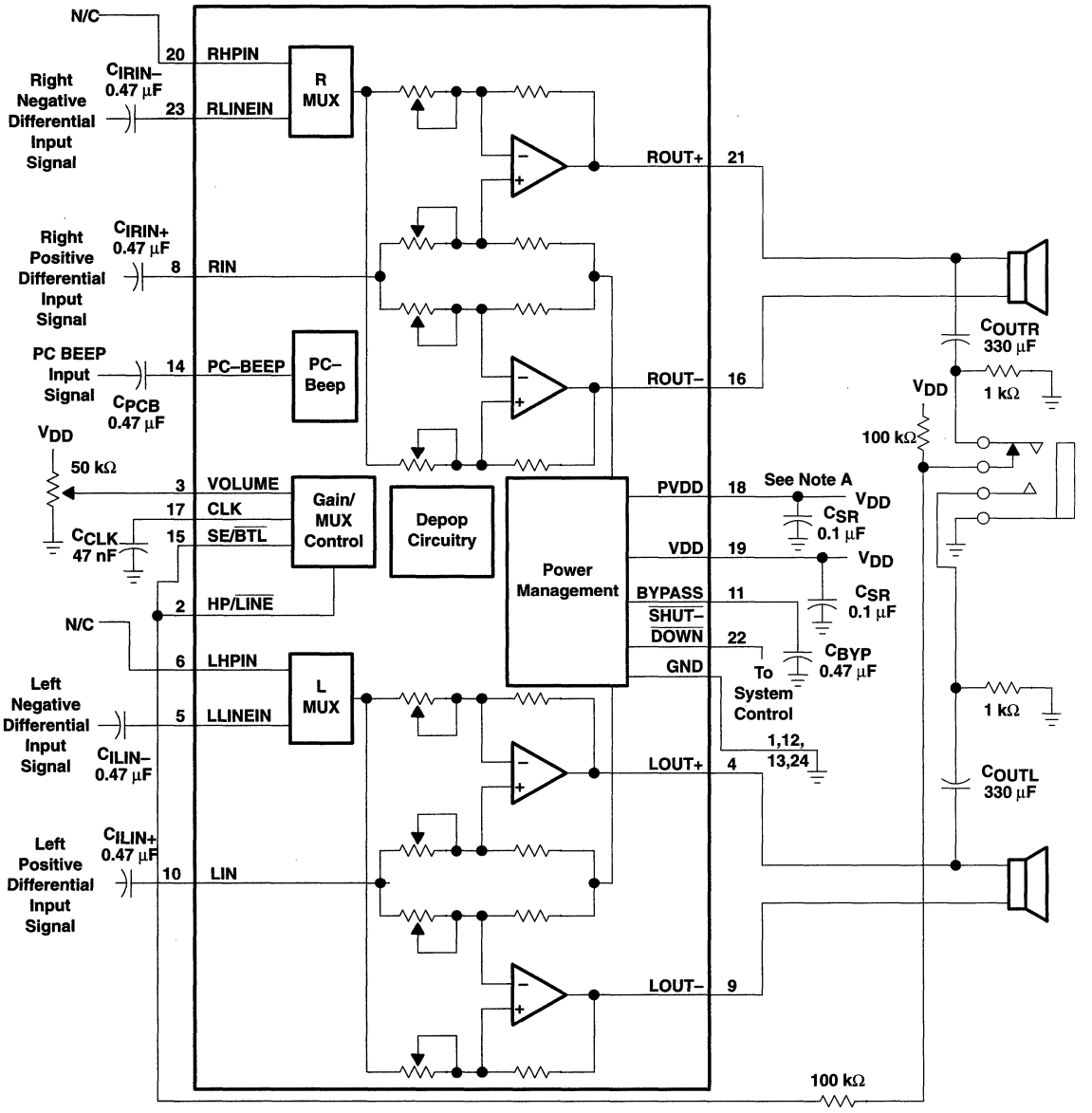
APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0232 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0232 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.

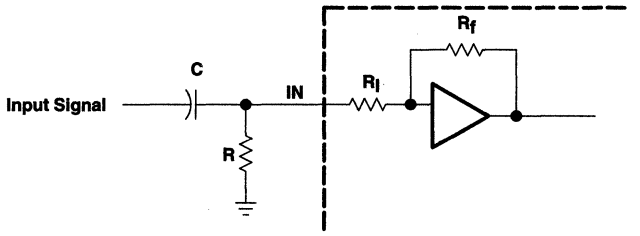


Figure 32. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 28.

The –3 dB frequency can be calculated using the following formula:

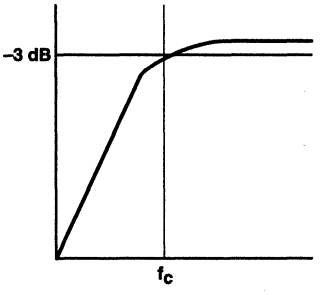
$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_{IN} C_I} \quad (2)$$



APPLICATION INFORMATION

input capacitor, C_I (continued)

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0232 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

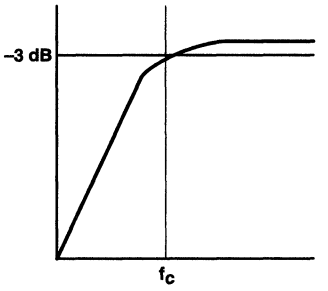
Bypass capacitor, C_{BYP}, values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 33 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0232 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

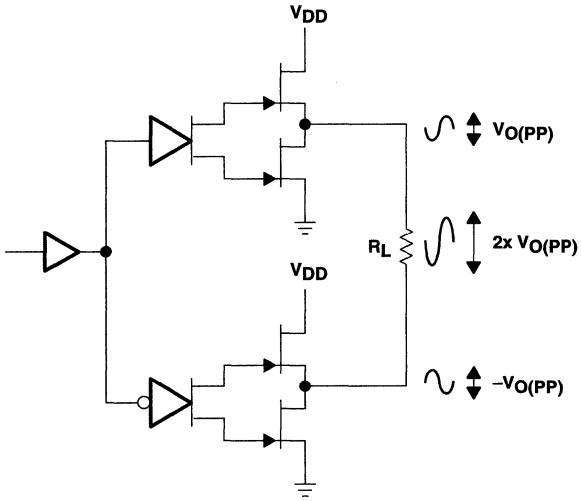


Figure 33. Bridge-Tied Load Configuration

APPLICATION INFORMATION

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 34. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \quad (6)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

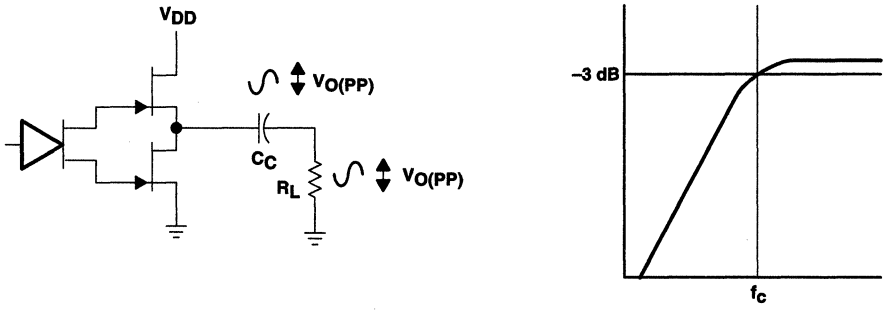


Figure 34. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 33 and Figure 34), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain by 6 dB.

input MUX operation

The input MUX allows two separate inputs to be applied to the amplifier. This allows the designer to choose which input is active independent of the state of the SE/$\overline{\text{BTL}}$ terminal. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs are active.

APPLICATION INFORMATION

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 35).

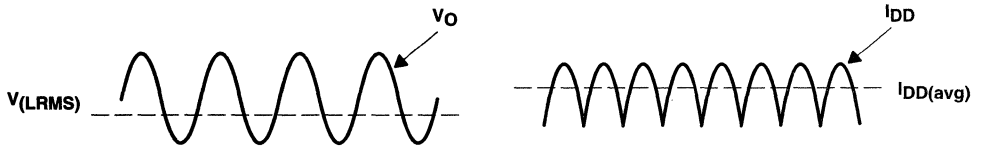


Figure 35. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L\text{rms}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

and $P_{SUP} = V_{DD}\, I_{DD}\text{avg}$ and $I_{DD}\text{avg} = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$

Therefore,

$$P_{SUP} = \frac{2 V_{DD} V_P}{\pi R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2R_L}}{\frac{2 V_{DD} V_P}{\pi R_L}} = \frac{\pi V_P}{4 V_{DD}}$$

Where:

$$V_P = \sqrt{2 P_L R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
I_{DD}avg = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

APPLICATION INFORMATION

Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA0232 data sheet, one can see that when the TPA0232 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\ W}{1\ W} = 6\ dB \qquad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

APPLICATION INFORMATION

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

$$= 63 \text{ mW (18 dB crest factor)}$$

$$= 125 \text{ mW (15 dB crest factor)}$$

$$= 250 \text{ mW (9 dB crest factor)}$$

$$= 500 \text{ mW (6 dB crest factor)}$$

$$= 1000 \text{ mW (3 dB crest factor)}$$

$$= 2000 \text{ mW (15 dB crest factor)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0232 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0232 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 5. TPA0232 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

APPLICATION INFORMATION

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (12)$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0232 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:
Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0232 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0232 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0232, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0232 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0232 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 36.

APPLICATION INFORMATION

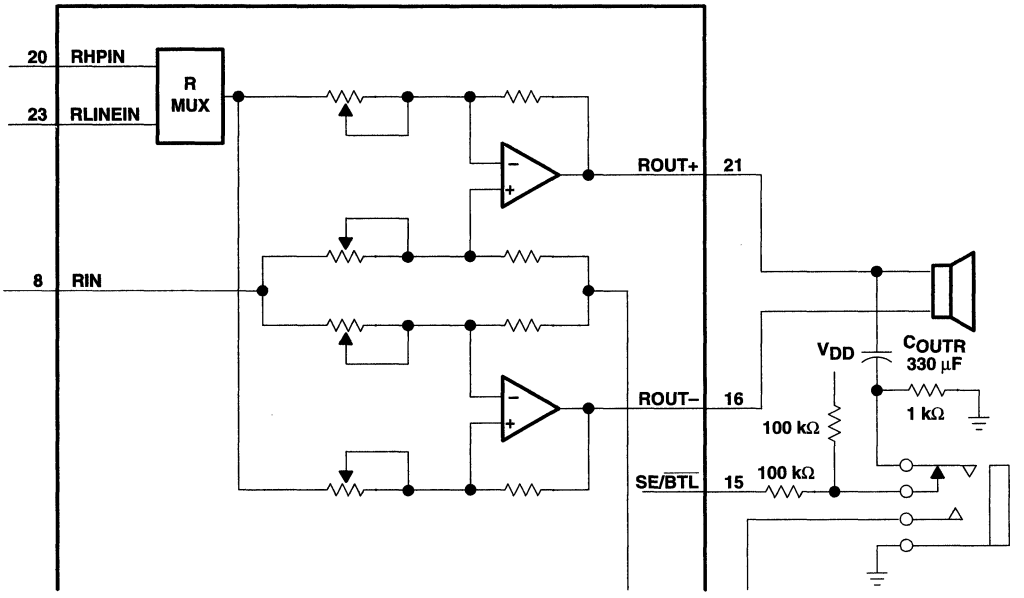


Figure 36. TPA0232 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is normally activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

APPLICATION INFORMATION

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

shutdown modes

The TPA0232 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{SHUTDOWN}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SHUTDOWN}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 μA. $\overline{SHUTDOWN}$ should never be left unconnected because amplifier operation would be unpredictable.

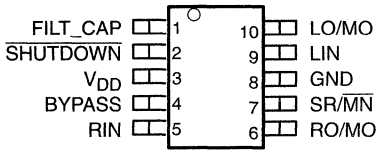
Table 6. HP/$\overline{LINE}$, SE/$\overline{BTL}$, and Shutdown Functions

INPUTS†			AMPLIFIER STATE	
HP/$\overline{LINE}$	SE/$\overline{BTL}$	$\overline{SHUTDOWN}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4-Ω From 5-V Supply**
- **0.6 W Into 4-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Mono (BTL) Signal Created by Summing Left and Right Signals**
- **Wide Power Supply Compatibility 3 V to 5 V**
- **3 V to 5 V**
- **Meets PC99 Portable Specs (target)**
- **Low Supply Current**
  - **4 mA Typical at 5 V**
  - **3.3 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)

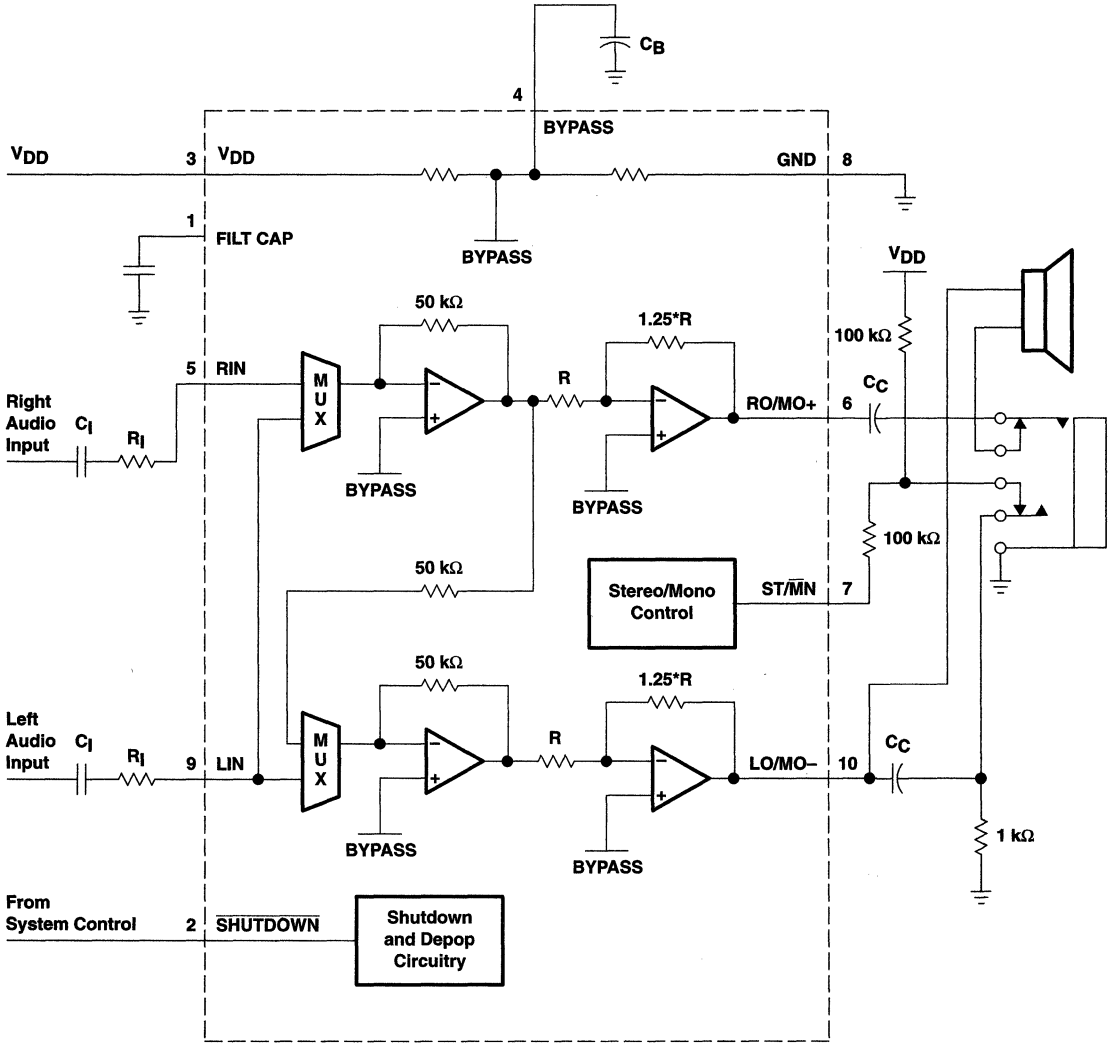


description

The TPA0233 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The mono signal is created by summing left and right inputs. The amplifier can be reconfigured on-the-fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0233 can delivery 2-W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0233 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
–40°C to 85°C	TPA0233DGQ	AEJ

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0233DGQR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
MONO-IN	1	I	Mono input terminal
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
V_{DD}	3	I	V_{DD} is the supply voltage terminal.
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
RIN	5	I	Right-channel input terminal
RO/MO	6	O	Right-output in SE mode and mono positive output in BTL mode
SR/$\overline{\text{MN}}$	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO	10	O	Left-output in SE mode and mono negative output in BTL mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			3.3	4.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			660		mW
		THD = 0.1%,	SE mode,	R_L = 32 Ω		33		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW,	f = 20 Hz to 20 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO}\rvert$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			4	5	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

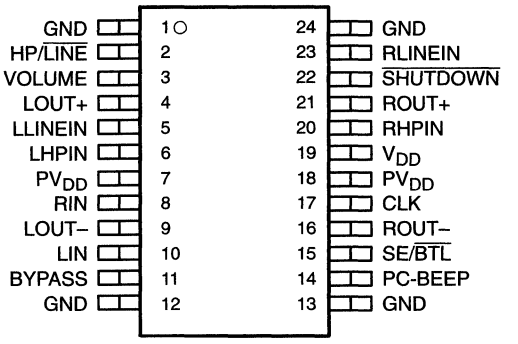
operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			2		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		92		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 2.5,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume Control From 20 dB to –40 dB**
- **2-W/Ch Output Power Into 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



description

The TPA0242 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-Ω loads. This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0242 has less than 0.22% THD+N across its specified frequency range.

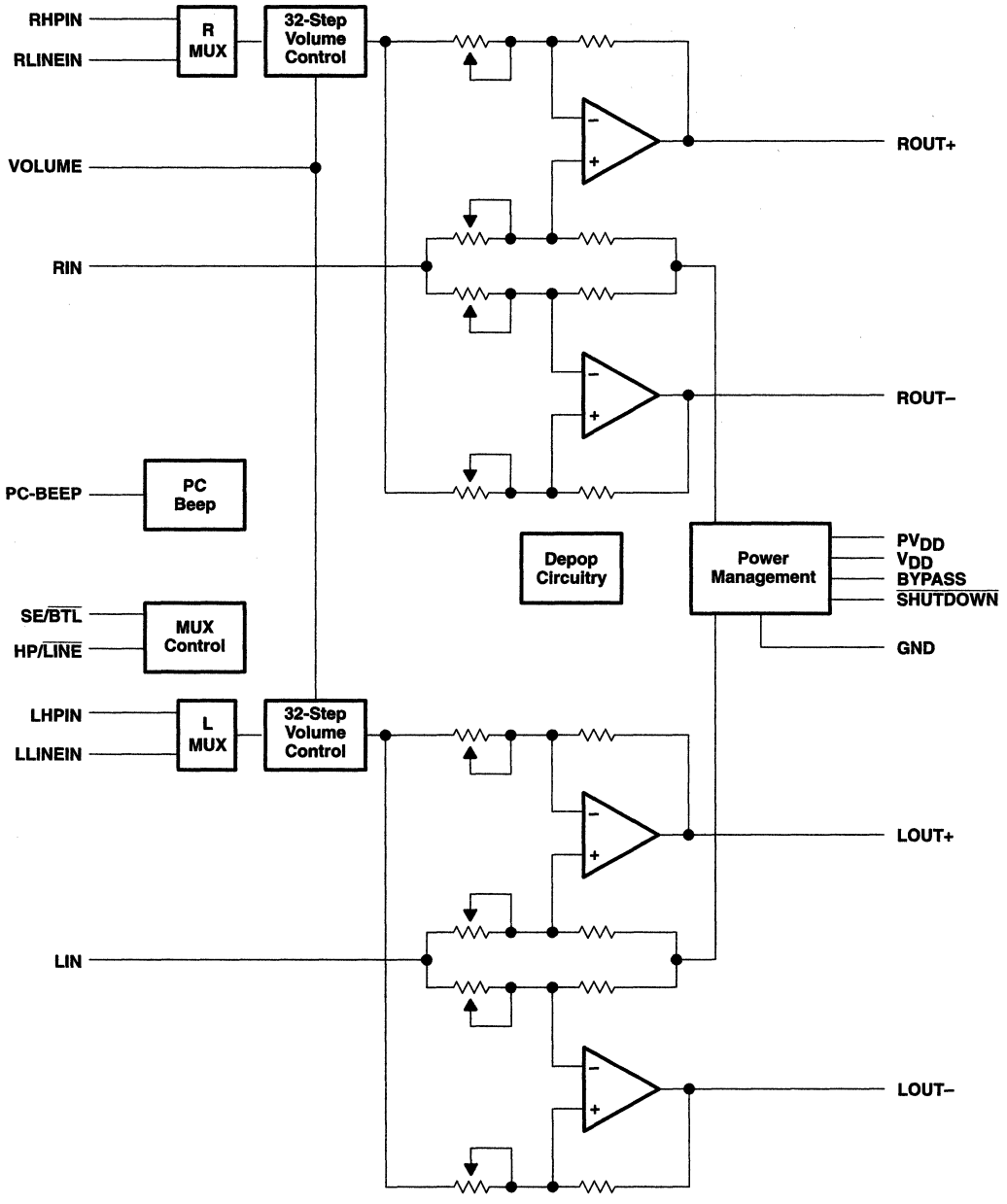
Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by a dc voltage input on the VOLUME terminal. There are 31 discrete steps covering the range of 20 dB (maximum volume setting) to –40 dB (minimum volume setting) in 2 dB steps. When the VOLUME terminal exceeds 3.54 V, the device is muted. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0242 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this effectively reduces the gain by 6 dB.

The TPA0242 consumes only 20 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0242 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	TSSOP† (PWP)
–40°C to 85°C	TPA0242PWP

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0242PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0242 generates an internal clock. An external clock can override the internal clock input to this terminal.
GND	1, 12 13, 24		Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
LOUT–	9	O	Left channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
HP/$\overline{\text{LINE}}$	2	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PC-BEEP	14	I	The input for PC Beep mode. PC-BEEP is enabled when a > 1-V (peak-to-peak) square wave is input to PC-BEEP.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
ROUT–	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	3	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to –40 dB for dc levels of 0.15 V to 3.54. When the dc level is over 3.54 V, the device is muted.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W‡	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$	4		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		3	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage (measured differentially)	V_I = 0, A_V = 2 V/V			25	mV
	Supply ripple rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\lvert I_{IH}\rvert$	High-level input current	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL}\rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode		20		mA
		SE mode		10		
$I_{DD(SD)}$	Supply current, shutdown mode			150	300	µA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω, Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 1%,	f = 1 kHz		2		W
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 15 kHz		0.22%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	C_B = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		34		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Voltage gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Bandwidth	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Bandwidth	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

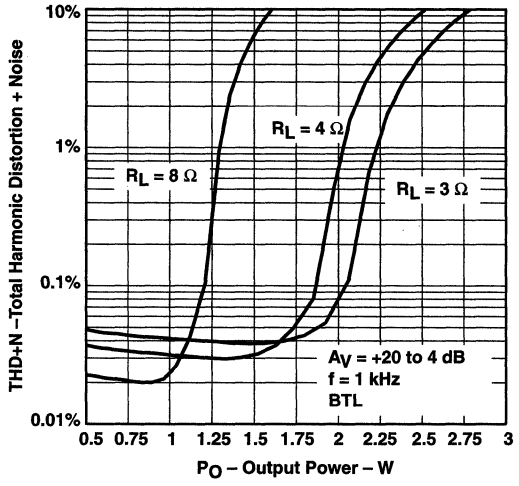


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
VOLTAGE GAIN

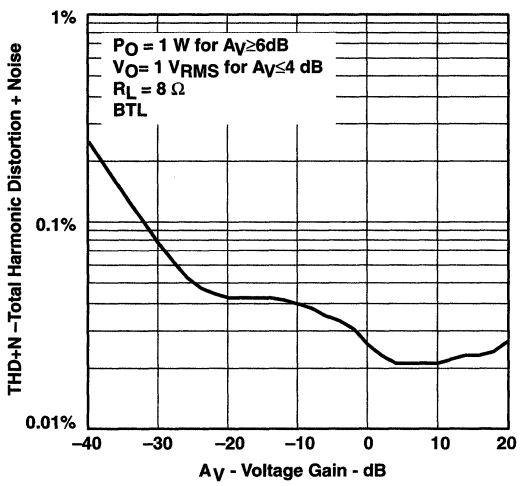


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

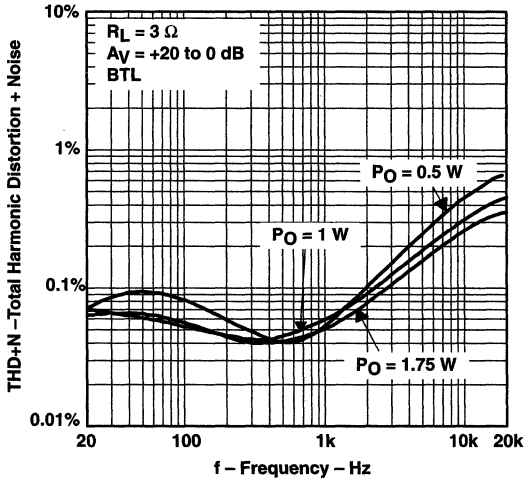


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

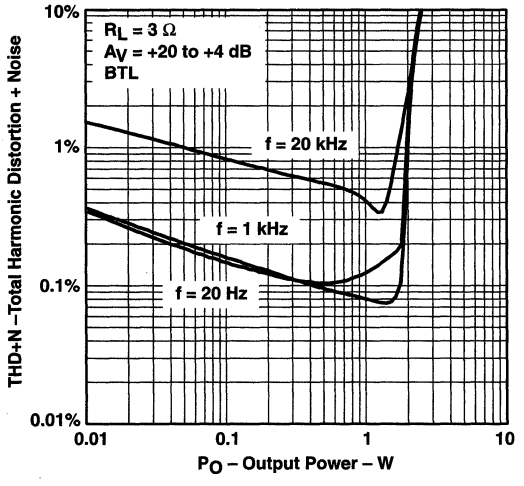


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

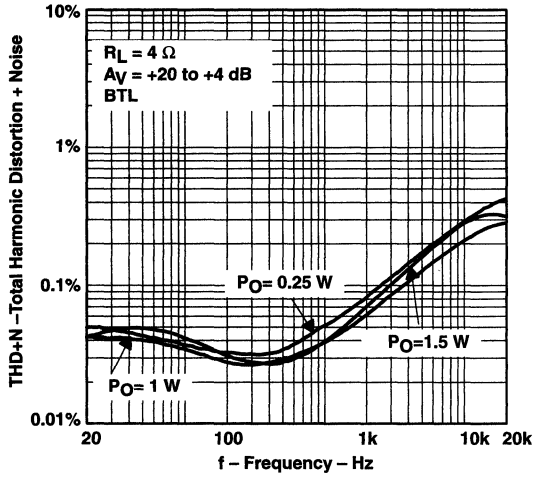


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

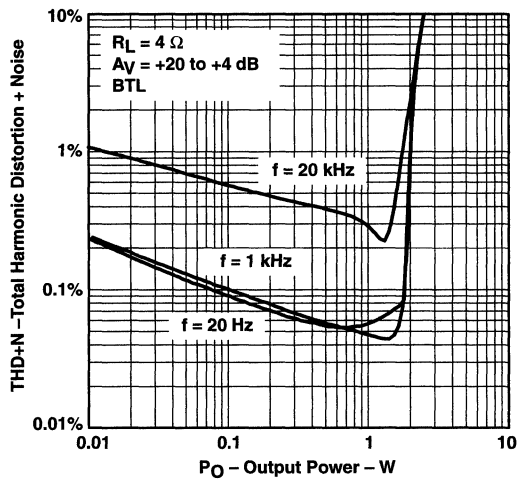


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

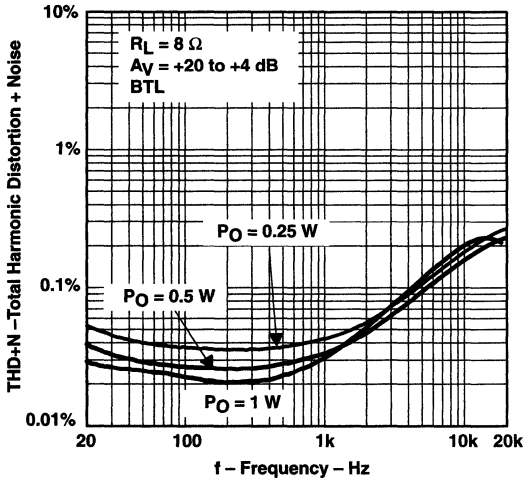


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

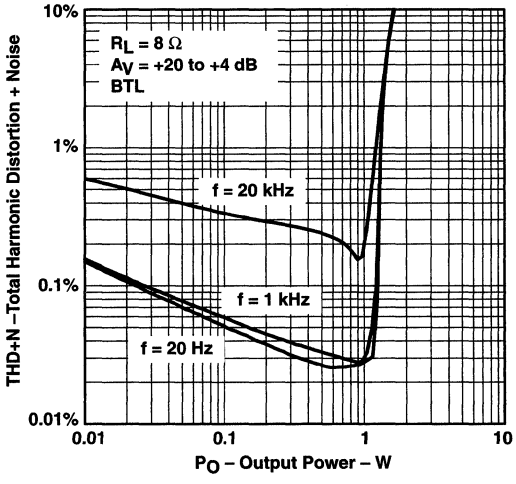


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

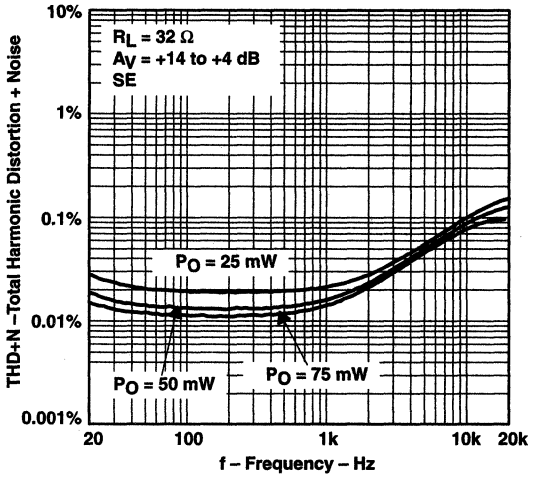


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

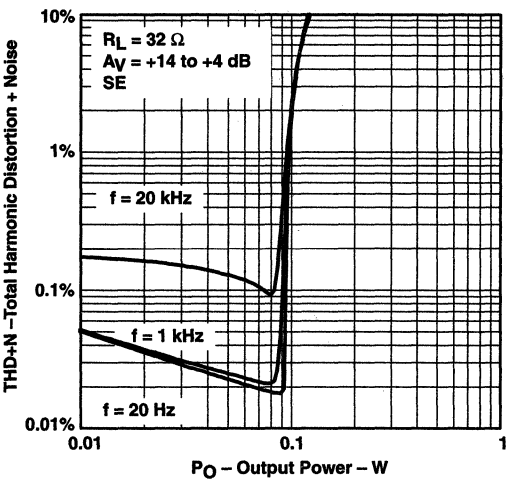


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

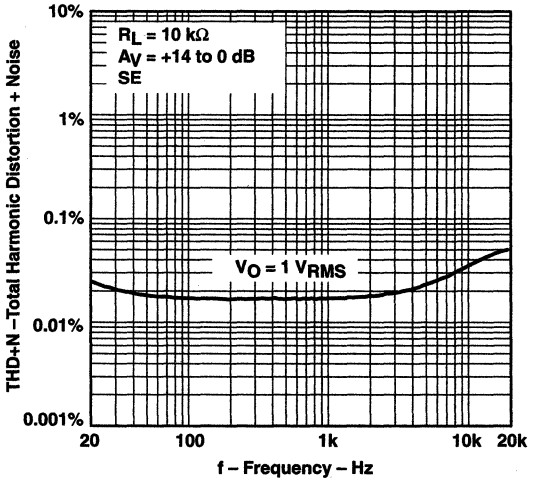


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

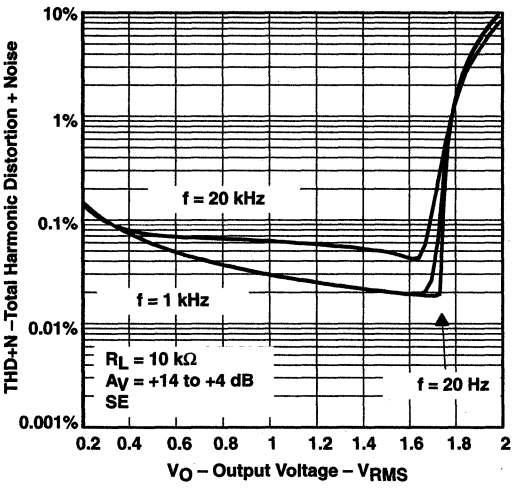


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

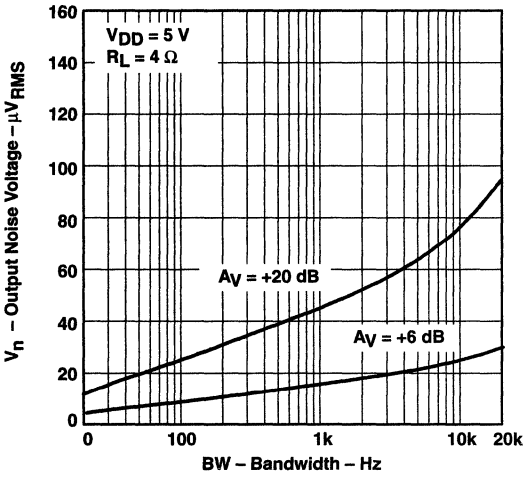


Figure 13

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

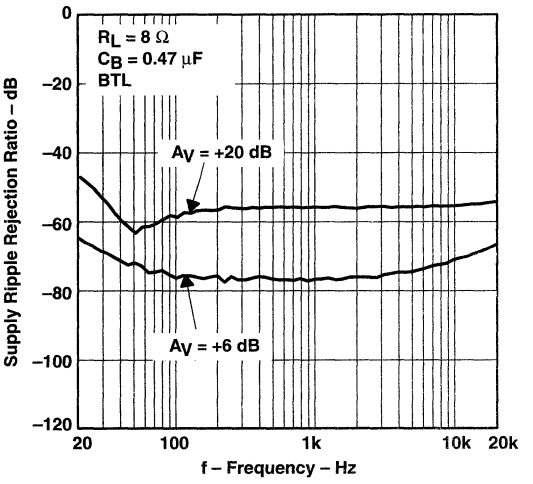


Figure 14

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

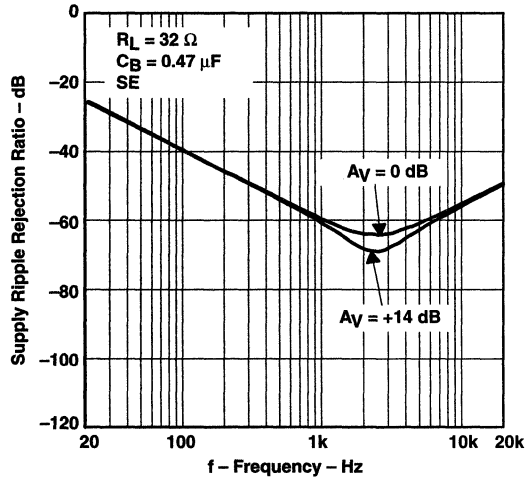


Figure 15

CROSSTALK
vs
FREQUENCY

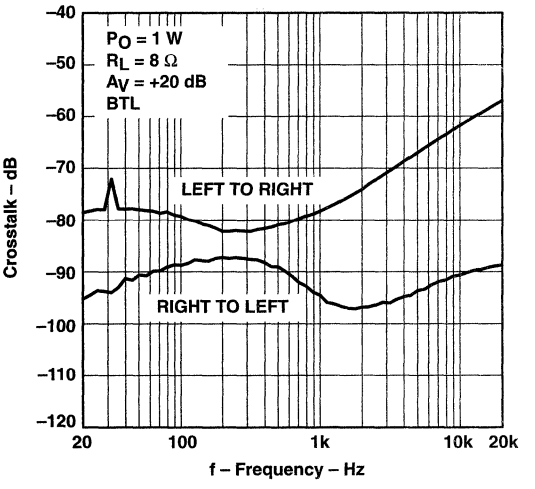


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

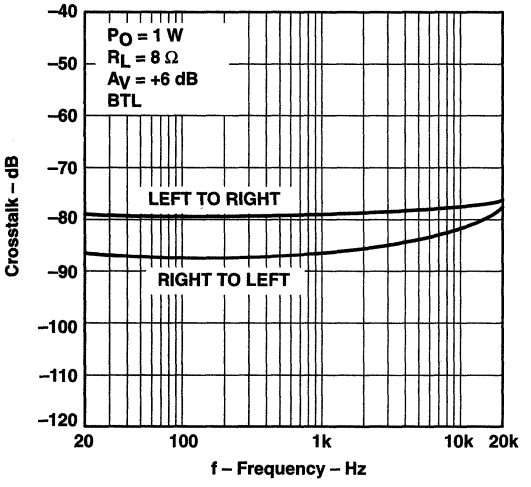


Figure 17

CROSSTALK
vs
FREQUENCY

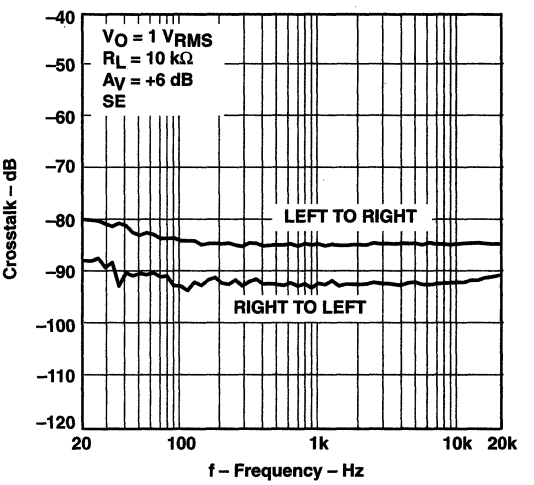


Figure 18

SHUTDOWN ATTENUATION
vs
FREQUENCY

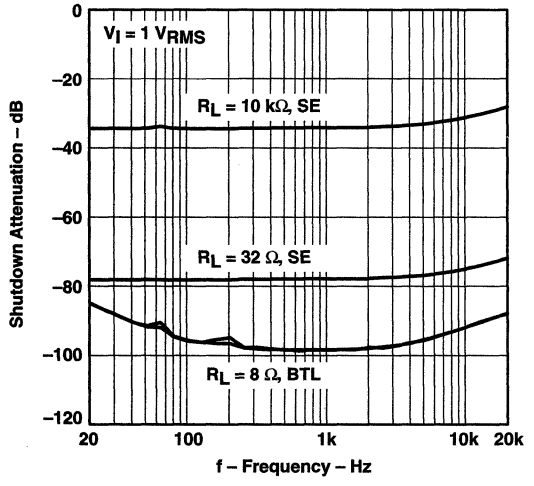


Figure 19

SIGNAL-TO-NOISE RATIO
vs
BANDWIDTH

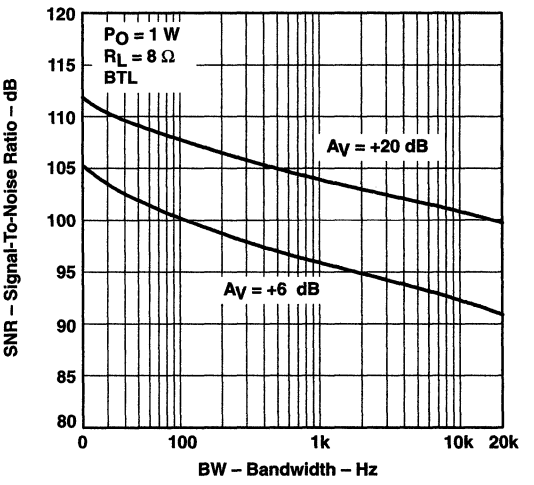


Figure 20

TYPICAL CHARACTERISTICS

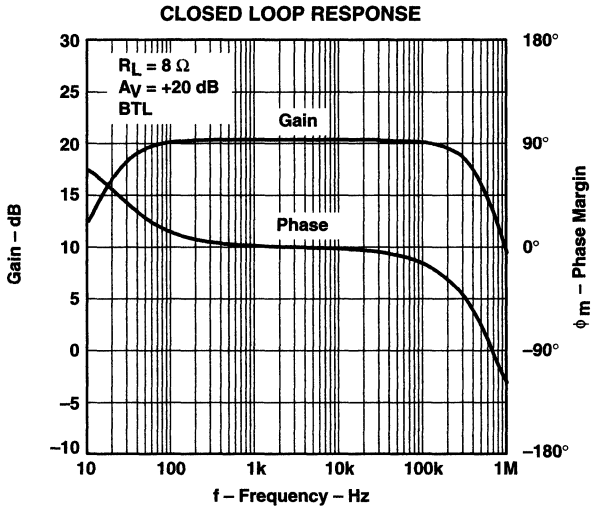


Figure 21

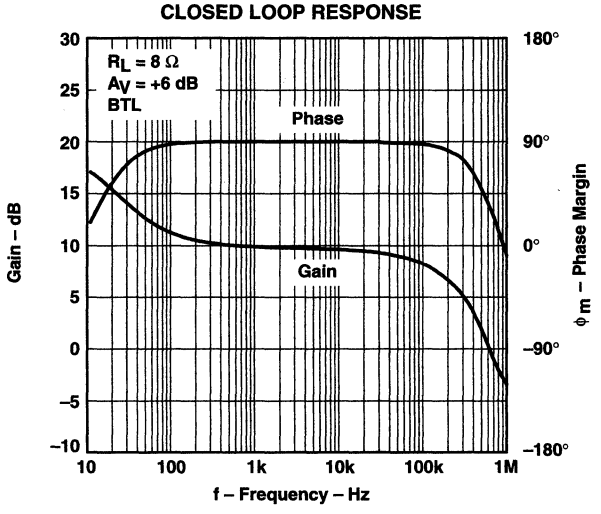


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
LOAD RESISTANCE

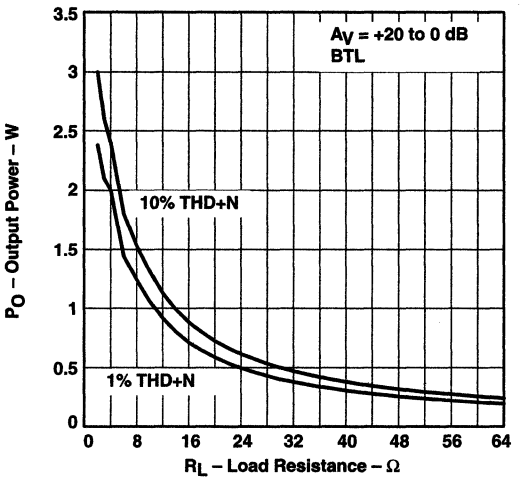


Figure 23

OUTPUT POWER
vs
LOAD RESISTANCE

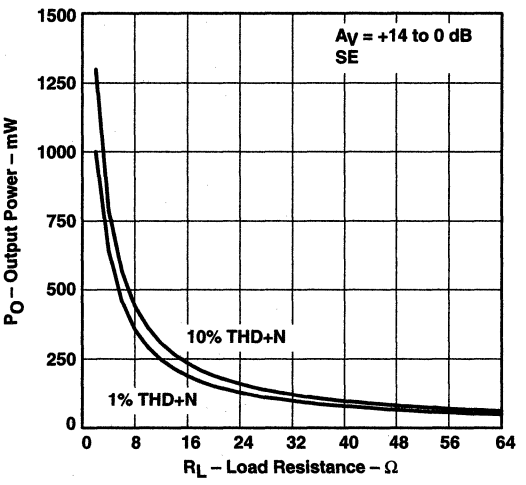


Figure 24

POWER DISSIPATION
vs
OUTPUT POWER

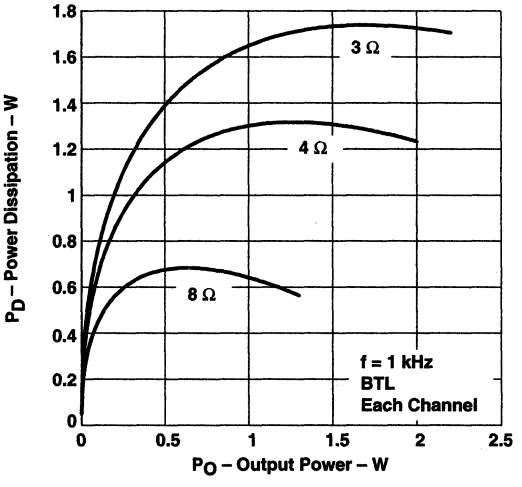


Figure 25

POWER DISSIPATION
vs
OUTPUT POWER

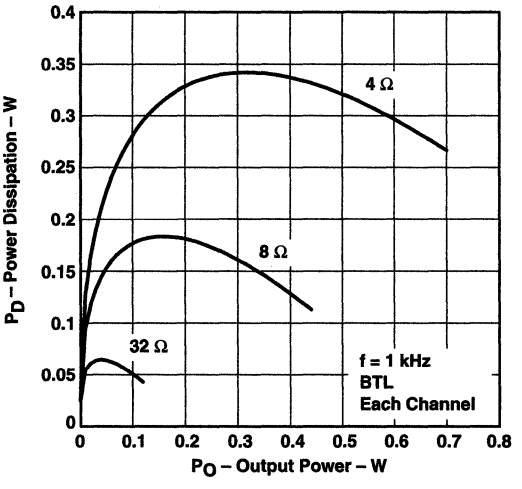


Figure 26

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
AMBIENT TEMPERATURE

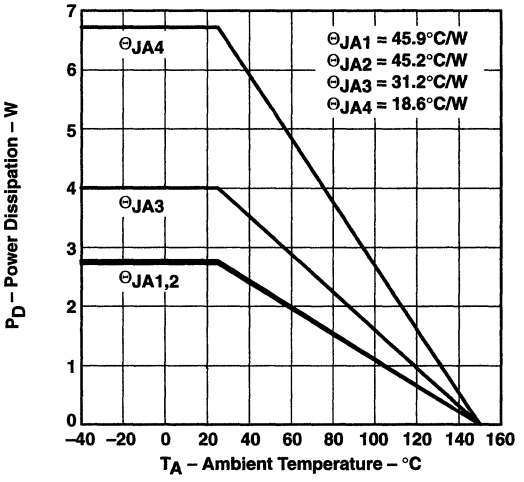


Figure 27

INPUT IMPEDANCE
vs
GAIN

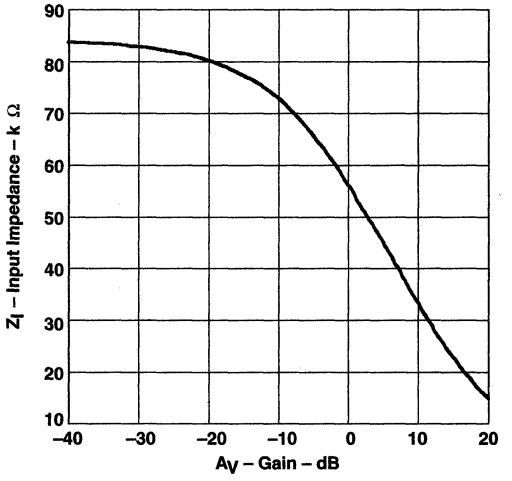


Figure 28

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 29) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

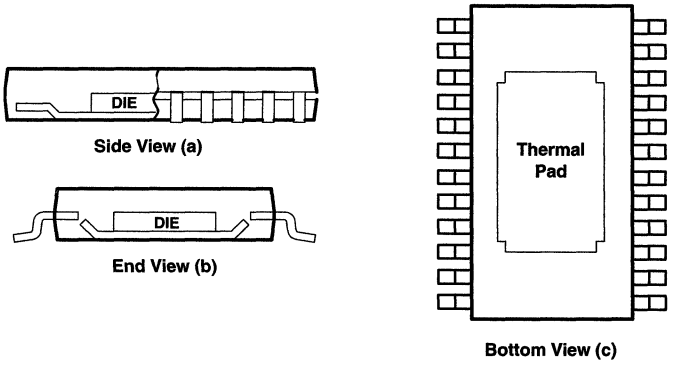


Figure 29. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

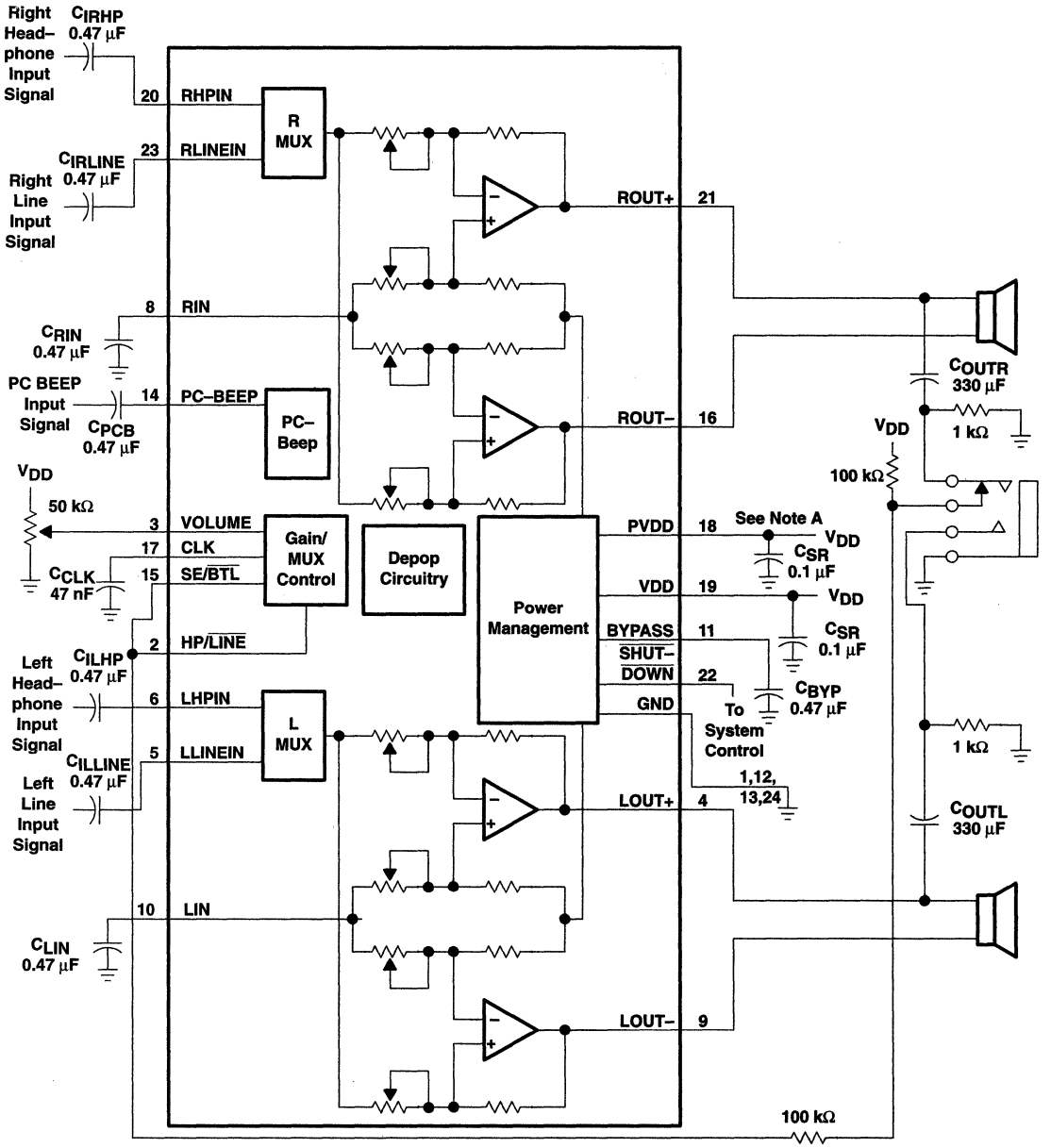
Table 1. DC Volume Control

VOLUME (Terminal 3)		GAIN of AMPLIFIER (dB)
FROM (V)	TO (V)	
0	0.15	20
0.15	0.28	18
0.28	0.39	16
0.39	0.5	14
0.5	0.61	12
0.61	0.73	10
0.73	0.84	8
0.84	0.95	6
0.95	1.06	4
1.06	1.17	2
1.17	1.28	0
1.28	1.39	−2
1.39	1.5	−4
1.5	1.62	−6
1.62	1.73	−8
1.73	1.84	−10
1.84	1.95	−12
1.95	2.07	−14
2.07	2.18	−16
2.18	2.29	−18
2.29	2.41	−20
2.41	2.52	−22
2.52	2.63	−24
2.63	2.74	−26
2.74	2.86	−28
2.86	2.97	−30
2.97	3.08	−32
3.08	3.2	−34
3.2	3.31	−36
3.31	3.42	−38
3.42	3.54	−40
3.54	5	−85

selection of components

Figure 30 and Figure 31 are schematic diagrams of typical notebook computer application circuits.

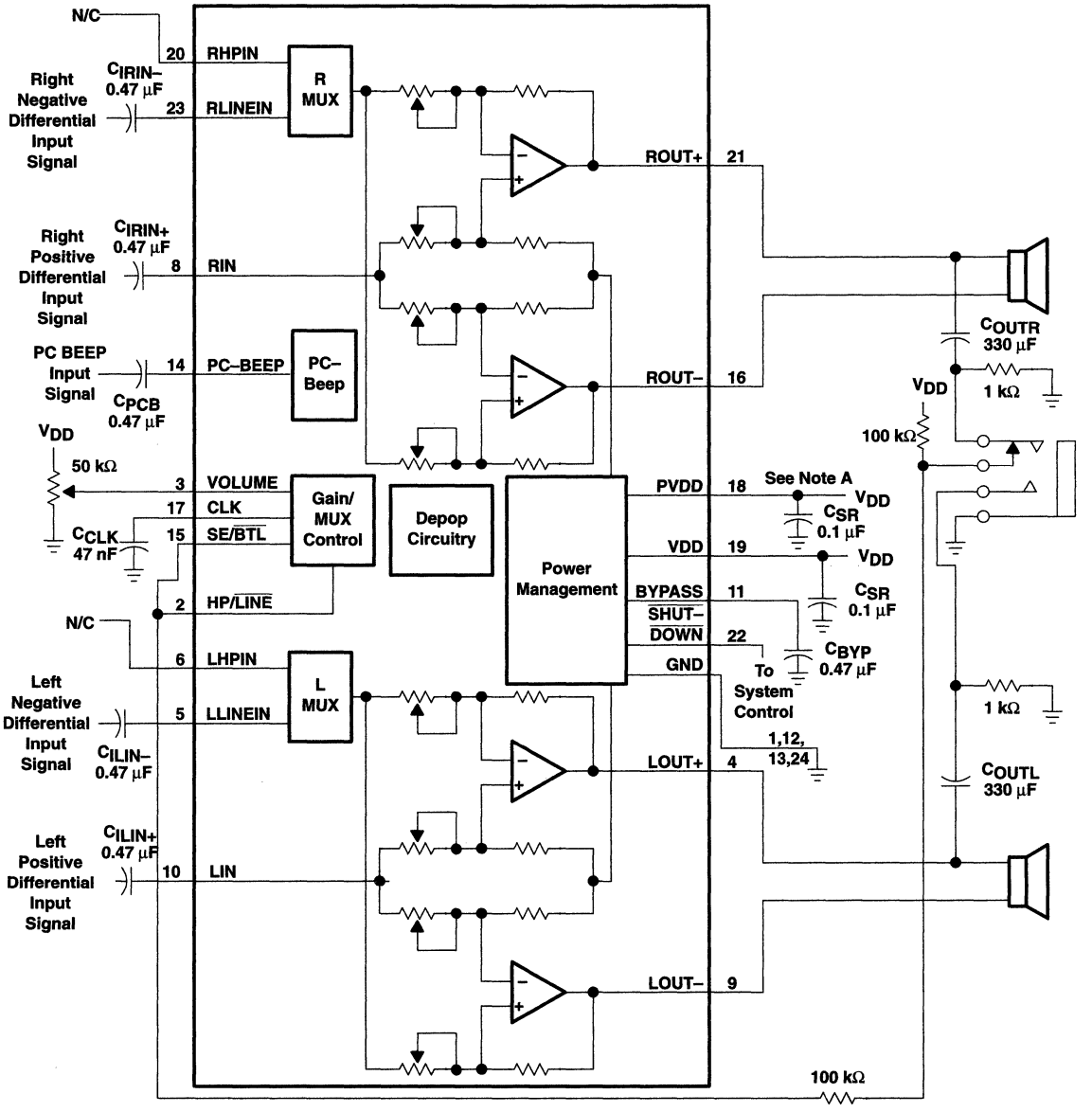
APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0242 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION



NOTE A. A 0.1 µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower–frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0242 Application Circuit Using Differential Inputs

APPLICATION INFORMATION

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency will also change by over 6 times. If an additional resistor is connected from the input pin of the amplifier to ground, as shown in the figure below, the variation of the cut-off frequency will be much reduced.

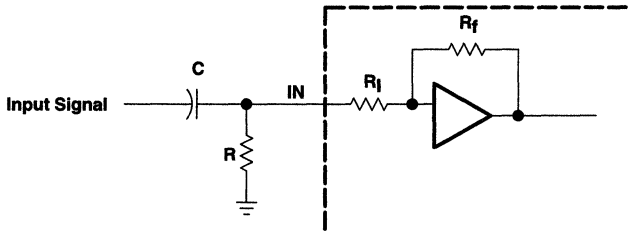


Figure 32. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in Figure 28:

The –3 dB frequency can be calculated using the following formula:

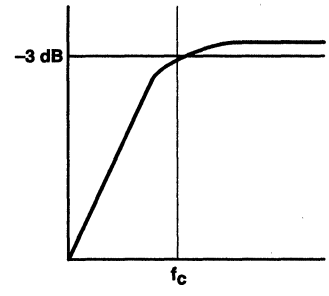
$$f_{-3\ dB} = \frac{1}{2\pi\ C\left(R \parallel R_I\right)} \quad (1)$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier, Z_I, form a high-pass filter with the corner frequency determined in equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_{IN} C_I} \quad (2)$$



APPLICATION INFORMATION

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 710 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 3.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (3)$$

In this example, C_I is 5.6 nF so one would likely choose a value in the range of 5.6 nF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0242 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_{BYP}

The midrail bypass capacitor, C_{BYP}, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor, C_{BYP}, values of 0.47 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

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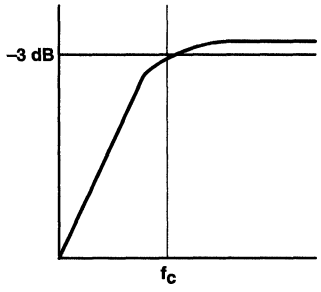
output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad (4)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

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bridged-tied load versus single-ended mode

Figure 33 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0242 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (5)$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

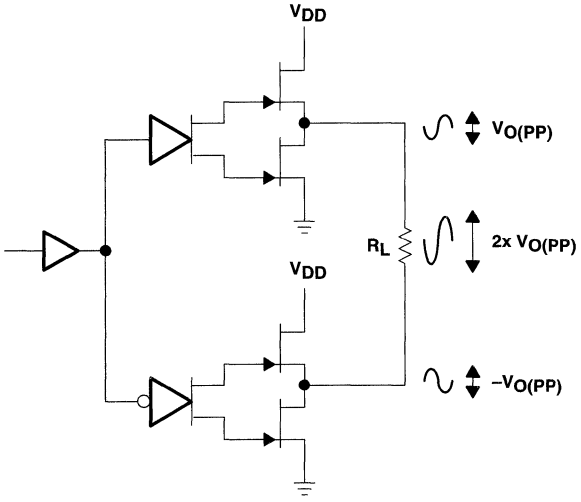

Figure 33. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 34. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C} \qquad (6)$$

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For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

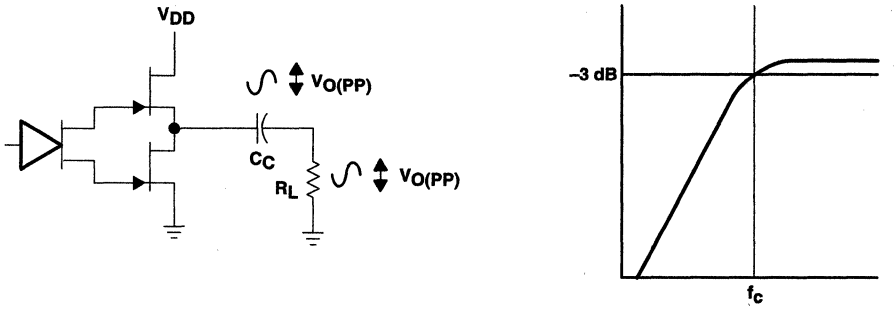

Figure 34. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended operation

In SE mode (see Figure 33 and Figure 34), the load is driven from the primary amplifier output for each channel (OUT+, terminals 21 and 4).

The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain by 6 dB.

input MUX operation

The input MUX allows two separate inputs to be applied to the amplifier. This allows the designer to choose which input is active independent of the state of the SE/$\overline{\text{BTL}}$ terminal. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs are active.

BTL amplifier efficiency

Class-AB amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 35).

APPLICATION INFORMATION

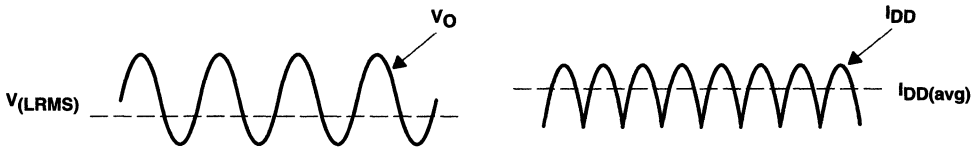

Figure 35. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{7}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}} \tag{8}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

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Table 3 employs equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the TPA0242 data sheet, one can see that when the TPA0242 is operating from a 5-V supply into a 3-Ω speaker that 4 W peaks are available. Converting watts to dB:

$$P_{dB} = 10\text{Log}\frac{P_W}{P_{ref}} = 10\text{Log}\frac{4\text{ W}}{1\text{ W}} = 6\text{ dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB – 15 dB = –9 dB (15 dB crest factor)
6 dB – 12 dB = –6 dB (12 dB crest factor)
6 dB – 9 dB = –3 dB (9 dB crest factor)
6 dB – 6 dB = 0 dB (6 dB crest factor)
6 dB – 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (10)$$

= 63 mW (18 dB crest factor)
= 125 mW (15 dB crest factor)
= 250 mW (9 dB crest factor)
= 500 mW (6 dB crest factor)
= 1000 mW (3 dB crest factor)
= 2000 mW (15 dB crest factor)

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This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation in the TPA0242 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0242 Power Rating, 5-V, 3-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	–3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	96°C

Table 5. TPA0242 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5 W	1250 mW (3 dB crest factor)	0.55	100°C
2.5 W	1000 mW (4 dB crest factor)	0.62	94°C
2.5 W	500 mW (7 dB crest factor)	0.59	97°C
2.5 W	250 mW (10 dB crest factor)	0.53	102°C

The maximum dissipated power, P_{Dmax}, is reached at a much lower output power level for an 8 Ω load than for a 3 Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for an 8 Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (11)$$

However, in the case of a 3 Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 3 Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table (see page 4). Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \quad (12)$$

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To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0242 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D \quad (13)$$

$$= 150 - 45(0.6 \times 2) = 96°C \text{ (15 dB crest factor)}$$

NOTE:

Internal dissipation of 0.6 W is estimated for a 2-W system with 15 dB crest factor per channel.

Tables 4 and 5 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0242 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 4 and 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0242 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0242, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 15) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 9 and 16). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0242 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0242 as an SE driver from LOUT+ and ROUT+ (terminals 4 and 21). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 36.

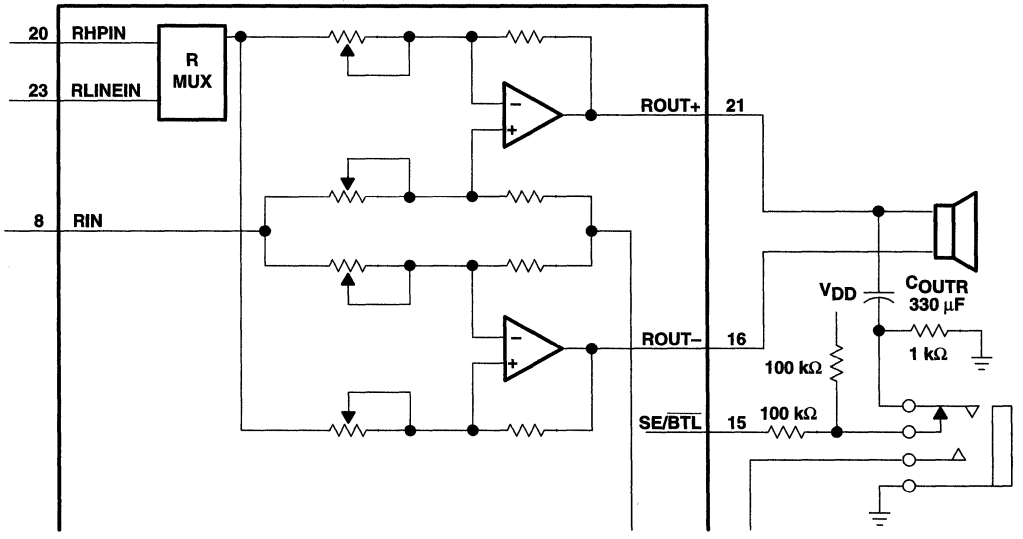


Figure 36. TPA0242 Resistor Divider Network Circuit

APPLICATION INFORMATION

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC BEEP operation

The PC BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC BEEP input is active, both of the LINEIN and HPIN inputs are deselected and both the left and right channels are driven in BTL mode with the signal from PC BEEP. The gain from the PC BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC BEEP input is deselected, the amplifier will return to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC BEEP will take the device out of shutdown and output the PC BEEP signal, then return the amplifier to shutdown mode.

When PCB ENABLE is held low, the amplifier will automatically switch to PC BEEP mode after detecting a valid signal at the PC BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1 V_{pp} or greater. To be accurately detected, the signal must have a minimum of 1 V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of 8 rising edges. When the signal is no longer detected, the amplifier will return to its previous operating mode and volume setting.

If it is desired to ac-couple the PC BEEP input, the value of the coupling capacitor should be chosen to satisfy the following equation:

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB} (100\ k\Omega)} \quad (14)$$

The PC BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally sits at midrail when no signal is present.

shutdown modes

The TPA0242 employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

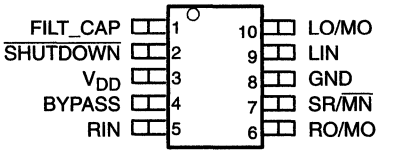
Table 6. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS†			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

† Inputs should never be left unconnected.
X = do not care

- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4-Ω From 5-V Supply**
- **0.6 W Into 4-Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Mono (BTL) Signal Created by Summing Left and Right Signals**
- **Wide Power Supply Compatibility 3 V to 5 V**
- **Meets PC99 Desktop Specs (target)**
- **Low Supply Current**
  - **10 mA Typical at 5 V**
  - **9 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)

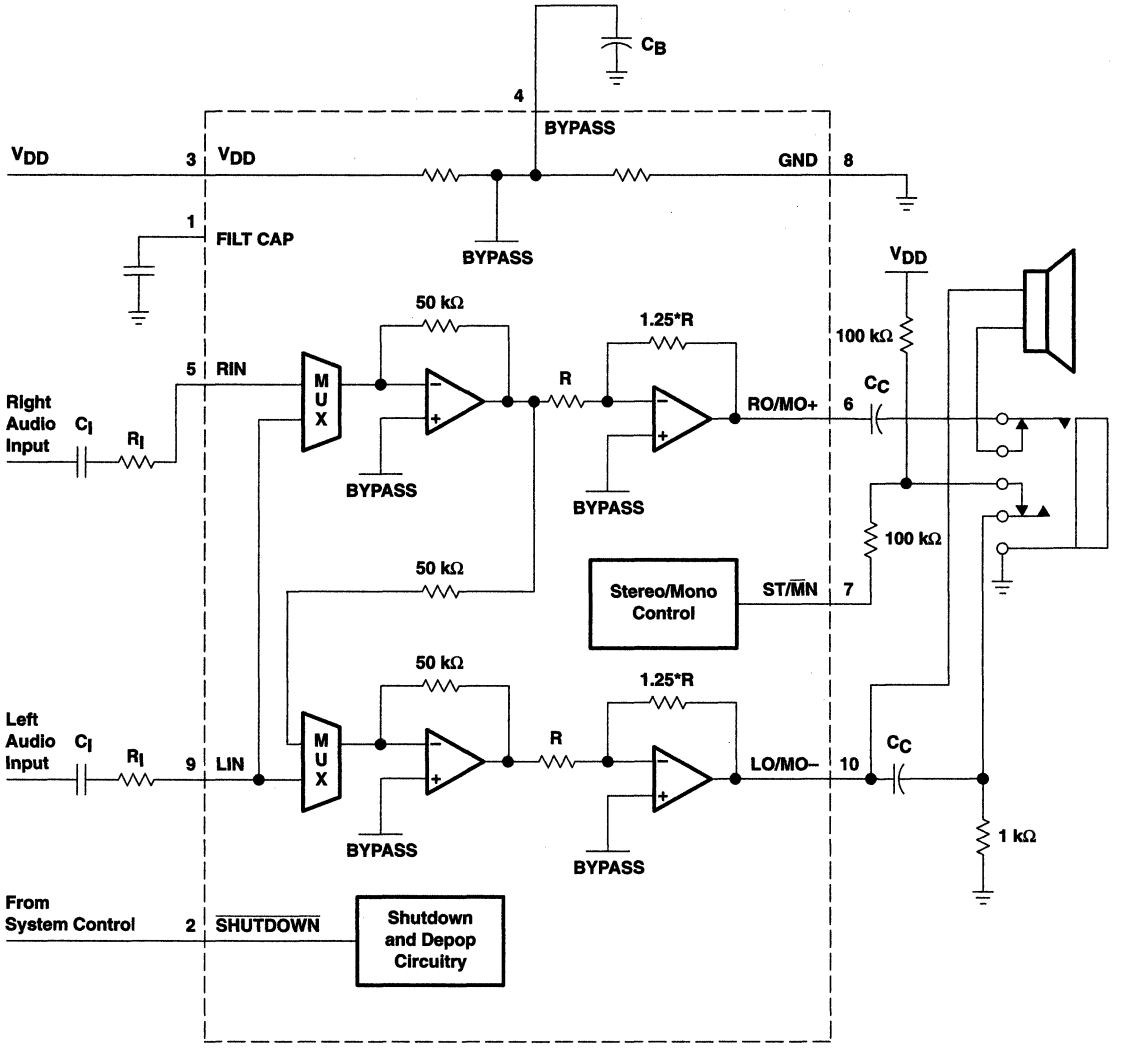


description

The TPA0243 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The mono signal is created by summing left and right inputs. The amplifier can be reconfigured on-the-fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0243 can delivery 2-W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0243 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of –40°C to 85°C.



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
–40°C to 85°C	TPA0243DGQ	AEK

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0243DGQR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MONO-IN	1	I	Mono input terminal
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
V_{DD}	3	I	V_{DD} is the supply voltage terminal.
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor.
RIN	5	I	Right-channel input terminal
RO/MO	6	O	Right-output in SE mode and mono positive output in BTL mode
SR/$\overline{\text{MN}}$	7	I	Selects between Stereo and Mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO	10	O	Left-output in SE mode and mono negative output in BTL mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			–40	85	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			9	14	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			660		mW
		THD = 0.1%,	SE mode,	R_L = 32 Ω		34		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW,	f = 20 Hz to 20 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			10	14	mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

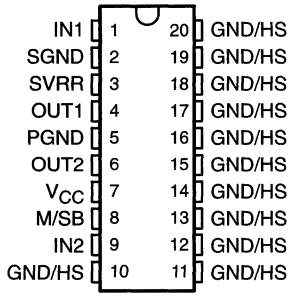
operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			2		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		95		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 2.5,	THD = 2%			20		kHz

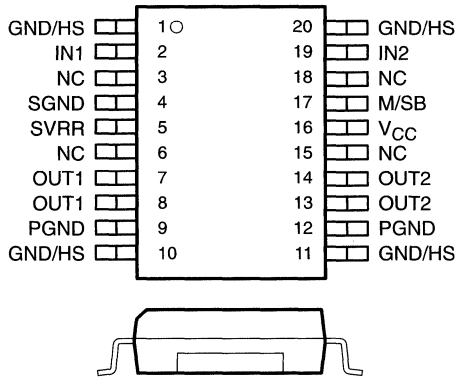
NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

- **TDA1517P Compatible**
- **High Power Outputs (6 W/Channel)**
- **Surface Mount Availability**
  20-Pin Thermal SOIC PowerPAD™
- **Thermal Protection**
- **Fixed Gain . . . 20 dB**
- **Mute and Standby Operation**
- **Supply Range . . . 9.5 V – 18 V**

NE PACKAGE
(TOP VIEW)



DWP PACKAGE
(TOP VIEW)



Cross Section View Showing PowerPAD

NC – No internal connection

description

The TPA1517 is a stereo audio power amplifier that contains two identical amplifiers capable of delivering 6 W per channel of continuous average power into a 4-Ω load at 10% THD+N or 5 W per channel at 1% THD+N. The gain of each channel is fixed at 20 dB. The amplifier features a mute/standby function for power-sensitive applications. The amplifier is available in Texas Instruments patented PowerPAD 20-pin surface-mount thermally-enhanced package (DWP) that reduces board space and facilitates automated assembly while maintaining exceptional thermal characteristics. It is also available in the 20-pin thermally enhanced DIP package (NE).

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	THERMALLY ENHANCED PLASTIC DIP	THERMALLY† ENHANCED SURFACE MOUNT (DWP)
–40°C to 85°C	TPA1517NE	TPA1517DWP

† The DWP package is available taped and reeled. To order a taped and reeled part, add the suffix R (e.g., TPA1517DWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

Terminal Functions

TERMINAL NAME	TERMINAL DWP NO.	TERMINAL NE NO.	I/O	DESCRIPTION
IN1	2	1	I	IN1 is the audio input for channel 1.
SGND	4	2	I	SGND is the input signal ground reference.
SVRR	5	3		SVRR is the midrail bypass mode enable.
OUT1	7, 8	4	O	OUT1 is the audio output for channel 1.
PGND	9, 12	5		PGND is the power ground reference.
OUT2	13, 14	6	O	OUT2 is the audio output for channel 2.
V_{CC}	16	7	I	V_{CC} is the supply voltage input.
M/SB	17	8	I	M/SB is the mute/standby mode enable. When held at less than 2 V, this signal enables the TPA1517 for standby operation. When held between 3.4 V and 8.8 V, this signal enables the TPA1517 for mute operation. When held above 9.2 V, the TPA1517 operates normally.
IN2	19	9	I	IN2 in the audio input for channel 2.
GND/HS	1, 10, 11, 20	10– 20		GND/HS are the ground and heatsink connections. All GND/HS terminals are connected directly to the mount pad for thermal-enhanced operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 22 V
Input voltage, V_I (IN1, IN2) ..... 22 V
Continuous total power dissipation ..... Internally limited (See Dissipation Rating Table)
Operating free-air temperature range, T_A ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DWP or NE package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These devices have been classified as Class 1 ESD sensitive products per MIL-PRF-38535 Method 3015.7. Appropriate precautions should be taken to prevent serious damage to the device.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DWP‡	2.94 W	23.5 mW/°C	1.88 W	1.53 W
NE‡	2.85 W	22.8 mW/°C	1.82 W	1.48 W

‡ See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9.5		18	V
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics, V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current			45	70	mA
$V_{O(DC)}$	DC output voltage	See Note 2		4		V
$V_{(M/SB)}$	M/SB on voltage			9.5		V
$V_{O(M)}$	Mute output voltage	V_I = 1 V (max)		2		mV
$I_{CC(SB)}$	Supply current in standby mode			7	100	μA

NOTE 2: At 6 V < V_{CC} < 18 V the DC output voltage is approximately $V_{CC}/2$.

electrical characteristics, V_{CC} = 14.5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current			50	80	mA
$V_{O(DC)}$	DC output voltage	See Note 2		5		V
$V_{(M/SB)}$	Voltage on M/SB terminal for normal operation			9.5		V
$V_{O(M)}$	Mute output voltage	V_I = 1 V (max)		2		mV
$I_{CC(SB)}$	Supply current in standby mode			7	100	μA

NOTE 2: At 6 V < V_{CC} < 18 V the DC output voltage is approximately $V_{CC}/2$.

operating characteristic, V_{CC} = 12 V, R_L = 4 Ω, f = 1 kHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (see Note 3)	THD = 0.2%		3		W
		THD = 10%		6		
SNR	Signal-to-noise ratio			84		dB
THD	Total harmonic distortion	P_O = 1 W, R_L = 8 Ω, f = 1 kHz		0.1%		
$I_{O(SM)}$	Non-repetitive peak output current			4		A
$I_{O(RM)}$	Repetitive peak output current			2.5		A
	Low-frequency roll-off	–3 dB		45		Hz
	High-frequency roll-off	–1 dB	20			kHz
	Supply ripple rejection ratio	M/SB = On, f = 1 kHz		65		dB
Z_I	Input impedance			60		kΩ
V_n	Noise output voltage (see Note 4)	R_S = 0, M/SB = On		50		μV(rms)
		R_S = 10 kΩ, M/SB = On		70		μV(rms)
		M/SB = Mute		50		μV(rms)
	Channel separation	R_S = 10 kΩ		58		dB
	Gain		18.5	20	21	
	Channel balance			0.1	1	dB

NOTES: 3. Output power is measured at the output terminals of the IC.
4. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

operating characteristic, V_{CC} = 14.5 V, R_L = 4 Ω, f = 1 kHz, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (see Note 3)	THD = 0.2%		4.5		W
		THD < 10%		6		W
SNR	Signal-to-noise ratio			84		dB
THD	Total harmonic distortion	P_O = 1 W		0.1%		
$I_{O(SM)}$	Non-repetitive peak output current			4		A
$I_{O(RM)}$	Repetitive peak output current			2.5		A
	Low-frequency roll-off	–3 dB		45		Hz
	High-frequency roll-off	–1 dB	20			kHz
	Supply ripple rejection ratio	M/SB = On		65		dB
Z_I	Input impedance			60		kΩ
V_n	Noise output voltage (see Note 4)	R_S = 0, M/SB = On		50		μV(rms)
		R_S = 10 kΩ, M/SB = On		70		μV(rms)
		M/SB = Mute		50		μV(rms)
	Channel separation	R_S = 10 kΩ		58		dB
	Gain		18.5	20	21	dB
	Channel balance			0.1	1	dB

NOTES: 3. Output power is measured at the output terminals of the IC.
4. Noise voltage is measured in a bandwidth of 22 Hz to 22 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
I_{CC}	Supply current		vs Supply voltage	1
	Power supply rejection ratio		vs Frequency	2, 3
THD + N	Total harmonic distortion plus noise	V_{CC} = 12 V	vs Frequency vs Power output	4, 5, 6 10, 11
		V_{CC} = 14.5 V	vs Frequency vs Power output	7, 8, 9 12, 13
	Crosstalk		vs Frequency	14, 15
	Gain		vs Frequency	16
	Phase		vs Frequency	16
V_n	Noise voltage		vs Frequency	17, 18
P_O	Output power		vs Supply voltage vs Load resistance	19 20
P_D	Power dissipation		vs Output power	21, 22

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

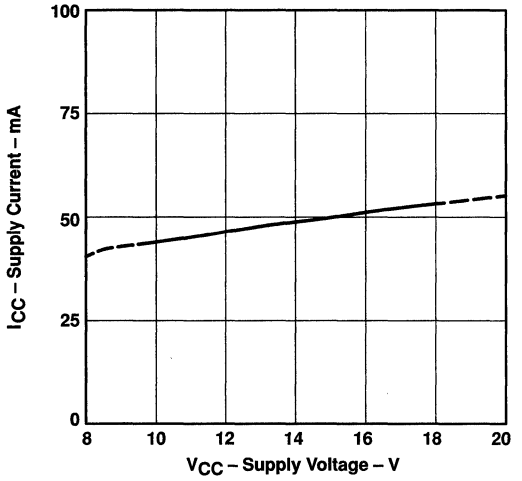


Figure 1

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

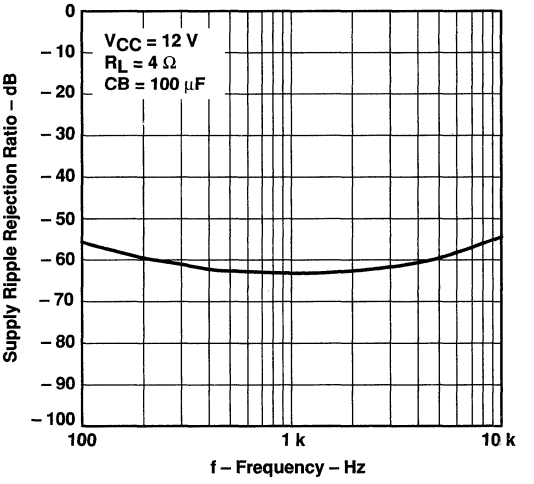


Figure 2

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

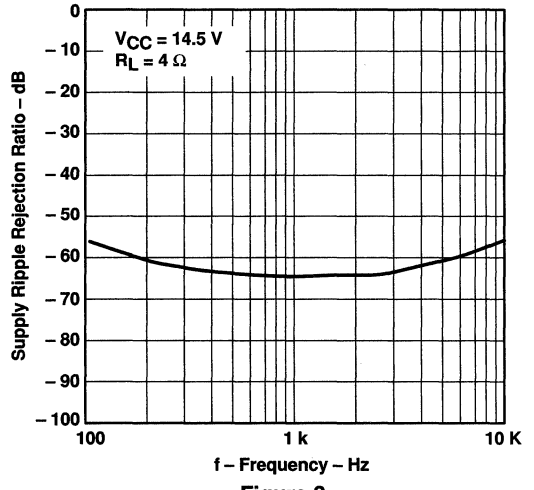


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

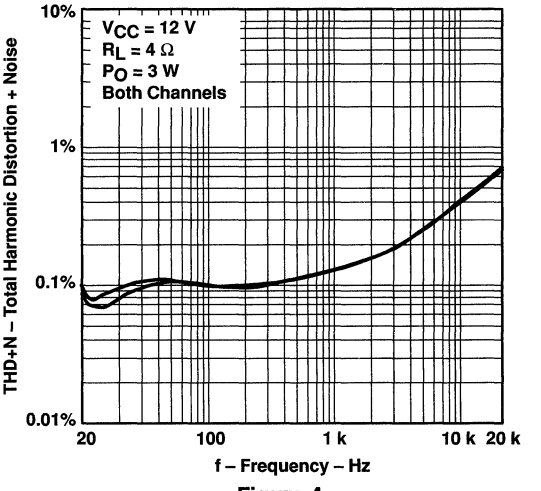


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

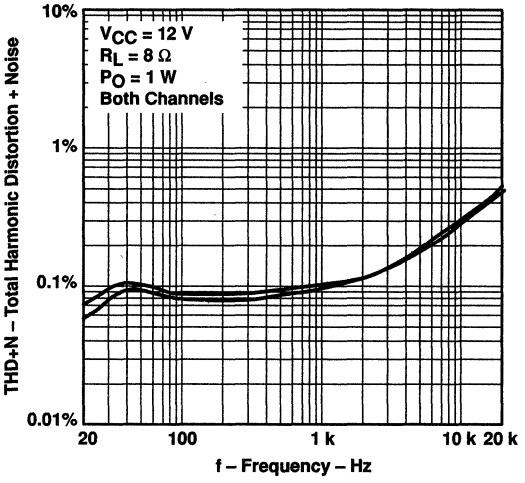


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

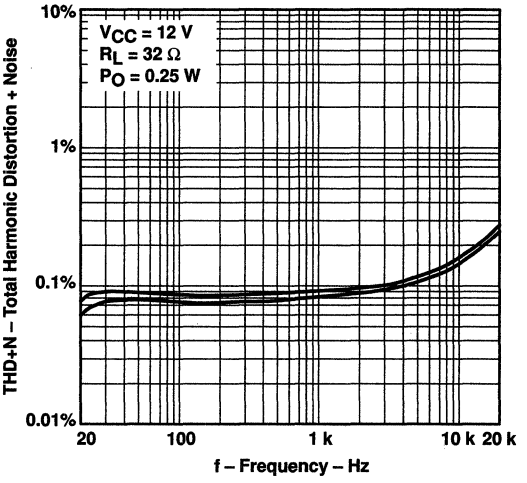


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

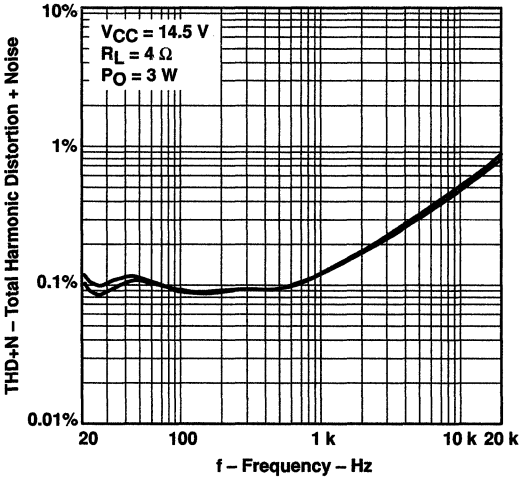


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

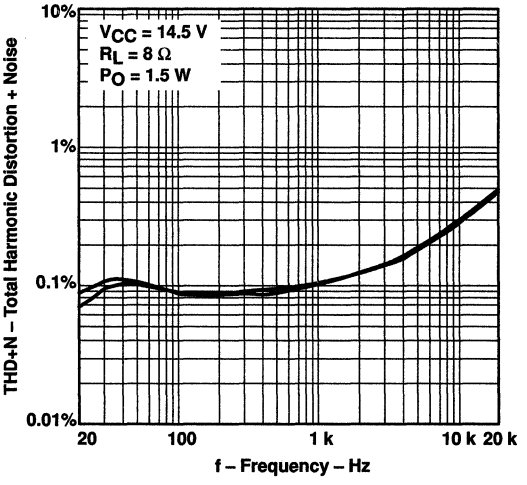


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

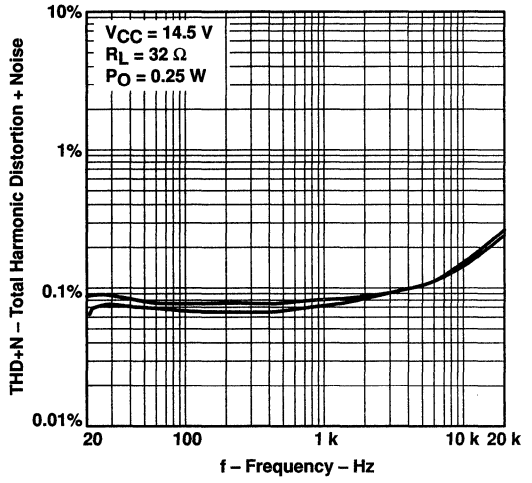


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

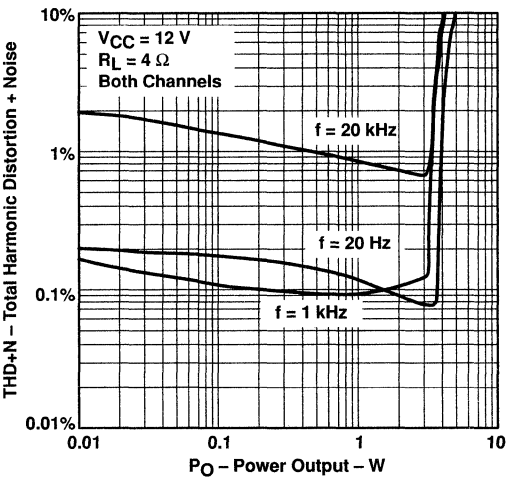


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

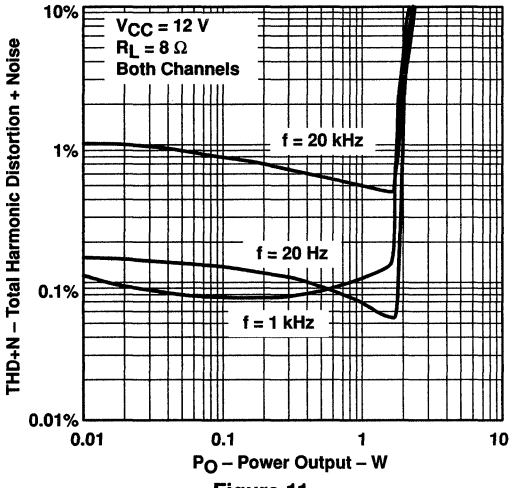


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
POWER OUTPUT

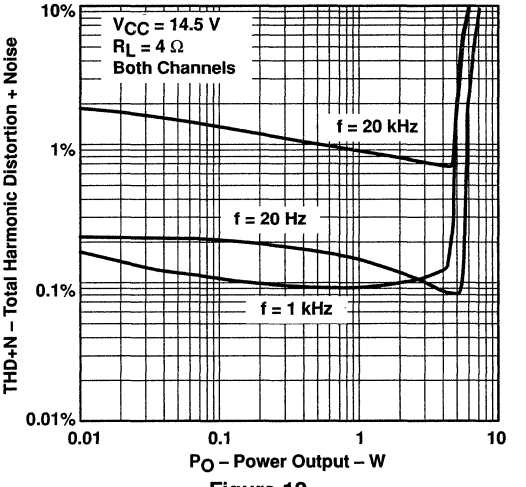


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

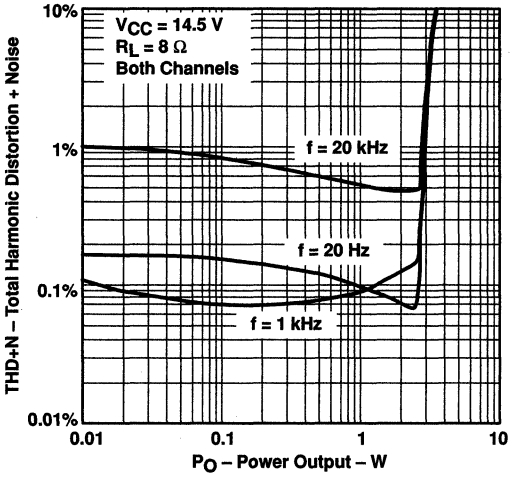


Figure 13

CROSSTALK vs FREQUENCY

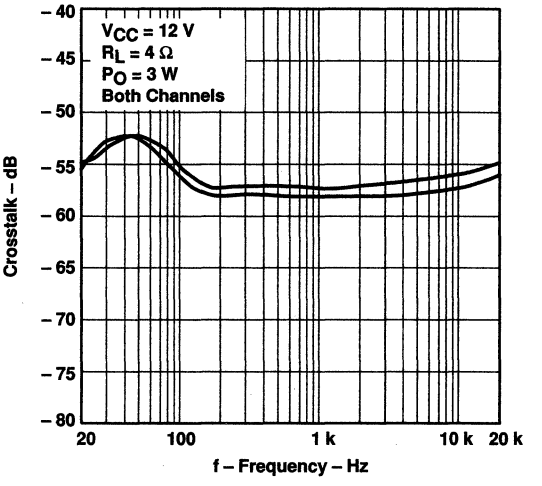


Figure 14

CROSSTALK vs FREQUENCY

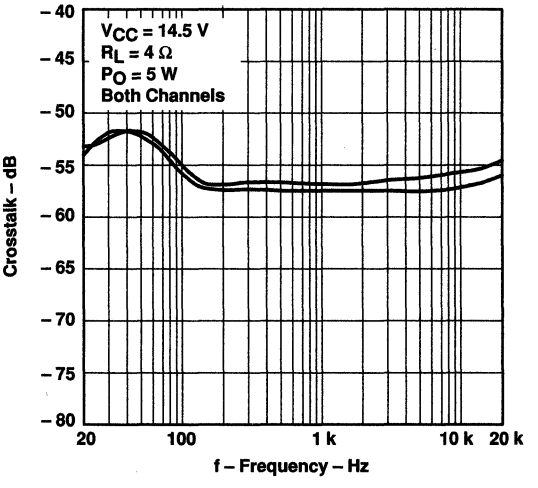


Figure 15

TYPICAL CHARACTERISTICS

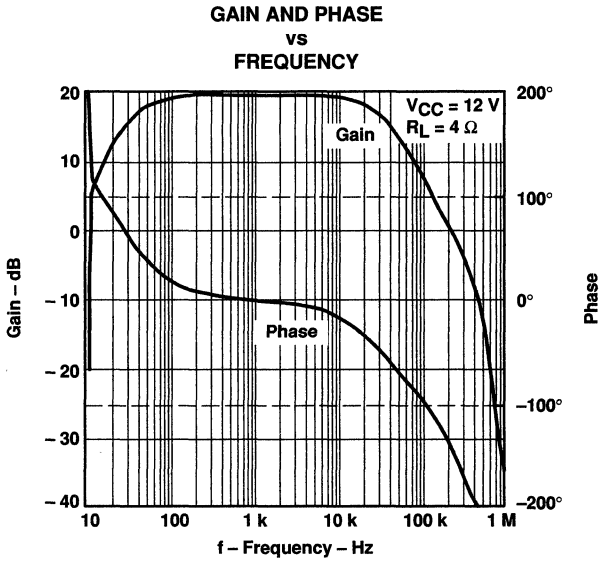


Figure 16

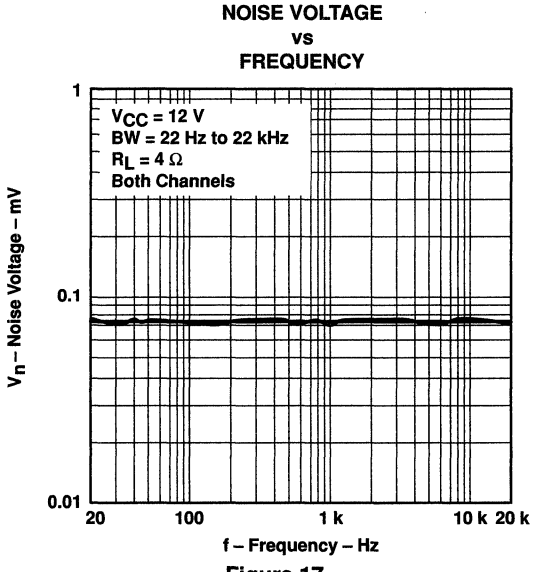


Figure 17

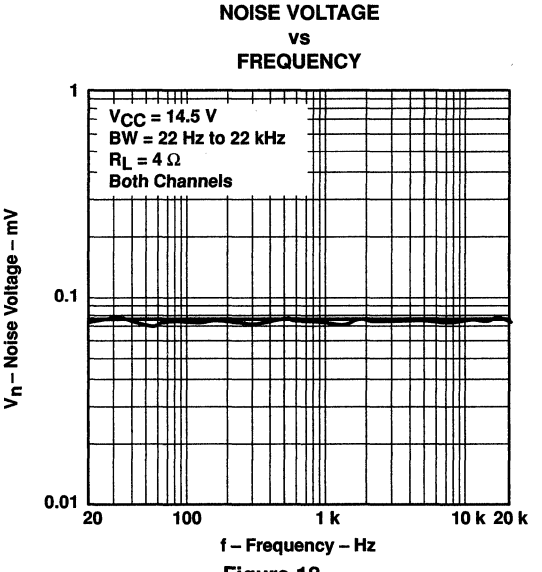


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT POWER vs SUPPLY VOLTAGE

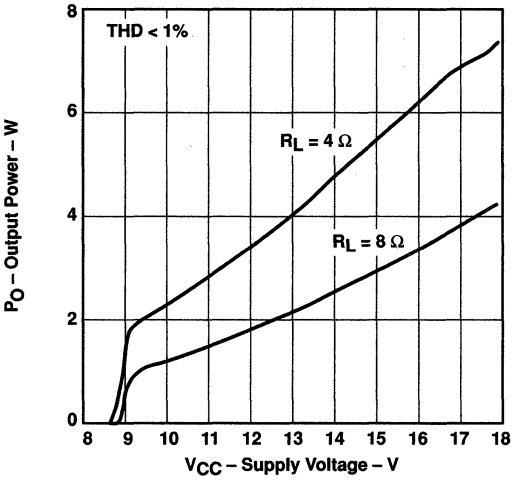


Figure 19

OUTPUT POWER vs LOAD RESISTANCE

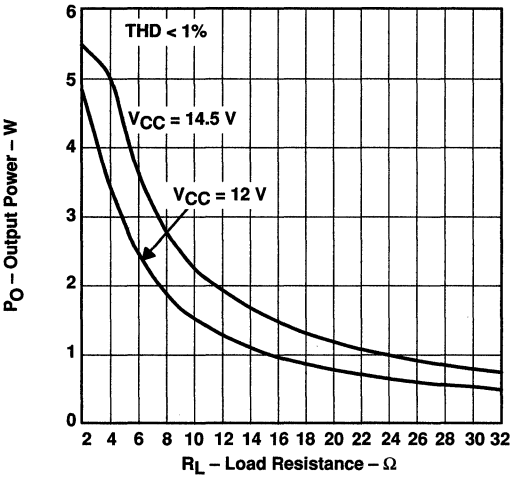


Figure 20

POWER DISSIPATION vs OUTPUT POWER

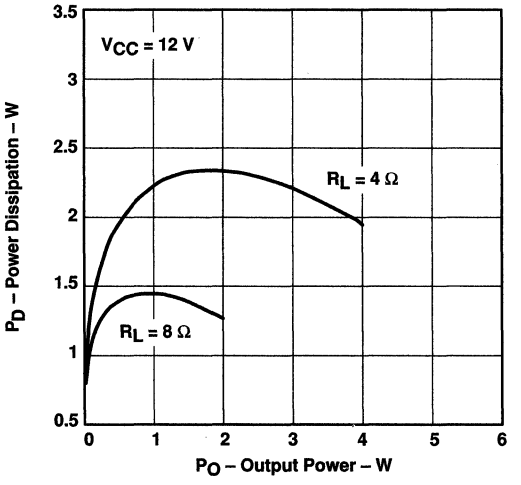


Figure 21

POWER DISSIPATION vs OUTPUT POWER

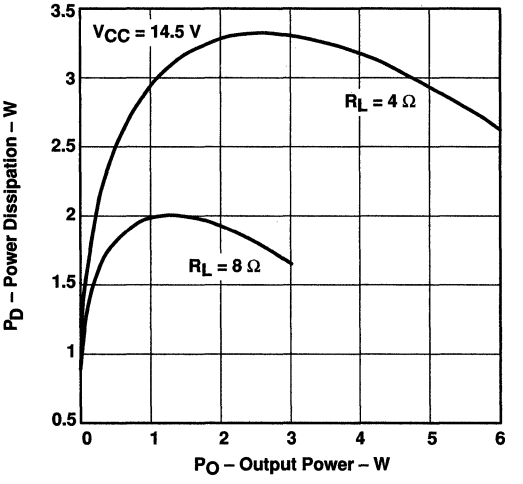
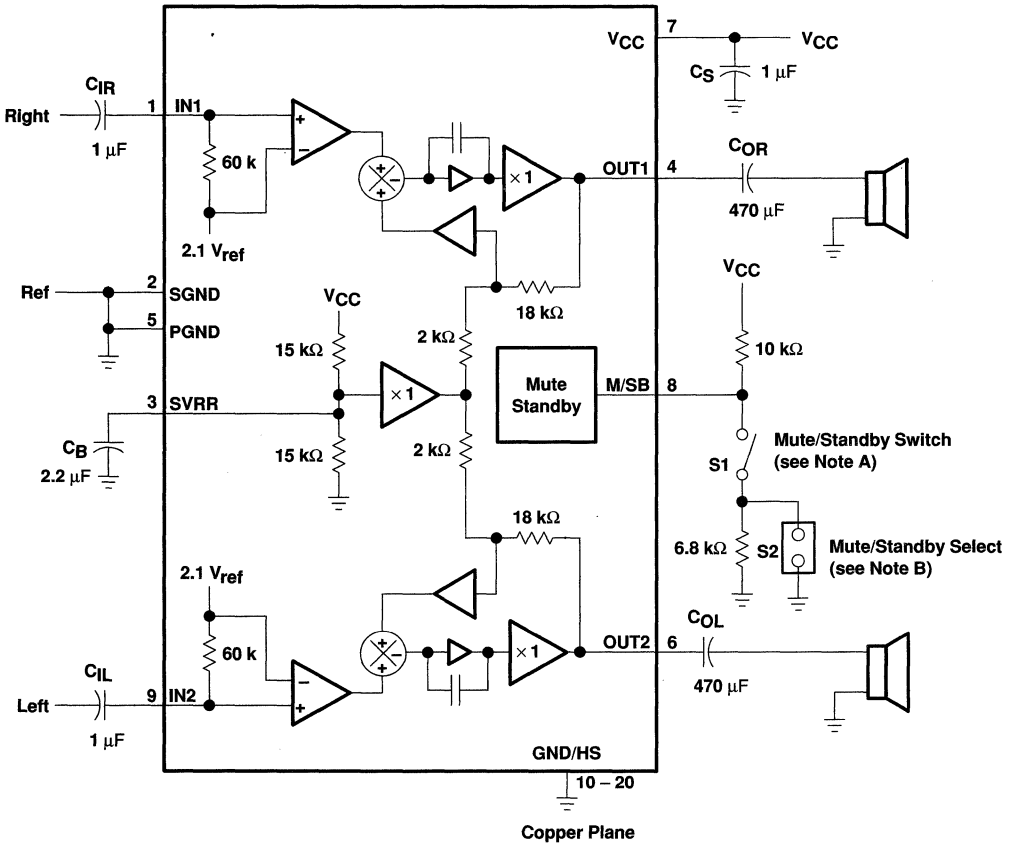


Figure 22

APPLICATION INFORMATION

amplifier operation

The TPA1517 is a stereo audio power amplifier designed to drive 4-Ω speakers at up to 6 W per channel. Figure 23 is a schematic diagram of the minimum recommended configuration of the amplifier. Gain is internally fixed at 20 dB (gain of 10 V/V).



NOTES: A. When S1 is open, the TPA1517 operates normally. When this switch is closed, the device is in mute/standby mode.
B. When S2 is open, activating S1 places the TPA1517 in mute mode. When S2 is closed, activating S1 places the TPA1517 in standby mode.
C. The terminal numbers are for the 20-pin NE package.

Figure 23. TPA1517 Minimum Configuration

The following equation is used to relate gain in V/V to dB:

$$G_{dB} = 20 \text{ LOG}\left(G_{V/V}\right)$$

APPLICATION INFORMATION

The audio outputs are biased to a midrail voltage which is shown by the following equation:

$$V_{MID} = \frac{V_{CC}}{2}$$

The audio inputs are always biased to 2.1 V when in mute or normal mode. Any dc offset between the input signal source and the input terminal is amplified and can seriously degrade the performance of the amplifier. For this reason, it is recommended that the inputs always be connected through a series capacitor (ac coupled). The power outputs, also having a dc bias, must be connected to the speakers via series capacitors.

mute/standby operation

The TPA1517 has three modes of operation; normal, mute, and standby. They are controlled by the voltage on the M/SB terminal as described in Figure 24. In normal mode, the TPA1517 amplifies the signal applied to the two input terminals providing low impedance drive to speakers connected to the output terminals. In mute mode, the amplifier retains all bias voltages and quiescent supply current levels but does not pass the input signal to the output. In standby mode, the internal bias generators and power-drive stages are turned off, thereby reducing the supply current levels.

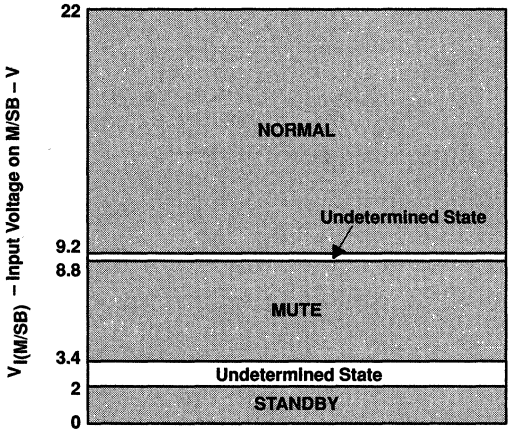
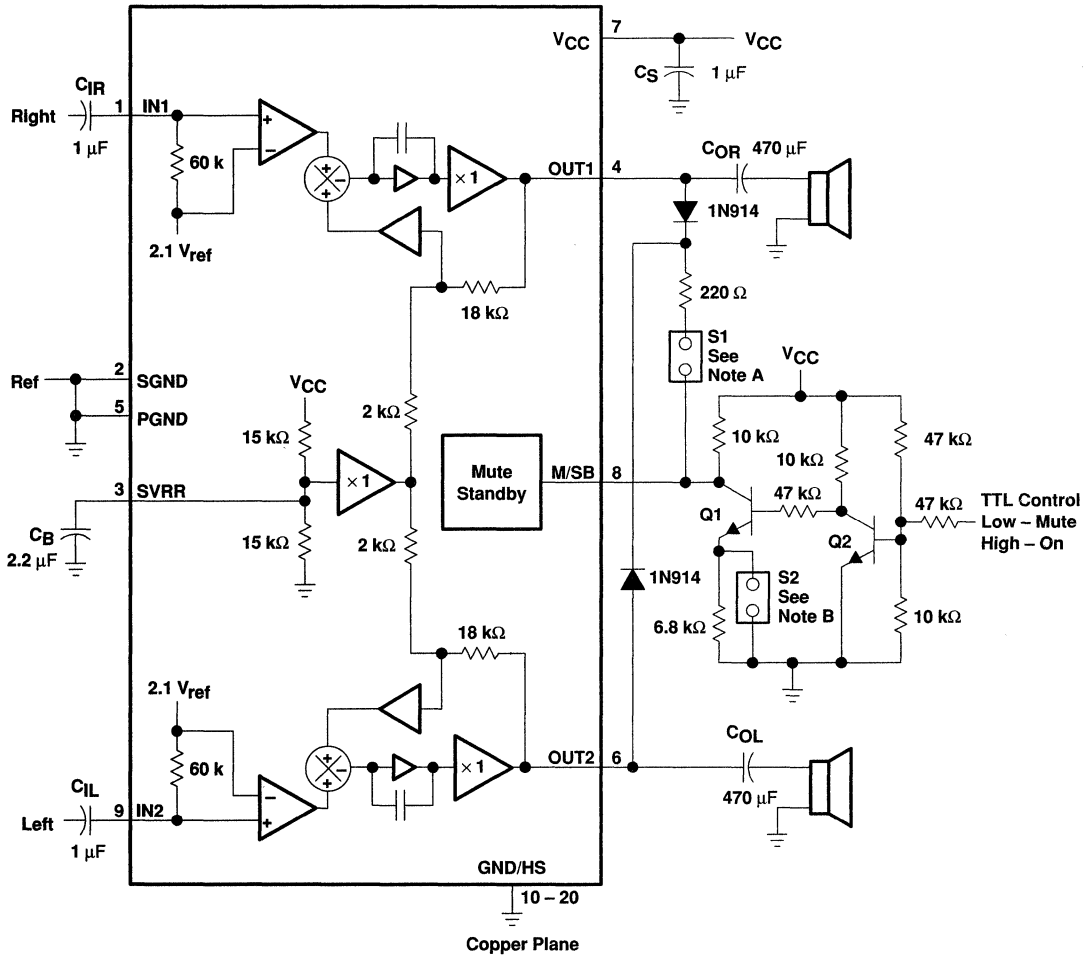


Figure 24. Standby, Mute, and Normal (On) Operating Conditions

The designer must take care to place the control voltages within the defined ranges for each desired mode, whenever an external circuit is used to control the input voltage at the M/SB terminal. The undefined area can cause unpredictable performance and should be avoided. As the control voltage moves through the undefined areas pop or click sounds may be heard in the speaker. Moving from mute to normal causes a very small click sound. Whereas moving from standby to mute can cause a much larger pop sound. Figure 25 shows external circuitry designed to help reduce transition pops when moving from standby mode to normal mode.

APPLICATION INFORMATION

Figure 25 is a reference schematic that provides TTL-level control of the M/SB terminal. A diode network is also included which helps reduce turn-on pop noises. The diodes serve to drain the charge out of the output coupling capacitors while the amplifier is in shutdown mode. When the M/SB voltage is in the normal operating range, the diodes have no effect on the ac performance of the system.



NOTES: A. When S1 is closed, the depop circuitry is active during standby mode.
B. When S2 is open, activating S1 places the TPA1517 in mute mode. When S2 is closed, activating S1 places the TPA1517 in standby mode.
C. The terminal numbers are for the 20-pin NE package.

Figure 25. TTL Control with POP Reduction

APPLICATION INFORMATION

component selection

Some of the general concerns for selection of capacitors are:

- Leakage currents on aluminum electrolytic capacitors
- ESR (equivalent series resistance)
- Temperature ratings

leakage currents

Leakage currents on most ceramic, polystyrene, and paper capacitors are negligible for this application. Leakage currents for aluminum electrolytic and tantalum tend to be higher. This is especially important on the input terminals and the SVRR capacitor. These nodes encounter from 3 V to 7 V, and need to have leakage currents less than 1 μA to keep from affecting the output power and noise performance.

equivalent series resistance

ESR is mainly important on the output coupling capacitor, where even 1 Ω of ESR in C_O with an 8-Ω speaker can reduce the output drive power by 12.5%. ESR should be considered across the frequency range of interest, (i.e., 20 Hz to 20 kHz). The following equation calculates the amount of power lost in the coupling capacitor:

$$\% \text{ Power in } C_O = \frac{ESR}{R_L}$$

In general, the power supply decoupling requires a very low ESR as well to take advantage of the full output drive current.

temperature range

The temperature range of the capacitors may or may not seem like an obvious thing to specify, but it is very important. Many of the high-density capacitors perform very differently at different temperatures. When consistent high performance is required from the system over temperature in terms of low THD, maximum output power, and turn-on/off popping, then interactions of the coupling capacitors and the SVRR capacitors need to be considered, as well as the change in ESR on the output capacitor with temperature.

turn-on pop consideration

To select the proper input coupling capacitor, the designer should select a capacitor large enough to allow the lowest desired frequency pass and small enough that the time constant is shorter than the output RC time constant to minimize turn-on popping. The input time constant for the TPA1517 is determined by the input 60-kΩ resistance of the amplifier, and the input coupling capacitor according to the following generic equation:

$$T_C = \frac{1}{2\pi RC}$$

For example, 8-Ω speakers and 220-μF output coupling capacitors would yield a 90-Hz cut-off point for the output RC network. The input network should be the same speed or faster (> 90 Hz T_C). A good choice would be 180 Hz. As the input resistance is 60 kΩ, a 14-nF input coupling capacitor would do.

The bypass-capacitor time constant should be much larger (×5) than either the input coupling capacitor time constant or the output coupling capacitor time constants. In the previous example with the 220-μF output coupling capacitor, the designer should want the bypass capacitor, T_C, to be in the order of 18 Hz or lower. To get an 18-Hz time constant, C_B is required to be 1 μF or larger because the resistance this capacitor sees is 7.5 kΩ.

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In summary, follow one of the three simple relations presented below, depending on the tradeoffs between low frequency response and turn-on pop. If depop performance is the top priority, then follow:

$$7500\ C_B > 5R_LC_O > 300000\ C_I$$

If low frequency ac response is more important but depop is still a consideration then follow:

$$\frac{1}{2\pi 60000\ C_I} < 10\ \text{Hz}$$

Finally, if low frequency response is most important and depop is not a consideration then follow:

$$\frac{1}{2\pi 60000\ C_I} \leq \frac{1}{2\pi R_L\ C_I} \leq f_{low}$$

thermal applications

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. Figure 19 shows that when the TPA1517 is operating from a 12-V supply into a 4-Ω speaker that approximately 3.5 W peaks are possible. Converting watts to dB using the following equation:

$$P_{dB} = 10\text{Log}\left(\frac{P_W}{P_{ref}}\right)$$

$$= 10\text{Log}\left(\frac{3.5}{1}\right)$$

$$= 5.44\ \text{dB}$$

Subtracting dB for the headroom restriction to obtain the average listening level without distortion yields the following:

$$5.44\ \text{dB} - 15\ \text{dB} = -9.56\ \text{dB (15 dB headroom)}$$

$$5.44\ \text{dB} - 12\ \text{dB} = -6.56\ \text{dB (12 dB headroom)}$$

Converting dB back into watts:

$$P_W = 10^{P_{dB}/10} \times P_{ref}$$

$$= 111\ \text{mW (15 dB headroom)}$$

$$= 221\ \text{mW (12 dB headroom)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst cast, which is 3.5 W of continuous power output with 0 dB of headroom, against 12-dB and 15-dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, internal dissipation in the TPA1517 and maximum ambient temperatures are shown in Table 1.

APPLICATION INFORMATION

Table 1. TPA1517 Power Rating

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
3.5	3.5 W	2.1	–34°C
3.5	1.77 W (3 dB)	2.4	–61°C
3.5	884 mW (6 dB)	2.25	–48°C
3.5	442 mW (9 dB)	1.75	–4°C
3.5	221 mW (12 dB)	1.5	18°C
3.5	111 mW (15 dB)	1.25	40°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the derating factor for the NE package with 4 square inches of copper area is 22.8 mW/°C and 38.8 mW/°C respectively. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating}}$$

$$\text{For 0 CFM:} \quad = \frac{1}{0.0228}$$

$$= 43.9°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given θ_{JA}, the maximum allowable junction temperature and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA1517 is 150°C.

$$T_A \text{ Max} = T_J \text{ Max} - \theta_{JA} P_D$$

$$= 150 - 43.9(1.25 \times 2) = 40°C \text{ (15 dB headroom, 0 CFM)}$$

Table 1 clearly shows that for most applications some airflow is required to keep junction temperatures in the specified range. The TPA1517 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Using the DWP package on a multilayer PCB with internal ground planes can achieve better thermal performance. Table 1 was calculated for a maximum volume system; when the output level is reduced, the numbers in the table change significantly. Also using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

APPLICATION INFORMATION

TPA1517 NE THERMAL RESISTANCE, θ_{JA}
vs
COPPER AREA

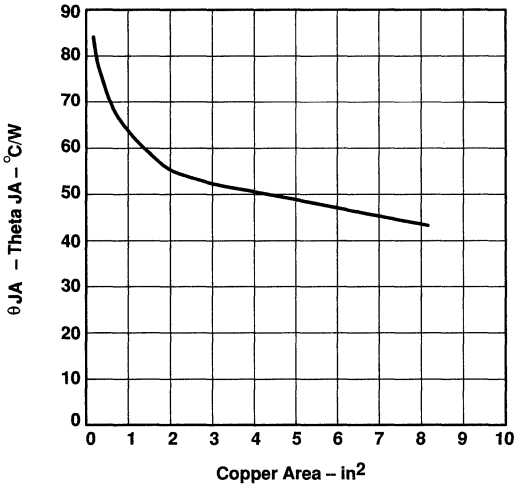
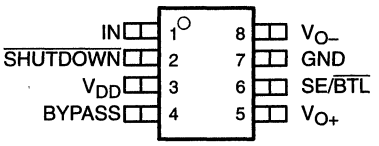


Figure 26

Contents

- **Ideal for Wireless Communicators, Notebook PCs, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4-Ω From 5-V Supply**
- **0.6 W Into 4-Ω From 3-V Supply**
- **Wide Power Supply Compatibility 3 V to 5 V**
- **Low Supply Current**
  - **8 mA Typical at 5 V**
  - **4 mA Typical at 3 V**
- **Shutdown Control . . . < 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **–40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGN PACKAGE
(TOP VIEW)



description

The TPA0211 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The device is ideal for use in small wireless communicators, notebook PCs, PDAs, anyplace a mono speaker and stereo head phones are required. From a 5-V supply, the TPA0211 can delivery 2-W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = -R_F/R_I$). The power stage is internally configured with a gain of –1.25 V/V in SE mode, and –2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0211 is available in the 8-pin thermally-enhanced MSOP package (DGN) and operates over an ambient temperature range of –40°C to 85°C.

PRODUCT PREVIEW

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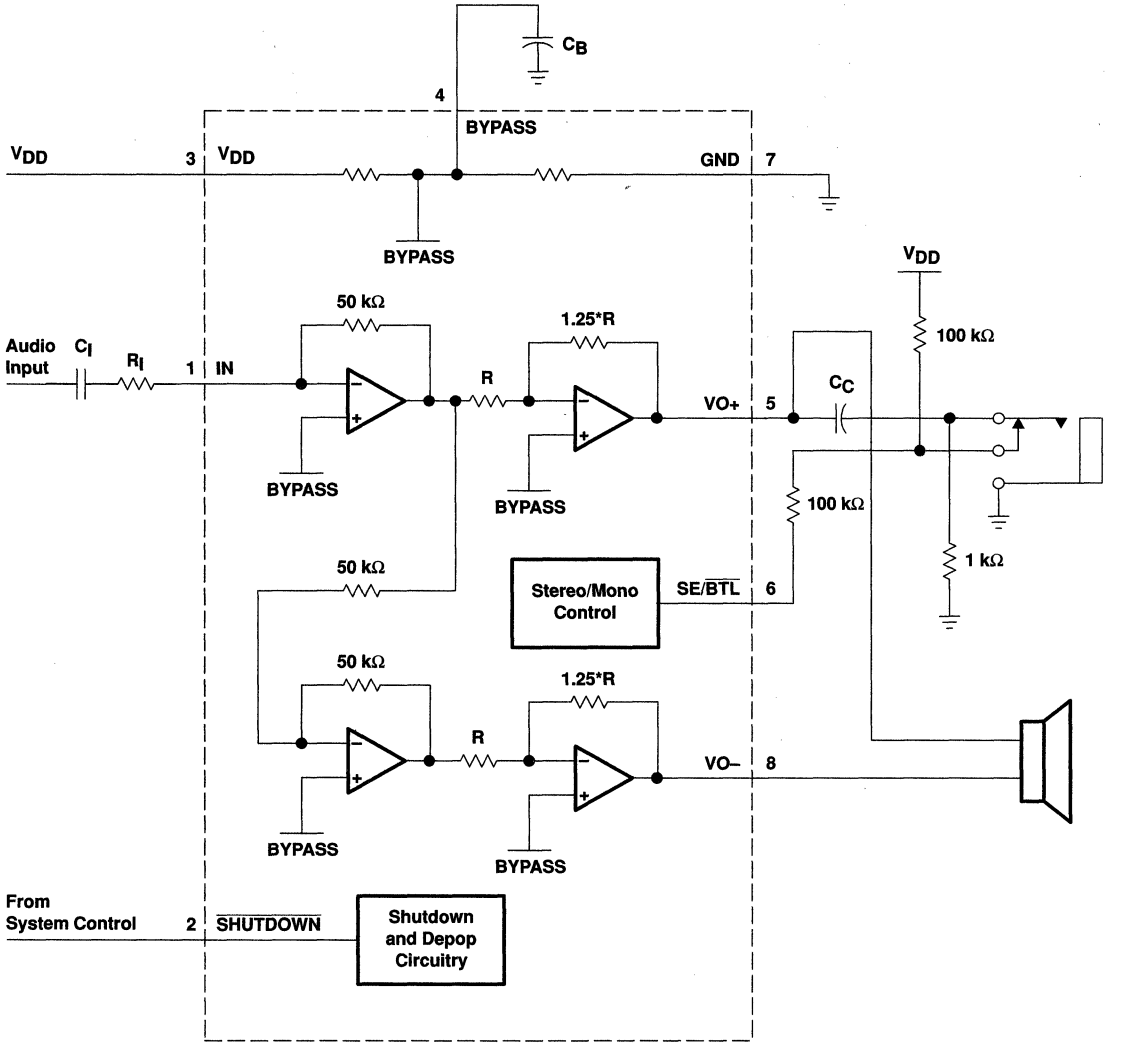
PRODUCT PREVIEW



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGN)	
–40°C to 85°C	TPA0211DGN	AEG

† The DGN package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0211DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-μF to 1-μF capacitor.
GND	7		GND is the ground connection.
IN	1	I	IN is the audio input terminal.
SE/$\overline{\text{BTL}}$	6	I	When SE/$\overline{\text{BTL}}$ is held low, the TPA0211 is in BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the TPA0211 is in SE mode.
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
V_{DD}	3		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive output for BTL and SE modes.
V_O-	8	O	V_O- is the negative output in BTL mode and a high-impedance output in SE mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{DD} ..... 6 V
Input voltage, V_I ..... –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation ..... internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) ..... –40°C to 85°C
Operating junction temperature range, T_J ..... –40°C to 150°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGN	2.14 W¶	17.1 mW/°C	1.37 W	1.11 W

¶ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			–40	85	°C

PRODUCT PREVIEW

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			4		mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			660		mW
		THD = 0.1%,	SE mode,	R_L = 32 Ω		33		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW,	f = 20 Hz to 20 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)				30	mV
I_{DD}	Supply current			8		mA
$I_{DD(SD)}$	Supply current, shutdown mode			1	10	μA

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%,	BTL mode			2		W
		THD = 0.1%,	SE mode,	R_L = 32 Ω		92		mW
THD + N	Total harmonic distortion plus noise	P_O = 1.5 W,	f = 20 Hz to 20 kHz			0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 2.5,	THD = 2%			20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

PRODUCT PREVIEW

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Design Considerations for Class-D Audio Power Amplifiers Application Report

Literature Number: SLOA031
August 1999

TEXAS INSTRUMENTS

Printed on Recycled Paper

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Design Considerations for Class-D Audio Power Amplifiers

Richard Palmer

ABSTRACT

This application report provides background information, general equations, and component selection criteria for proper design and implementation of the Texas Instruments class-D audio power amplifiers. Topics include class-D switching and charge pump circuits, signal conditioning of the audio inputs and outputs for both the class-D and class-AB headphone amplifiers, IC control and indicator circuits, power supply decoupling, and PCB layout.

1 Introduction

Circuit design and layout plays a large role in creating or reducing distortion in class-D audio power amplifiers. The high-frequency-switching characteristics of class-D output stages offer some interesting design challenges over conventional class-AB amplifiers. This application report provides the background information necessary to properly design Texas Instruments (TI™) class-D stereo audio power amplifiers into an audio solution.

Texas Instruments offers several class-D stereo audio power amplifiers, each of which is featured on an evaluation module (EVM), available from TI. All information appearing in this report originated from the design of the SLOP204 EVM, which features the TPA005D14 class-D stereo audio power amplifier IC. The TPA005D14 EVM is capable of driving 2 W into a 4-Ω load from a 5-V power supply. This and similar TI EVMs allow customers to evaluate the performance of TI's class-D audio products without spending the time and resources normally required to design and build a test circuit. In addition, each EVM is compatible with the TI plug-n-play audio amplifier evaluation platform, which provides the power, standard audio interconnects, signal conditioning, and speakers required to operate the audio system.

TI class-D EVMs are available with or without an internal class-AB headphone amplifier circuit. The ICs with the headphone circuit are equipped with the necessary internal interface logic to select between the class-D and headphone modes of operation. Each EVM includes onboard pushbutton switches for manual muting and shutdown, and input pins for logic control of mode, mute, and shutdown. A miniature stereo headphone jack is mounted on the EVMs that have the internal headphone amplifier to allow convenient connection of headphones.

The modules have single in-line header connector pins mounted to the underside of the boards. These pins allow the module to be plugged into the plug-n-play platform, which automatically makes all of the signal input and output, power, and control connections to the module. The module connection pins are on 0.1-inch centers to allow easy use with standard perf board- and plug board-based prototyping systems, or for direct wiring into existing circuits and equipment when used stand-alone.

These EVMs and the plug-n-play platform can be found at the TI web site: http://www.ti.com/sc/apa.

2 Class-D Amplifier Circuits

The class-D amplifier IC consists of an analog input circuit section, switching circuit, a pulse-width modulation circuit, charge pump and gate drive circuit, and an output circuit. All of these circuits, except the pulse-width modulator, require external components for operation. This section focuses on the criteria for determining these external components.

2.1 Input Circuit

The input stage of each channel of the class-D amplifier is a differential amplifier, which means filters are required for both the noninverting and the inverting inputs as shown in Figure 1. These input filters serve two purposes: they set the low frequency corner, f_{LO}, and they block dc voltages and currents.

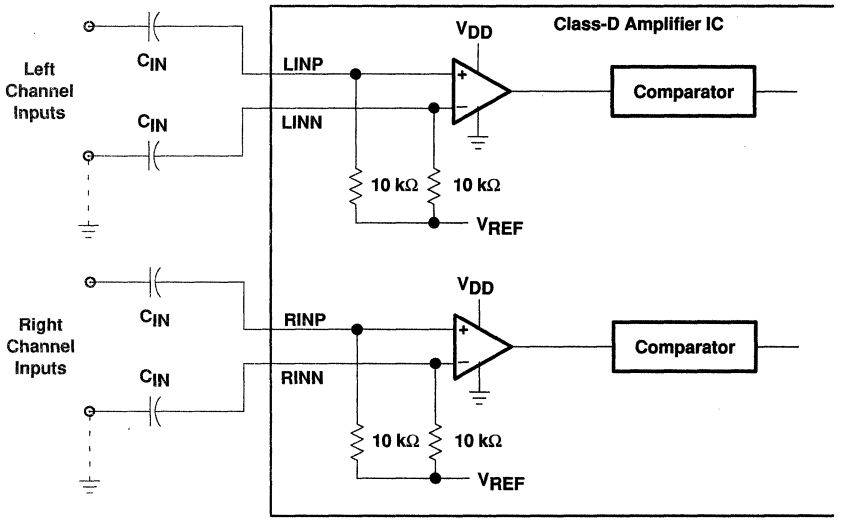

Figure 1. Class-D Input Circuit and Filter

Each filter consists of one external capacitor (C_{IN}) in series with the internal resistance (R_{IN}) of the amplifier input. Such a configuration creates a first-order, high-pass filter (HPF) with a –3 dB cutoff frequency of

$$f_{LO} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \quad (1)$$

where $R = R_{IN} = 10\ k\Omega \pm 20\%$ (typical) and $C = C_{IN} = 1\ \mu F$ for a –3 dB value of 15.9 Hz for the class-D EVMs. The f_{LO} can be easily adjusted by changing the value of C_{IN}.

The inputs can also be driven single-ended by applying the audio input signal to the noninverting input and ac-grounding the inverting input as shown by the dashed line in Figure 1. This is necessary to avoid mismatching the impedance of the two inputs, which creates a differential voltage and a potential for popping in the speakers when power is applied to the system. The capacitor also prevents dc current flow from the internal voltage reference to ground.

The internal gain of the class-D amplifier limits the input voltage to a maximum of

$$V_{IN} = \frac{\sqrt{P_O \cdot R_L}}{A_V} \quad (2)$$

where P_O is the maximum output power, R_L is the dc load resistance, and A_V is the internal gain of the class-D amplifier. The large gain and low input currents of the class-D amplifier reduces the input voltage to much less than 1 V and allows the use of small, ceramic capacitors on the inputs.

The input capacitors should be placed as close to the input pins as possible to reduce noise pickup. Connecting the inputs differentially further reduces the input noise. Surface-mount, ceramic capacitors are readily available in 0805 for X7R and Y5V, and can even be found in 0603 Y5V. Ceramic capacitors are preferred over electrolytic for their small size, low equivalent series resistance (ESR), low noise, and longer life of the component.

2.2 Output Circuit

The class-D amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either fully on or off, which reduces the R_{DSON} and the power dissipated in the device, increasing efficiency. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. There are several options available as to what type of filtering should be used to recover the audio signal. The output may be directly applied to the speaker if the speaker is inductive at the class-D switching frequency and EMI is not an issue, or a half filter could be used.[1] However, for this application it is assumed that EMI is a consideration, and the focus is therefore the full output filter shown in Figure 2.

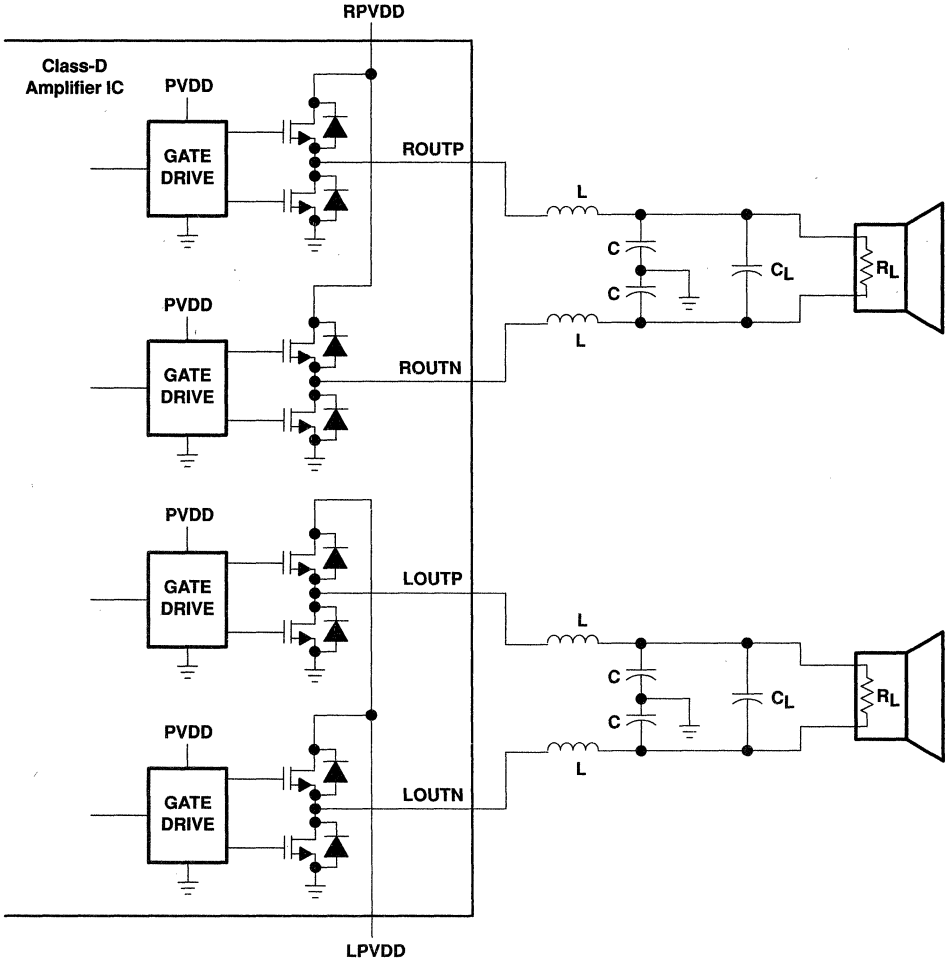

Figure 2. Class-D Output Circuit and Filter

The main goal of the output filter is attenuation of the high frequency switching component of the class-D amplifier while preserving the signals in the audio band. This describes the characteristic of a low-pass filter (LPF), which is specified by its cutoff frequency (–3 dB point), gain and ripple in the pass band, and attenuation in the stop band. The order of the filter determines how many poles exist at the same frequency, with each order increasing the attenuation above the cutoff frequency by –20 dB per decade. The switching frequency (f_S) of the class-D amplifier can influence the choice of the filter order — the higher the f_S, the lower the order required to achieve a given attenuation within a specified passband. This would seem to dictate the use of the highest switching frequency possible. The tradeoff is that increasing f_S increases the switching losses and the EMI, and decreases the efficiency of the amplifier.

A second order LPF reduces f_S by –40 dB per decade to one percent of its prefiltered value. A 5-V signal at 250 kHz is reduced by –40 dB over one decade to 50 mV. If increased attenuation is desired, two alternatives remain; a higher order filter could be implemented, increasing the number of components and the cost, or f_S could be increased, lowering the overall efficiency and increasing EMI.

2.2.1 Filter Design

The output filter is a simple, second-order, LC-type filter designed using a Butterworth approximation. This type of filter is desired for the relatively flat pass-band response it provides and the small number of parts it requires. The transfer function for a second order Butterworth approximation is

$$H(s) = \frac{1}{s^2 + \sqrt{2}\ s + 1} \tag{3}$$

The first step is to realize the circuit and derive the transfer function, beginning with a half circuit model and moving to the full-bridge circuit. The half circuit model of the BTL output is shown in Figure 3, with half of the desired dc load resistance (R_H) of the speaker shown. The input signal (V_{IN}) is the 250-kHz square wave output of the class-D amplifier, while the output (V_O) is the voltage developed across the speaker.

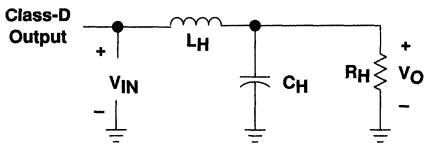

Figure 3. BTL Half-Circuit Model

Converting the inductance and capacitance into S-domain representations (L⇒ Ls and C ⇒ 1/Cs), solving for the transfer function, and manipulating the terms into the form of equation 3 gives the transfer function for the half-circuit model.

$$H(s) = \frac{V_O(s)}{V_{IN}(s)} = \frac{\frac{1}{L_H \cdot C_H}}{s^2 + \frac{1}{R_H \cdot C_H}\, s + \frac{1}{L_H \cdot C_H}} \tag{4}$$

Equating the s terms and the real terms of equations 3 and 4 provide the half-circuit values for C_H and L_H, respectively. These values are for the case where $\omega_0 = 1$ radian per second and should be frequency scaled by dividing through by $\omega_0 = 2\pi f_C$.

$$C_H = \frac{1}{\sqrt{2} \cdot R_H} = \frac{1}{2 \cdot \pi \cdot f_C \cdot \sqrt{2} \cdot R_H} \tag{5}$$

$$L_H = \frac{1}{C_H} = \sqrt{2} \cdot R_H = \frac{\sqrt{2} \cdot R_H}{2 \cdot \pi \cdot f_C} \tag{6}$$

Two half-circuit models are then combined to yield the actual BTL circuit as shown in Figure 4. The capacitors and resistors are then combined to provide the final BTL equations.

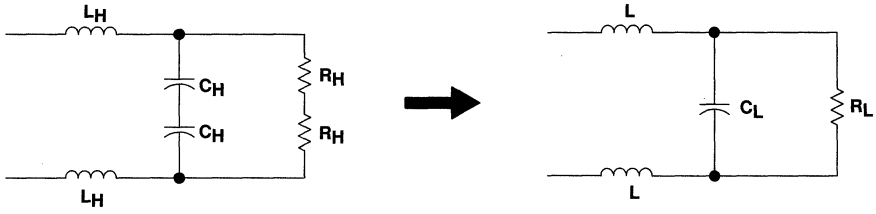

Figure 4. Combination of Two Half-Circuit Models

$$R_L = 2 \cdot R_H \tag{7}$$

$$C_L = \frac{1}{2\sqrt{2} \cdot \pi \cdot R_L \cdot f_C} \tag{8}$$

$$L = L_H = \frac{\sqrt{2} \cdot R_L}{2 \cdot \omega_0} = \frac{\sqrt{2} \cdot R_L}{4 \cdot \pi \cdot f_C} \tag{9}$$

The inductor values actually remain the same for the half- and full-bridge circuit since there are two inductors in the BTL circuit. The –3-dB cutoff frequency for the LC filter, based on the BTL values, is

$$f_C = \frac{1}{2 \cdot \pi \cdot \sqrt{2 \cdot LC_L}} \tag{10}$$

where the $\sqrt{2}$ in the denominator is the result of transposing the values for L and C from the half-circuit model to the full BTL circuit.

Table 1 shows values for L and C_L for a given f_C and R_L.

Table 1. Second-Order Butterworth LC_L Values

DC LOAD RESISTANCE (R_L – Ω)	CUTOFF FREQUENCY (f_C – kHz)	INDUCTOR VALUE (L – μH)	CAPACITOR VALUE (C_L – μF)
4	20	22.5	1.41
4	25	18	1.13
4	30	15	0.94
4	35	12.9	0.80
8	20	45	0.70
8	25	36	0.56
8	30	30	0.47
8	35	26	0.40

The capacitors labeled C in Figure 2 serve as high frequency bypass capacitors, and are empirically chosen to be approximately 10% of $2 \cdot C_L$. Their small value has a negligible impact on the filter cutoff frequency.

The choice of filter components and f_C may dictate the use of a series RC Zobel network placed in parallel with the load.[1] This depends on the Q of the circuit, which changes when a speaker, which is highly reactive, is connected as the load.

2.2.2 Design Example

The class-D audio system will have a passband of 20 Hz to 20 kHz and a switching frequency (f_S) of 250 kHz. The pass-band attenuation of f_S should be 40 dB, and the corner frequency of the LPF will be set to avoid attenuating audio signals by more than 1 dB across the audio spectrum. The speaker dc resistance is 4 Ω. A second-order LC filter is to be used. What inductor and capacitor values are required?

The inductance and capacitance are calculated using the BTL equations:

$$C_L = \frac{1}{2 \cdot \pi \cdot \sqrt{2} \cdot R_L \cdot f_C} = \frac{1}{2 \cdot \pi \cdot \sqrt{2} \cdot 4\Omega \cdot 25\ \text{kHz}} = 1.1\mu\text{F} \quad (11)$$

$$L = \frac{\sqrt{2} \cdot R_L}{4 \cdot \pi \cdot f_C} = \frac{\sqrt{2} \cdot 4\Omega}{4 \cdot \pi \cdot 25\ \text{kHz}} = 18\ \mu\text{H} \quad (12)$$

These values are checked by substituting into equation 10 and found to be correct. Reviewing available component values shows options for L of 15 μH and 22 μH, and the closest value for C_L is 1 μF. The values for C_L = 1 μF and L = 15 μH push the filter cutoff frequency out to 29 kHz.

The filter is now complete, except for the high frequency bypass capacitors labeled C in Figure 2. These capacitors should be approximately 10% of $2 \cdot C_L$, or 0.2 μF. The nearest standard value of 0.22 μF is selected.

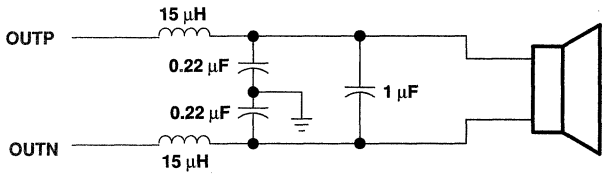

Figure 5. Complete BTL Output FIlter

2.2.3 Component Selection

The output inductors are the key elements in the performance of the class-D audio power amplifier system. The most important specifications for the inductor are the dc resistance and the dc and peak current ratings. The dc resistance directly impacts the efficiency by adding to the total load resistance seen by the power supply. An approximation of the efficiency is

$$\eta = \frac{POUT}{PIN} = \frac{I^2 \cdot R_L}{I^2 \left[2 \left(R_{DSON} + R_{IND}\right) + R_L\right]} \tag{13}$$

where R_L is the dc resistance of the speaker, R_{DSON} is the on resistance of the DMOS power transistors, and R_{IND} is the dc resistance of the inductors.

The inductor current ratings must be high enough to avoid magnetic saturation, which will cause an increase in audio signal distortion or, if completely saturated, will cause the inductor to appear as a short rather than an open circuit to the PWM output. This could potentially damage the device or speakers from the resulting high current surge that may occur during turn on, or the increased quiescent current during normal operation. It would seem best, then, to choose an inductor that has a much higher current rating. The tradeoff is that the size and cost increase as the current capability increases. Shielded inductors will also help reduce distortion and EMI, minimizing crosstalk in the process.

The filter capacitors should be ceramic capacitors with X7R characteristics for stability over voltage and temperature, and can be found in common surface-mount packages as small as 0805. The values of capacitance calculated in the example above are readily available in ceramic chip and metal film capacitor product lines. Measurements have shown little difference between the performance of these two types of capacitors, though some audiophiles will strongly recommend the metal film. The capacitors should be rated to handle the sum of the dc and ac voltages, which will be

$$V_{CAP} = \left(\frac{V_{SUPPLY}}{2}\right) + \left(0.707 \cdot \sqrt{P_{MAX} \cdot R_L}\right) \tag{14}$$

where V_{SUPPLY} is the power supply input voltage, P_{MAX} is the maximum rms power output for the amplifier, and R_L is the dc resistance of the speaker. This is the minimum supply voltage needed, and allowances must be made for temperature, applied voltage, and transient voltage spikes. As a rule of thumb, the voltage rating should be twice what is calculated.

2.3 Charge Pump Circuit

The charge pump circuit consists of one or more external charge pump capacitors, an external charge storage capacitor, and an internal circuit that controls the flow of charge in the circuit. Figure 6 shows the internal and external components and functions that make up a tripler charge pump circuit where C_{CP1} and C_{CP2} are the charge pump capacitors and C_{VCP} is the charge storage capacitor.

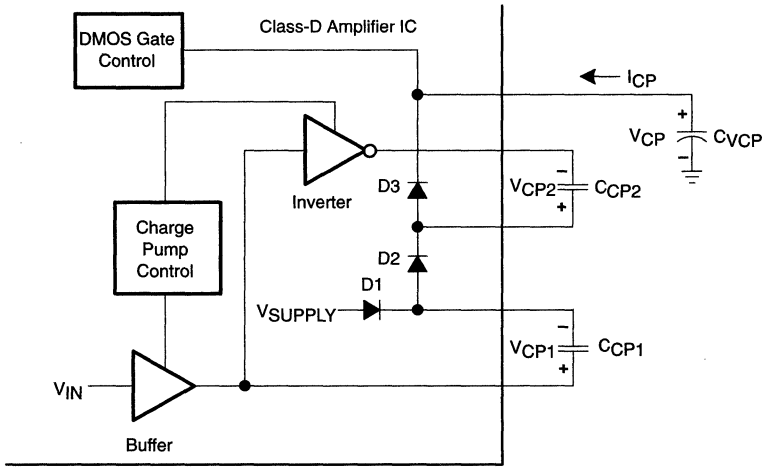

Figure 6. Tripler Charge Pump Circuit

V_{IN} is a switching waveform that transitions between V_{SUPPLY} and 0 V. When V_{IN} is low, the output of the buffer is low, D1 is on, and C_{CP1} charges to V_{SUPPLY}. The inverter then provides a high output voltage to C_{CP2}, D2 remains off, preventing any charge transfer from C_{CP1} to C_{CP2}, and D3 turns on. Charge is then shared between C_{CP2} and C_{VCP}. When V_{IN} goes high the buffer output goes high, and the voltage across C_{CP1} becomes $(2 \cdot V_{IN})$, turning D1 off. The inverter output simultaneously provides a low output to C_{CP2}, turning D2 on and D3 off. Charge from C_{CP1} is then shared with C_{CP2}. This process continues until the charge builds up and V_{CP} is in the operational range of $(V_{SUPPLY} + 6V)$ to $(3 \cdot V_{SUPPLY})$ for a charge tripler, and $(V_{SUPPLY} + 6V)$ to $(2 \cdot V_{SUPPLY})$ for a charge doubler. The charge from C_{VCP} is then used to drive the DMOS output transistor gates.

The value for V_{CP} must be large enough to supply the charge required by the DMOS gate capacitance, yet small enough to fully charge within one-half of the class-D switching period. If these conditions are not met, C_{VCP} fails to fully charge during each switching cycle the $R_{DS(ON)}$ can increase substantially and degrade the operation of the DMOS output transistors.

The proper capacitance is recommended in the device data sheets and in evaluation module user guides. The values required for these capacitors are relatively small and are readily available in surface-mount ceramic chips. The capacitors must be relatively stable over the expected operating temperature. Good quality X7R, ±10% ceramic capacitors should be used with voltage ratings greater than the maximum voltage of the charge pump, V_{CP}, stated in the device data sheets. Power dissipation is not a factor in this circuit as the currents are low and the frequency of operation is high.

2.4 Switching Circuit

The switching circuit consists of a ramp generator and compensation capacitors for each channel. These circuits all require external capacitors in order to function. Selection of these capacitors is important for providing a balanced triangular waveform and accurate regulation of the duty cycle for the output transistors. The switching circuit is identical for each channel of the class-D amplifier. Figure 7 shows the switching circuit for the right channel.

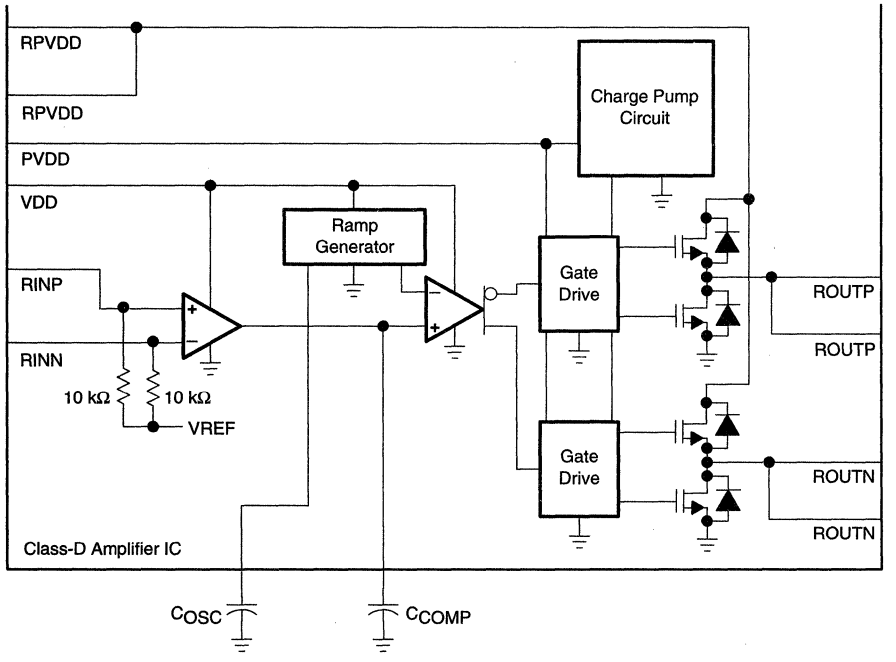

Figure 7. Switching Circuit for the Right Channel

The ramp generator is the heart of the class-D amplifier — it sets the operational frequency for the system from 100 kHz to 500 kHz. Oscillator capacitor C_{OSC} charges and discharges at a constant rate with an applied constant current to form a triangular waveform that is applied to one input of the comparator. The capacitance is directly proportional to the period — doubling the capacitance doubles the length of the period, decreasing the switching frequency (f_S). The data sheets and EVM user guides provide the value of capacitance required to generate a nominal f_S of 250 kHz. Knowing the value of this capacitance (C_{250}), f_S, and the desired switching frequency, the new capacitance, C, can be easily calculated for any desired frequency of oscillation, f, from the ratio of two capacitors as shown in equation 15.

$$C_{OSC} = C_{250} \cdot \left(\frac{f_S}{f}\right) \tag{15}$$

The compensation capacitors, C_{COMP} are used to stabilize the comparator inputs and should be identical to C_{OSC}. Ceramic capacitors with C0G temperature characteristics are the common type available in such a small capacitance. These capacitors do not exhibit a change in value with changing ac or dc voltages, and are extremely stable over large temperature ranges. A standard 50-V C0G-type capacitor with a maximum of ±5% tolerance is recommended, with much tighter tolerances available if desired.

3 Headphone Circuit

Some of the class-D amplifier ICs feature class-AB headphone (HP) amplifier circuits capable of driving 50 mW of power into a 32-Ω load from a 5-V supply. TTL-compatible interface logic (a mode pin) is provided to select between class-D or class-AB modes of operation. Each HP channel consists of an internal operational amplifier and pins for connecting external components that control the gain and filtering for the headphones.

Class-D EVMs are available that integrate the HP amplifier functions. A typical channel of the HP circuit for such an EVM is shown in Figure 8. External pins on the EVMs allow easy connections to the inputs and outputs, and a miniature headphone jack has been provided on the EVM board for easy testing of the HP amplifier. The HP jack includes the control pins necessary to control the IC mode. An onchip regulator provides the 5 V required for operation of the HP amplifier circuit. The power decoupling capacitor, C, is discussed in the *Device Power Supply Decoupling* section of this report. Capacitor C_{V2P5} stabilizes the HP circuit, and should be the size recommended in the data sheets and the EVM user guides.

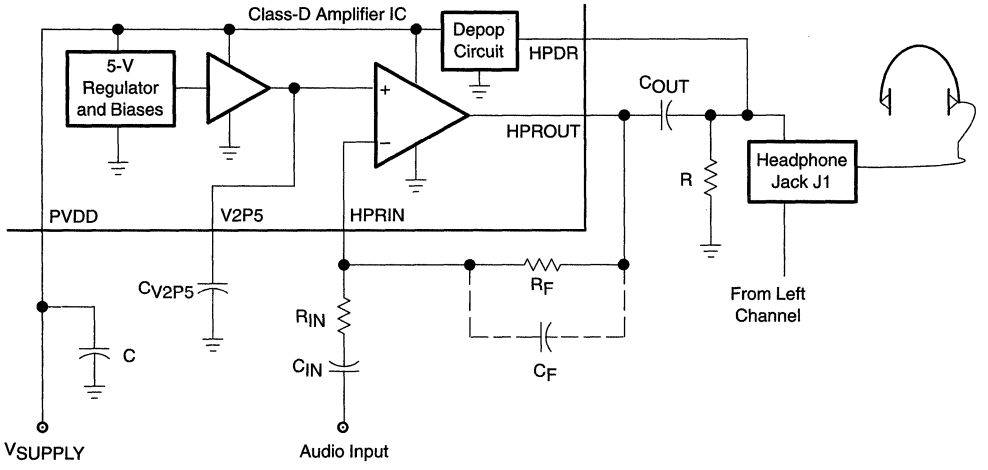

Figure 8. Headphone Amplifier Circuit, Right Channel

Each amplifier is configured as an inverting operational amplifier with externally controlled gain. The transfer function for this circuit, ignoring C_{OUT}, R, and any load resistance, R_L, is shown in equation 16 where $\omega_1 = (C_F \cdot R_F)^{-1}$ and $\omega 2 = (C_{IN} \cdot R_{IN})^{-1}$.

$$H(j\omega) = \frac{V_O}{V_{IN}} = \frac{\left(-\frac{R_F}{R_{IN}}\right)}{\left(1 + \frac{\omega_1}{j\omega}\right)\left(1 + \frac{j\omega}{\omega_2}\right)} \quad (16)$$

Input capacitor C_{IN} serves to ac-couple the input. The series combination of R_{IN} and C_{IN} in this circuit creates a LPF function in the denominator, which then acts as a HPF to set the low frequency corner shown in equation 17, where R = R_{IN} and C = C_{IN}. f_{LO} can be easily adjusted by changing C_{IN} or R_{IN}.

$$f_{LO} = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{17}$$

Capacitor C_F is recommended for stability purposes when the gain is greater than or equal to –10 V/V. The parallel combination of R_F and C_F then creates a HPF function which, when in the denominator, acts as a LPF to set the high frequency corner (f_{HI}) of the circuit. equation 17 may be used to calculate f_{HI}, with R = R_F and C = C_F. This corner frequency should be about 300 kHz, well above the audio band.

Capacitor C_{OUT} is required for all single-ended audio circuits to ac-couple the output, preventing dc current from flowing into the HP. C_{OUT} forms another LPF in conjunction with the dc resistance (R_L)of the headphones. Resistor R may be included if the IC mode control interface is implemented with the HP jack, and is much larger than R_L and can be ignored in this analysis. The class-D EVMs with HP amplifiers use such a circuit. equation 17 is again used to calculate the low frequency corner for this filter. It should be noted that the corner frequencies of the input and output filters will overlap to some degree.

The HP circuit includes some internal depop circuitry that is used to minimize the pop in the speakers when the HP is activated and deactivated. The largest capacitor that is recommended for use with this circuit is 33 µF. Higher values may be used, but will decrease the effectiveness of the depop circuit.

Ceramic capacitors are available for the small values of capacitance used for the input and feedback path. The voltage rating of the input capacitor will depend upon the gain of the circuit, which should be greater than the passband gain (A_V) in equation 18.

$$A_V = \left| \frac{R_F}{R_{IN}} \right| \tag{18}$$

This is then used to calculate the maximum input voltage in equation 19.

$$V_{IN} = \frac{5V}{A_V} \tag{19}$$

The voltage rating of the feedback capacitor should be a minimum of 5 V, and is readily available in a ±5% C0G package for such a low capacitance. The input capacitors are larger and available in a ±10%, X7R package, depending upon the value.

4 Control and Indicator Circuits

The Texas Instruments class-D audio power amplifiers have three main control input pins (shutdown, mute, and mode) for external control of chip functions. Each of these inputs is TTL compatible to allow easy interface with logic. The shutdown and mute controls are provided with each class-D device, while the mute control is only applicable to devices that incorporate a class-AB headphone amplifier.

Two indicator pins (fault0 and fault1) are also provided to allow monitoring of chip status. They provide feedback when an under-voltage, over-current, or thermal fault exists. These pins are provided on each of the devices.

4.1 Shutdown

The shutdown control pin allows the device to be placed into a power-saving sleep mode to minimize current consumption. This pin is TTL active low — a voltage of less than 0.8 V at this pin will shut down the entire device. The device will become active when the voltage at the pin rises above 2 V. When in shutdown, the IC draws a maximum quiescent current that is less than 1 μA.

In typical applications, as often found in notebook computers, portable audio products, and such, the internal speakers mute when headphones are plugged into the headphone jack, or internal speakers mute when external speakers are connected. In applications using separate speaker and headphone amplifiers, the one not being used can be shut down to conserve power.

4.2 Mute

The mute control pin turns on the low-side output transistors, shorting the load to ground and muting the outputs of the device. This pin is TTL active low — a voltage of less than 0.8 V will mute the device outputs. The outputs will turn on when the voltage at the mute pin rises above 2 V. When muted, the class-D device draws only a few mA of quiescent current.

4.3 Mode

The mode control pin selects either the class-D or the headphone amplifier as the active amplifier, placing the inactive amplifier in a power-saving sleep mode. This pin is TTL compatible, with a voltage less than 0.8 V activating the class-D amplifier, and a voltage greater than 2 V activating the headphone amplifier.

This function can easily be controlled with a headphone jack that contains an internal switch to change the state of the control line, and has been successfully implemented on the EVMs for the class-D amplifiers that integrate headphone circuits. Figure 9 shows an example of this type of circuit.

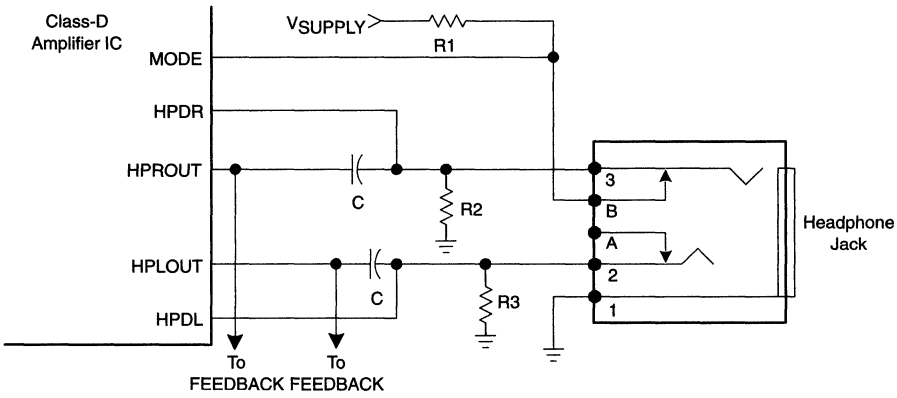

Figure 9. Mode Control Circuit Featuring Headphone Jack Control

Resistors R1 and R2 form a divider network when a headphone plug is not inserted into the headphone jack. The ratio of these resistors should be such that the mode pin is held below 0.8 V to activate the class-D amplifier. When a headphone plug is inserted into the jack, contact B is disconnected from pin 3 of the jack and no current flows through R1, causing the mode pin to float to V_{SUPPLY}. This deactivates the class-D amplifier and activates the headphone amplifier. Removal of the headphone plug from the jack then connects contact B to pin 3 and pulls the MODE pin low, causing the device to revert to class-D operation. Resistor R3 is included in the remaining channel to balance the outputs of the two channels when the headphone amplifier is active.

4.4 Fault Indicators

Two fault indicator pins on the class-D amplifier IC provide feedback when a fault condition exists. Signals on these pins indicate the status of the class-D amplifier: operational, over-current, thermal fault, and under-voltage lockout. The only status reported for the class-AB headphone amplifier is for a thermal fault, which is indicated by the same error code as for the class-D amplifier. The device data sheets list the error codes for each of these conditions.

The TTL-compatible fault pins are connected to open drain outputs and require a pullup resistor to limit the current flow into the pins to a maximum of 1 mA. Once a fault is triggered, the appropriate fault pins remain active until the fault is cleared by cycling the shutdown pin, mute pin, or the power supply to the device.

5 Device Power Supply Decoupling

Adequate delivery of power and proper grounding reduces distortion and ensures correct operation of the class-D device. Power supply filtering and appropriate ground connections are discussed below.

Power supply filtering has two objectives: decouple the power supply from the class-D amplifier and provide a path for high frequency noise to bypass the device. There are three main power inputs for the device: class-D analog input and controls (VDD), charge pump and headphone (PVDD), and the output (RPVDD and LPVDD). Figure 10 shows the power bus and recommended filtering for a class-D audio power amplifier.

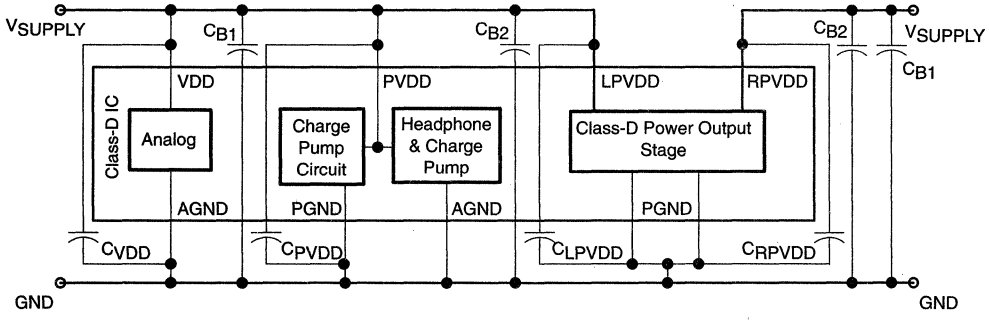

Figure 10. Class-D Power Bus, 48-Pin TSSOP Package

All of the capacitors connected to the power bus (V_{SUPPLY}) are working to decouple the circuit from the power supply. The large bulk capacitors (C_{B1} and C_{B2}) are provided for each channel to supply the majority of the switching current required by the amplifier. Smaller capacitors (C_{VDD}, C_{PVDD}, C_{LPVDD}, and C_{RPVDD}) are placed adjacent to the various power pins to supply the initial charge of the switching current. The only power pins located on the right side of the chip (RPVDD) are for the high power output section of the right channel. The remaining power pins (VDD, PVDD and LPVDD) are located on the left side of the chip and will be the focus of the discussion. The right channel capacitors will then be identical to those of the left channel.

5.1 Bulk Capacitors

Real-world capacitors are modeled using parameters such as equivalent series resistance (ESR), equivalent series inductance (ESL), capacitive reactance (X_C) and inductive reactance (X_L). The equivalent impedance of a capacitor over frequency is simply modeled by

$$Z = \sqrt{ESR^2 + (X_C - X_L)^2} \tag{20}$$

X_L is small for frequencies below 1 MHz and can be neglected since the switching frequency range of the TPA005D14 is 100 kHz to 500 kHz. The capacitive reactance is maximum and dominates at dc. It decreases as the frequency increases until resonance is reached ($X_C = X_L$), at which point Z = ESR. The ESR of a capacitor is considered to be constant over the 100 kHz to 500 kHz switching frequency range of the class-D amplifier, and is usually provided by the manufacturer.

The values for the bulk capacitors C_{B1} and C_{B2} are the primary concern, and are calculated using the circuit shown in Figure 11. It is assumed that L_{IN} is large (steady current flows from the power supply) and has a negligible ripple, the capacitor current for C is negligible, and the switching frequency and dc load resistance is known.

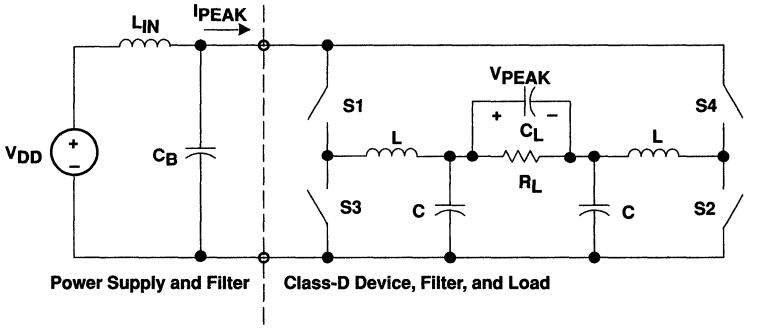

Figure 11. Power Supply Bulk Decoupling Capacitor Circuit

The peak power for a given load is then used to calculate the peak voltage, which is then used to calculate the peak current.

$$V_{PEAK} = \sqrt{P_{PEAK} \cdot R_L} \tag{21}$$

$$I_{PEAK} = \frac{V_{PEAK}}{R_L} \tag{22}$$

This current flows from C_B through S1, the load, and S2 to ground. The minimum capacitance required to supply this peak switching current is

$$C = \frac{I_{PEAK} \cdot T_D \cdot D_{MAX}}{V_{RIPPLE}} \tag{23}$$

where $T_D = 1/f_{switch}$ is the period, D_{Max} is the maximum duty cycle, and V_{Ripple} is the desired ripple voltage, or droop, that will appear at the output of the amplifier. This is the capacitance required to limit the ripple voltage based on the capacitance alone. In most every case, the ripple voltage caused by the ESR will dominate. The maximum ESR required to achieve the same V_{Ripple} for the same I_{Peak} from equation 22 is calculated in equation 24 below.

$$ESR = \frac{V_{RIPPLE}}{I_{PEAK}} \tag{24}$$

The total ripple voltage contributed by the bulk capacitor C_B is the sum of equations 23 and 24. The requirements of the application will determine the acceptable tradeoffs in the selection of components that meet these criteria. It should be noted that the total ripple voltage seen at the output of the class-D amplifier will be approximately equal to that calculated in equation 25.

$$V_{RIPPLE}^{MAX} = I_{PEAK}\left[\left(\frac{T_D \cdot D_{MAX}}{C}\right) + ESR + R_{DS(ON)}\right] \quad (25)$$

There are various ways to implement the bulk capacitance that is selected: one large capacitor that meets the requirements of both equations (23) and (24) can be used; two or more capacitors can be paralleled to reduce the ESR and the size of the capacitors; or two different types of capacitors can be used to supply the current and meet the ESR specifications. Keep in mind that the ESR of the actual capacitor used should be 30% – 50% lower than the calculated value to allow for increases due to temperature, ESL, and aging.

Electrolytic capacitors, aluminum or tantalum, are the best choice right now for large capacitance requirements, though ceramic capacitors of up to 100 μF are being produced in low voltage packages. The electrolytic capacitors are normally useful for applications below 1 MHz. This is due to their low resonant frequency and is the reason for using smaller, ceramic capacitors in parallel with the electrolytic. Electrolytic capacitors, in particular the tantalum type, are subject to damage by stress from exceeding the voltage rating. They must be chosen such that they will retain the minimum required capacitance and maximum ESR over the entire temperature range and for the voltage range to avoid damage and early failure of the components. The voltage rating should be greater than the sum of the supply voltage and the total maximum ripple voltage of equation 24.

5.2 Small Decoupling Capacitors

The large capacitance of C_{B1} and C_{B2} means a slower response time due to the large time constant formed with the resistance of the circuit, and is why the smaller capacitors C_{VDD}, C_{PVDD}, C_{LPVDD} and C_{RPVDD} are used. These capacitors provide a smaller time constant for a much quicker discharge time, and supply the initial transient charge required for the high frequency switching pulses of the class-D amplifier. Their low value pushes the resonant frequency of the capacitor out — they appear capacitive at much higher frequencies due to the smaller X_L of equation 20. This serves to bypass unwanted high frequency signals.

The current for the VDD pin is very low and can have the transient requirements satisfied by a 0.1 μF or 1 μF capacitor. The PVDD pin will draw less than 100 mA of current and should have a 1-μF decoupling capacitor. These must have a voltage rating that is greater than the sum of the supply voltage and the maximum ripple voltage of equation 25.

The values required for these capacitors are small and readily available in surface-mount ceramic chips. The capacitors should be relatively stable over the expected operating temperature. Good quality X7R, ±10% ceramic capacitors are available for the capacitance required, though ±20% or +80/–20% Y5V capacitors may be used, depending upon the application. Power dissipation is a factor in this circuit as the currents can be quite high.

6 PCB Layout

Good layout practices and well thought out design provide excellent performance for the TI class-D audio power amplifiers. There are three main areas of concern in the layout: the ground plane, power plane, the inputs and the outputs. Each is discussed briefly below. See the TI website for more information on class-D layouts.

6.1 Ground Plane

Experimentation with several types of ground planes has shown that, with some careful planning and good layout practices, a solid ground plane works as well as other types of grounding schemes. This is due in part to the relatively low frequencies of operation for the system, and to the careful layout of the components and traces. The solid ground plane also serves to assist the PowerPAD^2 in the dissipation of heat, keeping the class-D amplifier relatively cool and negating the need for an external heat sink. Connection to the PowerPAD is discussed later in this section. Finally, the ground plane can act as a shield to help isolate the power pins from the output, reducing the impact of EMI on the traces and pins.

It is important that any components connecting an IC pin to the ground plane be connected to the nearest ground for that particular pin. Table 2 lists the ground pins for the various sub-circuits that are part of the TPA005D14 class-D IC to assist in determining where a component should be grounded. Care should be taken to prevent the ground return path of any high current components (such as the output filter capacitors) from directly passing through other ground connections of the IC, particularly the input.

Table 2. Audio Power Amplifier Subcircuit Ground Pins

GROUND PIN No.	APPLICABLE CIRCUITS	TPA005D14 RELATED PINS†
47	Controls (shutdown, mute, mode)	1, 2, 3
	Class-D outputs	4, 5, 44, 45
	Ramp generator	6, 43, 48
	Grounds	7, 46
	Input power (VDD)	8
	Fault indicators	41, 42
12, 13, 36, 37	Output power (LPVDD, RPVDD)	9, 16, 33, 40
	Class-D outputs	10, 11, 14, 15, 34, 35, 38, 39
20	Headphone	17, 18, 19, 23, 26, 29, 30, 31, 32
27	Charge pump	21, 22, 23, 24, 25, 26, 28

† Pin numbers may vary in other class-D devices.

6.2 Power Plane

There are three main power sections on the chip: the input circuit power pins (VDD), the output stage power pins (LPVDD and RPVDD), and the power for the headphone and charge pump circuits (PVDD), as shown in Figure 9. When the device is operating (i.e. audio is being applied to the amplifier), the VDD pin draws only a few mA of current and the PVDD pins draw several tens of mA. This is in sharp contrast to the amps of current drawn by the LPVDD and RPVDD pins.

The power traces are kept short and the decoupling capacitors placed as close to the power pins as possible. This is particularly true for the small decoupling capacitors that are to be placed adjacent to each IC power pin. Terminate the capacitor ground close to the ground for the particular power section as possible while paying attention to ground return current paths. This minimizes ground loops and provides very short ground return paths and high frequency loops.

The VDD pin supplies power for sensitive analog circuitry and is the most sensitive pin of the device. It must, therefore, be kept as noise free as possible. The demand for peak current is small and mostly satisfied by the charge of the small decoupling capacitor. The PVDD pin(s) are not as sensitive to noise as the VDD pin. They supply the current for the headphone regulator and control circuits when the device is in class-AB mode (when applicable), and the charge pump circuit when in class-D mode. The power traces for these power inputs should be connected to the main power bus at a point near the large decoupling capacitor(s). The small inductance of the traces and the charge supplied by the large decoupling capacitor greatly reduces the ripple current of the main power bus seen by these pins. Terminate the capacitor ground side close to the ground for the particular power section while paying attention to ground return current paths. Again, this minimizes ground loops and provides very short ground return paths and high frequency loops.

The main power bus should terminate into the LPVDD and RPVDD pins, with the small decoupling capacitors for each channel placed adjacent to each pair of pins. When more than one bulk capacitor is used, place the smaller of the two between the power pins and the large bulk capacitor. These traces should be wide enough to handle the maximum peak current per channel over the operating temperature range, and symmetric to facilitate even power distribution. Place them directly over the ground plane to reduce EMI and minimize the ground return path.

6.3 Inputs and Outputs

The pinout of the class-D amplifiers facilitates the separation of the inputs and outputs, enabling isolation of ground return paths and high frequency loops. The class-D and headphone amplifier input traces should be kept as short as possible between the ac coupling capacitors and the amplifier IC input pins to reduce noise pickup. Keep the inputs separated from the outputs, particularly from the inductors if unshielded units are used, to minimize magnetic coupling. The headphone traces may be in close proximity with the class-D output since the two amplifiers are not active at the same time.

The control (shutdown, mute, and mode) input pins have almost no current flow through them, and inductance and resistance of the traces is of a minimal concern. The indicator output pins (fault0 and fault1) have less the 1 mA of current flow, and should be sized accordingly. There are no special considerations for the layout of these traces — standard layout practices will apply.

It is critical to minimize the trace lengths between the device class D output pins and the LC filter components, particularly those that contain the full square wave. The traces to the inductors should be kept short, yet separated from the input circuit as much as possible. Routing the pre-inductor output traces of a particular channel (i.e., ROUTP and ROUTN) on adjacent layers so that they overlap will cause the magnetic fields to subtract from each other, reducing the EMI. All high-current output traces should be wide enough to allow the maximum peak current to flow over the entire operating temperature range of the system. Failure to do so will create excessive voltage drops, a decrease in efficiency, and an increase in distortion.

6.4 General PowerPAD Considerations

The class-D IC is mounted in a special package that incorporates a thermal pad designed to transfer heat from the silicon die of the IC directly to the PCB. The PowerPAD™ package is constructed using a downset leadframe. The die is mounted on the leadframe with the chip ground tied to the pad through a low impedance. The bottom surface of the leadframe is exposed and serves as a metal thermal pad on the underside of the IC package. This metal is then soldered directly to the PCB, providing direct contact between the die and the PCB etch, which, in turn, provides an exceptional thermal transmission path. Excellent thermal performance can then be achieved by providing this thermal path on the PCB.

The following steps illustrate the recommended approach to properly heatsink a TI class-D audio power amplifier 48-pin DCA package that integrates the PowerPAD with a circuit board.

1. Prepare the PCB for proper connection to the class-D IC with a top layer etch pattern as shown in Figure 12. Etch should be provided for both the IC leads and the PowerPAD.

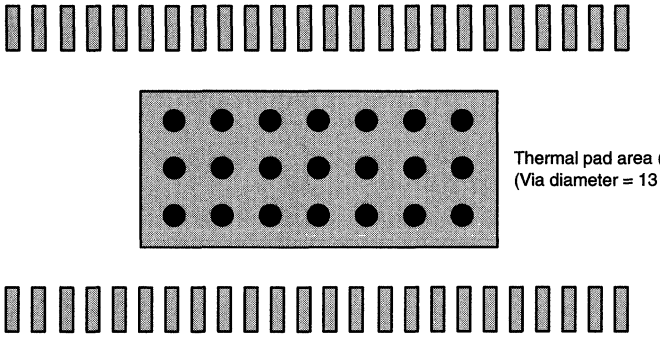

Figure 12. PowerPAD PCB Etch and Via Pattern

2. Place 21 vias evenly spaced in three rows (seven per row) in the area for the PowerPAD. These vias should be 13 mils in diameter to minimize solder wicking through the holes during reflow soldering, ensuring a good connection between the IC thermal pad and the PCB etch.
3. Additional vias may be placed anywhere along the thermal plane outside of the PowerPAD area to assist with heat dissipation. These vias are not restricted to the 13 mils of step 2 since they are not used to connect the IC to the PCB.
4. Connect all of these vias to the PCB ground plane. The ground plane now becomes the heatsink for the amplifier IC.
5. Do not use a web or spoke connection when connecting these vias to the ground plane. Web connections have a high thermal resistance that is used to slow heat transfer to the ground plane, making soldering of these vias easier. This would impair the flow of heat between the PowerPAD and the circuit board ground plane and is not recommended.
6. The solder mask on the top layer should then leave the etch pads for the IC pins and PowerPAD exposed. The bottom layer solder mask should, however, cover the entire thermal pad as well as the via edges, leaving tiny holes in the very center of each via. This prevents the solder connecting the IC thermal pad to the PCB from being wicked away during reflow.
7. Apply solder paste to the exposed etch pads for the IC pins and PowerPAD.
8. The class-D IC is then soldered in position during the reflow process. Actual thermal performance achieved with the package will depend upon the application. The Texas Instruments Technical Brief, *PowerPAD Thermally Enhance Package*, Literature Number SLMA002, contains more information on the PowerPAD package and its thermal characteristics.

7 References

[1] The Texas Instruments application report, *Reducing and Eliminating the Class-D Output Filter*, literature number SLOA023.

[2] The Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package*, literature number SLMA002, contains more information on the PowerPAD package and its thermal characteristics.

Mono Configuration of the TPA005D02 Class-D Audio Power Amplifier Application Report

Literature Number: SLOA028
July 1999

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Mono Configuration of the TPA005D02 Class-D Audio Power Amplifier

Edward A. Thomas

ABSTRACT

Class-D Audio Power Amplifiers (APAs) are becoming an extremely popular choice for audio solutions in battery-powered applications. The increased efficiency and reduction in heat dissipation of a Class-D APA versus that of a Class-AB APA allows the battery life on an application to be extended. The TPA005D02 is monolithic stereo Class-D APA offered from Texas Instruments. This document discusses how to configure the TPA005D02 to be used in a mono configuration. The actual specifications of the TPA005D02 can be found in the published Texas Instruments data sheet (literature #SLOS227A).

Design Problem

Many battery-powered applications would like to take advantage of the increased efficiency of the TPA005D02 APA but do not need stereo output. This document will show the specific application circuit in a mono configuration. The use of this device in the mono configuration saves board space, cost, and supply current when compared with the same device used in a stereo configuration.

Solution

The use of the TPA005D02 APA in the mono configuration eliminates the need for many of the surrounding components required to operate the device in the stereo configuration. The schematic for the TPA005D02 APA is in the TPA005D02 *Evaluation Module User's Guide* (literature #SLOU032A). The modifications needed to be made to the evaluation board for the mono configuration of the TPA005D02 are shown in the schematic shown in Figure 1.

The TPA005D02 APA integrated circuit consists of two separate amplifiers inside the device, one for the right channel and one for the left channel. To operate in the mono configuration, only one of the two amplifiers inside the TPA005D02 will be used. The TPA005D02 has two pins (LCOMP and RCOMP) that can be used to shut down power to the respective amplifier. Tying the respective xCOMP to GND will stop the bridge from switching and will save quiescent power of the device. In this document, the left amplifier will be shut down to allow operation of the device in the mono configuration. In order to shut down the left amplifier, LCOMP (pin 43) and input pins LINP (pin 5) and LINN (pin 4), will be tied directly to GND (see Figure 1). The operation of this device in the mono configuration eliminates ten external components when compared with use of this device in the stereo configuration. The capacitors on the inputs of the unused amplifier and on the xCOMP will be eliminated from use in the mono configuration. The two inductors and three capacitors on the output of the unused amplifier will also be eliminated.

The V_{DD} power supply pin sets for both amplifiers in the TPA005D02 must be connected even though one amplifier (left in this example) is shut down. No power will be pulled by the unused amplifier. The V_{DD} supply pin sets are connected through a guard ring internally, the device can be destroyed if only one supply pin set is connected. The unused amplifier (see Figure 1) will not pull large current transients through the power pins, therefore the 1 μF bypass capacitor (C13) on the LPV_{DD} (pin 16) can be replaced with a 0.1 μF ceramic capacitor (shown). The bypass capacitors C15 (220 μF) and C11 (10 μF) on the unused channel may be removed. The output pins LOUTP (10, 11) and LOUTN (14, 15), for the unused amplifier, will be left floating.

The MUTE and FAULT features of the TPA005D02 will operate normally in this mono configuration. The two detectable fault conditions are the charge pump under-voltage lock-out condition and the thermal fault condition. More details on the functionality of these features can be found in the product's data sheet.

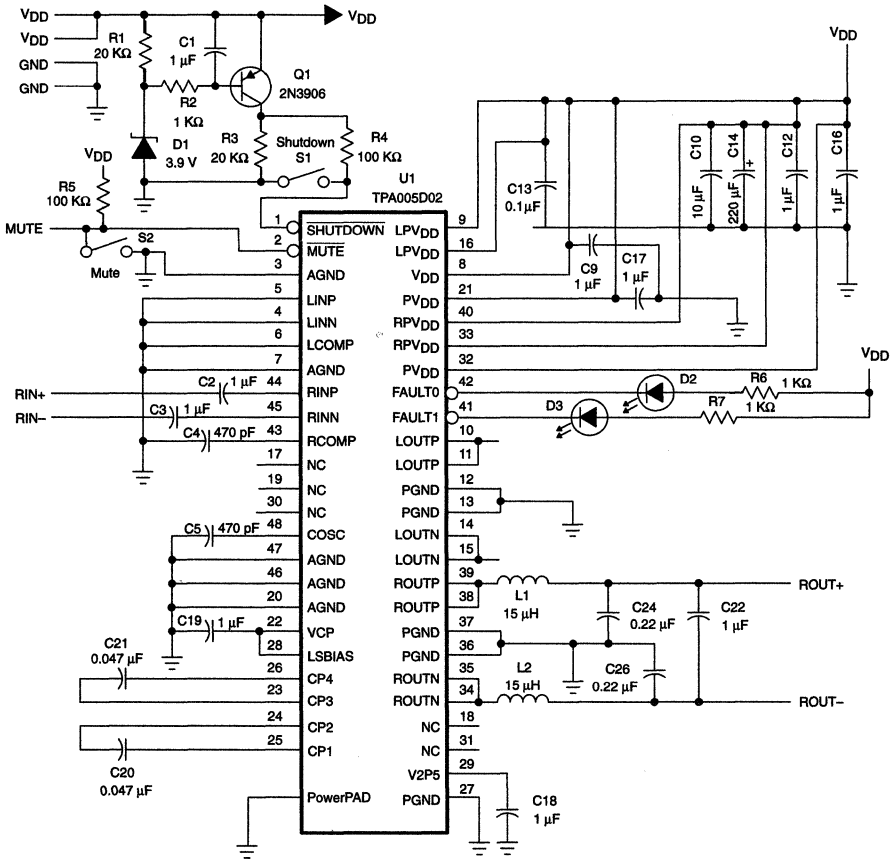

Figure 1. TPA005D02 Class-D EVM Schematic Diagram for Mono Configuration

Conclusion

The Class-D APA is an effective, highly efficient, audio solution for many battery-powered applications. A comparison of class D amplifier versus linear amplifier supply current is included in the TPA005D02 datasheet. The results at normal listening levels show the linear amplifier to have three times the current draw of the class D device. This comparison is important in showing the selection of the type of audio amplifier used in a battery-powered system can extend battery life by three times, if a class-D amplifier is used. Offering flexibility in the way to configure the TPA005D02 allows both mono and stereo configurations the advantage of this increased efficiency in battery-powered systems. This allows use of this device in many different applications that could benefit from Texas Instruments, Class-D technology.

PowerPAD Thermally Enhanced Package

TECHNICAL BRIEF: SLMA002

Mixed Signal Products

Semiconductor Group
21 November 1997

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PowerPAD Thermally Enhanced Package

Abstract

The PowerPAD thermally enhanced package provides greater design flexibility and increased thermal efficiency in a standard size IC package. PowerPAD's improved performance permits higher clock speeds, more compact systems and more aggressive design criteria.

PowerPAD packages are available in several standard surface mount configurations. They can be mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. This document will focus on the specifics of integrating a PowerPAD package into the PCB design.

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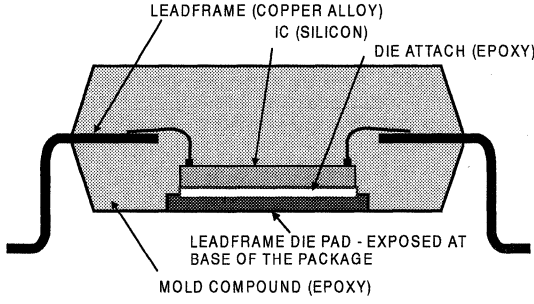
1. Introduction

The PowerPAD concept is implemented in a standard epoxy-resin package material. The integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance (Θ_{jc}) path between the IC junction and the exterior of the case. Because the external surface of the leadframe die pad is on the PCB side of the package, it can be attached to the board using standard flow soldering techniques. This allows efficient attachment to the board, and permits board structures to be used as heat sinks for the IC. Using vias, the leadframe die pad can be attached to a ground plane or special heat sink structure designed into the PCB. For the first time, the PCB designer can implement power packaging without the constraints of extra hardware, special assembly instructions, thermal grease or additional heat sinks.

Figure 1. Schematic Representation of the PowerPAD Package Components



Section View of a PowerPAD(tm) PACKAGE

Because the exact thermal performance of any PCB is dependent on the details of the circuit design and component installation, exact performance figures cannot be given here. However, representative performance is very important in making design decisions. The data shown in Table 1 is typical of the performance that can be expected from the PowerPAD package.

Table 1. Typical Power Handling Capabilities of PowerPAD Packages

Package Type	Pin Count	Standard Package	PowerPAD Package
SSOP	20	0.75 W	3.25 W
TSSOP	24	0.55 W	2.32 W

Notes: 1) Assumes 150° C junction temperature and 80° C ambient temperature.
2) Values are calculated from Θ_{ja} figures shown in Appendix A.

For example, the user can expect 3.25 watts of power handling capability for the PowerPAD version of the 20-pin SSOP package. The standard version of this package can only handle 0.75 watts. Details for all package styles and sizes are given in Appendix A.

2. Installation and Use

2.1 PCB Attachment

Proper thermal management of the PowerPAD package requires PCB preparation. This preparation is not difficult, nor does it use any extraordinary PCB design techniques, however it is necessary for proper heat removal.

Figure 2. Bottom and Top View of the 20 pin TSSOP PowerPAD Package

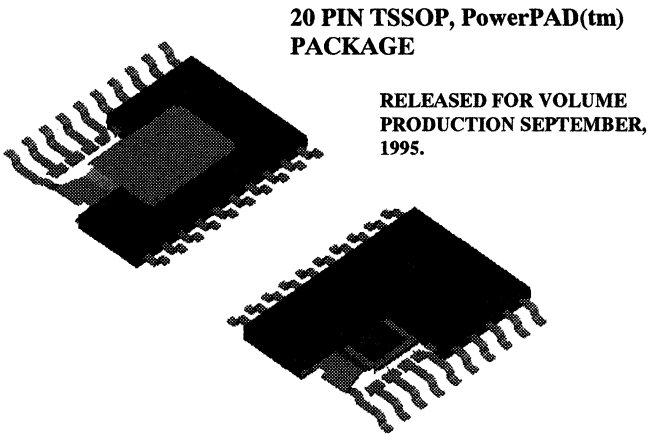
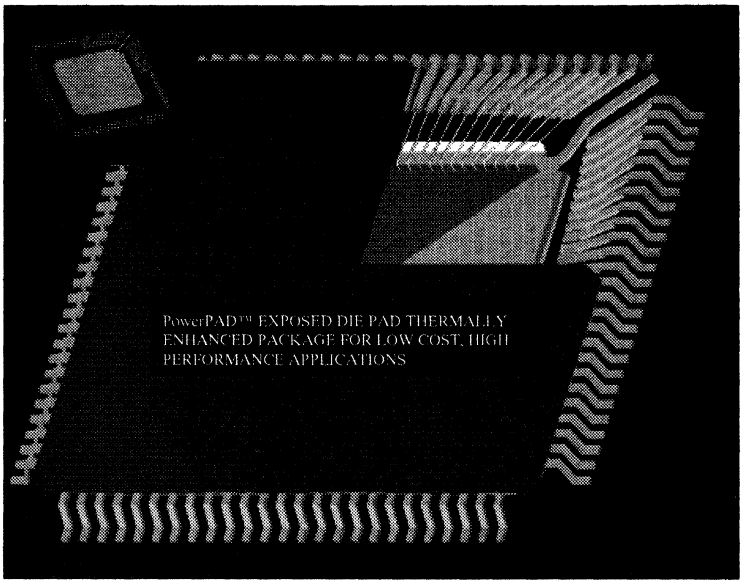


Figure 3. 64 Pin, 14 x 14 x 1.0mm Body TQFP PowerPAD Package



All of the thermally enhanced packages incorporate features that provide a very low thermal resistance path for heat removal from the integrated circuit - either to and through a printed circuit board (in the case of zero airflow environments), or to an external heatsink. The TI PowerPAD implementation does this by creating a leadframe where the bottom of the die pad is even with a surface of the package (as opposed to the case where a heat slug is embedded in the package body to create the thermal path). (See Figure 2 and Figure 3.)

2.2 PCB Design Considerations

The printed circuit board that will be used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently.

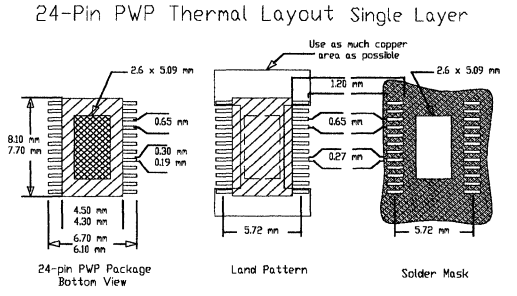
As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. As detailed below, the thermal land will vary in size depending on the PowerPAD package being used, the PCB construction and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed below.

2.3 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD package. During normal surface mount flow solder operations the leadframe on the underside of the package will be soldered to this thermal land creating a very efficient thermal path. Normally, the PCB thermal land will have a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. The size of the thermal land should be as large as needed to dissipate the required heat.

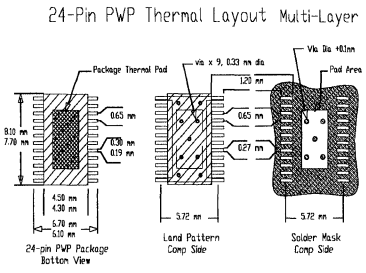
For simple, double-sided PCBs, where there are no internal layers, the surface layers must be used to remove heat. Shown in Figure 4 is an example of a thermal land for a 24-pin package. Details of the package, the thermal land and the required solder mask are shown. If the PCB copper area is not sufficient to remove the heat, the designer can also consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware connection.

Figure 4. Package and PCB Land Configuration for a Single Layer PCB



For multilayer PCBs, the designer can take advantage of internal copper layers (such as the ground plane) for heat removal. The external thermal land on the surface layer is still required, however the thermal vias can conduct heat out through the internal power or ground plane. Shown in Figure 5 is an example of a thermal land used for multilayer PCB construction. In this case, the primary method of heat removal is down through the thermal vias to an internal copper plane.

Figure 5. Package and PCB Land Configuration for a Multi-Layer PCB



Shown in Figure 6 are the details of a 64 pin TQFP PowerPAD package. The recommended PCB thermal land for this package is shown in Figure 7.

The maximum land size for TQFP packages is the package body size minus 2.0 mm. This land is normally attached to the PCB for heat removal, but can be configured to take the heat to an external heat sink. This is preferred when airflow is available.

Figure 6. 64 pin TQFP Package with PowerPAD Implemented, Bottom View

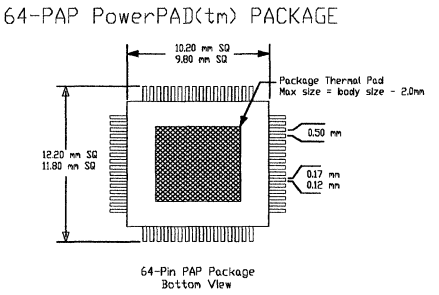
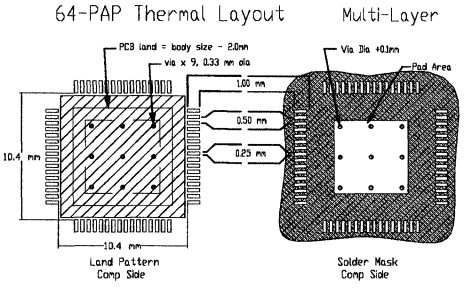


Figure 7. PCB Thermal Land Design Considerations for Thermally Enhanced TQFP Packages



2.4 Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. The number of vias used, the size of the vias and the construction of the vias are all important factors in both the PowerPAD package thermal performance and the package-to-PCB assembly. Recommendations and guidelines for thermal vias follow.

Shown in Figure 8 and Figure 9 are the effects on PCB thermal resistance of varying the number of thermal vias for various sizes of die for 2- and 4-layer PCBs. As can be seen from the curves, there is a point of diminishing returns where additional vias will not significantly improve the thermal transfer through the board. For a small die, having from five to nine vias should prove adequate for most applications. For larger die, a higher number may be used simply because there is more space available under the larger package. Shown in Figure 10 are examples of ideal thermal land size and thermal via patterns for PowerPAD™ packages using 0.33mm (13 mil) diameter vias plated with 1 oz. copper. This thermal via pattern set represents a copper cross section in the barrel of the thermal via of approximately 1% of the total thermal land area. Fewer vias may be utilized and still attain a reasonable thermal transfer into and through the PCB as shown in Figures 8 and 9.

The number of thermal vias will vary with each product being assembled to the PCB, depending on the amount of heat that must be moved away from the package, and the efficiency of the system heat removal method. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at an optimum value for a given board construction. Then the number of vias required can be determined for any new design to achieve the desired thermal removal value.

Figure 8. Impact of the Number of Thermal Vias versus Chip Area (Die Area)

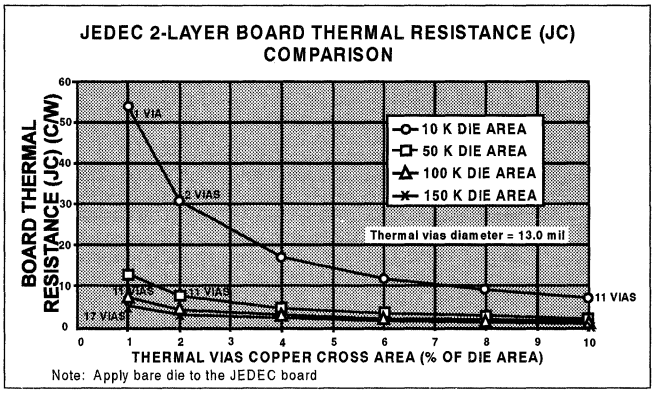


Figure 9. Impact of the Number of 0.33mm (0.013 inch) Diameter Thermal Vias versus Chip Area (Die Area)

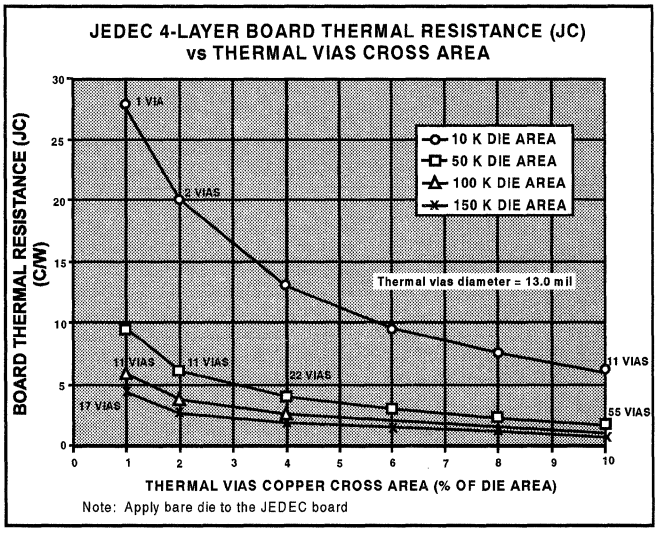
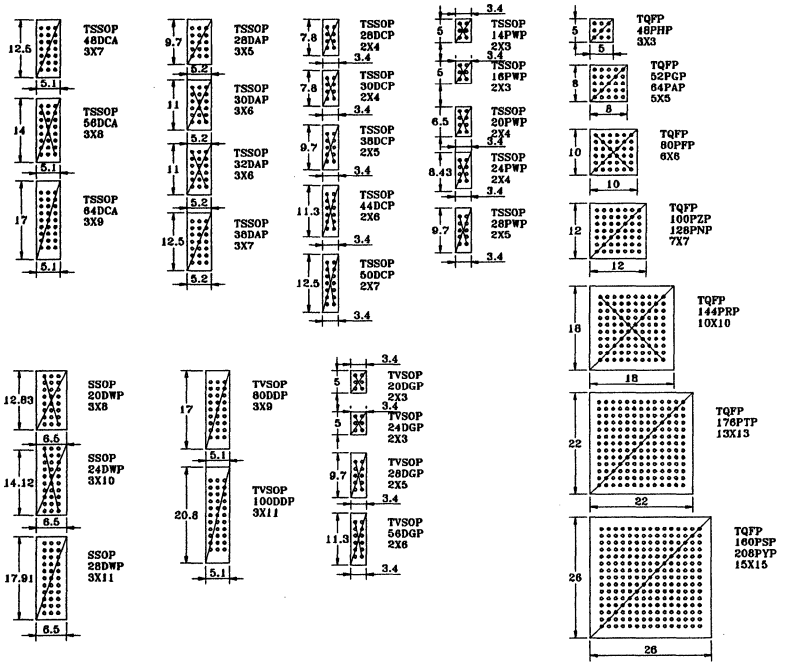


Figure 10. Ideal Thermal Land Size and Thermal Via Patterns for PowerPAD



Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias will not be plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1mm minimum. This will prevent the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

To assure the optimum thermal transfer through the thermal vias to internal planes or the reverse side of the PCB, the thermal vias used in the thermal land should *not* use web construction techniques. Web construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is *not* desirable for heat removal from the PowerPAD package. Therefore it is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter. Web construction for thermal vias is not recommended.

2.5 Solder Stencil Determination

A series of experiments were conducted at Solectron-Texas to determine the effects of solder stencil thickness on the quality of the solder joint between the thermal pad of a PowerPAD package and the thermal land on the surface of the PCB. Stencil thickness of 5, 6, and 7 mils were used in conjunction with a metal squeegee to deposit solder in the desired locations on the board. Note: 6 and 7 mil thick solder stencil is normally used with package lead pitch of 0.5 and 0.65mm respectively. A 5 mil thick stencil is normally used for packages with 0.4mm lead pitch to avoid solder bridging during reflow.

It was found that the standoff height for the package being attached to the PCB was critical in making good solder joints between the thermal pad of the package and the thermal land on the PCB. Note: during this series of experiments, a good solder joint was defined as a connection that joined at least 90% of the area of the smallest pattern to its intended connection point - such as the thermal pad of the package to the thermal land on the PCB. When the standoff height of the package (i.e., the distance between the bottom of the package leads and the bottom of the package body) was in the range of 0 to 2 mils, the package tended to float on the solder. This led to the possibility that all leads of the package would not be soldered to the lead traces on the board. This happened even when the 5 mil thick stencil was utilized. There were also cases when the solder was squeezed out from the desired land area, and then formed solder balls during the reflow process - an undesirable result that could cause shorting between package leads on the board surface, or short the thermal land on the PCB to the lead traces. A standoff height of 2.0 to 4.2 mils provided good solder joints for both the leads and the thermal pad for stencil thickness of 5, 6, and 7 mils. When the standoff height of the package was between 4.2 and 6.0 mils, only the 6 and 7 mil thick stencil provided consistently good solder joints for both the package leads and the thermal-pad to thermal-land bond. A general guideline would be to use the thickest solder stencil that works well for the products being assembled for the most process margin in assembling thermally enhanced parts to a PCB.

The Joint Electron Devices Engineering Council (JEDEC) specification for the standoff height of TSSOP and TQFP packages is the range of 0.05 to 0.15mm (1.97 to 5.91 mils), and is an acceptable range when the solder stencil thickness of 6 and 7 mils are used. Texas Instruments has elected to center the stand-off height of the PowerPAD packages at 3.5 mils (within the JEDEC specification range) to provide good package to PCB solder joint characteristics for standard solder stencil thickness of 5, 6, and 7 mils - the most common range within industry practice today.

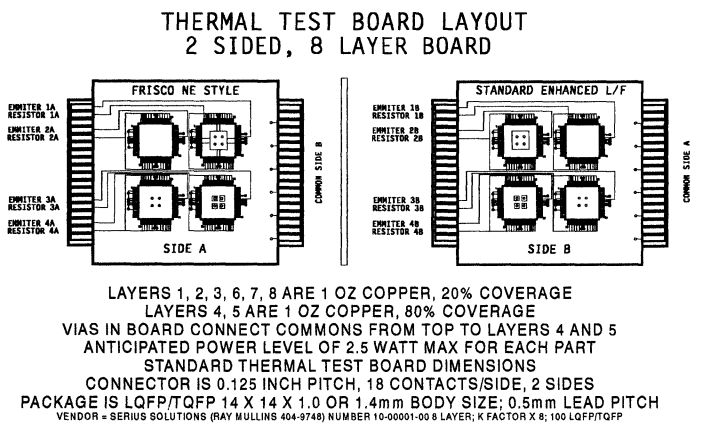
3. Assembly

Solder joint inspection in the attachment area of the thermal pad of the thermally enhanced packages to the thermal land on the PCB is difficult to perform with the best option to date being x-ray inspection. Tests performed within Texas Instruments and during the joint PCB experiments with Solectron-Texas indicate that x-ray inspection will allow detection of voiding within the solder joint and could be used either in a monitor mode, or for 100% inspection if required by the application. However, this is a slow and costly process so an effort was made to determine the minimum amount of solder required in this joint before degradation of the thermal performance became significant.

The experimental vehicle used in determining the amount of solder required was a 6S2P double sided test board with copper thermal lands on the surface of the board representing 0%, 7.5%, 22%, and 83% of the package body area. The package used was a 100 pin PowerPAD package (side B - standard enhanced I/f side of the PCB) as shown in Figure 11. There was additional copper area on the surface of the A side of the board due to connections between selected pins and the thermal land area. Four thermal vias were created in each thermal land area with connections to the internal power or ground plane, and continuing to make connection to the thermal land on the opposite side of the board.

A thermal test chip (Texas Instruments x-1158240) with dimensions of 6.1mm (0.240-inch) square was assembled in the test packages using die pad sizes of 6.0mm square, and 9.0mm square. The assembled units were then mounted to the PCB using either eutectic Sn63:Pb37 solder or thermally conductive epoxy adhesive. Measurement of the thermal resistance junction-to-case and thermal resistance junction-to-ambient with the individual packed parts powered at 2.5 watts was made using standard techniques for these measurements. Results are shown in Table 1 for tests with and without attachment between the package thermal pad and the board thermal land, as well as a comparison between solder and thermally conductive epoxy attachment. Table 2 provides the effective connection area obtained for each of the measurement points.

Figure 11. Test Board for Measurement of Θ_{jc} and Θ_{ja} Using 100 pin PowerPAD TQFP Packages



The relative thermal land size and location is shown along with the location of the thermal vias that connect the surface thermal land to the internal power or ground plane, and continuing to connect to the thermal land on the opposite side of the board. The board is approximately 82.5mm (3.25 inch) square.

Table 2 and Table 3 show the thermal resistance data for Θ_{jc} and Θ_{ja} (junction to case, and junction to ambient) for the 8 layer thermal test board, with the copper thermal land on the PCB shown as a percentage of the area of the package body.

Table 2. Measured Θ_{jc} from Test Board

		MEASURED DATA				
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**9.3**		**9.9**	**11.4**	
4B	7.5			**7.2**	**5.8**	**7.2**
2B	22	**6.8**		**6.3**	**7.2**	**7.5**
3B	83	**6.2**		**6.2**	**6.2**	**6.2**
2A	0	8.7	7.4	**9.1**	**7.8**	**7.8**
3A	7.5	7.6	8.3	**6.3**	**6.8**	**6.8**
1A	30		8		**6.6**	**6.5**
4A	85	7.5	7.3	**6.4**	**6.4**	**6.9**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 3. Measured Θ_{ja} from Test Board

		MEASURED DATA				
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**33.8**		**40.6**	**44.3**	
4B	7.5			**27**	**23.1**	**25.5**
2B	22	**28.4**		**25.8**	**25**	**24.3**
3B	83	**24.2**		**26.9**	**24.6**	**24**
2A	0	34.4	34	**33.3**	**32.3**	**25.8**
3A	7.5	33.5	33	**24.4**	**24.9**	**25.2**
1A	30		31		**24.4**	**23.2**
4A	85	33.3	30	**25.5**	**24.6**	**24**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

Small changes in the percentage of copper land area (between the "A" side of the PCB and the "B" side of the PCB) do not significantly affect the thermal resistance.

Table 4 and Table 5 show the relationship of the solder joint area between the thermal pad in the PowerPAD package and the thermal land of the PCB for the thermal resistance values obtained in Table 2 and Table 3.

Table 4. Relationship of the Solder Joint Area on Θ_{jc}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Position on PCB	PCB Copper land size on PCB	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 5. Relationship of the Solder Joint Area on Θ_{ja}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

In this example, there is significant improvement in thermal heat removal with solder joint areas as small as 16%, and the thermal removal efficiency as measured by Θ_{jc} and Θ_{ja} are within measurement error tolerance for all solder joint areas greater than 32%.

Based on the measured data for this test board configuration, Texas Instruments recommends a minimum solder joint area of 50% of the package thermal pad area when the part is assembled on a PCB. The results of the PCB assembly study conducted with Solectron-Texas indicate that standard board assembly processes and materials will normally achieve >80% solder joint area without any attempt to optimize the process for thermally enhanced packages. A characterization of the solder joint achieved with a given process should be conducted to assure that the results obtained during testing apply directly to the customer application, and that the thermal efficiency in the customer application is similar to the thermal test board results for the power level of the packaged component. If the heat removal is not at the efficiency desired, then either additional thermal via structures will have to be added to the PCB construction, or additional thermal removal paths will need to be defined (such as direct contact with the system chassis).

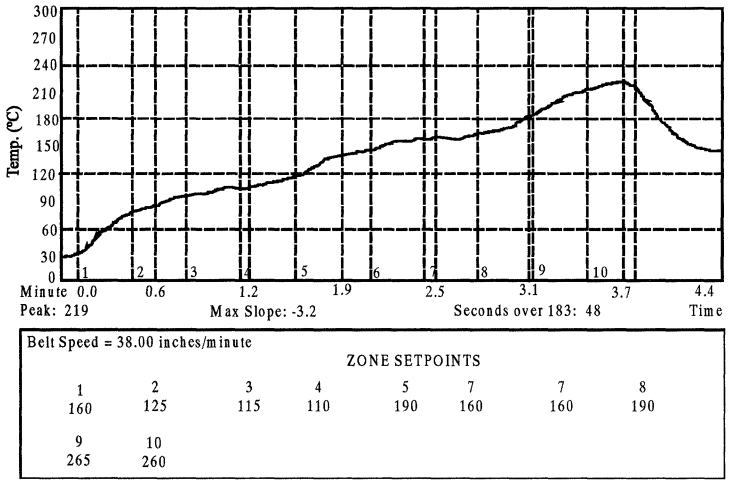
An alternative to attaching the thermal pad of the package to the thermal land of the PCB with solder is to use thermally conductive epoxy for the attachment. This epoxy can either be dispensed from the liquid form with a material that will cure during the reflow cycle, or a "B" staged preform that will receive the final cure during the reflow cycle. These materials can be the same as normally used with externally applied heat sinks. When epoxy is used as the attachment mechanism, then the effective attachment area is 100% of the die pad area, and there is some added benefit as thermal transfer to the PCB can occur, even with no copper thermal land at the surface of the PCB.

3.1 Solder Reflow Profile Suggestion

The reflow profile for IR board assembly using the Texas Instruments PowerPAD packages does not have to change from that used with conventional plastic packaged parts. The construction of the package does not add thermal mass, and the only new thermal load is due to the increased solder area between the package thermal pad and the thermal land on the PCB. A typical IR oven profile for fine pitch surface mount packages is shown in Figure 11. for eutectic Sn63:Pb37 solder. Nitrogen purged, convection IR reflow will be advantageous for this part to PCB assembly to minimize the possibility of solder ball formation under the package body.

Figure 12 shows a typical infrared (IR) oven profile for a fine pitch plastic package assembly mounted to an FR-4 PCB using eutectic Sn63:Pb37 solder.

Figure 12. Typical Infrared Oven Profile



Peak temperature should be approximately 220 degrees centigrade, and the exposure time should normally be less than 1 minute at temperatures above 183 degrees centigrade.

3.2 Installation and Assembly Summary

The PowerPAD package families can be attached to printed circuit boards using conventional Infrared solder reflow techniques that are standard in the industry today without changing the reflow process used for normal fine pitch surface mount package assembly. A minimum solder attachment area of 50% of the package thermal pad area is recommended to provide efficient heat removal from the semiconductor package, with the heat being carried into or through the PCB to the final thermal management system. This attachment can be achieved either by the use of solder for the joining material, or through the use of thermally conductive epoxy materials. Typical PCB thermal land pattern definitions have been provided that have been shown to work with 4 and 8 layer PCB test boards, and can be extended for use by other board structures.

4. Repair

Reworking thermally enhanced packaged semiconductors that have been attached to PCB assemblies through the use of solder or epoxy attachment can present significant challenges, depending on the point at which the re-work is to be accomplished. Tests of re-work procedures to date indicate that part removal from the PCB is successful with all of the conventional techniques used in the industry today. The challenge is part replacement on the board due to the combined thermal enhancement of the PCB itself, and the addition of thermal removal enhancement features to the semiconductor package. The traditional steps in the rework or repair process can be simply identified by the following steps for solder attached components:

1) Unsolder old component from the board
2) Remove any remaining solder from the part location
3) Clean the PCB assembly
4) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
5) Target, align, and place new component on the PCB
6) Reflow the new component on the PCB
7) Clean the PCB assembly

When thermally conductive epoxy has been used to attach the thermal pad of the package to the thermal land on the PCB, the same basic steps in the rework or repair procedure can be followed with only minor modifications:

1) Unsolder old component and torque package to remove from the board
2) Remove any remaining solder from the part location
3) Remove any remaining epoxy from the thermal land on the PCB
4) Clean the PCB assembly
5) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
6) Place new thermally conductive "B" staged epoxy preform or dispense epoxy on thermal land
7) Target, align, and place new component on the PCB
8) Reflow the new component on the PCB

9) Complete epoxy cure (if required as a separate step)

10) Clean the PCB assembly

4.1 Part Removal From PCBs

Almost any removal process will work to remove the device from the PCB, even with the thermal pad of the package soldered to the PCB. Heat is easily transferred to the area of the solder attachment either from the exposed surface thermal land of the PCB (single layer example), or through the thermal vias in the PCB (multi-layer example) from the backside of the PCB.

Re-work has been performed for both the TSSOP and TQFP PowerPAD style packages using METCAL removal irons and hot air. The specific example of a 20 pin TSSOP PowerPAD part removal is discussed in detail.

A 750-Watt METCAL removal iron was used in conjunction with hot air to verify the removal method efficiency to take 20 pin PowerPAD TSSOP packages off of assembly test boards. The hot air method is recommended as it subjects the PCB and surrounding components to less thermal and mechanical stress than other methods available, and has been proven to be much easier to control than some of the hot bar techniques. Use of the hot air method may require assemblers to acquire tools specifically for the smaller packages since most assemblers use a hot bar method for packages of this size. (Note: This same tool will also be needed for part re-attachment to the PCB when the hot air method is employed). A tool with an integrated vacuum pick up tip will be an advantage in the part removal process so the part can be physically removed from the board as soon as the solder reaches liquidus. Preheating of the local area of the PCB to a temperature of approximately 160 degrees centigrade can make the part removal easier. This is especially helpful in the case of larger packages such as 56 pin TSSOP or 100-pin TQFP style packages. This preheat will be required in the thermal removal method if the semiconductor package is a heat slug package rather than the TI PowerPAD package version. Some experimentation will be required to find the optimum procedure to use for any specific PCB construction and thermally enhanced package version.

After the part has been removed from the PCB, conventional techniques to clean the area of the part attachment - such as solder wicking - will be needed to prepare the location for subsequent attachment of a new component.

When thermally conductive epoxy has been used for attachment of the package thermal pad to the thermal land on the PCB, a slightly different approach to part removal must be used. This will require a tool that has dimensions that will allow contact with the sides of the package body directly above the leads, and will allow the package to be twisted or rotated horizontally when the solder joints of the package leads have reached liquidus. The temperature at the epoxy interface to the package thermal pad or the PCB thermal land must be above the glass transition temperature of the epoxy (typically less than 180 degrees centigrade) to break the adhesion between the epoxy and the attach location with the twisting or rotational method discussed above. In most cases, any remaining epoxy on the PCB after part removal can be removed by peeling it from the surface - occasionally, it will be necessary to apply heat to the epoxy location so it will peel away from the PCB cleanly.

4.2 Attachment of a Replacement Component to the PCB

Preparation of the PCB for attachment of a new component follows normal industry practice with respect to the lands on the board and the leads of the package. Both may be tinned, and/or solder paste applied to the lands for new component attachment. In addition, when solder will be used to re-attach the thermal pad of the package to the thermal land on the PCB, solder paste will need to be applied to the surface of the thermal land on the board. This may be in the form of stripes of solder paste with sufficient volume to achieve the desired solder coverage, or a solder preform may be applied to the location for attachment. In a factory environment, the component is then placed in the desired location and alignment, and processed through a reflow oven to re-establish the desired solder joints. This is the most desirable process and is normally the easiest to accomplish.

When a manual or off-line attachment and reflow procedure is to be used, the challenge of supplying sufficient heat to the components and solder becomes a greater concern. In most cases, the corner leads of the package being attached will be tack soldered to hold the component in alignment so the balance of the leads and the thermal pad to thermal land solder reflow can be accomplished without causing part movement from its desired location. As in the part removal case, it is advisable to pre-heat the board or the specific device location to a temperature below the melting point of the solder to minimize the amount of heat that must be provided by the reflow device as the part is being attached. A good starting point is to pre-heat to approximately 160 degrees centigrade. A hot gas reflow tool can then be used to complete the solder joint formation both at the leads and for the connection of the thermal pad to the thermal land of the PCB. Care must be taken at this operation to avoid blowing solder out from the thermal pad to thermal land interface and causing solder balling under the package or creating

lead to lead or thermal land to lead shorts. The thermal enhancement of the package and the PCB will require a higher temperature gas or higher gas flow to reach solder liquidus than would be needed with an assembly lacking these enhancements. The tool should be specifically sized to the part being reworked to minimize possible damage to surrounding components or the PCB itself.

If the re-attachment of the interface between the thermal pad of the package and the thermal land of the PCB using solder attachment is too difficult to control using hot gas methods, then the best approach is to use either a thermally conductive "B" staged epoxy preform cut to the shape of the thermal land on the PCB, or dispensing liquid thermally conductive epoxy in a pattern on the thermal land that will result in at least a 50% void free connection between the pad and the land. Virtually any epoxy material that is used for the attachment of external heat sinks to packaged components is suitable for this application, and cure time/temperature requirements can be matched to the product need (anywhere from 24 hours at room temperature to less than 1 hour at temperatures below 100 degrees centigrade). Care must be taken to choose a material with limited run-out to avoid the possibility of shorting adjacent package leads together or shorting the thermal land of the PCB to the package leads.

It should be noted that the Texas Instruments PowerPAD packages are easier to rework at the board level than other semiconductor packages utilizing metal slugs for the thermal path between the chip and the PCB. This is due to the additional requirement for heating the total mass of the slug to reflow temperatures versus heating the thermal pad of the PowerPAD package. The hot gas temperature and/or flow becomes critical for effective joining of the components without causing damage to the adjacent components or the PCB. In either case, the use of thermally conductive epoxy materials will make the rework task easier and more reliable to perform in a manual repair environment.

5. Summary

An overview of the design, use and performance of the Texas Instruments PowerPAD package has been presented. The package is simple to use and can be assembled and repaired using existing assembly and manufacturing tools and techniques. Package performance is outstanding. By exposing the leadframe on the package bottom, extremely efficient thermal transfer between the die and the PCB can be achieved.

The simplicity of the PowerPAD package not only makes for a low cost package, but there is no additional cost in labor or material for the customer using standard surface mount assembly techniques. The only preparation needed to implement a PowerPAD design is at the PCB design stage. Simply by including a thermal land and thermal vias on the PCB the design can use the PowerPAD package effectively.

Appendix A. Thermal Modeling of PowerPAD Packages

Table 6. Thermal Characteristics for Different Package and PCB Configurations

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964
	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235

General

Thermal modeling is used to estimate the performance and capability of IC packages. From a thermal model, design changes can be made and thermally tested before any time is spent on manufacturing. It can also be determined what components have the most influence on the heat dissipation of a package. Models can give an approximation of the performance of a package under many different conditions. In this case, a thermal analysis was performed in order to approximate the improved performance of a PowerPAD thermally enhanced package to that of a standard package.

Modeling Considerations

There are only a few differences between the thermal models of the standard packages and models for PowerPAD. The geometry of both packages was essentially the same, except for the location of the lead frame bond pad. The pad for the thermally enhanced PowerPAD package is deep downset, so its location is further away from the lead fingers than a standard package lead frame pad. Both models used the maximum pad and die size possible for the package, as well as using a lead frame that had a gap of one lead frame thickness between the pad and the lead fingers. The lead frame thickness was:

TQFP/LQFP: 0.127 mm, or 5 mils
TSSOP/TVSOP/SSOP: 0.147 mm, or 5.8 mils

In addition, the board design for the standard package is different than the PowerPAD. One of the most influential components on the performance of a package is board design. In order to take advantage of PowerPAD's heat dissipating abilities, a board must be used that acts similarly to a heat sink and allows for the use of the exposed (and solderable) deep downset pad. This is Texas Instruments' recommended board for PowerPAD (see

Figure 13). A summary of the board geometry is included below.

Texas Instruments Recommended Board for PowerPAD

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

2 oz. copper traces located on the top of the board (0.071 mm thick)

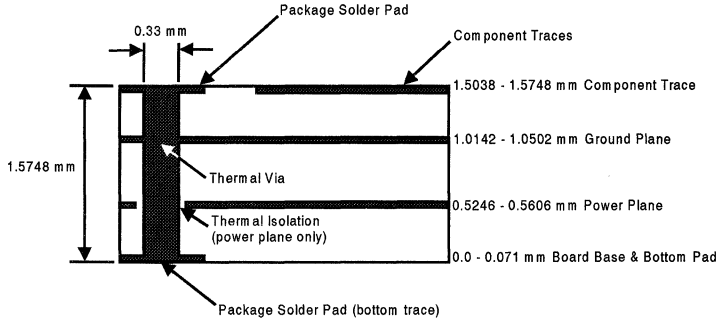
Copper areas located on the top and bottom of the PCB for soldering

Power and ground planes, 1 oz. copper (0.036 mm thick)

Thermal vias, 0.33 mm diameter, 1.5 mm pitch

Thermal isolation of power plane

Figure 13. Texas Instruments Recommended Board (Side View)



The standard packages were placed on a board that is commonly used in the industry today, following the JEDEC standard. It does not contain any of the thermal features that are found on the Texas Instruments recommended board. It only has component traces on the top of the board. A summary of the standard is located below:

JEDEC Low Effective Thermal Conductivity Board (Low-K)

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

1 oz. copper traces located on the top of the board (0.036 mm thick)

These boards were used to estimate the thermal resistance for both PowerPAD and the standard packages under many different conditions. While the PowerPAD can be used on a JEDEC low-k board, in order to achieve the maximum thermal capability of the package, it is recommended that it be used on the Texas Instruments heat dissipating board design. It allows for the exposed pad to be directly soldered to the board, which creates an extremely low thermal resistance path for the heat to escape.

A general modeling template was used for each PowerPAD package, with variables dependent on the package size and type. The package dimensions and an example of the template used to model the packages are shown in Figure 14 and Table 7. While only 1/4 of the package was modeled (in order to simplify the model and to lessen the calculation time), the dimensions shown are those for a full model.

Figure 14. Thermal Pad and Lead Attachment to a PCB Using the PowerPAD Package

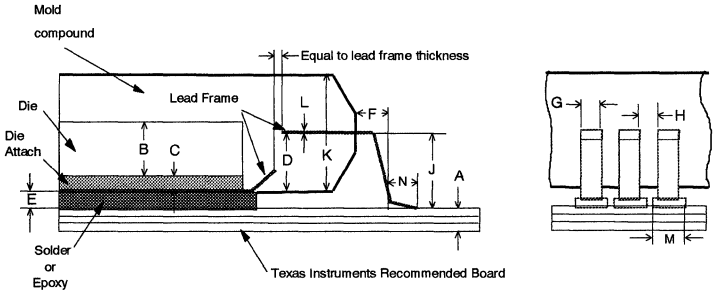


Table 7. PowerPAD Package Template Description

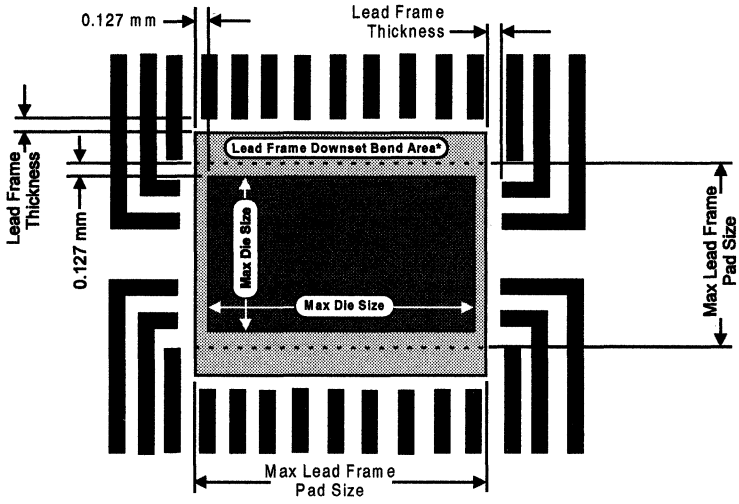
(A)	PCB Thickness:	1.5748 mm	(K)	Package Thickness:	(3)
	PCB Length:	76.2 mm (1)		Package Length:	(3)
	PCB Width:	76.2 mm (1)		Package Width:	(3)
(B)	Chip Thickness:	0.267 mm	(L)	Pad Thickness:	0.147 mm (8)
	Chip Length:	(2)		Pad Length:	(3)
	Chip Width:	(2)		Pad Width:	(3)
(C)	Die Attach Thickness:	0.0127 mm		PCB Trace Length:	25.4 mm
(D)	Lead Frame Downset:	(3)		PCB Trace Thkn:	0.071 mm
	Tie Strap Width:	(3)		PCB Backplane Th:	0.0 mm (4)
(E)	PCB to Package Bottom:	0.09 mm		PCB Trace Width:	0.254 mm
(G)	Shoulder Lead Width:	(3),(5),(6)	(M)	Foot Width:	(5)
(H)	Shoulder Lead Space:	(3),(6)	(N)	Foot Length on PCB:	(3)
(J)	Shoulder to PCB Dist.:	(7)			

Notes: 1) 99.6mm for packages > 27mm max length
2) Chip size is 10 mils smaller than the largest pad size (5 mils from each side)
3) Dependent on package size and type
4) The recommended board requires the addition of two internal copper planes, solder pads, and thermal vias
5) Foot width was set equal to shoulder lead width for model efficiency
6) Lead pitch is equal to the shoulder lead width plus the shoulder lead space (pitch = G + H)

7) The shoulder to board distance is equal to the downset plus the board to package bottom distance (J = D + E)
8) The pad thickness for TQFP/LQFP is equal to 0.127 mm
9) All dimensions are in millimeters.

In addition to following a template for the dimensions of the package, a simplified lead frame was used. A description of the lead frame geometry is seen in Figure 15.

Figure 15. General Leadframe Drawing Configuration



NOTE:
The lead frame downset bend area = 20 mils (lead frame thickness). For SSOP, TSSOP, and TVSOP packages, add the bend area to the width of the pad. For TQFP and LQFP, add the bend area to both the width and length of the pad.

Results

The purpose of the thermal modeling analysis was to estimate the increase in performance that could be achieved by using the PowerPAD package over a standard package. For this package comparison, several conditions were examined:

Case 1. PowerPAD soldered to the TI recommended board

Case 2. PowerPAD not soldered to the TI recommended board

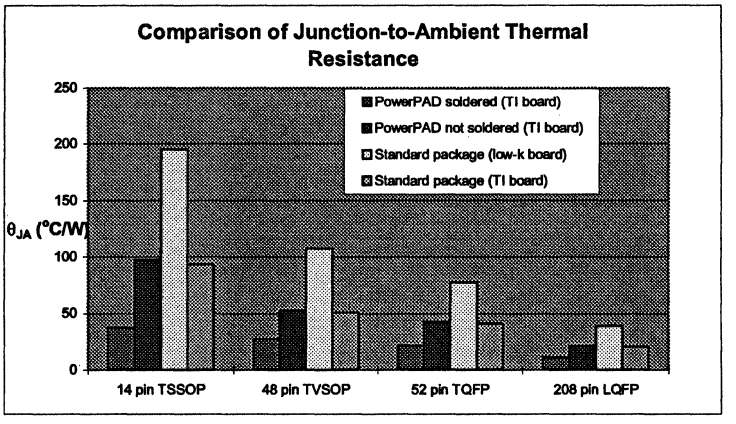
Case 3. A standard package configuration on a low-k board

Case 4. A standard package on the TI recommended board

The first three cases show a comparison of PowerPAD packages on the recommended board to standard packages on a board commonly used in the industry. The results are shown in Table 6. From these results, it was shown that the PowerPAD, when soldered to the TI recommended board, performed an average of 47% cooler than when not soldered, and 73% cooler than a standard package on a low-k board.

For the final case, a separate analysis was performed in order to show the difference in thermal resistance when the standard and the thermally enhanced packages are used on the same board. The results showed that the PowerPAD, when soldered, performed an average of 44% cooler than the standard package (See Figure 18).

Figure 18. Comparison of θ_{JA} for Various Packages

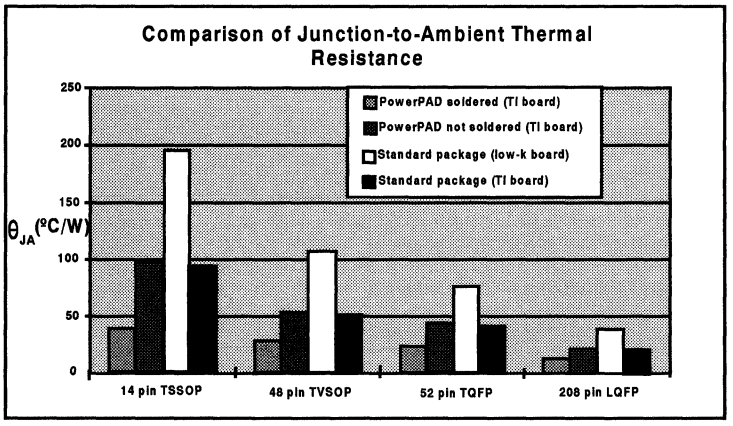


However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

Conclusions

The deep downset pad of a PowerPAD package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink will improve standard package performance, but greatly increases the cost of a package. The PowerPAD package improves performance, but maintains a low cost. The results of the thermal analysis showed that by soldering the PowerPAD package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

Figure 18. Comparison of θ_{JA} for Various Packages



However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

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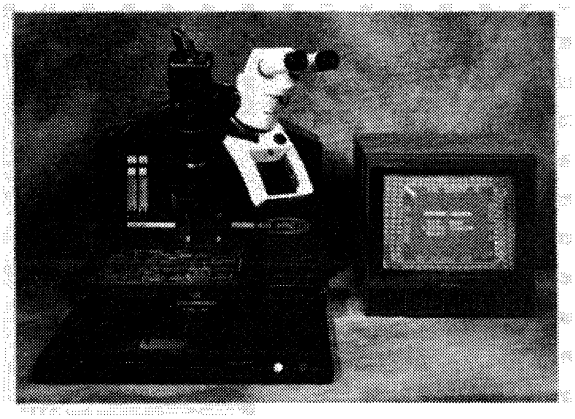
Appendix B. Rework Process for Heat Sink TQFP and TSSOP PowerPAD Packages - from Air-Vac Engineering

Introduction

The addition of bottom side heat sink attachment has enhanced the thermal performance of standard surface mounted devices. This has presented new process requirements to effectively remove, redress, and replace (rework) these devices due to the hidden and massive heat sink, coplanarity issues, and balance of heat to the leads and heat sink. The following is based on rework of the TQFP100 and TSSOP20/24 pin devices.

Figure 19. DRS22C Reworking Station

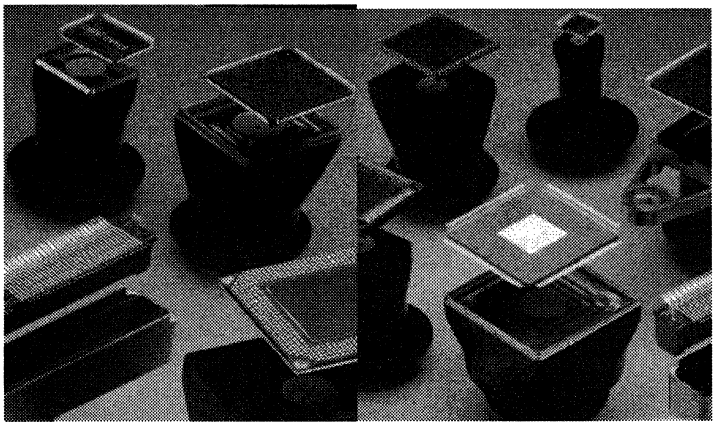


Equipment

The equipment used was the Air-Vac Engineering DRS22C hot gas reflow module. The key requirements for the heat sink applications include: stable PCB platform with sufficient bottom side preheat, alignment capabilities, very accurate heat control, and proper nozzle design.

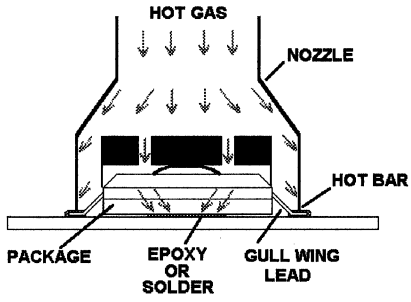
PCB support is critical to reduce assembly sagging and to provide a stable, flat condition throughout the process. The robust convection-based area heater provides sufficient and accurate bottom side heat to reduce thermal gradient, minimize local PCB warpage, and compensate for the heat sink thermal characteristics. The unique pop-up feature allows visible access to the PCB with multiple easy position board supports.

Figure 20. Reworking Nozzles of Various Sizes



During removal, alignment, and replacement, the device is held and positioned by a combination hot gas/hot bar nozzle. Built-in nozzle tooling positions the device correctly to the heat flow. A vacuum cup holds the component in place. Hot gas is applied to the top of the device while hot gas/hot bar heating is applied to the component leads. The hot bar feature also insures bonding of the fine pitch leads.

Figure 21. Nozzle Configuration



Profile

The gas temperature, flow, and operator step-by-step instructions are controlled by an established profile. This allows complete process repeatability and control with minimal operator involvement. Very accurate, low gas flow is required to insure proper temperature control of the package and to achieve good solder joint quality.

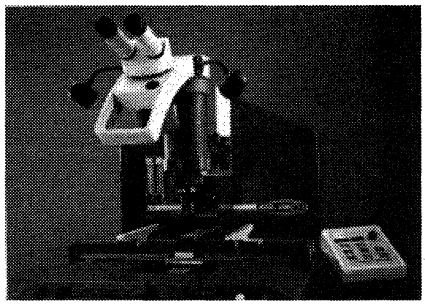
Removal

The assembly is preheated to 75 °C. While the assembly continued to preheat to 100 °C, the nozzle is preheated. After the preheat cycle, the nozzle is lowered and the device is heated until reflow occurs. Machine settings: TSSOP 20/24 - 220 °C at 0.39 scfm gas flow for 50 seconds (preheat) above board level, 220 °C at 0.39 scfm for 10 seconds. TQFP 100 - 240 °C at 0.10 scfm for 60 seconds (preheat) above board level, 250 °C at 0.65 scfm for 15 seconds. The built in vacuum automatically comes on at the end of the cycle and the nozzle is raised. The time to reach reflow was approximately 15 seconds. The component is released automatically allowing the part to fall into an appropriate holder.

Site Redress

After component removal the site must be cleaned of residual solder. This may be done by vacuum desoldering or wick. The site is cleaned with alcohol and lint-free swab. It is critical that the heat sink area be flat to allow proper placement on the leads on new device. Stenciling solder paste is the preferred method to apply new solder. Solder dispensing or reflowing the solder bumps on the pads for the leads may also be an alternative, but reflow (solid mass) of solder to the heat sink is not.

Figure 22. Air-Vac Vision System



Alignment

A replacement device is inserted into the gas nozzle and held by vacuum. The device is raised to allow the optical system to be utilized. The optical system used for alignment consists of a beam-splitting prism combined with an inspection quality stereo microscope or camera/video system. the leads of the device are superimposed over the corresponding land pattern on the board. This four sided viewing allows quick and accurate operator alignment.

Replacement

Once aligned, the x/y table is locked and the optical system retracts away from the work area. The preheat cycle is activated. The device is then lowered to the board. An automatic multi-step process provides a controlled reflow cycle with repeatable results. Machine settings for TSSOP 20/24: 160 °C at 0.39 scfm gas flow for 40 seconds (preheat), 220 °C at 0.39 scfm for 60 seconds above board level, 220 °C at 0.39 scfm for 10 seconds. For TQFP 100: 100 °C at 0.78 scfm for 40 seconds (preheat), 240 °C at 0.10 scfm for 90 seconds above board level, 250 °C at 0.65 scfm for 15 seconds (2 stages).

Conclusion

Rework of heat sink devices, TQFP and TSSOP, can be successful with attention to the additional issues they present. With respect to proper thermal profiling of the heat sink, die, and lead temperatures, the correct gas nozzle and profile can be developed to meet the requirements of the device and assembly. Existing equipment and nozzle design by Air-Vac can provide the tools and process knowledge to meet the heat sink TQFP and TSSOP rework application.

Appendix C. PowerPAD Process Rework Application Note from Metcal

The following report references six of Texas Instruments' fine pitch, surface mount prototype packages (TSOP20, TSOP56, TSOP24, TQFP100, and TQFP64). The shapes and sizes are not new to the circuit board industry. Normally, I would use Metcal conduction tools to simply remove and replace these components. However, these packages are unique because all packages include a 'dye lead' on the underside of the package. This dye lead cannot be accessed by contact soldering. Therefore, convection rework methods are necessary for component placement.

NOTE:
Conduction tools can be used for removal. But, convection rework techniques are required for placement, and recommended for removal.)

Removal

Conduction (optional): All packages can be removed with Metcal conduction tips. Use the following tips:

Component	Metcal Tip Cartridge	OK Nozzle
TSOP20	SMTC-006	N-S16
TSOP56	SMTC-166	N-TSW32
TSOP24	SMTC-006	N-S16
TQFP100	SMTC-0118	N-P68
TQFP64	SMTC-112	N-P20

The dye lead, which is not in contact with the Metcal tip, will easily reflow as heat passes through the package.

Conduction Procedure

1) Tin the tip, contact all perimeter leads simultaneously, and wait 3-5 seconds for the leads to reflow.

2) Lift the package off the board (surface tension will hold it in the tip cartridge). Dislodge the component from the tip by wiping the tip cartridge on a damp sponge.

Convection Procedure

1) Flux the leads. Preferably, use a liquid RMA/rosin flux. Pre-heat the board at 100C. Use a convection or IR preheater, like the SMW-2201 from OK Industries. The settings 2-4 will generally heat a heavy board to 100° in 60 seconds.

2) Remove the component with the OK Industries FCR hot air system. Use a nozzle that matches the size and shape of the component (see above). With the preheat still on, heat the top of the board for 30-45 seconds on a setting of 3-4 (depending on board thickness and amount of copper in board*).

Since convection is NECESSARY for placement, convection is recommended for removal.

Placement Procedure

1) Pads can be tinned by putting solder paste on the pads and reflowing with hot air. Simply apply a fine bead of solder paste (pink nozzle, 24AWG) to the rows of pads. Be sure to apply very little paste. Excessive paste will cause bridging, especially with fine pitch components.

2) Once the pads are tinned, apply gel flux (or liquid flux) to the pads. RMA flux is preferable. Be sure to apply gel flux to the dye pad as well. It is important that your pads not be OVER tinned. If too much solder has formed on the dye pad, the component will sit above the perimeter leads, causing co-planarity problems. The gel flux is tacky and helps with manual placement. The joints require very little solder, so stenciling is not necessary. The pads are so thin that a minimal amount of solder is needed to form a good joint. Use a hot air nozzle for the FCR system. Pre-heat the board and (setting 3-5). Use low air flow (5-10 liters/minute) and topside heat (setting 3-4) for about 30-45 seconds*.

NOTES:

The quality of the dye lead's solder joint cannot be visually inspected. An X-ray machine, cross sectioning, or electrical testing will be required.

The vias on the test board are not solder masked very well which causes some bridging and solder wicking.

*Specific board and component temperatures will vary from board to board and from nozzle to nozzle. Larger nozzles require a higher setting because the heat must travel farther away from the heat source. There will be a slight convection cooling effect from pushing hot air through long flutes, and depending on how wide the nozzle is. However, as a rule, keep the board temperature at 100 °C (as thermocoupled from the TOP). You can regulate the board temperature by setting the temperature knob on the bottom side pre-heater. Apply a HIGHER topside heat from the FCR heating head. As a rule, use a maximum of 200-210°C for a short peak period (10 seconds). Look for the flux to burn off. For board profiling purposes, you can visually inspect the condition of the solder joints during the removal process. Note the time allotted for reflow and set the system to Auto Remove or Auto Place at the same time designation for good repeatability. Be sure not to overheat the joints. Excessive heat can cause board delamination and discoloration. Alignment will 'self-correct' once all the solder has reflowed. Tap board lightly. Remove any solder bridges with solder braid. Also, limit the board's heating cycles to a minimum. Excessive heat shock may warp the board or cause cracking in the solder joints.

Reducing and Eliminating the Class-D Output Filter Application Report

SLOA023
August 1999

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Reducing and Eliminating the Class-D Output Filter

Michael D. Score

ABSTRACT

This application report investigates reducing and eliminating the LC output filter traditionally used in class-D audio power amplifier applications. The filter can be completely eliminated if the designer is using a predominantly inductive speaker; however, the supply current and the EMI are higher than if using the full second-order Butterworth low-pass filter. The designer can use half of the components in the originally recommended second-order Butterworth low-pass filter to reduce the supply current, but the EMI is still higher than that of the full filter. The half and no filter class-D applications outperform the full second-order Butterworth filter in total harmonic distortion plus noise (THD+N) and intermodulation distortion (IMD). This document shows speaker requirements with and without a filter, fidelity and electromagnetic Interference (EMI) results, and indicates what type of filter fits various system requirements.

1 Introduction

A properly designed class-D output filter provides many advantages by limiting supply current, minimizing electromagnetic interference (EMI), and protecting the speaker from switching waveforms. However, it also significantly increases the total solution cost. The current recommended second-order output filter for the TPA005D02 is 30% of the audio power amplifier (APA) solution cost. This application report discusses the recommended second-order Butterworth filter as well as two reduced filtering techniques, each providing a different price/performance node. The first alternative to the Butterworth filter reduces the output filter by half and the second option completely eliminates the filter.

The total harmonic distortion plus noise (THD+N) and intermodulation distortion (IMD) of the class-D amplifier with full filter, half filter, and no filter were measured using a Texas Instruments TPA005D02 Class-D APA. Near-field EMI was measured and methods to reduce EMI are suggested for each application. Filter selections were then made based on system requirements.

This document gives speaker and filter component recommendations for each filter application.

2 Second-Order Butterworth Low-Pass Filter

The second-order Butterworth low-pass filter is the most common filter used in class-D amplifier applications. The second-order Butterworth low-pass filter as shown in Figure 1 uses two inductors and three capacitors for a bridged-tied load (BTL) output [1].

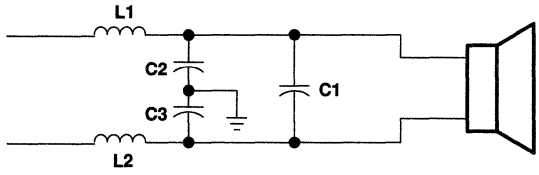


Figure 1. Full Second-Order Butterworth Filter

The primary purpose of this filter is to act as an inductor to keep the output current constant while the voltage is switching. If the amplifier outputs do not see an inductive load at the switching frequency, the supply current will increase until the device becomes unstable. Higher inductance at the output yields lower quiescent current (supply current with no input), because it limits the amount of output ripple current.

The filter also protects the speaker by attenuating the ultrasonic switching signal. Inductors L1 and L2, and capacitor C1 form a differential filter that attenuates the signal with a slope of 40 dB per decade. The majority of the switching current flows through C1, C2, and C3, leaving very little current to be dissipated by the speaker. The filter also greatly reduces EMI, which is discussed in a subsequent section.

3 Half Filter

The half filter, as shown in Figure 2, eliminates one of the inductors and the two capacitors to ground from the full filter.

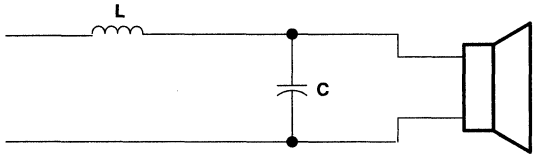


Figure 2. Half Filter

For the cut-off frequency to remain unchanged, the value of the inductor is doubled while the value of the capacitor across the load stays the same. The capacitors to ground are removed to prevent one of the amplifier outputs from seeing a capacitive load, which would greatly increase the supply current. This filter is still inductive at the switching frequency because the capacitor looks like a short at that frequency.

Aside from the primary advantage of reduced system cost, the half filter also decreases the quiescent current. In the case of the full filter, part of the switching current is shunted to ground through one of the capacitors. In the half filter, the absence of a capacitor to ground eliminates this waste. Furthermore, each output sees the full inductance value, which effectively reduces the rate of change in the inductor current, providing less power loss in the filter. Although this filter attenuates the differential signal, which reduces the magnetic field radiation, it does not attenuate the common mode signal, which causes the electric field radiation. Sources of EMI and methods to reduce EMI are covered in Section 9.

4 No Filter

The filter can be completely eliminated if the speaker is inductive at the switching frequency. For example, the filter can be eliminated if the class-D audio power amplifier is driving a midrange speaker with a highly inductive voice coil, but cannot be eliminated if it is driving a tweeter or piezo electric speaker, neither of which are highly inductive. The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

The main drawback to eliminating the filter is that the power from the switching waveform is dissipated in the speaker, which leads to a higher quiescent current, $I_{DD(q)}$. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive. A more inductive speaker yields lower quiescent current, so a multilayer voice coil speaker is ideal in this application.

The switching waveform, driven directly into the speaker, may damage the speaker. The rail-to-rail square wave driving the speaker when power is applied to the amplifier is the first concern. With a 250-kHz switching frequency, however, this is not as significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is insignificant [2]. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. Section 5 focuses on selecting the speaker and includes a derivation for choosing the power requirements of the speaker when not using an output filter.

Eliminating the filter also causes the amplifier to radiate EMI from the wires connecting the amplifier to the speaker. Therefore, the filterless application is not recommended for EMI sensitive applications. Methods of reducing EMI are discussed in Section 9.

5 Speaker Selection

5.1 Class-D With Full Filter and Half Filter

Selecting an appropriate speaker for a half-filter or full-filter class-D application is approximately the same as specifying a speaker for a class-AB application. First, the speaker should be efficient, or it should provide better than average sound pressure level (SPL) output for a given power input. Second, the speaker must also have a good frequency response, meaning a relatively constant SPL across a wide frequency range for a given input power.

A speaker should have a low inductance voice coil if designing with a filter, as the inductance causes a peak to appear in the output at the corner frequency of the filter. Peaking is not a significant problem in class-D applications though, because the corner frequency of the filter is set outside the audible frequencies. The class-D output filter should have a corner frequency of 25 kHz or higher, so the peaking may slightly affect the upper frequencies of the audio band. However, this peaking should be so small that it has an insignificant effect on the sound quality.

5.1.1 Zobel Networks Reduce Peaking

If the peaking does cause problems in a given system, a simple RC matching network, also called a Zobel network, may be placed in parallel with the speaker, as shown in Figure 3.

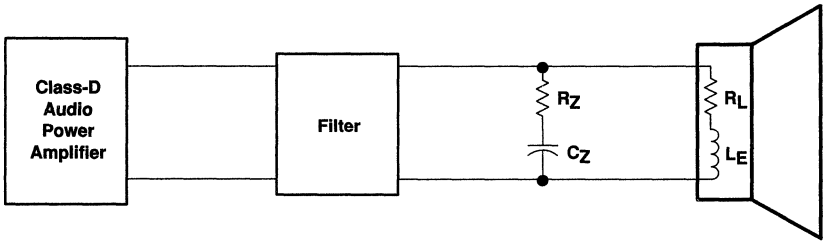


Figure 3. Class-D Amplifier With Zobel Network

The resistor and capacitor act to dampen the reactance of the load. The equations for the components of the Zobel network are shown in equations 1 and 2. R_L is the DC resistance of the speaker, and can be measured with an ohmmeter. L_E is the electrical inductance at DC, and is usually given as a speaker parameter. The power rating of the resistor and capacitor of the Zobel network are dependent upon the selected component values and must be calculated. The power rating of the resistor will be high for many applications, making this solution impractical for many systems in which cost and size are important.

$$R_Z \cong 1.25 \times R_L \quad (1)$$

$$C_Z = \frac{L_E}{R_L^2} \quad (2)$$

5.2 Class-D Without Filter

The major difference in selecting a speaker for a class-D amplifier without a filter is that the speaker must have a high inductance. Furthermore, the speaker power rating must be slightly increased to account for the switching waveform being dissipated by the speaker instead of by the filter.

5.2.1 High-Inductance Speakers

The filterless class-D application requires a speaker with a high inductance to keep the output current relatively constant while the output voltage is switching. As a result, the filterless approach may be impractical for use with a tweeter or a piezo electric speaker, both of which typically have small inductances. Without the filter, the peaking problem with the full and half filter application disappears because there is no filter to form a resonant circuit.

The additional quiescent current due to switching waveform power dissipation in the speaker can be calculated by first thinking of the speaker as a complex load. The switching current dissipated in the speaker can be calculated if the impedance and phase of the speaker is known for frequencies greater than the switching frequency. The magnitude and phase of the impedance of the speaker may be measured with a network analyzer from the switching frequency and higher to get an exact measurement on the switching loss in the speaker.

$$P_{DIS} = \sum_{n=1}^{\infty} \frac{V_{SW}\left(n \times f_{SW}\right)^2 \times \cos\left(\phi_{SPKR}\left(n \times f_{SW}\right)\right)}{\left| Z_{SPKR}\left(n \times f_{SW}\right)\right|} \quad (3)$$

The Fourier series needs to be calculated for the switching waveform that is being applied to the speaker. This is not as difficult with the TPA005D02, which has the standard modulation scheme, because the switching waveform voltage, V_{SW}, is a square wave, which is composed of the sum of many sine waves with frequencies of the odd harmonics of the switching frequency. The RMS value of the harmonics are shown in equation 4. The impedance and phase must then be calculated at each odd harmonic of the switching frequency.

$$V_{SW}\left(n \times f_{SW}\right) = \frac{0.707 \times V_{DD}}{n} \text{ for } n = 1, 3, 5, 7, 9, 11, \ldots \quad (4)$$

The impedance and phase of the speaker that Texas Instruments provides with the TI Plug-N-Play Audio Evaluation Platform can be seen in Figure 4 and Figure 5.

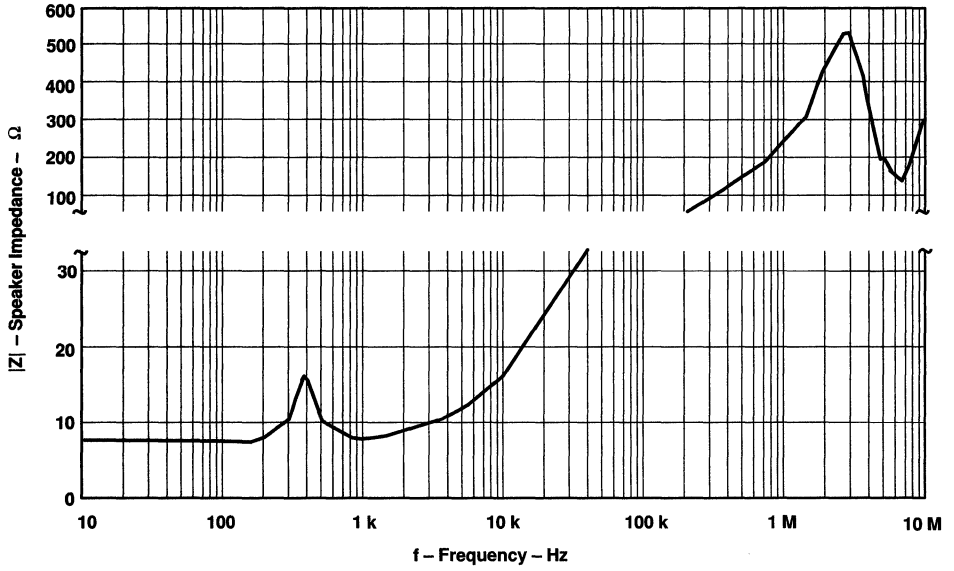


Figure 4. TI Speaker Impedance vs Frequency

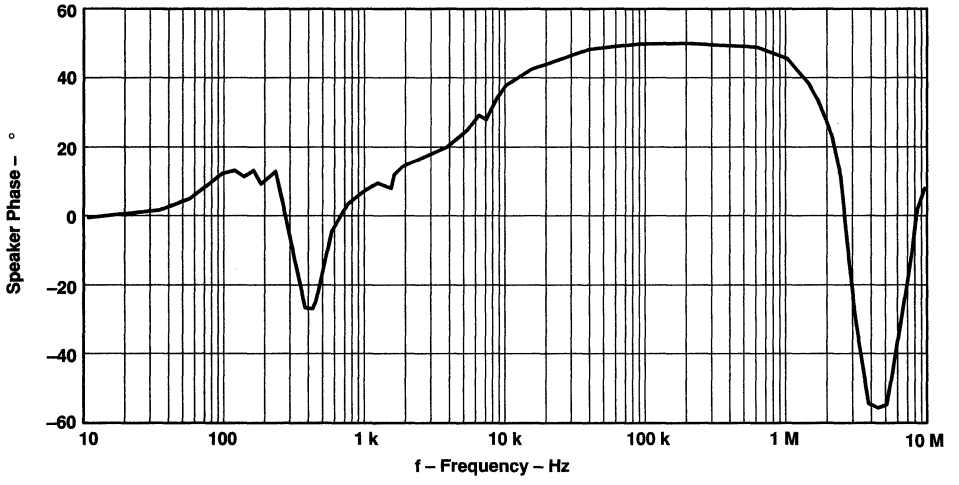


Figure 5. TI Speaker Phase vs Frequency

After measuring and calculating the value of the components at the harmonics, equation 5 can be used to calculate the added current drawn from the supply. The constant 0.58 is required in finding the RMS current from the peak current of a triangle wave.

$$\Delta I_{DD(q)} = \sum_{n=1}^{\infty} \frac{0.58 \times V_{DD} \times \cos\left(\phi_{SPKR}\left(n \times f_{SW}\right)\right)}{n^2 \times \left| Z_{SPKR}\left(n \times f_{SW}\right)\right|} \quad (5)$$

Table 1 shows an example of calculating the added quiescent current drawn when using the TPA005D02 to drive the TI speaker without a filter. The TPA005D02 has 23 mA of quiescent current with no load or filter. The added quiescent current from power dissipated in the speakers is 2 × 22.5 mA (from Table 1). Thus, the total quiescent current when using the TPA005D02 to drive the TI plug-n-play speaker is: 23 + 2 × 22.5 = 68 mA. This value is slightly low because the harmonics over 11 were not realized in the calculation and there were other losses in the class-D amplifier.

Table 1. Additional Quiescent Current per Channel from Switching Loss in Speaker Without Filter

HARMONIC (n)	$\lvert Z_{spkr}\rvert$ (Ω)	ϕ_{spkr} (degrees)	$\Delta I_{DD(q)}$ (n) (mA)
1	90	50	20.71
3	188	45	1.21
5	316	38	0.29
7	420	30	0.12
9	530	10	0.07
11	500	0	0.05
Total per channel:			22.5

As the speaker becomes more inductive, the phase approaches 90 degrees and the power dissipated in the speaker goes to zero (cos(90)=0). Unfortunately, at the switching frequency, most speakers have only approximately 40 degrees of phase shift. An example showing the importance of phase is that the switching current into the LC filter is actually higher than the current into the speaker without a filter. However, the quiescent current of the class-D amplifier with the filter is less than the quiescent current without the filter, because the filter has a much greater phase shift than the speaker.

5.2.2 Speakers with Slightly Higher Power Rating

The additional power from switching signal dissipated by the speaker can overheat and damage the voice coil. The speaker power rating must be specified to ensure that the additional power will not damage the voice coil. The additional power can be calculated using equation 6, where P_{SW} is the added power dissipated in the speaker, $I_{DD(q)(with\ speaker\ load)}$ is the quiescent current measured with speaker load, $I_{DD(q)(no\ load\ or\ filter)}$ is the quiescent current measured with no load, V_{DD} is the supply voltage, and N is the number of channels.

$$P_{SW} < \frac{\left(I_{DD(q)\ (with\ speaker\ load)} - I_{DD(q)\ (no\ load\ or\ filter)}\right) \times V_{DD}}{N} \quad (6)$$

Using the quiescent current measured in Section 7, the added power from the switching waveform can be calculated. A quiescent current of 83 mA was measured with the TPA005D02 EVM connected to the speakers provided with the TI plug-n-play platform kit. The supply current with no load was measured to be 23 mA. A 5-V supply was used, and the TPA005D02 is a stereo device, so N = 2. Thus, the maximum added switching power dissipated in the speaker is 150 mW. Thus, the filter solution requires 3-W speakers and the filterless solution requires 3.15-W speakers.

Even using the notebook speaker from Section 7, which had a quiescent current of 215 mA in the same example, only requires an additional 0.5 Watts per speaker. As long as the designer allows for the added power dissipated in the speaker, damage to the voice coil can be avoided.

6 Filter Component Effect on Efficiency

Like the speaker for the filterless application, the filter must have a phase shift close to 90 degrees near the switching frequency to limit the amount of power dissipated in the filter. Estimating added quiescent current due to filter loss is much easier than estimating speaker loss without a filter because the inductance and series resistance of the filter is much more constant over frequency than the impedance of a speaker.

The first step in calculating the filter loss is to calculate the ripple current through the inductor. The following calculation will focus on the half filter with a class-D amplifier with the full H-bridge and the A-D modulation scheme. During the first half of the switching period, the voltage across the inductor is at the positive supply voltage, and during the second half of the switching period is the negative of the supply voltage. The rate of change of the inductor current can be calculated using equation 7, where V is the voltage across the inductor, L is the inductor value, and di/dt is the rate of change of the inductor current.

$$V = L \times \frac{di}{dt} \tag{7}$$

The magnitude of the voltage across the inductor is constant over each half of the switching period, only changing in polarity. Thus, di/dt is constant for a constant inductance. The constant inductance generates a triangle wave with a peak-to-peak current given by equation 8.

$$i_{L\,(pk-pk)} = \frac{T_{SW} \times V_{DD}}{2 \times L} = \frac{V_{DD}}{2 \times L \times f_{SW}} \tag{8}$$

Using the inductor current and the resistance of the filter and other components, the power dissipated in the output filter can be calculated. The resistance, R, is a combination of resistances that are in the path from the power supply to ground through the filter. R includes two $R_{DS(on)}$s, the DCR of the inductor, the ESR of the filter capacitor, the resistances of the circuit traces, and the ESR of the power supply capacitor. The ESR of the power supply capacitor is required because the majority of the current from the switching waveform is provided by the power supply capacitor. Equations 7 and 8 show the filter loss when not switching, as a more complicated equation is required to include switching losses. For very low transistor switching times, however, equations 9 and 10 are relatively accurate.

$$P_{Filter} = \frac{i_{L\,(pk-pk)}^{\,2} \times R}{6} \tag{9}$$

$$P_{Filter} = \frac{(V_{DD})^2}{24 \times L^2 \times f_{SW}^{\,2}} \times \left(DCR_{filter\,L} + ESR_{filter\,C} + \left(2 \times R_{DS(on)}\right) + ESR_{supply\,C}\right) \tag{10}$$

The change in the quiescent current per channel, shown in equation 11, is the power calculated in equation 10 divided by the supply voltage then multiplied by the number of channels.

$$\Delta I_{DD(q)} = \frac{N \times V_{DD} \times \left(DCR_{filter\ L} + ESR_{filter\ C} + \left(2 \times R_{DS(on)}\right) + ESR_{supply\ C}\right)}{24 \times L^2 \times f_{SW}{}^2} \quad (11)$$

Note that the value of the inductor and the switching frequency have much more of an effect on the power dissipated than any of the resistive elements in the filter. To demonstrate the effect of the inductor on the change in supply current, consider an example using the TPA005D02. The TPA005D02 is a stereo device that has an $R_{DS(on)}$ of 310 mΩ, a switching frequency of 250 kHz, and an assumed value for $DCR_{filter\ L} + ESR_{filter\ C} + ESR_{supply\ C}$ is 0.38 Ω. If a 15-µH inductor is used, ΔI_{DD} = 6 mA, and if L = 30 µH, ΔI_{DD} = 1.5 mA.

The supply current will be slightly higher than the calculated ΔI_{DD} added to the quiescent current with no filter or load, because there are other losses and the filter components are not ideal. Most inductors are rated at ±20%, which means that a 30-µH inductor could have an inductance between 36 µH and 24 µH.

The total quiescently dissipated power, P_Q, is given by equation 12, where P_{SW} is the switching loss and $P_{Q(No\ load\ or\ filter)}$ is the quiescent power dissipated with no load or filter. P_Q is independent of output power.

$$P_Q = P_{Q\ (No\ load\ or\ filter)} + P_{Filter} + P_{SW} \quad (12)$$

Switching losses actually increase slightly with output power, but the increase is minimal and is dominated by conduction losses, which are the power dissipated in the output transistors and filter. Due to how the filter components affect efficiency, it is important to select components with low resistance to get the maximum efficiency from a class-D amplifier. The efficiency of a class-D amplifier is shown in equation 13.

$$\text{Efficiency} = \frac{P_{OUT}}{P_{OUT} + \frac{P_{OUT}\left(2 \times R_{DS(on)} + DCR_{filter\ L}\right)}{R_L} + V_{DD}\ I_{DD\ (q)\ (no\ load\ or\ filter)} + P_{Filter} + P_{SW}} \quad (13)$$

7 Quiescent Current

While the quiescent current of a class-AB amplifier is constant regardless of load, the quiescent current of a class-D amplifier is more complicated and changes with filter and load. The quiescent current of the class-D amplifier takes into account quiescent current with no load or filter, filter loss, and switching loss.

The quiescent current for the full filter, half filter, and no filter applications were measured and appear in Table 2.

Table 2. Quiescent Current for Various Filter Applications Using the TPA005D02 and the TPA0102

APPLICATION	LOAD	L (μH)	$I_{DD(q)}$ (mA)
Full Filter	Any size resistor or speaker load	15	39
Half Filter (L = DS3316–P–xxx)	Any size resistor or speaker load	15	42
	Any size resistor or speaker load	22	35
	Any size resistor or speaker load	33	29.5
	Any size resistor or speaker load	47	27
Half Filter (L = DS5022–P–xxx)	Any size resistor or speaker load	68	25
	Any size resistor or speaker load	100	24
	Any size resistor or speaker load	150	23
No Filter	Notebook speaker	N/A	215
	NXT speaker	N/A	199
	TI P-N-P speaker	N/A	83
	Bose 151 speaker	N/A	83
	No speaker	N/A	23
TPA0102	Any load	N/A	19

The quiescent current of the full filter and half filter applications were independent of the load and varied greatly with the filter inductor value. The no filter application quiescent current, however, was dependent on the inductance of the speaker. The full filter quiescent current was measured using the filter designed for a 4-Ω load, where L1 = L2 = 15 μH, C2 = C3 = 0.22 μF, and C1 = 1 μF, with the components labeled in Figure 1. The quiescent current of the half filter application shown in Figure 2 was measured with C = 1 μF, and L was varied to show how increasing inductance decreases ripple current at the output.

The recommended half circuit filter for a 4-Ω load is L = 33 μH and C = 1 μF, which had a quiescent current of 29.5 mA. The recommended half filter for an 8-Ω load is L = 68 μH and C = 0.56 μF, which had a quiescent current of 25 mA. The quiescent current for the filterless application varied with load. The TI P-N-P speaker and the Bose 151 speaker had quiescent current of 83 mA, while the lower inductance flat panel NXT speakers [3] had a quiescent current of 199 mA. A commercial notebook speaker was even less inductive and resulted in a quiescent current of 215 mA. The class-AB amplifier had a quiescent current of 19 mA, which was much lower than the class-D with no filter and is less than half the class-D with full filter, but not much lower than the class-D with half filter.

8 Fidelity

Total harmonic distortion plus noise (THD+N) and intermodulation distortion (IMD) are the two most common measurements used to rate the sound quality or fidelity of an amplifier. THD+N and IMD were measured for the full filter, half filter, and no filter applications. Each measurement was done using the TPA005D02 class-D 2-Watt amplifier. A measurement was made in each case with the TPA0102 class-AB amplifier to use as a comparison. The measurement set up and results are discussed for each test.

8.1 Total Harmonic Distortion Plus Noise (THD+N)

THD+N versus output voltage and THD+N versus frequency were measured with the Audio Precision II analyzer. In each measurement, an RC filter with a cutoff frequency of 37 kHz was added between the output to ground to filter out the common mode signal into the analyzer. The bandwidth of the analyzer was set to 10 Hz through 22 kHz and an internal 20 kHz low-pass filter was also used to ensure that the switching frequency did not influence the THD+N measurement. In other words, band-limiting the measurement ensured that only the audible harmonic distortion and noise were measured.

Amplifier gain was 22.5 V/V. The gain of the TPA005D02 is fixed at this value and the gain of the TPA0102 was set to this value with external resistors, which put the TPA0102 at a slight disadvantage because it exhibits higher performance at lower gains. THD+N versus output voltage at 1 kHz was measured with the TPA005D02 with full filter, half filter, and no filter. The same test was performed using the TPA0102. The measured THD+N versus output voltage is shown in Figure 6.

The class-D full filter and half filter applications had approximately the same THD+N across all power levels. The class-D without the output filter actually had lower THD+N at the lower power levels than the TPA005D02 with the filter and the TPA0102. The TPA0102, had approximately the same THD+N as the TPA005D02 with the full and half filters at low- to mid-powers, and lower THD+N at the higher powers.

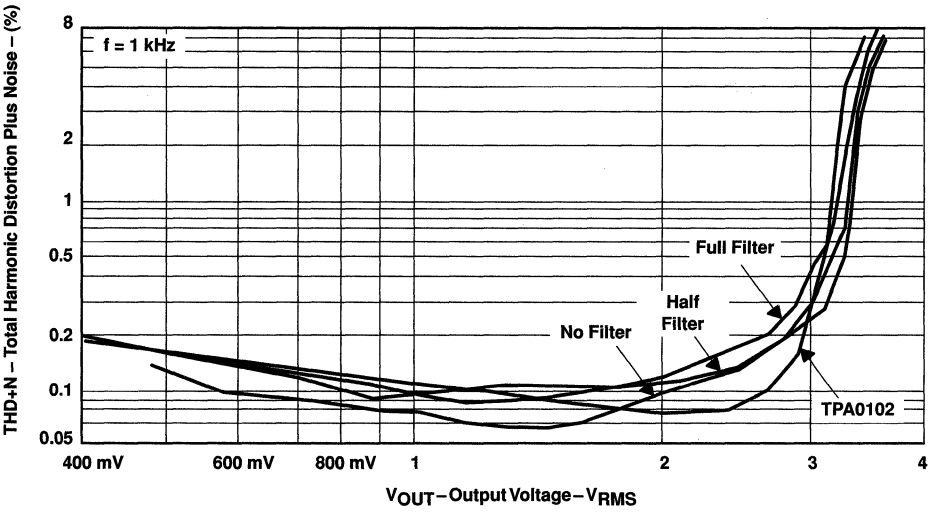


Figure 6. Total Harmonic Distortion Plus Noise vs Output Voltage

THD+N versus frequency was set up the same way that the THD+N versus output voltage was configured, but the output voltage was set to 2.5 V. Figure 7 shows that the THD+N is approximately the same for the different class-D filter options, and the TPA0102 THD+N was less than 0.1% lower than the class-D. The THD+N is relatively constant over frequency for all devices. Then the THD+N decreases at frequencies greater than 10 kHz, because of the filtering done by the Audio Precision II.

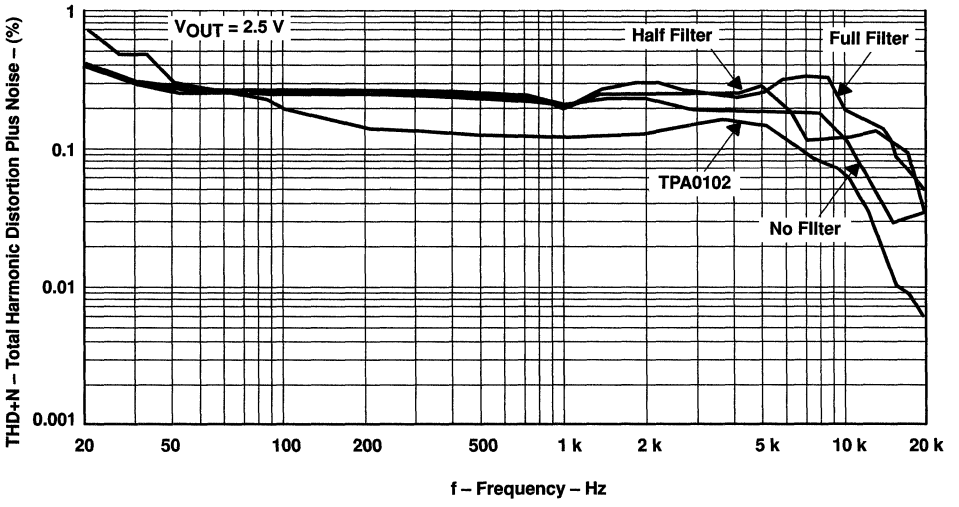


Figure 7. Total Harmonic Distortion Plus Noise vs Frequency

8.2 Intermodulation Distortion (IMD)

Intermodulation distortion (IMD) occurs when two or more signals of different frequencies are input into an amplifier and the sum and difference of the input frequencies are present at the output. IMD is a good measurement of linearity (the lower the IMD, the more linear the device under test). IMD is the ratio of magnitude of the sum and difference signals to the original input signal. The IMD equation is shown below; where V_{f2} is the voltage at the input frequency f2, V_{f2+f1} is the voltage at the sum of input frequencies f1, and f2, V_{f2-2f1} is the voltage at the difference of input frequencies f1 and 2f2, etc.

$$IMD = \frac{\sqrt{\left(V_{f2-f1} + V_{f2+f1}\right)^2 + \left(V_{f2-2f1} + V_{f2+2f1}\right)^2 + \left(V_{2f2-f1} + V_{2f2+f1}\right) + \cdots}}{V_{f2}} \quad (14)$$

The Society of Motion Picture and Television Engineers (SMPTE) standard IMD test is the most common IMD measurement. The SMPTE IMD test inputs a low frequency (60 Hz) and high frequency (7kHz) sine wave into the device. The low frequency sine wave has four times the amplitude of the high frequency sine wave [4]. The SMPTE IMD versus input voltage of the class-AB and class-D amplifier with the full filter, half filter, and no filter was measured and is shown in Figure 8.

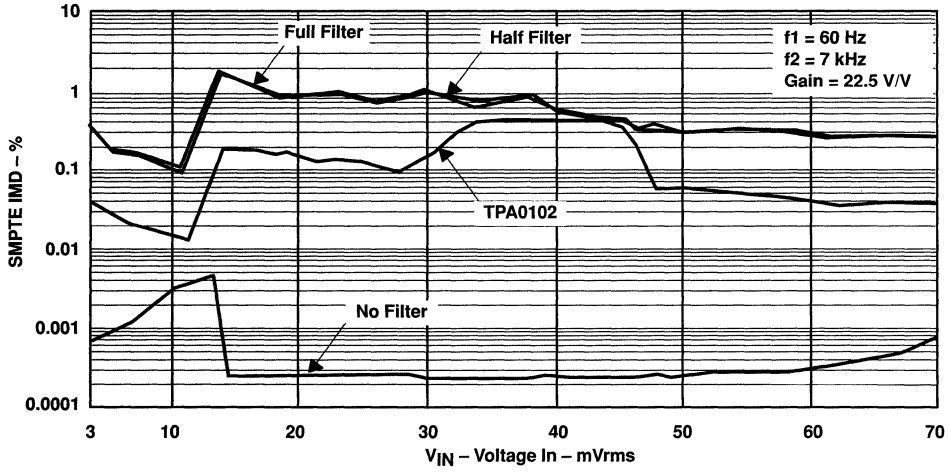


Figure 8. SMPTE Intermodulation Distortion vs Input Voltage

The same set up used for the THD+N measurement was used for the IMD measurements. The full and half filter circuits had equal IMD, and had slightly higher IMD than the class-AB amplifier. The class-D without a filter had the lowest IMD.

The CCIF, or Twin-Tone, IMD is another distortion measurement of the amplifier using two high frequency input signals of equal amplitude. Figure 9 shows CCIF IMD versus difference frequency. The center frequency was set to 13 kHz and the difference frequency was swept from 80 Hz to 1 kHz. The class-D amplifier with full filter had the highest CCIF IMD, ranging from 0.4 % to 0.5 %, and the half filter application CCIF IMD was approximately 0.1% lower over the tested frequency range. The class-AB amplifier had a lower CCIF IMD, which was 0.05 %. The class-D without an output filter had the lowest CCIF IMD, which was 0.01 %.

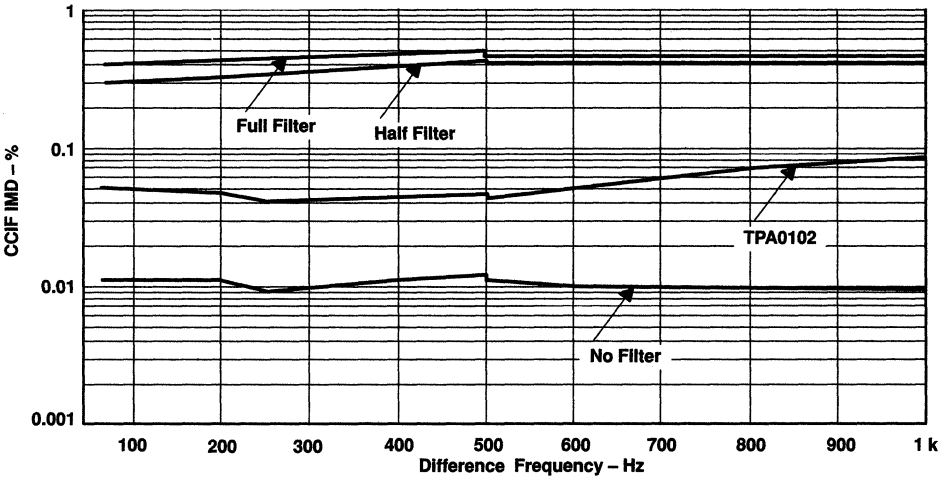


Figure 9. CCIF Intermodulation Distortion vs Difference Frequency

9 Electromagnetic Interference (EMI)

Radiated electromagnetic interference (EMI) is radiation caused by the transfer of electromagnetic energy through a nonmetallic medium, such as air. EMI is caused either by an instantaneous change in current resulting in a magnetic (H) field or by a differential voltage resulting in an electric (E) field. The inductor in the filter, or the inductance in the speaker if not using a filter, keeps the change in current low, which decreases the magnetic field. The electric field, which is a common mode issue, could be quite large due to the switching voltage.

The full filter includes a differential and a common-mode filter, so the E and H fields are attenuated. The half filter has a differential filter, but no common mode filter. The differential filter is good for lowering quiescent current but does not help to decrease EMI. Without the filter, the inductance of the speaker keeps the output switching current low, which reduces the magnetic field and makes the electric field dominant. The good news about the EMI is that the electric field can be easily shielded and common mode methods of reducing EMI will work. If EMI is a problem, the designer should use shielded speaker wires and speakers, and make the amplifier and speaker enclosure into a shield if possible.

The E and H fields of the speaker wires and the traces near the TPA005D02 were measured with the full filter, half filter, and no filter applications, using an oscilloscope and EMCO E and H field probes (EMCO 7405–904 and EMCO 7405–901). The circuit was configured with both channels of the TPA005D02 EVM active with no input to see the EMI generated by the switching waveform.

An 18-inch speaker wire connected the EVM to the speaker. Each speaker was spread apart, away from the EVM board to ensure the EMI from the traces did not add to the EMI measured from the speaker wire and vise versa. The measurements were done in the near field, one-half inch above the traces and speaker wire. The measurements were done in the time domain to enable the system designer to see from what part of the switching waveform the EMI was radiating.

9.1 E and H Field Measurements

Figure 10 shows the E field measured one-half inch above the speaker wires for the full filter, half filter, and no filter applications. Although both channels were active, the EMI was measured over the speaker wire of only one of the channels. The full filter E field at one-half inch was below the noise level of the system. The half filter radiated approximately 5 mV peak-to-peak at the switching edges. The half filter had a maximum peak-to-peak voltage of 25 mV.

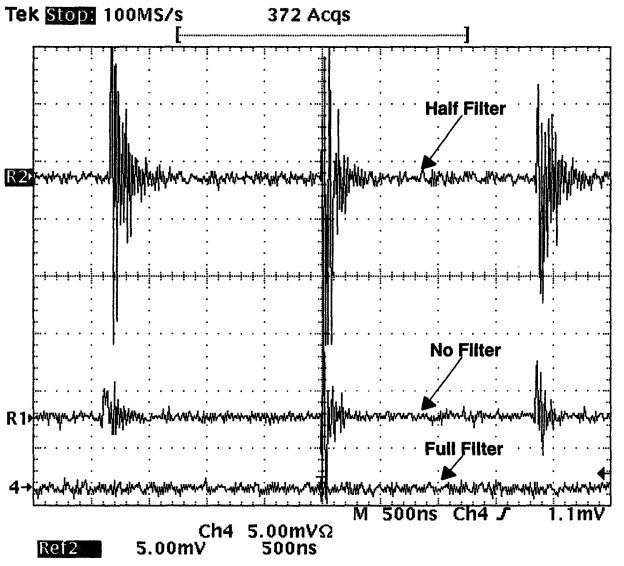


Figure 10. E Field Measured ½ Inch Above Speaker Wire

Figure 11 shows the H field of the full filter, half filter, and no filter class-D applications measured one-half inch above the speaker wire. Again, the EMI of the half and no filter applications is generated from the switching edges and the EMI of the half filter is greater than that of the class-D without the filter. The H field generated by the class-D with the full filter is lower than the noise floor.

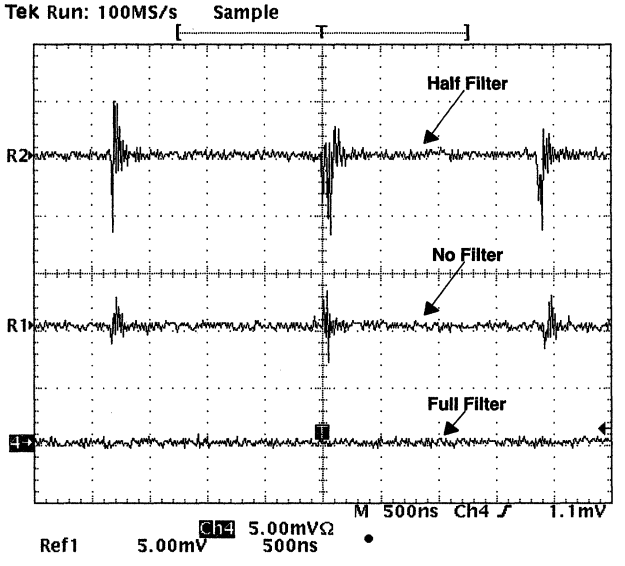


Figure 11. H Field Measured ½ Inch Above Speaker Wire

Figure 12 shows the E field of the full filter, half filter, and no filter applications measured one-half inch above the traces near the TPA005D02 on the TPA005D02 EVM. In this measurement, both channels were active, so unlike the EMI measured from the speaker wire, both channels will add to the measured near-field E and H fields.

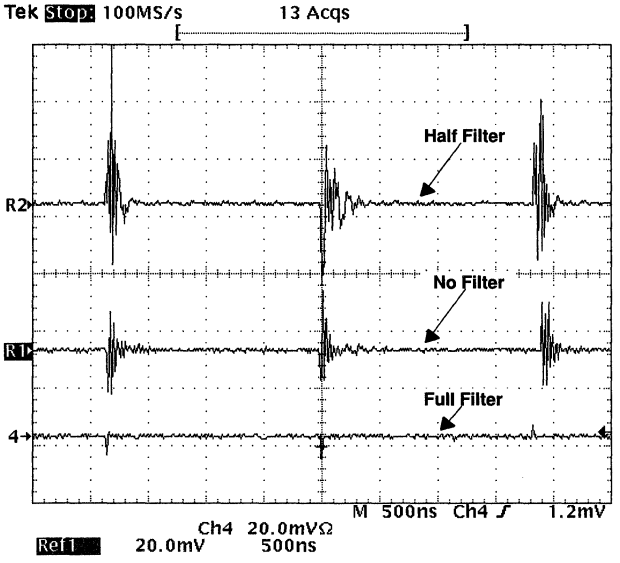


Figure 12. E Field Measured ½ Inch Above Class-D Output Traces

Figure 13 shows the H field generated by the class-D with a full filter, half filter, and without a filter, measured one-half inch above the output traces.

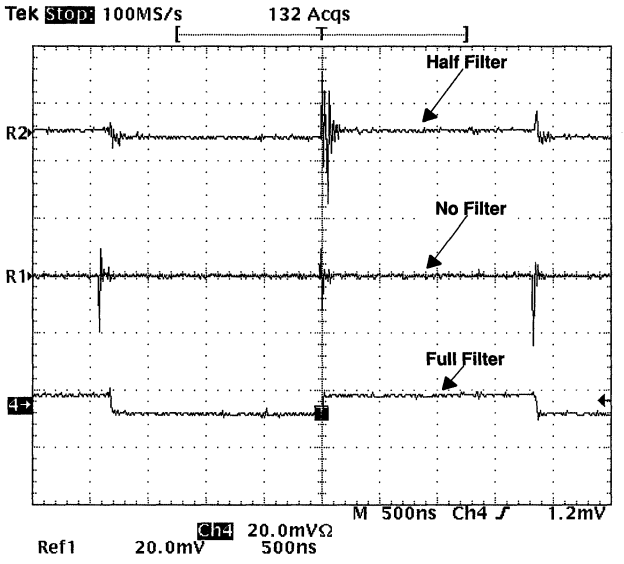


Figure 13. H Field Measured ½ Inch Above Class-D Output Traces

9.2 EMI Measurement Conclusions

Full Filter

The class-D amplifier is designed to have switching MOSFETs create a rail-to-rail square wave that is driven into an inductor. The inductor keeps the current from changing despite the fact that the voltage changes very rapidly at the switching edges. The rapid rise and fall times of the voltage at the input to the inductor in conjunction with the inductor keeping the current constant generates transients at the output. The full filter has capacitors to ground at the output that form a high frequency ac path to ground, which reduces the transients at the output. Unlike the half and no filter applications, the E and H fields radiating from the speaker wire, shown in Figures 10 and 11, are below the system noise floor, which is a direct result of these capacitors to ground.

The EMI above the traces of the full filter application were much worse than above the speaker wire. The E field had small transients at the switching edges. The E field around the output traces was also much smaller than the half and no filter applications because of the capacitor to ground in the full filter. However, the H field measured at one-half inch was much worse than the full and half filters, because the inductors with the H field probe act as a transformer. The windings of the inductors act as the primary and the loop of the H field probe as the secondary. The shielded inductors drop the amplitude of the H field, but it is still very easy to make out the square wave in Figure 13. The H field drops off with distance at a much faster rate than the E field. Therefore, the H field is a concern in a system with a nearby current loop that might pick up the EMI from the inductors, but the EMI due to the H field radiated from the inductors at a distance should not be a major concern.

Half Filter

The major difference between the full and half filter is that the half filter does not have the capacitors to ground, just a differential filter. The positive output is filtered with respect to the negative output, where both outputs are applying the AC transients to each other without giving the transients a path to system ground. These transients at the output, which are caused by the inductor keeping the current constant during switching, caused EMI at the switching times. The EMI at the switching times was evident in both E and H fields, both above the traces and above the speaker wires.

The EMI from the half filter application was even greater than that of the no filter application because the speaker has resistive elements which reduce the sharp voltage transients at the output. The H field above the traces was very similar to that of the full filter. Again, the inductors and the H field probe essentially formed a transformer. The H field of the half filter had approximately half the magnitude of the full filter because there was only one transistor to inductively couple with the probe.

No Filter

Similar to the filtered applications, the EMI from the filterless circuit was generated at the switching edges. The E field was greater than the H field with no filter in all cases. The class-D without a filter had less EMI than the half filter for three main reasons. First, common mode EMI is dominant and the half filter only forms a differential filter with no low impedance AC path to system ground. Second, the filterless application was more resistive, causing less dissipation at the switching times. Third, the half filter has an inductor that creates a transformer effect with any other current loops.

9.3 Reducing EMI

Reduced Wire Length

Reducing the length of the traces and speaker wire will reduce EMI. Shortening and widening the output traces and wires reduces the inductance of the wire, which reduces the E field generation. Shortening the wire also reduces H field because it makes the current loop smaller. Therefore, it is very important to place the speakers as close to the amplifier as possible, reducing the wire length, especially in the half filter and no filter applications.

Shielded and Toroid Inductors

Shielded inductors were used in the EMI measurements described above, which significantly reduced the EMI over the nonshielded inductors. A problem with these inductors, however, is that the windings are wrapped such that the current flow is parallel to the board, causing inductive coupling with any current loop near the inductors. If the inductor were wrapped such that the current flow were perpendicular to the plane of the circuit board, inductive coupling with current loops would be greatly reduced. The inductor should also be shorter. The taller inductor causes a longer the magnetic field path, which causes the EMI to be higher further away from the inductor.

If shielded inductors are not sufficient, a toroid inductor may provide a solution. The toroid is made of a donut-shaped core with a high permeability. The windings are wrapped from the outside through the center of the core, which causes the magnetic field generated from the current flowing through the windings to be confined to inside the core. However, the core is not ideal and must have gaps, which are sources of radiation. A powder core radiates less than a core with a single air gap, because a powder core has several very small air gaps throughout, causing very little radiation compared to one large air gap.

Shielded Speakers

Similar to the filter inductor, the voice coil in a speaker can be a radiator that causes inductive coupling. Shielded speakers were originally designed so they could be placed next to a monitor without the magnet from the speaker affecting the image generated by the cathode ray tube. The shield itself on a shielded speaker is just a metal cap with a high permeability placed over the permanent magnet. The cap does not totally envelop the magnet, but rather provides a path of less magnetic resistance. In other words, the shield keeps more of the magnetic field in the shield itself rather than in the air. Reducing the magnetic field in the air reduces both the magnetic radiation from the magnet and also from the voice coil.

Shielded Speaker Wires

Standard speaker wire is not designed for low EMI radiation because it was intended to carry waveforms of frequencies from 20 Hz to 20 kHz, which have very little EMI problems. When using a class-D amplifier with a half filter or no filter, it may be necessary to shield the wires. A shielded twisted pair cable is recommended for reducing EMI, because the shield reduces the radiation path to ground and the intertwined wires tend to cancel some of the common mode signal.

When using a shielded twisted pair cable, choose a single point to ground the shield as close to earth ground as possible. Also, ensure that the shield does not pick up radiation in routing itself to ground, because it could make the shield into an antenna. It may be necessary to take the ground from another part of the system to avoid pickup in the shielding and to have a good ground reference. In doing this, however, make sure that the pickup from the shield is not injecting the switching noise into that part of the circuit. The recommended circuit diagram showing the shielded wire appears in Figure 14.

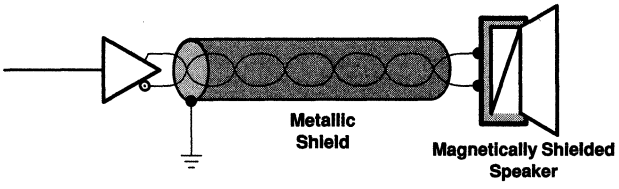


Figure 14. Shielded Twisted Pair Speaker Connection

The E and H fields of the shielded twisted pair and the standard speaker wire were measured using the same method used in the EMI measurements above. Both the E and H fields of the shielded twisted pair were lower than the standard speaker wire. The results are shown in Figures 15 and 16.

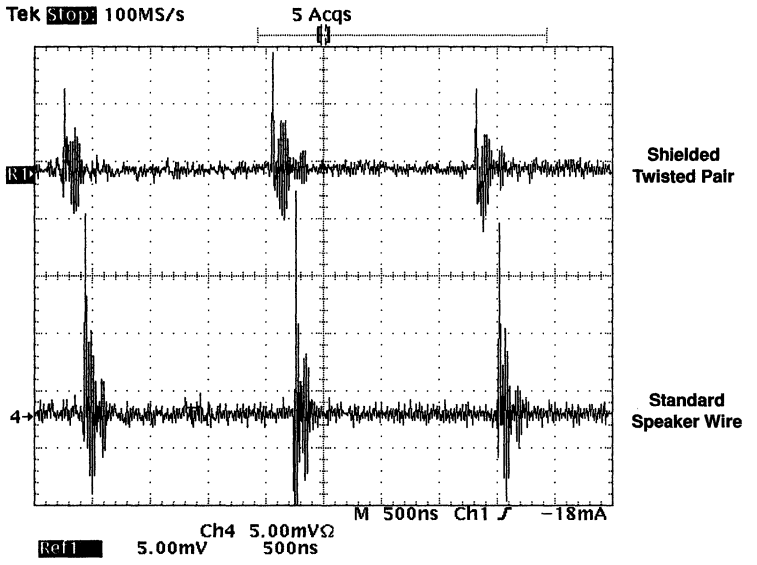


Figure 15. Standard Speaker Wire and Shielded Twisted Pair E Field vs Time

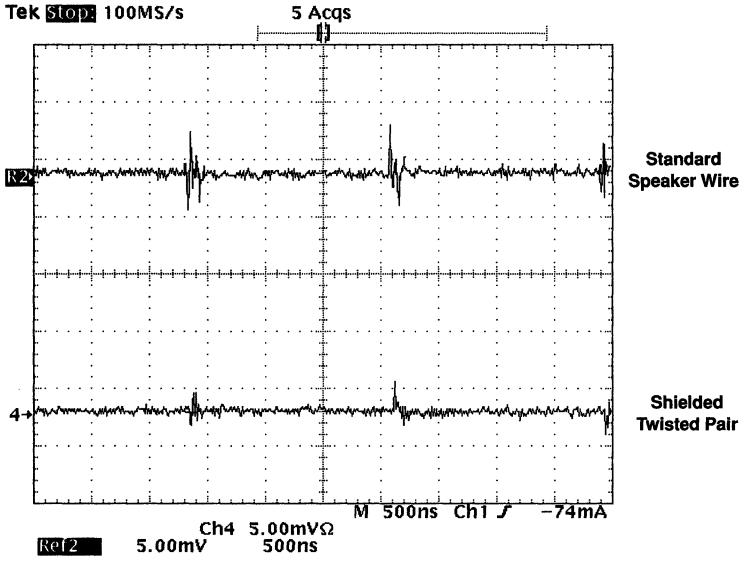


Figure 16. Standard Speaker Wire and Shielded Twisted Pair H Field vs TIme

Shielded Enclosure

The best method of shielding is using what most electronics already have, an enclosure. If coated properly, the enclosure can be made into a Faraday cage. There are many coatings that one can add to an enclosure to make it an effective shield. The higher the permeability of the coating material, the better the shield. The Faraday cage attenuates both the E field and the H field. To attenuate the H field, the shielding must completely enclose the source of radiation, but partial shielding will work in attenuating the E field.

10 Filter Selection from System Requirements

This section provides an overview of the results and provides recommendations on which filter to use with predetermined system constraints. Table 3 ranks each filter by category and shows system concerns that are met by each filter application.

Table 3. Performance Ranking of Full Filter, Half Filter, and No Filter Applications

APPLICATION	COST	$I_{DD(q)}$	THD+N	IMD	EMI	SYSTEM REQUIREMENTS
No Filter	1	3	1	1	2	**Primary:** low cost, low heat, high fidelity
						Secondary: long battery life, low EMI
						Example: stand-alone amplified speaker
Half Filter	2	2	2	2	3	**Primary:** long battery life, low heat
						Secondary: low EMI
						Example: notebook computer
Full Filter	3	1	2	2	1	**Primary:** low EMI, low heat
						Secondary: low cost
						Example: speaker far from amplifier

NOTE:
Applications are ranked by performance from 1 to 3 in each category: best = 1, worst = 3.

10.1 No Output Filter

The class-D without the output filter application not only had lower THD+N and IMD than the class-D with the filter, but also outperformed the class-AB device. The two big disadvantages of using the class-D amplifier without the output filter are high quiescent current and high EMI. Quiescent current can be lowered using a speaker with a high inductance, but it is doubtful whether it could ever be lower than an application that uses a filter. EMI can be lowered using ferrite beads at the output of the amplifier, shielded speakers, and shielded speaker wires. EMI can also be reduced by making the distance from the amplifier to the speaker as short as possible and keeping the positive and negative output wires very close together to reduce common mode radiation.

A good application for a class-D amplifier without a filter is one in which quiescent current and EMI are not important, but system cost, maximum power supply current rating, and heat are important. A good example of this is a powered speaker. The class-D without the filter is less efficient than the class-D with the filter at lower output levels, due to the higher quiescent current. However, the class-D efficiency is approximately the same with and without the filter at high output levels (2 to 3 times more efficient than class-AB).

A 10-W powered speaker could use a class-D amplifier without the output filter or heat sink, and use a lower-rated power supply than a class-AB amplifier. The system cost of this application is less than the class-D with the full filter or half filter because the filter is eliminated, and is very close to the cost of the class-AB solution, if not less expensive. The heat sink is eliminated and the power supply is reduced in a 10-W class-D filterless application, but the class-D amplifier itself is slightly more expensive than an equivalent class-AB amplifier. As mentioned in Section 9, the speaker inductance must be high, and the amplifier must be close to the speaker.

10.2 Half Filter

Class-D with a half filter had a lower quiescent current and performed as well or better than the class-D with full filter in THD+N and IMD. The quiescent current diminishes as the value of the inductor of the half filter increases. However, as inductance increases, peaking occurs at the corner frequency of the filter. The corner frequency can be set outside the audio band so the peaking has no effect on sound quality. Peaking occurs regardless when using a speaker load and the filter was designed for a resistive load. The half filter designed for a 4-Ω resistive load uses a 33-μH inductor with a 1-μF capacitor, and the half filter designed for an 8-Ω resistive load uses a 68-μH inductor and a 0.56-μF capacitor.

Each of these examples exhibits peaking at the corner frequency because the speaker is not purely resistive at the corner frequency. An RC Zobel network can be placed in parallel with the load to reduce reactance of the load to limit peaking. If quiescent current is very important, the designer can increase L and lower C. This will decrease quiescent current and keep the corner frequency in place. The designer should design the filter with the speaker load to ensure the corner frequency peaking is outside the audio band.

The only disadvantage with the half filter application is it has higher common mode EMI than the full filter due to the filter not having a common mode filter. The common mode EMI should not be a problem in most systems if the positive and negative output signal paths are very close, wire lengths are short, and shielding is used. The filter should be as close to the amplifier as possible to reduce EMI. EMI can be further reduced with ferrite beads, shielded speaker wire, and using good board layout.

The class-D with half filter is an ideal circuit where battery life, heat, and system cost are primary issues. The class-D with half filter is the most efficient circuit and has a lower cost than the class-D with full filter. These issues make the half filter class-D the ideal circuit for notebook PCs. Notebook PCs are very concerned with battery life and heat, while system costs are still important. EMI issues are well understood by notebook designers, so the additional EMI generated by the half filter implementation should not be a problem.

10.3 Full Filter

Class-D with full filter had lower IMD than the class-D without a filter and higher quiescent current than class-D with a half filter. It also has a higher system cost than either circuit. Designers should use class-D with the full output filter when heat, battery life, and EMI are all primary concerns. An example of this would be in a boombox, where the amplifier is in the same location as an AM receiver, where the switching frequency is close to the band of frequencies that the AM receiver is demodulating. Another example would be any device that has wires connecting the amplifier to the speakers. The wires act as an antenna, and if not filtered, the switching frequency could radiate to other devices in the vicinity.

11 Conclusion

It is possible to reduce the output filter in certain applications. The tests and measurements described in this application report prove that reducing the output filter does not mean a reduction in quality. The class-D amplifier with and without the output filter had approximately the same THD+N. The class-D amplifier actually had lower IMD without the output filter. The quiescent current of the class-D amplifier was lower using the half filter than the full filter, making the class-D amplifier even more efficient.

A designer that is primarily concerned with maximum heat and power supply constraints, and is not concerned with EMI and quiescent current, could use the class-D amplifier without a filter to save cost. A designer that is primarily concerned with heat and battery life and has EMI as a secondary concern could use a class-D amplifier with a half filter. Applications that are very EMI sensitive and/or have devices operating around the switching frequency of the class-D amplifier should use a full filter.

12 References

[1] TPA005D02 Class-D Stereo Audio Power Amplifier Evaluation Module Users Guide, Texas Instruments, Inc., September 1998, publications number SLOU032.

[2] Colloms, Martin, High Performance Loudspeakers, Pentech Press Limited, London, 1985, pp. 18–26.

[3] http://www.nxtsound.com/

[4] Metzler, Bob, Audio Measurement Handbook, Audio Precision, Inc., 1993, pp. 37–39.

For the latest information on TI audio power amplifiers, visit http://www.ti.com/sc/apa.

Contents

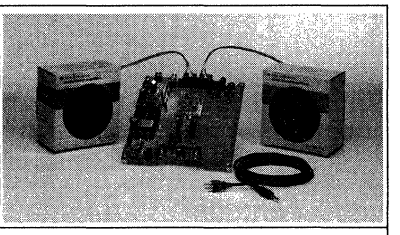
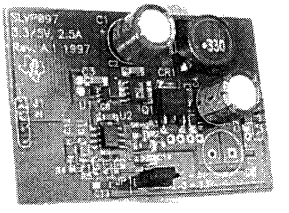
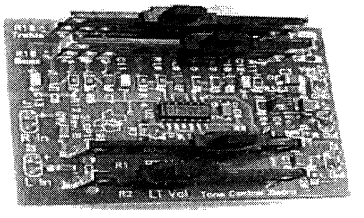
Audio Power Amplifier Plug-n-Play Evaluation Modules

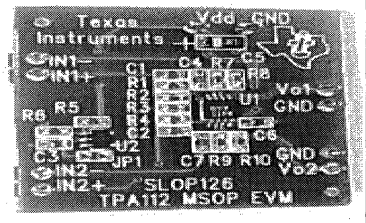
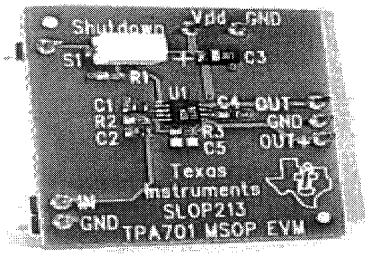
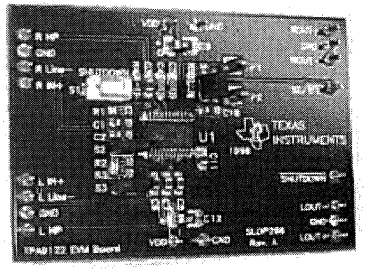
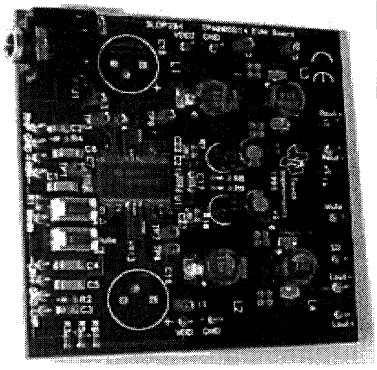
Texas Instruments is the only supplier that offers an audio power amplifier evaluation platform that allows designers to listen to any TI audio power amplifier in less than 30 seconds. TI develops an evaluation module (EVM) for every TI APA available. Each EVM plugs directly onto the Plug-n-Play platform. No soldering and no addition of external circuitry is needed, which significantly decreases preparation time and allows more time for actual evaluation.

The Plug-n-Play platform provides three dedicated sockets for testing either two mono amplifiers or one stereo amplifier. Headphone and speaker drivers can be evaluated simultaneously. Also provided is a 'signal conditioning' socket in order to tailor the platform to a particular application. The platform can be
powered by an external power supply or a 9-V battery which is plugged into an on-board socket. Together with DC-DC buck converter module it produces either a 5-V or 3.3-V supply.

The Table provides a description and a photo of the Plug-n-Play Base Kit and a sample of different APA EVMs that plug into the Plug-n-Play platform.

Table 1. Audio Power Amplifier Plug-n-Play Platform and sample individual modules.

The Plug-n-Play Base Kit provides the interface to the modular EVMs, stereo speakers and headphones, audio source and power supply. It has three dedicated sockets for testing either two mono or one stereo amplifier, a headphone socket and a 9-V battery socket. It also includes a DC/DC Converter and signal conditioning EVM.	
The DC/DC buck converter provides a 5 V or 3.3 V output with 2.5 A given an input voltage range of 5.5 V to 12 V. The TL5001 PWM controller operates at a nominal frequency of 275 kHz and is configured for a maximum duty cycle of 100% with built-in short circuit protection. Included with Plug-n-Play Base Kit.	
The Tone Control EVM provides volume and bass/treble control. This module uses the TLC2274 or TLC 074 quad rail-to-rail output operational amplifiers and the TLV2461 single rail-to-rail input and output operational amplifier. Included with Plug-n-Play Base Kit.	

The TPA112 is a stereo 150 mW single ended audio power amplifier ideal for driving headphones. The TPA112 EVM features the ultra-small 8-pin MSOP PowerPAD package that minimizes PCB space.	
The TPA701 is a 700 mW bridge-tied load (BTL) mono amplifier with ultra-low supply and shutdown current (I_{SD}= 5.5 nA). The TPA701 is characterized at 3.3 V and 5 V. The TPA701 EVM features the ultra-small 8-pin MSOP PowerPAD package that minimizes PCB space.	
The TPA0122 is a 2 W stereo audio power amplifier with internal gain-settings, and is optimized for fidelity. The amplifier is designed to drive both stereo speakers and stereo headphones. The TPA0122 EVM features the 24-pin TSSOP PowerPAD package.	
The TPA2000D2 is one of TI's next generation fully integrated, stereo Class-D audio amplifiers that extends battery life and lowers thermal dissipation. It is capable of driving stereo speakers at 2 W continuously with 5 Wpeaks and stereo headphones from a 5-V supply. The device also features improved shutdown control to further minimize supply current and extend battery life.	

The Plug-n-Play platform and the individual APA EVMs are available world wide. For a complete listing of all TI's APA EVMs and ordering information contact your local distributor or go to TI's website at: http://www.ti.com/sc/docs/tools/analog/index.html then choose ***amplifiers***.

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audio power analysis program

The Audio Power Analysis Program, only available from Texas Instruments, gives designers for the ability to simulate real world audio amplifier operation on any TI audio power amplifier. This program calculates **actual power dissipation** and **thermal analysis** that until now have been over-estimated with tonal analysis. By replacing tones with real music, the program gives insight into how audio systems truly operate.

When using tonal analysis to measure amplifier operation characteristics, general relationships between these tones and different types of music have to be assumed. This leads to over compensation in the audio power system because of the values that are used. The Audio Power Analysis Program allows the system designer to accurately account for the audio amplifier's needs in the system and then specifically design in the needed requirements.

The Audio Power Analysis Program uses .wav format files to calculate power, heat and current at every point in a waveform. Files of this format containing any user-recorded signals, music, voice or sounds can be used to accurately represent end product use.

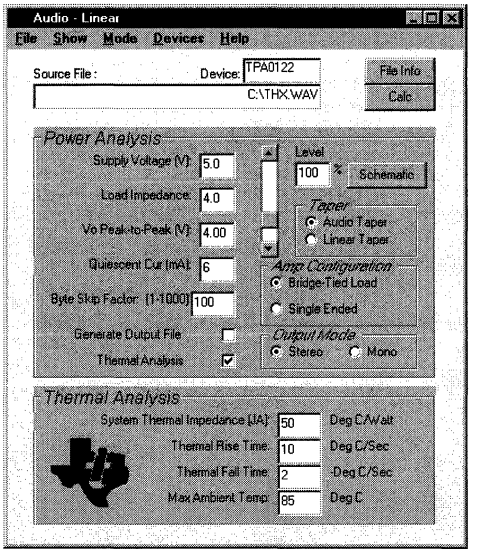

Figure 1. Audio Power Analysis Input Screen

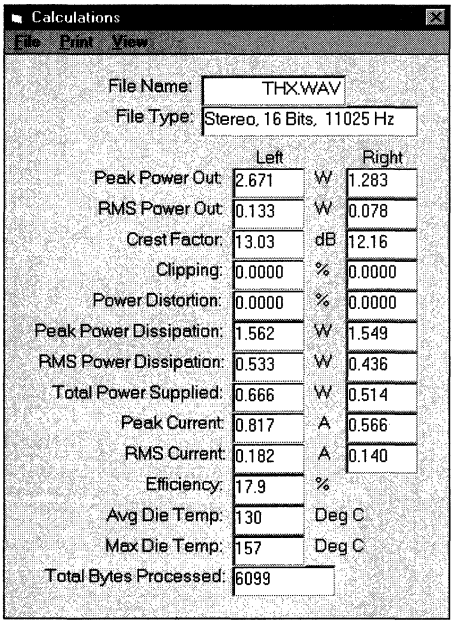

Figure 2. Audio Power Analysis Output Screen

By taking advantage of modern technological advances in microprocessors, the CPU now efficiently handles all of the complicated equations used in measuring characteristics of the amplifier and test clips.

The Audio Power Analysis Program makes an excellent companion for another audio amplifier support tool, the Plug-n-Play evaluation kit. Used in conjunction, these tools invite designers to a new method of designing the best audio systems possible. In today's modern designs, cost,

heat, space, and weight are all major concerns. Any reduction in unnecessary power management and supply componentry allows for smaller, lighter and more cost-effective solutions. The Audio Power Analysis Program allows designers to extend battery lives,

reduce transformer size and offer better power management options because of the new found application accuracy.

You can access more information about the Audio Power Analysis Program and download the software at: http://www.ti.com/sc/apasw

Plug-n-Play Audio Amplifier Evaluation Platform

User's Guide

SLOU011
April 1998

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Preface

Related Documentation From Texas Instruments

The TI Plug-N-Play Audio Amplifier Evaluation Platform is designed for use with TI audio power amplifier evaluation modules (EVM). Each audio amplifier EVM uses a TI audio amplifier integrated circuit and is shipped with a user's guide for the module and a data sheet for the IC. For information on additional TI audio ICs or audio EVMs:

- ***Amplifiers, Comparators, and Special Functions Data Book*** (TI literature number SLYD011) This data book contains the data sheets for the TI audio amplifier integrated circuits that are used in the TI Audio Power Amplifier Evaluation Modules
- Individual data sheets for TI audio amplifier integrated circuits
- User's guides for TI audio power amplifier evaluation modules

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Chapter 1

Introduction

This chapter provides an overview of the Texas Instruments (TI™) Plug-N-Play Audio Amplifier Evaluation Platform (SLOP097). It includes a list of features and a brief description of the platform illustrated with both a pictorial and a functional block diagram.

Topic **Page**

1.1 Feature Highlights

The TI Plug-N-Play Audio Amplifier Evaluation Platform includes the following features:

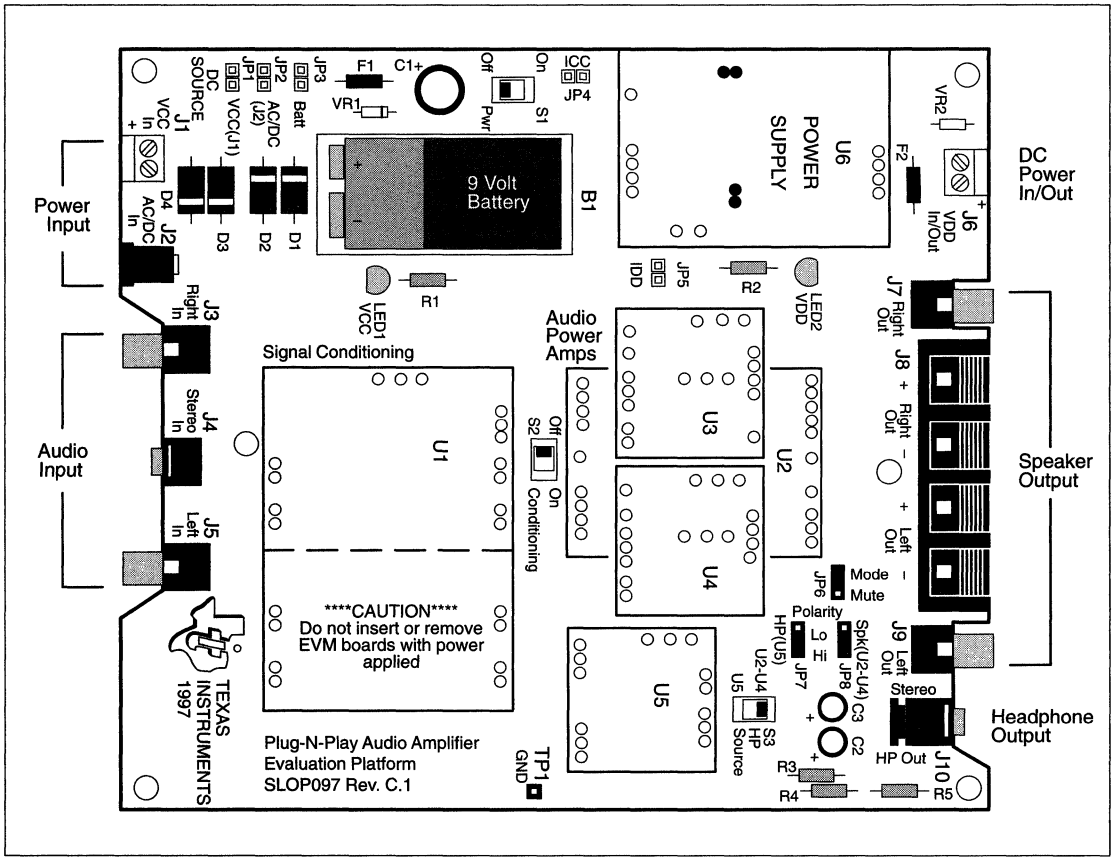
- Quick and Easy Configuration
  - TI evaluation modules simply plug into the platform
  - Evaluation modules are keyed and cannot be installed incorrectly
  - Install only as many modules as needed
  - On-board jumpers select power and control options
  - On-board switches route signals
  - Add or change modules at any time
- Flexible Power
  - On-board 9-V battery
  - External 5-V – 15-V DC V_{CC} supply input through screw-terminal connectors
  - External 5-V – 15-V AC/DC supply input through standard coaxial power connector
  - On-board bridge rectifier and filter for AC input-power conversion and conditioning
  - Socket for on-board 5 V/3.3 V V_{DD} voltage regulator EVM
  - External regulated V_{DD} input through screw terminals
  - On-board overvoltage and reverse polarity power protection
- Quick and Easy Audio Input and Output Connections
  - Left and right RCA phono jack inputs
  - Miniature stereo phone jack input
  - Left and right RCA phono jack outputs
  - Left and right compression speaker terminal outputs
  - Miniature stereo headphone jack output

1.2 Description

The TI Plug-N-Play Audio Amplifier Evaluation Platform is a convenient vehicle for evaluating, testing, and demonstrating TI's audio power amplifier and related evaluation modules (EVMs). The platform saves the time, trouble, and expense of having circuit boards designed and fabricated to evaluate a specific IC. TI audio EVMs simply plug into the platform, which automatically provides power to the modules, interconnects them correctly, and connects them to a versatile array of standard audio input and output jacks and connectors. Easy-to-use configuration controls allow the platform and EVMs to quickly model many possible end-equipment configurations. There is nothing to build, nothing to solder, and nothing but the included speakers to "hook up."

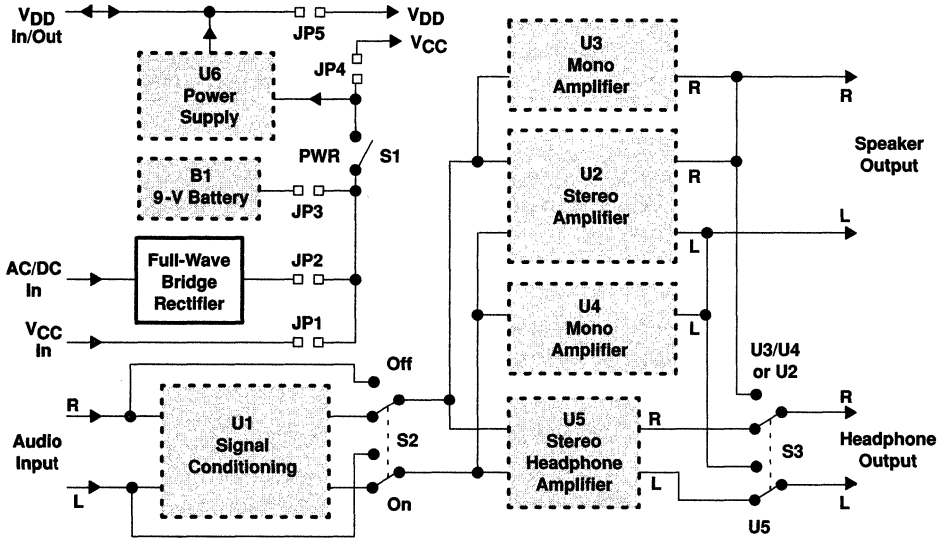
The platform consists of a 6.5 inch by 7 inch piece of G–10 circuit board equipped with various signal input and output connectors, power connections, pin-sockets for TI audio EVMs, and switches and jumpers for signal routing and option selection (Figure 1–1). All the inputs are at one end, the outputs are at the other end, and the EVM sockets are in between for a straight signal path.

Figure 1–1. The TI Plug-N-Play Audio Amplifier Evaluation Platform



The audio EVM sockets are arranged into two stages on the platform (Figure 1–2): an input signal conditioning stage (socket U1) and an output power amplifier stage (sockets U2 through U5). The signal conditioning EVM can include such functions as volume and tone controls as well as the mixing of several sources, and can be bypassed with a switch on the platform. The output amplifier stage can be populated with a wide variety of EVMs, including both single-channel and stereo units, and is intended to drive speakers and headphones.

Figure 1–2. Functional Block Diagram



Signals are input through either a pair of RCA phono jacks (left and right channels) or a miniature stereo phone jack. These inputs are grounded when the jacks are not in use. Signal conditioning EVMs may have additional input connectors, as in the case of the Microphone Mixer EVM (SLOP107), which has a microphone input jack mounted on its circuit board.

The platform includes a pair of sockets for single-channel power amplifiers (U3 and U4) and a socket for a stereo power amplifier (U2). These sockets physically overlap each other such that either one or both mono amplifiers can be installed, ***OR***, a single stereo amplifier can be installed — but not any combination of stereo with mono amplifiers. Output to speakers is through a pair of RCA phono jacks and compression connectors for use with stripped speaker wire.

Socket U5 is typically for a stereo headphone amplifier EVM. A miniature stereo headphone jack is capacitively coupled to either the headphone amplifier outputs or the power amplifier outputs as selected by a switch.

The platform V_{CC} supply can be provided by a wide variety of sources, including an on-board 9-V battery for low-power or short-duration projects and unregulated external AC or DC between 5 V and 15 V for other applications. For TI audio EVMs that require a regulated 3.3-V or 5-V V_{DD} supply, a voltage regulator EVM can be installed on the platform (U6), or external regulated V_{DD} power can be applied to a connector on the platform.

Chapter 2

Quick Start

This chapter contains a quick-start list that explains how to configure the platform, connect power, connect the inputs and outputs, and power up the system.

2.1 Precautions

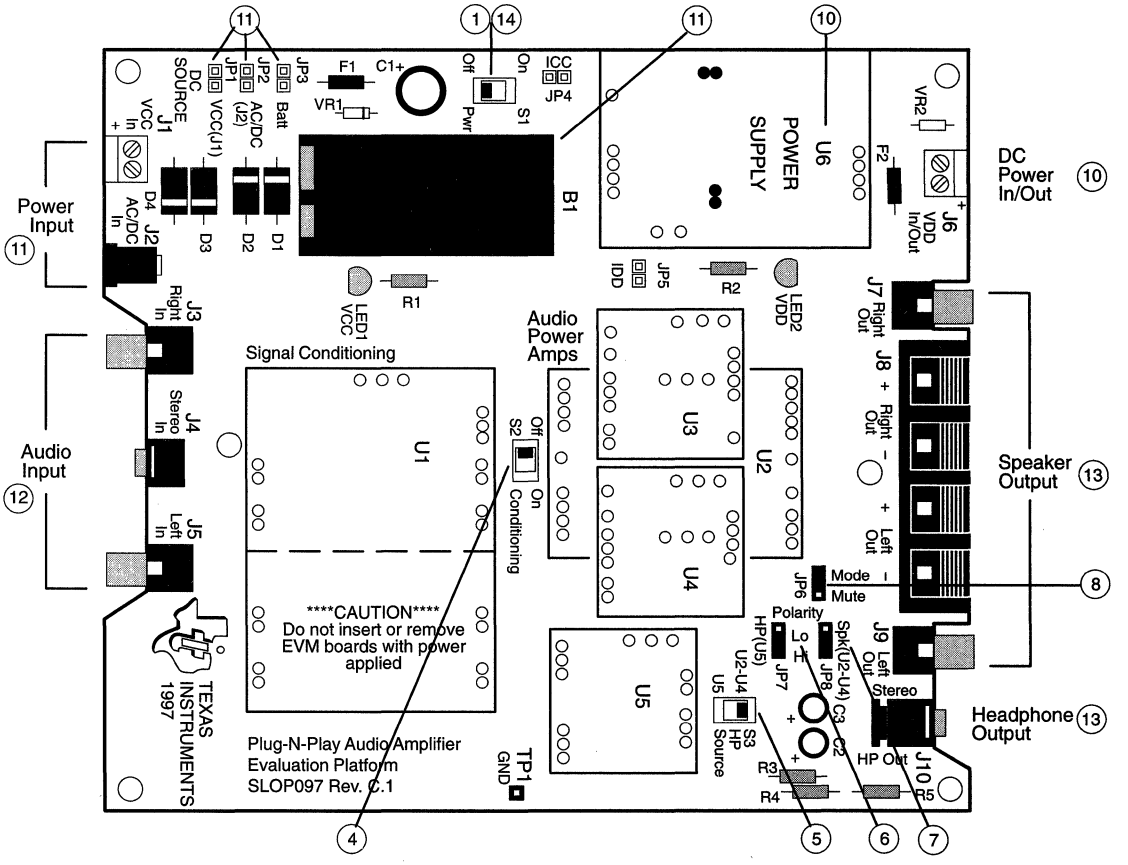
Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected to V_{CC} power input connector J1, J2, and/or V_{DD} power input connector J6 are correct. Overvoltage or reverse-polarity power applied to these terminals can open on-board soldered-in fuses and cause other damage to the platform, installed evaluation modules, and/or the power source.

Inserting or Removing EVM Boards

Do not insert or remove EVM boards with power applied — damage to the EVM board, the platform, or both may result.

Figure 2–1. Quick Start Map



2.2 Quick Start List

The following steps can be followed to quickly prepare the TI Plug-N-Play Audio Amplifier Evaluation Platform and EVMs for use. Numbered callouts for selected steps are shown in Figure 2–1 and details for each step appear in Chapter 3.

❑ **Configure the platform**

1) Ensure that all external power sources are set to ***OFF*** and that the platform power switch **S1** is set to ***OFF***; set gain controls to minimum
2) Select the TI audio evaluation modules to be used
3) Install the modules on the platform in the appropriate sockets
4) Use switch **S2** to select or bypass the signal conditioning EVM (U1)
5) If the headphone jack (J10) output will be used, set source switch **S3** to ***U5*** or ***U2–U4*** according to which sockets have power amplifiers installed
6) Consult the User's Guide for the power amplifier installed in U5 (if any) and set control signal **Polarity** jumper **JP7** to either ***Hi*** or ***Lo***
7) Consult the User's Guide for the power amplifiers installed in U2–U4 (if any) and set control signal **Polarity** jumper **JP8** to either ***Hi*** or ***Lo***
8) Consult the User's Guide for the power amplifiers installed in U2–U4 (if any) and set jumper **JP6** to select either the ***Mute*** or ***Mode*** control input

❑ **Connect power supplies**

9) Consult the User's Guides for the modules installed and select external power supplies that will provide a voltage appropriate for the modules installed (platform V_{CC} must be within the range of 5.5 V to 15 V, or 5.5 V to 12 V with a SLVP097 regulator module installed in U6, for example)
10) If any module installed on the platform requires a regulated V_{DD} of 3.3 V or 5 V for operation, install a SLVP097 regulator EVM (or equivalent) in U6 or connect an external regulated power supply adjusted to the correct voltage to screw terminals **J6,** taking care to observe marked polarity
11) Connect power to, and jumper ***ONE*** of the following V_{CC} power inputs:
    a) Connect an external DC power supply to screw terminals **J1,** taking care to observe marked polarity, and jumper **JP1**
    b) Plug a coaxial power connector (AC or DC) into **J2** and jumper **JP2**
    c) Install a 9-V battery into **B1** and jumper **JP3**

❑ **Connect inputs and outputs**

12) Connect the audio source to left and right RCA phono jacks **J3** and **J5** or stereo miniature phone jack **J4**
13) Connect 4-Ω – 8-Ω speakers to left and right RCA jacks **J7** and **J9** or to stripped wire connectors **J8**, or plug headphones into **J10**

❑ **Power up**

14) Verify correct voltage input polarity and set external power supplies to ***ON***, then set platform power switch **S1** to ***ON***

LED1 should light indicating the presence of V_{CC}, LED2 should light indicating the presence of V_{DD} (if used), and the evaluation modules installed on the platform should begin operation.

15) Adjust signal source levels and EVM gain controls as needed

Chapter 3

Details

This chapter provides details on the steps in the Quick-Start List and additional information on the TI Plug-N-Play Audio Amplifier Evaluation Platform.

Topic **Page**

3.1 Precautions

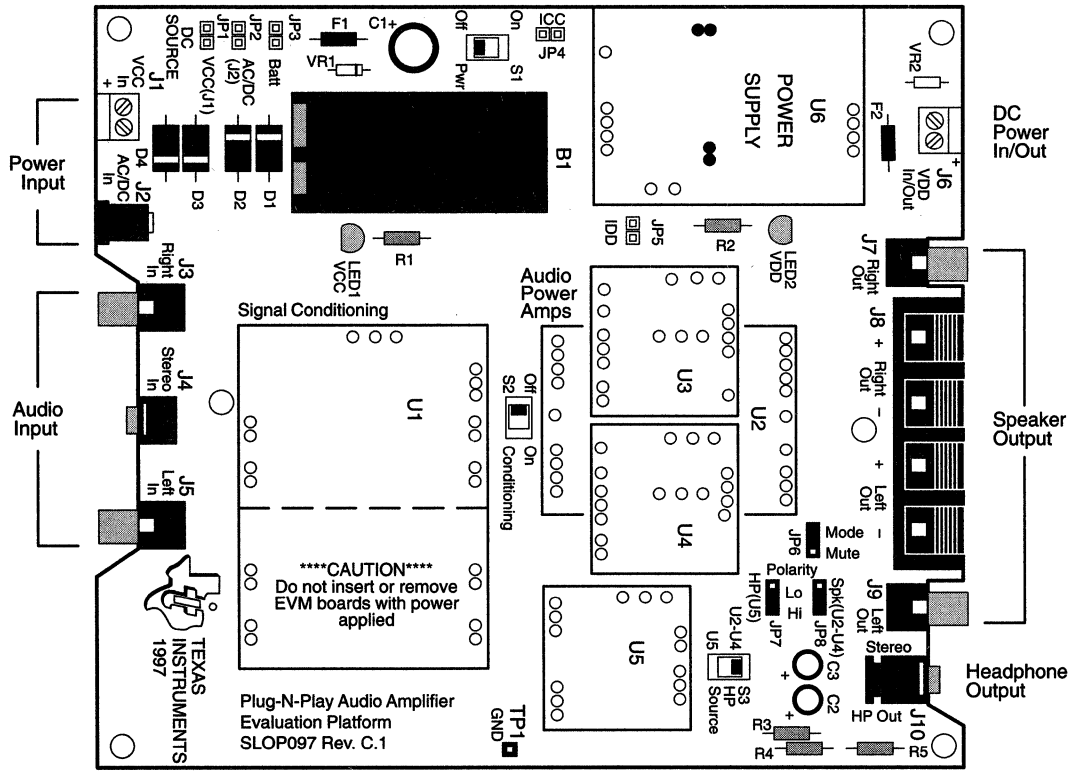
Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected to V_{CC} power input connector J1, J2, and/or V_{DD} power input connector J6 are correct. Overvoltage or reverse-polarity power applied to these terminals can open on-board soldered-in fuses and cause other damage to the platform, installed evaluation modules, and/or the power source.

Inserting or Removing EVM Boards

Do not insert or remove EVM boards with power applied — damage to the EVM board, the platform, or both may result.

Figure 3–1. The Platform



3.2 Configuration

Configuring the TI Plug-N-Play Audio Amplifier Evaluation Platform consists of selecting the appropriate TI audio EVMs for the application to be modeled, installing the modules on the platform, routing the signal, and setting the mode and mute options of the amplifier.

3.2.1 TI Audio EVMs

There are a wide variety of TI audio EVMs available for the platform. Contact any TI sales office to obtain additional audio EVMs or for information on any new audio EVMs that may have been released.

The platform is equipped with six evaluation module sockets (Figure 3–1):

- U1 Signal conditioning EVM socket
- U2 Stereo audio power amplifier EVM socket
- U3 Mono audio power amplifier EVM socket
- U4 Mono audio power amplifier EVM socket
- U5 Headphone audio power amplifier EVM socket
- U6 DC/DC converter/voltage regulator EVM socket

Various modules can be installed in combination, with the minimal configuration being simply a power output amplifier and a 9-V battery. Or, the platform can be populated with a full complement of modules. If a power output amplifier is to be installed, however, a choice must be made between either a stereo power output amplifier in socket U2, or one or two monaural power amplifier modules in sockets U3 and/or U4. A stereo headphone power amplifier can be installed in socket U5 whether any other power amplifiers are installed or not.

3.2.2 Installing and Removing EVM Boards

TI Plug-N-Play evaluation modules use single-in-line header pins installed on the underside of the module circuit board to plug into sockets on the platform. The EVM pins and the platform sockets are keyed such that only the correct type of EVM can be installed in a particular socket, and then only with the proper orientation.

Evaluation modules are easily removed from the platform by simply prying them up and lifting them out of their sockets. Care must be taken, however, to prevent bending the pins.

3.2.2.1 EVM Insertion

1) Remove all power from the evaluation platform
2) Locate the appropriate socket on the platform
3) Orient the module correctly

4) Carefully align the pins of the module with the socket pin receptacles

5) Gently press the module into place

6) Check to be sure that all pins are seated properly and that none are bent over

3.2.2.2 EVM Removal

1) Remove all power from the evaluation platform

2) Using an appropriate tool as a lever, gently pry up one side of the module a small amount

3) Change to the opposite side of the module and use the tool to pry that side up a small amount

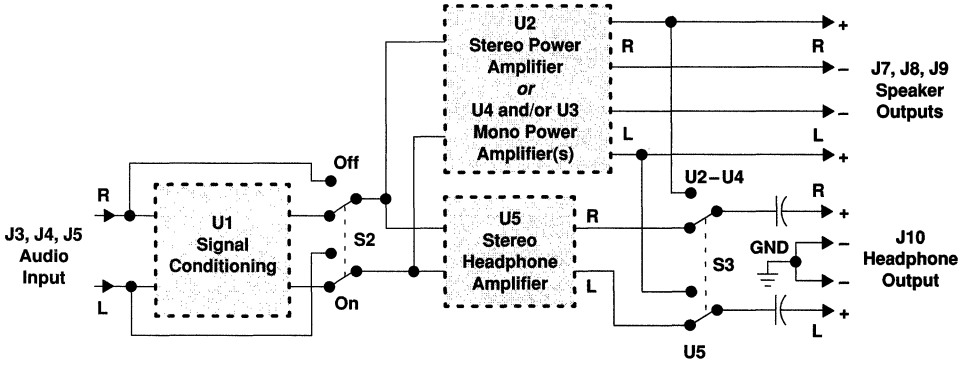
4) Alternate between sides, prying the module up a little more each time to avoid bending the pins, until it comes loose from the socket

5) Lift the EVM off of the platform

3.2.3 Signal Routing

The audio signal from the input jacks can be applied to the signal conditioning socket (U1) if a signal conditioning EVM is installed, or socket U1 can be bypassed and the audio input signal applied directly to the inputs of the installed power amplifiers. Switch S2 selects signal conditioning or bypasses it (Figure 3–2).

Figure 3–2. Signal Routing Switches



Switch S3 is the source select for the stereo headphone output jack, J10. The headphone jack is capacitively coupled and can output either the signal from the headphone amplifier in socket U5, or the output signal from the power amplifier(s) installed in socket U2 or U3 and/or U4, as determined by the setting of S3.

3.2.4 Muting and Mode

Many TI audio power amplifier EVMs have control inputs that mute the output and/or change the operating mode (from bridged to single-ended output, for example) in response to a signal applied to a control input. The typical application, as often found in notebook computers, portable audio products, and such, would have the internal speakers mute when headphones are plugged into the headphone jack, or have internal speakers mute when external speakers are connected.

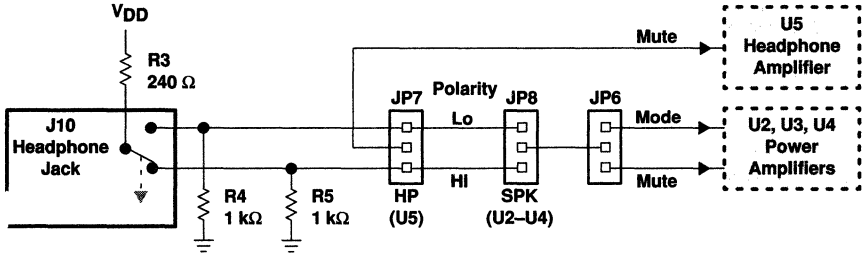
In applications using separate speaker and headphone amplifiers, the one not being used can be shut down (muted) to conserve power. In applications that use a single power amplifier to run either the speakers or the headphones, or either the internal speakers or the external speakers, often the amplifier must switch its output mode to single-ended to be able to cope with the 3-wire headphone or external speaker connector that returns the signal to ground.

The TI Plug-N-Play Audio Amplifier Evaluation Platform has been designed to provide complete flexibility in selecting control signal polarity and functionality for amplifier muting and mode select.

3.2.4.1 Headphone Jack Control Signals

The platform headphone jack (J10) contains an internal switch that changes the state of a pair of control lines when a headphone plug is inserted. Each control line is pulled down by a 1-kΩ resistor to ground (R4 and R5). The switch in the headphone jack pulls one line or the other up to V_{DD} through a 240 Ω resistor (R3) depending on whether a headphone plug is inserted in J10 or not (Figure 3–3).

Figure 3–3. Mute/Mode Control



A 3-pin jumper header (JP7), functioning as a SPDT switch, selects the control signal polarity by connecting either the active-low or the active-high line from the headphone jack to the mute control input of the headphone amplifier socket, U5.

For the power amplifiers, sockets U2 – U4, a second three-pin jumper header (JP8) selects the control signal polarity by connecting either the active-low or the active-high line from the headphone jack to jumper JP6. JP6 connects the control signal from the headphone jack to either the mute or the mode control input of the power amplifier sockets.

3.2.4.2 Muting Polarity Select for Headphone Amplifier in U5 (JP7)

Jumper JP7 as indicated in the User's Guide for the amplifier installed in U5, or:

- ❑ To mute EVMs that are being used as headphone amplifiers in U5 when the plug is *removed* from the headphone jack, jumper JP7 as follows:
  - If the EVM mutes on a low control signal, jumper **JP7** to ***Hi***
  - If the EVM mutes on a high control signal, jumper **JP7** to ***Lo***

3.2.4.3 Mute/Mode Select for Power Amplifiers in U3/U4 or U2 (JP6)

Jumper JP6 as indicated in the User's Guide for the power amplifiers installed in U2 or in U3/U4, or:

- ❑ To change the mode (from BTL to SE, for example) of the power amplifiers installed in U3/U4 or U2 when a plug is *inserted* in the headphone jack, jumper **JP6** to ***Mode***
- ❑ To mute the power amplifiers installed in U3/U4 or U2 when a plug is *inserted* in the headphone jack, jumper **JP6** to ***Mute***

3.2.4.4 Mute/Mode Polarity Select for Power Amplifiers in U3/U4 or U2 (JP8)

Jumper JP8 as indicated in the User's Guide for the power amplifiers installed in U2 or in U3/U4, or:

- ❑ To mute or change the mode of the power amplifiers installed in U3/U4 or U2 when a plug is *inserted* in the headphone jack, jumper JP8 as follows:
  - If the power amplifiers mute or change to the desired mode on a low control signal, jumper **JP8** to ***Lo***
  - If the power amplifiers mute or change to the desired mode on a high control signal, jumper **JP8** to ***Hi***

3.2.4.5 Mute/Mode Jumper Select Table

Table 3–1 shows the relationship between the control line polarity select jumpers (JP7 and JP8), the Mute/Mode select jumper (JP6), and the headphone plug for amplifier EVMs with *active-high* control inputs.

Table 4–1. Mute/Mode/Polarity Jumper Select Table

POWER AMPLIFIERS			HEADPHONE PLUG	HEADPHONE AMPLIFIER	
JP6	JP8	U2–U4		U5	JP7
Mute	Lo	Active	Present	Active	Lo
		Mute	Not present	Mute	
	Hi	Mute	Present	Mute	Hi
		Active	Not present	Active	
Mode	Lo	Mode A	Present		
		Mode B	Not present		
	Hi	Mode B	Present		
		Mode A	Not present		

3.3 Power

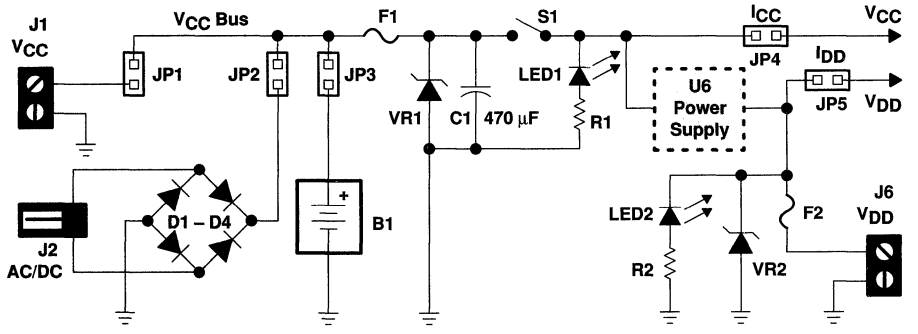
TI audio modules installed in the TI Plug-N-Play Audio Amplifier Evaluation Platform operate from either an unregulated V_{CC} supply or a regulated V_{DD} supply. The platform can be powered from an on-board battery or from any of several different external sources.

3.3.1 Platform Power Distribution

The platform is equipped with a number of connectors for power input, and a V_{CC} bus and a V_{DD} line for on-board power distribution. The V_{CC} bus uses jumper block JP1 ***OR*** JP2 ***OR*** JP3 to connect it to the desired power input connector. Only ***ONE*** of these jumpers should be installed at any one time.

On-board switch S1 applies V_{CC} power to the modules installed on the platform. Note that S1 also controls V_{DD} power only when V_{DD} is supplied by a power supply/voltage regulator module plugged into platform socket U6, and not when V_{DD} power is supplied from an external source at screw terminals J6. LED1 and LED2 indicate the presence of power on the V_{CC} bus and the V_{DD} line, respectively (Figure 3–4).

Figure 3–4. Platform Power Distribution



Jumper JP4 is in series with the V_{CC} bus and allows easy monitoring of module V_{CC} current consumption (I_{CC}). JP5 is in series with the V_{DD} line for I_{DD} measurement. Both current monitoring points are on the load side of the indicator LEDs, so their current consumption will not be part of the measurement.

3.3.2 Platform Power Protection

The platform V_{CC} bus and the V_{DD} line are protected against both excessive voltage levels and reverse power polarity by zener diodes and fuses connected to form crowbar circuits.

A zener diode is connected backwards between the V_{CC} bus and ground so that it is reverse-biased. If the input voltage exceeds the zener breakover voltage, the diode suddenly conducts heavily, forming a low-impedance path to ground. The resulting high current opens the fuse, removing the voltage.

If a reverse-polarity voltage is input, the zener, being forward biased, conducts immediately, and again the fuse opens. A similar circuit protects the V_{DD} line.

Note that the V_{CC} bus protection components are ahead of the platform power switch. And since there is no power switch for the V_{DD} line, both protection circuits will respond to reverse power polarity and overvoltage conditions at the moment they are applied to the platform power input connectors. Power polarity and voltage levels must be set and verified before external power is applied to the platform.

Correct polarity and maximum voltage levels should always be strictly observed because not only is the operation of the crowbar circuit always destructive to some degree (at a minimum, the opened fuse must be unsoldered and replaced), there is always the chance for damage to the platform, the installed modules, and/or the external power source before the fuse opens.

Damage to the protection circuit and/or the platform (beyond an open fuse) can occur if the external power supply is unable to provide at least 3 amps of current to ensure the fuse opens quickly. Lower currents can cause failure of the zener diode and possibly damage to the platform PCB traces from overheating.

3.3.3 Platform Power Inputs

The evaluation modules installed on the platform can be powered by a wide variety of V_{CC} sources including:

- ❑ On-board 9-V battery
- ❑ Unregulated external DC at screw terminals J1
- ❑ Unregulated external AC or DC at coaxial power connector J2

And for those TI audio EVMs that require a regulated V_{DD} supply:

- ❑ Regulated DC from on-board power supply/regulator (socket U6)
- ❑ Regulated external DC at screw terminals J6

Selecting the appropriate power source may depend on the requirements of the various modules in the audio system assembled on the platform, or simply on what is available (as long as platform and EVM requirements are met).

3.3.3.1 Power Requirements

Platform V_{CC} voltage limits are governed by the lowest level that will operate all of the installed modules and the highest level that the modules (or the platform overvoltage protection circuit) will tolerate. In general, however, the V_{CC} input voltage should be in the range of:

- Approximately 3.3 V to a maximum of 15 V
- Approximately 5.5 V to a maximum of 12 V if a SLVP097 power supply/voltage regulator module is installed in U6

Some TI audio EVMs require a regulated V_{DD} supply (3.3 V or 5 V typical) for operation. This can be provided by a power supply/voltage regulator EVM installed in platform socket U6 (runs off of the platform V_{CC} bus) or by an external regulated supply. If an external V_{DD} source is used, depending on the EVM requirements, V_{DD} should be:

- 3.3 V or 5 V, and must not exceed 6 V

3.3.3.2 On-Board 9-V Battery

Many low-power portable and battery-powered audio systems can be modeled on the platform with TI audio EVMs. It may make sense, then, to power these system models on the platform using an on-board battery. The platform is equipped with a snap-in battery holder for a common 9-V battery and jumper JP3 connects the battery to the V_{CC} bus, which routes the battery voltage to the various EVM sockets.

Since the V_{CC} bus also supplies the on-board power supply/voltage regulator socket, the battery voltage can be input voltage for a power supply/regulator EVM plugged into U6. The regulator EVM then supplies regulated voltage to the V_{DD} line for use by those EVMs that require regulated V_{DD} power.

For high-power audio system evaluation and demonstration, one of the other platform power supply options should be selected.

3.3.3.3 Unregulated External DC at Screw Terminals J1

Unregulated DC voltage from a bench-type supply or any other source of DC power within the required voltage range can be connected to screw terminals J1 for V_{CC} power. Jumper JP1 connects J1 to the V_{CC} bus for distribution.

Voltage applied to screw terminals J1 *MUST* be of the correct polarity and *MUST NOT* exceed 15 V or the power protection circuit on the V_{CC} bus will trip.

3.3.3.4 Unregulated External AC or DC at Coaxial Power Connector J2

The coaxial power jack, J2, matches a large number of the typical wall-cube-type power transformers/power supplies. Although the jack is of a standard size (5.5 mm O.D. × 2.1 mm I.D.), there does not seem to be any standard for voltage polarity or power type (AC or DC) among wall-cubes and other power sources using a coaxial power plug. To ensure the widest possibility compatibility, the platform is equipped with a full-wave bridge rectifier between the coaxial connector and the V_{CC} bus to allow DC voltage of either polarity, or AC voltage to be input through J2. Jumper JP2 connects J2 to the V_{CC} bus for distribution.

The bridge rectifier eliminates the need to determine the plug polarity for input voltage at J2 and rectifies AC voltage applied to J2 into DC before it is connected to the V_{CC} bus. An on-board filter capacitor on the bus smooths the rectified AC.

With DC voltage applied to J2, the bridge rectifier introduces a voltage drop of approximately 1.4 V (two diode forward-drops). This drop must be taken into account if the DC voltage applied to J2 is at or near the minimum required for operating a module installed on the platform, and the external voltage supply adjusted accordingly.

With an AC voltage applied to J2, V_{CC} bus voltage depends on several factors, including the load on the bus. As a general rule for typical AC voltage inputs, however, V_{CC} bus voltage will be approximately the peak value of the applied AC voltage.

The bridge rectifier also causes the platform ground bus to be approximately 0.7 V above the ground of other equipment that might be operated by the same external power supply. Platform V_{CC} and EVM voltage measurements should be referenced to the platform ground bus (test point TP1, for example) and not the external power supply ground when V_{CC} voltage is supplied from J2.

V_{CC} voltage *MUST NOT* exceed 15 V or the overvoltage protection circuit on the V_{CC} bus will trip.

3.3.3.5 Regulated DC From On-Board Regulator (Socket U6)

A power supply/voltage regulator EVM can be installed in platform socket U6 to provide a a regulated V_{DD} voltage (3.3 V or 5 V typical) for audio evaluation modules installed on the platform that require it. The regulator EVM uses power from the V_{CC} bus as an input and provides the appropriate regulated voltage to the platform V_{DD} line.

V_{DD} voltage also appears at screw terminals J6, where it can be used as a source of regulated power for off-board use, subject to the maximum current capabilities of the regulator module installed in U6 and the platform V_{CC} supply.

Do not allow the V_{CC} voltage to exceed the maximum specified for the installed power supply/voltage regulator EVM.

3.3.3.6 Regulated External DC at Screw Terminals J6

Regulated voltage (3.3 V or 5 V typical — 6 V maximum) from an external source can be connected to screw terminals J6 to supply the platform V_{DD} line for audio evaluation modules installed on the platform that require a regulated V_{DD} supply.

Voltage applied to screw terminals J6 *MUST* be of the correct polarity and *MUST NOT* exceed 6.1 V or the power protection circuit on the V_{DD} line will trip.

3.4 Inputs and Outputs

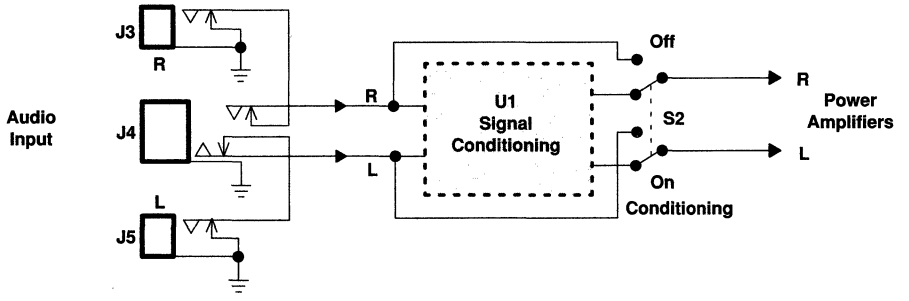
TI Plug-N-Play Audio Amplifier Evaluation Platform is equipped with several standard conectors for audio inputs and outputs.

3.4.1 Inputs

In most cases, audio signals enter the platform through either a pair of RCA phono jacks (J3 and J5) or a miniature (1/8") stereo phone jack (J4). Certain EVMs, however, may have additional signal input connectors mounted on the module circuit board.

The platform audio signal input jacks (J3, J4, and J5) are of the closed-circuit type and are interconnected such that the stereo phone jack is in series with the RCA phono jacks, and the signal lines are grounded when no plugs are inserted (Figure 3–5).

Figure 3–5. Platform Audio Input Jacks



The internal switches in the RCA phono jacks (J3 and J5) connect the signal lines to ground when a plug is not inserted. The internal switches in the stereo phone jack (J4) connect the module signal inputs to the RCA phono jacks when a plug is not inserted in the stereo phone jack. These connectors operate as follows:

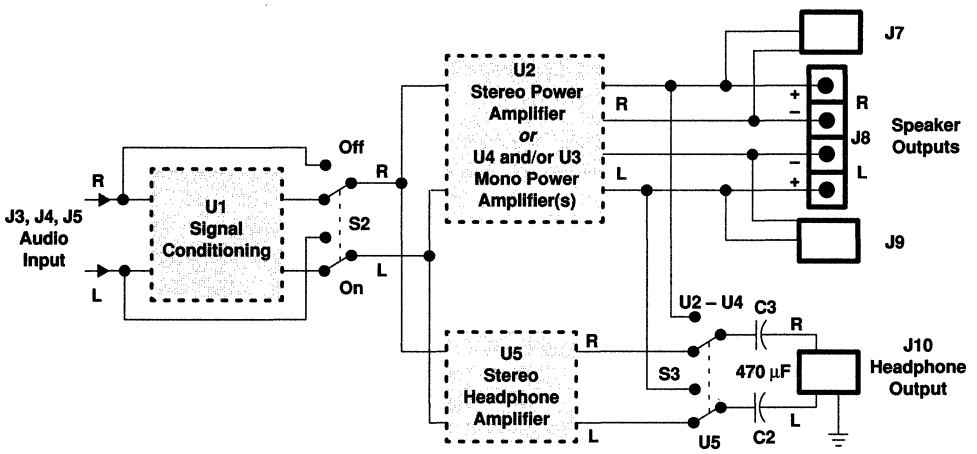
- With no plugs inserted, the signal lines to the inputs of the signal conditioning socket, U1*, are shorted to ground.
- With plugs inserted into the RCA phono jacks (J3 and J5) only, the signal from the phono plugs is routed through the stereo phono jack internal switches and then on to socket U1*.
- With a plug inserted into the stereo phone jack (J4), the RCA phono jacks are disconnected from the input and the signal from the phone plug is applied to socket U1*.

* or to power amplifier sockets if S2 is set to ***OFF*** to bypass conditioning

3.4.2 Outputs

Amplified audio signals leave the platform through left and right RCA phono jacks (J7 and J9), left and right pairs of compression connectors for stripped speaker wires (J8), and a capacitively-coupled miniature (1/8") stereo phone jack (J10) for headphones (Figure 3–6).

Figure 3–6. Platform Audio Output Jacks and Connectors



3.4.2.1 *Power Amplifier Outputs/Jacks*

The audio output lines from the power amplifiers are separate all the way to the edge of the platform (output jacks J7, J8, and J9) — the Out – lines from the power amplifier sockets are not tied to each other or to platform ground. This allows certain power amplifier EVMs to operate in various output drive modes, including some highly-efficient bridged configurations. To reduce possible emissions, limit the length of speaker wiring to 1 meter or less.

3.4.2.2 *Headphone Amplifier Output/Jack*

The headphone jack (J10) is a stereo miniature phone jack that is capacitively coupled (via 470 µF electrolytics) to S3. Source select switch S3 connects the headphone jack to the output lines of either the headphone amplifier socket U5, or to the output lines of the power amplifier sockets (U2, U3, and U4).

Some of the TI power amplifier EVMs that can be installed in sockets U2, U3, or U4 normally operate in the single-ended output mode, and some have the ability to switch from a bridged output mode to single-ended in response to a mode control signal. S3 should not be set to the power amplifier position unless power amplifiers that can operate in the single-ended mode are installed.

When S3 is set to the power amplifier position (***U2 – U4***), the headphone jack is connected to the power amplifier Out + output lines. When a headphone plug is inserted into the jack, these output lines are returned to the common platform ground inside J10, requiring single-ended power amplifier outputs. For power amplifier modules that have selectable output modes, a switch inside the headphone jack sends a control signal to the power amplifier sockets that can select the single-ended output mode when a headphone plug is inserted.

3.5 Troubleshooting

This section covers some of the possible difficulties that might be encountered with platform operation.

- ❑ The platform is connected to an external power source for V_{CC} and a voltage regulator EVM is installed in U6. Neither LED is lit and the EVM modules are not receiving power.
  - Check that platform power switch S1 is set on ***ON***
  - Check that JP1 or JP2 or JP3 is jumpered and corresponds to the power source
  - Check fuse F1; replace it if it is found to be open
  - Check platform power switch S1; replace it if it is found to be faulty
- ❑ The platform is connected to an external power source for V_{CC} and a voltage regulator EVM is installed in U6. Only LED1 (V_{CC}) is lit. There is no V_{DD} at JP5 and the installed EVMs do not function properly.
  - Check that the voltage regulator EVM is fully seated in socket U6 and that none of the pins are bent over
  - Substitute a known-good voltage regulator EVM for the module in U6
- ❑ The platform is connected to an external power source for V_{DD} at J6. LED2 (V_{DD}) is dark and V_{DD} is not reaching the EVMs.
  - Check for correct V_{DD} input supply voltage
  - Check fuse F2; replace it if it is found to be open
- ❑ Power amplifier EVMs installed in U2, U3, and/or U4 are powered correctly but produce no sound.
  - Consult the User's Guide for the installed power amplifier and determine 1) if the EVM is mute active-high or mute active-low, and 2) which pin on the module is the mute control input. Measure the voltage at the mute control input pin of the installed module with *no* plug inserted in headphone jack J10. If the EVM is mute active-high and the mute pin of the EVM measures V_{DD}, the EVM is being held in the mute mode. Jumper the *other* pin on JP8 to reverse the mute control line polarity.
- ❑ The power amplifier EVM installed in U5 is powered correctly, but there is no sound from headphones when plugged into headphone jack J10.
  - Check that the headphone jack source select switch (S3) is set to the ***U5*** position
  - Consult the User's Guide for the installed power amplifier and determine 1) if the EVM is mute active-high or mute active-low, and 2) which pin on the module is the mute control input. Measure the voltage at the mute control input pin of the installed module *with* the headphone plug inserted in jack J10. If the EVM is mute active-high and the mute pin of the EVM measures V_{DD}, the EVM is being held in the mute mode. Jumper the *other* pin on JP7 to reverse the mute control line polarity.

3.6 Parts List

Table 4–2. Plug-N-Play Audio Amplifier Evaluation Platform Parts List

Ref	Description	Source	Part No.
B1	Battery, 9-V		
C1	Capacitor, Aluminum, 470 µF, 25 V	Digi-Key	P5704-ND
C2	Capacitor, Aluminum, 470 µF, 16 V	Digi-Key	P6230-ND
C3	Capacitor, Aluminum, 470 µF, 16 V	Digi-Key	P6230-ND
D1	Diode, Rectifier, 3 A, 50 V	Mouser	583-1N5400
D2	Diode, Rectifier, 3 A, 50 V	Mouser	583-1N5400
D3	Diode, Rectifier, 3 A, 50 V	Mouser	583-1N5400
D4	Diode, Rectifier, 3 A, 50 V	Mouser	583-1N5400
F1	Fuse, Pico II, 3 A, 125 V, Fast-acting	Littelfuse	251-003
F2	Fuse, Pico II, 3 A, 125 V, Fast-acting	Littelfuse	251-003
J1	Connector, 2-pin, screw connector, 0.2″ centers	Mouser	506-2MV02
J2	Jack, Power, 2.1 mm, PC mount	Mouser	163-5004
J3	Phone Jack, switched, PC mount	Mouser	16PJ396
J4	Phone Jack, Stero, 1/8″	Mouser	161-3504
J5	Phone Jack, switched, PC mount	Mouser	16PJ396
J6	Connector, 2-pin, screw connector, 0.2″ centers	Mouser	506-2MV02
J7	Phone Jack, switched, PC mount	Mouser	16PJ396
J8	Connector, 4-pin	Radio Shack	274-622A
J9	Phone Jack, switched, PC mount	Mouser	16PJ396
J10	Phone Jack, 1/8″ with SPDT switch	Mouser	161-3503
JP1 – JP8	Header, 2-pin, 100-mil centers, 0.23″ top, 0.22″ bottom	Digi-Key	S1022–36–ND
LED1	LED, T1-3/4, Org, 25-mA		
LED2	LED, T1-3/4, Red, 25-mA		
R1	Resistor, CF, 430 Ohm, 1/2 W, 5%		
R2	Resistor, CF, 150 Ohm, 1/4 W, 5%		
R3	Resistor, CF, 240 Ohm, 1/4 W, 5%		
R4	Resistor, CF, 1.0 K Ohm, 1/4 W, 5%		
R5	Resistor, CF, 1.0 K Ohm, 1/4 W, 5%		
S1	Switch, DPDT, 0.2-A, 30-V, pc mount	Digi-Key	EG1908-ND
S2	Switch, DPDT, 0.2-A, 30-V, pc mount	Digi-Key	EG1907-ND
S3	Switch, DPDT, 0.2-A, 30-V, pc mount	Digi-Key	EG1907-ND
VR1	Diode, Zener, 15 V, 1 W, 5%, DO-41	Diodes, Inc.	1N4744A
VR2	Diode, Zener, 6.2 V, 1 W, 5%, DO-41	Diodes, Inc.	1N4735A
XB1	Battery Holder, 9-V, pc mount	Keystone	1294K
PCB	Printed Circuit Board, 2-layer		SLOP097
	Socket Pins, 0.022″–0.032″ (Qty: 106) Mil-Max #0295–0–	Digi-Key	ED5008-ND
	Standoff, Nylon, 0.375″/6–32 (Qty: 6)	Digi-Key	8441BK-ND
	Screw, 0.25″/6–32 (Qty: 6)	Digi-Key	
	SHUNT, black, closed top (Qty: 3)	Mouser	151-8010
	SHUNT, red, open top (Qty: 3)	Mouser	151-8003

3.7 Platform EVM Socket Pinouts

Figure 3–7. Signal Conditioning Socket U1 Pinout

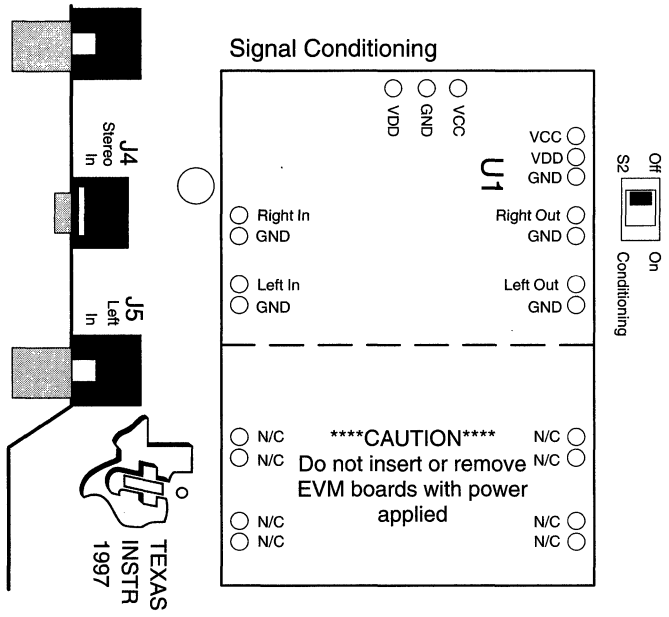


Figure 3–8. Power Amplfier Socket U2 Pinout

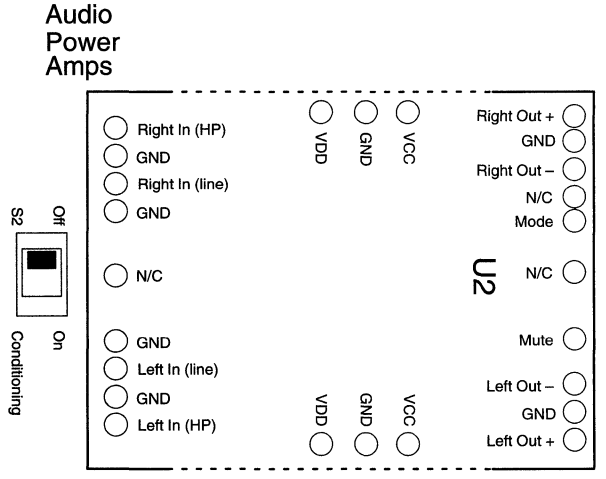


Figure 3–9. Power Amplfier Socket U3/U4 Pinout

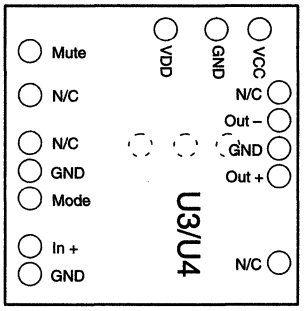


Figure 3–10. Headphone Amplfier Socket U5 Pinout

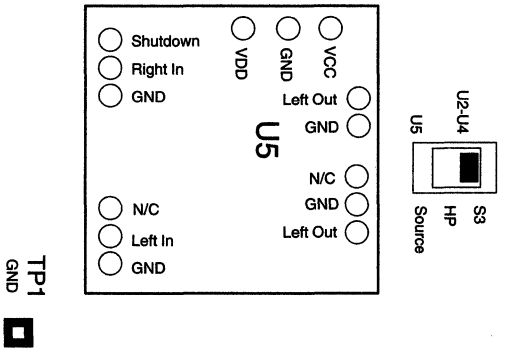
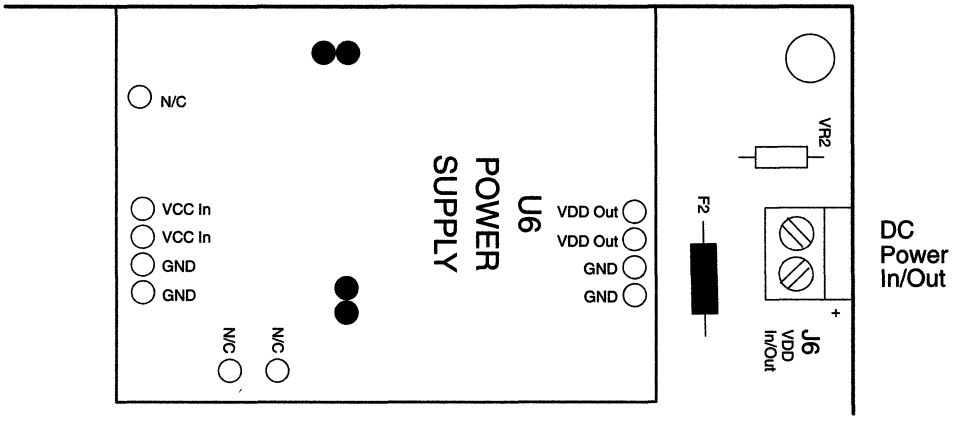


Figure 3–11. Power Supply/Regulator Socket U6 Pinout



SLVP097 Buck Converter Evaluation Module User's Guide

Literature Number: SLVU002A
July 1998

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Preface

Read This First

About This Manual

This user's guide is a reference manual for the SLVP097 Buck Converter Evaluation Module. This document provides information to assist managers and hardware engineers in application development.

How to Use This Manual

This manual provides the information and instructions necessary to design, construct, operate, and understand the SLVP097. Chapter 1 describes and lists the hardware requirements; Chapter 2 describes design considerations and procedures.

Related Documentation From Texas Instruments

The following books describe the TL5001 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TL5001 Pulse-Width-Modulation Control Circuits Data Sheet (Literature number SLVS084C).

Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

TPS2816, TPS2817, TPS2818, and TPS2819 Single-Channel High-Speed MOSFET Driver Data Sheet (Literature number SLVS160)

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Contents

Figures

Chapter 1

Hardware

The SLVP097 Buck Converter Evaluation Module (SLVP097) provides a method for evaluating the performance of a buck converter using the TL5001 pulse-width-modulation (PWM) controller coupled with a TPS2817 MOSFET driver. This manual explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

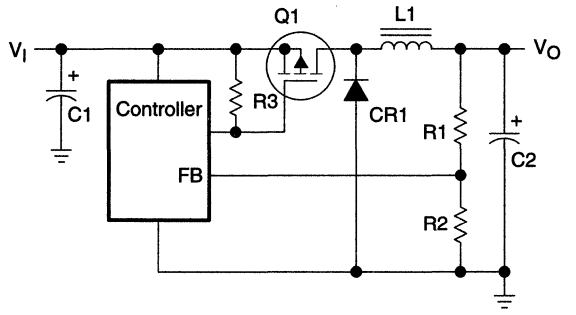
Topic **Page**

1.1 Introduction

Low cost and design simplicity make buck converters popular solutions in dc/dc step-down applications where lack of isolation from the input source is not a concern. Loop compensation for the buck converter can be set for high bandwidths. This mode is desirable for the low peak-to-average current ratio, easing the component worst-case design parameters.

Figure 1–1 shows a block diagram of a typical buck converter. The converter passes a duty-cycle modulated waveform through a low-pass output filter. To maintain the desired output voltage, a controller senses the output voltage, compares it to an internal reference voltage and adjusts the width of the power switch (Q1) on time, . A commutating diode (CR1) maintains continuous current through the inductor when the power switch is turned off.

Figure 1–1. Typical Buck Converter Block Diagram



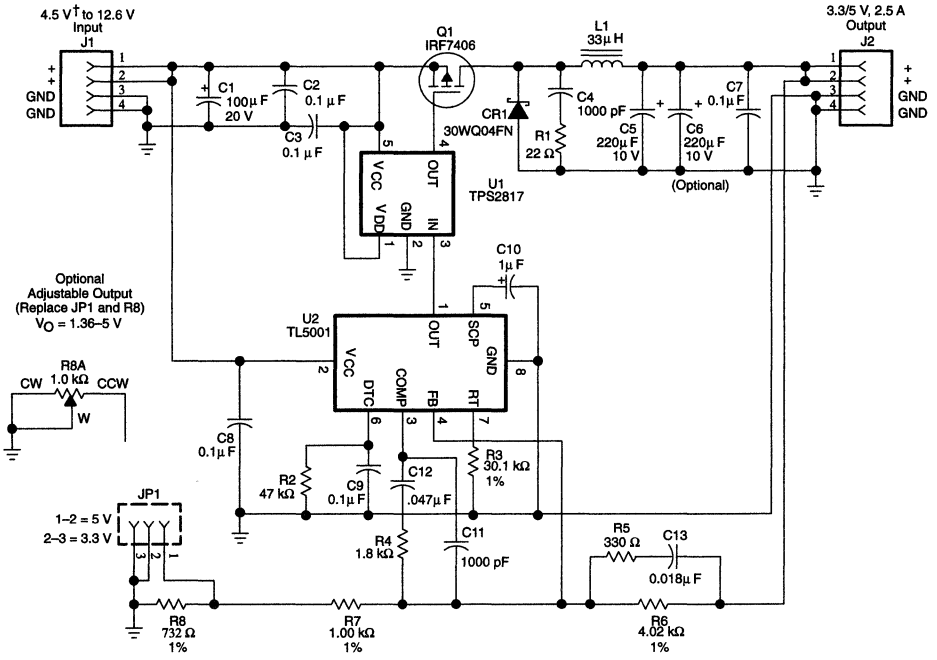
The SLVP097 buck converter uses the TI TL5001 PWM controller and the TPS2817 MOSFET driver to give a 0- to 2.5-A output with a selectable output voltage of either 3.3 V or 5 V. The converter operates over an input voltage range of 5.5 V to 12 V with a typical efficiency of 90 percent. Chapter 2 lists full design specifications.

Note: Peak currents in excess of 2.5 A may be obtained from this EVM, but due to thermal restraints, should not be subtained. This EVM shuts down when a short circuit is encountered. Input power must be recycled to restart the module.

1.2 Schematic

Figure 1–2 shows the SLVP097 schematic.

Figure 1–2. SLVP097 Schematic



† Input voltage range for 3.3 V output. When using 5-V output, minimum input voltage must be greater than 5.5 V.

Notes: 1) Frequency set to 275 kHz by R3.

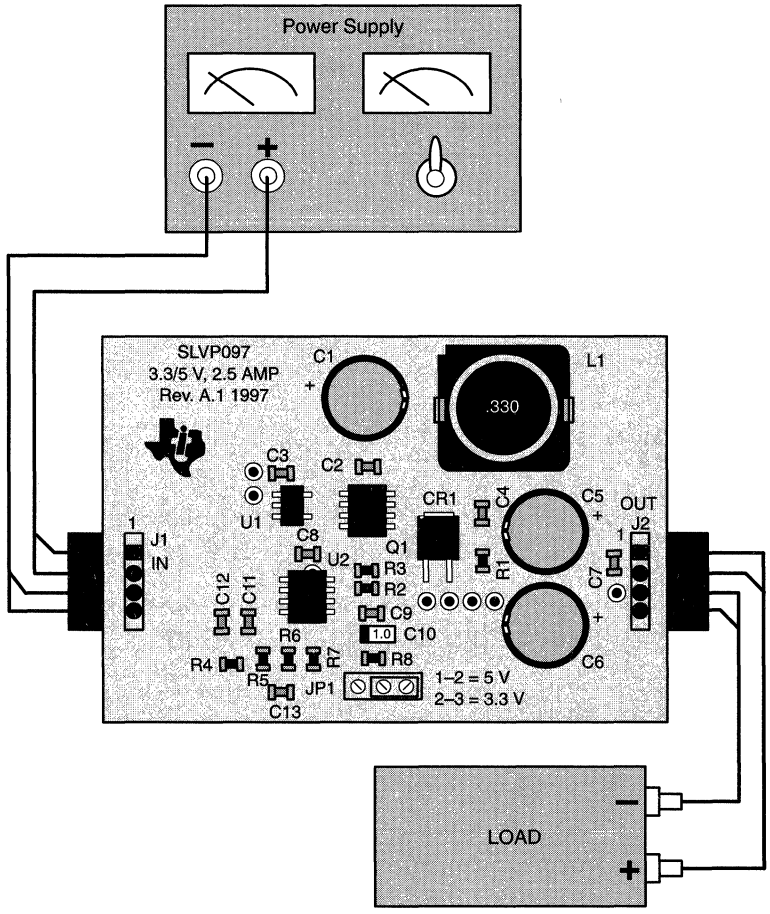
2) This unit and the components are thermally rated to 2.5 A. The output current should not exceed 2.5 A unless proper thermal management is put in place.

3) DO NOT change the set output voltage jumper (JP1) while power is applied to the unit.

1.3 Input/Output Connections

Figure 1–3 shows the SLVP097 input and output connections.

Figure 1–3. I/O Connections



Notes: 1) The input power supply should be rated at least 3 A with current limit set high enough for proper operation.
2) The load should be rated at least 2.5 A with proper power dissipation. Fixed or variable resistors may be used.

1.4 Board Layout

Figures 1–4 through 1–6 show the SLVP097 board layout.

Figure 1–4. Board Layout

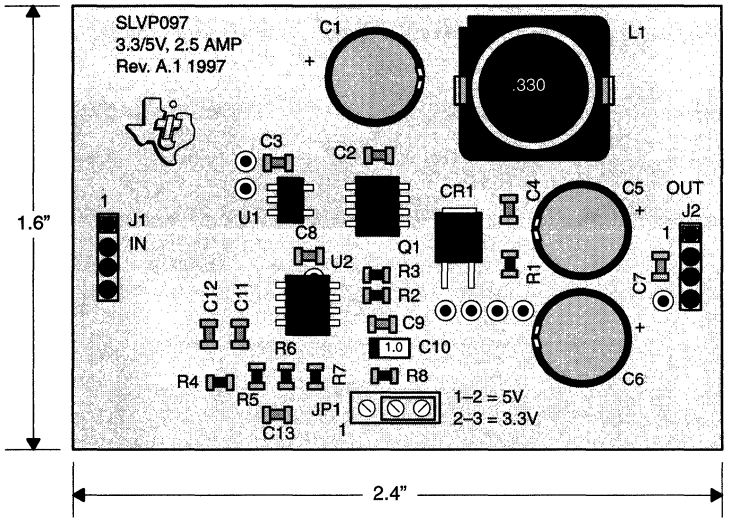


Figure 1–5. Top Layer

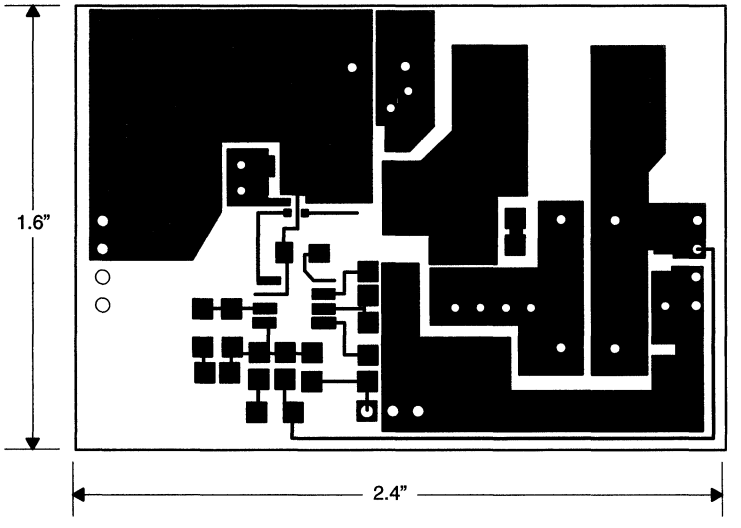
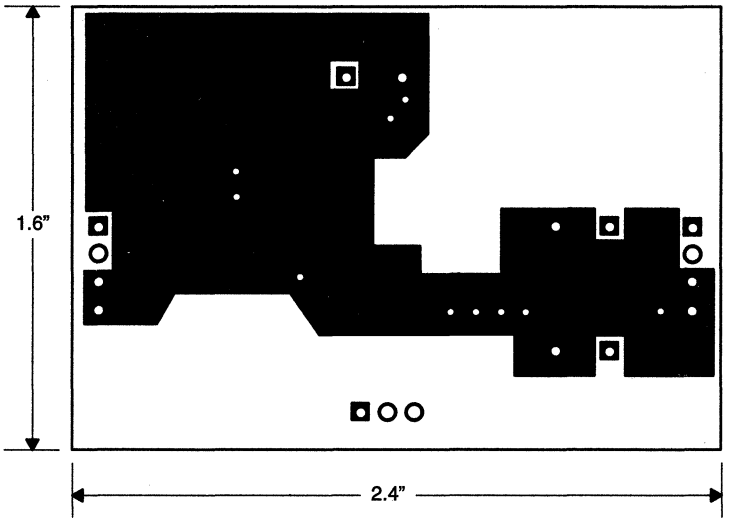


Figure 1–6. Bottom Layer



1.5 Bill of Material

Table 1–1 lists materials required for the SLVP097.

Table 1–1. Bill of Materials

Reference	Part Number	Mfr	Description
C1	20SA100M	Sanyo	Capacitor, Os-Con, 100 μF, 20 V, F-case
C2			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C3			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C4			Capacitor, Ceramic, 1000 pF, 50 V, 1206
C5	10SA220M	Sanyo	Capacitor, Os-Con, 220 μF, 10 V, F-case
C6*	10SA220M	Sanyo	Capacitor, Os-Con, 220 μF, 10 V, F-case
C7			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C8			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C9			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C10	ECS-T1EY105R	Digikey	Capacitor, Tantalum, 1.0 μF, 25 V, 1206
C11			Capacitor, Ceramic, 1000 pF, 50 V, 1206
C12			Capacitor, Ceramic, 0.047 μF, 50 V, 1206
C13			Capacitor, Ceramic, 0.018 μF, 50 V, 1206
CR1	30WQ04FN	IR	Diode, Schottky, 3.3 A, 40 V, D-Pak
J1			Header, 4-pin, 0.025" sq × 0.100" centers
J2			Header, 4-pin, 0.025" sq × 0.100" centers
JP1			Header, 3-pin, 0.025" sq × 0.100" centers
L1	SLF12565-330M2R8	TDK	Inductor, 33 μH, 2.8 A, 0.041 Ω, 0.50" square
Q1	IRF7406		MOSFET, P-Ch, 30 V, 0.045 Ω, 4.7 A, SO-8
R1			Resistor, CF, 22 Ω, 1/10 W, 5%, 1206
R2			Resistor, CF, 47 kΩ, 1/10 W, 5%, 0805
R3			Resistor, MF, 30.1 kΩ, 1/10 W, 1%, 0805
R4			Resistor, CF, 1.8 kΩ, 1/10 W, 5%, 0805
R5			Resistor, CF, 330 Ω, 1/10 W, 5%, 0805
R6			Resistor, MF, 4.02 kΩ, 1/10 W, 1%, 0805
R7			Resistor, MF, 1.00 kΩ, 1/10 W, 1%, 0805
R8			Resistor, MF, 732 Ω, 1/10 W, 1%, 0805
R8A*	CT9W102-ND	Digikey	Potentiometer, 1 kΩ, 10%, 18-turn, 9mm-square
U1	TPS2817DBV	TI	MOSFET driver, noninverting, single channel, SOT-25
U2	TL5001CD	TI	PWM controller, SO-8
—			Shunt, standard profile
—	SLVP097	TI	PCB, TPS2817 EVM, 2.40" × 1.60"

* Optional parts not on present board.

1.6 Test Results

Figures 1–7 through 1–11 show test results for the the SLVP097.

Figure 1–7. Output Voltage Vs Output Current (3.3-V Mode)

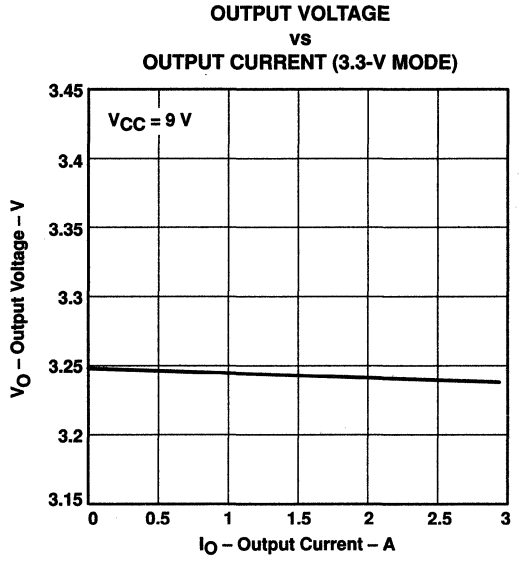


Figure 1–8. Output Voltage Vs Output Current (5-V Mode)

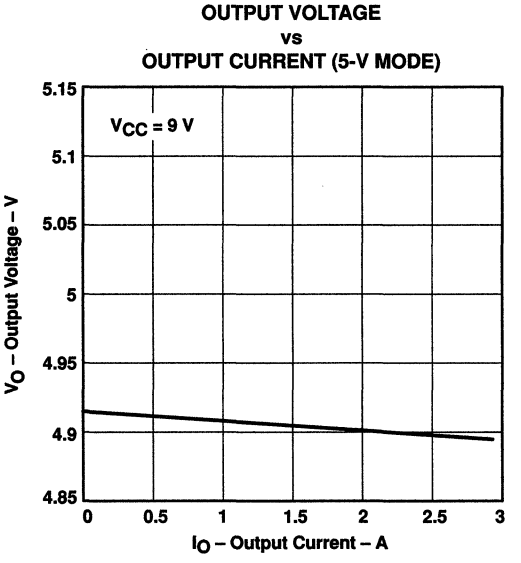


Figure 1–9. Output Voltage Vs Supply Voltage (3.3-V Mode)

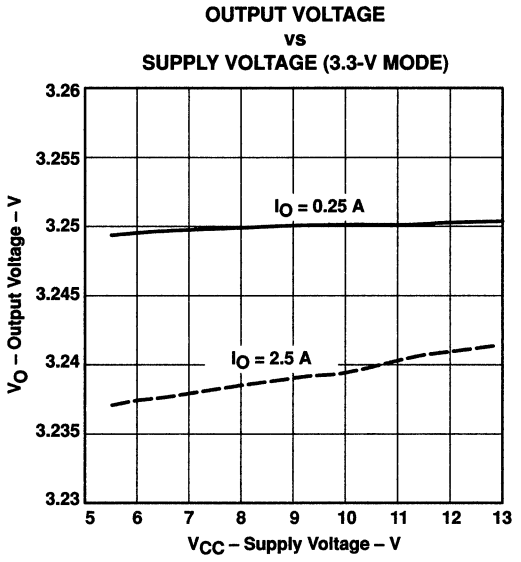


Figure 1–10. Output Voltage Vs Supply Voltage (5-V Mode)

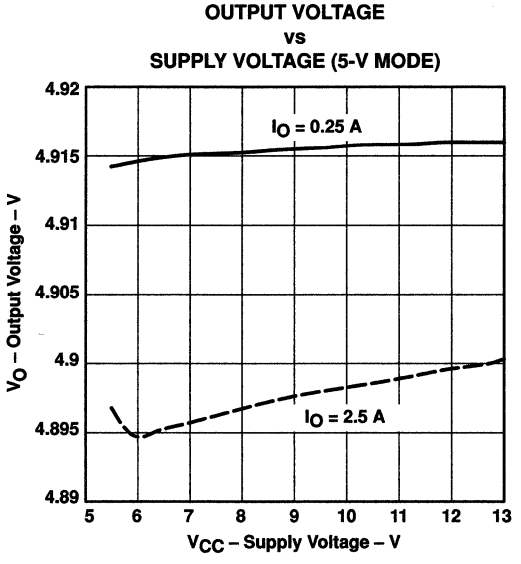
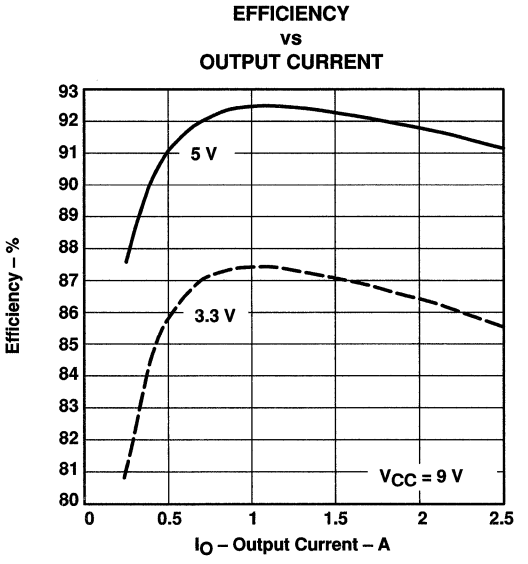


Figure 1–11. Efficiency Vs Output Current (5-V Mode)



Chapter 2

Design Procedure

The SLVP097 evaluation module provides a method for evaluating the performance of the TPS2817 MOSFET driver and the TL5001 PWM controller. The TPS2817 contains all of the circuitry necessary to drive large MOSFETs, including a voltage regulator for higher voltage applications. This section explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP097 is a dc-dc buck converter module that provides a 5-V or 3.3-V output at up to 2.5 A with an input voltage range of 5.5 V to 12 V. The controller is a TL5001 PWM operating at a nominal frequency of 275 kHz. The TL5001 is configured for a maximum duty cycle of 100 percent and has short-circuit protection built in. Output voltage selection is implemented with jumper JP1.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP097.

Table 2–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage Range	4.5†		12.6	V
Output Voltage Range				
5-V Mode	4.7	5.0	5.3	V
3.3-V Mode	3.1	3.3	3.5	V
Output Current Range	0		2.6	A
Operating Frequency		275		kHz
Output Ripple			50	mV
Efficiency	85%	90%		

† For 3.3 V only, minimum input voltage for 5 V output is 5.5 V.

2.3 Design Procedures

Detailed steps in the design of a buck-mode converter may be found in *Designing With the TL5001C PWM Controller* (literature number SLVA034) from Texas Instruments. This section shows the basic steps involved in this design, using the 3.3-V output mode.

2.3.1 Duty Cycle Estimate

The duty cycle for a continuous-mode step-down converter is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{SAT}}$$

Assuming the commutating diode forward voltage V_d = 0.5 V and the power switch on voltage V_{SAT} = 0.1 V, the duty cycle for V_i = 5.5, 9, and 12 V is 0.70, 0.42, and 0.32, respectively.

2.3.2 Output Filter

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 6 percent of the rated output load:

$$\Delta I_O = 2 \times 0.06 \times I_O = 2 \times 0.06 \times 2.5 = 0.30 \text{ A}$$

The inductor value is:

$$L = \frac{(V_I - V_{SAT} - V_O) \times D \times t}{\Delta I_O}$$

$$= \frac{(12 - 0.1 - 3.3) \times 0.32 \times \left(3.63 \times 10^{-6}\right)}{0.30} = 33.3 \ \mu\text{H}$$

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times \left(\Delta V_O\right)} = \frac{0.3}{8 \times \left(275 \times 10^3\right) \times 0.05} = 2.73 \ \mu\text{F}$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.3} = 0.167 \ \Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used a 220-µF OS-Con capacitor in parallel with a ceramic to reduce ESR.

2.3.3 Power Switch

Based on the preliminary estimate, $r_{DS(ON)}$ should be less than 0.10 V ÷ 2.5 A = 40 mΩ. The IRF7406 is a 30-V p-channel MOSFET with $r_{DS(ON)}$ = 40 mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_D = \left(I_O^2 \times r_{DS(ON)} \times D\right) + \left(0.5 \times V_i \times I_O \times t_{r+f} \times f\right)$$

Assuming total switching time, t_{r+f}, = 100 ns, a 55°C maximum ambient temperature, and $r_{DS(ON)}$ adjustment factor (for high temperature) = 1.6, then:

$$P_D = \left[2.5^2 \times (0.04 \times 1.6) \times 0.7\right] + \left[0.5 \times 5.5 \times 2.5 \times \left(0.1 \times 10^{-6}\right) \times \left(275 \times 10^3\right)\right] = 0.41 \text{ W}$$

The thermal impedance $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (90 \times 0.41) = 92°C$$

2.3.4 Rectifier

The catch rectifier conducts during the time interval when the MOSFET is off. The 30WQ04 is a 3.3-A, 40-V rectifier in a D-Pak power surface-mount package. The power dissipation is:

$$P_D = I_O \times V_D\left(1 - D_{Min}\right) = 2.5 \times 0.6 \times 0.68 = 1.02 \text{ W}$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and the rectifier connect. This is usually a trial-and-error sequence of steps to optimize the network; but as a starting point, select a snubber capacitor with a value that is 4–10 times larger than the estimated capacitance of the catch rectifier. The 30WQ04 has a capacitance of 110 pF, resulting in a snubber capacitor of 1000 pF. Then, measuring a ringing time constant of 20 ns, R is:

$$R = \frac{20 \times 10^{-9}}{C} = \frac{20 \times 10^{-9}}{1000 \times 10^{-12}} = 20\ \Omega$$

A 22-Ω resistor is used in the design.

2.3.6 Controller Functions

The controller functions, oscillator frequency, soft-start, dead-time control, short-circuit protection, and sense-divider network are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in Figure 6 of the TL5001 data sheet. For 275 kHz, a value of 30.1 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100% is chosen. Then *R* is calculated as:

$$R = \left(R_{OSC} + 1.25\ \text{k}\Omega\right)\left[D\left(V_{O(100\%)} - V_{O(0\%)}\right) + V_{O(0\%)}\right]$$
$$= (30.1\ \text{k}\Omega + 1.25\ \text{k}\Omega)[1(1.4 - 0.6) + 0.60] = 44\ \text{k}\Omega \Rightarrow 47\ \text{k}\Omega$$

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 5 ms is used:

$$C = \frac{t_R}{R_{DT}} = \frac{0.005\ s}{47\ k\Omega} = 0.1\ \mu F$$

The TL5001 has short circuit protection (SCP) instead of a current sense circuit. If not used, the SCP terminal must be connected to ground to allow the converter to start up. If a timing capacitor is connected to SCP, it should have a time constant that is greater than the soft-start time constant. This time constant is chosen to be 75 ms:

$$C(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.075\ s = 0.93\ \mu F$$

2.3.7 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load, line, and gain conditions. A buck-mode converter has a two-pole LC output filter with a 40-dB-per-decade rolloff. The total closed-loop response needed for stability is a 20-dB-per-decade rolloff with a minimum phase margin of 30 degrees over the full bandwidth for all conditions. In addition, sufficient bandwidth must be designed into the circuit to assure that the converter has good transient response. Both of these requirements are met by adding compensation components around the error amplifier to modify the total loop response.

The first step in design of the loop compensation network is the design of the output sense divider. This sets the output voltage and the top resistor determines the relative size of the rest of the compensation design. Since the TL5001 input bias current is 0.5 μA (worst case), the divider current should be at least 0.5 mA. Using a 1-kΩ resistor for the bottom of the divider gives a divider current of 1 mA. Since this is a dual-voltage output, the divider must be selectable. For a 5-V output, the divider was set for 1 kΩ and 4 kΩ. The bottom of the divider is calculated for the 3-V mode as:

$$R = \frac{R_T}{V_O - V_{REF}} = \frac{4\ k\Omega}{3.3 - 1} = 1.74\ k\Omega$$

The pulse-width modulator gain can be approximated as the change in output voltage divided by the change in PWM input voltage:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{COMP}} = \frac{9-0}{1.4-0.6} = 11.25 \Rightarrow 21\ dB$$

The LC filter has a double pole at:

$$\frac{1}{2\pi\sqrt{LC}} = 1.87\ kHz$$

and rolls off at 40-dB per decade after that until the ESR zero is reached at:

$$\frac{1}{2\pi R_{ESR} C} = \frac{1}{2\pi(0.027)\left(220 \times 10^{-6}\right)} = 26.8\ kHz$$

This information is enough to calculate the required compensation values. Figure 2–1 shows the power stage gain and phase plots.

Figure 2–1. Power Stage Response

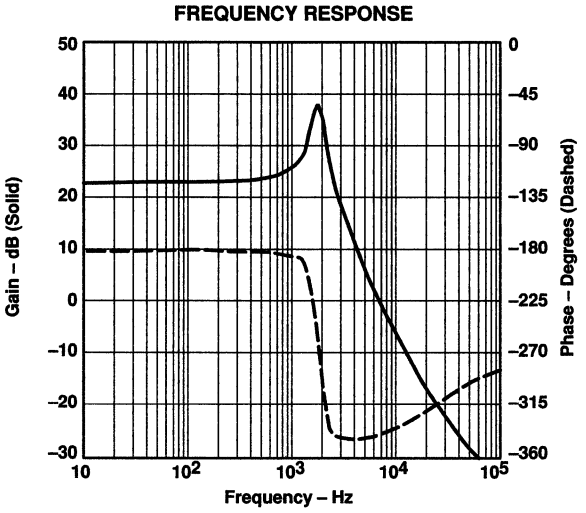
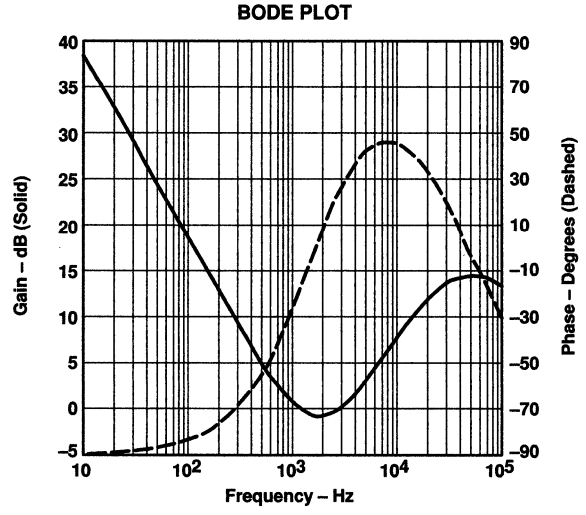


Figure 2–2 shows the required error amplifier compensation response.

Figure 2–2. Required Compensation Response



This response can be met with the following:

- ❑ A pole at zero to give high dc gain
- ❑ Two zeroes at 1.87 kHz to cancel the LC poles
- ❑ A pole at 26.8 kHz to cancel the ESR zero
- ❑ A final pole to roll off high-frequency gain above 100 kHz

The sum of the gains of the modulator, the LC filter, and the error amplifier needs to be 0 dB at the selected unity-gain frequency of 20 kHz. The modulator and LC filter gain is –14 dB. The two zeroes at 1.87 kHz in the compensation network that cancels the LC poles will have a total gain of 41.2 dB at 20 kHz. Therefore, the pole at zero frequency needs to furnish 0–(–14+41.2) = –27.2 dB (voltage gain = 0.04365) at 20 kHz. R5 and C12 provide this pole. R6 is already chosen as 4 kΩ. Calculate C12 as:

$$C12 + C11 = \frac{1}{(2\pi)(f)(R6)(\text{Required Gain})}$$

In practice C12 is much greater than *C*11, therefore:

$$C12 = \frac{1}{(2\pi)(20\ \text{kHz})(4\ \text{k}\Omega)(0.04365)} = 0.045\ \mu\text{F} \quad \text{Use C12} = 0.047\ \mu\text{F}$$

R4 provides the first zero at the LC break point:

$$R4 = \frac{1}{(2\pi)(1.87\ \text{kHz})(C12)} = 1.89\ \text{k}\Omega \qquad \text{Use R4} = 1.8\ \text{k}\Omega$$

C13 provides the other zero at the LC break point:

$$C13 = \frac{\frac{1}{(1.87\ \text{kHz})} - \frac{1}{(20\ \text{kHz})}}{2\pi(R6)} = 0.019\ \mu\text{F} \qquad \text{Use C13} = 0.018\ \mu\text{F}$$

R5 provides the compensation for the ESR zero:

$$R5 = \frac{1}{(2\pi)(26.8\ \text{kHz})(C13)} = 330\ \Omega$$

Finally, C11 provides a rolloff filter at high frequency, chosen at 100 kHz:

$$C11 = \frac{1}{(2\pi)(100\ \text{kHz})(R4)} = 0.00088\ \mu\text{F} \qquad \text{Use C11} = 1000\ \text{pF}$$

Tone Control Evaluation Module User's Guide

Literature Number: SLOU031
January 1999

TEXAS INSTRUMENTS

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Preface

Related Documentation From Texas Instruments

- ***TI Plug-N-Play Audio Amplifier Evaluation Platform*** (literature number SLOU011) provides detailed information on the evaluation platform and its use with TI audio evaluation modules.

- ***TLC2274 Advanced LinCMOS RAIL-TO-RAIL OPERATIONAL AMPLIFIERS*** (literature number SLOS190) This is the data sheet for the TLC2274 Quad operational amplifier integrated circuit used in the Tone Control EVM.

- ***TLV2231 Advanced LinCMOS RAIL-TO-RAIL LOW-POWER SINGLE OPERATIONAL AMPLIFIER*** (literature number SLOS158) This is the data sheet for the TLV2231 operational amplifier integrated circuit used in the Tone Control EVM.

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Contents

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Chapter 1

Introduction

This chapter provides an overview of the Texas Instruments (TI™) Tone Control Evaluation Module (SLOP109). It includes a list of EVM features, a brief description of the module illustrated with a pictorial diagram, and a list of EVM specifications.

Topic **Page**

1.1 Feature Highlights

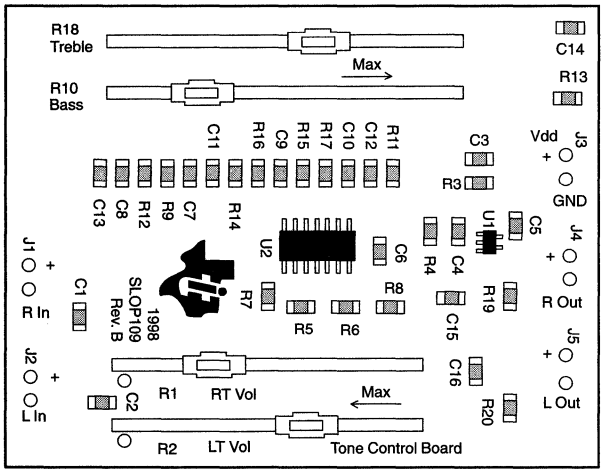
The TI Tone Control Evaluation Module and the TI Plug-N-Play Audio Amplifier Evaluation Platform include the following features:

- Tone Control Evaluation Module
  - Individual slide pots for left and right channel volume control
  - Individual slide pots for bass and treble — the bass control adjusts both channels simultaneously and the treble control adjusts both channels simultaneously
  - 20-dB cut and 15-dB boost for both bass and treble
  - 3.3-V and 5-V operation
- Quick and Easy Configuration with The TI Plug-N-Play Audio Amplifier Evaluation Platform
  - Evaluation module is designed to simply plug into the platform, automatically making all signal, control, and power connections
  - Platform provides flexible power options
  - Jumpers on the platform select power and module control options
  - Switches on the platform route signals
  - Platform provides quick and easy audio input and output connections
- Platform Power Options
  - External 5-V – 15-V DC V_{CC} supply inputs
  - External regulated V_{DD} supply input
  - Socket for onboard 5-V/3.3-V V_{DD} voltage regulator EVM
  - Onboard overvoltage and reverse polarity power protection
- Platform Audio Input and Output Connections
  - Left and right RCA phono jack inputs
  - Miniature stereo phone jack input
  - Left and right RCA phono jack outputs
  - Left and right compression speaker terminal outputs
  - Miniature stereo headphone jack output

1.2 Description

The Tone Control Evaluation Module is a complete audio volume level and base and treble control board that is designed primarily for use with the TI Plug-N-Play Audio Amplifier Evaluation Platform. It consists of separate slide pots for the right- and left-channel volume control, a slide pot for controlling the bass response of both channels, a slide pot for adjusting the treble response of both channels, a single-channel operational amplifier IC, a quad operational amplifier IC, and a small number of passive components mounted on a circuit board that measures approximately 2 1/4 inches by 1 3/4 inches (Figure 1–1).

Figure 1–1. The Tone Control Evaluation Module



Single in-line header pins extend from the underside of the module circuit board to allow the EVM to be plugged into the TI Plug-N-Play Audio Amplifier Evaluation Platform, or to be wired directly into existing circuits and equipment when used stand-alone.

The platform, with room for a single tone control evaluation module, is a convenient vehicle for evaluating TI's audio power amplifier and related evaluation modules. The EVMs simply plug into the platform, which automatically provides power to the modules, interconnects them correctly, and connects them to a versatile array of standard audio input and output jacks and connectors. Easy-to-use configuration controls allow the platform and EVMs to quickly model many possible end-equipment configurations.

There is nothing to build, nothing to solder, and nothing but the speakers included with the platform to hook up.

1.3 Tone Control EVM Specifications

Supply voltage range, V_{DD}	3 V to 5.5 V
Supply current, I_{DD}	6.85 mA max
Audio input voltage, V_I	4 Vpp max
Audio output voltage, V_O	4 Vpp max

Chapter 2

Quick Start

Follow the steps in this chapter to quickly prepare the Tone Control EVM for use. Using the Tone Control EVM with the TI Plug-N-Play Audio Amplifier Evaluation Platform is a quick and easy way to connect power, signal, and control inputs, and signal outputs to the EVM using standard connectors. However, the Tone Control EVM can be used stand-alone by making connections directly to the module pins, and can be wired into existing circuits or equipment.

Topic **Page**

2.1 Precautions

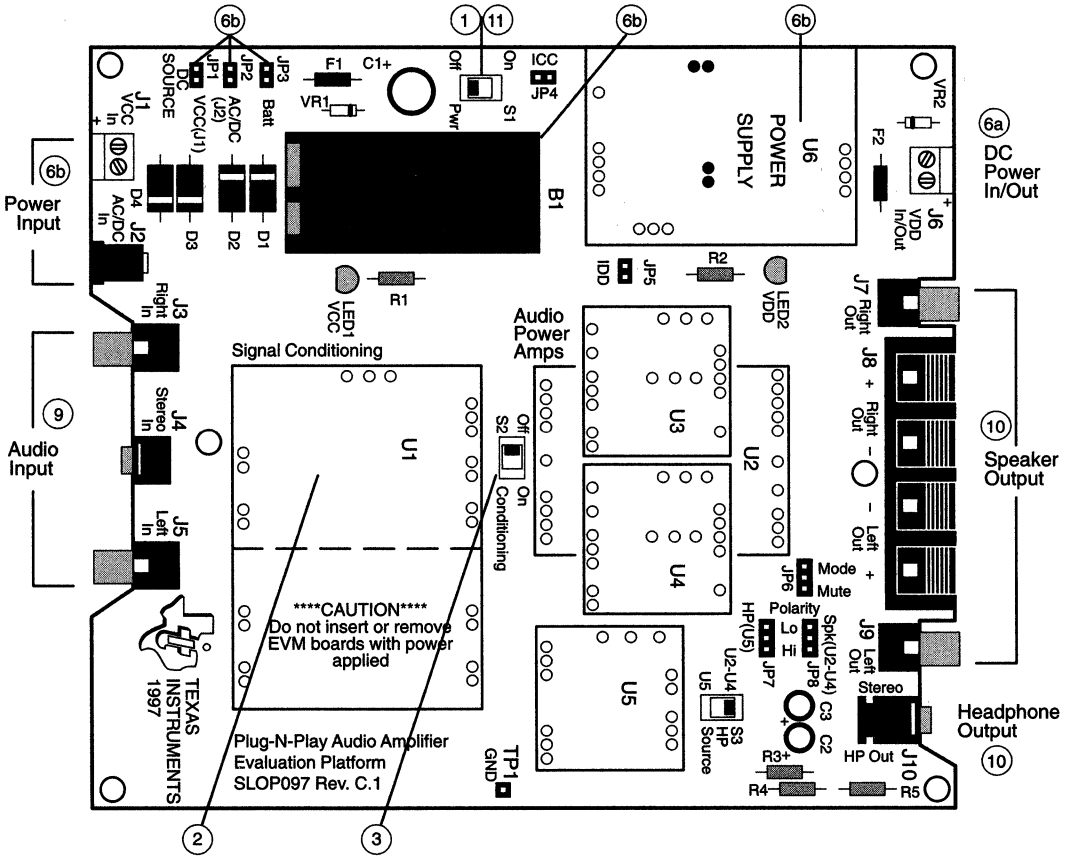
Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected to V_{CC} power input connector J1, J2, and/or V_{DD} power input connector J6 are correct. Overvoltage or reverse-polarity power applied to these terminals can open onboard soldered-in fuses and cause other damage to the platform, installed evaluation modules, and/or the power source.

Inserting or Removing EVM Boards

Do not insert or remove EVM boards with power applied — damage to the EVM board, the platform, or both may result.

Figure 2–1. Quick Start Platform Map



2.2 Quick Start List for Platform

Follow these steps when using the Tone Control EVM with the TI Plug-N-Play Audio Amplifier Evaluation Platform (see the platform user's guide, SLOU011, for additional details). Numbered callouts for selected steps are shown in Figure 2–1, and details appear in Chapter 3.

❑ **Platform preparations**

1) Ensure that all external power sources are set to ***OFF*** and that the platform power switch **S1** is set to ***OFF.***

2) Install the tone control module in the **Signal Conditioning** platform socket **U1,** taking care to align the module pins correctly.

3) Set switch **S2** to ***ON*** to select signal conditioning by the Tone Control EVM.

4) Install power amplifiers and/or a headphone amplifier module in the appropriate platform sockets (see the amplifier module User's Guide for details).

5) Set platform jumpers and switches in accordance with the user's guide for each amplifier module installed on the platform.

❑ **Power supply**

6) Select and connect the power supply (ensure power supply is set to ***OFF***):

   a) Connect an external regulated power supply set to 5 V to platform V_{DD} power input connector **J6** taking care to observe marked polarity,
   or

   b) Install a voltage regulator EVM (SLVP097 or equiv.) in platform socket **U6**. Connect a 7 V – 12 V power source to a platform V_{CC} power input **J1** or **J2** and jumper the appropriate power input (see platform user's guide).

❑ **Inputs and outputs**

7) Ensure that the audio signal source level is set to minimum.

8) Set the EVM right and left volume slide pots to minimum.

9) Connect the audio source to left and right RCA phono jacks **J3** and **J5** or stereo miniature phone jack **J4.**

10) Connect 3-Ω – 8-Ω speakers to left and right RCA jacks **J7** and **J9** or to stripped wire speaker connectors **J8,** *or* plug headphones into **J10**.

❑ **Power Up**

11) Verify correct voltage and input polarity and set the external power supply to ***ON.*** If V_{CC} and an onboard regulator EVM are used to provide V_{DD}, set platform power switch **S1** to ***ON.***

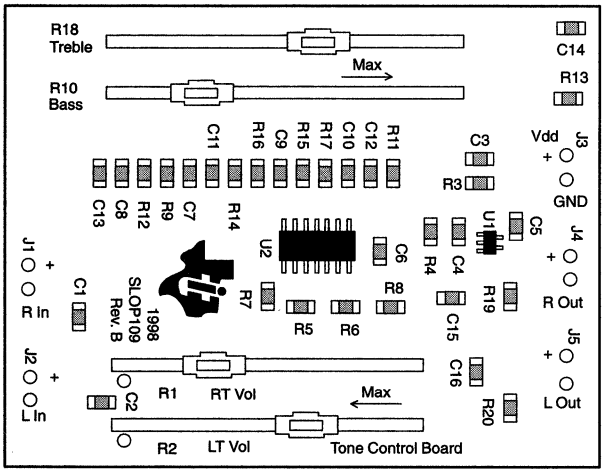
Platform LED2 should light indicating the presence of V_{DD}, and the evaluation modules installed on the platform should begin operation.

12) Adjust the signal source and Tone Control EVM audio levels as needed.

2.3 Quick Start List for Stand-Alone

Follow these steps to use the Tone Control EVM stand-alone or when connecting it into existing circuits or equipment. Connections to the tone control module header pins can be made via individual sockets, wire-wrapping, or soldering to the pins, either on the top or the bottom of the module circuit board. The Tone Control EVM is shown in Figure 2–2 and details appear in Chapter 3.

Figure 2–2. Quick Start Module Map — Stand-Alone



❑ **Power supply**

1) Ensure that all external power sources are set to ***OFF.***

2) Connect an external regulated power supply set to 5 V to the module **VDD** and **GND** pins taking care to observe marked polarity.

❑ **Inputs and outputs**

3) Ensure that audio signal source level adjustments are set to minimum.

4) Set the Tone Control EVM volume slide pots to minimum.

5) Connect the audio source to the module **R IN** and **L IN** pins, taking care to observe marked polarity.

❑ **Power Up**

6) Verify correct voltage and input polarity and set the external power supply to ***ON.***

The EVM should begin operation.

7) Adjust the signal source and Tone Control EVM audio levels as needed.

Chapter 3

Details

This chapter provides details on the Tone Control EVM, the steps in the Quick-Start List, additional application information, and a parts list for the Tone Control evaluation module.

Topic **Page**

3.1 Precautions

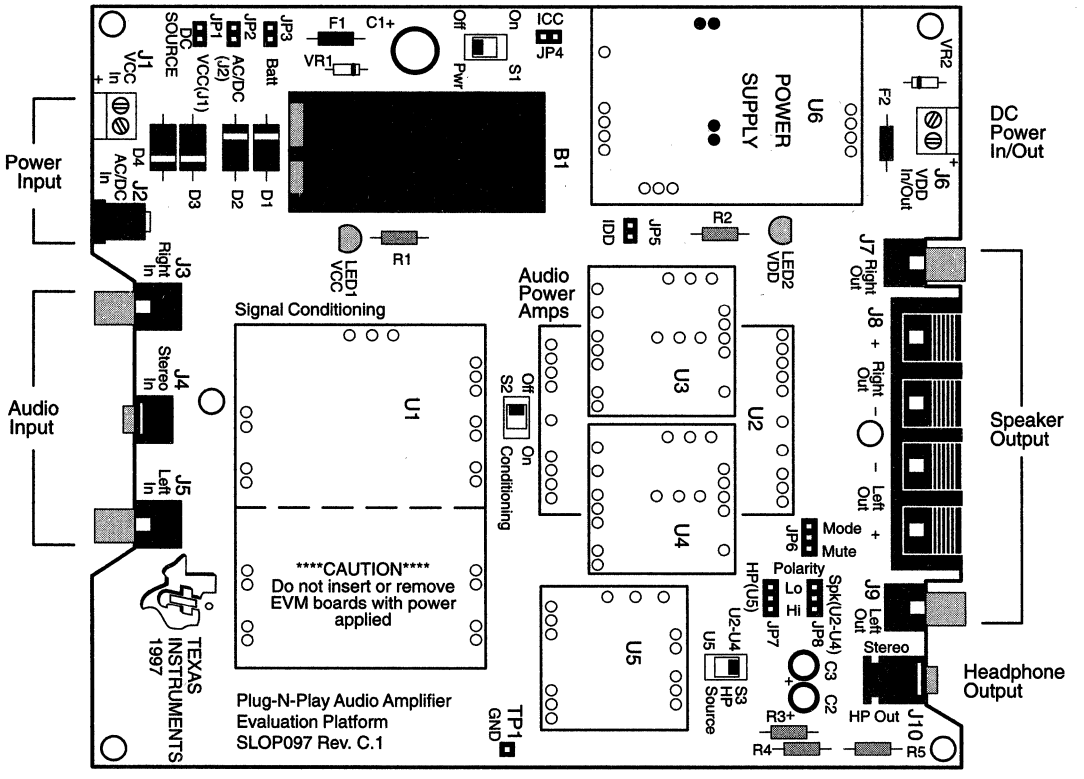
Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected to V_{CC} power input connector J1, J2, and/or V_{DD} power input connector J6 are correct. Overvoltage or reverse-polarity power applied to these terminals can open onboard soldered-in fuses and cause other damage to the platform, installed evaluation modules, and/or the power source.

Inserting or Removing EVM Boards

Do not insert or remove EVM boards with power applied — damage to the EVM board, the platform, or both may result.

Figure 3–1. The TI Plug-N-Play Audio Amplifier Evaluation Platform



3.2 The Tone Control Evaluation Module

The Tone Control Evaluation Module provides a convenient way to control the audio volume and the tonal response of audio amplifier EVMs plugged into the TI Plug-N-Play Audio Amplifier Evaluation Platform. Tone controls allow the frequency response of the audio system to be adjusted to compensate for the response of speakers and their enclosures, or to simply provide a more pleasing sound. A pair of slide pots adjusts the volume of each channel independently, while a single slide pot adjusts the bass response of both channels simultaneously and another slide pot adjusts the treble response of both channels. The module provides a gain of 2 at the maximum volume setting when both tone controls are at their midpoints (flat).

Although the Tone Control EVM is designed to be used with the TI Plug-N-Play Audio Amplifier Evaluation Platform (Figure 3–1), it can be wired directly into circuits or equipment. The module has single in-line header connector pins mounted to the underside of the board. These pins allow the module to be plugged into the TI platform, which automatically makes all the signal input and output, power, and control connections to the module.

The module connection pins are on 0.1-inch centers to allow easy use with standard perf board and plug board-based prototyping systems. Or, the EVM can be wired directly into existing circuits and equipment when used stand-alone.

The module appears in Figure 3–2 and its schematic is shown in Figure 3–3.

Figure 3–2. Tone Control EVM

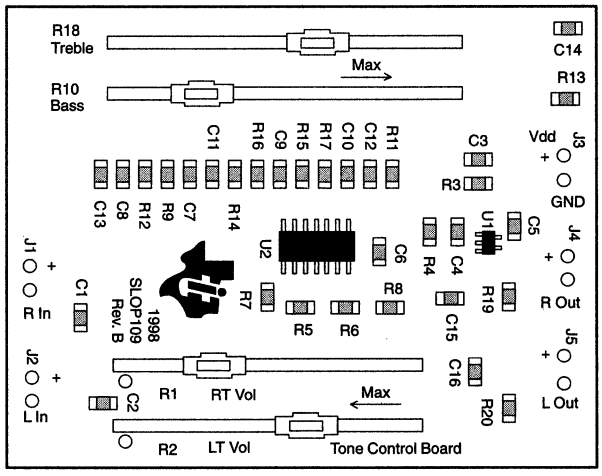
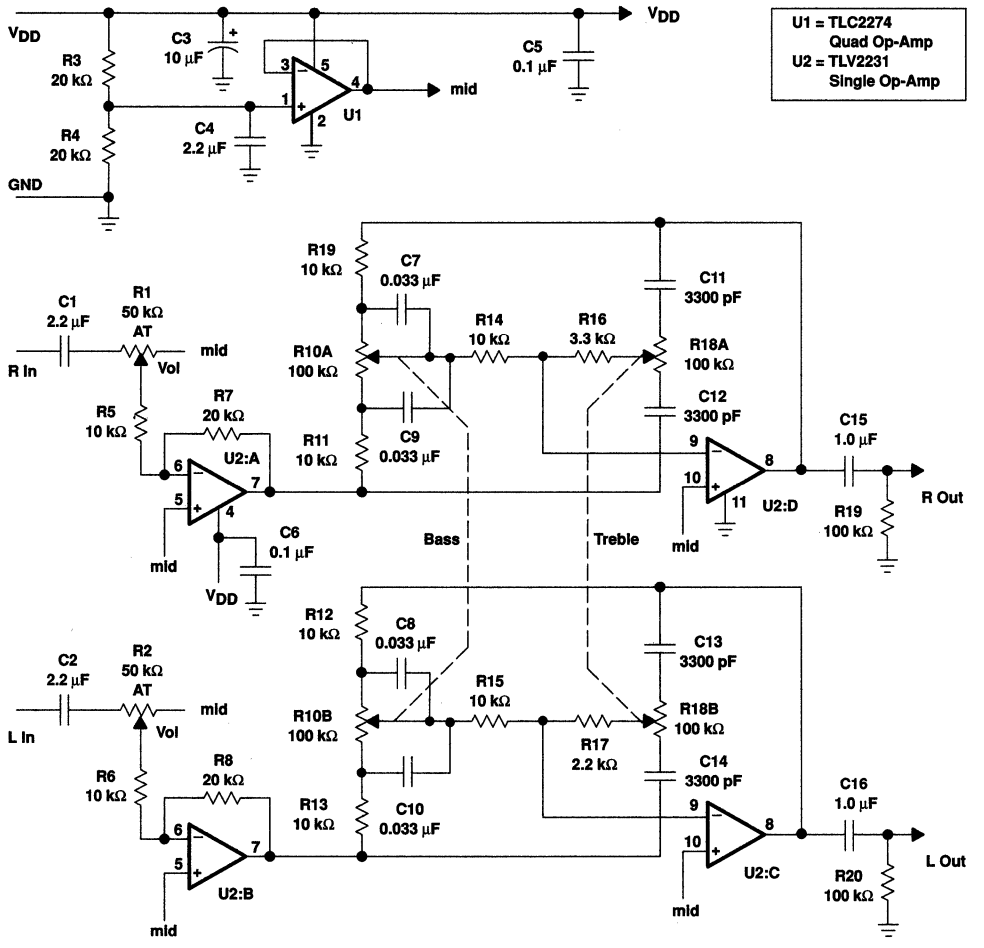


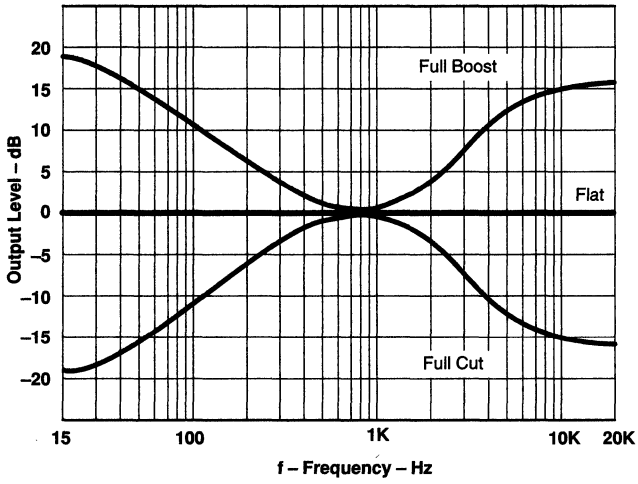
Figure 3–3. Tone Control EVM Schematic Diagram



The Tone Control EVM is a variation of the classic and very popular Baxandall negative feedback tone control. This circuit allows a range of adjustment from cut, through flat, to boost in bass response with a single potentiometer. Another potentiometer provides the same range of adjustment for the treble response. The component values indicated in the schematic provide the response curve shown in Figure 3–4. Each of the tone adjusting potentiometers is a dual unit, allowing the simultaneous adjustment of both channels with a single control. A separate volume control for each channel allows the adjustment of balance between the channels as well as volume.

A single TLC2274 quad rail-to-rail operational amplifier IC contains all the amplifiers required for both channels. A TLV2231 operational amplifier IC is connected to provide a midpoint voltage (and signal ground) for proper operation of the TLC2274.

Figure 3–4. Tone Control Evaluation Module Frequency Response

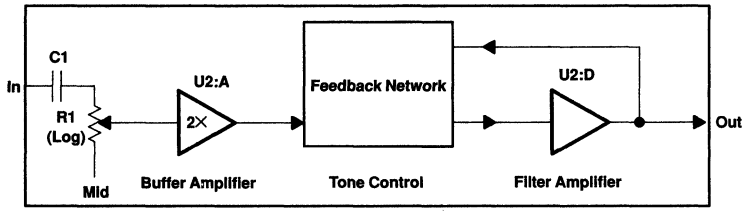


3.2.1 Tone Control EVM Circuit Description

Each of the two separate channels on the Tone Control EVM is basically an active filter built around an IC operational amplifier. An active filter design was chosen over a passive filter circuit because active filters have the frequency-response adjusting components located in the feedback loop of the filter amplifiers, providing much lower THD, little or no insertion loss, and a symmetrical response about the axis in both boost and cut, compared with most passive designs. Each channel also includes an input buffer amplifier to provide some gain, isolation from source impedance variations, signal inversion, and a low-impedance drive for the filter circuit.

A block diagram of the right channel of the Tone Control EVM is shown in Figure 3–5. The left channel is identical.

Figure 3–5. Tone Control EVM Block Diagram



The input buffer amplifier provides a gain of approximately 2 (R_F/R_{IN}) with the resistor values installed on the module. Input capacitor C1 blocks DC and sets the overall low-frequency rolloff of the EVM at approximately 16 Hz with the installed value of 2.2 µF. Volume control R1 has an audio taper to provide a perceived response in volume that is proportional to the physical position of the slider and gives an adjustment range at the output of the buffer amplifier of from 0 V to approximately 2× the audio signal input voltage.

The tone adjusting action in each channel of the Tone Control EVM is provided by an equalized amplifier (or active filter) created by placing a frequency-dependent negative feedback network around an operational amplifier. Almost any overall gain-versus-frequency characteristic can be defined by the design of the feedback network.

The EVM provides the familiar *Hi-Fi tone control,* in which the low audio frequencies can be boosted or cut approximately 20 dB with the bass control and the high audio frequencies can be boosted or cut approximately 20 dB with the treble control. Middle frequencies are not affected by the tone controls. An overall flat response (no boost or cut at frequency extremes) is obtained when the tone controls are at their mid-point position.

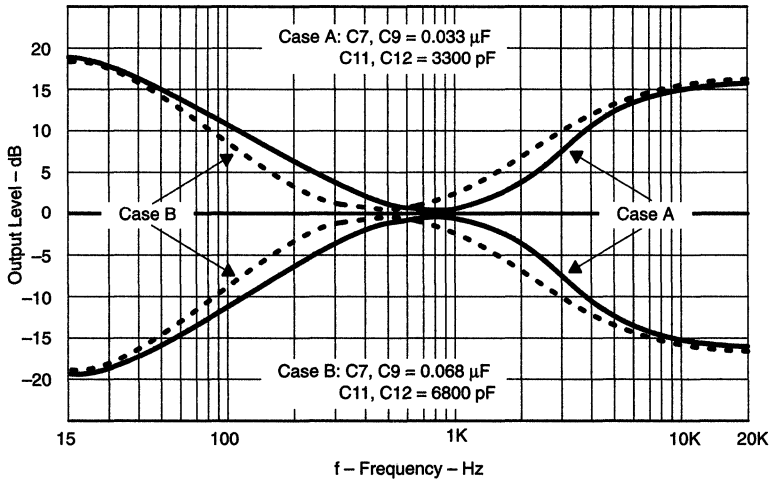
3.2.2 Tone Control EVM Frequency Response

The overall Tone Control EVM frequency response can be shifted up or down by changing the values of capacitors C7, C9, C11, and C12 in the tone adjusting networks on the module. Care must be taken, however, because the surface-mount solder pads on the board are somewhat fragile and will not survive a large number of soldering/desoldering operations.

To shift the EVM frequency response downward, for example, increase the values of the capacitors in the tone adjusting networks. Doubling the values of C7, C9, C11, and C12 shifts the break frequency downward a full octave (Case B, Figure 3–6). Conversly, halving the values of C7, C9, C11, and C12 shifts the break frequency upward a full octave.

Note that to keep the boost and cut break frequencies the same, the value of C7 must equal that of C9, and the value of C11 must equal that of C12. In addition, although the bass and treble break frequencies can be adjusted separately if desired, to maintain the overall shape and symmetry of the response, all four capacitors must be increased or decreased by the same factor.

Figure 3–6. Bass and Treble Tone Control Response



3.3 Using The Tone Control EVM With the Plug-N-Play Evaluation Platform

The Tone Control Evaluation Module was designed to be used with the TI Plug-N-Play Audio Amplifier Evaluation Platform. It simply plugs into socket U1.

The following paragraphs provide additional details for using the Tone Control EVM with the platform.

3.3.1 Installing and Removing EVM Boards

TI Plug-N-Play evaluation modules use single-in-line header pins installed on the underside of the module circuit board to plug into sockets on the platform. The EVM pins and the platform sockets are keyed such that only the correct type of EVM can be installed in a particular socket, and then only with the proper orientation.

Evaluation modules are easily removed from the platform by simply prying them up and lifting them out of their sockets. Care must be taken, however, to prevent bending the pins.

3.3.1.1 EVM Insertion

1) Remove all power from the evaluation platform.
2) Locate the appropriate socket on the platform.
3) Orient the module correctly.
4) Carefully align the pins of the module with the socket pin receptacles.
5) Gently press the module into place.
6) Check to be sure that all pins are seated properly and that none are bent over.

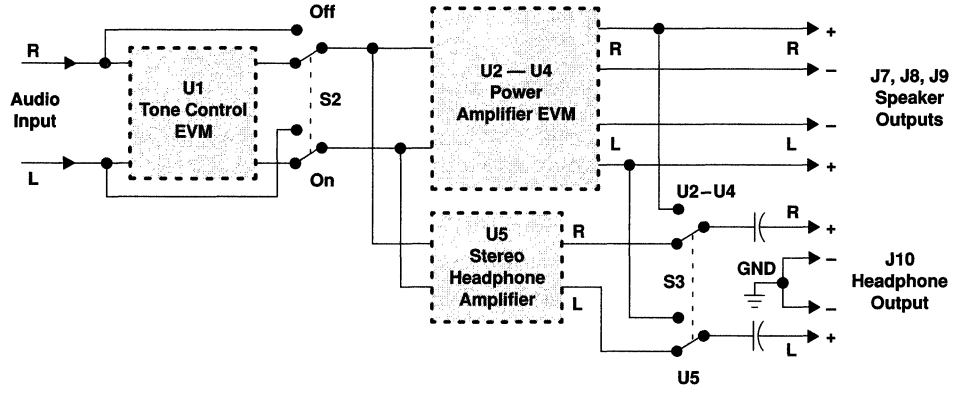
3.3.1.2 EVM Removal

1) Remove all power from the evaluation platform.
2) Using an appropriate tool as a lever, gently pry up one side of the module a small amount.
3) Change to the opposite side of the module and use the tool to pry that side up a small amount.
4) Alternate between sides, prying the module up a little more each time to avoid bending the pins, until it comes loose from the socket.
5) Lift the EVM off of the platform.

3.3.2 Signal Routing

Signal flow on the platform is controlled by two signal routing switches, as shown in Figure 3–7.

Figure 3–7. Platform Signal Routing and Outputs



3.3.2.1 Signal Conditioning

The Tone Control EVM plugs into the Signal Conditioning socket (U1) on the platform. The audio signal from the platform input jacks can be applied to the signal conditioning socket (U1) or can bypass socket U1 as determined by conditioning switch S2.

- ❑ Switch **S2** selects the tone control signal conditioning or bypasses it

3.3.2.2 Headphone Output Jack

Switch S3 is the source select for the stereo headphone output jack, J10. The headphone jack is capacitively coupled (via 470 µF electrolytics) and can output either the signal from the headphone amplifier in socket U5, or the signal from the power amplifier installed in sockets U2 – U4, as determined by the setting of headphone source select switch S3.

When S3 is set to the power amplifier position (U2 – U4), the headphone jack is connected to the power amplifier OUT+ output lines. When a plug is inserted into the jack, signals output through J10 are returned to platform ground, requiring single-ended power amplifier operation. A switch inside the headphone jack produces a control signal that can be routed to the power amplifier socket to shut down the power amplifier EVM or switch it to single-ended output mode when a plug is inserted.

See the User's Guide for the power amplifier and/or the headphone amplifier installed on the platform for information on the correct setting of switch S3.

3.3.3 Mute/Mode/Etc.

Some power amplifier EVMs have a mute or mode control input pin. This allows the power amplifier to enter the mute state for decreased power consumption or to switch output modes in response to a control signal applied to this pin.

In typical applications, as often found in notebook computers, portable audio products, and such, the internal speakers mute when headphones are plugged into the headphone jack, or internal speakers mute when external speakers are connected. In applications using separate speaker and headphone amplifiers, the power amplifier can be shut down (muted) to conserve power when the headphone amplifier is in use.

Output mode switching allows some power amplifier EVMs to operate in the bridge-tied load (BTL) output mode for increased power to internal speakers and then switch to single-ended mode to drive headphones when a plug is inserted into the headphone jack, eliminating the need for a separate headphone amplifier.

The platform is equipped with mute/mode control signal select and polarity jumpers and a headphone source switch to provide the maximum flexibility in configuring the operation of the various power amplifier and headphone amplifier EVMs that might be installed on the platform. See the User's Guide for the power amplifier and/or the headphone amplifier installed on the platform for information on the correct settings of platform mute, mode, polarity jumpers, and the platform headphone source switch.

3.3.4 Power Requirements

The Tone Control Evaluation Module can operate from any voltage between approximately 3 V and 5.5 V. For best performance (highest output power with lowest distortion), the module should be operated at approximately 5 V unless there is a specific reason for operating it from a lower voltage.

The TI Plug-N-Play Audio Amplifier Evaluation Platform with a voltage regulator EVM installed on it can provide a regulated V_{DD} supply from a wide variety of unregulated V_{CC} voltage inputs between approximately 5.5 V and 12 V, including an onboard 9-V battery. Or, an external regulated power source can be used to supply V_{DD} voltage to the platform and the tone control evaluation module installed on it.

Although the Tone Control EVM draws a very small amount of current from the supply, power amplifiers installed on the platform can draw as much as approximately 2 A from the power supply during continuous full power output. Any power supply connected to the platform should be capable of providing adequate current to the power amplifier installed on the platform to avoid clipping of the output signal during peaks. Current consumption driving speakers at normal listening levels is typically 0.5 A or less.

The platform is equipped with overvoltage and reverse-polarity supply voltage input protection in the form of fused crowbar circuits.

- V_{DD} voltage applied to platform screw terminals J6 *MUST NOT* exceed the absolute maximum rating for *any* EVM installed on the platform, or damage may result. In no case should V_{DD} voltage of the incorrect polarity or in excess of 6.1 V be applied to screw terminals J6 of the platform, or the power protection circuit on the V_{DD} line will trip.
- V_{CC} voltage applied to the platform *MUST NOT* exceed the maximum voltage input specified for the voltage regulator module installed in socket U6 (12 V for the SLVP097), or damage to the voltage regulator module may result. In no case should V_{CC} voltage applied to the platform exceed 15 V, or the overvoltage protection circuit on the V_{CC} bus will trip.

3.3.5 Inputs and Outputs

The TI Plug-N-Play Audio Amplifier Evaluation Platform is equipped with several standard conectors for audio inputs and outputs.

3.3.5.1 Inputs

Audio signals enter the platform through either a pair of RCA phono jacks (J3 and J5) or a miniature (1/8″) stereo phone jack (J4). The platform audio signal input jacks (J3, J4, and J5) are of the closed-circuit type, grounding the signal input lines when no plugs are inserted.

3.3.5.2 Outputs

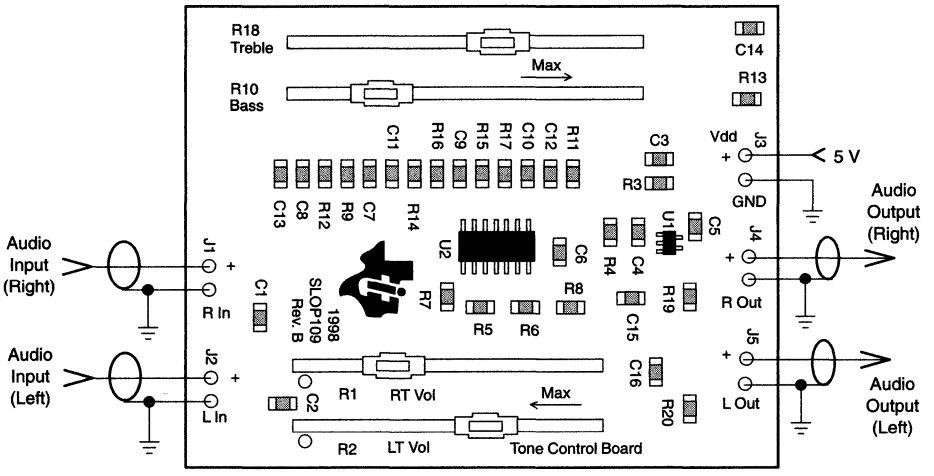
Amplified audio output signals leave the platform through left and right RCA phono jacks (J7 and J9), left and right pairs of compression connectors for stripped speaker wires (J8), and optionally, through a miniature (1/8″) stereo phone jack (J10), for headphones.

3.4 Using The Tone Control EVM Stand-Alone

Using the Tone Control Evaluation Module stand-alone is much the same as using it with the platform. The same 5-V power supply requirement exists.

3.4.1 Tone Control EVM Connected for Stand-Alone Operation

Figure 3–8. Tone Control EVM Stand-Alone Operation



3.5 Tone Control Evaluation Module Parts List

Table 3–1. Tone Control EVM Parts List

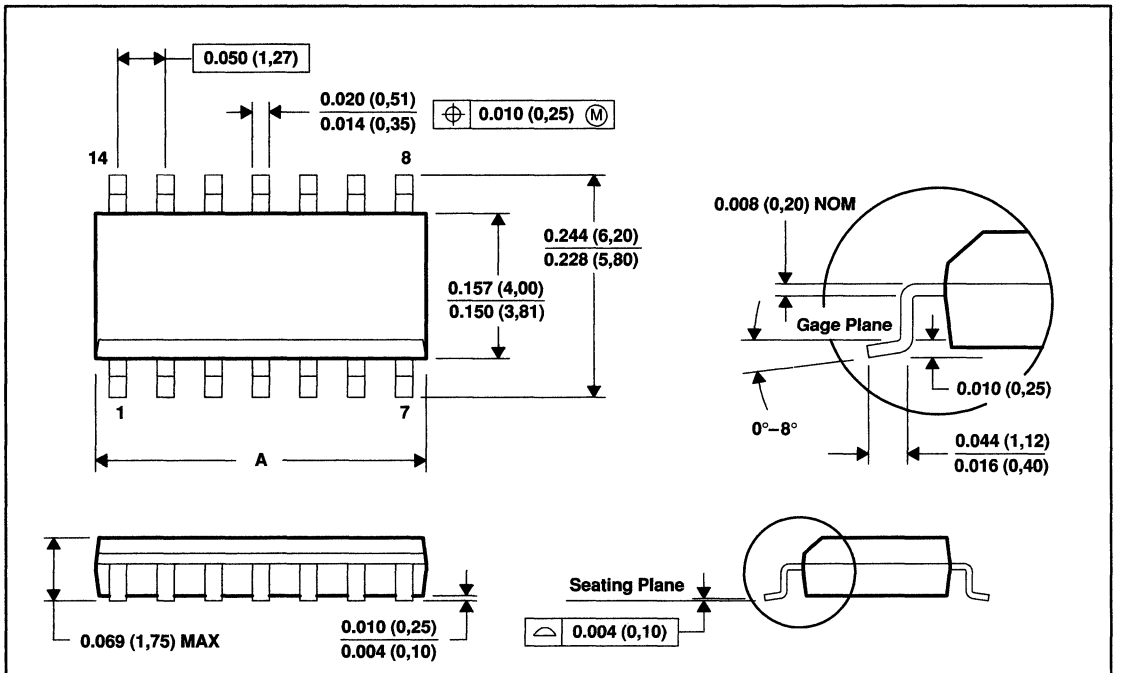
Reference	Description	Size	EVM Qty.	Source/ Part Number
C1, C2, C4	Capacitor, ceramic, 2.2 μF, 16 V, YV5	1206	3	TDK C3216Y5V1C225Z
C3	Capacitor, ceramic, 10 μF, 16 V, YV5	1210	1	TDK C3216Y5V1C106Z
C15, C16	Capacitor, ceramic, 1 μF, 16 V, YV5	1206	2	TDK C3216Y5V1C105Z
C7, C8, C9, C10	Capacitor, ceramic 0.033 μF, 50 V, NPO	1206	2	Digi-Key
C5, C6	Capacitor, ceramic, 0.1 μF, 50 V, X7R	1206	2	Digi-Key PCC104BCT–ND
C11, C12, C13, C14	Capacitor, ceramic 3300 pF, 50 V, NPO	1206	4	Digi-Key
R10, R18	Dual potentiometer, 100 kΩ, linear taper, slide control		2	CTS 448XC351109
R1, R2	Potentiometer, 50 kΩ, audio taper, slide control		2	CTS 448XC3503BAN
R5, R6, R9, R11, R12, R13, R14, R15	Resistor, CF, 10 kΩ, 1/8 W, 5%	1206	8	
R3, R4, R7, R8	Resistor, CF, 20 kΩ, 1/8 W, 5%	1206	4	
R16, R17	Resistor, CF, 3.3 kΩ, 1/8 W, 5%	1206	2	
R19, R20	Resistor, CF, 10 kΩ, 1/8 W, 5%	1206	2	
J1–J5	Header, 2 position, 100-mil centers		5	Digi-Key S1022–36ND
U1	TLV2231IDBV IC operational amplifier	SOT-23	1	TI
U2	TLC2274CD quad IC operational amplifier	SOIC	1	TI
PCB	PCB, Tone Control EVM		1	TI SLOP109

Contents

7 Mechanical Data

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

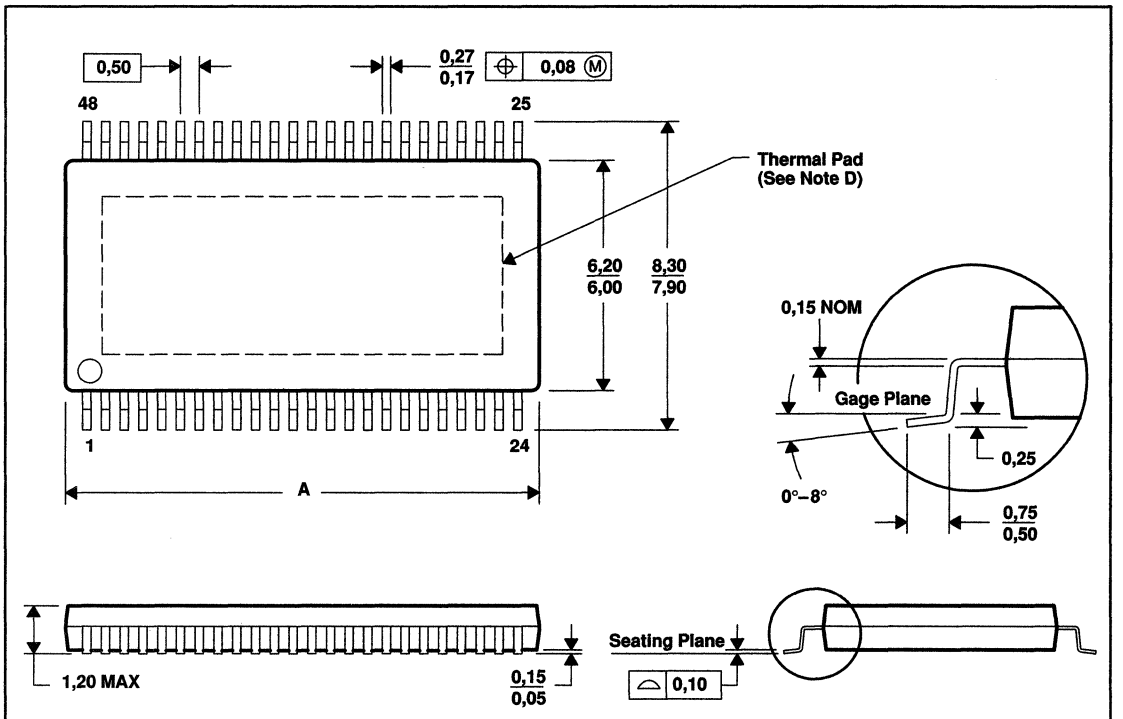
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DCA (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

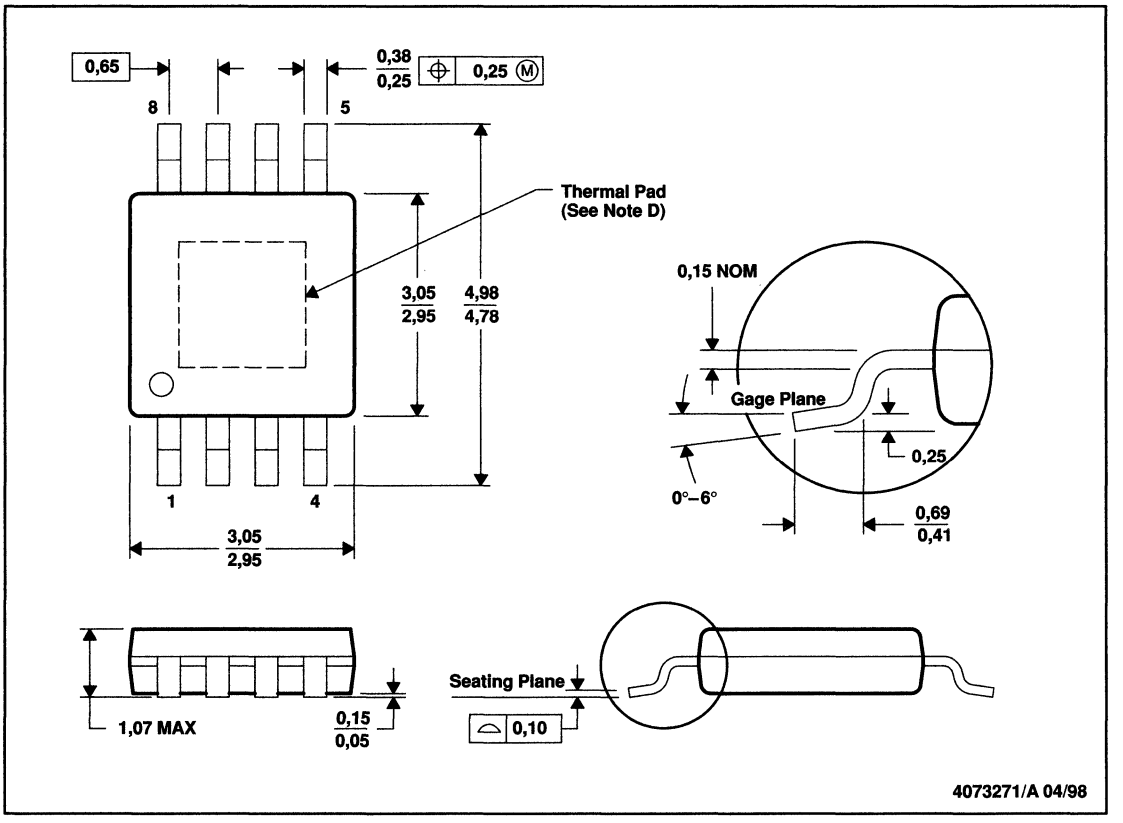
4073259/A 01/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 68 mils (height as illustrated) × 70 mils (width as illustrated) (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MO-187

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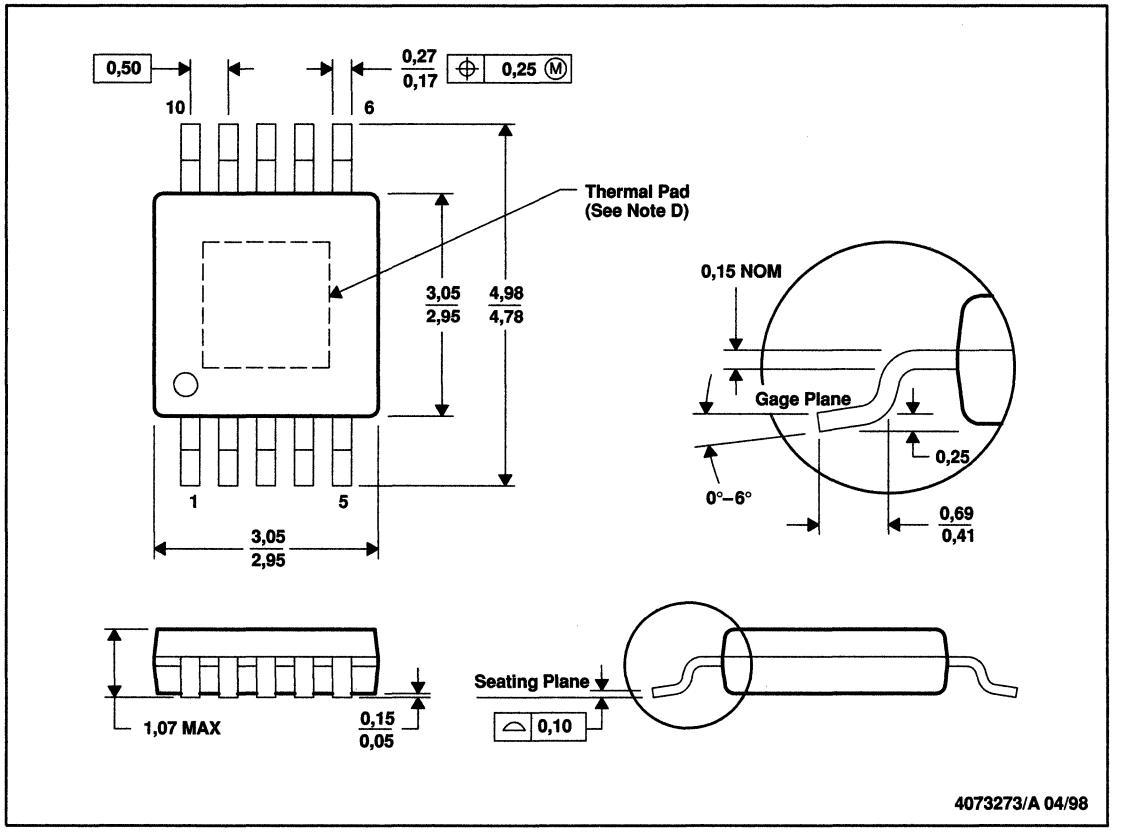
MECHANICAL INFORMATION

DGQ (S-PDSO-G10) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 68 mils (height as illustrated) × 70 mils (width as illustrated) (maximum). The pad is centered on the bottom of the package.

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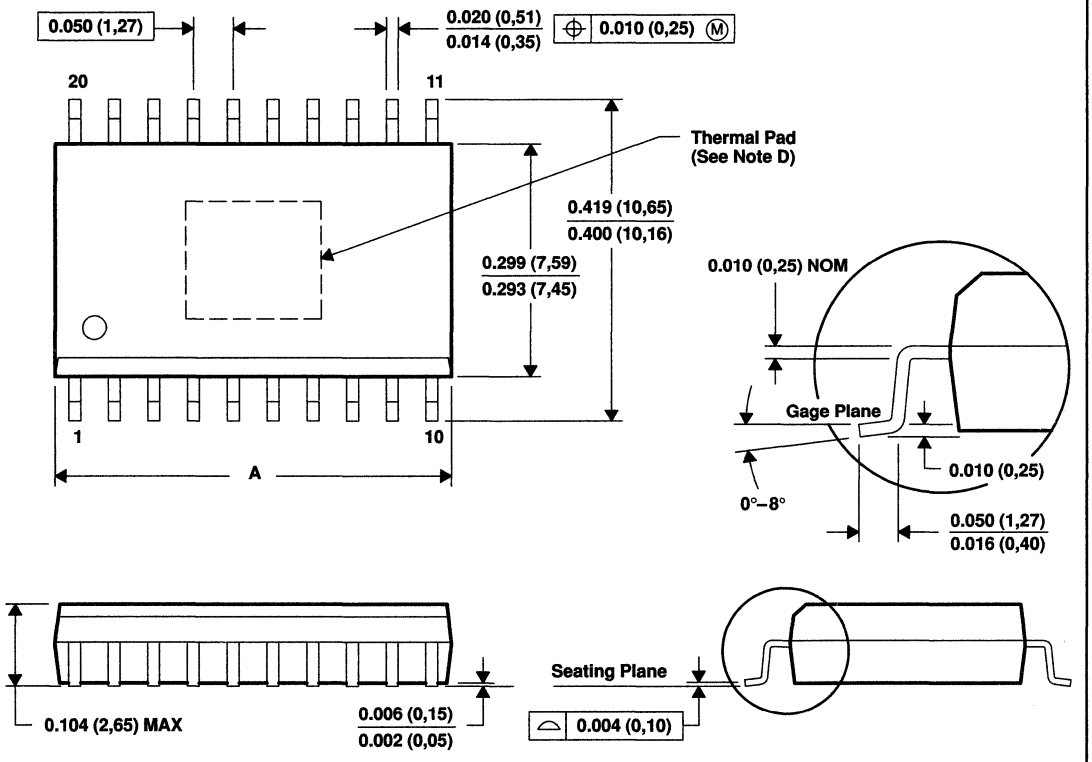
MECHANICAL INFORMATION

DWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/A 04/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

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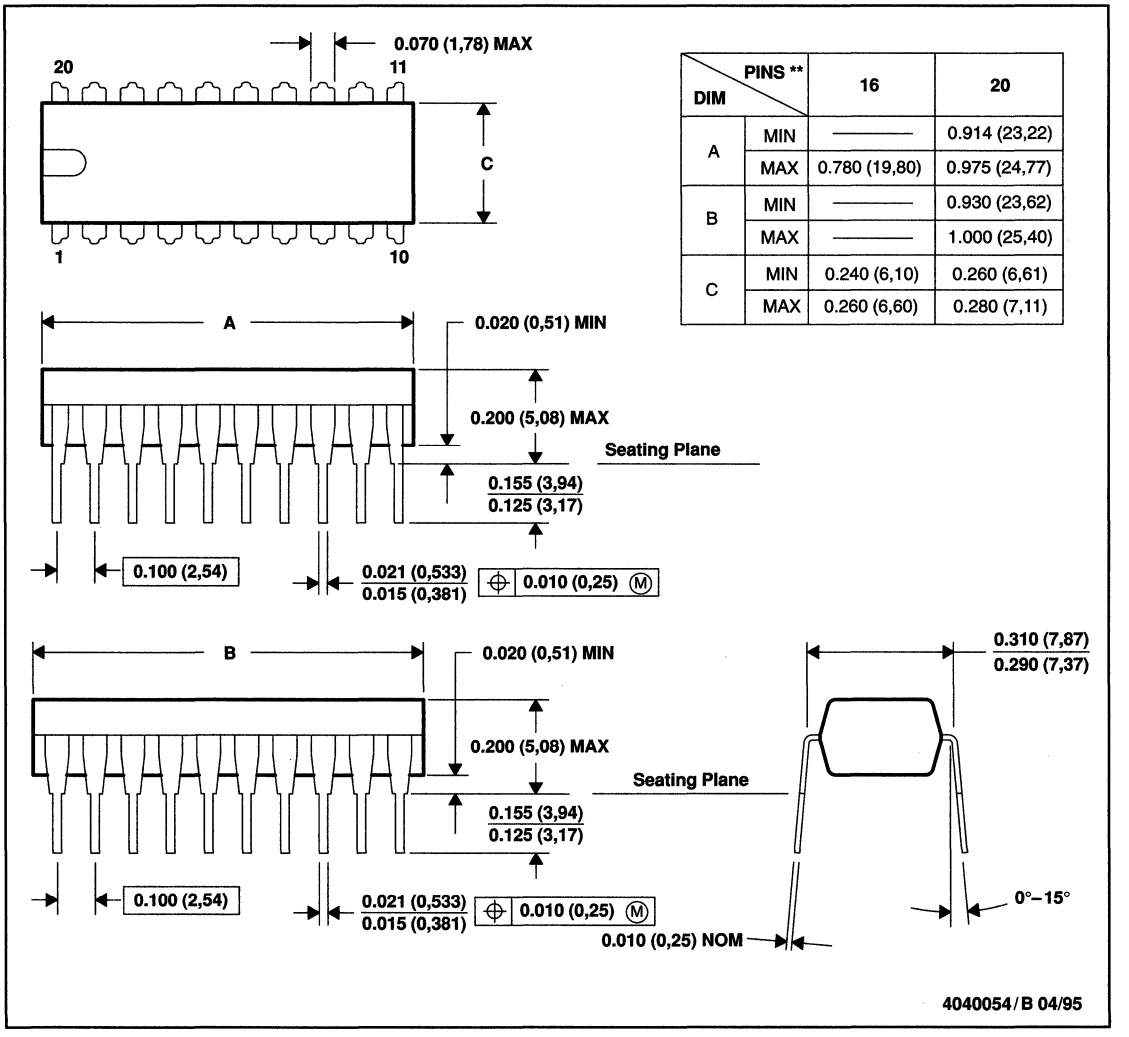
MECHANICAL INFORMATION

NE (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

20 PIN SHOWN



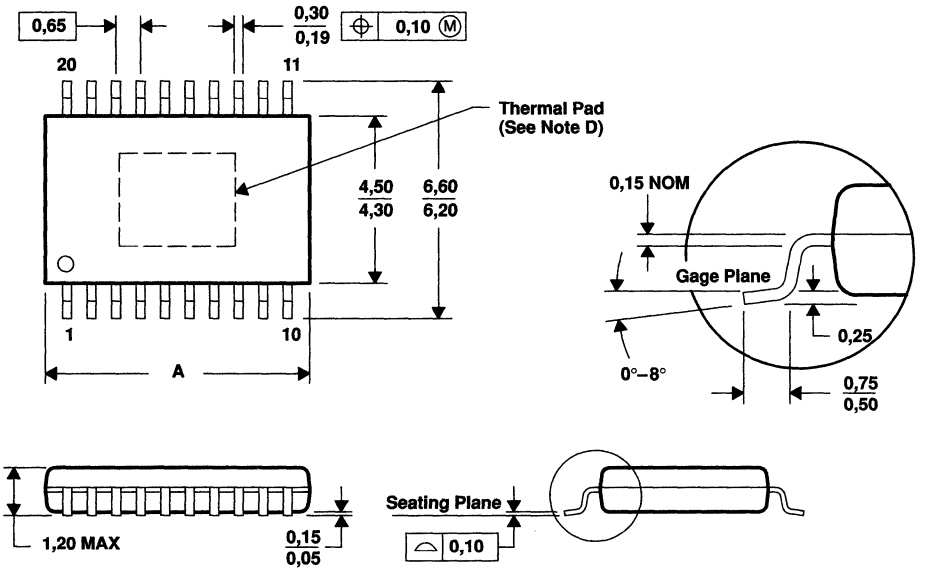
DIM \ PINS **		16	20
A	MIN	———	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	———	0.930 (23,62)
	MAX	———	1.000 (25,40)
C	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (16 pin only)

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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Indonesia	001-801-10	-800-800-1450
Korea	080-551-2804	-
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