Using Cross-Point Arrays to Achieve Fast Write Speeds

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Rambus Inc.

August 22, 2012

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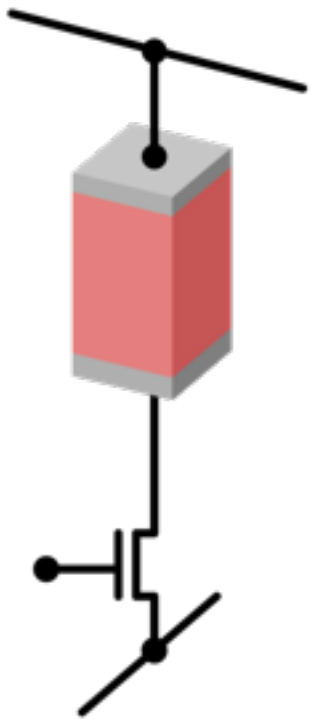
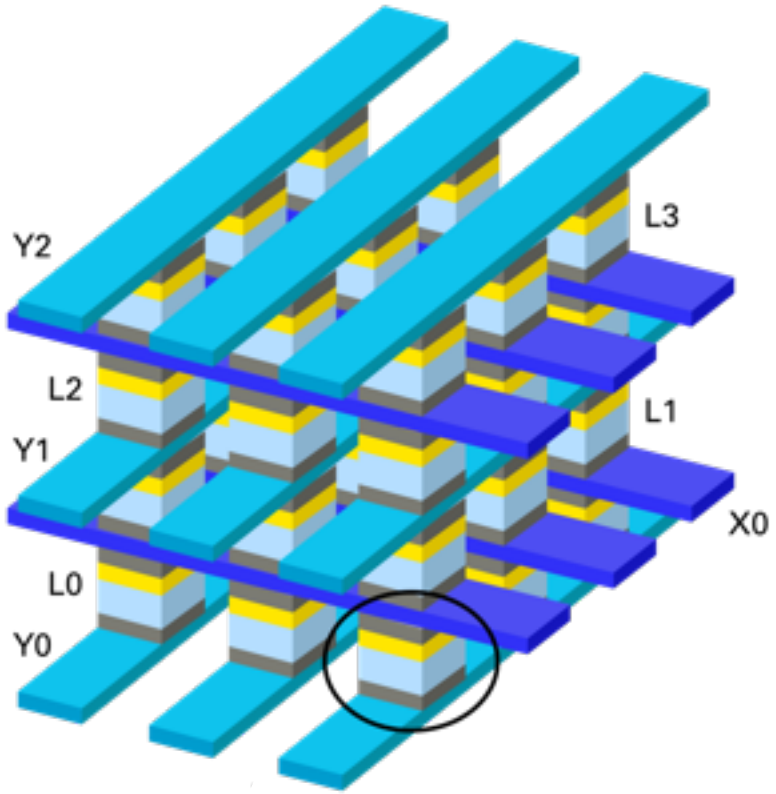
True Cross Point Arrays, without a transistor per cell, are necessary to achieve high density memories. Can they be fast too?



Typical RRAM cell has a transistor as select device



RRAM cell in a cross point for very high density

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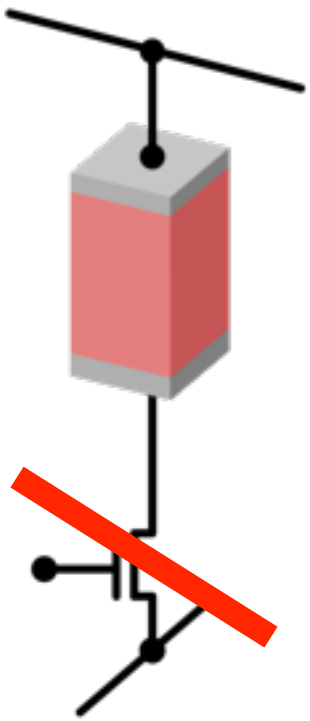

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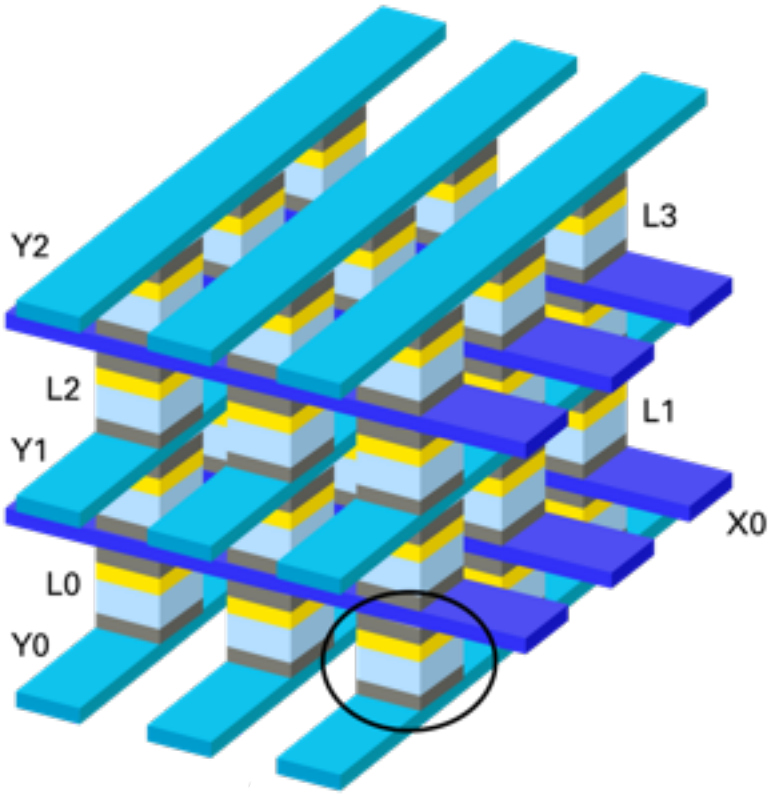

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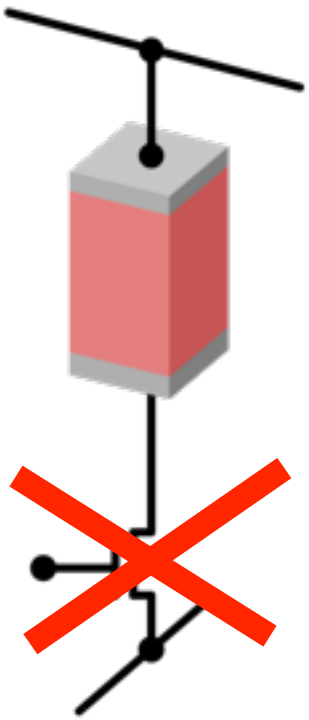

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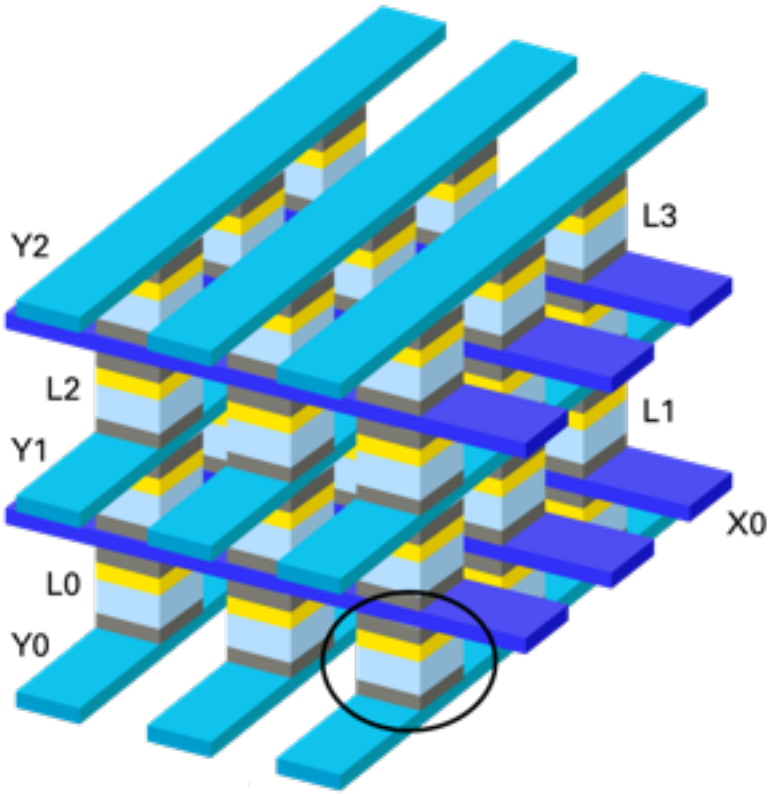

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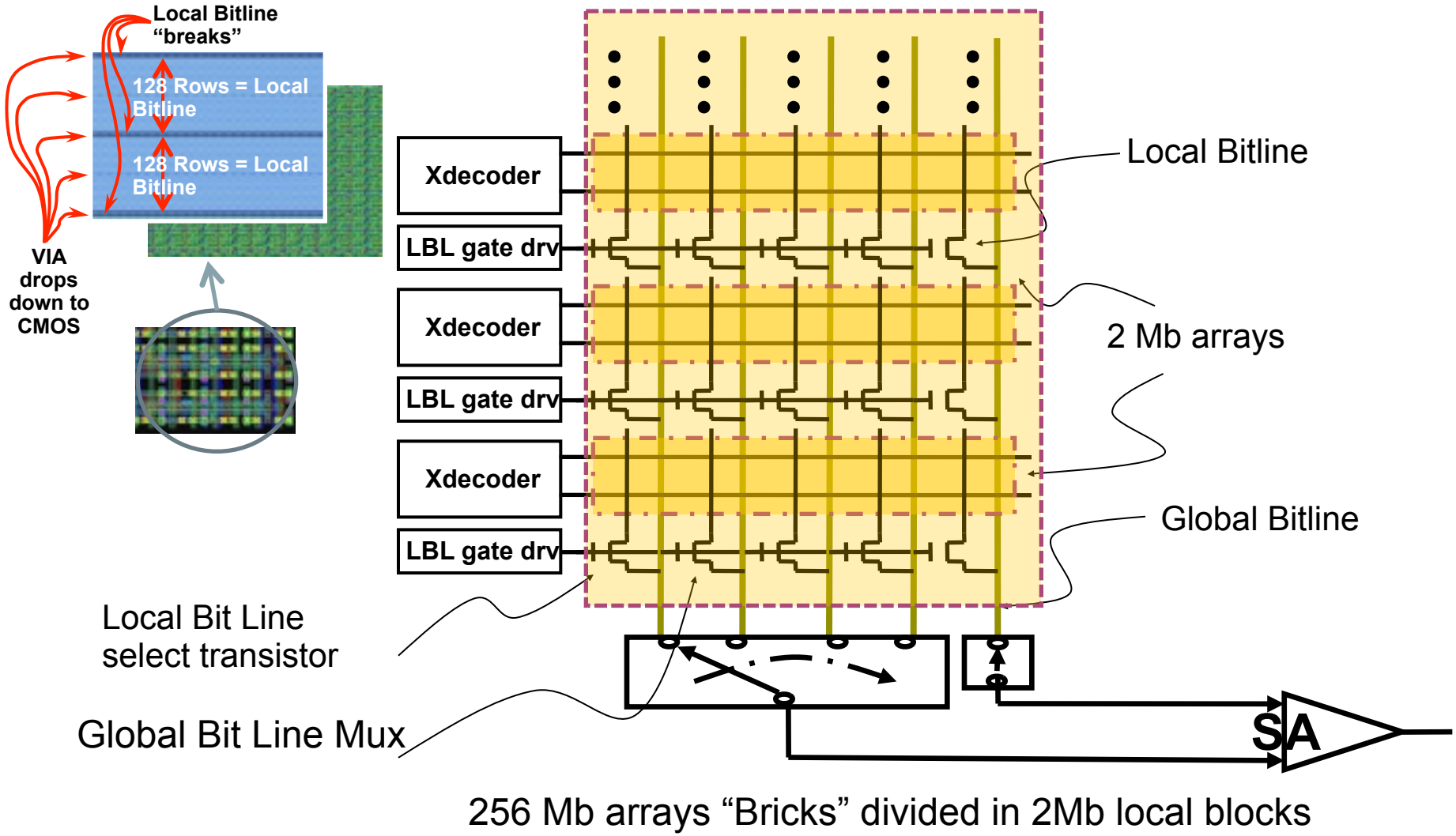
Cross Point Arrays can achieve high read and write bandwidth in high density memories

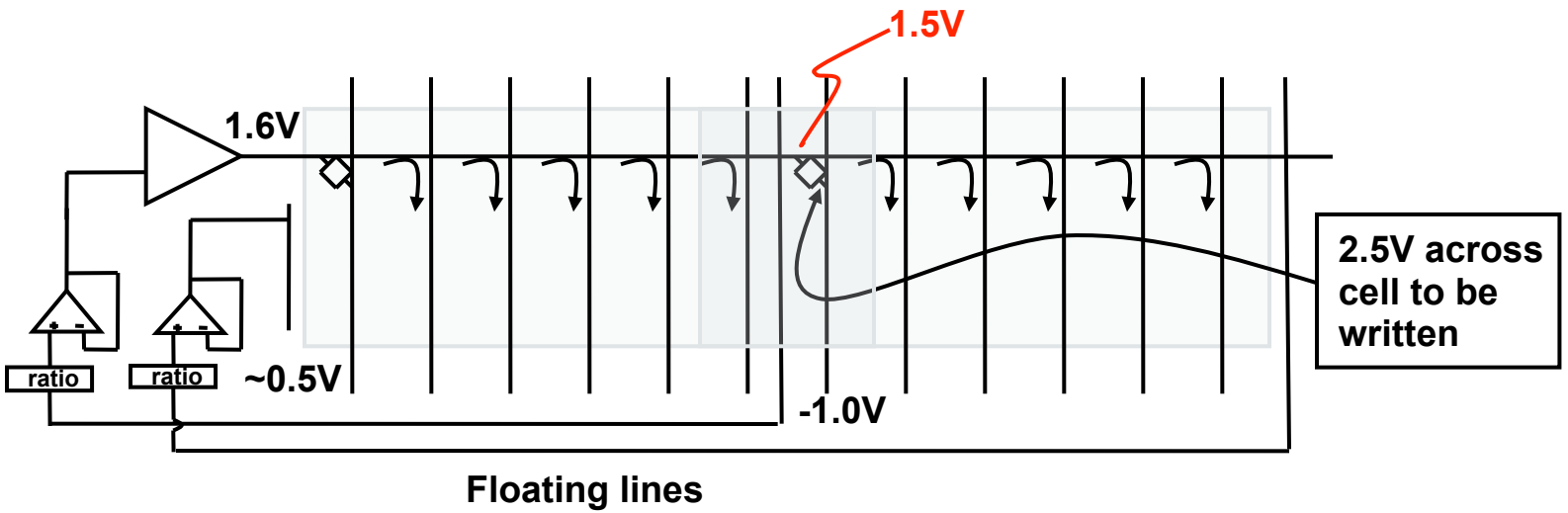
- Techniques:
  - Hierarchical Bit Line structure
  - IR drop compensation
  - Low current cell
  - Gain Stage Sensing
  - Parallelism

- Impact:
  - Improved read / write throughput
  - Improved read latency

Local Bitline Architecture



Row IR Drop with ΔV and location compensation, plus counter bias



- Adjust Driver voltage depending on location of cells being programmed
- Added bias on unselected Word Lines will bias unselected Bit Lines
- Total Word Line current around 100 uA

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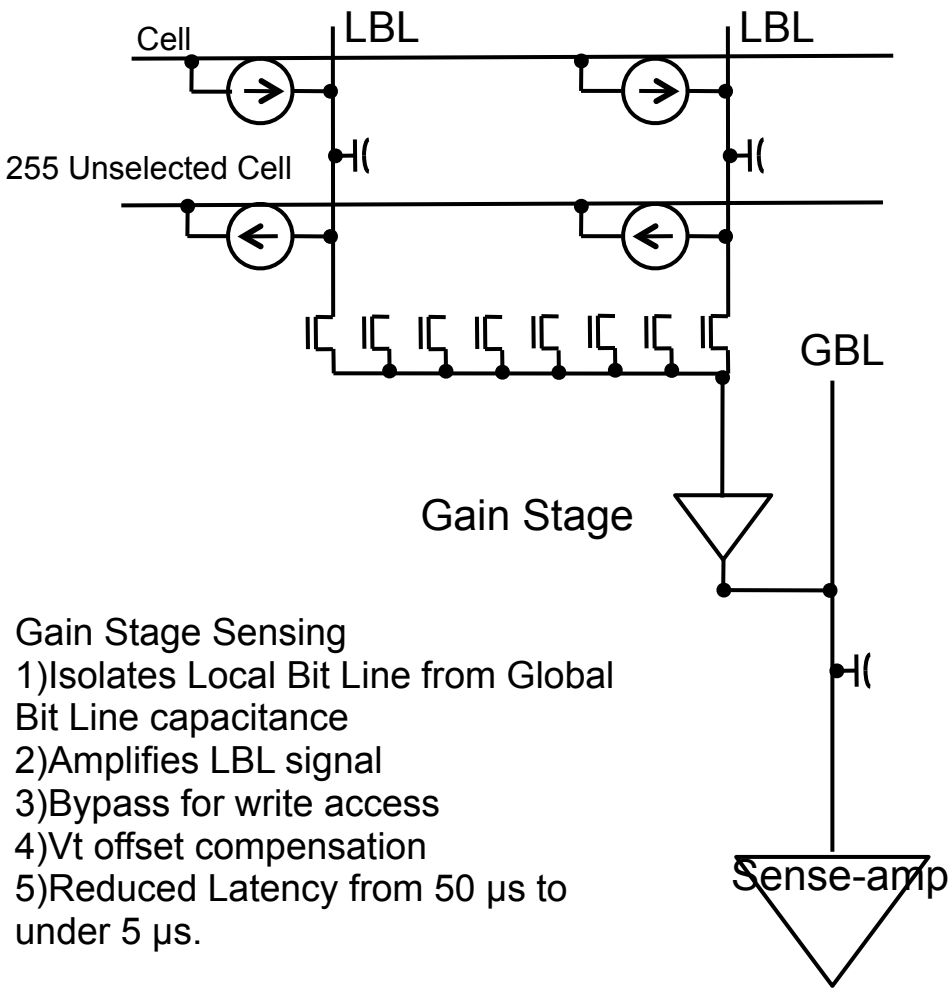
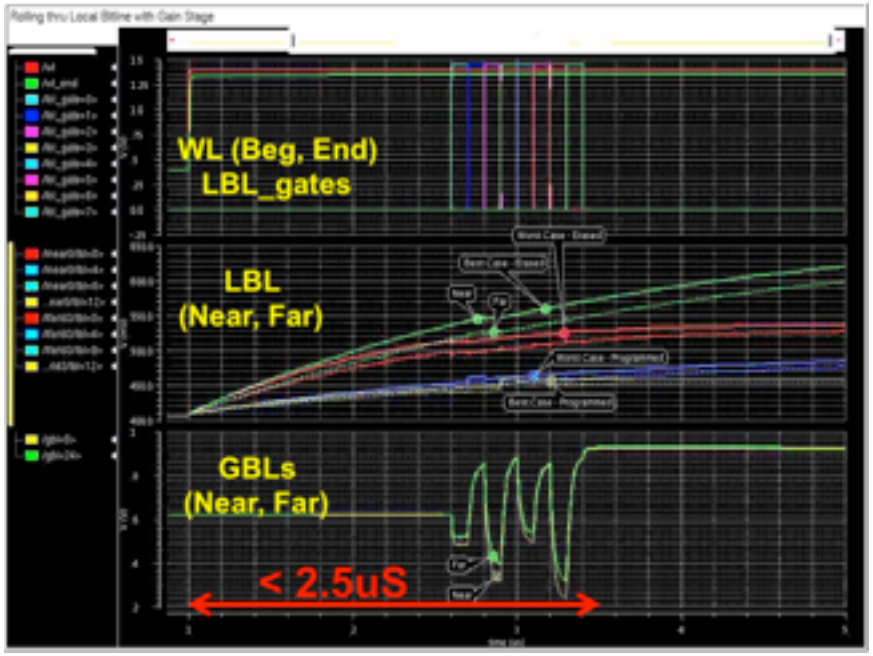
Latency - constrained by sensing

Small array ➔ shorter latency

Low current ➔ longer latency





Gain Stage Sensing
1)Isolates Local Bit Line from Global Bit Line capacitance
2)Amplifies LBL signal
3)Bypass for write access
4)Vt offset compensation
5)Reduced Latency from 50 µs to under 5 µs.

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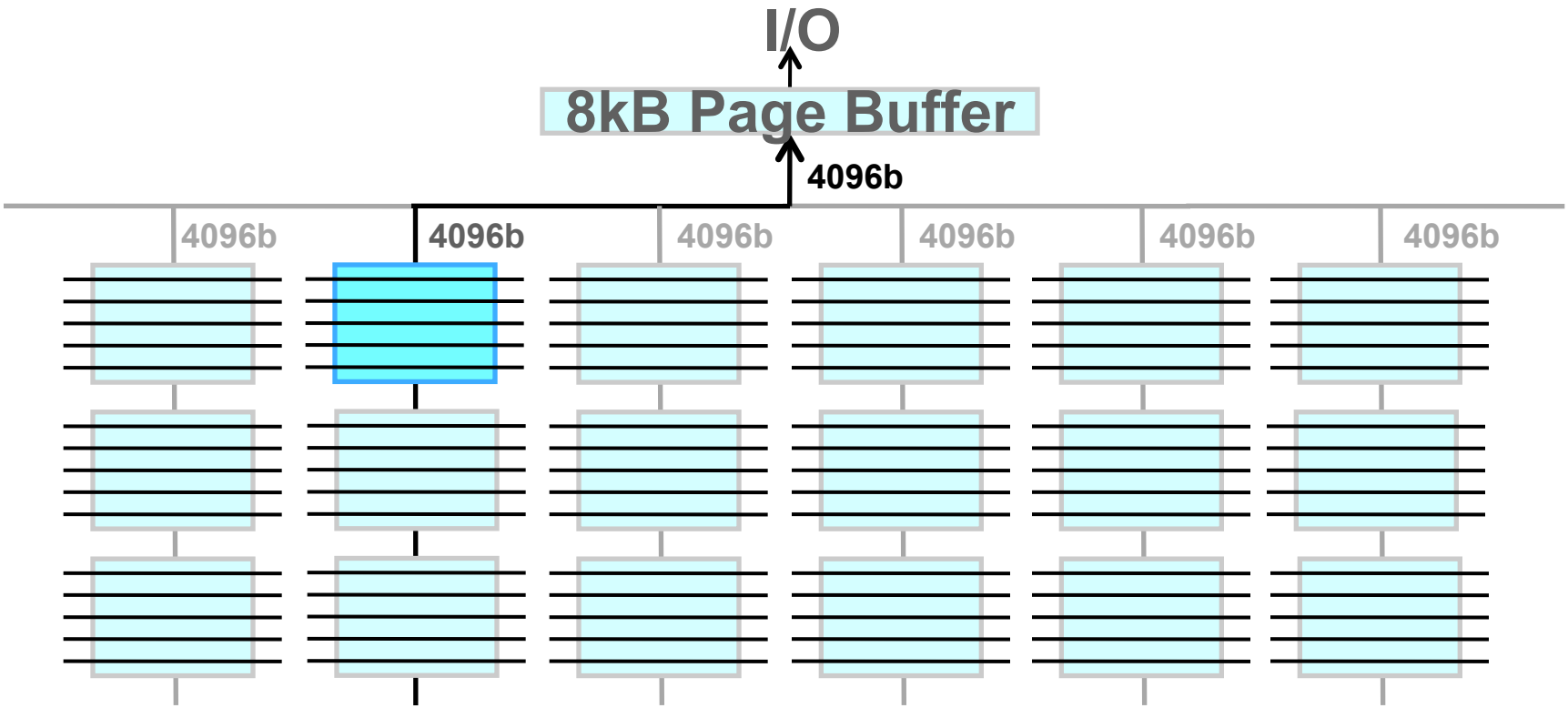
Power and Speed: Single Block Throughput

Read 16 rows in 1 Block to fill page buffer
16x50uS = 800µS → 10MB/sec



= 4096b sub-word read from Tile in one 50us sensing cycle

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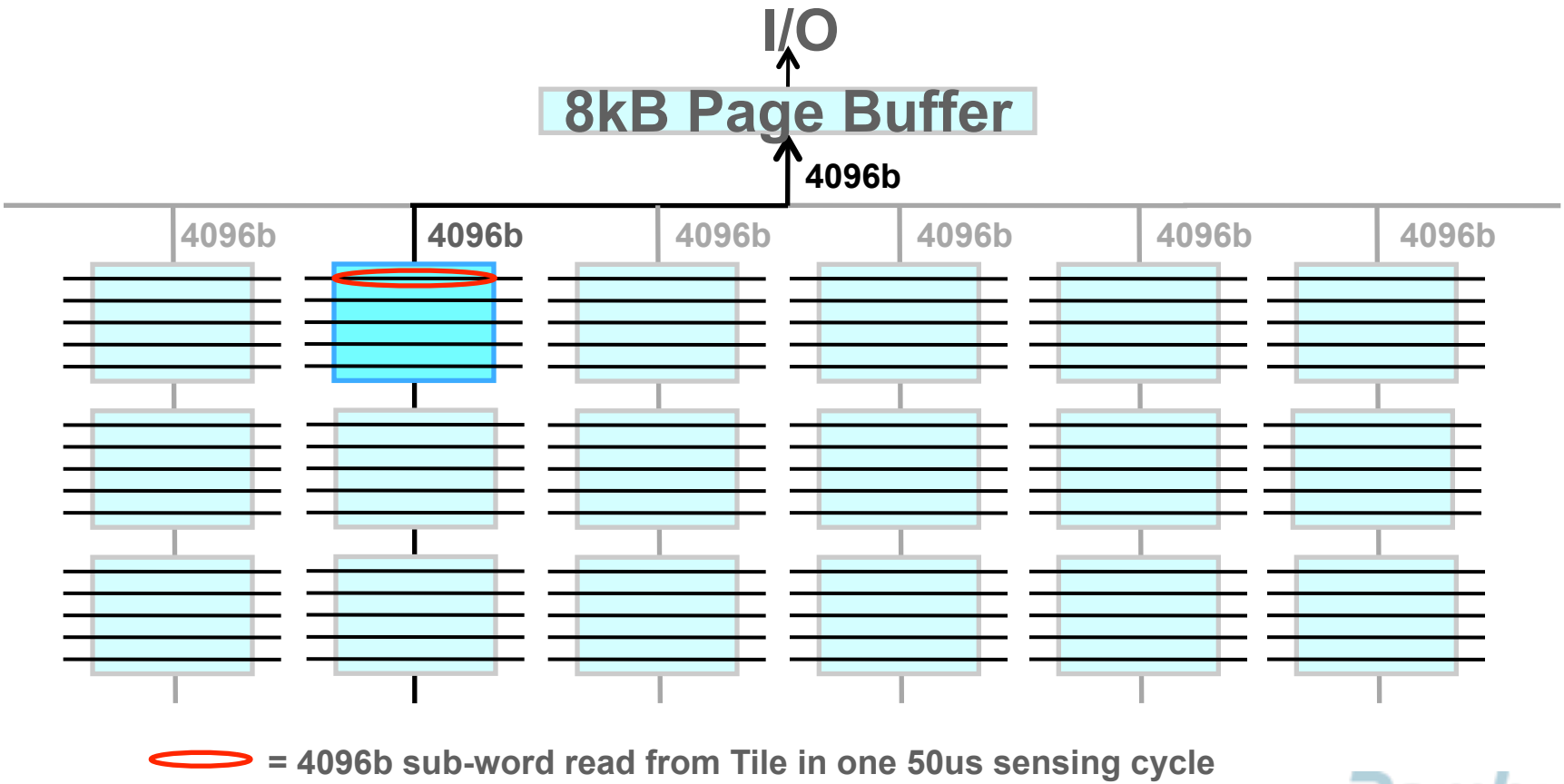

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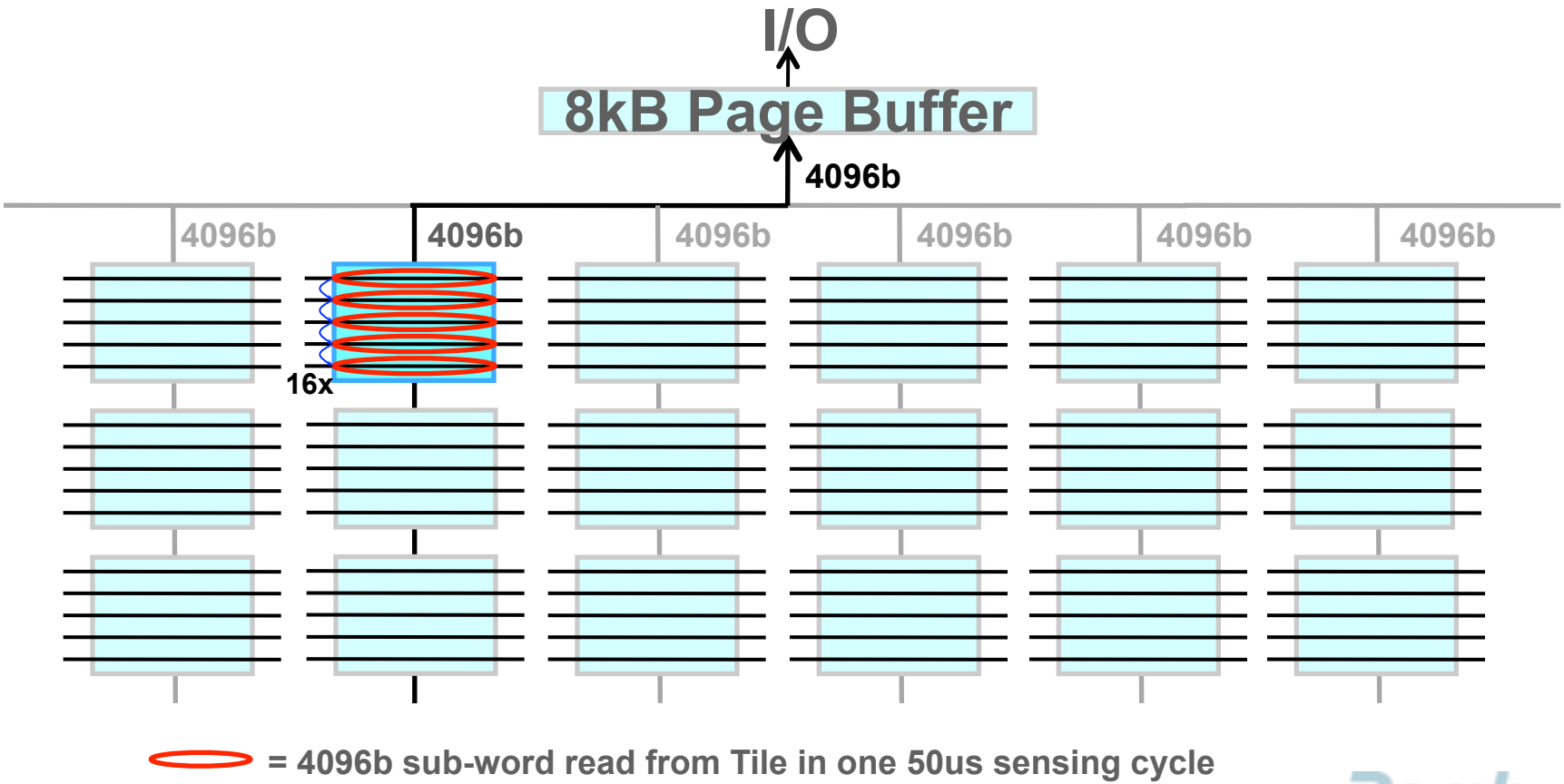

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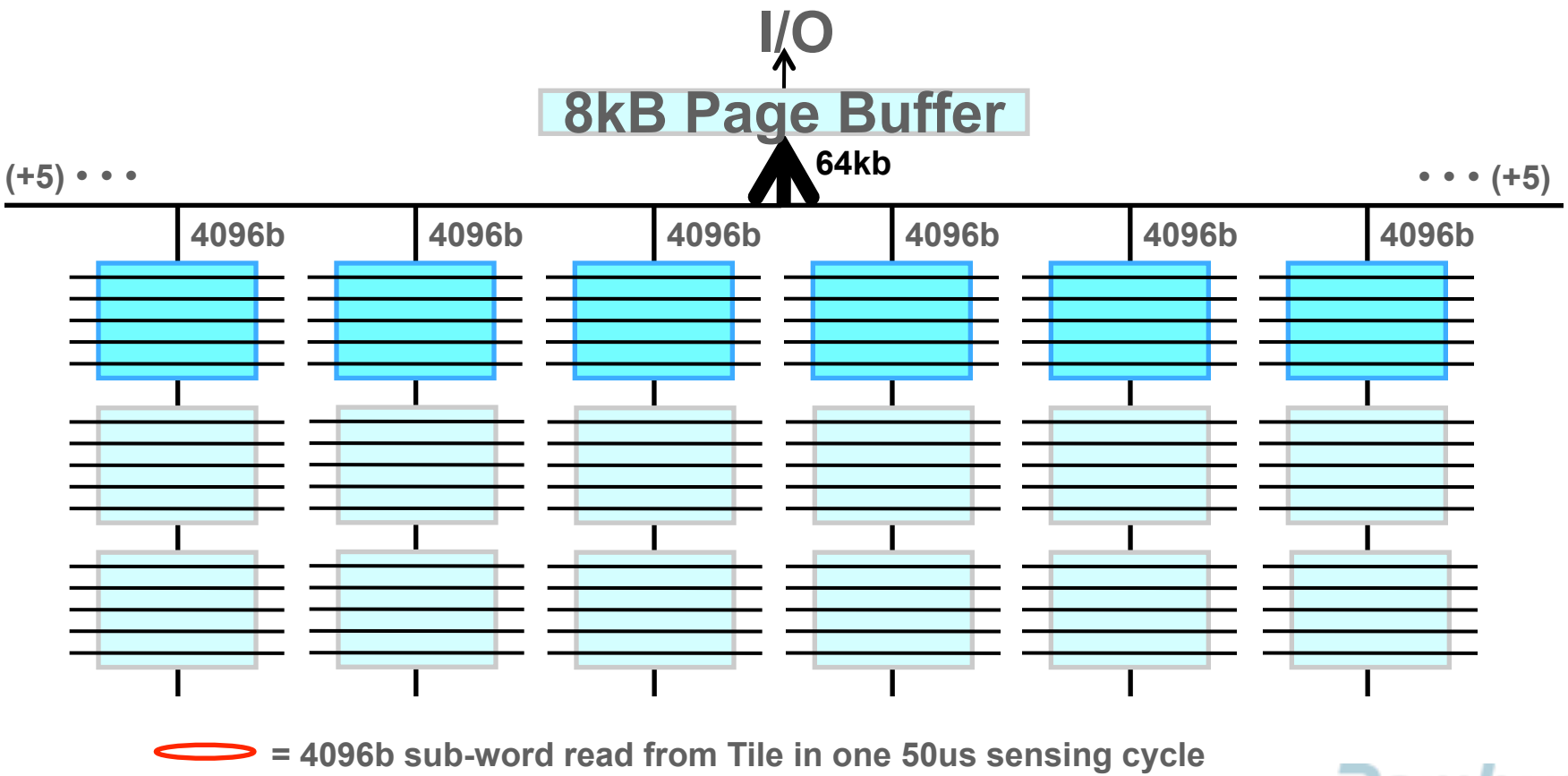
Power and Speed: 16 Block Throughput

Read 1 row in 16 Blocks to fill page buffer
1x50uS = 50uS → 160MB/sec



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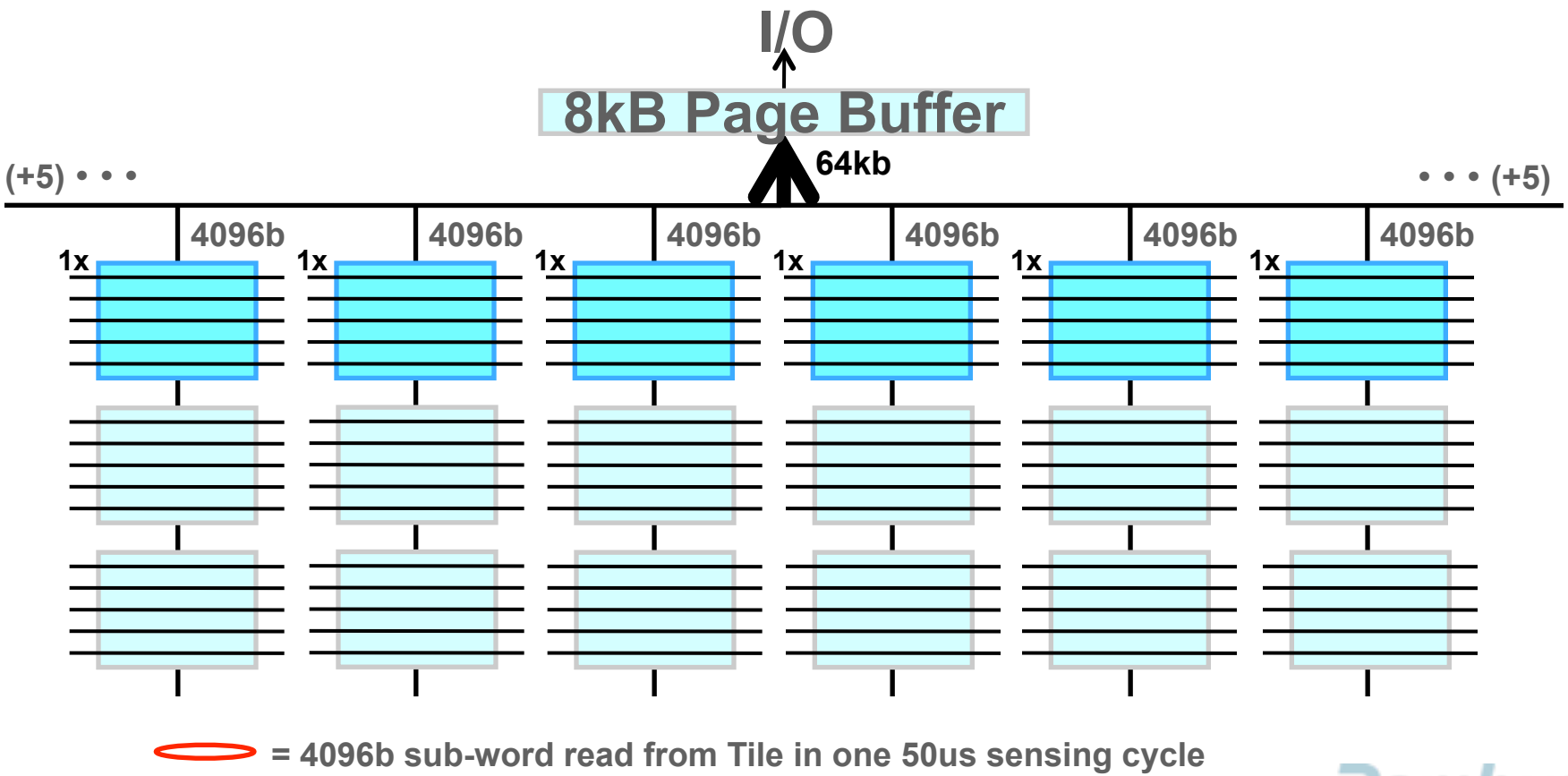

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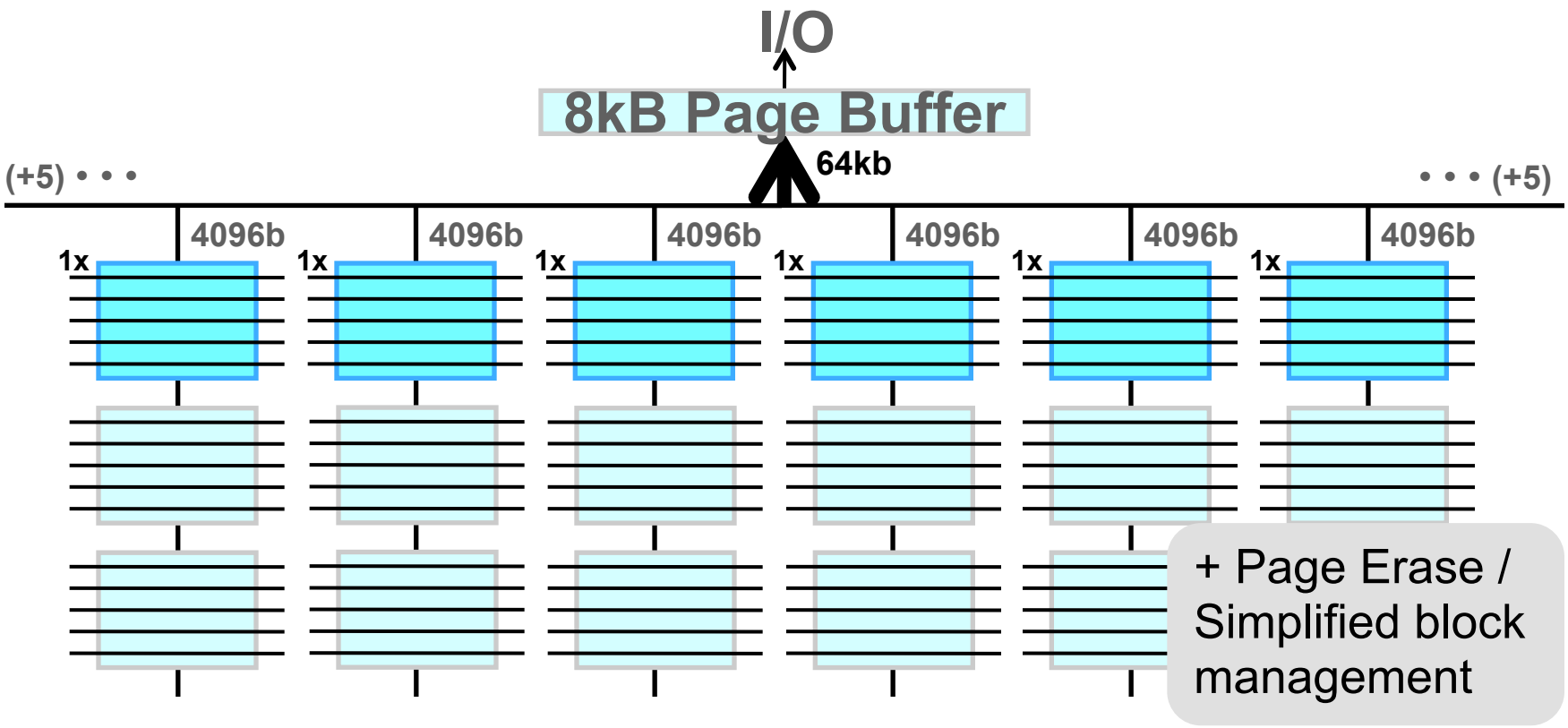

+ Page Erase / Simplified block management

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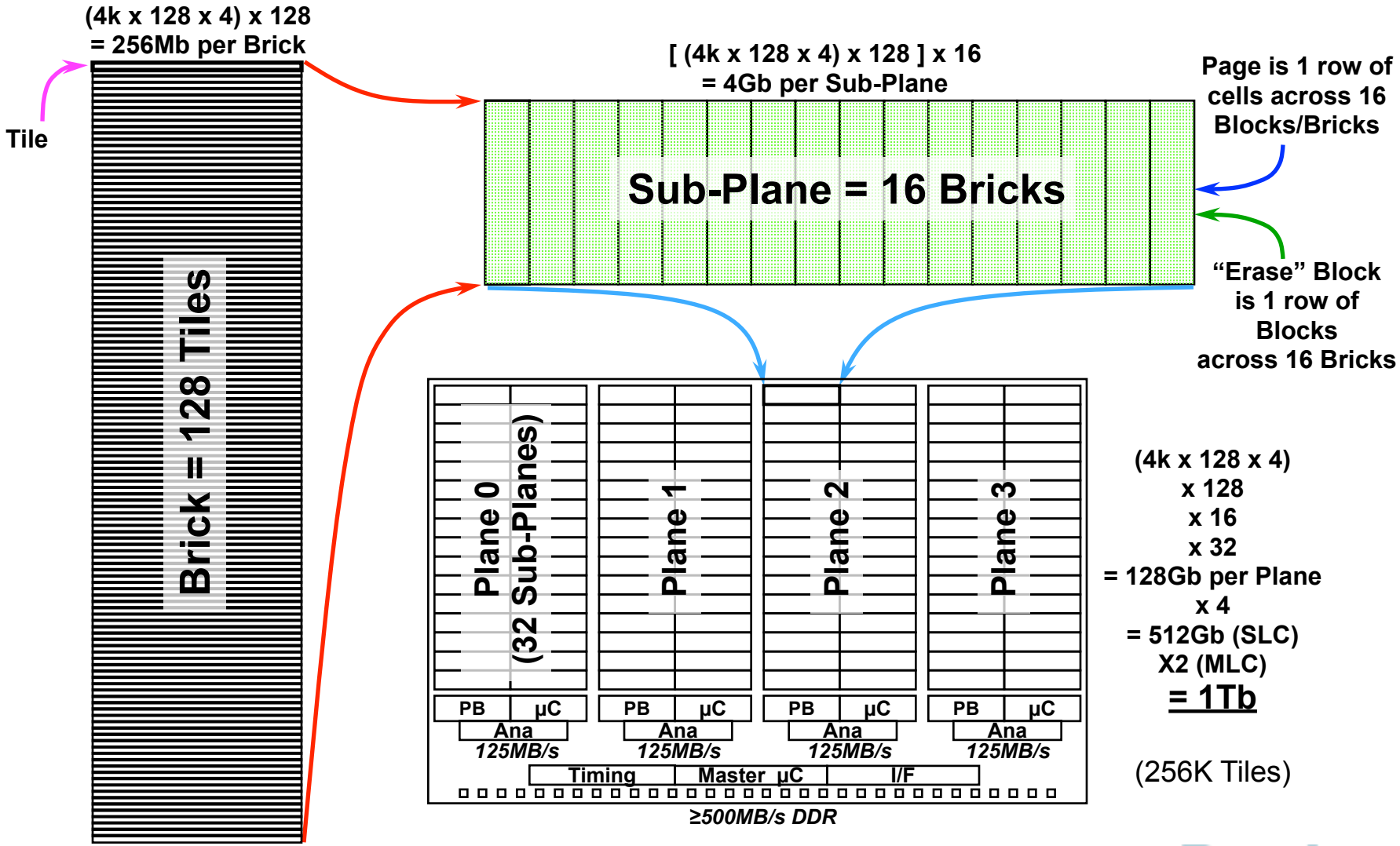
512Gb/1Tb Storage Chip with Multi-Plane Architecture



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Conclusion
from RRAM Cell to System

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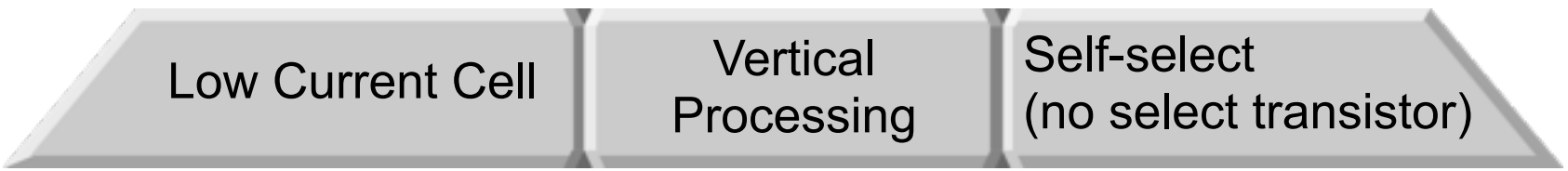

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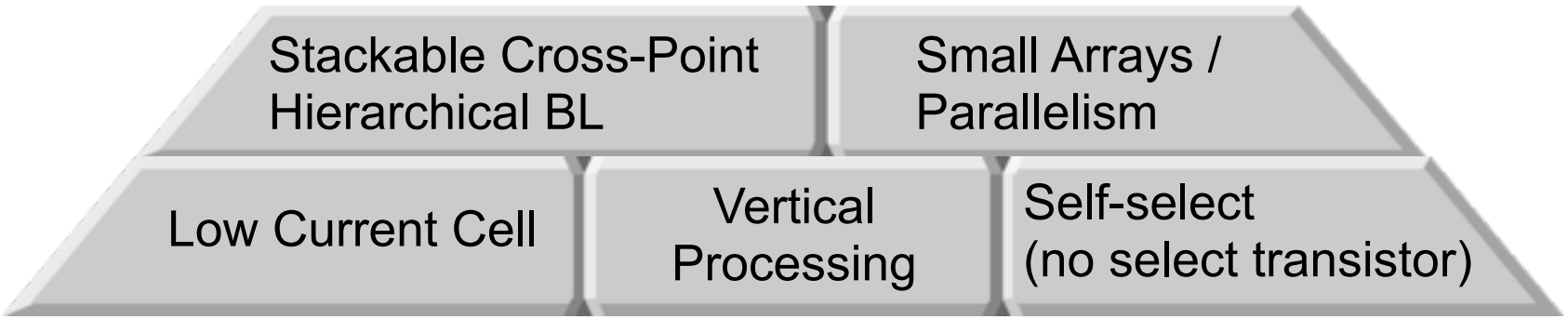

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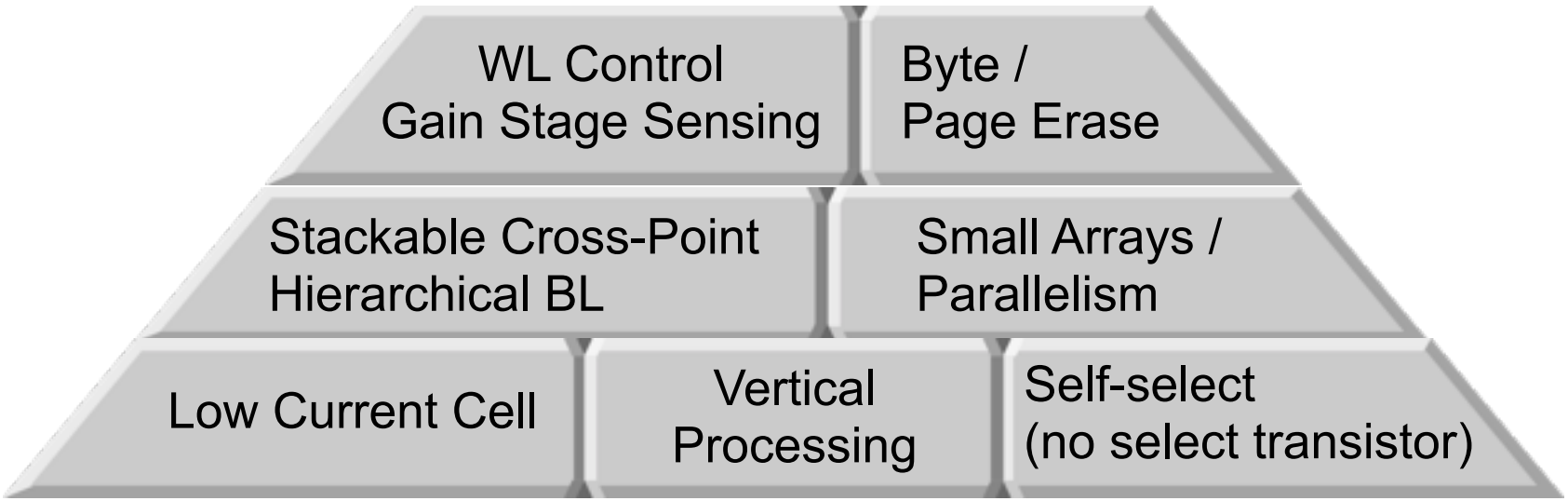

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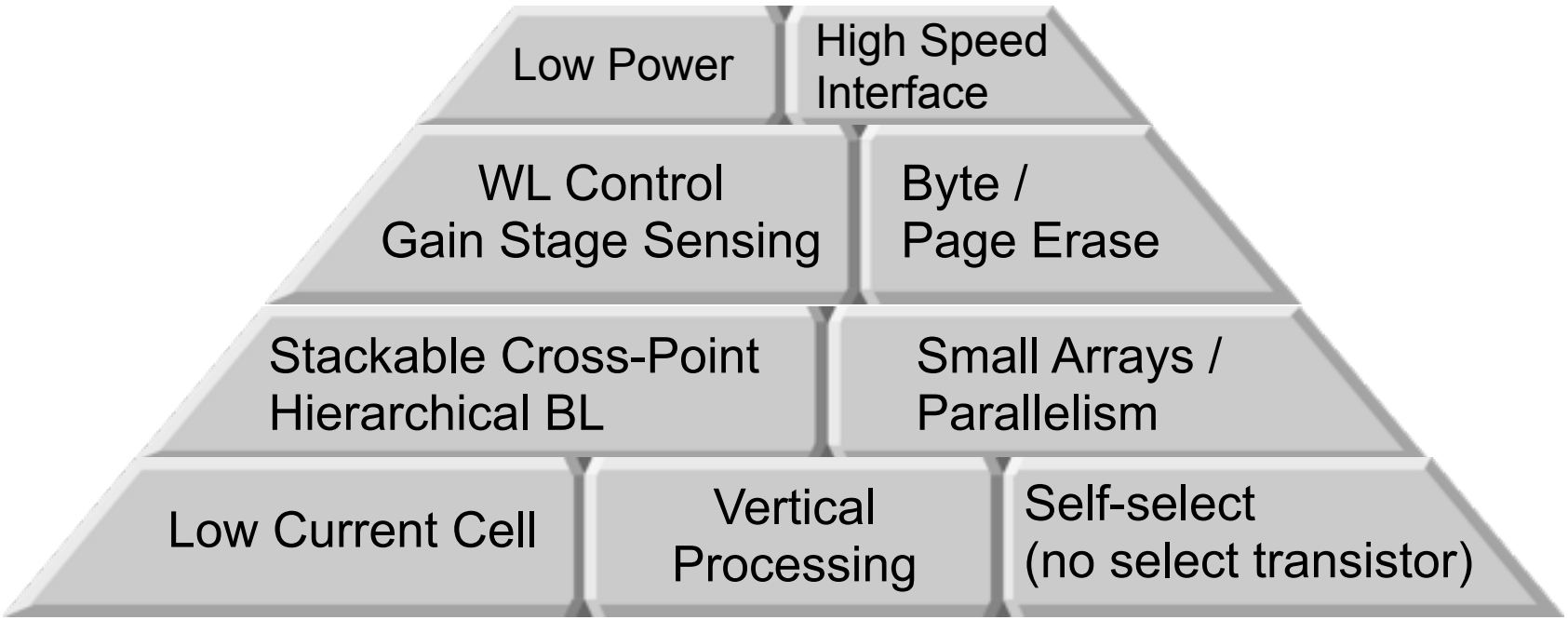

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