IBM Field Engineering Handbook

System/360 Model 30

IBM

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System/360 Model 30

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Endicott, New York 13760

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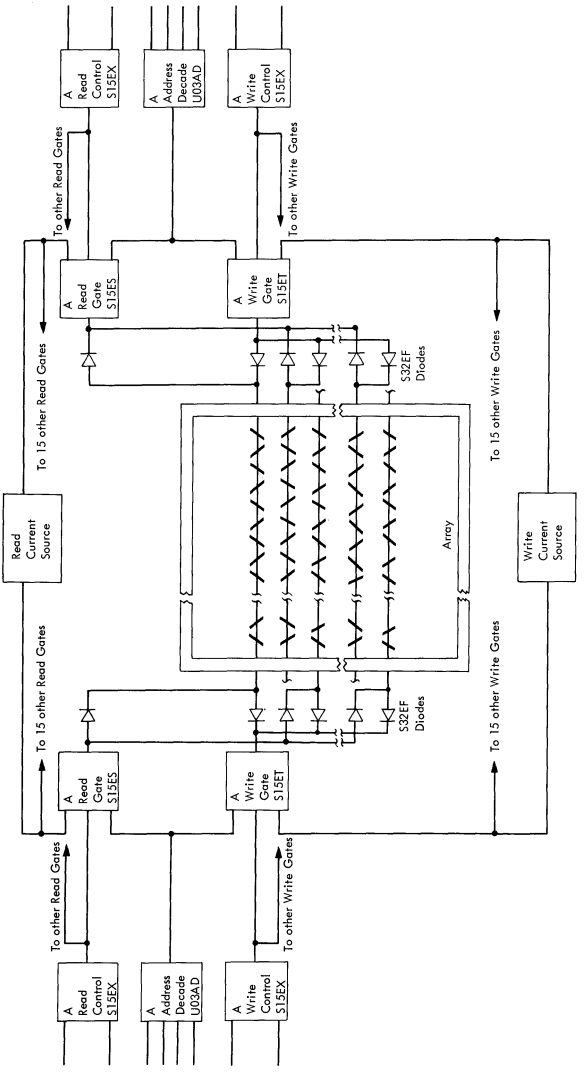
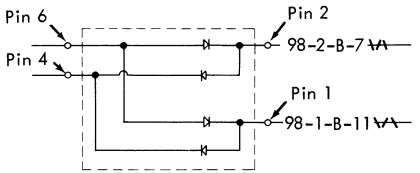

A Read Control S15EX
A Address Decode U03AD
A Write Control S15EX
To other Read Gates
To other Write Gates
A Read Gate S15ES
A Write Gate S15ET
To 15 other Read Gates
To 15 other Write Gates
S32EF Diodes
Read Current Source
Write Current Source
Array

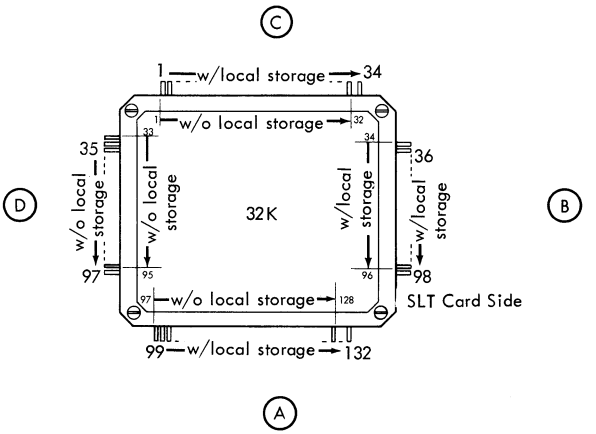
DIODE PACK - P/N 2391181

Schematic - Each diode pack contains 4 diodes connected as follows:



The example shown is taken from MM870 X-Drive Diode Pin # 1.

DIODE LAYOUT - 32K ARRANGEMENT



ORIENTATION OF DIODE PACK (BY DIODE #)

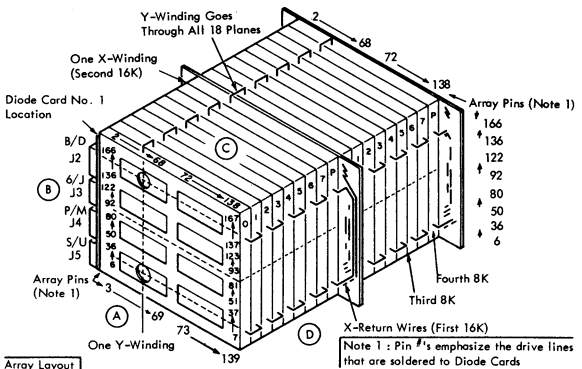
	SIDE A Count Towards Large Card	SIDE B Count Top To Bottom (Evens)	SIDE C Count Towards Large Card	SIDE D Count Top To Bottom (Odds)
Diode Card 1 8/16/32K	99-132	36-98	1-34	35-97
Diode Card 1 32K W/O Local	97-128	34-96	1-32	33-95
Diode Card 2 8/16K	35-68	None	1-34	None
Diode Card 2 32K	99-132	36-98	1-34	35-97
Diode Card 2 32K W/O Local	97-128	34-96	1-32	33-95

POWER RESISTOR LOCATION

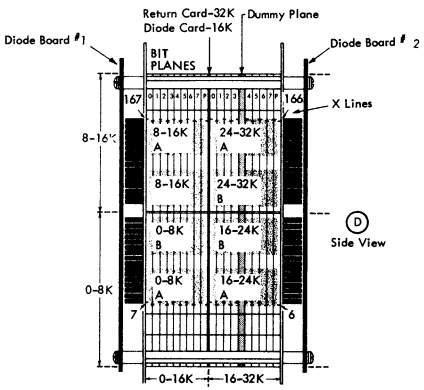
TOP OF FRAME

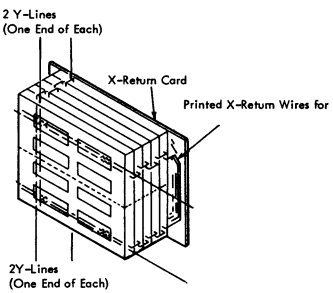
A	0 Bit		I
	1 Bit		N
	2 Bit		H
	6 Bit	0-16K	I
	7 Bit		B
	P Bit		I
	0 Bit		T
	1 Bit		
	2 Bit	16-32K	R
	3 Bit		E
	4 Bit		S
B	3 Bit		I
	4 Bit	0-16K	S
	5 Bit		T
	5 Bit		O
	6 Bit	16-32K	R
	7 Bit		S
C	P Bit		
	Y Read		X-Y
	Y Write		DRIVE
	X Read 8/24K		
	X Write 16/32K		

BOTTOM OF FRAME



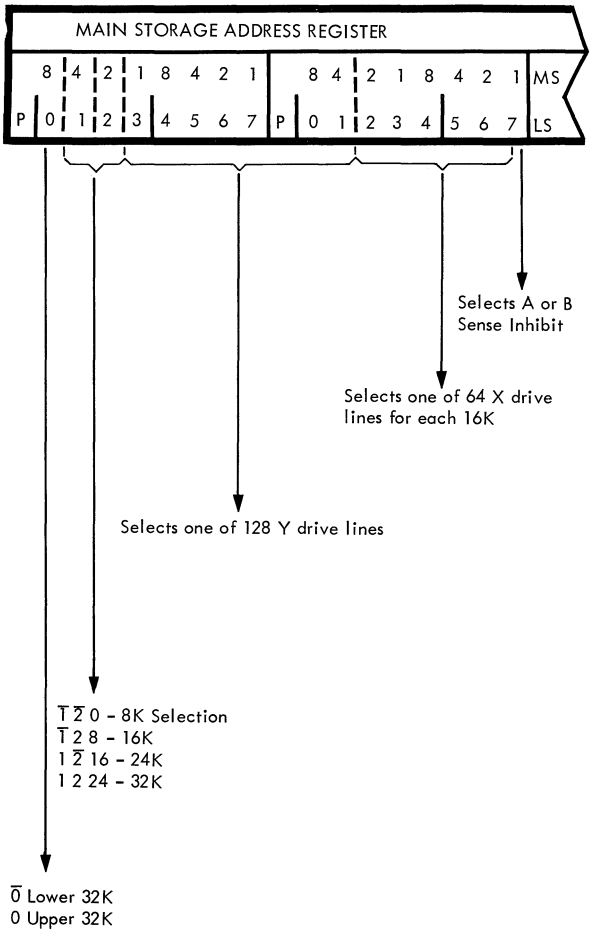
Array Layout



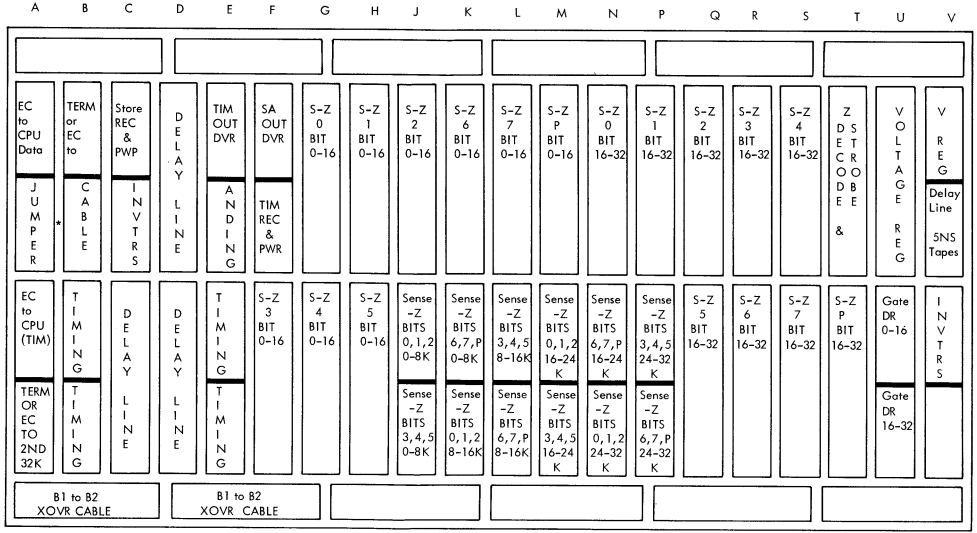


8K Array

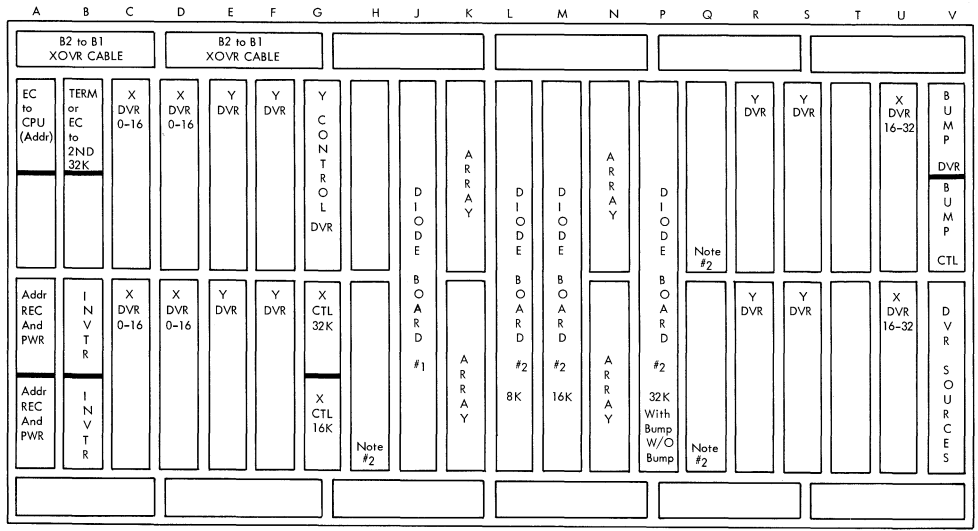
MAIN STORAGE ADDRESS REGISTER LAYOUT (M & N)



NOTES: 1. B1B2 and B1A5 Sockets have 5803577 Installed if Memory is Highest Addressable CSU, Otherwise these Sockets are used for Intermemory Cable Chaining.
2. *Denotes Cable 5802515 Installed on 8, 16, 32K, or 1st 32K But Not 2nd 32K.



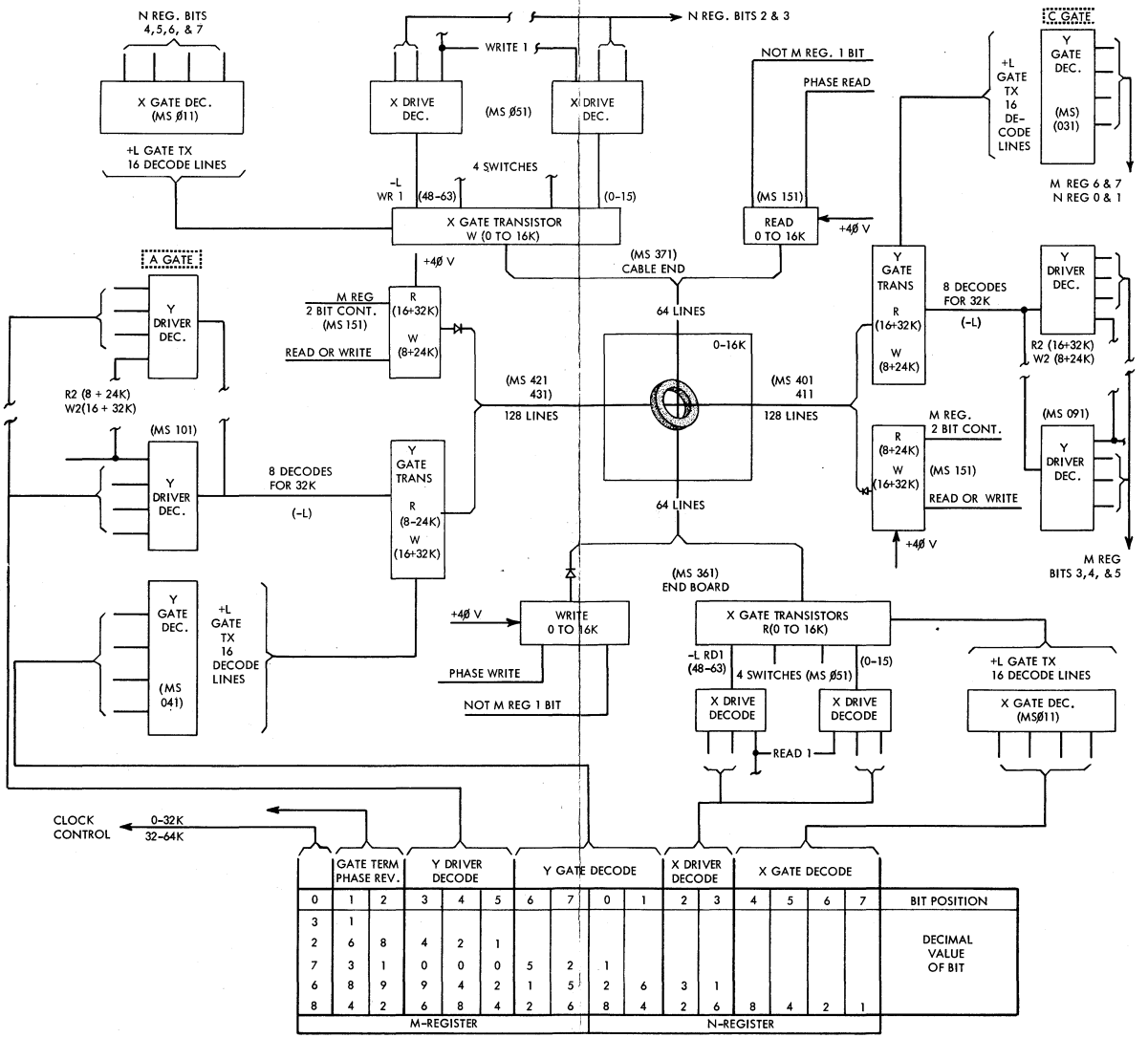
NOTES: 1. B2B2 Socket has 5803577 Installed if Memory is Highest Addressable CSU, Otherwise This Socket is Used for Intermemory Cable Chaining.
2. These Sockets Not Available for Cards.



PLUG CHART - B2 BOARD

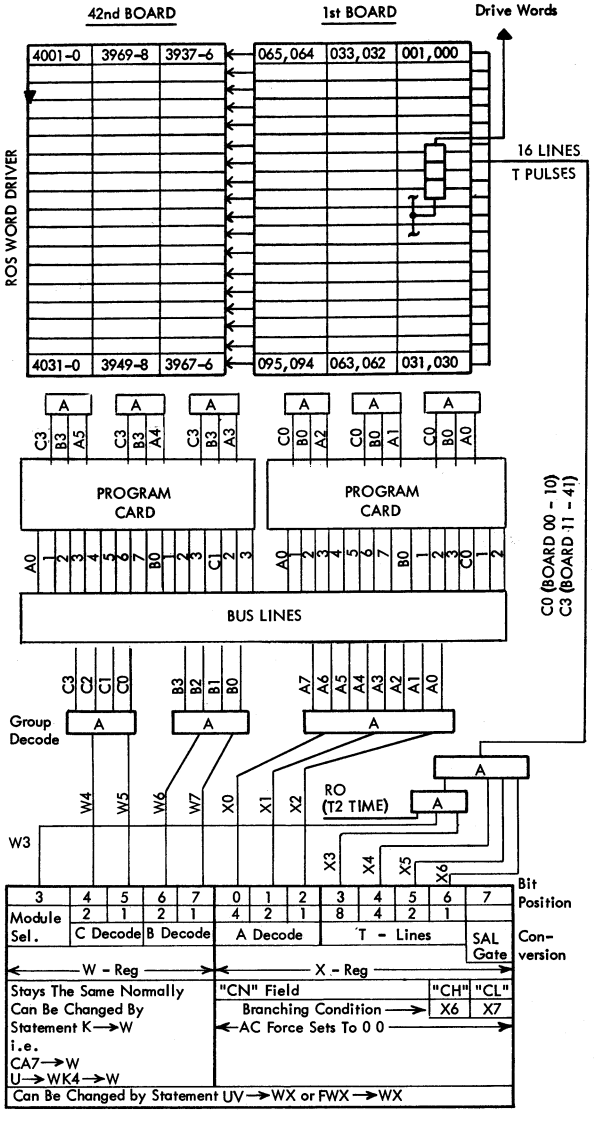
NOTES

MAIN STORAGE ADDRESSING
2 MICRO-SECOND MEMORY



	GATE TERM PHASE REV.		Y DRIVER DECODE			Y GATE DECODE				X DRIVER DECODE		X GATE DECODE				BIT POSITION
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
3	1															
2	6	8	4	2	1											DECIMAL VALUE OF BIT
7	3	1	0	0	0	5	2	1								
6	8	9	9	4	2	1	5	2	6	3	1					
8	4	2	6	8	4	2	6	8	4	2	6	8	4	2	1	
M-REGISTER								N-REGISTER								

ROS ADDRESSING BLOCK DIAGRAM



ROS ADDRESSING - CARD POSITIONS

EVEN				ODD				EVEN				ODD			
Bd. No.		Pos.	Hex	Bd. No.		Pos.	Hex	Bd. No.		Pos.	Hex	Bd. No.		Pos.	Hex
0	-	0	000	0	-	1	001	11	-	0	420	11	-	1	421
		2	018			3	019			2	438			3	439
		4	030			5	031			4	450			5	451
		6	048			7	049			6	468			7	469
1	-	0	060	1	-	1	061	12	-	0	480	12	-	1	481
		2	078			3	079			2	498			3	499
		4	090			5	091			4	4B0			5	4B1
		6	0A8			7	0A9			6	4C8			7	4C9
2	-	0	0C0	2	-	1	0C1	13	-	0	4E0	13	-	1	4E1
		2	0D8			3	0D9			2	4F8			3	4F9
		4	0F0			5	0F1			4	510			5	511
		6	108			7	109			6	528			7	529
3	-	0	120	3	-	1	121	14	-	0	540	14	-	1	541
		2	138			3	139			2	558			3	559
		4	150			5	151			4	570			5	571
		6	168			7	169			6	588			7	589
4	-	0	180	4	-	1	181	15	-	0	5A0	15	-	1	5A1
		2	198			3	199			2	5B8			3	5B9
		4	1B0			5	1B1			4	5D0			5	5D1
		6	1C8			7	1C9			6	5E8			7	5E9
5	-	0	1E0	5	-	1	1E1	16	-	0	600	16	-	1	601
		2	1F8			3	1F9			2	618			3	619
		4	210			5	211			4	630			5	631
		6	228			7	229			6	648			7	649
6	-	0	240	6	-	1	241	17	-	0	660	17	-	1	661
		2	258			3	259			2	678			3	679
		4	270			5	271			4	690			5	691
		6	288			7	289			6	6A8			7	6A9
7	-	0	2A0	7	-	1	2A1	18	-	0	6C0	18	-	1	6C1
		2	2B8			3	2B9			2	6D8			3	6D9
		4	2D0			5	2D1			4	6F0			5	6F1
		6	2E8			7	2E9			6	708			7	709
8	-	0	300	8	-	1	301	19	-	0	720	19	-	1	721
		2	318			3	319			2	738			3	739
		4	330			5	331			4	750			5	751
		6	348			7	349			6	768			7	769
9	-	0	360	9	-	1	361	20	-	0	780	20	-	1	781
		2	378			3	379			2	798			3	799
		4	390			5	391			4	7B0			5	7B1
		6	3A8			7	3A9			6	7C8			7	7C9
10	-	0	3C0	10	-	1	3C1	21	-	0	7E0	21	-	1	7E1
		2	3D8			3	3D9			2	7F8			3	7F9
		4	3F0			5	3F1			4	810			5	811
		6	408			7	409			6	828			7	829

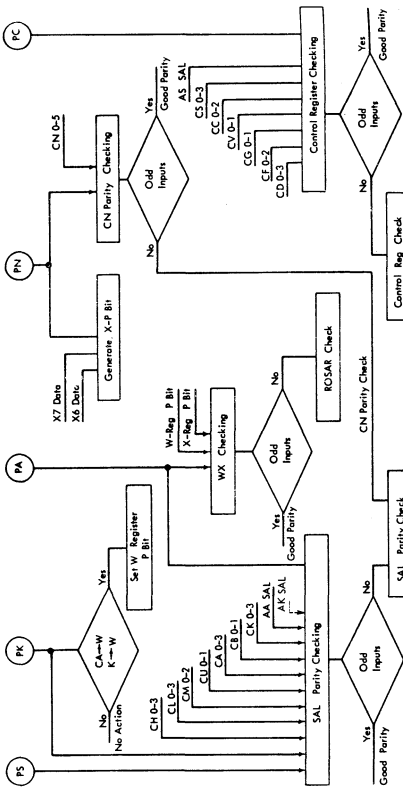
EVEN			ODD			EVEN			ODD		
Bd. No.	Pos.	Hex	Bd. No.	Pos.	Hex	Bd. No.	Pos.	Hex	Bd. No.	Pos.	Hex
22	0	840	22	1	841	32	0	C00	32	1	C01
	2	858		3	859		2	C18		3	C19
	4	870		5	871		4	C30		5	C31
	6	888		7	889		6	C48		7	C49
23	0	8A0	23	1	8A1	33	0	C60	33	1	C61
	2	8B8		3	8B9		2	C78		3	C79
	4	8D0		5	8D1		4	C90		5	C91
	6	8E8		7	8E9		6	CA8		7	CA9
24	0	900	24	1	901	34	0	CC0	34	1	CC1
	2	918		3	919		2	CD8		3	CD9
	4	930		5	931		4	CF0		5	CF1
	6	948		7	949		6	D08		7	D09
25	0	960	25	1	961	35	0	D20	35	1	D21
	2	978		3	979		2	D38		3	D39
	4	990		5	991		4	D50		5	D51
	6	9A8		7	9A9		6	D68		7	D69
26	0	9C0	26	1	9C1	36	0	D80	36	1	D81
	2	9D8		3	9D9		2	D98		3	D99
	4	9F0		5	9F1		4	DB0		5	DB1
	6	A08		7	A09		6	DC8		7	DC9
27	0	A20	27	1	A21	37	0	DE0	37	1	DE1
	2	A38		3	A39		2	DF8		3	DF9
	4	A50		5	A51		4	E10		5	E11
	6	A68		7	A69		6	E28		7	E29
28	0	A80	28	1	A81	38	0	E40	38	1	E41
	2	A98		3	A99		2	E58		3	E59
	4	AB0		5	AB1		4	E70		5	E71
	6	AC8		7	AC9		6	E88		7	E89
29	0	AE0	29	1	AE1	39	0	EA0	39	1	EA1
	2	AF8		3	AF9		2	EB8		3	EB9
	4	B10		5	B11		4	ED0		5	ED1
	6	B28		7	B29		6	EE8		7	EE9
30	0	B40	30	1	B41	40	0	F00	40	1	F01
	2	B58		3	B59		2	F18		3	F19
	4	B70		5	B71		4	F30		5	F31
	6	B88		7	B89		6	F48		7	F49
31	0	BA0	31	1	BA1	41	0	F60	41	1	F61
	2	BB8		3	BB9		2	F78		3	F79
	4	BD0		5	BD1		4	F90		5	F91
	6	BE8		7	BE9		6	FA8		7	FA9

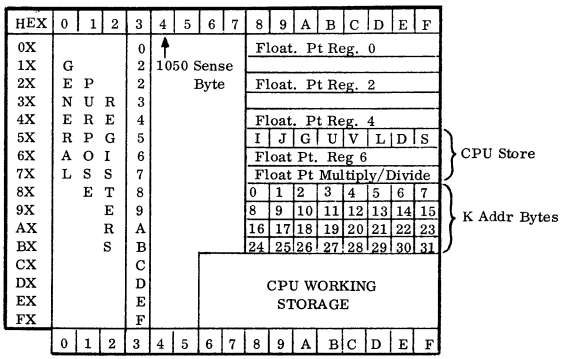
The chart indicates the first word on the document card. The ROS Card location of any word can be found by using this chart.

EXAMPLE: 500 = Board 13 Card 2 615 = Board 16 Card 1

This chart also applies to compatibility, add 50 to Board #.

EXAMPLE: Board #66 is equal to Board 16.


PC
PN
PA
PK
PS
CN 0-5
CN Parity Checking
Odd Inputs
Yes
Good Parity
No
AS SAL
CS 0-3
CC 0-2
CV 0-1
CG 0-1
CF 0-2
CD 0-3
Control Register Checking
Yes
Good Parity
Odd Inputs
No
Control Reg Check
X7 Data
X6 Data
Generate X-P Bit
W-Reg P Bit
X-Reg P Bit
WX Checking
Odd Inputs
No
ROSAR Check
Yes
Good Parity
CN Parity Check
Set W Register P Bit
Yes
CA—W
K—W
No
No Action
CH 0-3
CL 0-3
CM 0-2
CU 0-1
CA 0-3
CB 0-1
CK 0-3
AA SAL
AK SAL
SAL Parity Checking
Odd Inputs
No
SAL Parity Check
Yes
Good Parity

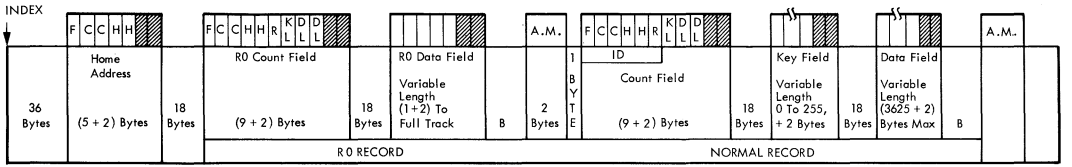


FORMAT FOR K ADDRESSABLE BYTES

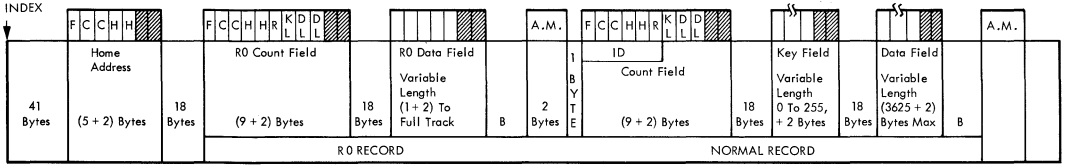
Ø	1	2	3	4	5	6	7	BITS
1	Ø	CNØ	KØ	1	K1	K2	K3	

(*K→N)

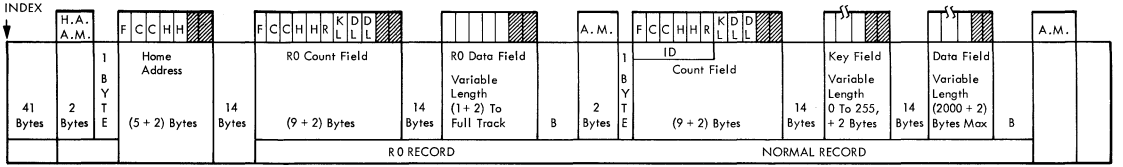
K ADDR	HEX ADDR	USE
Ø	88	MPX Intrp Buffer Unit Address
1	89	MPX T Reg Store
2	8A	MPX R Reg Store
3	8B	MPX Intrp-Buffer Unit Status
4	8C	PSW, Bit, Position 1, and Instruction Length, Pos. 4-7
5	8D	Sel Chan 1 Unit Address
6	8E	Sel Chan 1 Next CCW Addr Hi
7	8F	Sel Chan 1 Next CCW Addr Lo
8	98	MPX Unit Address Temp Storage
9	99	1050 Unit Status
10	9A	CPU Working Storage
↓	↓	
15	9F	
16	A8	Instruction Counter Unavailable
17	A9	Instruction Counter Hi
18	AA	Instruction Counter Lo
19	AB	Unassigned
20	AC	Sel Chan Chaining R Reg. Storage
21	AD	Sel Chan 2 Unit Address
22	AE	Sel Chan 2 Next CCW Addr Hi
23	AF	Sel Chan 2 Next CCW Addr Lo
24	B8	System Mask
25	B9	Prot Key 0-3 and A M W P 4-7
26	BA	Unassigned
27	BB	Condition Reg. 4 PGM Mask
28	BC	Op Code Mask
29	BD	Sel Chan S Reg. Store
30	BE	Sel Chan U Reg. Store
31	BF	Sel Chan V Reg. Store



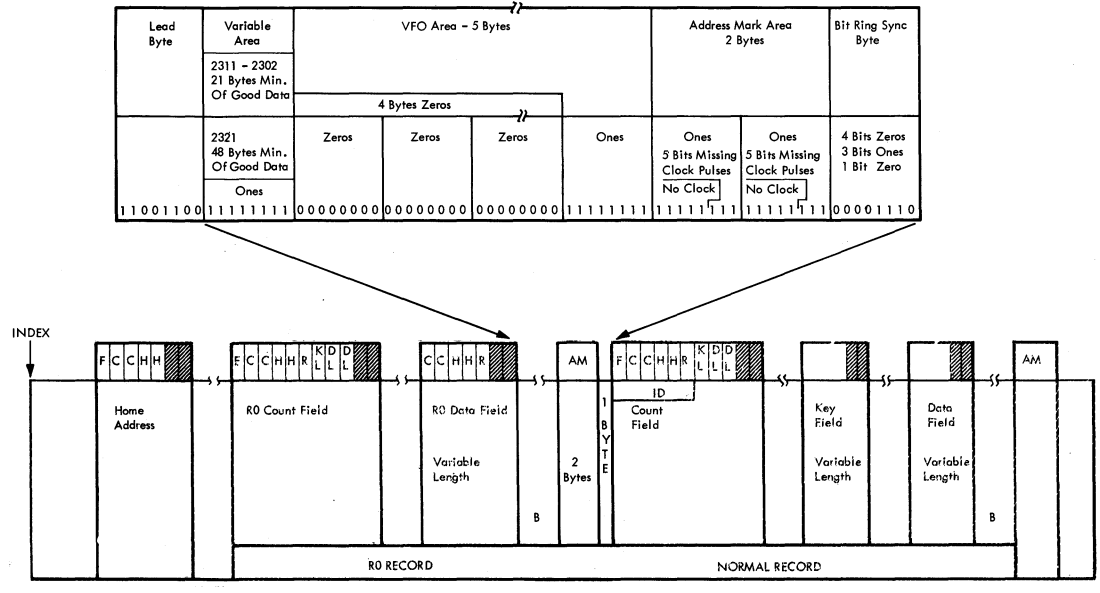
2311



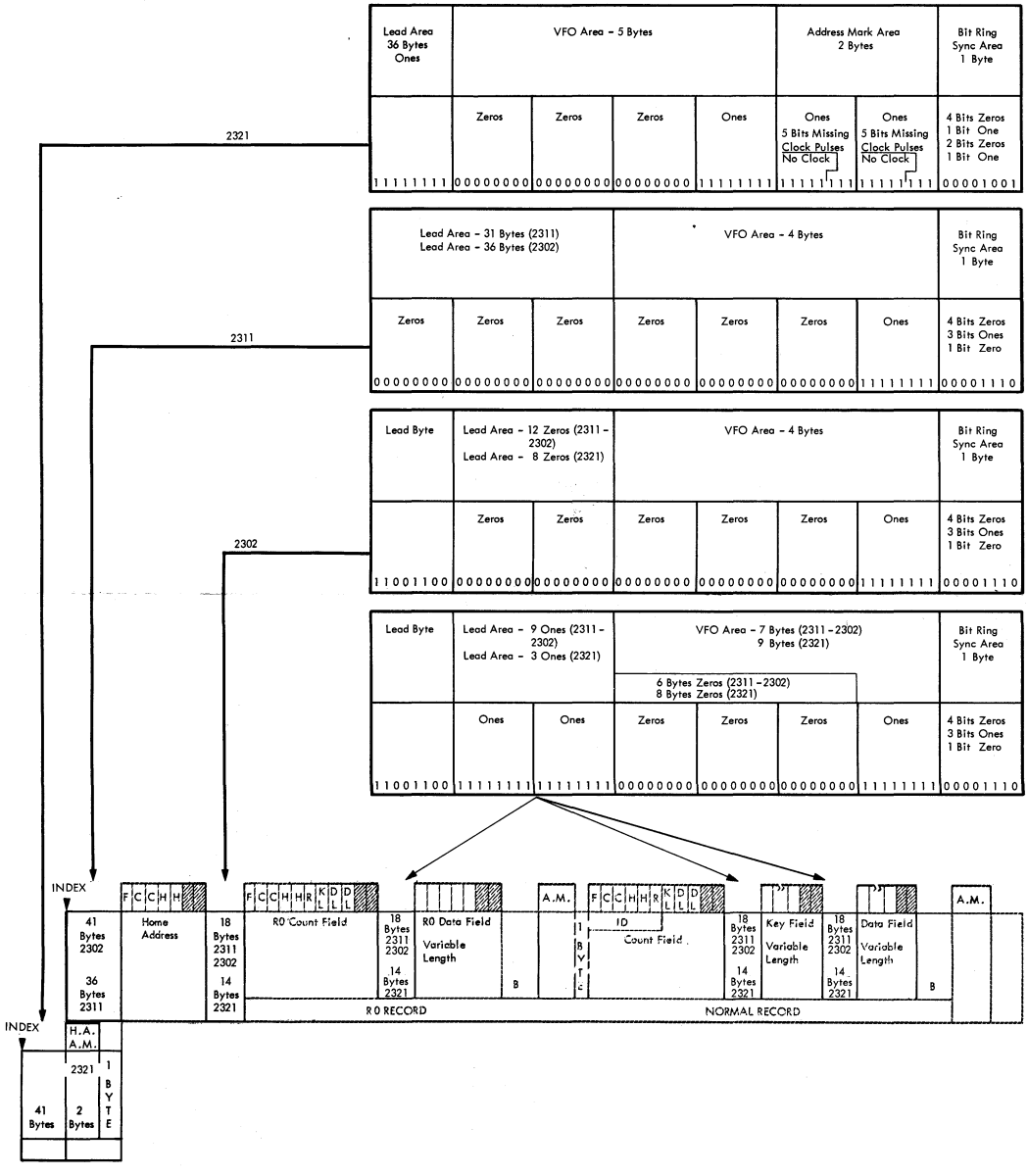
2302



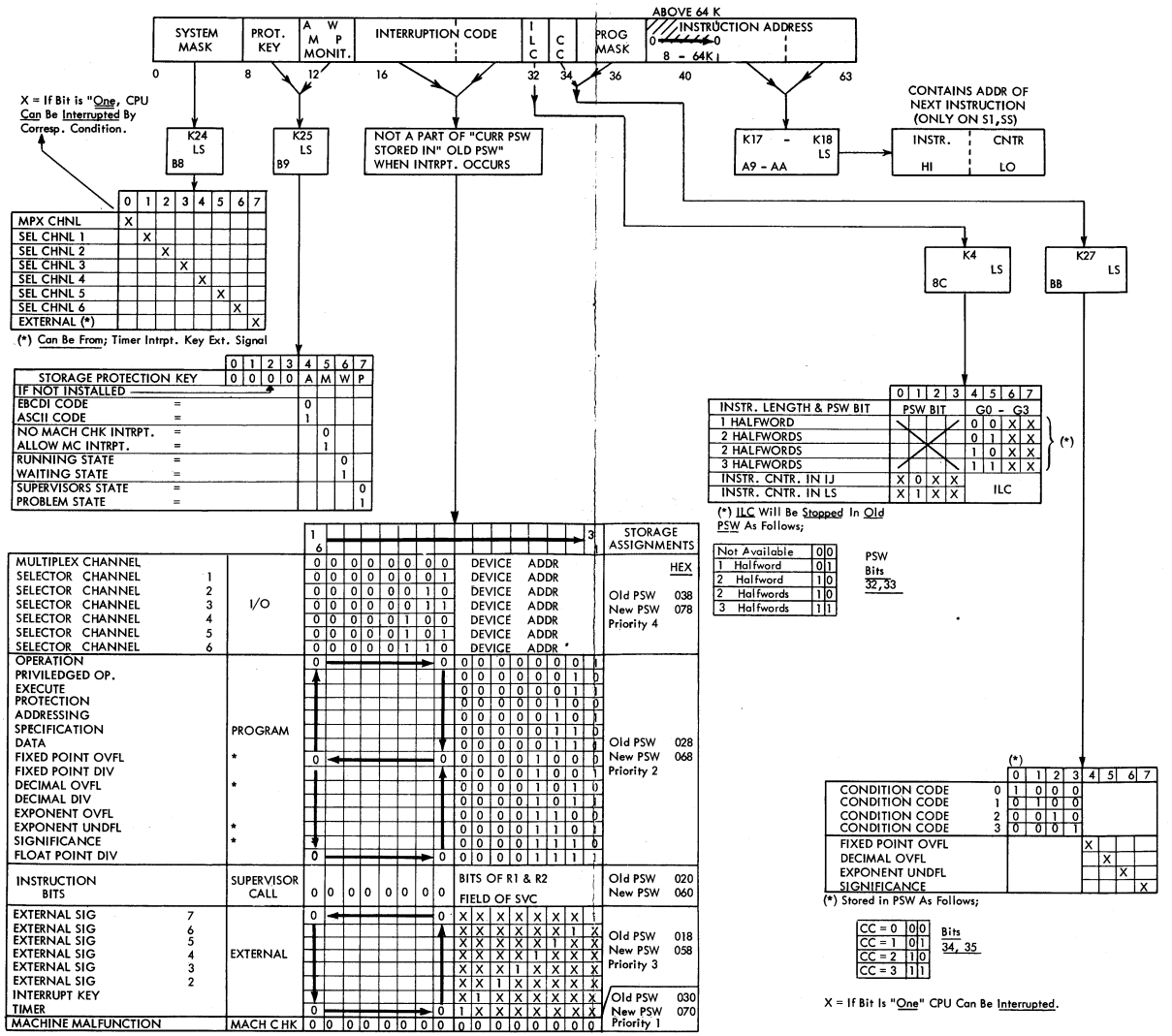
2321



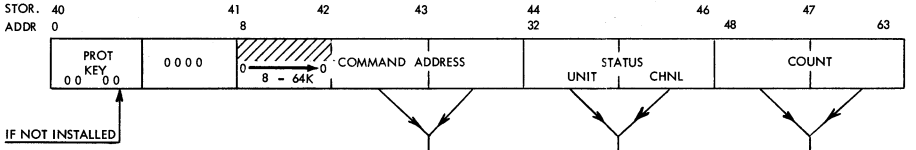
BETA GAP BIT CONFIGURATION


Lead Area 36 Bytes Ones
VFO Area – 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Area 1 Byte
2321
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses No Clock
Ones 5 Bits Missing Clock Pulses No Clock
4 Bits Zeros 1 Bit One 2 Bits Zeros 1 Bit One
1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
0 0 0 0 1 0 0 1
Lead Area – 31 Bytes (2311)
Lead Area – 36 Bytes (2302)
VFO Area – 4 Bytes
Bit Ring Sync Area 1 Byte
2311
Zeros
Zeros
Zeros
Zeros
Zeros
Zeros
Ones
4 Bits Zeros 3 Bits Ones 1 Bit Zero
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 0
Lead Byte
Lead Area – 12 Zeros (2311 – 2302)
Lead Area – 8 Zeros (2321)
VFO Area – 4 Bytes
Bit Ring Sync Area 1 Byte
2302
Zeros
Zeros
Zeros
Zeros
Zeros
Ones
4 Bits Zeros 3 Bits Ones 1 Bit Zero
1 1 0 0 1 1 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 0
Lead Byte
Lead Area – 9 Ones (2311 – 2302)
Lead Area – 3 Ones (2321)
VFO Area – 7 Bytes (2311 – 2302)
9 Bytes (2321)
6 Bytes Zeros (2311 – 2302)
8 Bytes Zeros (2321)
Bit Ring Sync Area 1 Byte
Ones
Ones
Zeros
Zeros
Zeros
Ones
4 Bits Zeros 3 Bits Ones 1 Bit Zero
1 1 0 0 1 1 0 0
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
0 0 0 0 1 1 1 0
INDEX
F C C H H
41 Bytes 2302
36 Bytes 2311
Home Address
18 Bytes 2311 2302
14 Bytes 2321
F C C H H R K D L D L
R0 Count Field
18 Bytes 2311 2302
14 Bytes 2321
R0 Data Field Variable Length
B
A.M.
F C C H H R K D L D L
ID Count Field
18 Bytes 2311 2302
14 Bytes 2321
Key Field Variable Length
18 Bytes 2311 2302
14 Bytes 2321
Data Field Variable Length
B
A.M.
1 BYTE
R0 RECORD
NORMAL RECORD
INDEX
H.A.
A.M.
2321
41 Bytes
2 Bytes
1 BYTE

PROGRAM STATUS WORD

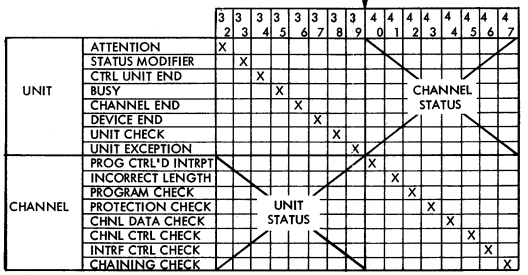


CHANNEL STATUS WORD



CONDITIONS	CONTENTS
CHANNEL CTRL CHECK	UNPREDICTABLE
STATUS STORED BY START I/O STATUS STORED BY HALT I/O	UNCHANGED
INVALID CCW ADDR. SPEC. IN TIC INVALID CCW ADDR. IN TIC	ADDRESS OF TIC + 8
INVALID CCW ADDR. GENERATED	ADDR OF 1ST INVAL. CCW + 8
INVALID COMMAND CODE INVALID COUNT INVALID DATA ADDRESS INVALID CCW FORMAT	ADDRESS OF INVALID CCW + 8
INVALID SEQUENCE - 2 TIC'S	ADDR of 2ND TIC + 8
PROTECTION CHECK	ADDR OF INVALID CCW + 8
CHAINING CHECK TERMINATION UNDER CNT CTRL TERMINATION BY I/O DEVICE TERMINATION BY HALT I/O	ADDR OF LAST USED CCW + 8
SUPPRESSION OF COMMAND CHAINING DUE TO UNIT CHECK OR UNIT EXCEPTION WITH DEVICE END OR CTRL UNIT END	ADDR OF LAST CCW USED IN COMPLETED OPN. + 8
TERMINATION ON COMMAND CHAINING BY ATTN., UNIT CHECK, OR UNIT EXCEPTION	ADDR OF CCW SPECIFYING THE NEW OPN. + 8
PROGRAM CTRL'D INTERRUPTION INTERFACE CTRL CHECK	ADDR OF LAST USED CCW + 8
CHNL END AFTER HIO (SEL CHNL) CONTROL UNIT END DEVICE END ATTENTION BUSY STATUS MODIFIER	0 → 0 0 ← 0

COUNT FIELD	CONDITION
UNPREDICTABLE	CHANNEL CTRL CHECK
UNCHANGED	STATUS STORED BY START I/O STATUS STORED BY HALT I/O
UNPREDICTABLE	PROTECTION CHECK
CORRECT	CHAINING CHECK TERMINATION UNDER CNT CTRL TERMINATION BY I/O DEVICE TERMINATION BY HALT I/O
CORRECT RESIDUAL COUNT OF LAST CCW USED IN COMPLETED OPERATION	SUPPRESSION OF COMMAND CHAINING DUE TO; UNIT CHECK OR UNIT EXCEPTION WITH DEVICE END OR CTRL UNIT END
CORRECT ORIGINAL COUNT OF CCW SPECI- FYING NEW OPERATION	TERMINATION ON COMMAND CHAINING BY; ATTENTION UNIT CHK OR UNIT EXCEPTION
UNPREDICTABLE	PROG. CTRL'D INTERRUPTION (PCI)
0 → 0 0 ← 0	CHNL END ATER HIO (SEL CHNL) CTRL UNIT END DEVICE END ATTENTION BUSY STATUS MODIFIER
HI-ORDER BYTE CON- TAINS CAT- ALOG NO.	THE MULTIPLEX ERROR ROUTINE DETECTED A PROGRAM CHECK
UNPREDICTABLE	MACHINE CHECK



CATALOG NUMBERS (MPX CHNL ONLY)

01	CCW COUNT ZERO
02	HARDWARD FORCED WRAP OR INVALID ADDR
03	HI-ORDER 5 BITS OF CHNL ADDR NON-ZERO
04	1ST COMMAND WAS TIC
05	INVALID CCW COMMAND -XXXX0000
06	BYTE 1 OF CCW NOT ZERO
07	BAD CAW FORMAT
08	TIC TO A TIC
09	TIC FORMAT BAD
0A	MEM ADDR WRAP ON NEXT CCW ADDR CC IMMED
0B	BAD CCW FORMAT
0C	MEM ADDR WRAP ON NEXT CCW ADDR CDA
0D	CCW COUNT ZERO CMD CHANING
0E	LOW 3 FLAG BITS NON ZERO
0F	INVALID FLAGS
1F	MEMORY WRAP ON CMD CHAIN
2F	INVALID CMD BYTE ON CMD CHAIN

TRAPS IN PRIORITY ORDER

PRI	ROS TRAP ADDR	DESCRIPTION	H REG	CLD PAGE
1	000	System Reset		QA951
2	004	Machine Check	1	QA961
3	002	I P L	0	QC351
4	001	Force I J From Switch	4	QA941
5	020	Storage Wrap	2	QA961
6	040	Storage Protect	3	QA961
7	080	Stop Key	--	QA941
8	00B	Selector Chain Request	5	QD111
8	008	Sel. Int. Request	5	QD121
9	010	MPX Share Request	6	QC201

ROS ADDRESSES

ROS HEX ADDR	DESCRIPTION			CLD PAGE NO.
000	System Reset to 328			QA951
008	Sel. Int. Request			QD121
100	I Cycles Start			QA001
OFF	Soft Stop			QA941
OAE	Wait State			QA941
OB2	2nd Error has Occurred			QA961
328	Stop After System Reset			QA951
BF6	Alter			QB851
BF7	Display			QB851
BF1 *	Ros Scan			QB861
BF0 *	Storage Scan			QB711
BF9 *	Clear Storage			QB711
BFF *	Diagnostics to ABC			QB611
AC0	All Bits but PS PC	CN = AFC	Basic	QB871
AC3	All Bits but PS PC			QB871
AC1	CNP, PS, PC	CN = AOO		QB871
AC2	CNP, PS, PC			QB871
1AE0	All Bits but PS PC	CN = 15FC	1400 Comp.	QB871
1AE1	All Bits but PS PC			QB871
1AC2	CNP, PS, PC	CN=1500		QB871
1AC3	CNP, PS, PC			QB871
BBB *	MPX Diag.			QB881
BE3 *	MPX Diag., w/Loop (80 in G)			QB881
10FF	1401 Soft Stop			QE691
1402	IPL from 1402 1401 Mode			QE521
1442	IPL from 1442 1401 Mode			QE521
1729	IPL from 28xx 1401 Mode			QE521
1230	1401 Start Reset			QE631

* Micro Diagnostics

NOTE: ROS addresses can change depending upon the E. C. Level of CCROS.

Field	Hex	Mnemonic	Old Form	Operation
0-5 CN	-	-	-	Shown in Hex on Right Side of Line 7 in the CLD Box. Sets Position 0 through 5 of the X-Register for Next Address.
0-3 CH Set 6th Position of X-Register	-	-	-	Shown on Left Side of Line 7 in the CLD Box.
	0	0	0	Set X-6 to ZERO
	1	1	1	Set X-6 to ONE
	2	R0	R0	Set X-6 to the Condition of R-Register Position 0
	3	VZ	V=00	Set X-6 to ONE, if the V-Register Positions 6 and 7 are ZERO
	4	ST	STI	Status in (I/O)
	5	OP	OPI	OP in (I/O)
	6	AC	AC	Set X-6 to ONE: if there is a Carry Out of ALU Position 0
	7	S0	S0	Set X-6 to ONE, if the Tested Position of the S-or G-Register is Equal to ONE
	8	S1	S1	
	9	S2	S2	
	A	S4	S4	
	B	S6	S6	
	C	G0	G0	
	D	G2	G2	
	E	G4	G4	
	F	G6	G6	
0-3 CL Set 7th Position of X-Register	-	-	-	Shown on Left Side of Line 7 in the CLD Box-Example; CH, CL
	0	0	0	Set X-7 to ZERO
	1	1	1	Set X-7 to ONE
	2	CAhh→W	W=CA	Set Value of CA Field into W-Register, Set X-7 to ONE. hh is the Hex Value of the CA Field and AA Field
	3	AI	AI	Address in (I/O)Address)
	4	SVI	SVI	Service in (I/O)
	5	R=VDD	RVDD	Set X-7 to ONE if the R-Register Contains Valid Decimal Digits
	6	1BC	1BC	Set X-7 to ONE if there is a Carry Out of ALU Position One
	7	Z=0	Z=0	Set X-7 to ONE if the Z-Bus (Bits 0-7) is ZERO
	8	G7	G7	Set X-7 to ONE, if the Tested Position of the S-or G-Register is Equal to ONE
	9	S3	S3	
	A	S5	S5	
	B	S7	S7	
	C	G1	G1	
	D	G3	G3	
	E	G5	G5	
	F	INTR	INTR	Test for any Interrupt, Set X-7 to ONE if there is a Interrupt
0-2 CM Storage Control	-	-	-	Shown on Left Side of Line 4 in the CLD Box
	0	WRITE	WRITE	Write the Data in the R-Register into the Storage Position Addressed by the M-and N-Registers
	1			No Mnemonic-Compute Cycle, Storage not Used
	2	STORE	STORE	Write NEW R-Register Data into the Storage Position Addressed by the M-and N-Registers
	3	LJ→MN	LJ	Set the M-and N-Registers to the Address in the I- and d-Registers and Read from Storage at that Address
	4	UV→MN	UV	Set the M-and N-Registers to the Address in the U- and V-Registers and Read from Storage at that Address
	5	T→MN	T	Set the N-Registers to the Address in the T-Register and Read from Storage at that Address
	6	*aa	K	Set the N-Register using the CK Field (Note 1)
	7	YP	GUV	Dummy Symbol-No Action or Can be Used in a diagnostic Area. (Old From was a Selector Channel Code).
0-1 CU Storage Selection	-	-	-	Shown on Right Side of Line 4 in the CLD Box
	0	MS	MEM	Addressing MAIN Storage
	1	LS	CPU	Addressing Auxiliary Storage-LOCAL Store Section
	2	MPX	UCW	Addressing Auxiliary Storage-Multiplexor UCW Sect.

Field	Hex	Mnemonic	Old Form	Operation
0-1 CU Storage Selection (Cont'd)	3	M/LS	M, C	Addressing MAIN Storage or LOCAL Store Section, Depending on the OP Code-RR Format Selects LS In 1400 Mode this Selects the Local Storage Area for NPL Area
0-1 Alternate CU	- 0	-	-	Shown on Right Side of Line 4 in the CLD Box No Action
	1	GR	Use GR	Use the GR-Register in the Selector Channel in Place of the R-Register for Storage Input and Output
	2	K→W	W=K	Set the W-Register to the Hex Value of the CK Field
	3	FWX→WX	WX=FWX	Set the W-and X-Registers to the Address in the Multiplexor Back-Up Registers (FW and FX)
0-3 CA A-Register Source Control	-	-	-	Shown on Left Side of Line 3 in the CLD Box
	0	FT	FT	Multiplexor Channel Tags in
	1	TT	TT	1050 Tags in
	2	YA		Dummy Symbol-No Action or Can be Used in a Diagnostic Area
	3	YB		Dummy Symbol-No Action or Can be Used in a Diagnostic Area
	4	S	S	Gate the S-Register to the A-Register Via the A-Bus
	5	H	H	Gate the H-Register to the A-Register Via the A-Bus
	6	FI	FI	Multiplexor Channel Bus In
	7	R	R	} Gate the - Register to the A - Register Via the A-Bus
	8	D	D	
	9	L	L	
	A	G	G	
	B	T	T	
	C	V	V	
	D	U	U	
	E	J	J	
	F	I	I	
0-3 Alternate CA Activated by "AA"=1	-	-	-	Shown on Line 4 of the CLD Box
	0	F	F	Gate the F-Register to the A-Register Via A-Bus (External Interrupts).
	1	FG	FG	Gate the F-and G-Switches to the A-Register Via the A-Bus
	2	MC	MC	Gate the Machine Check Register to the A-Register Via the A-Bus
	3	YC		Dummy Symbol-No Action or Can be Used in the Diagnostic Area
	4	C	C	Gate the C-Register to the A-Register Via the A-Bus (Interval Timer)
	5	Q	Q	Gate the Q-Register to the A-Register Via the A-Bus (Protect Storage)
	6	JI	JI	Direct Data Channel Bus In
	7	TI	TI	1050 Bus In
	8	YD		} Dummy Symbols - No Action or Can be Used in the Diagnostic Area
	9	YE		
	A	YF		
	B	YG		
	C	GR	GR	Gate the GR-Register (Selector Channel) to A-Register Via A-Bus
	D	KZ GS	GS	Gate the GS-Register (Selector Channel) to A-Register Via A-Bus
	E	KY GT	GT	Gate the GT-Register (Selector Channel) to A-Register Via A-Bus
	F	KW GJ	GJ	Gate the GJ-Register (Selector Channel) to A-Register Via A-Bus
0-1 CB B-Register Source Control	-	-	-	Shown on Line 3 of the CLD Box
	0	R	R	Gate the R-Register to the B-Register Via the B-Bus
	1	L	L	Gate the L-Register to the B-Register Via the B-Bus
	2	D	D	Gate the D-Register to the B-Register Via the B-Bus
	3	K	K	Gate Hex Value of the CK Field to the B-Register Via the B-Bus
	-	-	-	
0-3 CK Emit Value	-	- - - -	- - - -	Shown on Line 2 of the CLD Box
	0	0 0 0 0	0 0 0 0	} Binary Bit Form of the Hex Number is Routed to the Selected Area When Requested.
	1	0 0 0 1	0 0 0 1	
	2	0 0 1 0	0 0 1 0	

Field	Hex	Mnemonic	Old Form	Operation
0-3 CK Emit Value (Continued)	3	0 0 1 1	0 0 1 1	Binary Bit Form of the Hex Number is Routed to the Selected Area When Requested.
	4	0 1 0 0	0 1 0 0	
	5	0 1 0 1	0 1 0 1	
	6	0 1 1 0	0 1 1 0	
	7	0 1 1 1	0 1 1 1	
	8	1 0 0 0	1 0 0 0	
	9	1 0 0 1	1 0 0 1	
	A	1 0 1 0	1 0 1 0	
	B	1 0 1 1	1 0 1 1	
	C	1 1 0 0	1 1 0 0	
	D	1 1 0 1	1 1 0 1	
	E	1 1 1 0	1 1 1 0	
	F	1 1 1 1	1 1 1 1	
0-3 Alternate CK Activated by "AK"=1	-	-	-	Shown on Left Side of Line 6 of the CLD Box
	0	O→DIAG	RESET DIAG	Reset the Diagnostic Latch
	1	UV→WX	WX UV	Gate the U-and V-Register to the W-and X-Registers Via the WX-Bus
	2	WRAP→Y	RESTORE WRAP	Gate the Wrap Buffer Latch to the Wrap Latch
	3	WRAP→X6	TEST WRAP	Set X6 to ZERO if Wrap Latch is On
	4	HJ→B	HJ	Gate the H-and J-Switches to the B-Register Via the B-Bus
	5	AC FORCE	AC FORCE	Set X-Register to ZERO, if an ALU Carry Occurred in Previous Cycle
	6	YM		Dummy Symbol-No Action or Used in Diagnostic Area. Old Mnemonic was Reset 1050 Line Latch
	7	YN		Dummy Symbol-No Action or Used in Diagnostic Area. Old Mnemonic was Set 1050 Line Latch
	8	1→OE	OE=1	Force an ALU Check (Note 3)
	9	ASCII→X6	TEST ASCII	Set X-6 to ZERO if the ASCII Latch is On
	A	INT→X6, X7	TEST INT	Set X-6 and X-7 per Stacked Interrupts (Note 4)
	B	0→MC	MC=0	Set Machine Check Register to All ZEROS
	C	Y→WRAP	STORE WRAP	Gate the Wrap Latch to the Wrap Buffer Latch
	D	0→LOAD	LOAD	Reset the LOAD, ODD/EVEN, and INTRODUCE ALU CHECK Latches
	E	0→F	F=0	Reset the F-Register to ALL ONES. Note: The Reset Condition of the F-Register is ALL ONES
	F	1→F0	F0=1	Set the F-Register Position 0 to ZERO
0-3 CD Destination of ALU Output	-	-	-	Shown on Line 3 of the CLD Box
	0	Z	Z	To Show That the Z-Bus is the Only Place the Output of the ALU is Routed
	1	TE		
	1	TE	TE	1050 Bus Out (Exit)
	2	JE	JE	Direct Data Channel Bus Out (Exit). Set JE-Register from D-Register, Z-Bus not Used.
	3	Q	Q	Gate the Output of the ALU to the Q-Register Via the Z-Bus
	4	TA	TA	1050 Tags Out
	5	H	H	Gate the Output of the ALU to the ___Register Via the Z-Bus
	6	S	S	
	7	R	R	
	8	D	D	
	9	L	L	
	A	G	G	
	B	T	T	
	C	V	V	
	D	U	U	
	E	J	J	
	F	I	I	
0-2 CF A-Register to ALU	-	-	-	Shown on Line 3 of the CLD Box
	0	0	0	Block A-Register Exit to the ALU. Route ALL ZEROS to ALU Entry for the A-Register
	1	L	L	Block High 4 Bits of A-Register. Route 4-ZEROS and Bits 4-7 of A-Register to the ALU

Field	Hex	Mnemonic	Old Form	Operation
A-Register to ALU (Continued)	2	H	H	Block Low 4 Bits of A-Register, Route 4-ZEROS and Bits 0-3 of A-Register to the ALU
	3			Gate the Entire A-Register to the ALU
	4	SP	STOP	Conditional Machine Stop (Note 5)
	5	XH	XH	Block A-Register Bits 0-3 Exit Gate A-Register Bits 4-7 to ALU Entry Bits 0-3 and 4-ZEROS to Bits 4-7
	6	XL	XL	Block A-Register Bits 4-7 Exit, Gate A-Register Bits Bits 0-3 to ALU Entry Bits 4-7 and 4-ZEROS to Bits 0-3
	7	X	X	Gate A-Register Bits 0-3 to ALU Entry Bits 4-7 and Gate A-Register Bits 417 to ALU Entry Bits 0-3
0-1	-	-	-	Shown on Line 3 of the CLD Box
CG	0	0	0	Block B-Register Exit to the ALU, Route All ZEROS to the ALU Entry for the B-Register
B-Register to ALU	1	L	L	Block High 4-Bits of the B-Register, Route 4-ZEROS and Bits 4-7 of the B-Register to the ALU
	2	H	H	Block Low 4 Bits of the B-Registers, Route 4-ZEROS and Bits 0-3 of the B-Register to the ALU
	3			Gate the Entire B-Register to the ALU
0-1	-	-	-	Shown on Line 3 of the CLD Box
CV	0	+	+	True Add B-Register Data
Arithmetic	1	-	-	Complement Add B-Register Data
Functions	2	±	±	Binary Add or Subtract Depending on the Status of 50
	3	±	@	Decimal Add or Subtract Depending on the Status of 50
0-2	-	-	-	Shown on Line 3 of the CLD Box
CC	0	0	0	Block Carry
Arithmetic	1	1	1	Insert Carry
Controls	2	.	*	AND Function-Check to See if Same Bits are Set to ONE in both the A-and B-Register Using the ALU
	3	Ω	$	OR Function-Check to See if Either Bit in the Same Position of the A-and B-Register is Set to ONE
	4	0C	CO	No Carryin, Set S3 to ONE if a Carrout Occurs
	5	1C	C1	Insert A Carryin and Set S3 to ONE if a Carryout Occurs
	6	CC	CC	Allow Carryin from Carry Latch and Set S3 to ONE if a Carryout Occurs
	7	⊻	⊻	Exclusive OR Function-Check to See if Only the A-or B-Register has the Same Bit Position Set to ONE
0-3	-	-	-	Shown on Line 5 of the CLD Box
CS	0			No Action
Status Conditions	1	LZ→S5	S5=LZ	Set S5 to ONE if Bits 4-7 of the Z-Bus Are 0. Reset S5 if Non-Zero
	2	HZ→S4	S4=LZ	Set S4 to ONE if Bits 0-3 of the Z-Bus are 0. Reset S4 if Non-Zero
	3	HZ→S4, LZ→S5	S4,S5=HZ, LZ	Combines the Conditions of CE Field Mnemonics S5 and HZ S4
	4	0→S4,S5	S4,S5=0	Set S4 and S5 to ZERO
	5	TREQ→S1	S1=TREQ	Set S1 to ONE if a 1050 Request has Occurred. Set S1 to ZERO if no 1050 Request
	6	0→S0	S0=0	Set S0 to ZERO
	7	1→S0	S0=1	Set S0 to ONE
	8	0→S2	S2=0	Set S2 to ZERO
	9	ANSNZ→S2	S2 ANSNZ	Set S2 to ONE if the Output from the ALU is Non-Zero (Note 6)
	A	0→S6	S6 0	Set S6 to ZERO
	B	1→S6	S6=1	Set S6 to ONE
	C	0→S7	S7=0	Set S7 to ZERO
	D	1→S7	S7=1	Set S7 to ONE
	E	K→FB	FB=K	Multiplexor Channel Tags Out
	F	K→FA	FA=K	Multiplexor Channel Tags Out

Field	Hex	Mnemonic		Old Form	Operation
0-3 Alternate CS Selector Channel Activated by "AS"=1 Selected by Hardware	-		-	-	Shown on Line 5 of the CLD Box
	0	YH	-	-	Dummy Symbols
	1	YJ	-	-	
	2	KS→R	-	-	Used for Selector Channel Operations. These are Selector Channel Registers (Note 2)
	3	KC→R	-	-	
	4	KD→R	-	-	
	5	KK→R	-	-	
	6	KUV→KCD	GUV→GCD	GCD=GUV	
	7	R→KK	GR→GK	GK=GR	
	8	R→KF	GR→GF	GF=GR	
	9	R→KG	GR→GG	GG=GR	
	A	R→KU	GR→GU	GU=CR	
	B	R→KV	GR→GV	GV=GR	
	C	K→KH	K→GH	GH=K	
	D	R→KS	GI→GR	GR=GI	
	E	K→KB	K→GB	GB=K	Selector Channel Tags Out
	F	K→KA	K→GA	GA=K	Selector Channel Tags Out

Note 1	Note 2	Note 3	Note 4	X6	X7	Note 5	Note 6
N-Register Set as Follows: N0-Forced to ONE N1-Forced to ZERO N2-CN 0Bit N3-CK 0Bit N4-Forced to ONE N5-CK 1Bit N6-CK 2Bit N7-CK 3Bit	These Mnemonic Depends on the Channel Requested. Mnemonics may be of Three Types for one Hex Number. Example - Alternate CA Field. Hex E can be KY, GT, or HT	Used on Diagnostics to Force Parity	Timer/External	0	0	Micro Program Stop or Process Loop Stop	In Diagnostic Mode, if the "Malfunction Trap Latch" is Set, this Mnemonic will Cause Machine Stop.
			Channel 1	1	0		
			Channel 2	0	1		
			Multiplexor Channel	1	1		

S-REGISTER	
SØ	Complement
S1	1050 Req
S2	Ans. NZ
S3	Carry
S4	Hi Z Bus
S5	Lo Z Bus
S6	Misc.
S7	Misc.

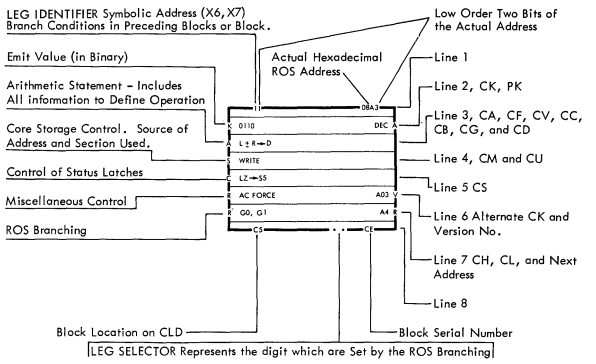
MC-REGISTER	
Ø	A - Parity Check
1	B - Parity Check
2	MN - Parity Check
3	Ctrl. - Reg. P. C.
4	SAL. - Parity Check
5	ROAR Check
6	R-Parity Check
7	ALU Check

H-REGISTER	
Ø	Prev. IPL-Trap (Mach. Check)
1	2nd Mach. Check (Hard Stop)
2	Prev. Memory Wrap Trap
3	Prev. Memory Protect Trap
4	Prev. Force IJ Request Trap
5	SX ROS Request (Chain Data, Chain Request)
6	MPX ROS Request (Chain Data, Chain Request)
7	Not used

ALU CONTROLS

	CON	LM	$\overline{N}$
ADD	Off	Off	On
XOR	On	Off	On
AND	On	On	Off
OR	On	Off	Off

MICRO - WORD FORMAT (NEW)



ROS CONTROL FIELD DESCRIPTION

PN - Odd Parity On CN Field

CN - Next ROS Address

PS - Odd Parity For SAL's

PA - Odd Parity For ROS Word Address

CH - ROS Address Branching

CL - ROS Address Branching

CM - Address Register/Read Write Select

CU - Main Storage or Local Storage Data Destination

CA - Input Source for A Buss and A Register

CB - Input Source for B Buss and B Register

CK - Constant Generator

PK - Parity for CA or CK Fields Depending on Mnemonic Used. CK Field When K←W, CA When CAhh←W

PC - Odd Parity On Control Registers

CD - Destination From Z Buss

CF - Controls the Hi/Lo, Crossed/Straight Functions of the A Register Entry Into the ALU

CG - Controls the Hi/Lo Functions of the B Register Entry Into the ALU

CV - True/Complement and Binary/Decimal Controls

CC - Carry Control and Logic Control

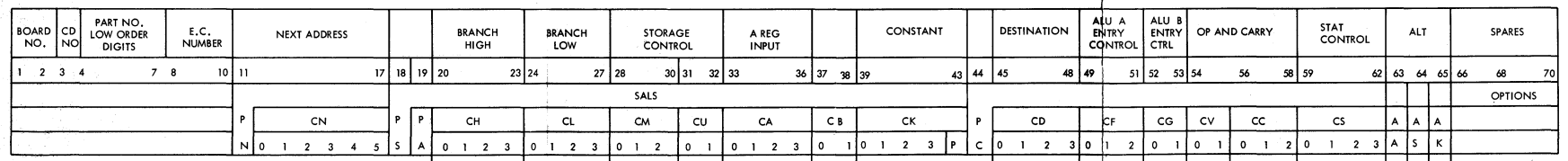
CS - Status Control

AA - Alternate CA Decoder Bit

AS - Alternate CS Decoder Bit

AK - Alternate CK Decoder Bit

ROS CONTROL FIELD CHART



AC	ADDRESS CARRY (ALU CARRY)
ACS	ALTERNATE CS
ACU	ALTERNATE CU
AC FORCE	SET X REG=0 IF AC ON PREVIOUS WORD
AI	ADDRESS IM (I/O ADDRESS)
ANS NZ	ANSWER NON ZERO
ASCII	PSW BIT 12
C	COUNTER FOR INTERVAL TIMER
LS	LOCAL STORAGE
F	EXTERNAL INTERRUPT REGISTER
FA	MX CHANNEL CONTROL
FB	MX CHANNEL CONTROL
FG	SWITCHES FG
FI	MX CHANNEL BUSS IN
FT	MX CHANNEL TAGS IN
FWX	MX CHANNEL BACKUP ROMAR
GA	SX CH TAGS OUT CTRL
GB	SX CH CONTROLS
GCD	SX CH COUNT REG
GF	SX CH FLAG REG
GG	SX CH COM REG
GH	SX CH CONTROLS
GJ	SX CH K FIELD CTRL A-REG ENTRY
GK	SX CH PROT KEY REG
GMWM	GROUP MARK-WORD MARK
GR	SC CH DATA REG
GS	SX CH A-REG ENTRY
GT	SX CH A-REG ENTRY
GUV	SX CH DATA ADDR REG
HJ	SWITCHES HJ
H	HOLDING REGISTER-PRIORITY
HZ	HIGH Z BUSS
INT	INTERRUPT
JE	DIRECT DATA CHANNEL BUSS OUT (EXIT)
JI	DIRECT DATA CHANNEL BUSS IN
LOAD	RESET LOAD, ODD/EVEN CTRL. INTRO ALU CHK
LZ	LOW Z BUSS
MS	MAIN MEMORY
M/LS	MAIN MEMORY OR LOC STOR - (LOC STOR
MC	MACHINE CHECK
MRST	MACHINE RESET
OE	ODD, EVEN AND ALU CHECK CTRL
OP	OP IN (I/O)
PA	ADDRESS PARITY (ROS ADDRESS)
PN	NEXT ADDRESS PARITY
PS	SAL PARITY
Q	STORAGE PROTECT REGISTER

0000	0	0	0	WRITE	MS	FT	R		Z
0001	1	1 (GMWM)	1		LS	TT	L		TE
0010	2	R0	CAhh→W	STORE	MPX	YA	D		JE
0011	3	VZ	AI	IJ→MN	M/LS	YB	K		Q
0100	4	STI	SVO	UV→MN		S			TA
0101	5	OPI	R = VDD (R1)	T→MN		H			H
0110	6	AC	1 B C	*aa (LT)→		FI			S
0111	7	S0	Z = 0	GUV		R			R
1000	8	S1 (R2)	G7			D			D
1001	9	S2	S3			L			L
1010	A	S4	S5			G			G
1011	B	S6	S7			T			T
1100	C	G0	GJ (R3)			V			V
1101	D	G2	G3			U			U
1110	E	G4	G5			J			J
1111	F	G6	INT			I			I

								0	+
								L	∓ (DEC)
								H	± (BIN)
								SP	1
								KL	•
								KH	Ω
								K	
									C C
								I	C C
								C	≠ C

									LZ→S5
									HZ→S4
									HZ→S4 LZ→S5
									0→S4, S5
									TREQ→S1
									0→S0
									1→S0
									0→S2
									ANS NZ→S2
									0→S6
									1→S6
									0→S7
									1→S7
									K→FB
									K→FA

○ Denotes Altered Functions When In 1401 Mode (W3 = 1)

Alternate CPU Decoder Activated By CM ≠ 3 - 7

GR	F	0→DIAG		
K→W	FG	UV→WX		
FWX→WX	MC	WRAP→Y		
	YC	WRAP→X6		
	C	HJ→B		
	Q	AC→FORCE		
	JI	YM		
	TI	YN		
	YD	1→0E		
	YE	TEST ASCII X6		
	YF	TEST INT X6X7		
	YG	0→MC		
GR		Y→WRAP		
GS		0→LOAD		
GT		0→F		
GJ		1→F0		

Selector Chan Option

Alternate CA Decoder Activated By AA (Col 63)=1

Alternate CK Decoder Activated By AK (Col 65)=1

Selector Channel Option

				GUV→GCD
				GR→GK
				GR→GF
				GR→GG
				GR→GU
				GR→GV
				K→GH
				GI→GR
				K→GB
				K→GA

Alternate CS Decoder Activated By As (Col 64)=1

1 Activates Ctrl = K Decoder In PS Parity

1 Activates Alternate CS Decoder In PC Parity

1 Activates Alternate CA Decoder In PS Parity

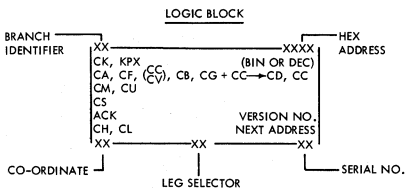
R=VDD	R VALID DECIMAL DIGIT
ST	STATUS IN (I/O)
ST	STOP
STOR	WRITE BUT DON'T SET R (CLEAR)
SV	SERVICE IN (I/O)
TE	1050 BUSS OUT (EXIT)
TI	1050 BUSS IN
TREQ	1050 REQUEST
TT	1050 TAGS IN
TA	1050 TAGS OUT
MPX	MPX STORAGE
VZ	V67 00
CA→K	GATE CA FIELD TO W STORAGE WRAP LATCH
WRAP	STORAGE WRAP LATCH
WRITE	WRITE AND SET R
1BC	ONE BIT CARRY
•	AND
⩛	OR
⩒	EXCLUSIVE OR

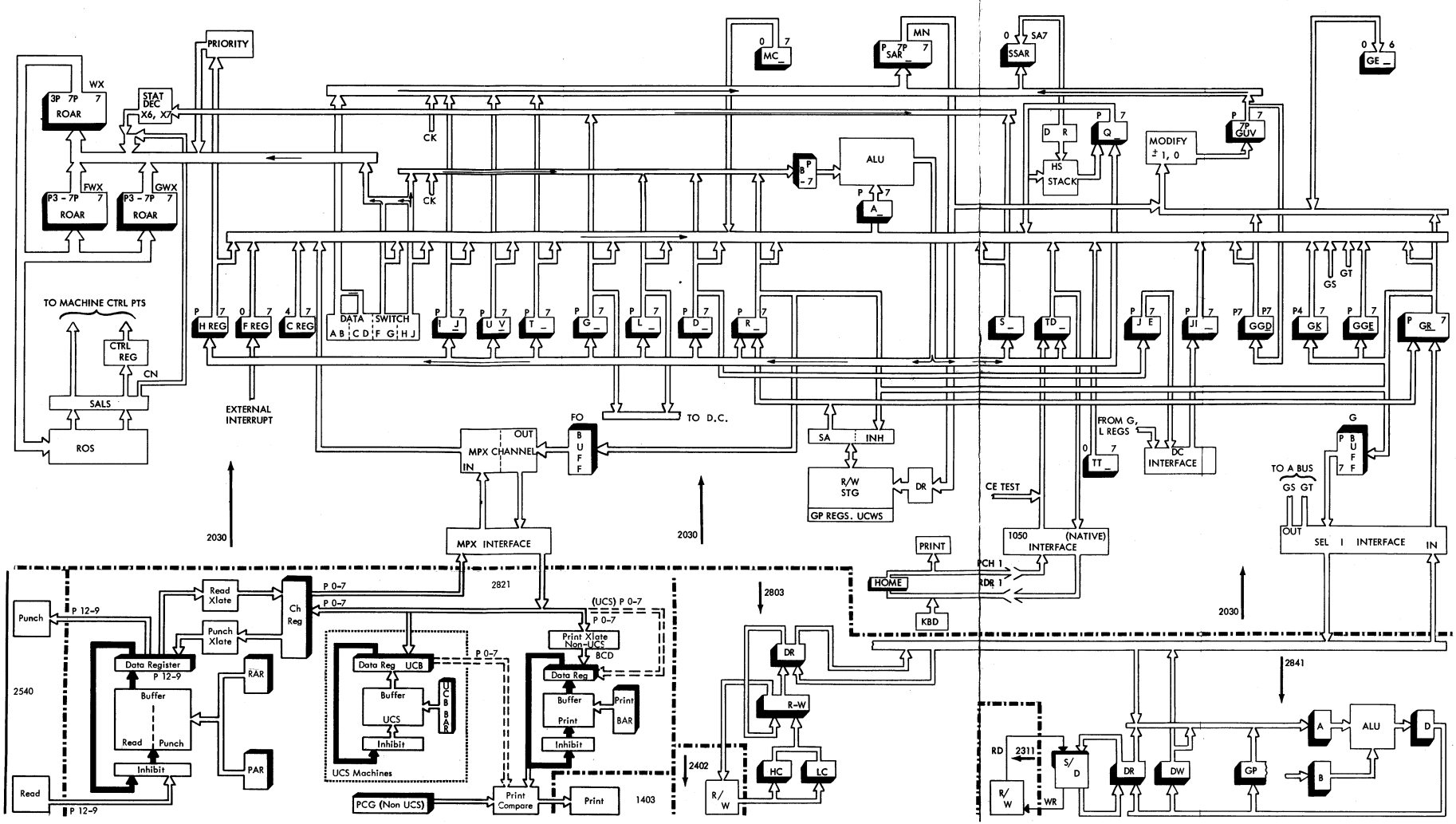
NOTE: ⩛ ± SETS WAIT LATCH ON
⩒ ± SETS MACH CH MASK LATCH
FROM R5 AND ASCII LATCH FROM R4.

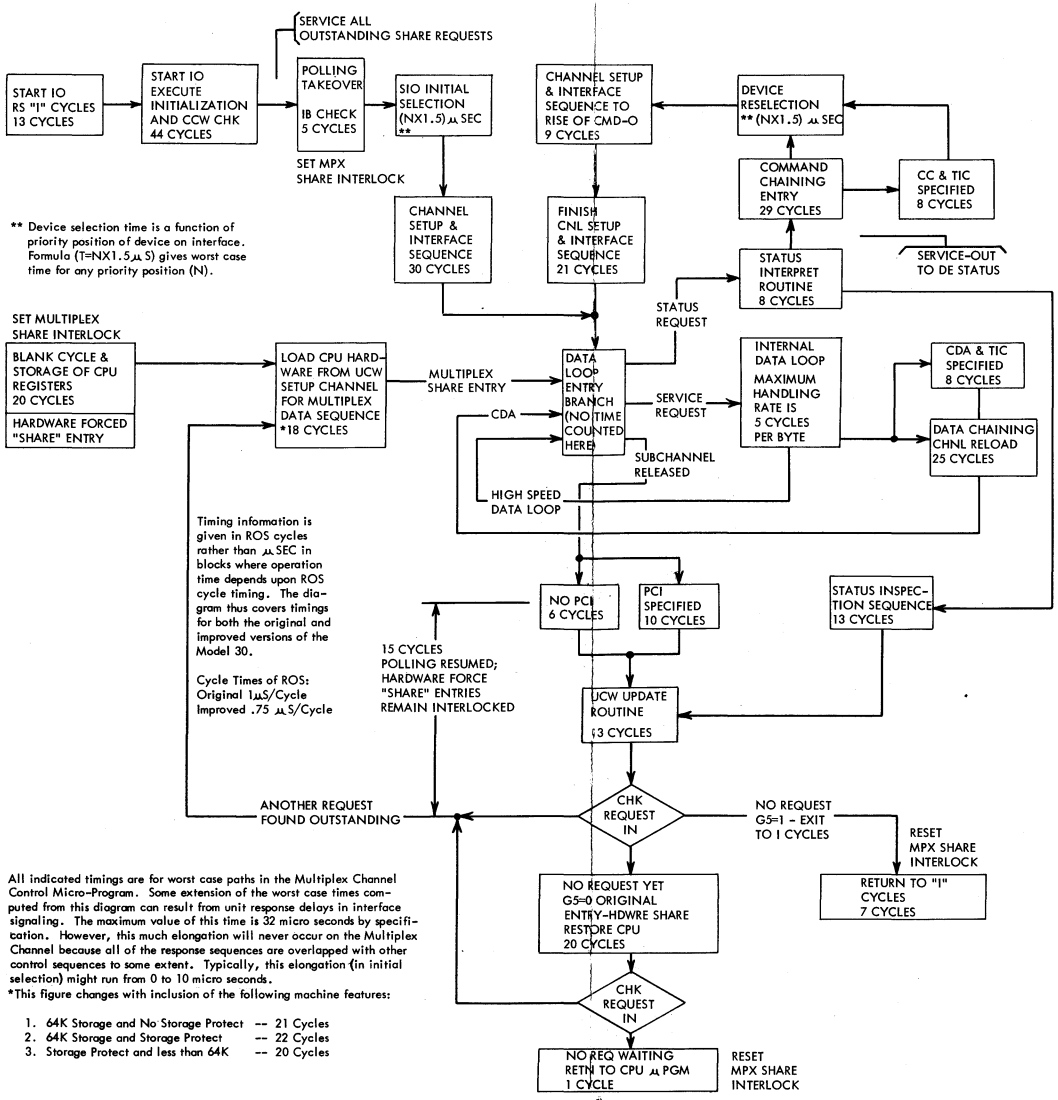
*aa In Storage Control Means aa Is Low Order Digits Of Effective Address Formed By The K Field

NOTE: Only The Fields And Lines Necessary In A Logic Block Are Specified. Fields Not Specified Are Considered To be the Zero or Blank Combination as Required.

LOGIC BLOCK




PRIORITY
WX
3P 7P 7
ROAR
STAT DEC X6, X7
FWX
P3 - 7P 7
ROAR
GWX
P3 - 7P 7
ROAR
CK
CK
TO MACHINE CTRL PTS
CTRL REG
CN
SALS
ROS
EXTERNAL INTERRUPT
P 7 H REG
0 7 F REG
4 7 C REG
DATA SWITCH A B C D F G H J
P 7 I J
P 7 U V
P 7 T
P 7 G
P 7 L
P 7 D
P 7 R
0 7 MC
P 7 SAR
MN
0 SA7 SSAR
0 6 GE
B P -7
ALU
P 7 A
D R
P 7 Q
HS STACK
MODIFY ± 1, 0
P 7 GUV
P 7 S
TD
P 7 J E
P 7 JI
P7 GGD
P4 7 GK
P 7 GGE
P GR 7
GS
GT
FO
OUT
MPX CHANNEL
IN
BUFF
TO D.C.
SA
INH
R/W STG
DR
GP REGS. UCWS
FROM G, L REGS
0 7 TT
DC INTERFACE
CE TEST
1050 (NATIVE) INTERFACE
G
P BUFF 7
TO A BUS
GS GT
OUT
SEL I INTERFACE
IN
2030
2030
2030
MPX INTERFACE
2821
PRINT
PCH 1
RDR 1
HOME
KBD
2803
2841
Punch
P 12-9
Read Xlate
Punch Xlate
Ch Reg
P 0-7
P 0-7
(UCS) P 0-7
P 0-7
Print Xlate Non-UCS
BCD
Data Register
P 12-9
RAR
Buffer
Read
Punch
Inhibit
PAR
2540
Read
P 12-9
Data Reg UCB
Buffer
UCS
Inhibit
UCS Machines
P 0-7
UCB BAR
Data Reg
Buffer
Print
Inhibit
Print BAR
PCG (Non UCS)
Print Compare
Print
1403
2402
DR
R-W
HC
LC
R/W
RD
2311
R/W
WR
S/D
DR
DW
GP
A
ALU
D
B

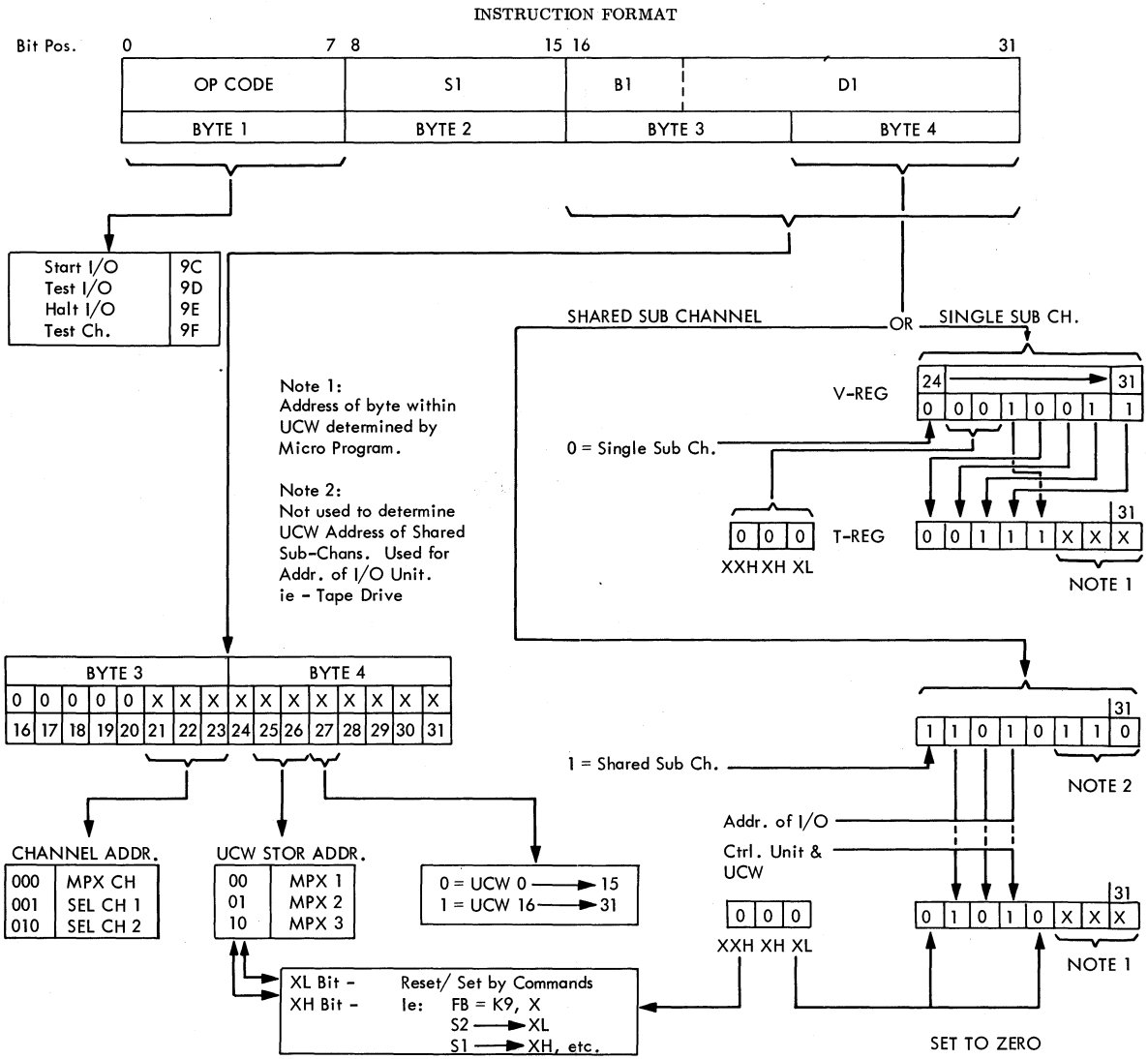


All indicated timings are for worst case paths in the Multiplex Channel Control Micro-Program. Some extension of the worst case times computed from this diagram can result from unit response delays in interface signaling. The maximum value of this time is 32 micro seconds by specification. However, this much elongation will never occur on the Multiplex Channel because all of the response sequences are overlapped with other control sequences to some extent. Typically, this elongation (in initial selection) might run from 0 to 10 micro seconds.

*This figure changes with inclusion of the following machine features:

1. 64K Storage and No Storage Protect -- 21 Cycles
2. 64K Storage and Storage Protect -- 22 Cycles
3. Storage Protect and less than 64K -- 20 Cycles

ADDRESSING OF UCW - I/O FORMAT



UNIT CONTROL WORD

Status	Flag OP	Count Hi	Count Lo	Data Addr Hi	Data Addr Lo	Next CCW Addr Hi	Next CCW Addr Lo	Hex Addr	0-15	Local Storage
X0	X1	X2	X3	X4	X5	X6	X7			
X8	X9	XA	XB	XC	XD	XE	XF	Hex Addr	16-31	

0 | 7 0 | 7 0→7 0→7 0→7 0→7 0→7 0→7 Bits

Indicates Data Addr. Wrap for 64K

0	Chain Data Address
1	Chain Command
2	Suppress Incorrect Length -SIL
3	Skip Flag
4	* Program Control Interrupt - PCI
5	**Active Bit
6	Output (1) Input (0)
7	Decrement (1) Increment (0) (Data Addr.)

* IPL Routine

**Set During Start I/O, Reset By I/O Interrupt or Test I/O Instruction

0		Zero Count - 1050 Only	
1		Channel Control Check	
2		Interface Control Check	
3	00	Sub Channel Expects Data	"Active Bit" Must Be On To Be Meaningful.
4	01	Sub Channel Term. Data X Fer - Status Exp.	
	10	Status From Unit - Qued Back - Inter. Buffer Full	
	11	Status From Unit - Accepted - Now In Inter. Buffer	
5		Wrong Length Record	
6		Program Check	
7		Protection Check	

MULTIPLEX CHANNEL CONTROL

	CK Field P	0	1	2	3		
CK0→FA	1					Command Start	K0 0 FA
CK1→FA					1	Service Out	Fall of Serv or Stat In
CK2→FA				1		Command Out	Fall of Addr Stat or Serv In
CK4→FA			1			Address Out	
CK8→FA		1				Buss Out Ctrl.	Fall of Add Ser or Cmd Out
						NOTE: Some functions may be combined. Blanks in CK Field Are Not Significant	
						FB Reg Latches	Description
CK5→FB		0	1	0	1	Operational Out	Ctrl's Op Out Line
CK6→FB		0	1	1	0	MPX Op Latch	Determines Chnl/CPU Error
CKA→FB		1	0	1	0	Suppress Out Ctl	Ctrl's Supp Out
CKC→FB		1	1	0	0	MPX Interrupt	IB Full
						Mask Latches	
CK3→FB	0	0	0	1	1	MPX Channel	Controlled by R0
						Sel 1 Channel	Controlled by R1
						Sel 2 Channel	Controlled by R2
						External Mask	Controlled by R7
						Bump Addr Lat	
CK9→FB	0	1	0	0	1	XXH MPX 1	Controlled by S0
						XL MPX 2	Controlled by S1
						XH MPX 3	Controlled by S2

MULTIPLEX CHANNEL CONTROL

FT - BUS - CONTROLLED BY CA FIELD

Ft Reg	Function
Ø	Suppress Out (Diagnostic Use Only)
1	Hold - In Latch (Direct Data Channel)
2	Multiplexor Operation Latch
3	Multiplexor-Share-Request Signal (if command start is off)
4	Initial - Program Load Latch
5	Select - In Interface Signal
6	Select - Out (Diagnostic Use Only)
7	Multiplexor Channel Interrupt Latch

STATUS - IN and SERVICE - IN BRANCHES

Stat-In	Serv-In	Function
1	1	Operational-In is Down
Ø	1	Service-In and Operational-In Up
1	Ø	Status-In and Operational-In Up
Ø	Ø	None of the above, Note 1.

NOTE 1: Usually "Operational In" Up, and "Service In" and "Status In" Down

SELECTOR CHANNEL CONTROL

CM Field	
7	Diag. Control - (GUV→MN)
ALT CA Field	
C	GR
D	GS
E	GT
F	GJ
ALT CS Field	
6	GUV→GCD (Count)
7	GR→GK (Prot. Key)
8	GR→GF (Flags)
9	GR→GG (Command)
A	GR→GU
B	GR→GV (Data Address)
C	K→GH *
D	GI→GR* (Bus In)
E	K→GB *
F	K→GA *

* Decode from SALS (others from Ctrl. Req.)

SELECTOR CHANNEL CONTROL
K→GB, K→HB CONTROLS
[continued]

CK FIELD DECODE	NAME	REASON
K0	Program Check	Zero Count Except for TIC, Invalid Memory Key, Memory Wrap, Three Low Order Flag Bits Not Zero, First CCW is a TIC, Two TIC's in Succession, CCW Not on Word Boundaries or Invalid Command.
K1 (0 or 1)	SX2 Selection	0 = SX1, 1 = SX2
K2	Operational-Out Reset	
K3	Reset PCI	
K4	Selector Interrupt Set	
K5	Channel Control Check	A Machine Check Trap (H-Register 5 Latch On) Indicates Hardware Failure, or an MN or GHYZ Parity Check During a Selector Share Cycle.
K6	Set GR to Zero	
K7	CPU Stored	
K8 (0 or 1)	Count Ready	0 = Reset, 1 = Set
K9 (0 or 1)	Channel Reset	0 = Not Poll Control Reset, 1 = Poll Control Reset
K10 (0 or 1)	Suppress-Out	0 = Reset, 1 = Set
K11 (0 or 1)	Poll Control	0 = Reset, 1 = Set
K12	Reset Select-Out	
K13	Channel Busy	
K14	See Halt I/O Latch	
K15	Interface Control Chk.	Address Mismatch, No Response, Time Out, Unit Busy on Chaining, Address or Status Parity Error.

*(0 or1) Refers to the CK Field Parity Bit

GA or HA Reg (K→ GA)

CK Field Bit		Prog. Symbol
CK Ø	Bus Out Ctrl.	K8
CK 1	Address Out	K4
CK 2	Command Out	K2
CK 3	Service Out	K1

GJ Entry into A-Reg (K→GJ)

EMIT		
K Ø		
K 1	GC→GJ	
K 2	GD→GJ	
K 3	GK→GJ	A - Reg. Parity Ignored
K 4	GE→GJ	
K 5		
K 6	SX1 or 2 Ctrls→GJ	Diag. Ctrls
K 7	SX1 or 2 Tags→GJ	
K 8	GO or HO → GJ	

GH or HH Reg (K→GH)

EMIT		
K Ø	SX1, SX2 Mach. Reset	Diag. Ctrls
K 1	Set Diag. Mode & Tag Ctrl	
K 2	Reset Diag. Tag Ctrl	
K 3		
K 4		
K 5		
K 6		
K 7	Set Chain Detect	
K12	Set Select Out	

SELECTOR CHANNEL CONTROL
[continued]

Input to GJ Assembler

Bit	GE Bus	Diagnostic Controls Bus	Diag. Tags Bus
P	None	None	None
O	PCI	Count Ready, Not Zero	Input
1	Incorrect Length	SLI Flag	Suppress Out
2	Program Check	Output	SX1 ROS Request
3	Protection Check	Count Ready, Zero	Address Out
4	Channel Data Check	Selector Chnl. Data Trans.	Command Out
5	Channel Control Check	CC Flag	Service Out
6	Interface Control Chk.	Read Backward	Bus-Out Control
7	Not Used	Skip Flag	Operational Out

GS or HS Entry into A - Reg

GSØ, HSØ	GR Full
1	Chain Detect
2	Select Out
3	Interrupt Condition
4	CD Flag
5	SX1 Gate (1 SX1 Gate, Ø)
6	
7	Interface Check

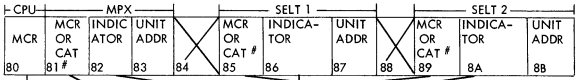
GT or HT Entry into A - Reg

GTØ, HTØ	Select In
1	Serv in & Not Serv Out
2	Poll Ctrl
3	Chnl Busy
4	Address In
5	Status In
6	SX1 (or 2) Interrupt LA
7	Operational In

GR or HR Entry into A - Reg

GRØ, HRØ	
1	
2	
3	Device Address
4	or
5	Device Status
6	
7	

CPU CHANNEL LOGOUT



MACH CHECK REGISTER	
BIT	CONDITION
0	A REG
1	B REG
2	MN REG
3	CR
4	SALS
5	ROAR
6	R REG/Q REG
7	ALU

INDICATOR BYTE

0	1	2	3	4	5	6	7
ACCUMULATED LOG-OUT C NT.							

SET TO 1 ON ANY LOG-OUT CONDITION

INTERFACE STATE	
BITS	MEANING
0 0	INTRF CLEAR (OP IN DOWN) AT ERR OCCURRENCE
0 1	HIO RESET REQUIRED AND SUCCESSFUL
1 0	SELECTIVE RESET REQUIRED AND SUCCESSFUL
1 1	INTRF LOCKED UP; SELECTED RESET FAILED

1	CATALOG NUMBER STORED
0	MCK REGISTER STORED

} DETERMINES INFORMATION TO BE STORED IN BYTES 81, 85, or 89.

MULTIPLEX CHANNEL, CATALOG NUMBERS		
HEX NO	MEANING OR CONDITION	CCN SOURCE
20	FALSE SHARE REQUEST, CONS.	QC601 GG
31	NO ADDR MATCH ON INITIAL SELECTION	QC051 GJ
41	NO ADDR MATCH ON INITIAL SELECTION	QC051 GJ
50	TIME-OUT (FALL) OF OPERATIONAL-IN LINE	QC161 CE
51	FALSE REQUEST, WITHOUT SELECT-IN PROPOGATED	QC211 EF
70	DOUBLE SELECTION (CONSOLE AND OTHER	QC 211 ED
77	USED BY A NUMBER OF ICC TIMEOUTS DURING THE VARIOUS SEQUENCES. THE EXIT WORD IS 500 AND IS ENTERED BY WAY OF THE AC FORCE MICRO COMMAND. TO FIND THE ERROR, SET SYSTEM TO EARLY ROAR STOP ON ROS ADR 500.	QC151 GE
80	DATA LOOP TIMED OUT. NO RESPONSE FROM UNIT	QC081 NF
90	NO UNIT RESELECTION ON COMMAND CHAINING	QC091 CD
A0	NO SELECTION AND NO SELECT IN	QC091 CD
B0	UNIT DID NOT STOP AS TOLD AFTER CCW EXHAUSTED OR TERMINATED	QC081 LF

SELECTOR CHANNEL CATALOG NOS.	
HEX NO	MEANING OR CONDITION
10	POLL CTRL TIME-OUT (SIO, TIO, HIO).
20	QUE STATUS TIME-OUT (SIO, TIO, HIO).
30	NO ADDR-IN, STATUS IN, OR SEL-IN. (CC OR INIT. SELECT SIO, TIO, HIO).
40	ADDR MISMATCH (SIO, TIO HIO OR COMMAND CHAIN).
50	NO STATUS-IN OR INITIAL SELECT (SIO, TIO, HIO, OR COMMAND CHAIN).
60	BAD ADDR. OR STATUS BYTE ON INITIAL SELECT (SIO, TIO, HIO, OR COMMAND CHAIN).
70	STATUS-IN TIME OUT ON INITIAL SELECT (TIO)
80	STATUS-IN TIME-OUT ON COMMAND CHAINING.
90	SELECT-IN ON CMD CHAINING RESELECTION.
A0	CONTROL UNIT BUSY ON COMMAND CHAINING
B0	ADDRESS MISMATCH ON TIO OR HALT IO
C0	STATUS-IN OR OP-IN CANNOT BE RESET ON CSW STORE
E0	POLL CTRL CANNOT BE SET ON HIO
F0	OP-IN CANNOT BE RESET ON HIO

MPX AND SX MICRO PROGRAM

Main functions of initial Selection of MPX and SX with the micro Program Address where they are performed.

Example: With ROAR STOP, one single cycle should be done to perform the function.

MPX:

Function	Addr.	Notes
Address Out	536	Unit addr. is displayed on Bus Out
Select Out	5A0	If the Addr. Out has been recognized by a Ctrl. Unit, OP IN is displayed
Test OP IN	59D	
Test Addr. IN	5A8	Addr. IN on Bus IN can be displayed with FI (Switch E)
Test Addr. Match	5A9	
Command Out	5BD	Command Out stays UP only few microseconds and only Status In, as an answer is displayed. Status on Bus IN can be displayed with FI.
Test Status IN	5C1	
Test Status 0	604	
Service Out	609	Service Out stays Up only few microseconds and only Service IN as an answer is displayed.

SX1:

Address Out	93D	Unit addr. is displayed in Data Reg.
Select Out	9C7	
Address IN	9B5	Address is displayed in A-Reg.
Command Out	94D	Command is displayed in Data Reg.
Status IN	9B3	Status is displayed in R-Reg.
Service Out	9B9	
Service In	9C5	

Note: ROS Addresses can change, depending upon the EC level of CCROS

REG.	Description
TI	Data to A from 1050
TE	Data to 1050 from Z buss
TT	Tags in to A entry

BITS	
0	Cancel
1	RDR 2 Ready
2	End
3	1050 Operational
4	Home start
5	Intervention req.
6	Attention
7	Data check

REG.	
TA	Tags out Z buss to 1050

BITS	
0	Set home RDR start
1	Set RDR 2 to run
2	Force Share Request
3	Set proceed
4	Audible alarm
5	Set carrier return and line feed
6	Attention reset
7	1050 Reset

T REQ to S1, Set S1 on if 1050 share req.

Note: *Indicates that you cannot manually store data in the designated register.

Register to be Displayed	Usual Function	Where Displayed
I	Instruction Address (high-order bits)	A-register (also the high-order eight bits of the main-storage address register if the allow-write indicator is off)
J	Instruction Address (low-order bits)	A-register (also the low-order eight bits of the main-storage address register if the allow-write indicator is off)
U	Data Address (high-order bits)	A-register (also the high-order eight bits of the main-storage address register if the allow-write indicator is off)
V	Data Address (low-order bits)	A-register (also the low-order eight bits of the main-storage address register if the allow-write indicator is off)
L	Data Length	A-register
T	Auxiliary Storage Address	A-register
D	General Purpose Data Register	A-register
R	Storage Data Register	A-register (Also has own display in main-storage data-register indicators)
S	Status (CPU)	A-register
G	Instruction Operation Code	A-register
H	Priority Status Register	A-register
*FI	Multiplexor Channel Bus-In	A-register
*FT	Multiplexor Channel Tags	A-register
Q	Storage-Protection key in PSW (High 4-bits) Storage-Protection key of block of storage just used (low 4-bits)	A-register
*C	Interval Timer Count	A-register
*F	External Interrupt: Interval Timer (bit 0) Console (bit 1) Six direct-control interrupts (bits 2 through 7)	A-register
*TT	1050 Documentary Console Tags	A-register
*TI	1050 Documentary Console Bus-In	A-register
*JI	Direct Control Bus-In	A-register
*GS	Selector Channel One Status	A-register
*GT	Selector Channel One Tags	A-register
*GUV-GCD	GUV contains storage address for data for selector-channel one. GCD contains the current byte count for selector-channel one	GUV in main-storage address register. GCD in count register (18 bits each).
*HS	Selector Channel Two Status	A-register
*HT	Selector Channel Two Tags	A-register

Register to be Displayed	Usual Function	Where Displayed
*HUV-HCD	HUV contains storage address for data for selector-channel two. HCD contains the current byte count for selector-channel two	HUV in main-storage address register. HCD in count register (18 bits each)

Note: *Indicates that you cannot manually store data in the designated register.

The functions of the 1407/1447 in run, character display, and alter modes are available through equivalent procedures on the IBM 1052 Printer Keyboard.

The following list gives the corresponding 1050 operations or indications:

1407/1447 Functions	1050 Equivalents
Request key	Request key
Enter light	Proceed light
Respond key	Operate alternate code key and the 5-key
Type-out key	Not available
Clear key light	During a read-into-storage operation, this function is performed by operating the alternate-code key and the 0-key. During a write-out-of-storage operation, this function is not available.
Cancel key	Cancel key
Release key	EOB key

1	Read
2	Print
3	Print-Read
4	Punch
5	Read-Punch
6	Print-Punch
7	Print-Read-Punch
8	Read Release
9	Punch Release
A	Add
B	Branch
C	Compare
D	Move Digit
E	Edit
F	Form Control
H	Store B Star
K	Stacker Select
L	Load
M	Move
N	No Op
P	Move Record
Q	Store A Star
S	Subtract
U	Unit Control
V	Branch — WM or Zone
W	Branch — Bit Equal
X	Move — Insert Zeros
Y	Move Zone
Z	Move Zero Suppress
.	Stop
□	Clear Wordmark
/	Clear Storage
,	Set Wordmark
%	Divide
#	Modify Address
@	Multiply
?	Zero and Add
!	Zero and Subtract

d CHARACTERS FOR BRANCH

BIId

d-Character	Branch On
b	Unconditional
9	Carriage #9
@	Carriage Channel #12
A	"Last Card" Switch (Sense Switch A)
B	Sense Switch B*
C	Sense Switch C*
D	Sense Switch D*
E	Sense Switch E*
F	Sense Switch F*
G	Sense Switch G*
K	End of Reel * **
L	Tape Transmission Error*
N	Access Inoperable*
?	Reader Error if I/O Check Stop Switch is off**
!	Punch Error if I/O Check Stop Switch is off**
P	Printer Busy (print storage feature)*
‡	Print Error if I/O Check Stop Switch is off**
/	Unequal Compare (B ≠ A)
*	Inquiry Clear*
Q	Inquiry Request*
R	Printer Carriage Busy (print storage feature)*
S	Equal Compare (B=A)*
T	Low Compare (B < A)*
U	High Compare (B > A)*
V	Read-Write Parity Check or Read-Back Check Error*
W	Wrong-Length Record*
X	Unequal-Address Compare*
Y	Any Disk-Unit Error Condition*
Z	Overflow**
%	Processing Check with Process Check Switch off**

* Special Feature.

** Conditions tested are reset by a BRANCH IF INDICATOR ON instruction.

d CHARACTERS FOR BRANCH IF WORDMARK OR ZONE

VIIIBBBd

d-Character	Condition
1	Wordmark
2	No zone (No-A, No-B bit)
B	12-zone (A-B bits)
K	11-zone (B, No-A bit)
S	Zero-zone (A, No-B bit)
3	Either a wordmark, or no zone
C	Either a wordmark, or 12-zone
L	Either a wordmark, or 11-zone
T	Either a wordmark, or zero-zone

d CHARACTERS FOR FORM CONTROL

Fd

d	Immediate skip to	d	Skip after print to
1	Channel 1	A	Channel 1
2	Channel 2	B	Channel 2
3	Channel 3	C	Channel 3
4	Channel 4	D	Channel 4
5	Channel 5	E	Channel 5
6	Channel 6	F	Channel 6
7	Channel 7	G	Channel 7
8	Channel 8	H	Channel 8
9	Channel 9	I	Channel 9
0	Channel 10	?	Channel 10
#	Channel 11	.	Channel 11
@	Channel 12	□	Channel 12

d	Immediate space	d	After print-space
J	1 space	/	1 space
K	2 spaces	S	2 spaces
L	3 spaces	T	3 spaces

BCD TO CM6 CONVERSION
1401 CODE TO SYSTEM/360 CODE

DEF CHAR	CARD CODE	BCD	CM6	CM6 WM
Blank		C	40	00
.	12-3-8	BA8 21	4B	0B
¤	12-4-8	BA84	4C	0C
[	12-5-8	BA84 1	4D	0D
<	12-6-8	BA842	4E	0E
≠	12-7-8	BA8421	4F	0F
&	12	BA	50	10
$	11-3-8	B 8 21	5B	1B
*	11-4-8	B 84	5C	1C
]	11-5-8	B 84 1	5D	1D
;	11-6-8	B 842	5E	1E
Δ	11-7-8	B 8421	5F	1F
-	11	B	60	20
/	0-1	A 1	61	21
,	0-3-8	A8 21	6B	2B
%	0-4-8	A84	6C	2C
V	0-5-8	A84 1	6D	2D
\	0-6-8	A842	6E	2E
≠	0-7-8	A8421	6F	2F
ъ	2-8	A	7A	3A
#	3-8	8 21	7B	3B
@	4-8	84	7C	3C
:	5-8	84 1	7D	3D
>	6-8	842	7E	3E
↰	7-8	8421	7F	3F
?	12-0	BA8 2	C0	80
A	12-1	BA 1	C1	81
B	12-2	BA 2	C2	82
C	12-3	BA 21	C3	83
D	12-4	BA 4	C4	84
E	12-5	BA 4 1	C5	85
F	12-6	BA 42	C6	86
G	12-7	BA 421	C7	87
H	12-8	BA8	C8	88
I	12-9	BA8 1	C9	89
!	11-0	B 8 2	D0	90
J	11-1	B 1	D1	91
K	11-2	B 2	D2	92
L	11-3	B 21	D3	93
M	11-4	B 4	D4	94
N	11-5	B 4 1	D5	95
O	11-6	B 42	D6	96
P	11-7	B 421	D7	97
Q	11-8	B 8	D8	98
R	11-9	B 8 1	D9	99
≠	0-2-8	A8 2	E0	A0
S	0-2	A 2	E2	A2
T	0-3	A 21	E3	A3
U	0-4	A 4	E4	A4
V	0-5	A 4 1	E5	A5
W	0-6	A 42	E6	A6
X	0-7	A 421	E7	A7
Y	0-8	A8	E8	A8
Z	0-9	A8 1	E9	A9
0	0	8 2	F0	B0
1	1	1	F1	B1
2	2	2	F2	B2
3	3	21	F3	B3
4	4	4	F4	B4
5	5	4 1	F5	B5
6	6	42	F6	B6
7	7	421	F7	B7
8	8	8	F8	B8
9	9	8 1	F9	B9

1412, 1418, 1419, 1428 Optical and Magnetic Sorter Readers	(1st)	08
	(2nd)	09
1442 Card/Reader/Punch		0A
1443 Printer		0B
2540 Card Reader (1st)		0C
2540 Card Punch (1st)		0D
1403 Printer (1st)		0E
1403 Printer (2nd)		0F
1403 Printer (3rd)		10
2540 Card Reader (2nd)		12
2540 Card Punch (2nd)		13
2501 Card Reader		14
2520 Card Reader/Punch		15
1285 Roll Reader		16
1231 Page Reader		17
Channel-Channel Adapter		18
2671 Paper Tape Reader		07
1050 Console		1F
2701/2702 Teleprocessing (1st)		20
2701/2703 Teleprocessing (2nd)		30
2400 Magnetic Tapes (1st TAU)		8X
Storage Control		9X
2400 Magnetic Tapes (2nd TAU)		AX

On all stops at ROS address 10FF except for Set-IC and Sense Switch operations, a coded digit is displayed in the main storage data register (MSDR) to indicate the reason for the stop, and all the ALU output register lights are off. The 1400 decimal instruction address is displayed in the BA register lights and the 1400 decimal A-address is displayed in the MN register lights. The 1400 decimal B-address can also be displayed manually in the UV registers by the Normal 2030 procedure.

MSDR	Reason for Stop
00	Normal stop, Appears when the stop is caused by pressing the stop key, ending an instruction-execute in instruction-step mode, or getting a match in SAR Delayed-Stop mode.
01	Attempted to use invalid 1400 B-address.
02	Attempted to use invalid 1400 A-address.
03	Attempted to use invalid 1400 A- and B-address.
04	Attempted to use invalid 1400 operation code.
05	Invalid I/O operation attempted; either unit selection or unit number invalid.
06	Storage wrap occurred when address was used, which was outside of system capacity.
07	Storage protection occurred in 1400 mode.
08	Attempted to switch to 2030 mode without the PMS feature.
09	Invalid source or destination address on one of the special PMS tape operations.
0A	Attempted to convert to binary an address that was less than the bias (offset) address on a clear storage or store STAR operation.
0B	Storage wrap-around 1400-address 0000.
0C	Attempted to start a 1400 I-cycle at main storage address 0000.

1400 COMPATIBILITY PROGRAMMED AND ERROR STOPS
[continued]

MSDR	Reason for Stop
0E	Attempted to index without advanced programming comment in CID.
10	FILE - Read-back check stop.
11	1050 - Some other device attempted to take a multiplexor channel data cycle while in the data-transfer portion of a 1050 operation.
20	FILE - No channel or device ends received.
21	Word mark missing from 1400 operation code during I-Op.
22	TAPE-SM Channel - Wrong address sent back from channel.
30	FILE - Wrong address sent back from the channel.
31	Word mark in A-address of an I/O instruction.
3F	2540 or 2501 reader error, or invalid character occurred. *
40	FILE - Unit check status response to seek command.
41	An 8F character was detected at an address other than the offset address while in 1400 mode.
42	TAPE - SM Channel - Invalid channel status on data transfer.
4F	1442 - Reader intervention required. * 2540 or 2501 - Reader intervention required. *
50	FILE - Operational interlock.
51	An I/O operation was attempted on a device for which the compatibility feature is not installed.
52	TAPE - SM Channel - Device end signal before encountering a GMWM or a tape write operation.
55	A 1400 start reset function was performed using the console interrupt key.
5F	1442 - Punch intervention required. * 2540 - 2520 Punch intervention required. *

1400 COMPATIBILITY PROGRAMMED AND ERROR STOP
[continued]

MSDR	Reason for Stop
60	Module mis-match detected
61	Sterling Process check marked misalignment.
62	TAPE - S Channel - Status in and service in on a tape write. M Channel - Operational in disconnect on a tape write.
6F	1403 - 1443 - Printer intervention required. *
71	Sterling Process check, invalid character.
7F	2540 - Select stacker instruction given after maximum time-out. *
80	1442/1443 - Wrong address sent back from the channel. 2540 (or 2501 and 2520)/1403 - No address compare, or punch-transfer error.
81	Sterling marked in add or subtract pence or shilling position.
82	TAPE - S Channel - Status in and service in on a read move operation.
8F	TAPE - SM Channel - Tape-unit intervention required. *
90	2540/2501 - Operation-in disconnect on reader. 1442/1443 - Invalid d-modifier
92	TAPE - SM Channel - Error on a 1400 tape initial program load.
A0	1442/1443 - No GMWM in storage. 1403 - Operational-in disconnect
A2	TAPE - S Channel - Invalid channel status was received on a branch if error operation.
B0	2540/2520 - Operational-in disconnect or punch. 1442 - Error on read or punch operation.
B2	TAPE - S Channel - Status in and service in on a 1400 read load operation.
C2	TAPE - M Channel - Operational in disconnect on a read operation.

MSDR	Reason for Stop
CF	1050 - Intervention required. *
D2	TAPE - M Channel - Premature end to a sense operation.
DF	1050 - Alter or display stop. **
E2	TAPE - M Channel - Operational in disconnect on mode set operation.
F0	A 1400 halt instruction performed satisfactorily.
F1	A 1400 halt instruction performed satisfactorily. (Address in B-Star is invalid)***
F2	A 1400 halt instruction performed satisfactorily. (Address in A-Star is invalid)***
F3	A 1400 halt instruction performed satisfactorily. (Address in A & B Star is invalid)***
FF	A 1400 halt and branch instruction has been executed.

* On these stops the operator may correct the condition and then try the instruction that caused the stop by again pressing the 2030 console start key.

** Restart by pressing the 2030 start key.

*** Information described in parentheses indicate the validity of the A & B Star when a 1401 halt operation is performed. These statements do not indicate a machine failure.

S Selector channel.

M Multiplexor channel.

BIT ASSIGNMENTS FOR BYTES IN 1401 BUMP (2030 AUX. STOR.) K ADDRESSABLE BYTES

BIT		CPU
"XX98"	0	A-Last Card Sense Sw
	1	B-Sense Switch
	2	C-Sense Switch
	3	D-Sense Switch
K8	4	E-Sense Switch
	5	F-Sense Switch
	6	G-Sense Switch
	7	
"XX99"	0	U-Hi
	1	/-≠ Not Equal
	2	T-Lo
	3	S- = Equal
K9	4	
	5	Z- Overflow
	6	Q- Inq Request
	7	
"XX9A"	0	1 for 64K
	1	1 for 32K, 64K
	2	1 for 16K, 32K, 64K
	3	1
K10	4	1
	5	1
	6	1
	7	1 except for 64K
"XX9B"	0	X-Unequal Addr. Compare
	1	\-Access Busy
	2	W-Wrong Length Record
	3	Y-Any Disk Cond
K11	4	V-Disk Error
	5	N-Access Inop
	6	RBC Interlock
	7	End Alternate Track
"XX9C"	0	IO Check Stop
	1	Adv Prog Feature
	2	Expanded Edit
	3	Mode Sw on Inv Ops
K12	4	
	5	Mode Sw on Halt
	6	Tape on SX2
	7	Mode Sw on Error Stops
"XX9D"	0	Mode Sw on Inv IO Ops
	1	Mode Sw on Console Ops
	2	Mode Sw on Printer Ops
	3	Mode Sw on Rdr/Pch Ops
K13	4	
	5	Mode Sw on Tape Ops
	6	Mode Sw on File Ops
	7	
"XX9E"	0	
	1	
	2	
	3	
K14	4	
	5	
	6	
	7	
"XX9F"	0	
	0	
*	1	
	2	
	3	Alt 9 Track Mode
K15	4	0
	5	Allow IO Traps
	6	0
	7	0

BIT		MPX/UCW	
		1402/1403	1442/1443
"XX89"	0		
	1	51 Column	
	2		
	3		
K1	4	Reader Address	Reader 1 Address
	5		
	6		
	7		
"XX8A"	0		
	1	TEMPORARY FORMS INFORMATION	TEMPORARY FORMS INFORMATION
	2		
	3		
K2	4		
	5	Initialize to 08	Initialize to 00
	6		
	7		
"XX8B"	0		
	1		
	2		
	3		
K3	4	Punch Address	"13" or "39" Char Bar
	5		
	6		
	7		
"XX8C"	0	132 Print Pos	
	1		
	2		
	3		
K4	4	Printer Address	Reader 2 Address
	5		
	6		
	7		
"XX8D"	0		
	1	Temporary Stacker-	
	2	Select Information	
	3		
K5	4	Initialize to-	Printer Address
	5	ID for 2540	
	6	0D for 2501-2520	
	7		
"XX9A"	0	Last Op was Fwd Sp Rec.	
	1	This Op is Fwd Sp Rec.	
	2	Erase Latch	
K10	3		
	4	1050 Error	
	5	Reader Error	
	6	Punch Error	
	7	Printer Error	
"XX9F"	0		
	1		Load Mode
	2		Type "H" Ball on 1052
K15	3		
	4		
	5		
	6		
	7		

* Addresses are as shown for CPU-L.S. or MPX - i.e. "XX9F" is address of K15 CPU-L.S.

LOCAL STORAGE - 1401 MODE

			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1401 AUX STORAGE A - CPU	UNITS	0X	00	01	02	03	04	05	06	07	08	09	F0	F3	F4	F5	F6	F7
	TENS	1X	00	(0A)X	(14)X	(1E)X	(28)X	(32)X	(3C)X	(46)X	(50)X	(5A)X	10	10	10	10	10	10
	HUNDS-LO	2X	(Y)X	(Y+64)X	(Y+C8)X	(Y+2C)X	(Y+90)X	(Y+F4)X	(Y+58)X	(Y+BC)X	(Y+20)X	(Y+84)X	10	10	10	10	10	10
	BIN DEC	3X	00	61	23	84	46	08	69	31	82	44	06	67	29	90	52	14
	SCD NPL	4X	40	F1	F2	F3	F4	F5	F6	F7	F8	F9	F0	7B	7C	7D	7E	7F
		5X	7A	61	E2	E3	F4	E5	E6	E7	E8	F9	E0	6B	6C	6D	6E	6F
		6X	60	D1	D2	D3	D4	D5	D6	D7	D8	D9	D0	5B	5C	5D	5E	5F
		7X	50	C1	C2	C3	C4	C5	C6	C7	C8	C9	C0	4B	4C	4D	4E	4F
		8X	Tape CH		TAPE					Tape Stat	0	1	2	3	4	5	6	7
		9X	CARD LOAD I	CARD LOAD J	TAPE LOAD I	TAPE LOAD J			RPQ	9 TRK TAPE FLAG	8	9	10	11	12	13	14	15
		AX	WORKING STORAGE								16	17	18	19	20	21	22	23
		BX									24	25	26	27	28	29	30	31
	BIT SIGNIFICANT OP CODE TABLES	CX	?)1C	A)18	B)08	C)1F	D)12	E)16	F)2A	34	H)B1	34	34	,)02	#)15	34	34	34
		DX	I)1D	34	K) 29	L) 90	M) 80	N) 06	34	P) 1E	Q)F1	34	34	34	34	34	34	34
		EX	34	/)05	S)19	34	U)20	V)3A	W)3B	34	Y)13	Z)17	34	,)04	%)1B	34	34	34
		FX	34	1) 21	2) 22	3) 23	4) 24	5) 25	6) 26	7) 27	8) 06	9) 06	34	#) 14	@)1A	34	34	34
1401 AUX STORAGE B-UCW	HUNDS - HI	0X	00	05	01	06	02	07	03	08	04	09						
		1X																
		2X	Z+C	Z+00+C	Z+00+C	Z+01+C	Z+01+C	Z+01+C	Z+02+C	Z+02+C	Z+03+C	Z+03+C						
		3X																
	NPL BCD NOTE 5	4X	00	40	40	4B	4C	40	40	40	40	40	40	3B	3C	3D	3E	3F
		5X	30	40	40	5B	5C	40	40	40	50 (A) 4E (H)	40	40	2B	2C	2D	2E	2F
		6X	20	11	40	6B	6C	40	40	40	60	61	40	1B	1C	1D	1E	1F
		7X	40	40	4E (A) 50 (H)	7B	7C	40	40	40	40	40	10	OB	OC	OD	OE	OF
		8X	FILE SENSE 0	FILE SENSE 1	FILE SENSE 2	FILE SENSE 3					0	1	2	3	4	5	6	7
		9X	FILE UNIT 0 ADDR	UNIT 0 CYC	FILE UNIT 1 ADDR	UNIT 1 CYC	FILE UNIT 2 ADDR	UNIT 2 CYC	FILE UNIT 3 ADDR	UNIT 3 CYC	8	9	10	11	12	13	14	15
		AX	CYC # 00	CYC # 32	CYC # 0A	CYC # 3C	CYC # 14	CYC # 46	CYC # 1E	CYC # 50	16	17	18	19	20	21	22	23
		BX	H	R	00	DL	DL				24	25	26	27	28	29	30	31
	NPL BCD	CX	3A	31	32	33	34	35	36	37	38	39	40	50 (A) 4E (H)	40	48	4C	56
		DX	2A	21	22	23	24	25	26	27	28	29	40	60	40	40	46	5D
		EX	1A	40	12	13	14	15	16	17	18	19	40	4E(A) 50(H)	40	49	4F	56
		FX	0A	01	02	03	04	05	06	07	08	09	40	F0	40	40	44	5F

NOTES: 1. X Indicates the quantity in parenthesis is crossed in the table
2. Z = Memory Bias-Hi
3. Y = Memory Bias-Lo
C = Carry from addition to get entry in Hunds-Lo Table
4. A = 1403 A Chain
H = 1403 H Chain
5. See 1443 Load Variations Table

K ADDRESSABLE BYTE UTILIZATION

	CPU		UCW
0	I BACK-UP	0	ERROR CODE
1	J BACK-UP	1	
2	U BACK-UP	2	USED BY
3	V BACK-UP	3	1402 -03
4	L BACK-UP	4	1442 -43
5	T BACK-UP	5	
6	G BACK-UP	6	0 STAR H1
7	S BACK-UP	7	0 STAR L0
8	SENSE SW BYTE	8	FILE UNIT 4 ADDR
9	HI-LO EQ BYTE	9	UNIT 4 CYLINDER
10	MEM SIZE BYTE	10	I/O ERROR

	CPU		UCW
11	FILE BR BYTE	11	TAPE TRK IN ERROR
12	1401 CONTROL	12	
13	PMS CONTROL	13	A HUNDS BACK-UP
14	D BACK-UP	14	B HUNDS BACK-UP
15	ALLOW I/O TRAPS	15	1050 STATUS
16	WORKING STORAGE	16	CYL #28
17	WORKING STORAGE	17	CYL #5A
18	WORKING STORAGE	18	PREVIOUS FILE OPER
19	WORKING STORAGE	19	RESERVED FOR 1402 -03
20	CONSTANT 1F	20	00
21	STERLING FEAT	21	00

	CPU		UCW
22	STERLING FEAT	22	C
23	STERLING FEAT	23	H
24	STERLING FEAT	24	WORKING STORAGE
25	1400 TAPE	25	WORKING STORAGE
26	CONSTANT-OF	26	WORKING STORAGE
27		27	WORKING STORAGE
28		28	WORKING STORAGE
29		29	WORKING STORAGE
30	CONSTANT-2E	30	WORKING STORAGE
31	RPQ	31	WORKING STORAGE

DEFINITIONS OF ALD PAGE NUMBER PREFIXES

A.	Adders	
	1. Addressing Adder	AA-AB
	2. IC Incrementer	AC-AD
	3. Exponent Adder	AE-AF
	4. Main Adder	AM-AQ
	5. Serial Adder	AS
	6. VFL and DEC Adder	AV-AW
B.	Decoders	
	1. Op Decoders	DN
	2. FLP and Gen. Decoder	DP
	3. Addressing and Pre FTH	DA
	4. Trap Decode	DB
	5. Reg Decode	DG
	6. ROM Decode	DR-DS
C.	Counters	
	1. Instruction Ctrs.	CA-CB
	2. Local Store Address Ctr.	CC-CD
	3. Misc. Ctr.	CE-CZ
D.	Busing (Excluding Memory Bus)	BA-BZ
E.	Registers	
	1. A-Reg.	RA
	2. B Reg.	RB
	3. D Reg.	RD
	4. E Reg.	RE
	5. F Reg.	RF
	6. G Reg.	RG
	7. H Reg.	RH
	8. J Reg.	RJ
	9. K Reg.	RK
	10. L Reg.	RL
	11. M Reg.	MA
	12. N Reg.	MA
	13. P Reg.	RP
	14. Q Reg.	KW
	15. R Reg.	MB
	16. S Reg.	RS
	17. T Reg.	RT
	18. U Reg.	RU
	19. V Reg.	RV
	20. W Reg.	RW
	21. X Reg.	RX
	22. VFL and Decoder Reg, Mod. 70	RY
	23. Direct Data Reg	RZ
	24. MC Reg.	KR
F.	Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Busses, SAR, SBI "OR", M and N Regs in Mod. 30)	MA-MC
G.	Controls	
	1. Advance or Seq Cntls	KA
	2. Branch and IC Cntls	KB
	3. Clock Cntls	KC
	4. 1 Exec (Mod 70) 1 Fetch & Exec (Mod. 60)	KD
	5. Chan Cntrls	KE
	6. Fix Seq Cntls	KF
	7. Gen Reg Cntls	KG
	8. FLT Cntls	KH
	9. ROS Cntls	KK
	10. Local Store Cntls	KL
	11. Priority and Interrupt Cntls	KM
	12. I/O Instr Cntls	KN
	13. VFL Cntls	KP
	14. VFL Cntls	KQ
	15. Check Triggers	KR
	16. Status Triggers	KS
	17. VFL Cntls & Decimal Cntls	KY
	18. Any Misc. Cntls such as FP	KT-KU
	19. Fixed Pt, Storage Protect, Real Time clk, Status Cntls	KW-KZ
H.	Consoles	PA-PE, PJ-PZ
	1052 Console Adapter	PF, PG, PH
I.	Local Store	LS-LT
J.	TROS	EA-EC
K.	CROS	ED-EF
L.	Spec. Features	XA-XZ
M.	Hardware Oriented Pages	ZA-ZZ
N.	I/O Channels	
	Multiplex Channel	FA-FZ
	Selector Channel No. 1	GA-GZ
	Selector Channel No. 2	HA-HZ
	Direct Data	JA-JZ
O.	ROS Flow charts	QA-QZ
P.	Power Supplies	YA-YZ

1620 Op Codes and Their Equivalent Bit Significant Translated Codes from the MPX Auxiliary Storage Area.

The Translated Code is read from the MPX Auxiliary Storage Area by using the 1620 Code as the Low Order Digits of the Read-out Address.

Instruction	Mnemonic	1620 Code	Xlated Code
Add	A	21	2C
Add (1)	AM	11	AC
AND to Field	ANDF	93	19
Branch	B	49	A4
Branch Back	BB	42	F0
Branch Conditionally and Modify Index Register	BCX	63	DA
Branch Conditionally and Modify Index Register (1)	BCXM	64	DB
Branch on Bit	BBT	91	61
Branch on Digit	BD	43	64
Branch Indicator	BI	46	EC
Branch and Load Index Register	BLX	65	D6
Branch and Load Index Register (1)	BLXM	66	D7
Branch on Mark	BMK	91	61
Branch and Modify Index Register	BX	61	D8
Branch and Modify Index Register (1)	BXM	62	D9
Branch No Flag	BNF	44	40
Branch No Group Mark	BNG	55	62
Branch No Indicator	BNI	47	EE
Branch No Record Mark	BNR	45	60
Branch and Select	BS	60	C0
Branch and Store Index Register	BSX	67	D4
Branch and Transmit	BT	27	00
Branch and Transmit (1)	BTM	17	80
Branch and Transmit Address	BTA	20	02
Branch and Transmit Address (1)	BTAM	10	82
Branch and Transmit Floating	BTFL	07	03
Clear Flag	CF	33	84
Compare	C	24	0E
Compare (1)	CM	14	8E

CLF 201 1620 OP CODES
(continued)

Instruction	Mnemonic	1620 Code	Xlated Code
Complement Octal Field	CPLF	94	13
Control	K	34	E8
Decimal to Octal Conversion	DTO	97	B6
Divide	D	29	3E
Divide (1)	DM	19	BE
Dump Numerically	DN	35	E2
Exclusive OR to Field	EORF	95	1A
Floating Add	FADD	01	0C
Floating Divide	FDIV	09	08
Floating Multiply	FMUL	03	09
Floating Shift Left	FSL	05	33
Floating Shift Right	FSR	08	2F
Floating Subtract	FSUB	02	0D
Halt	H	48	F8
Load Dividend	LD	28	15
Load Dividend (1)	LDM	18	95
Move Address	MA	70	1C
Move Flag	MF	71	14
Multiply	M	23	16
Multiply (1)	MM	13	96
No Operation	NOP	41	F4
Octal to Decimal Conversion	OTD	96	17
OR to Field	ORF	92	18
Read Alphamerically	RA	37	E5
Read Binary Paper Tape	RBPT	37	E5
Read Numerically	RN	36	E7
Seek	SK	34	E8
Set Flag	SF	32	86
Subtract	S	22	2D
Subtract (1)	SM	12	AD
Transfer Numerical Fill	TNF	73	34
Transfer Numerical Strip	TNS	72	0F
Transmit Digit	TD	25	1F
Transmit Digit (1)	TDM	15	9F
Transmit Field	TF	26	30
Transmit Field (1)	TFM	16	B0
Transmit Floating	TFL	06	01
Transmit Record	TR	31	1E
Transmit Record No RM	TRNM	30	1D
Write Alphamerically	WA	39	E4
Write Numerically	WN	38	E6

When the system stops in 1620 mode, the low-order byte of the Main Storage Address Register (MSAR) displays a stop code for the programmed or error stop. The appropriate operator action required to restart the system is given here.

* These stops are initiated only by the I/O Control Program.

MSAR	Reason for Stop	Operator Action
01	Correct switch F or G function executed	Press Start for NSI
02	Incorrect switch F or G function executed	Check switches, or press Start for NSI
03	Entry into 1620 mode executed	Press Start for NSI
07	Console stop key pressed, or rate switch set to INSTR STEP position	Set switch to process, or press Start for NSI
1F	Exponent flag error	Press Start for NSI
20*	Invalid Typewriter control	Press Start for NSI
21*	No device address	Reload IOCP and restart System/360 program load
22*	Machine check	Load SEREP program for analysis of machine malfunction
2F	Mantissa-length error (not equal, too long)	Press Start for NSI
30*	I/O release (attention bit on)	Press Start for NSI
31	Invalid decimal data used in DTO	Press Start for NSI
33*	Program check (in IOCP)	Reload IOCP and restart System/360 program load
3F	Floating-point address check	Press Start for NSI

PROGRAMMED AND ERROR STOPS
(continued)

MSAR	Reason for Stop	Operator Action
F1	Right-to-left "wipe-out" attempted, or an even alpha address used in TNF operation	Press Start for NSI
F3*	Typewriter not ready (read)	Ready the I/O device and press Start for NSI. (See Note.)
F4*	Typewriter not ready (write)	Ready the I/O device and press Start for NSI. (See Note.)
F5*	Paper tape reader not ready	Ready the I/O device and press Start for NSI. (See Note.)
F6*	Card punch not ready	Ready the I/O device and press Start for NSI. (See Note.)
F7*	Card reader not ready	Ready the I/O device and press Start for NSI. (See Note.)
F8*	Printer not ready	Ready the I/O device and press Start for NSI. (See Note.)
F9*	Disk drive 0 not ready	Ready the I/O device and press Start for NS1. (See Note.)
FA*	Disk drive 1 not ready	Ready the I/O device and press Start for NSI. (See Note.)
FB*	Disk drive 2 not ready	Ready the I/O device and press Start for NSI. (See Note.)

PROGRAMMED AND ERROR STOPS
(continued)

MSAR	Reason for Stop	Operator Action
41	Quotient wrap-around	Press Start for NSI
44*	Invalid input command	Press Start for NSI
48	Halt instruction executed	Press Start for NSI
4F	Storage wrap-around in transmit field	Press Start for NSI
51	Invalid decimal digit used as P-field data in an ADD,SUBTRACT, or COMPARE operation	Press Start for NSI
55*	Incorrect I/O device code	Press Start for NSI
5F	Field length greater than 255 characters in TFL, BTFL, BTA, or BTAM operation	Press Start for NSI
61	Divide P-address is not less than 99	Press Start for NSI
6F	No BT (or BTM) given before a BB instruction	Press Start for NSI
71	Storage wrap-around detected in sign and field-length operation	Press Start for NSI
77*	Error in reading overlay from disk	Press Start to try operation again
7F	Invalid band 0 selection	Press Start for NSI
81	Storage wrap-around detected in a logic operation	Press Start for NSI
88*	Paper tape overrun condition. (See IBM 2671 Paper Tape Reader section)	Press Start for NSI
8F	Storage wrap-around on index execute	Press Start for NSI
90	Specified sector count is invalid	Press Start for NSI

PROGRAMMED AND ERROR STOPS
(continued)

MSAR	Reason for Stop	Operator Action
91	Field longer than 255 digits detected in sign and field length routine	Press Start for NSI
9F	Invalid modifier in BRANCH AND SELECT (BS) instruction	Press Start for NSI
A0	Specified storage address is odd	Press Start for NSI
AF	Branch to an odd location attempted	Press Start for NSI
B0	Write-address switch is on	Press Start for NSI The instruction causing this stop is not executed.
B1	Storage wrap-around detected on a right-to-left operation	Press Start for NSI
C0	Write-address switch is on	Press Start for NSI The instruction causing this stop is not executed.
C1	Invalid decimal digit used in multiplicand (P-field)	Press Start for NSI
CF	Invalid address used or addressed location not is mapped storage area	Press Start for NSI
D0	Disk-control field is at an odd address	Press Start for NSI
D1	Invalid decimal digit used in multiplier (Q-field)	Press Start for NSI
DF	Address wrap-around attempted	Press Start for NSI
E0	I/O operation code incorrect	Press Start for NSI
E1	Product area wrap-around	Press Start for NSI
EF	Invalid operation code used	Press Start for NSI

PROGRAMMED AND ERROR STOPS
(continued)

MSAR	Reason for Stop	Operator Action
FC*	Disk drive 3 not ready	Ready the I/O device and press Start for NSI. (See Note.)
FE	Left-to-right "wipe-out" executed	Press Start for NSI

ROS CONTROL FIELD CHANGES

ROS Field Changes			
ROS Field	Decode	Normal Function	Compatibility Function
CH	3	V00	S1
	4	STI	RHVDD
	5	OPI	RLVDD
	8	SI	R2
CL	3	AI	RL = E
	4	SVI	G1
	6	1BC	R1
	C	G1	R3
CM	5	T→MN	LT→MN
CS	5	TREQ→S1	1→S1
	F	K→FA	0→S1

General Register 8 Routine Pointer	General Register 7 Device Code Pointer	Function
12	00	Alpha Input for Typewriter
12	0A	Alpha Input for Card Reader
12	06	Alpha Input for Paper Tape
14	00	Numeric Input for Typewriter
14	0A	Numeric Input for Card Reader
14	06	Numeric Input for Paper Tape
06	02	Alpha Output for Typewriter
06	08	Alpha Output for Card Punch
06	12	Alpha Output for Printer
0A	02	Numeric Output for Typewriter
0A	08	Numeric Output for Card Punch
0A	12	Numeric Output for Printer
0E	02	Dump Numeric for Typewriter
0E	12	Dump Numeric for Printer
0E	08	Dump Numeric for Card Punch
00	02	Typewriter Control
02	12	Printer Control Immediate
04	12	Printer Control Delayed
08	12	Alpha Output/Space Supp. for Printer
10	12	Dump Numeric/Space Supp. for Printer
0C	12	Numeric Output/Space Supp. for Printer
18	06	Binary Input for Paper Tape

ROUTINE POINTERS

Pointers	Routine
Non Disk	
00	Typewriter Control
02	Printer Control Immediate
04	Printer Control Delayed
06	Alpha Output
08	Alpha Output with Printer Space Suppress
0A	Numeric Output
0C	Numeric Output with Printer Space Suppress
0E	Dump Numeric
10	Dump Numeric with Printer Space Suppress
12	Alpha Input
14	Numeric Input
16	Invalid
18	Binary Paper-Tape Input
Disk	
5A	Seek
00	Read Disk - Sector Mode
02	Write Disk - Sector Mode
04	Check Disk - Sector Mode
20	Read Disk, SLRC - Sector Mode
22	Write Disk, WLRC - Sector Mode
24	Check Disk, WLRC - Sector Mode
00	Read Disk - Track Mode
04	Write Disk - Track Mode
08	Check Disk - Track Mode
0C	Read Disk, WLRC - Track Mode
10	Write Disk, WLRC - Track Mode
14	Check Disk, WLRC - Track Mode
18	Return to 1620 I-Cycles

INITIALIZATION MESSAGE

Code	Message
01A	Non-Control Card Received
02A	Operation Field Error
03A	No Blank in Operand Field
04A	ASSGN Card Operand Error
05A	CONFG Card Operand Error
06A	S/360 or 1620 Size Error
07A	EMEND Card Operand Error
08A	Card Reader Error
09A	Disk Read Error

DISK FORMAT MESSAGE

Code	Message
01A	Disk Drive not Ready
02A	Card Reader not Ready
03A	360 Disk Address not Specified
04A	Disk Write Error
05A	Card Read Error
06A	Control Card Error
07A	End-of-Job
08A	First Card of this Section in Error
09A	Card was not ASSEM output Card
10A	No End Card for this Section

Notes:

1. A flagged character is generated by typing the flag (shift W) and then the Character. The printed image is, for example, ⁸0.
2. The first output character is for Write Numeric (operation code 38). The second character is for Dump Numeric (operation code 35).
3. In contrast to the IBM 1620, the Dump output onto cards for a flagged zero is 11-0 (same a Write Numeric).
4. If an invalid input character is encountered, the read-check indicator (06) is turned on.

The 1620 Compatibility Feature input/output codes and graphics that are compatible with the IBM 1620 system are shown in the following two figures.

1620 Char	1620 Compat Feature Digit (Hex)	INPUT					OUTPUT		
		Typewriter	Card	Paper Tape			Typewriter	Card	Printer
0	0	0 or Blank	0 or 12-0 or Blank	0	C	C01	0	0	0
1	1	1 or A or /	1 or A or /	1	X01	C01	1	1	1
2	2	2 or B or S	2 or B or S	2	X02	C02	2	2	2
3	3	3 or C or T	3 or C or T	C21	CX021	021	3	3	3
4	4	4 or D or U	4 or D or U	4	X04	C04	4	4	4
5	5	5 or E or V	5 or E or V	C41	CX041	041	5	5	5
6	6	6 or F or W	6 or F or W	C42	CX042	042	6	6	6
7	7	7 or G or X	7 or G or X	421	X0421	C0421	7	7	7
8	8	8 or H or Y	8 or H or Y	8	X08	C08	8	8	8
9	9	9 or I or Z	9 or I or Z	C81	CX081	081	9	9	9
-0	Flagged 0	⁸0 or -or+ ①	11-0 or & or -	CX0	X		0	11-0 ③	-
-1	Flagged 1	⁸1 or J	J	CX1			1	J	J
-2	Flagged 2	⁸2 or K	K	CX2			2	K	K
-3	Flagged 3	⁸3 or L	L	X21			3	L	L
-4	Flagged 4	⁸4 or M	M	CX4			4	M	M
-5	Flagged 5	⁸5 or N	N	X41			5	N	N
-6	Flagged 6	⁸6 or O	O	X42			6	O	O
-7	Flagged 7	⁸7 or P	P	CX421			7	P	P
-8	Flagged 8	⁸8 or Q	Q	CX8			8	Q	Q
-9	Flagged 9	⁸9 or R	R	X81			9	R	R
ǂ	A	ǂ	8-2 or 0-8-2	082			Terminate/ǂ ②	0-8-2	Terminate/Z ②
ǂ	Flagged A	⁸ǂ	11-8-2	X82			Terminate/ǂ	11-8-2	Terminate/W
	B	= or . or ,	# or . or ,	821			Terminate/#	0-8-2	Terminate/Z
	Flagged B	$	$	CX821			Terminate/$	11-8-2	Terminate/W
Numeric Blank	C	@ or ¤ or) or (	@ or ¤ or %	C84	CX084	084	@	Blank/@	Blank/@
Flagged Numeric Blank	Flagged C	*	*	X84			⁸@	Blank/*	Blank/*
ǂ	F	ǂ	0-8-7	08421			Terminate/ǂ	0-8-7	Terminate/G
ǂ	Flagged F	⁸ǂ	12-8-7	X8421			Terminate/ǂ	12-8-7	Terminate/X
Invalid Input ④	0	Any Other	Any Other	Any Other					

Notes: 1. If an invalid input character is encountered, the read-check indicator (06) is turned on.

2. If an invalid output character is encountered, the write-check indicator (07) is turned on.

3. An x denotes any hexadecimal character except 0 or 5.

1620 Char	1620 Compat Feature Digit (Hex)	INPUT			OUTPUT				
							Printer		
		Typewriter	Card	Paper Tape	Typewriter	Card	1443	1403 AN	1403 HN
Blank	00	Blank	Blank	C	Blank	Blank	Blank	Blank	Blank
	02	None	None	None	■	0-8-2	?	Blank	Blank
.	03	.	.	X0821	.	.	.	.	.
)	04	)	¤	CX084	)	¤	)	¤	)
+	10	&	&	CX0	&	&	&	+	+
	12	None	None	None	■	11-8-2	1	-	-
$	13	$	$	CX821	$	$	$	$	$
*	14	*	*	X84	*	*	*	*	*
-	20	-	-	X	-	-	-	-	-
/	21	/	/	C01	/	/	/	/	/
	22	None	None	None	≠	0-8-2	≠	Blank	Blank
,	23	,	,	C0821	,	,	,	,	,
(	24	(	%	084	(	%	(	%	(
	26	None	None	C0842	■	Blank	Blank	Blank	Blank
=	33	=	#	821	=	#	=	#	=
@	34	@	@	C84	@	@	@	@	'
	35	None	None	None	■	5	:	0	0
A...1	41...49	A...1	A...1	X01...CX081	A...1	A...1	A...1	A...1	A...1
	50	None	11-0	None	-	11-0	-	-	-
J...R	51...59	J...R	J...R	CX1...X81	J...R	J...R	J...R	J...R	J...R
	61	None	None	None	Z	/	/	/	/
S...Z	62...69	S...Z	S...Z	C02...081	S...Z	S...Z	S...Z	S...Z	S...Z
0	70	0	0 or 12 - 0	0	0	0	0 ↖	0	0
1...9	71...79	1...9	1...9	1...C81	1...9	1...9	1...9	1...9	1...9
ǂ	0A	ǂ	8 - 2 or 0 - 8 - 2	082	Terminate	0 - 8 - 2		Terminate	
	0B	None	11 - 8 - 2	None	Terminate	0 - 8 - 2		Terminate	
	xA ③	None	None	None	Terminate	0 - 8 - 2		Terminate	
	xB	None	None	None	Terminate	0 - 8 - 2		Terminate	
ǂ	5A	ˇǂ	11 - 8 - 2	X82	Terminate	11 - 8 - 2		Terminate	
	5B	None	None	None	Terminate	11 - 8 - 2		Terminate	
ǂ	0F	ǂ	0 - 8 - 7	08421	Terminate	0 - 8 - 7		Terminate	
	xF	None	None	None	Terminate	0 - 8 - 7		Terminate	
ǂ	5F	ˇǂ	12 - 8 - 7	X8421	Terminate	12 - 8 - 7		Terminate	
Invalid Input ①	00	Any Other	Any Other	Any Other					
Invalid Output ②	Any Other				■	Blank		Blank	

Converting 1620 Decimal Addresses to 1620-Mode Hexadecimal Addresses

a	b	c	d		
1620 Address (Dec.)		Note 1.		20K Constant	1620 Digit Address (Hex.)
00000/2 =	00000	(0)	0000	+ 0E00 =	0E00 (high)
00843/2 =	00421	(1)	01A5	+ 0E00 =	01A5 (low)
19999/2 =	09999	(1)	270F	+ 0E00 =	350F (low)
a	e	f	g		
1620 Address (Dec.)		Note 2.		20K Constant	1620 Flag Address (Hex.)
00000/8 =	00000	(0)	0000	+ 3600 =	3600, bit 0
00843/8 =	00105	(3)	0069	+ 3600 =	3669, bit 3
19999/8 =	02499	(7)	09C3	+ 3600 =	3FC3, bit 7

Note 1: If there is a remainder, the digit portion of this 1620 character is placed in the four high-order bits of the 2030 byte.

Note 2: The remainder of this division identifies the bit-position within the flag byte.

Converting 1620-Mode Hexadecimal Effective Addresses to Actual 1620 Decimal Addresses (Digit and Flag Portions)

k		m	n		p		
1620 Digit Address (Hex.)	20K Constant					Note 1.	Actual 1620 Address (Decimal)
0E00 (high)	- 0E00 =	0000	00000	x 2 =	00000	+ 0 =	00000
0FA5 (low)	- 0E00 =	01A5	00421	x 2 =	00842	+ 1 =	00843
350F (low)	- 0E00 =	270F	09999	x 2 =	19998	+ 1 =	19999

r		s	t		u		
1620 Flag-Byte Address (Hex.)	20K Constant					Note 2.	Actual 1620 Address (Decimal)
3600, bit 0	- 3600 =	0000	00000	x 8 =	00000	+ 0 =	00000
3669, bit 3	- 3600 =	0069	00105	x 8 =	00840	+ 3 =	00843
3FC3, bit 7	- 3600 =	09C3	02499	x 8 =	19992	+ 7 =	19999

Note 1: Add 1 if the 1620 address was contained in the low-order four bits of the 2030 digit byte.

Note 2: Add the bit-position number that represents the flag-bit's location within the flag byte.

ADDITIVE CARD CODE (ACC)
(ALD FEATURE ASSIGNMENTS)

Code	Feature
	Basic
ADA	1051 Attachment
ADFT	1051, First on Line
ADLT	1051, Last on Line
BAE3	Basic to Board B-E3
CBS1	1401/1440/1460 Basic Compatibility
CHC	Channel to Channel Adapter
DCT	Direct Control
EIC	External Interrupt
SC0	Selector Channel, First
SC1	Selector Channel, Second
SC0*	No Selector Channel, Second
ST0	Storage 8K Model C
ST1	Storage 16K Model D
ST2	Storage 32K Model E
ST3	Storage 64K Model F
STC0	Storage Protect and Sel Ch, First
STC1	Storage Protect and Sel Ch, Second
STP	Storage Protection
TIM	Interval Timer
HSMX	High Speed MPXR Ch
HMC0	High Speed MPXR Ch or Sel Ch, First
HMC1	High Speed MPXR Ch or Sel Ch, Second

ROS PAGE ASSIGNMENTS

QA001 - QA151	Instruction Cycles
QA161 - QA251	Branches, Storage Protect
QA261 - QA301	Converts
QA311 - QA401	Shifts
QA411 - QA501	Fixed Point Arithmetic, Logics, Sign Ctrl. Load, Store, Mple Load, Mple Store.
QA511 - QA751	Fixed Point Multiple and Divide
QA761 - QA851	Storage to Storage Moves and Logics, Pack Unpack, Move With Offset, Translate, Translate and Test
QA861 - QA991	PSW and misc forced address routines
QB001 - QB251	Decimal Option (*19-21)
QB261 - QB601	Floating Point Option (*33-37)
QB611 - QB991	Micro-Diagnostics
QC001 - QC011	Decoding of I/O OP Codes
QC021 - QC501	Multiplex Channel
QC511 - QC901	1050 Console and Features (*22-23)
QC911 - QC921	Direct Control Feature
QC931 - QC991	Unassigned
QD001 - QD301	Selector Channel (*24-26)

1400 COMPATIBILITY -- ROS PAGE ASSIGNMENTS

QE001 - QE401	Instruction Cycle and Index
QE411 - QE501	I/E Change
QE511 - QE991	Trap and Interrupt Routine, Mode Switch and Stops
QF001 - QF151	Multiply and Divide
QF161 - QF251	Edit
QF261 - QF401	Add, Sub, and Compare
QF411 - QF651	Moves, Loads, Set WM, Clear WM, Move Record, Move and Zero Suppress, Move Zone, Move Digit, Move Column Binary, Reset Add and Sub.
QF661 - QF801	Branches
QF811 - QF991	Clear, Store Stars, Modify Address
QG001 - QG101	I/O Common
QG111 - QG251	1050 Typewriter (*74-75)
QG261 - QG501	1442 - 1443 (*71-73)
QG511 - QG751	1402 - 1403 (*71-73)
QG761 - QG991	Tapes on Multiplex Channel (*76-78)
QH001 - QH251	Tapes on Selector Channel (*76-78)
QH261 - QH751	Files (*79-84)

*DENOTES CROSS BOARD LOCATION

1620 COMPATIBILITY -- ROS PAGE ASSIGNMENTS

QJ001 - QM991	1620 Compatibility
QP001 - QP491	Sterling

ROS FEATURE ASSIGNMENTS

VERS. #	FEATURE
000	Basic (Leave Version Blank on basic pages)
001	8K Storage
002	16K Storage
003	32K Storage
004	64K Storage
005	224 UCW's (Available only with 32K or 64K Storage)
006	Storage Protect
007	Decimal Option
008	Floating Point Option
009	Direct Control
010	1050 Console (Addr. 1F unless Ver 012 or 013)
011	Audible Alarm for 1050
012	1050 Console w/Addr. 5F (Only w/16K, 32K, 64K)
013	1050 Con. w/Addr. DF (Only w/32K, 64K, & 224USW's)
014	Selector Channel #1
015	Selector Channel #2
016*	1401 Compatibility
017*	Tapes on Multiplex Channel
018*	Tapes on Selector Channel
019*	1442 - 1443
020*	1402 - 1403
021*	Column Binary
022*	1050 Console for 1401 Compatibility
023*	Program Mode Switching
024*	Files
025	50 Cycle (Int. Timer)
026*	Sterling Feature
027*	Period - Comma inversion feature
028	
029	
030	
031	
032	
033	
034	
035	
036	
037	
038	
039	
040	1620 Compatibility
041	
906	Storage Protect Diagnostic
914	Selector Channel Diagnostic
995	Local Storage Dump
996	R/W Storage Diagnostic 1.5 us
997	Multiplex Channel Diagnostic
998	R/W Storage Diagnostic 2.0 us

* Available only as part of 1401 Compatibility Feature

COMBINATION VERSION ASSIGNMENTS

VERS. #		
,00		
A01	003, 014	32K and Selr Chan #1
A02	004, 014	64K and Selr Chan #1
A03	006, 014	Storage Prot and Selr Chan #1
A04	014, 015	Selr Chan #1 and Selr Chan #2
A05	006, 010	Storage Prot, 1050 Console
A06	006, 010, 012	Storage Prot, 1050 Console, Addr 5F
A07	006, 010, 013	Storage Prot, 1050 Console, Addr DF
,08	001, 010	8K and 1050 Console
A09		
A10	010, 013	1050 Console, Addr DF
A11	005, 006	224 UCW's*, Storage Prot
A12	010, 011	1050 Console, Audible Alarm
A13	010, 012	1050 Console, Addr 5F
A14	016, 023	1401 Compatibility, Prog Mode Switch
A15	016, 025	1401 Compatibility, 50 Cycle
A16	003, 005	32K and 224 UCW's
A17	004, 005	64K and 224 UCW's
A18	016, 026	1401 Compatibility and Sterling Feature
A19	001, 006	32 UCW's* and Storage Prot
A20	004, 006	64K and Storage Prot
A21	004, 006, 010, 012	64K and Storage Prot and 1050 Con. Addr 5F
A22	004, 010, 012	64K and 1050 Console Addr 5F
A23	004, 010, 013	64K and 1050 Console, Addr DF
A24	004, 006, 010, 013	64K Storage Prot, 1050 Con., Addr DF
A25	016, 027	1401 Compatibility and period-comma inversion
A26	014, 030	Sel Chan #1, Hi Speed MPX Channel
A27	005, 010, 013	224 UCW's, 1050 Console Addr DF
A28	005, 010, 012	224 UCW's, 1050 Console Addr 5F
A29	005, 010	224 UCW's 1050 Console
A30	010, 011, 012	1050 Aud Alarm, Adr. 5F
A31	007, 010	Decimal, 1050
A32	005, 006, 010	224 UCW's, Storage Protect, Decimal
A33	010, 011, 013	1050, Aud. Alarm, Addr. DF
A34	008, 014	Floating point, Sel. Channel #1
A35	018, 022	Tapes on Sel. Channel, 1050 colsole 1401
A36	016, 020	1401 Compatibility, 1402 - 1403
A37	016, 018	1401 Compatibility, Tapes on Sel. Channel
A38	018, 020	Tapes on Selector Channel, 1402 - 1403
A39	021, 026	Col. Binary, Sterling
A40	016, 019	1401 Compatibility, 1442 - 1443
A41	016, 024	1401 Compatibility, File
A42	018, 024	Tapes on Selector Channel, File
A43	014, 025	Selector Channel, 50 cycle
A44	020, 021	1402 - 1403, Col. Binary
A45	018, 019	Tape on Selector Channel, 1442 1443
A46	002, 014	16K and Selector Channel #1
A47	021, 027	Column Binary and Period, Comma Inversion
A48	020, 022	
A49	019, 022	
A50	020, 024	
A51	018, 020, 024	
A52	018, 023	
A53	017, 023	
A54	018, 026	
A55	018, 019, 024	
A56	019, 024	

COMBINATION VERSION ASSIGNMENTS
(continued)

* 32 UCW's means 8K (Ver 001)

96 UCW's means 16K 32K, or 64K without additional UCW option (Ver 002, 003, or 004)

224 UCW's means 32K, or 64K with additional UCW option (Ver 002, 003, or 004 combined with 005)

Version # can be located in CLD I. D. Block, extreme right hand bottom corner.

ALD VERSION ASSIGNMENTS

000	Basic
001	Retry (EC 126837)
002	Retry and Board)1A-E3 (see note)
003	Retry and 1. 5 us memory
004	1. 5 us memory
005	Conversion of)1B-E3 to)1A-E3
008	1. 5 us memory and board)1A-E3
009	Retry, 1. 5 us memory and board)1A-E3
101	1620 Compatibility
102	1620 Comp with 1. 5 us memory and without)1A-E3
103	1620 Comp, 1. 5 us memory and)1A-E3
104	1620 Comp and)1A-E3
105	1620 Comp and 1. 5 us memory
106	RPQ E41376 - External Alarm Control
107	RPQ W12097 - Remote Interrupt
200	RPQ 881650

RPQ VERSION ASSIGNMENTS

No.	Description
101	RPQ W12173 - Branch on Zero
102	RPQ E39692 - 1050 Addr 09 (32K mach w/o 224 UCW's only)
103	RPQ W12378 - Provide 7th tape dr on Sel Chan (1400 Compat)
104	RPQ E42126 - A Bit Compat (No charge)
105	RPQ F13141 - Group Mark Compat
106	RPQ W14479 - Branch on Column Binary
107	RPQ F14421 - Character Insert on Read Validity Error
108	Branch on Zero indicate with Compare Digit Only
109	Move Record to Lozenge Compat RPQ Y46595
110	RPQ E43217 - Putnam Fund
111	RPQ Y25092 - Inverse Move (WTC)
112	RPQ Y25108 - Inverse Move Compat
113	- Additional Index Registers

No.	Description
H01	016-101-108 (logic only) (J14 & 016) (was J23)
J01	018-101 Tape Sel. Chan. & RPQ (Br. on 0)
J02	023-101 PMS & RPQ (Br. on 0)
J03	010-102 1050 & RPQ (1050 Addr.)
J04	017-101 Tape MPX & RPQ (Br. on 0)
J05	006-010 102 Stor. Prot., 1050 & RPQ (1050 Addr.)
J06	018-103 Tape Sel. Chan. & RPQ (7th tape dr.)
J07	020-104 1402 & A Bit Compat.
J08	020-021-104 1402, Col. Bin, A Bit Compat.
J09	020-105 1402 & Group Mark Compat.
J10	020-021-105 1402, col. bin., Group Mark Compat.
J11	020-106 1402 & Branch on Col. Bin.
J12	020-107 1402 & Character Insert on Read Validity Error
J13	016-106 Basic, 1402 & Branch on Col. Bin.
J14	016-101 1400 and RPQ 101 (logic page only)
J15	020-104-106-107 1402, A Bit Compat., Branch on Col. Bin., Char. Insert on Read Validity Error
J16	020-106-107 1402, Branch on Col. Bin, Char. Insert on Read Validity Error
J17	020-104-106 1402, A Bit Compat., Branch on Col. Bin
J18	101-108 Branch on Zero with Compat. Digit
J19	016-108 Basic & Branch on Zero with Compat. Digit (logic page only)
J20	017-103 Tape MPX & RPQ 103 (logic only)
J21	018-108 Tape Sel. Chan., Branch on Zero with Compat. Digit
J22	017-108 Tape MPX, Branch on Zero with Compat. Digit
J23	014-040 1620 & Sel. Chan. (logic only)
J24	016-110
J25	016-112
J26	018-023-101
J27	016-109
J28	018-019-103
J29	020-101
J30	020-108
J31	017-023-101
J32	020-103
J33	018-020-103
J34	016-113
J36	020-110

ZONE AND 8-9 PUNCHES	DIGIT PUNCHES 1-7																							
				1			2			3			4			5			6			7		
		1403	1443		1403	1443		1403	1443		1403	1443		1403	1443		1403	1443		1403	1443		1403	1443
12-9	C9	I	I	01			02			03			04			05			06			07		
12-8-9	08			09			0A			0B			0C			0D			0E			0F		
11-9	D9	R	R	11			12			13			14			15			16			17		
11-8-9	18			18			1A			1B			1C			1D			1E			1F		
0-9	E9	Z	Z	21			22			23			24			25			26			27		
0-8-9	28			29			2A			2B			2C			2D			2E			2F		
9	F9	9	9	31			32			33			34			35			36			37		
8-9	38			39			3A			3B			3C			3D			3E			3F		
12-0-9	89			41			42			43			44			45			46			47		
12-8	C8	H	H	49			4A			4B			4C	¤	←	4D		(	4E		+	4F		±
12-11-9	99			51			52			53	·	·	54			55			56			57		
11-8	D8	Q	Q	59			5A			5B	$	$	5C	*	*	5D		)	5E		;	5F		¢
11-0-9	A9			E1			62			63			64			65			66			67		
0-8	E8	Y	Y	69			E0			6B	,	,	6C	%	%	6D		Y	6E		-	6F		±
12-11-0-9	B9			71			72	‡	‡	73			74			75			76			77		
8	F8	8	8	79			7A	±	:	7B	#	#	7C	@	@	7D		·	7E		=	7F		✓
12-0	C0	&	>	81			82			83			84			85			86			87		
12-0-8	88			80			8A			8B			8C			8D			8E			8F		
12-11	6A			91			92			93			94			95			96			97		
12-11-8	98	-	<	90			9A			9B			9C			9D			9E			9F		
11-0	D0			A1			A2			A3			A4			A5			A6			A7		
11-0-8	A8			A0			AA			AB			AC			AD			AE			AF		
12-11-0	70			B1			B2			B3			B4			B5			B6			B7		
12-11-0-8	B8			B0			BA			BB			BC			BD			BE			BF		
12	50	&	&	C1	A	A	C2	B	B	C3	C	C	C4	D	D	C5	E	E	C6	F	F	C7	G	G
12-0-8-9	48			00			CA			CB			CC			CD			CE			CF		
11	60	-	-	D1	J	J	D2	K	K	D3	L	L	D4	M	M	D5	N	N	D6	0	0	D7	P	P
12-11-8-9	58			10			DA			DB			DC			DD			DE			DF		
0	F0	0	0	61	/	/	E2	S	S	E3	T	T	E4			E5	V	V	E6	W	W	E7	X	X
11-0-8-9	68			20			EA			EB			EC			ED			EE			EF		
NONE	40			F1	1	1	F2	2	2	F3	3	3	F4	4	4	F5	5	5	F6	6	6	F7	7	7
12-11-0-8-9	78			30			FA			FB			FC			FD			FE			FF		

* 1403 Graphics are for Type "A" chain

** 1443 Graphics are, as shown, for 1443N1 with 63 Character SMS Bar.

BITS 4 - 7 (rows) / BITS 0 - 3 (columns)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BA	A8 2 8	B 8 2 —	8 2 0	BA	A8 2 8	B 82 —	82 0	A 82 8	B 82 —	A	82 0	A 82 8	B 82 —	A	82 0
1	BA 1 A	B 1 J	A 1 /	1 1	BA 1 A	B 1 J	A 1 /	1 1	BA 1 A	B 1 J	A 1 /	1 1	BA 1 A	B 1 J	A 1 /	1 1
2	BA 2 B	B 2 K	A 2 S	2 2	BA 2 B	B 2 K	A 2 S	2 2	BA 2 B	B 2 K	A 2 S	2 2	BA 2 B	B 2 K	A 2 S	2 2
3	BA 21 C	B 21 L	A 21 T	21 3	BA 21 C	B 21 L	A 21 T	21 3	BA 21 C	B 21 L	A 21 T	21 3	BA 21 C	B 21 L	A 21 T	21 3
4	BA 4 D	B 4 M	A 4 U	4 4	BA 4 D	B 4 M	A 4 U	4 4	BA 4 D	B 4 M	A 4 U	4 4	BA 4 D	B 4 M	A 4 U	4 4
5	BA 4 1 E	B 4 1 N	A 4 1 V	4 1 5	BA 4 1 E	B 4 1 N	A 4 1 V	4 1 5	BA 4 1 E	B 4 1 N	A 4 1 V	4 1 5	BA 4 1 E	B 4 1 N	A 4 1 V	4 1 5
6	BA 42 F	B 42 O	A 42 W	42 6	BA 42 F	B 42 O	A 42 W	42 6	BA 42 F	B 42 O	A 42 W	42 6	BA 42 F	B 42 O	A 42 W	42 6
7	BA 421 G	B 421 P	A 421 X	421 7	BA 421 G	B 421 P	A 421 X	421 7	BA 421 G	B 421 P	A 421 X	421 7	BA 421 G	B 421 P	A 421 X	421 7
8	BA8 H	B 8 Q	A8 Y	8 8	BA8 H	B 8 Q	A8 Y	8 8	BA8 H	B 8 Q	A8 Y	8 8	BA8 H	B 8 Q	A8 Y	8 8
9	BA8 1 I	B 8 1 R	A8 1 Z	8 1 9	BA8 1 I	B 8 1 R	A8 1 Z	8 1 9	BA8 1 I	B 8 1 R	A8 1 Z	8 1 9	BA8 1 I	B 8 1 R	A8 1 Z	8 1 9
A	BA8 2 +	B 8 2 —	A8 2 &	8 2 0	BA8 2 +	B 8 2 —	A8 2 &	8 2 0	BA8 2 +	B 8 2 —	A8 2 &	8 2 0	BA8 2 +	B 8 2 —	A8 2 &	8 2 0
B	BA8 21 .	B 8 21 $	A8 21 ,	8 21 # | =	BA8 21 .	B 8 21 $	A8 21 ,	8 21 # | =	BA8 21 .	B 8 21 $	A8 21 ,	8 21 # | =	BA8 21 .	B 8 21 $	A8 21 ,	8 21 # | =
C	BA84 ← |)	B 84 *	A84 % | (	84 @ | '	BA84 ← |)	B 84 *	A84 % | (	84 @ | '	BA84 ← |)	B 84 *	A84 % | (	84 @ | '	BA84 ← |)	B 84 *	A84 % | (	84 @ | '
D	A84 % | (	BA84 ← |)	A84 1	84 @ | '	A84 % | (	BA84 ← |)	A84 1	84 @ | '	A84 % | (	BA84 ← |)	A84 1	84 @ | '	A84 % | (	BA84 ← |)	A84 1	84 @ | '
E	BA8 2 +	B 842	A8 21 ,	8 21 # | =	BA8 2 +	B 842	A8 21 ,	8 21 # | =	BA8 2 +	B 842	A8 21 ,	8 21 # | =	BA8 2 +	B 842	A8 21 ,	8 21 # | =
F	BA8421	B 8421	A8421	8421	BA8421	B 8421	A8421	8421	BA8421	B 8421	A8421	8421	BA8421	B 8421	A8421	8421

2821 PRINT HAMMER DRIVER LOCATIONS

Print Position	Location	Print Position	Location	Print Position	Location
01	G-25	45	G-14	89	G-10
02	G-25	46	E-14	90	G-10
03	E-18	47	E-14	91	G-21
04	E-18	48	G-14	92	G-21
05	G-18	49	G-14	93	E-09
06	E-18	50	G-14	94	E-09
07	E-18	51	G-23	95	G-09
08	G-18	52	G-23	96	E-09
09	G-18	53	E-13	97	E-09
10	G-18	54	E-13	98	G-09
11	G-25	55	G-13	99	G-09
12	G-25	56	E-13	100	G-09
13	E-17	57	E-13	101	G-20
14	E-17	58	G-13	102	G-20
15	G-17	59	G-13	103	E-08
16	E-17	60	G-13	104	E-08
17	E-17	61	G-22	105	G-08
18	G-17	62	G-22	106	E-08
19	G-17	63	E-12	107	E-08
20	G-17	64	E-12	108	G-08
21	G-24	65	G-12	109	G-08
22	G-24	66	E-12	110	G-08
23	E-16	67	E-12	111	G-20
24	E-16	68	G-12	112	G-20
25	G-16	69	G-12	113	E-07
26	E-16	70	G-12	114	E-07
27	E-16	71	G-22	115	G-07
28	G-16	72	G-22	116	E-07
29	G-16	73	E-11	117	E-07
30	G-16	74	E-11	118	G-07
31	G-24	75	G-11	119	G-07
32	G-24	76	E-11	120	G-07
33	E-15	77	E-11	121	G-19
34	E-15	78	G-11	122	G-19
35	G-15	79	G-11	123	E-06
36	E-15	80	G-11	124	E-06
37	E-15	81	G-21	125	G-06
38	G-15	82	G-21	126	E-06
39	G-15	83	E-10	127	E-06
40	G-15	84	E-10	128	G-06
41	G-23	85	G-10	129	G-06
42	G-23	86	E-10	130	G-06
43	E-14	87	E-10	131	G-19
44	E-14	88	G-10	132	G-19

INTERFACE CONNECTOR CHART

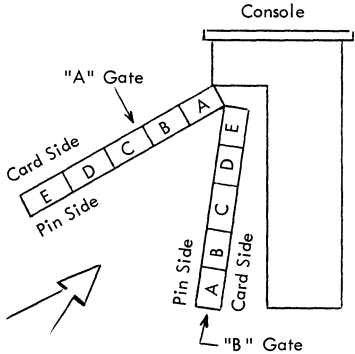
	B	D	CONNECTOR 1	CONNECTOR 2
2	○	○		
3	•	+3	Bus Out P	Operational In
4	○	•	Bus Out Ø	Status In
5	•	○	Bus Out 1	Address In
6	-3	•	Bus Out 2	Service In
7	○	○		
8	•	○	Bus Out 3	Select In
9	○	•	Bus Out 4	Select Out
10	•	○	Bus Out 5	Address Out
11	+6	•	Bus Out 6	Command Out
12	•	○	Bus Out 7	Suppress Out
13	○	•		Service Out

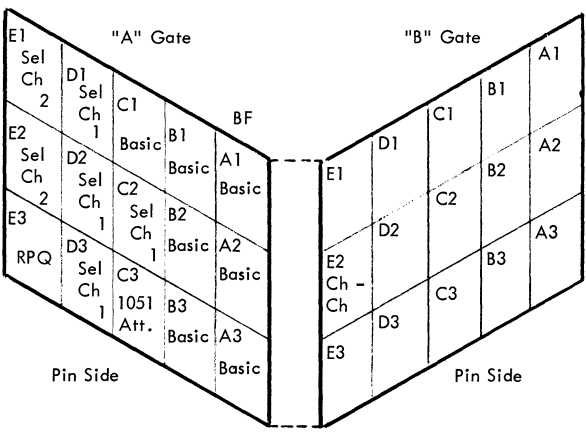
○ Ground Shield

• Signal

	G	J	CONNECTOR 1	CONNECTOR 2
2	○	○		
3	•	+3	Bus In P	Clock Out
4	○	•	Bus In Ø	Metering Out
5	•	○	Bus In 1	Metering In
6	-3	•	Bus In 2	Request In
7	○	○		
8	•	○	Bus In 3	
9	○	•	Bus In 4	
10	•	○	Bus In 5	
11	+6	•	Bus In 6	
12	•	○	Bus In 7	Hold Out
13	○	•		Operational Out

2030 BOARD - LOCATION





CIRCUIT		INPUT** TWILIGHT ZONE		OUTPUT** LIMITS		OUTPUT** NORMAL		CIRCUIT FLYER		DELAY (NS) TURN ON		DELAY (NS) TURN OFF		NONE INV.	REMARKS
		Up	Down	Up	Down	Up	Down	LOADED	NOT LOADED	Nom*	Max	Nom*	Max		
AI	and - inverter	1.4	0.5		.3	3.0	0.0 to 0.3	T03 - AB	T03 - AA	25.0	35.0	21.0	35.0		
AOI	and - or - inverter	2.0	0.9		.3	3.0		T03 - AE	T03 - AD	34.0	60.0	21.0	32.0		
API	and - power - inverter	1.6	0.46			3.0		T03 - AJ	T03 - AF	13.0	22.0	27.0	42.0		
DCI	direct couplet-inverter	0.8	0.58			3.0		T05 - AB	T05 - AA	17.0	25.0	17.0	25.0		N
HPD	High powered driver	0.8	0.58		2.88	3.1	0.3	T15 - AA	T15 - AE	17.0	25.0	17.0	25.0		
II	Isolating inverter	2.2	0.58				0.0 to 0.3	S05 - AH	S05 - AS		40.0		50.0		N
ID SCR		2.0							S55 - EG						
LR		2.03						S06 - AN	S06 - AK						
LSA	Line sense amplifier						0.3				15.0		46.0		
LTN	Line terminator	1.8	0.9								60.0		55.0		
PH	polarity hold } data contr.	1.4 1.9	0.14		1.8	2.0		T03 - AK		26.0	20.0	32.0	50.0		
XOR	Exclusive - OR	1.9				2.5	0.0 to 0.3	T03 - AI	T03 - AP		40.0		64.0	(N.I.)	OE
A OR	- AND + OR	2.4						T03 - AC	T03 - CE					(N.I.)	
TD	Time delay								S45 - EA/SB					(N.I.)	

* Varies with load etc. All values quoted are to upper limit of normal operation. ** All voltages quoted are positive (+).

CARD DESCRIPTION DMA4 Version 3 or higher

SCT/DMI/O (End Card Minus 10)
Defines Loader-Input-Output Device (Users Guide)

SCT-SRT (1st of 8 = End Card Minus 8)
Defines System Configuration (Users Guide)

SCT-UDT (End Card Minus 15)
Defines I/O Equip on System (Users Guide)

IPL LOADER #1
1st Card DMA4 (Users Guide)

IPL LOADER #2
2nd Card DMA4 (Users Guide)

ESD (1st Card Section Deck)
Gives Name, Origin, & Length of Program Section of Test Deck

TXT (Follows IPL Loader 2)
Gives Text of Program in Monitor & Test Deck

REP (Last Card Before RLD Crd)
Used to set Sense Switches, Used to Overlay Data (Users Guide)

RLD
Ignored DMA4

DAT (Used in Place of LDT Cards)
Indicate to Monitor That Data Cards Follow-Must Proceed Each Set of Data Cards. (Users Guide)

LDT (Last Card of Section Deck)
Load Terminate Card-If Missing Next Section Will Reject. (Users Guide)

END - Ignored by DMA4

BLANK - Valid in DMA4

LOAD DMA4 - Users Guide (840034)

HANG UP CONDITIONS DMA4 - Users Guide

1. If a section halts with an error, it can be restarted by depressing System Reset & hitting Start Key twice.
2. If a section halts with an error and you wish to bypass it, hitting the Interrupt Key once will allow the machine to continue from the point of error. Hitting the Interrupt Key twice will terminate that section and start next section.

SENSE SWITCHES DMA4

NUMBER

20	OFF	Dm Will Load Each Sect In Seq
	ON	Dm Will Halt After Each Sect
21	ON	Short Format Error Msg's
	OFF	Long Format Error Msg's
24	OFF	Print All Msg S & T
	ON	Prevent Print S & T
25	OFF	No Halt After Error
	ON	Halt After Error
26	OFF	Normal
	ON	Cycle CE Run Request
27	OFF	Allow All Printing
	ON	Prevent All Printing
28	OFF	No Cyc Prog Sect In Storage
	ON	Cycle Prog Sect In Storage
30	OFF	Print Error Msg's
	ON	Prevent Print Error Msg's
31	OFF	Normal DMA4 Output Msg Format
	ON	8K System - No Effect 16 K or Larger - Transfer Control to Message Editor to Print DMA4 Messages

Each section has its won sense switch settings, they must be looked up in section

SWITCH SETTINGS FOR CONSOLE OVERLAY DMA4

	F	G H J
NORMAL	0	Do Not Care
LOAD FROM	8	Section Search Number
LOAD TO	9	Section Search Number
EXECUTE	1	Do Not Care
SW OFF		
MONITOR	2	7 Sense Sw Number
SECTION	2	8 Sense Sw Number
SW ON		
MONITOR	3	7 Sense Sw Number
SECTION	3	8 Sense Sw Number
CYCLE		
ACTIVE	5	5 Do Not Care
SELECT	5	6 Routine Number
PRINT SEC	6	Dump & Print Sect
PRINT MON	7	Dump & Print Monitor
OUTPUT UNIT	4	Ch Addr I/O Addr
ENTER SEC	E	To Change Section
ENTER MON	F	To Change Monitor
INITIALIZE	D	Do Not Care

*PZZZL	SVC D1 D2 Error Msg's
*PZZZL CU	SVC D3 Error Msg
*DIO DMA4	Monitor I/O Error
*EIE	External Interrupt Error
HLT	With Error Msg When Halt on Error Indicated
HLT PZZZL	SVC DA Halt Request
*IOE	Prog Sect I/O Error
*ISC DMA4	Invalid Supervisor Call Interrupt Error in DM
*ISC PZZZL	Invalid Supervisor Call Interrupt Error in Sect
*MCK DMA4	Machine Check Interrupt Error in Monitor
*MCK PZZZL	Machine Check Interrupt Error in Section
OIR	Operator Intervention Requested or Required
*PGM DMA4	Program Interrupt Error in Monitor
*PGM PZZZL	Program Interrupt Error in Section
PNF DMA4	Program Not Found
REJ PZZZL	Section Rejected
REL PZZZL	Reload
RNV PZZZL	Requested Unit Not Found
S PZZZL	Start of Section
SDO PZZZL	Line. CPU is Optional
*SDO PZZZL	SVC DO Error ID Line CUU is Optional
T	Terminal End of Section
T*	Abnormal Termination
*UIO PZZZL	Unassigned I/O Interrupt Error
WTE DMA4	Wait Message

Section #	Title	Search #
32011	Standard Set 1 Sec 1	201
32021	Standard Set 1 Sec 1	202
32611	Standard Set 2 Sec 1	261
32621	Standard Set 2 Sec 2	262
32630	Standard Set 2 Sec 3	263
32640	Standard Set 2 Sec 4	264
32911	Float Point Section 1	291
32921	Float Point Section 2	292
32931	Float Point Section 3	293
32E10	Decimal Arith Sec 1	2E1
32E20	Decimal Arith Sec 2	2E2
338F0	Usage Meter	38F
33900	R/W Storage	390
33C90	Stor Prot	3C9
34300	Chan Function	430
34470	Sel Chan 1 Fault Locating	447
344A0	Sel Chan 2 Fault Locating	44A
34E10	Direct Ctrl	4E1
F5011	Tape Function Sec 1	501
F5022	Tape Function Sec 2	502
F5032	Tape Function Sec 3	503
F5042	Tape Function Sec 4	504
F5051	Tape Function Sec 5	505
F5061	Tape Function Sec 6	506
F5071	Tape Function Sec 7	507
F5081	Tape Function Sec 8	508
F5091	Tape Function Sec 9	509
F51A2	Error Detection Sec 1	51A
F51B2	CRC Generation Sec 1	51B
F5211	IRG (Write) Sec 1	521
F5221	IRG (Read) Sec 2	522
F5231	IRG (Write 8K) Sec 1	523
F5241	IRG (Read 8K) Sec 2	524
F6002	2841/2311 Function Test	600
F6011	2841/2311 Function Test	601
F6021	2841/2311 Function Test	602
F6031	2841/2311 Function Test	603
F6041	2841/2311 Function Test	604
F6051	2841/2311 Function Test	605
F6061	2841/2311 Function Test	606
F6071	2841/2311 Function Test	607
F6081	2841/2311 Function Test	608
F6091	2841/2311 Function Test	609
F6101	2311 Diagnostic Test	610
F6111	2311 Diagnostic Test	611
F6121	2311 Diagnostic Test	612
F6131	2311 Diagnostic Test	613

SYSTEM/360 DIAGNOSTICS
(continued)

Section #	Title	Search #
F8041	2821/2540 Reader Punch Scan	804
F8051	2821/2540 Buff Addr Test	804
F8060	2821/2540 Pnch Xlator Test	804
F8081	2821/1403 Non UCS Scan	808
F8090	2821/1403 Non UCS Scan	808
F80C4	2821/1403 UCS Scan Rtn 1 & 2	80C
F80D2	2821/1403 UCS Scan Rtn 3 & 4	80C
F8102	2540 Reader Function Sec 1	810
F8111	2540 Reader Function Sec 2	811
F8152	2540 Reader Col Bin	815
F8170	2540 Reader 14XX Mode	817
F8202	2540 Punch Function Sec 1	820
F8212	2540 Punch Function Sec 2	821
F8231	2540 Punch Feed Read	823
F8251	2540 Punch Col Bin	825
F8303	1403 Printer Function Test Sec 1	830
F8313	1403 Printer Function Test Sec 2	831
F8323	1403 Printer Function Test Sec 3	832
F8330	1403 Printer Function Test Sec 4	833
F8362	1403 Ripple Print	836
F8382	1403 Carriage Snse Channel 9 & 12	838
F8394	1403 Carriage Forms Space & Skip	839
F83F0	1403 Selective Tape Lister	83F
F8500	1404 Printer Function Test	850
F8510	1404 Printer Read Compare	851
F8520	1404 Printer Seq of Commds	852
F9000	1052 Basic op Test	900
F9010	1052 Mech Func Test	901
F9020	1052 Reader Keyboard Test	902
*FOFF	Tape Editor	OFF
*3FDO	I/O Exerciser	FDO
*3FE1	SEREP	FE1
*FC1	8K Sys Test (SEVA)	FC1
3447	Selector Channel 1 Fault Locating	447

* These programs are stand alone programs and will not run with a monitor program.

1401 COMPATIBILITY

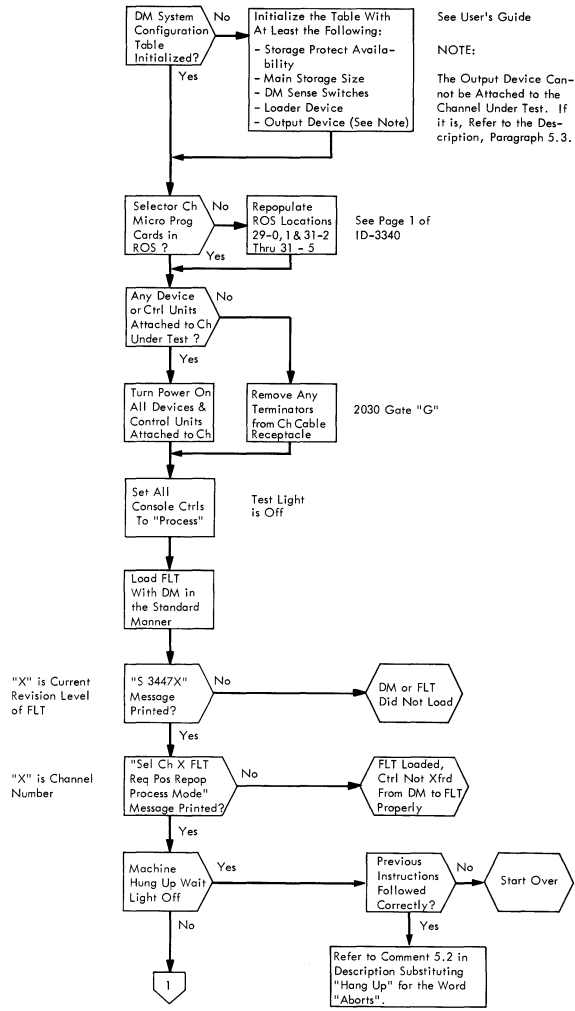
Section #	Title	Search#
3F00	14XX Compatibility CPU	F00
3F01	14XX Compatibility CPU Sec 1	F01
3F02	14XX Compatibility CPU Sec 2	F02
3F03	14XX Compatibility CPU Sec 3	F03
3F04	14XX Compatibility CPU Sec 4	F04
3F05	14XX Compatibility CPU Sec 5	F05
3F06	Prog Mode SW 1401 Compatibility	F06
3F07	1402 Read-Punch 1401 Compat.	F07
3F08	1402 PFR 1401 Compatibility	F08
3F09	1402 Col Bin 1401 Compatibility	F09
3F0C	1403 PRTR TST 1401 Compatibility	F0C
3F10	1442 Read-Punch 1401 Compat.	F10
3F13	1443 Bar Printer 1401 Compat.	F13
3F16	Mag. Tape Test 1401 Compat.	F16
3F19	2311/1311 File Test 1401	F19
3F1C	Cons. Type Test 1401 Compat.	F1C

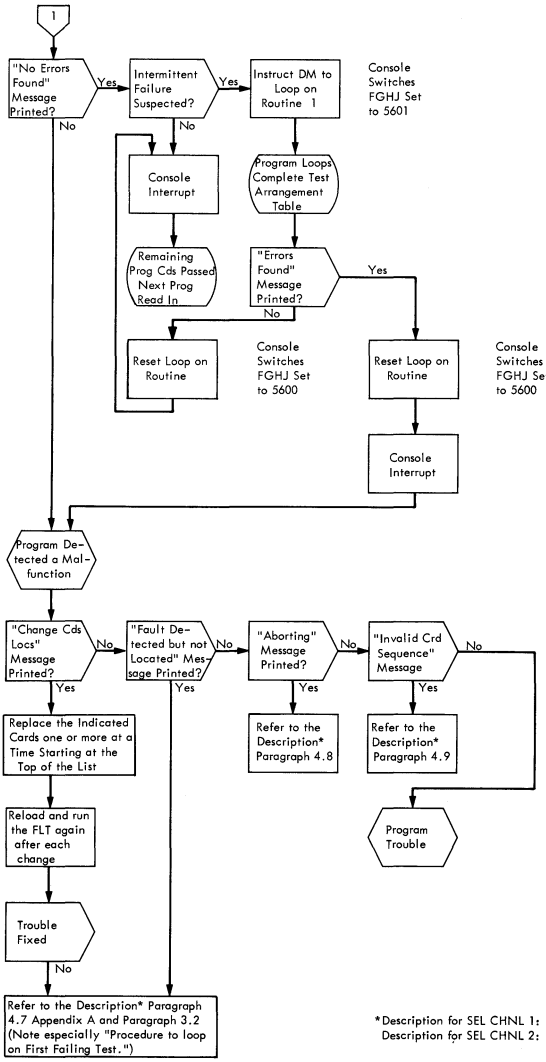
1620 COMPATIBILITY

Section #	Title	Search #
3F40	1620 Compatibility Feature	F40
3F41	1620 Non Disk I/O	F41
3F42	1620 Set Clear MV 20K Flg.	F42
3F43	1620/360 Output Xlator	F43
3F44	1620/360 Input Xlator	F44
3F45	1620/360 Xlator Count	F45
3F46	1620 CPU Tests	F46
3F47	1620 Dsk Sk Cy Ovfl Ad Ck	F47
3F48	1620 Init Rd Wr Chk Dsk	F48
3F49	Rd Wr Chk Dsk 80K Sect	F49
3F4A	Disk Sect Data Movement	F4A
3F4B	Disk Trk Data Movement	F4B
3F4C	Set 40K & 60K 1620 Flags	F4C
3351	1620 Micro Diagnostics	351

MISCELLANEOUS

Section #	Title	Search #
3FC1	Systems Test Description -A-	FC1
3FC2	System Test Description -B-	FC2
3FD0	3 Cd Hex Ldr & Gen I-O Ex	FD0
3FD1	Ls Map Description	FD1
3FE1	SEREP Description	FE1


DM System Configuration Table Initialized?
No
Initialize the Table With At Least the Following:
- Storage Protect Availability
- Main Storage Size
- DM Sense Switches
- Loader Device
- Output Device (See Note)
See User's Guide
NOTE:
The Output Device Cannot be Attached to the Channel Under Test. If it is, Refer to the Description, Paragraph 5.3.
Yes
Selector Ch Micro Prog Cards in ROS ?
No
Repopulate ROS Locations 29-0, 1 & 31-2 Thru 31 - 5
See Page 1 of ID-3340
Yes
Any Device or Ctrl Units Attached to Ch Under Test ?
No
Yes
Turn Power On All Devices & Control Units Attached to Ch
Remove Any Terminators from Ch Cable Receptacle
2030 Gate "G"
Set All Console Ctrls To "Process"
Test Light is Off
Load FLT With DM in the Standard Manner
"X" is Current Revision Level of FLT
"S 3447X" Message Printed?
No
DM or FLT Did Not Load
Yes
"X" is Channel Number
"Sel Ch X FLT Req Pos Repop Process Mode" Message Printed?
No
FLT Loaded, Ctrl Not Xfrd From DM to FLT Properly
Yes
Machine Hung Up Wait Light Off
Yes
Previous Instructions Followed Correctly?
No
Start Over
No
Yes
Refer to Comment 5.2 in Description Substituting "Hang Up" for the Word "Aborts".
1



*Description for SEL CHNL 1: ID 3447
Description for SEL CHNL 2: ID 344A

CHART A

DMA4 OPERATOR'S FLOW CHART

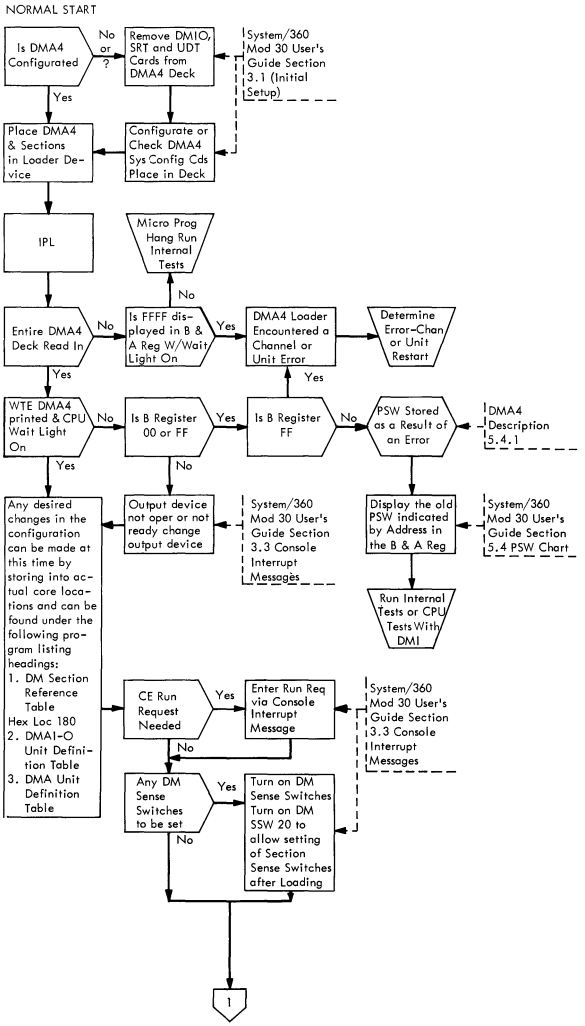


CHART B

DMA4 OPERATOR'S FLOW CHART

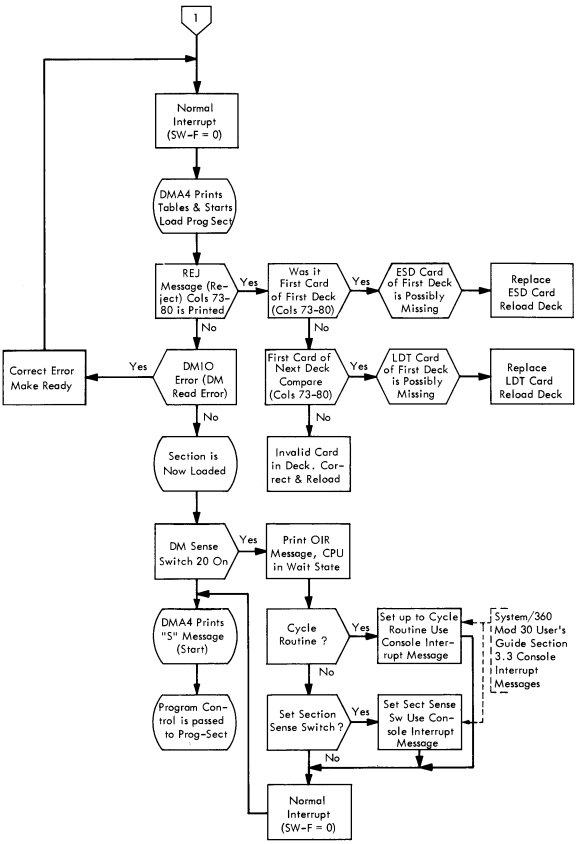
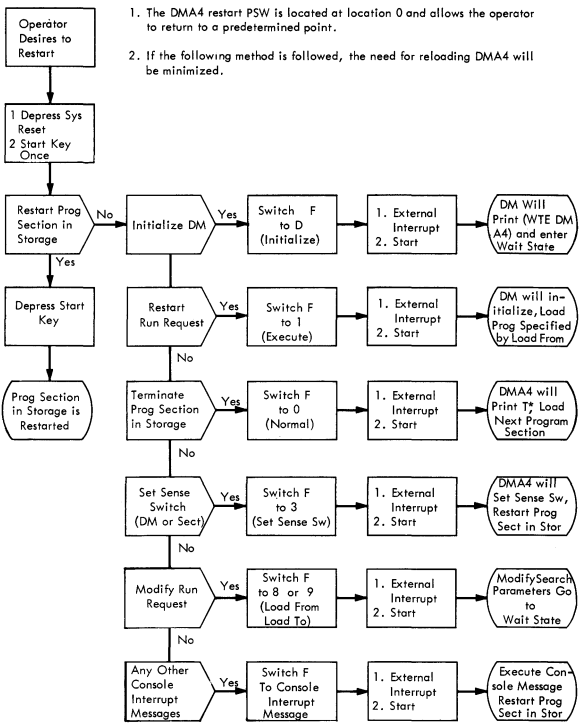


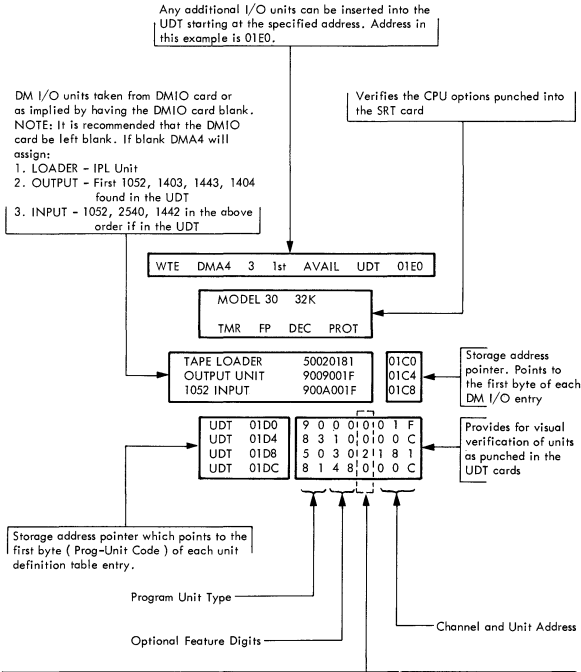
CHART C

DMA4 RESTART PROCEDURES

1. The DMA4 restart PSW is located at location 0 and allows the operator to return to a predetermined point.

2. If the following method is followed, the need for reloading DMA4 will be minimized.





1. A two in this position indicates that the unit has been withdrawn from the UDT table, and will not be assigned to any program section.

2. To withdraw any unit from the UDT, store a two in this position of the corresponding UDT entry. (Example : Withdraw the 1052. Store into loc 01D2 A 20)

3. To add a withdraw unit, remove the two from that unit's UDT entry. (NOTE : If loading from tape, never remove the two from the load device)

INDEX

CUT ALONG DOTTED LINE

IBM Field Engineering Handbook, System/360 -- Model 30, Form 229-2116-2

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Circle one of the comments and explain in the space provided:

Suggested Addition (page ___) Suggested Deletion (page ___) Error (page ___)

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