Publication Number 29-326R01

M46-100
CRT
INSTRUCTION MANUAL

CONSISTS OF:

Installation Specification	02-310A20
Programming Specification	02-310R01A22
Schematic	02-310B08

INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

May 1974

02-310A20
May 1973

M46-100
CRT (LOW END)
INSTALLATION SPECIFICATION

1. GENERAL

The low-end CRT has two Marketing Numbers; M46-100 for the 115V/60 Hz version and M46-101 for 240V/50 Hz. Each product consists of the desk-top CRT with keyboard. No other hardware is included. The cables and interfaces which are required may be purchased separately. Table 1 relates Marketing and hardware numbers. The interconnections are shown in Figures 1 and 2.

TABLE 1. CRT MARKETING/HARDWARE NUMBERS

MARKETING NUMBER	HARDWARE NUMBER	DESCRIPTION
M46-100	27-053F00	CRT-TTY Replacement, 115V, 60 Hz
M46-101	27-053F01	CRT-TTY Replacement, 240V, 50 Hz
M46-106	17-272	CABLE, CRT-PASLA, 25 Ft.
M46-104	17-273	CABLE, CRT-TTY INF, 25 Ft.
M46-107	02-324	CRT/TTY 7" INF, 1200 Baud
M46-102	02-279	PASLA 7" INF, RS-232
	29-327	CRT VENDOR's Manual

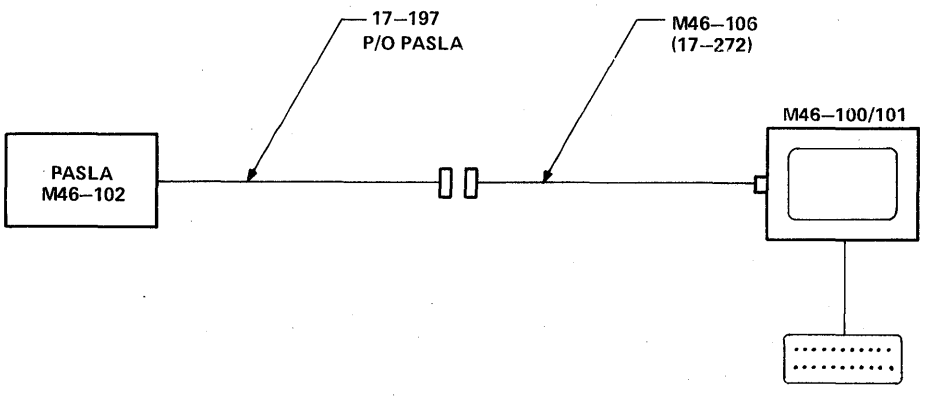

Figure 1. PASLA–CRT Connection

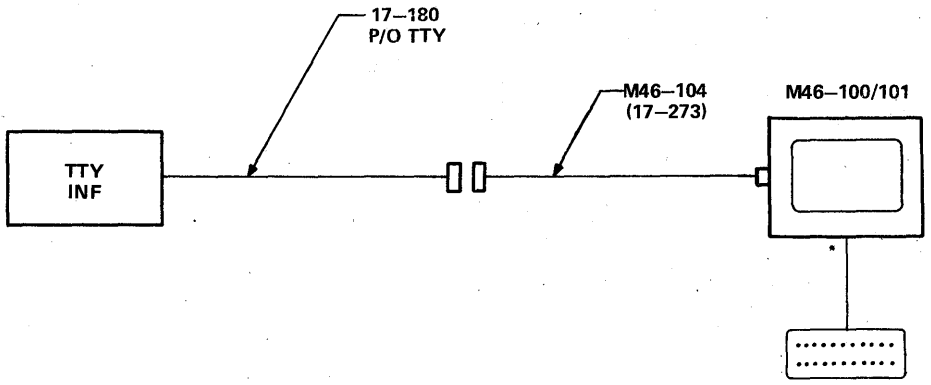

Figure 2. TTY Interface–CRT Connection

2. INSTALLATION

The CRT Terminal has been carefully packed to insure its arrival in operating condition; however, use the following procedures to establish the mechanical integrity of the unit and prepare it for operation.

2.1 Unpacking

Inspect the shipping carton for external damage. As the equipment is unpacked, check for signs of damage or missing parts.

2.2 Equipment Placement

The CRT Terminals are self-contained and include an attractive enclosure and non-scuffing rubber feet for protection of desk and table tops. Connectors are provided for power (2-wire plus ground), detachable keyboard, video output for remote TV monitor, and communication line (telephone modem or direct connection to Processor.) Clearance is required for convection cooling of the electronics.

2.3 Options

Optional features are normally enabled at the factory. If the features are specified at time of order, they are pre-set at the factory. If, however, the CRT is not purchased with an interface or if the customer does not specify options, it is necessary to inspect the PC boards in the CRT and adjust the option switches for the individual requirement. In order to do this, proceed as follows:

1. Release the three 1/4 turn fasteners on the back panel, pull back the two slide latches (at the bottom) rear corners), and push forward and upward (enclosure rotates from the bottom front).

2. Remove the FUNCTION CONTROL (Position 5) and TTY INTERFACE (Position 6) printed circuit boards from the card cage.

3. Check the vendor manual, 29-327, for each switch identification and implement the required options. See Section 4.1 and 4.2.

4. Replace the two PC boards and check the remaining PCs for socket engagement.

5. Verify that the AC power switch on the top cross-member in the housing is set properly for 115 or 240V operation. Note that this switch selects AC input for the high voltage power supply only.

2.4 115/240V, 50/60 Options

The 50/60 Hz option is implemented by changing the switch position on the TIMING GENERATOR board. With the P C component side up, card edge connector to the right, adjust the switch ⊕ for 60 Hz and ⊖ for 50 Hz.

The 115/240 V option is implemented by adjusting the switch at the left of the POWER switch UP for 240 V and DOWN for 115V.

3. APPLYING POWER

Before connecting power to the Terminal:

1. Turn the POWER switch on the back panel to OFF.

2. Plug the keyboard cable into KB-J3 on the back panel. Insure that the slide locks on the connector are securely fastened.

3. Attach the appropriate interface cable to J1 and fasten securely with the two 4-40 screws.

4. Attach the power cord to the POWER CONNECTOR on the back panel and to a standard 115VAC, 60 Hz, 3 wire grounded outlet (or to 240VAC if so ordered).

WARNING

CUTTING THE SAFETY GROUND PIN ON THE POWER CORD FOR USE WITH A 2-HOLE SOCKET WILL PRESENT A SHOCK HAZARD. USE A 3 PRONG ADAPTER WITH SAFETY GROUND PROPERLY CONNECTED.

5. Turn the POWER switch to ON. When power is applied to the unit, the POWER switch is illuminated. If the switch fails to light, check the 2 amp fuse on the back panel.

6. Allow approximately one minute for the CRT filament to warm up. The blinking cursor should appear in the lower left corner of the screen. If it does not, adjust the BRIGHTNESS control on the front panel below the screen. If the cursor still does not appear, a malfunction is indicated.

7. Set the 80/72 switch to 80; the FDX/HDX switch to FDX and SEL/TTY to SEL. The 06-146 CRT Test Program may now be executed.

4. INTERFACE CONNECTIONS

The CRT may be interfaced to an INTERDATA Processor through the PASLA or any of the TTY interfaces (Model 70 or 80 built-in or the 7 inch TTY interface), or with the 7 inch CRT/TTY interface (M46-107). The latter is a 7 inch TTY interface (M48-010) which is modified to run at 1200 baud.

4.1 PASLA Interconnect

The PASLA contains the hardware to receive and transmit most of the normal RS-232C lines in an asynchronous mode. These lines include: RING, DSRDY, CARRIER, DTR, RQ2S, CL2S, TDATA, RDATA, REV CHAN REC, and REV CHAN TRANS.

When connecting the PASLA to a CRT (or most other local terminals), it is necessary to disable (force to zero) the RS-232 status bits which are not equipped on the terminal. The PASLA has wire-wrap stakes equipped for this purpose. The following is a summary of PASLA straps required for operation with the M46-100 or M46-101 CRT.

STRAP	FUNCTION
7-8 (Add)	FDX option
CF-GO (Add)	Force CARR Status = 0
CB-G3 (Add)	Force CL2S active
HD-G4 (REMOVE)	FDX Option

In addition, the straps A1-K1 must be equipped to select the required baud rate. This may be in the range of 75 to 9600 baud and is described in the PASLA Instruction Manual, Publication Number 29-301, which is included with the PASLA. Note that the character format/baud rate of PASLA is programmable. The CRT must be strapped to match these programmed characteristics.

4.2 TTY Interface Connect

The CRT contains the current loop interface required to connect to any of the INTERDATA TTY Interfaces. The TTY Interfaces have a fixed character format/baud rate and the switches in the CRT must be implemented to match these characteristics. The following is a summary of required switch-implemented options in the CRT.

RECEIVER SPEED	110/1200*
TRANSMITTER SPEED	110/1200*
PARITY	EVEN
STOP BITS	10 BITS/CHARACTER (1 STOP BIT)
INTERFACE	CURRENT LOOP
AUTO-CARRIAGE RETURN	LOCAL ONLY

* 1200 Baud for M46-107 only.

02-310R01A22
May 1974

M46-100
CRT
PROGRAMMING SPECIFICATION

1. INTRODUCTION

This specification contains a description of the CRT and the information necessary to program the system. The CRT interfaces to the Multiplexor Bus or Selector Channel Bus through the M46-102 Programmable Asynchronous Single Line Adapter (PASLA) or any of the TTY interfaces (Model 70 or 80 built-in or a 7 inch TTY Interface or a 7 inch CRT/TTY Interface).

The PASLA comprises one full duplex interface with an even device address for the Receive side and an odd address for the Transmit side. There is an Interrupt flip-flop associated with each side.

2. CONFIGURATION

The CRT can be used on any Model 50, 70, 74, 80, 85 Processor or equivalent.

3. OPERATING PROCEDURES

3.1 Power

Before applying power to the terminal, turn the POWER Switch on the back panel to OFF. See Figure 1. Plug the keyboard cable into the KB-J3 Connector on the back panel. Attach the power cord to the POWER CONNECTOR on the back panel and to a standard 115 VAC, 60 Hz grounded outlet.

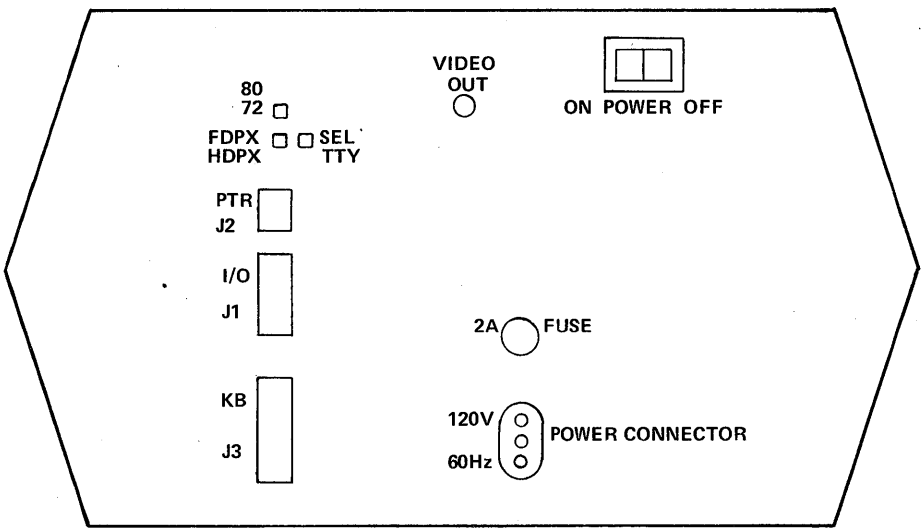

Figure 1. Back Panel

3.2 Keyboard

The CRT terminal uses the basic keyboard arrangement of a Teletypewriter. Figure 2 shows the keyboard layout. As displayable keys are depressed, the characters appear above the cursor on the bottom line of the screen and the cursor is moved right one position. Near the end of a line, the bell in the keyboard rings. The cursor remains at the end of the line until a Carriage Return is received.

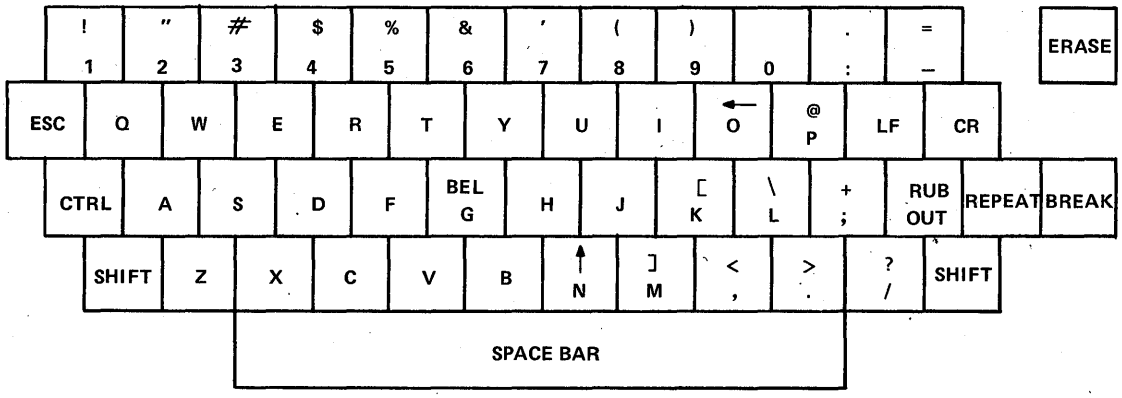

Figure 2. Keyboard Arrangement

Refer to Table 1 for the ASCII codes generated for each key.

The codes in Columns 0 and 1 of Table 1 are generated by use of the CTRL key plus the corresponding keys in Columns 4 and 5 respectively. Codes in brackets in Column 0 are used within the Terminal. Codes in parenthesis in Columns 0 and 1 are also generated directly on the keyboard. All other codes in Columns 0 and 1 are ignored by the Terminal.

TABLE 1. TERMINAL CODE CHART

BITS 7	6	5	4	Column → / Row ↓	0 (0 0 0)	1 (0 0 1)	2 (0 1 0)	3 (0 1 1)	4 (1 0 0)	5 (1 0 1)	6 (1 1 0)	7 (1 1 1)
0	0	0	0	0	NUL	DLE	SPACE	0	@	P		
0	0	0	1	1	SOH	DC1	!	1	A	Q		
0	0	1	0	2	STX	DC2	"	2	B	R		
0	0	1	1	3	ETX	DC3	#	3	C	S		
0	1	0	0	4	EOT	DC4	$	4	D	T		
0	1	0	1	5	ENQ	NAK	%	5	E	U		
0	1	1	0	6	ACK	SYN	&	6	F	V		
0	1	1	1	7	[BEL]	ETB	'	7	G	W		
1	0	0	0	8	[BS]	CAN	(	8	H	X		
1	0	0	1	9	HT	EOM	)	9	I	Y		
1	0	1	0	A	[(LF)]	SUB	*	:	J	Z		
1	0	1	1	B	VT	(ESC)	+	;	K	[		
1	1	0	0	C	FF	FS	,	<	L	\		
1	1	0	1	D	[(CR)]	GS	-	=	M	]		
1	1	1	0	E	SO	RS	.	>	N	↑		
1	1	1	1	F	SI	US	/	?	O	←		RUB OUT

4. DATA FORMAT

The PASLA may be programmed to accomodate a variety of character formats and baud rates. See the PASLA Programming Specification, 02-270A22, in the 29-301 PASLA Instruction Manual. The TTY Interface operates at 110 baud or 1200 baud for M46-107 with a fixed character format. The Programming Specification, 02-262A22, in the 29-288 TTY Interface Instruction Manual contains TTY Programming information. In addition, the CRT has switch options to select parity, number of stop bits, and baud rate. This information is in Manual 29-327 which is included with the CRT.

The following lists the standard characteristics:

	PASLA	TTY
BAUD RATE	9600	*110
DATA BITS	7	7
PARITY	EVEN	EVEN
STOP BITS	1	1

*1200 baud for M46-107.

Figure 3 shows the Character Format:

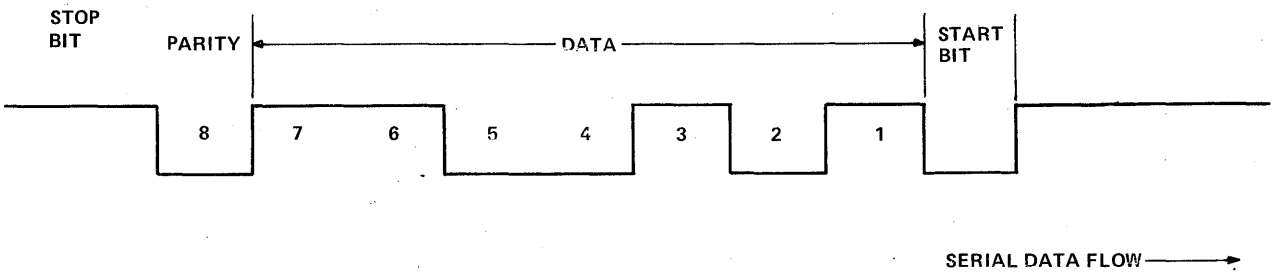

Figure 3. Character Format

5. PROGRAMMING INSTRUCTIONS

The Processor I/O instructions are used to communicate with the CRT Terminal through the PASLA/TTY. The following paragraphs describe how Processor I/O instructions may be used with the system.

5.1 Program Instructions

5.1.1 Sense Status (SS or SSR). The Sense Status instruction is used to determine if character transfers are complete and correct.

5.1.2 Output Command (OC or OCR). The Output Command instruction is used to set the PASLA to the Receive or Transmit Mode and tc select character format. Two command bytes are required to perform these functions with PASLA. If TTY, only one Output Command is required to establish read or write mode.

5.1.3 Write Data (WD or WDR). The Write Data instruction is used to output characters to the CRT terminal screen.

5.1.4 Read Data (RD or RDR). The Read Data instruction is used to input characters from the CRT terminal keyboard.

5.1.5 Acknowledge Interrupt (AI or AIR). The Acknowledge Interrupt instruction is used to service interrupts. Execution of this instruction returns the address and status of the interrupting line.

5.1.6 Communications Instructions (PASLA only). The PASLA accomodates the Communication Instructions in the Communications Processors.

5.2 Status and Command Bytes

Table 2 contains the PASLA and TTY Interface Status and Command Byte Data applicable to the CRT Terminal.

TABLE 2. STATUS AND COMMAND BYTE DATA

	BIT NUMBER	0	1	2	3	4	5	6	7
PASLA	STATUS (REC)	OV	PF	FR ERR	0	BSY	EX	0	0
PASLA	STATUS (TRANS)	0	0	0	0	BSY	0	0	0
PASLA	COMMAND 1	DIS	EN	DTR	ECHO-PLEX	0	TRANS. LB	WRT/ RD	1
PASLA	COMMAND 2	0	CLK	← DATA	BITS →	STOP BITS	← PARITY →		0
TTY	STATUS	OV	0	LINE BREAK	0	BSY	EX	0	DU
TTY	COMMAND	DIS	EN	UN-BLOCK	BLOCK	WRT	READ	0	0

STATUS

*OV — The Overflow status bit is set if the previously received character is not read before the present character is assembled. Overflow is reset at the end of the next Read Data only if the failure condition disappears (i.e. a Read Data is issued).

*PF — This bit is set when the received parity disagrees with the programmed parity (EVEN parity). The PF status is reset at the end of the next character if the failure condition disappears. The PASLA is normally programmed for no parity checking (Bits 5 and 6 of Command 2 = 00) so PF will never set.

*FRERR — This bit is set to indicate that the received character has no stop bits. If the assembled character is zero, then a line break sequence is indicated. This occurs when the Break key is depressed. This bit will reset only when a valid character with stop bits is received.

*BRK — This bit is set whenever the serial data line remains at zero for longer than one character time. This occurs when the Break Key is depressed.

BSY — When this bit is inactive, the device is ready to transfer data. This bit is forced active if the CRT Terminal is Off-Line. In the Read Mode, BSY is active when a character is not assembled; in the Write Mode, BSY is active if the CRT Terminal has not yet accepted a character. If enabled, an interrupt is generated when BSY goes inactive. In the Read Mode, when an OV occurs and the BSY status bit is zero, a Read Data instruction must be issued to set the BSY bit to its correct (ONE) state.

EX — This bit is set whenever OV, PF, FRERR or BRK is set on the Receive side. This bit is always zero on the Transmit side.

DU — This bit is set whenever the CRT Terminal is Off-Line or Powered Down. An interrupt is generated, if enabled, when DU goes active.

With PASLA, to determine whether the CRT Terminal is On-Line or not, the status of the Receive side must be examined. If the status byte is 'OC' (BUSY and EX), a Device Unavailable condition is indicated.

*These status bits are set at End of Character time when the BUSY drops. Since the resetting of BUSY causes an interrupt (if enabled), these bits do not generate individual interrupts. At this point a Read Data instruction must be issued to set the Busy bit to its correct (ONE) state.

COMMANDS

In the PASLA Command 1, the DTR, ECHOPLEX, and WRT/RD bits are shared by the Transmitter and Receiver, however, the EN/DIS bits are separate for Transmit and Receive. In FDX operation, the EN/DIS must be independently programmed as follows. To change EN/DIS on the Receive side, issue a Command with the WRT/RD bit = 0. To change the EN/DIS on the Transmit side, issue a Command with the WRT/RD bit = 1.

CLK

Setting this bit selects the highest strapped clock rate. Resetting this bit selects the lowest strapped clock rate.

DATA BITS

These two command bits select the number of data bits transferred per character as follows:

BIT 2	3	
0	0	5 Data Bits
0	1	6 Data Bits
1	0	7 Data Bits
1	1	8 Data Bits

STOP BITS

This command bit selects the number of stop bits transferred per character.

BIT 4	
0	1 Stop Bit
1	2 Stop Bits

PARITY

These two command bits select the parity checking logic in the PASLA.

BIT 5	6	
0	0	None
0	1	None
1	0	Odd
1	1	Even

The second PASLA command is shared by both the Transmit and Receive Sides, and consequently may be issued to either device number. The second command has the preferred value of X'66' that conditions the PASLA to the following:

1. Highest strapped baud rate (9600 baud standard)
2. 8 data bits per character
3. Even Parity
4. Two stop bits

DISABLE	ENABLE	
0	0	No change
0	1	Enable
1	0	Disable (Interrupt queued)
1	1	Complement (Change state)

TRANS LB

Transmits a continuous space (zero) to the Terminal. This bit should always be a zero.

DTR

This bit must always be a one to enable character transfers between PASLA and the CRT.

ECHO-PLEX

When this bit is active, it causes data received from the CRT Keyboard to be transmitted back to the CRT on the TRANSMITTED DATA (BA) line. The PASLA also assembles the character as in the normal data mode. This feature is normally used to provide visual verification of the data received by the CRT. This command must not be issued while transmitting a character. When this bit is inactive, characters read from the Keyboard are not displayed.

UNBLOCK	Setting this bit causes characters read from the keyboard to be displayed on the CRT screen in addition to being assembled by the TTY Interface.
BLOCK	Setting this bit prevents characters read from the keyboard from being displayed. These characters, however, are assembled by the TTY Interface.
WRT/RD	Setting this bit places the PASLA in the Write Mode. Clearing this bit places the PASLA in the Read Mode. This bit should always be set in FDX except as noted in commands above.
WRITE	Setting this bit places the interface in the Write Mode, allowing data to be output from the Processor to the CRT.
READ	Setting this bit places the interface in the Read Mode, allowing data to be transferred from the CRT to the Processor.

6. PROGRAMMING SEQUENCES

6.1 Table 3 shows a sample program for transferring data from the CRT keyboard using PASLA.

6.2 Table 4 shows a sample program for transferring data to the CRT screen using PASLA.

7. INTERRUPTS

An interrupt will occur, if enabled, when BSY→0 for either the PASLA or TTY Interface. In addition, the TTY Interface generates an interrupt when DU changes state.

8. INITIALIZATION

When the Initialize Switch on the Display Panel is engaged (or power failure restart sequence), the PASLA is placed in the Disable Mode. The OV, PF, and BRK status bits cannot be guaranteed. Because of this, the programmer should take precautions to ignore these bits on the first interrupt. A Read Data (RD or RDR) should be issued to insure that BUSY is equal to a one (1).

TABLE 3. SAMPLE PROGRAM FOR DATA INPUT FROM THE KEYBOARD

```
*INPUT VIA PASLA
*
*
*A BYTE WILL BE INPUT TO R4 FROM THE KEYBOARD.
*REGISTERS R3, R4 AND R15 WILL BE USED.
*CALLING SEQUENCE IS BAL, R15, INPUT
*
*
*INPUT    LHI     R3, DEVNO          LOAD DEVICE NUMBER
          OC      R3, COMND          SET UP
          OC      R3, COMND+1        PASLA MODE
SENS      SSR     R3, R4             TEST STATUS
          BTBS    15, 1              LOOP
          RDR     R3, R4             INPUT BYTE
          BR      R15                RETURN

*
R3        EQU     3                  REGISTER ASSIGNMENTS
R4        EQU     4
R15       EQU     15
DEVNO     EQU     10                 PASLA DEVICE NUMBER
*
COMND     DC      X'9366'
          END
```

TABLE 4. SAMPLE PROGRAM FOP DATA OUTPUT TO THE CRT SCREEN

```
*OUTPUT VIA PASLA
*
*
*A BYTE WILL BE OUTPUT FROM R4 TO THE CRT
*REGISTERS R3, R4, R5, R15 WILL BE USED
*CALLING SEQUENCE IS BAL R15, OUTPUT
*
*
*
OUTPUT    LHI     R3, DEVN0+1          LOAD DEVICE NUMBER
          OC      R3, COMND            SET UP
          OC      R3, COMND+1          PASLA MODE
SENS      SSR     R3, R5               TEST STATUS
          BTBS    15, 1                LOOP
          WDR     R3, R4               OUTPUT BYTE
          BR      R15                  RETURN

*
R3        EQU     3                    REGISTER ASSIGNMENTS
R4        EQU     4
R5        EQU     5
R15       EQU     15
DEVN0     EQU     10                   PASLA DEVICE NUMBER
*
COMND     DC      X'9166'
          END
```

9. DEVICE NUMBER

The PASLA is normally strapped for addresses X'10' and X'11'. The even address is for the Receive side and the odd address is for the Transmit side.

10. SAMPLE PROGRAMS

See Section 6.

11. TESTING

The PASLA is tested independently at INTERDATA using the PASLA OFF-LINE TEST PROGRAM, 06-127. The PASLA and CRT Terminal are then tested together using the CRT TEST PROGRAM, 06-146.

INTERDATA

TEC NO	TERMINAL	SIGNAL WIRING	MONITOR
99/1933-001	D.SX-XXXXA-	VIEW A	VIEW A
99/1933-002	D.SX-XXXXB-	VIEW B	VIEW B
99/1933-003	TEC-7325A	VIEW C	VIEW C

REVISIONS

RELEASED FOR PRODUCTION

ENG. J. PISARCIK DATE 8-16-73

P11
SIGNAL WIRING TO MONITOR VIEW B

10 PIN CONNECTOR

P12 3 PIN CONNECTOR

5 HORIZ · 7 SIGGND · 9 VERT · 10 SIGGND · 7 VIDEO · 2 · 3 · 8

BRN 1 · RED 2 · ORN 3 · BRIGHT

P2-23 · P2-25 · P2-27 · P2-29 · P2-26

CARD CAGE
VIEW B

P1-3 BLU -5V
11 ORN -10V
P1-4 12 VIO -15V
P1-6 14 YEL +15V
P1-5 13

BUS 85-86

BUS 1-2

VA · VG

VIDEO RG58A/U

SIGNAL WIRING TO BACK PANEL J12

BNC CONN

30 PIN CONNECTOR

POWER IN H G N

115/230 SELECT SWITCH 115

PWR SW

V SEL SW

LINE PLUG & FILTER

2 AMP SLOW-BLOW F1

BLK · GRN · GRN

WHT · BLK · WHT · WHT

POWER SWITCH

BLK

PCB ASSY 933069 CIRCUIT SIDE

-15V VIO · -10V ORN · -5V BLU

+15V YEL · C+ RED · RED 20VAC · C- BRN · 20VAC RED · GND GRN · YEL CT

BRN · RED · GRN

SPLICES

GRN · GRN · GRN/YEL

C1 · C2

XFORMER 75/1043-0C

WHT · BLU · ORN · BLK

BLK 1 · RED/BLK 2 · YEL/BLK 3 · BLK/GRN 4

4 PIN CONNECTOR

BRN · BRN · BRN · BRN · GRN · WHT · WHT · WHT · BLU · BLU · BLU · ORN · ORN · ORN · BLK · BLK · BLK · RED · RED · RED · RED

1 GND
2 115/230V. AC N
3
TB1
4
5 115/230 VAC H
6 +5V 5V POWER SUPPLY

SIGNAL WIRING FROM CARD CAGE

MONITOR - 740031-XXX
VIEW B

WHT 1 · BLU 2 · ORN 3 · BLK 4

4 PIN CONNECTOR

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

NOTES

SHEET INDEX — REV. LEVEL / SHT. NO. 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

NAME	TITLE	DATE
B GRAY	DRAFT	8-10-73
R CERO	CHK	
J PISARCIK	ENGR	8-16-73
N. MASI	TEST	8-16-73
J PISARCIK	MGR	8-16-73

TITLE WIRE & CABLE DIAGRAM-MODEL 440 TERMINAL

SIZE 03038 · DWG NO. 02-310 B08 · REV 1 · SHEET 32

BRUNING 44 7-51 TH042

INTERDATA

990038

REVISIONS				
REV.	DESCRIPTION	DCN	APPD	DATE
A	RELEASED	-	JWJ	9/SEP/73

X6-9
X11
X13

1-6	+5V	1	2	+5V		6
1-6	-5V	3	4	-10V		6
1-6	+15V	5	6	-15V		6
—		7	8			—
—		9	10			—
—		11	12			—
—		13	14			—
—		15	16			—
—		17	18			—
—		19	20			—
—		21	22			—
—		23	24			—
—		25	26			—
—		27	28			—
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—		45	46			—
—		47	48			—
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1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
—	24MHZ	83	84	12MHZ		1-4
X,1-4 1-6	GND	85	86	GND		1-6

P1
TIMING GENERATOR

1-6	+5V	1	2	+5V		1-6
1-6	-5V	3	4	-10V		1-6
1-6	+15V	5	6	-15V		1-6
—		7	8			—
2-6	SPACE 2	9	10	INHDSP		2-6
2-3	DBLM 1	11	12	DBLM 2		2-3
2-3	DBLM 3	13	14	DBLM 4		2-3
2-3	DBLM 5	15	16	DBLM 6		2-3
2-3	DBLM 7	17	18	CHDET		2-6
—		19	20			—
—		21	22	CVIDEO	Y1	
Z5	HDRIVE	23	24	SGND	Y2	
Z1	SGND	25	26	NVIDEO	Z7	
Z9	VDRIVE	27	28	SGND	—	
Z10	SGND	29	30	LMCLK		2-4
1-6		31	32			1-6
1-6		33	34			1-6
1-6		35	36			1-6
1-6		37	38	LMLOAD		1-4
1-4		39	40			1-2
2-6	CA-1	41	42			1-6
2-6	CA+1	43	44	DECPRA		2-6
2-6	LFCOL	45	46	ST2448		2-6
2-6	OPRBEL	47	48	SETLMC		2-6
1-3	RPT 1	49	50	RPT 2		1-3
1-2	SCCT 1	51	52	SCCT 2		1-2
1-2	SCCT 3	53	54	SCCT 4		1-2
1-6		55	56			1-2
1-4		57	58	PUCLR		1-6
1-2	ENAB72	59	60	ENABBO		1-6
1-6	DOT A	61	62	DOT B		1-6
1-6	DOT C	63	64	DOT D		1-6
1-6	DOT E	65	66	DOT F		1-6
1-6	SCAN A	67	68	SCAN B		1-6
1-6	SCAN X	69	70	ROWEN		1-6
1-6	DOT 1	71	72	DOT 2		1-6
1-6	DOT 3	73	74	DOT 4		1-6
1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
—		83	84	12 MHZ		1-4
1-6	GND	85	86	GND		1-6

P2
LINE MEM — CHAR GEN

1-6	+5V	1	2	+5V		1-6
1-6	-5V	3	4	-10V		1-6
1-6	+15V	5	6	-15V		1-6
3-6	SPACE 1	7	8	EXCSPG		3-6
2-6	SPACE 2	9	10	INHDSP		2-6
2-3	DBLM 1	11	12	DBLM 2		2-3
2-3	DBLM 3	13	14	DBLM 4		2-3
2-3	DBLM 5	15	16	DBLM 6		2-3
2-3	DBLM 7	17	18	CHDET		2-6
3-6	CLRSCN	19	20	PGSTOP		3-6
3-6	DBPM 1	21	22	DBPM 2		3-6
3-6	DBPM 3	23	24	DBPM 4		3-6
3-6	DBPM 5	25	26	DBPM 6		3-6
3-6	DBPM 7	27	28			3-6
3-6		29	30	LMCLK		2-4
1-6		31	32			1-6
1-6		33	34			1-6
1-6		35	36			1-6
1-6		37	38	LMLOAD		1-4
1-4		39	40	PMLOAD		3-6
2-6	CA-1	41	42			1-6
2-6	CA+1	43	44	DECPRA		2-6
2-6	LFCOL	45	46	ST2448		2-6
2-6	OPRBEL	47	48	SETLMC		2-6
1-3	RPT 1	49	50	RPT 2		1-3
3-4	LSBCCT	51	52	NSBCCT		3-4
3-4		53	54			3-4
1-6		55	56	PGCLKA		3-4
1-4		57	58	PUCLR		1-6
3-6		59	60	ENABBO		1-6
1-6	DOT A	61	62	DOT B		1-6
1-6	DOT C	63	64	DOT D		1-6
1-6	DOT E	65	66	DOT F		1-6
1-6	SCAN A	67	68	SCAN B		1-6
1-6	SCAN X	69	70	ROWEN		1-6
1-6	DOT 1	71	72	DOT 2		1-6
1-6	DOT 3	73	74	DOT 4		1-6
1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
—		83	84	12 MHZ		1-4
1-6	GND	85	86	GND		1-6

P3
PAGE MEMORY

1-6	+5V	1	2	+5V		1-6
1-6	-5V	3	4	-10V		1-6
1-6	+5V	5	6	-15V		1-6
3-6	SPACE 1	7	8	EXCSPG		3-6
2-6	SPACE 2	9	10	INHDSP		2-6
4-6	TWOMHZ	11	12	LOC-REM		4-6
4-6	FRCFDP	13	14	FRCTTY		4-6
4-6	TENBIT	15	16	SLSPDX		4-6
4-6		17	18	CHDET		2-6
3-6	CLRSCN	19	20	PGSTOP		3-6
3-6	DBPM 1	21	22	DBPM 2		3-6
3-6	DBPM 3	23	24	DBPM 4		3-6
3-6	DBPM 5	25	26	DBPM 6		3-6
3-6	DBPM 7	27	28			3-6
3-6		29	30	LMCLK		2-4
1-6		31	32			1-6
1-6		33	34			1-6
1-6		35	36			1-6
1-6		37	38	LMLOAD		1-4
1-4		39	40	PMLOAD		3-6
2-6	CA-1	41	42			1-6
2-6	CA+1	43	44	DECPRA		2-6
2-6	LFCOL	45	46	ST2448		2-6
2-6	OPRBEL	47	48	SETLMC		2-6
4-6	CRSOVR	49	50	XRNRST		4-6
3-4	LSBCCT	51	52	NSBCCT		3-4
3-4		53	54			3-4
1-6		55	56	PGCLKA		3-4
1-4		57	58	PUCLR		1-6
3-6		59	60	ENABBO		1-6
1-6	DOT A	61	62	DOT B		1-6
1-6	DOT C	63	64	DOT D		1-6
1-6	DOT E	65	66	DOT F		1-6
1-6	SCAN A	67	68	SCAN B		1-6
1-6	SCAN X	69	70	ROWEN		1-6
1-6	DOT 1	71	72	DOT 2		1-6
1-6	DOT 3	73	74	DOT 4		1-6
1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
—		83	84	12 MHZ		1-4
1-6	GND	85	86	GND		1-6

P4
PAGE CONTROL

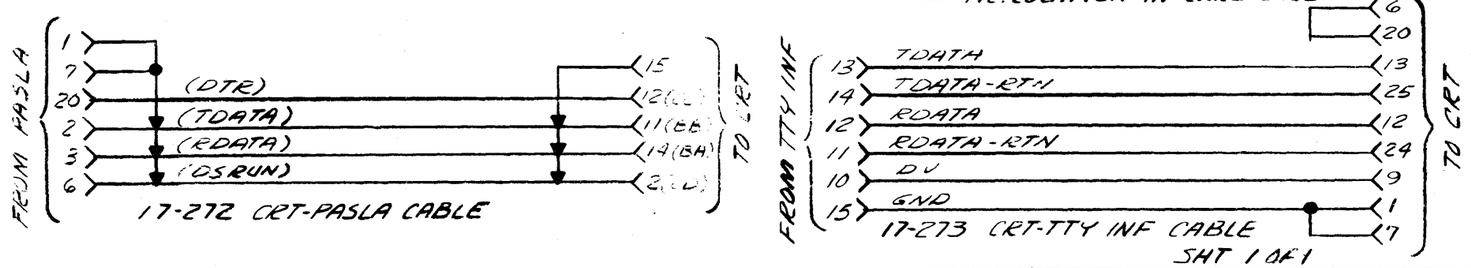
1-6	+5V	1	2	+5V		1-6
1-6	-5V	3	4	-10V		1-6
1-6	+5V	5	6	-15V		1-6
3-6	SPACE 1	7	8	EXCSPG		3-6
2-6	SPACE 2	9	10	INHDSP		2-6
4-6	TWOMHZ	11	12	LOC-REM		4-6
4-6	FRCFDP	13	14	FRCTTY		4-6
4-6	TENBIT	15	16	SLSPDX		4-6
4-6		17	18	CHDET		2-6
3-6	CLRSCN	19	20	PGSTOP		3-6
3-6	DBPM 1	21	22	DBPM 2		3-6
3-6	DBPM 3	23	24	DBPM 4		3-6
3-6	DBPM 5	25	26	DBPM 6		3-6
3-6	DBPM 7	27	28			3-6
3-6		29	30	LMCLK		5-6
1-6		31	32			1-6
1-6		33	34			1-6
1-6		35	36			1-6
1-6		37	38			5-6
5-6		39	40	PMLOAD		3-6
2-6	CA-1	41	42			1-6
2-6	CA+1	43	44	DECPRA		2-6
2-6	LFCOL	45	46	ST2448		2-6
2-6	OPRBEL	47	48	SETLMC		2-6
4-6	CRSOVR	49	50	XRNRST		4-6
5-6		51	52	XSRCLK		5-6
5-6	RSDATA	53	54	XRNSTP		5-6
1-6		55	56			5-6
5-6	BELL	57	58	PUCLR		1-6
3-6		59	60	ENABBO		1-6
1-6	DOT A	61	62	DOT B		1-6
1-6	DOT C	63	64	DOT D		1-6
1-6	DOT E	65	66	DOT F		1-6
1-6	SCAN A	67	68	SCAN B		1-6
1-6	SCAN X	69	70	ROWEN		1-6
1-6	DOT 1	71	72	DOT 2		1-6
1-6	DOT 3	73	74	DOT 4		1-6
1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
		83	84			
1-6	GND	85	86	GND		1-6

P5
FUNCTION CONTROL

1-6	+5V	1	2	+5V		1-6
1-6	-5V	3	4	-10V		1-6
1-6	+5V	5	6	-15V		1-6
3-6	SPACE 1	7	8	EXCSPG		3-6
2-6	SPACE 2	9	10	INHDSP		2-6
4-6	TWOMHZ	11	12	LOC-REM		4-6
4-6	FRCFDP	13	14	FRCTTY		4-6
4-6	TENBIT	15	16	SLSPDX		4-6
4-6		17	18	CHDET		2-6
3-6	CLRSCN	19	20	PGSTOP		3-6
3-6	DBPM 1	21	22	DBPM 2		3-6
3-6	DBPM 3	23	24	DBPM 4		3-6
3-6	DBPM 5	25	26	DBPM 6		3-6
3-6	DBPM 7	27	28			3-6
3-6		29	30			5-6
1-6		31	32			1-6
1-6		33	34			1-6
1-6		35	36			1-6
1-6		37	38			5-6
5-6		39	40	PMLOAD		3-6
2-6	CA-1	41	42			1-6
2-6	CA+1	43	44	DECPRA		2-6
2-6	LFCOL	45	46	ST2448		2-6
2-6	OPRBEL	47	48	SETLMC		2-6
4-6	CRSOVR	49	50	XRNRST		4-6
5-6		51	52	XSRCLK		5-6
5-6	RSDATA	53	54	XRNSTP		5-6
1-6		55	56			5-6
5-6	BELL	57	58	PUCLR		1-6
3-6		59	60	ENABBO		1-6
1-6	DOT A	61	62	DOT B		1-6
1-6	DOT C	63	64	DOT D		1-6
1-6	DOT E	65	66	DOT F		1-6
1-6	SCAN A	67	68	SCAN B		1-6
1-6	SCAN X	69	70	ROWEN		1-6
1-6	DOT 1	71	72	DOT 2		1-6
1-6	DOT 3	73	74	DOT 4		1-6
1-6	DOT 5	75	76	DOT 6		1-6
1-6	DOT 7	77	78	DCRST		1-6
1-6	ESYNC	79	80	72-80		1-6
1-6	HSYNC	81	82	VSYNC		1-6
		83	84			
1-6	GND	85	86	GND		1-6

P6
INTERFACE

P.C. LOCATION IN CARD CAGE



SHT 1 OF 1

X

1	GND	85,86
2		85,86
3		85,86
4		85,86
5		NC
6		
7	+5V	
8		
9		
10		NC
11	5V	3
12	0V	4
13	+5V	5
14	-15V	6
15		NC

Y

1	VIDEO	P2 22
2	SGND	P2 24

Z

1	SGND	P2-25
2		NC
3		NC
4		NC
5	HDRIVE	P2-23
6		NC
7	NVIDEO	P2-26
8		NC
9	VDRIVE	P2-27
10	SGND	P2-29

NAME	TITLE	DATE
B GRAY	DRAFT	7-18-73
R CERO	CHK	
J PISARICK	ENG	
J PISARICK	MGR	

TITLE CARD CAGE CONNECTIONS
27-053 CRT

SIZE D | DRAWING NO 02-310 | A
SCALE | SHT 2 OF 32

990055

A	RELEASED	

VIDEO AMP

PIN
1 - GND
2 - 150V (WHT)
3 - BRT. CRT. LUG (YEL)
4 - OPEN
5 - HOR. SYNC. (YEL/BLU.)
6 - OPEN
7 - VIDEO INPUT
8 - GND
9 - V. SYNC. (RED/GRN.)
10 - GND

P.C. EDGE CONNECTOR

VIDEO INPUT 7 — R5 250 CONTRAST 18D67559A03 — C4 47/35V "ER" — R8 1.8K — R7 4.7K — 30V B++ — R9 2.7K — R10 4K — VIDEO BIAS 18D6640IA44 — R11 120 — C6 470/16V "EB" — Q2 VIDEO PREAMP 7324/P4C — Q3 VIDEO OUT 4919/A1M — R13 3.9K 7W — 150V B+++ — BOOT — R17 2 MEG — FOCUS 18D67858A12 — R12 470 — 48D67120A11 D6 D8 — Q4 VIDEO DR 7317/A8H — C7 270 10% X5F — R14 82 — C8 470-10% XF5 — R15 56

IN CRT. LEADS — R18 1K — R19 47K — R20 47K — R32 270K — GRN — RED — BLU — BRN — BLK — YEL — WHT — SPARK GAPS ALL CONNS. (PART OF CRT SOCKET)

CRT 12" CLINTON CE226-12P4S15-XM354-20 965227A01 / CE226-12P3S15-XM354-40 965234A01 — G2

C10 .22/160V 10% HS ON PANEL — R23 39K

HORIZONTAL

B++ 30V — R25 27K — Q5 7317/A8H — HOR. SYNC. 5 — R70 2.2K — R27 2.2K — C13 330 10% X-5F — C14 — R28 180K — R29 180K — D7 & DET 4917 D/C

R30 47K — C16 10UF +40-20 15V 23S102 29A07 — R31 100K — C17 .033/250V KT — R32 3.3K — R33 6.8K 5% — C18 .01 10% CLASS "E" — C19 .0082 10% CLASS "E" — L1 24D68822 A08 (AK-268A) HOR. HOLD — R34 390 — C15 2.7K 10% 25F

R37 1K — Q6 HOR. OSC. 7317/A8H — Q7 HOR. PULSE SHAPER 7324/P4C — R38 1K 5% — C20 .01 160V 10% HX — R39 82 — 30V B++ — Q8 HOR. DR. 4919/A8H — R40 1K 1W — R41 220 — C21 1K 10% X5F — R42 1.5K

T1 HOR. DRIVER TRANS. 25D67440A03 — C25 1K 10% X5F — C22 100/63V HX — R43 1.5K 3W GLASS — R44 4.7Ω 2W WW — C24 150UF 10V 23C65 282A40 — C23 22-10% N150 — R45 180K 1W

Q9 HOR. OUTPUT 4996/A3H — D4 H.V. RECT. 48513720I/D3S (TV-18) — R46 33K 1W "AB" — T2 H.V. TRANS. 24D69791A04 — D1 DAMPER 4821 DND — D2 PULSE LIMITER — C28 .0068 5% 1KV "MP" — C29 .56 250V 10% "D" — C30 .047 160V 10% HS ON PANEL — D5 48S191 A05 B+++ RECT. — 150V B++++ — C43D 20/200

R47 680K — BOOT — R48 4.7M — ON PANEL — C26 47 630V — C27 LO 10% 630V "MM" — 150V B++++ — C31 330 10% X5F — R49 150 — L3 LIN 24D69163A09

C32 5K 10% 1KV 38F

POWER SUPPLY

F2 0.4AMP 655138562 — BLK/RED — T4 POWER TRANS. 25D63164A17 (DC-364) — 115V 50/60HZ — BLK/YEL — RED/GRN/YEL — RED — D11 — D10 — D12 — D9 — 48S191A05 — V1 HEATER 6.3V — GRN — YEL — F1 0.4 AMP 655138562 — 21S10330A05 C45 1.5K 20% 1.4KV

178B32662 R79 105Ω 10W W.W. — Q16 7368/A8W — C43A 400/125V — R77 100 — Q14 49521AJ2 — R78 5.6K — R76 5.6K — R75 1K — Q15 7315/A8G — D6 ZENER 7266/D4H — C44 .01 50V Z5V

73V B+++ — R71 2.7K A-S — R74 2K 17D65620A57 — R73 2.2K — R72 15K — R69 1.2K 5W IRC — B+++ — C43B 600V 100V — C43C 200/50V — 23C65807A47

VERTICAL

R50 6.2K 5% — R55 18K 5% — C36 4.7UF +80-10 100V — C33 .47 100V — C35 .01 160V 10% HX — Q10 VERT. OSC. 1 7324/P4C — Q11 VERT. OSC. 2 7317/A8H — C44 .01 160V 10% — R54 33 — R53 68 — R57 6.8K — R56 39K — R58 82K 5% — D3 48567120A18 — C37 2.2UF 10% 100V "MM" — C38 2.2UF 100V 10% "MM" — R59 4K — R62 4.7K — R61 820 1W — 30V B++ — Q12 VERT. DRIVER 7325/A8L — R63 1K — VERT. LIN 18D66401A44 — C39 .22 160V 10% HS — R60 1.8K — C40 1UF 100V 10% "MM" — R64 10 1W F.C. ONLY — R65 15 — VERT. SIZE 17D65820A34 — VERT. SYNC 9 10

Q13 VERT OUTPUT 4900/A1C — R67 18K — ON PANEL — V.D.R. R80 6C66263A08 — C41 .01 10% 600V 85100644A06 — R66 4.7K 1W "AB" — T3 VERT. OUT. TRANS. 25D6584A22 — 73V B+++ — L4 24D69163A10 (WIDTH) — RED — BLK — GRN — C42 1.5K 10% X5F — R68 150 — L5 YOKE 24D68523A10

UNLESS OTHERWISE SPECIFIED:
RESISTORS: (COMP.) 10%, 1/2W
F.C. FIXED COMPOSITION
W.W.-WIRE WOUND
"AB" IS SELECTED SUPPLIER
CAPACITORS: CERAMICS ARE DISC.
PF, 500 V.D.C. GMV
OR +80%-20%
TUBULARS: 100 V.D.C. MYLAR
MFD ± 20%
"HS", "HX" IS MYLAR
"HB," "HW," "MN" IS METALIZED MYLAR
"MP" IS MYLAR PAPER
LYTICS: "T" IS TANTALUM
TRANSISTOR PART NO PREFIX-48513
------ INDICATES PRINTED CIRCUIT BOARD
⊗ INDICATES WIRE WRAP TERMINAL

SHT 1 OF 1

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS ±
DECIMALS
ONE PLACE (.0) ±
TWO PLACE (.00) ±
THREE PLACE (.000) ±
ANGLES ±
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

NEXT ASSY. | FIRST USED
MATERIAL
FINISH

TITLE: SCHEMATIC - MOTOROLA MONITOR - 12 INCH

SIZE D | DRAWING 02-310 | REV A
SCALE NONE | SHT 1 OF 1

INTERDATA

REVISIONS				
SYM	DESCRIPTION	DCN	APPD	DATE
A	RELEASED	—		
B	REV PER DCN	8165		
C	REV PER DCN	8206		
D	REV PER DCN	8205		
E	REV PER DCN	8212		
F	REV PER DCN	8265		
G	B/M CHG ONLY	8403		
G1	B/M CHG ONLY	8423		
H	NO CHG - SEE DCN	8531		

FROM POWER TRANSFORMER

AC
CT
AC
C+
C
C−

DB1

C1 5500 µF 25V
C2 5500 µF 25V
C3 6.8 µF 35V
C4 6.8 µF 35V

D1
R1 1.5Ω
Q1 2N3740
IC 1 LM305
C6 100 PF
R2 47K
R3 2K
R4 5.1K
D2
C5 15 µF 20V
R5 2.2K

+15VDC
GND

R8 2K
R9 6.8K
IC 2 LM304
C7 15 µF 10V
D3
R10 2.7KΩ
Q2 2N3740
D4
R7 2.4K
C8 100 PF
R6 1.5Ω 1/2W
−15VDC

R18 2K
R19 1.6K
R21 15Ω 10W
R22 15Ω 10W
IC 4 LM304
C11 15 µF
D7
R20 680Ω
Q4 2N3740
D8
R17 2.4K
C12 100 PF
R16 1.5Ω 1/2W
C13 15 µF 20V

−10VDC
R13 2K
R14 4.7K
IC 3 LM304
C9 15 µF 20V
D5
R15 1.5KΩ
Q3 2N3740
D6
R12 2.4K
C10 100 PF
R11 1.5Ω 1/2W

272743 POWER SUPPLY P.C.B.

−5VDC

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W, 5%.
2. DIODES D1 THRU D8 ARE IN4003.
3. LAST DESIGNATION USED: R22, C13, Q4, DB1, D8.
4. Q1–Q4: 2N3741 MAY BE SUBSTITUTED FOR 2N3740.

SHT 1 OF 1

933069-000	440	
NEXT ASSY.	FIRST USED	
MATERIAL		
FINISH		

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS ±
DECIMALS
ONE PLACE ±
TWO PLACES ±
THREE PLACES ±
ANGLES ±
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

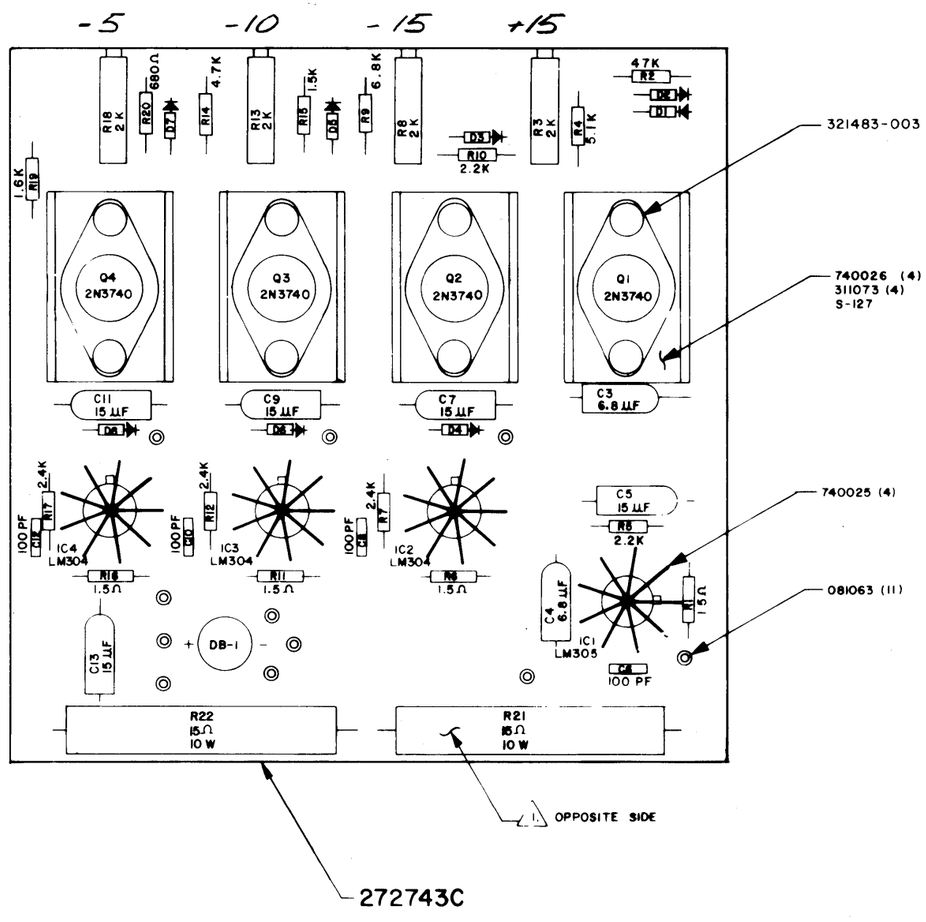
TITLE: SCHEMATIC— POWER SUPPLY

8-6-72	SIZE D	DRAWING NO. 930310	REV. H
2-JUN 72	SCALE NONE	SHEET 4 OF 32	
1-JUN 72			

INTERDATA

T-933069-000

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED	——		6-22-71
B	REV PER DCN	8165		13 MAY 72
C	REV PER DCN	8206		26 JUL 72
D	REV PER DCN	8205		4 AUG 72
E	REV PER DCN	8212		17 AUG 72
F	REV PER DCN	8265		8 SEP 72
G	B/M CHG ONLY	8403		10/11/72
G1	B/M CHG ONLY	8423		10/25/72
H	REV PER DCN	8531		23 JAN 73



NOTES

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD
5. Q1-Q4: 2N3741 MAY BE SUBSTITUTED FOR 2N3740.

PARTS LIST ISSUED

SHT 1 OF 1

440			TITLE P.W. ASSY- POWER SUPPLY	
6-3-21	SIZE D	DRAWING NO. 02-310		REV H
9 SEP 72	SCALE 2/1	SHEET 5 OF 32		
6-22-71				

992408

INTERDATA

A	RELEASED	8184
B	NO CHG	8184
C	NO CHG	8220
D	REV PER DCN	8498
E	NO CHG SEE DCN	

NOTES
1. UNLESS OTHERWISE SPECIFIED
   A. ALL DIODES ARE TEC-102
   B. ALL RESISTORS ARE 1/4 W, 0%
2. ⟶ INDICATES NO CONNECTION

UNUSED ELEMENTS

IC8 K115 (pins 2, 3)

CHIP TYPE	DESIGNATION
7400	IC7
7402	IC8, IC9
7408	IC5, IC6
7493	IC3, IC4
74123	IC10
74151	IC1
74154	IC2

SHT 1 OF 2

933183	272462		
MATERIAL			
FINISH			

TITLE: SCHEMATIC – KEYBOARD, TTY RFL EKA-9100

1 13 71 | D | DRAWING NO 02-310 | E

NONE | SHT 6 | 32

INTERDATA

992408

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED			
B	NO CHG	8184		
C	NO CHG.	8184		
D	REV PER DCN	8220		
E	NO CHG SEE DCN	8498		

IC2
K200

IC1
K201

SHIFTABLE KEYS

SHIFTABLE

+5V

CR

LINE FEED

ESC

RUB OUT

SP

R30 1K
R31 1K
R32 1K
R33 1K
R34 1K
R35 1K
R36 1K
R37 1K

SHT 2 OF 2

SCHEMATIC — KEYBOARD, TTY, RPL
EKA-9100

933183 272462

1-3-71 D 02-310 E
2-1-72 NONE 7 32

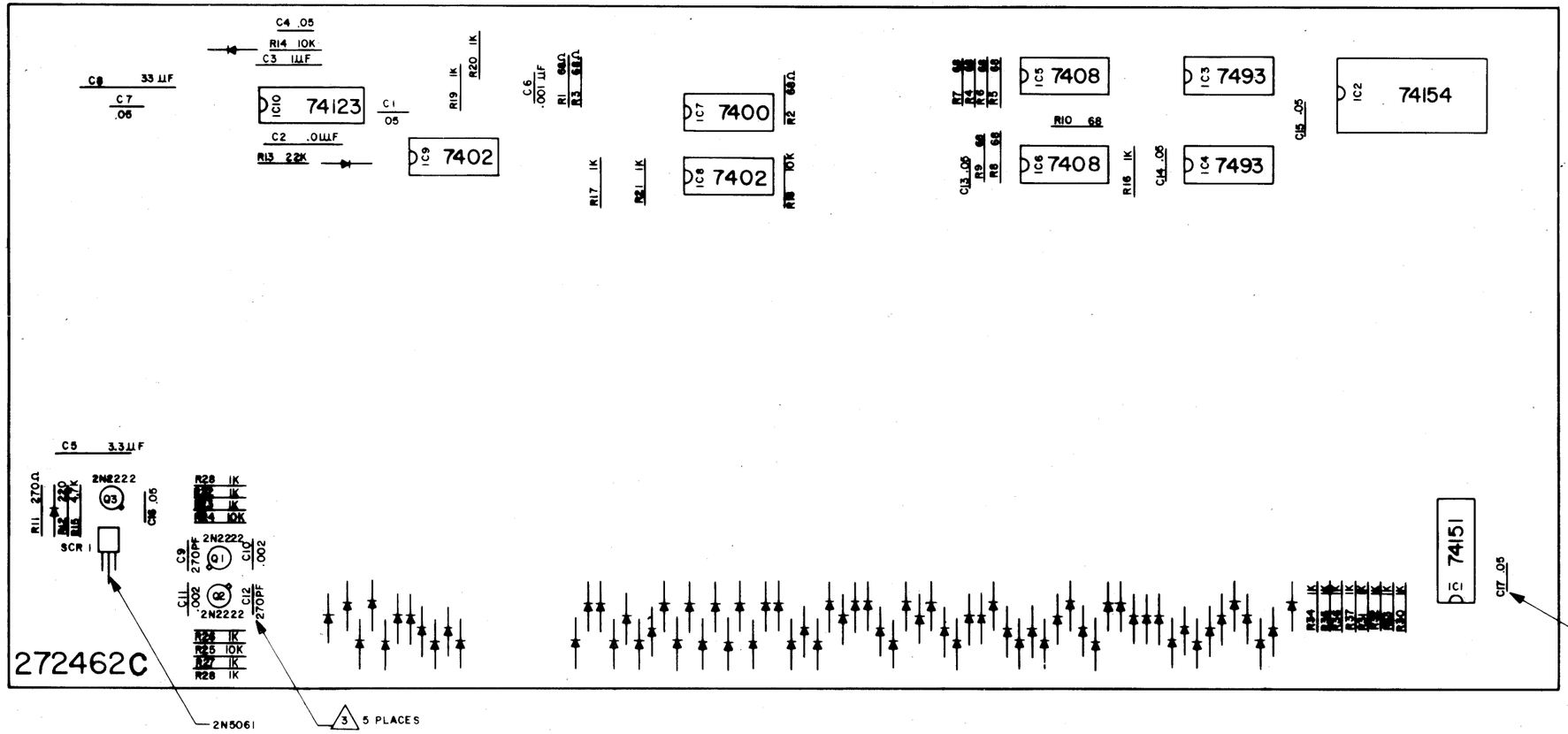
INTERDATA

933183

B	RELEASED	
C	MOVED BELL TO THIS SIDE ADJUST DCR D.M	
D	REV B REDRAWN	8220
E	REV PER DCN	8498

NOTES:

1. ALL RESISTORS AND DIODES ARE ON .400 CENTERS.
2. ALL DIODES ARE TEC-102.
3. COMPONENTS MUST BE INSTALLED SO THEY LAY FLAT ON PRINTED CIRCUIT BOARD.
4. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
5. SOLDER COMPONENTS TO CIRCUIT SIDE OF PCB PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
6. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.



PARTS LIST ISSUED

SHT 1 OF 1

933184	440 TTY	
NEXT ASSY	FIRST USED	
MATERIAL		
FINISH		

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
FRACTIONS
DECIMALS
ONE PLACE .0
TWO PLACE .00
THREE PLACE .000
ANGLES

REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

TITLE PCB ASSY — KEYBOARD EKA 9100

3-6-72	SIZE D	DRAWING NO 02-310	REV E
3-6-72			
3-16-72	2/1	SHEET 8	32

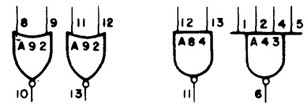
INTERDATA

990039

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED	—		
B	REV PER DCN	8223		
C	REV PER DCN	8264		
D	NO CHG SEE DCN	8448		

NOTES
1 UNLESS OTHERWISE SPECIFED, ALL RESISTORS ARE 1/4W, 5%
2 LAST REFERENCE DESIGNATION USED R2, C19, Y1, T119, T232, T314

UNUSED ELEMENTS



CHIP TYPE	LOCATIONS
7400	A64, 71, 74, 84, 94
7402	A92,
7404	A52
7410	A51
7420	A42, 43, 80
7430	A41
7474	A51, 53, 73, 81, 82, 83, 91, A93, 103
74177	A40, 50, 53, 54, 60, 62, 70, A72
74H04	A102
74H74	A104

PG	NAME	PIN		NAME	PG
1	+5V	1	2	+5V	1
	−5V	3	4	−10V	
	+15V	5	6	−15V	
		7	8		
		9	10		
		11	12		
		13	14		
		15	16		
		17	18		
		19	20		
		21	22		
		23	24		
		25	26		
		27	28		
		29	30		
		31	32		
		33	34		
		35	36		
		37	38	LMLOAD	
3	50HZ	39	40		
		41	42		
		43	44		
		45	46		
		47	48		
3	RPT 1	49	50	RPT 2	3
1	SCCT 1	51	52	SCCT 2	1
1	SCCT 3	53	54	SCCT 4	1
		55	56		
		57	58	PUCLR	
1	ENAB72	59	60	ENAB80	1
2	DOT A	61	62	DOT B	2
2	DOT C	63	64	DOT D	2
2	DOT E	65	66	DOT F	2
1	SCAN A	67	68	SCAN B	1
1	SCAN X	69	70	ROWEN	1
2	DOT 1	71	72	DOT 2	2
2	DOT 3	73	74	DOT 4	2
2	DOT 5	75	76	DOT 6	2
2	DOT 7	77	78	DCRST	2
3	ESYNC	79	80	72−80	1
3	HYSNC	81	82	VSYNC	3
2	24MHZ	83	84	12MHZ	2
	GND	85	86	GND	

SHT 1 OF 3

BD. 1

TITLE
SCHEMATIC—
TIMING GENERATOR

SIZE D | DRAWING NO. 02-310 | REV D

SCALE NONE | 9 32

INTERDATA

99039

A	RELEASED	—
B	REV PER DCN	8223
C	REV PER DCN	8264
D	NO CHG SEE DCN	8448

COMPONENT NOT REQUIRED

Y1 23.9616 MHZ

C19 33PF

R1 180Ω

R2 270Ω

C10 10 PF

C16 100 PF

COMPONENTS NOT REQUIRED.

+5V

HSYNC 1, 3

A102 T200 · A102 T201 · A102 T202 · A102 T203 · A104 T204 · A104 T205 · A102 T206 · A103 T207 · A94 T208 · A103 T209

A63 T210 · A73 T211 · A73 T212 · A83 T213 · A93 T214 · A93 T215 · A83 T216

A61 T217 · A52 T218 · A64 T219 · A64 T220 · A74 T221 · A74 T222 · A74 T223 · A74 T224 · A61 T225 · A84 T226 · A84 T227 · A94 T228 · A94 T229 · A94 T230 · A94 T231 · A92 T232

DOT A · DOT B · DOT C · DOT D · DOT D · DOT E · DOT E · DOT F · DOT 1 · DOT 2 · DOT 2 · DOT 3 · DOT 4 · DOT 5 · DOT 6 · DOT 7

DCRST · 24 MHZ · 12 MHZ

PI-61 · PI-62 · PI-63 · PI-64 · PI-65 · PI-66 · PI-71 · PI-72 · PI-73 · PI-74 · PI-75 · PI-76 · PI-77 · PI-78 · PI-83 · PI-84

SHT 2 OF 3 BD-1

SCHEMATIC— TIMING GENERATOR

D 02-310 D

NONE 10 OF 32

INTERDATA

990039

A	RELEASED	—		
B	REV PER DCN	8223		
C	REV PER DCN	8264		
D	NO CHG SEE DCN	8448		

A102

PI-39

50HZ

60 HZ — 50 HZ — +5V

50/60 HZ OPTION SWITCH

DOT E

DOT D

+5V

A70 T300 — A60 T301 — A50 T302 — A40 T303 — A54 T308

A80 T304 — A80 T305 — A71 T306 — A41 T307

A91 T309 — A91 T310 — A81 T311 — A81 T312 — A71 T313 — A71 T314

RPT 1 → PI-49

RPT 2 → PI-50

ESYNC 1 → PI-79

HSYNC 1,2 → PI-81

VSYNC → PI-82

LDEJVS 1

SHT 3 OF 3 BD-1

		DO NOT SCALE DRAWING
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS ONE PLACE ± TWO PLACE ± THREE PLACE ± ANGLES ±
	(272388)	
933037	440	
NEXT ASS'Y	FIRST USED	
MATERIAL		REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS
FINISH		

TITLE: SCHEMATIC — TIMING GENERATOR

SIZE	DRAWING NO	REV
D	02-310	D
SCALE	NONE	SHEET 11 OF 32

INTERDATA

933037

A	RELEASED	
B	REV PER DCN	8223
C	REV PER DCN	8264
D	REV PER DCN	8448

933037 [redacted] TIMING GEN TTY SN [redacted]

COMPONENTS NOT ADDED AT TIME OF ASSEMBLY

888

2723

		7420	74177	74177	74177	74177
		7474	7474	7400	7410	7474	7430
C3 15 µF	74H04	7402	7474	74177	74177	7404	7420
	7474	7474	7474	7474	7474	74177	7420
C2 15 µF	74H74	7400	7400	7400	7400	74177	

NOTES:

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL
4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD
5. CEMENT CRYSTAL TO BOARD USING S-254 RESIWELD
6. POSITION SWITCH AS SHOWN TO SELECT 60 HZ.

PARTS LIST ISSUED

SHT 1 OF 1

PC B ASSY – TIMING GENERATOR TTY

D 02-310 D

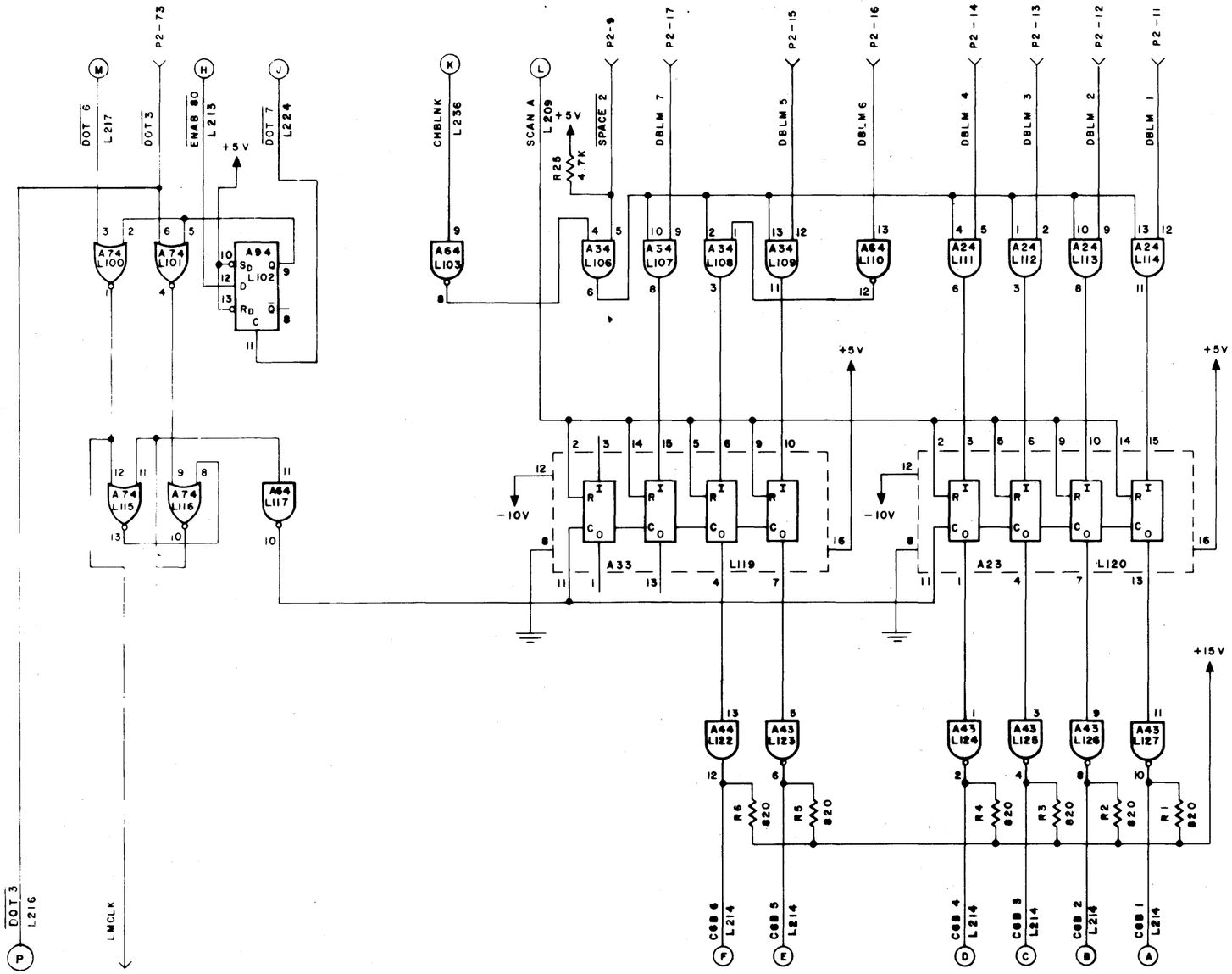
12 32

INTERDATA

990041

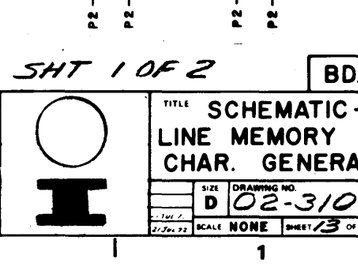
A	RELEASED	—	
B	REV PER DCN	8222	
C	REV PER DCN	8254	
D	REV PER DCN	8496	

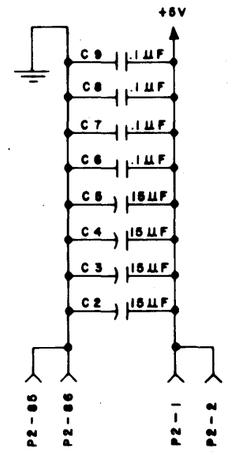
NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W, 5%.
2. LAST REFERENCE DESIGNATION USED: C9, R27, Q1, LI27, L238



	+5V	1	2	+5V	
	−5V	3	4	−10V	
	+15V	5	6	−15V	
		7	8		
1	SPACE 2	9	10	INHDSP	2
1	DBLM 1	11	12	DBLM 2	1
1	DBLM 3	13	14	DBLM 4	1
1	DBLM 5	15	16	DBLM 6	1
1	DBLM 7	17	18	CHDET	2
		19	20		
		21	22	CVIDEO	2
2	HDRIVE	23	24	SGND	
	SGND	25	26	NVIDEO	2
2	VDRIVE	27	28	SGND	
	SGND	29	30	LMCLK	1
		31	32		
		33	34		
		35	36		
		37	38	LMLOAD	
		39	40		
	CA−1	41	42		
	CA+1	43	44	DECPRA	
	LFCOL	45	46	ST2448	
	OPRSEL	47	48	SETLMC	
	RPT 1	49	50	RPT 2	2
	SCCT 1	51	52	SCCT 2	
	SCCT 3	53	54	SCCT 4	
		55	56		
		57	58	PUCLR	
2	ENAB 72	59	60	ENAB 80	2
	DOT A	61	62	DOT B	
	DOT C	63	64	DOT D	
	DOT E	65	66	DOT F	
2	SCAN A	67	68	SCAN B	2
2	SCAN X	69	70	ROWEN	2
	DOT 1	71	72	DOT 2	1
1	DOT 3	73	74	DOT 4	
	DOT 5	75	76	DOT 6	
2	DOT 7	77	78	DCRST	
	ESYNC	79	80	72−80	2
2	HSYNC	81	82	VSYNC	2
		83	84	12 MHZ	2
	GND	85	86	GND	
PG	NAME	PIN		NAME	PG

UNUSED ELEMENTS





CHIP TYPE	LOCATION
7400	A93, 102, 84
7402	A74, 103
7404	A64
7406	A43
7407	A44
7408	A24, 34, 83, 73
7410	A92
7474	A82, 83, 94
7486	A72
74H04	A54
MK1007	A23, 33
MK2102	A42

SHT 1 OF 2

BD. 2

	(272392)
933061 NEXT ASSY	440 FIRST USED
MATERIAL	
FINISH	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS
DECIMALS
ONE PLACE
TWO PLACE
THREE PLACE
ANGLES
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

TITLE SCHEMATIC — LINE MEMORY & CHAR. GENERATOR

SIZE D | DRAWING NO. 02-310 | REV D

SCALE NONE | SHEET 13 OF 32

INTERDATA

990041

A	RELEASED	
B	REV PER DCN	8222
C	REV PER DCN	8254
D	REV PER DCN	84960

*(2) CAPACITORS: SELECTED FOR CABLE MATCHING (LONG COAX RUNS – USERS OPTION.)

93306	440	(272392)
NEXT ASS'Y	FIRST USED	
MATERIAL		
FINISH		

DO NOT SCALE DRAWING

SHT 2 OF 2

BD-2

TITLE SCHEMATIC — LINE MEMORY & CHAR. GENERATOR

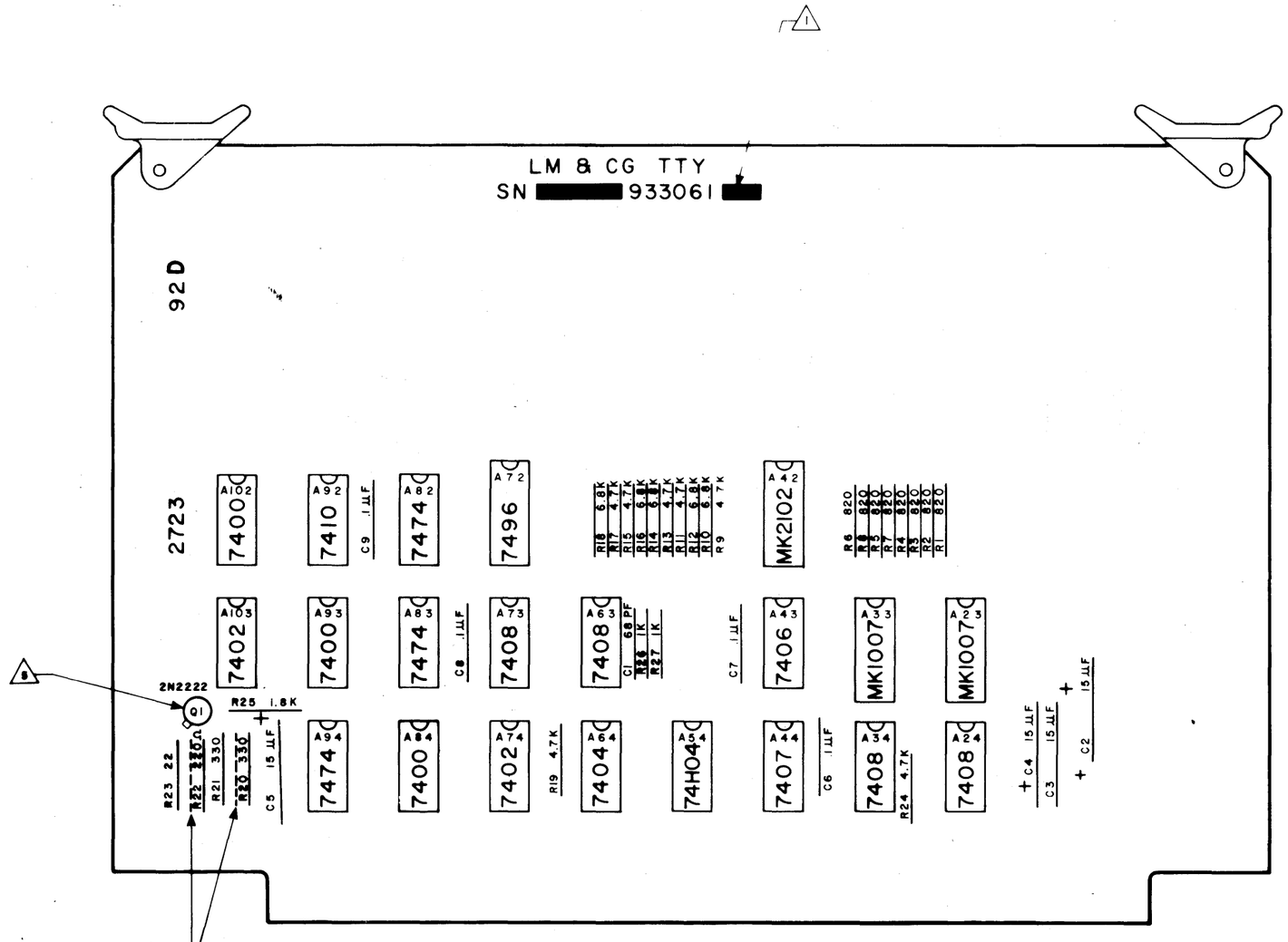
D 02-310 D

NONE 14 OF 32

INTERDATA

933061

B	REV & REDRAWN	8222		
C	REV PER DCN	8254		
D	REV PER DCN	8496		



NOTES:

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
5. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

PARTS LIST ISSUED

SHT 1 OF 1

NEXT ASSY	FIRST USE		

TITLE P.C.B. ASSY—
LINE MEM & CHAR GEN—TTY

DRAWING NO. 02-310 REV. D

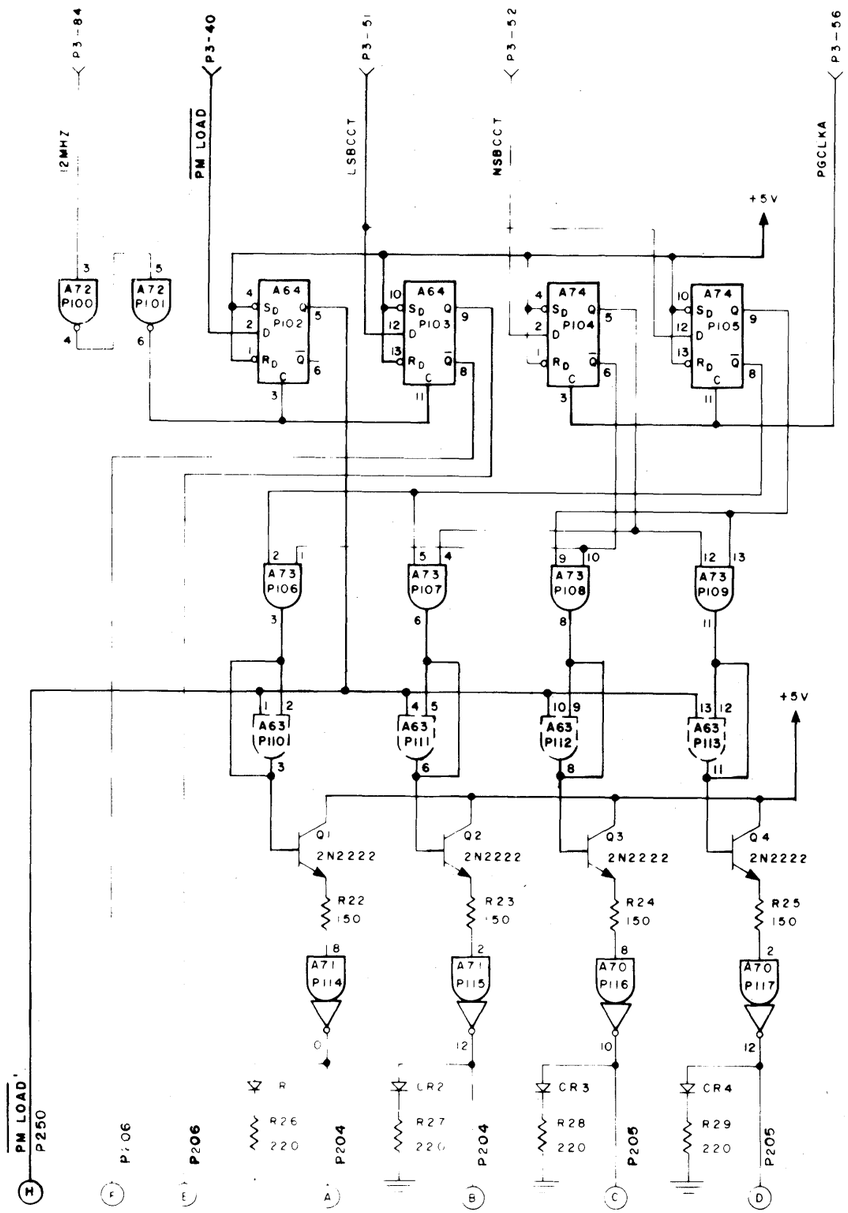
SIZE D | 2/1 | SHEET 15 OF 32

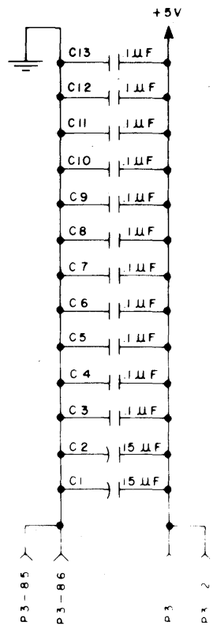
INTERDATA

990042

A	RELEASED	
B	REV PER DCN	8224
C	NO CHG - SEE DCN	8414
D	REV PER DCN	8497

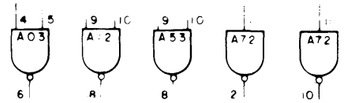
NOTES
UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE .4W 5%
2 LAST REFERENCE DESIGNATION USED C3, R29, Q4, CR4, P7, P249





	+5V	1	2	+5V	
	-5V	3	4	-10V	
	+15V	5	6	-15V	
2	SPACE 1	7	8	EXCSPG	
	SPACE 2	9	10	INHDSP	
2	DBLM 1	11	12	DBLM 2	2
2	DBLM 3	13	14	DBLM 4	2
2	DBLM 5	15	16	DBLM 6	2
2	DBLM 7	17	18	CHDET	
	CLRSCN	19	20	PGSTOP	
2	DBPM 1	21	22	DBPM 2	2
2	DBPM 3	23	24	DBPM 4	2
2	DBPM 5	25	26	DBPM 6	2
2	DBPM 7	27	28		
		29	30	LMCLK	
		31	32		
		33	34		
		35	36		
		37	38	LMLOAD	
		39	40	PMLOAD	1
	CA-1	41	42		
	CA+1	43	44	DECPRA	
	LFCOL	45	46	ST2448	
	OPRBEL	47	48	SETLMC	
		49	50		
1	LSBCCT	51	52	NSBCCT	1
		53	54		
		55	56	PGCLKA	1
		57	58	PUCLR	
		59	60	ENAB80	
	DOT A	61	62	DOT B	
	DOT C	63	64	DOT D	
	DOT E	65	66	DOT F	
	SCAN A	67	68	SCAN B	
	SCAN X	69	70	ROWEN	
	DOT 1	71	72	DOT 2	
	DOT 3	73	74	DOT 4	
	DOT 5	75	76	DOT 6	
	DOT 7	77	78	DCRST	
	ESYNC	79	80	72-80	
	HSYNC	81	82	VSYNC	
		83	84	12 MHZ	1
	GND	85	86	GND	
PG	NAME	PIN		NAME	PG

UNUSED ELEMENTS



CHIP TYPE	LOCATION
7400	A03, 13, 23, 43, 53
7408	A73
7451	A02, 22, 42, (A62)
74H00	A12, 52
74H04	A72
74H74	A64, 74
0009	A70, 71
1404	A00, 01, 10, 11, 20, 21, 30, 31, A40, 41, 50, 51, (A60, 61)

933062 (272393) 440

SHT 101 BD. 3

SCHEMATIC — PAGE MEMORY

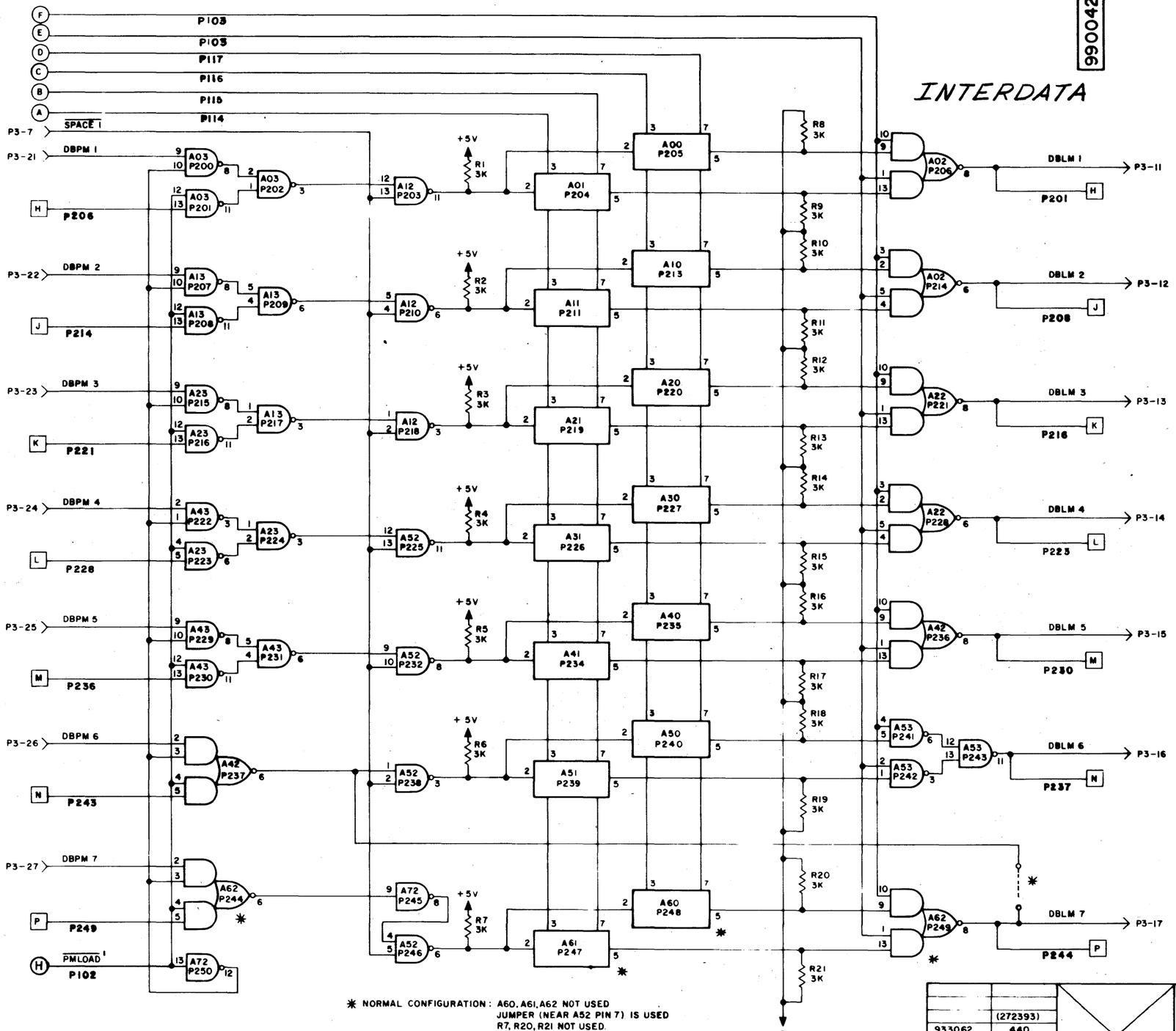
D 02-310 D

NONE 16 OF 32

990042

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED	—		
B	REV PER DCN	8224		
C	NO CHG — SEE DCN	8414		
D	REV PER DCN	8497		

INTERDATA



* NORMAL CONFIGURATION: A60, A61, A62 NOT USED
JUMPER (NEAR A52 PIN 7) IS USED
R7, R20, R21 NOT USED.

SHT 2 OF 2

BD-3

	(272393)
933062	440
NEXT ASSY	USED

TITLE SCHEMATIC - PAGE MEMORY

SIZE D | DRAWING NO 02-310 | REV D

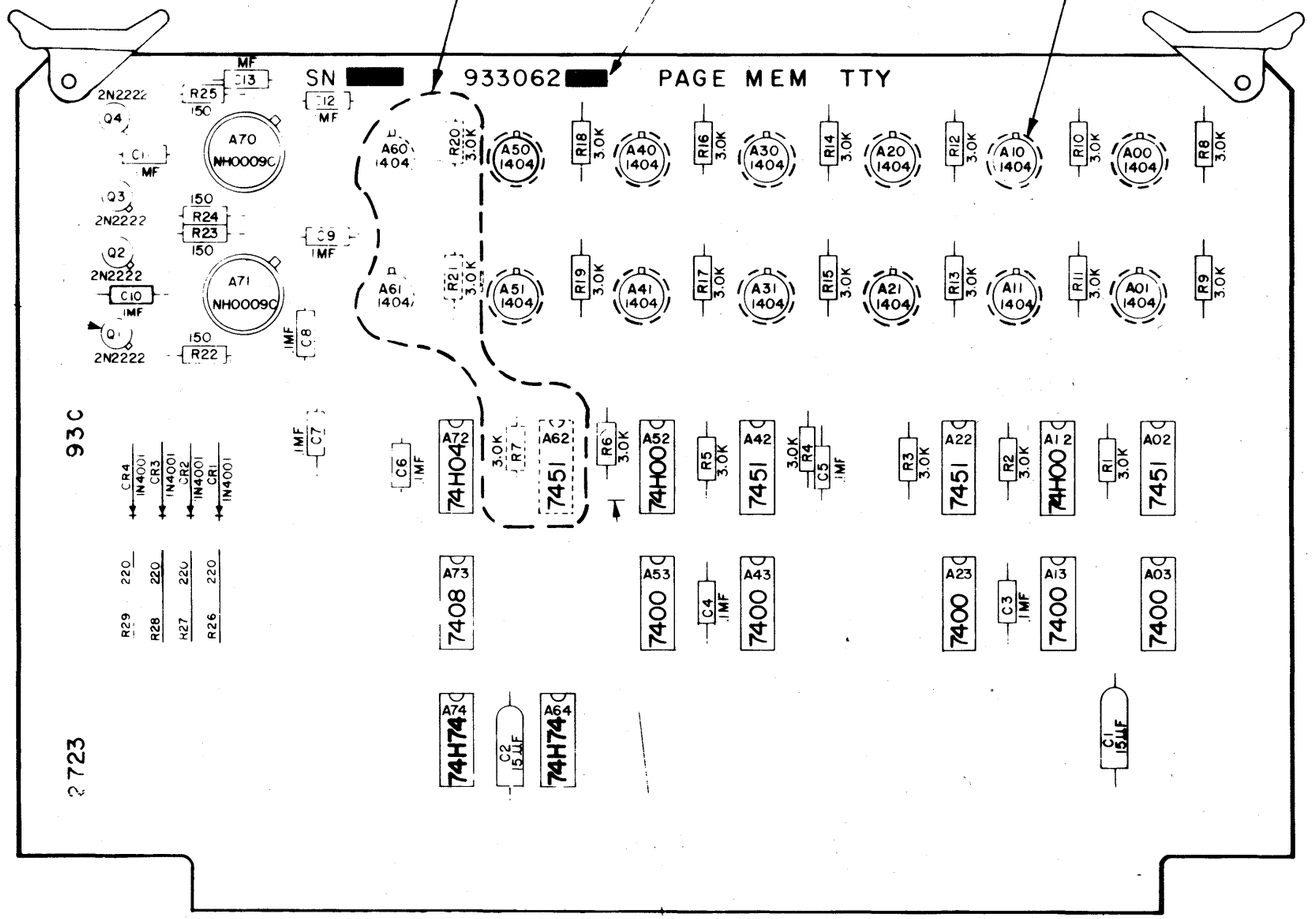
SCALE | SHEET 17 OF 32

INTERDATA

933062

A	RELEASED	
B	REV PER DCN	8224
C	REV PER DCN	8418
D	REV PER DCN	8497

COMPONENTS A60, A61, A62, R7, R20 & R21 ARE NOT USED FOR NORMAL CONFIGURATION.



NORMAL CONFIGURATION: JUMPER INSTALLED.

NOTES

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL
4. .050 MAX [illegible] LEAD PROJECTION ON CIRCUIT SIDE OF BOARD
5. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.
6. HEAT SINK 740025 TO BE INSTALLED ON ALL 1404 UNITS. (12)

PARTS LIST ISSUED

SHT 1 OF 1

TITLE P.W. ASSY- PAGE MEMORY TTY			
3-12-71	SIZE D	DRAWING NO 02-310	REV D
	SCALE 2/1	18 x 32	

INTERDATA

990043

REV	DESCRIPTION	NO.	APPD	DATE
A	RELEASED PROTO LAYOUT			
B	REVISED PER DCN	8225		
C	REV PER DCN	8253		
D	B/M CHG ONLY	8413	[illegible]	[illegible]

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, 10%.
2. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE TEC 102
3. LAST REFERENCE DESIGNATIONS USED: C10, R5, C140, C242, C338

	+5V	1	2	+5V	
	−5V	3	4	−10V	
	+15V	5	6	−15V	
	SPACE 1	7	8	EXCSPG	2
	SPACE 2	9	10	NMOSP	
		11	12		
		13	14		
		15	16		
		17	18	CHDET	2
	CLRSCN	19	20	POSTOP	1
	DBPM 1	21	22	DBPM 2	
	DBPM 3	23	24	DBPM 4	
	DBPM 5	25	26	DBPM 6	
	DBPM 7	27	28		
		29	30	LMCLK	3
		31	32		
		33	34		
		35	36		
		37	38	LMLOAD	
1	50HZ	39	40	PMLOAD	
3	CA−1	41	42		
3	CA+1	43	44	DECPRA	2
3	LFCOL	45	46	ST2448	1
3	OPRBEL	47	48	STLMC	3
3	CRSOVR	49	50		
2	LSBCCT	51	52	NSBCCT	2
		53	54		
		55	56	PGCLKA	3
		57	58	PUCLR	
		59	60	ENABCO	
	DOT A	61	62	DOT B	1
	DOT C	63	64	DOT D	
1	DOT E	65	66	DOT F	
1	SCAN A	67	68	SCAN B	3
3	SCAN X	69	70	ROWEN	1
	DOT 1	71	72	DOT 2	
	DOT 3	73	74	DOT 4	
	DOT 5	75	76	DOT 6	
	DOT 7	77	78	DCRST	3
3	ESYNC	79	80	72-80	3
	HSYNC	81	82	VSYNC	1
		83	84	12 MHZ	1
	GND	85	86	GND	
PG	NAME	PIN		NAME	PG

A94 A94 A94 A51

UNUSED ELEMENTS

A41 A13 A11 A73

CHIP TYPE	LOCATION
7400	A41, A53, A63, A82
7402	A10, A51, A84
7404	A11, A42, A54
7408	A81, A83, A94
7420	A12, A32
7430	A50
7453	A60
7474	A21, A61, A71, A72, A93
7486	A23, A30, A40, A60
74123	A14
74177	A31
74193	A20, A22, A33, A52, A62
74H00	A34, A43, A70, A74
74H04	A13, A73
74H74	A24, A44

+5V
C7 .1 µF
C6 .1 µF
C5 .1 µF
C4 .1 µF
C3 .1 µF
C2 15 µF
C1 15 µF
P4-86 P4-85 P4-2 P4-1

SHT 1 OF 3

BD.4

	(272394)
933063	440
NEXT ASSY	FIRST USED
MATERIAL	
FINISH	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS ±
DECIMALS
ONE PLACE ±.1
TWO PLACE ±.01
THREE PLACE ±.001
ANGLES ±
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

TITLE: SCHEMATIC – PAGE CONTROL

SIZE D | DRAWING NO 02-310 | D

SCALE — | SHEET 19 OF 32

INTERDATA

990043

A	RELEASED, PROTO LAYOUT	
B	REVISED PER DCN	8225
C	REV PER DCN	8253
D	B/M CHG ONLY	8213

DFCPRA P4-44

12 MHZ

+5V

R1 10K

R2 10K

A14 C200

A14 C201

A93 C242

A40 C205

A40 C206

A40 C207

A40 C208

A44 C203

A24 C204

A34 C209

A34 C210

A34 C211

A20 C212

A12 C213

A10 C214

A10 C215

A50 C216

A33 C222

A73 C217

A70 C218

A34 C219

A53 C220

A63 C221

A22 C223

A24 C224

A13 C225

A60 C226

A60 C227

A60 C228

A42 C229

A23 C230

A23 C231

A42 C232

A32 C233

A70 C234

A10 C235

A11 C236

A32 C237

A73 C238

A41 C239

A13 C240

A13 C241

PGCLKA

LSBCCT

NSBCCT

P4-51

P4-52

CHDET

P4-18

ERCH48

EXCSPG

CHZERO

P4-8

SHT 2 OF 3

BD.4

SCHEMATIC - PAGE CONTROL

D 02-310 D

20 OF 32

933063

(272394)

440

INTERDATA

990043

A	RELEASED, PROTO LAYOUT	
B	REVISED PER DCN	8225
C	REV PER DCN	8253
D	B/M CHG ONLY	8413

P4 8C
A54 C300
A54 C309
A53 C310
A54 C311
A53 C315
A53 C316
A63 C325
A63 C326
R4 68
C10 470
CRSOVR
OPRBEI
P4 49
P4 47

LFCOL P4 45
CA- P4-41
CA+ P4 43
ESYNC P4 39
A42 C301
A42 C302
A41 C312
R5 4.7K
+5V
A51 C303
A54 C318
R3 47K
A52 C317
A62 C327
A61 C304
A61 C319
A63 C320
A73 C332
A84 C333
P4-56
PGCLKA
A B C D E F G

NMCLK H
MCLK P4 33
SCAN B P4 68
SCAN A P4 69
ST WC P4 48
DCRST P4-78
12 MHZB V
A84 C305
A84 C306
A54 C308
A93 C338
A84 C313
A84 C314
A83 C321
A83 C322
A83 C323
A83 C324
A82 C328
A82 C329
A82 C330
A82 C331
A81 C334
A81 C335
A81 C336
A80 C337

SHT 3 OF 3 BD. 4

933063 (272394) 440

SCHEMATIC - PAGE CONTROL

D 02-310 D

21 OF 32

INTERDATA

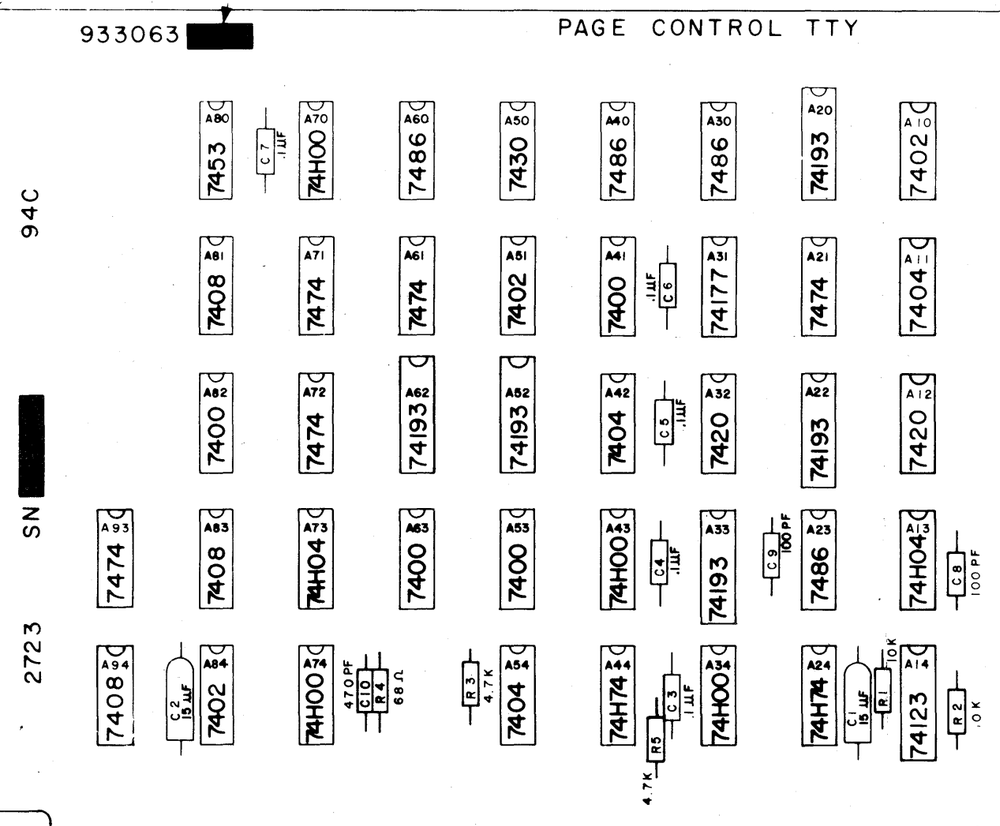
933063

A	RELEASED			
B	REV PER DCN	8225		
C	REV PER DCN	8253		
D	B/M CHG ONLY	8413		

933063 ■ PAGE CONTROL TTY

94C

2723 SN ■



NOTES

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
4. 050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD

PARTS LIST ISSUED

SHT 1 OF 1

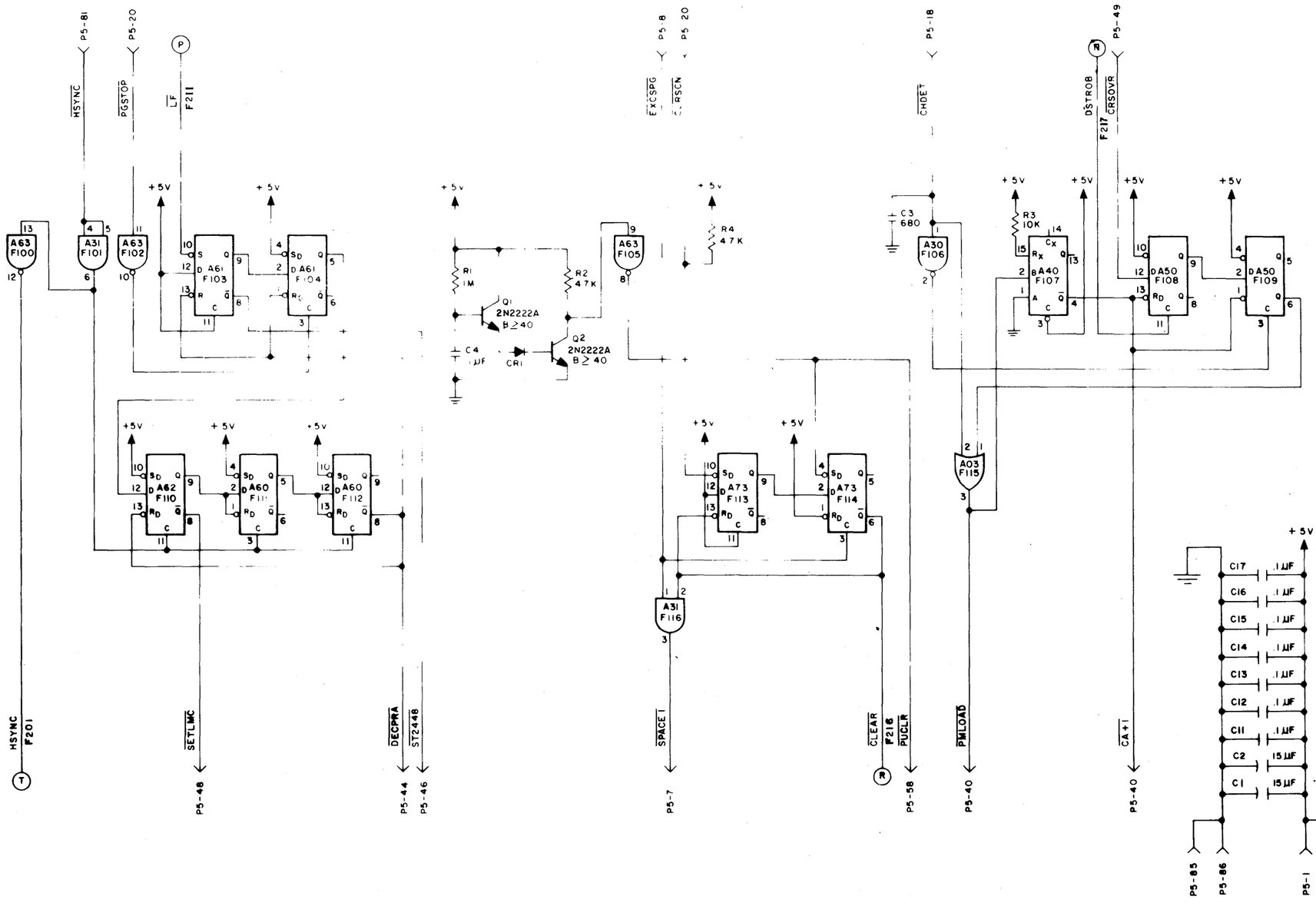
TITLE	P.C.B. ASSY– PAGE CONTROL TTY		
4-28-71	SIZE D	DRAWING NO 02-310	REV D
DRAWN	SCALE 2/1	SHEET 22 OF 32	

INTERDATA

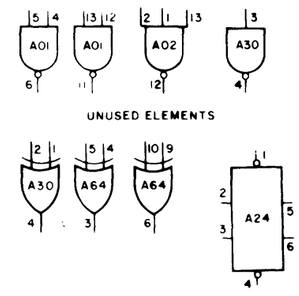
T-990044

B	REVISED, REDRAWN	8227	
C	B/M CHG ONLY	8405	
D	REV PER DCN	8495	
E	REV PER DCN	8534	

NOTES
1 UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4W, 10%
2 LAST REFERENCE DESIGNATION USED: C18, R29, CR1, Q2, S3, Y1, F116, F217, F339, F436
3 UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE TEC 102



PG	NAME	PIN	NAME	PG
	+5V	1 2	+5V	
	-5V	3 4	-10V	
	+15V	5 6	-15V	
1	SPACE I	7 8	EXCSPG	1
		9 10		
4	TWOMHZ	11 12	LOC-REM	4
4	FRCFDP	13 14	FRCTTY	4
3	TENBIT	15 16	SLSPDX	4
		17 18	CHDET	1
1	CLRSCN	19 20	PGSTOP	1
2	DBPM 1	21 22	DBPM 2	2
2	DBPM 3	23 24	DBPM 4	2
2	DBPM 5	25 26	DBPM 6	2
2	DBPM	27 28		
		29 30		
		31 32		
		33 34		
		35 36		
		37 38		
		39 40	PMLOAD	1
2	CA-1	41 42		
1	CA+1	43 44	DECPRA	1
2	LFCOL	45 46	ST2448	1
2	OPRBEL	47 48	SETLMC	1
1	CRSOVR	49 50		
		51 52		
2	RSDATA	53 54		
		55 56		
2	BELL	57 58	PUCLR	1
		59 60	ENAB80	
	DOT A	61 62	DOT B	
	DOT C	63 64	DOT D	
	DOT E	65 66	DOT F	
	SCAN A	67 68	SCAN B	
	SCAN X	69 70	ROWEN	
	DOT 1	71 72	DOT 2	
	DOT 3	73 74	DOT 4	
	DOT 5	75 76	DOT 6	
	DOT 7	77 78	DCRST	
	ESYNC	79 80	72-80	
	HSYNC	81 82	VSYNC	
		83 84		
	GND	85 86	GND	



CHIP TYPE	LOCATION
7400	A01, A04, A13, A41, A71, A93
7404	A30, A63, A101
7408	A00, A31, A82, A81
7410	A02, A72, A102
7430	A10, A14, A32, A42, A43, A44
7432	A03, A11, A12
7474	A24, A50, A51, A60, A61, A62, A73, A91, A92
7475	A33, A34
7486	A64
7495	A53, A54
74123	A40
74177	A70, A82, A83, A100, A103, A104
74193	A22, A23

SHT 1 OF 4

BD.5

933067 (272741) 440

SCHEMATIC - FUNCTION CONTROL

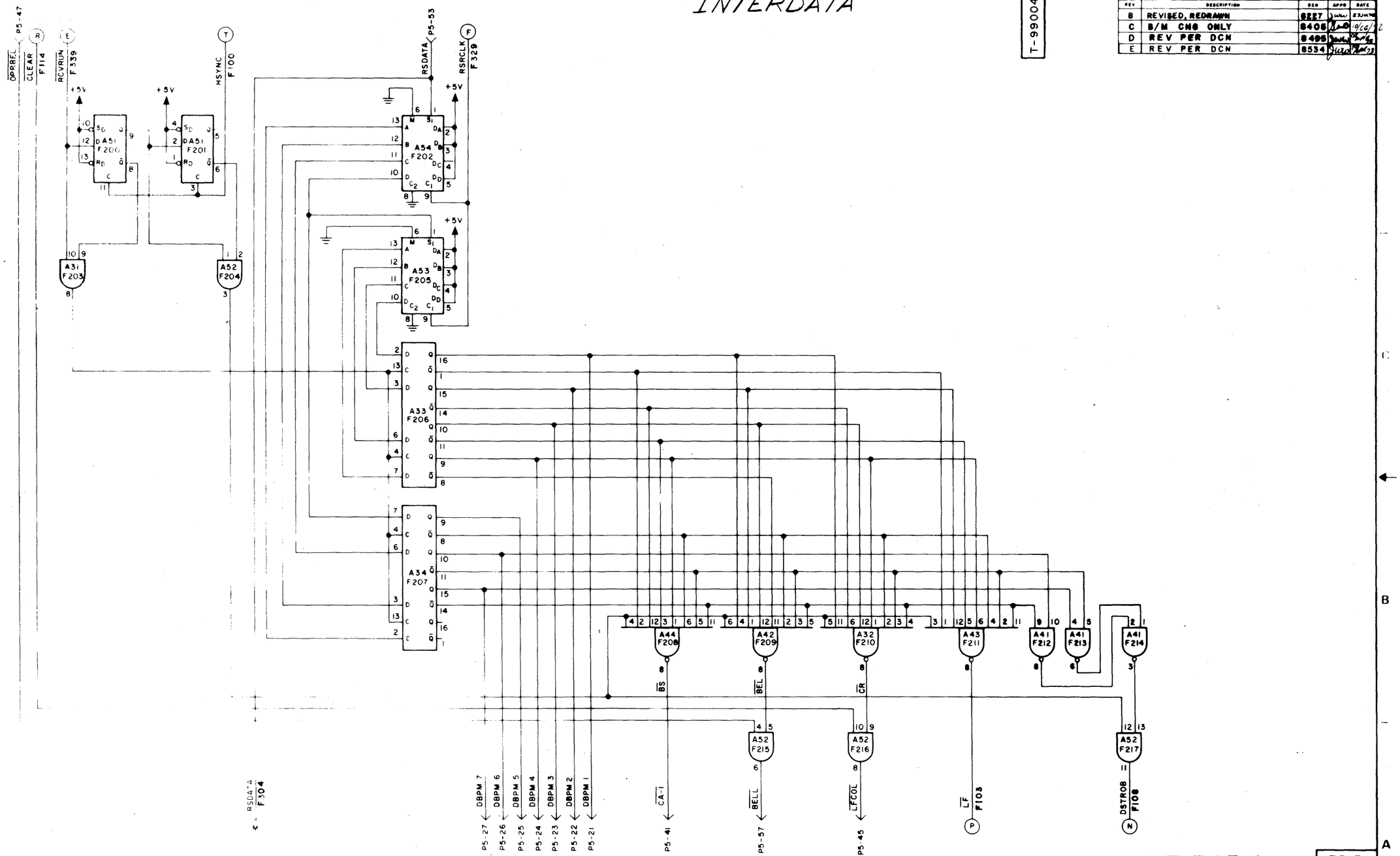
D 02-310 E

23 OF 32

INTERDATA

T-990044

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
B	REVISED, REDRAWN	8227	WW	23JUN72
C	B/M CHG ONLY	8408	[illegible]	19Oct72
D	REV PER DCN	8498	[illegible]	[illegible]
E	REV PER DCN	8534	[illegible]	[illegible]



SHT 2 OF 4

BD.5

	(272741)	
933067	440	

TITLE: SCHEMATIC — FUNCTION CONTROL

SIZE D | DRAWING NO. 02-310 | REV E

SCALE — | SHEET 24 OF 32

INTERDATA

T-990044

B	REVISED, REDRAWN	8227	
C	B/M CHG ONLY	8405	
D	REV PER DCN	8495	
E	REV PER DCN	8534	

D
C139 F419
C142 F406
C104 F417
A93 F300
A102 F301
A101 F302
A101 F303
+5V
A103 F309
A104 F310
A102 F317
A101 F318
A92 F311
A93 F319
A93 F320
A101 F321
A81 F322
A81 F329
A101 F330
A81 F331
A93 F332
A100 F334
A102 F337
A92 F339
RCV RUN
RSRCLK F202
F
A
RCVCLK F411
M
RSDATA F202
A71 F304
A91 F312
E
RCVRUN F200
TENBIT
P5-15
L
C139 F435
K
C142 F420
J
C104 F433
A41 F305
A72 F306
A63 F307
A63 F308
A83 F313
A82 F314
A72 F323
H
XMTCLK F428
A62 F315
A91 F316
A63 F324
A71 F325
A71 F326
A101 F327
A81 F328
P5-50
XRNRST
A71 F333
A03 F335
A70 F336
A72 F338
XRNSTP
P5-54
XSRCLK
P5-52
B
1
2
3

SHT 3 OF 4

BD.5

933067 (272741) 440

SCHEMATIC—
FUNCTION CONTROL

D 02-310 E

25 OF 32

INTERDATA

T-990044

B	REVISED, REDRAWN	8227	
C	B/M CHG ONLY	8405	
D	REV PER DCN	8495	
E	REV PER DCN	8534	

R5 270 R6 270 C5 10 C6 10 C18 4700 C7 100 C9 100 C8 33 Y1 8.000 MHZ

A30 F400 A30 F401 A30 F402 A30 F403

A23 F404 A22 F405

A00 F406 A12 F407 A12 F408 A12 F409 A12 F410 A13 F415 A03 F417 A13 F418

R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 (10) 4.7K

S2: 110 150 300 600 1200 1800 2400 4800 7200 9600

A01 F416 A02 F417 A00 F419

R18 4.7K

SEL TTY (UP) (DN) S1

R19 4.7K

A00 F420 A00 F422

R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 (10) 4.7K

S3: 110 150 300 600 1200 1800 2400 4800 7200 9600

A01 F431 A02 F433 A31 F435

A11 F421 A11 F423 A11 F424 A11 F425 A13 F429 A03 F432 A13 F434

A14 F411 A10 F426 A04 F436

A64 F412 A24 F413 A40 F414 R7 22K C10 .1μF

A04 F427 A04 F428 A04 F430

TWOMHZ → P5-11

RCVCLK F318 (A)

FRCFDP → P5-13

C104 F303 (B)

C142 F300 (C)

C139 F309 (D)

FRCTTY → P5-14

SLSPDX → P5-16

XMTCLK F315 (H)

C104 F308 (J)

C142 F305 (K)

C139 F305 (L)

SHT 4 OF 4

BD.5

SCHEMATIC— FUNCTION CONTROL

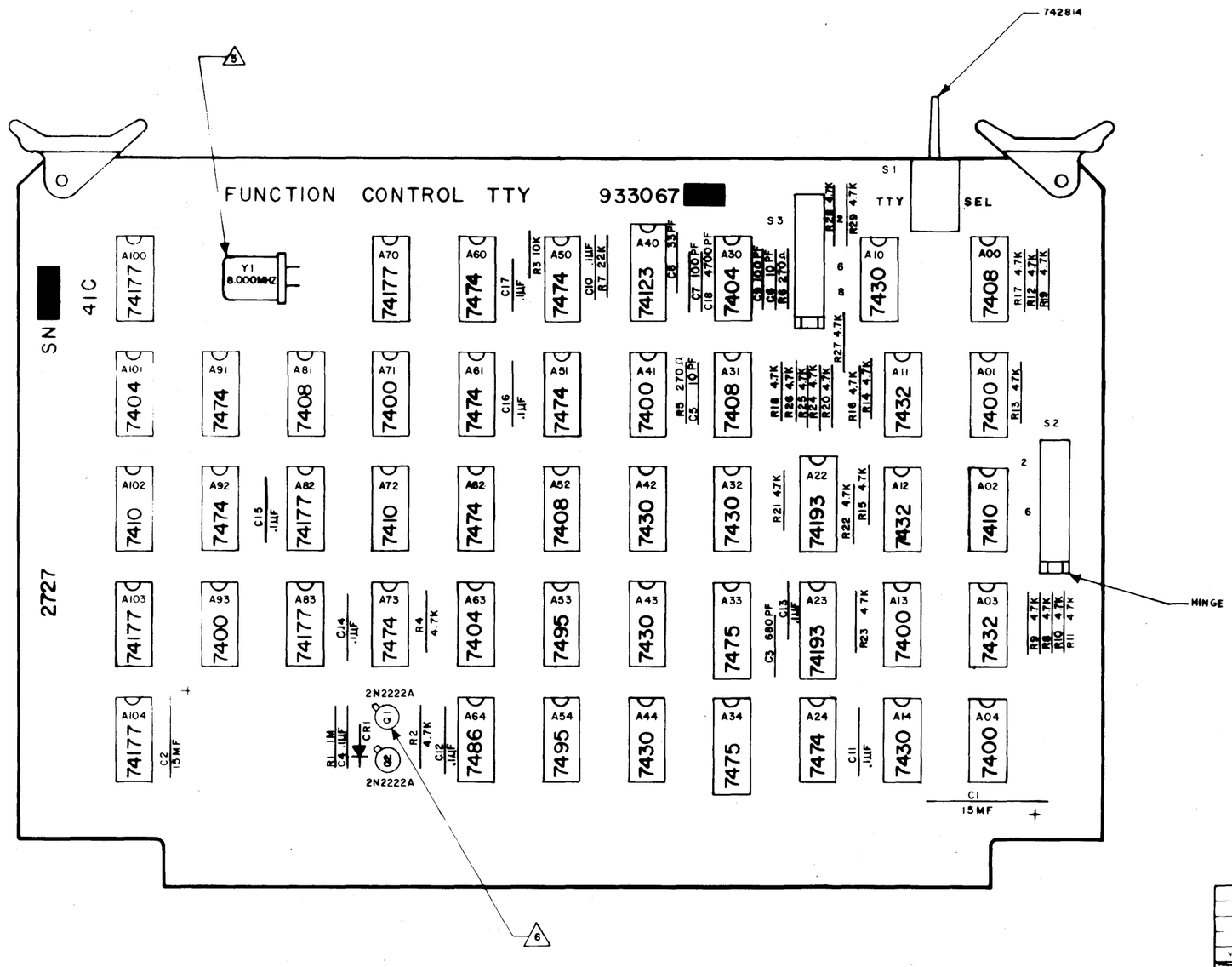
D 02-310 E

26 of 32

933067 (272741) 440

T-933067

REVISIONS				
REV.	DESCRIPTION	DCN	APPD	DATE
B	REV A REDRAWN	8227		6/30/72
C	B/M CHG ONLY	8405		7/24/72
D	REV PER DCN	8495		9/6/72
E	REV PER DCN	8534		9/27/72



NOTES:

⚠ APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.

2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.

⑤ CEMENT CRYSTAL TO BOARD USING S-254 RESIWELD.

⑥ ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

PARTS LIST ISSUED

SHT 1 OF 1

P.C.B. ASSY— FUNCTION CONTROL TTY

524-72 D 02-310 E

2/1 27 32

990045

INTERDATA

REV	DESCRIPTION	APPD
A	RELEASED, PROTO LAYOUT	
B	REVISED PER DCN	8226
C	REVISED PER DCN	8255
D	NO CHG – SEE DCN	8414

COMPONENT NOT LOADED

	+5V	1	2	+5V	
	-5 VDC	3	4	-10 VDC	
1	+15 VDC	5	6	-15 VDC	1
	SPACE 1	7	8	EXCSPG	
	SPACE 2	9	10	INHDSP	
3	TWOMHZ	11	12	LOC-REM	1
1	FRCFDP	13	14	FRCTTY	2
2	TENBIT	15	16	SLSPDX	3
		17	18	CHDET	
1	CLRSCN	19	20	POSTOP	
	DBPM 1	21	22	DBPM 2	
	DBPM 3	23	24	DBPM 4	
	DBPM 5	25	26	DBPM 6	
	DBPM 7	27	28		
		29	30		
		31	32		
		33	34		
		35	36		
		37	38		
		39	40	PMLOAD	
		41	42		
		43	44	DECPRA	
		45	46	ST2448	
		47	48	SETLMC	
2	CRSOVR	49	50	XRNRST	
		51	52	XSRCLK	2
1	RSDATA	53	54	XRNSTP	3
		55	56		
1	BELL	57	58	PUCLR	1
		59	60	ENABOO	
	DOT A	61	62	DOT B	
	DOT C	63	64	DOT D	
	DOT E	65	66	DOT F	
	SCAN A	67	68	SCAN B	
	SCAN X	69	70	ROWEN	
	DOT 1	71	72	DOT 2	
	DOT 3	73	74	DOT 4	
	DOT 5	75	76	DOT 6	
	DOT 7	77	78	DCRST	
	ESYNC	79	80	72-80	
3	HSYNC	81	82	VSYNC	
		83	84	12 MHZ	
	GND	85	86	GND	
PG	NAME	PIN	NAME	PG	

UNUSED ELEMENTS

CHIP TYPE	LOCATION
7400	A22, A23, A53, A54, A73, A81
7404	A32, A52, A71, A72, A101
7408	A21, A64, A74
7410	A84
7430	A102
7451	A91, A92
7453	A62
7474	A31, A33, A34, A42, A44, A82
7486	A63, A103
7496	A83, A93
74123	A24
75150	A50
75154	A41
MCT2	A80A, A80B

NOTES
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, 10%
2. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE TEC 102
3. LAST REFERENCE DESIGNATION USED C11, R34, CR10, DB2, Q4, S4, S115, S237, S338

SHT 1 OF 3

BD.6

E	CHG ON B/M ONLY	8490	
D1	NO CHG – SEE DCN	8425	

933068 (272742) 440

SCHEMATIC – TTY INTERFACE

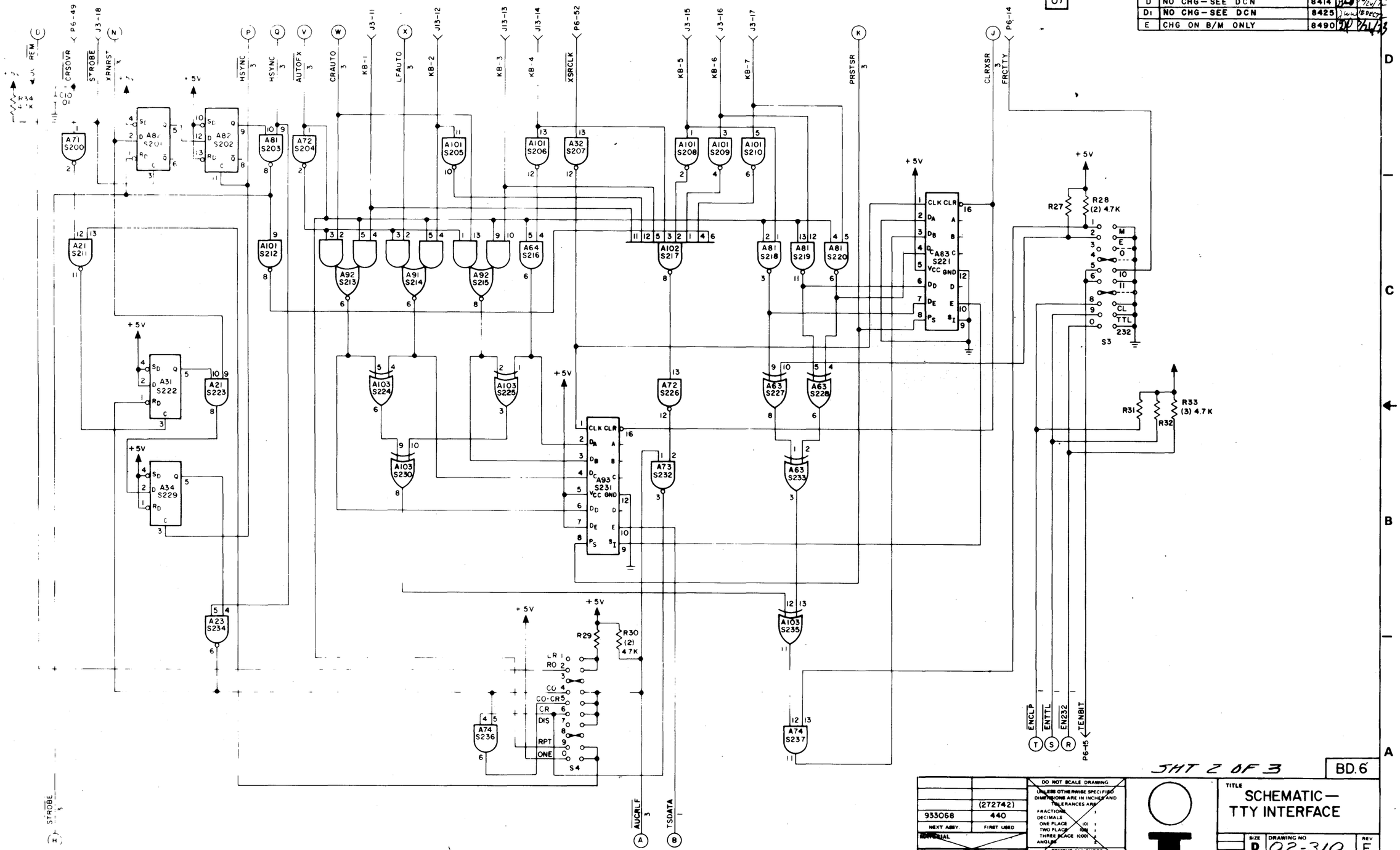
02-310 E

28 32

INTERDATA

990045

REVISIONS				
REV	DESCRIPTION	DCN	APP'D	DATE
A	RELEASED, PROTO LAYOUT			
B	REVISED PER DCN	8226		
C	REVISED PER DCN	8255		
D	NO CHG—SEE DCN	8414		
D1	NO CHG—SEE DCN	8425		
E	CHG ON B/M ONLY	8490		



SHT 2 OF 3

BD.6

		DO NOT SCALE DRAWING	TITLE: SCHEMATIC— TTY INTERFACE
	(272742)	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: FRACTIONAL ± DECIMALS ONE PLACE (01) ± TWO PLACE (00) ± THREE PLACE (000) ± ANGLES ±	
933068	440		SIZE D · DRAWING NO 02-310 · REV E
NEXT ASSY.	FIRST USED		SCALE —— · SHEET 29 OF 32
MATERIAL		REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS	
FINISH			

INTERDATA

990045

REV		
A	RELEASED, PROTO LAYOUT	
B	REVISED PER DCN	8226
C	REVISED PER DCN	8255
D	NO CHG - SEE DCN	8414
D1	NO CHG - SEE DCN	8428
E	CHG ON B/M ONLY	8490

HSYNC P6-81 · AUCRLF 2 · BREAK · PUCLR · XMMSTP P6-34 · TXRQSTZ P6-11 · STRQSTZ 2 · SLSPDX P6 16

A74 S300 · A74 S301 · A44 S304 · A31 S305 · A33 S306 · A33 S307 · A42 S308 · A32 S309 · A44 S310 · A34 S311 · A32 S312 · A64 S313 · A23 S314 · A42 S315 · A24 S316 · A24 S317 · A22 S327 · A64 S318 · A54 S319 · A53 S320 · A54 S321 · A53 S322 · A54 S323 · A21 S324 · A84 S325 · A22 S326 · A32 S328 · A84 S329 · A84 S330 · A54 S331 · A91 S332 · A52 S333 · A64 S334 · A21 S335 · A23 S336 · A22 S337 · A23 S338

+5V · R17 82K · C1 .15μF · CR7 · R18 12K

TXDATA · TRDATA · DTR · CXDATA · CRDATA · FGND · XDATA · RDATA · DSR · SGND · CXDATA · CRDATA

J1

SGND · PRTRSM · PRTPTL

J2

+5V · +5V · PGND · PGND · PGND · XMTACK · KB 1 · KB-2 · KB-3 · KB-4 · KB 5 · KB-6 · KB-7 · STROBE · CLRSCN · SGND · SGND · BELL · BREAK · SGND · SGND · SGND · SGND · SGND · SGND · SGND

J3

HSYNC 2 · HSYNC 2 · AUTOFX 2 · LFAUTO 2 · CRAUTO 2 · CLRSR 2 · XRNRST 2 · PRSTSR 2 · P6 50 XRNRST · XMTACK J3-6

SHT 3 OF 3

BD 6

	(272742)
933068	440
NEXT ASSY	FIRST USED
MATERIAL	
FINISH	

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:
FRACTIONS ±
DECIMALS
ONE PLACE (0) ±
TWO PLACE (00) ±
THREE PLACE (000) ±
ANGLES ±
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

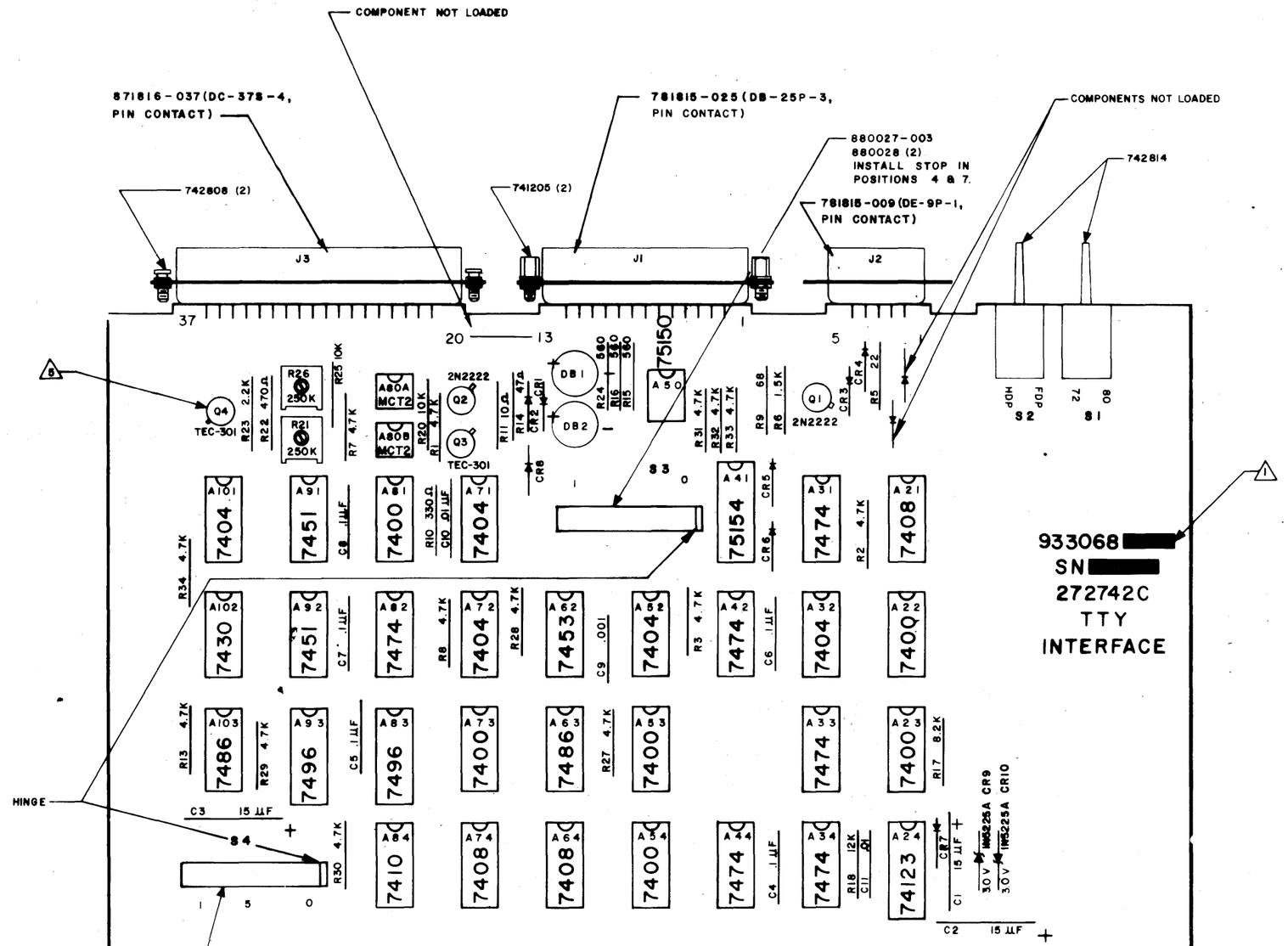
TITLE: SCHEMATIC — TTY INTERFACE

SIZE D · DRAWING NO. 02-310 · REV E · SHEET — 30 32

INTERDATA

933068

B	REV & REDRAWN	8225
C	REVISED PER DCN	8225
D	REV PER DCN	8414
D1	REV PER DCN	8425
E	CHG ON B/M ONLY	8490



NOTES:

1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
5. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

PARTS LIST ISSUED

SHT 1 OF 1

	(272742)
(990045)	440
NEXT ASSY	FIRST USED

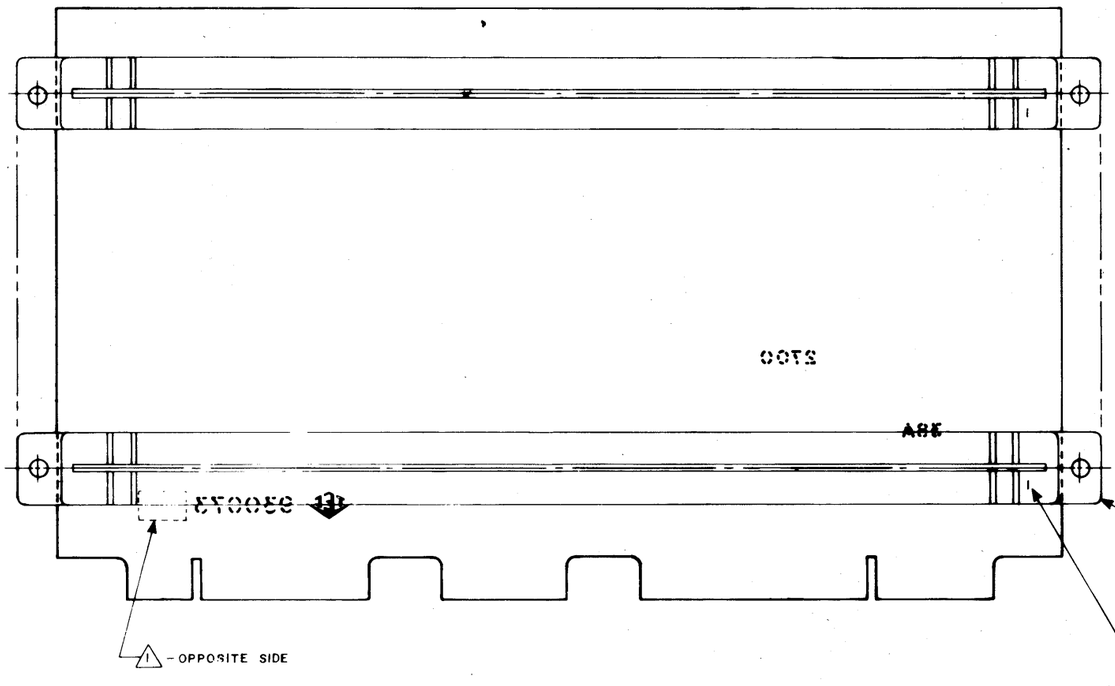
P.C.B. ASSY—
TTY INTERFACE

8-30-72 | DRAWING NO. D 02-310 E | SHEET 31 OF 32

INTERDATA

930073

REVISIONS				
REV	DESCRIPTION	INIT	APPD	DATE
A	RELEASED	—		



NOTES:
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
2. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.32 OF TEC WORKMANSHIP MANUAL.

SHT 1 OF 1

NEXT ASSY | FIRST USED

MATERIAL

FINISH

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCE ARE

FRACTIONS .
DECIMALS
ONE PLACE .0
TWO PLACE .00
THREE PLACE .000
ANGLES °

REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS

TITLE P.C.B. ASSY. MOTHERBOARD, 27-053 CRT

5-1-72	SIZE D	DRAWING NO. 02-310	REV A
5-1-72	SCALE 2/1	SHEET 32 OF 32	